High Power Inverter EMI characterization and Improvement Using Auxiliary Resonant Snubber Inverter

by

Yuqing Tang

Thesis submitted to the Faculty of the

Virginia Polytechnic Institute and State University

In partial fulfillment of the requirements for the degree of

Master of Science

in

Electrical Engineering

Approved by

Dr. Jason Lai, Chairman

Dr. Dan Y. Chen

Dr. Alex Q. Huang

December 17, 1998

Blacksburg, Virginia

Keywords: EMI, noise reduction, high power inverter, hard switching, soft switching

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(Abstract)

Electromagnetic interference (EMI) is a major concern in inverter motor drive systems. The sources of EMI have been commonly identified as high switching dv/dt and di/dt rates interacting with inverter parasitic components. The reduction of parasitic components relies on highly integrated circuit layout and packaging. This is the way to deal with noise path. On the other hand, switching dv/dt and di/dt can be potentially reduced by soft-switching techniques; thus the intensity of noise source is reduced.

In this paper, the relation between the dv/dt di/dt and the EMI generation are discussed. The EMI sources of a hard-switching single-phase PWM inverter are identified and measured with separation of common-mode and differential-mode noises. The noise reduction in an auxiliary resonant snubber inverter (RSI) is presented. The observation of voltage ringing and current ringing and the methods to suppress these ringing in the implementation of RSI are also discussed. The test condition and circuit layout are described as the basis of the study. And the experimental EMI spectra of both hard- and soft-switching inverter are compared. The effectiveness and limitation of the EMI reduction of the ZVT-RSI are also discussed and concluded.

The control interface circuit and gate driver design are described in the appendix. The implementation of variable charging time control of the resonant inductor current is also explained in the appendix.

Acknowledgement

I am greatly indebted and respectful to my advisor, Dr. Jason Lai, for his great support, guidance, and encouragement, not only to my research work, but also to my life; and for his diligence and generosity.

I'd like to express my heartfelt thanks to Dr. Dan Y. Chen and Dr. Alex Q. Huang, for the time and efforts they spent as my committee members.

I would like to pay my deep gratitude to Dr. Chingchi Chen of Ford Motor Company, for his help and direction in my research, and for his friendship.

I'd like to thank Dr. Fred C. Lee, without whose admission and recommendation, I could not have the opportunity to study in Virginia Power Electronics Center; and could not have Dr. Lai as my advisor.

I would like to thank our previous VPEC lab manger, Jeffery, who is so responsible for his duty, and is always eager to help others. I am also grateful for the help of VPEC other faculty and stuff.

I would like to appreciate Huibin Zhu, Byeong-Mun Song, Dengming Peng, Xiukuan Jing, Yuxin Li, Jianwen Shao, Changrong Liu, Huijie Yu, Ivana, Naveen, and other VPEC members, for the share of friendships and knowledge, and for the days and nights we passed together in VPEC.

Last but not least, I would like to thank my wife, Jianghong Wei, for her consistent love, support, encouragement, and self-sacrifice, for the life we experienced together, both in my good time and hard time.

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Chapter I

INTRODUCTION

1.1 EMI issues in high power inverter

Pulse-Width Modulation technique is widely used in variable-speed motor drives, especially after the high power rating, fast switching IGBT come up, which enables a higher switching frequency and thus better performance in dynamic response and reduction in the size, weight and acoustic noise of the system are achievable. However, as the Electromagnetic Compatibility (EMC) regulation becomes more stringent, Electromagnetic Interference (EMI) becomes a major concern for inverter driven motor drives, particularly when this kind of motor drives are used in electric vehicles. This is because the conducted and radiated EMI noise may cause malfunction of other electronic equipment of the electric vehicle.

Many researching works show that the switching dv/dt and di/dt are the EMI noise sources. The higher switching dv/dt and di/dt, the higher EMI emission. Since soft-switching techniques can significantly reduce the switching dv/dt and di/dt, it is conceivable that the EMI noise generated by a hard-switching inverter could be reduced by soft-switching techniques. Much effort of earlier work on the EMC performance of power electronic systems has tended to concentrate on switched mode power supply and may not be directly applicable to PWM motor drives, which is more complicated in terms of its power stage construction, external connections to the motor and supply, control circuit, and operation modes.

Some recent research focusing on the mechanism of EMI noise generation and propagation have been published. However, these efforts only concentrate on the hard-switching

inverter. The effect of soft switching upon EMI noise reduction is still not fully investigated. There are many questions remain unknown. For example, how much EMI noise will be generated by the auxiliary switches and components that are necessary to achieve soft switching? If the total EMI emission of the circuit is reduced, how much reduction can be achieved? These are the issues to be verified through experiments in this thesis.

The conducted EMI noise in a PWM inverter can be viewed as consisting of two parts, differential mode (DM) noise and common mode (CM) noise, which are illustrated in Fig. 1.1. The dv/dt at the midpoints of the three legs of the inverter are normally identified as CM noise source. The dv/dt caused by the switch turn on/turn off, coupled through the parasitic capacitance between the IGBT collector and the module base-plate that is normally grounded through the heat-sink, generate CM noise current. The CM noise current flows into the ground and through the stray capacitance inside the motor to the motor frame and back to the source via the power mains. The CM noise current also flows into the ground and through the stray capacitance inside the power supply and back to the noise source. The di/dt in the dc bus is normally identified as DM noise source. This change of current is also caused by the switching operation of the inverter. The DM noise current flows into power supply and back to the inverter. The DM current also flows through the motor phase windings, and through the stray capacitance inside the motor, and then back to the power mains via the dc bus and the rectifier. The stray capacitance between stator windings has been previously shown relatively small and negligible

1.2 EMI reduction by using soft switching

The EMI issue involves three aspects: susceptible device, noise path and noise source. How to protect the susceptible device is out of the scope of the thesis. The normal methods to

deal with EMI noise are aimed at the noise propagation path, such as the insertion of EMI filter and the compact layout of power stage. With the compact layout, the stray inductance of the power circuit can be reduced and thus the resonance in the power circuit can be reduced. With the application of the EMI filter, the noise generated by the inverter can be either separated or localized, as shown in Fig. 1.2. For example, most of the DM and CM noise current generated by the inverter are blocked and shunted by the EMI filter from flowing into power supply.

In conducted EMI measurement, a standard network, known as Line Impedance Stabilization Network (LISN), is used to provide standard load impedance to the noise source. The voltage across this load is measured as conducted noise emission of the device under test.

Seen from the LISN, the whole system could be simplified as equivalent noise source, noise path and load. (LISN serves as the load). This is shown in Fig. 1.3. Noise source is time variant. Noise path is also time-variant and non-linear due to the switching operation. The noise measured at LISN is determined by the excitation of the noise source and the response of the noise transmission network. If in frequency domain, the noise source is expressed by its transfer function as N(s), and the noise transmission network is expressed by its transfer function as Z(s), then the noise measured at LISN, F(s), can be expressed in frequency domain as the production of N(s) and Z(s).

$$F(s) = N(s) * Z(s) \tag{1.1}$$

If the magnitude of each item in above formula is represented in dB, then we have following equation:

$$20\log\left|F(s)\right| = 20\log\left|N(s)\right| + 20\log\left|Z(s)\right| \tag{1.2}$$

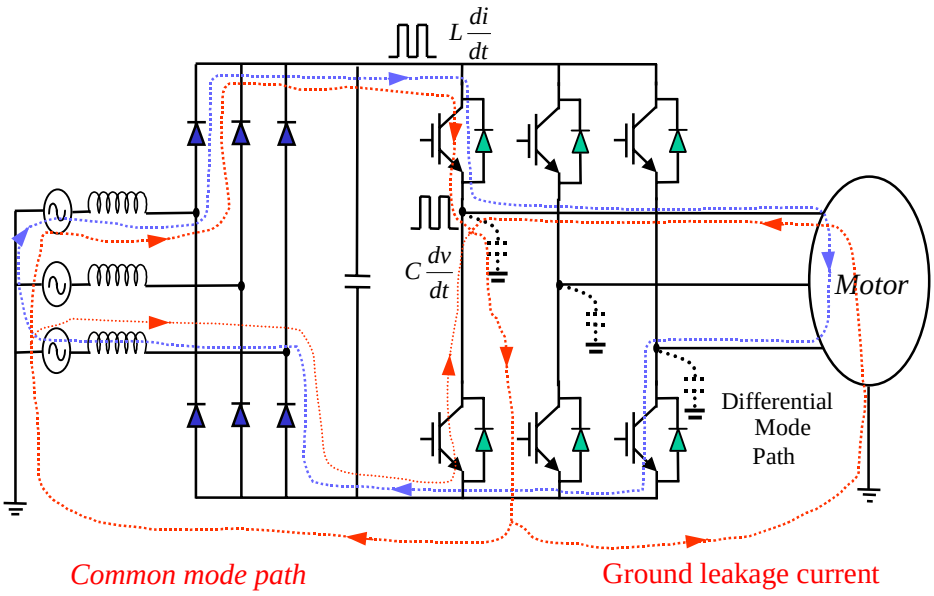


Fig. 1.1 Common-mode and differential-mode current paths in a typical PWM drive

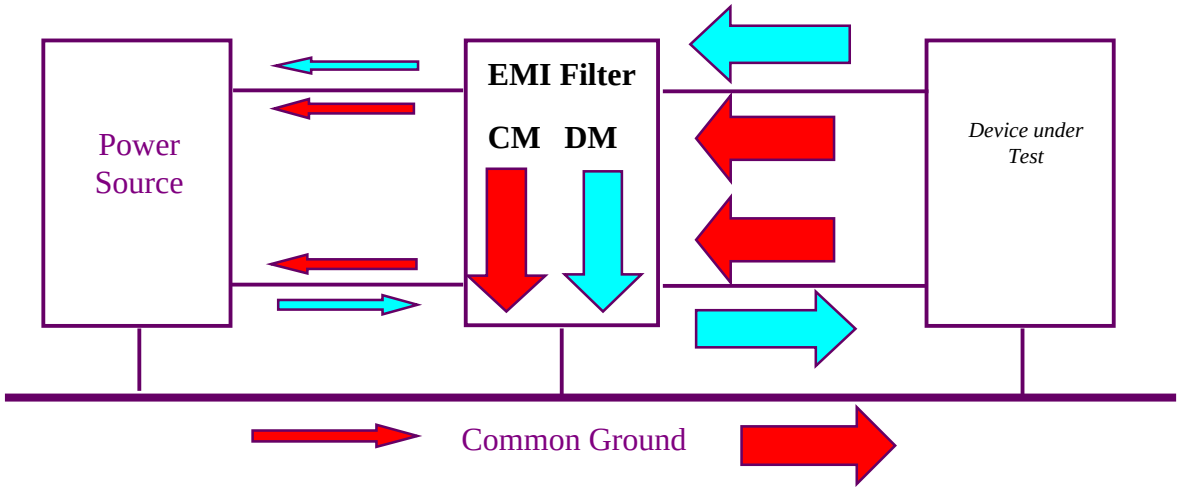


Fig. 1.2 EMI filter blocks and shunts the noise current generated by DUT

This means the dB value of the noise measured at LISN is the summation of the dB value of the transfer function of noise source and the dB value of the transfer function of noise transmission network.

As aforementioned, the insertion of EMI filter can reduce the noise measured at LISN by reducing the dB value of |N(s)|, whereas soft switching is a method to reduce the emission of noise source. In hard switching, the waveform of the voltage across collector and emitter of the switch and the waveform of the current in dc bus is close to square wave, which has very steep rising edge and falling edge. With soft switching, the slope of the rising edge and falling edge of the waveform is greatly reduced, in other words, the dv/dt and di/dt is greatly reduced. This idea is illustrated in Figs. 4 and 5.

For a periodical trapezoidal waveform, shown in Fig. 1.4, if the period is T, the slope of rising or falling edge is t_r. Then the magnitude of its Fourier series can be expressed as:

$$I_n = 2Id \frac{\sin(n\pi d)}{n\pi d} \frac{\sin(n\pi t_r / T)}{n\pi t_r / T} \tag{1.3}$$

Its magnitude is shown in Fig. 1.5.

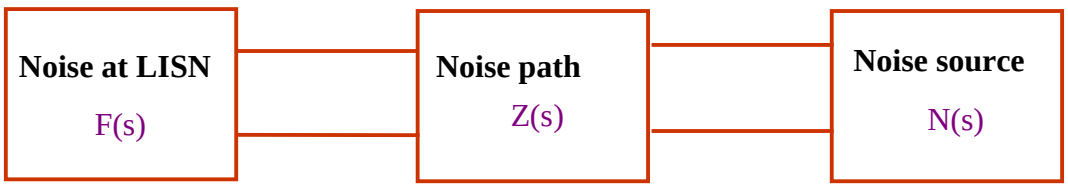


Fig. 1.3 Block diagram of a simplified noise propagation

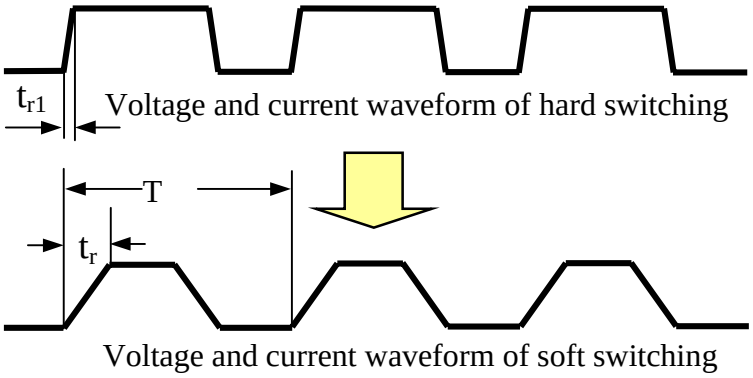


Fig. 1.4 The slope of the edge of the current and voltage waveform is reduced by soft switching

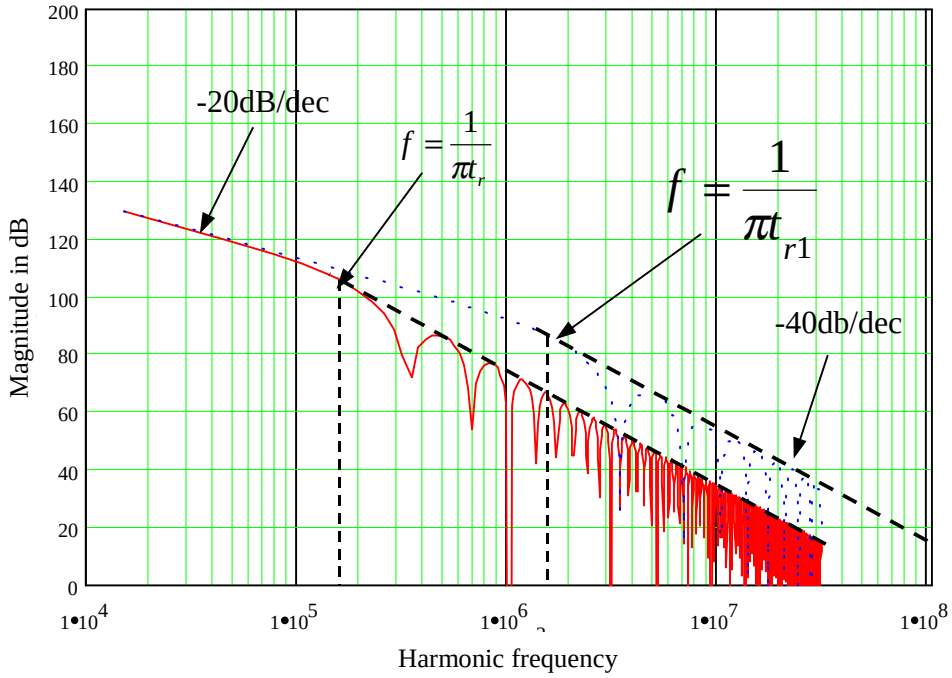


Fig. 1.5 Fourier series of trapezoidal waveform with different slope of edge

From Fig. 1.5, it is seen that the envelope of the harmonic frequencies has two slopes. At low frequency range, the magnitude of the harmonics is reduced at a rate of –20dB/dec. At high frequency range, the magnitude is reduced at –40dB/dec. The turning frequency of this two different attenuation rate is determined by the slope of the rising and falling edge of the waveform, namely dv/dt and di/dt. If the slope of the edge of the waveform is reduced by 10 times, then the turning frequency can be reduced by 10 times, and further magnitude reduction of the harmonics can be achieved. However, it is also clearly seen that reducing dv/dt and di/dt doesn't help reducing the magnitude of the harmonics in low frequency range. This is the limitation of soft switching method for noise reduction.

1.3 Scope of the thesis

In this thesis, the configurations of the experiments are described in Chapter II. Some issues relating to EMI measurement are also discussed in this chapter.

In Chapter III, the turn on/ turn off dv/dt and di/dt test of IGBT is introduced. The operation principles of a single-phase full-bridge hard-switching inverter and a single-phase full-bridge Resonant Snubber Inverter (RSI) are explained. These two circuits service as the test beds for all the EMI experiment conducted in this thesis. The implementation of RSI is discussed and the EMI spectra are analyzed and characterized. The variable timing control and fixed timing control are realized and the effects are tested and discussed.

Conclusions are drawn in Chapter IV. Future research works are also suggested in this chapter.

The design of the control interface board and gate drive board for IGBT and MCT are given in appendix. This is crucial to the operation of the inverter and the EMI experiment.

Chapter II

EMI EXPERIMENT CONFIGURATION AND MEASUREMENT

In this chapter, the conducted EMI noise measurement setup and procedures are introduced. The common mode noise and different mode noise measurement is briefly reviewed. Some general issues about EMI noise measurement are also described.

2.1 Conducted EMI noise measurement setup

The conducted EMI measurement is made in a shielded enclosure, EMI lab, in order to reduce the interference of the outside radio frequency noise and ensure valid, repeatable measurement results.

The goal of the experiment is to investigate the soft switching effects in motor drive applications, and make a comparative studies of conducted EMI between hard switching inverter and resonant snubber inverter, not to determine the compliance with Federal Communications Commission (FCC) emission requirements. Therefore, the experiment procedures do not strictly follow the FCC electromagnetic compatibility testing rules.

The noise testing circuit is shown in Fig. 2.1. This circuit is used to measure total conducted noise, which refer to the noise propagated from the device back into public electrical power network via the supply cord. As required by the FCC, the two input power leads of the inverter is individually connected through Line Impedance Stabilization network (LISN) to the input power source. LISN provides specified measuring impedance for noise voltage

measurement and isolates the EUT and the measuring equipment from the supply mains at radio noise frequencies.

The noise voltage measurement is made at the plug end of the inverter power cord and is expressed as the voltage developed across the 50-Ω port terminated by a 50-Ω measuring instrument. This noise voltage is measured with respective to ground.

The HP8568B Spectrum Analyzer is used in the test to measure the noise emission of the inverter. Instead of International Special Committee on Radio Interference (CISPR, from its title in French) quasi-peak function, the 'peak-hold' mode, which is the only available operation mode of this type of spectrum analyzer, is used for the measurement. The noise frequency range covered by the Spectrum Analyzer is from 0 Hz to 1500 MHz; our interested range is from 10 kHz to 30 MHz.

For total noise measurement, one 50-Ω connector of a LISN is connected to spectrum analyzer, which has a 50 Ω termination inside. The 50-Ω connector of the other LISN is resistively terminated in 50-Ω when not connected to the measuring instrument. Thus, the noise current flow through the LISN can be balanced.

As specified by FCC, the LISN provides 50Ω impedance over the interested frequency range when terminated with 50Ω resistor. The tolerance is ±20%.

Measurements of conducted interference are reported in terms of dB (mV), which is the default setting of HP8568B Spectrum Analyzer.

The power stage and the noise measurement setup in the EMI lab is shown in Fig. 2.2.

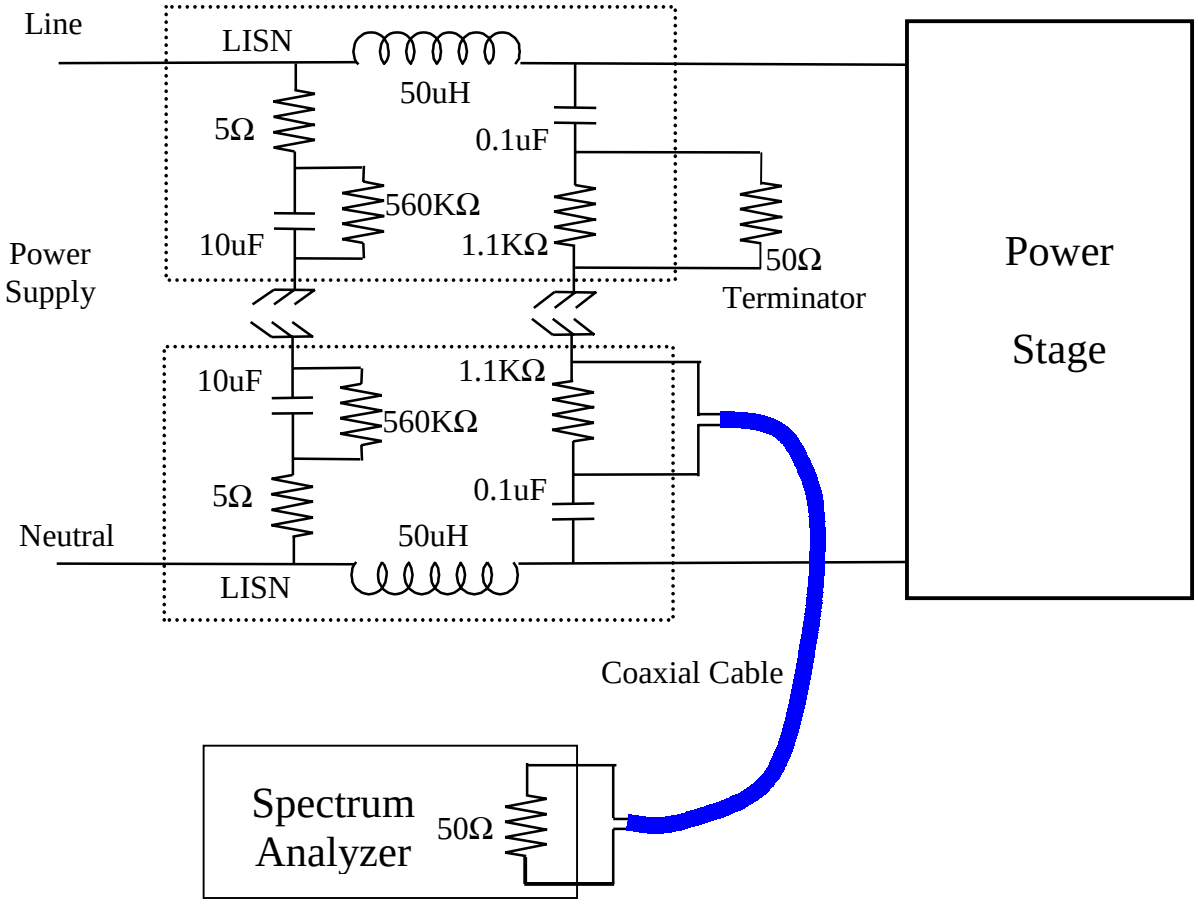


Fig. 2.1 Total noise measurement with LISN and Spectrum Analyzer

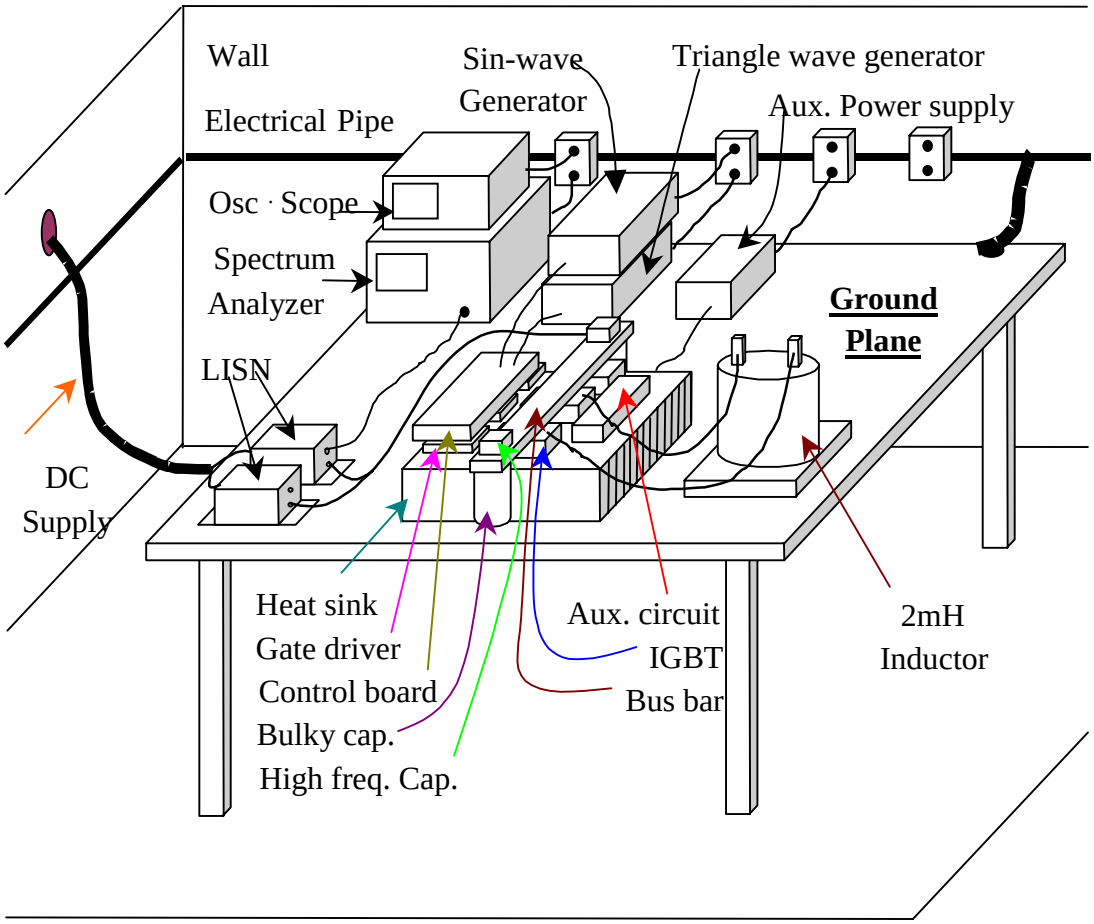


Fig. 2.2 Test setup in EMI room

The test bench is covered by a thick copper sheet that is used as ground plane. The ground plane is connected to the electrical pipe via a copper foil. The electrical pipe is connected to the ground of power mains. The power stage, inductive load, LISNs and all the testing equipment are put on top of the ground plane. The LISN housing, the measuring instrumentation case, the base plate of the load inductor and the heat sink of the power stage are electrically bonded together with ground plane, so that they have the same reference potential. The IGBTs of the inverter, IGBT gate drivers, control circuit and auxiliary circuit are all mounted on heat sink. A DC power supply that can provide 0~300V is used in the experiment. The DC power supply is outside the EMI room and is connected to the power stage via a power cord through a hole in the wall.

The pictures of the experiment setup in EMI room and the power stage are shown in Figs. 2.3 and 2.4, respectively.

2.2 Common mode and differential mode noise separation

FCC Electromagnetic Compatibility testing procedures doesn't require the separation of CM noise and DM noise. However, it is necessary for us to better understand the mechanism of noise generation and find an effective method to suppress the noise with different characteristics.

The concept of CM noise and DM noise are shown in Fig. 2.5.

The currents flowing equally in the two conductors, but in opposite directions, are known as the differential mode currents. The currents flowing in the same direction along both conductors are defined as common mode currents. Common mode current must flow through the common ground of the conductors.

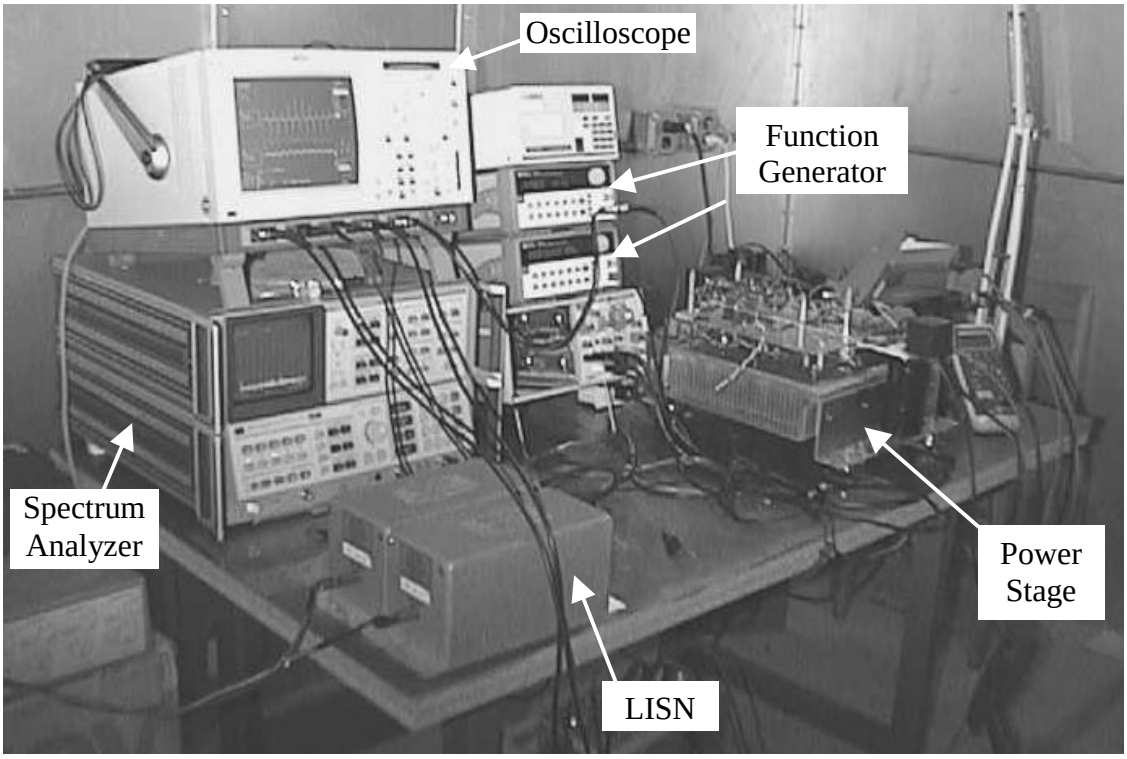


Fig. 2.3 Experiment setup in EMI room

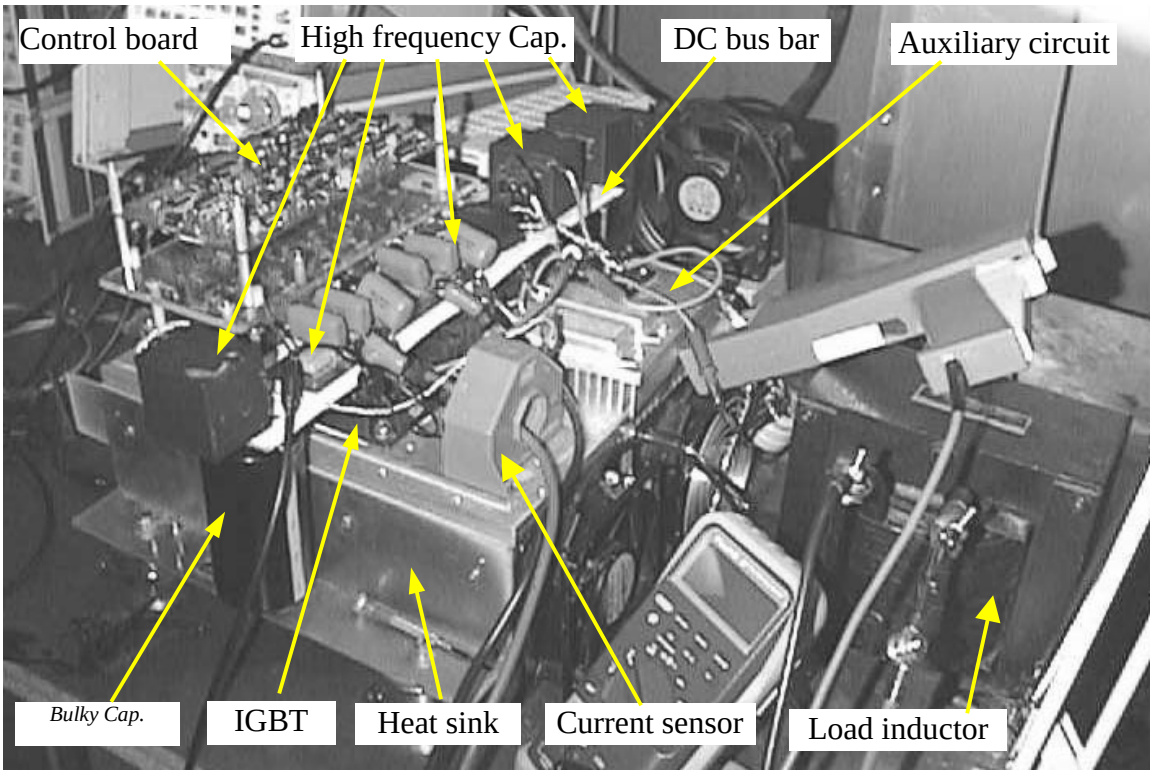


Fig. 2.4 Power stage setup

Actually, there is only one current in one conductor. However, this current can be viewed as the summation of DM current and CM current. In Fig 2.5, I_1 and I_2 are the real currents flowing in the two conductors. V_1 and V_2 are the real noise voltages across the 50Ω terminators provided by the LISNs.

$$I_1 = I_{CM1} - I_{DM} \tag{2.1}$$

$$I_2 = I_{CM2} + I_{DM} \tag{2,2}$$

$$V_1 = V_{CM1} - V_{DM} \tag{2.3}$$

$$V_2 = V_{CM2} + V_{DM} \tag{2.4}$$

Therefore, the CM current and voltage are defined as:

$$I_{CM} = \frac{1}{2}(I_1 + I_2) \tag{2.5}$$

$$V_{CM} = \frac{1}{2}(V_1 + V_2) \tag{2.6}$$

and the DM current and voltage are defined as:

$$I_{DM} = \frac{1}{2}(I_2 - I_1) \tag{2.7}$$

$$V_{DM} = \frac{1}{2}(V_2 - V_1) \tag{2.8}$$

To separate common mode noise and differential mode noise, a differential mode rejection network (DMRN) and a common mode rejection network (CMRN) are required. The measurement setup for CM and DM noise separation is shown in Fig. 2.6.

The outputs of two LISNs are connected to the two input terminals of CMRN or DMRN via coaxial cables. The output of CMRN or DMRN is then connected to the Spectrum Analyzer.

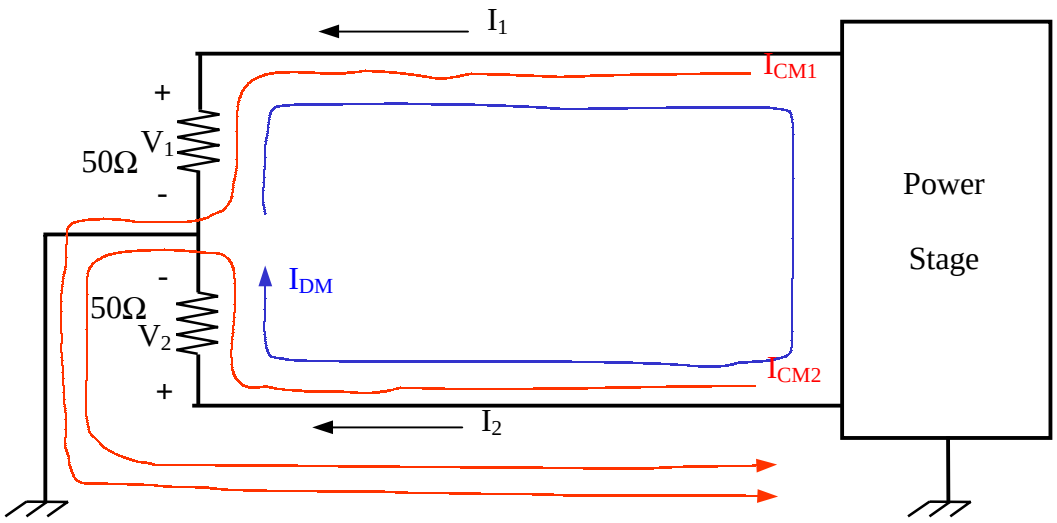


Fig. 2.5 Common mode and differential mode noise current

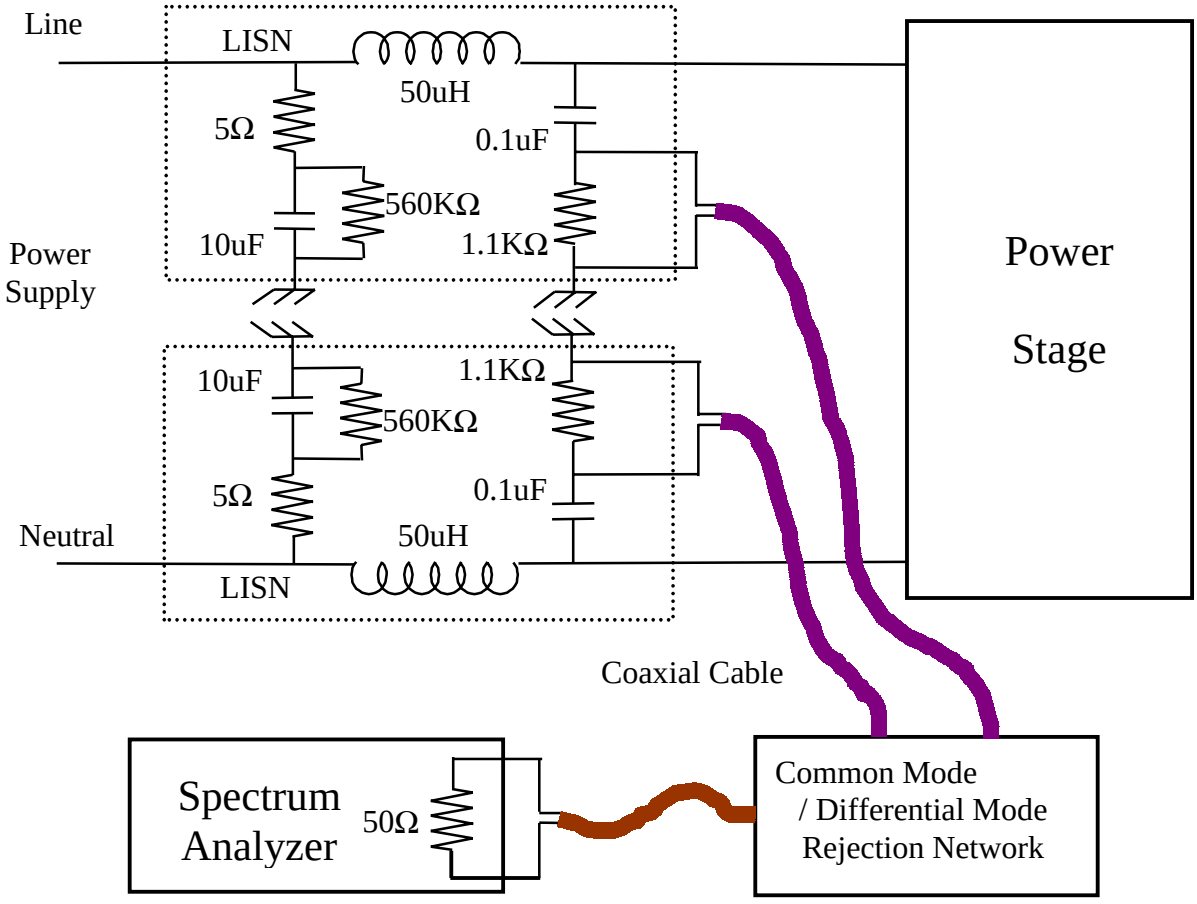


Fig. 2.6 Common mode and differential mode noise measurement setup

The common mode rejection ratio (CMRR) of CMRN and the differential mode rejection ratio (DMRR) of DMRN varied with frequency. For example, the CMRR of the CMRN used in the test is 58 dB at 1 kHz and 14.5 dB at 10 MHz. Therefore the measurement result of CM or DM noise may not be accurate at high frequency. However, it is an acceptable indication of the noise distribution at different frequency ranges. And it is sufficient for the purpose of comparison between hard- and soft- switching, because all the test and measurement conditions are the same. Once the CM noise and DM noise are separated, different solutions can be adopted to deal with different noises accordingly.

2.3 Some issues about noise measurement

FCC requires that during conducted noise voltage testing, the bandwidth of the spectrum analyzer should not be less than 9 kHz over the frequency range 450 kHz to 30 MHz. For the frequency range 10 kHz to 450 kHz, the bandwidth should not be less than 300 Hz. If bandwidths are greater than those specified above, higher readings may result for EUTs with broadband emanations.

Since EMI noise measurement involves three classes signal, and for different signal class different control settings of spectrum analyzer is required to get more accurate result, it is important to know the characteristic of the three classes signal.

The three signal classes are narrow-band, broadband and random signal.

Narrow-band signals refer to sinusoidal signals. Also, any signal that can be considered as the superposition of individual sine wave falls into the sine-wave or continuous wave (CW)/narrow-band spectrum classification. This class of signals is a Fourier series based

spectrum. The signal can be represented by Fourier series. The narrow-band designation does not refer to the occupied spectrum width of the signal, but to the individual spectral components. Each component is a sine wave, whose bandwidth is narrow, ideally, zero. The total spectrum, however, can occupy a very wide bandwidth.

Measurement of such signals with spectrum analyzer is simple as long as the individual Fourier components can be resolved, or separated. To separate the individual components of the signal requires the resolution bandwidth of the spectrum analyzer to be less than the frequency spacing between each component. Absolute amplitude is measured in dBm, rms power. Measurement accuracy, for both amplitude and frequency, will be within whatever the spectrum analyzer is normally able to achieve.

During the measurement of narrow-band signal, if the spectral components are sufficiently close together in frequency and the resolution bandwidth of the spectrum analyzer is larger than the frequency spacing, the narrow-band signal will appear like a broadband signal. Therefore, the resolution bandwidth plays an important role in the measurement.

Broadband spectral intensity distributions describe a second class of signals. It doesn't mean the occupied bandwidth of the signal is very wide. The major feature of this class of signal is that no individual sinusoidal components can be discerned. The spectrum is a continuous distribution with frequency; hence, measurement is expressed as volt per hertz. The signal is represented by Fourier integral, rather than Fourier series. The signal is composed of a group of impulses, and the spectrum is the composite spectral intensity of these impulses.

The measurement result is affected by the choice of resolution bandwidth, as well as the video filter bandwidth. Video bandwidth filtering will average the result. If the video filter

bandwidth is smaller than resolution bandwidth, the displayed signal level drops significantly, so that the true amplitude can not be measured. Therefore, video filtering should not be used in the measurement of spectral intensity of this kind of signal.

Random and probability distribution of the occurrences in time and amplitude describe the characteristic of the third signal class. The term is most frequently applied to the limiting case where the number of transient disturbances per unit time is large, so that the spectral characteristics are the same as those of thermal noise. The amplitude measurement is in units of power per hertz of random noise bandwidth. The random, fluctuating, nature of the signal requires display smoothing. This is accomplished by digital averaging, video bandwidth filtering, or both. The display level depends on the measuring bandwidth, but the measured amplitude in units per hertz is independent of the bandwidth.

It is important that the signal needs to be smoothed for measurement, and accurate amplitude determination requires knowledge of the random noise bandwidth.

The bandwidth of video filter has an important effect on how the spectrum analyzer behaves. Making the bandwidth very narrow will smooth, or average, the spectrum signal. Hence, it is necessary to use video filter averaging for random noise signals measurement. The narrower the video bandwidth the longer the sweep time.

Unlike random noise that needs to be averaged, impulsive signals, or broadband signals, must be measured at the peak value. The application of narrow video filter bandwidth will reduce signal display level. Therefore, the video filter bandwidth should be as wide as possible in order to have negligible effect on the measurement.

It is seen from above that the measurement of different class of signals requires different control settings of spectrum analyzer, such as resolution bandwidth, video filter bandwidth, and sweeping time. Some times these requirements are opposite to each other for the measurement of different class signals. EMI noise is a signal involves all the three classes of signals. How to make the settings of spectrum analyzer to obtain a better measurement? Compromise has to be made according to the characteristic of EMI noise. For example, random noise is not a significant component in the total EMI noise. The measuring error of the random noise does not affect the EMI noise too much, whereas the impulse noise and harmonic noise generated from the inverter dominate the total EMI noise. Therefore, the determination of the video frequency bandwidth should be made according to the requirement of impulse noise, and the requirement of random noise could be ignored.

FCC has resolution bandwidth requirement for EMI noise measurement in different frequency range. Moreover, the settings of video filter bandwidth and sweeping time are coupled to the setting of resolution bandwidth. Once the resolution bandwidth is chosen, the video bandwidth and sweeping time are also determined. Usually it is taken that a video filter bandwidth equal to the resolution bandwidth is adequate.

In summary, the EMI noises comprise three different classes of signals. Different classes of signals have different characteristics and require different settings of spectrum analyzer. A better knowledge of these will improve the precision of the EMI noise measurement.

Chapter III

EMI CHARACTERIZATION AND IMPLEMENTATION OF HIGH POWER INVERTERS

In this chapter, the test of switching characteristics of an IGBT module is illustrated. This type of IGBT modules is used in the hard-switching and soft-switching inverters, which serve as EMI test beds in this thesis. Then, the implementation of the hard-switching inverter and a resonant snubber inverter is described. The EMI comparisons are made between the hard- and soft-switching inverters. The mechanism of EMI noise emission and propagation of the inverters are investigated and characterized. Some implementation issues of resonant snubber inverter are discussed. The noise reduction effects and limitations of the resonant snubber inverter are also addressed in this chapter.

3.1 Turn-on/off characteristics of a IGBT

The purpose of the experiment is to investigate how much effect the gate resistor and snubber capacitor will bring upon the switching operation of the IGBT. The tested IGBT module is TOSHIBA MG400J2YS50 600V/400A. The test is conducted at 300V DC bus voltage, which is supposed to be the DC link voltage of electric vehicle.

The testing circuit is shown in Fig. 3.1

The test is applied to the lower side IGBT in the module. The gate of the upper side IGBT is shorted to the emitter of upper side IGBT to prevent its turn-on. A 2mH inductor is

connected in parallel with the upper side IGBT. A 5mΩ current shunt is inserted in the circuit. The current flowing through the switch can be derived from the voltage across the current shunt.

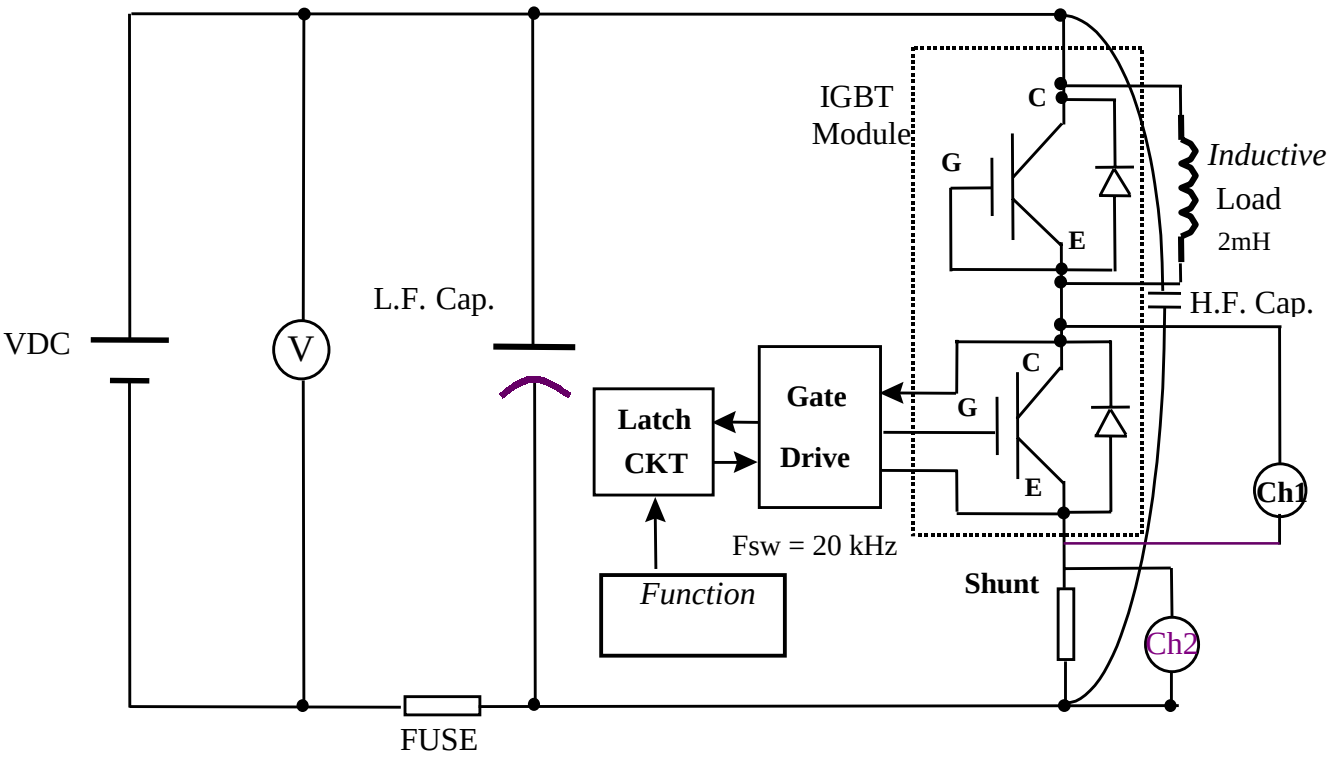


Fig. 3.1 IGBT turn on / turn off testing circuit

The switching frequency of the lower side IGBT is 20kHz. By manually changing the duty ratio of switching cycle, the current flowing through the switch could be adjusted to the desired value. The gate driver control signal is obtained from a pulse generator, which can produce very short pulse at low frequency. This control signal is fed to the IGBT gate driver through a latch circuit. The latch circuit, together with gate driver board, provides a short circuit protection function to the IGBT. The gate driver board can detect the de-saturation of the IGBT when the short circuit occurs, and as soon as the de-saturation is detected, it sends out a fault

signal to the latch circuit. Then the latch circuit shuts down the control signal, and the IGBT is thus protected.

The current flowing in lower side IGBT is shown in Fig. 3.2

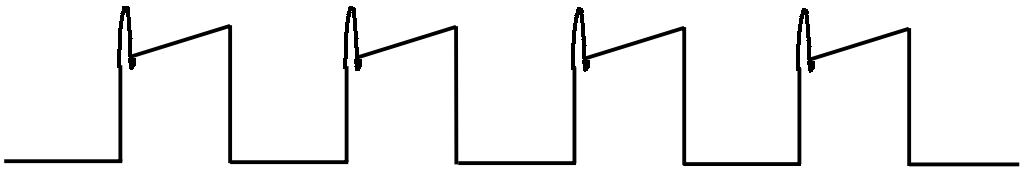


Fig. 3.2 The waveform of the current flowing through the switch

Whenever the lower side IGBT turns on, the 300V DC bus voltage is applied to the 2mH load inductor, and the current in the inductor is charged up. When the lower side IGBT turns off, the inductor current freewheels through the upper-side anti-parallel diode. After a few cycles, the current in the inductor will be stabilized.

Effect of gate resistor:

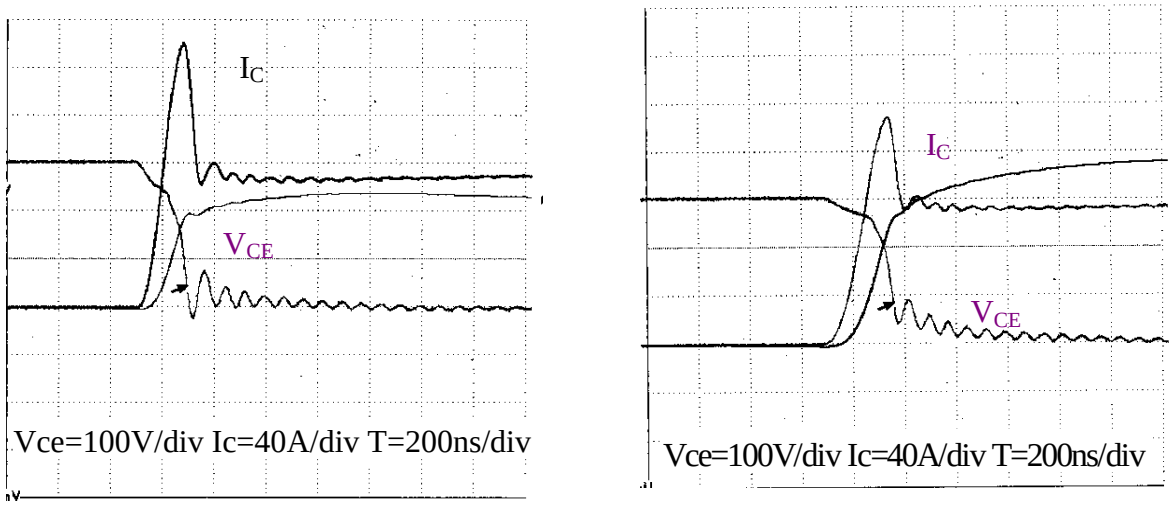
Different gate resistor has different effect upon the IGBT turn on di/dt. The larger gate resistor, the smaller di/dt. This is shown in Fig. 3.3

In Fig. 3.3 (a), the gate resistor is 2.4Ω. The stabilized switch current is 100 A, whereas the current spike in the turn on transition is 220 A, 120% higher than the stabilized switch current. The di/dt in this case is about 2750A/μs. In Fig. 3.3 (b), the gate resistor is increased to 4.7Ω. The stabilized switch current is also 100A, but the turn-on transition current spike is reduced to 190A, and the di/dt is reduced to 950A/μs.

The reason for the current spike is upper side diode reverse recovery. When the lower side IGBT turns on, 300V is applied to the load inductor, and the anti-parallel diode of the upper

side IGBT is also reverse biased. During the diode reverse recovery transition, the diode is still in conduction. Thus the DC bus is short circuit by the upper side diode and lower side IGBT during the diode reverse recovery period. If we slow down the IGBT turn on speed with larger gate resistor, then, during the upper side diode reverse recovery period, the lower side IGBT is still not fully turned on, therefore the current spike is reduced.

However, since the IGBT turn-on transition is prolonged, the overlap area of the current waveform and voltage waveform is increased, namely the turn-on loss is increased.



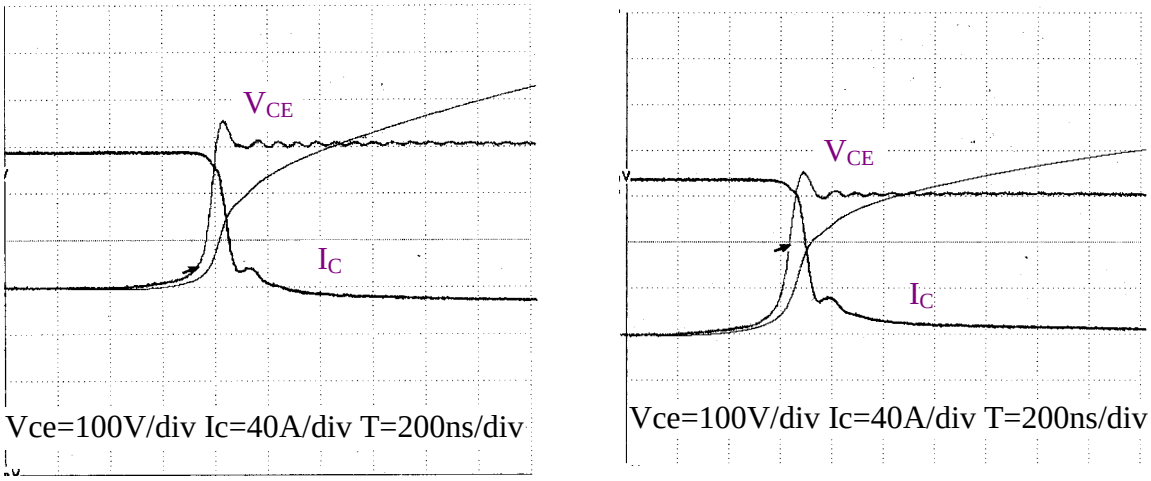
(a) Rg = 2.4Ω (b) Rg = 4.7Ω

Fig. 3.3 IGBT turn on with different gate resistor

Unlike the effect gate resistor brings upon IGBT turn-on, the variation of gate resistance doesn't have significant effect upon IGBT turn-off. This is shown in Fig. 3.4.

In Fig. 3.4 (a), the gate resistor is 2.4Ω. In Fig. 3.4 (b), the gate resistor is 4.7Ω. For both cases, the bus voltage is 300V and the switch current before turn-off is 120A. The voltage spike is 50V, 16% of the bus voltage. This is not very large. The voltage rising slope of the two cases is about the same. Therefore, the different gate resistance doesn't have much effect upon the IGBT turn-off dv/dt.

In the test, it is also observed that the variation of gate resistance doesn't bring too much difference to the turn-on dv/dt and turn-off di/dt. These results are further verified by using other gate resistor values, such as 0Ω and 10Ω. Here only show the results of 2.4Ω and 4.7Ω.



(a) Rg = 2.4Ω (b) Rg = 4.7Ω

Fig. 3.4 IGBT turn off with different gate resistor

The effect of gate resistance variation upon turn-on di/dt is listed in table 3.1. The data are also visualized as curves in Fig.3.5

Table 3.1 IGBT turn-on di/dt at different gate resistance

Gate Resistance	di/dt (A/μs)		
	Ic = 40A	Ic = 80A	Ic = 130A
0 Ω	2500	2667	3250
2.4 Ω	667	1152	1447
4.7 Ω	545	640	711
10 Ω	320	457	472

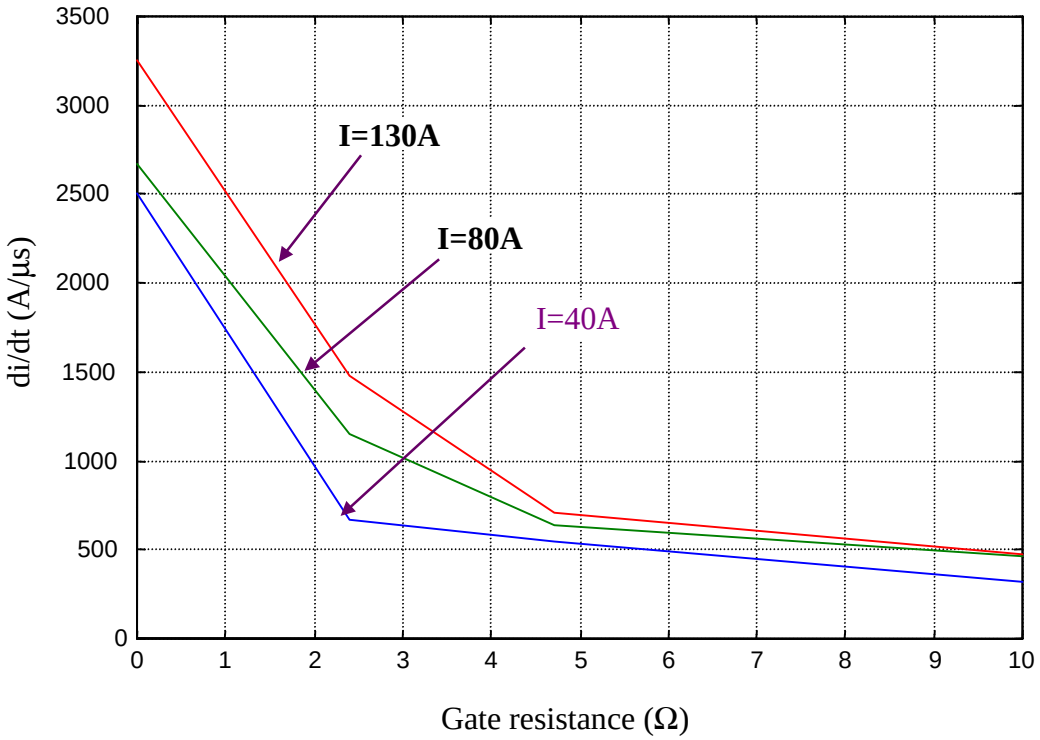


Fig. 3.5 IGBT turn-on di/dt at different gate resistance

Table 3.2 shows the total experiment result. Moreover, the switching loss is listed in the table. The switching loss is calculated according to the voltage and current waveform during the turn-on / turn-off transition. The calculation can be easily made through the integration function provided by the digital oscilloscope. The formula for calculating the switching energy is as simple as follows:

$$E_{on} = \int_0^{t_{on}} I_c(t) \cdot V_{CE}(t) \cdot dt \tag{3.1}$$

$$E_{off} = \int_0^{t_{off}} I_c(t) \cdot V_{CE}(t) \cdot dt \tag{3.2}$$

The switching loss could be estimated by multiplying the energy loss of each switching operation with the switching frequency.

Table 3.2: Comparison of the dv/dt, di/dt, and the switching losses of the IGBT with gate resistor variations @ $C_R = 0.22\mu F$

(TOSHIBA IGBT Model: MG400J2YS5D, 600V-400A)

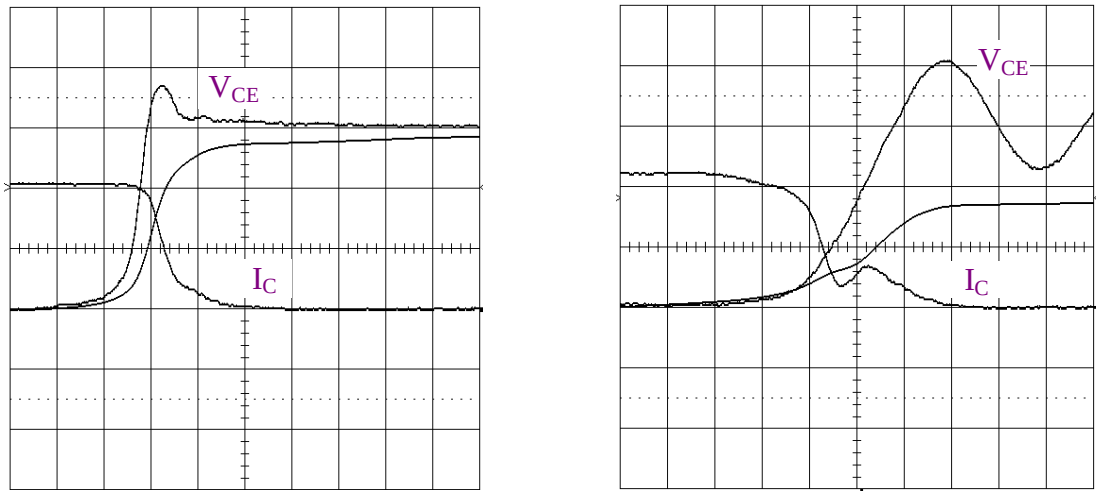
Gate Resistors [Ω]	Test # 1					Test # 2					Test # 3				
	Turn-off		Turn-on	Switching Energy		Turn-off		Turn-on	Switching Energy		Turn-off		Turn-on	Switching Energy	
	ste.dv/dt [V/us]	Typ. dv/dt [V/us]	di/dt [A/us]	Eon [MJ]	Eoff [MJ]	ste. dv/dt [V/us]	typ. dv/dt [V/us]	di/dt [A/us]	Eon [MJ]	Eoff [MJ]	ste. v/dt [V/us]	typ.dv/ dt [V/us]	di/dt [A/us]	Eon [MJ]	Eoff [MJ]
0	300	261	2,500	10.2 @25A	0.48 @ 66A	500	438	2,667	27 @ 80A	1.6 @ 128A	667	585	3,250	38 @ 130A	3.8 @ 184A
2.4	325	310	667	10.8 @ 25A	0.73 @68A	523	450	1,152	14.4 @ 72A	2.1 @ 132A	750	530	1,474	19.2 @ 140A	6.0 @ 216A
4.7	340	315	545	14.0 @ 40A	1.1 @80A	450	430	640	17.5 @80A	2.42 @ 130A	730	480	711	26.4 @ 150A	6.8 @ 230A
10	357	300	320	14.4 @ 40A	1.38 @ 81A	575	400	457	11.2 @ 80A	3.3 @ 134A	714	430	472	24.5 @ 130A	7.4 @ 212A

- The typical performance criteria for dv/dt and di/dt are based on from 10% to 90% of the final value.
- Ste: steepest. Typ.: typical.

Effect of snubber capacitor

Snubber capacitor is used to limit the IGBT turn-off dv/dt. The larger the snubber capacitor, the smaller the turn-off dv/dt. The purpose of the experiments is to quantitatively determine the relations between the snubber capacitor and the turn-off dv/dt, and find a proper value of the snubber capacitor for the application of resonant snubber inverter.

Fig. 3.6 shows the effect of different snubber capacitor upon IGBT turn-off dv/dt.



(a) Cr = 0 μF (b) Cr = 0.22μF

Vce=100V/div, Ic=100A/div, T=0.2us/div

Fig. 3.6 The effect of snubber capacitor upon IGBT turn-off dv/dt

In above figure, it is seen that for the same voltage and current conditions, hard turn-off has a larger dv/dt. The steepest slope is about 5000V/μs. With a 0.22μF snubber capacitor, the turn-off dv/dt is reduced to 645V/μs. In addition, the overlap of the voltage and current waveform is reduced; hence, the turn-off loss is reduced. It is also observed that there is a bump in the switch current tail when the snubber capacitor is used. This effect slightly reduces the benefit of the reduction of turn-off loss.

The turn-off dv/dt at different snubber capacitor and load current is listed in table 3.3 and drawn in Fig. 3.7

Table 3.3 IGBT turn-off dv/dt at different snubber capacitor and load current

Snubber Capacitor (μF)	dv/dt (V/μs)		
	Ic = 90A	Ic = 140A	Ic = 200A
0	3333	3750	4000
0.022	2250	2500	3000
0.1	792	1000	1150
0.22	340	450	900
0.47	180	250	500

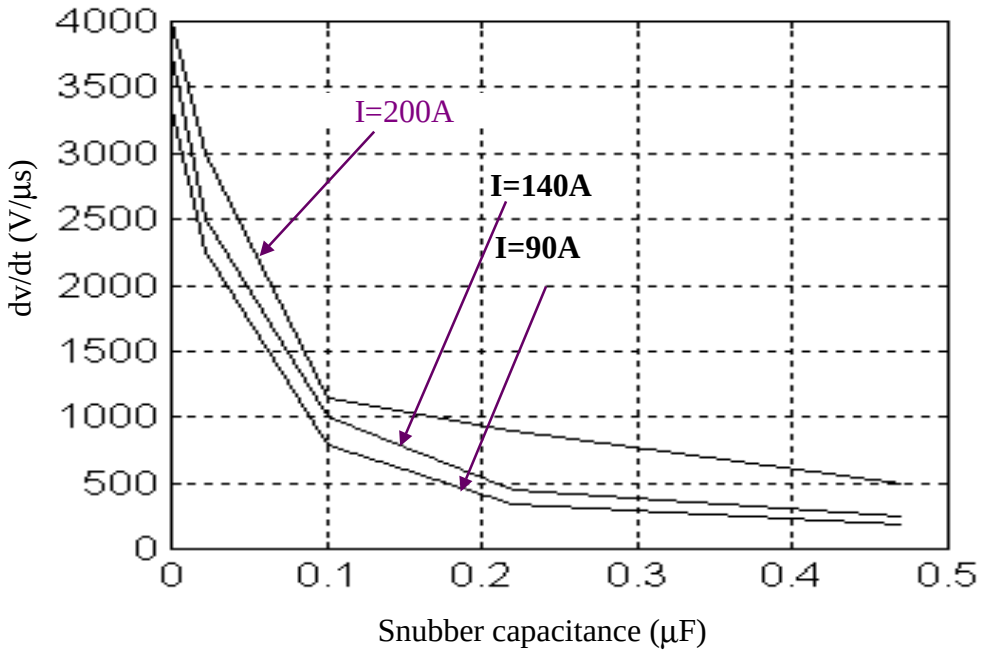


Fig. 3.7 IGBT turn-off dv/dt at different snubber capacitor and load current

It is seen in Fig. 3.7 that when the snubber capacitance is increased from 0 to 0.1μF, the turn-off dv/dt is reduced a lot. When the snubber capacitance is increased from 0.1μF to 0.47μF, the reduction rate of the dv/dt is reduced. Therefore, a very large capacitance is not optimal for the reduction of dv/dt. A better choice of the snubber capacitance is in the range of 0.1 to 0.22μF.

To reduce the voltage ringing bring about by the snubber capacitor at turn off, which is shown in Fig. 3.6, a high frequency capacitor is needed. In the test, a polyester capacitor is used. It has small equivalent series inductance (ESL) and equivalent series resistance (ESR). In addition, tight connections of the capacitor leads with the IGBT terminals are required to reduce the resonance occurred at switch turn off.

The total experiment result of the variations of snubber capacitor is listed in table 3.4. The calculation of switching energy is same as aforementioned.

Another consideration in choosing the snubber capacitance is the IEEE standard for motor protection.

Figure 3.8 shows IEEE standard 522-1992, which sets up a limit for PWM inverter output dv/dt. This standard is designed for 300 V dc bus and 200 A load current inverter to drive a 208 V_{l-l} motor. The turn-off dv/dt with and without snubber capacitor are marked in the figure. It is seen that without snubber capacitor, or hard turn-off, the turn-off dv/dt exceeds the limit. Additional protection method is needed for the motor. Otherwise, motor winding insulation is subject to breakdown.

Table 3.4. Comparison of the dv/dt, di/dt, and switching losses of the IGBT with snubber capacitors

(TOSHIBA IGBT Model: MG400J2YS5D, 600V-400A)

Capaci-tors [uF]	Test # 1					Test # 2					Test # 3				
	Turn-off		Turn-on	Switching Energy		Turn-off		Turn-on	Switching Energy		Turn-off		Turn-on	Switching Energy	
	ste.dv/dt [V/us]	typ. dv/dt [V/us]	di/dt [A/us]	Eon [MJ]	Eoff [MJ]	ste. dv/dt [V/us]	typ. dv/dt [V/us]	di/dt [A/us]	Eon [MJ]	Eoff [MJ]	ste. v/dt [V/us]	typ.dv/dt [V/us]	di/dt [A/us]	Eon [MJ]	Eoff [MJ]
0	3,333	1,714	1,143	2.7 @ 50A	3.7 @ 96A	3,750	1,900	711	8.5 @ 96A	7.5 @ 144A	4,000	2,000	1,300	8.8 @ 130A	14.5 @ 200A
0.022	2,250	1,043	880	4.2 @ 44A	3.0 @92A	2,500	1,200	840	7.2 @ 84A	6.9 @ 144A	3,000	1,500	1,200	19.2 @ 180A	14.4 @ 220A
0.1	792	650	880	8.0 @ 44A	1.8 @96A	1,000	850	773	16.0 @116A	5.2 @ 160A	1,150	960	866	18.0 @ 130A	7.2 @ 190A
0.22	340	315	640	14.0 @ 40A	1.1 @ 80A	450	380	711	17.5 @ 80A	2.42 @ 130A	900	750	545	26.4 @ 150A	6.8 @ 230A
0.47	180	141	400	25.0 @ 30A	0.32 @ 72A	250	240	900	33.0 @ 90A	1.0 @ 132A	500	375	1,066	43.0 @ 160A	2.7 @ 210A

- The typical value of dv/dt and di/dt are calculated based on 10% to 90% of the transition slope.

However, the snubber capacitor can not be added to the IGBT directly without relevant method to deal with the turn-on loss. Because each time at turn on, the snubber capacitor is shorted by the switch, and the energy stored in the capacitor will dump into the switch and cause significant loss.

In the case of resonant snubber inverter, the turn-on loss introduced by snubber capacitor can be avoided by zero voltage transition. Thus, the dv/dt is limited by the snubber capacitor without doing any harm to the reduction of turn-on loss.

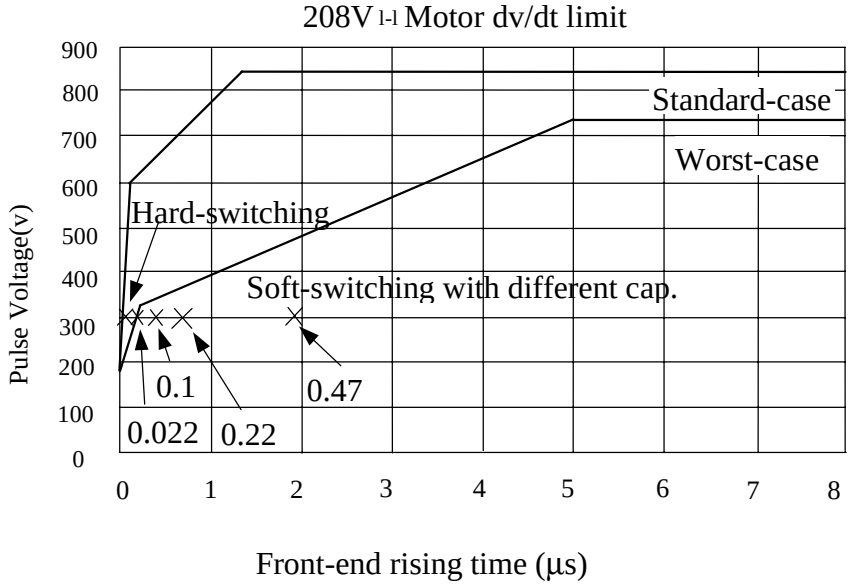


Figure 3.8 PWM inverter output compliance with IEEE Std. 522 -1992
for 300V dc bus and 200A load current

From above figure we can see 0.22μF snubber capacitor can satisfy the dv/dt requirement and with enough margin.

In summary, increasing the gate resistance can reduce the turn-on di/dt, increasing the snubber capacitance can reduce turn-off dv/dt. However, this doesn't mean a larger value is better. A proper value need to be determined based on comprehensive consideration of dv/dt,

di/dt, switching loss, and other requirements. In our experiment, 4.7Ω gate resistor and 0.22μF snubber capacitor are utilized for all the tests.

3.2 Implementation and EMI characterization of a hard –switching inverter

A single-phase full-bridge hard-switching inverter was used as a test bed for EMI characterization and for comparison with a soft-switching inverter. The test setup is described in chapter II. Fig.3.9 shows the schematic of the hard-switching inverter.

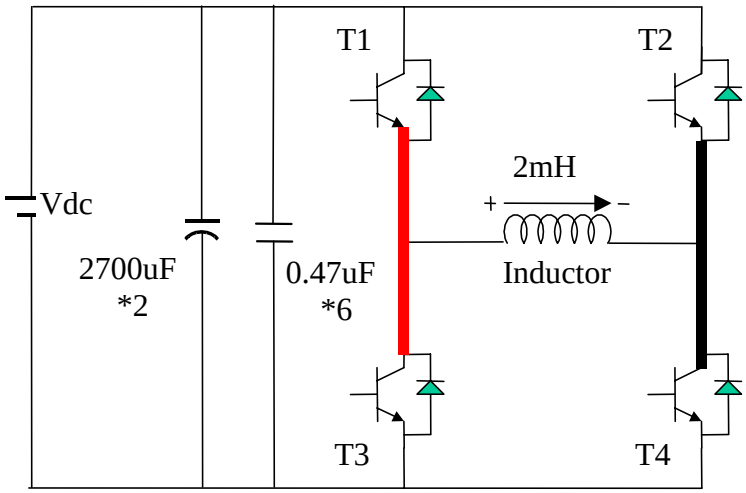
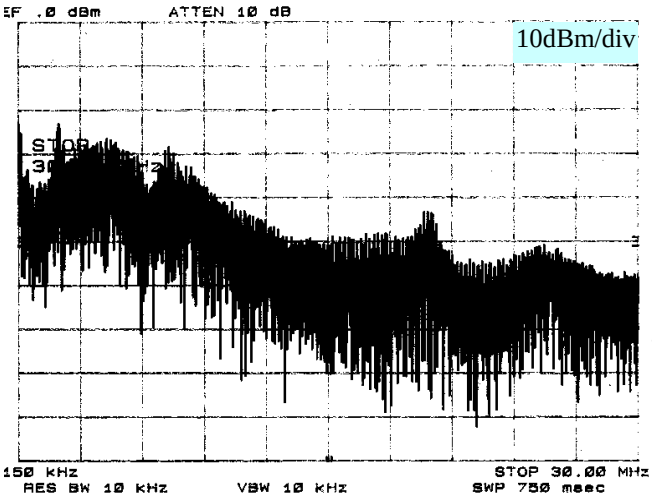


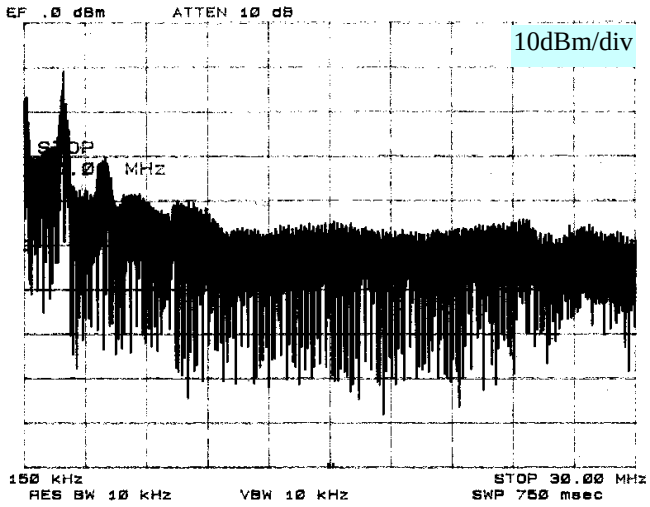
Fig. 3.9 Single-phase full-bridge hard-switching inverter

The control signal was obtained by comparing a 200Hz sinusoidal signal with a 20kHz triangular waveform. T1 and T4 turn on / off simultaneously. T2 and T3 turn on / off simultaneously. The positive load current direction is defined as above.

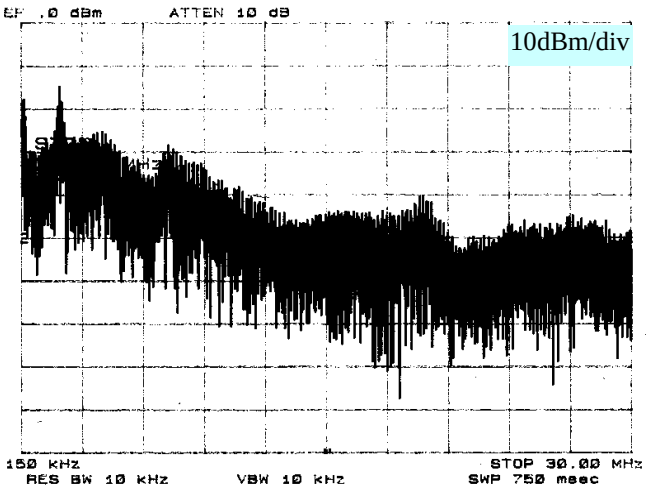
In the initial test, only two 2700μF electrolytic aluminum capacitors and two small high frequency cap were used. The CM/DM and total noise spectrum are shown in Figs. 3.10 (a), (b), (c), respectively. These spectra were achieved based on the circuit in Fig. 3.9. The input DC voltage was 300 V, and the maximum load current was 45 A.



(a) CM noise spectrum



(b) DM noise spectrum



(c) Total noise spectrum

Fig. 3.10 Hard-switching EMI spectrum

It is seen that the CM noise is peaks mainly in the 3MHz and 10MHz range, whereas the DM noise dominated the low frequency range, which is less than 2 MHz. The spike at 2 MHz was caused by hard turn-on and turn-off. This spike can be seen in both the CM and DM noise spectra and the corresponding noise can be found at DC bus voltage as shown in Fig. 8.

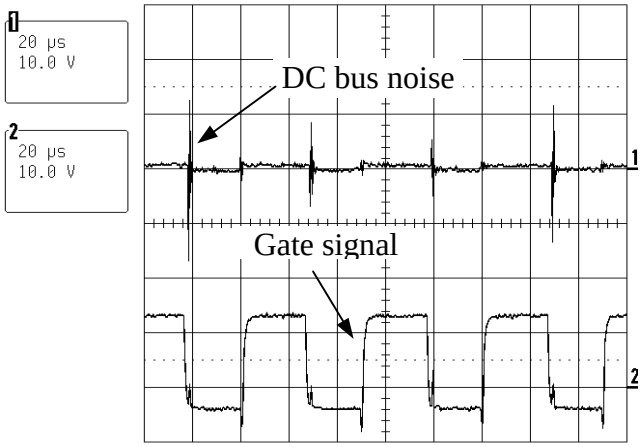


Fig. 3.11 AC coupled DC bus noise at turn-on and turn-off

The DC bus noise could be reduced by adding some high frequency low ESL capacitors. After six 400 V/0.47 µF polypropylene capacitors were closely and tightly screwed to the DC bus, the 2 MHz peak was reduced, and its peaking frequency was shifted to a lower value. This effect can be seen in Fig. 3.12.

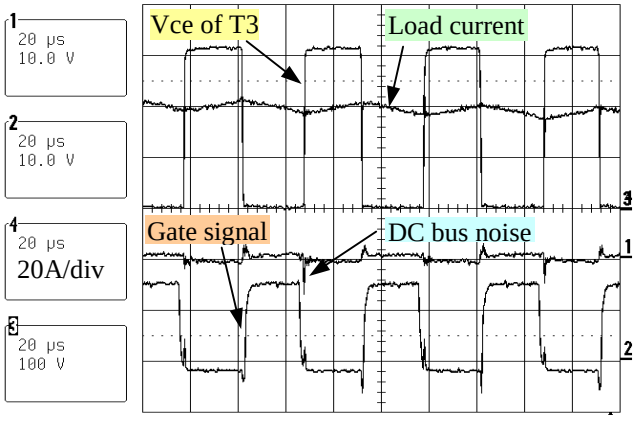


Fig. 3.12 DC bus noise at turn-on turn-off after adding high frequency capacitors

It is seen that the peak-to-peak DC bus noise spike drops from 30 V to 9 V. The spike at 2 MHz in the previous total noise spectrum was also reduced and the frequency of the reduced spike was pushed down to about 1 MHz. The total noise spectrum is shown in Fig. 3.13.

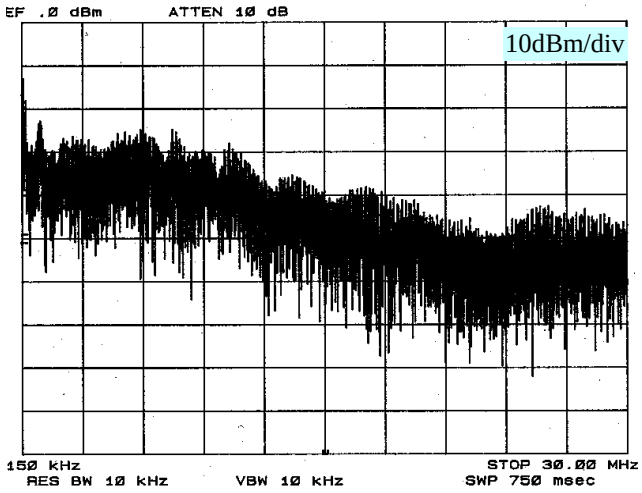


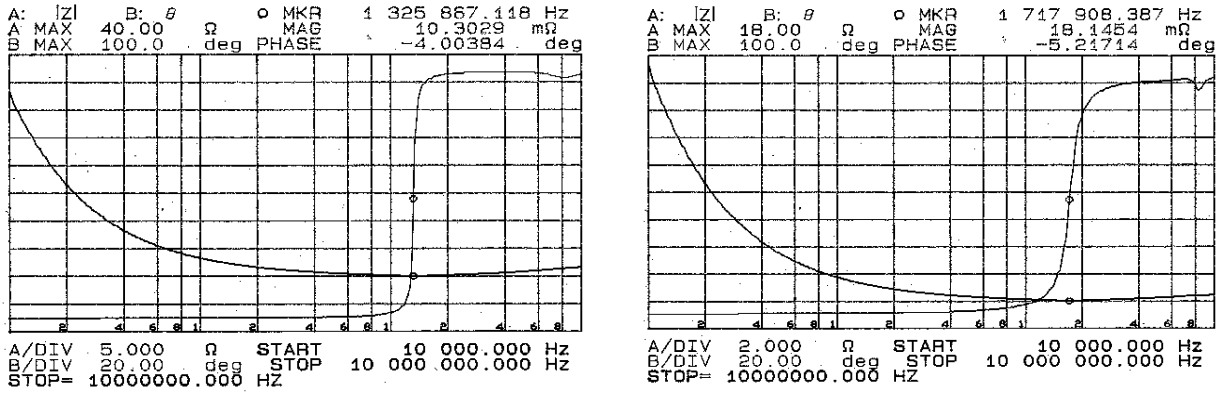
Fig. 3.13 Total noise spectrum of hard switching after adding high frequency capacitors

It can be seen that the noise spectrum envelope dropped several dBm at 2 MHz after adding the high frequency capacitors.

Since adding high frequency capacitors can reduce noise level, nine more surface-mount 400V/1μF polyester capacitors were tightly mounted on DC bus. This is shown in Fig. 2.4.

The capacitors' impedance characteristic with frequency is shown in Fig. 3.14. It is seen that polypropylene capacitor has only 10mΩ at 1.3 MHz, and polyester capacitor has only 18mΩ at 1.7 MHz. So high frequency noise current can find an easy path through these capacitors, therefore, the noise seen at the LISN is reduced.

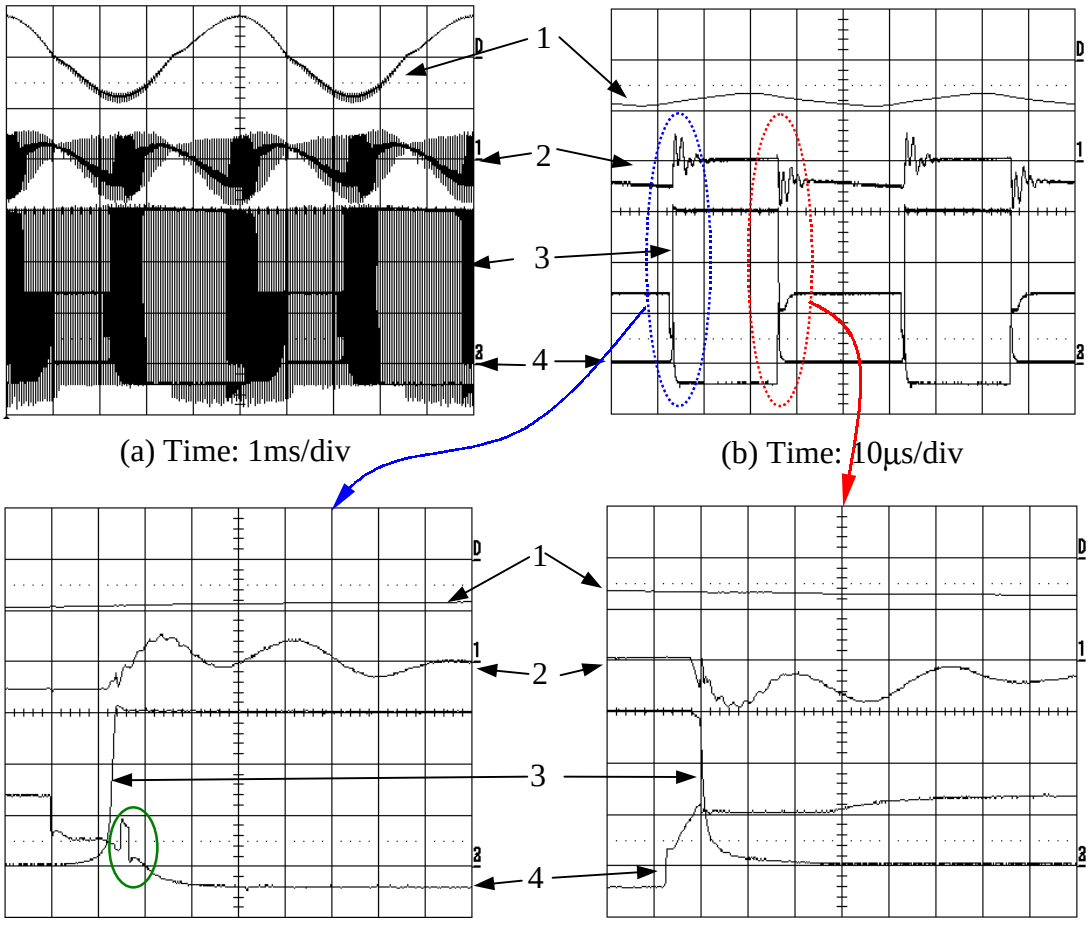
The load current waveform, voltage waveform of the IGBT T3, DC bus voltage ripple, and noise voltage across the LISN were checked. This effort is try to build relations between the noise voltage at LISN and the resonance in the circuit, thus to identify the noise source and investigate the noise propagation mechanism.



(a) Polypropylene **(b) Polyester**

Fig. 3.14 High frequency capacitor impedance characteristics

The load current, dc bus voltage ripple, and voltage across T3 are shown in Fig. 3.15.



(a) Time: 1ms/div (b) Time: 10μs/div

(c) Time: 0.5μs/div (d) Time: 0.5μs/div

1)Load current 50A/div; 2)dc bus voltage ripple 2V/div; 3)Vce of T3 100V/div; 4)Vge of T3 10V/div

Fig. 3.15 dc bus voltage of hard switching

In Fig. 3.15 (a), it is seen the peak to peak value of dc bus noise ripple is further reduced from previous 9V to 3V. In addition, the envelope of the dc bus noise ripple is modulated by the load current. The maximum ripple voltage occurs when the load current reaches its peak. The ripple voltage becomes zero when the load current cross zero. This dc bus voltage ripple is caused by the IGBT turn on/off, and is clearly shown in Fig. 3.15(b), (c), and (d). Fig. 3.15(b) is an excerption of Fig. 3.15(a) when the load current is in negative direction. Fig. 3.15(c) and (d) shows the IGBT turn off and turn on transition respectively. The sharp rising edge and falling edge of Vce has a large dv/dt about 2500V/μs, which forms a notable CM noise source. The voltage ringing in the dc bus at the switching transition is about 650kHz. The Miller effect is also observed in Fig.3.15(c) while the IGBT turn off. This may cause IGBT false on if without the –5V turn-off gate voltage level.

Noise Voltage across LISN

Total noise

The total noise voltage across LISN is shown in Fig. 3.16 (a), (b), (c), (d), and (e). (a) shows the noise of four cycles. (b) and (c) show the noise voltage when the load current reaches positive maximum, (d) and (e) show the noise voltage when the load current reaches negative maximum.

It is seen in Fig. 3.16(b) and (c), the total EMI noise is composed of a series sharp spikes, and each spike is followed by a 7 MHz high frequency ringing. The magnitudes of the spikes are around 20V. The largest peak to peak value of the high frequency resonance is about 3V, and then damped with time. It is similar in Fig. 3.16 (d) and (e), except the magnitudes of the spikes are smaller.

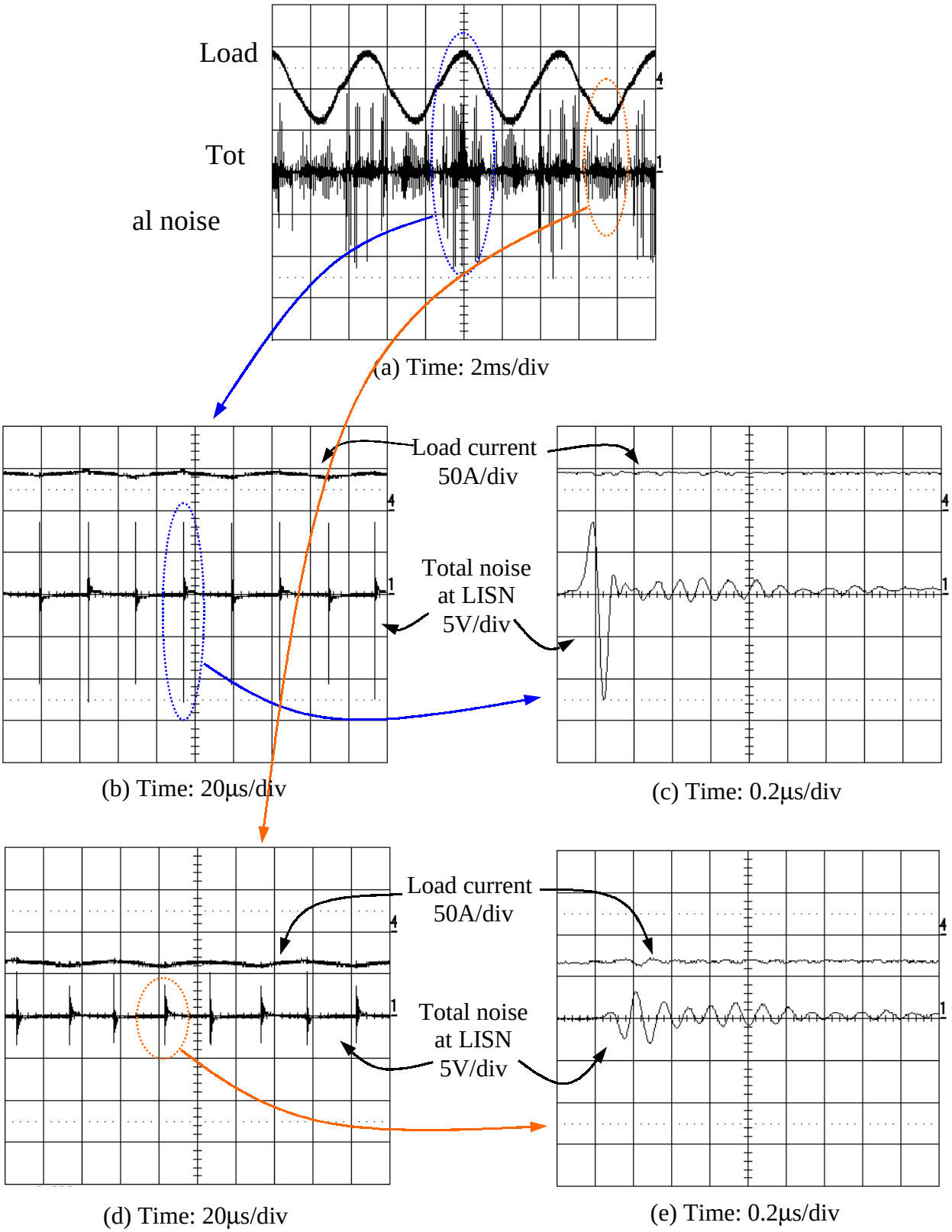


Fig. 3.16 Hard-switching inverter total noise at LISN

Differential Mode Noise

The differential mode noise across LISN is shown in Fig. 3.17.

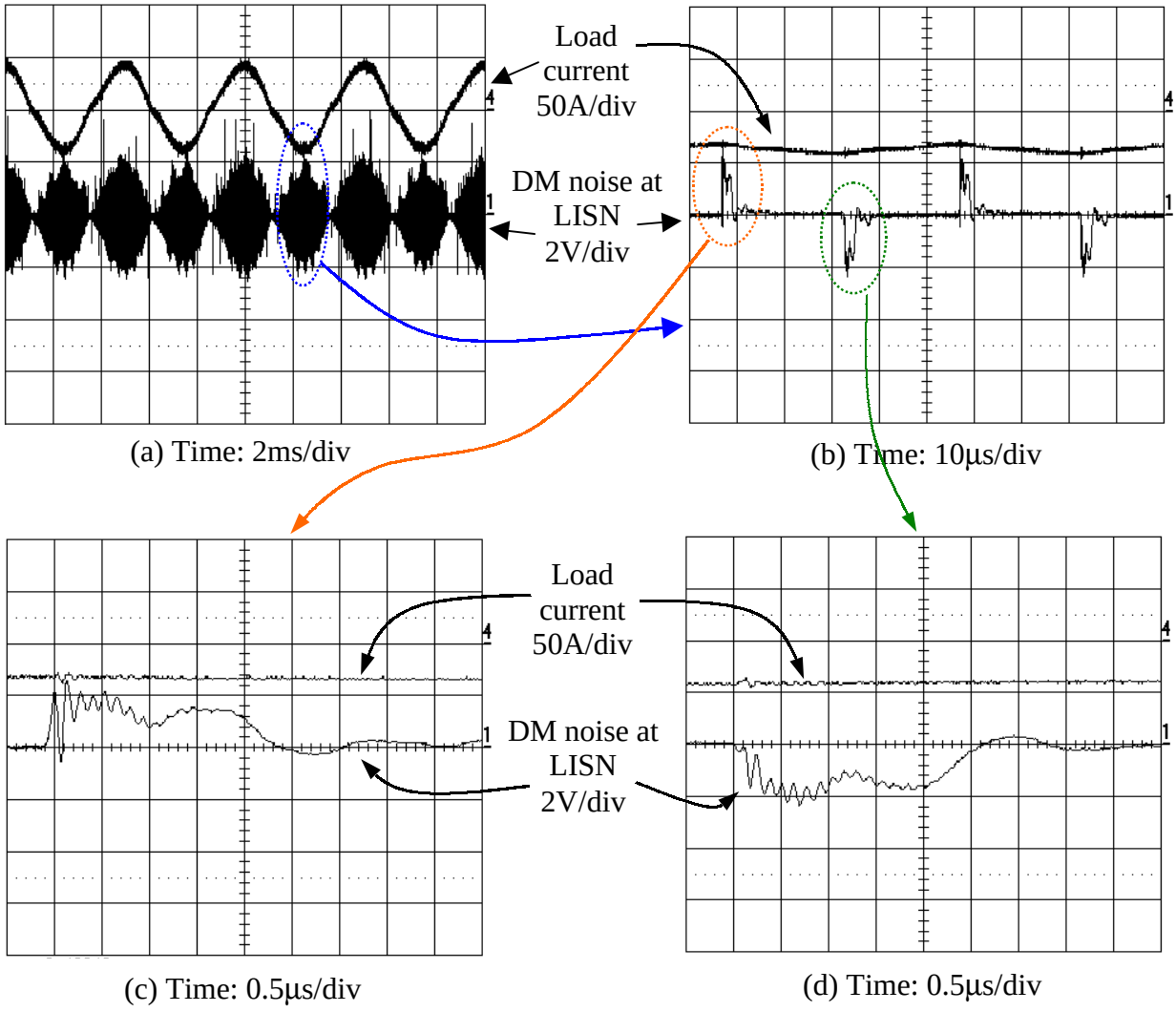


Fig. 3.17 Hard-switching inverter DM noise at LISN

In Fig. 3.17 (a), we can find the magnitude of the spike in DM noise is much smaller than that in total noise. The peak to peak value of the spike in DM noise is about 3V. In addition, the envelope of the DM noise is modulated by the load current. This is similar to the voltage ripple in dc bus. Furthermore, it is seen in Fig. 3.17 (c) and (d), the noise voltage shape and frequency are close to that of dc bus voltage ripple. Therefore, the DM noise at LISN is the reflection of

the dc bus ripple voltage, and it can be reduced by proper selection and connection of high frequency capacitors.

Common Mode Noise

Common mode noise across the LISN is shown in Fig. 3.18

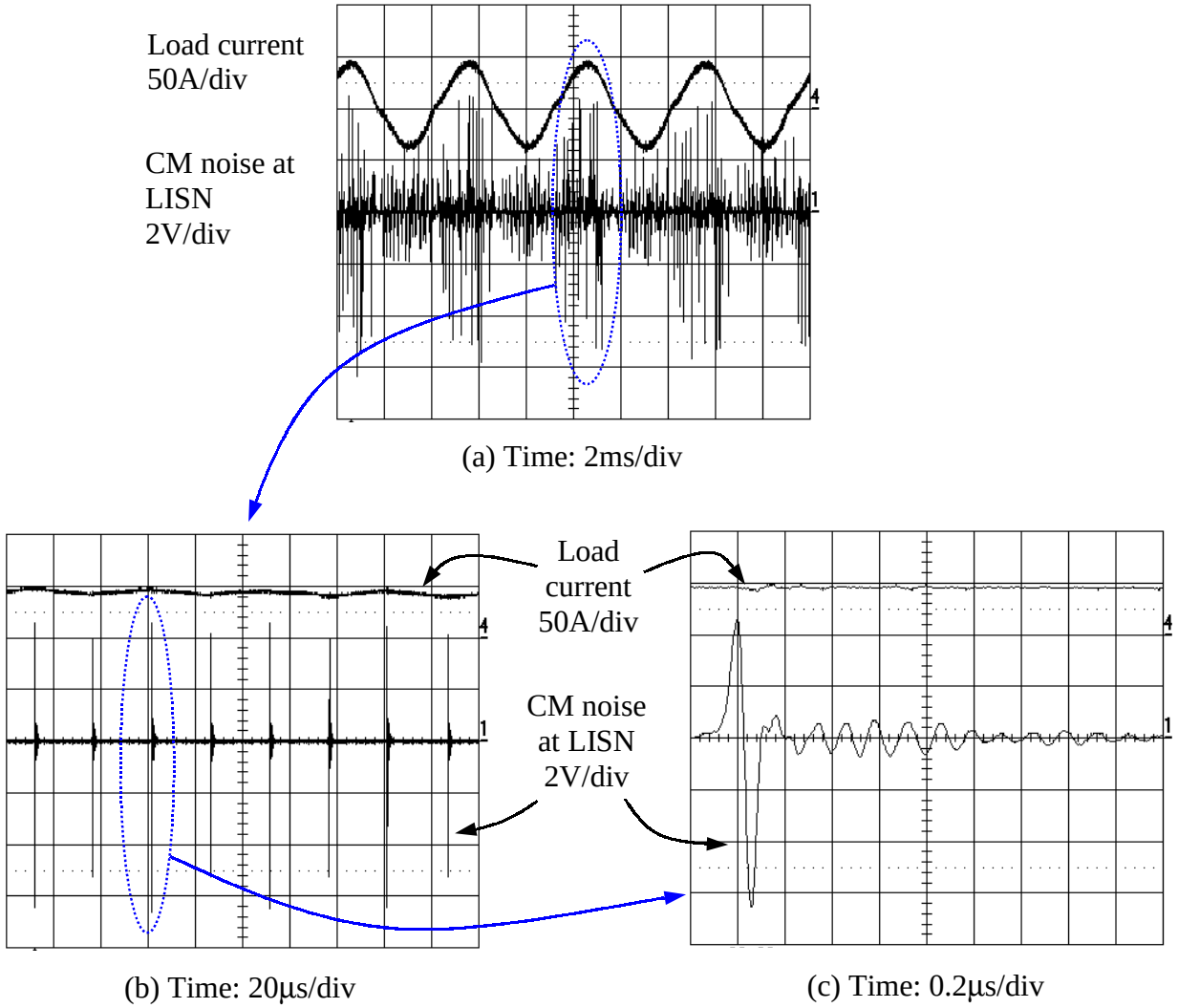


Fig. 3.18 Hard-switching inverter CM noise at LISN

It is seen that the CM noise is much larger than DM noise. The peak to peak magnitude of the spike in CM noise is about 12V. Each spike is followed by a 7MHz high frequency ringing. The CM noise voltage waveform is very close to the total noise voltage waveform. This indicates that CM noise is the dominant part of total EMI noise. Therefore, the effort of EMI reduction should be concentrate on the reduction of CM noise.

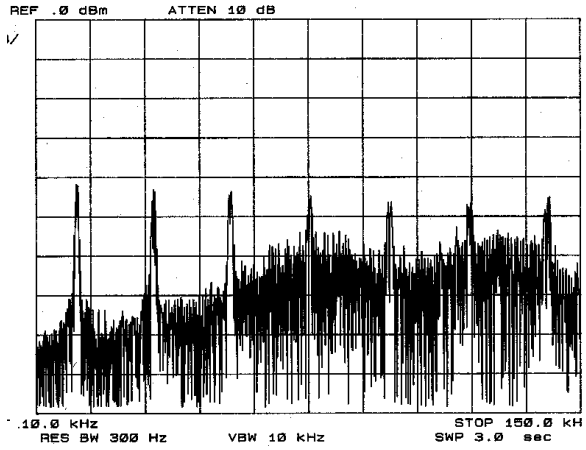
EMI noise spectra

The EMI time domain features are also reflected from their frequency domain spectra. Fig. 3.19 shows the EMI spectra which corresponds to the waveforms shown in Fig.3.16 to Fig. 3.18.

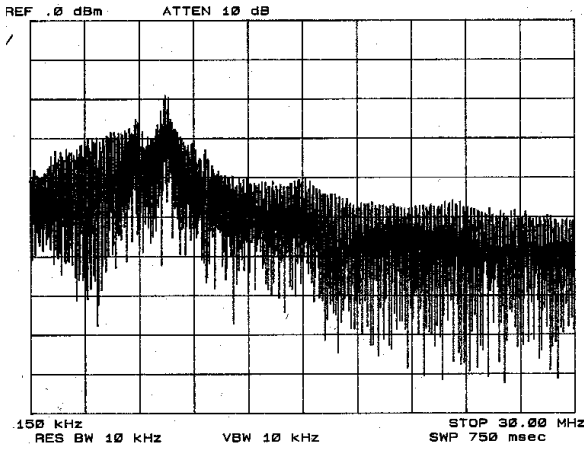
Since sharp spikes, or impulses, have very rich high frequency components, CM noise is much larger than DM noise in high frequency range. This is seen in Fig. 3.19 (b) and (d). However, Comparing Fig. 3.19 (a) and (c), it is clearly seen that DM noise dominate the low frequency range. Comparing the high frequency DM noise in Fig. 3.19 (d) with the DM noise in Fig. 3.10 (b), we can find DM noise is greatly reduced for the frequency above 15MHz. However, for the frequency range from 3MHz to 15 MHz, Fig. 3.19(d) is slightly higher than that in Fig. 3.10 (b).

For common mode noise reduction, adding high frequency capacitors is not effective. This is verified if we compare Fig. 3.19 (b) with Fig. 3.10 (a). There is no reduction in CM noise spectrum. And unfortunately, a small spike appears at about 7MHz, which corresponds to the ringing in the CM noise voltage at LISN.

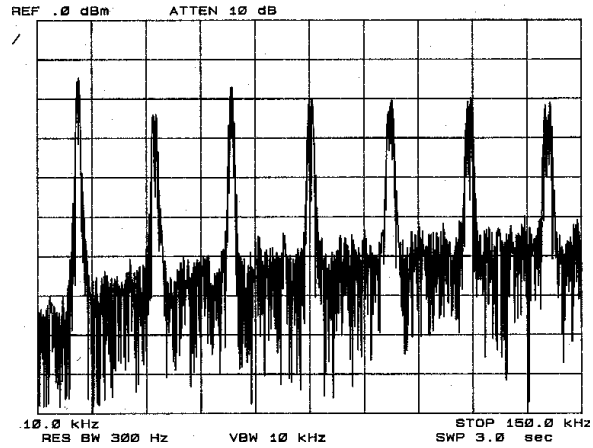
We need other method to deal with CM noise. Soft switching is a possible solution.



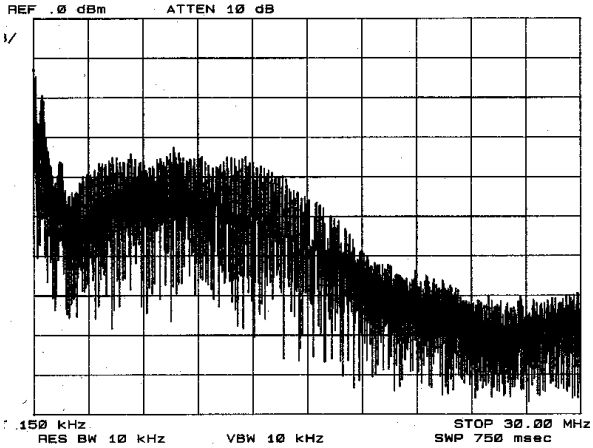
(a) CM noise, 10kHz ~ 150kHz



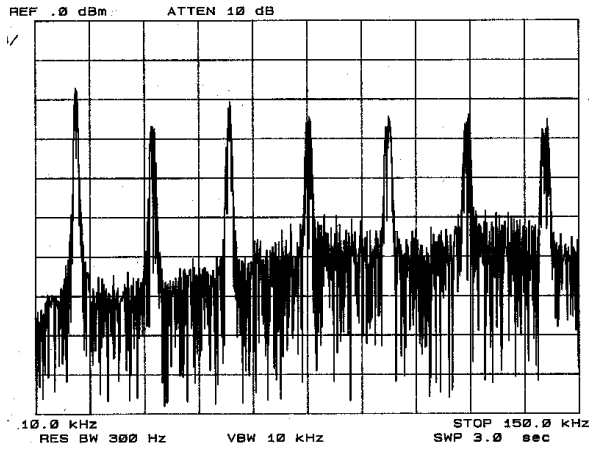
(b) CM noise, 150kHz ~ 30MHz



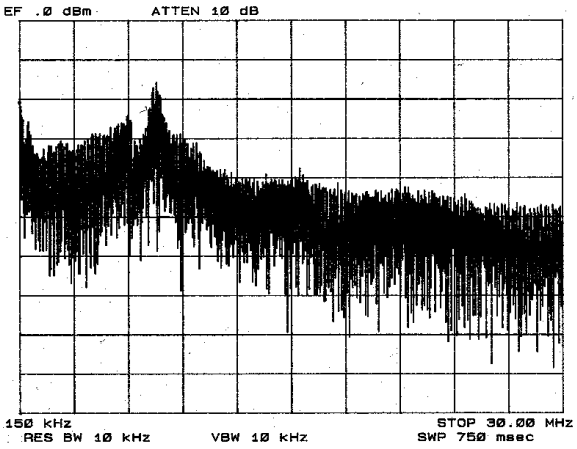
(c) DM noise, 10kHz ~ 150kHz



(d) DM noise, 150kHz ~ 30MHz



(e) Total noise, 10kHz ~ 150kHz



(f) Total noise, 150kHz ~ 30MHz

Fig. 3.19 Hard-switching inverter EMI spectra

3.3 Implementation and EMI characterization of a resonant snubber inverter

3.3.1 Operation Principle

The resonant snubber inverter (RSI) is shown in Fig. 3.20. Four snubber capacitors and one resonant branch are added to the hard-switching inverter and make it a resonant snubber inverter, which can achieve zero voltage turn-on (ZVT) of main switch and zero current turn-off (ZCT) of auxiliary switch. SA1,SA2 are two IGBTs in half-bridge module. DA1, DA2 are fast reverse recovery diode.

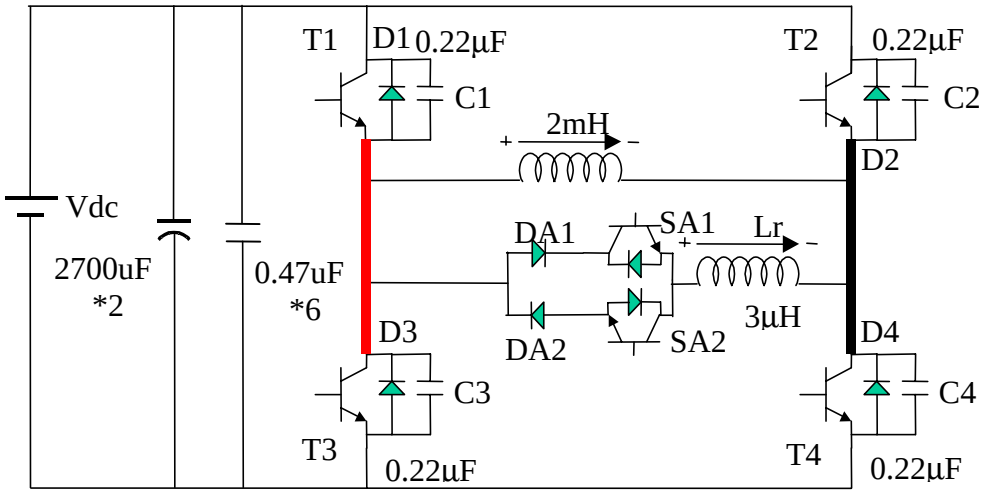


Fig. 3.20 Single-phase full-bridge resonant snubber inverter

The principle of the circuit operation is simple. The idea is that before turn on each main switch, the relevant auxiliary switch should be turned on first. Thus the resonance between the resonant inductor Lr and all the snubber capacitors would make the corresponding pair of snubber capacitors fully discharged, and the main switch can turn on at zero voltage condition.

The relevant waveform and timing sequence is illustrated in Fig. 3.21. Assume the load current is in positive direction. T2, T3 are on, but the load current is flowing through anti-parallel diode D3 and D2. The objective is to realize zero voltage turn on of T1 and T4.

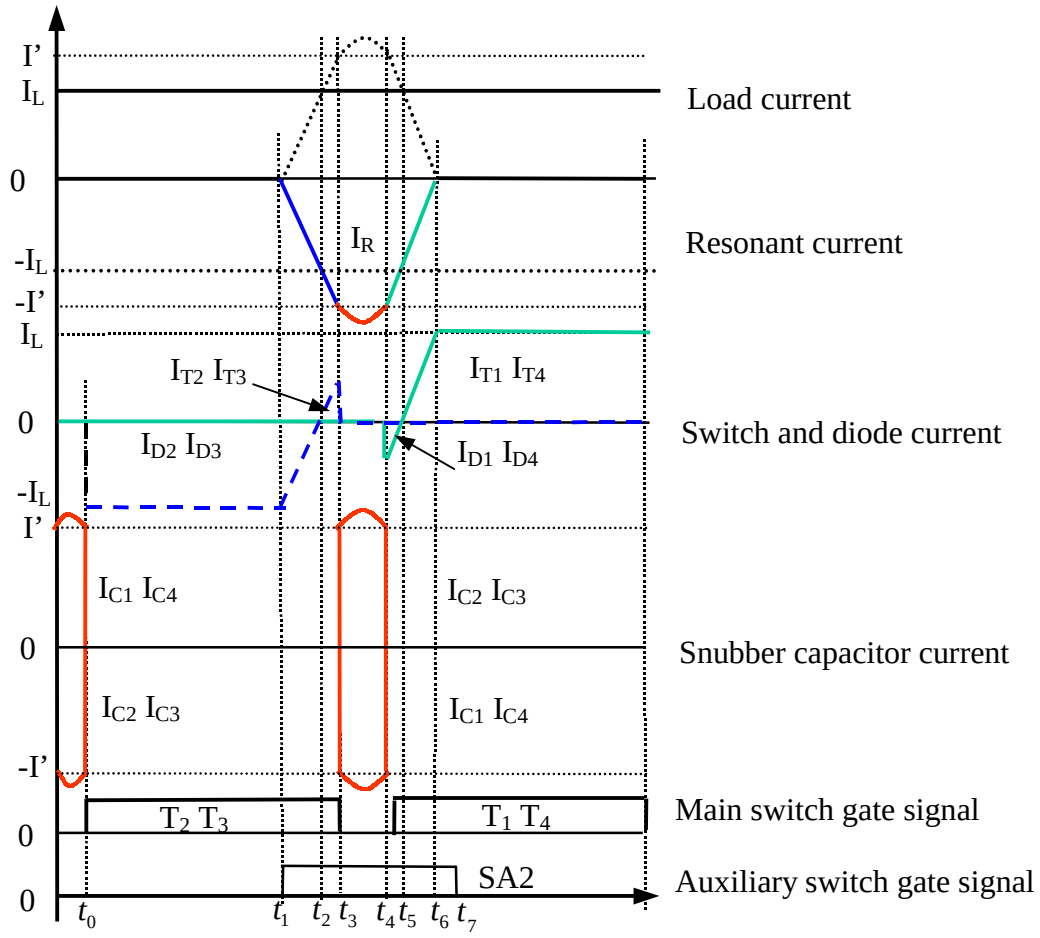


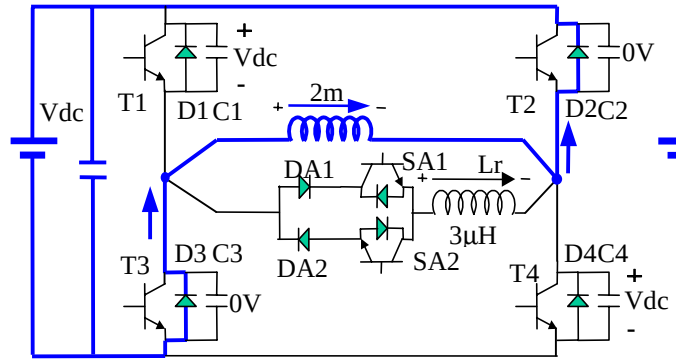
Fig. 3.21 Time sequence and operational waveform of resonant snubber inverter

The detailed operation modes are illustrated in Fig. 3.22.

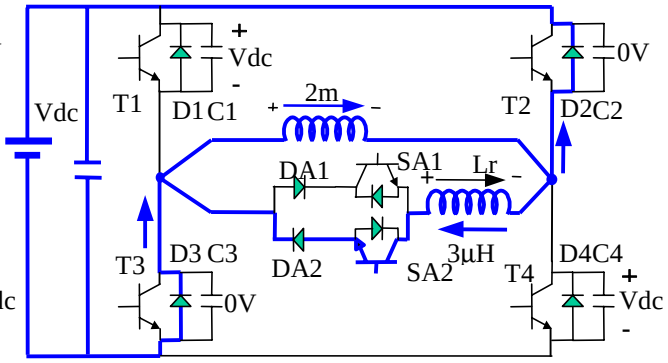
Since load current is 200Hz, whereas the switching frequency is 20kHz. During the period of interesting, the load inductor can be viewed as a current source, and the load current can be viewed as constant.

Mode 0: $I_r = 0$, $(t_0 - t_1)$

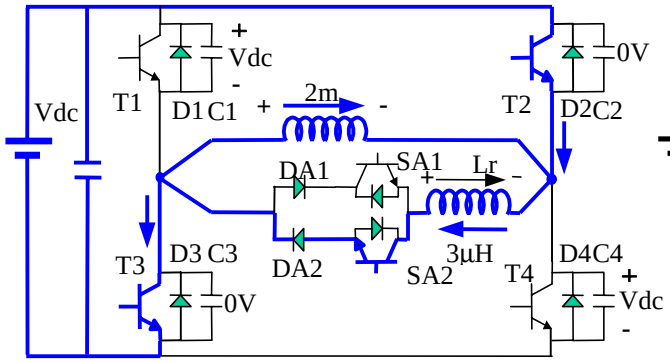
T3 and T2 are on; T1 and T4 are off. Load current is flowing through anti-parallel diode D3 and D2. The auxiliary switch SA1 and SA2 are off. Resonant current is zero. Since D3, D2 are in conduction and T1, T4 are off, C3, C2 are shorted and C1, C4 are fully charged to the dc bus voltage. This is shown in Fig. 3.22 (a).



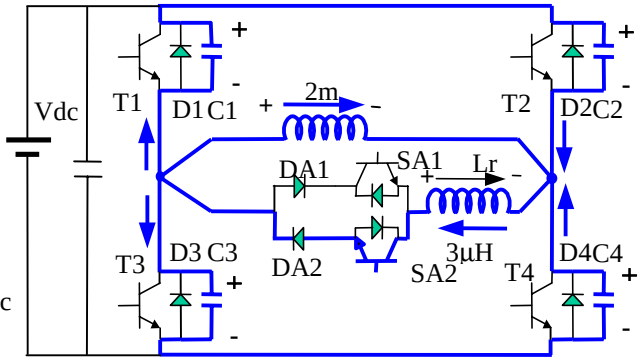
(a) Mode 0



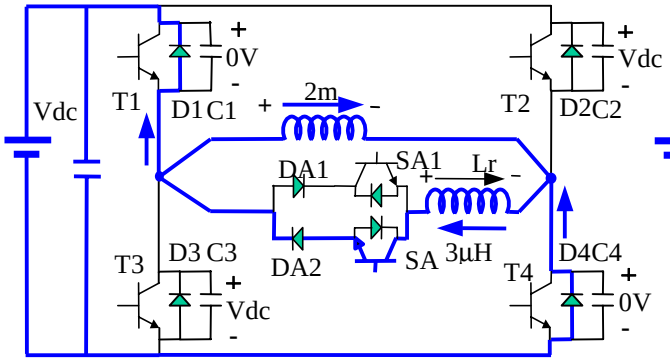
(b) Mode 1



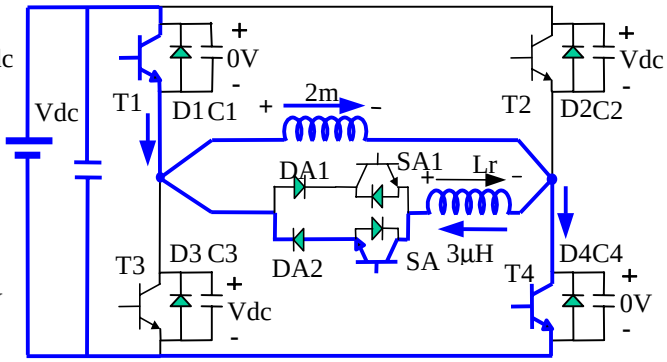
(c) Mode 2



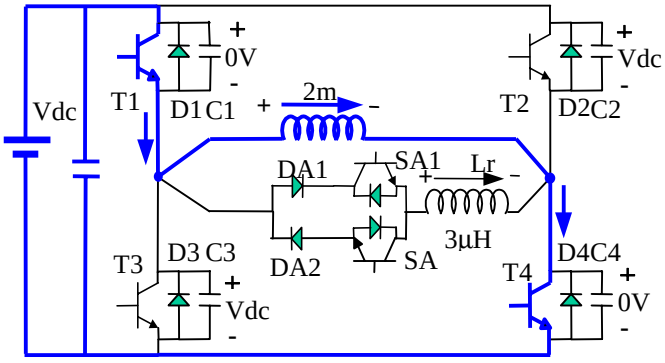
(d) Mode 3



(e) Mode 4



(f) Mode 5



(g) Mode 6

Fig. 3.22 Resonant snubber inverter operation mode

Mode 1: $0 < I_r \le I_L;\ (t_1 - t_2)$

Before turn off T2, T3, turn on SA2 first. Thus, the dc bus voltage is applied directly to the resonant inductor Lr, and Ir is linearly charged up from zero at the rate Vdc/Lr. Meanwhile, the current in D3 and D2 decreases at the same rate. Hence, load current is diverted from D3 and D2 to the resonant branch. The current path is shown in Fig. 3.22 (b). The current in D2 and D3 reduce to zero by t_2 when the resonant current equals the load current.

Mode 2: $I_L < I_r \le 2 \cdot I_L,\ (t_2 - t_3)$

When the resonant current equals the load current, the current in D2 and D3 becomes zero, and D2, D3 turn off naturally. Since T2 and T3 are still on, current is converted to switch T2, T3, and inductor current keep increasing. Switch T2 and T3 will be turned off at t3 when the resonant inductor has stored sufficient energy to discharge C1 and C4.

Mode 3: $(t_3 - t_4)$

T2 and T3 are turned off at T3. Then Lr resonates with all the snubber capacitors. Current flows out off C1, C4 and flows into C2, C3 as indicated in Fig. 3.22 (d). Thus the voltage across C1, C4 decrease and the voltage across C2, C3 increase. By the time of t_4, C1, C4 are completely discharged and the voltage across T1, T4 become zero; C2, C3 are fully charged and the voltage across T2, T3 become Vdc.

Mode 4: $(t_4 - t_5)$

The resonant inductor is sufficiently charged in Mode 2, and Ir will flow continuously for a short period. Thus, D1 and D4 will conduct. The voltage of the mid-point of T1 and T3 will then be clamped to the bus voltage by D1. The voltage of the mid-point of T2 and T4 will then be clamped to the ground voltage by D4. During this short period, since D1 and D4 are in conduction, T1 and T4 can be turned on at zero voltage condition.

Mode 5: $(t_5 - t_6)$

The current flowing in D4 and D1 is quickly reduced to zero. The resonant inductor current is equal to the load current at this moment. Since T1, T4 is already on, Vdc is applied to the resonant inductor in an opposite direction. The resonant inductor current decreases continuously at rate Vdc/Lr. The current flowing in T1, T4 increases at the same rate. However, the load current keeps constant. In other words, the resonant current is diverted back to load current. All these will keep going until the resonant inductor current reduces to zero and the current flowing in T1, T4 equals to the load current.

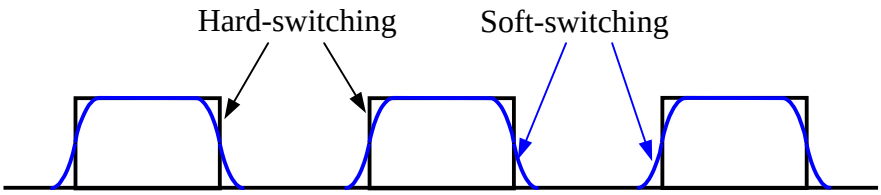
Mode 6: $(t_6 - t_7)$

After t_6, DA2 blocks the resonant inductor current from flowing inversely and the auxiliary switch can be turned off at zero current condition at t_7.

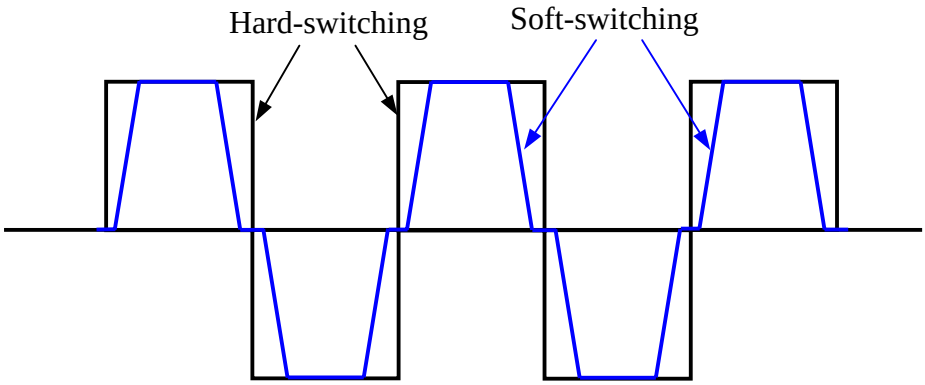
If the initial load current is in the negative direction and its magnitude is large enough, then the load current itself can fully discharge the snubber capacitors C4, C1 within the dead time. Therefore T1, T4 can turn on at zero voltage condition without the help of resonant current. If the load current is not large enough to discharge C1, C4 by itself, then resonant current is necessary to assist realizing zero voltage turn-on of T1, T4.

If resonant current is less than enough, the zero voltage turn-on may not be achieved. If resonant current is more than enough, the loss and noise may be increased. Since load current is sinusoidal, at different switching moment, the load current level is different. Therefore, the magnitude of resonant current should be determined according to the load current level, which requires a variable charging time of the resonant inductor. This will be discussed in the Appendix.

With soft switching, the dv/dt of the mid-point of T1, T3 and the mid-point of T2, T4 can be reduced. The di/dt of the dc bus current also can be reduced. This is shown in Fig. 3.23



(a) The dv/dt of the mid-point of each leg is reduced



(b) The di/dt of the dc bus current is reduced to Vdc/Lr

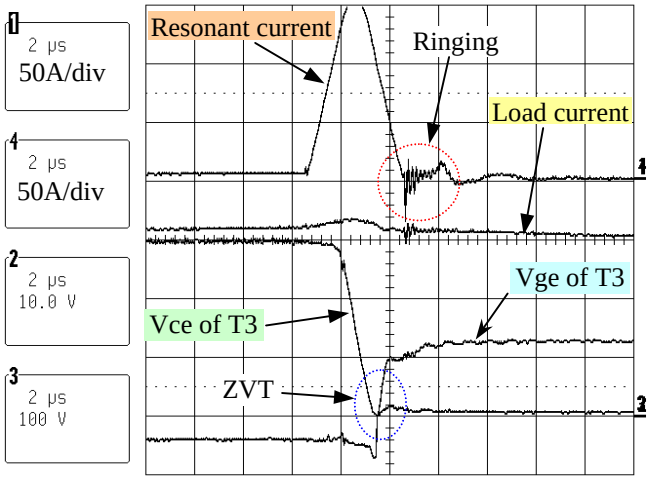
Fig. 3.23 dv/dt and di/dt of the inverter is reduced by soft-switching

The most important is the diode reverse recovery problem of main switch has been avoided. Since the inverter dv/dt and di/dt was reduced, a better EMI reduction was thus expected. However, the improvement in the initial test was limited.

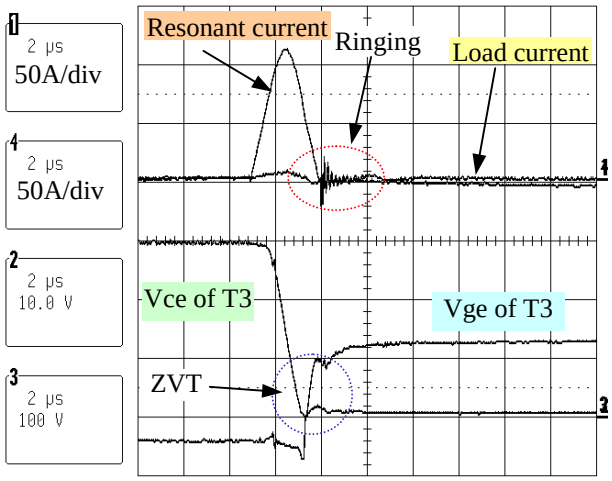
3.3.2 Current ringing in the resonant snubber circuit

The switching transition of the resonant snubber inverter is shown in Fig.3.24. The referenced positive direction of load current and resonant current is the same at that shown in Fig. 3.20. Due to the tight connection, the switch current can not be measured directly by current probe. An alternative method is adopted to verify ZVT. From Fig.3.24 (a) (b) (c) it is seen that

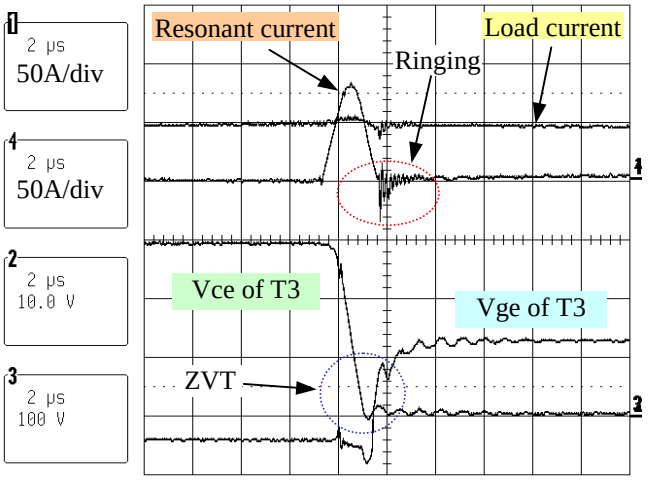
the gate signal is applied after Vce dropped to zero. This means zero voltage turn on is achieved. Moreover, at different load current level, the magnitude of resonant current is also different. This shows the effect of the variable charging time control. The dv/dt of main switch is reduced to 200V/μs. However, the resonant current turn off is not smooth, a high frequency ringing is generated at its turn off.



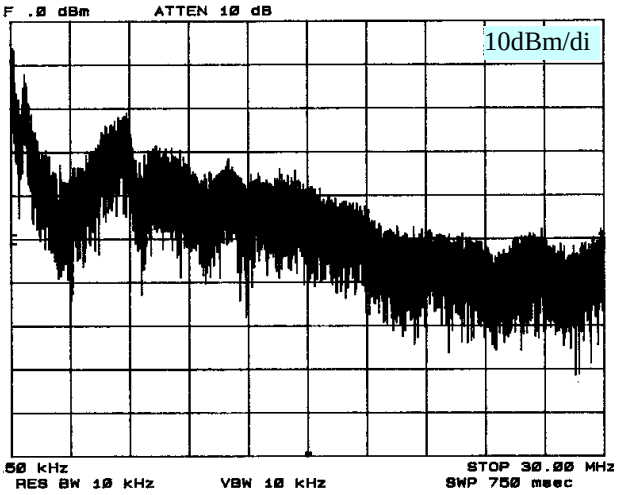
(a) Load current at negative maximum



(b) Load current cross zero



(c) Load current at positive maximum



(d) Corresponding Total noise spectrum

Fig.3.24 Switching transition of resonant snubber inverter

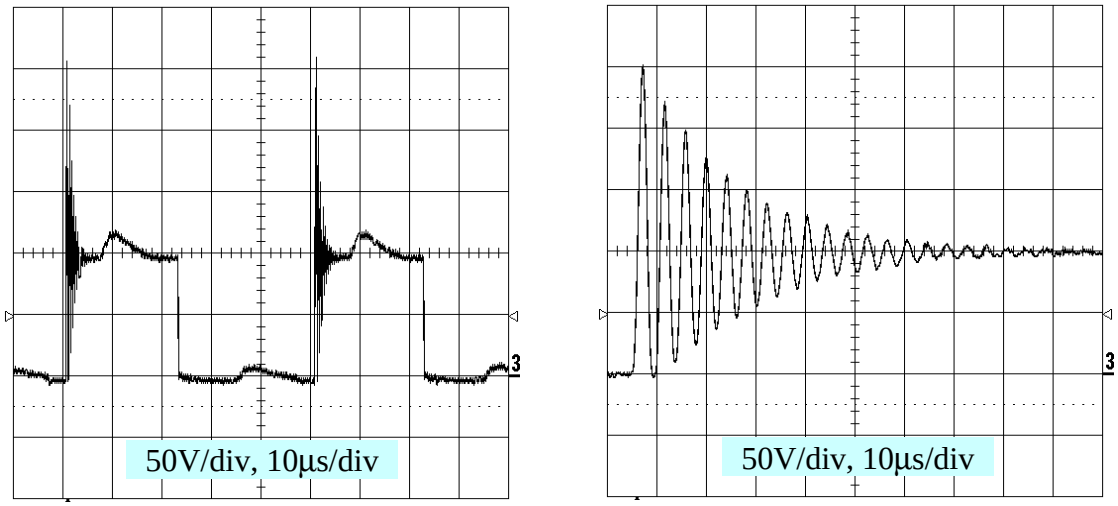
The total noise spectrum of soft switching is shown in Fig.3.24 (d). Comparing this spectrum with that of hard switching in Fig.3.13 and Fig.3.19 (f), it can be seen that the envelopes of the total noise spectrum of soft switching has only a slight reduction than hard switching. It is even worse at 6 MHz due to the ringing in the resonant current.

The reason for this ringing can be explained as follows. Assume that the resonant current is charged through T1 $\rightarrow$ DA1 $\rightarrow$ SA1 $\rightarrow$ Lr $\rightarrow$ T4. Main devices T1 and T4 are turned off after Lr is sufficiently charged, and then the resonant current in Lr begins to charge C1, C4 and to discharge C2, C3. This is all within the resonant period. When the voltage of the mid-point of T1, T3 equals the voltage of the mid-point of T2, T4, the voltage across the resonant inductor becomes zero and the resonant current reaches its peak. After this, the voltage across Lr is reversed and the resonant current starts decreasing. When the voltages of C2 and C3 drop to zero or negative, the diode across T2 and T3 turn on, and then T2 and T3 can be turned on at zero voltage condition. After T2 and T3 are turned on, the resonant inductor current continues decreasing. When the resonant current drops to zero, it would not stop instantaneously because diode DA1 requires a finite time for reverse recovery. Therefore, the current in Lr is increased in the reverse direction, with a current from the mid-point of T2 and T4 to the mid-point of T1 and T3. In addition, due to the output capacitance of switch SA2, this inductor current resonates at a frequency near 6 MHz as indicate in Fig.3.24 (d).

3.3.3 Voltage ringing in the resonant snubber circuit

Not only current ringing is found in the circuit, but also voltage spike is observed in the initial test, at the cost of several auxiliary devices.

The voltage ringing across the auxiliary switch is shown in Fig.3.25. These waveforms were obtained when the dc bus voltage was lowered to 100V to secure no over voltage upon the switch.



(a) (b)

Fig.3.25 Voltage ringing across auxiliary switch

From Fig.3.25 it is seen the magnitude of the voltage spike is 250V, 2.5 times the dc bus voltage, which is merely 100V. Therefore, if the dc bus voltage is raised to 300V, the voltage spike could be more than 600V. This is even dangerous to the safety of the device, let alone to reduce EMI emission.

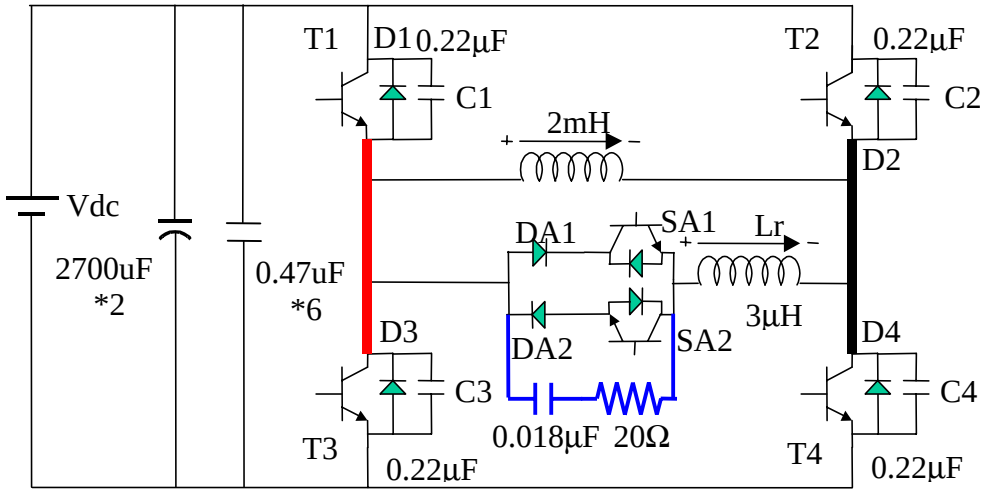
Effect of snubber in resonant branch

A normal way to reduce the voltage spike is to add RC snubber to the auxiliary switch. The circuit and its effect are shown in Fig.3.26

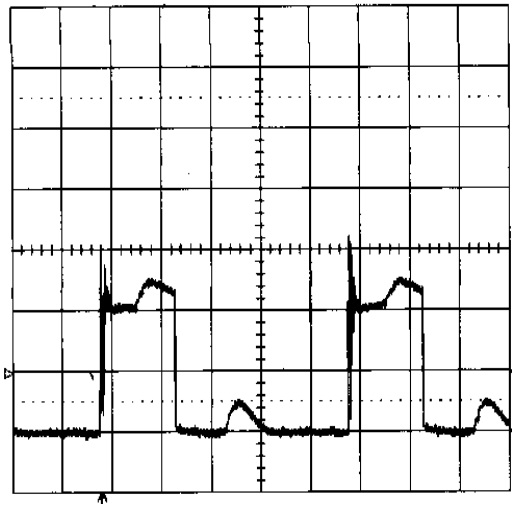
It is seen that after adding RC snubber, the magnitude of the voltage spike is reduced from 250V to 150V when the dc bus voltage is 100V. Although the RC snubber has certain

effect to reduce voltage spike, the voltage ringing has not been eliminated. Moreover, the snubber circuit introduces more energy loss, which ruins the benefits of soft switching.

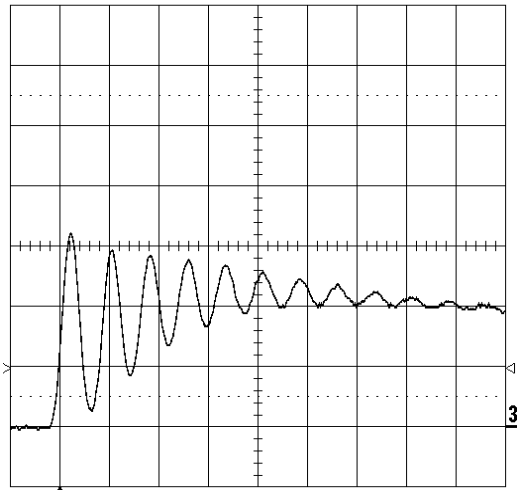
Other methods need to be investigated to deal with the ringing in the circuit.



(a) Snubber in the resonant branch



(b) 50V/div, 10μs/div



(c) 50V/div, 0.2μs/div

Fig. 3.26 Voltage ringing in reduced by snubber capacitor

Effect of saturable inductor

Saturable inductor could also be a solution to the ringing. A saturable inductor is connected in series with the resonant inductor, and the resonant inductor is adjusted to 1μH, accordingly. The circuit is shown in Fig.3.27. A test at 100V dc bus was conducted to check the effect. The voltage of auxiliary branch is shown in Fig.3.28.

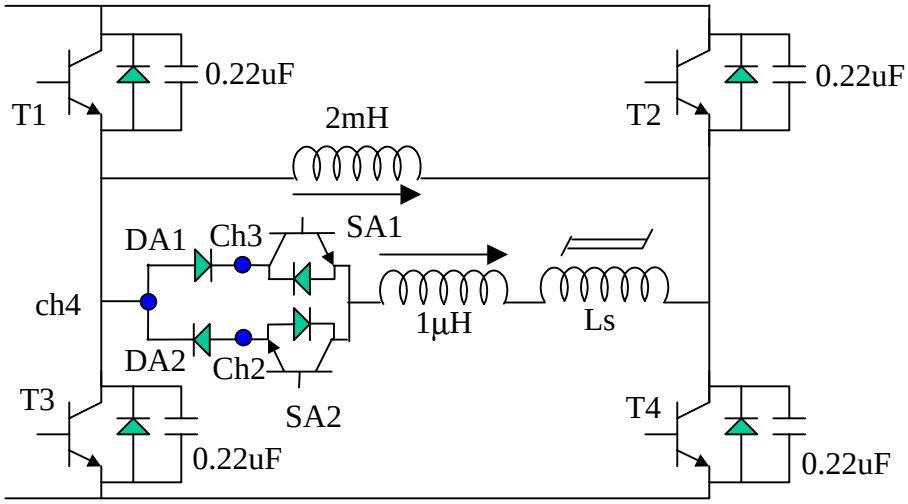


Fig.3.27 Saturable inductor is added to the auxiliary branch

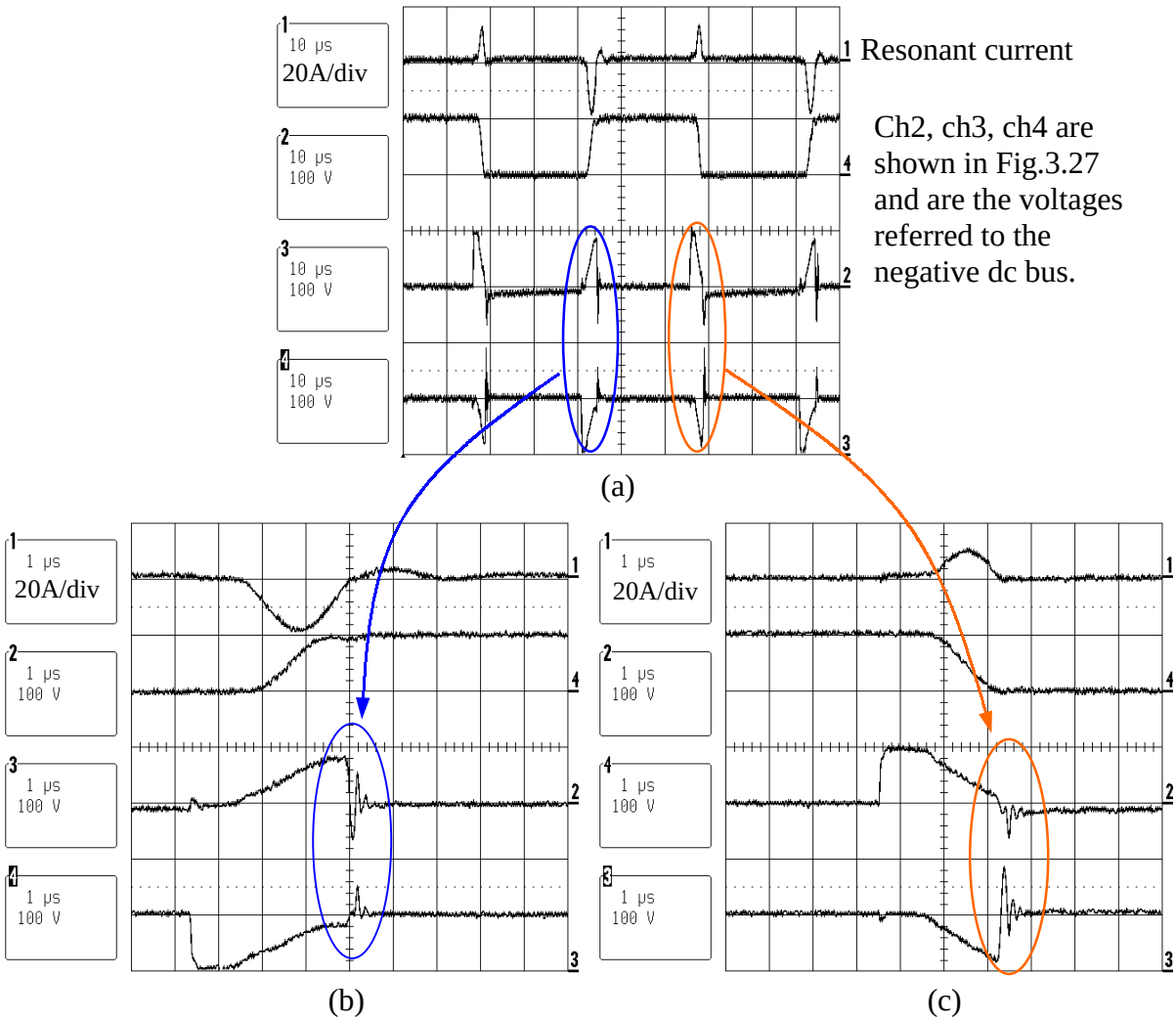
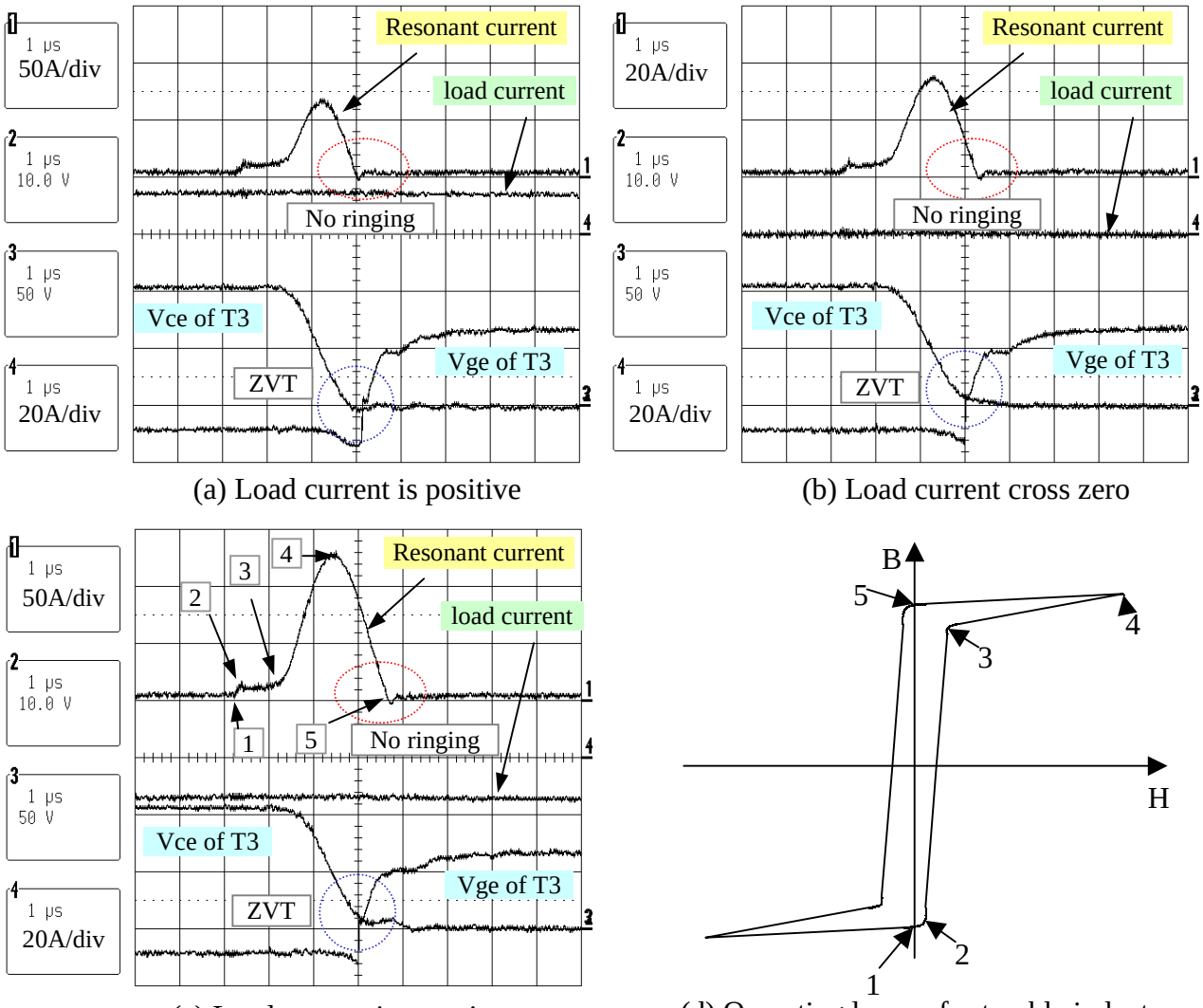


Fig.3.28 Voltage ringing in resonant branch is reduced by saturable inductor

It can be seen from Fig.3.28 that the voltage spike in the resonant circuit is reduced after adding saturable inductor. The amount of ringing reduction is similar to that of using RC snubber. Moreover, using saturable inductor can also eliminate the current ringing occurred at turn-off of resonant current. This is shown in Fig.3.29.



(a) Load current is positive

(b) Load current cross zero

(c) Load current is negative

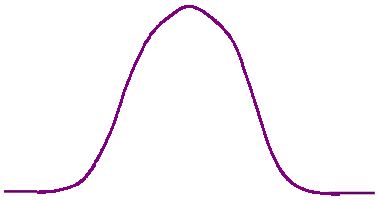
(d) Operating locus of saturable inductor

Fig.3.29 Current ringing is eliminated after adding saturable inductor

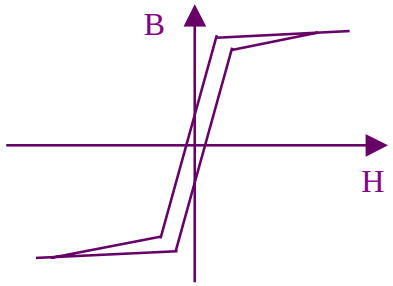
It is clearly shown in Fig.3.29 that the current ringing is eliminated and zero voltage turn-on is still maintained at various load current level.

Compare the resonant current waveform in Fig.3.29 (c) and the B-H of the saturable inductor in Fig.3.29 (d), we can find that they are closely related with each other. Point 1 corresponds to the instant of auxiliary switch turn-on. At this moment, the saturable inductor is still in saturation, the instant permeability is small and the inductance is small. Therefore a larger di/dt is seen in the initial part of the resonant current. At point 2, the operating point moves out of saturation part, the permeability becomes very large and the inductance is very large. Thus, from point 2 to point 3 the resonant current becomes flat, di/dt is reduced. From point 3 to point 4 the saturable inductor is saturated, its inductance becomes very small. The di/dt is mainly determined by the resonant inductor during this period. From point 4 to point 5, the operating point is still in saturation part of the B-H curve. Particularly at point 5, since the resonant inductor is still saturated, it doesn't help limit di/dt at this turn-off moment.

The expected resonant current waveform should have small di/dt at turn on and turn off, which is shown in Fig.3.30.



(a)Preferred shape of Ir



(b)Preferred B-H curve of saturable inductor

Fig.3.30 Preferred resonant current shape and resonant inductor B-H curve

To obtain small di/dt at resonant current turn on and turn off, a high initial permeability is required for the saturable core. In addition, a low saturation flux density, a narrow hysteresis loop of the saturable core can reduce the magnetic loss. These characteristics are not easily found in nowadays saturable core.

Although saturable inductor has good effect in reducing current and voltage ringing in the resonant branch, it cause much loss, which makes it not suitable for high power application.

Effect of splitting inductor

In order to suppress the ringing of the resonant current at its turn off, we split the resonant inductor in two. The modified circuit is shown in Fig.3.31. With 100 V dc bus voltage, test results are shown in Fig.3.32. It can be seen that the resonant current turn-off becomes smooth, and the high frequency ringing is eliminated.

An explanation of the suppression of the ringing is as below.

Assume the resonant current is charged through T1 $\rightarrow$ Lr1$\rightarrow$ DA1 $\rightarrow$ SA1 $\rightarrow$ T4. Main devices T1 and T4 are turned off, and then the resonant current in Lr1 begins to charge C1, C4 and to discharge C2, C3. When the voltage at the mid-point of T1 T3 and the voltage at the mid-point of T2 T4 reached half of the DC bus voltage, the polarity of the voltage across the resonant branch reverses, and the magnitude of the voltage increases as the voltage across C1 and C4 charges up. In this case, the voltage across the output capacitor of SA2 is charged to dc bus voltage before T2 and T3 are turned on at zero-voltage condition. Therefore, there is no high frequency ringing between Lr2 and the output capacitance of SA2 after DA1 rings back from reverse recovery.

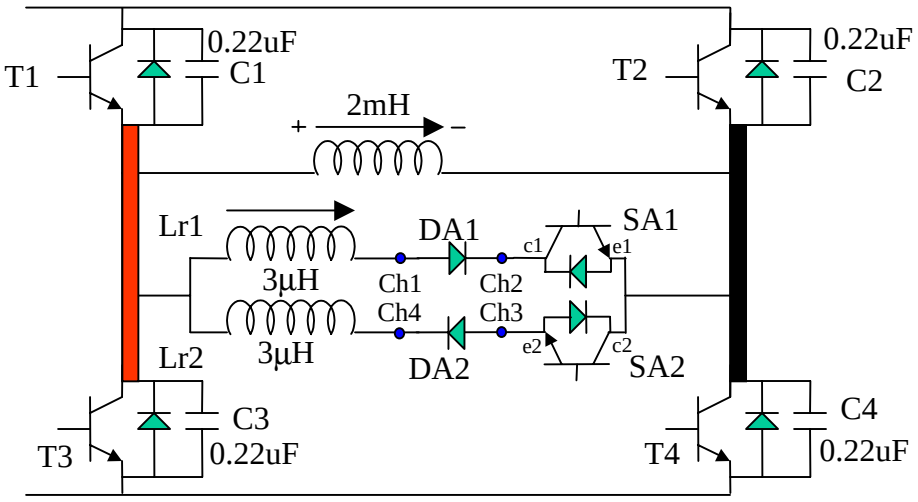
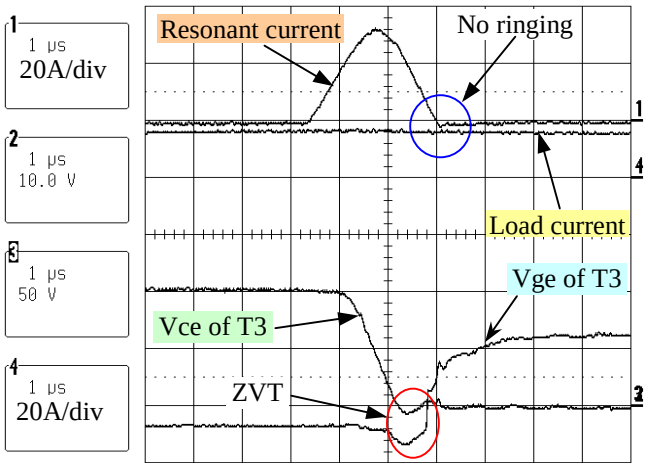
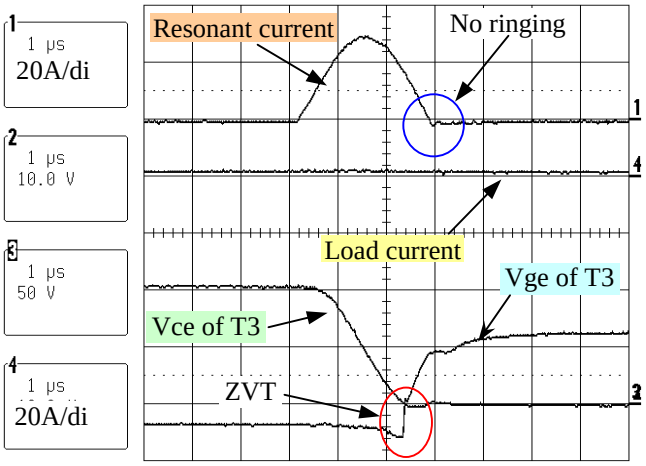


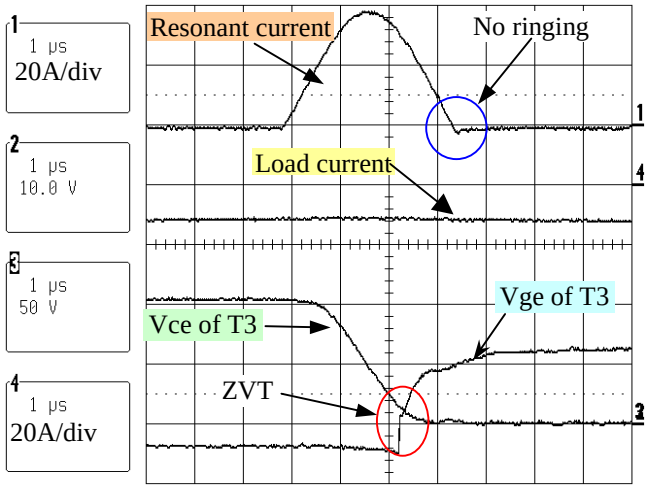
Fig.3.31 Split resonant inductor in the soft-switching inverter



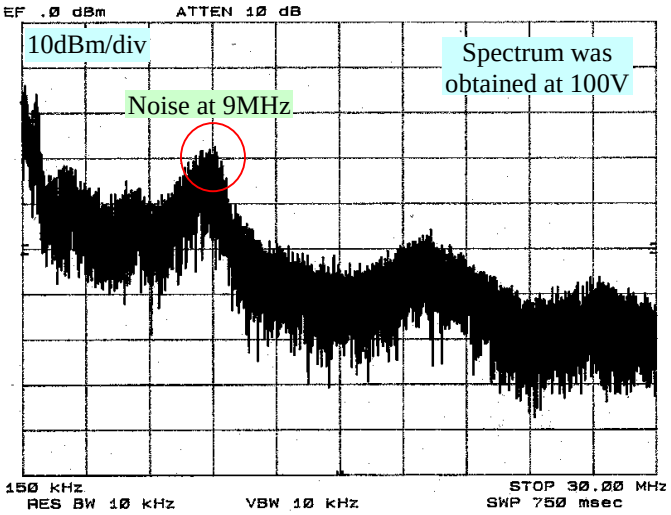
(a) Load current reached positive maximum



(b) Load current crossed zero



(c) Load current reached negative maximum



(d) Total noise spectrum

Fig. 3.32 Clean resonant current after split resonant inductor

Comparing the case of single resonant inductor and the case of split resonant inductors, it can be seen that the resonance between the resonant inductor and the parasitic capacitance across auxiliary switches SA1 and SA2 are the major noise sources. In Fig.3.20, when DA1 and SA1 are in conduction, the voltage across DA2 and SA2 are almost zero. After T2 and T3 turn on, the voltage across the auxiliary branch reverses. SA2 has to block the bus voltage. Thus, the voltage of the output capacitor of SA2 has to be charged up to the bus voltage while DA1 is blocking the inversely charged current of Lr. Therefore, the resonance between Lr and the output capacitor of SA2 starts with an initial condition that voltage across the capacitor is zero and the current of the inductor is small. The equivalent circuit and the state plane are shown in Fig.3.33 where Cout is the equivalent output capacitor of the auxiliary switch.

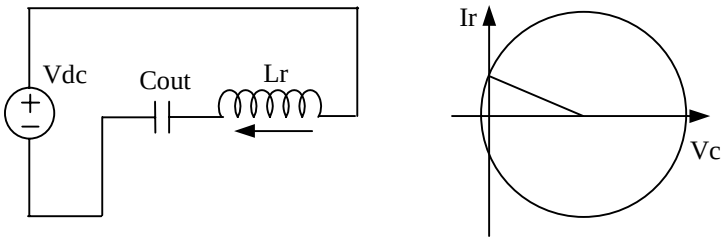


Fig. 3.33 Equivalent circuit and state plane of the resonance

For the case of split resonant inductors, the voltage across the output inductor of SA2 is slowly built up with the resonance between Lr1 and C1 ~ C4. Hence, when T2 and T3 turn on, the voltage across SA2 is already equal to the DC bus voltage. There is no voltage to charge Lr2, and the resonance between Lr2 and the output capacitor of SA2 is eliminated. However, the current inversely charged in Lr1 will find its path and cause ringing in the circuit.

The corresponding total EMI noise spectrum after splitting resonant inductor is shown in Fig.3.32 (d). In this spectrum, the 6 MHz peak shown in the previous parasitic ringing is

reduced by 20 dB, but a 9 MHz peak appears. This peak is related to the voltage ringing at the anode of DA2 and the cathode of DA1. Due to diode reverse recovery, for example, during the charging period, the resonant current is charged through T2 → SA2 → DA2 → Lr2 → T3. Devices T2 and T3 turn off after the current is sufficiently charged, and then inductor Lr2 resonates with C1 ~ C4. When the voltages of C1 and C4 drop to zero, T1 and T4 can be turned on at zero-voltage. Then Vdc applied to Lr2 from the mid-point of T1 and T4 to the mid-point of T2 and T3. The current in Lr2 decreases to zero but increases inversely because diode DA2 enters the reverse recovery period. When diode DA2 regains its blocking capability, the inversely charged Lr2 resonated with the junction capacitor of DA2 and voltage ringing was thus generated with a 9 MHz frequency.

The splitting inductor can eliminate current ringing, but it is not effective to reduce voltage ringing caused by diode reverse recovery in the resonant branch. The voltage ringing in the resonant circuit is shown in Fig.3.34. These voltages were measured at points ch1, ch2, ch3, and ch4, shown in Fig.3.31, with respect to the negative DC bus. This kind of ringing, coupling through the parasitic capacitance between the circuit and the ground, becomes a severe common mode noise source.

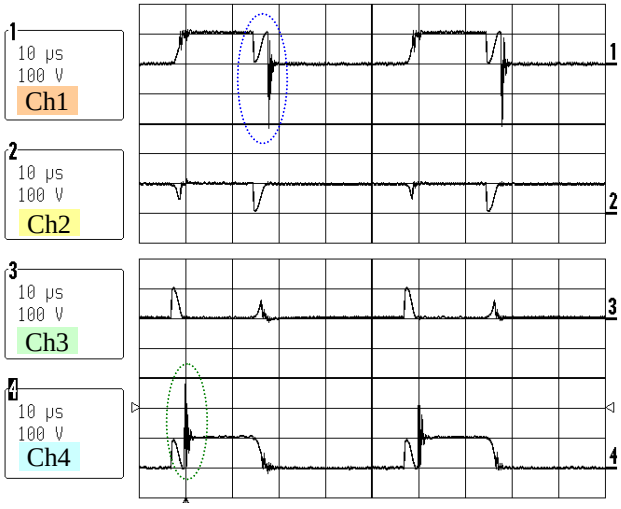
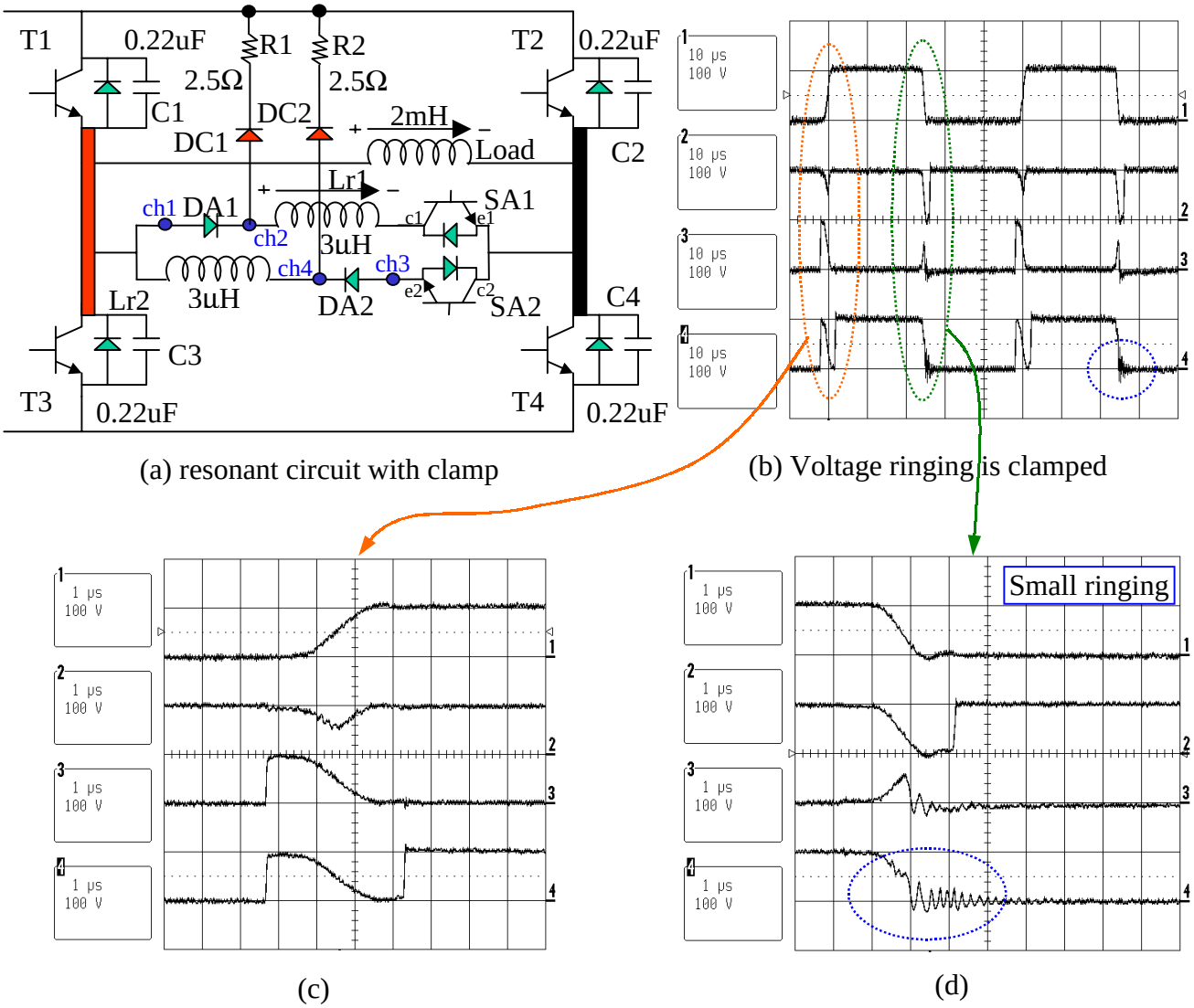


Fig.3.34 Voltage ringing in the resonant branch after splitting resonant inductor

Use clamp circuit to suppress voltage ringing

Knowing that the voltage ringing is caused by the inversely charged resonant inductor current during the diode reverse recovery period, a simple clamp circuit is adopted along with split resonant inductor to deal with the voltage ringing . Several topology have been tested and finally the one shown in Fig.3.35 (a) is found best to serve the purpose.



(a) resonant circuit with clamp

(b) Voltage ringing is clamped

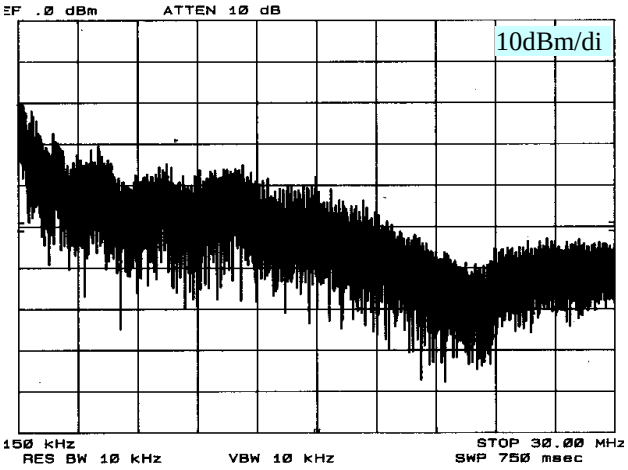
(c)

(d)

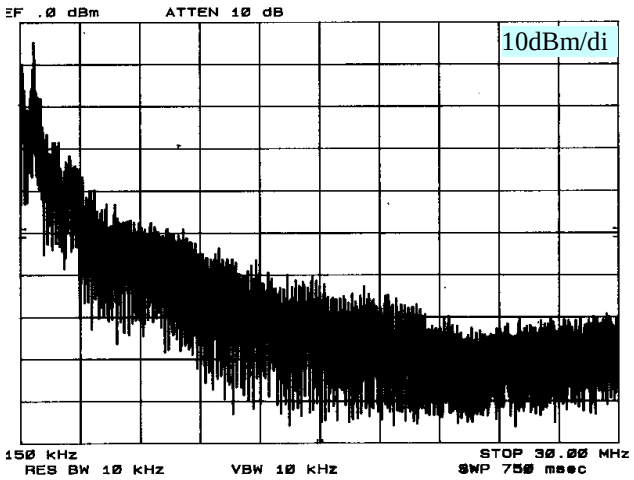
Fig.3.35 Soft-switching with clamp in the resonant branch

The clamp circuit provides a free path for the inversely charged current in the resonant inductor, and therefore the resonance between the resonant inductor and the diode junction capacitor is avoided. For Lr1, the path is along DC1, T2 and the anti-parallel diode of SA1. For Lr2, the path is along DC2 and T1. In Fig.3.35 (b), (c) and (d), the voltages are measured with respect to the negative dc bus. The measured points are shown in Fig.3.35(a). These figures show that the voltage ringing in the resonant branch has been significantly suppressed.

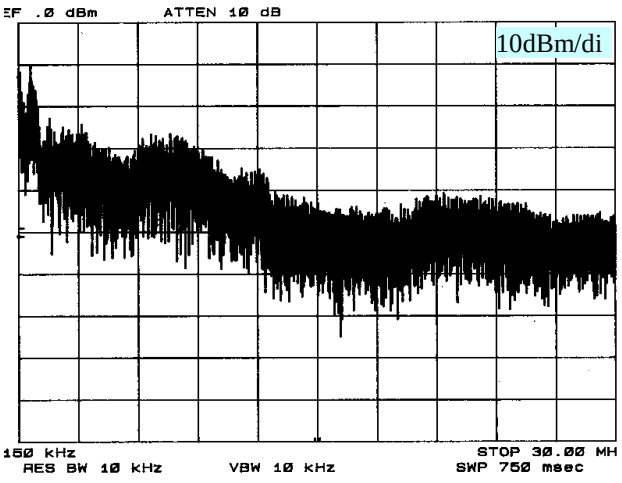
The noise spectra, measured at 300 V DC input and 50 A peak load current, are shown in Figs. 3.36 (a), (b) and (c) for common mode, differential mode, and total noise, respectively.



(a) CM noise spectrum



(b) DM noise spectrum



(c) Total noise spectrum

Fig. 3.36 EMI spectrum of soft switching with clamp

Comparing the EMI measurement result shown above with those of hard switching shown in Fig.3.10 and Fig.3.19, it can be seen that, in general, the conductive noise emission generated by soft-switching inverter is slightly lower than that generated by hard-switching in most of the concerned frequency range (150 kHz ~ 30 MHz). But at the frequency around 700 kHz, the noise of soft-switching topology is higher than that of hard-switching scheme. This will be explained below. Since the total noise is composed of CM noise and DM noise, it is necessary to compare them separately for different switching schemes.

For a hard-switching scheme, the DM noise is peaking at a frequency less than 2 MHz, whereas the CM noise dominates the frequency range from 2 MHz to 12 MHz. For the frequency range from 12 MHz to 30 MHz, the emissions of CM noise and DM noise are comparable. However, if high frequency capacitors are properly used, the DM noise is even lower than CM noise in this frequency range. Generally, the total noise is determined by the CM noise for most of the concerned frequency range.

For soft-switching topology, it is the same that the DM noise dictates the noise emission at the frequency less than 2 MHz. The difference is that for frequencies from above 2 MHz to 30 MHz, the CM noise is always higher than DM noise.

Comparing the CM noise, less noise was generated by the soft-switching scheme than by the hard-switching scheme, though not as low as what is expected. The peak in the CM spectrum occurred at a different frequency range. This is because in the soft-switching scheme, the snubber capacitors slow down the rising voltage speed when the main switches turn off, thus less common mode current is generated through the parasitic capacitance of the main switches during their turn-off. Although the CM noise generated by the main switches was decreased, the resonant branch also generated some common mode noise. As explained previously, the reverse

recovery of diodes in the resonant branch caused high frequency voltage ringing. This voltage ringing, coupled through the parasitic capacitance between the circuits and ground, generated some CM noise. This means the diode reverse recovery problem of the main switch is now shifted to the auxiliary branch, although it is not as severe as in the hard-switching condition. This is an important issue that needs to be dealt with.

For DM noise, it is obvious that the DM noise emission of soft-switching scheme is significantly reduced in the frequency range of 2 MHz to 30 MHz than that of hard-switching scheme. However, the spike at 700 kHz is much higher than that in hard-switching noise spectrum. As we know, the high di/dt is the DM noise source. But the high di/dt, introduced by the reverse recovery of the anti-parallel diode of the main switch, is already reduced with the application of ZVT. Why is there still a high spike in the spectrum? One answer is the high magnitude resonant current. In the hard-switching scheme, the peak value of the load current was 40 A, and even considering the diode reverse recovery, the current overshoot was about 100A. However, in the soft-switching scheme, the highest resonant current could be more than 150 A. Although the di/dt is not as high as that in hard-switching, the energy of noise emission is still high. This explanation prompts that a precise variable timing control of the resonant current is necessary to limit the noise emission.

RSI with a simplified resonant branch

A resonant snubber inverter with simplified resonant branch is shown in Fig.3.37. The two auxiliary switches are 600V/75A MCTs, which have lower turn-on voltage drop and higher capability to withstand burst current. These characteristics make MCT very suitable to handle resonant current. The two diodes DA1 and DA2 are fast reverse recovery diodes. They serve

two purposes, blocking the resonant current from flowing inversely and protecting the MCT from reverse over voltage. DC1 and DC2 also provide easy paths for the resonant current charged during DA1 and DA2 reverse recovery period, thus voltage ringing is avoided. For the current charged during DA1 reverse recovery period, the free wheeling path is DC1, T2,DA2 and Lr. For the current charged during DA2 reverse recovery period, the free wheeling path is DC2, T1, DA1 and Lr. 15 Ω resistor is inserted in each clamp to damp high frequency ringing. A very small snubber capacitor is connected in parallel with each MCT to reduce high dv/dt at turn off.

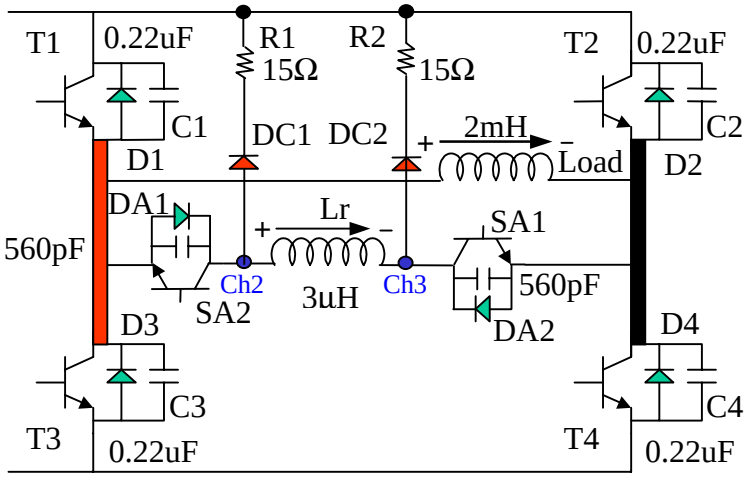


Fig.3.37 Resonant snubber inverter with a simplified auxiliary branch

To compare with the noise generated in hard switching, the noise voltage across LISN is also investigated while soft switching. The noise waveform was obtained while the inverter working at 300 V dc bus voltage and 50A load current.

Total noise voltage across LISN

Fig.3.38 shows the waveform of the total noise voltage across LISN. Fig.(a) shows total noise voltage in four cycles. Fig.(b) shows one cycle noise in Fig.(a), in more detail. Figs.(c) and (d) show more details in Fig.(b).

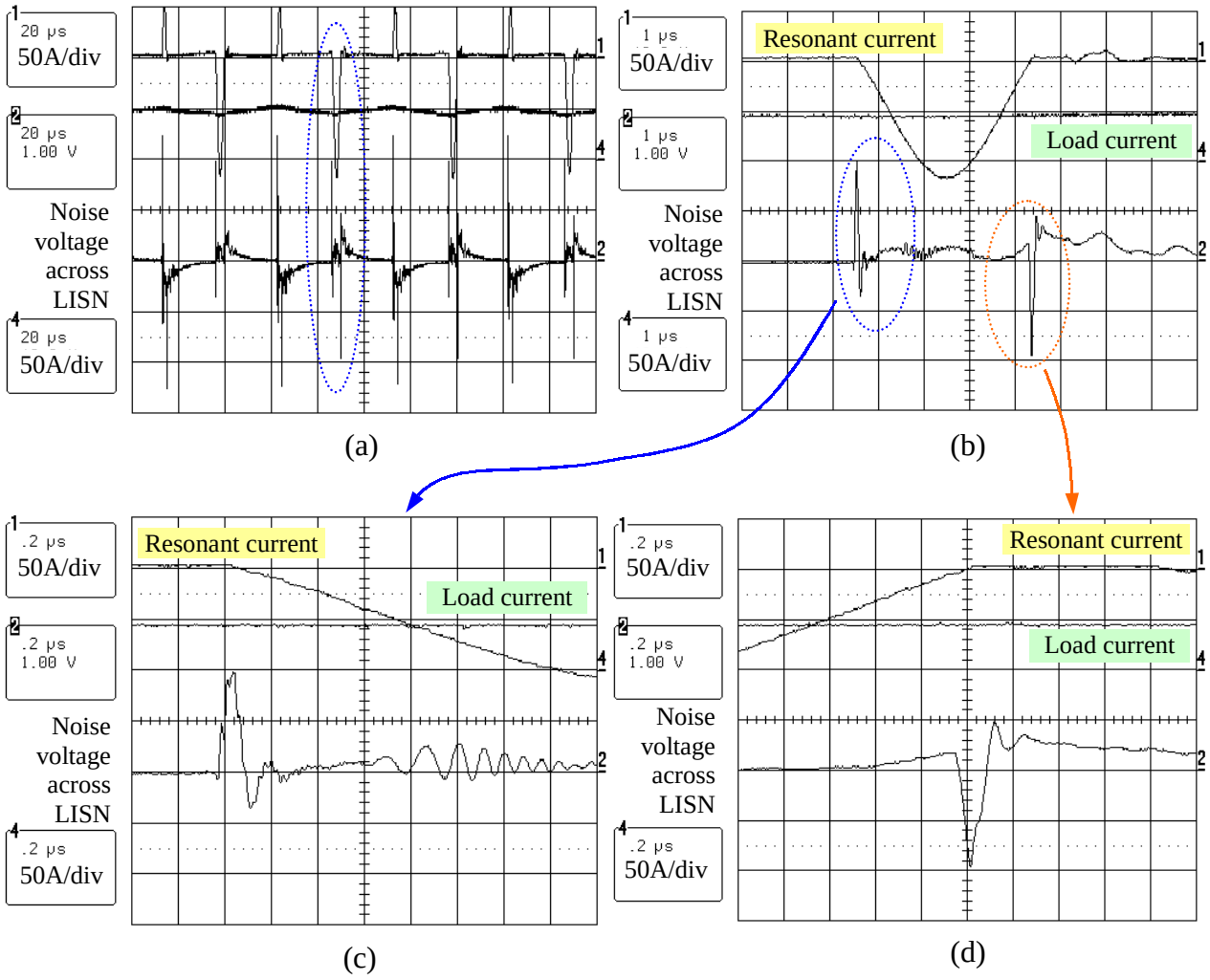


Fig.3.38 Total noise voltage across LISN while soft switching

It is seen in Fig.3.38(a) that the noise is composed by a series sharp spikes, with each spike followed by a ringing. Fig.3.38 (a) looks similar to Fig.3.16(b), except the magnitude of the spikes shown in Fig.3.38(a) is much smaller, around 5V. If we check the timing carefully we can find that for hard switching, the spike occurs when main switch turn on / turn off. However, in soft switching, the noise spike voltage corresponds to the resonant current turn on / turn off. This implies the noise spike induced by hard switching is suppressed, but soft-switching itself generates new noise spike, although this spike is smaller than that caused by hard switching.

DM noise voltage across LISN

The waveform of DM noise voltage across LISN is shown in Fig.3.39.

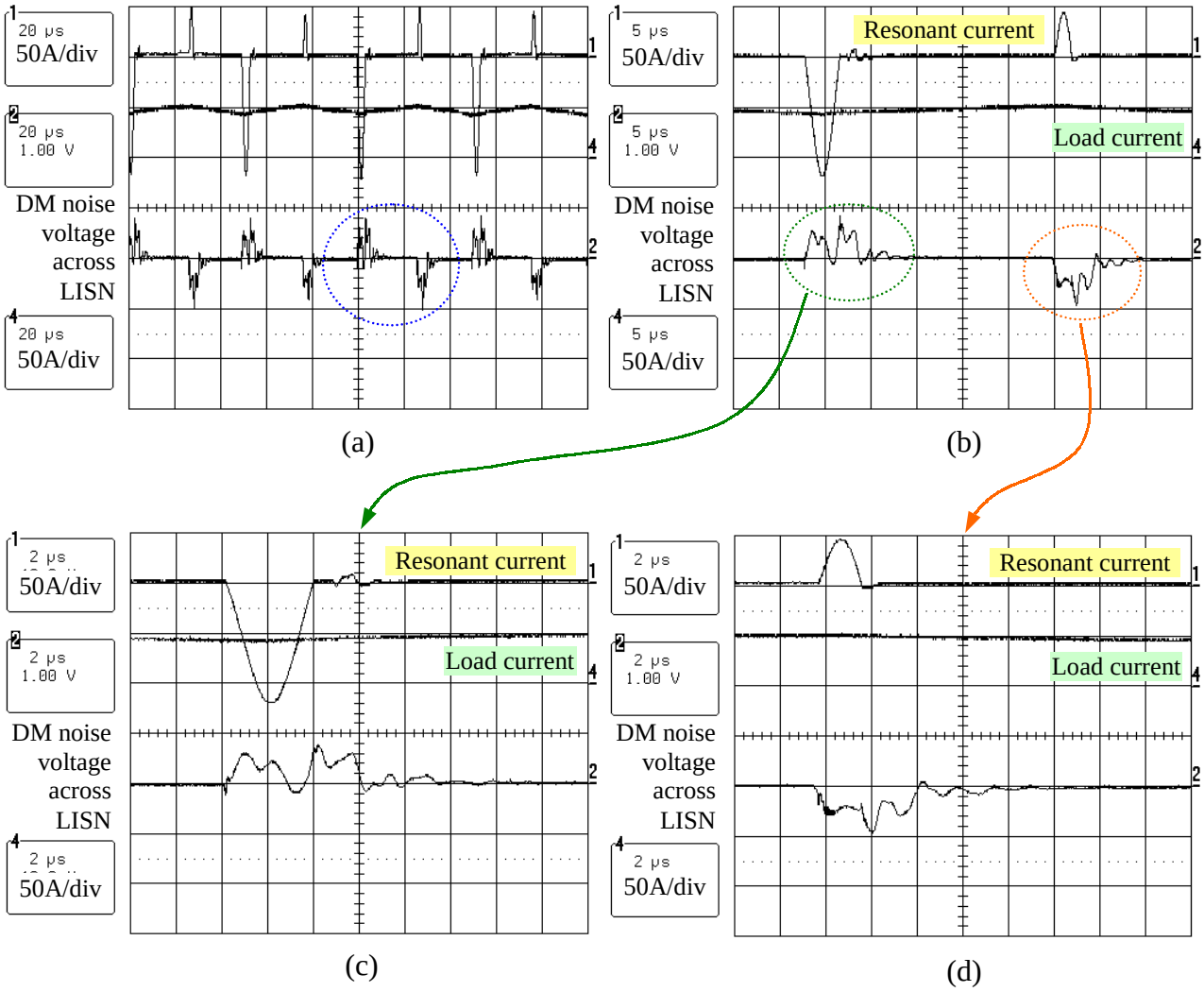


Fig.3.39 DM noise voltage across LISN while soft switching

The magnitude of DM noise generated while soft switching is smaller that of hard switching. The peak to peak value of the magnitude is less than 1V, but the noise voltage lasts longer than that of hard switching. The noise voltage is trigged by the turn on of resonant current and lasts longer than the resonant period.

CM noise voltage across LISN

The waveform of CM noise voltage across LISN is shown in Fig.3.40.

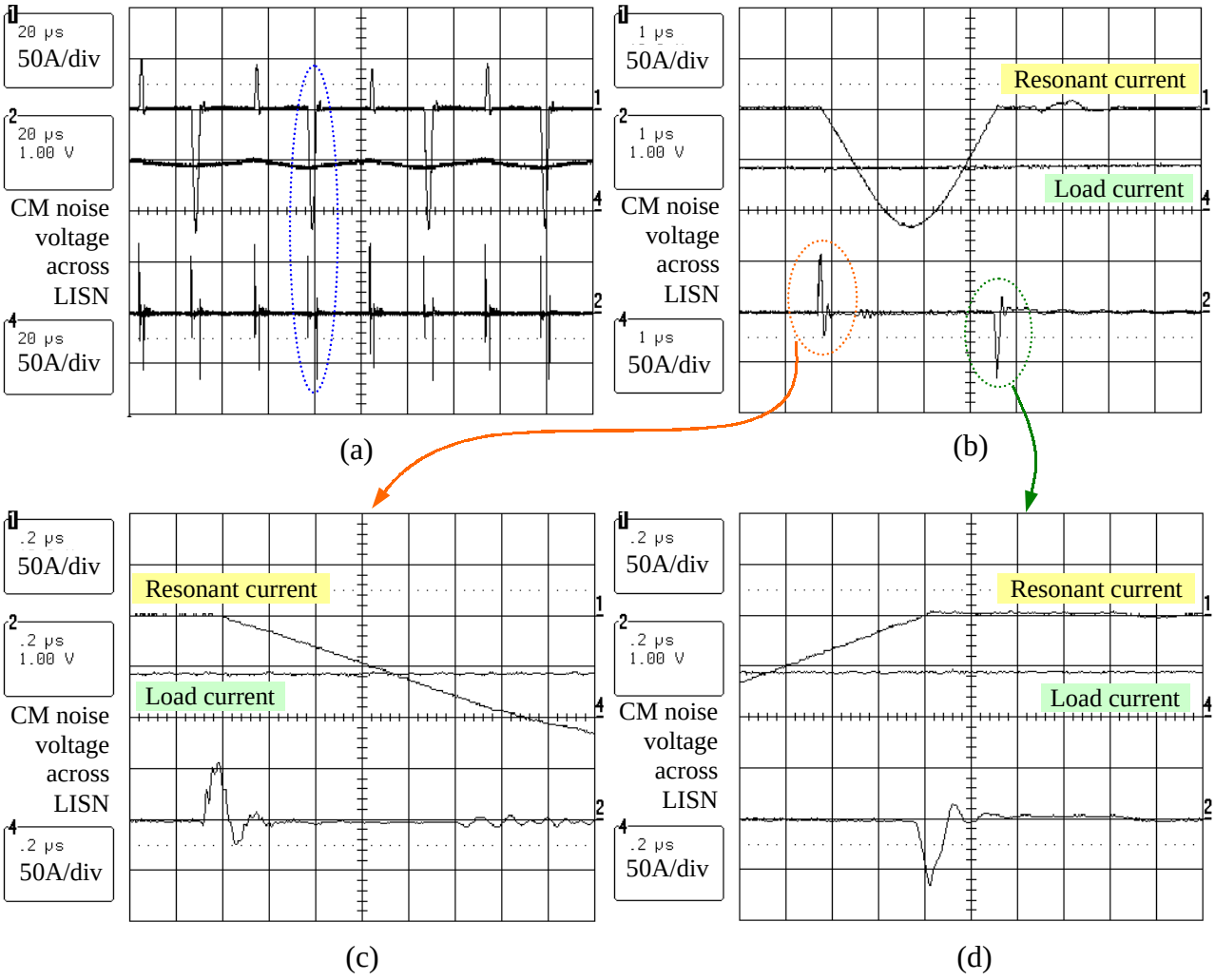
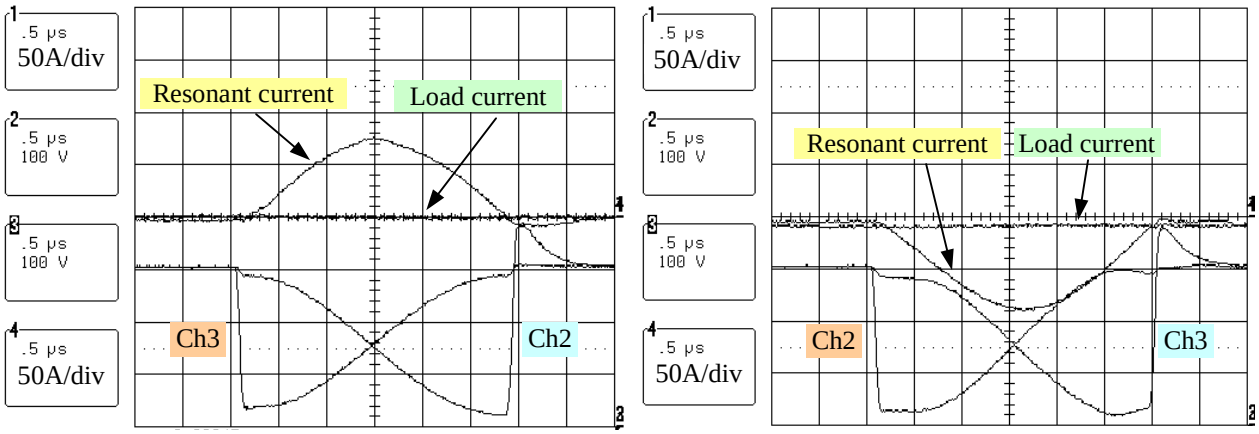


Fig.3.40 CM noise voltage across LISN while soft switching

The CM noise voltage spike is less than 2V, much smaller than that of hard switching. The CM noise spike occurs at the resonant current turn on and turn off. Since CM noise is mainly related with high dv/dt, there must be sharp voltage transition occurs while resonant current turn on and turn off.

Further experiment shows that the resonant current turn on spike is related to the hard turn on of MCT, the auxiliary switch. The resonant current turn off spike is still caused by the resonant branch diode reverse recovery. Although there is a snubber capacitor across the MCT, it is not large enough to dv/dt during the diode reverse recovery period. If a large snubber capacitor is chosen, the switching loss will increase and the turn on spike could be worse. The voltage waveform is shown in Fig.3.41.

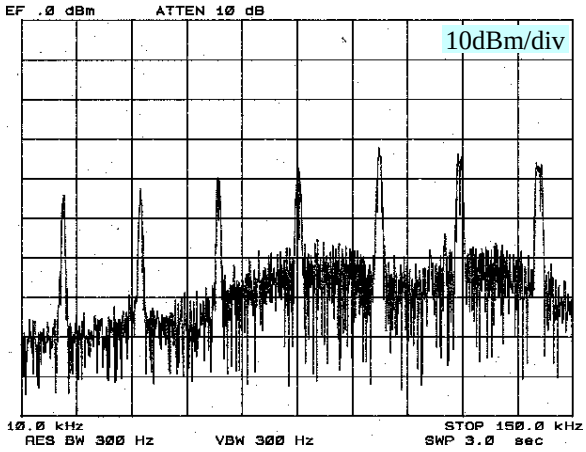


(a) Resonant current is positive (b) Resonant current is negative

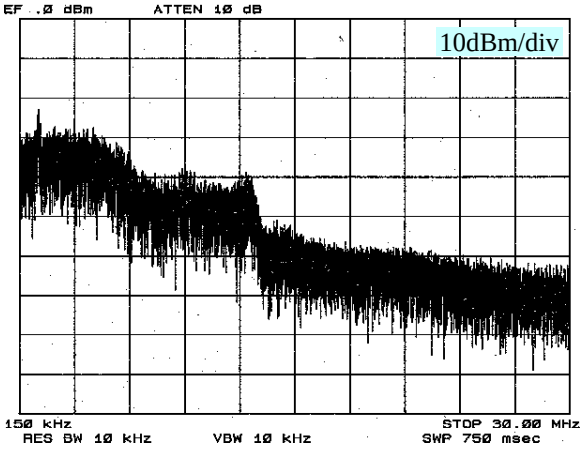
Fig.3.41 Sharp voltage transition at clamp point while resonant current turn on / turn off

Ch2 and ch3 are the points shown in Fig.3.37. The voltage is measured with respect to the negative dc bus. It is clearly seen that when SA1 turn on, the dv/dt of voltage drop at ch3 is about 2500V/µs. The dv/dt of voltage rise at ch2 is about 3200V/µs. These dv/dt is larger than that of hard switching. Only because the capacitance between these clamping points to ground is small, the C(dv/dt) is small and the CM noise is not as severe as that of hard switching.

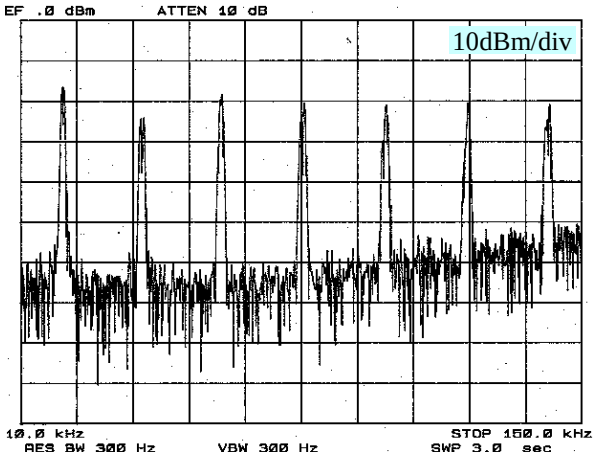
The correspondent EMI spectra (obtained at 300V 45A load) are shown in Fig.3.42. Compare with previous hard switching inverter EMI spectra shown in Fig.3.19, it could be found that the CM noise reduction is not significant, whereas the DM noise is reduced by 10 to 20dBm.



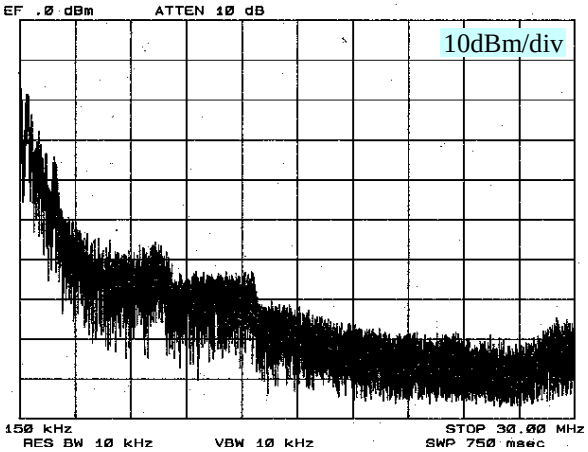
(a) CM noise, 10kHz ~ 150kHz



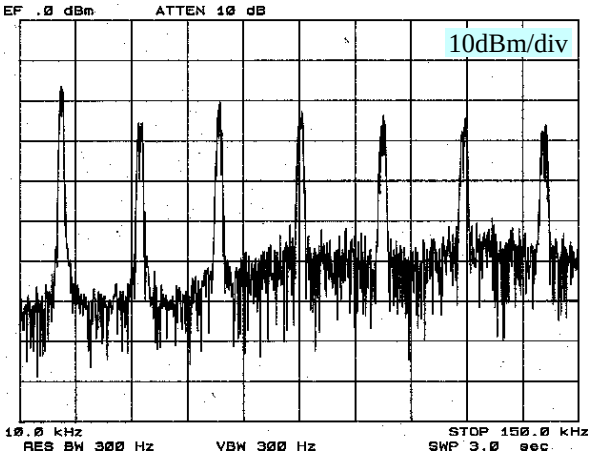
(b) CM noise, 150kHz ~ 30MHz



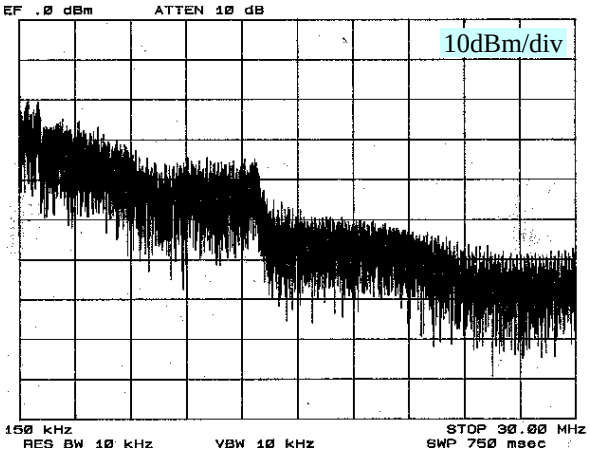
(c) DM noise, 10kHz ~ 150kHz



(d) DM noise, 150kHz ~ 30MHz



(e) Total noise, 10kHz ~ 150kHz



(f) Total noise, 150kHz ~ 30MHz

Fig. 3.42 Resonant snubber inverter EMI spectra

Since CM noise dominate the total noise, so the total noise reduction is also limited. For the low frequency range from 10kHz to 150kHz, soft switching has no effect on noise reduction. This is also verified the analytical conclusion discussed in chapter I that soft switching could be a solution to reduce only high frequency noise.

Chapter IV

CONCLUSIONS AND FUTURE WORK

4.1 Conclusions

To reduce EMI emission is becoming increasingly important as the fast switching devices are widely used in industry. The normal methods focus on EMI filter design, which is a way to deal with noise propagation path. EMI filter either blocks the noise path or provides a short path to the noise to localize it. Although it is very effective, its bulky size and cost make it not suitable in some cases.

Soft switching is a way to deal with noise source. It can reduce noise emission by reducing dv/dt and di/dt during the circuit operation. Its effectiveness is mathematically analyzed. Ideally, EMI reduction that could be achieved depends on the reduction of dv/dt and di/dt in the circuit. However, the practical EMI reduction is affected by many factors.

Based on above knowledge, a single-phase full-bridge hard-switching inverter and a single-phase full-bridge resonant snubber inverter are built and used as test bed for EMI noise comparison and characterization. The switching characteristics of the main device are obtained through many experiments.

For hard switching inverter, diode reverse recovery problems at turn on and high turn off dv/dt are the major EMI noise source. The noise voltage are measured and analyzed both in time domain and frequency domain.

For resonant snubber inverter, a better implementation is more important for EMI reduction. High power inverter has its peculiarity compared with low power inverter. Timing, protection circuit, thermal design, and proper control and are extremely important for its application. Otherwise, the device in the circuit could easily be damaged.

Much effort has been paid to find a way to suppress the current and voltage ringing without cause too much energy loss. Because the ringing not only generate EMI noise, but also endanger the safety of the device.

Variable charging time control is implemented and proved to be effective in loss and noise reduction.

The EMI noises generated while soft switching are also measured and analyzed in time and frequency domain.

Soft switching reduce DM noise by 10 to 20 dBm at frequency higher than 3MHz because it eliminates main switch diode reverse recovery problem.

Soft switching does not significantly improve CM noise reduction due to the diode reverse recovery in the auxiliary branch.

In conclusion, the soft-switching technique provides the potential to reduce EMI emission, but the ringing caused by diode reverse recovery in the resonant branch and the hard turn-on of auxiliary switch decreases the benefits achieved from the soft-switching of main switches. A compact layout and better implementation are inevitable for further reduction of EMI.

4.2 Future work

Future work can be divided into two aspects:

1. Continue the Experiment on the single-phase full-bridge inverter.

2. Modeling and simulation.

The experiment could continuously focus on the single-phase full-bridge inverter to get better understandings about the mechanisms of the EMI generation and propagation. For example, the hard turn on of auxiliary switch and diode reverse recovery of the auxiliary branch induce a lot of noise. A way should be found to solve these problems for better EMI reduction.

The Modeling and simulation work could be conducted in several aspects:

a) Modeling the turn on / off characteristics of the currently used IGBT device, because its internal connection is already known and its ESL is tested by TDR. The characterization should consider the case of different gate resistor, different bus voltage and different switch current.

b) Modeling the diode turn on/off characteristics because diode reverse recovery is big problem for EMI issue.

c) If MCT is still used as auxiliary switch, its turn on/off characteristic should also be modeled, because its hard turn on is also a severe EMI source.

d) The characteristics of some passive components at high frequency should also be tested and modeled, such as the load inductor, resonant inductor, snubber capacitor, DC bus capacitors (electrolytic, polyester, polypropylene), and the power cord.

e) Parasitic capacitance between the device and the ground should be tested and modeled.

f) The parasitic parameters in the whole circuit should be identified, thus the noise path could be completely identified.

g) The EMI introduced by gate drive circuit should be investigated.

h) Simulation of the whole circuit could be done once the above is known, some simple simulation could also be conducted based on some simple component model. The purpose of simulation is to help identify the noise source and path and try to find the relation between the noise seen by the LISN and the noise source and path. Therefore, we can try to find ways to reduce EMI through simulations. The simulation result should agree with the experimental result to a good extent.

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Appendix

AUXILIARY RESONANT SNUBBER INVERTER GATE DRIVER AND CONTROL INTERFACE DESIGN

In the appendix, the detailed circuit design of IGBT gate driver and MCT gate driver are described. These gate drivers are important for the inverter's operation. The design of control interface board is also explained in this chapter.

A.1 IGBT Gate driver design

The TOSHIBA 400A/600V IGBT is a half-bridge module. It has two IGBTs connected in series and sealed in one package. Each IGBT has about 45nF gate capacitance and requires large current driving capability of the gate driver board.

The IGBT gate driver board consists of three parts: input buffer, upper-side gate drive, and lower-side gate drive. Input buffer is used to provide high impedance for the input control signal and supply enough current to drive downstream circuit. Upper-side gate drive is used to drive the upper-side IGBT. Lower-side gate drive is used to drive the lower-side IGBT.

The gate drive circuit structure is shown in Fig. A-1

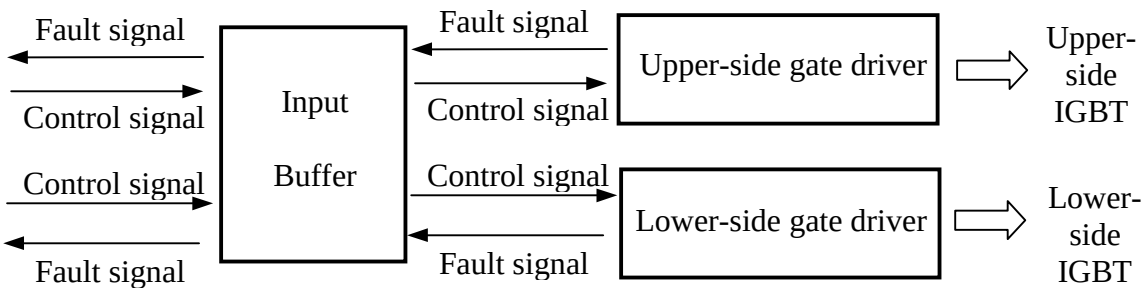


Fig A-1 IGBT gate driver structure

Since the ground of the upper-side gate driver is connected to the mid-point of the half-bridge, during the IGBT turn on / turn off, the potential of this ground will be either 300V or 0V. This fluctuating ground can generate a lot of CM noise and propagate back to the control interface circuit and cause its malfunction.

To reduce the noise coupled to the control interface board, the grounds of the three parts have to be separated. The input control signals are transferred to the gate driver through opto-coupler. There is no direct electric connection between the input and the gate driver, thus the CM noise is reduced.

Input buffer:

The power supply voltage level is +5V, and is obtained from control circuit board. The input buffer is any hex driver or inverting hex driver as long as it has large input impedance and 25mA output source current capability, such as 74HC04, 74LS04, or DM74ALS1004. This part of circuit is shown in Fig. A-2.

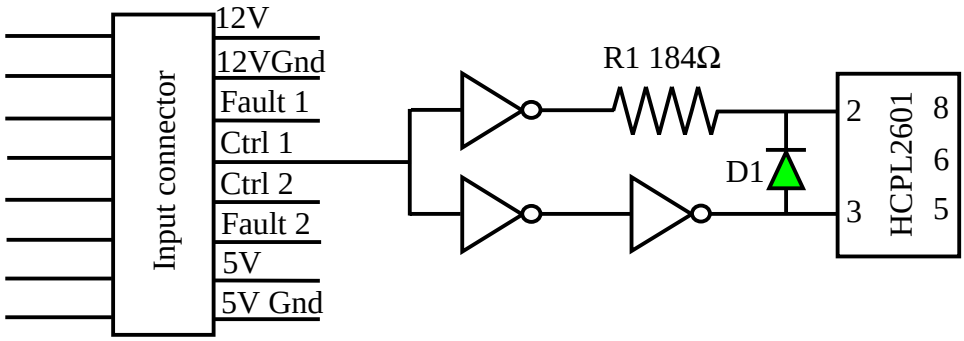


Fig. A-2 IGBT gate driver input buffer and input connector

The topside of the circuit board is used for ground layer. Most of the traces are at the bottom side of the board. R1 is used to limit the driving current around 25mA. The actual high level current required by HCPL 2601 is about 15mA. A larger current can improve the opto-coupling. The top layer ground of this part is used for the 5V power supply. This ground is connected to the ground of the control interface board.

Opto-coupler HCPL2601

HCPL2601 is a digital opto-coupler. Its output only reflects the voltage level change at input side. It is not a linear opto-coupler. Its output can not duplicate the voltage transition at the input side.

The input signal to the opto-coupler should be applied to Pin 2(+) and Pin 3(-). Diode D1 is 1N4144. It is connected at the input terminal to protect the internal LED from reverse side over voltage.

Pin 7 is enable pin. It should be always connected to logic high in this application.

The output signal is at Pin 6.

Since the output of HCPL2601 is open collector, a pull up resistor is necessary to be connected between the output and the Vcc. Here in this circuit, the Vcc is connected to 0V and the GND is connected to –5V.

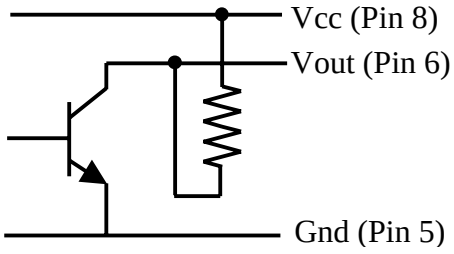


Fig. A-3 HCPL2601 open collector output

When the output transistor is on, the output is logic low; when the output transistor is off, the output is logic high. In the circuit, a 390Ω pull up resistor is connected between Pin 8 and Pin 6. Pin 8 is connected to 0V, Pin 5 is connected to –5V.

Gate driver:

The gate driver consists of three parts: DC power supplies module, MC33153 gate driver chip, and an output amplifier. It is shown in Fig. A-4.

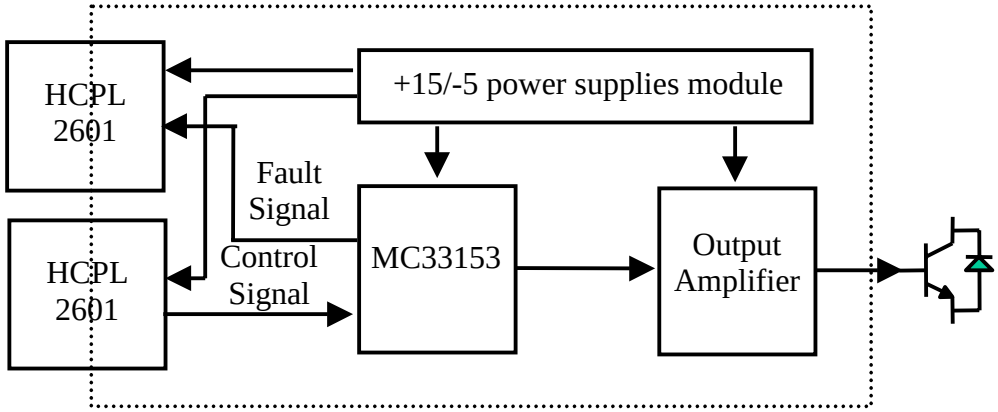


Fig. A-4 IGBT gate driver structure

A 12V DC source provide power to the two gate drive circuit through two DC/DC converter modules NMD120515S. Each of which can provide two separate outputs, +15V and +5V. By proper connection, a +15V output and a –5V output with a same ground can be obtained. The ground of the 12V input side is separate from the ground of the output side.

To turn on IGBT, +15V is suggested. A higher gate voltage can reduce the IGBT voltage drop when it is in conduction. The gate voltage should not be over 20V; otherwise the insulation layer of the gate of the IGBT may be damaged. Transient voltage suppressor can be added to the gate to prevent it from over voltage.

To prevent IGBT false turn-on, which could be caused by Miller effect during the transition of IGBT turn off, a –5V is applied to the gate to provide a negative bias voltage.

The power rating of NMD120515S power converter module is only 1W. This is constant power rating. The larger transient energy required to turn on IGBT is provided by the output capacitor of the converter module. Assume the charge of Q is needed to turn on IGBT, the output capacitor of power module is C, then the output voltage drop is:

$$\Delta V = Q/C$$

The output capacitor is replenished while IGBT turn off. To reduce the output voltage fluctuation, larger capacitance is necessary. In the circuit a 47μF tantalum capacitor and a 1μF monolithic-ceramic capacitor are used. They have better high frequency characteristics.

MC33153 driver chip:

MC33153 driver chip is the core of the total circuit. It has 1 A source / 2 A sink current capability. This chip has a feature of de-saturation function, which can provide short circuit protection for the IGBT. It also has negative gate drive capability.

Vcc (Pin 6) is connected to +15V; Vee (Pin 3) is connected to –5V; Current sense (Pin1) is connected to +15V.

A 390Ω pull up resistor is connected between Gnd (Pin 2) and Input (Pin 4). Because input is active low, when there is no input signal, the input pin should be pulled up to high.

A small blank capacitor should be connected between De-sat (Pin 8) and Gnd. The capacitance is 20 ~ 400pF. This capacitor determines the reaction time of the protection logic and filters out high frequency noise. If it is too big, for example, 0.01μF, the protection will never work, because there is a 270μA current source inside the chip. This current source will charge the blank capacitor every switching cycle. If the capacitor is too big, it can never be charged above 6.5V within the period of each cycle, and can not trigger the protection function.

If the de-sat pin (Pin 8) is open, the protection logic will work every cycle, and the output will be shut down every cycle. The output waveform looks like the one shown in Fig. A-5.

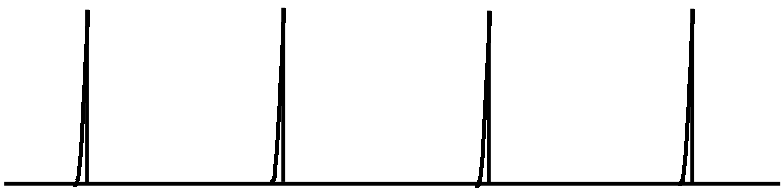


Fig. A-5 Output of gate driver when de-saturation works

If de-sat pin (Pin 8) is connected to Gnd, then the current of the internal 270 μA current source will flow through this path, and the voltage of de-sat pin (Pin 8) will never go above 6.5V. Then the output pin (Pin 5) can send out normal gate drive signal as in Fig. A-6.

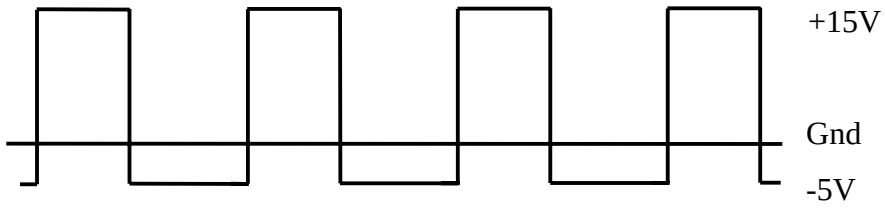


Fig. A-6 Normal output of gate driver

The fault pin (Pin 7) is active high. Whenever over current is detected, MC33153 will shut down for this cycle and restart at next cycle as long as the control signal is applied. Therefore the fault signal should be sent out to the control board to shut down the control signal for the whole circuit. The fault signal is also sent out through opto-coupler HCPL2601 to the control board.

The detailed information can be found in Motorola MC33153 data sheet.

Output amplifier

The driving capability of MC33153 is not large enough for high power rating IGBT. Therefore an output amplifier is used to increase the driving capability. The output amplifier is composed of two power transistors. One is MJD200 NPN type, the other is MJD210 PNP type. They have 5A continuous collector current rating and 10A in peak.

The Vceo is 25V, just enough for 20V voltage rating requirement. The circuit is shown in Fig.A-7.

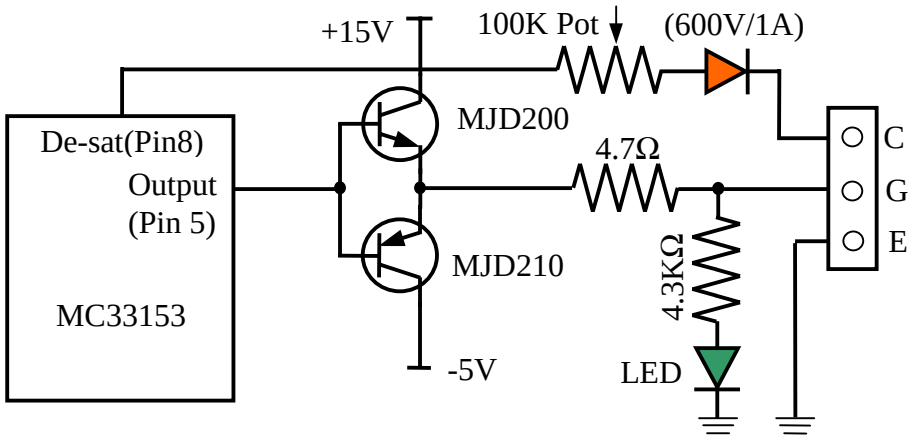


Fig.A-7 Output amplifier of gate driver circuit

An LED is added to the circuit to indicate whether the circuit is in operation or not. A 100K potential meter and a diode is used to sense the de-saturation voltage of Vce.

A.2 MCT Gate driver design

To turn on / turn off MCT, different gate driver is required. Harris MCTV75P60E1, which 75A, 600V P-type MCT, is used in the resonant snubber inverter as auxiliary switch. It turns on with a negative voltage pulse and turns off with a positive voltage pulse. Its input capacitance is 10nF, smaller than that of the aforementioned high power IGBT. Thus the required driving capability could also be smaller than that of IGBT gate driver.

The circuit is very simple with HCPL3120 IGBT gate drive optocoupler, as illustrated in Fig.A-8.

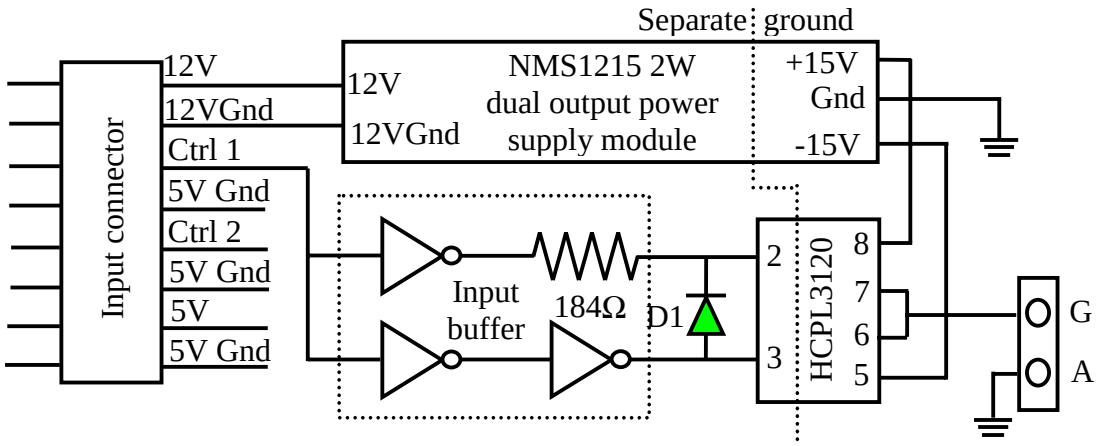


Fig.A-8 MCT gate driver

The circuit is composed of input buffer, NMS1215 dual output power supply module, and HCPL3120 gate drive optocoupler. The input buffer is the same as that in IGBT gate driver. The input and output of the power supply module are isolated. The HCPL3120 can provide 2A current driving capability, and the input and output are also isolated. Thus there is no direct connection between the high power side and the control side. The CM noise propagated to the control board can be reduced.

A.3 Control Interface design

Control interface board is the core of the inverter. It generates gate signals and sends them out to the gate driver boards to turn on / turn off main switches and auxiliary switches of the inverter. It also senses the feedback signals from gate driver boards and from current sensor to realize short circuit protection and variable timing control.

A.3.1 Introduction to the control interface board

The control interface board is used to realize the control of a single-phase full-bridge resonant snubber inverter. It also can realize the control of a single-phase full-bridge hard-switching inverter by proper connection of the jumper in the control board. The basic control method is Pulse Width Modulation (PWM) control.

The control board is composed of PWM signal generating circuit, short pulse eliminating circuit, current sensing and processing circuit, variable timing control circuit, main switch gate signal generating circuit, auxiliary switch gate signal generating circuit, and short circuit protection circuit.

The block diagram of the control interface board is shown in Fig.A-9

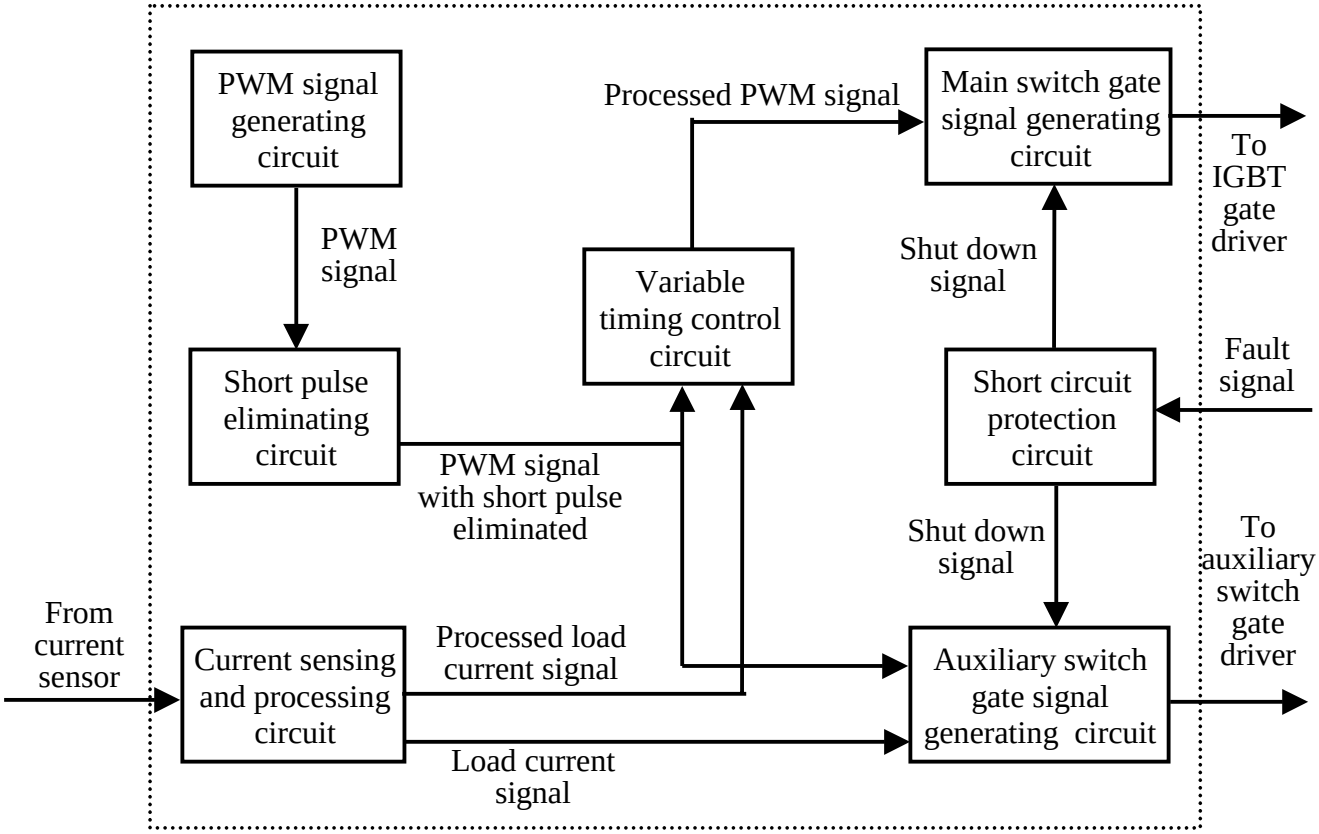


Fig.A-9 The control interface board block diagram

The function of PWM signal generating circuit is to generate a PWM signal. The positive and negative short pulse of the PWM signal will be eliminated by the short pulse eliminating circuit. This PWM signal is used as a time base and sent to variable timing control circuit and auxiliary switch gate signal generating circuit. The output of auxiliary switch gate signal generating circuit is sent to auxiliary switch gate driver. The output of variable timing control circuit is sent to main switch gate signal generating circuit to produce main switch gate signals, and then these main switch gate signals are sent to main switch gate drivers. The load current signal is sensed and transformed to appropriate voltage signals by the current sensing and processing circuit, and then sent to variable timing control circuit and auxiliary switch gate signal generating circuit to provide necessary control signals. Short circuit protection circuit will shut down all the gate signals once it receives fault signal from any gate driver board. The whole system can be reset manually by pressing a reset button.

The timing of PWM signal and gate signal is shown in Fig.A-10. The corresponding RSI inverter is shown in Fig. 3.20.

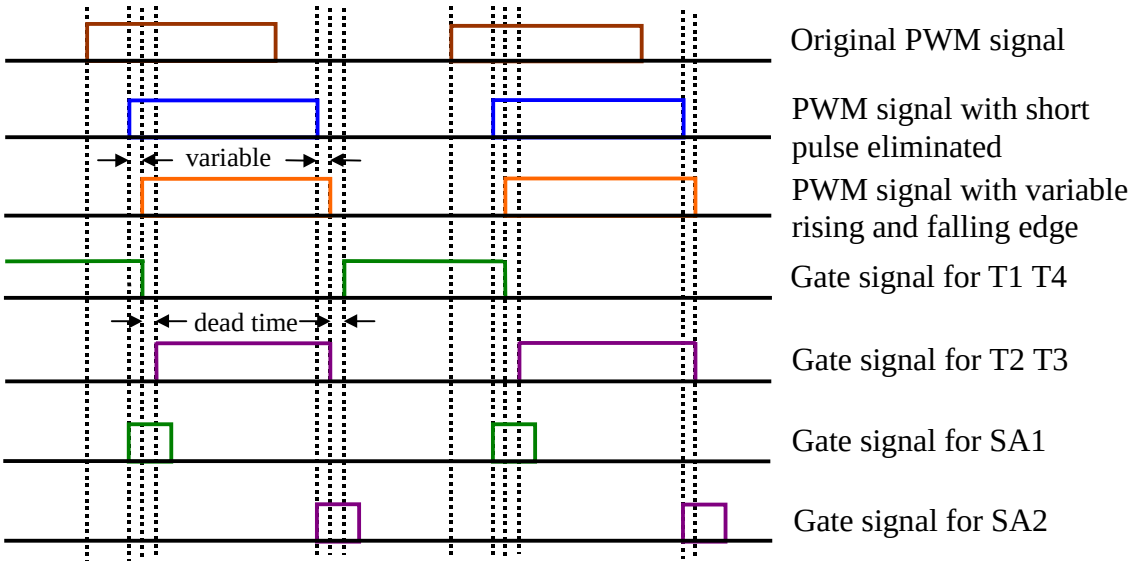


Fig.A-10 The timing of PWM signals and gate signals

Fig.A-10 shows that the auxiliary switch gate signal is triggered by the PWM signal. Main switch gate signal is triggered by the PWM signal whose rising and falling edge is variably delayed from the previous PWM signal. From turn on of auxiliary switch to turn off of the relevant main switch is the charging time of resonant inductor current. Since main switch is variably delayed based on the load current, the charging time of resonant inductor current is also varies with load current.

The control interface board has two separate grounds. One ground is for the circuits dealing with analog signal, which includes PWM signal generating circuit and current sensing and processing circuit. The other ground is for the circuits dealing with digital signal, which includes the rest circuits. The signals of different ground are coupled through digital and linear optocouplers. The voltage level for analog circuits is ±15V, obtained from an off-line power supply. The voltage level for digital circuits is +5V, also obtained from an off-line power supply.

A.3.2 PWM signal generating circuit

The PWM signal generating circuit is used to generate the PWM signal. It is a simple voltage comparator. It compares a sinusoidal waveform and a triangular waveform to get a PWM waveform. The frequency of sinusoidal waveform is low, varied from 20Hz to 200Hz in the experiment. Its peak magnitude is in the range of 1.5V to 3V. The triangular waveform is fixed at 20kHz. Its peak magnitude is ±5V. Both the sinusoidal waveform and triangular waveform are obtained from the function generator.

The waveform comparison is shown in Fig.A-11.

The circuit is shown in Fig.A-12.

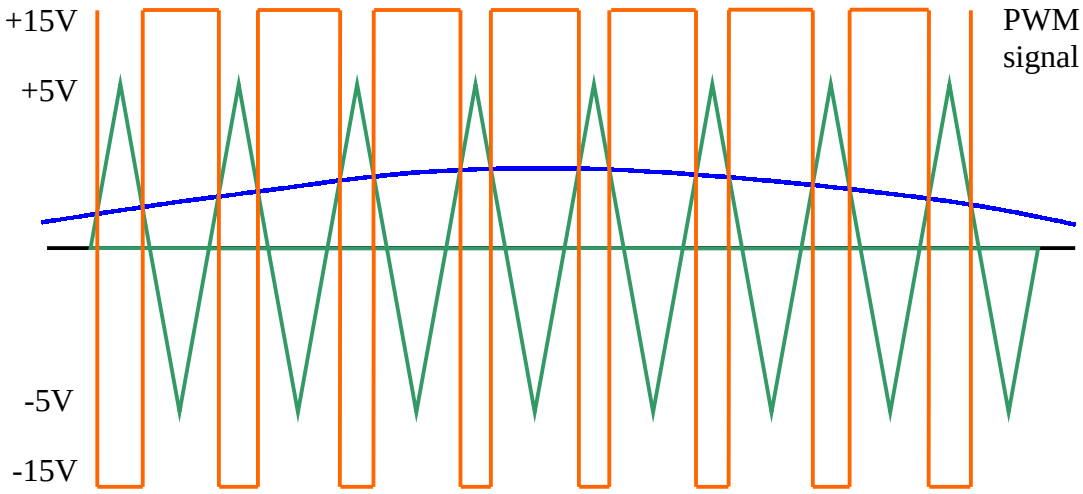


Fig.A-11 Comparing sinusoidal waveform and triangular waveform to get PWM signal

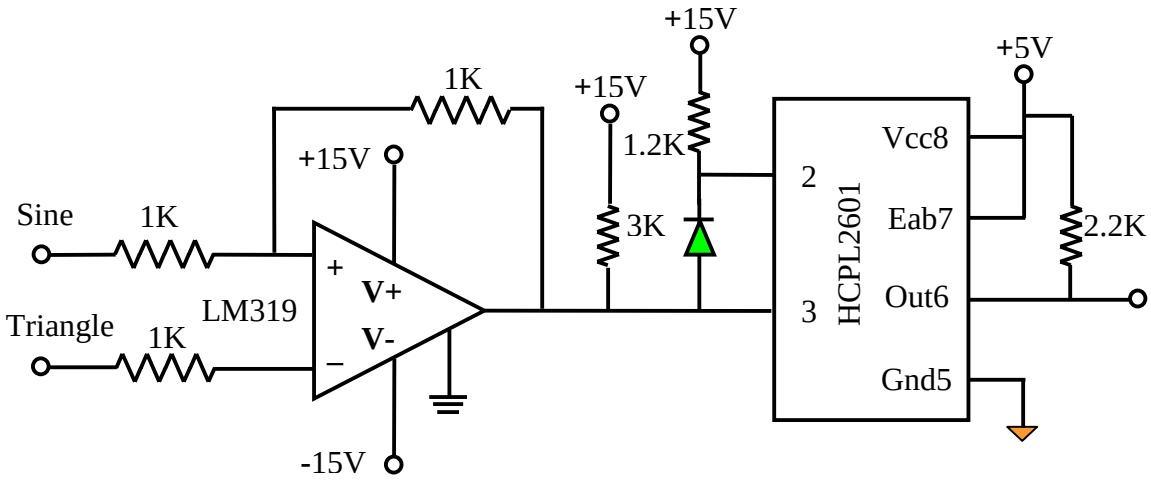


Fig.A-12 PWM generating circuit

The output of the voltage comparator is sent to next functional circuit through optocoupler, and the output voltage level of optocoupler is 5V, compatible with TTL digital logic voltage level.

A.3.3 Short pulse eliminating circuit

The function of short pulse eliminating circuit is to eliminate the short pulse in PWM signal. Since the auxiliary switch gate signal is triggered by the rising edge and falling edge of PWM signal, if the rising edge and falling edge are close to each other, then the two auxiliary gate signals may overlap in a short period of time. This will affect the normal function of the resonant branch in resonant snubber inverter. The short pulse of PWM signal doesn't make much contribution to change the load current. If the short pulses are eliminated, then the number of switching operation can be reduced, and switching loss can be reduced. However, the harmonic components of the load current will increase, though only insignificantly.

The circuit is composed of two mono-stable multi-vibrator 74LS123, a positive-edge-triggered D flip-flop, and a AND gate. It is shown in Fig.A-13.

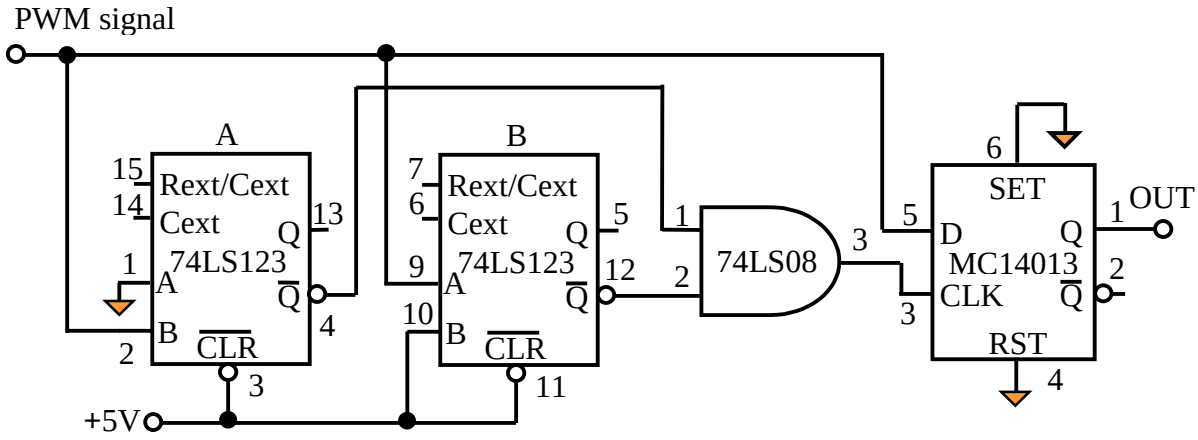


Fig.A-13 Short pulse eliminating circuit

The major issue in the design is hazardous problem, which is solved by using D flip-flop. The principle of the circuit is explained as follows.

Multi-vibrator A is triggered by the rising edge of PWM signal, multi-vibrator B is triggered by the falling edge of PWM signal. Once triggered, both A and B are set to send out a 6 μs pulse. If the PWM pulse, either positive or negative, is less than 6μs, it will be eliminated, at a cost that the output PWM signal has to be delayed for 6μs. This is shown in Fig.A-14.

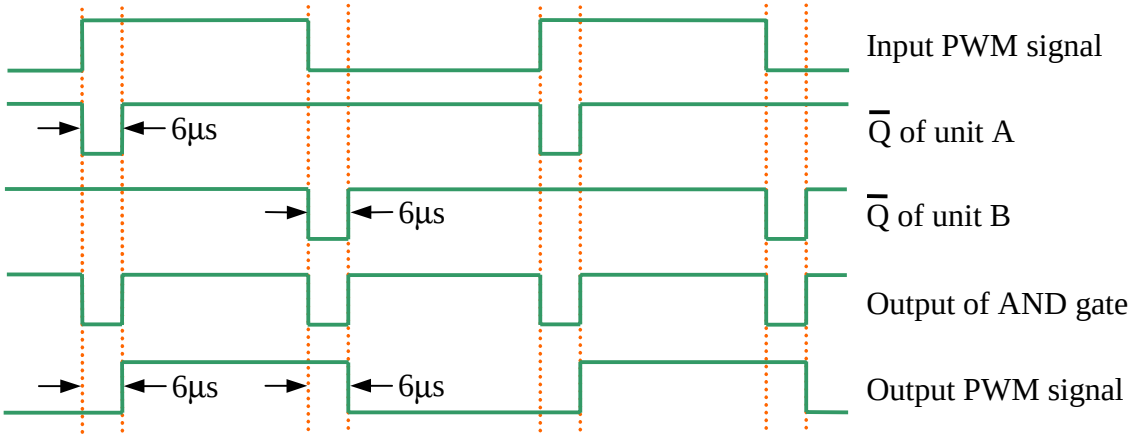


Fig.A-14 The output PWM signal has been delayed for 6μs

The information on the D input is accepted by the flip-flop only on the positive going edge of the clock pulse. The voltage level on the D input may be changed while the clock is low or high without affecting the output. The output of the AND gate is used as clock signal for the D flip-flop, while the input PWM signal is used as D input.

The elimination of short pulse is shown if Fig.A-15.

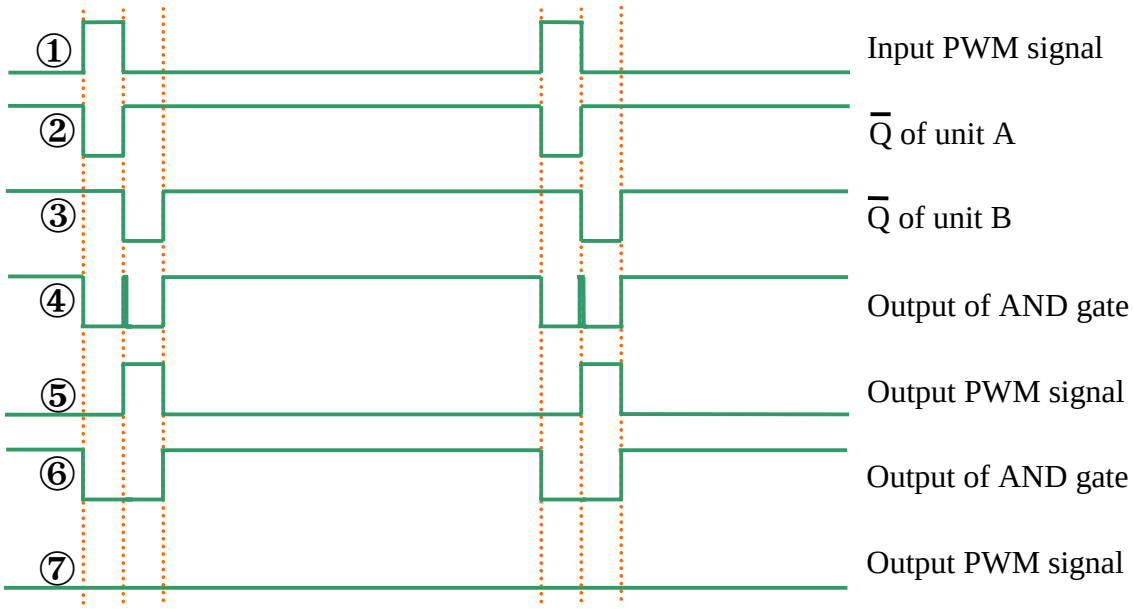


Fig.A-15 Elimination of positive short pulse of PWM signal

Fig.A-15 shows how the positive short pulse of PWM signal is eliminated. If the pulse width is very close to 6μs, then there could be a spike at the output of the AND gate, and the short pulse can still pass through the circuit. This is shown in waveform ④ and ⑤ of Fig.A-15. If the pulse width is less than 6μs, then it will be eliminated from the output PWM signal. This is shown in waveform ⑥ and ⑦ of Fig.A-15. It is the same for the elimination of the negative short pulse of the PWM signal.

A.3.4 Current sensing and processing circuit

The load current is sensed by LEM Model LA305-S current transducer. The output current of the transducer is 1/2500 of the load current. This current flows through a 50Ω measuring resistor. The voltage developed on this resistor is sensed and processed by this circuit.

The structure of this part is shown in Fig.A-16.

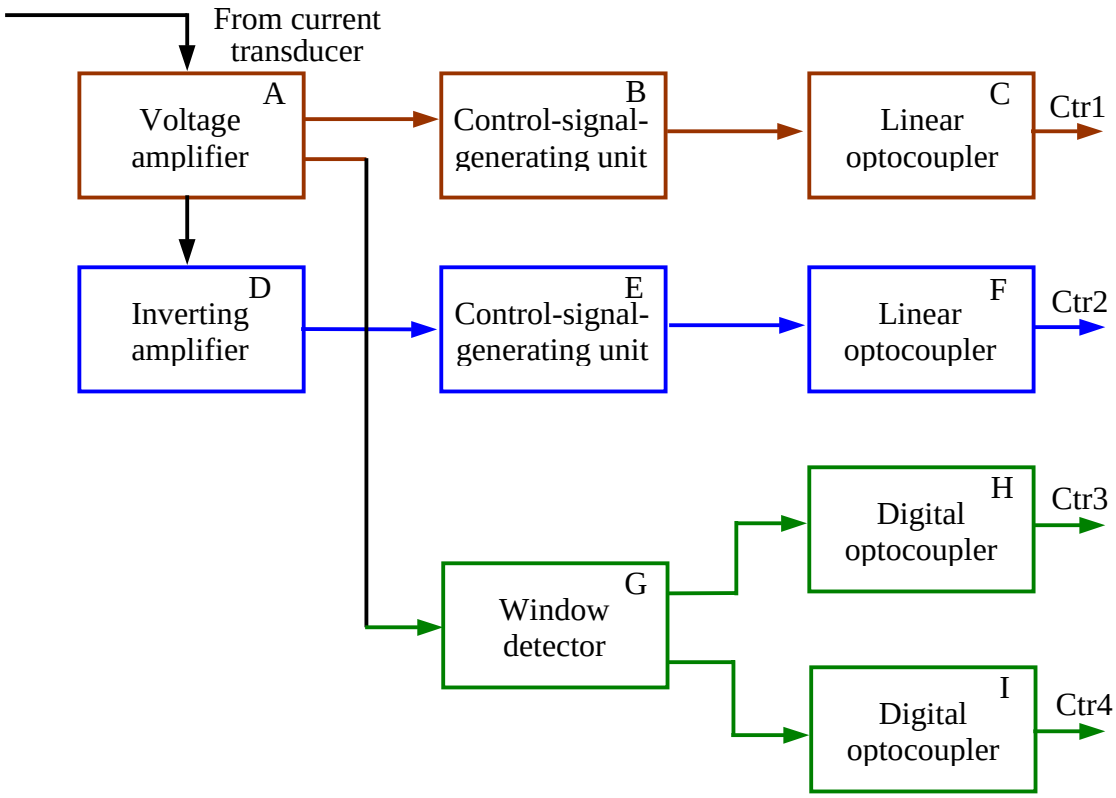


Fig.A-16 Structure of current sensing and processing circuit

The voltage developed across measuring resistor is amplified by voltage amplifier to drive the down stream circuit. UNITS B and E are used to generate necessary waveform for variable timing control. This is explained later. UNITS B and E are exactly the same.

Units C, F, H, I are used to provide isolation, C and F are exactly the same, H and I are exactly the same.

The unit A, voltage amplifier is shown in Fig.A-17.

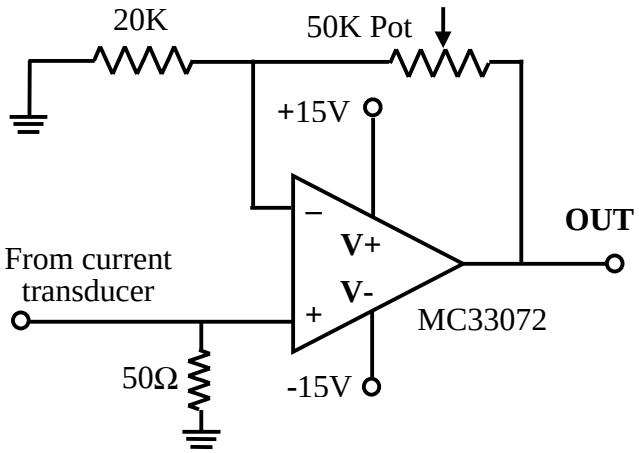


Fig.A-17 Voltage amplifier for load current sensing

If the 50kΩ potential-meter is reduced to zero, then the circuit becomes a voltage follower. The unit D, inverting amplifier is shown in Fig.A-18

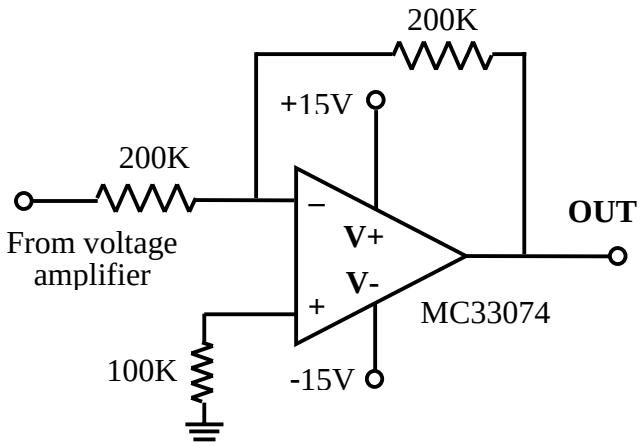


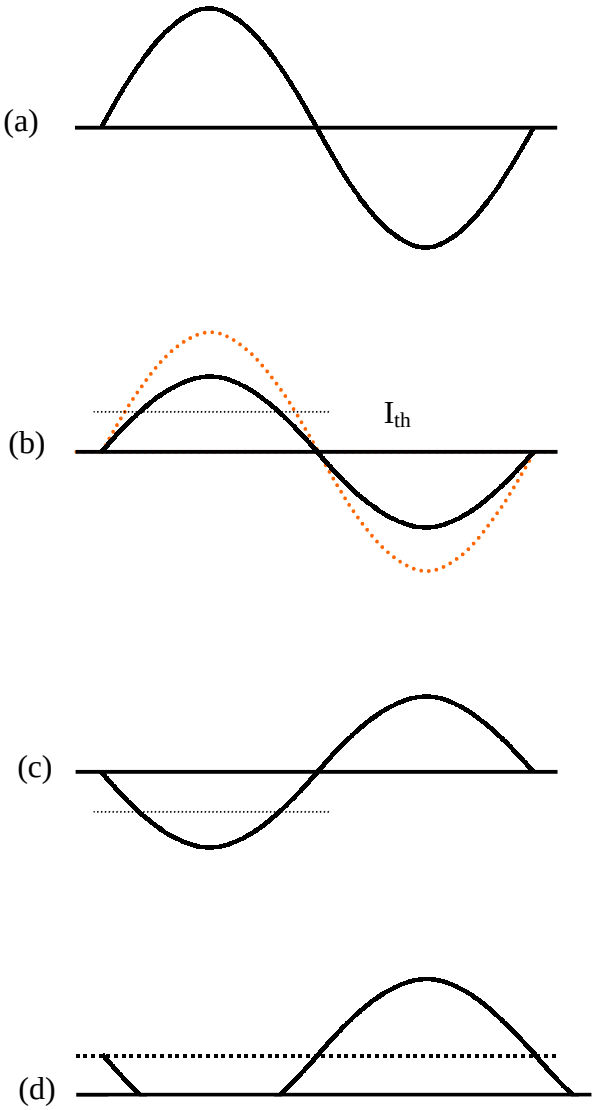
Fig.A-18 Inverting amplifier for load current sensing

The control-signal generating unit is to generate a voltage for variable timing control. This voltage signal is produced based on the magnitude and direction of load current. As shown in Fig. 3.20, if the load current is in the positive direction, and T1 T4 on is going to change to T2 T3 on, the load current will discharge C2 and C3 during the dead time, thus help realize zero voltage turn-on. If the load current is large, less resonant current is needed, and less charging time for the resonant inductor is required. If the load current is small, more resonant current is needed; thus more charging time for the resonant inductor is required. If the load current is in the negative direction, and T1 T4 on is going to change to T2 T3 on, then more charging time for the resonant inductor is needed to divert load current to resonant branch and to obtain enough resonant current to discharge C2 C3 within the dead time.

The variable resonant inductor charging time is obtained by the variable delay of the turn off time of the main switch, as shown in Fig.A-10.

The resonant inductor charging time changes with the load current magnitude and direction. The objective is to get just enough resonant current for soft switching, no more, no less. If the resonant current is too large, more EMI noise and energy loss will be generated. If the resonant current is too small, ZVT can not be obtained. Fig.A-19 shows how to get control voltage waveform for T1 T4 from the sensed load current waveform.

For T2 T3 the inverting load current waveform is needed to generate the control voltage signal for variable timing control.



Unit A output voltage, represents the shape of load current.

Scale down the voltage in (a).
When the load current is above certain value, for example, $I_{th,}$ no delay of main switch is needed. Load current itself is large enough to realize ZVT.

Inverting the voltage in (b)

Shift up the voltage in (d). This is the voltage signal for variable timing control. Its top is clamped to make sure its magnitude is more than 0V and less than 3.5V, in order to satisfy the requirement of variable timing control circuit.

Fig.A-19 Get variable timing control voltage from load current

The circuit of control signal generating unit is shown in Fig.A-20

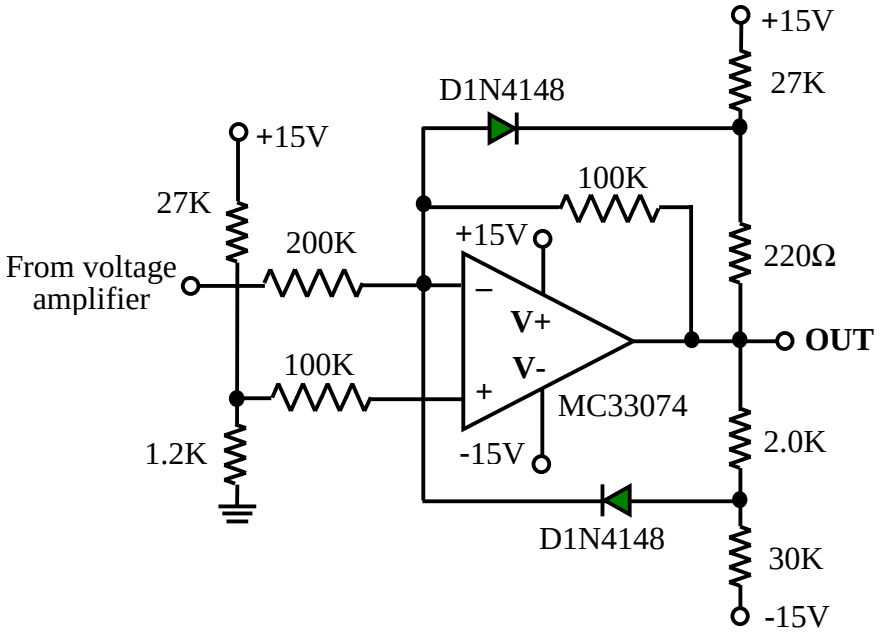


Fig.A-20 Control signal generating unit

Since the control voltage is analog, a linear optocoupler is necessary for signal coupling and ground isolation. The applied linear optocoupler is SIEMENS IL300. The circuit schematic is shown in Fig.A-21.

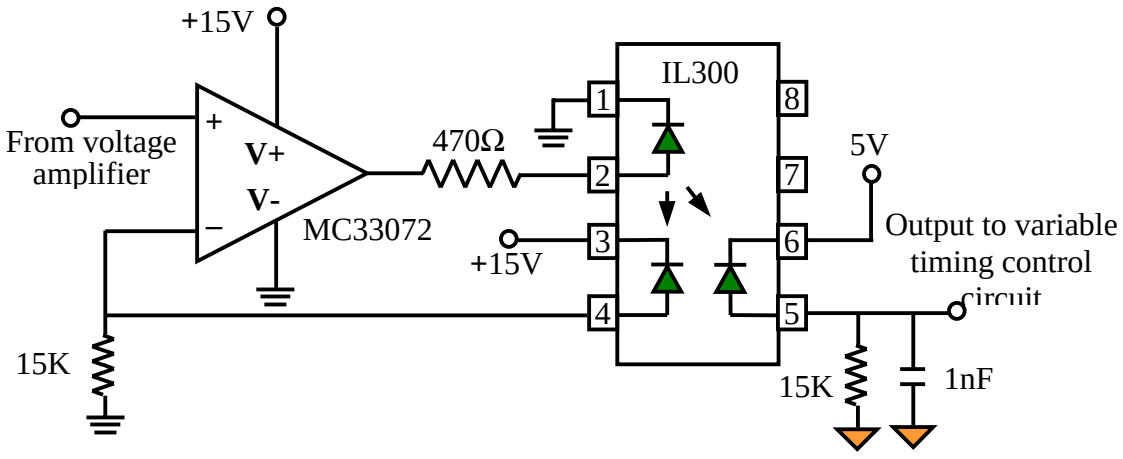


Fig.A-21 Linear optocoupler

The window detector and digital optocoupler are shown in Fig.A-22. Its function is simple. Whenever the magnitude of load current is above a certain value, the circuit will send out a signal to shut down the correspondent auxiliary-switch. Because, when the load current is high enough, it can discharge the resonant capacitors within the dead time by itself, thus ZVT can be obtained naturally and the resonant inductor current is not necessary at this condition. However, to obtain the ZVT of the other pair of main switch, it is still needed to turn on the correspondent auxiliary switch.

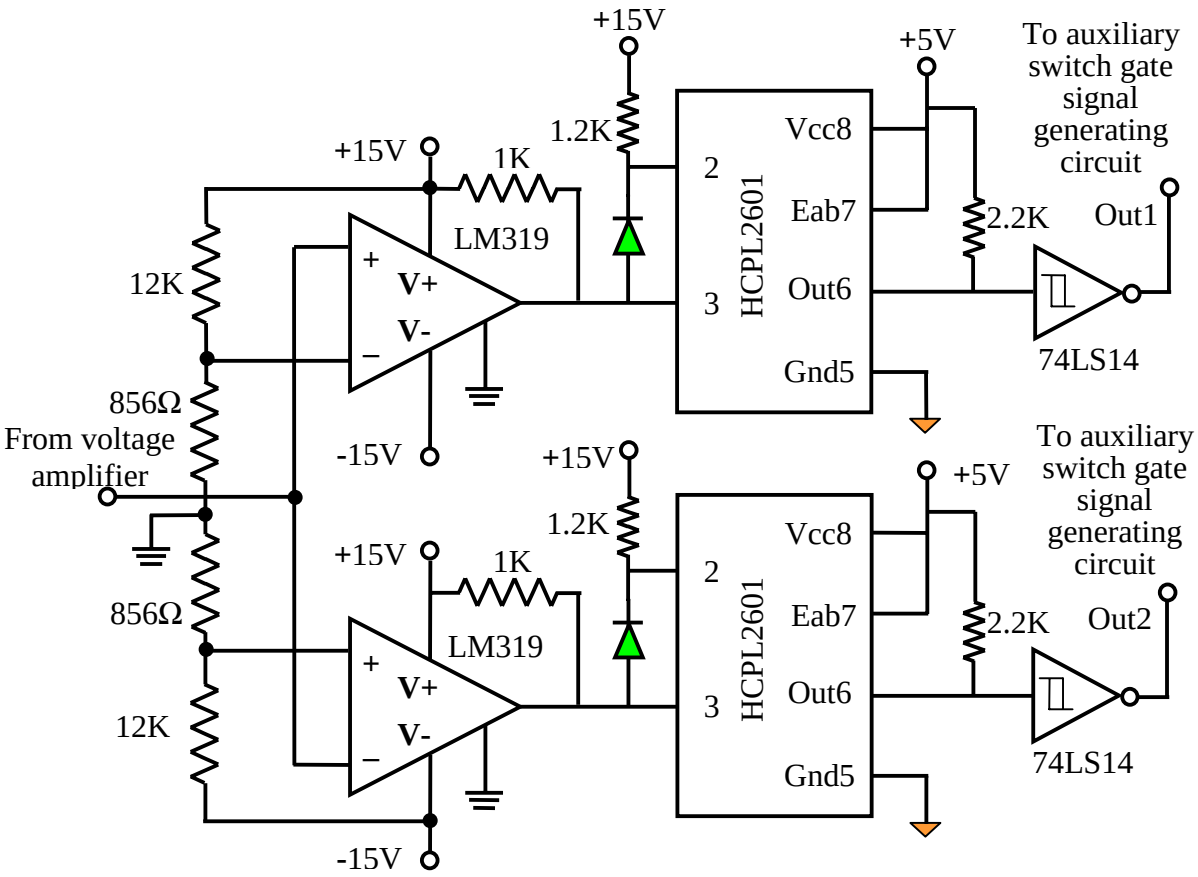


Fig.A-22 Window detector and optocoupler

The threshold for the window detector is set at ±1V, which corresponds to 50 A load current. The load current that can discharge 0.22μF from 300V to 0V within 2μs should be: (The equivalent resonant capacitance of the resonant capacitors shown in Fig. 3.20 is 0.22μF, and the load current is considered as constant in the 2μs dead time.)

$$I = c\frac{dv}{dt} = 0.22\mu F * \frac{300V}{2\mu s} = 33A$$

Therefore 50 A load current should be large enough to realize ZVT.

A.3.5 Variable timing control circuit

This circuit receives short-pulse-eliminated PWM signal and generates a new PWM signal with variable delayed rising and falling edge. This PWM signal is used to produce main switch gate signal. The delayed time of the rising and falling edge is contingent with the magnitude of load current magnitude and direction.

The circuit is shown in Fig.A-23.

The upper half of the circuit is to deal with the rising edge of the PWM signal, and the lower half of the circuit is to deal with the falling edge of the PWM signal. LM311 is voltage comparator. Its positive input voltage should not be over 3.89V when the power supply voltage is 5V, otherwise no matter what its negative input voltage is, its output is always high. 1N5287 is current regulator diode. As long as the voltage across the diode is more than 1V and less than 100V, the current flowing through the diode is regulated to 0.33mA. The two hex inverting gates and the 1nF capacitor are used to filter the spikes of the signal. If the output of the D flip-flop is clean, then this filter can be removed, because it increases the propagation delay.

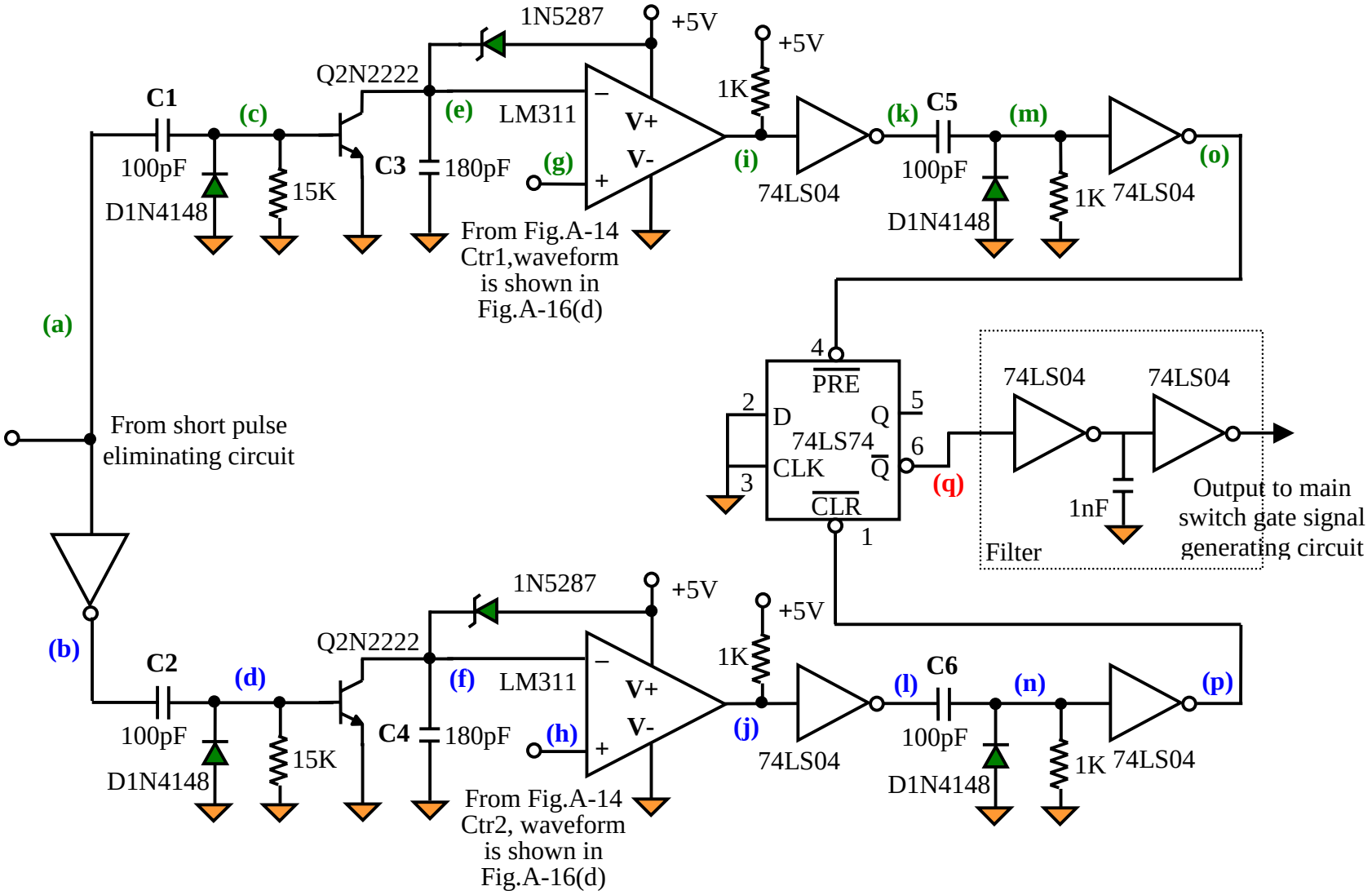


Fig.A-23 Variable timing control circuit

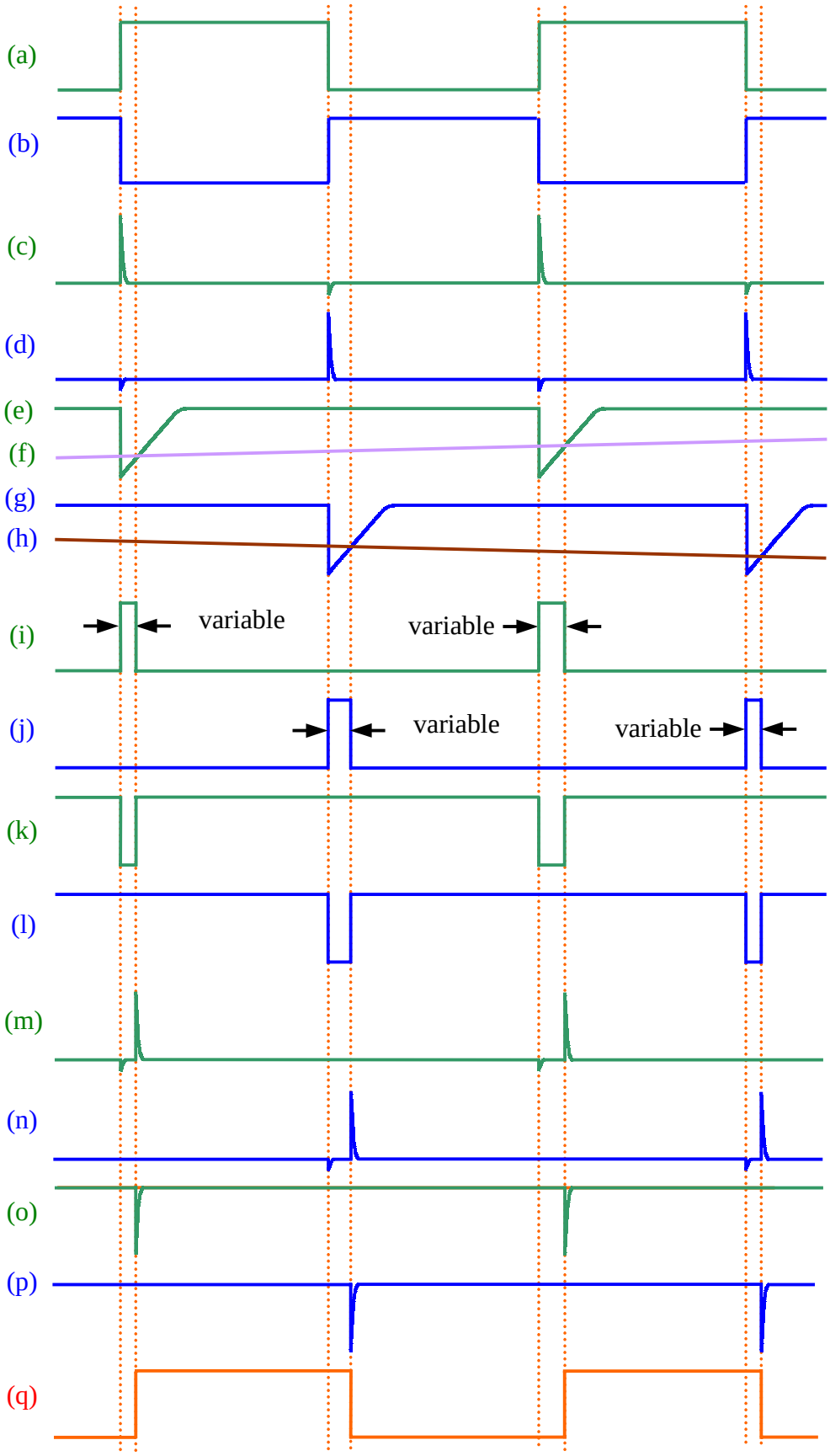


Fig.A-24 Waveforms of variable timing control circuit

The waveform of each point in Fig.A-23 is shown in Fig.A-24. It clearly shows the principle of the circuit. The capacitance of C3 & C4 in Fig.A-24 determines the delay time of the rising and falling edge. The relation between this capacitance and the required charging time is almost linear. The capacitance should be adjusted in the experiment.

A.3.6 Main switch gate signal generating circuit

The function of this circuit is to generate main switch gate signal. This function is realized by IXYS IXDP630, an inverter interface and digital dead-time generator. The circuit is shown in Fig.A-25.

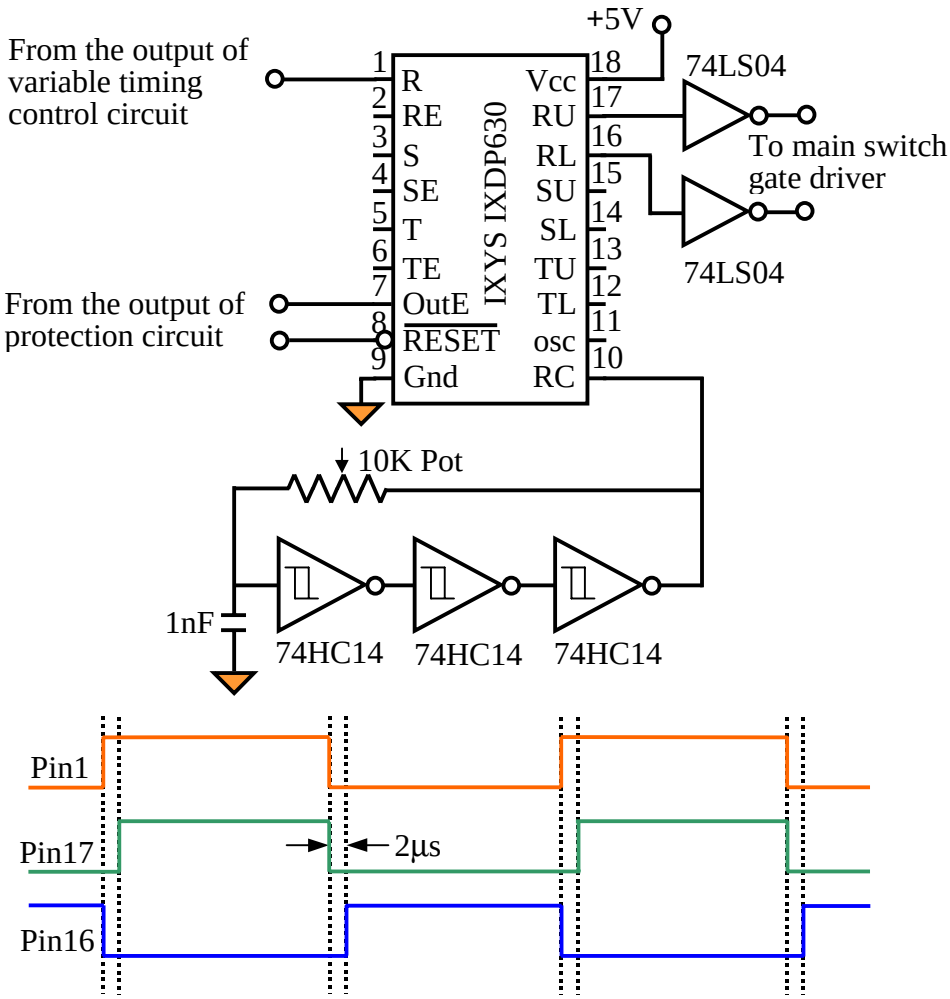


Fig.A-25 Main switch gate signal generating circuit

The input to R is the PWM signal from the output of variable timing control circuit. The two outputs are sent out to gate drivers through inverting gate 74LS04 to make the logic correct. RU is sent to T1 T4 and RL is sent to T2 T3 (T1 ~ T4 are shown in Fig.3.20).

The DEADTIME is fixed at 8 times the period of the clock signal at RC(Pin10). For 2μs dead time, the frequency of the RC resonant circuit is set at 4MHz.

OutE (Pin7) is output enable. Low input logic level will inhibit all outputs (low). The RESET signal is active low, when a logic low RESET is applied, all outputs will go low. After releasing the RESET command within the generated delay, the outputs will align with the phase input level after the programmed delay internal.

A.3.7 Auxiliary switch gate signal generating circuit

The function of this circuit is to generate auxiliary switch gate signal. It is triggered by the PWM signal with short pulse eliminated. Its output will be inhibited when the load current is high enough to realize ZVT by itself.

The circuit is shown in Fig.A-26.

Unit A C D are AND gate and are used as buffer. Unit A is necessary to reshape the PWM signal, making its edge steep, otherwise the circuit won't work properly. The pulse width of the auxiliary switch gate signal is set to 6μs by unit G and H. The output pulse of units J and I is set to 7μs, and one output will block the other one. Thus the overlap of the auxiliary switch gate signal can be avoided. The RC circuit in the output is used to adjust the gate signal delay and to match the propagation delay in the variable timing control circuit.

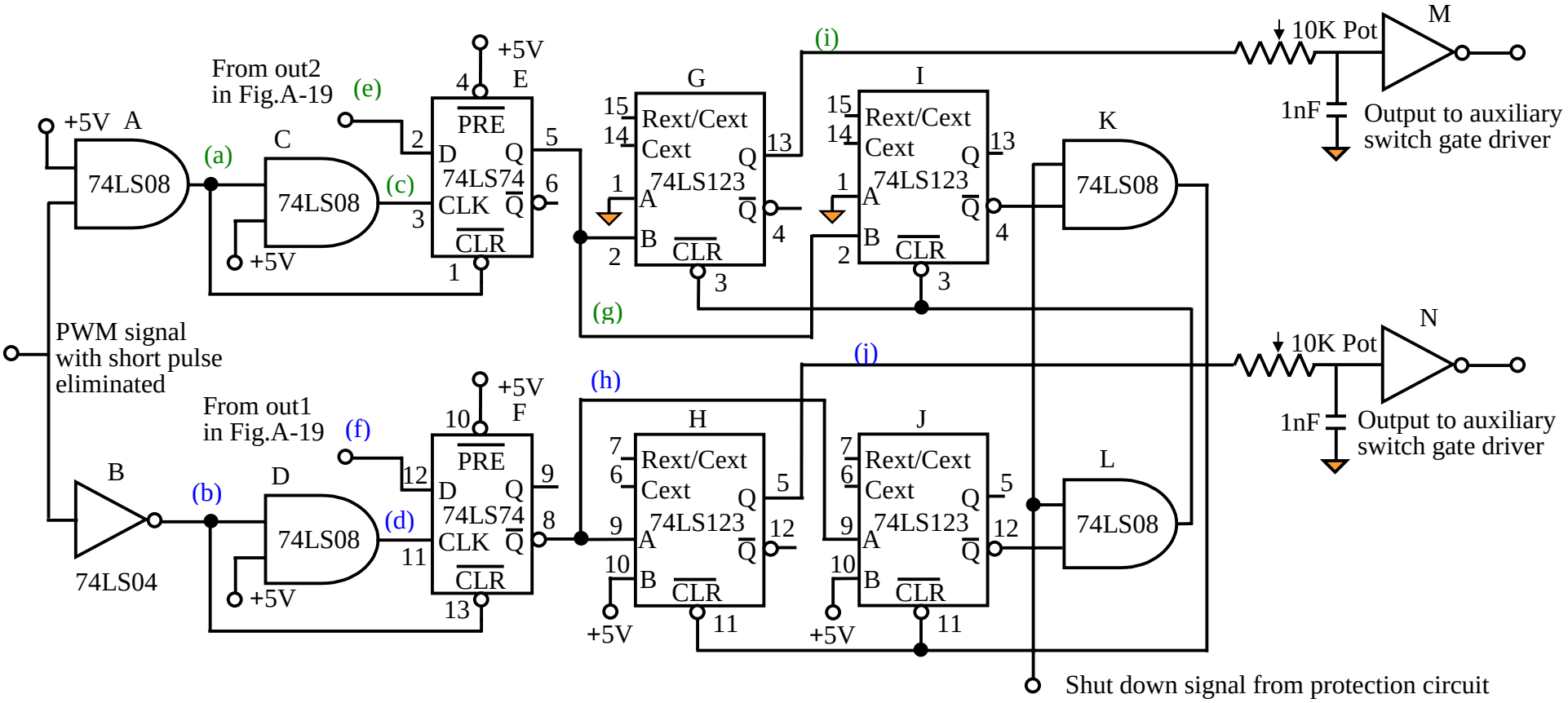


Fig.A-26 Auxiliary switch gate signal generating circuit

The auxiliary switch gate signals are generated by unit G and H. G is triggered by the rising edge of PWM signal. H is triggered by the falling edge of PWM signal. As the shut down of the auxiliary switch gate signal should be controlled separately, the PWM signals are separated and sent to the correspondent chip. Units K and L are used to receive signal (active low) from protection circuit and to shut down both auxiliary switches. Units E and F are positive-edge triggered D flip- flops, and their output is cleared every cycle by the PWM signal. Units C and D are used to provide a propagation delay time to avoid the output uncertainty which occurs when the PWM signal rising edge is applied to CLK and CLR simultaneously.

Some waveforms of Fig.A-26 are shown in Fig.A-27.

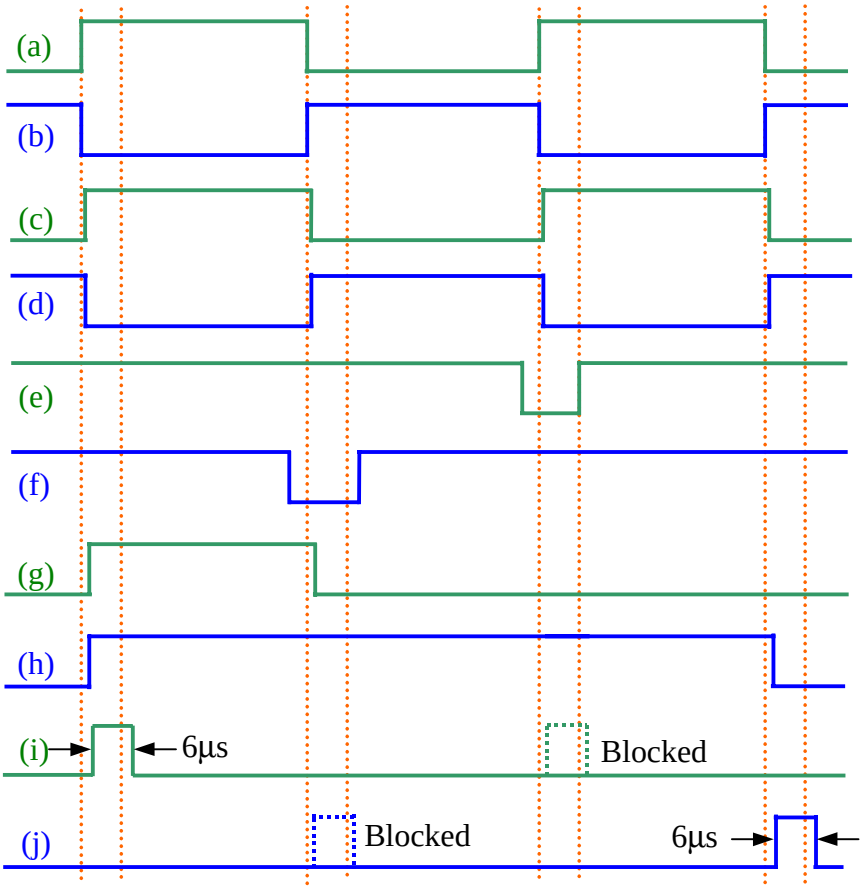


Fig.A-27 Waveforms of auxiliary switch gate signal generating circuit

A.3.8 Short circuit protection circuit

The function of this circuit is to receive the short circuit signal from the main-switch gate driver boards and to shut down all the gate signals. The key chip is CD4044B tri-state NAND R/S latches. It can generate and latch the shutdown signals, and can be reset manually by pressing a reset button added to the circuit. The circuit is shown in Fig.A-28.

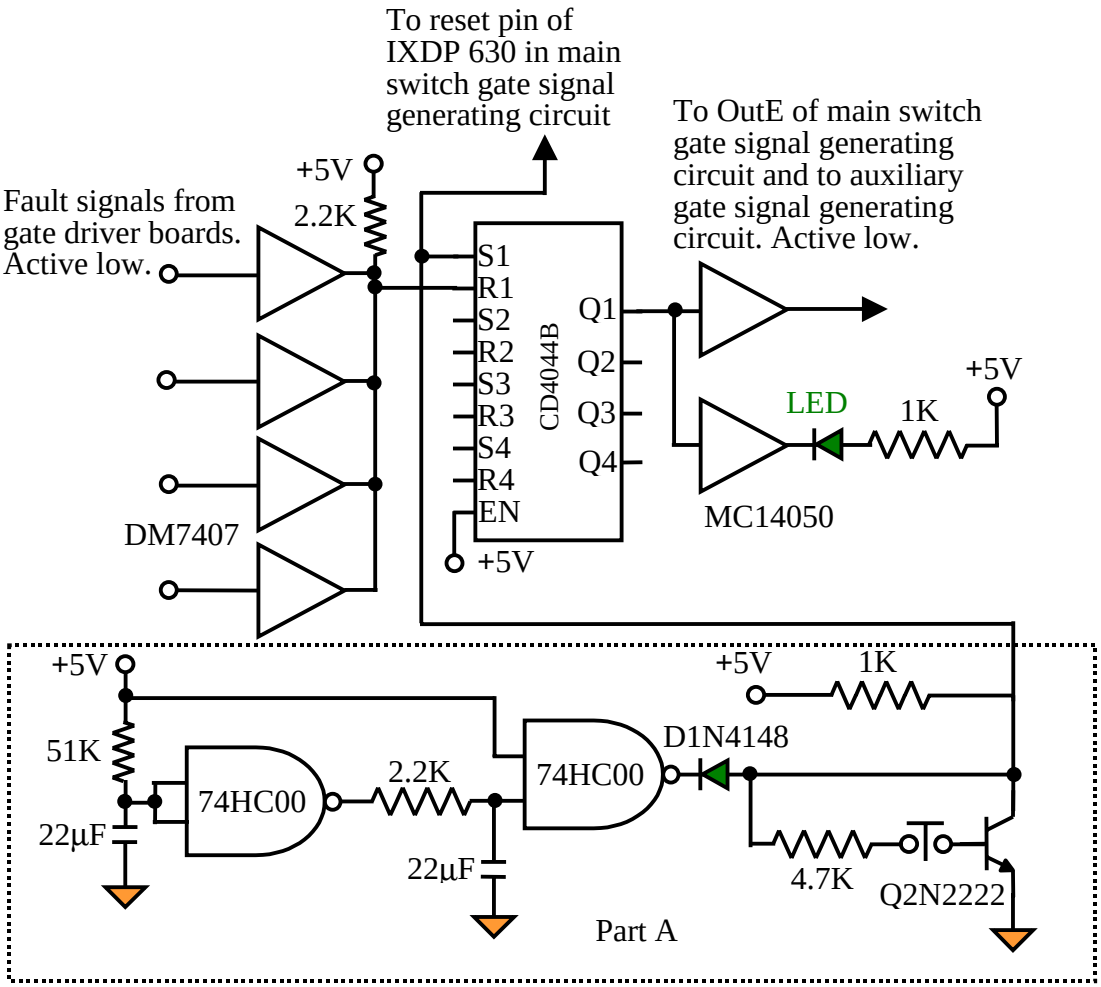


Fig.A-28 Short circuit protection circuit

DM7407 is open collector non-inverting buffer. NC14050 is hex non-inverting buffer. LED is used to indicate fault of the circuit. The truth table of CD4044B NNAD R/S latches is shown as follows:

S	R	E	Q
X	X	0	OC
1	1	1	NC
0	1	1	1
1	0	1	0
0	0	1	ΔΔ

OC: Tri-state

NC: No changes

X: Don't care

ΔΔ: Dominated by R=0 input

Table A-1 CD4044B truth table

The normal status is S=1, R=1, Q=1. When a fault is detected, R changes from 1 to 0, Q changes from 1 to 0. Even when R changes back from 0 to 1, Q will stay at 0 without changes. When fault signal is removed, R becomes 1, Q can be reset to 1 by manually setting S to 0, then when S changes back to 1, Q will stay at 1.

Over voltage and over current protection function can also be added to this circuit.

The part A in Fig.A-25 provides alternate input of 1-0-1 for S to set Q to 1 when the circuit starts up.

Fig.A-29 shows the variable timing control effect and the shut-down of auxiliary switch gate signal when load current is high enough.

Fig.A-30 shows the picture of the control interface board.

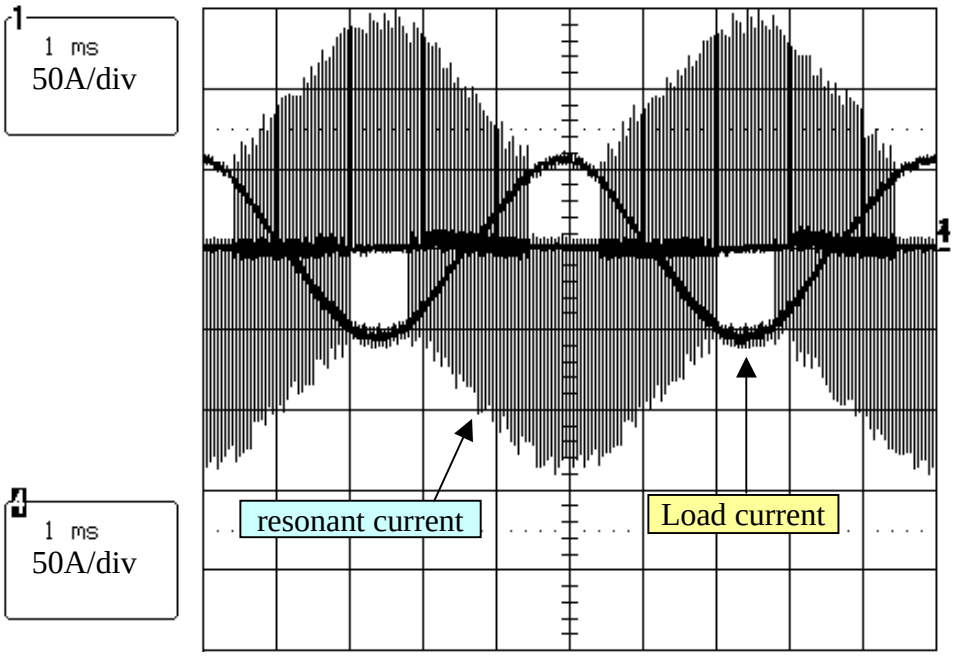


Fig.A-29 Resonant current is blocked when load current is high enough

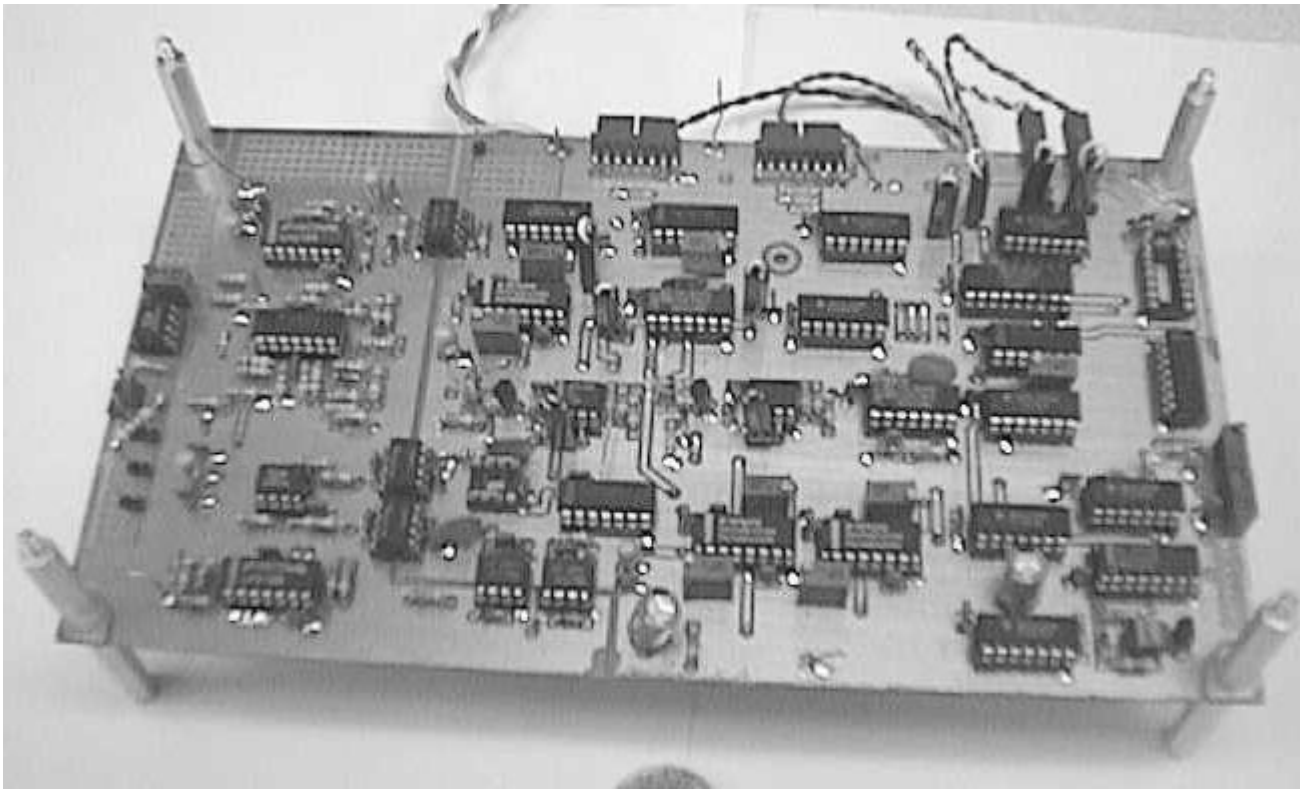


Fig.A-30 Control interface board

VITA

Yuqing Tang

The author was born in Beijing, China. He received his B. S. degree in Electrical Engineering from Tsinghua University in 1990. From 1990 to 1992 he worked as a research assistant in E. E. Dept. of Tsinghua University. In 1995 he received his M. S. degree in Power Systems area from the E. E. Dept. of Tsinghua University. He began his study in Virginia Polytechnic Institute and State University from August 1995. In May 1996, he joined Virginia Power Electronics Center as a research assistant and study towards a M. S. degree in Power Electronics area. His current research interests are high power inverter EMI prediction and reduction, DC-DC converter analysis and design.