Current Sharing Method for Resonant DC-DC Transformers

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Abstract

An ever present trend in the power conversion industry is to get higher performance at a lower cost. In a computer server system, the front-end converter, supplying the load subsystems, is typically a multiple output power supply. The power supply unit is custom designed and its output voltages are fully regulated, so it is not very efficient or cost effective. Most of the load systems in this application are supplied by point-of-load converters (POLs). By leaving the output voltage regulation aspect to POLs, the front-end converter does not need to be a fully regulated, multiple output converter. It can be replaced by a dc-dc transformer (DCX), which is a semi-regulated or unregulated, single output dc-dc converter. A DCX can be made using a modular design to simplify expansion of the system capacity. To realize this concept, the DCX block must have a current sharing feature.

The current sharing method for a resonant DCX is discussed in this work. To simplify the system architecture, the current sharing method is based on the droop method, which requires no communication between paralleled units. With this method, the current sharing error is inversely proportional to the droop voltage. In traditional DCX implementations, the droop voltage depends on the resistive voltage drops in the power stage, which is not sufficient to achieve the desired current sharing error. The resonant converter has the inherent characteristic that its conversion gain depends on the load current, so the virtual droop resistance can realized by the resonant tank and the droop voltage can be obtained without incurring conduction loss. An LLC resonant converter is investigated for its droop characteristic. The study shows the required droop voltage is achievable at very high switching frequency. To lower the switching frequency,

a notch filter is introduced into the LLC resonant tank to increase the sensitivity of the conversion gain versus the operating frequency. The design of the multi-element resonant tank is discussed. Depending solely on the resonant tank, the droop characteristic is largely varied with the component tolerance in the resonant tank. The current sharing error becomes unacceptable. The active droop control is imposed to make the output regulation characteristic insensitive to the component tolerance. The proposed resonant DCX has simpler circuit structure than the fully regulated resonant converter. Finally simulation and experimental results are presented to verify this concept.

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1. Introduction

Data centers are continually expanding around the world due to the increase in internet usage. Their operating cost consists mainly of the energy costs. Computer servers consume the majority of the electrical energy at the typical data center. As the energy production becomes more and more expensive, the computer servers require increasingly energy-efficient design.

In the typical computer server, the power delivery path from the input to the load subsystems is generally equipped with a front-end converter and multiple point-of-load converters (POL). The front-end converter is a fully-regulated multiple-output power supply for providing the power to the system board, the hard drives and the cooling fans. The system board employs many POLs to locally regulate the load subsystem voltages. The front-end converter is no longer involved in load voltage regulation. From this configuration, we can see that the front-end power supply does not need to be a fully regulated type of power supply. The traditional front-end converter could be replaced by a dc-dc transformer (DCX), a semi-regulated or unregulated single-output dc-dc converter. POLs on the system board generally accept the input of 12 V±10%. Being a single-output design with the standard voltage of 12 V, the DCX can be made as a standard product. The modular design concept allows system expansion without entirely re-designing the unit. To realize the modular design, each DCX unit should have current sharing capability. This work investigates the current sharing issue and the simplified implementation of the DCX.

1.1. Review of the power architecture in the computer servers

The distributed power architecture is common in the computer systems today. As shown in Figure 1.1, the power system comprises two parts; a front-end power supply and POLs located

on the system board [1]. The front-end unit can be separated into two blocks; a power factor correction stage (PFC) and an isolated dc-dc converter. The PFC stage converts the ac input voltage into the dc voltage of 400 V for the isolated dc-dc stage. The dc-dc converter stage in the front-end unit is typically a fully-regulated multiple output dc-dc converter.

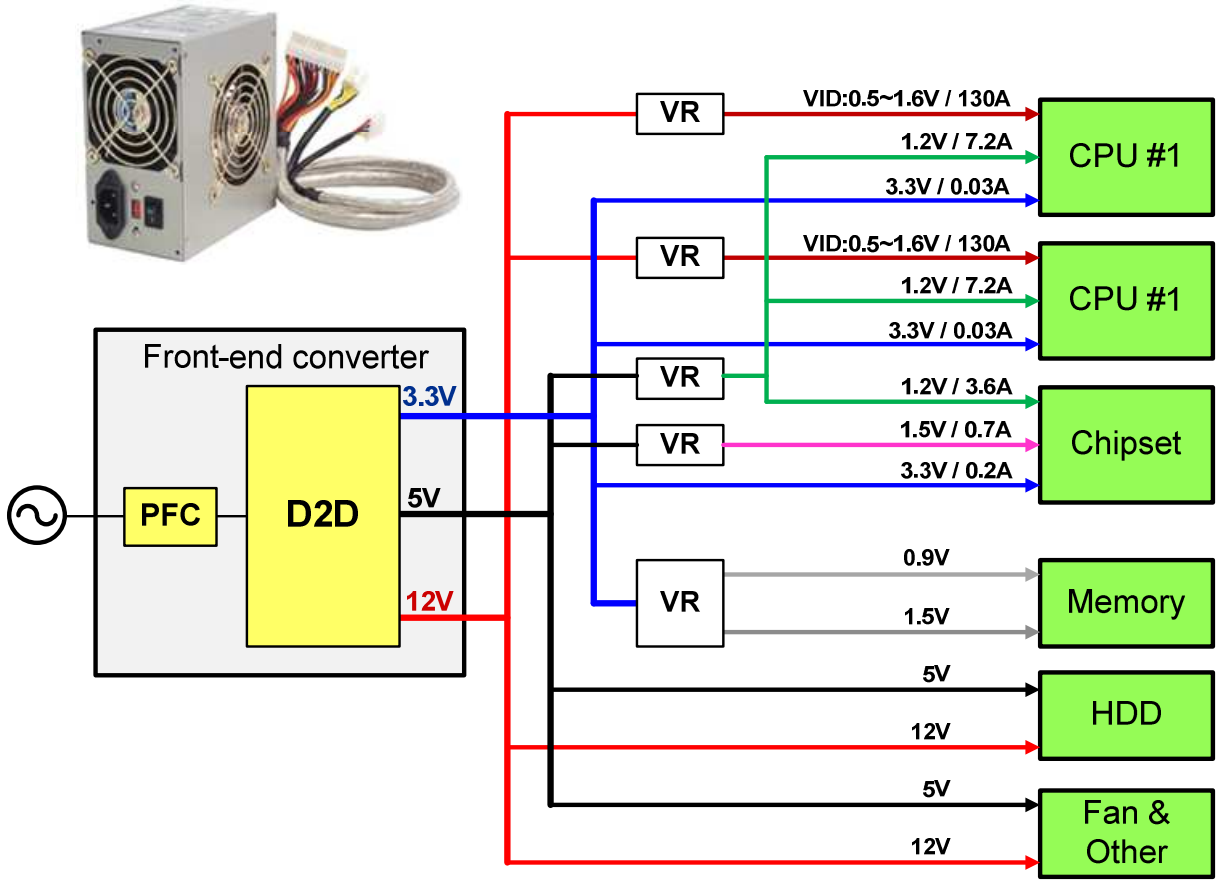

Figure 1.1 State-of-the-art power architecture in the computer server systems

In Figure 1.1, we can see that most of the outputs from the front-end power supply do not go to the load directly. The load subsystems are mostly fed and regulated by POLs. For this reason, the isolated dc-dc stage does not have to be the fully regulated multiple output type; it can be substituted by the DCX.

Recently Intel has proposed a 400 Vdc direct distribution bus for data center applications in order to reduce the number of power conversion stages and power loss in the power distribution

path [2], as shown in Figure 1.2. By eliminating an ac uninterruptible power supply (UPS) and a transformer in the power distribution unit (PDU), the overall efficiency can be improved by 3-5%.

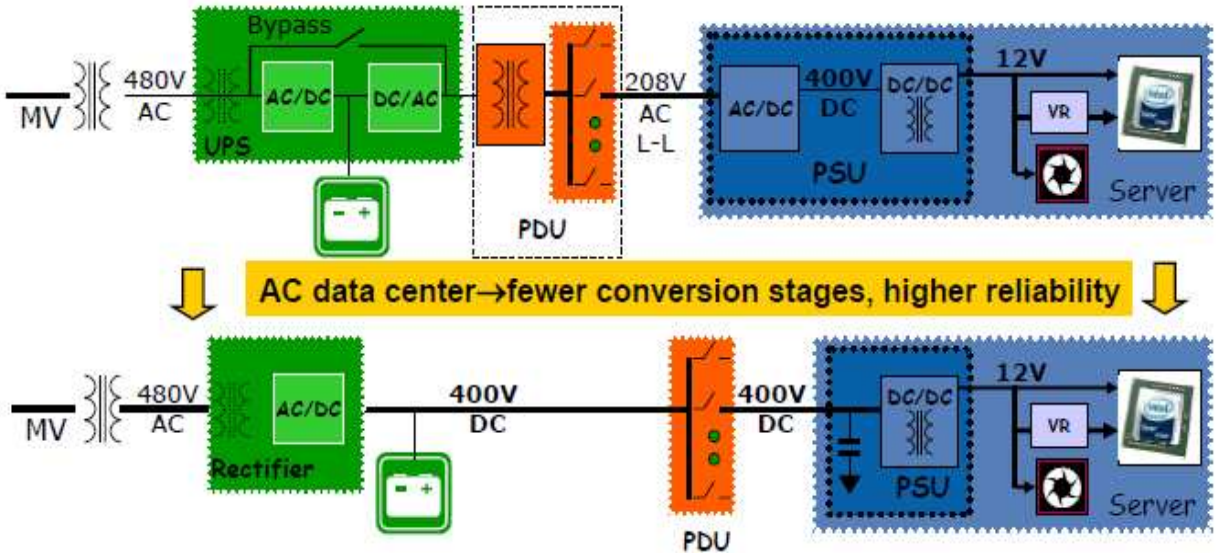

Figure 1.2 Traditional ac distribution and an emerging 400-Vdc distribution for data centers

With the emerging 400 Vdc bus and the proposed front-end unit based on DCX, the alternative power architecture can be depicted using Figure 1.3.

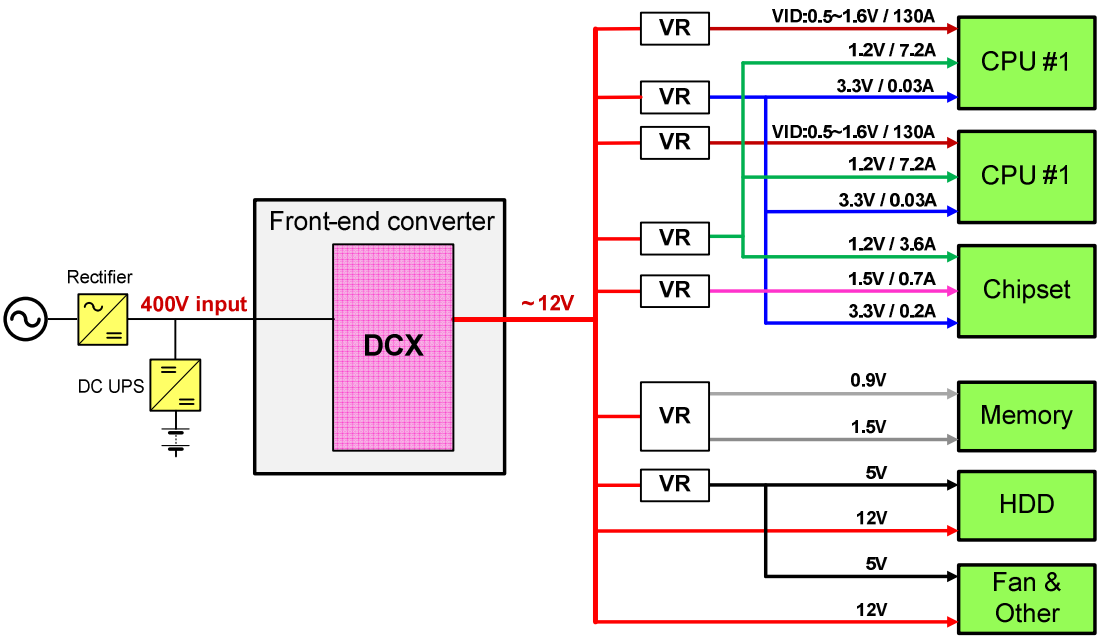

Figure 1.3 Alternative power architecture based on DCX

Since the DCX block has a standard input and output voltage and becomes a single output design, it can be made as using a modular design. Then, the standard DCX module can be fully optimized for both efficiency and cost. The modular design allows system capacity expansion with reduced engineering effort. The system can get better efficiency at a potentially lower cost. Figure 1.4 shows the proposed power architecture based on the modularly designed DCX.

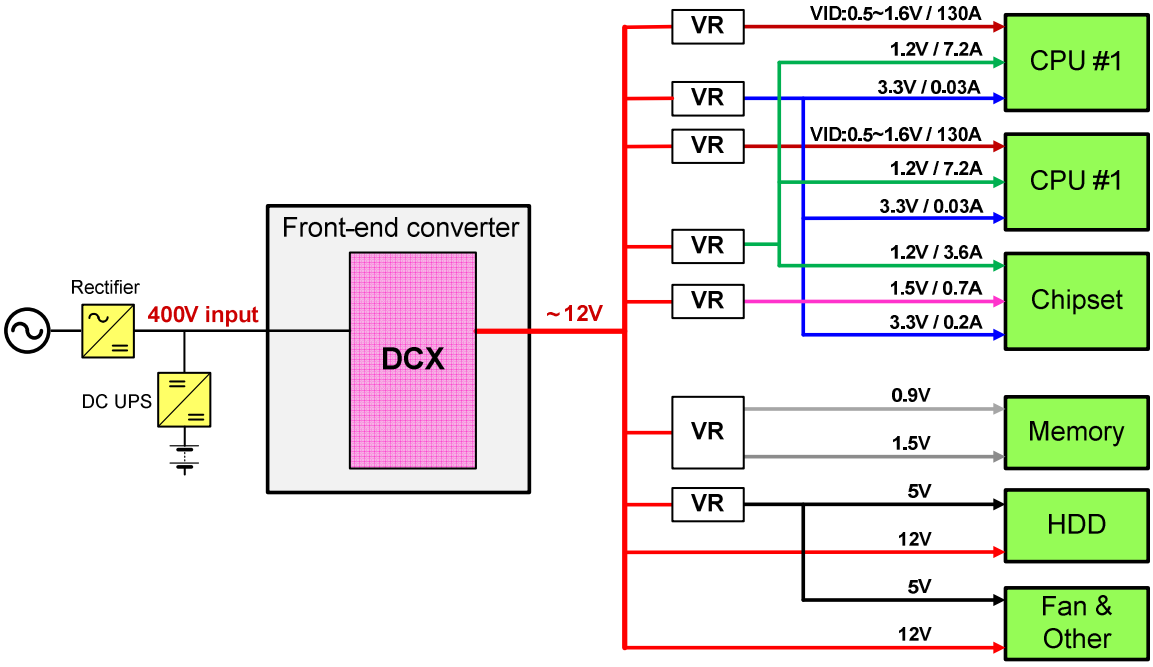

Figure 1.4 Scalable power architecture based on the modular designed DCX

1.2. LLC resonant converter

In this work, a 300-W DCX module having 400 V input and 12 V, 25 A output is going to be developed to demonstrate the power system architecture based on the modular designed DCX. At this power level, the half bridge structure seems to be a suitable choice [3]. Two popular topologies based on the half-bridge structure are a half-bridge PWM converter and a half-bridge resonant converter.

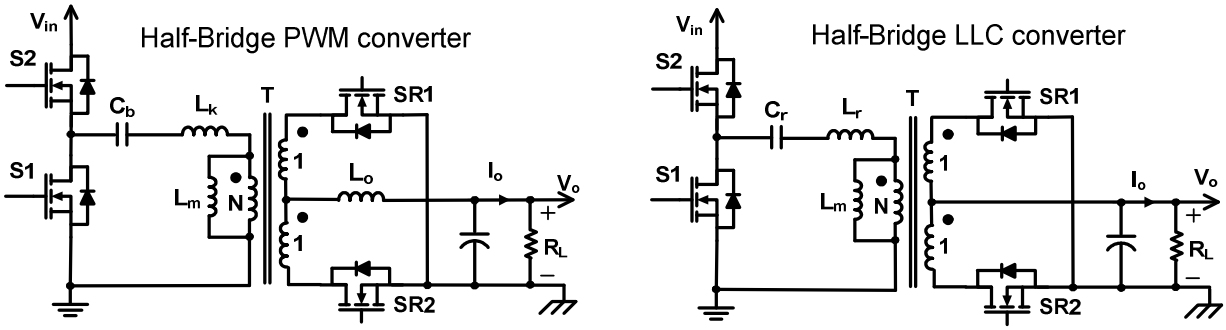

Figure 1.5 Half-bridge DCX topologies

The half-bridge PWM converter designed for DCX application operates at 50% duty cycle and achieves zero voltage switching (ZVS) by either using the energy stored in the leakage or the magnetizing inductance of the transformer. Using the energy in the leakage inductance, the converter may lose ZVS at light load and require a high voltage rating for the synchronous rectifier (SR) due to the resonance between its junction capacitor and the leakage inductance of the transformer. The design with low magnetizing inductance can achieve ZVS for the entire load range. This approach yields lower voltage stress on the output rectifier but suffers from higher conduction loss on the primary side because the magnetizing current has to be equal to the load current reflected to the primary side [4].

The half-bridge LLC resonant converter is basically a series resonant converter with finite magnetizing inductance. The magnetizing current facilitates ZVS for whole load range. The circuit has three operational modes [5]; these are at the resonant frequency, below the resonant frequency, and above the resonant frequency.

The first mode is the operation at the resonant frequency. The key waveforms of this operation mode are shown in Figure 1.6. In this mode, the converter operates at the most efficient point. The primary switches (S1, S2) work in ZVS condition and the output rectifiers (SR1, SR2) work in zero current switching (ZCS) condition. The current transfers to the secondary side circuit for the entire half-switching cycle. The RMS currents on both the primary and secondary sides are the lowest. The currents in the secondary-side circuit or in the output rectifier are in-phase with the primary driving signal, so the synchronous rectifier can be driven by the primary driving signal. The slope of the current in SR during turn-off is small due to ZCS operation and the perfect synchronous rectifier driving signal is easy to obtain, so the body diode conduction and reverse recovery loss are minimal

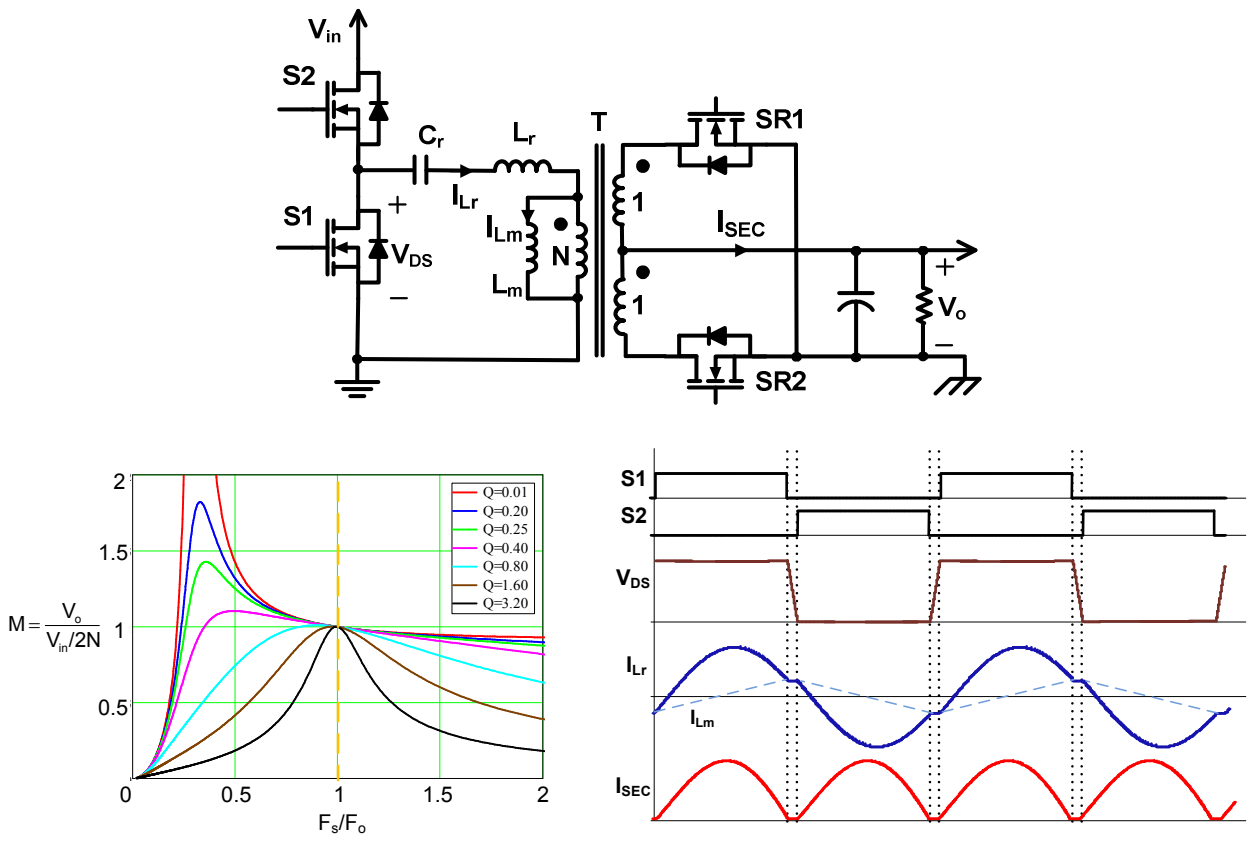

Figure 1.6 Key waveforms of the LLC resonant converter running at the resonant frequency

The second mode of operation of the half-bridge LLC resonant converter is operation below the resonant frequency. The key waveforms are shown in Figure 1.7. The primary switches work in ZVS condition and the output rectifiers work in ZCS condition. The current transfers to the secondary side circuit for a period that is less than 50% of the duty cycle. The RMS current on both the primary and secondary sides are higher than the current in the LLC circuit running in the first mode. From Figure 1.7, we can see that the current in the output rectifier reaches zero before the primary switches are turned off. Therefore, the current flowing in SR FET is needed to generate the proper driving signal [6]. The current is indirectly sensed by the voltage drop across the drain-source terminal of the SR FET. The parasitic inductance in the package of the SR FET will cause the driving signal to turn off the SR device earlier than expected, which incurs body

diode conduction loss and reverse recovery loss. This issue can be alleviated using a complicated compensation circuit.

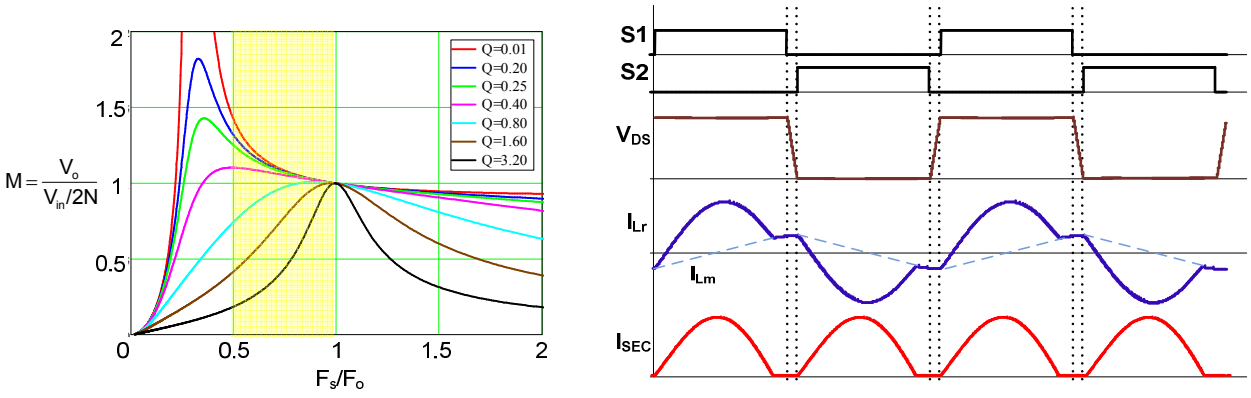

Figure 1.7 Key waveforms of the LLC resonant converter running below the resonant frequency

The third mode of operation of the half-bridge LLC resonant converter is operation above the resonant frequency. The key waveforms are shown in Figure 1.8. The primary switches work in ZVS condition. The output rectifiers are not turned off under ZCS condition. The turn-off di/dt of SR FET in this operation mode is much higher than that in the other two modes, which results in higher reverse recovery loss. The RMS currents on both the primary and secondary sides are lower than the currents in LLC circuit running below the resonant frequency because the current flows in the secondary side for the entire half cycle. The synchronous rectifier driving scheme for this mode can be as simple as the implementation for the circuit running at the resonant frequency.

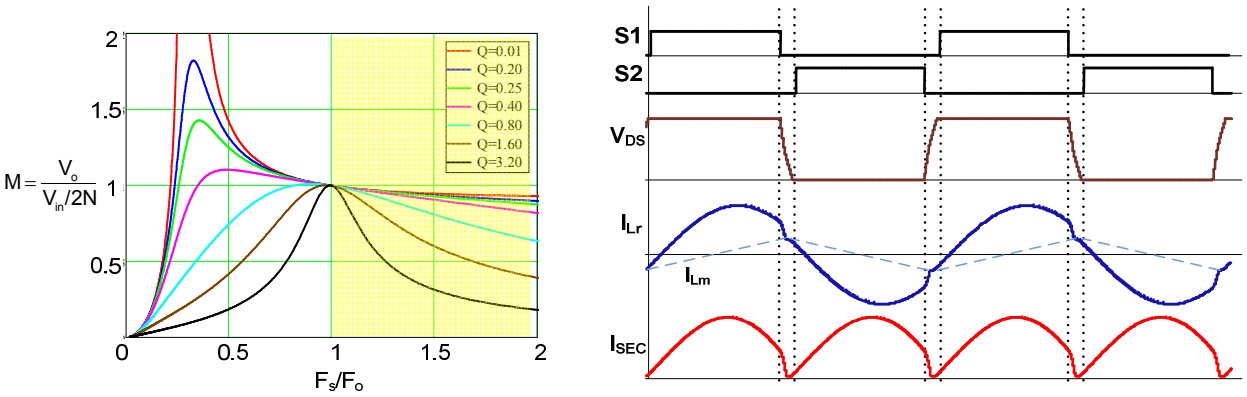

Figure 1.8 Key waveforms of the LLC resonant converter running above the resonant frequency

In this work, operation at the resonant frequency or above the resonant frequency is selected, as using this mode of operation means that the synchronous rectifier driving scheme is less complicated. This circuit is expected to have similar or better performance than the traditional LLC resonant converter working below the resonant frequency with much simpler circuit structure.

1.3. Current sharing technique

To realize a power distribution system based on the modular DCX concept, the DCX module must have current sharing (CS) capability. The available current sharing techniques can be categorized into 2 schemes, an active current sharing method and a droop current sharing method [7].

In the active current sharing method, there are a current sharing bus and a current sharing controller to ensure the current balance between the paralleled power supplies. The current sharing controller compares the output current of the unit with the current reference command derived from the current sharing bus. The presence of the current sharing bus poses some difficulty in parallel operation of the power supplies. The stability issue of the whole system must be considered carefully when the feedback control used. Moreover, the modules from the

different vendors cannot be paralleled together due to incompatible current sharing bus definitions and different control loop design characteristics.

The droop method relies on the slope of the load regulation characteristic of the paralleled converters [8]. The output voltage droops as the load current is increased. Its operation mechanism is to program the output impedance to achieve current sharing among converters. To demonstrate the droop current sharing approach, Figure 1.9 shows the parallel connection of two power supplies, which have a slight mismatch in the output voltage set point. As can be seen from Figure 1.9, the unit#1 having a higher output voltage setpoint carries more load current than the unit#2.

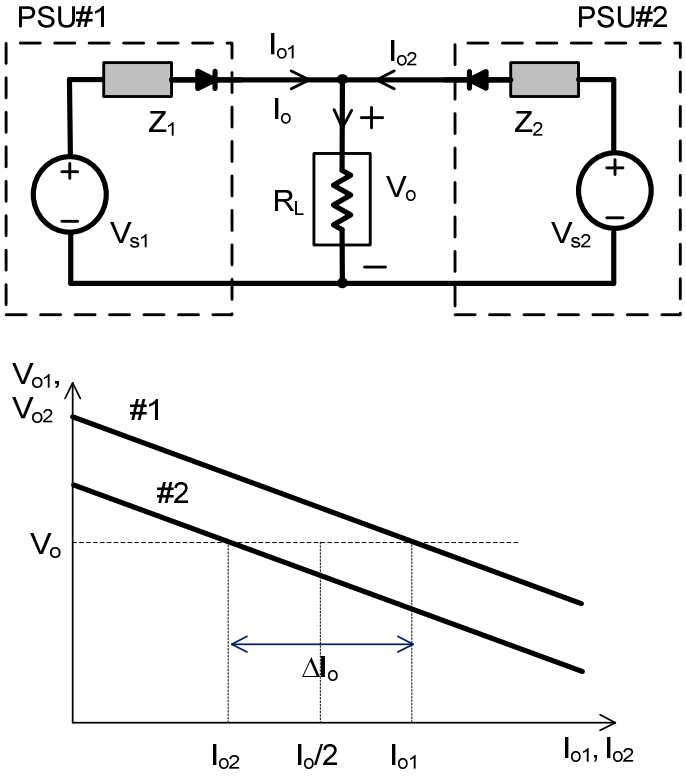

Figure 1.9 Droop current sharing

Generally, the current sharing error, which is the difference between the output current of the individual units, is determined by the magnitude of the output voltage setpoint error and the slope of their regulation characteristic.

Figure 1.10 shows the effect of the current sharing error from the mismatch in the setpoint voltage. The current sharing error is reduced as the setpoint tolerance becomes smaller. Figure 1.11 shows the effect of the load regulation characteristic slope to the current sharing error. The current sharing error is improved with a larger droop characteristic. It should be noted that the current cannot be shared among the paralleled units with an ideal voltage source characteristic.

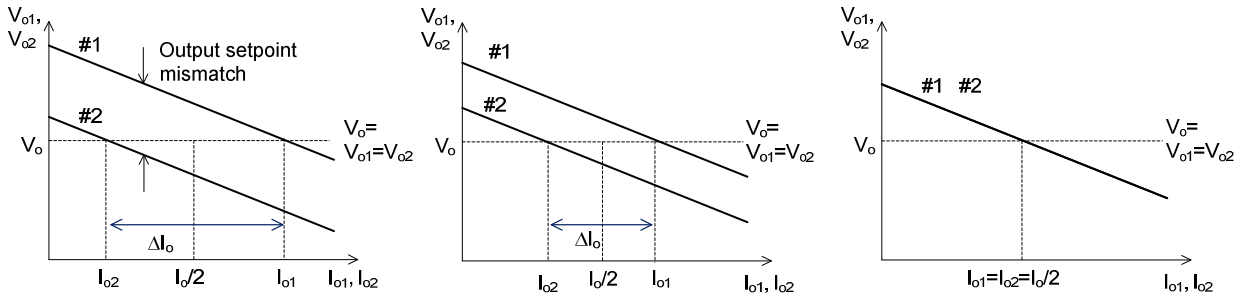

Figure 1.10 Effect of output voltage setpoint mismatch on the current sharing error

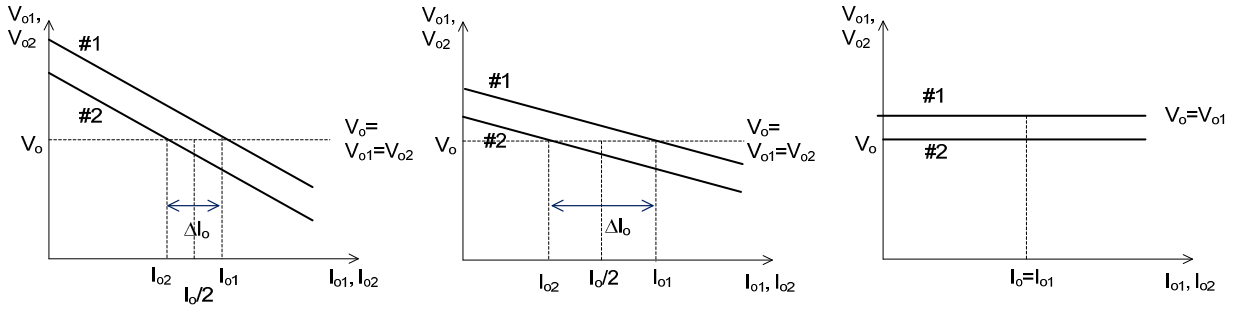

Figure 1.11 Effect of output regulation characteristic slope on voltage on the current sharing error

The resonant converter having the load dependent output regulation characteristic was identified as a suitable implementation for the current sharing operation [9], but the current sharing performance with the component tolerance was clearly addressed. The current sharing

operation of LLC was demonstrated in [10]. The inherent current sharing property of the LLC resonant converter was claimed but the effect of the component tolerance in the resonant tank to the current sharing performance was not mentioned. This problem is the main subject of the work in [11]. The 3-phase power circuit with floating star connection and the phase control scheme are proposed to deal with the component tolerance. However, this approach is not suitable for the modular designed DCX since it requires the dedicated master controller.

1.4. Thesis organization

This thesis focuses on a current sharing method for the resonant DCX. The topology for the DCX is based on the LLC resonant converter. The effect of the component tolerance is investigated. The solution to the component tolerance is proposed. The merit of the proposed DCX is discussed and compared with the fully regulated resonant dc-dc converter.

Chapter 1 has provided an overview of the state-of-the-art power architecture in the computer server, the LLC resonant converter, and current sharing methods. The current sharing performance of the resonant DCX and the concept of the passive droop are discussed in Chapter 2. A multi-element resonant tank is proposed to improve the current sharing performance and efficiency. The design of the multi-element resonant is also addressed. Chapter 3 proposes an active droop current sharing method to deal with the component tolerance in the converter. The circuit complexity related to the SR driving scheme of the fully-regulated resonant converter (D2D) and DCX is discussed in Chapter 4. Finally Chapter 5 is the conclusion and a summary of possible future works.

2. Passive droop current sharing method

The current sharing performance of the resonant converters is investigated in this chapter. The required additional droop is quantified. The passive droop method creating the additional droop voltage by means of the resonant tank is discussed. The multi-element resonant tank is employed to improve the overall efficiency. Finally the effect of the passive component tolerance is evaluated.

2.1. Current sharing in LLC resonant converter

The LLC resonant converter has three operational modes as described in Chapter1. To simplify the SR driving scheme, the operation at the resonant or above resonant frequency is considered to realize a modular DCX.

The current sharing method employed in this work is based on the droop current sharing method. The desired output regulation characteristic to facilitate the droop current sharing is depicted in Figure 2.1

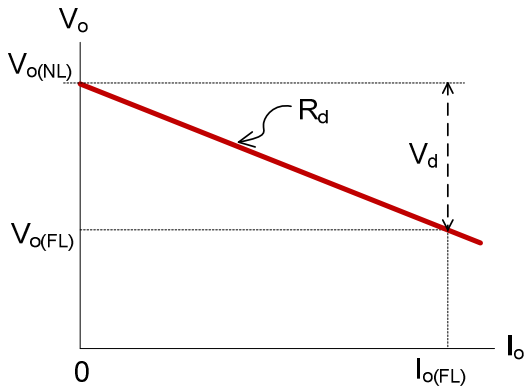

Figure 2.1 Output regulation characteristic for the droop current sharing

The droop voltage and droop resistance are defined as

$$V_d = V_{o(NL)} - V_{o(FL)} \tag{2.1}$$

$$R_d = V_d / I_{o(FL)} \tag{2.2}$$

, where $V_{o(NL)}$ and $V_{o(FL)}$ are the no-load and full-load voltage respectively. $I_{o(FL)}$ is the rated full-load current.

The LLC-DCX is the most efficient when running at the resonant frequency, so the LLC-DCX operating at the resonant frequency should be a suitable implementation for a DCX with current sharing capability. The conversion gain M of the resonant converter is defined as

$$M = \frac{V_o}{V_{in}/2N} \tag{2.3}$$

, where V_{in} is the input voltage and N is the transformer turn-ratio.

The conversion is unity at the resonant frequency. The dc equivalent circuit is shown in Figure 2.1. R_o is the equivalent droop resistance, which depends on the on-state resistance of the primary switches R_S, the on-state resistance of the synchronous rectifiers R_{SR}, the primary side winding resistance R_{PRI}, and the secondary side winding resistance R_{SEC}.

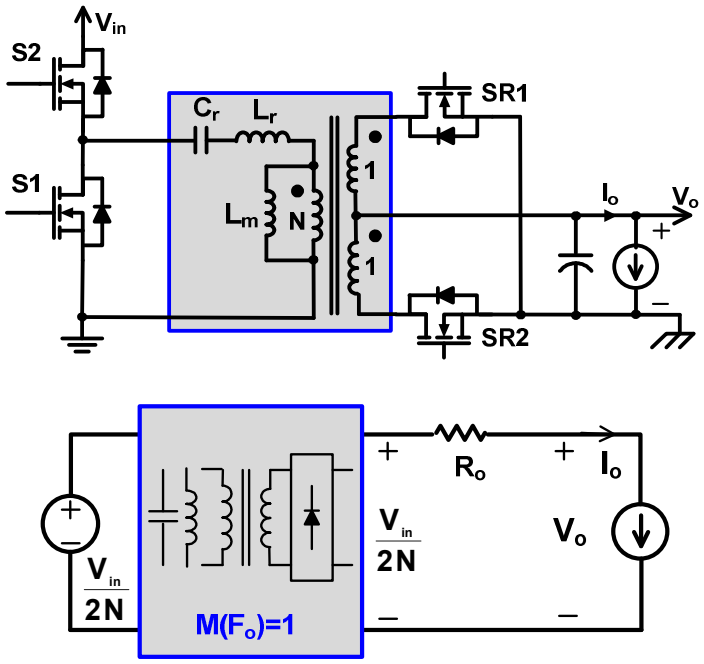

Figure 2.1 DC equivalent circuit of the LLC converter running at the resonant frequency

From Figure 2.1, the output voltage of the LLC resonant converter running at the resonant frequency and the equivalent droop resistance can be expressed as

$$V_o = \frac{V_{in}}{2N} - I_o R_o \tag{2.4}$$

$$R_o = \frac{\pi^2}{8}\left(\frac{R_S + R_{PRI}}{N^2} + R_{SEC} + R_{SR}\right) \tag{2.5}$$

The slope of the output regulation characteristic or the equivalent droop resistance of each unit depends on the parasitic resistances of the power stage. Any mismatch in the equivalent droop resistance will cause the current sharing error. The typical tolerance of the on-state resistance in MOSFET is in the range of ±22%. The tolerance of the winding resistance in wounded magnetic component is typically at ±10%.

In this 300-W DCX design, the resistances of the power components and their tolerances are shown in Table 2.1

Table 2.1: Resistance and tolerance of the power stage

Device	**Resistance**	**Tolerance (%)**
S1,S2 (R_S)	0.37 Ω	±22%
SR1, SR2 (R_{SR})	1.4 m Ω	±22%
Primary winding (R_{PRI})	80 m Ω	±10%
Secondary winding (R_{SEC})	1.4 m Ω	±10%
Effective droop res. (R_o)	5.4 m Ω	±17.4%

The effective droop resistance of this DCX (R_o) is 5.1 mΩ and its tolerance (t) is 17.4%.

The relative current sharing error is defined as the difference between the output current of individual unit normalized by the average current from N_p paralleled units.

$$CS_{error} = \frac{\Delta I_o}{I_o/N_p} \tag{2.6}$$

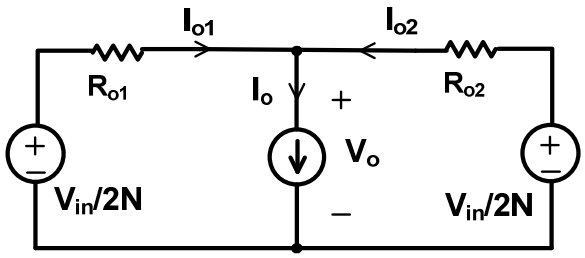

Figure 2.2 Equivalent circuit of two paralleled DCX

A system of two paralleled units is studied. The equivalent circuit of two parallel connected DCX can be shown in Figure 2.2. The current in the module#1 and the module#2 are

$$I_{o1} = \frac{R_{o2}}{R_{o1}+R_{o2}} \tag{2.7a}$$

$$I_{o2} = \frac{R_{o1}}{R_{o1}+R_{o2}} \tag{2.7b}$$

The current sharing error can be derived as

$$CS_{error} = \frac{\Delta I_o}{I_o/2} = \frac{R_{o2}-R_{o2}}{(R_{o1}+R_{o2})/2} \tag{2.8}$$

R_{o1} and R_{o2} are denoted as the effective droop resistance of the module#1 and module#2 respectively, which have the tolerance (t) of -17.4% and +17.4% respectively. R_o is the nominal droop resistance of the power stage. Then R_{o1} and R_{o2} equal to $R_o(1-t)$ and $R_o(1+t)$ respectively. The relationship between the current sharing error and the tolerance of the droop resistance is

$$CS_{error} = 2 \cdot t \tag{2.8}$$

The current sharing of 10% is commonly required in the industry. With the typical tolerance in the droop resistance in the power stage of ±17.4%, the current sharing error becomes unacceptably large as 34.7%.

The current sharing error can be improved by having a higher droop resistance, which can be simply done by adding an additional resistor R_{oe} to the output circuit of each unit, as shown in

Figure 2.3. To meet the current sharing error of 10%, R_{oe} can be calculated to be 13.5 mΩ, which corresponds to the additional droop voltage of 0.34 V at the output current of 25 A. This approach incurs excessive power loss.

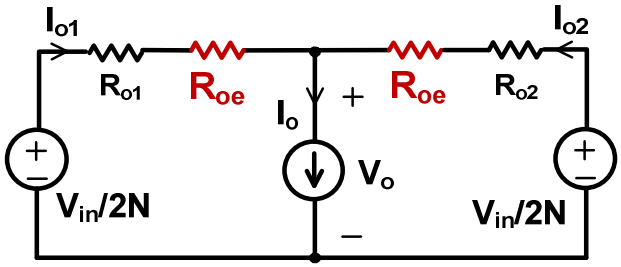

Figure 2.3 Current sharing improvement by adding the droop resistor R_{oe}

2.2. Virtual droop resistance concept

The virtual droop resistance concept is proposed to implement the additional droop resistance without excessive conduction loss. The conversion gain of the resonant converter operating above or below the resonant frequency is the function of the load current. The conversion gain reduces as the load increases, so the resonant converter has an inherent droop characteristic.

The operation above the resonant frequency is chosen to simplify the circuit design as previously discussed. The equivalent circuit of the converter in this operating region is shown in Figure 2.4. Let $M_{NL}(F)$ and $M_{FL}(F)$ be the conversion gain of the resonant converter at no-load and full-load conditions.

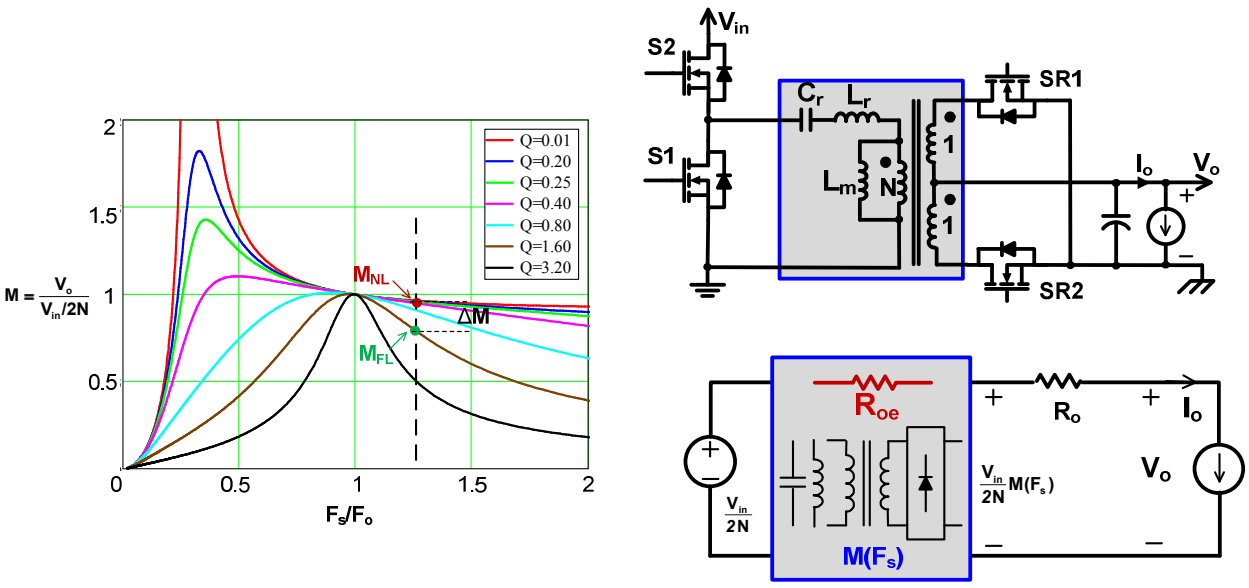

Figure 2.4 DC equivalent circuit of the LLC converter running above the resonant frequency

The output voltages at no-load and full-load conditions are

$$V_{o(NL)} = \frac{V_{in}}{2N} M_{NL}(F_s) \tag{2.9}$$

$$V_{o(FL)} = \frac{V_{in}}{2N} M_{FL}(F_s) - I_{o(FL)} R_o \tag{2.10}$$

The droop voltage, as defined in (2.1), is

$$V_d = \frac{V_{in}}{2N} (M_{FL}(F_s) - M_{NL}(F_s)) + I_o R_o \tag{2.11}$$

Define the virtual droop resistance as

$$R_{oe} = \frac{\frac{V_{in}}{2N} M(F_s)}{\Delta I_o} = \frac{\frac{V_{in}}{2N} (M_{FL}(F_s) - M_{NL}(F_s))}{I_{o(FL)}} \tag{2.12}$$

Then the output voltage can be expressed as

$$V_o = \frac{V_{in}}{2N} M_{NL}(F_s) - I_o (R_o + R_{oe}) = V_{o(NL)} - I_o (R_o + R_{oe}) \tag{2.13}$$

As we can see from (2.12) and (2.13), the virtual droop resistance can be created by the characteristic of the resonant tank. The additional droop can be realized for the current sharing improvement without excessive power loss.

2.3. LLC resonant converter design for the current sharing operation

The LLC resonant converter with 400-V input and of 12-V, 25-A output is designed for the modular DCX with an inherent current sharing feature. The main power stage component is shown in Figure 2.5. To achieve ZVS from no-load to full-load, the total resonant inductance (L_r) of 10 μH and the magnetizing inductance (L_m) of 100 μH are chosen. The resonant frequency (F_o) is defined in (2.14) is designed at 500 kHz for a good trade-off between the efficiency and the physical size.

$$F_o = \frac{1}{2\pi}\sqrt{\frac{1}{L_r C_r}} \tag{2.14}$$

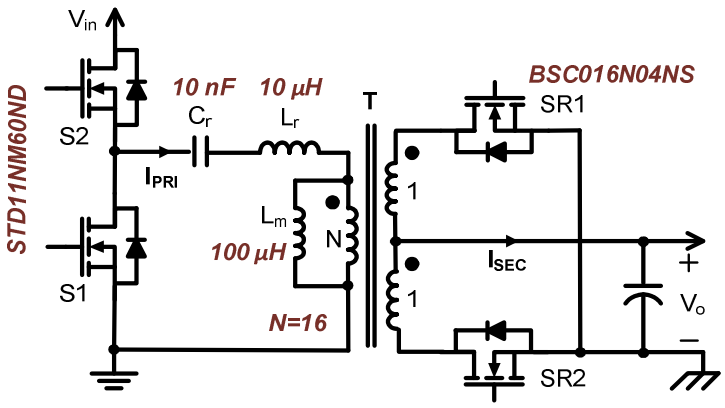

Figure 2.5 Power stage of the 300-W LLC DCX designed for current sharing application

The current on the secondary side (I_{SEC}) expanded in detail is depicted in Figure 2.6. As seen from the waveforms, the secondary side current continues to decrease with high di/dt after the primary switch is turned off. Using the primary driving signal to control the synchronous rectifier directly will cause the current flowing into the body diode which results in high body

diode conduction loss and reverse recovery loss. The falling edge delay circuit is added to alleviate these losses.

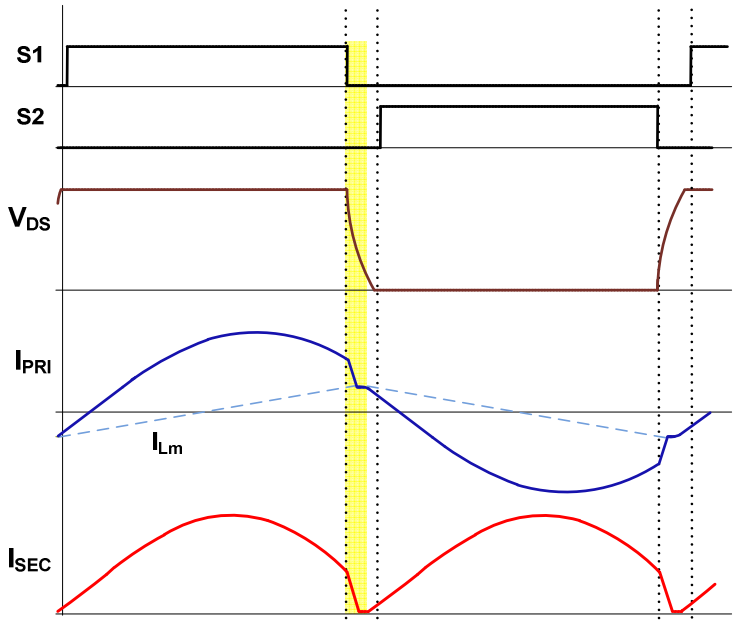

Figure 2.6 Detailed waveform of the LLC resonant converter running above F_o

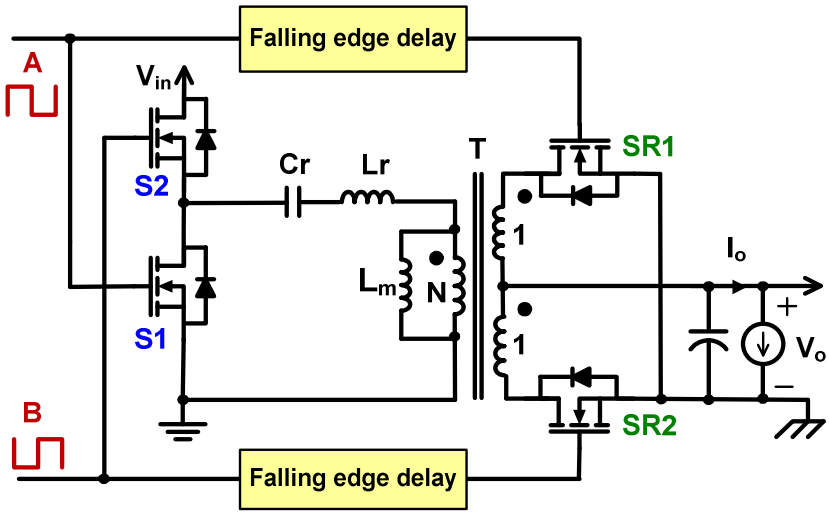

Figure 2.7 SR driving scheme for LLC DCX

Figure 2.8 shows the conversion gain of the designed LLC resonant converter and its corresponding output regulation characteristic. The converter has no droop characteristic at the

resonant frequency. To achieve the additional droop resistance of 13.5 mΩ or the droop voltage of 0.34 V, this converter has to run at 620 kHz.

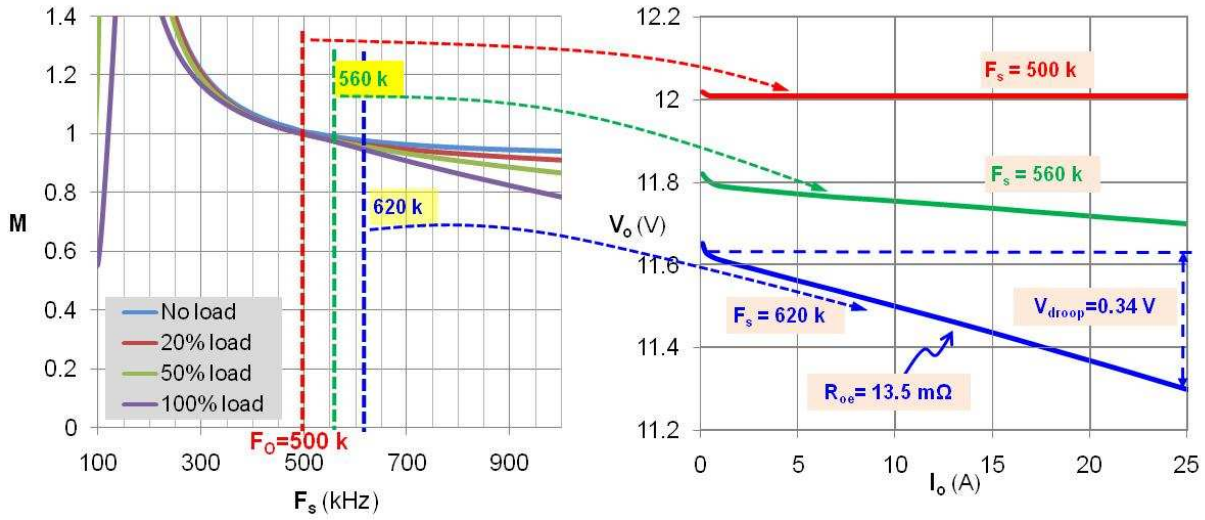

Figure 2.8 Conversion gain and output regulation characteristic of the LLC resonant converter

Figure 2.9 shows the operating waveform of the converter at 620 kHz. The deadtime in the SR driving signal of 20-30 ns is provided to accommodate the tolerance in the propagation delay of the MOSFET driver chips. The voltage spike in the SR FET is observed due to the turn-off with high di/dt. The loss model is created. The loss breakdown of this converter is shown in Figure 2.10. The test efficiency at 620 kHz as well as at the resonant frequency, 500 kHz is shown in Figure 2.11. The efficiency of the converter is dropped by 1.1% at full load in order to make to the droop characteristic suitable for the current sharing.

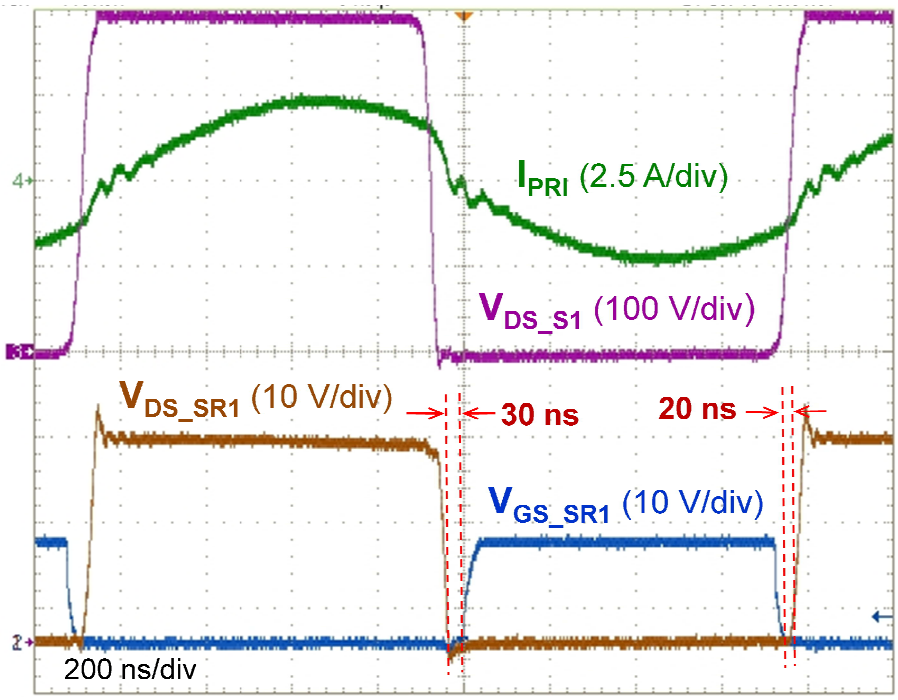

Figure 2.9 Operating waveform of the LLC resonant converter at 620 kHz

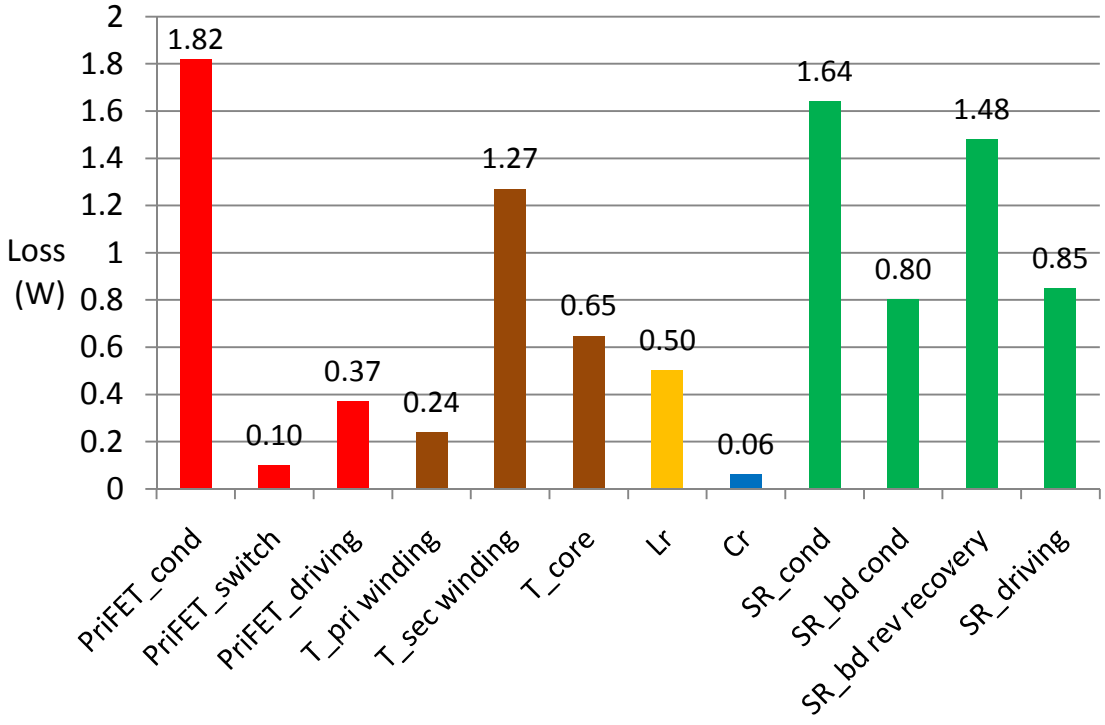

Figure 2.10 Loss breakdown for LLC DCX running at 620 kHz

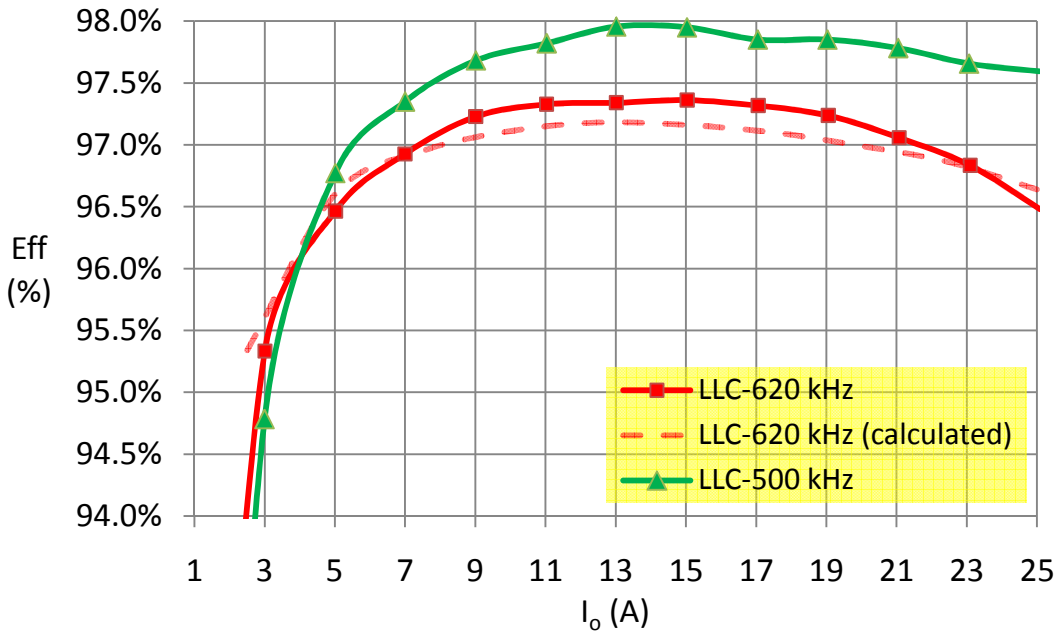

Figure 2.11 Efficiency of LLC DCX running at the resonant frequency and at 620 kHz.

The loss in the resonant converter is usually dominated by the conduction loss. Since the converter runs above the resonant frequency, the body diode conduction and reverse recovery losses are considerably large. These losses increase as the switching frequency moves farther away from the resonant frequency. It is desirable to keep the operating point of the resonant converter close to the switching frequency.

2.4. Multi-element resonant converter design for the current sharing operation

The operating point close to the resonant frequency is desirable for the best efficiency. A multi-element resonant tank proposed in [6] is considered. The multi-element resonant tank is the LLC tank with a notch filter. The circuit and typical frequency response are shown in Figure 2.12. This resonant tank has 3 critical frequencies F_{o1}, F_{o2}, and F_{o3} as shown below.

$$F_{o1} = \frac{1}{2\pi}\sqrt{\frac{L_sC_s+L_pC_p+L_pC_s-\sqrt{(L_sC_s+L_pC_p+L_pC_s)^2-4L_sC_sL_pC_p}}{2L_sC_sL_pC_p}} \tag{2.15}$$

$$F_{o2} = \frac{1}{2\pi}\sqrt{\frac{1}{L_p C_p}} \tag{2.16}$$

$$F_{o3} = \frac{1}{2\pi}\sqrt{\frac{L_s C_s + L_p C_p + L_p C_s + \sqrt{(L_s C_s + L_p C_p + L_p C_s)^2 - 4 L_s C_s L_p C_p}}{2 L_s C_s L_p C_p}} \tag{2.17}$$

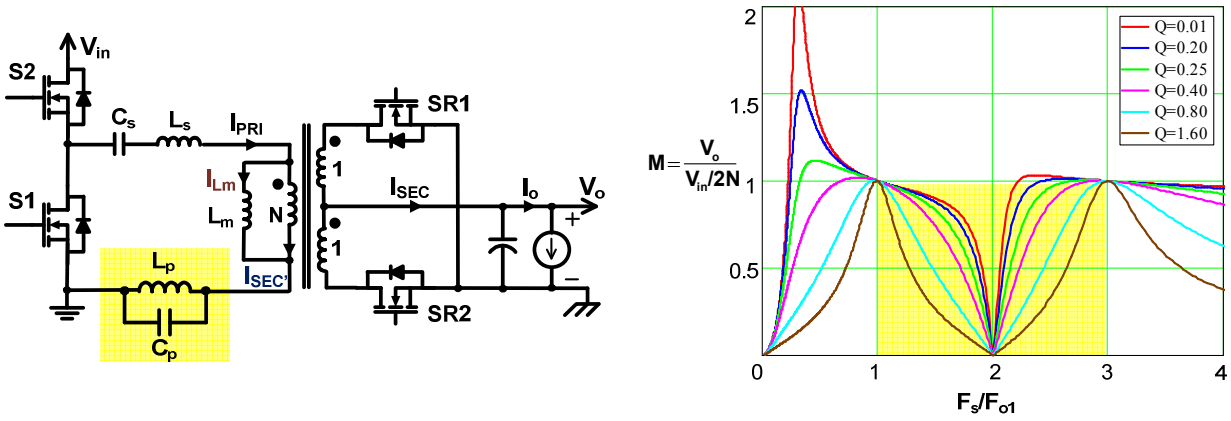

Figure 2.12 Multi-element resonant converter and conversion gain characteristic

F_{o1} is the bandpass frequency similar to the resonant frequency of the LLC tank (F_o) that lets the fundamental component of the current in the resonant tank pass thru the load. F_{o2} is the notch frequency, where the conversion gain is zero. F_{o3} is the higher bandpass frequency which allows the higher order harmonics current transfer to the load. The conversion gain above the resonant frequency, F_{o1}, is obviously more sensitive to the switching frequency than the gain of the LLC resonant tank due to the notch filter.

The primary current (I_{PRI}) in the resonant tank has two parts; the magnetizing inductance and the reflected load currents. The magnetizing current (I_{Lm}) is a triangular shape not depending on the position of F_{o2} and F_{o3}. The reflected load current ($I_{SEC'}$) is proportional to the load current and its wave shape highly depends on the position of F_{o2} and F_{o3}.

The conventional wisdom to design this resonant tank is to place F_{o2} at $2F_{o1}$ and F_{o3} at $3F_{o1}$. Due to the frequency selective nature of the resonant tank, the tank current excluding the magnetizing current mainly composes of the fundamental and the third harmonic component. At the resonant frequency, the fundament and third harmonic current are in-phase. The combination of these two components makes the current shape resemble to the square wave as shown in Figure 2.13.

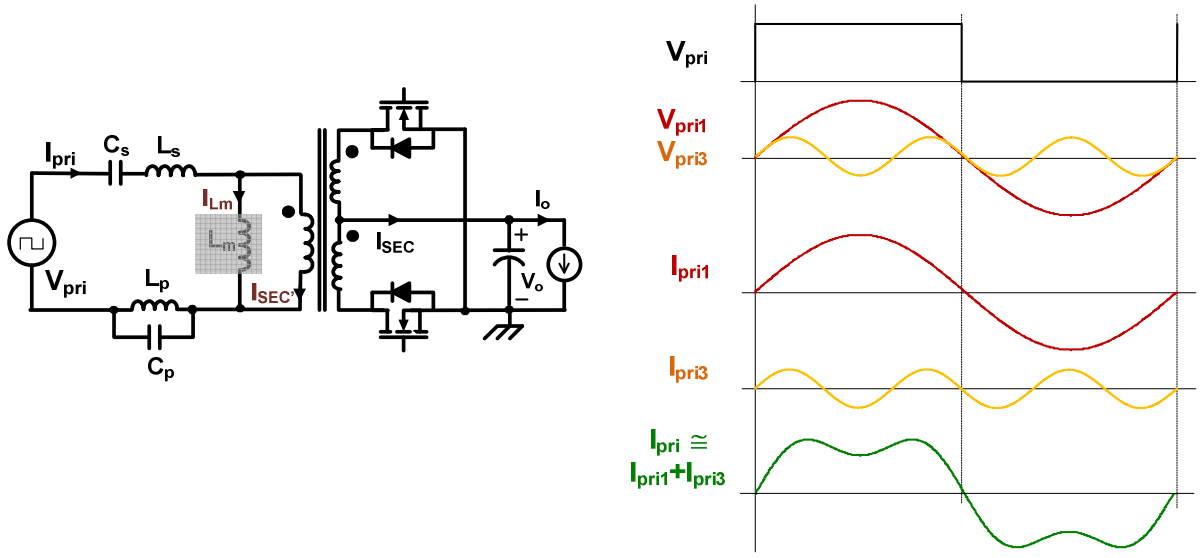

Figure 2.13 Current in the multi-element resonant tank, excluding the magnetizing current, at the resonant frequency

The typical phase response of the reflected load current, $I_{SEC'}$, under full-load condition with respect to the input voltage of the resonant tank, is shown in Figure 2.14. The phase is not equal to zero above the resonant frequency, so the fundamental and the third harmonic current are not aligned. Ideally, both components can be lined-up when the phase lag of the third harmonic becomes three times of the phase lag at the fundamental frequency. The phase response of the resonant tank is a non-linear function with the frequency. The notch filter contributes considerable phase lead after the notch frequency. The intended operating frequency for this

multi-element resonant converter is about 10% higher than the resonant frequency to have a reasonable current sharing error while maintaining good efficiency. As seen in Figure 2.14, the notch filter introduces significant phase lead after F_{o2}. The phase lag of the third harmonic is nearly equal to the phase lag of the fundamental component. In the other word, the phase lag at the third harmonic is considerably smaller than three times of the phase lag at the fundament component. In this condition, the reflected load current when the converter running above the resonant frequency can be depicted in Figure 2.15. The reflected load current clearly has higher RMS current than the case shown in Figure 2.13.

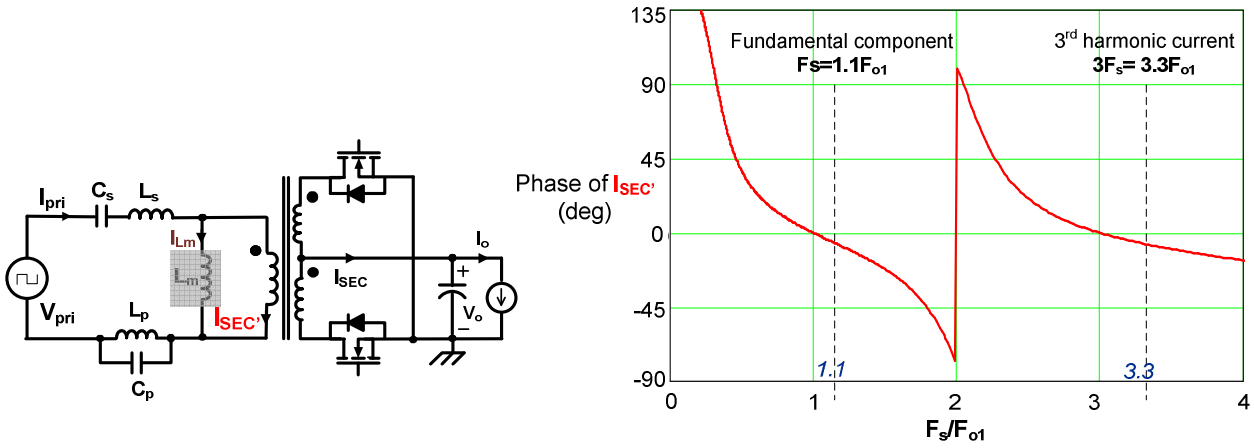

Figure 2.14 Phase response of the reflected load current in the multi-element resonant tank under full-load condition

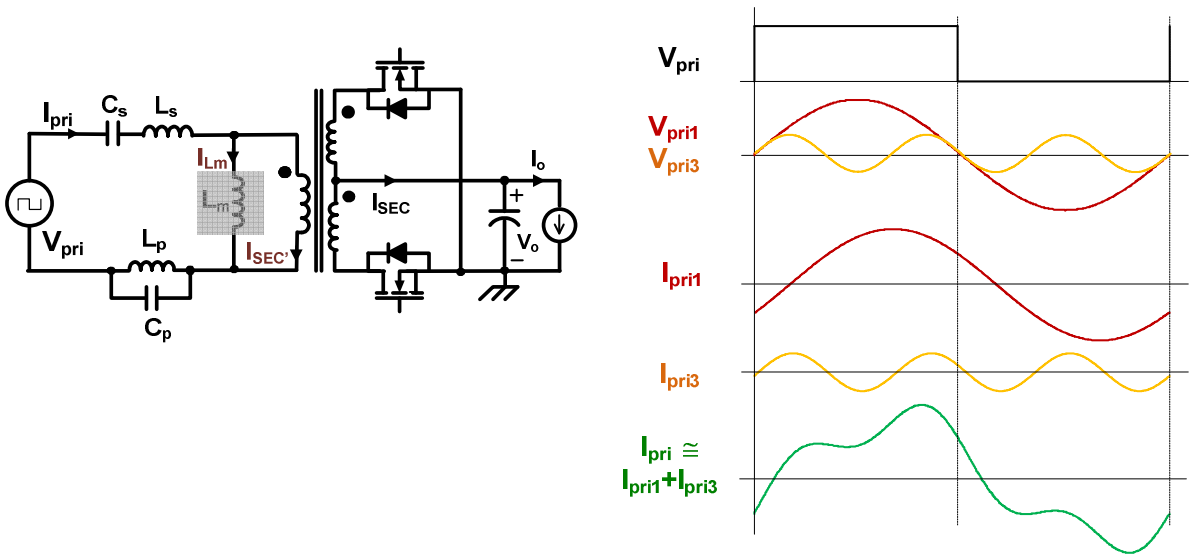

Figure 2.15 Current in the multi-element resonant tank, excluding the magnetizing current, above the resonant frequency

To have the third harmonic aligned with the fundamental frequency as much as possible, the phase lag at the third harmonic is to be increased by either moving down F_{o2} or F_{o3}.

The design objective of this resonant tank is to minimize loss or circulating energy in the circuit. The loss analysis in the previous section shows the highest loss component occurs at the secondary side. The primary current is the sum of the reflected load current ($I_{SEC'}$) and the magnetizing current (I_{Lm}). The latter part is only the function of the switching frequency. Therefore the secondary side RMS current is a suitable indicator in searching for the optimal F_{o2} and F_{o3}. Define the normalized frequency F_{o2n} and F_{o3n} as

$$F_{o2n} = \frac{F_{o2}}{F_{o1}} \tag{2.18a}$$

$$F_{o3n} = \frac{F_{o3}}{F_{o1}} \tag{2.18b}$$

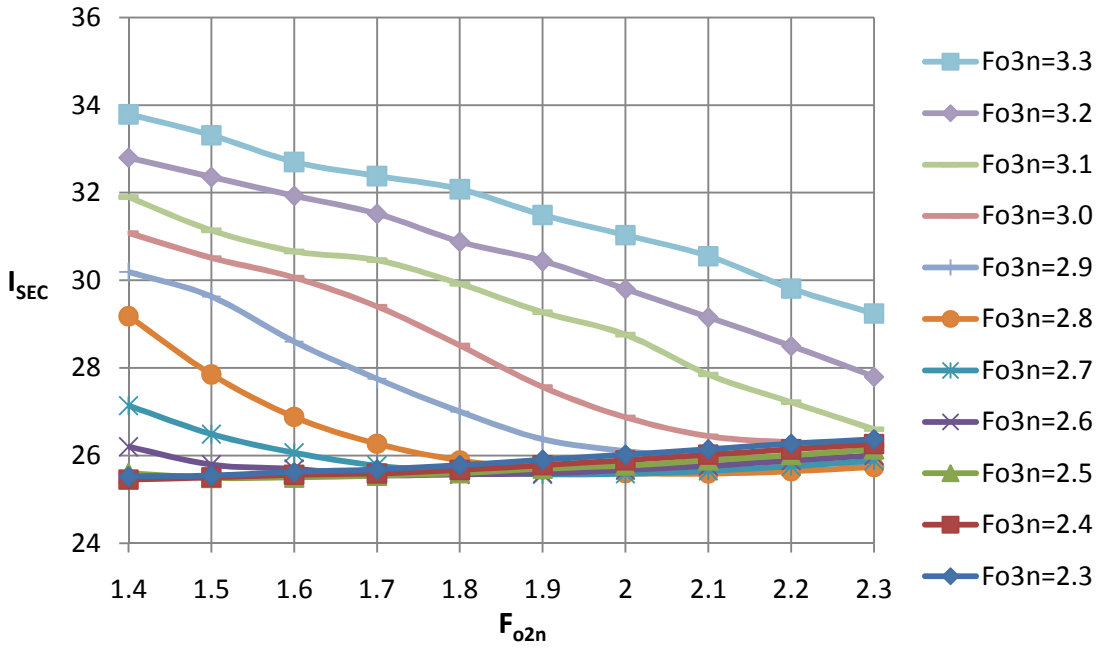

Figure 2.16 Secondary side RMS current plot with F_{o2n} and F_{o3n}

The plots of the secondary side RMS current with F_{o2n} and F_{o3n} as parameters are shown in Figure 2.16. F_{o3n} higher than three incurs excessively large loss on the secondary side due to the improper phase shift of the third harmonic. F_{o3n} below three is a preferred choice, as shown in Figure 2.17. The change in the position of the notch filter or F_{o2n} hardly has an impact on the secondary side RMS current when F_{o3n} is already below three.

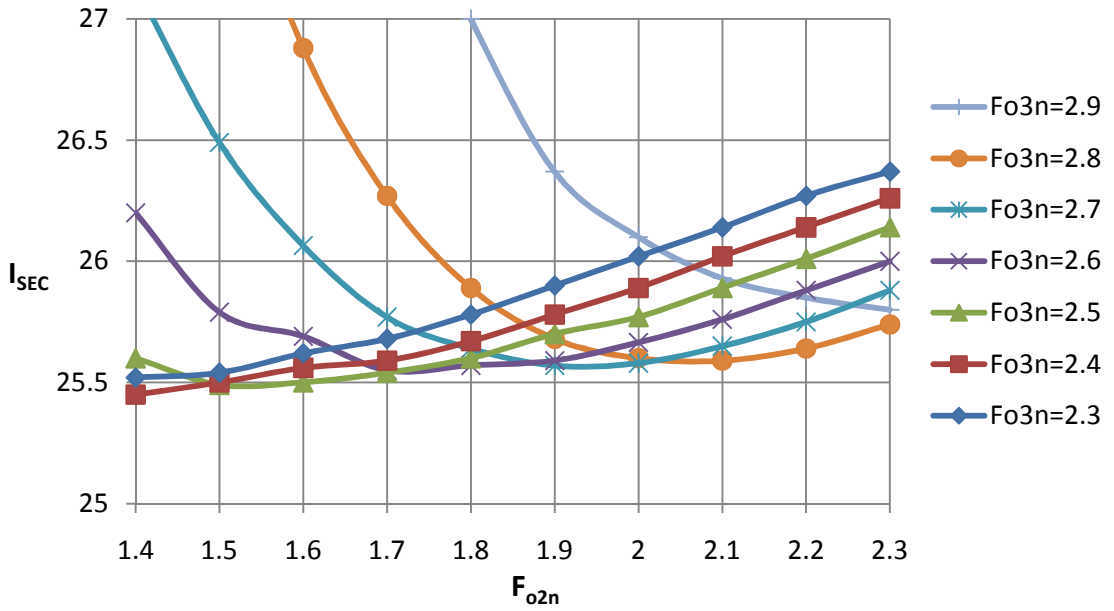

Figure 2.17 Detailed secondary side RMS current plot with F_{o2n} and F_{o3n}

The relationships between the primary RMS current with F_{o2n} and F_{o3n} are shown in Figure 2.18. The primary RMS current does not change much with the position of the notch filter.

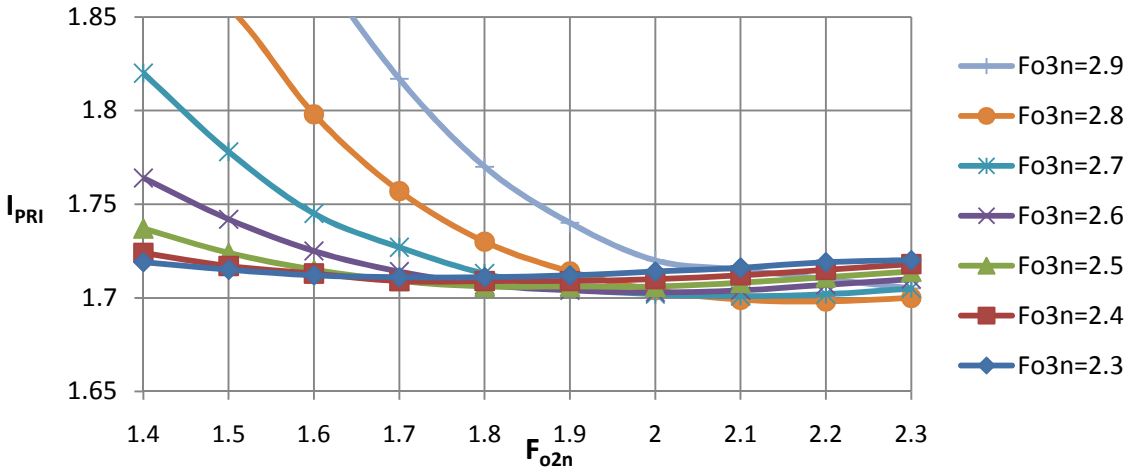

Figure 2.18 Primary side RMS current plot with F_{o2n} and F_{o3n}

The current in the notch inductor (L_p) equals to the primary current (I_{PRI}) plus the current in the notch capacitor (C_p). The phase of the current in the notch capacitor leads the current in the notch inductor by 180˚, so the current in the notch inductor is always higher than the primary

current. In the other word, there is a circulating current in the notch filter making its RMS current than the primary RMS current.

The position of the notch frequency F_{o2} has a strong impact on this circulation current as shown Figure 2.19. The circulating current in the notch filter increases by 30% when F_{o2n} is changed from 2 to 1.7. Moving F_{o2n} above two gives little benefit in the reduced circulating energy and requires the higher switching frequency to achieve the desired droop voltage. Running the converter at the higher switching frequency will incur more body diode related loss, whereas the conduction loss is not improved.

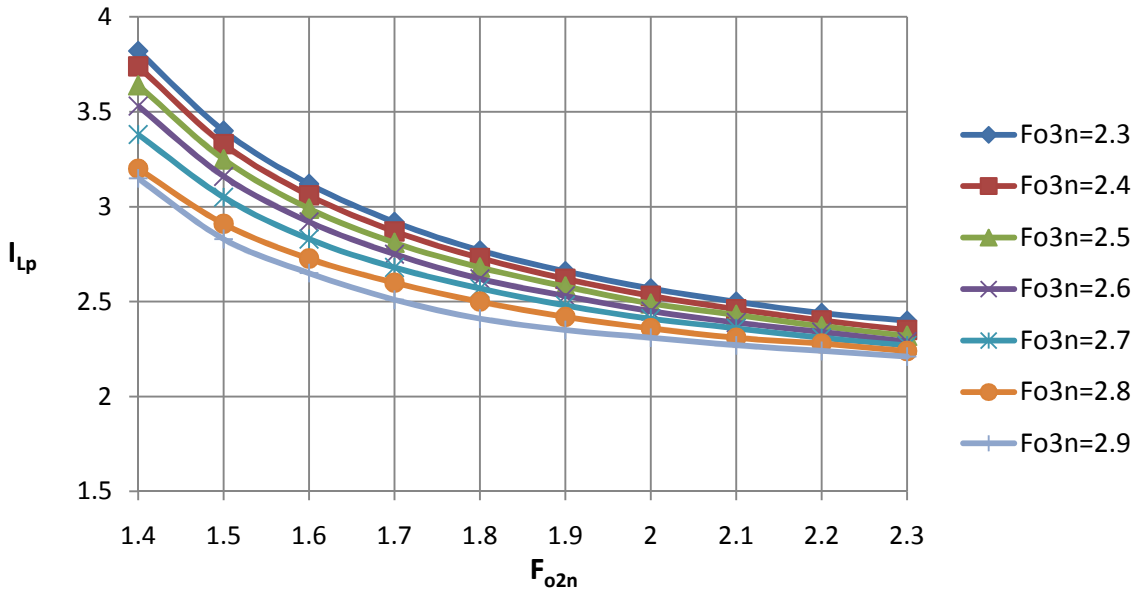

Figure 2.19 RMS current in the notch inductor L_p with F_{o2n} and F_{o3n}

Two different designs denoted as the design#1 and the designs#2 are tentatively selected. The design#1 with F_{o2n}=2 and F_{o3n}=2.7 and the design#2 with F_{o2n}=1.5 and F_{o3n}=2.5 are selected for the design comparison. The currents in the primary and secondary side look the same for both designs, as shown in the simulation result in Figure 2.20. The higher RMS and peak current in

the notch inductor of the design#2 cause higher conduction and core losses, so the design#1 is a design good choice.

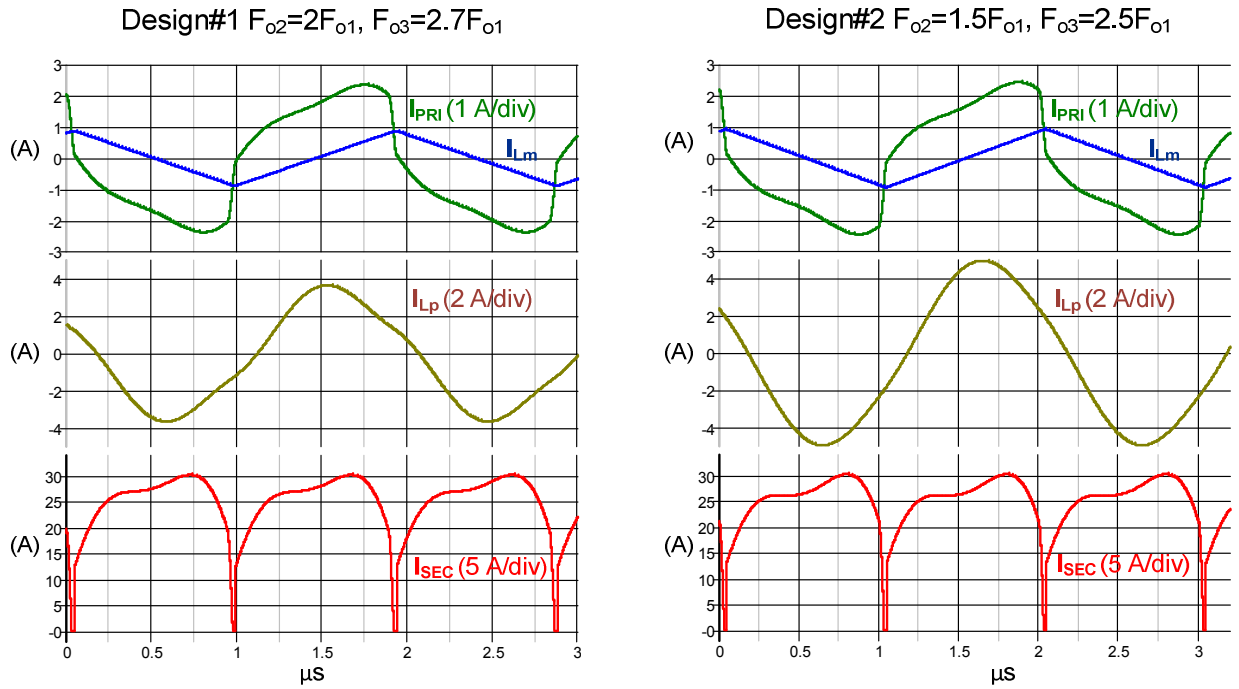

Figure 2.20 Simulation result for the design#1 and design#2

In the design of the multi-element tank, the primary objective is to have the notch filter confine the operation frequency to be reasonably close to its resonant frequency or its fundamental bandpass frequency. Only the fundamental and the third harmonic current mainly contribute to the power transfer. The operating frequency not equal to the resonant frequency causes the third harmonic current not coincided with the fundament component. Therefore, the location of the higher bandpass frequency (F_{o3}) is adjusted to get the first and third harmonics aligned as much as possible. Placing the notch frequency (F_{o2}) too close to either the fundamental or the third harmonic frequency makes the power transfer by respective harmonic component difficult, so the RMS current will eventually increase. Intuitively, the notch

frequency is placed at two times of the resonant frequency to get the minimum attenuation for both first and third harmonic currents.

The circuit detail of the design#1 is shown in Figure 2.21. Figure 2.22 shows the gain and the output regulation characteristic are plotted as did for the LLC design. To get the same droop characteristic as the LLC design, the multi-element resonant converter runs at 560 kHz. The test waveforms are shown in Figure 2.23. The loss breakdown and the efficiency curve are presented in Figure 2.24 and 2.25.

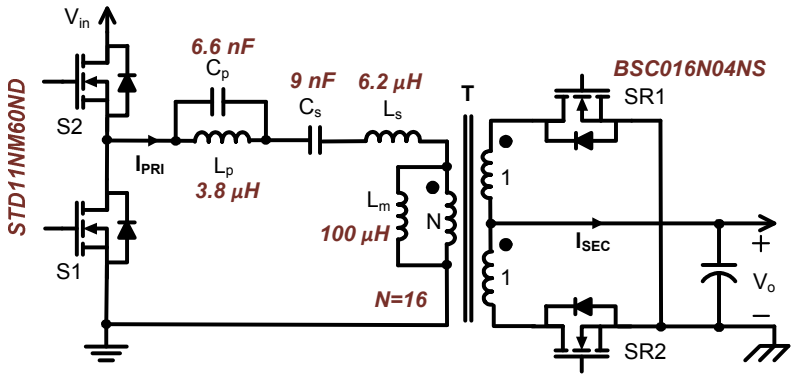

Figure 2.21 Power stage of the 300-W multi-element resonant DCX designed for current sharing application

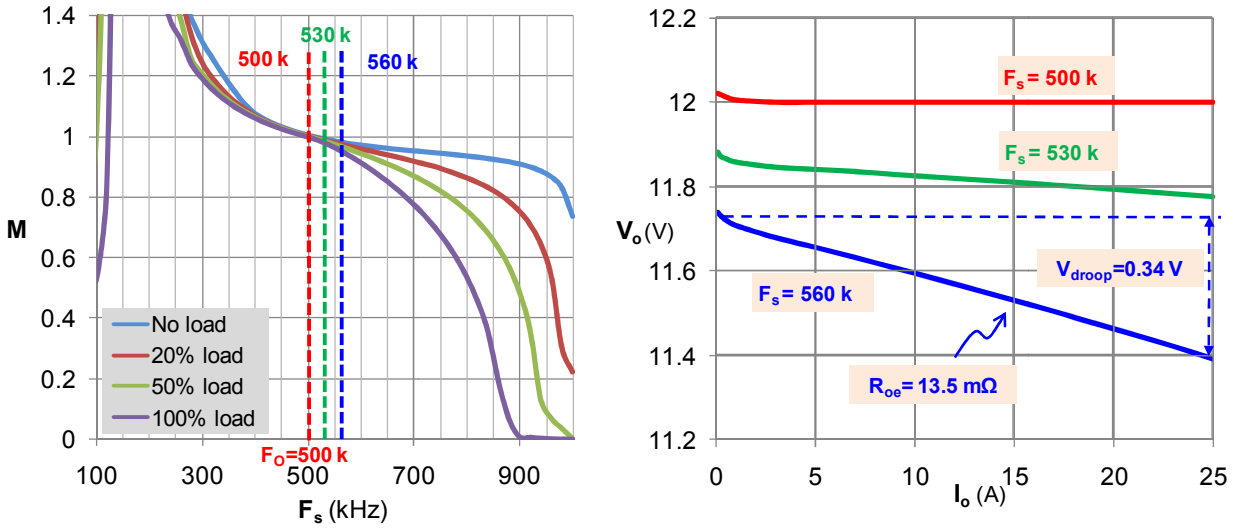

Figure 2.22 Conversion gain and output regulation characteristic of the multi-element resonant DCX

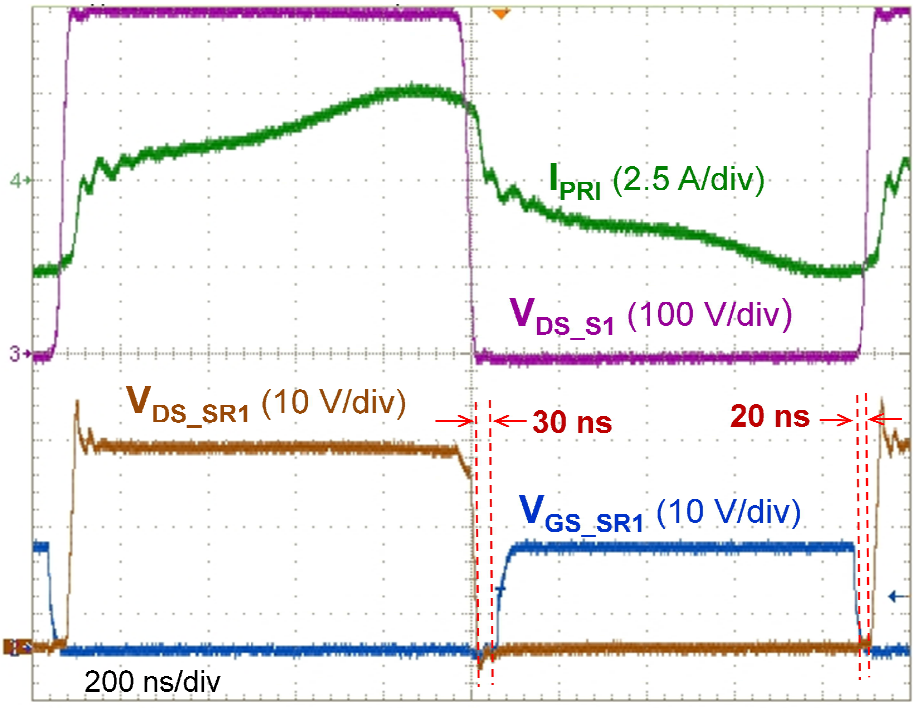

Figure 2.23 Operating waveform of the multi-element resonant converter at 560 kHz

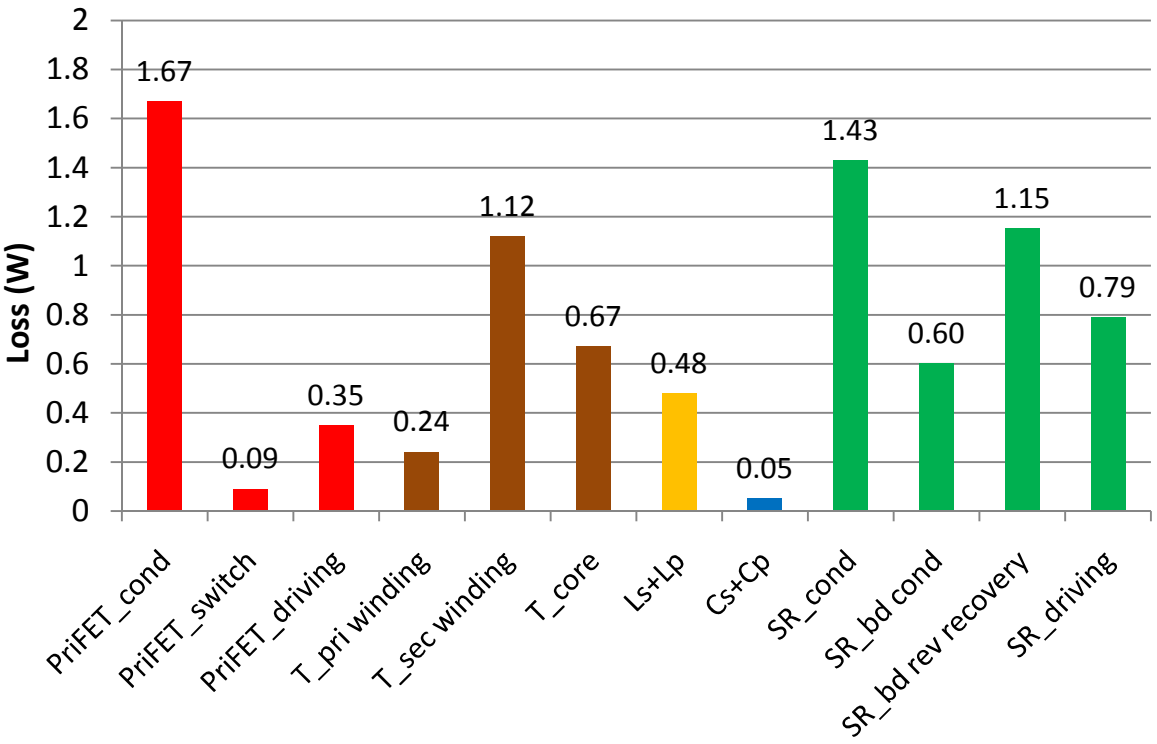

Figure 2.24 Loss breakdown for the multi-element resonant converter running at 560 kHz

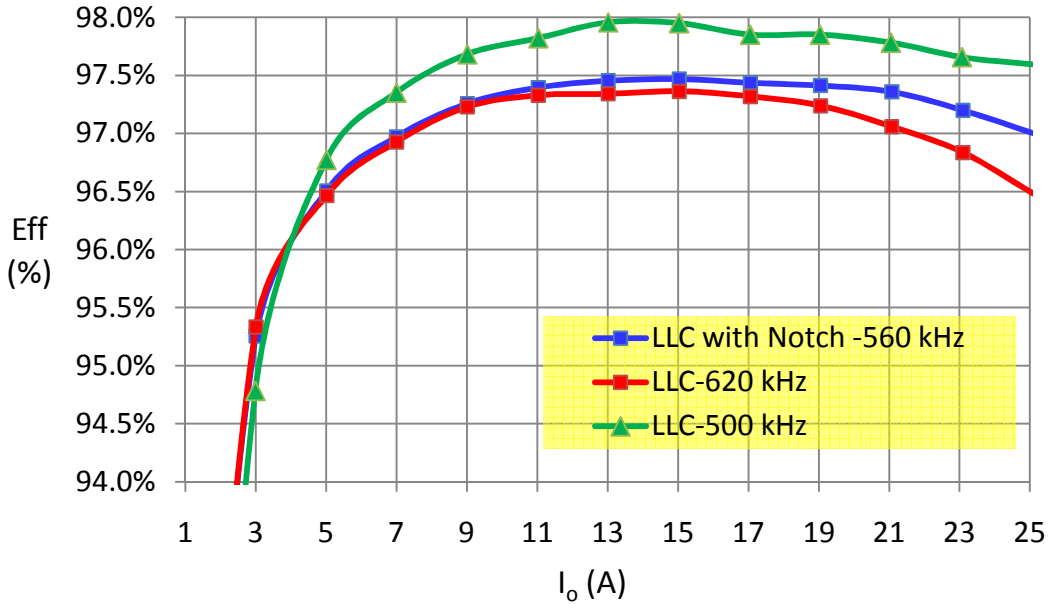

Figure 2.25 Efficiency of the multi-element resonant converter running at 560 kHz

Among three designs, the LLC-DCX running at the resonant converter is the most efficient but lags of the current sharing capability. To render the current sharing feature, the efficiency of

the 620-kHz LLC resonant converter is lowered by 1.1% as compared with the converter working at its resonant frequency, 500 kHz. With the notch filter introduced into the resonant tank, the switching frequency is reduced to 560 kHz and its full-load efficiency is gained by 0.5% as compared to the 620-kHz LLC case. Now the efficiency is just 0.6% lower than the best possible case. Due to the lower operating frequency, the body diode related loss is reduced. The conduction losses in both primary and secondary side are also reduced due to the contribution of the third harmonic current.

2.5. Effect of the passive component tolerance to the current sharing performance

The virtual droop resistance improves the current sharing error caused by the mismatch in the resistive voltage droop in the power stage. The additional droop voltage depends on parameters of the resonant tank. The tolerance in the passive component in each converter creates the mismatch in the droop characteristic among the paralleled units. The simulation result in Figure 2.26 shows the current sharing error becomes 36% when only the tolerance of 10% in the resonant inductor (L_s) exists. Reducing the current sharing error within 10% demands the switching frequency higher than 650 kHz. The efficiency will be greatly degraded.

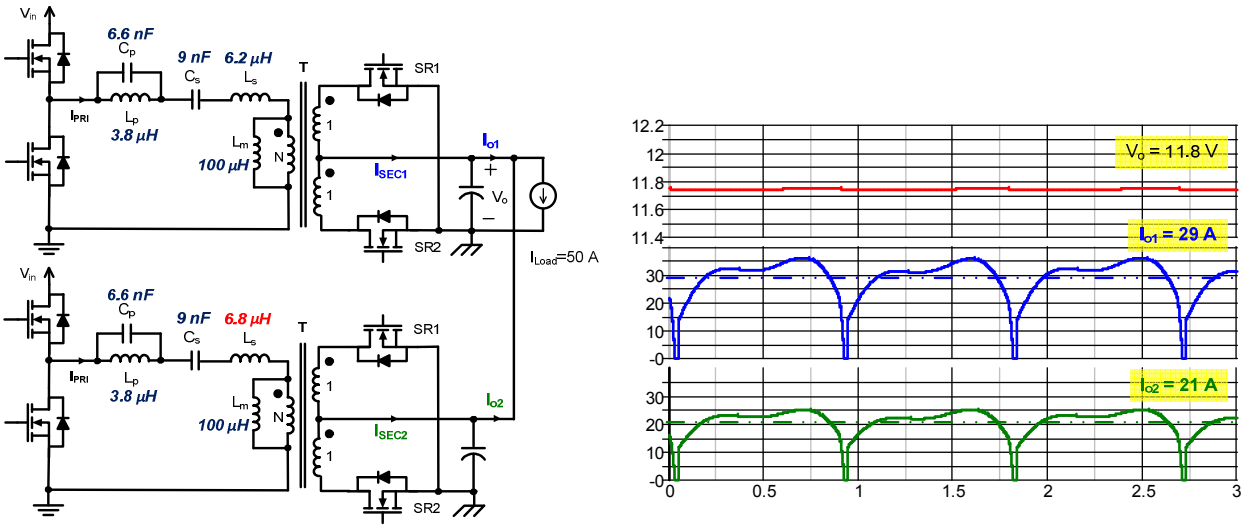

Figure 2.26 Effect of the component tolerance to the current sharing error

Only depending on the droop characteristic from the resonant tank, the current sharing error becomes unacceptable unless the switching frequency is increased. The method to improve the current sharing error caused by the component tolerance of the passive resonant tank will be addressed in Chapter 3.

3. Active droop current sharing method

The current sharing performance in paralleled DCX can be severely degraded by the component tolerance in the resonant tank. The open loop or fixed frequency control cannot handle the change in the resonant tank parameters, which results in a large mismatch in the regulation characteristics. The active droop control is proposed to deal with this component tolerance issue.

3.1. Active droop control

The principle of the active droop control is to use the feedback loop to set the desired droop characteristic rather than to rely on the droop characteristic of the resonant tank. The control structure is shown in Figure 3.1.

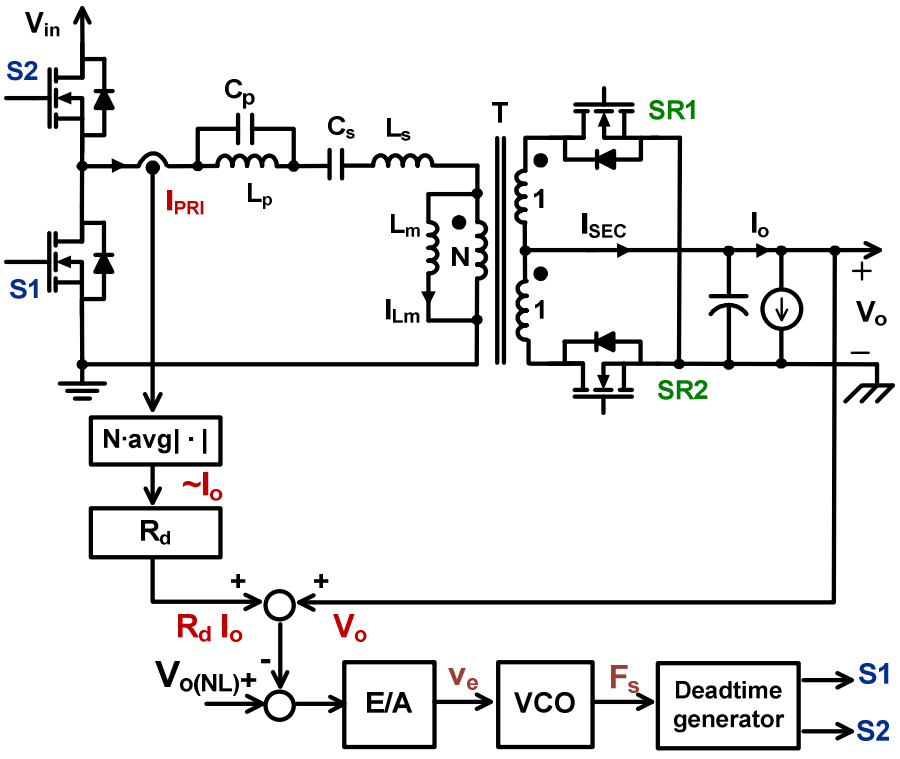

Figure 3.1 Block diagram of the active droop control

To implement the active droop control, the output voltage and the output current have to be sensed. In the real commercial products, the current transformer at the primary side is usually equipped for the circuit protection and safety requirement. The primary current composes of the magnetizing current and the reflected load current. The magnetizing current is relatively constant since the range of the operating frequency is small, within 10% of the resonant frequency. The output current information can be derived from the primary side current from a small current transformer. This method yields the lower loss and less component count. The sensed primary current is rectified and filtered to get the load current information. The average rectified primary current can be expressed as

$$avg|I_{PRI}| = avg|I_o/\mathrm{N} + I_{Lm}| \tag{3.1}$$

When I_{Lm} is constant and relatively small, the average rectified primary current is approximately equal to

$$avg|I_{PRI}| \cong avg|I_o/\mathrm{N}| \tag{3.2}$$

Assuming the gain of the error amplifier is high, it can be shown that the governing equation for the output voltage is

$$V_o = V_{o(NL)} - R_d I_o \tag{3.3}$$

, where $V_{o(NL)}$ is the reference voltage representing the no-load voltage and R_d is the slope of the regulation characteristic or the droop resistance.

The operating frequency is controlled to create the desired droop characteristic. The frequencies at no-load and full-load conditions are no longer at the same point. To get the best efficiency and preserve the simplicity of the SR driving scheme, the active droop controlled

resonant DCX is designed to operate at the resonant frequency at no-load condition and work slightly above the resonant frequency at full-load condition as depicted in Figure 3.2.

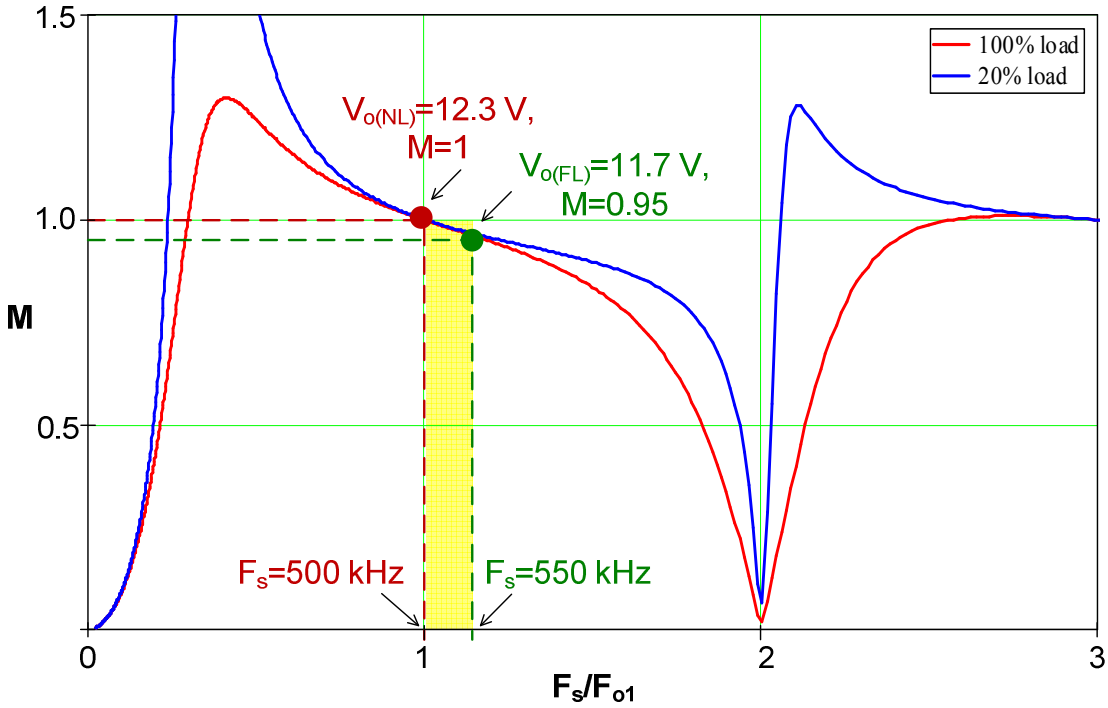

Figure 3.2 Operating point of the converter under active droop control

3.2. Required droop characteristic

Generally the current sharing error is reduced by enlarging droop resistance or droop voltage. Too large droop voltage requires the wide frequency range which eventually degrades the efficiency. The required droop voltage to satisfy the current sharing error with the given the parameter tolerance is quantified in this section. The control circuit is fully responsible for the droop characteristic, whereas the multi-element resonant power stage helps reduces the operating frequency range. Two control parameters, the no-load setpoint voltage ($V_{o(NL)}$) and the droop resistance (R_d) are related to the output regulation characteristic. The impacts of the variation in each parameter are analyzed.

The impact of the tolerance of the droop resistance or the slope of the regulation characteristic to the current sharing error is shown in Figure 3.3. Both units supposedly have the same no-load voltage. The droop resistance of the unit#1 (R_{d1}) is smaller than the droop resistance of the unit#2 (R_{d1}), so the unit#1 carries more load current. The nominal droop resistance is R_d, which is the average of R_{d1} and R_{d2}. The current from each unit is denoted as I_{o1} and I_{o2} and the average current of the two paralleled units at full load equals to $I_{o(FL)}$. From the diagram, the current different between 2 units in the full-load condition can be derived as

$$\Delta I_o = I_{o1} - I_{o2} = \frac{R_{d2}-R_{d1}}{(R_{d1}+R_{d2})/2} I_{o(FL)} \tag{3.4}$$

The current sharing error can be derived as

$$CS_{error} = \frac{\Delta I_o}{I_{o(FL)}} = \frac{\Delta R_d}{R_d} \tag{3.5}$$

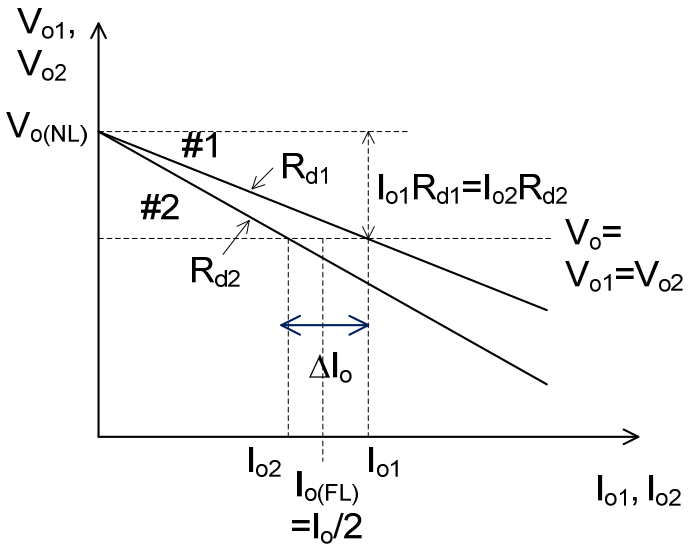

Figure 3.3 Current sharing error with the mismatch in the slope of the output regulation characteristic

From (3.5) the current sharing error is proportional with the tolerance in R_d, so the current sharing error caused by the mismatch in the slope of the output regulation characteristic cannot

be improved by increasing the droop characteristic. The effort to minimize the tolerance R_d should be made for good current sharing performance.

The impact of the tolerance of the no-load setpoint voltage to the current sharing error is shown in Figure 3.4. The slope of the output regulation characteristic of both units is assumed to be the same. The unit#1 has the higher setpoint voltage than the unit#2, so it carries more load current. The difference in the setpoint voltage of two units are denoted as $\Delta V_{o(SP)}$. From the diagram, the current different between 2 units in the full-load condition can be derived as

$$\Delta I_o = I_{o1} - I_{o2} = \frac{2 \cdot \Delta V_{o(SP)}}{R_d} \tag{3.6}$$

The current sharing error can be derived as

$$CS_{error} = \frac{\Delta I_o}{I_{o(FL)}} = \frac{2 \cdot \Delta V_{o(SP)}}{R_d \cdot I_{o(FL)}} \tag{3.7}$$

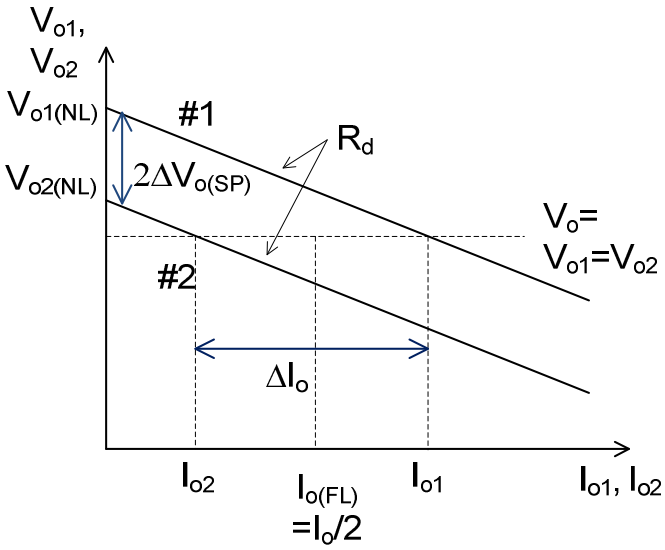

Figure 3.4 Current sharing error with the mismatch in the no-load setpoint voltage

By the definition, the droop voltage is

$$V_d = V_{o(NL)} - V_{o(FL)} = R_d \cdot I_{o(FL)} \tag{3.8}$$

For a specific current sharing error and a setpoint tolerance, the required droop voltage can be calculated as

$$V_d = \frac{2 \cdot \Delta V_{o(SP)}}{CS_{error}} \tag{3.9}$$

The current sharing is proportional to the setpoint error and inversely proportional the droop voltage. From the industrial practice, the output voltage setpoint can be trimmed within ±0.25-0.50%. In this work, the output voltage is 12 V. The trimming process can manage the setpoint error within ±30 mV. The current sharing error of 10% is normally required to fully utilize the module current rating under parallel operation. Then the droop voltage at least 0.6 V is required to satisfy the requirements

3.3. Circuit implementation

The circuit implementation of the active droop control resonant converter is shown Figure 3.5. The power stage is the half-bridge multi-element resonant converter. The resonant controller is placed at the secondary side to simplify the output voltage sensing and provide the accurate timing for the synchronous rectifier. The primary driving signal is transferred to the primary switch via a drive transformer. The synchronous rectifier is driven by the falling-edge delayed primary driving signal, as described in the previous chapter. The error amplifier A1 is the output voltage controller. Howland current source circuit [12], which is the circuit around the opamp A2, generates the current I_{CS} proportional to the primary current signal CS_{PRI}. This current signal, emulating the output load current, develops the voltage across the resistor R_i. With the sufficiently high gain of the error amplifier A1, the sum of the output voltage and the voltage droop across R_i is regulated to be equal to $V_{o(NL)}$. The output voltage, V_o, is programmed to have the droop characteristic as designed.

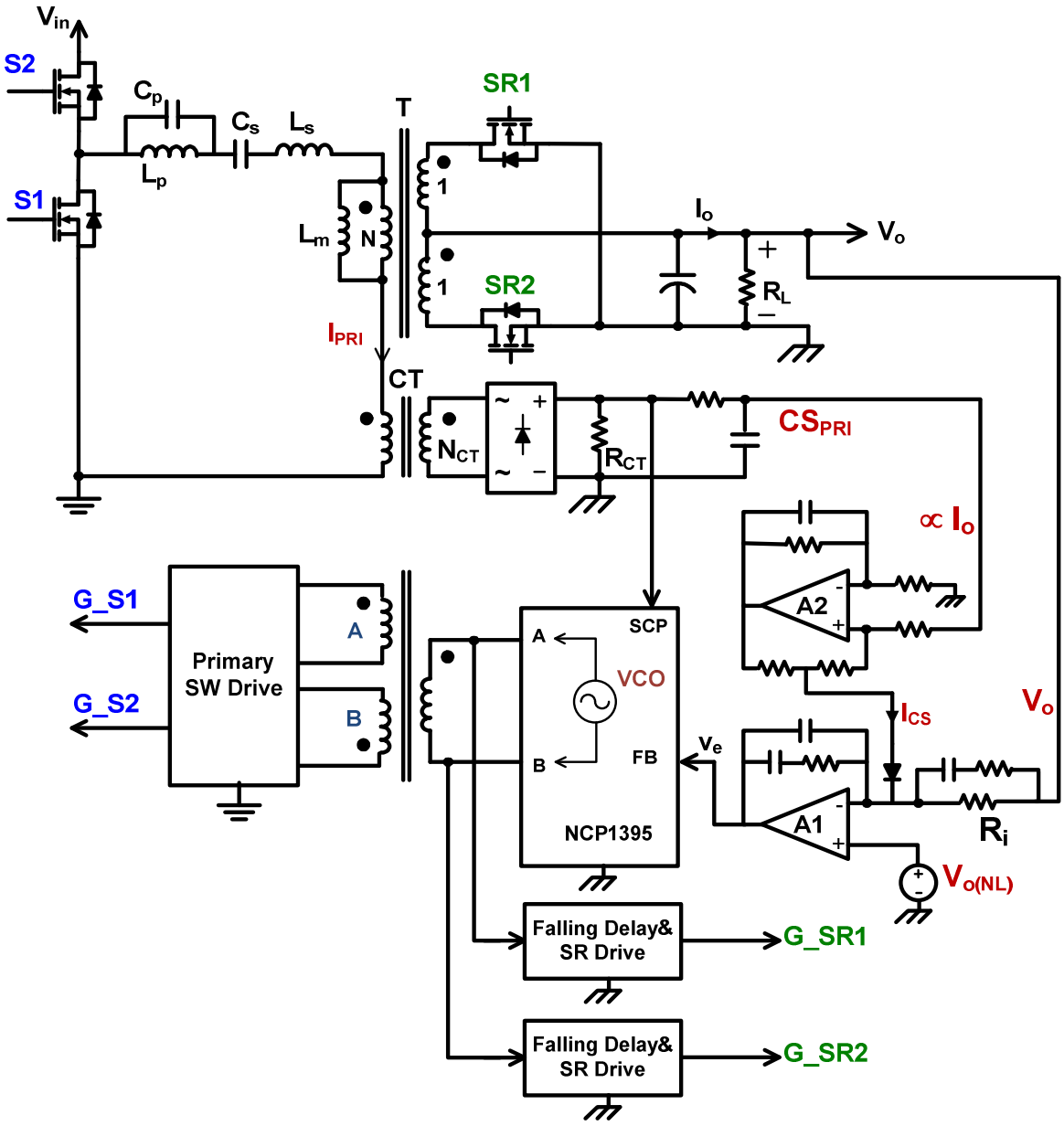

Figure 3.5 Control circuit implementation of the active droop controlled DCX

3.4. Experimental results

The active droop controlled multi-element resonant converter is built to verify the proposed concept. The distribution power system using 12 V bus can accommodate a regulation band of ±5%, which is translated to the output voltage range of 11.4-12.6 V. To have the new DCX compatible with the conventional system while having a good current sharing performance, the

droop voltage is determined to be 0.6 V at the full load and the regulation band is positioned to be at the center of the allowable regulation band, 12 V. The output voltage is 12.3 V at the no-load condition and is 11.7 V at the full-load condition.

The input voltage is 400 V. At no-load condition, the conversion gain is equal to one and the output voltage is 12.3 V. From (2.9), the turn ratio of the transformer, N, is equal to 16.

The switching frequency in the full-load condition around 500 kHz is desired to have a fair comparison with the 500-kHz standalone DCX and the 500-kHz fully regulated resonant converter (D2D). Therefore, the resonant tank is re-designed with F_{o1}=465 kHz. As discussed in the previous chapter, the notch frequency F_{o2} and higher bandpass frequency F_{o3} are placed at $2F_{o1}$ and $2.7F_{o1}$ respectively. The full-load switching frequency is 510 kHz. The power stage detail is shown in Figure 3.6.

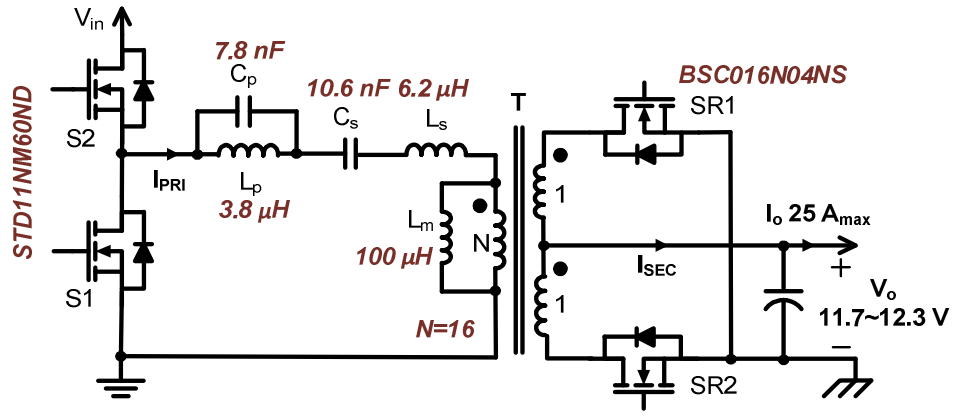

Figure 3.6 Power stage of the multi-element resonant converter for the active droop control

Two identical units are parallel connected to demonstrate the concept, as shown in Figure 3.7. Under the identical units, there is almost no current sharing error, as listed Table 3.1. Then all the component values of the resonant tank in the unit#2 are intentionally increased by 10% to verify the current sharing concept, as shown in Figure 3.8. Table 3.2 shows the current sharing error is well under 5%. The current sharing error here results from the mismatch in the

magnetizing current since two converter runs at the different frequency and the primary current is sensed to emulate the output current. Further improvement can be made by direct sensing output current but it comes with lower efficiency and more component count.

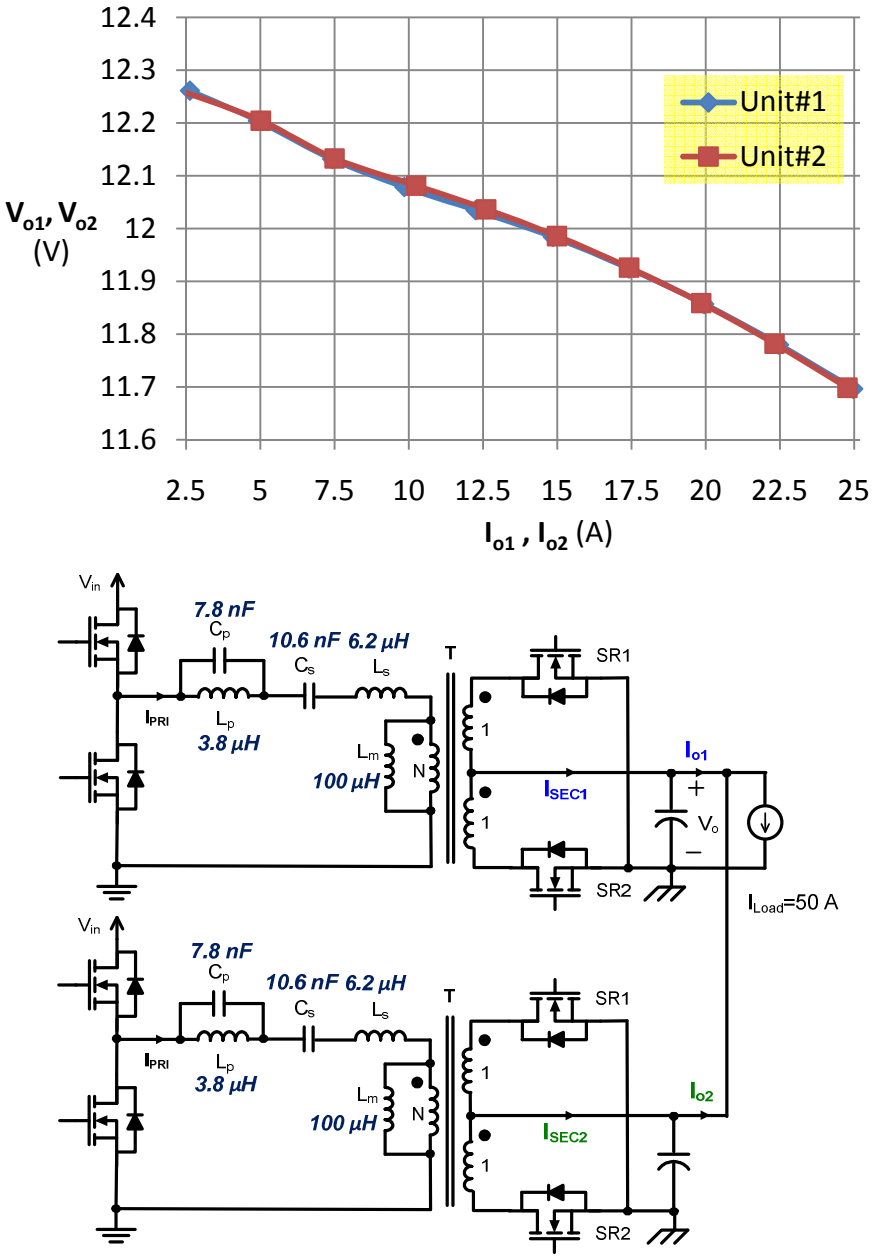

Figure 3.7 The output regulation characteristic of the active droop controlled DCX with no tolerance

Table 3.1: Current sharing error of the active droop controlled DCX with no tolerance

I_o (A)	ΔI_o (A)	CS_{error}(%)
10	0.13	0.52
25	0.43	1.73
50	0.05	0.18

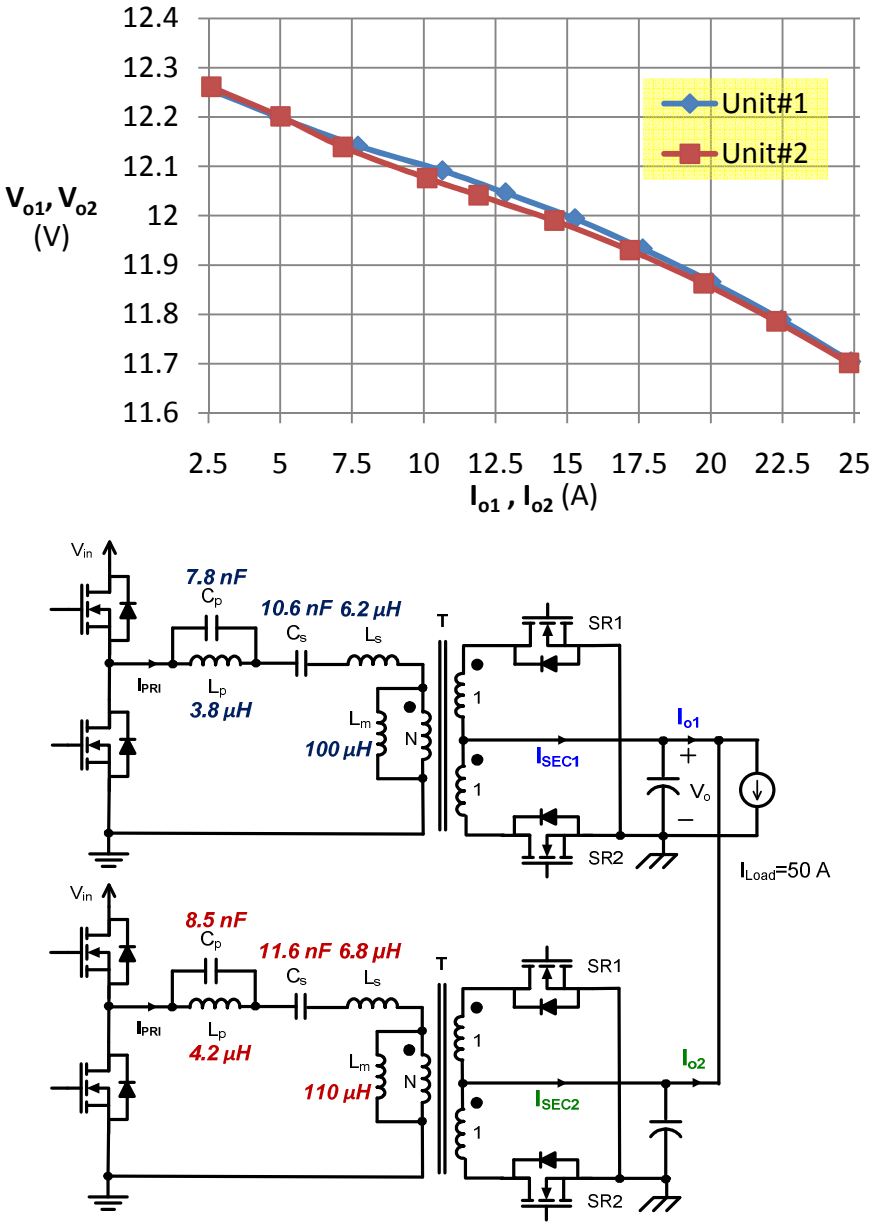

Figure 3.8 The output regulation characteristic of the active droop controlled DCX with +10% component tolerance on the unit#2

Table 3.2: Current sharing error of the active droop controlled DCX with component tolerance

I_o (A)	ΔI_o (A)	CS_{error}(%)
10	0.14	0.53
25	1.02	4.10
50	0.22	0.86

The efficiency of the DCX with active droop control is shown in Figure 3.9. The efficiency of the LLC DCX running at the resonant frequency of 500 kHz and the fully regulated resonant converter running at 500 kHz (D2D) are shown for comparison. It is clear that the LLC DCX running at the resonant frequency is the most efficient but has no current sharing capability. The active droop controlled DCX has similar full load efficiency to the resonant D2D. The light load efficiency is slightly improved since the frequency is decreased as the load is reduced.

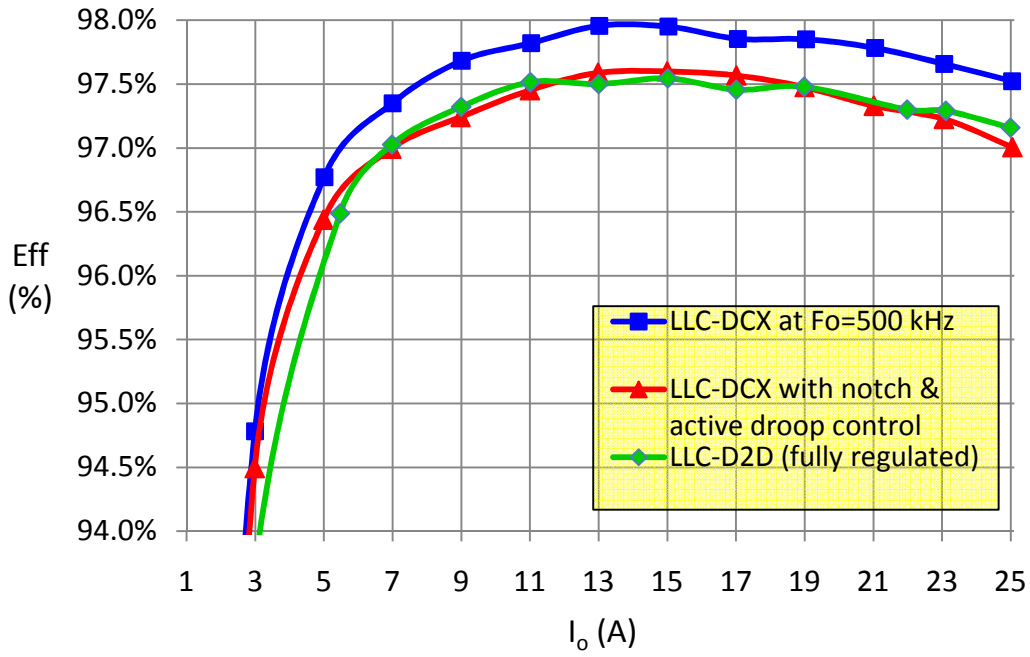

Figure 3.9 Efficiency of the active droop controlled DCX

4. Comparison of the circuit design complexity between the resonant D2D and DCX

This chapter discusses the circuit design complexity of the fully-regulated resonant converter (D2D) and the semi-regulated resonant converter (DCX).

The power stages for both designs have the same topology. The complexity of the output control circuit of the resonant D2D and DCX are similar. A droop circuit, which is a small single opamp circuit, is added the output voltage control part. Only the key difference among these two designs is the synchronous rectifier driving scheme.

4.1. SR driving scheme in the resonant D2D

The fully regulated resonant converter is designed to operate below the resonant frequency to accommodate the variation in the input voltage. The current in the synchronous rectifier ceases to zero before the primary switch is turned off.

The current information is required to generate the proper driving signal. The current flowing thru SR FET is normally detected by its drain-source voltage, as shown in Figure 4.1 Many commercial SR control IC, such as IR1167 for IR or TEA1761 from NXP, are available for this function. This control IC turns on SR FET when the body diode conducts the current or the drain-source voltage detected by SR control IC goes below -50 mV. Once SR FET is turned on, the drain-source voltage of SR FET equals to the voltage drop in its channel resistance, which is much lower the voltage drop in the body diode. The current flowing in SR FET is sinusoidal, so it resonates back to zero at the end of the resonant period. The voltage drop in the channel resistance is reduced to zero. The SR control IC continually monitors the drain-source voltage and deactivates the SR FET when the drain-source voltage nearly reaches zero (e.g. -5 mV in the commercial ICs).

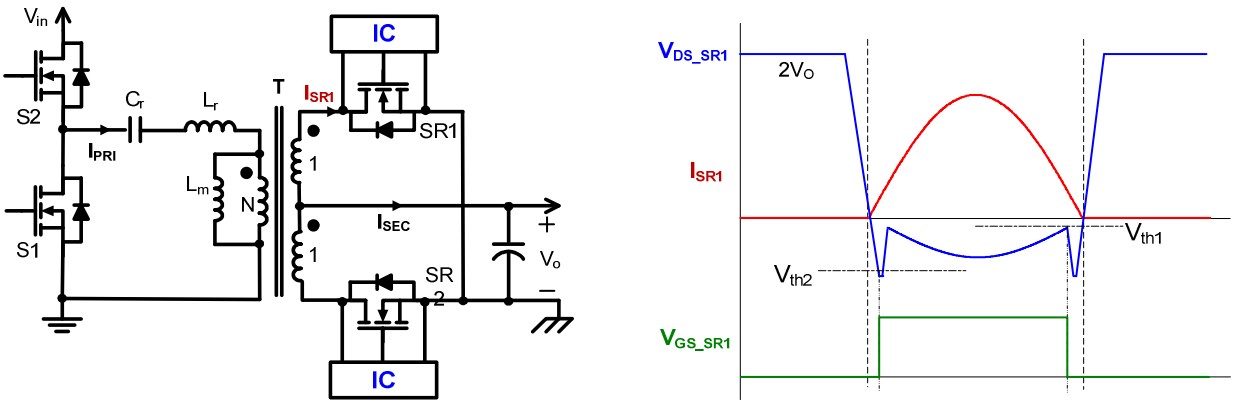

Figure 4.1 SR driving scheme based on the drain-source voltage sensing

Ideally the sensed voltage across SR FET can truly represent its current. The SR FET actually has parasitic drain and source inductance from its packaging as shown in Figure 4.2. The sensed voltage across SR FET has the resistive voltage drop in the channel resistance and the induced voltage in the package inductance. The sensed voltage across SR FET terminals has the leading phase with respect to the phase current. This causes the SR FET turn off too early.

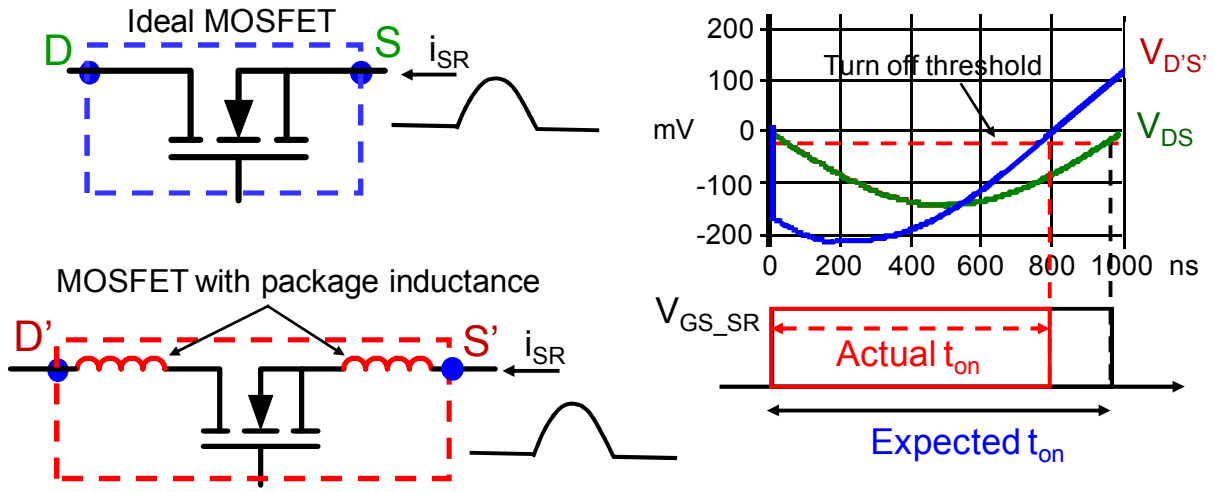

Figure 4.2 SR early turned-off due to the package parasitic inductance

The compensation network proposed in [6] is shown in Figure 4.3. It has a switched RC network to compensate the phase lead from the parasitic inductance. When SR is turned on, the switch Sa is on and Sb is off. The time constant of RC network is designed to match the time

constant of the channel resistance and package parasitic inductance of SR FET. The RC network is parallel connected to SR FET and reproduces the signal proportion to the SR current for accurate SR driving. When SR is turned off, the switch Sa is off and Sb is on. The RC compensation network is reset and ready for the operation in the next cycle. This network improves the efficiency by 0.3%.

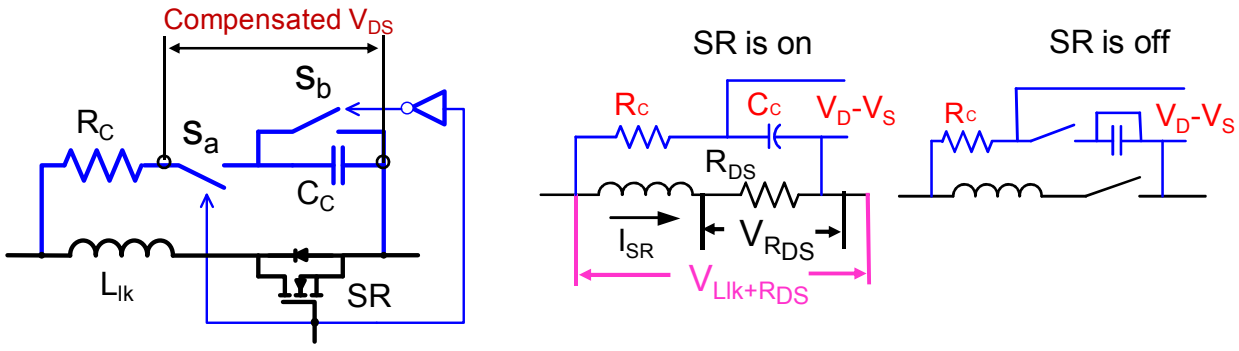

Figure 4.3 Compensation network for package parasitic inductance

The turn-on propagation delay of the SR control IC, IR 1167 is 60-90 ns, which is considerably large, compared to the half switching period of 1 μs. The turn-on compensation circuit is designed-in and enhances the efficiency by 0.12%.

The conceptual block diagram and the real circuit implementation of the synchronous rectifier circuit for the resonant D2D are shown in Figure 4.4. IC1 is IR1167, the SR control IC based on drain-source voltage detection of SR FET. IC2 is a MOSFET driver chip. Q1A and Q1B act as the switch Sa and Sb respectively. Q2 is an inverter circuit driving Q1B or Sb. The RC compensation network is R31 and C31 in the schematic. IR1167 control IC requires the setting of the minimum SR driving pulse wide to make the control IC not susceptible the noise [13], which can be programmed with the resistor R10. The turn-on compensation delay comprising of R11, C11, and D11, will generate one-shot signal to turn on SR FET upon the activation of the primary switch. It bypasses the time delay in the body diode detection circuit in

IR 1167. As we can see, the SR driving scheme for the resonant D2D is quite complex and requires many trimmings to deliver the optimum performance.

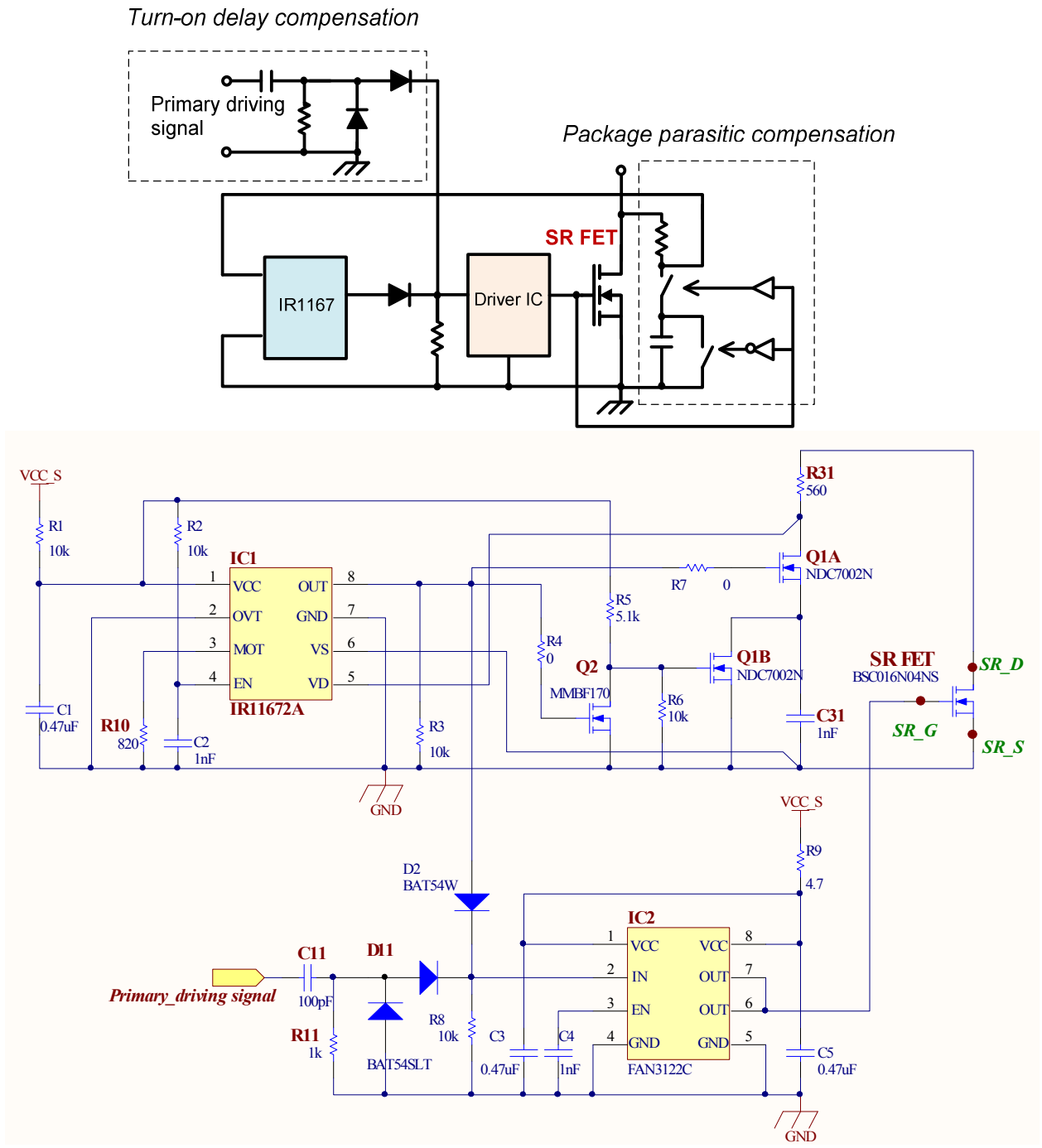

Figure 4.4 SR driving scheme for the resonant D2D

4.2. SR driving scheme in the resonant DCX

SR FET in the resonant DCX running above the resonant frequency can be easily driven by the falling-edge delayed primary driving signal. The SR driving circuit is shown in Figure 4.5. Only trimming needed in the circuit is the falling-edge time delay circuit, which are R11 and C11 in the figure.

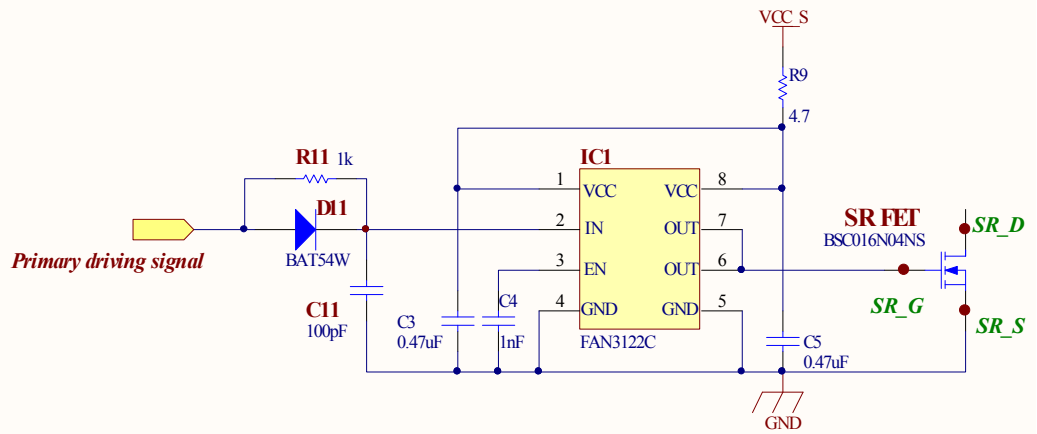

Figure 4.5 SR driving scheme for the resonant DCX

Compared two SR driving schematics, it is clear that the SR driving circuit in the resonant DCX is much simpler than the circuit required for the resonant D2D, which translate into the better reliability and lower cost. The aspect on SR driving scheme highly stresses out the benefit of the resonant DCX over the resonant D2D.

5. Conclusion and Future works

5.1. Conclusion

This thesis has examined the alternative power architecture, the DCX implementation, and the current sharing methods in DCX. DCXs are generally more efficient and have simpler circuit structure than D2Ds. Since most of the load systems in the computer and telecommunication equipment are regulated by POLs, the front-end power supply does not have to be a fully-regulated converter. DCX can be made as a modular design to simplify the system power capacity expansion. In this regard, this current sharing feature in DCX is important to realize the scalable power architecture. The droop current sharing method is applied in this work since it requires no communication bus between module and no converter stability related issues.

The LLC resonant converter operating at its resonant frequency has the best efficiency, so it can be a suitable implementation for DCX. The conversion gain of the converter running at the resonant frequency is independent of the load current. The current sharing performance of the aforementioned LLC resonant converter solely depends on the parasitic resistive component or the resistive droop voltage in the power stage. The tolerance in the on-state resistance of MOSFETs and magnetic winding resistance makes the current sharing error of two paralleled LLC converters unacceptably large. To improve the current sharing error, the higher droop resistance or droop voltage is required which leads to additional power losses.

The virtual droop resistance concept is introduced based on the fact that the conversion gain of the resonant tank is not only the function of the operating frequency but also the function of the load current. Additional passive droop resistance can be realized without incurring much conduction loss. The passive droop current sharing method can effectively reduce the current sharing error due to the tolerance of the resistive components in the power stage.

With the passive droop method, the operating frequency of the LLC resonant converter required to meet the specified current sharing error of 10% is found to be 20% above the resonant frequency, which significantly degrades the efficiency. A multi-element tank is created by adding a notch filter into the LLC resonant tank. The conversion gain of the multi-element tank is more sensitive to the frequency, so the required operating frequency can be reduced to the reasonable value. The design of the multi-element resonant tank is discussed. The notch filter should be placed with twice of the resonant frequency to minimize the attenuation of the first and third harmonics. The higher bandpass frequency is placed slightly below to three times of the resonant frequency to reduce the RMS current.

It was found that the tolerance of the passive components in the resonant tank has detrimental effect to the current sharing performance. The active droop control is proposed to overcome this issue. The active droop control scheme, using the output voltage and the primary tank current feedback, manipulates the operating frequency to obtain the desired the droop characteristic. The detailed circuit implementation is discussed. The active droop controlled resonant converter is designed to operate at the resonant frequency at no-load condition and to run above the resonant frequency as the load increases.

The proposed DCX with the active droop control has simpler circuit structure than the fully regulated resonant converter or D2D. It enables the modular design for the front-end power supply units, which leads to the lower cost and shorter development cycle. Operating at above resonant frequency simplified the SR driving circuit, which required to no drain-source voltage or current sensing. SR FETs can be driven by the falling-edge delayed primary driving signals. The current flows through the secondary side for an entire half-cycle, so the RMS current in the

secondary side is lower than that of the D2D case. However, SR FETs are turned off with high di/dt. The efficiency improvement in DCX is limited by their body diode related loss.

5.2. Future works

To improve the efficiency of the DCX, the loss in the body diode related loss in SR FETs should be reduced. The SR driving scheme in this work is implemented with an analog delay circuit. A finite deadtime has to be accommodated for the variation in the propagation delay of the MOSFET driver chips. This deadtime incurs more conduction and reverse recovery losses. A digital adaptive SR driving scheme should be investigated to further improve the efficiency.

The multi-element tank topologies should be specially investigated for the DCX application. As discussed in Chapter 2, the multi-element tank introduces comes with the second bandpass filter, which creates the third harmonic current into the primary current. The third harmonic is not aligned with the primary current, so it has less benefit to RMS current reduction. The resonant tank for DCX applications requires only a bandpass filter for the power transfer and a notch filter for the frequency range limitation and circuit protection. The research efforts should be made to find for more suitable or simpler tank circuits.

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