Low Power Merged LNA and Mixer Design for Medical Implant Communication Services

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(ABSTRACT)

The FCC allocated the spectrum of 402-405 MHz for MICS (Medical Implant Communication Services) applications in 1999. The regulations for MICS band apply to devices that support the diagnostic and/or therapeutic functions associated with implanted medical electronics. The implanted devices aid organs and control body functions of patients to support specific treatments, and monitor patients continuously so that necessary action can be taken in advance to avoid serious conditions. To enable to use MICS applications, several requirements must be satisfied. An implanted wireless device should have a small size, consume ultra-low power, and achieve the date rate of at least 200 kbps within 2 m distance. The major challenge is to realize ultra-low power devices. Thus the low-power design of the RF circuit is crucial for MICS applications as the power consumption of the wireless devices is mostly contributed by RF circuits.

This thesis investigates low-power design of an LNA and a down-conversion mixer of a receiver for MICS applications. The key idea is to stack an LNA and a mixer, while the LNA operates in the normal super-threshold region and the mixer in the sub-threshold region. In addition, a gm-boosting technique with a capacitor cross-coupled at the LNA input stage is also adopted to achieve a low noise figure (NF) and high linearity, which is critical to the overall performance of the receiver. The mixer operating in the sub-threshold region significantly reduces power dissipation and relaxes the voltage headroom without sacrificing the LNA performance. The relaxed voltage headroom enables stack of the LNA and the mixer with a low supply voltage of 1.2 V. The proposed circuit is designed in 0.18 μm RF CMOS technology. The merged LNA and

mixer consumes only 1.83 mW, and achieves 21.6 dB power gain. The NF of the block is 3.55 dB at 1 MHz IF, and the IIP3 is -6.08 dBm.

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Chapter 1:
Introduction

As a result of the radical technology revolution in the 20th century, people have started to carry portable electric devices such as cellular phones, pagers and MP3 players. In 1996, Zimmerman used the term wireless personal area network (PAN) [1], which later has been modified to body area network (BAN) to represent all applications and communications on, in and near the body [2].

One of the targeted applications of the Wireless Body Area Network (WBAN) is electric devices in medical environments where conditions of patients are continuously monitored in real time. The WBAN-based medical system brings significant advantages over the traditional wire-based patient data collection methods through increase of hospital capabilities, quality of patient care, and reduction of the overall medical cost [3].

Several wireless communication techniques are proposed for medical systems listed in Table 1-1[4], [7]. Wireless medical aided devices are expected to be implanted on or carried by patients, thus low power consumption is the primary concern for healthcare applications. As can be seen in Table 1-1, MICS (Medical Implement Communication Services), UWB(Ultra Wideband) and ZigBee are favorable for MICS applications due to its low transmitter power. However, ZigBee suffers from strong interference by other communication services in the same 2.4 GHz unlicensed ISM(Industrial, Scientific and medical) band comparing to MICS band which is specifically regulated for only medical usages. UWB, operating in the frequency band of 3-10 GHz, offers high data rates for short distance, but the circuit complexity may be high due to the wide and relatively high frequency band. As a result of brief comparison, MICS band seems the best candidate for healthcare systems adopting WBAN. More detailed characteristics of MICS band is discussed in Chap.2.

Table 1-1 Wireless technologies applicable for medical applications

	MICS	WMTS	UWB IEEE 802.15.6	ZigBee IEEE 802.15.4	Bluetooth IEEE 802.15.1	WLANs 802.11b/g
Frequency Band	402-405 MHz	608-614, 1395-1400, 1429-1432 MHz	3-10 GHz	2.4 GHz	2.4 GHz	2.4 GHz
Bandwidth	3 MHz	6MHz	>500MHz	5 MHz	1 MHz	20 MHz
Data Rate	19 or 76 kbps	76 kbps	850 kbps to 20 Mbps	250 kbps	721 kbps	>11 Mbps
Trans. Power	-16 dBm (25 μW)	>10 dBm and <1.8 dB	-41 dBm	0 dBm	20 dBm	250 mW
Operating Range	0-10 m	>100 m	1-2 m	1-100 m	1-100 m	0-100 m

Intensive research and development efforts for low-power design of WBAN have been made for medical systems and radio operating in MICS band [3]-[6]. A key design challenge for developing implantable devices is to prolong the device operation time typically powered by batteries. In order to reduce the overall power consumption of a radio, each basic building block should be designed to operate at low power. Basic building blocks for the RF front-end of a radio include low noise amplifier (LNA), mixer, filters, voltage controlled oscillator (VCO), and power amplifier (PA). However, minimization of the power dissipation for the RF circuitry poses critical design issues while achieving good performance. For example, the power dissipation of an LNA is reduced at the cost of the noise figure (NF). A mixer might not provide a high gain without consuming high power. The technical challenge for low-power design of those

building blocks is to achieve the desired performance while minimizing power dissipation.

This thesis investigates low-power design of an LNA and a down-conversion mixer for a receiver for MICS applications. The principal idea is to stack an LNA and a mixer, while the LNA operates in the normal super-threshold region and the mixer in the sub-threshold region. In addition, a gm-boosting technique with a capacitor cross-coupled at the LNA input stage is adopted to achieve low noise figure (NF) and high linearity. The mixer operating in sub-threshold region significantly reduces the power dissipation and relaxes the voltage headroom without sacrificing the LNA performance. The relaxed voltage headroom enables the stacked LNA and mixer to operate at a low supply voltage of 1.2 V. The proposed circuit was designed in TSMC 0.18 μm RF CMOS technology.

The thesis is organized as follows. Chapter 2 describes key specifications for the WBAN standards and general characteristics of MICS band. It also covers the operation technique for sub-threshold circuits. In chapter 3, the RF super heterodyne receiver architecture is reviewed and the typical performance metrics for an LNA and a down-conversion mixer for MICS applications are presented. Chapter 4 describes the proposed circuit design and layout techniques in detail. The simulation results are presented in Chapter 5, and a few conclusions for the proposed design are drawn in Chapter 6.

Chapter 2:
Preliminaries

This chapter reviews the draft of IEEE 802.15.6 WBAN standard followed by overview of MICS band. Then, it covers techniques and characteristics of sub-threshold circuits.

2.1 Wireless Body Area Network (WBAN) standards

Recently, IEEE developed the draft IEEE 802.15.6 standard for low power devices which operate on, in or around the human body to serve a variety of applications including medical, consumer electronics, personal entertainment and etc. The use of WBAN for the medical purpose especially requires low power consumption and high reliability whether its location is inside or on the body [5].

The WBAN standard can play a prominent role in developing both software and hardware designs for such applications. Table 2.1 summarizes the suggested physical (PHY) layer specifications for WBAN applications. As can be seen in the table, seven candidate bands are listed for the narrow band WBAN applications. For all the frequency bands except the 420 – 450 MHz band, the draft standard for PHY specifications employs differentially encoded PSK (Phase Shift Keying), also known as DBPSK (Differential Binary Phase Shift Keying). The DBPSK transceiver architecture makes it possible to implement a lower-cost non-coherent receiver rather than a coherent receiver that requires a carrier synchronization loop. An offset modulation scheme is adopted to enhance the signal bandwidth efficiency. The square root raised cosine (SRRC) scheme is also used to mitigate inter-symbol interference (ISI).

Table 2-1 IEEE 802.15.6 Draft PHY Specifications

	Frequency bands	Modulation	Symbol rate	Data rate[3]	Pulse Shape
1	402-405 MHz	π/2-DBPSK[1]	187.5 ksps	57.5-455.4 kbps	SRRC[4]
2	420-450 MHz	GMSK[2]	187.5 ksps	57.5-187.5 kbps	BT=0.5
3	863-870 MHz	π/2-DBPSK	250 ksps	76.7-607.1 kbps	SRRC
4	902-928 MHz	π/2-DBPSK	300 ksps	91.9-728.6 kbps	SRRC
5	950-956 MHz	π/2-DBPSK	250 ksps	76.7-607.1 kbps	SRRC
6	2360-2400 MHz	π/2-DBPSK	600 ksps	91.9-971.4 kbps	SRRC
7	2400-2483.5 MHz	π/2-DBPSK	600 ksps	91.9-971.4 kbps	SRRC

(1) DBPSK: Differential Binary Phase Shift Keying
(2) GMSK: Gaussian Minimum Shift Keying
(3) Data rate is dependent to the code rate and spreading factor.
(4) SRRC: Square Root Raised Cosine

2.2 Medical Implant Communication Services Band

The FCC allocated the spectrum of 402-405 MHz for MICS (Medical Implant Communication Services) applications in 1999, which is selected one of seven candidate bands for WBAN applications. The 402-405 MHz band best meets the technical requirements of MICS development for a number of reasons. The signal propagation characteristics in the band are favorable to the transmission of radio signals within the human body [5]. In addition, the relatively low RF frequency of 402-405 MHz can relax technical challenges for development of wireless devices in size, power, and complexity. Further, the use of the 402-405 MHz band for MICS devices is supported in various parts of the world including Europe, Canada, Australia, New Zealand, and the USA. Finally, the MICS frequency band does not pose a significant risk of interference to other radio operations in the band [3], [9].

The regulations for MICS band apply to devices that support diagnostic and/or therapeutic functions associated with implanted medical electronics. Possible applications

of MICS devices are illustrated in Figure 2-1. Most of devices in Figure 2-1 are stimulators such as a pacemaker, a neurostimulator, and a deep brain stimulator. Some of them aid the functionality of organs: cochlea (hearing aid), heart (heart assist), and bladder (bladder control). Lastly, implanted sensors in various positions monitor vital conditions.

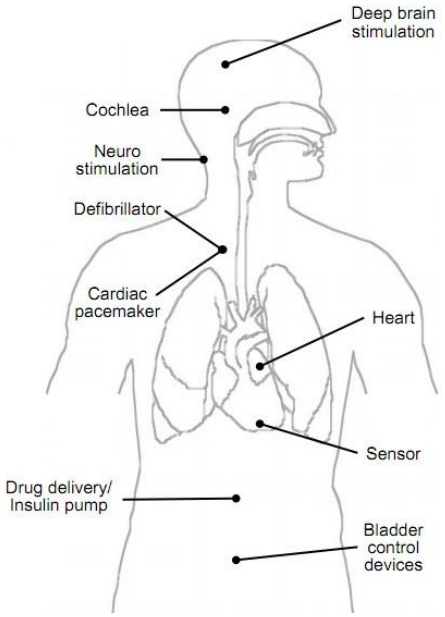

Figure 2-1 Illustration of MICS Applications

MICS communications sessions are initiated by a programmer/control transmitter, except for a "medical Implant Event". A medical implant event is one that requires the medical implant device to transmit data immediately in order to protect the safety of the person in whom the medical implant device has been placed. The key technical and operational conditions proposed for the use of MICS transmitter are [10]:

- Band of operation: 402-405 MHz.
- Maximum EIRP: 25 μW.
- Operation on a non-interference basis.

- Transmitters in implanted devices to transmit only when commanded to do so by external programmers/controllers, except for medical implant events.
- Programmer/controller devices to operate on a listen-before-transmit basis to identify and use the communication channel of lowest ambient noise.
- Frequency agility, to enable communication to occur on the lowest ambient noise channel determined to be available.

The above technical rules were established to minimize interference and ensure safe coexistence of multiple MICS devices.

In spite of the recognizable international supports, and interests from academia and industry, there are challenges for MICS developers. Implanted wireless electronics devices should be highly reliable and have ultra-low power consumption. Wireless module should also be realized with a minimum number of external components, and achieve required date rates within 2 m distance [3], [5], [6].

2.3 Sub-threshold Operation of MOSFETs

The sub-threshold operation denotes that the gate to source voltage, V_{GS}, of MOSFET is biased below the transistor's threshold voltage, V_{th}. The sub-threshold biasing technique has been widely adopted in digital, analog, and even RF circuits [1], [11] mainly because of its specific advantage, low power dissipation.

The main benefit of sub-threshold operation is the significant power saving. Figure 2-2 shows N-type MOSFET.

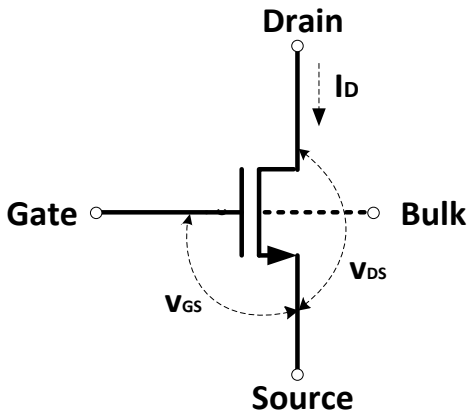

Figure 2-2 N type MOSFET

The drain current, I_D, under weak inversion is estimated by [11]

$$I_D = \frac{W}{L} I_{DO} exp\left(\frac{V_{GS}}{n\left(\frac{kT}{q}\right)}\right) \quad (2\text{-}1)$$

where W/L are the width and the length of a transistor. I_{DO} is a process-dependent factor, k the Boltzmann constant, 1.38 x 10^{-23} J/K, T the temperature (K), and q the charge of an electron, 1.6 x 10^{-19} C. n is a sub-threshold slope factor affected by the depletion region characteristics and is typically in the range of 1.4 - 1.5 for CMOS processes [12]. As can be seen in Equation (2-1), the drain current, $I_{D,}$ is exponentially proportional to the gate-source voltage, $V_{GS,}$ which is smaller than the threshold voltage, V_{th}. Thus I_D at sub-threshold operation is significantly abated comparing to I_D under the super-threshold operation. At the result, MOSFET under the sub-threshold operation consumes less DC power obtained as

$$P_{DC} = I_D \times V_{DD} \quad (2\text{-}2)$$

where V_{DD} is a supply voltage.

Sub-threshold circuits also require low voltage headroom [13], [14]. To make transistors operate in the saturation region, the drain to source voltage, V_{DS}, should be larger than V_{GS}-V_{TH} (overdrive voltage) in strong inversion. However, V_{DS} in weak inversion doesn't require a positive overdrive voltage so that sub-threshold biasing

technique is favorable for stacking or lowering a supply voltage, which further reduces DC power dissipation.

The sub-threshold operation also induces challenges to the circuit designers.

First, the absolute magnitude of trans-conductance, g_m, is notably small compared to that under strong inversion owing to the small DC bias current shown in Equation (2-3). The small g_m may cause an insufficient voltage gain to the circuit. The g_m is derived from Equation (2-1) and shown below

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

$$= \frac{\partial\left(\frac{W}{L} I_{DO} exp\left(\frac{V_{GS}}{n\left(\frac{kT}{q}\right)}\right)\right)}{\partial V_{GS}}$$

$$= \frac{\frac{W}{L} I_{DO} exp\left(\frac{V_{GS}}{n\left(\frac{kT}{q}\right)}\right)}{n\left(\frac{kT}{q}\right)}$$

$$= \frac{I_D}{n\left(\frac{kT}{q}\right)} \qquad (2\text{-}3)$$

To obtain a desired g_m with a small bias current in weak inversion, several publications have been suggested a possible solution [11], [13], [16]. Using an oversized transistor biased in weak inversion could generate to the same g_m of a small transistor operating in strong inversion. For example, a 20 μm/0.18 μm NMOS transistor biased in strong inversion with a bias current of 3 mA provides a g_m of 9.5 mS. The device provides a g_m of 0.8 mS when biased in weak inversion with a bias current of 39 μA. The g_m increases to 9.5 mS by increasing both the device width of 240 μm and the bias current to 468 μA in weak inversion. Hence, one can achieve the same trans-conductance for lower current by using a larger device still operating in the sub-threshold region [11].

Secondly, the transition frequency, f_T, of a MOSFET in weak inversion is much lower than that in strong inversion [11]. The f_T is a frequency at which the current gain is equal to unity thus transistors must be applied at frequencies well below f_T to be useful as

amplifiers. A low f_T of a transistor may limit the operating frequency of circuits. The f_T in sub-threshold region is given by

$$f_T = \frac{1}{2\pi}\frac{I_D}{\left(\frac{kT}{q}\right)}\frac{1}{WLC_{js}} \quad (2\text{-}5)$$

where C_{js} is the depletion region capacitance. As can be seen in Equation (2-5), f_T is negatively proportional to the width and the length of a transistor. Therefore, technology scaling down increases f_T with same values of I_D, kT/q, and the multi-GHz operating sub-threshold circuits have been published [16], [17]. In [11], simulation values of f_T with W/L of 120 μm/0.18 μm are calculated and obtained to 10 GHz when I_D is less than 1 mA.

Next, the noise performance of the MOSFET under the sub-threshold operation is worse comparing to one in the super-threshold operation. The sub-threshold operation might not be beneficial for the noise sensitive circuitry. However, low-rate wireless WBAN nodes require extremely low power front-ends with relaxed sensitivity specifications. Thus sub-threshold circuits are ideally suited for those applications [11], [17].

Chapter 3:
RF Receiver Architecture

This chapter reviews specific topics that should be considered for the proposed circuit design. The first section describes a heterodyne receiver architecture and its characteristics. Section 3.2 explains two particular blocks, LNA and down-conversion mixer, of the front-end heterodyne receiver. Section 3.3 reviews existing low power design of LNAs and down-conversion mixers, and merger of the two blocks.

3.1 Heterodyne Receiver

The specifications of the MICS PHY and the given bandwidth affect the design of the RF receiver architecture targeting for MICS applications. The band is the frequency spectrum in which a particular communication is granted to use, e.g., the MICS band spaning from 402 MHz to 405 MHz. The channel refers to the divided spectrum of the band for one user in the system. The MICS communication separates the band into ten channels. As a result, each channel occupies every 300 kHz within the 3 MHz band. A narrow channel at a high carrier frequency demands impractical high Q filters at the front-end of a receiver. To remedy the problem, the heterodyne receiver structure is widely adopted [18].

The premise of the heterodyne receiver architecture is to translate a high carrier frequency to a sufficiently low intermediate frequency (IF), which relaxes the required Q value of the filter. A block diagram of a basic super-heterodyne receiver front-end is illustrated in Figure 3-1.

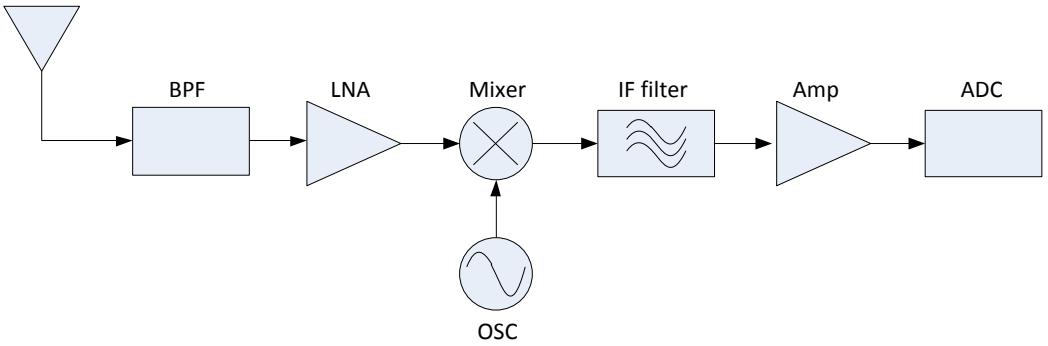

Figure 3-1 Typical Super-heterodyne Receiver Front-end

As can be seen in Figure 3-1, the low-noise amplifier (LNA) boosts up the signal induced at the antenna. The translation from the carrier frequency to an IF is performed by a mixer. The choice of the IF affects the circuit design as well as the system performance, which will be discussed in the following section. The mixer shifts the high frequency (ω_{HI}) to the IF (ω_{IF}) by mixing with the low frequency (ω_{LO}) of OSC as expressed in Equation (3-1).

$$A_1 cos(\omega_{IF})t = A_1 cos(\omega_{HI} - \omega_{LO})t \quad (3\text{-}1)$$

Then, the following IF filter removes high order harmonics. The amplifier at the final stage boosts up the filtered signal so that the analog signal is large enough to be converted to digital signal for the further processing.

3.1.1 Intermediate Frequency (IF) Selection

The IF is one of critical parameters of the system design. As explained in Section 3.1, a mixer performs the IF transaction. However, a simple analog mixer doesn't preserve the polarity of the difference between two input signals as the mixer operation is based on cosine function shown in Equation (3-2).

$$A_1 cos(\omega_{HI} - \omega_{LO})t = A_1 cos(\omega_{LO} - \omega_{IMAGE})t \quad (3\text{-}2)$$

As a result, both the desired frequency (ω_{HI}) and the undesired image frequency (ω_{IMAGE}) are down-shifted to appear at the IF frequency illustrated in Figure 3-2.

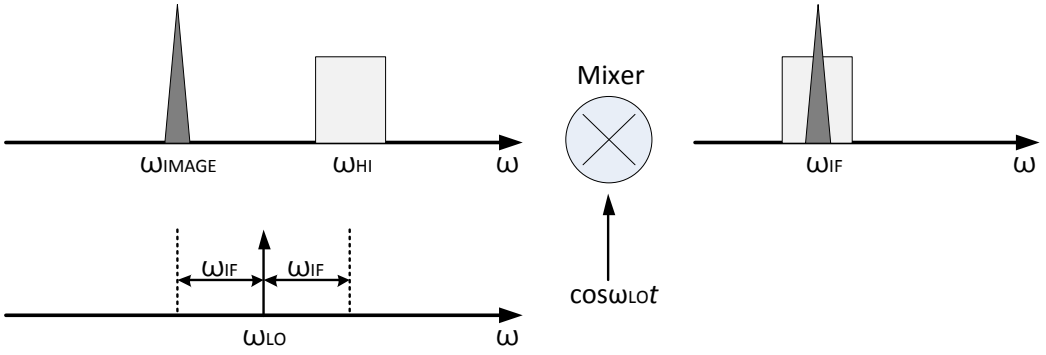

Figure 3-2 Image signal appearance at IF frequency

The image signal power could be higher than the desired signal power at the IF frequency. To solve the problem, an image rejection filter is usually placed before the mixer. Therefore, the image signal distanced by ω_{IF} from ω_{LO} can be suppressed before mixing with $\cos\omega_{LO}t$ depicted in Figure 3-3.

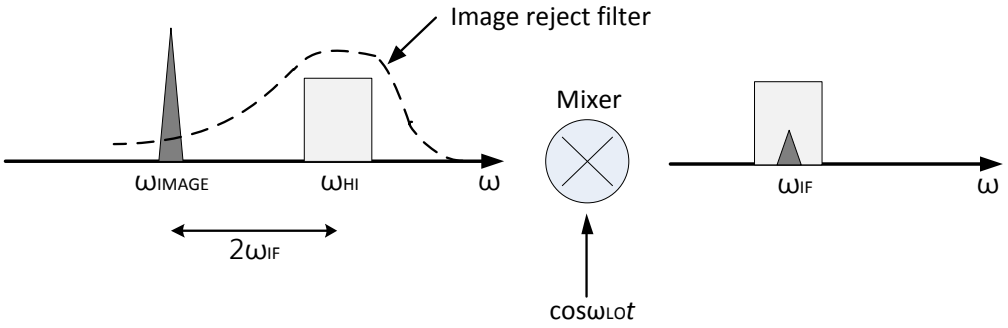

Figure 3-3 Image signal appearance at IF frequency after an image reject filter

As can be seen in Figure 3-3, the best performance of the filter can be achieved when the $2\omega_{IF}$ is large so that the image frequency is filtered out while the desired signal is preserved without requiring a high Q image rejection filter. However, a high IF frequency reduces the advantage of heterodyne receiver because a heterodyne receiver intends to reduce the burden of high Q channel selection filter by down-shifting the

carrier frequency to a relatively low IF frequency. Thus, the choice of IF depends on trade-offs between channel selection and image rejection. In addition, IF frequency directly affects not only the filter design but also the design of the oscillator later.

3.1.2 NF Analysis of Cascaded Stages in Heterodyne Receiver

A receiver consists of a cascade of multiple stages which process received signal successively. Thus, the overall system performance can be optimized through the proper trade off and balance of individual stages.

Figure 3-4 shows a cascade of multiple stages, where L, A_p, and NF indicate the loss, the available power, and the noise figure respectively.

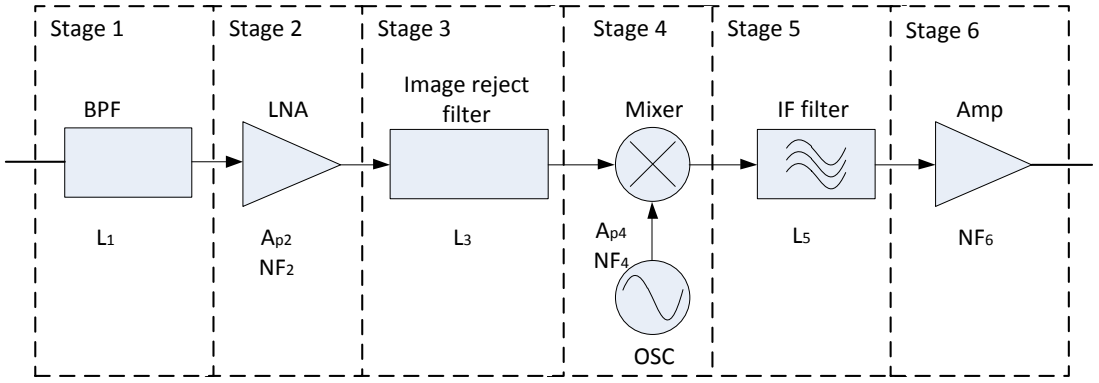

Figure 3-4 Multiple stages of heterodyne receiver

The overall system noise figure can be calculated in terms of the NF and gain of each stage based on Friis Equation given as follows [11], [18].

$$NF_{overall} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + \cdots + \frac{NF_6 - 1}{A_{p1}A_{p2}A_{p3}A_{p4}A_{p5}} \qquad (3\text{-}3)$$

According to the Friis Equation in Equation (3-3), the noise developed at each stage is attenuated by the gain of the preceding stage. As a result, the important design

consideration is obtained that the first few stages significantly contribute to NF of the overall system.

3.2 The LNA and the Down-conversion Mixer of a Heterodyne Receiver

The LNA and down-conversion mixer are the subject of the proposed research. Basic characteristics of LNA and down-conversion mixer are briefly discussed in this Section.

3.2.1 Low Noise Amplifier (LNA)

The LNA is the first block in a receiver path, and responsible for boosting up the RF signal induced at an antenna. Because the LNA is the first gain stage after the antenna, the NF of the LNA is directly added to the overall NF of the system as shown in the Friis Equation. Therefore, NF is considered as the most critical performance matrix of the LNA. Along with the NF, the third order intercept point (IIP3) determines a spurious-free dynamic range (SFDR) of the LNA [18]. The SFDR represents the maximum relative level of interferers that the receiver can tolerate while producing an acceptable signal quality from a small input level, and is obtained by

$$\text{SFDR} = \frac{2(P_{IIP3} - F)}{3} - SNR_{min} \qquad (3\text{-}4)$$

where F= -174 dBm + NF + 10log(BW) and SNR_{min} is the minimum SNR required in the system. The IIP3 also represents the linearity of the circuit. The input impedance of the LNA should be 50 Ω to achieve the maximum power transfer from the antenna with 50 Ω. The power consumption has become an important performance matrix of the LNA because of increasing usage of portable devices.

Table 3-1 summarizes, for example, performance matrix and typical values of a common gate LNA over the Bluetooth frequency band [19].

Table 3-1 LAN performance matrix and typical values for Bluetooth applications

Performance Matrix	Typical values
Noise Figure (NF)	< 5 dB
Gain	> 15 dB
In/Output Impedance	50 Ω
Power Consumption	50 mW

3.2.2 Down-conversion Mixer

A down-conversion mixer typically follows the LNA in the receiver chain. The mixer performs a frequency translation by multiplying two inputs, the RF signal and the LO signal. The signal amplified by the LNA is applied to the RF port of the mixer, thus the RF ports are expected to have low noise and high linearity. The LO signal is aperiodic waveform generated by the local oscillator. As the mixer multiplies two signals, it generates intermodulation products and high order harmonics besides the down-shifted signal desired. Therefore the linearity (IIP3) is the most important performance metric for the down-conversion mixer. For instance, the performance matrix and specifications of Gilbert Cell Mixer for Bluetooth applications are shown in

Table 3-2 [20] .

Table 3-2 Mixer performance matrix and typical values for Bluetooth applications

Performance Matrix	Typical values
Noise Figure (NF)	< 10 dB
Third Order Intercept point (IIP3)	> 20 dBm
Gain	> 8 dB
In/Output Impedance	50 Ω

Power Consumption	100 mW

3.3 Low-power Design of LNAs and the Down-conversion Mixers

The conventional front-end configuration of a heterodyne receiver is a cascaded LNA and down-conversion mixer. However, its high power consumption has become a significant obstacle to satisfy specifications of low power applications. Recently, the merged LNA and mixer configuration has been proposed in sub-mW receivers because it can reduce power consumption effectively by sharing the DC current path flowing into both of the LNA and the mixer [22]-[28]. This thesis investigates a merged LNA and down-conversion mixer, in which a primary goal is a low power design. Thus, this section reviews relevant merged LNA and mixer designs published [24]-[28].

Table 3-3 summarizes five recent designs of a merged LNA and down-conversion mixer. The all references shown in the table are designed in CMOS technology. The process varies from 65 nm to 0.18 μm, and supply voltages from 1.0 to 1.8 V. These works result a wide variety of NF, power dissipations, and gains. However, by examining these results from an architectural viewpoint, we can propose a customized merged LNA and down-conversion mixer design for targeting MICS applications.

Table 3-3 Summary of recent merged LNA and mixer works

	Ho *et al.* [24]	Amer *et al.* [25]	Song *et al.* [26]	Le *et al.* [27]	Yang *et al.* [28]
LNA topology	Differential CG	Differential CG	Single CS	Single CS	Single CG
Mixer topology	Double balanced mixer	Double balanced mixer	Single balanced mixer	Double balanced mixer	Single balanced mixer
Power consumption (mW)	34.5	9.8	0.5	1.62	0.61
NF (dB)	3.9	11.5	11.8	6	9.5
Gain (dB)	17.5	12.1	31.5	21	24
Process	0.13 μm	90 nm	0.18 μm	0.18 μm	65 nm
Supply voltage (V)	1.5	1.2	1.0	1.8	1.0
Operating frequency (Hz)	1 – 5.5 G	0.1 – 3.85 G	2.4 G	2.4 G	400 M
Year	2010	2007	2006	2009	2009

In Table 3-3, three approaches are utilized to realize the LNA stage: Differential common gate (CG), Single common source (CS), and Single CG. In general, CS topology adopted in [26], [27] provides better noise performance than other topologies and is favorable for an LNA circuit. However, high input impedance of CS stage in typical causes complicated or overloaded matching circuits to meet the input matching with 50 Ω. CG stage has inherently low input impedance and makes them ideal when trying to match

to 50 Ω for applications relaxing NF specifications. To compensate the noise performance of CG topology, special circuit treatment might be considered at the cost of circuit complexity and power dissipation. For example, the LNA noise cancellation scheme is adopted in [24] but the power dissipation of this work is too high to apply for low-power applications. Another observation for choosing the LNA stage is that the differential LNA scheme provides a better noise performance while the single-ended LNA topology consumes less power.

For the mixer stage, two topologies are selected: single balanced and double balanced. The single balanced configuration is that a mixer accommodates a differential LO signal but a single-ended RF signal. The double balanced mixer operates with both differential LO and RF inputs [18]. Examples of the configurations are depicted in Figure 3-5.

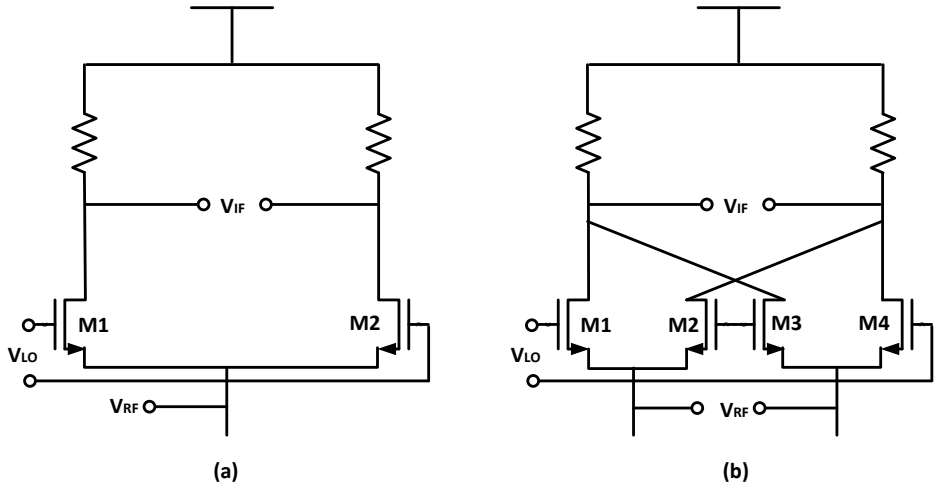

Figure 3-5 (a) Single balanced mixer, (b) Double balanced mixer

[24] and [26] adopt the single balanced mixer topology. In general, the single balanced mixer is more susceptible to noise and also cause the LO-IF freedthrough. In the case of the double balanced mixer, on the other hand, a differential output provides much more immunity to feedthrough of the RF signal to the IF output. [24] and [27] that selecting the double balanced mixer topology show the better NF over other works.

In terms of power consumption, the result of [26] and [28] is noticeable. In spite of a simple circuit topology, a merged LNA and mixer design in [26] consumes relatively low power. But this circuit requires an external current source, which make an implementation of the work unrealistic. Result in [28] also shows low power dissipation owing to the sub-threshold technique. This work targets relatively low frequency of 400 MHz thus a low transition frequency (f_t) of the sub-threshold circuit is not a problem. However, NF is too high so it will degrade the overall NF of the system.

After reviewing recent works for merged LNA and mixer design, we choose a CG LNA and double balanced mixer topology for our target application. The new idea is that the LNA operates in the normal super-threshold region and the mixer in the sub-threshold region. The mixer operating in sub-threshold region significantly reduces the power dissipation and relaxes the voltage headroom without sacrificing the LNA noise performance.

Chapter 4:
Proposed Merged LNA and Mixer Design

This chapter details the design process of the merged LNA and down-conversion mixer. After addressing the design specifications, the circuit design is explained step by step. The circuit topologies and proposed techniques are discussed, and the initial values for the circuit simulation are calculated. In Section 4-5, we deliberate the layout considerations for the circuit.

4.1 Design Specifications

The detailed specification for the proposed circuit is listed in

Table 4-1. The values are selected based on characteristics of MICS applications and existing references [9], [10], [22]-[26]. Note that the power specification is extremely low as mentioned earlier, and is the primary consideration for our proposed design.

Table 4-1 Target Specifications

	Specification Items	Values
1	Noise Figure	< 10 dB
2	Power Consumption	< 2 mW
3	Input Impedance	50 Ω
4	Input RF signal dynamic range	-85 dBm ~ -50 dBm (17.8 μV ~ 1 mV)
5	Gain	> 20 dB
6	Output impedance	~ 20 KΩ (calculated from the input impedance of the following function block, filter)
7	Output voltage dynamic range	0.18 mV ~ 10 mV

4.2 LNA Circuit Design

The typical considerations for a LNA are input matching, low noise figure, and high gain [17]. The low power consumption, however, is the primary goal for this proposed design besides the general considerations. The device parameters used in this section are based on TSMC 0.18 μm RF process technology.

4.2.1 Common-Gate (CG) LNA

For the LNA stage, we selected a Common-Gate (CG) amplifier since it has inherently low input impedance, thus provides an easy input matching. The noise performance of CG amplifier, however, is known not as good as the other topologies, therefore a noise performance requires some remedy to the circuit, which will be explained later. The common-gate LNA topology is shown in Figure 4-1.

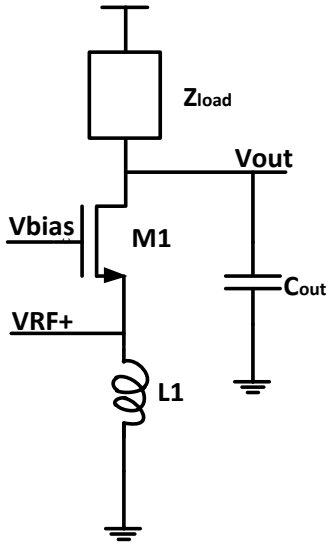

Figure 4-1 Common-Gate LNA

A small signal equivalent circuit is used to calculate the input resistance illustrated in Figure 4-2, where, g_m is a trans-conductance.

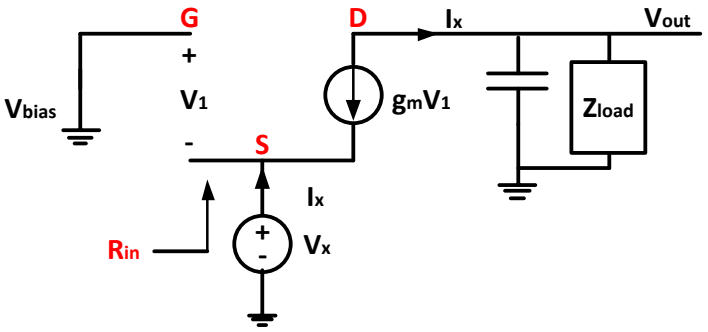

Figure 4-2 Small signal equivalent circuit of CG LNA

In Figure 4-2, L_1 is not added to calculate the input impedance since the inductance is resonated with a parasitic capacitance (e.g. C_{gs}) which is not shown in Figure 4-2. Ignoring the channel length modulation and the body effect, the input resistance is expressed in Equation (4-1).

$$R_{in} = \frac{V_x}{I_x} = \frac{-V_1}{-g_m V_1} = \frac{1}{g_m} \tag{4-1}$$

To address another essential characteristic of the LNA, the noise factor should be evaluated. The noise factor is defined as [38]

$$\mathrm{F} \equiv \frac{\text{total output noise power}}{\text{output noise power due to input source}}$$

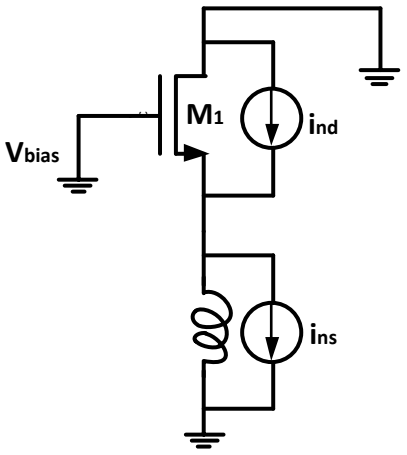

Figure 4-3 Noise sources of CG LNA

The dominant noise sources are the noise current, i_{ns}, of the source resistance and the drain current noise, i_{nd}, of the MOSFET shown in Figure 4-3. The induced gate noise is typically ignored for a CG LNA topology. The noise factor F is calculated through small signal analysis [29].

$$F = \frac{\overline{i_{ns}^2}\left(\frac{g_m R_S}{1+g_m R_S}\right)^2 + \overline{i_{nd}^2}\left(\frac{1}{1+g_m R_S}\right)^2}{\overline{i_{ns}^2}\left(\frac{g_m R_S}{1+g_m R_S}\right)^2} = 1 + \frac{\overline{i_{nd}^2}\left(\frac{1}{1+g_m R_S}\right)^2}{\overline{i_{ns}^2}\left(\frac{g_m R_S}{1+g_m R_S}\right)^2} = 1 + \frac{\overline{i_{nd}^2}}{\overline{i_{ns}^2}}\left(\frac{1}{g_m R_s}\right)^2 \tag{4-2}$$

With $\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f$, $\overline{i_{ns}^2} = 4kTR_s^{-1}\Delta f$ and $\alpha = g_m/g_{d0}$, the Equation (4-2) reduces to

$$F = 1 + \frac{4kT\gamma g_{d0}\Delta f}{4kTR_s^{-1}\Delta f}\left(\frac{1}{g_m R_s}\right)^2$$

$$= 1 + \frac{\Upsilon g_{d0}}{g_m^2 R_s} = 1 + \frac{\gamma}{\alpha}\Big|_{g_m R_s = 1} \quad (4\text{-}3)$$

where α and γ are empirical process- and bias-dependent parameters [29].

As can be seen in Equation (4-3), the noise factor is determined by the ratio of $\frac{\gamma}{\alpha}$, where $\alpha = g_m/g_{d0}$. Thus, once g_m is fixed to satisfy the input matching, the noise factor is also determined.

4.2.2 Gain-boosting Technique

To solve the contradiction of the input matching and noise performance addressed in Section 4.2.1, we adopt the Gain-boosting technique shown in Figure 4-4 [22], [30].

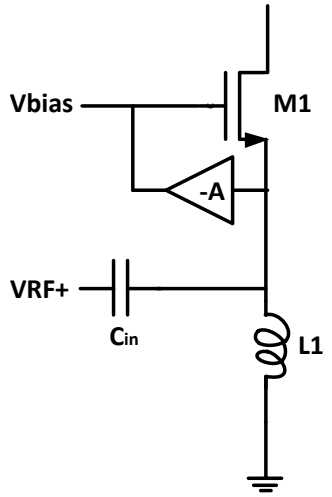

Figure 4-4 Gain-boosting technique

With an inverting gain inserted between a gate and a source terminal, the effective g_m is modified to (1+A)g_m. As consequence, the Input resistance, R_{in}, and Noise Factor, F, of the CG amplifier can be re-calculated as

$$R_{in} = \frac{1}{g_m(1+A)} \quad (4\text{-}3)$$

and

$$F = 1 + \frac{\gamma g_{d0}}{(1+A)^2 g_m^2 R_S} \quad (4\text{-}4)$$

where g_{d0}, and γ are empirical process- and bias-dependent parameters [21].

4.2.3 Differential CG LNA and Primary Calculation

The proposed LNA adopts the CG topology and the gain-boosting technique. In addition, the differential structure is chosen to support both I and Q phase signal mixing. The differential structure improves the noise performance by suppressing the common-mode noise [30]. The capacitor cross-coupled method is implemented as a g_m-boosting scheme discussed in Figure 4-4. The capacitor between a gate and a source provides an inverting gain A. Choosing a proper C_C, which determines A value, enhances the noise performance. The proposed differential CG LNA circuit is shown in Figure 4-5.

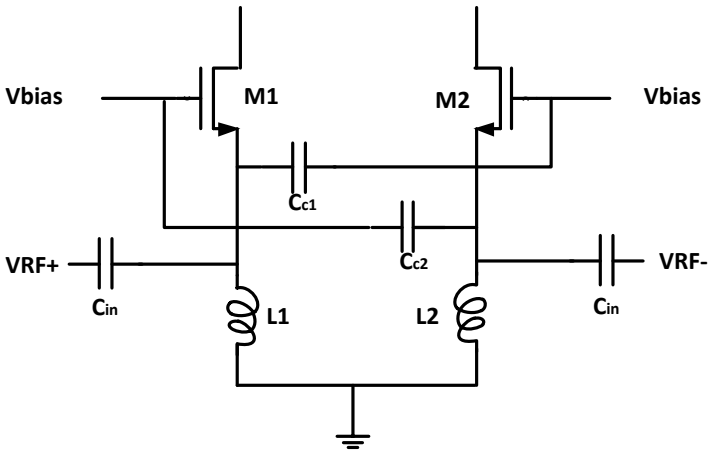

Figure 4-5 Differential CG LNA with the gain-boosting technique

With the model parameters provided by TSMC 0.18 μm RF process technology, the primary calculations are expressed as follows. So for a 50 Ω load applied to the input stage, the trans-conductance, g_m, of the input transistor is 20 mS.

$$50 = \frac{1}{g_m} \quad \therefore g_m = 20mS \quad (4\text{-}5)$$

As the specification of the total power consumption is 2 mW, for each path consumes 1 mW. The maximum current flowing from power supply is calculated based on the chosen voltage supply of 1.2 V as

$$I_D = \frac{P_{path}}{V_{DD}} = \frac{1\,mW}{1.2\,V} = 0.833\,mA \tag{4-6}$$

Then, the ratio of W/L of the transistor is determined as follows with approximate I_D of 0.8 mA.

$$g_m = \sqrt{2\mu_n C_{ox} I_D \frac{W}{L}} = 0.02 \qquad \therefore \frac{W}{L} \approx 730 \tag{4-7}$$

where, $\mu_n C_{ox} = 342 \times 10^{-6}\,A/V^2$ from the given model parameters.

For the transistor length, twice the minimum length of NMOS transistor is recommended in [32], and hence L is set to 360 nm. Then, the width of the input transistors is calculated to 263 μm.

Once the size of transistor is fixed, the parasitic capacitance can be calculated so that the required inductance is found. The parasitic capacitance of M1, dominated by C_{GS} in saturation region, can be calculated using the following expression. The model parameter of C_{GSO} is 1.92 x 10^{-10} F/m, and C_{OX} is 8.41 x 10^{-3} F/m^2.

$$C_{GS} = C_{GSO} W + \frac{2}{3} C_{ox} WL = 0.58\,pF \tag{4-8}$$

If without adding a capacitor between a gate and source terminal of M1, the resonant frequency of 403.5 MHz yields the required inductance L1 as follows.

$$f = \frac{1}{2\pi\sqrt{L_1 C_{GS}}} \qquad \therefore L_1 = \frac{\left(\frac{1}{2\pi f}\right)^2}{C_{GS}} = 0.27\,\mu H \tag{4-9}$$

The inductance is too large to implement on chip, so an additional capacitor, C_1, is added in to reduce the inductance value. A reasonable value of 15 nH for L_1 requires Cc_1 as

$$C_{c1} = \frac{\left(\frac{1}{2\pi f}\right)^2}{L_1} - C_{GS} \approx 9.9\,pF \tag{4-10}$$

Next, in order to make the current I_D = 1 mA, the proper bias voltages have to be applied to the gates of all transistors. As the DC voltage of input V_{in} is 0 V, and the threshold voltage of NMOS transistor V_{th} is around 0.47 V from the TSMC technology, we obtain the bias voltage, V_{bias}, of M1 from the following expression.

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{bias} - V_{in} - V_{th}) = 0.02 \quad \therefore V_{bias} = 0.57\,V \tag{4-11}$$

All above calculated values are meaningful for the initial simulation. There were some differences between the initial and the simulation values for the final design because the second order effects of the transistor are not considered in the initial calculation. The final component values are chosen to optimize the performance of the LNA, which is listed in Table 4-2.

Table 4-2 The final component values of the LNA

Components	Values
W/L of M1, M2	256 μm/360 nm
C_{c1}, C_{c2}	0.951 pF
L1, L2	12.85 nH
V_{bias}	0.53 V
I_d	0.764 mA
f_{rf}	403.5 MHz

4.3 Down-conversion Mixer Circuit Design

As addressed in the Chapter 3, a down-conversion mixer is designed to provide the low noise and high linearity performance. In addition, the power reduction technique plays the crucial role in designing the proposed mixer.

4.3.1 Double-balanced Mixer

The double-balanced mixer is one with both differential LO and RF inputs, which is shown in Figure 4-6. The double-balanced mixer generates less even-order distortion, thus relaxing the IF issues for a heterodyne receivers as addressed in the previous chapter.

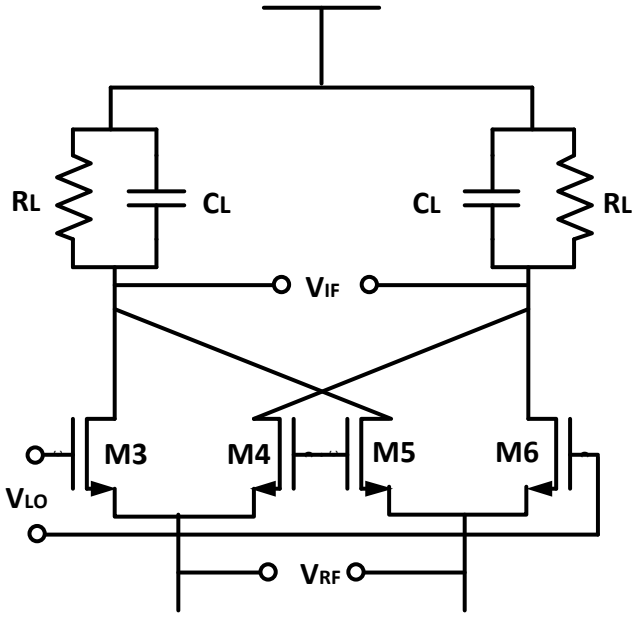

Figure 4-6 Double-balanced mixer

The mixer is stacked with the LNA to share the same bias current. The size of each transistor for the mixer is set to L = 360 nm and W = 128 μm, which are half size of the LNA, thus the current through each transistor is a half of that for the LNA. Targeting the mixer gain of 20 dB, the load resistance R_L of the mixer is obtained as

$$A_v = \frac{1}{2} g_m R_L = 10 \quad \therefore R_L = 1\ K\Omega \tag{4-12}$$

To improve the power gain, a capacitor C_L is added in paralleled with R_L acting as a low pass filter. The low pass filter filters out the high order harmonics of the mixer. As the LO frequency is 402 MHz and the frequency of the RF input 403.5 MHz, the cut-off frequency of the filter is f_c = 403.5 – 402 = 1.5MHz. Thus C_L is obtained as

$$f_c = \frac{1}{2\pi R_1 C_L} = 1.5MHz \qquad \therefore C_L = 0.2pF \tag{4-13}$$

These above values are selected for the initial simulation setting, and then optimized through extensive simulations.

4.3.2 Sub-threshold Operation

In this work, the strategy of the proposed mixer design is the sub-threshold operation while the input LNA stage operates in strong inversion. In consequence, the noise performance of the LNA is not degraded, and the output swing of the mixer has enough margins even under a low supply voltage of 1.2 V. As addressed in Chap 2, transistor under weak inversion has a lower f_t comparing to that under strong inversion. However, a low f_t is not an issue for our design as MICS band of 402-405 MHz is much lower than typical f_t.

Since the size of transistor is already determined, the bias voltage should be carefully decided for the mixer circuit in Figure 4-6. M3 and M4 of the differential mixer evenly divides the bias current I_D, and hence the current flowing in each path is $I_D/2$ = 0.4mA. Thus, the DC voltage of output V_{IF} can be found as

$$V_{IF\_DC} = V_{DD} - R_L \frac{I_D}{2} = 0.8\,V \tag{4-14}$$

The LO bias voltage determines the operation condition of the mixer and should meet the following conditions

$$0 < V_{gs} < V_{th}$$

$$0 < V_{LO_{bias}} - V_x < V_{th} \;\rightarrow\; 0 < V_{LO_{bias}} < V_x + V_{th} \tag{4-15}$$

where V_x is an intermediate voltage between the LNA and the mixer stages. The V_{th} is around 0.47 V.

The bias voltages of M3 and M4 should be equal because the differential mixer is symmetrical. Finally, an appropriate LO bias voltage meeting the above conditions was

obtained through simulations. The final component values of the mixer are tabulated in Table 4-3.

Table 4-3 The final component values of the differential mixer

Components	Values
W/L of M3,M4, M5, M6	128 μm/360 nm
R_L	2 KΩ
C_L	1 pF
V_{LObias}	0.65 V
f_{LO}	402 MHz
f_{if}	1.5 MHz

4.4 Merged LNA and Mixer Circuit Design

4.4.1 Merged LNA and Mixer Overall Schematic

To support BPSK modulation, two double-balanced mixers are implemented on the top of the LNA as shown in Figure 4-7. The transistor of M1 and M2 realize a CG LNA. Transistors from M3 to M10 realizing a mixer work like switching pairs with LO signals. The double balanced mixer produces In (I) and Quadrature (Q) phase of the IF signal. The RC tank considered with load capacitors at the mixer output builds a low-pass filter that filters out the high order harmonics. A fully differential structure improves the noise performance by suppressing the common-mode noise.

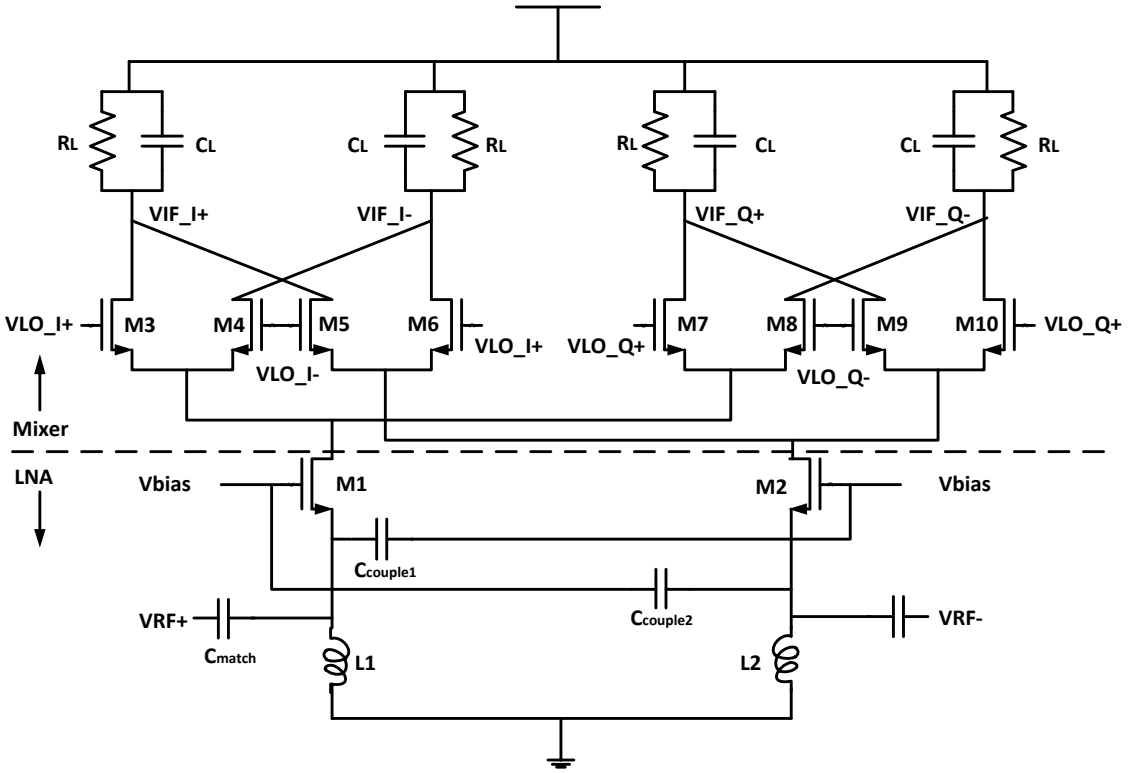

Figure 4-7 The proposed merged LNA and mixer

The merged LNA and mixer does not require an interstate matching network, thus saves chip area and cost in addition to saving power through reuse of the bias current.

4.5 Merged LNA and Mixer Layout

4.5.1 Layout considerations

The performance of analog and RF circuits are heavily influenced by the layout. There has been many issues regarding to proper layout for specific circuits, and typical layout considerations can be summarized as followed.

- Multi-finger transistors

The width of the transistor is much larger than the length for typical analog and RF transistors. Thus, the wide transistors are usually folded so that the gate resistance and

S/D junctions are reduced. For our design, all transistors have 32 fingers as shown in Figure 4-8.

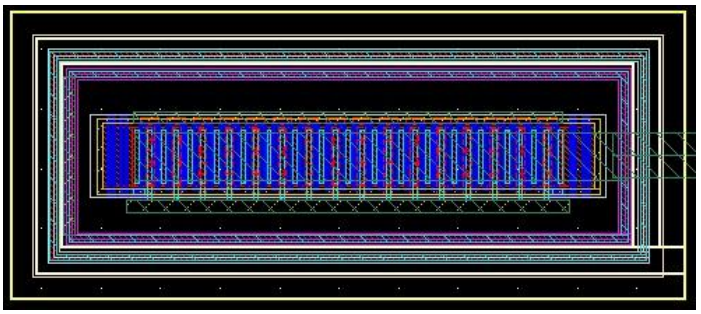

Figure 4-8 Multi-finger NMOS transistor

- Symmetry

In our layout design, the symmetry was considered with great care because the designed circuit is differential and symmetric. Any mismatch or non-symmetry may result in large offsets to the circuit performance. In addition, the symmetry must be applied to both the devices of interest and their surrounding environment.

- Reference distribution

The reference distribution is a hot issue not even in the analog/RF circuit layout but also in the digital circuit layout. The supply voltage is low, thus a small voltage fluctuation can affect significantly to the circuit performance. In the layout, the transistors of the LNA stage is placed close to the RF signal PAD so that the RF signal suffer less from the voltage drop and parasitic caused by long and winding wires.

- Passive components

In the given RF technology, there are six different types of resistor and four of capacitors. Each one has its own pros/cons. According to the proposed circuit's best interest, the MIM (metal-insulator-metal) capacitor is chosen. Regarding to the resistors, three different types of resistor are adopted to meet the need of resistor values: N-well

resistor, P+ poly resistor with salicide and P+ poly resistor w/o salicide. The 3-terminal P+ poly RF resistor is illustrated in Figure 4-9.

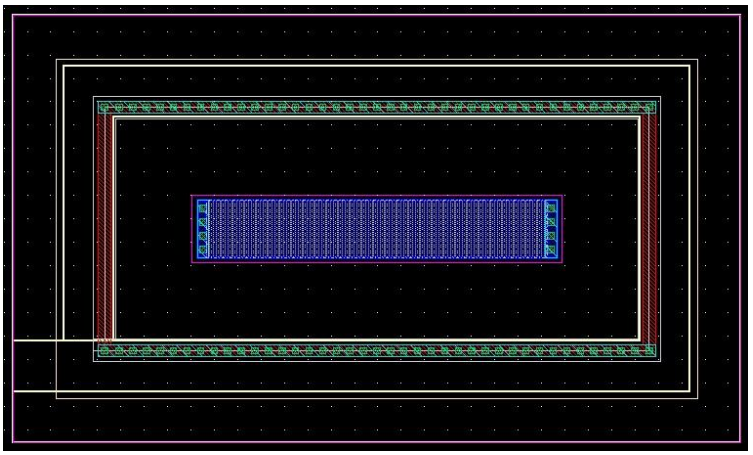

Figure 4-9 3-terminal P+ poly RF resistor with silicide

The most area consuming component is an inductor among passive components. The number and the size of inductors in the circuit normally indicate the size of full-chip. There are three different types of inductors (standard, symmetric, and symmetric with center tap) supported for the chosen CMOS technology. In this design, the standard inductor is chosen to meet our inductance value. The inductor drawn in metal 6 layer is illustrated in Figure 4-10.

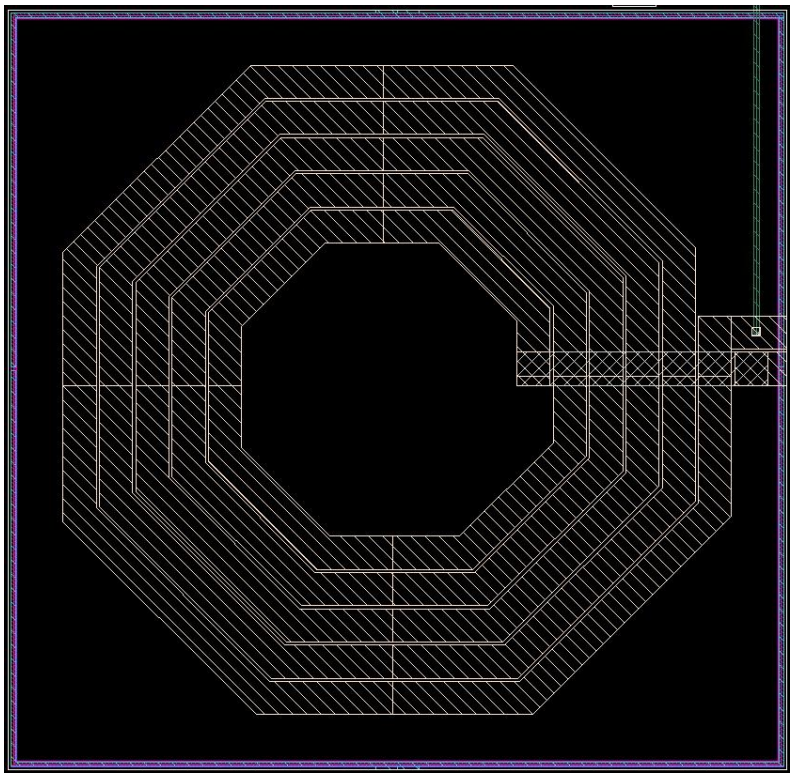

Figure 4-10 Standard inductor

- Metal interconnections

The effect of interconnections is not considered in the circuit design, however it plays crucial role in real circuit performance through the layout. The most troublesome phenomenon is the crosstalk. Two techniques are well known to reduce the crosstalk. The benefit of the differential signals sitting next each other is the first method. Next, the shielding is popular to less the crosstalk effect of signals.

4.5.2 Overall Layout

The final layout design is shown in Figure 4-11. As can be seen in the layout, the two inductors are placed symmetrically. The design itself is symmetric, thus half of the layout is duplicated as a mirror image. The total core size of the proposed circuit excluding pad spaces is 1465 x 945 μm^2.

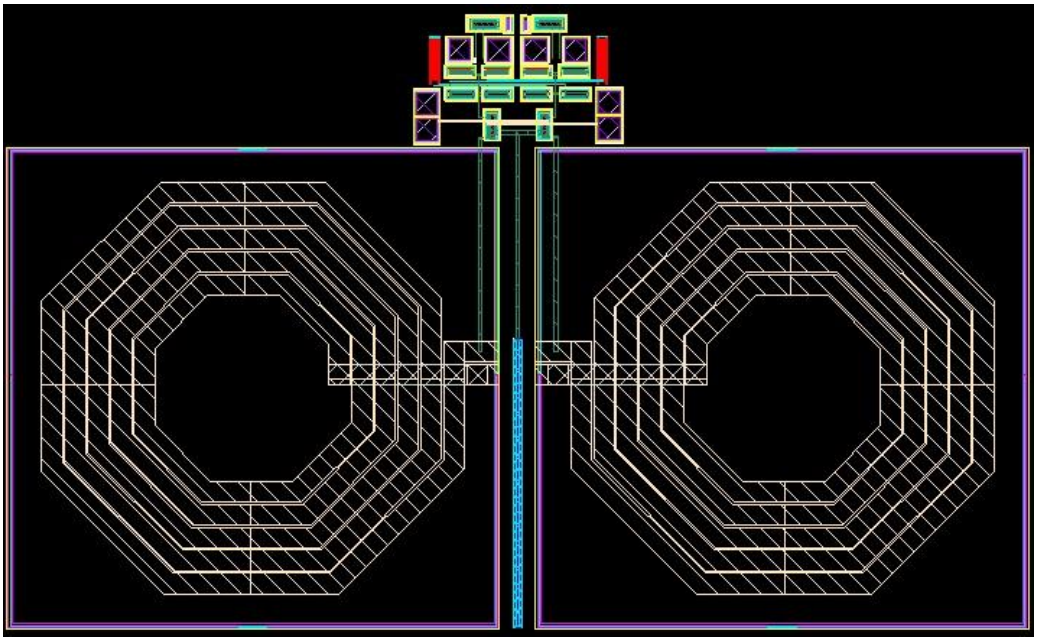

Figure 4-11 Full-chip layout

Chapter 5:
Simulation Results

The proposed merged LNA and mixer is designed in TSMC RF CMOS 0.18 μm technology and was simulated with SpectreRF. The pre-layout simulation results are presented in this chapter.

5.1 Simulation Environment

Error! Reference source not found. shows a test bench which is used to valuate the performance of the proposed merged LNA and down-conversion mixer through simulations. The test bench consists of a design under test (DUT) and input/output ports for the DUT. Port 1 is the RF signal source with an 50 Ω impedance, and the balun generates differential signals to the LNA input inside of DUT. Port 2, 3 generate LO signals and are followed by transformer to provide the 180° phase-shifted two LO signals to the down-conversion mixer. VLO_I and VLO_Q have 90° phase difference. The port 4 and 5 are output ports of the DUT. The decoupling capacitor, 10 nF, is placed between the output of the mixer and the ports. To provide a supply voltage and ground, V_{DC} of 1.2 V and GND is initiated in the test bench. The bias voltages for LNA, V_{bias}, and for mixer, $V_{LO\ bias}$, are set to 0.53 V and 0.65 V respectively. For the simulation, the V_{RF} is chosen to 403.5 MHz with a RF power of -50 dBm, and the V_{LO} to 402 MHz with a power of -16 dBm.

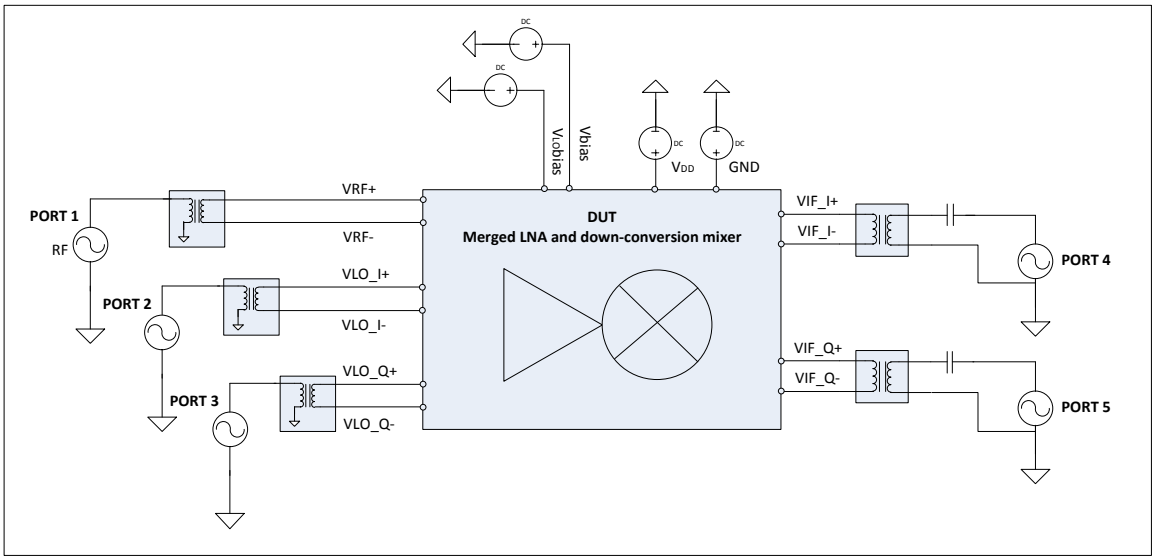

Figure 5-1 Circuit Simulation Test bench

5.2 Noise Figure (NF)

The NF is obtained to 3.52 dB at the chosen IF frequency of 1.5 MHz shown in Figure 5-2 . Comparing to other works in Table 3-3, the obtained NF is remarkably small. The NF would be degraded after the layout, pads, and packaging. However, the design specification for NF was 10 dB so 3.52 dB is good enough to meet our target design for the MICS applications.

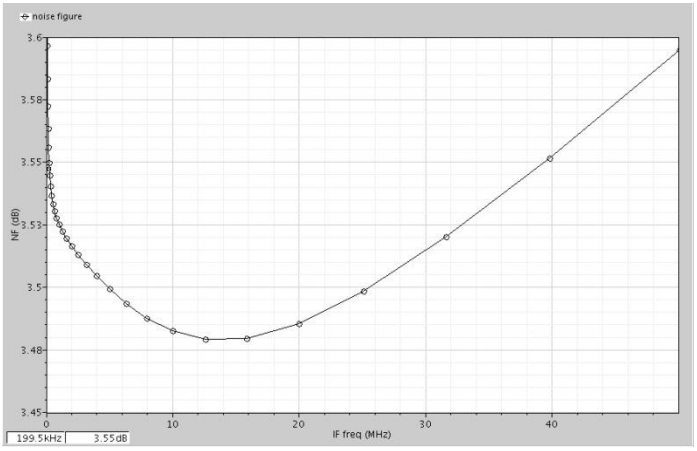

Figure 5-2 Noise Figure vs IF frequency

5.3 Conversion Gain

The input signal frequency (RF) and the output signal frequency (IF) of the proposed circuit are different due to the mixing operation. Thus, we calculate the conversion gain. The conversion gain is defined as the ratio of the rms voltage of the IF signal to the rms voltage of the RF signal [18]. Figure 5-3 shows the conversion gain for the proposed circuit. The conversion gain over the MICS frequency band, 402 - 405 MHz, is larger than 20 dB which is our target gain specification. The gain performance itself is not superior comparing to other publications [26], [28]. However, the proposed circuit is well balanced with overall circuit performances including a power dissipation and NF.

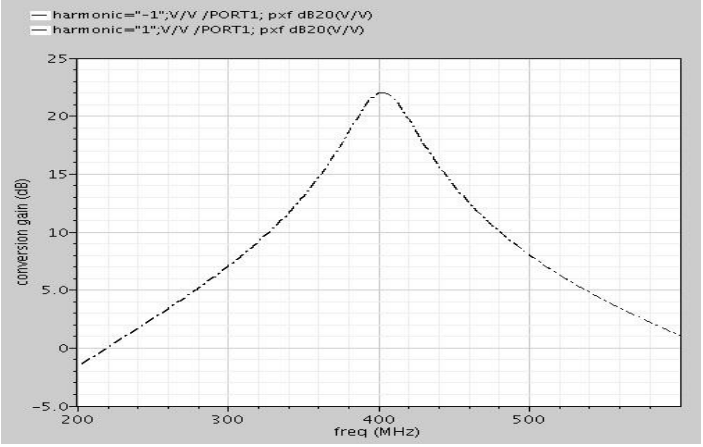

Figure 5-3 Conversion Gain versus Input RF frequency

5.4 S parameters

The S parameters indicate the power transform at the port or between ports. The S_{11} is the ratio of the reflected power over the incident power at the port 1 in the two-port system, and a smaller the reflected power is more desirable. The merged LNA and down-conversion mixer is the front-end of the receiver, thus S_{11} is meaningful to be checked. Figure 5-4 shows the S_{11} of the proposed circuit for the MICS band. S_{11} is less than -25 dB through the MICS band, which is considered good. The low S_{11} value implies a good input matching, which is mostly determined by the LNA input, not the mixer. Therefore,

we can conclude the sub-threshold operation of the switching transistors for the mixer does not degrade the input matching.

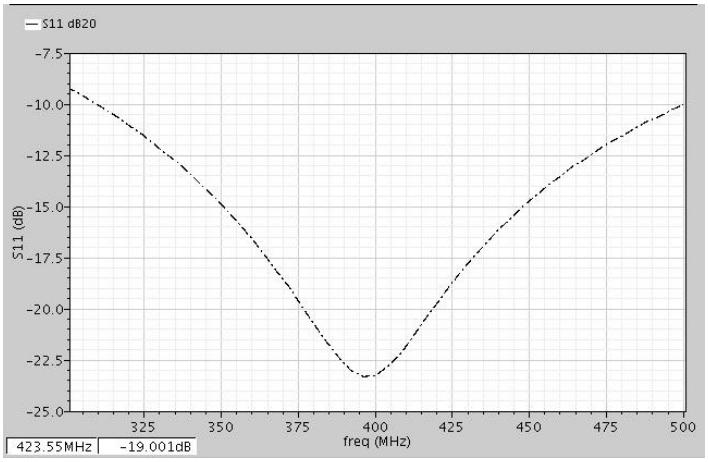

Figure 5-4 S_{11} versus input RF frequency

5.5 Linearity (P1dB and IIP3)

The distortion produced by a circuit is characterized at high frequencies, and particularly with narrowband circuits, in terms of a compression point or an intercept point. Two in-band sinusoid signals are applied to measure the distortion for a narrow band circuit, which is called a two-tone test. Two frequencies of 403.5 MHz and 404 MHz are set as RF for the two-tone test, and the LO frequency of 403 MHz. The input RF power for both signals varies from -85 dBm to 0 dBm while the power of the LO signal remains at -16 dBm.

The 1dB compression point, P1dB, is the point where the input signal level is decreased by an amount 1dB. The P1dB for the proposed circuit is obtained at the input power of -19.214 dBm shown in Figure 5-5. Since the input RF power is given between -85 dBm to -50 dBm, the 1dB compression point is out of the input dynamic range.

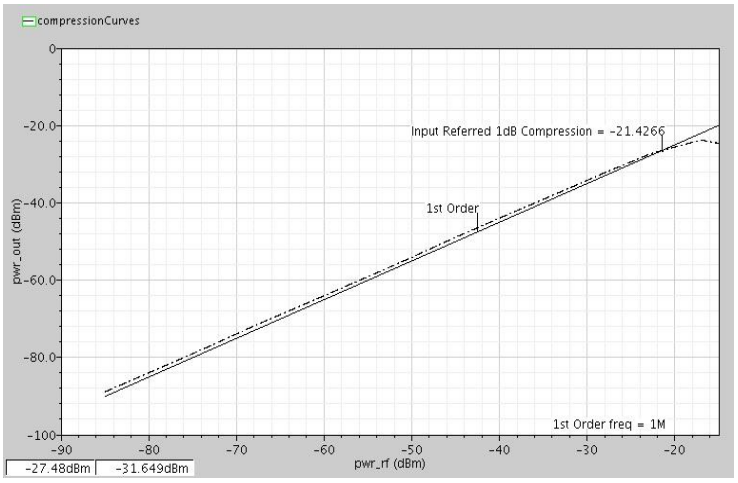

Figure 5-5 P1dB vs input power

The input referred 3rd order intercept point, IIP3, is a figure of merit to indicate the nonlinearity of the system. It is based on the idea that the distortion is mainly due to the 3rd order intermodulation. The IIP3 is the point where power of the 3rd order intermodulation term and the linearly amplified 1st order input power signal term meet. The IIP3 for the proposed circuit is obtained at the input power of -6.8 dBm shown in Figure 5-6. As addressed earlier, the input RF power is given between -85 dBm to -50 dBm, the IIP3 is out of the input dynamic range. Thus the system provides high linearity over the given RF power for MICS applications.

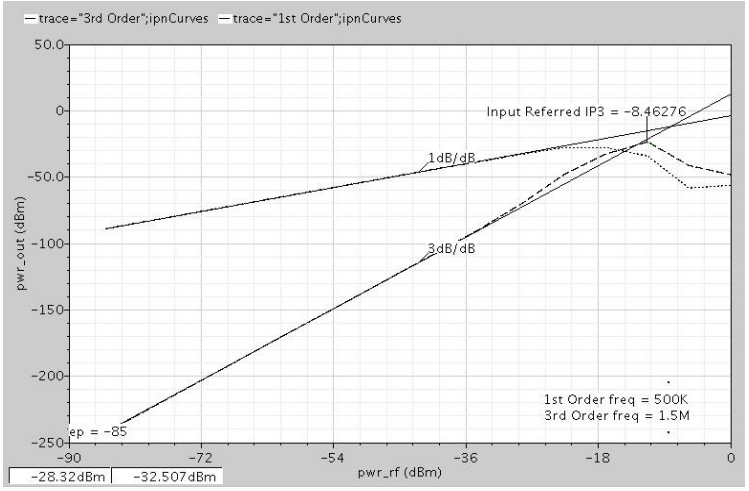

Figure 5-6 IIP3 vs input power

5.6 Result Summary

Table 5-1 summarizes the performance of the proposed merged LNA and a down-conversion mixer, and compares the result with that of other works in Table 3-3 [24], [25], [28]. Three references are chosen to be compared because the basic circuit topology of [24], [25] is the same as the proposed circuit, in which a CG LNA and a double-balanced mixer are adopted, and [28] realizes the sub-threshold operation.

Table 5-1 Performance of the Proposed Circuit and Other Existing Works

	This work	Ho *et al.* [24]	Amer *et al.* [25]	Yang *et al.* [28]
Process	TSMC RF 0.18 μm	CMOS 0.13 μm	CMOS 90 nm	CMOS 65 nm
Operating frequency (Hz)	402-405 M	1 – 5.5 G	0.1 – 3.85 G	400 M
Supply voltage (V)	1.2	1.5	1.2	1.0
Power dissipation (mW)	1.834	34.5	9.8	0.61
Noise figure (dB)	3.6	3.9	11.5	9.5
Conversion Gain (dB)	21.6	17.5	12.1	24
S_{11} (dB)	-26	< -8.8	< -10	-50
P1dB (dBm)	-19.214 @ f_{IF}=1MHz	-10.5	-12.8	NA
IIP3 (dBm)	-6.08	0.84	NA	NA

The power consumption of the proposed circuit is notably low comparing to [24], [25]. As we anticipated, the sub-threshold technique reduced power dissipation substantially. The result of [28] also consolidates our assumption as the transistors in [28] fully operate in weak inversion and shows a disadvantage of the sub-threshold technique, which the noise performance is degraded. In our proposed circuit, transistors for LNA are set in strong inversion while transistors for the mixer operate in weak inversion. Thus the noise performance wasn't debased. In addition, the input matching of LNA wasn't affected by the sub-threshold operation of the mixer. The conversion gain for the proposed circuit has a relatively less margin, however adding an extra amplifier after the mixer could possibly solve the problem at the cost of power dissipation. The linearity is not comparable with other works because the input signal power range varies according to the applications. However, the P1dB and IIP3 are out of input power range for our applications and implicate the high linearity over the input signal power range from -85 to -50 dBm.

Chapter 6:
Conclusion

Traditionally, communication schemes in medical devices used short-range magnetic coupling. These systems limit the communication range as it requires close coupling between the data center and monitoring devices. In 1999, the FCC established MICS band allocated from 402 to 405 MHz in frequency spectrum. The MICS applications overcome the range limitation of inductive systems and promote development of next generation medical devices. One major challenge associated with these implantable devices is to extend their operation lifetime under the limited energy source. Therefore, low-power realization is a primary design goal besides high reliability. In particular, the power consumption of the implemented electronics is rigorously related to the design of RF circuits. To address the challenge, this thesis investigates the front-end circuits of the heterodyne receiver, and proposes the sub-threshold merged LNA and a down-conversion mixer.

In Chapter 4, the sub-threshold merged LNA and down-conversion mixer circuit is designed and laid down in the RF CMOS 0.18 μm technology. To achieve the primary goal, low power design without degrading other performances, three main features are employed. The key feature of the proposed circuit is that transistors in the LNA stage operate in strong inversion while transistors consisting mixer are optimized to operate in weak inversion. The second one is that the LNA and the down-conversion mixer are stacked to share the same bias current through the LNA and the mixer. The last one is adoption of a gain boosting technique.

As expected, the mixer operating in weak inversion significantly reduces power consumption and relaxes the voltage headroom without sacrificing the LNA performance. The relaxed voltage headroom enables the stacking of the LNA and the mixer with a low supply voltage of 1.2 V. The performance of the circuit is presented in Chapter 5. The proposed merged LNA and mixer consume only 1.83 mW while achieving NF of 3.52 dB

at the chosen IF frequency of 1.5 MHz, which is a significant improvement than other published results. Although the noise performance would be degraded after layout, pads, and packaging, the result is good enough for the target MICS applications. The conversion gain over the MICS frequency band, 402 - 405 MHz, is obtained slightly larger than 20 dB. Because of the sub-threshold operation, the power gain is inferior to other works. The P1dB is obtained at the input power of -19.214 dBm, and the IIP3 of -6.08 dBm for input RF power ranging from -85 dBm to -50 dBm. These results show that the proposed circuit provides high linearity over the given RF power for MICS applications.

With obtained results of a super low-power consumption and reliable noise performance, we conclude the proposed circuit design is well suited for MICS applications.

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