Methodology for Switching Characterization of Power Devices and Modules

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This thesis submitted to the Faculty of Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

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In
Electrical Engineering
Approved:

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Key words: Switching characteristics, power MOSFET, IPEM, power module

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Abstract

In modern power electronics systems there is a growing trend to replace discrete devices with integrated power electronic modules (IPEMs). In this way, several components can be replaced by a single component. By using prefabricated building blocks, the engineer simplifies the design process, reducing the total design cycle time and cost. By integrating only the necessary components to provide power switching, the end user has a pre-optimized building block with the flexibility to be used in a large variety of applications.

Besides simplifying the design process, power modules should be designed in such a way as to improve the performance of the power converter. This begs the question as to how best to judge if one IPEM has better performance than another or better performance than its discrete counterpart. In analyzing a converter's performance, popular criteria include efficiency, power density, device stresses, and EMI. All of these criteria are strongly linked to the switching characteristics of the IPEM's power devices.

This thesis is a comprehensive study of the requirements for obtaining and analyzing the switching characteristics of the IPEM's power devices. It outlines the important switching characteristics and the implications of each characteristic on converter performance. It deals with the relevant measurement issues, specifically addressing the minimum requirements, which sensors are most suitable, and problems leading to inaccurate data. A parametric study is conducted to determine the effects of several circuit and operating parameters on the switching characteristics. Using the resulting data and the knowledge from the measurement study, we can decide how to design the testbed layout, what operating conditions should be chosen for testing, and what effects of the tester must be decoupled to truly see the effects of IPEM design. The thesis concludes with the design of standard test equipment and procedures.

Acknowledgements

I would like to thank my advisor Dushan Boroyevich. Many times, he came in early or left the office late to help me. Dr. Boroyevich is an advisor who is willing to work as hard for the student as the student works for him. He is a dynamic teacher whose courses will be an asset to my future in power electronics. With his enthusiasm and good humor, Dr. Boroyevich makes the study of power electronics fun and rewarding.

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I would like to thank my many friends and coworkers, the students at CPES. It is great to work with a group of people that are so willing to help. I have enjoyed my time here and wish the best of luck to everyone at CPES.

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I could not have made it this far without the love and encouragement of my parents Richard and Katherine Witcher. They have always supported me and been there to make sure I had what I needed. I also thank my sister, Dawn, and my brothers, Ricky and Shane who have been my strength in hard times.

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My aunt Sue and uncle Doug have helped me on many occasions. Working at Doug's company, Pressure Systems, during the summers of my junior and senior years in high school sparked some of my initial interest in electrical engineering. Since moving to Blacksburg, they have been a constant source of encouragement, and I appreciate all they have done for me.

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Chapter 1 – Introduction and Background

1.1 Motivation for the use of IPEMs

In modern power electronics systems there is a growing trend to replace discrete devices with integrated power electronic modules (IPEMs) [1,2]. In this way, several components can be replaced by a single component. By using prefabricated building blocks, the engineer simplifies the design process, reducing the total design cycle time and cost [1]. Besides simplifying the design process, power modules should be designed in such a way as to improve the performance of the power converter. For instance, the IPEM may be designed to minimize parasitic inductances and common-mode capacitances [3]. To this end, several packaging and interconnect technologies such as power overlay [4], embedded power [5] and flip-chip on flex [6] have been developed. These simple changes can decrease device voltage stresses, increase converter efficiency, and improve the EMI performance [1-3]. Other necessary features for the power device operation, such as the gate driver, can also be integrated into the module to further enhance performance. By integrating only the necessary components to provide power switching, the end user has a pre-optimized building block with the flexibility to be used in a large variety of applications.

1.2 Evaluation of Power Modules and Devices

If the continued evolution of power electronics, as experts believe, depends on the development of integrated modules, then industry must be given incentive to invest in IPEM technology. The high costs and low yields typically associated with new ventures don't provide much incentive. This means that the investor must have great faith or they must see the improvement in performance. This begs the question as to how best to judge if one IPEM has better performance than another or better performance than its discrete counterpart.

In analyzing a converter's performance, popular criteria include efficiency, power density, device stresses, and EMI [1]. One of the greatest contributors to the decrease in

a high frequency converter's efficiency is the switching energy loss of the power devices. Power density is limited by the maximum switching frequency of the power devices, which is limited by the minimum switching times and the switching losses of the devices [7]. Device stresses include voltage and current overshoots, which occur during the switching transitions due to circuit and power device parasitics in the presence of the high rates of current and voltage change [8-11]. The dv/dt's and di/dt's also create electromagnetic fields that interfere with the operation of the surrounding electronics [12-14]. Although IPEMs may become new "integrated devices", the switching characteristics of its power devices dominate the performance of a converter.

Whenever a new discrete power device technology is introduced, one of the primary focuses will be the improvement in the switching characteristics. For example, the newly developed CoolMOS transistor and SiC Schottky diode combination are exclaimed for their usefulness in high frequency PFC applications due to reduced losses, switching times and voltage stress [15,16]. Due to the power devices' intimate relationship with the converter performance, and therefore the value of the module, it seems only natural that the switching characteristics of the module's devices should be an integral part of the evaluation process.

1.3 Standardizing the Test Equipment and Procedures

Power module datasheets will typically indicate switching delay times and the drain-source (MOSFET) or collector-emitter (IGBT, BJT) voltage rise and fall times for a module's power devices [17]. When power devices are tested, the typical setup includes the device-under-test, a gate-drive, and a resistive load in series with the device output [17]. They will also provide some basic operating parameters such as gate resistance, gate voltage, voltage across the output of the device, and the current switched.

Several potential problems exist with the current approach. The amount of switching characteristics information may not be enough for the end user to know if a particular module is suitable for their application. It is well known and documented that switching losses are related to current rise and fall times, not just the voltage rise and fall times typically given in datasheets [7]. Switching energy loss is an important parameter in

determining maximum switching frequency and power density. Voltage and current stresses, which have implications on converter long-term reliability, are related to di/dt and dv/dt switching rates [8-11]. The aforementioned characteristics are a few of the device characteristics that are needed to demonstrate a module's performance.

In a typical converter, the power device is switching an inductive load current, which stays nearly constant over a switching cycle. The resistive load setup used to obtain the switching times in many datasheets does not emulate converter operation. To obtain useful data, testing of the power device should be done with similar operating conditions as the application circuit. A popular and widely accepted test circuit that better mimics converter operation uses a clamped inductive load rather than a resistor [8,18,19].

As the power electronics community continues to drive for increased power density and faster transient response, there is a growing need to increase switching frequency [1]. However, as the switching frequency increases, the adverse effects of circuit and module layout parasitics on the switching characteristics become more pronounced [8-13]. In light of this fact, a person testing a power device may find it very difficult to duplicate datasheet values. Also note that decreasing switching times usually implies smaller gate resistance. With testing now using gate resistances as low as 2 Ω, the output impedance of the gate drive becomes an important issue, since it is the combination of these impedances that determines the total driver circuit impedance. As switching speeds are increased, it may become important to provide circuit parameters such as the parasitic inductances and gate drive characteristics in addition to the device output voltage and current, gate resistor, gate voltage, and temperature.

To fairly analyze a module's performance and make comparisons amongst designs, it is imperative to use standard test equipment and test procedures. The switching characteristics measured will be sensitive to the electrical layout of both the IPEM and the test circuit. The characteristics may be sensitive to gate drive parameters and the operating current, voltage and temperature. The test equipment should be designed to be sensitive to changes in the module design, and the operating conditions should be chosen to be similar to those of the module's applications. Since the IPEMs are intended to be flexible building blocks, they may be used over a wide range of voltages, currents, and temperatures. For characteristics that are sensitive to changes in these operating

conditions, it may be necessary to sweep over a range of values to adequately characterize the module.

1.4 Thesis Objectives

The original objective of the project that led to this thesis was to build a simple tester to obtain the switching characteristics of the power devices of the IPEM shown below in Figure 1.1. The task turned out to be far from simple. Initial measurements showed unexpected characteristics in the switching waveforms. Continued measurements and initial simulations revealed that the switching characteristics were sensitive to several circuit layout, component and operating condition parameters. As such, the switching characteristics tester cannot be designed arbitrarily. Furthermore, it was determined with the aid of simulation that a number of measurement issues needed to be solved in order to collect accurate and consistent switching characteristics data.

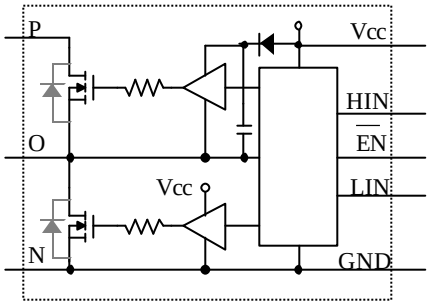

Figure 1.1. Schematic of the Gen. II IPEM developed at CPES Virginia Tech.

Hence, the main objective of this work is to evaluate the influence of the circuit and operating parameters that are external to the power device, on their switching characteristics, and to experimentally quantify the most significant relationships. This thesis specifically focuses on meeting the following goals:

1) Determine the measurement requirements for obtaining accurate switching characteristics data.
2) Determine the relationships between critical circuit and operating parameters and the switching characteristics.

3) Explore the requirements for modeling the test circuit for accurate simulation of the switching characteristics.
4) Propose a design for a switching characteristics tester as a standard tool for characterizing power devices and IPEMs.

Although it was attempted to make the discussions and conclusions as generic as possible, the study was restricted on the MOS-gated devices for low- to medium-power applications, specifically on the switching characteristics of power MOSFETs with breakdown voltages in the 400-600 V range and current ratings in the 5-50 A range."

1.5 Switching Characteristics

Collection of the switching characteristics for a power MOSFET is accomplished through measurements of the gate-source voltage (V_{gs}), drain-source voltage (V_{ds}), and the drain current (I_d). See Figure 1.2 below. While this example and the waveforms illustrated in sections 1.5.1 and 1.5.2 are for a power MOSFET, the definitions for the switching characteristics are general in that they can also be directly applied to IGBTs and other switching devices. Also note that this section does not intend to explain the general operation of a switching device. Thorough explanations of the general operation of power MOSFETs and IGBTs can be found in [7,8,11,17,18]. This section will instead define the switching characteristics measured and explain their key implications on a converter.

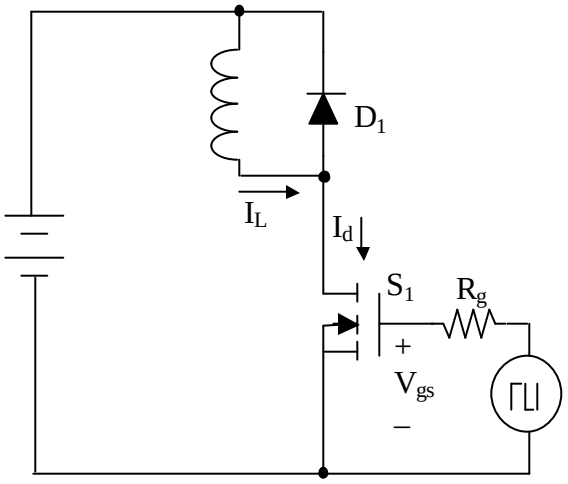

Figure 1.2. Clamped Inductive Load Test Circuit.

1.5.1 Turn-on Characteristics

Figure 1.3 shows the gate-source voltage, drain-source voltage and drain current waveforms for the turn-on transition. Each of the characteristics of interest are labeled in the figure and described in the following sections.

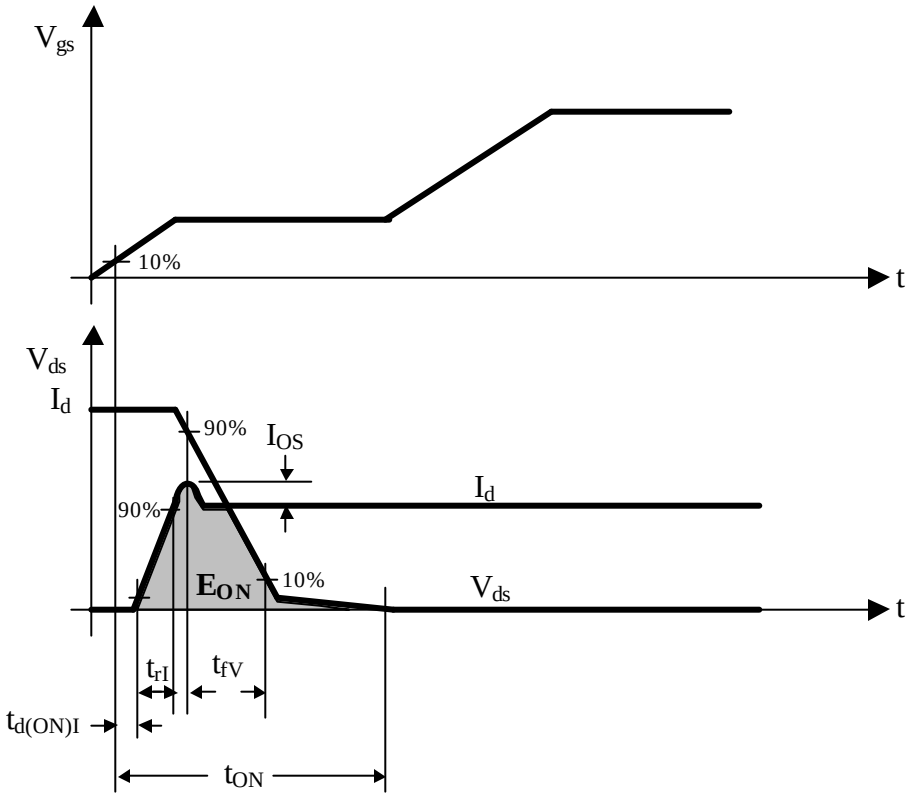

Figure 1.3. Turn-on Switching Characteristics.

1) Turn-on Time (t_{ON})

The turn-on time is the time from when the gate voltage (V_{gs}) rises to 10% of the nominal gate voltage to when the drain voltage (V_{ds}) reaches saturation. This parameter indicates how fast the device can be turned on, which will be a limiting factor for the maximum allowable switching frequency.

2) Current Turn-on Delay Time ($t_{d(ON)I}$)

The current turn-on delay time is the time from when the gate voltage rises to 10% of the nominal gate voltage to when the drain current rises to 10% of its nominal value.

This parameter indicates how fast the device reacts to being turned on, and is one of the contributing factors to the total turn-on time. As such, this delay time will limit the maximum switching frequency. Also note that a long turn-on delay time can lead to significant pulse-width distortion and phase lag (example of pulse-width distortion and phase lag is given in Appendix A).

3) Current Rise Time (t_{rI})

The current rise time is the time it takes for the drain current to rise from 10% to 90% of the nominal current. This parameter indicates how quickly the drain current can approach the load current. It is one of the contributing factors to the total turn-on time and switching energy and will partially determine the maximum possible switching frequency.

4) Voltage Fall Time (t_{fV})

The voltage fall time is the time it takes for the drain voltage to drop from 90% to 10% of its nominal value. This parameter indicates how quickly the drain voltage can approach saturation. It is one of the contributing factors to the total turn-on time and switching energy and will partially determine the maximum possible switching frequency.

5) Turn-on Switching Current Gradient

The turn-on switching current gradient, or di/dt(on), is the slope of the drain current during its rising edge, measured at 50% of the nominal current. This di/dt indicates current switching speed and contributes to parasitic ringing and EMI.

6) Turn-on Switching Voltage Gradient

The turn-on switching voltage gradient, or dv/dt(on), is the slope of the drain voltage during its falling edge, measured at 50% of the nominal drain voltage. This dv/dt indicates voltage switching speed and contributes to parasitic ringing and EMI.

7) Current Overshoot (I_{OS})

Current overshoot is the amount of current by which the drain current peak value exceeds the nominal value. This parameter is the current stress and can affect the reliability of the power device. It can also contribute significantly to the turn-on energy.

8) Turn-on Energy (E_{ON})

The turn-on energy loss is defined as the integral of the instantaneous product of the drain current and the drain voltage during the turn-on time. E_{ON} is one part of the total switching losses and is typically one of the largest sources of loss in a high frequency converter.

1.5.2 Turn-off Characteristics

Figure 1.4 shows the gate voltage, drain voltage and drain current waveforms for the turn-off transition. Each of the characteristics of interest are labeled in the figure and described in the following sections.

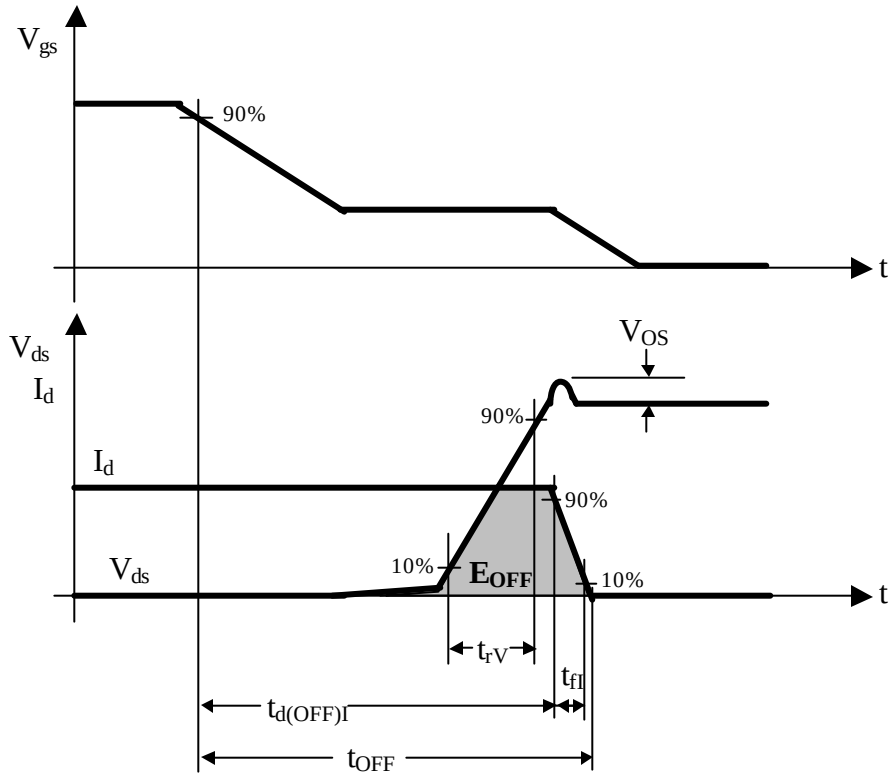

Figure 1.4. Turn-off Switching Characteristics.

1) Turn-off Time (t_{OFF})

The turn-off time is the time from when the gate voltage drops to 90% of the nominal gate voltage to when the drain current (I_d) reaches zero. This parameter indicates how fast the device can be turned off, which will be a limiting factor for the maximum allowable switching frequency.

2) Current Turn-off Delay Time ($t_{d(OFF)I}$)

The current turn-off delay time is the time from when the gate voltage drops to 90% of the nominal gate voltage to when the drain current drops to 90% of its nominal value. This parameter indicates how fast the device reacts to being turned off, and is one of the contributing factors to the total turn-off time. As such, this delay time will limit the maximum switching frequency and increase the pulse-width distortion.

3) Current Fall Time (t_{fI})

The current fall time is the time it takes for the drain current to fall from 90% to 10% of the nominal current. This parameter indicates how quickly the drain current can approach zero. It is one of the contributing factors to the total turn-off time and switching energy and will partially determine the maximum possible switching frequency**.**

4) Voltage Rise Time (t_{rV})

The voltage rise time is the time it takes for the drain voltage to rise from 10% to 90% of its nominal value. This parameter indicates how quickly the drain voltage can approach the bus voltage. It is one of the contributing factors to the total turn-off time and switching energy and will partially determine the maximum possible switching frequency.

5) Turn-off Switching Current Gradient

The turn-off switching current gradient, or di/dt(off), is the slope of the drain current during its falling edge, measured at 50% of the nominal current. This di/dt indicates current switching speed and contributes to parasitic ringing and EMI.

6) Turn-off Switching Voltage Gradient

The turn-off switching voltage gradient, or dv/dt(off), is the slope of the drain voltage during its rising edge, measured at 50% of the nominal drain voltage. This dv/dt indicates voltage switching speed and contributes to parasitic ringing and EMI.

7) Voltage Overshoot (V_{OS})

Voltage overshoot is the amount of voltage by which the drain voltage peak value exceeds the nominal value. This parameter is the voltage stress and can affect the reliability of the power device. V_{OS} also gives an indication of how well the layout and chosen switching speed match. A critically damped voltage transient yields a good compromise between switching losses and EMI content.

8) Turn-on Energy (E_{OFF})

The turn-off energy loss is defined as the integral of the instantaneous product of the drain current and the drain voltage during the turn-off time. E_{OFF} is one part of the total switching losses and is typically one of the largest sources of loss in a high frequency converter.

1.6 Thesis Outline and Accomplishments

The remainder of this thesis is dedicated to exploring the essential necessities for accurately obtaining the switching characteristics of power modules and devices. The first waveforms captured at the outset of this thesis work were discovered to have considerable error. It was found that making measurements of switching waveforms is a non-trivial task. Chapter 2 demonstrates the important measurement equipment specifications that must be satisfied to gain accurate voltage and current waveforms and data. This chapter also deals with some of the difficult measurement related problems that were overcome.

Chapter 3 gives the experimental setup for a parametric study that explores how and why several circuit parameters affect the switching characteristics. It provides the necessary circuit layout and component choice considerations. This chapter also gives

the modeling techniques that were applied. A simulation example is demonstrated, and further results are given in Appendix D. Most of the waveforms and data trends are very similar to the measured results, validating the success of the modeling efforts.

Chapter 4 provides and analyzes the switching waveforms and characteristics under the various conditions tested for the parametric study. A qualitative sensitivity analysis is performed that directly compares the relative effects of the varied parameters. The results of the parametric study and sensitivity analysis can be used to establish the relationship between several of the critical circuit and operating parameters and the switching characteristics. The results are also used to decide how the tester should be designed and what operating conditions and information should be applied for the creation of the switching characteristics datasheets.

Chapter 5 takes what is learned from the previous chapters in order to design a switching characteristics tester. General design considerations and guidelines are developed. This chapter specifically addresses the circuit layout considerations, measurement equipment specifications, and chosen operating conditions for the final tester. The last chapter will conclude and summarize the work presented and make suggestions for future work.

Chapter 2 – Important Issues in Measurement

2.1 Overview of general needs and limitations

By their nature, power switches have high current and voltage rates of change and radiate large electromagnetic fields. These phenomena make the gathering of accurate measurements of a power device's switching characteristics a difficult challenge. The waveform one see at the oscilloscope is not the same as the waveform at the tip of the probe, and it is certainly not the same as the electrical signal of the circuit under test. Under certain conditions (i.e. very fast switching), it may even become impossible to trust the measurement. The next several sections will describe some of the issues involved in acquiring accurate data and analyzing the limitations of the measurement equipment. The next two sections discuss how to determine the necessary bandwidth for a measurement and how to calculate the effective bandwidth of a measurement system. One section talks about the elimination of ground loops and how to improve voltage measurements by minimizing the probe tip-to-ground loop inductance. Two of the sections describe specific problems in measuring voltage and current waveforms.

2.2 Signal Equivalent Frequency

When measuring square-wave signals such as the switching waveforms of a power device, it is important to understand that the equivalent frequency of the signal measured is much greater than the switching frequency. A square-wave is made of an infinite Fourier series, as demonstrated in Equation 2.1 and Figure 2.1 below. The shape of the rising and falling edges of the waveforms is highly dependent on the higher order harmonics. To obtain an accurate representation of the shape of the signals during the switching intervals, the measurement equipment must be able to measure these higher frequency components.

$$f(t) = A + \frac{4A}{p}\left[\sin(w_0 t) + \frac{1}{3}\sin(3w_0 t) + \frac{1}{5}\sin(5w_0 t) + \ldots\right] \qquad (2.1)$$

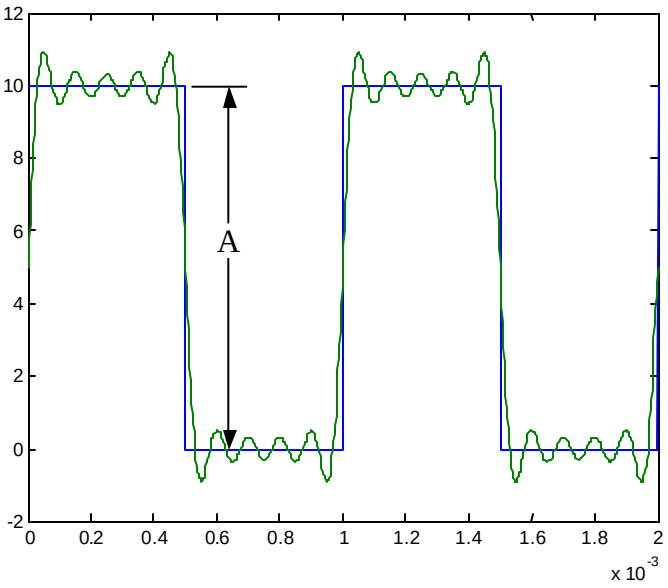

Figure 2.1. A square-wave consists of many harmonics.

Since bandwidth specifications are based on sinusoidal excitations, a sine-wave with the same slope and magnitude as the square-wave's edges can be used to approximate the signal's equivalent frequency. Referring to Figure 2.2, note that the sine-wave has a very similar shape as the rising edge of the square-wave signal. The measurement equipment must have a bandwidth much greater than the frequency of this sine signal to accurately represent the signal.

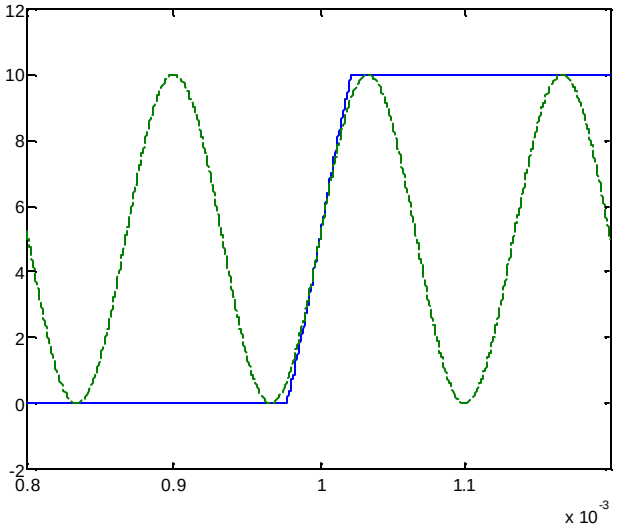

Figure 2.2. Using a sine-wave to determine a rising edge's equivalent frequency.

The frequency of the sine-wave signal can be approximated by the following equation:

$$f = \frac{0.25}{t_r} \tag{2.2}$$

where t_r is the 10% to 90% rise time of the square-wave signal. The derivation of Equation 2.2 is based on the slope and magnitude of the square-wave signal and is given in more detail in Appendix B.

2.3 Measurement System Bandwidth

A measurement system is made up of a probe and the oscilloscope. By connecting the probe to the oscilloscope, two frequency-dependent components are cascaded. The system bandwidth is not the same as that of the probe or oscilloscope alone. To determine if a given system will provide an adequate measurement, the calculation of Equation 2.3 below can be used to approximate the system bandwidth.

$$BW_{sys} = \frac{1}{\sqrt{\frac{1}{BW_{osc}^{\ 2}} + \frac{1}{BW_{probe}^{\ 2}}}} \tag{2.3}$$

The bandwidth of the system gives the limitation of the measurement to accurately represent the magnitude and phase of the electrical signal. Remember that at the bandwidth frequency, the measurement magnitude is about 70% of the real signal magnitude. For the magnitude consideration, the system bandwidth should be three to five times higher than the maximum equivalent frequency of the signal measured to provide an accurate representation [20]. For measurements of time intervals (such as measuring the time delay between signals), it important to understand that there is already a 45° phase shift at the probe bandwidth. For the phase consideration, the system bandwidth should be higher than ten times the highest equivalent frequency of the measured signal [20].

2.4 Grounding

The negative terminal of every probe input to the oscilloscope is common and tied to earth ground. The measurements of gate voltage, drain voltage, and drain current do have a common ground point, but the probes cannot physically lie directly on top of each other. So, there will be small ground loops. The impedances between these grounds in the presence of the large current rates of change will cause circulating energy to oscillate in the probe ground paths [20, 21]. It is imperative that these loops be made as small as possible.

2.4.1 Capacitively Coupled Ground Loops

Another constraint to the system is that no other earth ground points should appear in the circuit. The DC bus voltage source will use long wires to connect to the testbed, which will be a high impedance connection. Its output terminals should be differential and have low capacitance to the earth ground. Unfortunately, many supplies use copper foil for the windings of its isolation transformer, which will create a significant capacitive coupling to the earth ground. The result will be a capacitively coupled ground loop as shown in Figure 2.3. The parasitic inductance and capacitance of this loop causes common-mode ringing in the current measurement, I_d (refer to Figure 2.4).

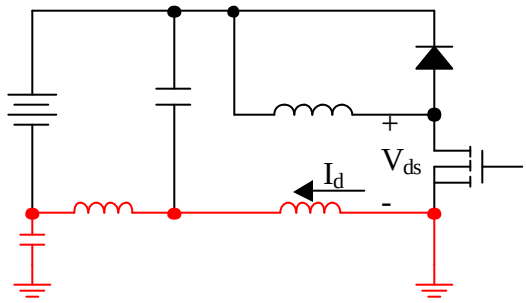

Figure 2.3. Capacitively coupled ground loop.

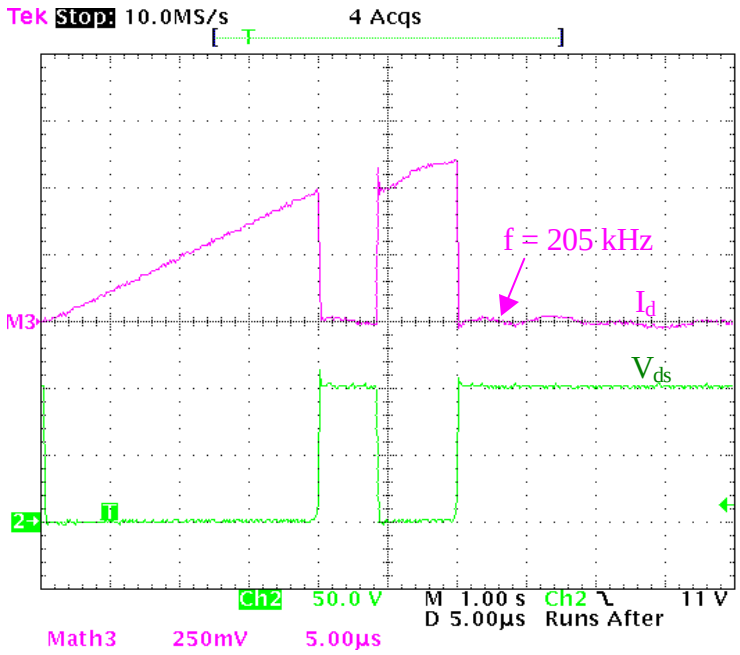

Figure 2.4. Current measurement without the common-mode choke.

To alleviate this problem, a common-mode choke with high impedance at the common-mode ringing frequency can be employed as in Figure 2.5 [22]. Figure 2.6 shows the measured impedance of the used choke. Note that this measurement was actually made across only one of the windings, so that the actual impedance is really twice that of the measurement shown. Because this impedance is so high at the common-mode signal frequency, essentially no current will flow through the capacitance to ground, and the loop is broken. Figure 2.7 shows the current waveform with common-mode choke included. Note that the 205 kHz common-mode ringing has been eliminated.

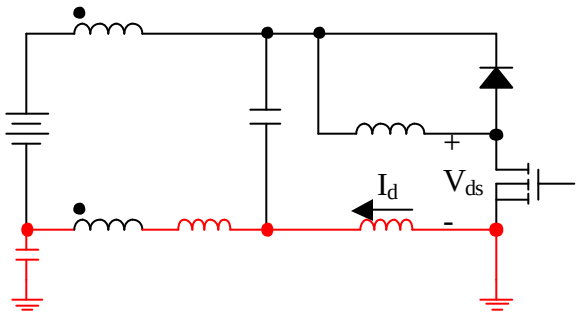

Figure 2.5. Decoupling of the ground loop using a common-mode choke.

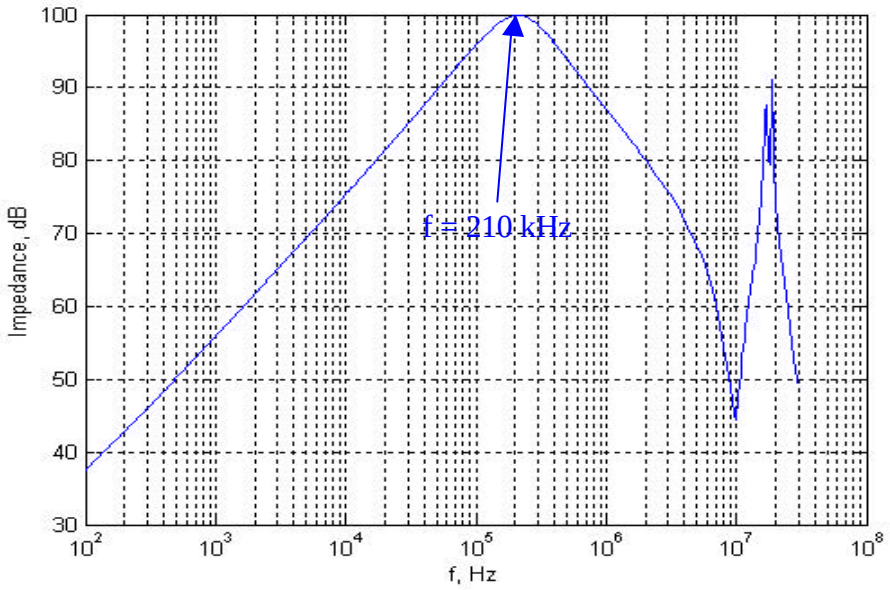

Figure 2.6. Common-mode choke impedance magnitude.

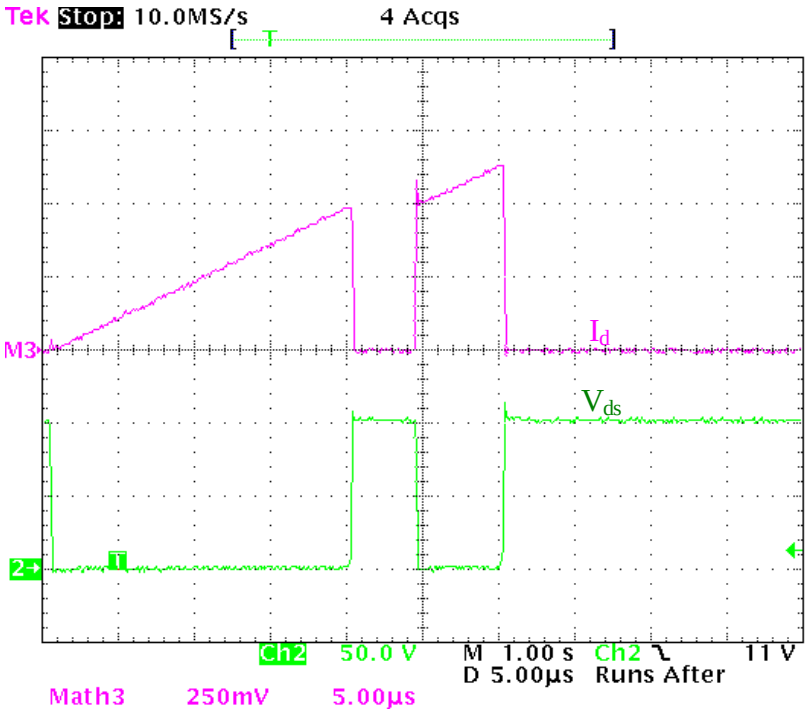

Figure 2.7. Current measurement with the common-mode choke.

2.4.2 Tip-to-Ground Loop Inductance

Another important parameter is the voltage probe tip-to-ground loop inductance. Figure 2.8 shows the equivalent model of a typical voltage probe. Probe ground leads are inductors in series with the measurement. In the presence of high dv/dt's and large electromagnetic fields, this wire will create errors in the voltage measurement. To reduce the measurement errors, a probe-tip adaptor, demonstrated in Figure 2.9, can be used to reduce the tip-to-ground loop inductance [20]. Figure 2.10 shows the drain voltage measurement made with probes using a typical ground lead and using the probe-tip adaptor.

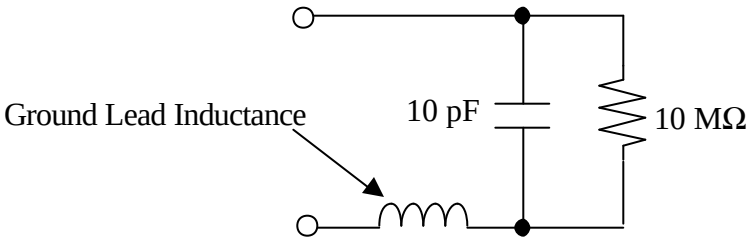

Figure 2.8. Equivalent model of a typical voltage probe.

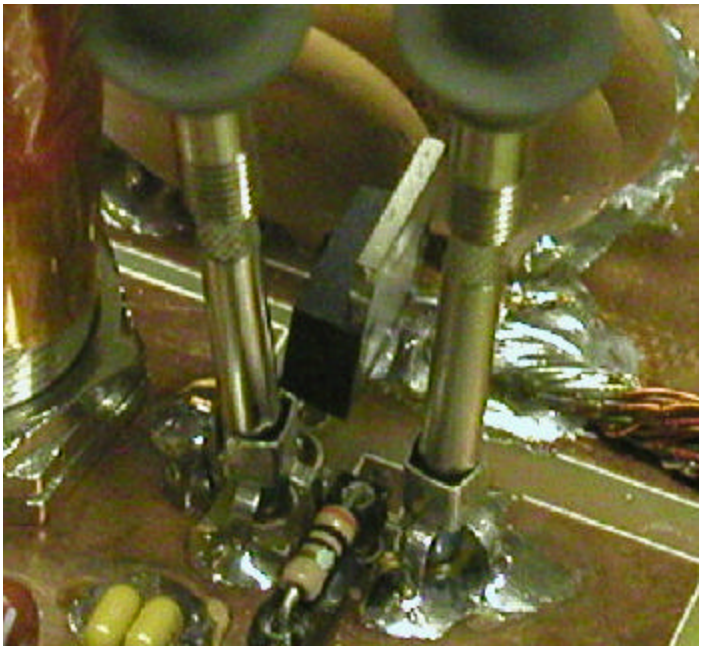

Figure 2.9. Reduced tip-to-ground loop using a probe-tip adaptor.

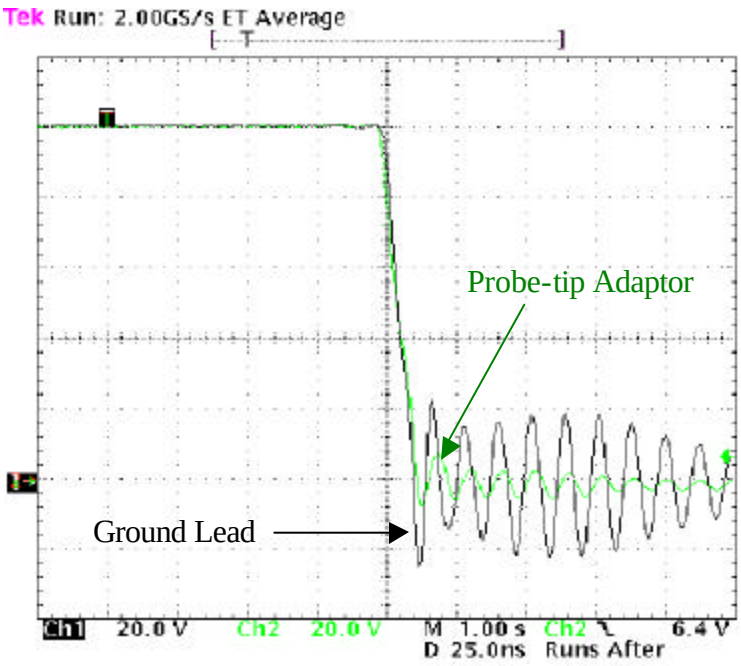

Figure 2.10. V_{ds} measurement using typical ground lead vs using probe-tip adaptor.

2.5 Voltage Measurement

The two voltage measurements that are necessary for device switching characterization are the gate voltage and drain voltage of the device-under-test (V_{gs} and V_{ds} in Figure 1.2). Some of the voltages measured will be in excess of 400 V. Three types of probes available for this high voltage measurement are differential probes, voltage divider probes and 10X attenuation passive probes [20].

2.5.1 Differential Probes

Differential probes have the advantage that the measurement is not referenced to earth ground, alleviating the worry about small ground loops between probes. However, high voltage differential probes are typically limited in bandwidth to around 100 MHz due primarily to its differential amplifier's slew rate [20]. In addition, the leads used to make the connection to the DUT are typically longer than those of a single-ended probe. The effect of this inductance can become significant for the fast transients measured.

2.5.2 Voltage Divider Probes

Voltage divider probes are often used where high bandwidth (even several gigahertz) is a necessity. Unfortunately, the oscilloscope used will limit the measurement system bandwidth, and its advantages cannot be fully realized. In addition, voltage divider probes often have relatively high resistive loading [20]. This loading can cause significant amplitude errors when measuring voltage across high impedance such as the drain-source voltage when the switch is off.

2.5.3 Single-ended 10X Passive Probes

The single-ended passive probes have significantly higher bandwidth than the differential probe. In addition, the single-ended probe can utilize probe-tip adaptors, greatly reducing the measurement loop parasitic inductance compared to the differential probe. Also, the 10X probe will have much lower resistive loading than the voltage divider probe. For these reasons, a passive probe was chosen for the voltage measurements in this thesis. Most oscilloscope manufacturers specify certain probes for specific scopes and specify the measurement bandwidth as a system bandwidth [20]. If the probe used is not one that is matched to the oscilloscope, the system bandwidth should be calculated as given in Equation 2.3 above. The oscilloscope/probe combination used in this thesis was the Tektronix TDS744A oscilloscope with the P6139 passive probe, which provides a system bandwidth of 500 MHz.

2.6 Current Measurement

Several different current measurement techniques exist, each with their own advantages and disadvantages. The tools most widely used for oscilloscope measurements are current transformers, Rogowski coils, surface mount resistors, and coaxial shunts [23-26]. It is among these tools that we should choose to measure the switch current and inductor current (I_d and I_L in Figure 1.2). Note that Hall-effect sensors are not considered for the current measurement. In the initial search for current sensors, it was observed that Hall-effect probes were generally limited in bandwidth to far less than the necessary bandwidth needed.

For the switch current measurement, the sensor must be able to accurately follow rise times less than 10 ns. This dictates that the bandwidth must be greater than 250 MHz to accurately represent the phase of the rising and falling edges. The current amplitude could be as low as 5 A and as high as 50 A. The measurement device must be sensitive enough to represent small currents in the presence of large noise sources, and it must not saturate at the high current end. In addition, the sensor should not create large insertion impedances into the test circuit. Because the current transducer for the switch current measurement will share a common point with the voltage measurements, it is not necessary to have galvanic isolation.

The inductor current frequency will always be less than 1 MHz, so the bandwidth should be greater than 10 MHz. The amplitude will be the same as the switch current, and has the same constraints. Because the inductor current transducer will not share a common point with the voltage measurement, it must have galvanic isolation from the test circuit.

2.6.1 Rogowski Coils

Rogowski coils have bandwidth and accuracy limitations that make them less reliable for the transient current measurement. The upper bandwidth limit is set according to the self-inductance and capacitance of the coil and the slew rate of the integrator, and it is typically less than 1 MHz [23]. Rogowski coils do exist that can measure higher frequencies (near 100 MHz), but not that can simultaneously measure the lower frequency components of current. For this reason, a Rogowski coil should not be used for measuring the switch current. For the coils available, the accuracy may vary by several percent depending on the position of the current-carrying conductor in the coil's loop. So, the Rogowski coil is also not used for the inductor current measurement.

2.6.2 Current Transformers

Current transformers (CT) have bandwidth limitations similar to those of the Rogowski coils. The CT cannot measure DC current and its high frequency cutoff will be limited by internal resonances [25]. A CT will not be used for the switch current measurement. However, a current transformer, Pearson Electronics model 411, is used

for the inductor current measurement. This CT has a bandwidth from 1 Hz to 20 MHz and does not suffer from the accuracy discrepancies like the Rogowski coil [24]. In addition, it provides the necessary galvanic isolation for the inductor current measurement.

2.6.3 Surface Mount Resistors

Using an ideal resistor, the bandwidth would be limited only by the voltage probe used. However, all resistors have a certain amount of series inductance. The voltage measured will have a very different shape from the current flowing through the resistor. Figure 2.11 shows a simulated pulse current measurement, where the voltage is measured across the resistor alone and where it is measured across the resistor and its parasitic inductance. Note that the series inductance gives the false impressions of a faster rise time and higher current overshoot. Even very small values of inductance can have a large impact on the measurement in the presence of fast rise times. Many surface mount resistors in parallel would be required to reduce this effect.

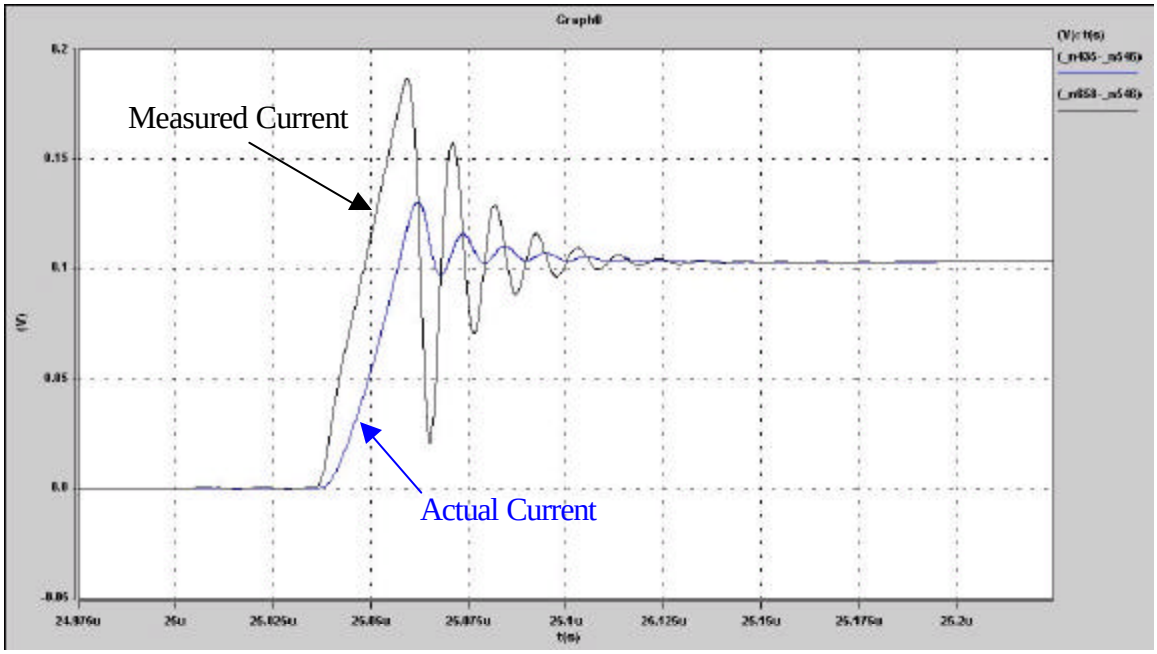

Figure 2.11. Actual current versus current measured with R=10mΩ, L=100pH.

In an effort to reduce the parasitics of the test circuit, it is necessary to place the resistor very near to the switching devices. The fields generated as a result of the switching action will induce errors in the voltage read from the resistor. Large values of resistance could be used to increase signal to noise ratio, but then the insertion impedance is large.

To analyze the ability of the measurement system to faithfully represent the current, the measurement bandwidth should be specified. This information is not readily available for surface mount resistors. For the many reasons listed, surface mount resistors are not used for the switch current measurement.

2.6.4 Coaxial Shunts

Coaxial shunts have many advantages over surface mount resistors. Refer to Figure 2.12, which shows the structure of a typical coaxial shunt. The current flowing in the shunt should not produce significant levels of magnetic flux in the region where the sense wires are placed. Therefore, the sense wires are not inductively coupled to the shunt current, and the output voltage does not contain any inductive component [26]. The outer shell provides shielding from the external fields generated by the switching action. Protection from the external noise sources and the internal fields of the current traveling through the resistive elements should yield an accurate measurement even for small output voltages and fast transitions.

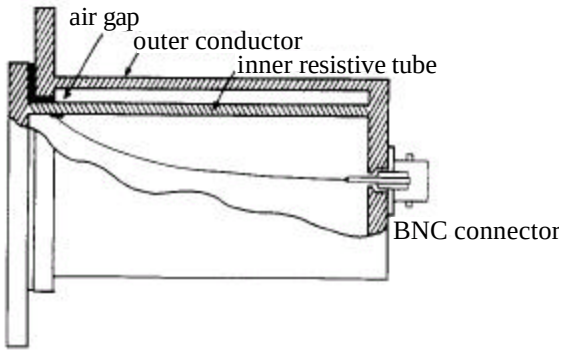

Figure 2.12. Structure of a typical coaxial shunt (drawing obtained from [26]).

The primary limitation to the shunt bandwidth is then the skin effect of the resistive material and the distributed capacitance of the structure [26]. The manufacturer provides

the bandwidth specification of the shunt. Knowing this specification, we can determine the limitation of the measurement system to accurately represent the fast current transients. We do not have the ability to make this specification when using surface mount resistors. Coaxial shunts can measure DC currents and have significantly higher bandwidths than Rogowski coils or CTs. For all of these reasons, the switch current should be measured using a coaxial shunt. The device *originally* chosen was the T&M Research A-2-01 current viewing shunt. This is a 10 mΩ shunt with a bandwidth of 400 MHz and rise time specification of 1 ns [27].

Thus far, we have discussed the basic principles behind the coaxial shunt, but this does not paint the whole picture. In truth, the coaxial shunt will have some amount of inductance due to the magnetic fields in the air gap (refer to Figure 2.12). Through matching of simulation and experimental waveforms, it is found that the inductance of the 10 mΩ shunt is approximately 100 pH. Figure 2.11 shown above gives the simulated current waveforms where the current is measured using a 10 mΩ resistor (actual current) versus a 10 mΩ resistor in series with a 100 pH inductor (measured current). Because of the parasitic inductance, the measured current experiences a much greater amplitude peak as well as a phase lead. If the resistance is increased to 100 mΩ, the resulting measurement is significantly improved, as shown in Figure 2.13.

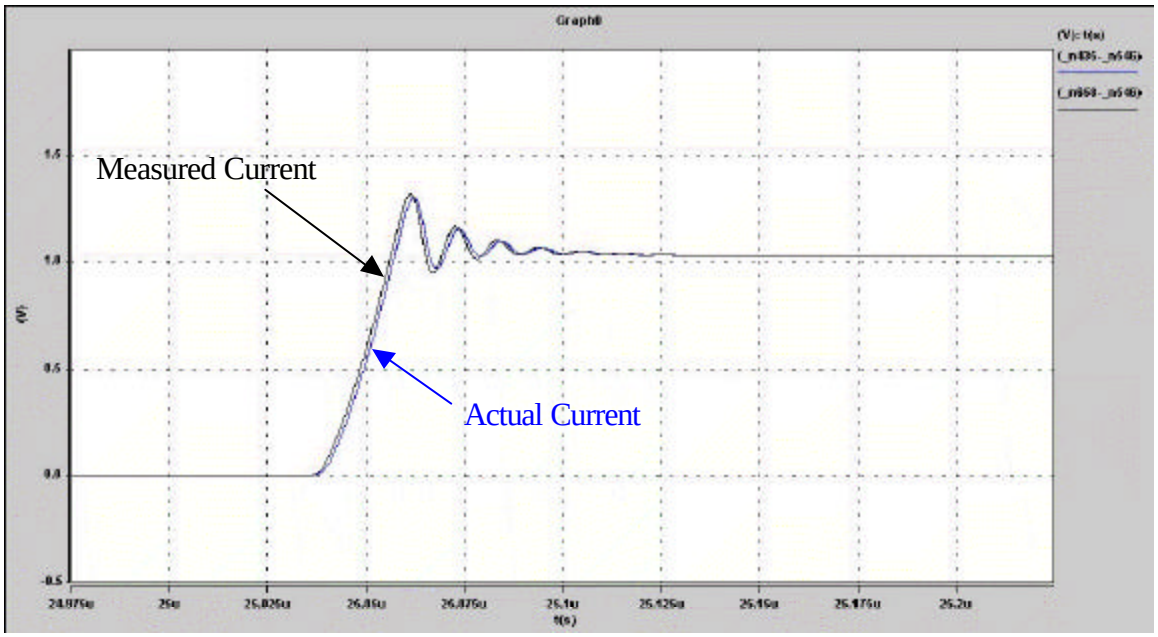

Figure 2.13. Actual current versus current measured with R=100mΩ, L=100pH.

What is learned from this exercise is that the shunt must satisfy not only bandwidth considerations due to skin effects, but also its resistance-to-inductance ratio (R/L) should be sufficiently high. Calculation of the necessary R/L ratio can be done in much the same way as a bandwidth calculation. If the shunt is modeled as a series resistance and inductance, its impedance will be resistive up to a corner frequency given by:

$$f = \frac{1}{2p}\frac{R}{L} \tag{2.4}$$

For the shunt with resistance of 10 mΩ and inductance of 100pH, the corner frequency is approximately 16 MHz. One should then question why the bandwidth is specified as 400 MHz when significant error is observed before 16 MHz. The reason lies in how the bandwidth is tested.

Determination of the bandwidth is done using a step current source and measuring the voltage output rise time [26]. A typical measurement may appear like Figure 2.14. Because current cannot change instantaneously in the series parasitic inductance, it must find some other path at the beginning of the step. In addition, if the shunt is modeled simply as a series R and L, the output voltage should lead the input current rising edge as in Figure 2.13 above. T&M Measurement uses a test pulse with di/dt in excess of 10^{12} A/s [28]. This translates, using Equation 2.2, to an equivalent frequency greater than 100 GHz. At this level of frequency, the series AC resistance (skin effect) and stray capacitances of the shunt begin to have a much greater effect than the parasitic inductance. The capacitance provides the necessary path for the current at the beginning of the step and gives the reasoning why the output voltage lags behind the rising edge of the input current. Under these conditions, the step response, and therefore the bandwidth specification, depends heavily on the capacitances of the structure and not on the inductance. In other words, the characterization will ignore the effect of the inductance.

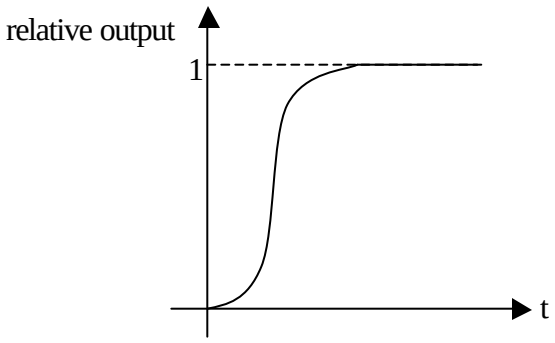

Figure 2.14. Typical Step Response for a Coaxial Shunt.

The current rise times for the IPEMs tested will yield equivalent frequencies in the range of tens of megahertz. In this range, the inductance will have a significant effect. For device testing purposes, the R/L corner frequency yields the most useful information in determining if the shunt voltage will faithfully represent the device current.

We normally determine system bandwidth from the sensor bandwidth and the oscilloscope bandwidth using Equation 2.3. This equation makes the assumption that the two cascaded tools (sensor and scope) are both first order low pass systems. The two systems would then together give a response that is less accurate than either individually. The worst case value (lowest bandwidth) then is to find the combined response. The assumption made in Equation 2.3 does not apply to the current shunt measurement. In fact, the phase lead from the shunt could partially offset the phase lag from the oscilloscope. When determining current measurement system performance, the worst case is to say that the system bandwidth is either the bandwidth of the oscilloscope or the R/L corner frequency of the shunt, whichever is lower.

To alleviate the problem a shunt with higher resistance and a lower inductance construction was utilized (SDN-10 from T&M Research). The SDN-10 is a 100 m? shunt with a 2 GHz bandwidth specification. The current measurement system bandwidth is limited by the oscilloscope to 500 MHz. Confidence that the current measurement is correct is be gained by making a simple observation. The current overshoot during turn-on is caused by the reverse recovery of the free-wheeling diode (D_1 in Fig. 1.2). The area under overshoot hump should be equal to the diode reverse recovery charge. If this equality holds true, then the current measurement is trustworthy.

Chapter 3 – Parametric Study Circuit

3.1 Introduction

A parametric study is carried out to determine the sensitivity of the switching characteristics of the device-under-test to several circuit parameters. The switching characteristics tester must be designed very carefully for parameters that have a significant effect on the switching characteristics. For example, suppose that it is known that some improvement in performance can be gained by reducing the parasitic inductance in the module. The first module has 20 nH of parasitic inductance and the second has 10 nH. If the tester has 1uH of parasitic inductance, overwhelming that of the modules, it will be impossible to observe the performance gain. For parameters that do not have a large impact on the switching characteristics, the tester can be designed in whatever way is convenient for its use. For example, if the parasitic inductance had no effect, we could make the connection to the module in a convenient way with no regard to the connection parasitics.

In most cases, there is a fundamental trade-off between good layout design and convenience of use. For instance, the parasitic inductance may be increased in the effort to make the connection to the module flexible. As these sacrifices are made, it becomes important to decouple what are the effects of the module tested and what are the effects of the test equipment. Suppose again that we are testing the modules with 20 nH and 10 nH parasitic inductances. If the tester has 30 nH, then the total change in inductance is only 20% while the change in module inductance is 50%. It is important to realize this change in sensitivity when analyzing a module's performance. It is only through this decoupling that we can fairly analyze the advantages and disadvantages among power devices and modules.

For each module tested, a datasheet will be generated. One of the goals of this parametric study is to determine under what operating conditions the tests should be performed. For instance, at what percentage of the rated voltage and current should the device be tested? How fast should the device be switched?

This parametric study also pushes the measurement equipment to its limits in terms of faithfully representing the switching characteristics. In doing so, we can determine what are the minimum specifications (bandwidth, rise time, etc.) that are necessary and what are its ultimate limitations.

In short, the parametric study allows us to decide on the necessary layout compromises, decouple the effects of the tester, determine the operating conditions, and analyze the quality of the measurement. The next few sections describe the basic tester circuit, parameter definitions, measurement procedures, and layout and component choice considerations. A simulation model is developed and simulation results are provided. Chapter 4 reveals and analyzes the parametric study results.

3.2 Basic tester circuit

The circuit used for the parametric study is a boost converter with clamped inductive load. A simplified circuit diagram is shown below in Figure 3.1. The MOSFET (S_1) chosen for the experiment is a 26 A, 500 V power MOSFET (IXYS part number IXFH26N50) [29]. This device is chosen because it has the same die as the one used in the Gen. II IPEM (Figure 1.1). Reverse recovery of the freewheeling diode (D_1) alters the MOSFET turn-on switching interval characteristics. Long reverse recovery times would limit how fast the device could be switched. Switching faster than these limitations would lead to excessive current and voltage spikes that could damage the device [10]. To minimize these effects, the diode is chosen to be a 12 A, 600V SiC Schottky diode (Infineon part number D12S60) [30]. SiC Schottky diodes have relatively low reverse recovery charge and time, allowing faster switching of the DUT [15].

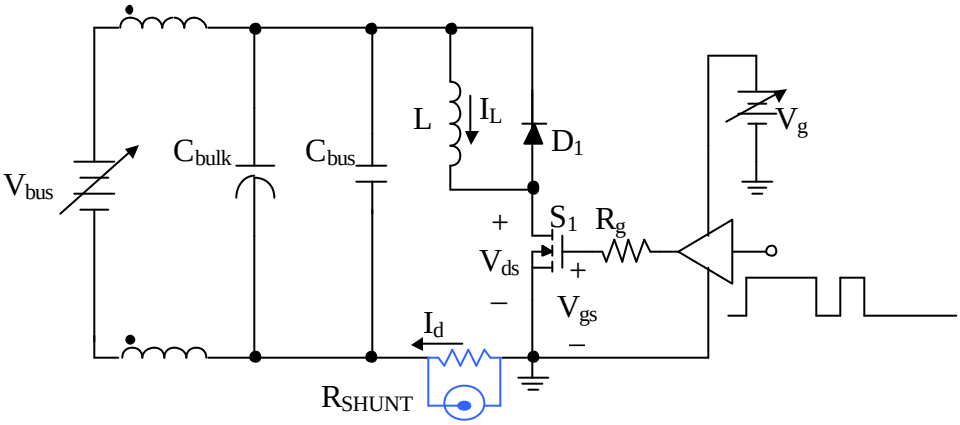

Figure 3.1. Parametric Study Test Circuit.

Circuit operation is controlled using a programmable signal generator to provide a double-pulse signal to the gate driver. Figure 3.2 shows the waveforms for the gate voltage (V_{gs}), drain voltage (V_{ds}), and drain current (I_d) under double-pulse operation. At time t_0, the device is turned on, and the switch is held on until I_D reaches the desired current level. At time t_1, the gate is forced low, and the turn-off switching characteristics of the DUT are recorded. From t_1 to t_2, the device is held off, and the inductor current freewheels through the diode. This freewheeling time should be long enough that any ringing in the drain voltage and current has subsided before the MOSFET is turned back on. It should also be short enough that the inductor current does not drop appreciably. At time t_2, the device is turned back on. The turn-on characteristics are then captured under very similar conditions as the turn-off case. The time from t_2 to t_3 should be long enough that any ringing has subsided and short enough that the drain current does not rise above device limitations. At time t_3, the device is turned off and held off for 50 ms. Keeping the duty cycle small ensures that the switching characteristics can be tested without heating the DUT.

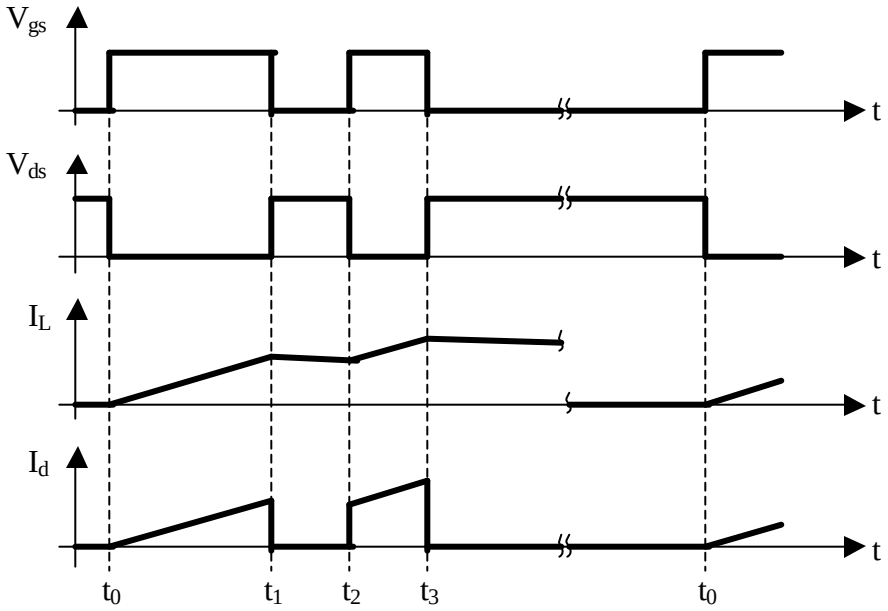

Figure 3.2. Double-pulse Waveforms.

3.3 Parameters

The following sections describe the parameters that are varied in the parametric study. Each section provides its respective parameter's definition and importance, along with the methods used to vary and measure the parameter. Also note that most of the parameter sections will refer back to Figure 3.1, which gives a simplified circuit diagram for the parametric study circuit.

3.3.1 Loop Inductance (L_{LOOP})

Loop inductance is the inductance of the loop formed by the bus capacitor (C_{bus}), diode (D_1), and MOSFET (S_1). Figure 3.3 shown below is essentially the same as Figure 3.1, with the exception that the parasitic inductances associated with the loop inductance are shown. Note from Figure 3.3 that the circuit outside of the loop has purposefully been faded and the inductors in **bold** are the parasitics that make up L_{LOOP}. Loop inductance is a critical layout consideration that is known to have implications on the voltage stress and current switching times of the device [8,9]. Study of this parameter is

intended to quantify these effects, as well as to determine its effects on other switching characteristics.

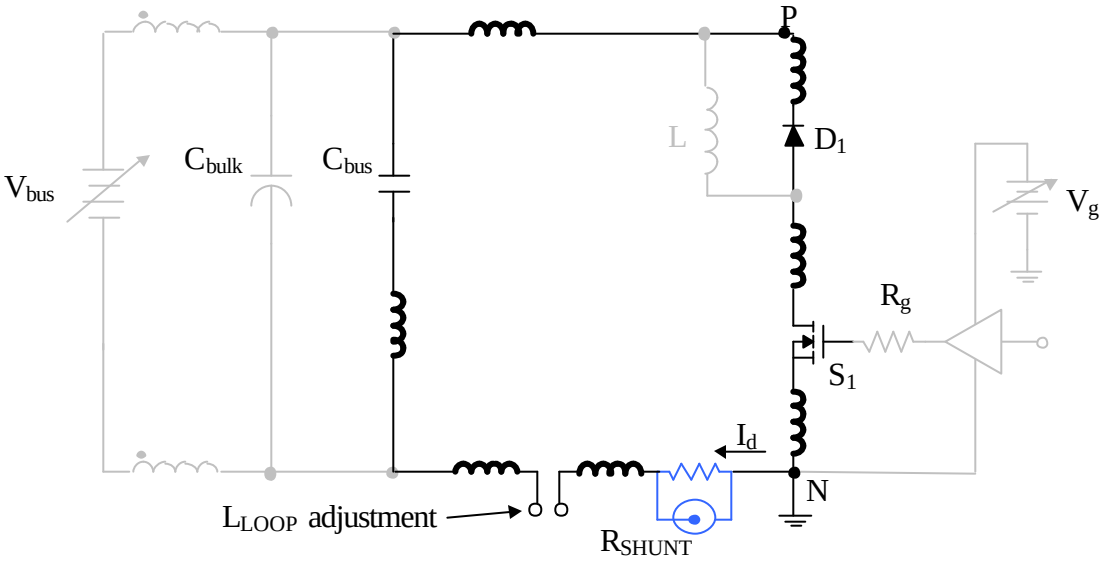

Figure 3.3. Test Circuit Showing Loop Inductance.

Since L_{LOOP} is to be varied from low values to relatively high values, its initial value must be very small and adjustable. Referring to Figure 3.3, note that there is a break in the loop labeled "L_{LOOP} adjustment." In the physical circuit, this break is connected using different lengths of wire to adjust the loop inductance.

To measure the loop inductance, the bulk electrolytic capacitor (C_{bulk}), load inductor (L), gate resistor (R_g), and the connection to the DC source (V_{bus}) must be removed. S_1 is off, and neither S_1 nor D_1 is shorted or has a bias voltage across them. The lead inductances of S_1, D_1 and R_{SHUNT} are included in the loop inductance measurement. The impedance is measured across the break in the loop using an impedance analyzer. The magnitude and phase data is exported as a text file and then recreated in Matlab. An equivalent R-L-C circuit model is created in Matlab, and the model's magnitude and phase are plotted on the same graphs with the measured data for comparison. Figure 3.4 shows the measured and simulated magnitude plots, and Figure 3.5 shows the phase plots. Both figures also show the equivalent circuit model simulated. The 550 pF capacitance is the series combination of C_{bus}, the diode capacitance and the MOSFET capacitances. The resistance of the loop is the dominant impedance near the resonant

frequency, so the 0.56 O is the resistance at that frequency (about 30 MHz). The inductance of 42 nH is the initial loop inductance with no wire inductance added for adjustment. Special care has been taken to minimize L_{LOOP}. As the loop was made quite small, 42 nH is not a surprising result.

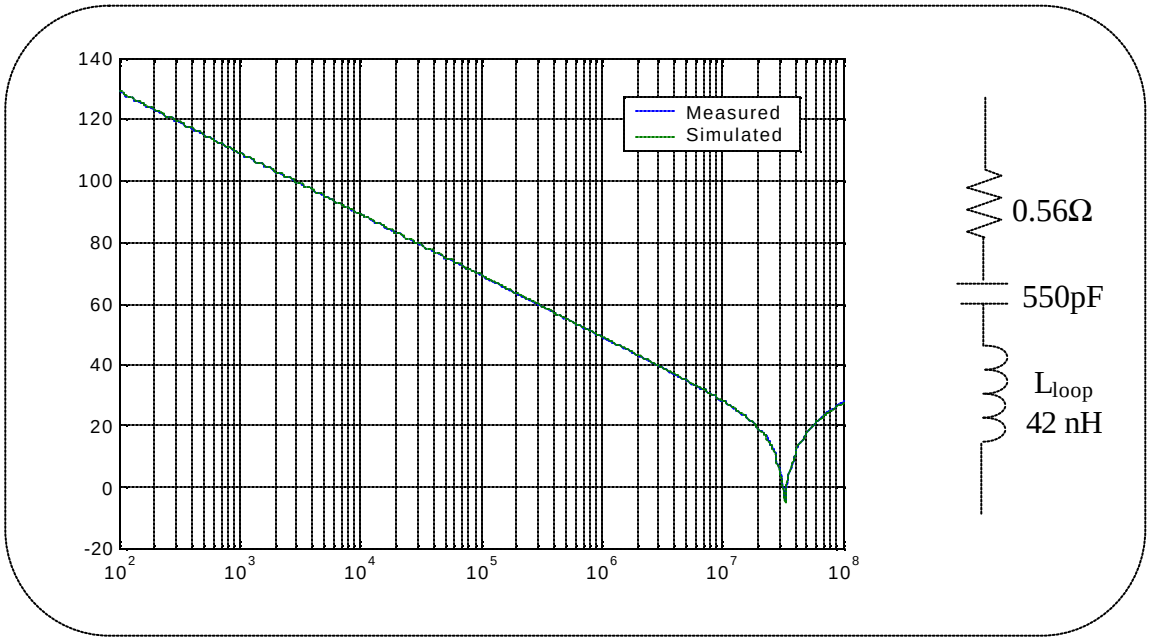

Figure 3.4. Impedance magnitude plot for measuring loop inductance.

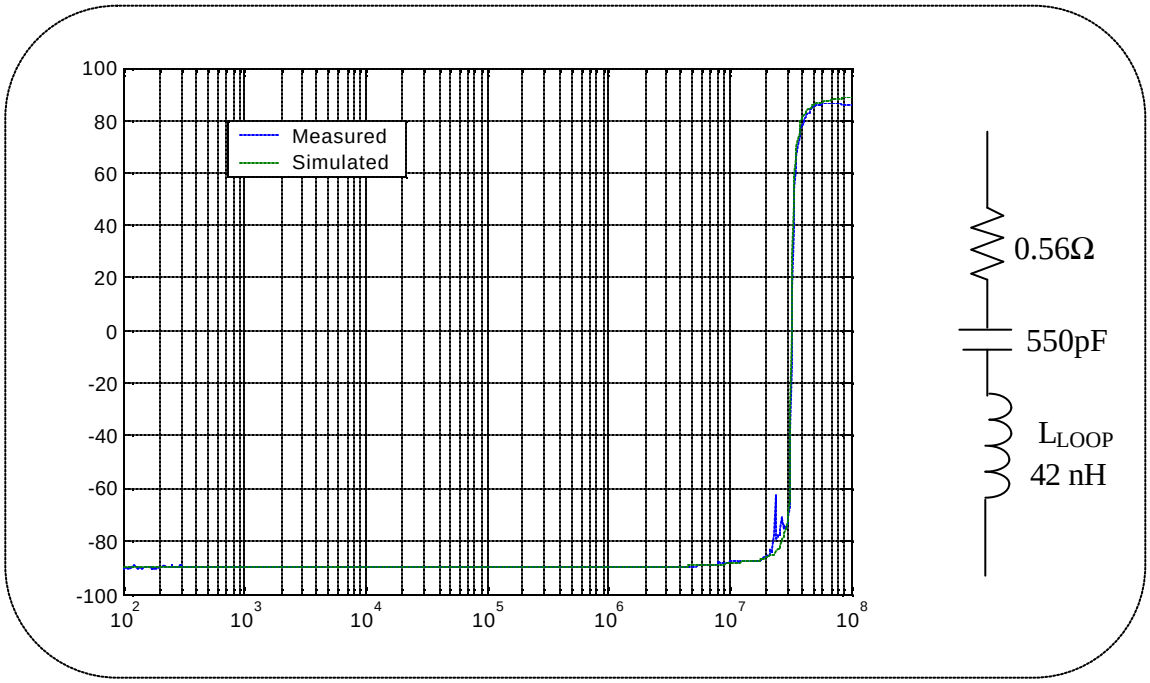

Figure 3.5. Impedance phase plot for measuring loop inductance.

3.3.2 Bus Capacitance (C_{bus})

The bus capacitance referred to here is that of the high frequency decoupling capacitors (C_{bus}) that are added across the DC bus near to the power devices (Figure 3.1). During switching transitions, V_{bus} and C_{bulk} will not be able to provide adequate energy quickly enough due to their high values of equivalent series resistances (ESR) and inductances (ESL). The result is large ringing of the voltage across P and N. Bus capacitors with low ESR and ESL are added to provide a low impedance path for the transient current. During transients, most of the current will flow in the loop described in the loop inductance section. In this way, C_{bus} decouples this loop from the rest of the circuit.

The effect of the bus capacitance on the switching characteristics is studied in an effort to learn how much capacitance should be used for the final tester. To perform the experiment properly, the C_{bus} should be adjusted without changing the loop inductance. However, C_{bus} has an ESL that contributes to the loop inductance. To minimize this effect, the bus capacitance is implemented with multiple single-layer (low ESL, ESR) ceramic capacitors varying in quantity from 6 to 18 capacitors. In doing so, a change from 18 capacitors to 6 results in only approximately 1 nH change in loop inductance (small enough to be neglected). This measurement was made by measuring L_{LOOP} under both conditions in the same manner as described in the loop inductance section.

3.3.3 Gate Resistance (R_g)

For this experiment, gate resistance refers to the external resistor added between the gate driver and the MOSFET gate pin (Figure 3.1). This parameter, among others, controls the switching speed of the DUT. For most tests, R_g is relatively large (30 Ω) to keep the switching speed slow. This way the experiment does not push the limits of the measurement equipment bandwidth. When varying R_g, the switching speed is pushed in order to test the trustworthiness of the measurement equipment. The trustworthiness is evaluated based on comparison to simulation results, as well as some fundamental observations that can be made.

3.3.4 Gate Voltage (V_g)

The gate voltage parameter refers to the value of V_{gs} when the device is fully on. V_g is controlled by a variable voltage supply that powers the gate driver (Figure 3.1). Gate voltage, among other parameters, controls the switching speed of the DUT. The primary reason for its testing is to gain an understanding of and quantify the advantages or disadvantages of lower or higher gate voltage in terms of switching characteristics. This study helps in choosing suitable gate voltage values for the final tester.

3.3.5 Drain Current (I_D)

The drain current is the current that flows into the drain pin of the MOSFET. However, it is measured along the DC link negative terminal (Figure 3.1). Note that the current in this path is indeed the same as the drain current. The measurement is made here so that the shunt would share a common point with the voltage probes for grounding purposes. The effects of I_d on the switching characteristics are studied in order to determine how the switching characteristics depend on device current and over what range of currents the device characterization should be done.

3.3.6 Bus Voltage (V_{bus})

The bus voltage is adjusted using a high voltage power supply, and it is measured as the steady state drain voltage after the device has been turned off. Like the drain current, V_{bus} is adjusted to determine what range of voltages will be useful in characterizing a power device. If the switching characteristics are very sensitive to bus voltage, the final characterization procedure may require the user to test the device at several voltage values.

3.3.7 Junction Temperature (T_j)

The junction temperature is adjusted using a hot plate and measured using an infrared temperature gun (Raytek ST60). The junction temperature effects are studied to determine if an IPEM datasheet should include switching characteristics for more than just ambient temperature.

3.4 The Physical Circuit

When building the actual circuit, there are several key layout constraints to consider. Loop inductance must initially be made small. This implies that the connection between the MOSFET's drain pin and the cathode D_1 must be very short, and the shunt that measures I_d should add as little as possible to the loop inductance. The bus capacitors must be very close to the power MOSFET and diode, and the ESL of C_{bus} should be small. In fact, this ESL must be negligible compared to the rest of the loop inductance. In satisfying this constraint, the loop inductance and bus capacitance can be considered decoupled.

Figures 3.6 and 3.7 show pictures of the top and bottom of the circuit board used for the parametric study. Note that the diode's pins are very close to the bus capacitors and the MOSFET. Multiple capacitors (up to 18) are used to implement the bus capacitance, reducing the effect of the ESL of C_{bus} on the loop inductance. The connection paths between the capacitors will add to the effective total ESL, so the distance between adjacent capacitors must also be short. Note from the figures that the capacitors are clustered together as close as was possible. For both the power devices and the bus capacitors, the components utilize both sides of the circuit board to reduce interconnection lengths to a minimum.

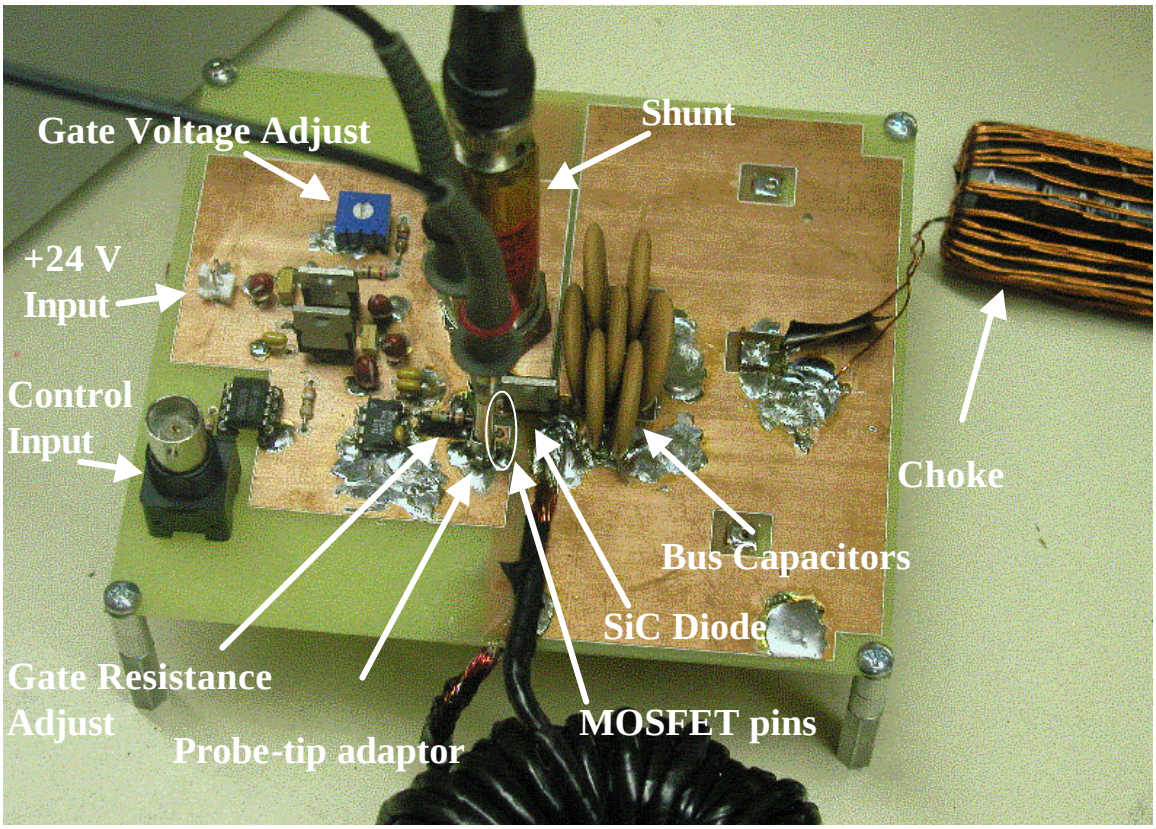

Figure 3.6. Top side of the circuit used for the parametric study.

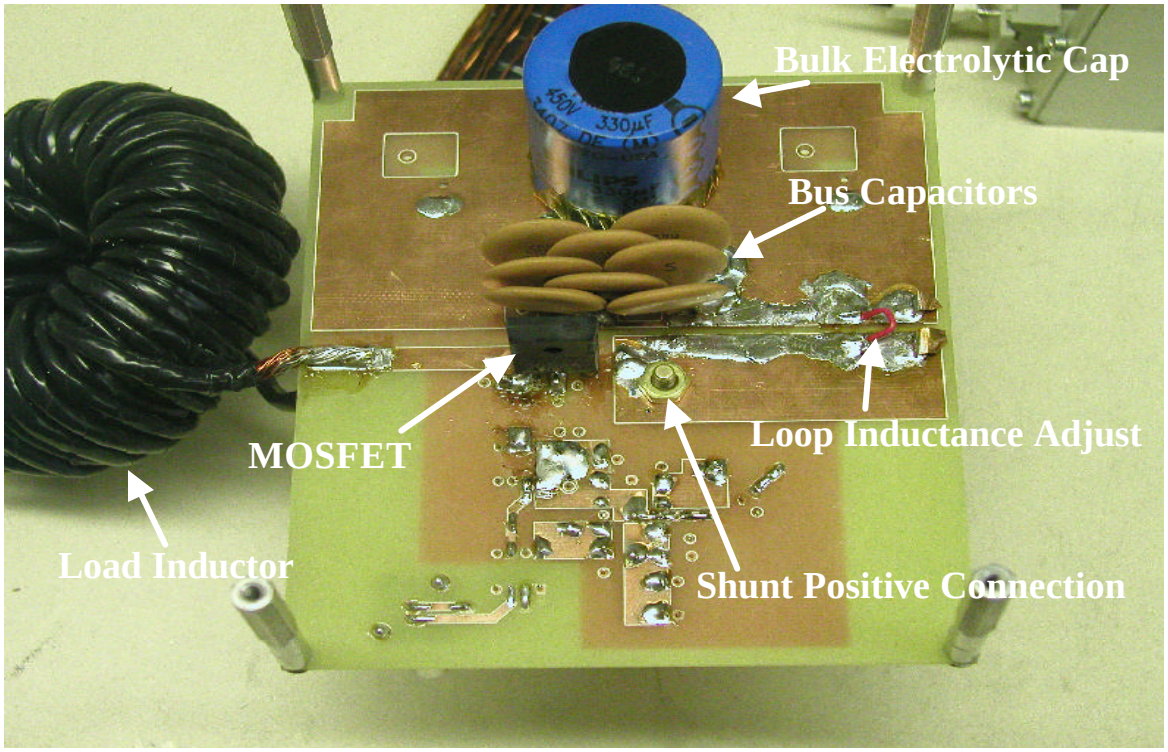

Figure 3.7. Bottom side of the circuit used for the parametric study.

Note that probe tip adaptors (see Chapter 2) are used for the gate and drain voltage measurements. Also, the ground connections for the shunt and the two voltage measurements were made as close as possible to reduce ground loop effects. The choke shown is necessary to break the capacitively coupled ground loop that results from the high voltage supply's capacitance to earth ground (see Chapter 2).

The +24V power supply voltage is brought onto the board to supply the variable output voltage regulator that is used to supply the gate driver. The gate voltage is controlled via the potentiometer labeled "Gate Voltage Adjust". The gate resistance is adjusted by plugging different values into the receptacle labeled "Gate Resistance Adjust". The control signal enters the board via a coaxial connection from a programmable signal generator and provides the means for varying the drain current (adjustment of the first pulse time).

3.5 Simulation Model

The figures provided in the previous sections are simplified in that they do not model many of the effects observed in measurement. In order to recreate the measurement results in simulation, we need to model each component and the connections between components. The modeling done here is based on matching of circuit impedance measurements and lumped parameter (discrete R, L, and C) models. Simulation of the transient behavior is carried out in Saber circuit simulation tool.

3.5.1 IXFH26N50 MOSFET Model

The model for the IXFH26N50 power MOSFET is provided in the Saber power MOSFET library. Ideally, a simulation model would duplicate every characteristic of the physical device. However, MOSFETs are complicated devices, and it would be impractical to try and model every detail. Because the model will only have a certain level of detail, it is important to determine if the characteristics that are important to a specific simulation are modeled correctly. For simulation of the switching characteristics, the primary concerns were that the following non-idealities might not be modeled sufficiently [8,31,32]:

1) dynamic capacitances of the MOSFET (C_{OSS}, C_{ISS}, and C_{RSS})
2) parasitic inductances of the pins (L_G, L_D, and L_S)

3.5.1.1 C_{OSS}, C_{ISS}, and C_{RSS}

The internal parasitic capacitances of a MOSFET are viewed as three device capacitances: C_{gs}, C_{gd} and C_{ds} (see Figure 3.8) [32]. For the common source configuration, the device capacitances are combined to reflect the capacitive reactance seen by the input (gate drive) and load. C_{OSS} is the effective output capacitance and is defined as: C_{ds} + C_{gd} with the gate pin shorted to the source. C_{ISS} is the effective input capacitance defined as: C_{gs} + C_{gd} with the drain-to-source "AC-shorted". AC-shorted means that there can be a DC source, but the drain-to-source must appear as a short circuit to an AC signal. This is usually accomplished using a suitable capacitor [17]. C_{RSS} is the reverse transfer capacitance and is equal to C_{gd}.

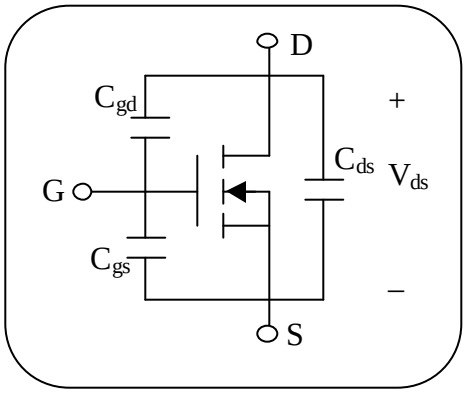

Figure 3.8. MOSFET Parasitic Capacitances.

The MOSFET parasitic capacitances are nonlinear in that their values change with drain-to-source voltage (V_{ds}). If these nonlinearities are not modeled, the resulting waveforms will yield misleading data. A series of AC sweep simulations can be performed to determine if the parameters listed above are modeled correctly. To test C_{OSS}, we must first short the gate and source pins and apply an AC source and DC bias across the drain and source pins (refer to Figure 3.9). An equivalent capacitance should be simultaneously simulated. The equivalent capacitance should be adjusted until it matches the capacitive portion of the impedance plot (impedance measured across the

drain and source). Figure 3.10 demonstrates this matching. A similar approach can be used to test C_{ISS} and C_{RSS}. For C_{ISS}, the AC source should be placed across the gate and source with a DC source across the drain and source (see Figure 3.11). The impedance is measured across the gate and source. C_{RSS} is determined through two steps. Figure 3.11 shows the circuit simulated in Saber. An AC source with DC bias is placed across the drain and source pins. The gate-to-drain is AC-shorted using an AC source with a magnitude of zero. Note that this source also has a DC bias with the same value as V_{ds}. This keeps the gate voltage at zero volts. The capacitance data from simulating this circuit is $C_x = C_{ds} + C_{gs}$. Using this data with that form C_{OSS} and C_{ISS} gives three equations ($C_{OSS} = C_{ds} + C_{gd}$, $C_{ISS} = C_{gs} + C_{gd}$, and $C_x = C_{ds} + C_{gs}$) with three unknowns (C_{ds}, C_{gs} and $C_{gd} = C_{RSS}$). For each V_{ds}, C_{RSS} is solved this way. Sweeping V_{ds}, the capacitance curves from the IXFH26N50 datasheet should be reproduced. Figures 3.12 and 3.13 show the datasheet curves and the curves extracted from simulation. Choosing a few values along each curve and comparing datasheet values to simulation model values, one can see that the capacitance trends of the IXFH26N50 were well modeled.

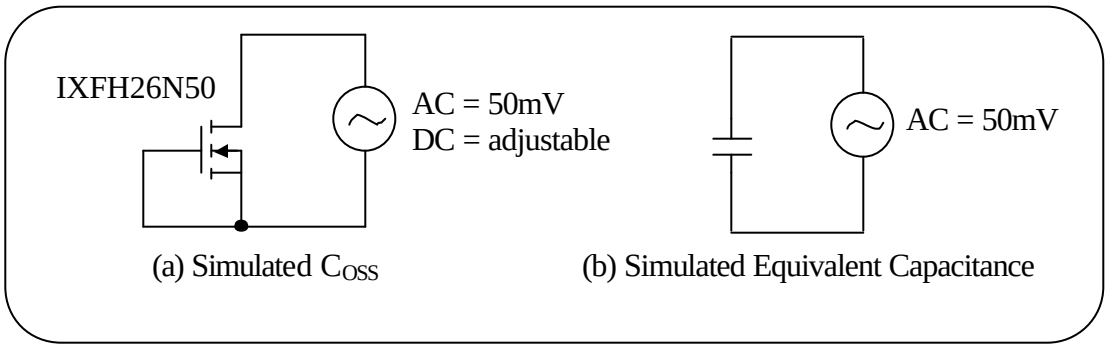

Figure 3.9. Simulation circuits to determine C_{OSS}.

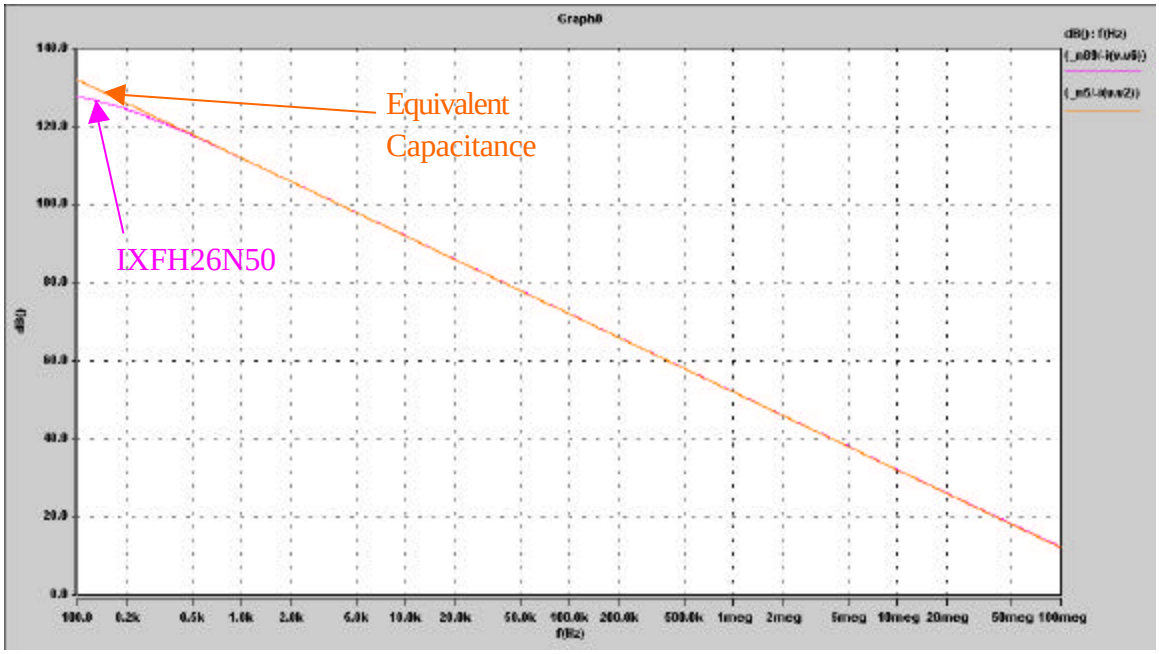

Figure 3.10. Impedance plots for the IXFH26N50 and the equivalent capacitance.

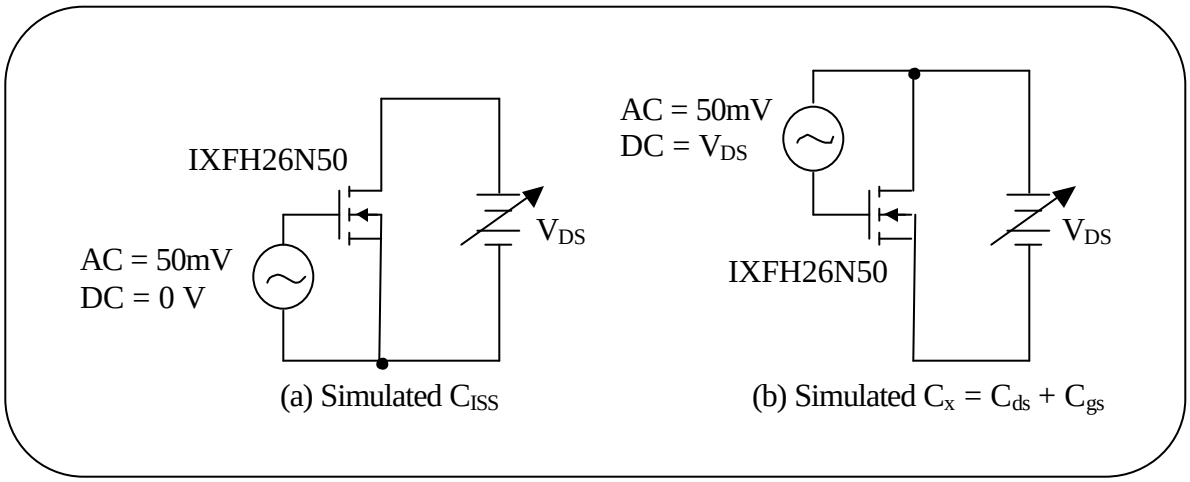

Figure 3.11. Circuits simulated to determine (a) C_{ISS} and (b) C_{RSS}.

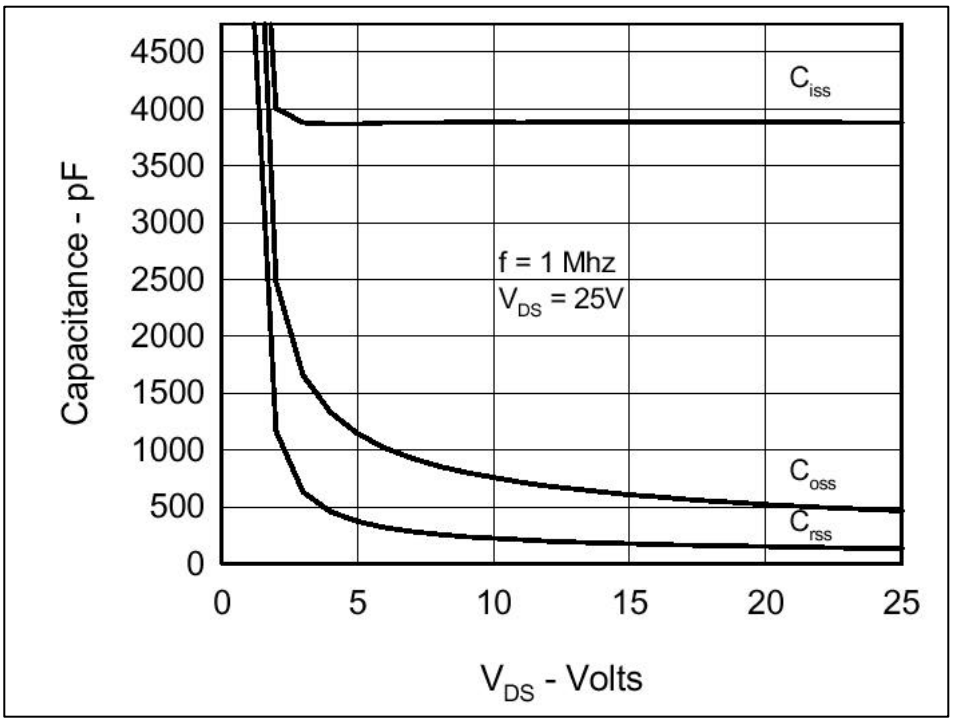

Figure 3.12. C_{OSS}, C_{ISS} and C_{RSS} curves from the IXFH26N50 datasheet.

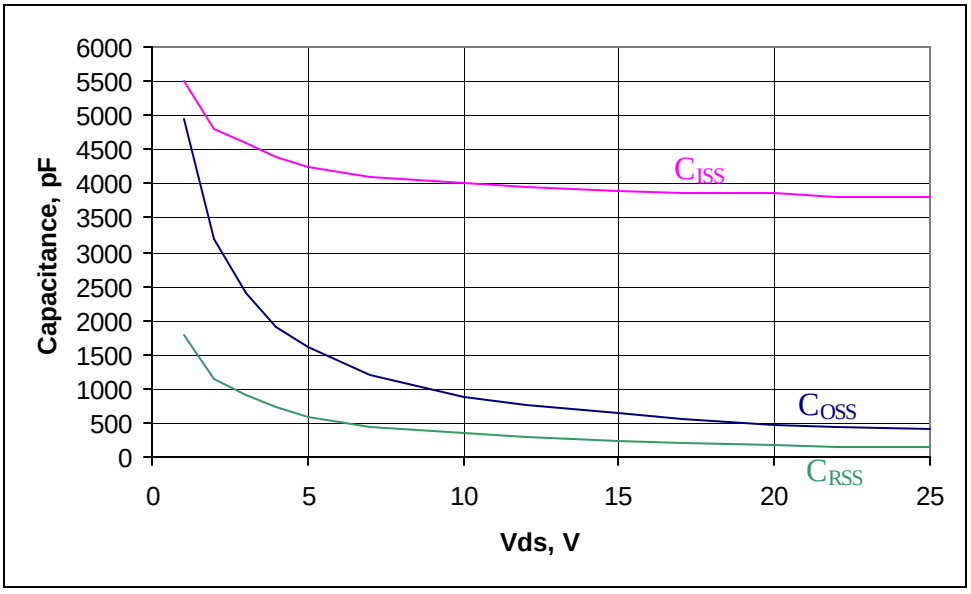

Figure 3.13. Simulated C_{OSS}, C_{ISS} and C_{RSS} curves.

3.5.1.2 L_G, L_D, and L_S

Note from Figure 3.10 above that there is no L-C resonance. This is because the pin inductances are not modeled. These values can be modeled by adding the appropriate inductors in series with the IXFH26N50 model in Saber. L_G, L_D, and L_S can be found by making three impedance measurements. In each case, the impedance is measured across two of the three pins of the MOSFET. The impedance analyzer (Agilent 4294A) has the ability to extract an equivalent R-L-C circuit for the impedance measured. The value of the inductance of the equivalent model is recorded. Measuring across the drain and source gives $L_D + L_S$. Measuring across the gate and source gives $L_G + L_S$. Measuring across the gate and drain gives $L_G + L_D$. Solving the three equations simultaneously yields L_G, L_D, and L_S. The final MOSFET model uses the Saber library model provided with the parasitic inductances added as shown in Figure 3.14.

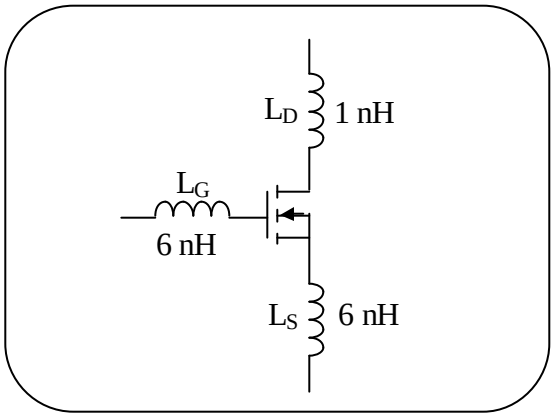

Figure 3.14. IXFH26N50 model including pin inductances.

3.5.2 D12S60 SiC Schottky Diode Model

Like the MOSFET model, it is important that the dynamic capacitance of the diode model is implemented correctly. Unfortunately, there is no commercially available model for the D12S60. However, there is a model available for the D06S60 diode, the 6A version from the same family of diodes. Figure 3.15 shows the junction capacitance of the D12S60 as a function of reverse voltage V_R from the device datasheet. Figure 3.16 shows the results of testing two D06S60 diodes in parallel in Saber. While the two plots

are not identical, they are close enough that the use of the parallel diode models should yield a similar transient response as the real diode.

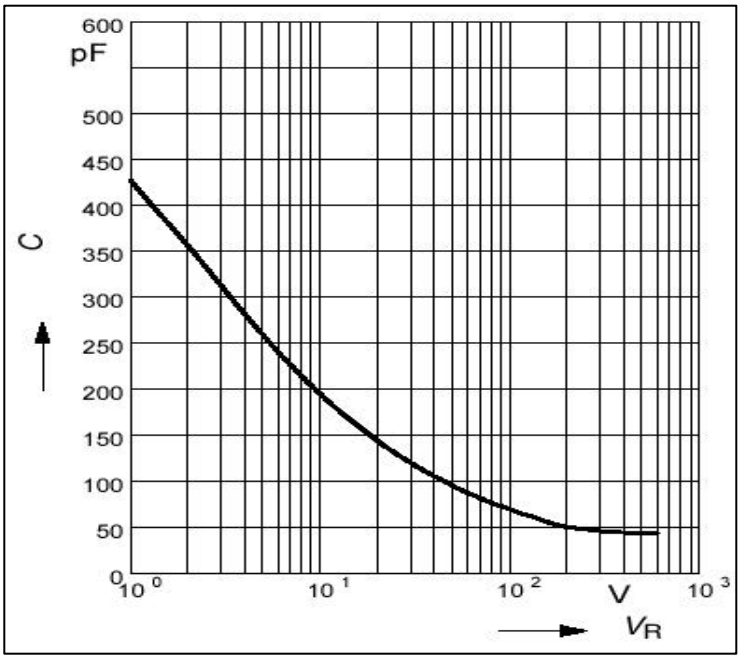

Figure 3.15. C(V) curve from the D12S60 SiC Schottky diode datasheet.

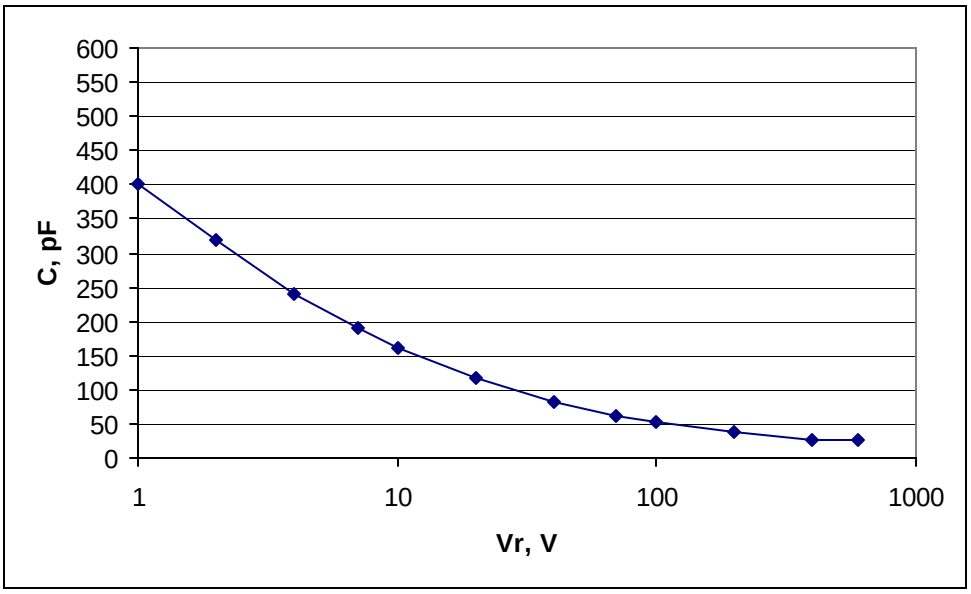

Figure 3.16. Simulated C(V) for two parallel D06S60 SiC Schottky diode models.

Figure 3.17 shows the simulated impedance plots of the two parallel diodes and of the equivalent R-L-C model (also given in the figure). Note that there is an L-C resonance in the plot, meaning that the pin inductance has already been modeled for the diodes. By

matching the equivalent R-L-C model to the diode impedance, the series parasitic inductance is found to be 6 nH. Physical measurement of the 12 A diode impedance reveals that it also has a series inductance of 6 nH, meaning that no series inductor needs to be added for the model.

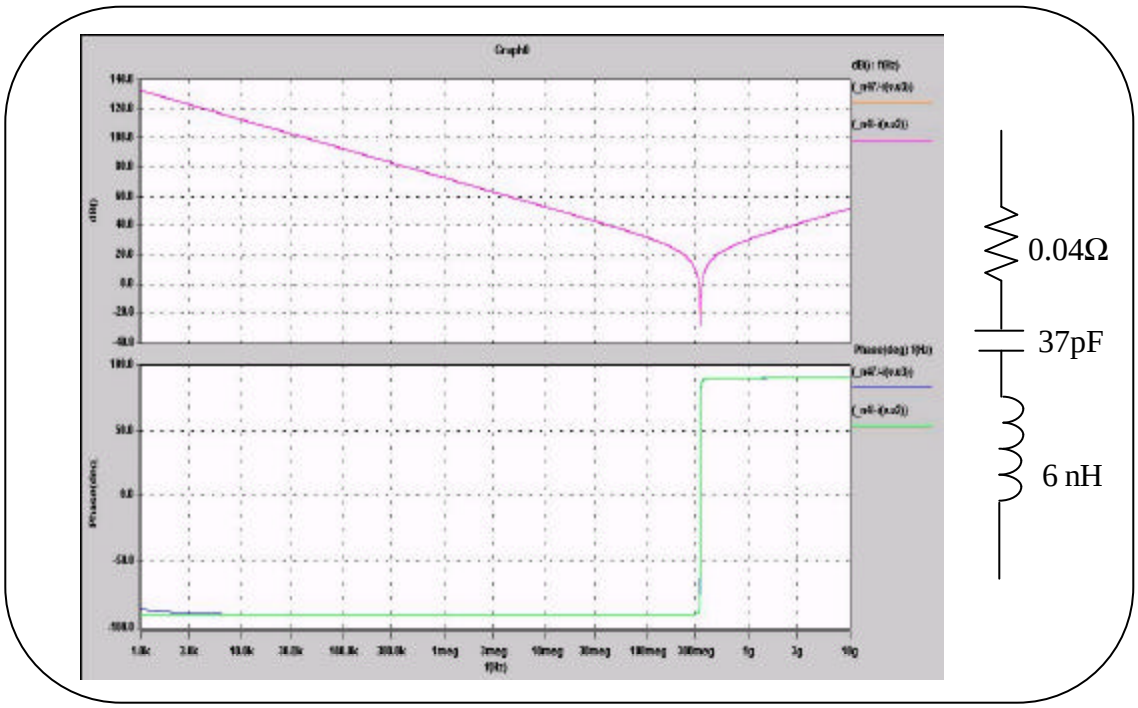

Figure 3.17. Simulated parallel D06S60 diodes and equivalent R-L-C circuit.

3.5.3 Load Inductor Model

Figures 3.18 and 3.19 show the magnitude and phase of the impedance measurement and simulated equivalent circuit for the load inductor. The model matches the measurement very well up to the first parallel resonance frequency. After that frequency, a transmission line effect can be observed. To model the multiple resonances would be impractical in that it would require many parts and simulation time could be increased. The model, shown in Figure 3.20, was kept simple by using a resistor in series with the parasitic capacitance to model the average impedance over the high frequency range.

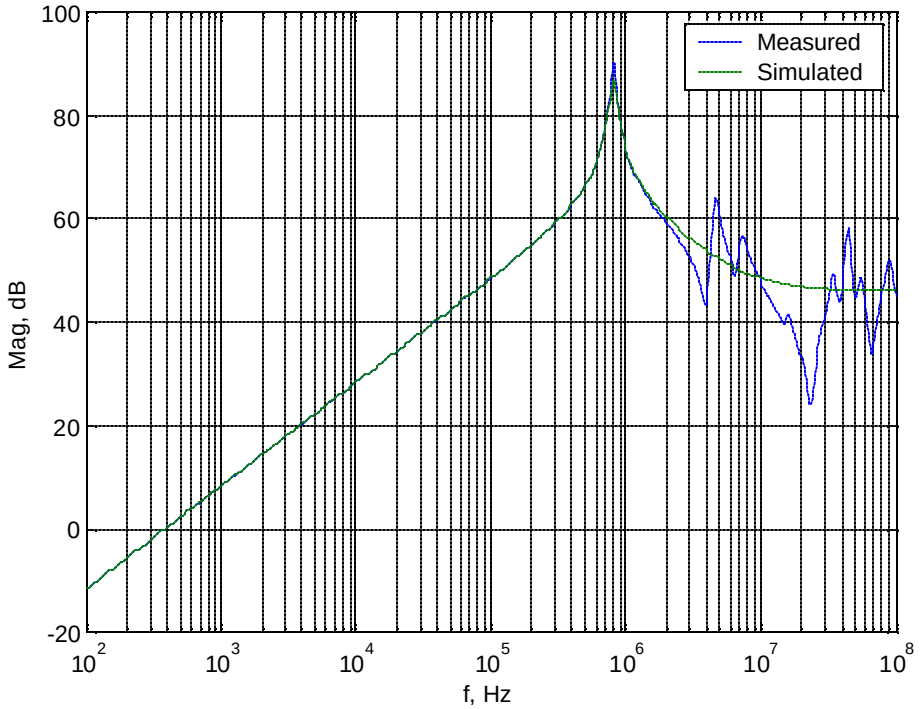

Figure 3.18. Magnitude plot for the load inductor impedance.

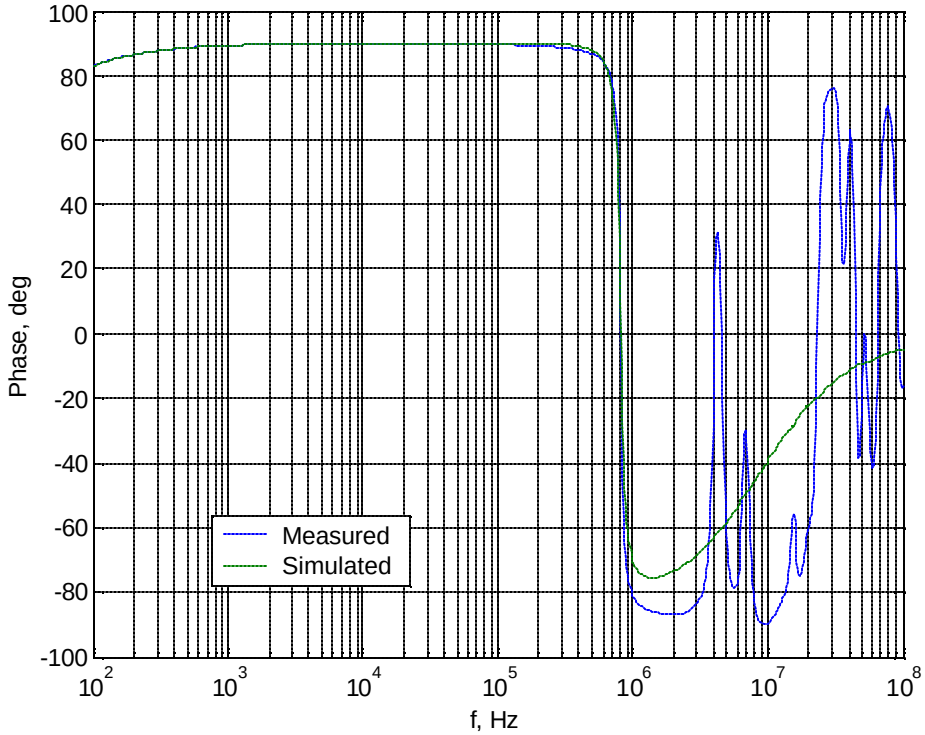

Figure 3.19. Phase plot for the load inductor impedance.

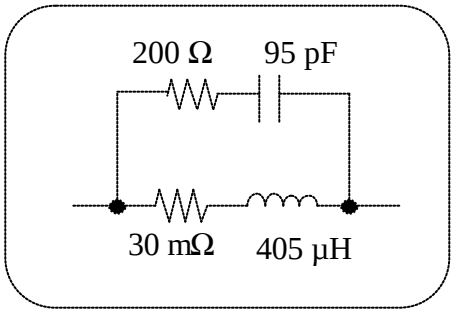

Figure 3.20. Model for the load inductor.

3.5.4 Bulk Capacitor Model

Figures 3.21 and 3.22 show the magnitude and phase of the impedance measurement and simulated equivalent circuit for the bulk electrolytic capacitor. Here, the additional resonance near 1 MHz is not modeled in order to keep the model simple.

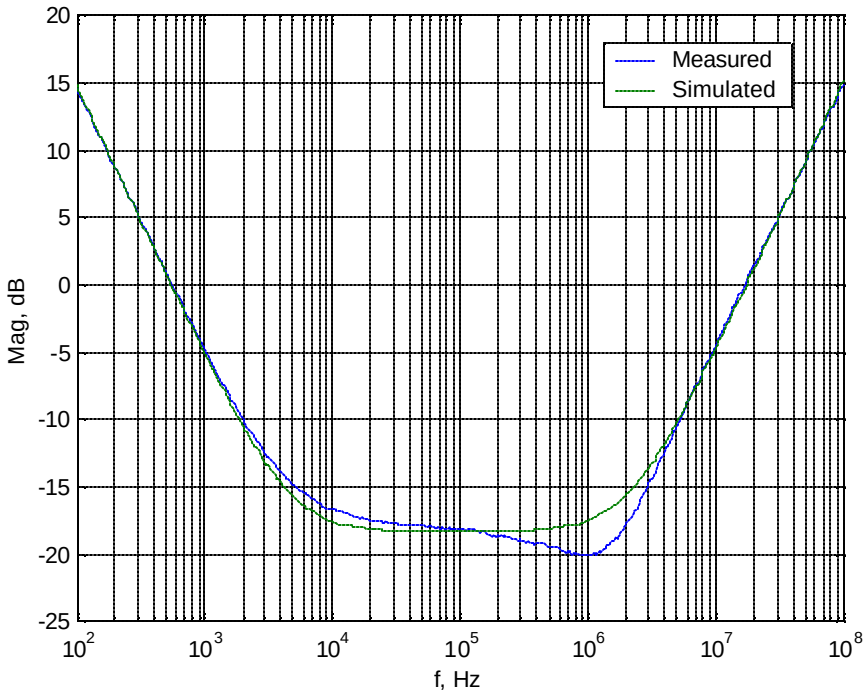

Figure 3.21. Magnitude plot for C_{bulk}.

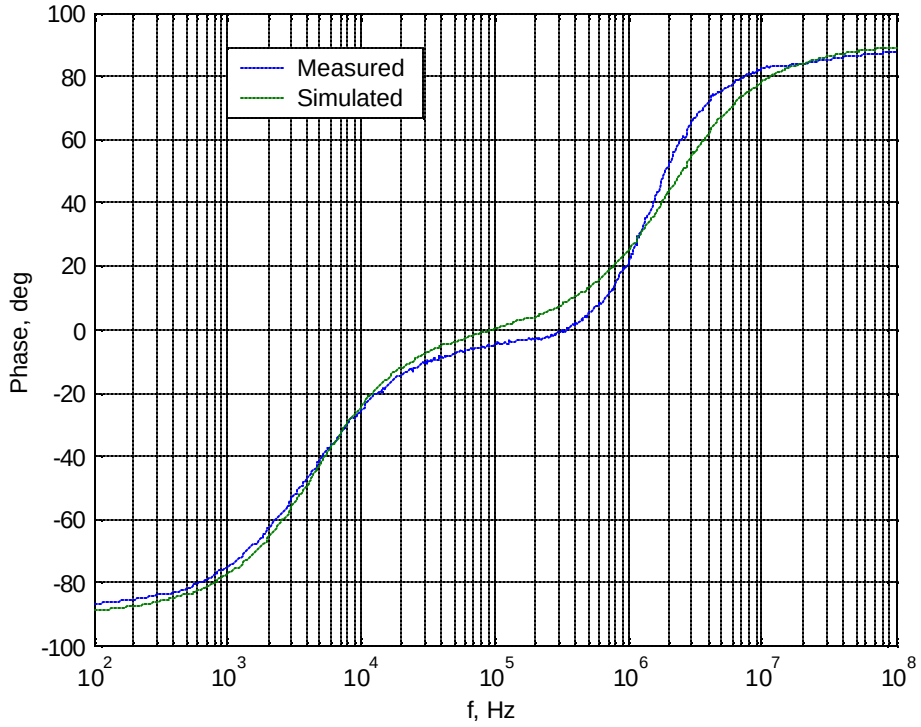

Figure 3.22. Phase plot for C_{bulk}.

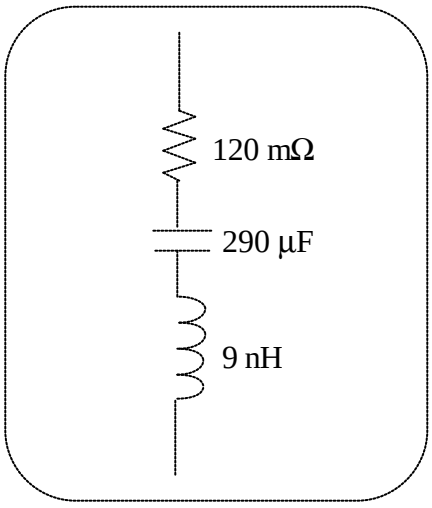

Figure 3.23. Model for C_{bulk}.

3.5.5 Bus Capacitance Model

Measurement of the parasitic ESR and ESL of the bus capacitance was challenging, because the C_{bus} is implemented with several capacitors, each with low values of ESR and ESL. Measuring each capacitor individually, it is found that they each have about 6

nH of ESL and about 40 mΩ of ESR. Theoretically, having 18 of these capacitors should give an inductance of 0.33 nH (6nH / 18) and an resistance of 2.2 mΩ (40mΩ / 18). Two problems exist with simply using these calculated values. First, at such low inductance values, the interconnections between capacitors become significant even for short connection paths. These interconnections must be accounted for. This means measuring the entire bus capacitor impedance at once, but obtaining consistent measurements for such low values of inductance and resistance is nearly impossible. More consistent results could be obtained by measuring the loop inductance (as described in 3.3.1). Changing the number of bus capacitors from 18 to 6, the change in inductance was 1 ± 0.3 nH. Note that when trying to measure such small differences, the tolerance is very loose (±30% in this case).

The second point that should be made is that the number of bus capacitors will be changed during the parametric study, but we do not want to have to change the value of the ESR and ESL every time we change the value of C_{bus} in simulation. If a change of 12 capacitors brings a change of 1 nH in ESL, then 18 capacitors (upper limit) should have about 0.7 nH and 6 capacitors (lower limit) should have about 2 nH. A midrange value of 1.3 nH is settled on for the bus capacitance ESL. The same reasoning is applied to the ESR, and a value of 8 mΩ is chosen. The final model is shown below in Figure 3.24.

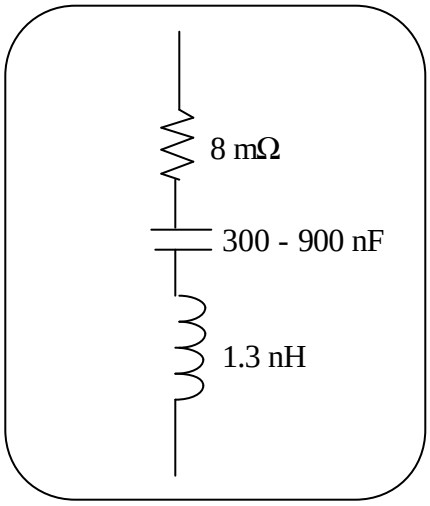

Figure 3.24. Model for C_{bus}.

3.5.6 Interconnection Models

Every time the resistance and inductance of an interconnection between two components is modeled, the impedance of a loop is measured. For example, to measure the interconnection between C_{bulk} and C_{bus}, the impedance of the loop shown below in Figure 3.25 is measured. C_{bulk}, the connection between V_{bus} and C_{bulk}, and the wire used for the loop inductance adjustment must be removed. The values of the ESR and ESL of C_{bus} are subtracted from the total resistance and inductance measured. By measuring the entire loop, we can get the impedance of both the top and bottom paths as well as automatically subtracting the mutual inductance. This same method is implemented for the connection between V_{bus} and C_{bulk}, the loop inductance path (see section 3.3.1), and the loop formed by the gate drive circuit and the MOSFET.

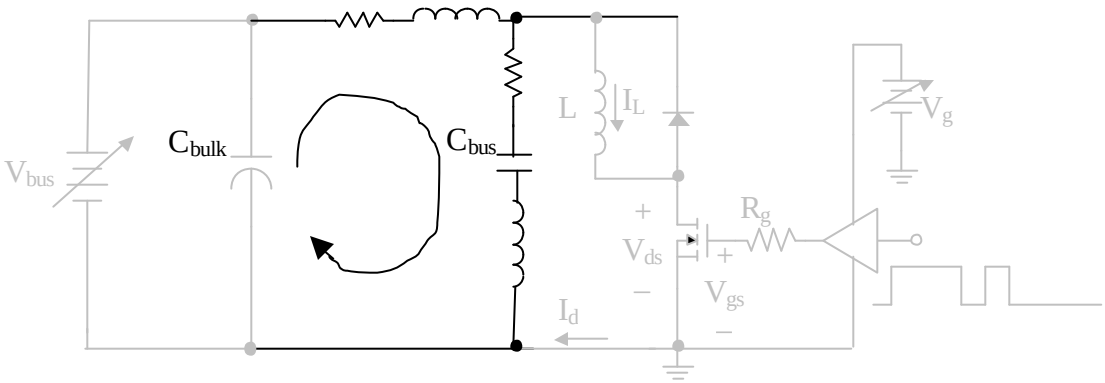

Figure 3.25. Loop measured to determine parasitics between C_{bulk} and C_{bus}.

The connection between V_{bus} and C_{bulk} contains the common-mode choke and has an impedance that is quite different from the other interconnection measurements. Figures 3.26 and 3.27 show the measured and simulated impedance plots, and Figure 3.28 gives the model used.

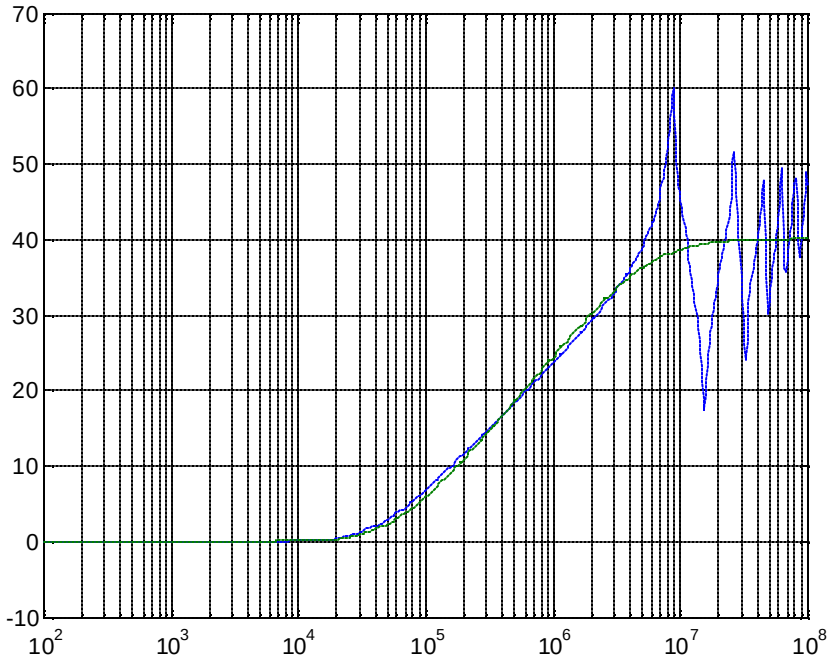

Figure 3.26. Magnitude plot for the connection between V_{bus} and C_{bulk}.

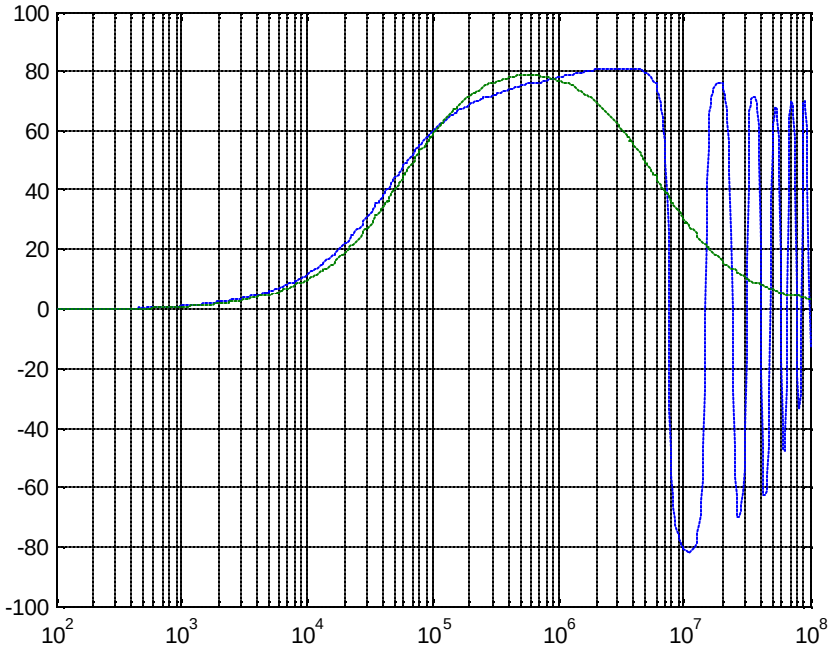

Figure 3.27. Phase plot for the connection between V_{bus} and C_{bulk}.

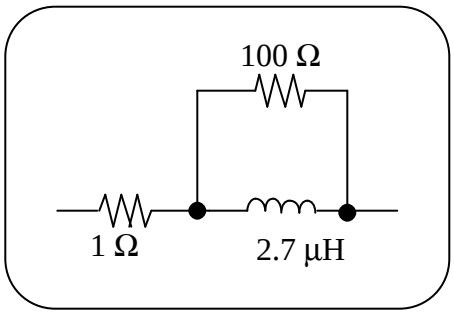

Figure 3.28. Model for the connection between V_{bus} and C_{bulk}.

3.6 Simulation Results

Figure 3.29 below shows the complete model used for simulation. Simulation has three primary purposes in this thesis work. One is to help with understanding and solving the measurement problems. For instance, the source of the problem with the common-mode ringing due to the capacitively coupled ground loop (section 2.4.1) was first identified by simulating this circuit with a capacitor added between the negative terminal of V_{bus} and earth ground. Suspicions that the errors in the current measurement with the 10 mΩ shunt were due to series inductance were confirmed using simulation. The second purpose is to verify that the trends in the measured waveforms and data are the expected ones. The third main purpose is to be able to simulate the waveforms that cannot be measured in the real circuit. The next few sections give sample simulations to demonstrate the second and third purposes described.

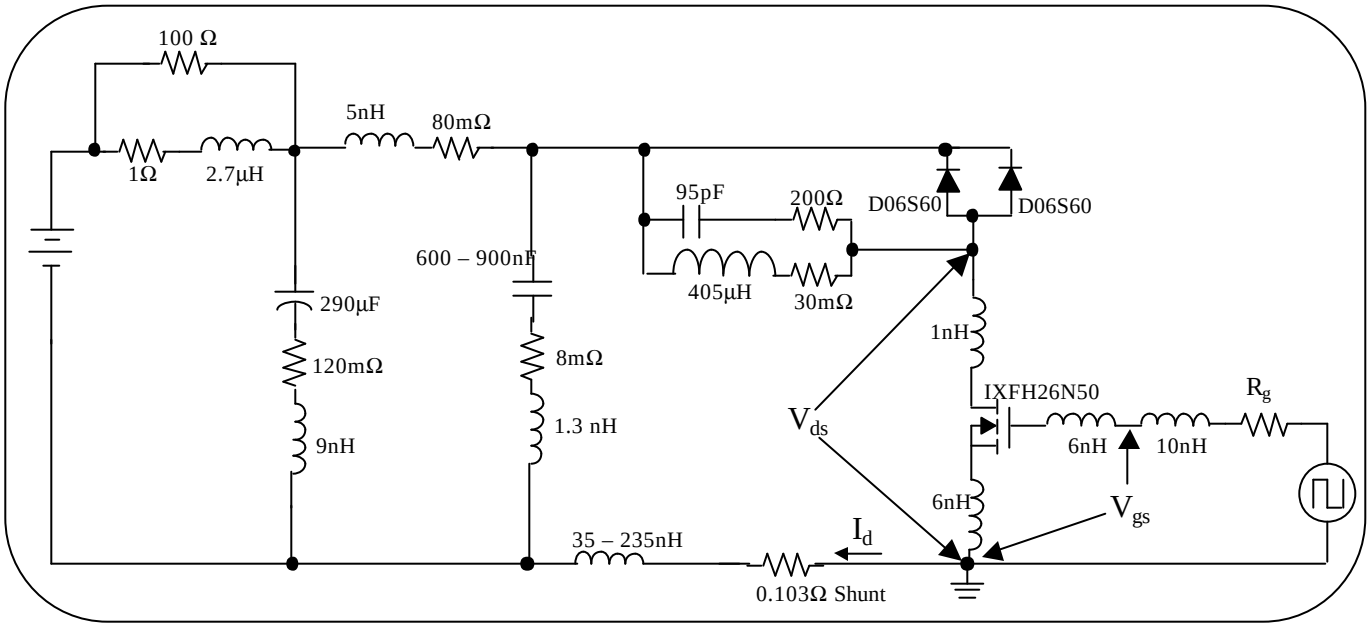

Figure 3.29. Complete simulation circuit model.

3.6.1 Change in Switching Waveforms with Varying Device Current

This simulation example shows the effect of varying device current (I_d) on the switching waveforms. Figures 3.30 through 3.32 show the measured and simulated waveforms for V_{ds}, V_{gs}, and I_d during the turn-off transition. From the figures, one can see that the trends for simulation are very similar to those of measurement.

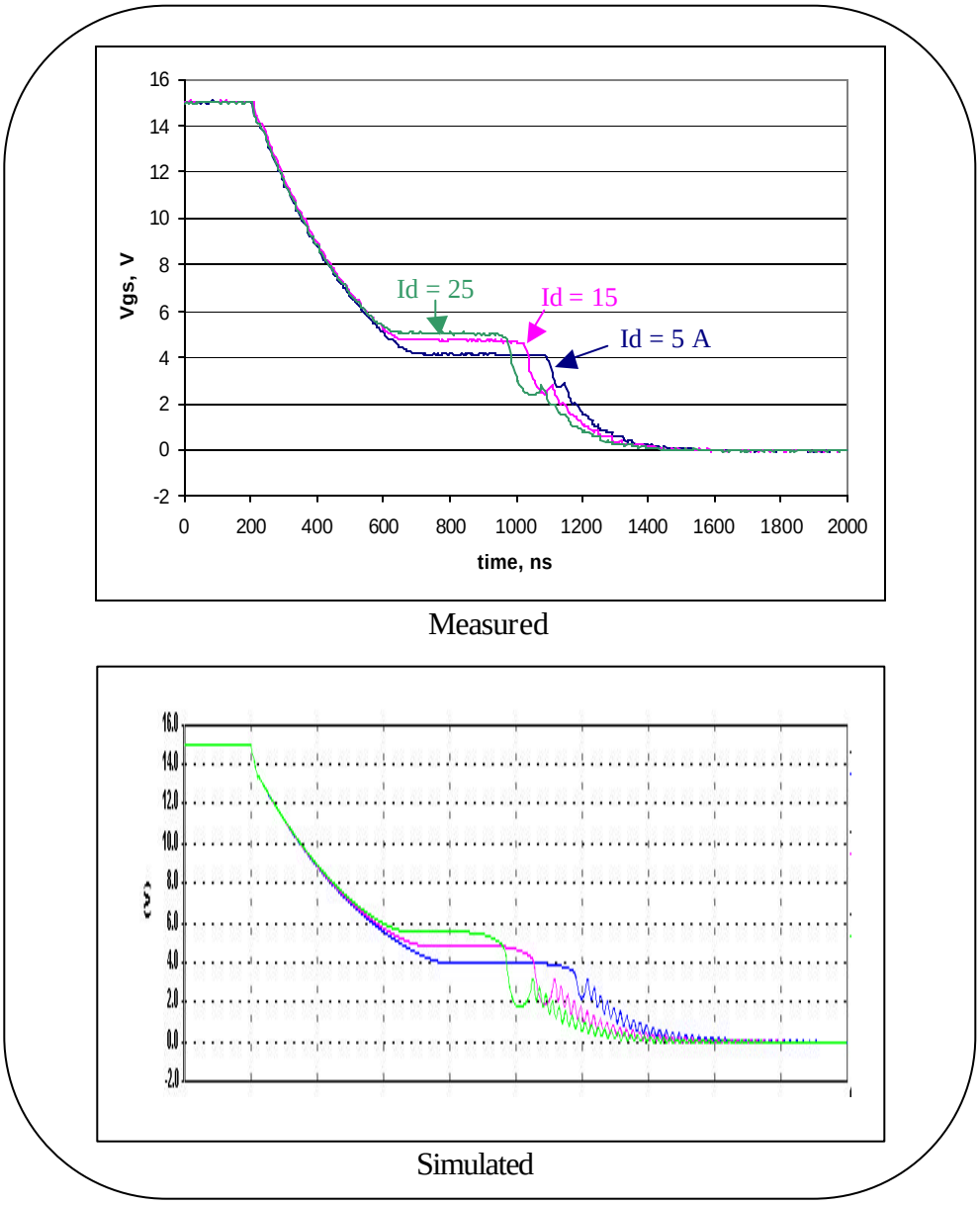

Figure 3.30. Comparison of V_{gs} for simulation and measurement.

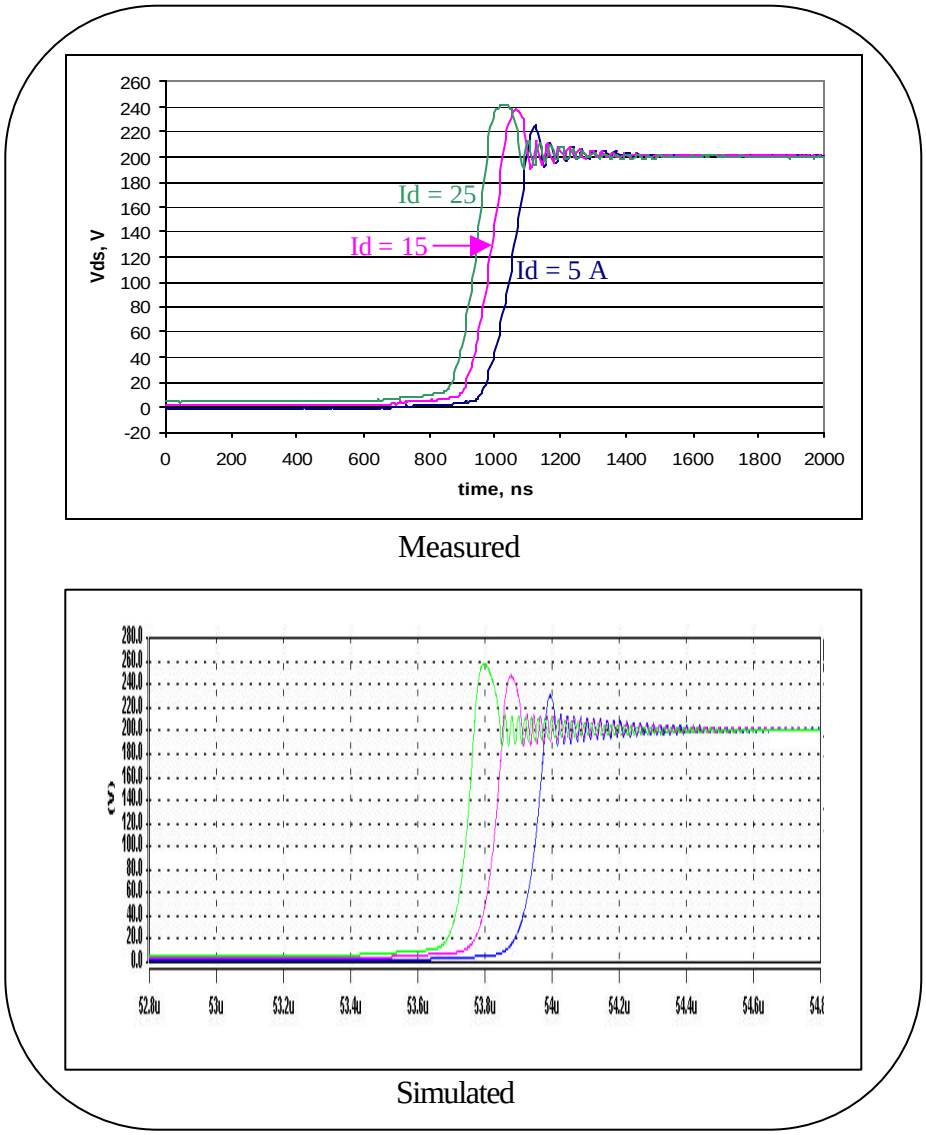

Figure 3.31. Comparison of V_{ds} for simulation and measurement.

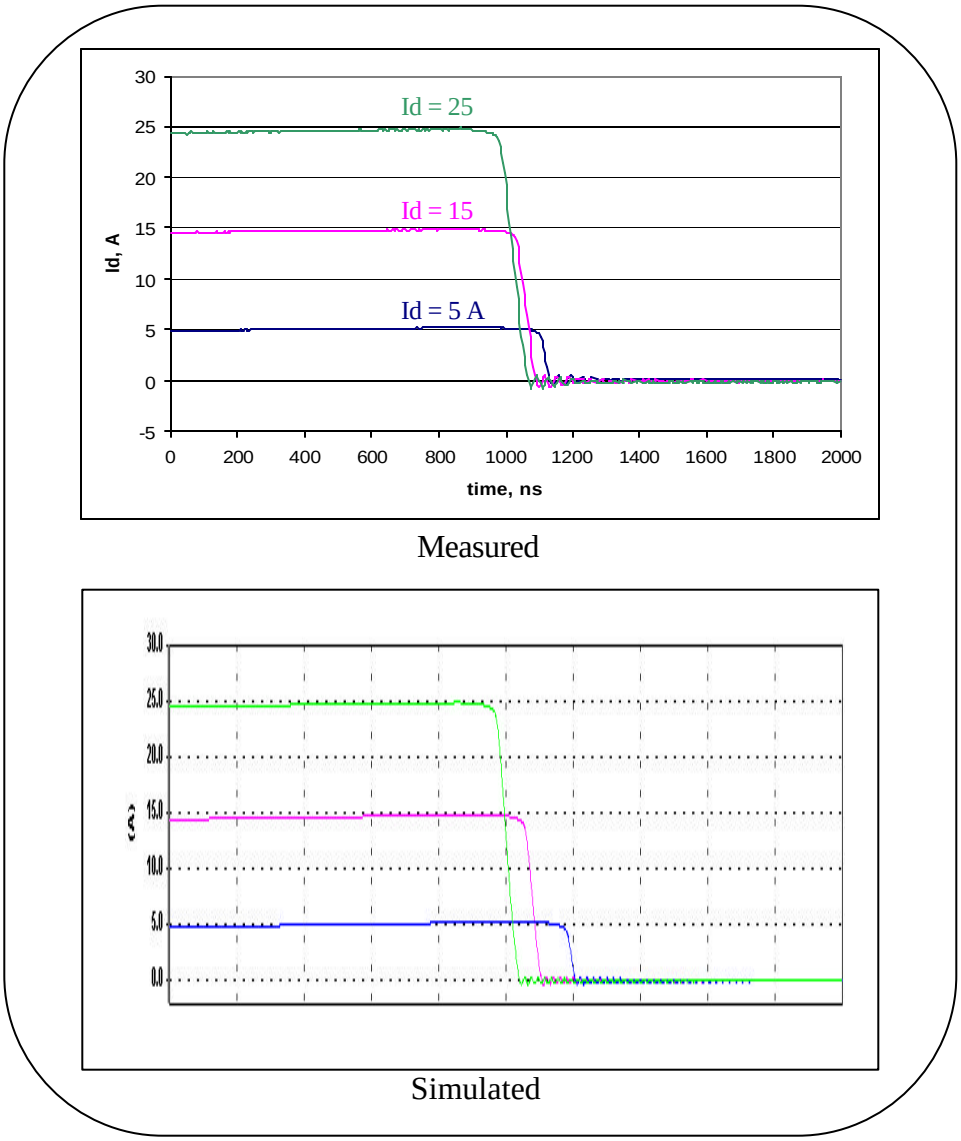

Figure 3.32. Comparison of I_d for simulation and measurement.

3.6.2 Change in Switching Waveforms with Varying L_S

This example shows the effects of the MOSFET's source pin inductance (L_S) on the switching waveforms (see section 3.5.1.2). Note that this variable is not available for adjustment in the real parametric study circuit. Figure 3.33 shows the simulated waveforms for V_{ds}, V_{gs}, and I_d during the turn-off transition. The figure shows that the voltage overshoot and current fall time are highly sensitive to L_S. This implies that it is very important that L_S is modeled accurately for the simulation circuit.

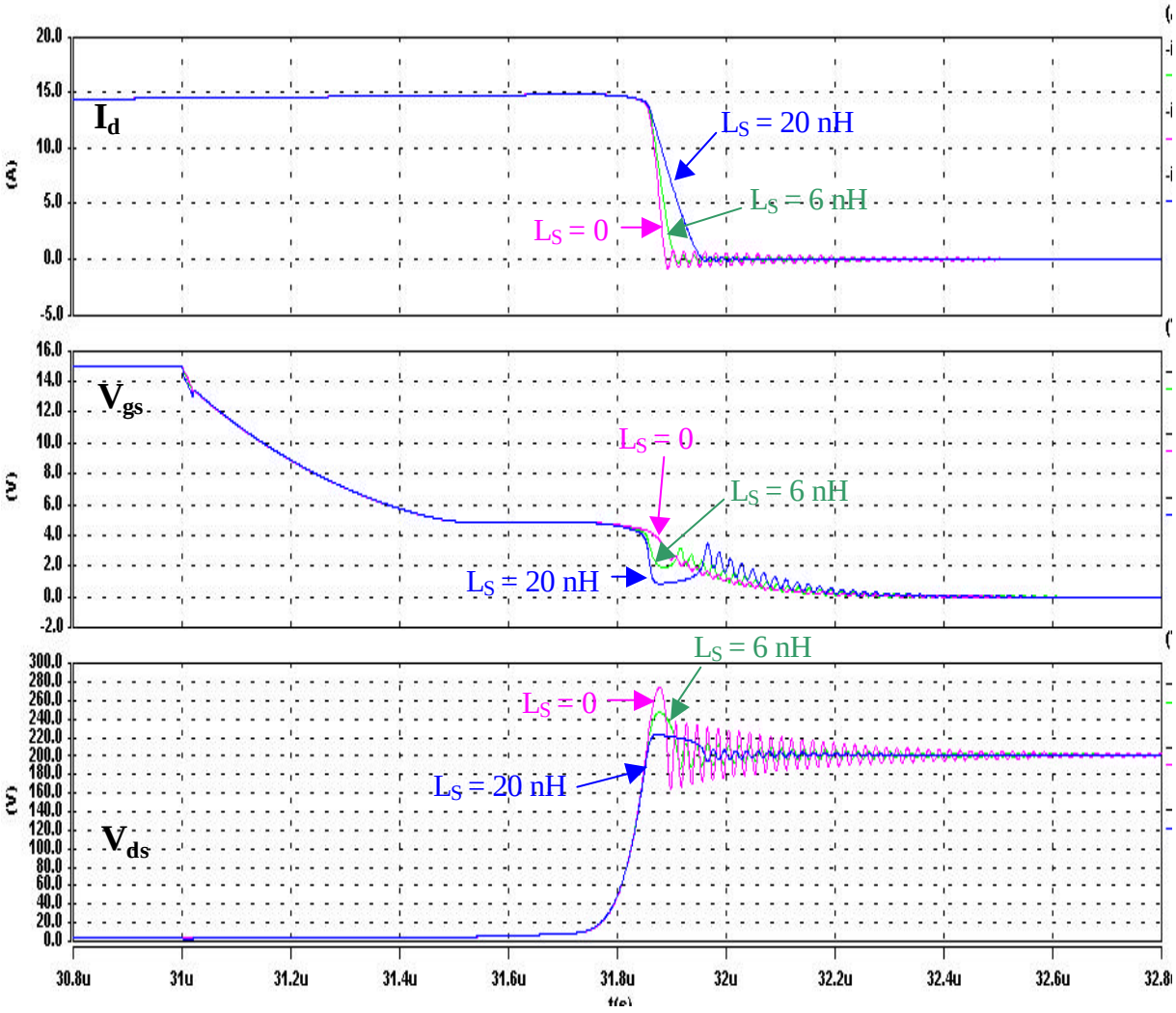

Figure 3.33. Switching waveforms for varying L_S.

Chapter 4 – Parametric Study Results

4.1 Introduction

This chapter presents the results for the parametric study described in Chapter 3. Section 4.2 describes the measurement procedure and considerations in very general terms. If more detail is needed, refer to Appendix C, which gives the step-by-step procedure used for obtaining the data. Section 4.3 explores the relative sensitivity of each switching characteristic to the varied parameters. By normalizing the varied parameters around their base values and plotting the relative effects of all parameters on a single plot, we can fairly analyze which circuit parameters and operating conditions most affect each characteristic. Sections 4.4 through 4.10 give the results for each varied parameter individually. Each section demonstrates graphically how the switching waveforms (V_{gs}, V_{ds} and I_d) change with changing parameters. Plots for each switching characteristic for each varied parameter are provided in Appendix D.

The test circuit and components were modeled, and a simulation circuit was developed in Saber as demonstrated in Chapter 3. The parametric study was performed in simulation, and the simulated results for the switching characteristics are given in the same plots with the measured data in Appendix D. A few general observations should be made regarding the comparison of the simulated and measured data. Though exact matching is desirable, it is not necessary for the purpose at hand. The simulation tool is used primarily to verify that general trends of the measured data are correct. Seeing similar trends in simulation gives comfort that the measured data is correct. If improved accuracy is necessary for future needs, more thorough modeling will be required, especially regarding the dynamic characteristics of the power devices.

Using the resulting data, we can decide how to design the tester layout, what operating conditions should be chosen for testing, and what effects of the tester must be decoupled to truly see the effects of DUT design.

4.2 Making the Measurements

This section discusses the procedure for obtaining the switching characteristics data presented throughout the remainder of this chapter. Generally, the data is determined by zooming in to the waveforms as closely as possibly and using the cursor functions of the oscilloscope to measure the desired values. For example, to measure the current rise time, one would zoom-in to the rising edge of the drain current and use the cursors to measure the time it takes for the current to rise from 10% to 90% of its nominal value. It is tempting to zoom-in to the entire switching transition in order to measure all of the switching characteristics quickly. However, one should instead zoom-in as closely as possibly to each characteristic individually. This slows the measurement process down, but it yields much more accurate results.

To measure the turn-on switching energy loss, one must zoom-out to the entire turn-on interval. Two of the oscilloscope math functions are used. The multiplication function is used to multiply V_{ds} and $-I_d$ (the current is negative because of the orientation of the shunt). The result of this multiplication is then saved as a reference waveform. The oscilloscope's integration function is then used to integrate the reference waveform. The resultant waveform is the negative of the energy.

4.3 Sensitivity Analysis

This section demonstrates the relative sensitivity of each switching characteristic to the varied parameters (gate resistance, loop inductance, etc.). Figures 4.1 through 4.15 plot the effects on the switching characteristics of Table 4.1 below (see section 1.5) for the varied parameters given below in Table 4.2.

Table 4.1. Switching characteristics.

Turn-on Characteristics		Turn-off Characteristics	
Characteristic	Symbol	Characteristic	Symbol
turn-on time	t_{ON}	turn-off time	t_{OFF}
current turn-on delay time	$t_{d(ON)I}$	current turn-off delay time	$t_{d(OFF)I}$
current rise time	t_{rI}	current fall time	t_{fI}
voltage fall time	t_{fV}	voltage rise time	t_{rV}
turn-on switching current gradient	di/dt(on)	turn-off switching current gradient	di/dt(off)
current overshoot	I_{OS}	turn-off switching voltage gradient	dv/dt(off)
turn-on energy	E_{ON}	voltage overshoot	V_{OS}
		turn-off energy	E_{OFF}

Table 4.2 Varied parameters and their base values.

Parameter Name	Parameter Symbol	Base Value
Gate Resistance	R_g	30 ohm
Gate Voltage	V_g	15 V
Bus Voltage	V_{bus}	200 V
Drain Current	I_d	15 A
Bus Capacitance	C_{bus}	600 nF
Loop Inductance	L_{Loop}	150 nH
Junction Temperature	T_j	25 °C

Each value of each parameter is normalized around its base value as follows:

$$x_{norm} = \frac{x}{x_{base}} \tag{4.1}$$

where x represents the parameter varied, x_{base} is the parameter's base value, and x_{norm} is the normalized value. Table 4.3 assigns a relative sensitivity of each varied parameter on each characteristic. Calculation of the sensitivity (S), is done with the following equation:

$$S = \frac{\left(y_{\max} - y_{\min}\right)/y_{base}}{x_{norm-\max} - x_{norm-\min}} \tag{4.2}$$

where y_{max} and y_{min} are the maximum and minimum values of the given switching characteristic, $x_{norm\text{-}max}$ and $x_{norm\text{-}min}$ are the maximum and minimum normalized parameter values, and y_{base} is the switching characteristic value at x_{base}. y_{base} is used to normalize the switching characteristic values (S should not have units).

The actual base value for the junction temperature is $T_{j\text{-}base}$ = 25 °C, but using this value for the sensitivity analysis would give a normalized value range of $T_{j\text{-}norm\text{-}min}$ = 1 to $T_{j\text{-}norm\text{-}max}$ = 4. The data for $T_{j\text{-}base}$ = 50 °C is used instead as the base values for the sensitivity analysis to reduce this range and make the trends in Figures 4.1 through 4.15 more visible. This is the reason that the junction temperature data will not necessarily meet the other parameters' data at a normalized value of 1.

Graphical results are not given for the turn-on switching voltage gradient, or dv/dt(on). As the drain voltage falls during turn-on, the shape of the waveform changes depending on switching speed and parasitic inductance. Since the general shape of the waveform at the voltage levels where the measurement is made will change, it is extremely difficult to make accurate measurements of this characteristic. However, the switching waveforms are provided in sections 4.4 through 4.10, and qualitative trends can be determined for the dv/dt(on) for each varied parameter.

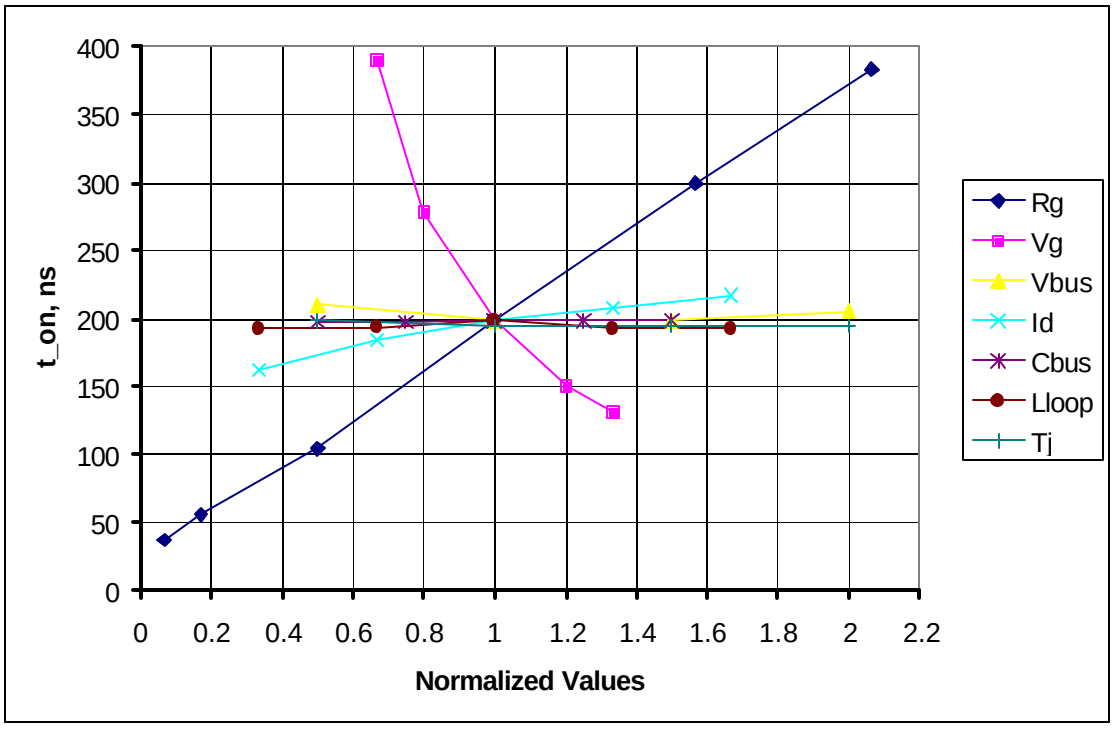

Figure 4.1. Sensitivity of t_{ON} to the varied parameters.

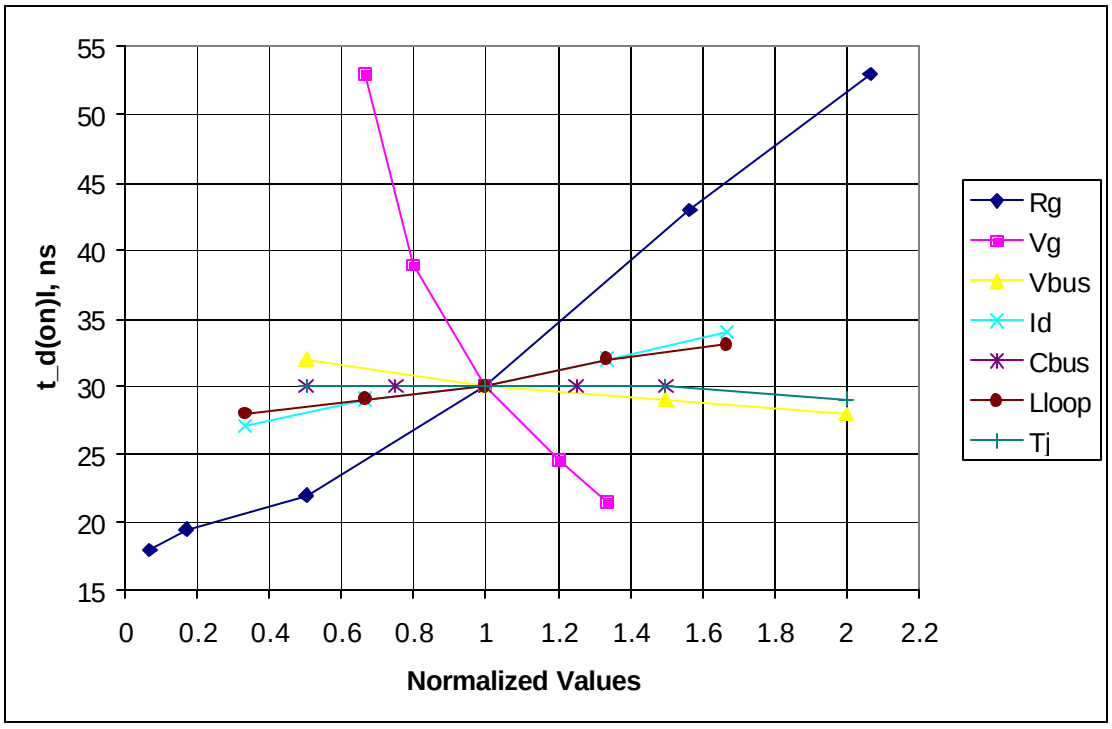

Figure 4.2. Sensitivity of $t_{D(ON)I}$ to the varied parameters.

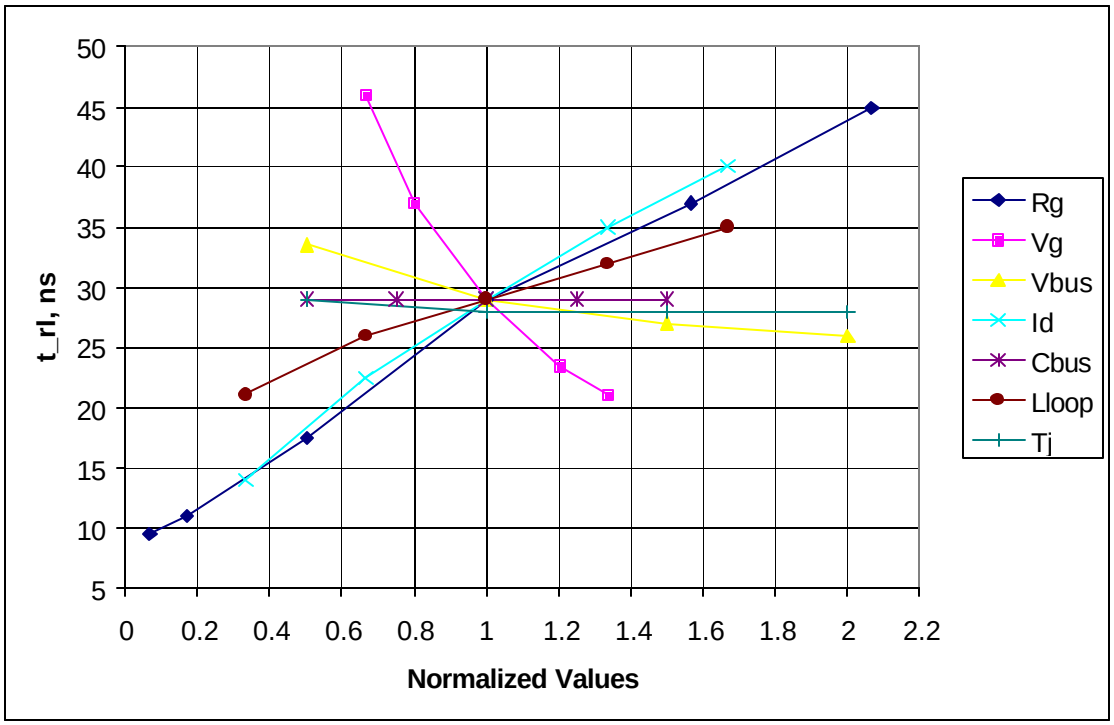

Figure 4.3. Sensitivity of t_{rI} to the varied parameters.

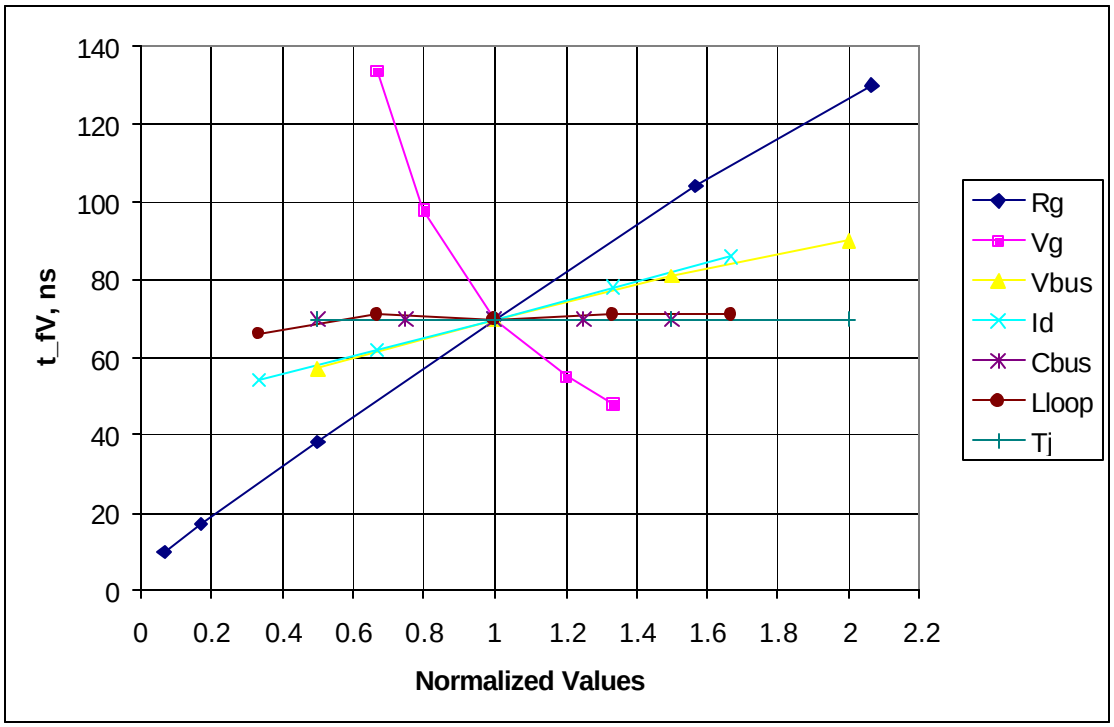

Figure 4.4. Sensitivity of t_{fV} to the varied parameters.

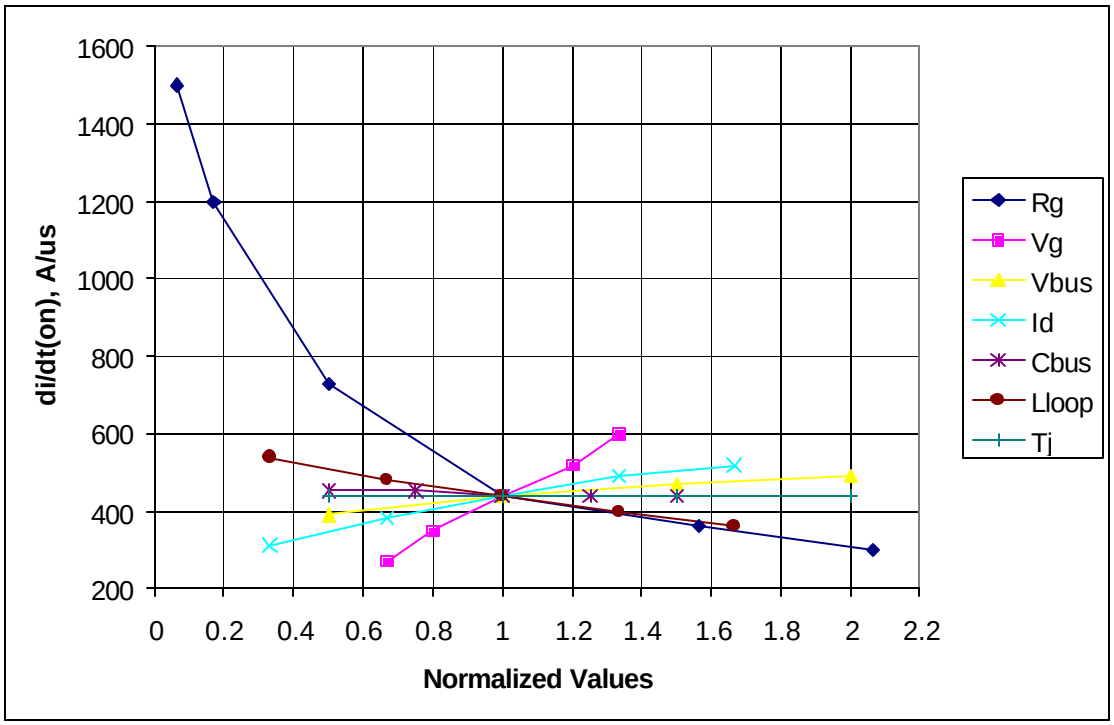

Figure 4.5. Sensitivity of di/dt(on) to the varied parameters.

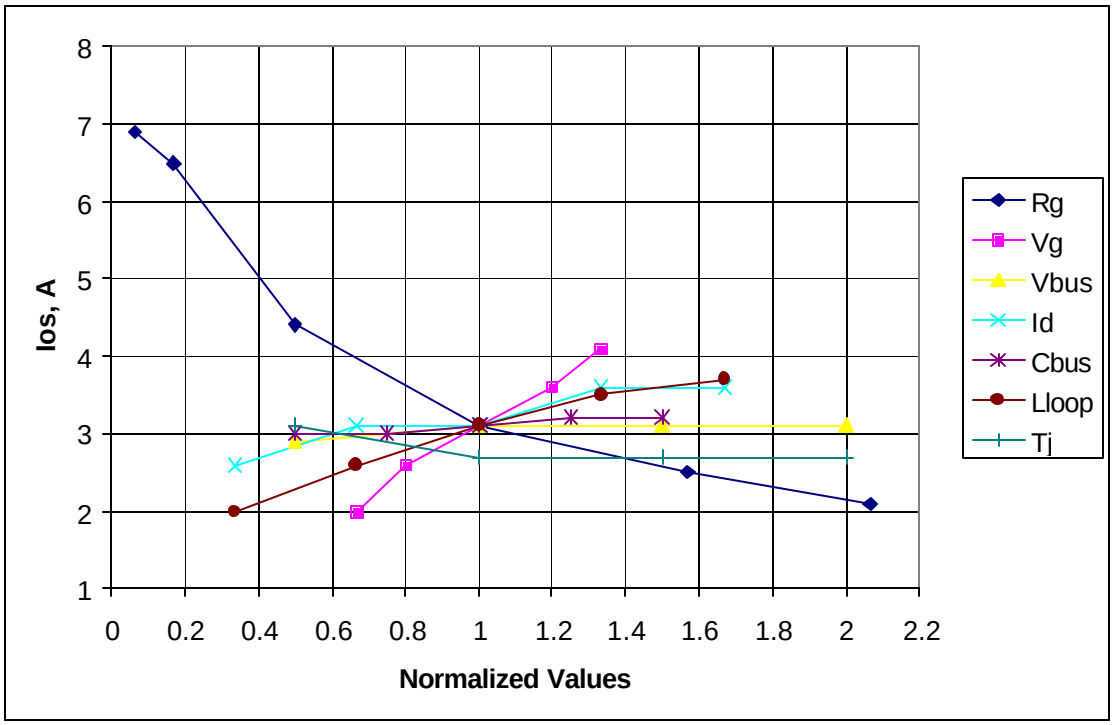

Figure 4.6. Sensitivity of I_{OS} to the varied parameters.

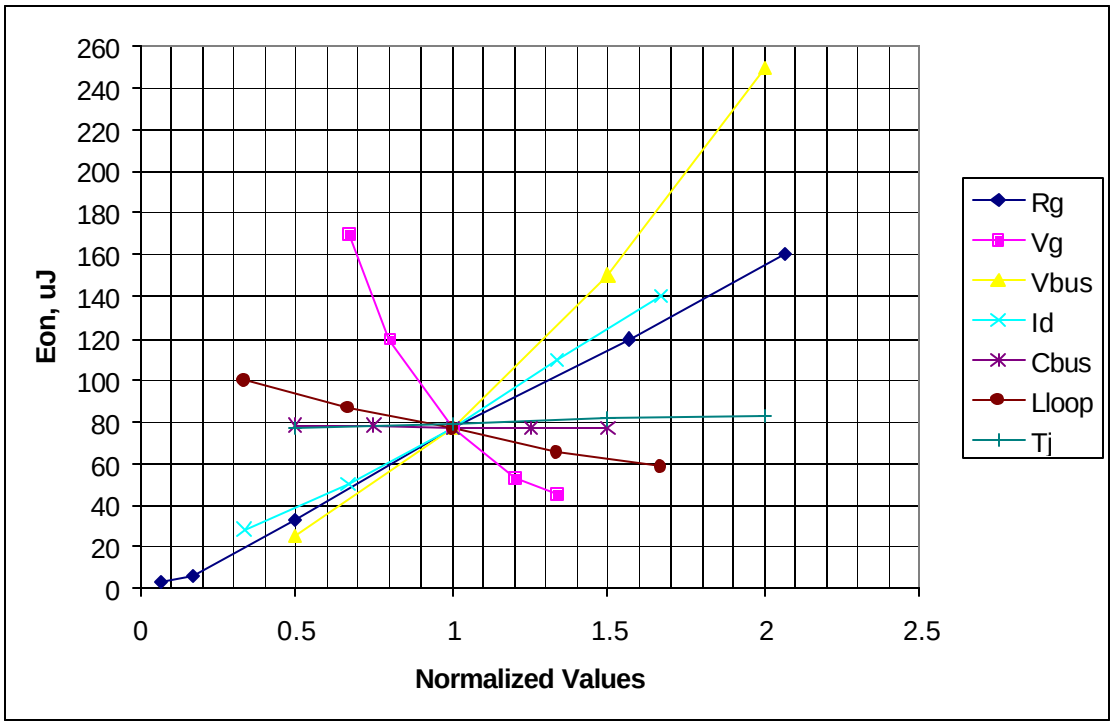

Figure 4.7. Sensitivity of E_{ON} to the varied parameters.

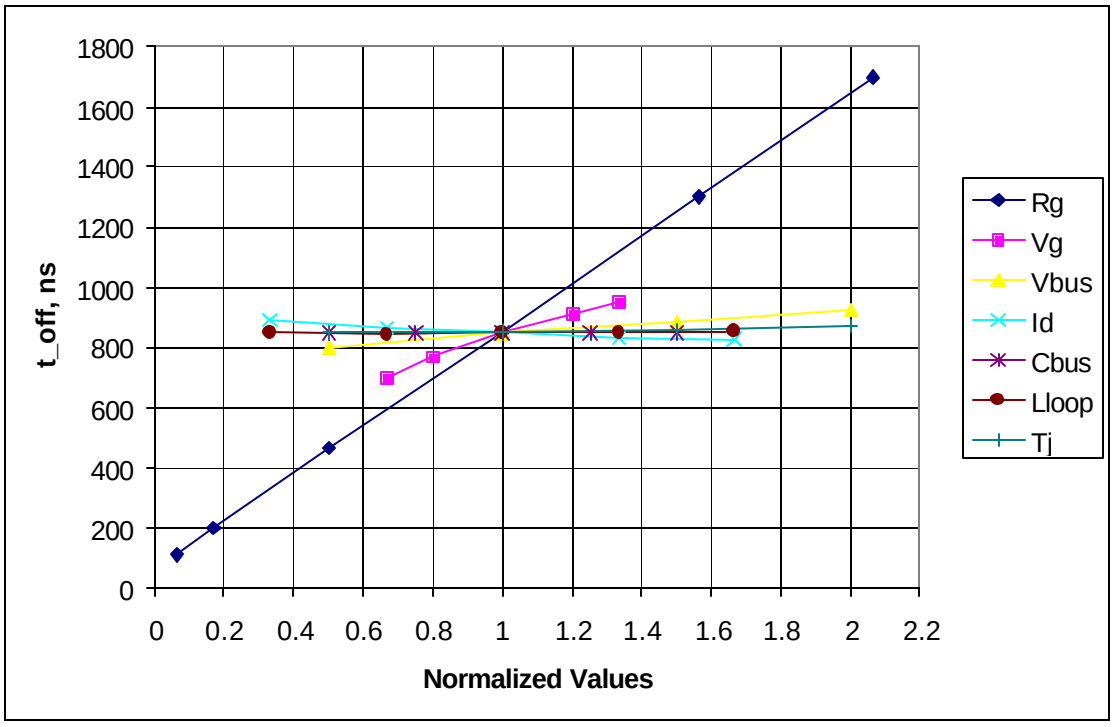

Figure 4.8. Sensitivity of t_{OFF} to the varied parameters.

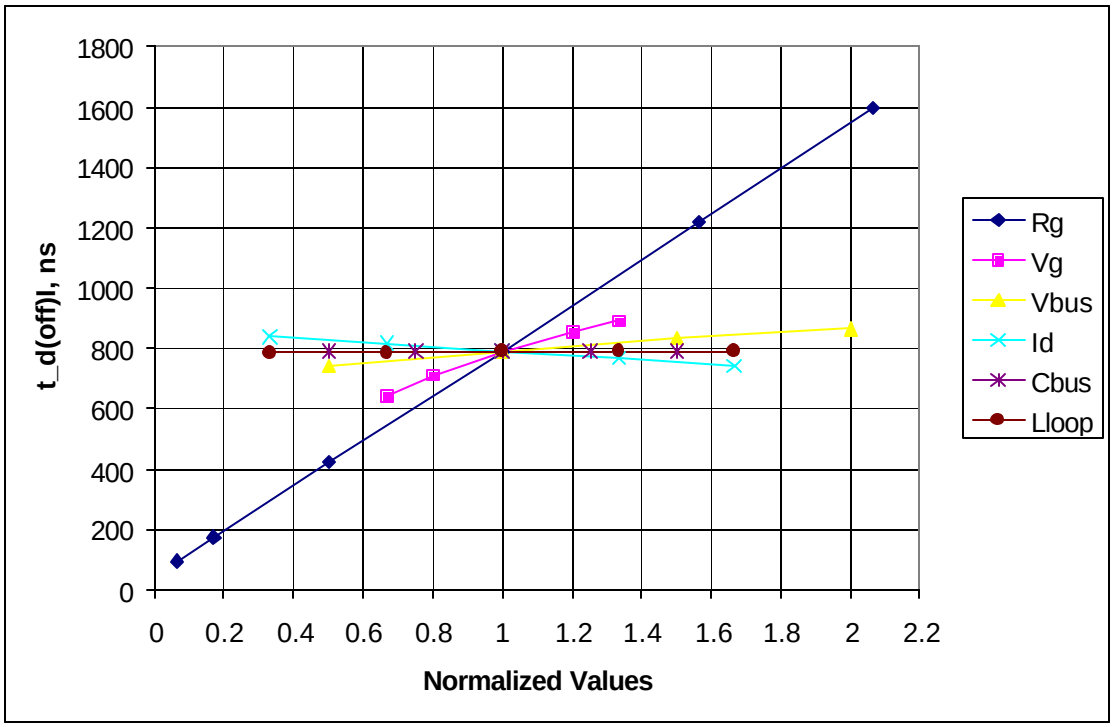

Figure 4.9. Sensitivity of $t_{D(OFF)I}$ to the varied parameters.

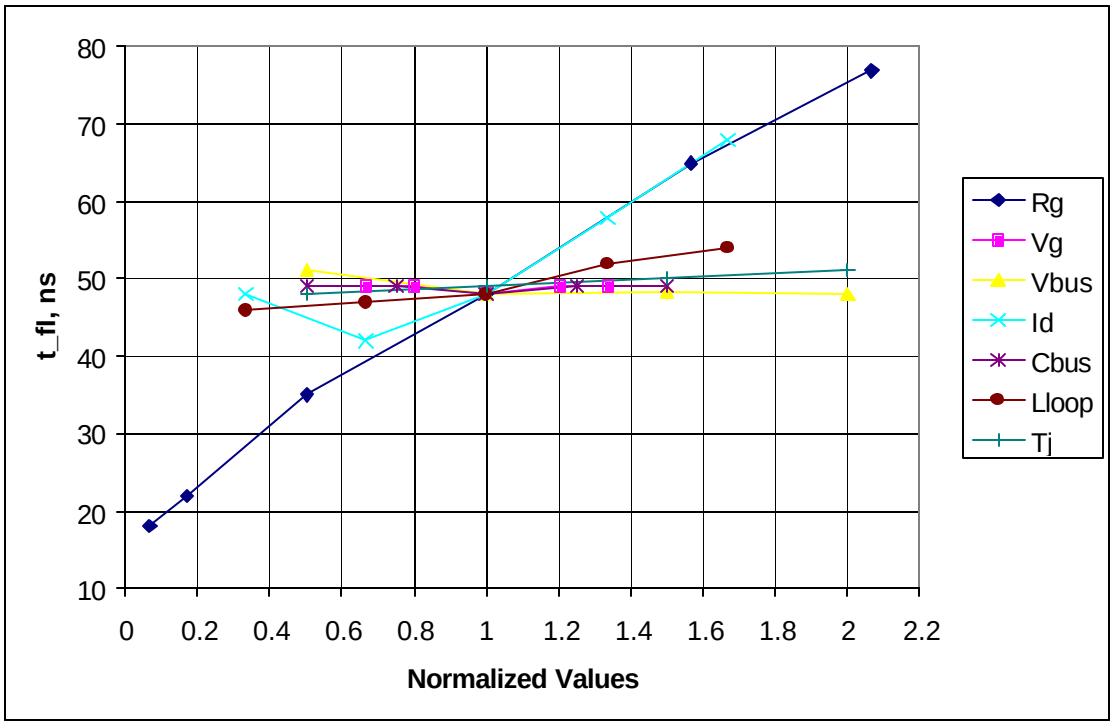

Figure 4.10. Sensitivity of t_{fl} to the varied parameters.

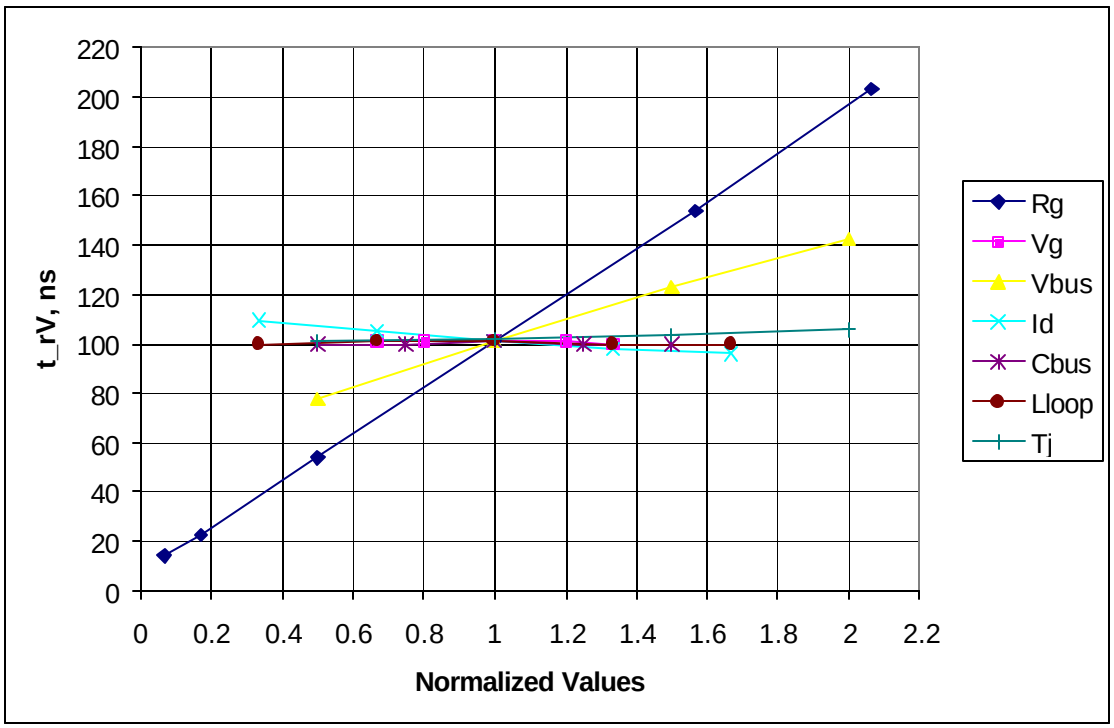

Figure 4.11. Sensitivity of t_{rV} to the varied parameters.

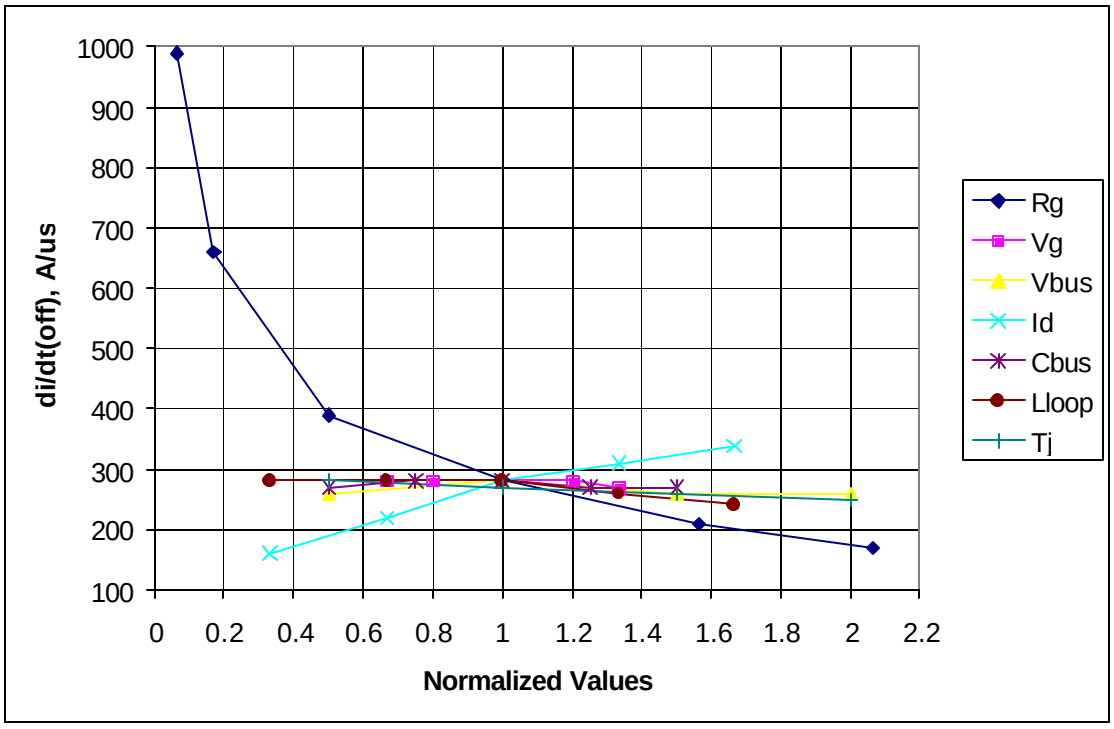

Figure 4.12. Sensitivity of di/dt(off) to the varied parameters.

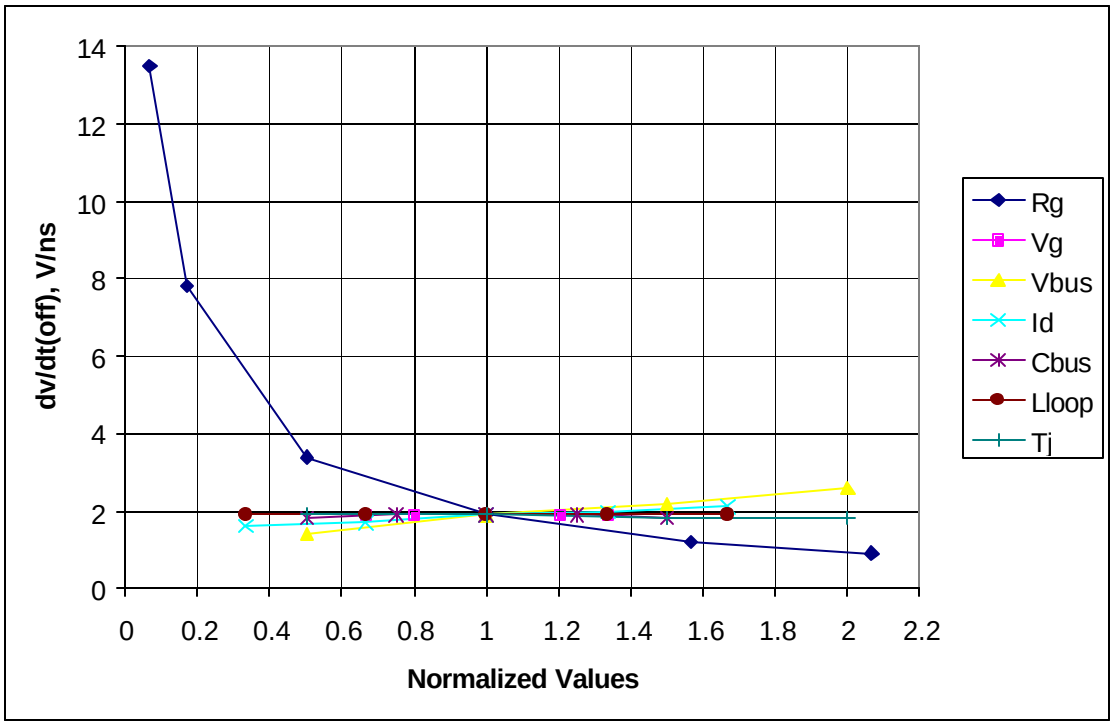

Figure 4.13. Sensitivity of dv/dt(off) to the varied parameters.

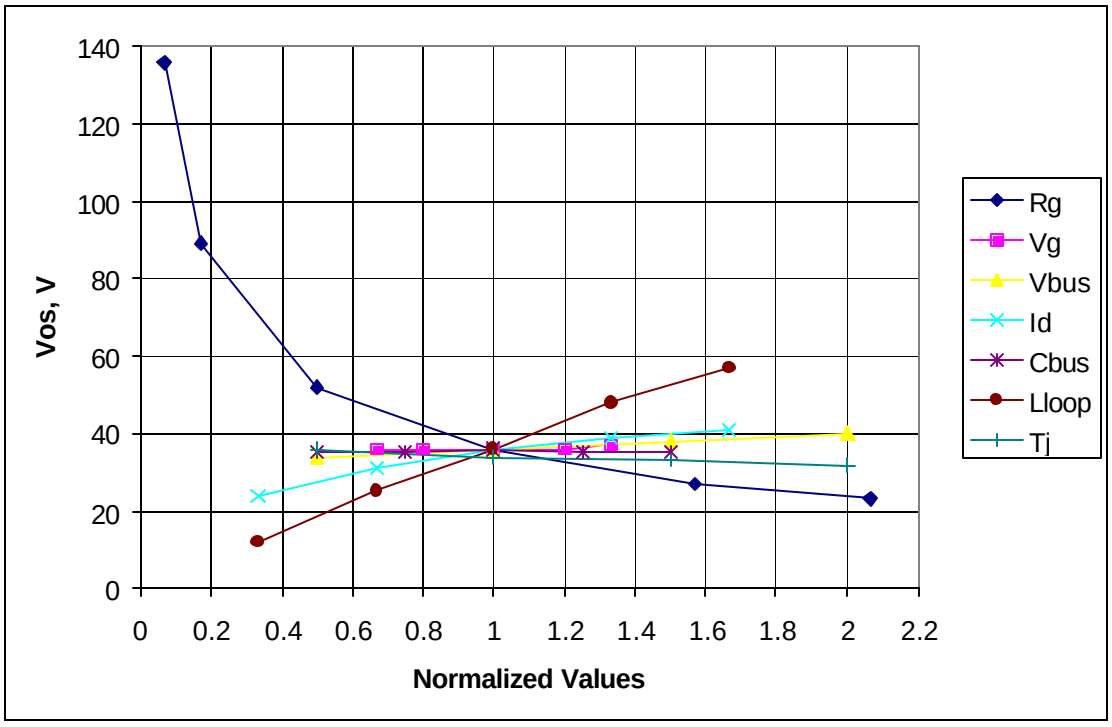

Figure 4.14. Sensitivity of V_{OS} to the varied parameters.

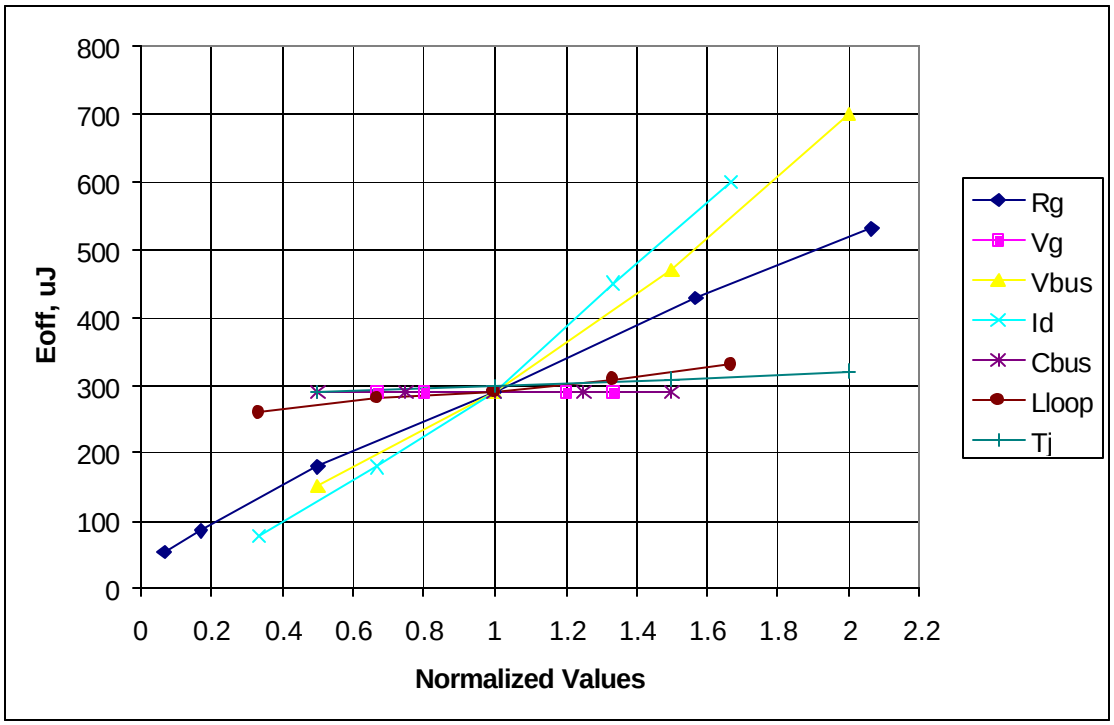

Figure 4.15. Sensitivity of E_{OFF} to the varied parameters.

Table 4.3. Normalized sensitivity (Eq. 4.2) of switching characteristics.

	Parameters Varied						
Characteristics	Rg	Vg	Lloop	Cbus	Vbus	Id	Tj
t_on	87	** -196	-2	1	-4	21	0
t_d(on)I	58	** -157	13	0	-9	18	-1
t_rI	61	** -129	36	0	-17	67	-1
di/dt(on)	** -136	112	-31	-2	15	36	0
t_fV	86	** -184	5	0	31	34	0
dv/dt(on)							
los	-77	** 102	41	6	4	24	-3
Eon	102	** -243	-41	-1	195	109	2
t_off	** 93	44	1	0	9	-6	1
t_d(off)I	** 95	47	1	0	10	-9	1
t_fI	** 61	3	13	+2	4	54	2
di/dt(off)	** -146	-5	-11	-4	-5	48	-3
t_rV	** 94	-1	-1	-1	43	-10	1
dv/dt(off)	** -331	0	0	-5	42	16	-1
Vos	** -157	4	94	-3	11	35	-3
Eoff	82	0	18	0	126	** 135	3
**: most sensitive -: decreasing trend (otherwise trend is increasing)							

From the plots and Table 4.3, one can see which parameters have the greatest effect on each switching characteristic. Since most of the characteristics are related to or are affected by switching speed, it is not surprising to find that the gate drive parameters (R_g and V_g) dominate many of the results. Loop inductance, bus voltage, and drain current also demonstrate significant effects on rise and fall times, device stresses and switching energy losses. Bus capacitance and junction temperature have little effect compared to the other parameters. The remainder of this chapter focuses on how and why each varied parameter affects the switching characteristics.

4.4 Varying gate resistance

Figures 4.16 through 4.18 show the gate-source voltage, drain-source voltage, and drain current for various values of gate resistance during the turn-on transition while all other parameters have the base values from Table 4.2. The higher resistance with the same applied voltage from the gate driver chip results in lower available current to drive the MOSFET. From Figure 4.16, one can see that increasing R_g slows down the initial

gate charging. The longer it takes for V_{gs} to reach its threshold value, the longer the current delay, as can be observed from Figure 4.18. The voltage and current gradients are also reduced, leading to longer total turn-on times, reduced current stress, and increased overlap of the V_{ds} and I_d waveforms. The longer overlap will increase switching energy losses.

The minimum R_g used was 2 O. There is no point in using smaller values, because the gate driver output impedance (approximately 1.5 O) that appears in series with R_g would then begin to dominate the total gate impedance.

The maximum R_g used was 62 O. The larger values of gate resistance were used initially, because of the lack of trust in the current measurement. Recall from Chapter 2 that the 10 mO shunt originally used had considerable error due to the small amount of series parasitic inductance. Faster switching caused increased errors. When the new shunt was first applied, larger R_g were used so that the measurement could more easily be trusted. Another reason for using large R_g is that the characteristics that change with R_g are exaggerated and become easier to notice. For instance, the plateau observed in the gate voltage during turn-on just looks like parasitic ringing for the smaller R_g but can be observed easily for the larger R_g.

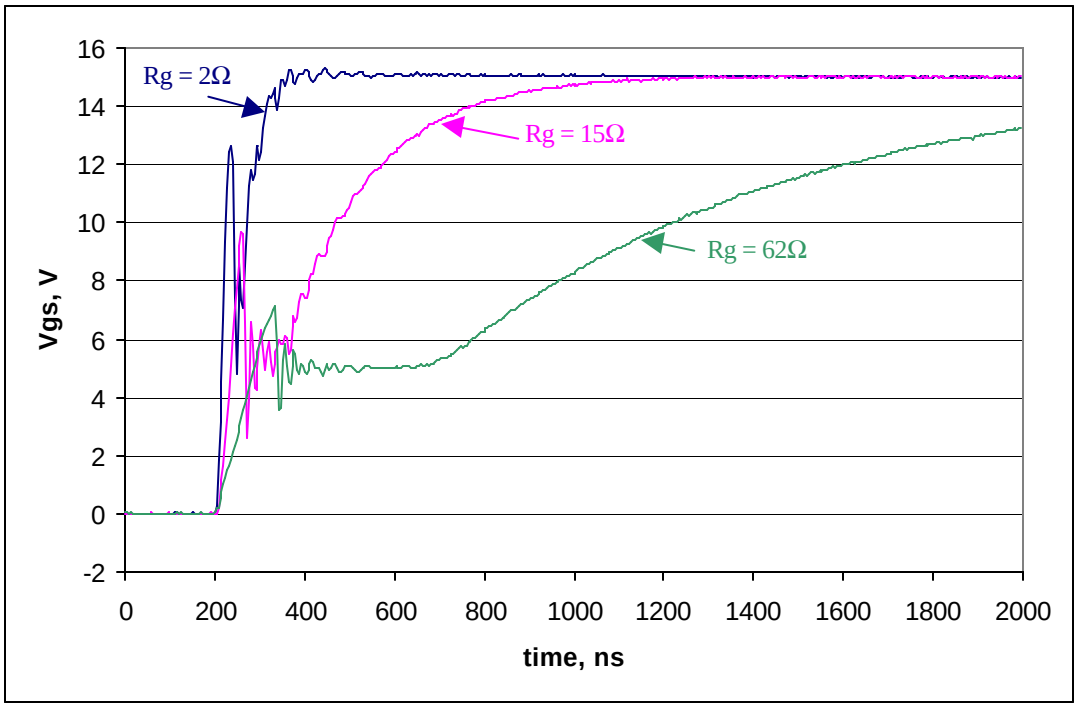

Figure 4.16. V_{gs} for different gate resistances during turn-on.

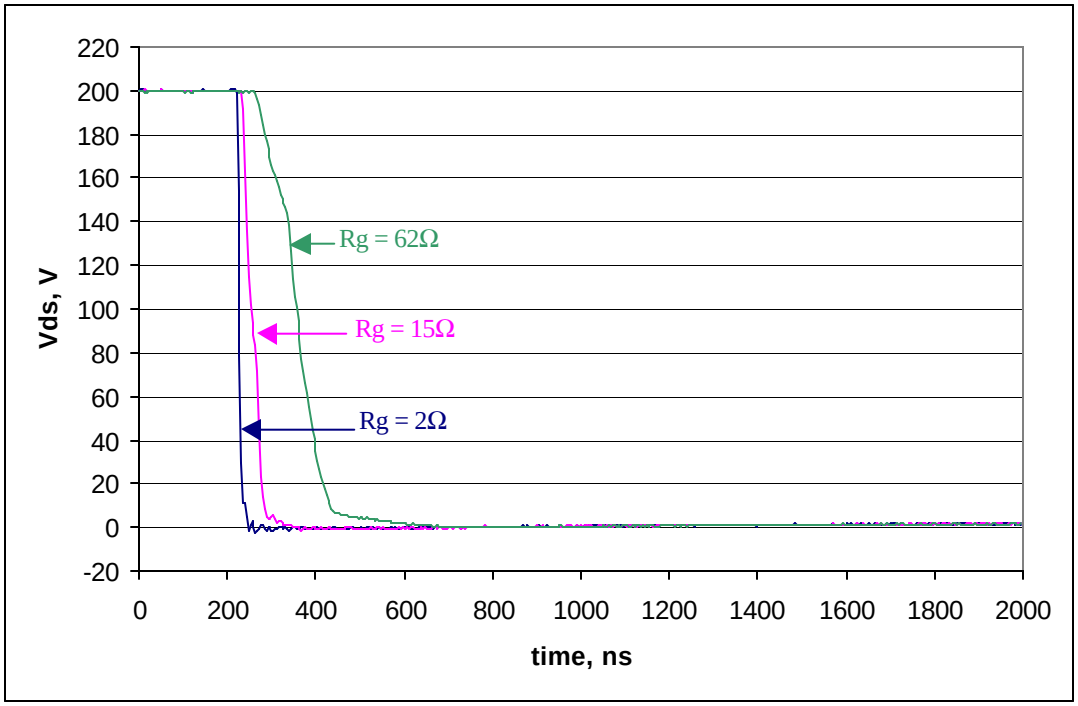

Figure 4.17. V_{ds} for different gate resistances during turn-on.

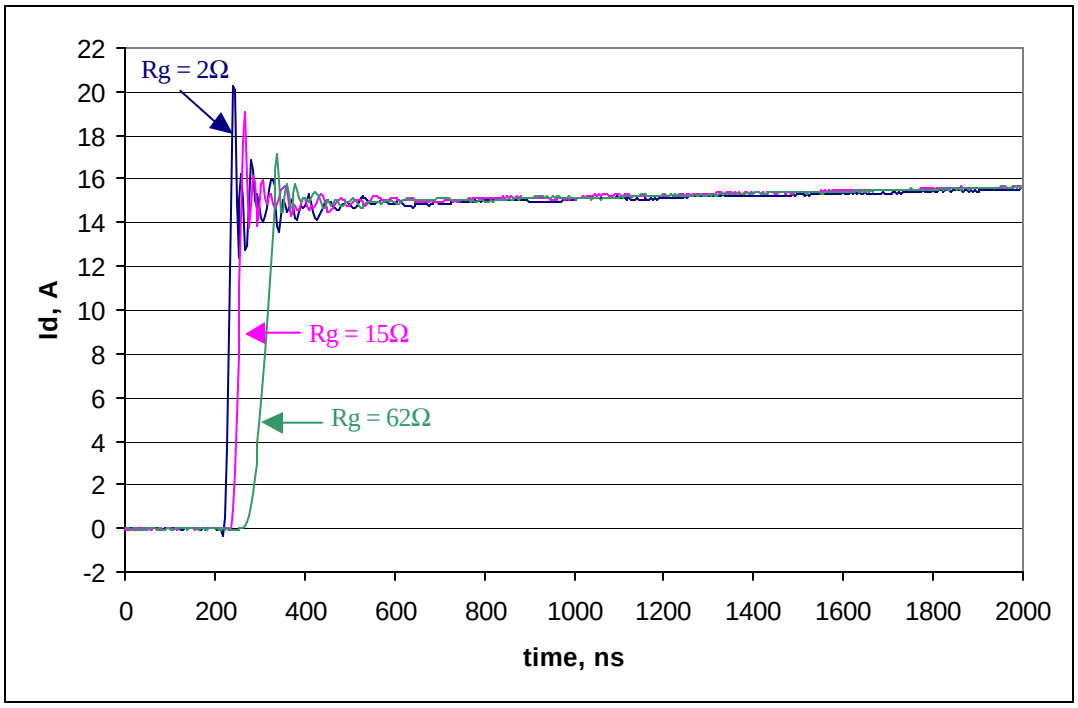

Figure 4.18. I_d for different gate resistances during turn-on.

Figures 4.19 through 4.21 show the gate voltage, drain voltage, and drain current for various values of gate resistance during the turn-off transition while all other parameters have the base values from Table 4.2. The higher resistance will cause the gate to discharge at a slower rate, leading to longer delays before V_{ds} begins to rise. The drain-source rise rate will also depend on how fast the gate-drain capacitance can be charged, which will be limited by the amount of current that can be sunk through the gate resistance. Large R_g will limit this current, reducing the dv/dt. The current gradient is also reduced. Much like the turn-on case, one would expect longer total turn-off time, reduced voltage overshoot and ringing, and increased energy loss.

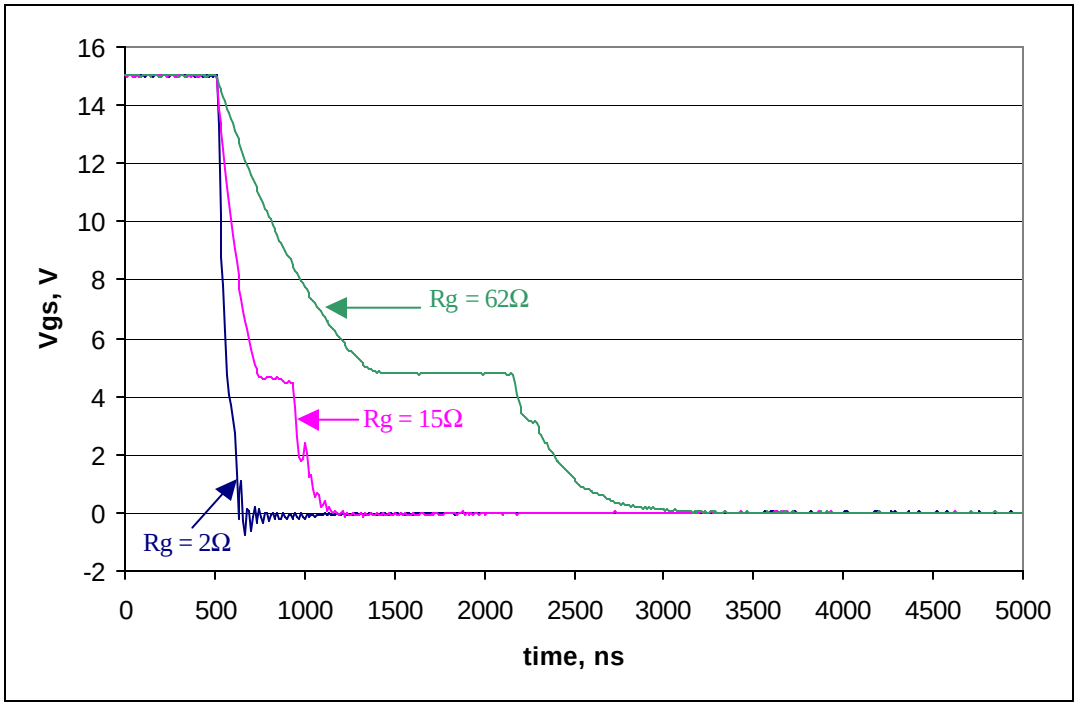

Figure 4.19. V_{gs} for different gate resistances during turn-off.

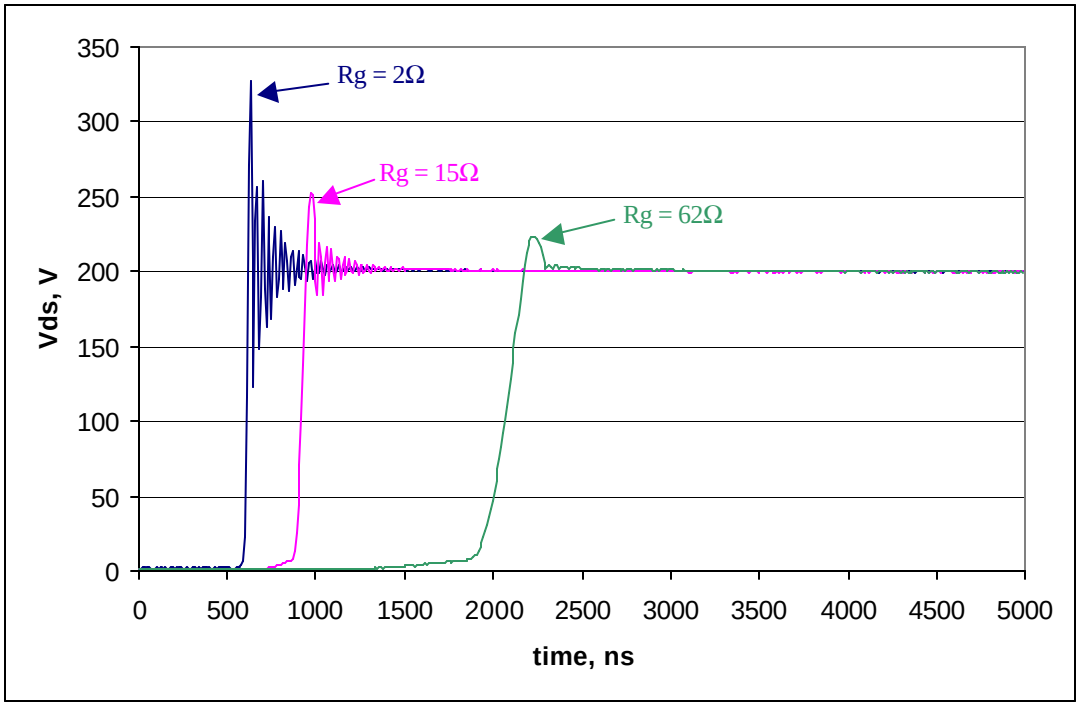

Figure 4.20. V_{ds} for different gate resistances during turn-off.

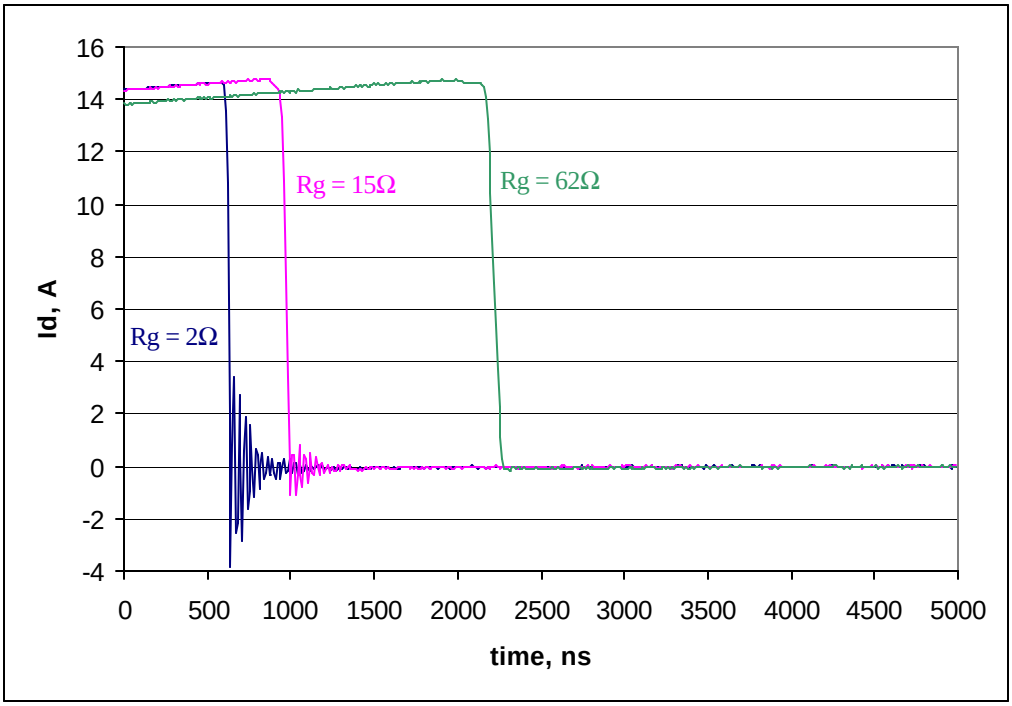

Figure 4.21. I_d for different gate resistances during turn-off.

4.5 Varying gate voltage

Figures 4.22 through 4.24 show the gate voltage, drain voltage, and drain current for various values of gate voltage during the turn-on transition while all other parameters have the base values from Table 4.2. The range of gate voltages tested covers the full range of useful values for a power MOSFET. From the figures, one can see similar results for increasing gate voltage as decreasing gate resistance. Increasing the gate voltage and keeping the gate resistance constant allows more current to charge the gate capacitance, and V_{gs} reaches the threshold voltage more quickly. Therefore, the current delay is reduced. The voltage and current gradients are increased just as described for changes in gate resistance, and the voltage fall times and current rise times decrease accordingly. The decreased fall times reduce the turn-on switching loss with the price of higher current overshoot and ringing.

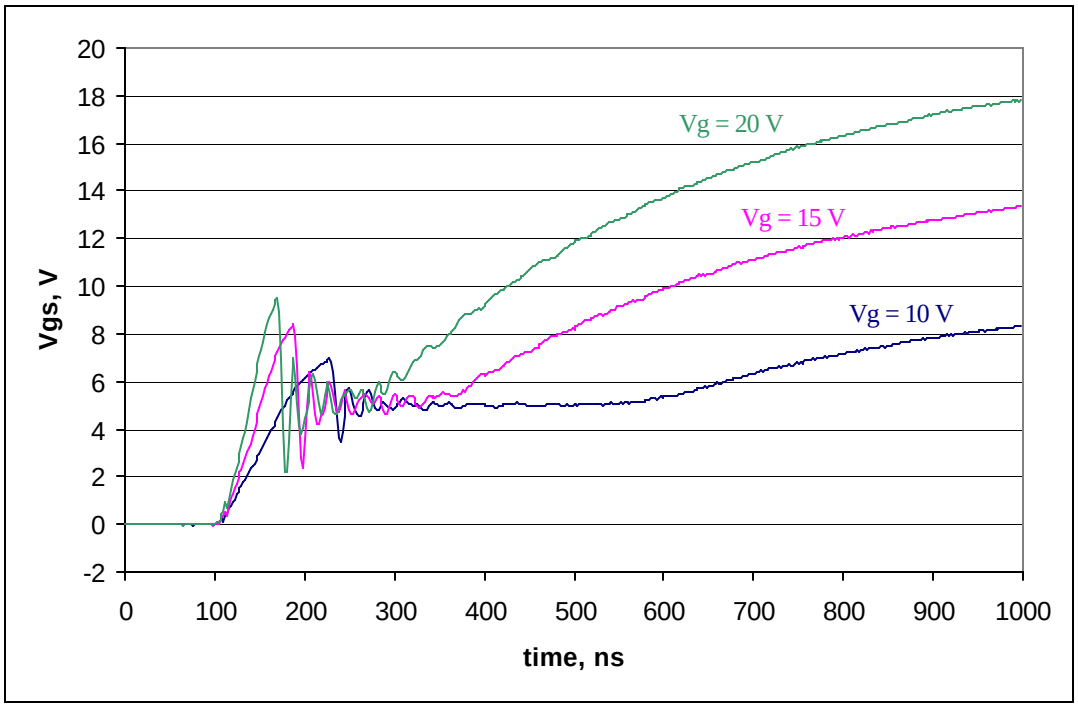

Figure 4.22. V_{gs} for different gate voltages during turn-on.

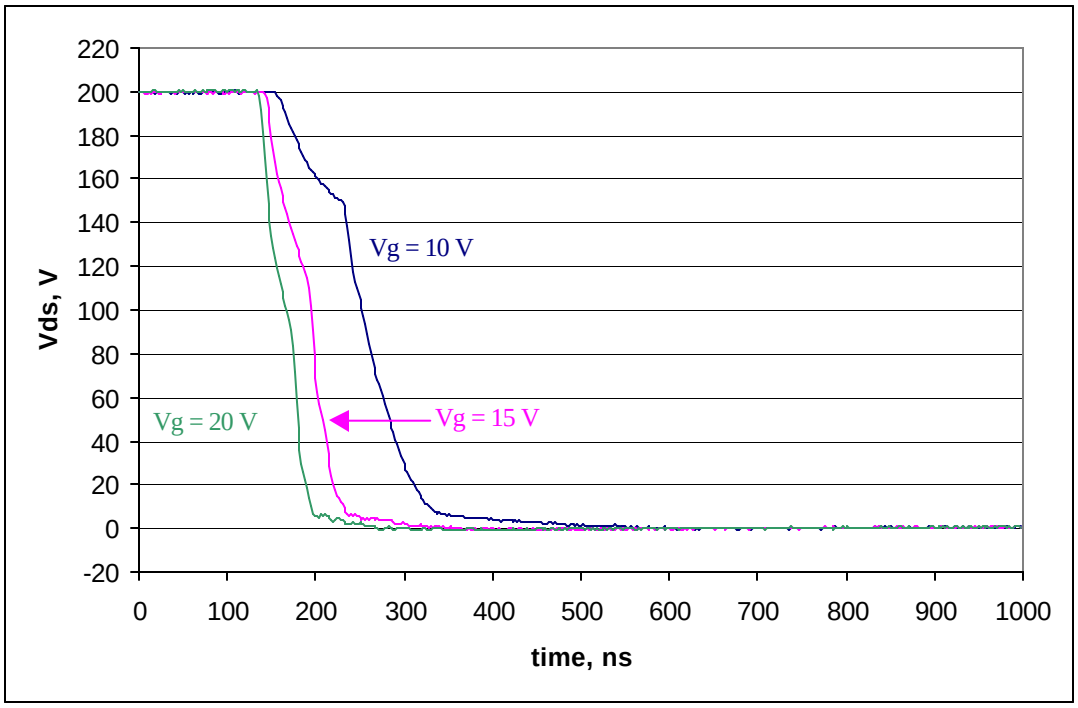

Figure 4.23. V_{ds} for different gate voltages during turn-on.

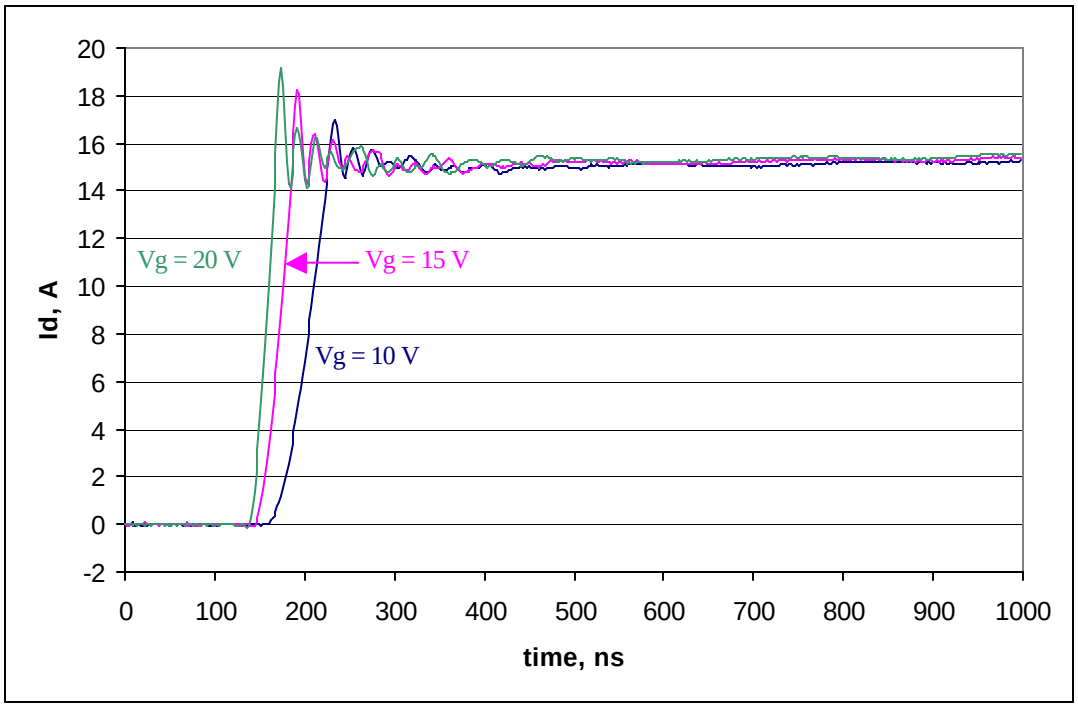

Figure 4.24. I_d for different gate voltages during turn-on.

Figures 4.25 through 4.27 show the gate voltage, drain voltage, and drain current for various values of gate voltage during the turn-off transition while all other parameters have the base values from Table 4.2. Referring to the sensitivity plots or Table 4.3, one will note that the gate voltage has effects on the turn-off current delay and the total turn-off time, but it has virtually no effect on the other turn-off characteristics. Viewing Figure 4.25, note that the gate voltages fall to the plateau voltage at 5 volts at nearly the same rate. When the gate driver is given the command to turn-off, the gate capacitance begins to discharge through the gate resistor and the output impedance of the gate driver chip. Since the applied voltage from the driver is zero, only this impedance determines the voltage rate of decent. Since the rate is the same and the gate voltage initial value is higher, it will naturally take the higher voltage longer to reach the plateau. The characteristics after reaching the plateau are the same no matter what the original applied gate drive voltage, since the impedance is the same. The result is that there is an increased current delay, and therefore total turn-off time, while there is no change in any of the other switching characteristics.

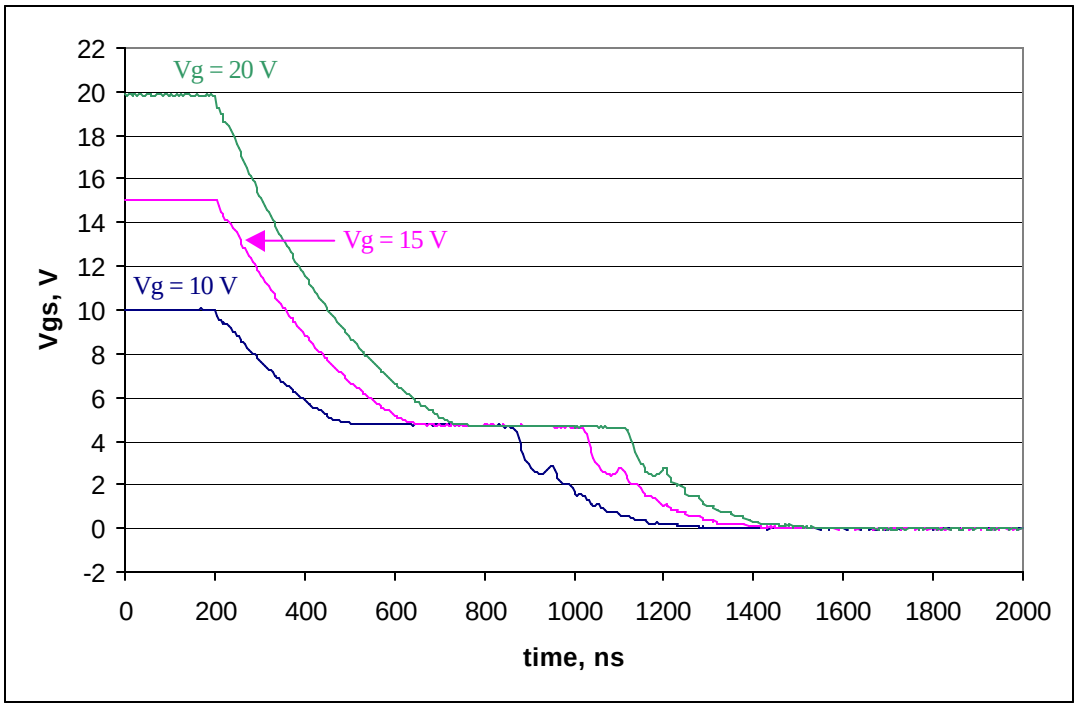

Figure 4.25. V_{gs} for different gate voltages during turn-off.

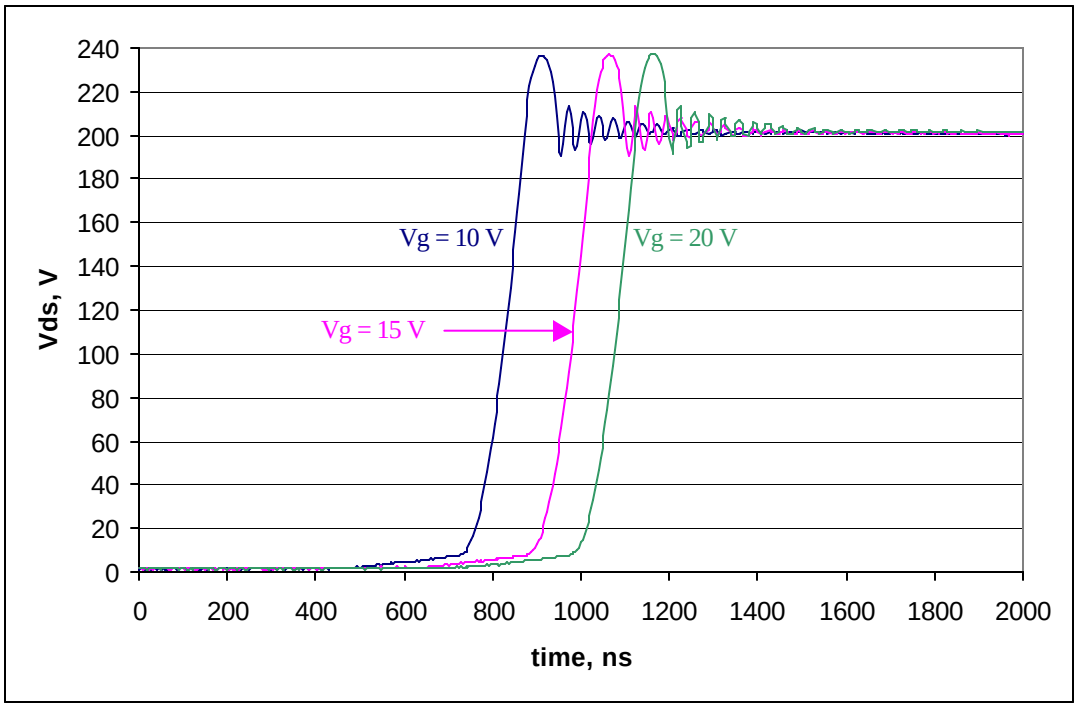

Figure 4.26. V_{ds} for different gate voltages during turn-off.

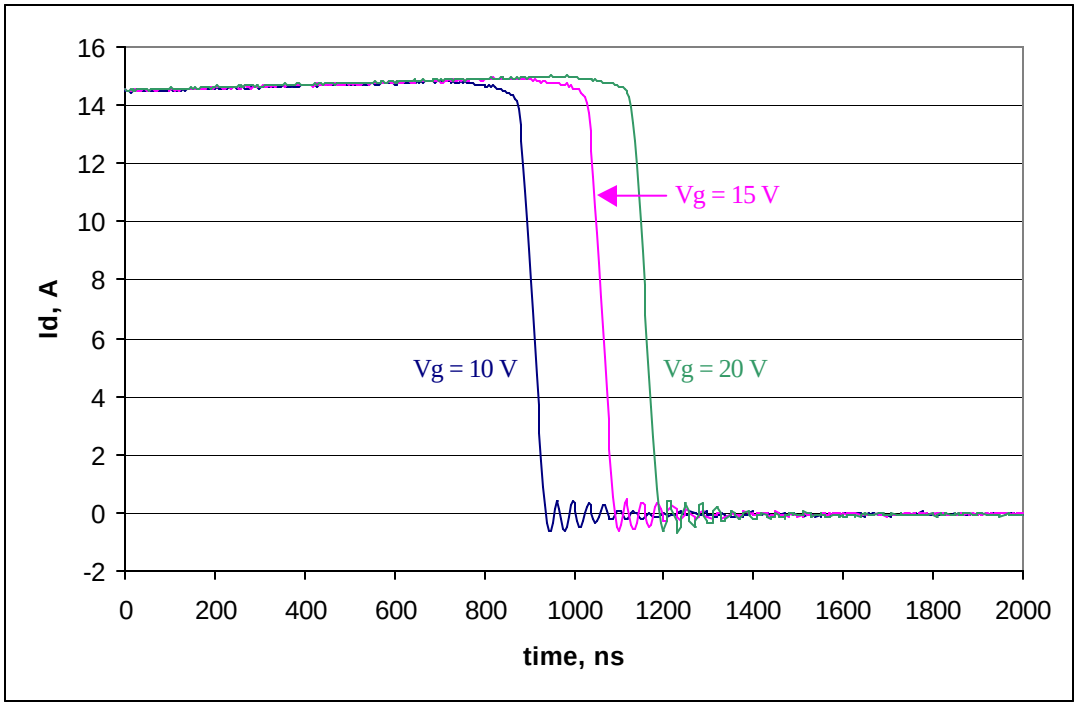

Figure 4.27. I_d for different gate voltages during turn-off.

4.6 Varying bus voltage

Figures 4.28 through 4.30 show the gate voltage, drain voltage, and drain current for various values of bus voltage during the turn-on transition while all other parameters have the base values from Table 4.2. When viewing the gate voltage, one see that there is little time difference between the time the gate voltage reaches the threshold for different bus voltages. Therefore, there is very little change in current delay. When viewing Figure 4.30, there is a slightly noticeable change in di/dt and current overshoot, but this is primarily due to a change in the level of current. Notice from the I_d plots, that the 200 V case has a larger "steady-state" current after the spike. This is why it appears to have a higher current overshoot and faster rising edge. From Figure 4.29, note that the drain voltage appears to have two main slopes. The first, slower slope results from L*di/dt while the drain current is rising from zero. Note that in all three drain voltage measurements, the level of this L*di/dt voltage drop is nearly the same, further implying that the change in di/dt for the different cases is minimal. The second, faster slope is due to the gate driver discharging the drain-source parasitic capacitor through the Miller capacitance. For both slopes, the rate of change should be independent of the bus voltage. From Figure 4.29, one can see that the slopes are similar for the different cases. This implies longer fall times for the drain voltage, which means increased turn-on switching losses.

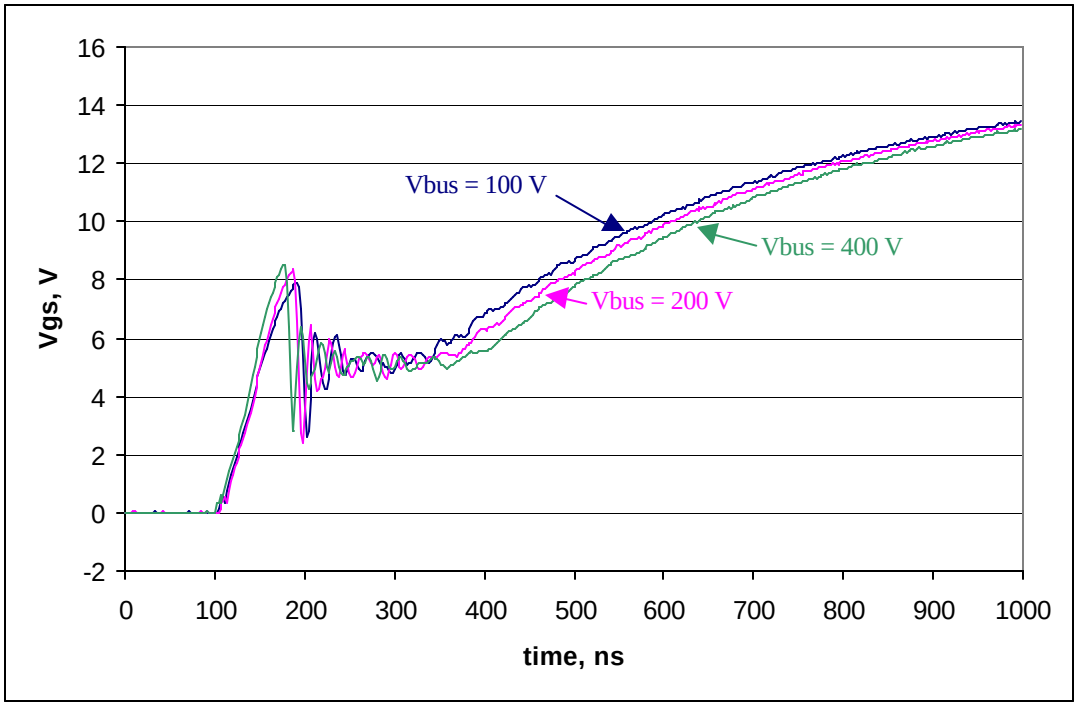

Figure 4.28. V_{gs} for different bus voltages during turn-on.

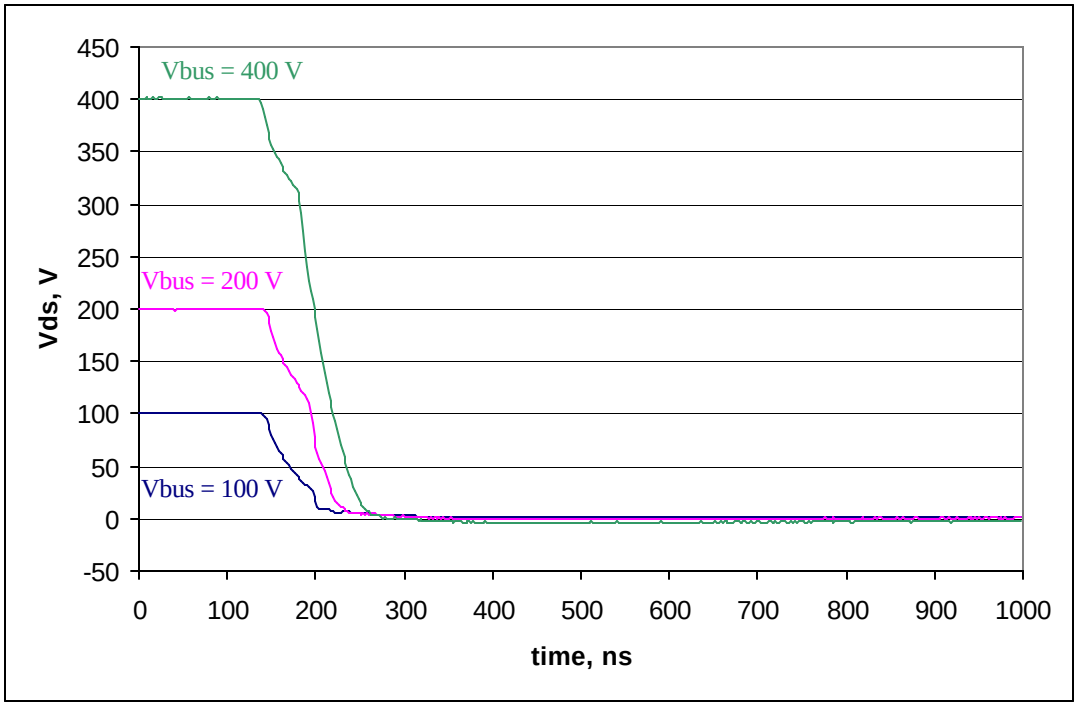

Figure 4.29. V_{ds} for different bus voltages during turn-on.

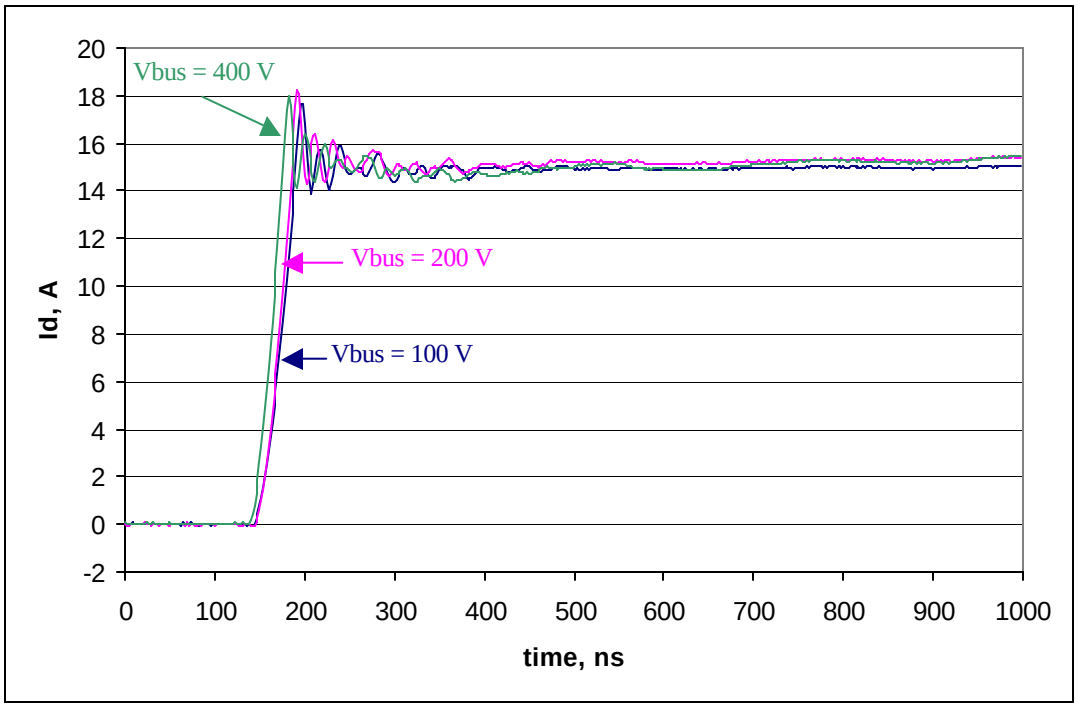

Figure 4.30. I_d for different bus voltages during turn-on.

Figures 4.31 through 4.33 show the gate voltage, drain voltage, and drain current for various values of bus voltage during the turn-off transition while all other parameters have the base values from Table 4.2. The conclusions for the turn-off are very similar to those for the turn-on with two notable exceptions. The first is that now the drain voltage rises before the drain current drops, which means that the delay caused by the increased rise time causes an increased current delay time (see Figure 4.33). The other notable factor is that, from the sensitivity analysis, we know that the drain voltage dv/dt is supposedly sensitive to the bus voltage (see Table 4.3). However, the plot in Figure 32 shows that the dv/dt is about the same for all of the values of bus voltage. The conflict here lies in the definition given for the measurement of the dv/dt. Note that dv/dt is the same for all bus voltages at a given voltage, say at 50 V. However, it is different at 50 V than at 100 V or 200 V. The definition has the measurement made at 50% of the bus voltage. The conclusion here is that while the collected data shows a change in dv/dt, there really isn't one. While the definition must be kept the same throughout the parametric study, it may need revision for the final datasheet and test procedures.

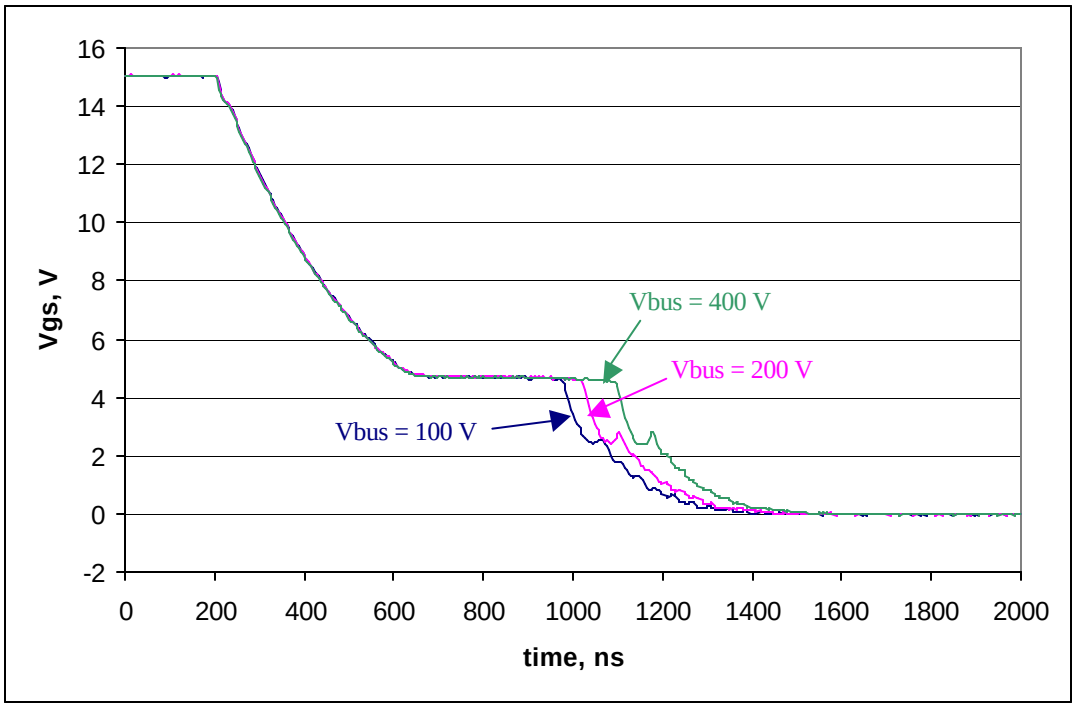

Figure 4.31. V_{gs} for different bus voltages during turn-off.

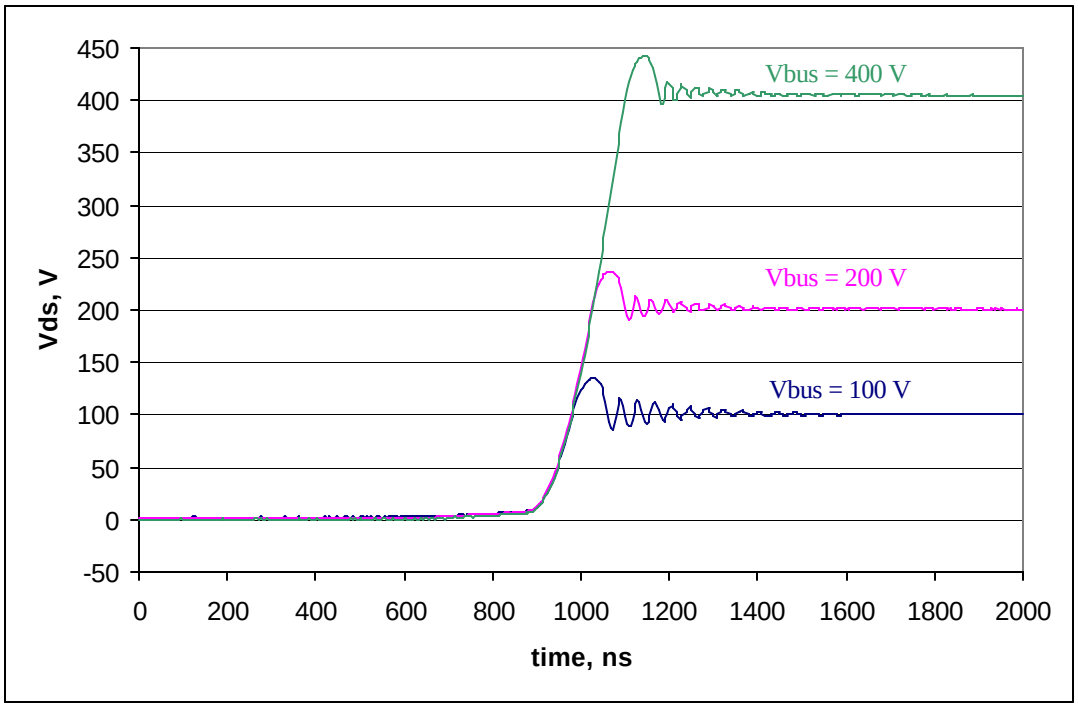

Figure 4.32. V_{ds} for different bus voltages during turn-off.

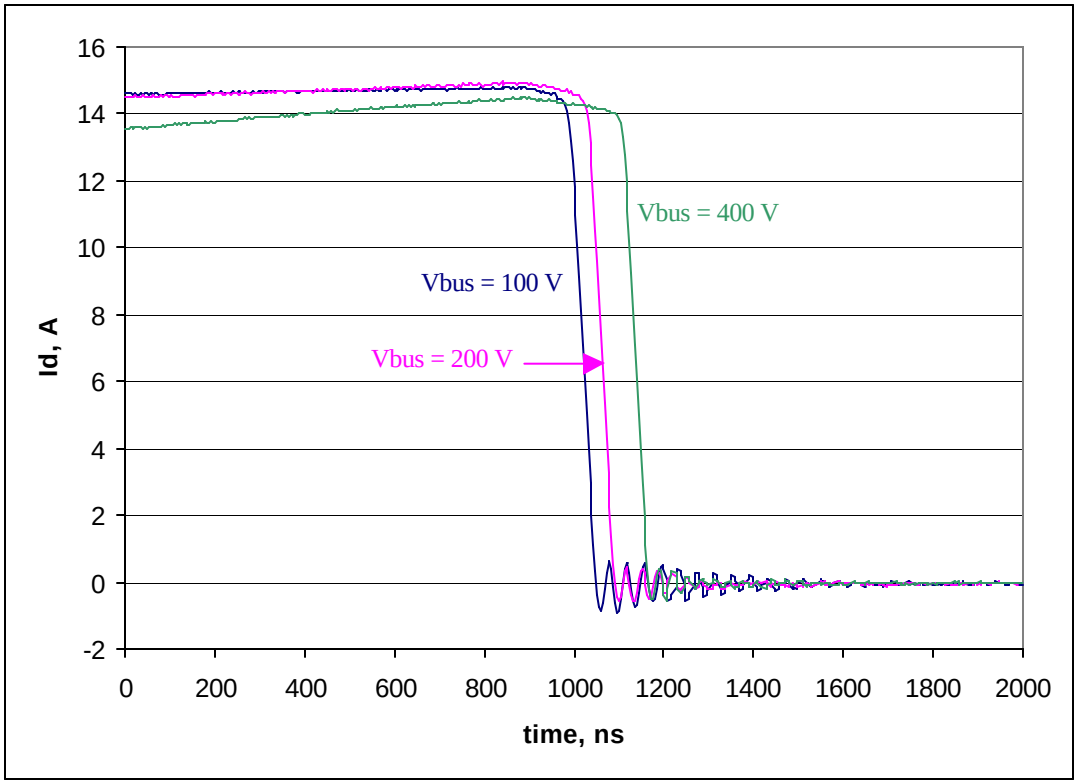

Figure 4.33. I_d for different bus voltages during turn-off.

4.7 Varying drain current

Figures 4.34 through 4.36 show the gate voltage, drain voltage, and drain current for various values of drain current during the turn-on transition while all other parameters have the base values from Table 4.2. The first thing noticed when one looks at Figure 4.34 is significant increase in the voltage spike before the plateau voltage. This is due to the increased current rise time (observable in Figure 4.36) and the parasitic inductance of the MOSFET's source pin [8]. Also note that the slope of the gate voltage during the first rising edge is the same for all three cases. Also, as discussed previously, the first falling slope of the drain voltage (Figure 4.35) is due to the drain current di/dt. This slope is also the same for all three cases. In addition, the rising slopes of the drain current for all cases lie on top of one another. So, there are three indicators that the di/dt should be the same in all cases, yet the data shows that the di/dt is sensitive to drain current "steady-state" level. The reasoning is the same as the bus voltage case, that the di/dt is constantly changing as it rises. Another notable factors are the increase in drain current rise time, which leads to increased current delay and total turn-on times. The increased rise time

and increased current magnitude also lead to significantly increased turn-on switching loss.

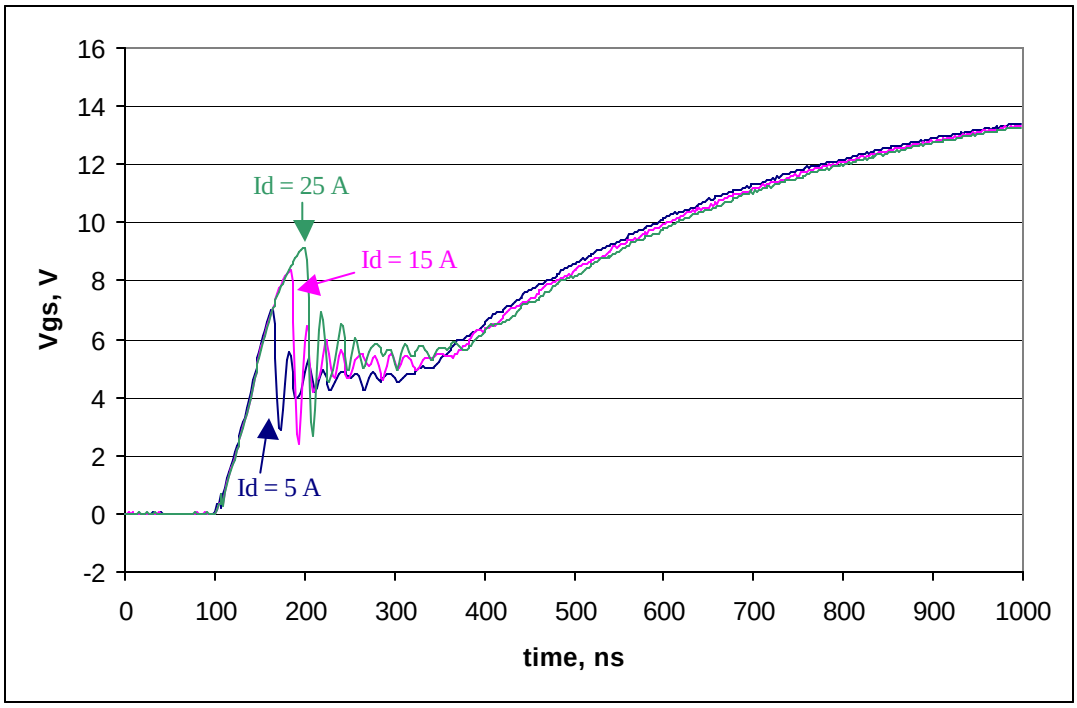

Figure 4.34. V_{gs} for different drain currents during turn-on.

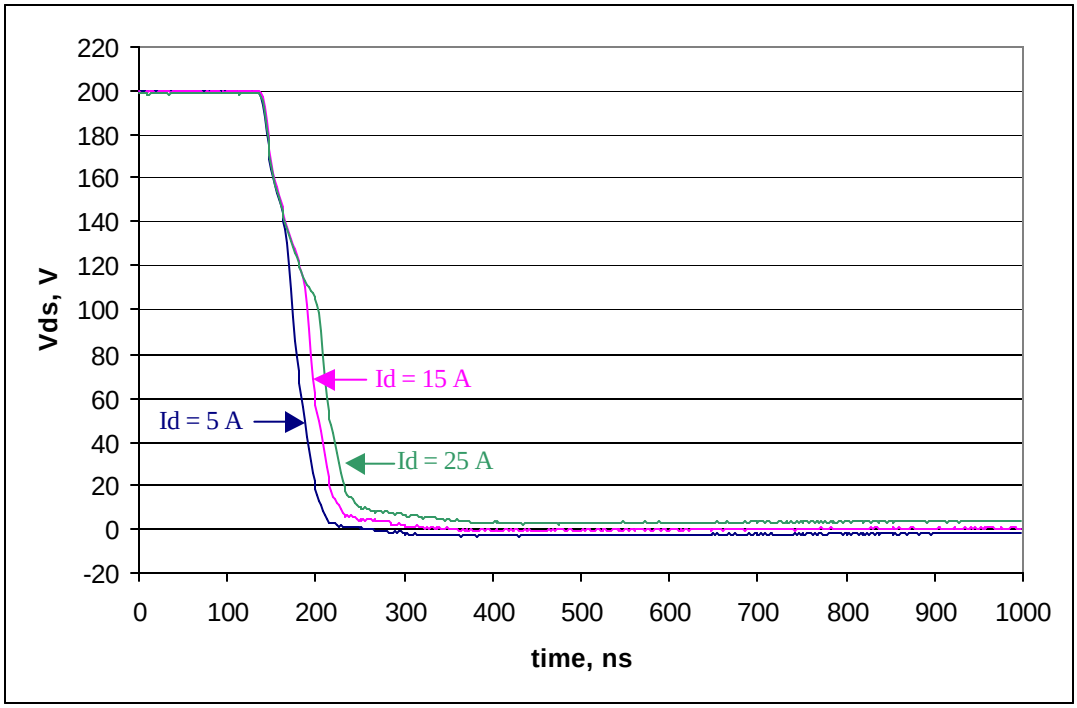

Figure 4.35. V_{ds} for different drain currents during turn-on.

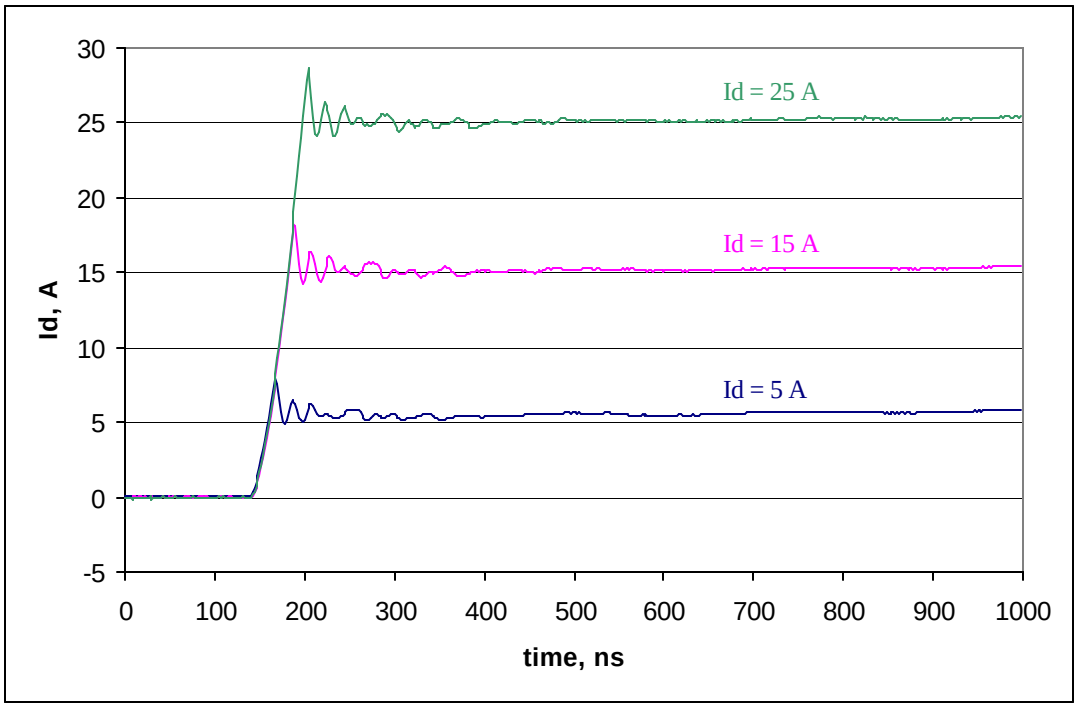

Figure 4.36. I_d for different drain currents during turn-on.

Figures 4.37 through 4.39 show the gate voltage, drain voltage, and drain current for various values of drain current during the turn-off transition while all other parameters have the base values from Table 4.2. From the gate voltage plots (Figure 4.38), note the increase in the level of the gate plateau voltage with increased current. The MOSFET resistances with higher current yield a higher plateau. From Figure 4.38, one sees that the drain voltage rise time is decreased slightly with increased current. The increased load current allows faster charging of the drain-source capacitance. The combined effects of the plateau beginning at a higher voltage and drain voltage rising faster, yield a shorter plateau (miller charging) time, which ultimately means shorter turn-off current delay and turn-off time.

Viewing Figure 4.10, one will see that the fall time is greater at 5 A than 10 A but increases for currents higher than 10 A. This is again a definition issue. Recall that current fall time is the time it takes for the drain current to fall from 90% of the nominal value to 10%. The current fall time should decrease whenever the current level is reduced (i.e. from 10 A to 5 A), but the 90% current for the 5 A case lies in the curved

part of the waveform before the steep slope (see Figure 4.39). For the 5 A case, part of the fall time includes the slowly changing portion of the waveform.

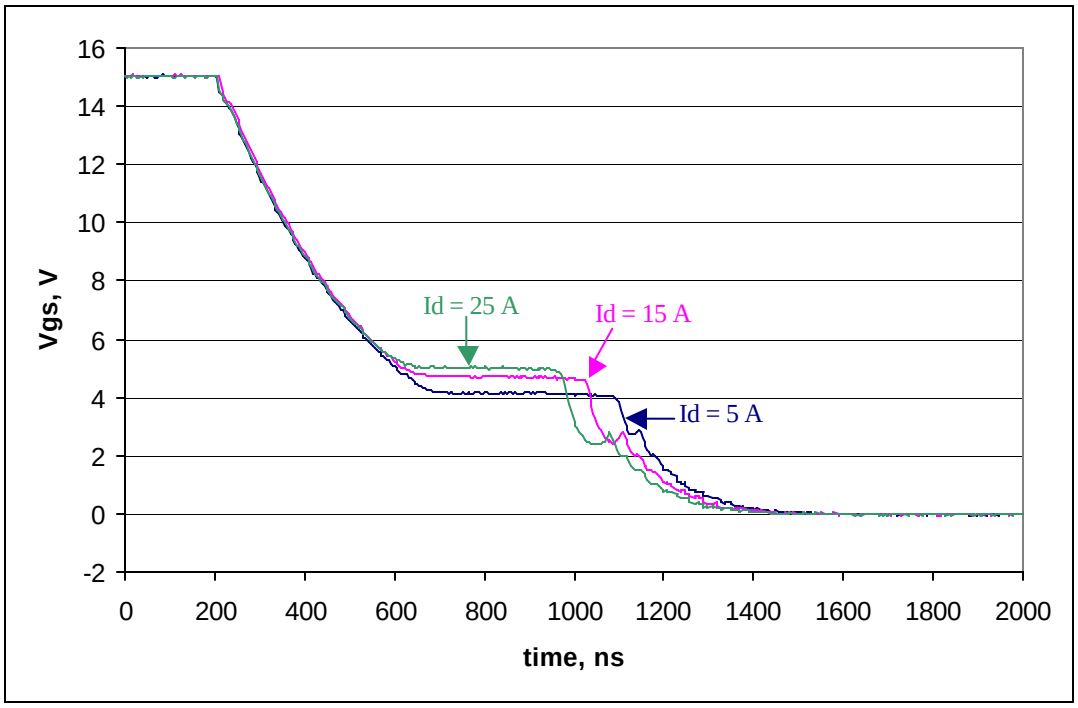

Figure 4.37. V_{gs} for different drain currents during turn-off.

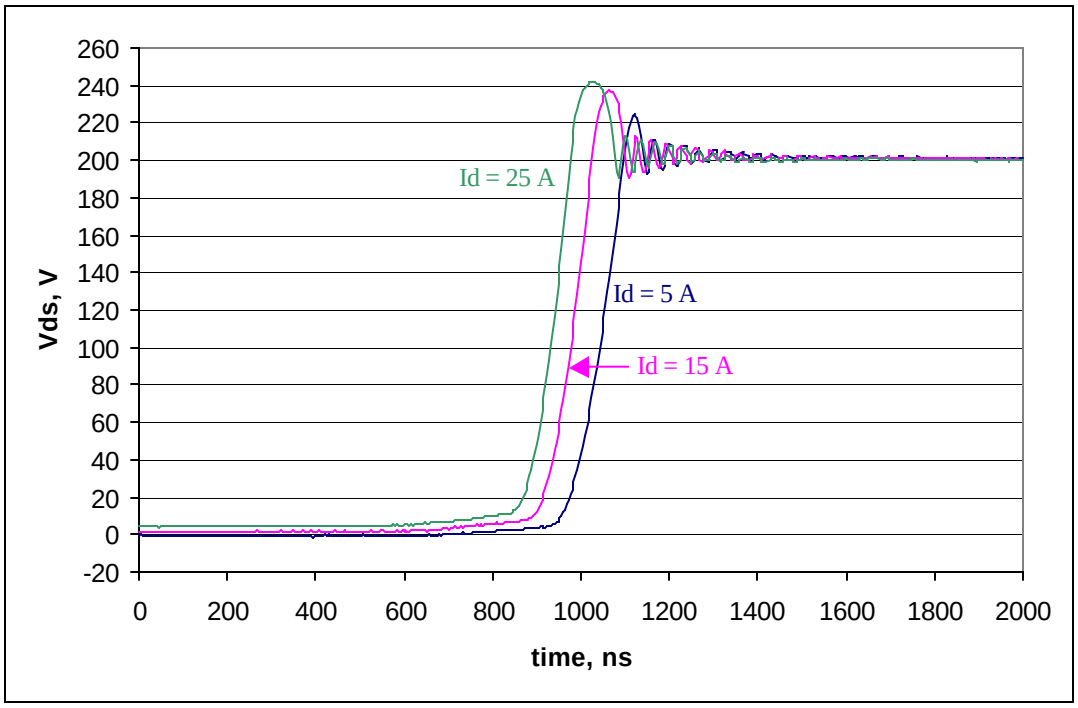

Figure 4.38. V_{ds} for different drain currents during turn-off.

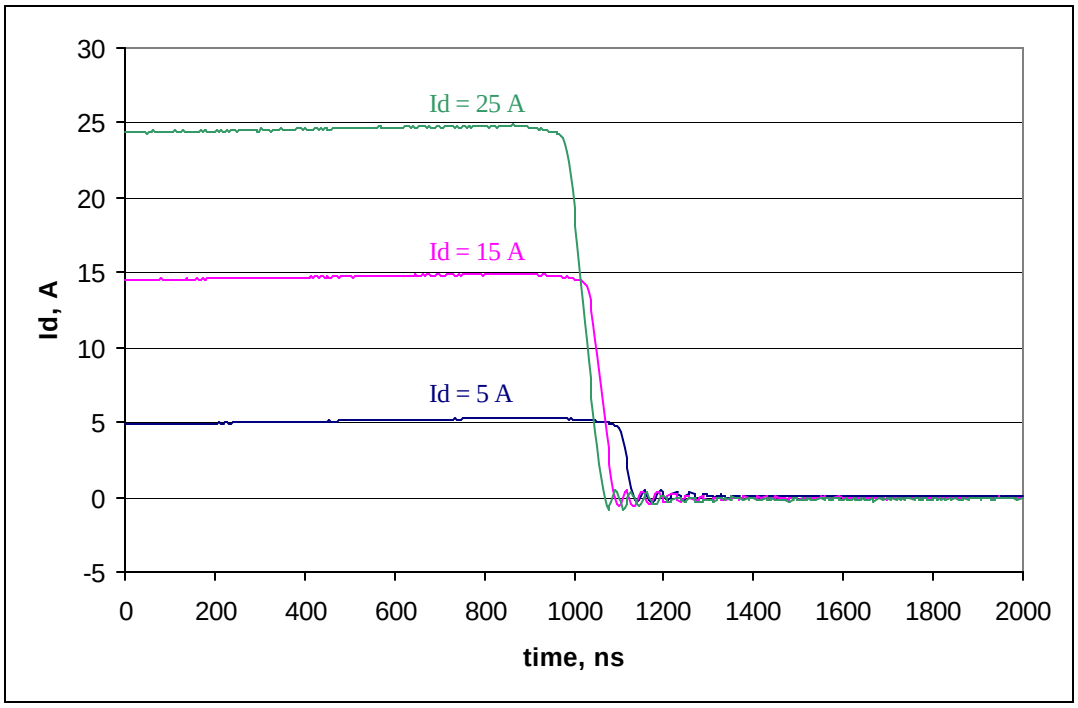

Figure 4.39. I_d for different drain currents during turn-off.

4.8 Varying bus capacitance

From the sensitivity plots and Table 4.3, it is observed that changes of bus capacitance over the chosen range (300 – 900nF) had virtually no effect on the switching characteristics. This means that the minimum capacitance of 300nF was still more than enough to adequately provide energy during switching transitions with the rest of the parameters at their base values. When building the final tester, the bus capacitance should be implemented in the same way as described in sections 3.3.2 and 3.5.5, and its effects on the switching characteristics should be tested under the worst case conditions. The worst case is the following:

1) R_g at minimum
2) V_g at maximum
3) V_{bus} at maximum
4) I_d at maximum

These conditions will give the fastest switching and highest transient energy. Loop inductance is not specified because it will not be adjustable in the final circuit. Junction

temperature effects are small, so the tests can be performed at room temperature. More detail for the design of the bus capacitance in the tester will be provided in Chapter 5.

4.9 Varying loop inductance

Figures 4.40 through 4.42 show the gate voltage, drain voltage, and drain current for various values of loop inductance during the turn-on transition while all other parameters have the base values from Table 4.2. From Figure 4.40, one can see that the initial rising edge before the threshold voltage is the same for all cases. The effects of the loop inductance begin to become noticeable after the threshold voltage when current begins to rise. From Figure 4.42, one can see that the loop inductance serves to limit the di/dt. The reduced di/dt decreases the voltage spike measured on the gate voltage that occurs just prior to the plateau voltage. This voltage spike occurs due to the MOSFET source pin parasitic inductance [8]. While L_{LOOP} increases by five times, the di/dt reduction is a much smaller factor. This can be observed from the drain voltage falling edge (Figure 4.41). As long as the current is rising, the drain voltage will fall due to the L*di/dt voltage drop across the loop inductance. While di/dt is reduced, the L*di/dt voltage drop is still increased because the loop inductance is increased by more than the di/dt is reduced. This voltage drop will result in less overlap of the drain voltage and current, ultimately leading to reduced turn-on switching energy loss. Another observation from Figure 4.42 is that while increasing L_{LOOP} slows the drain current's rising edge, the current overshoot increases. It seems counterintuitive that reduced switching speed should increase stress. In all cases, when the drain current reaches the load inductor current, the SiC Schottky begins to block voltage. However, in the 250 nH case, the loop inductance holds 5 times as much energy at that instant than in the 50 nH case.

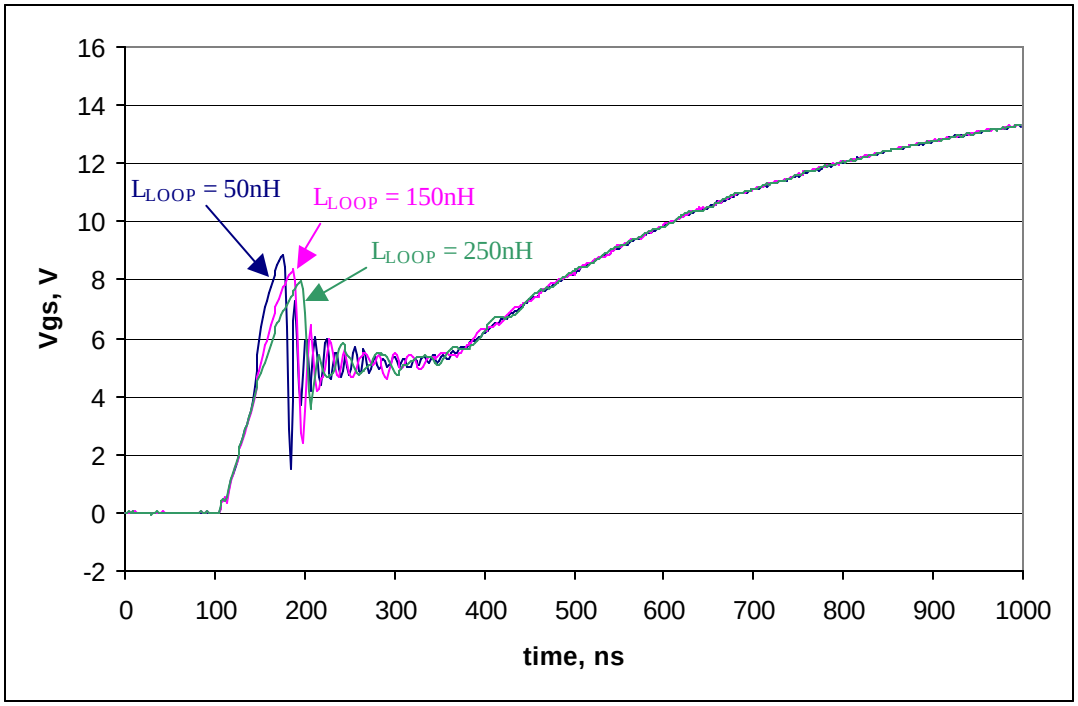

Figure 4.40. V_{gs} for different loop inductances during turn-on.

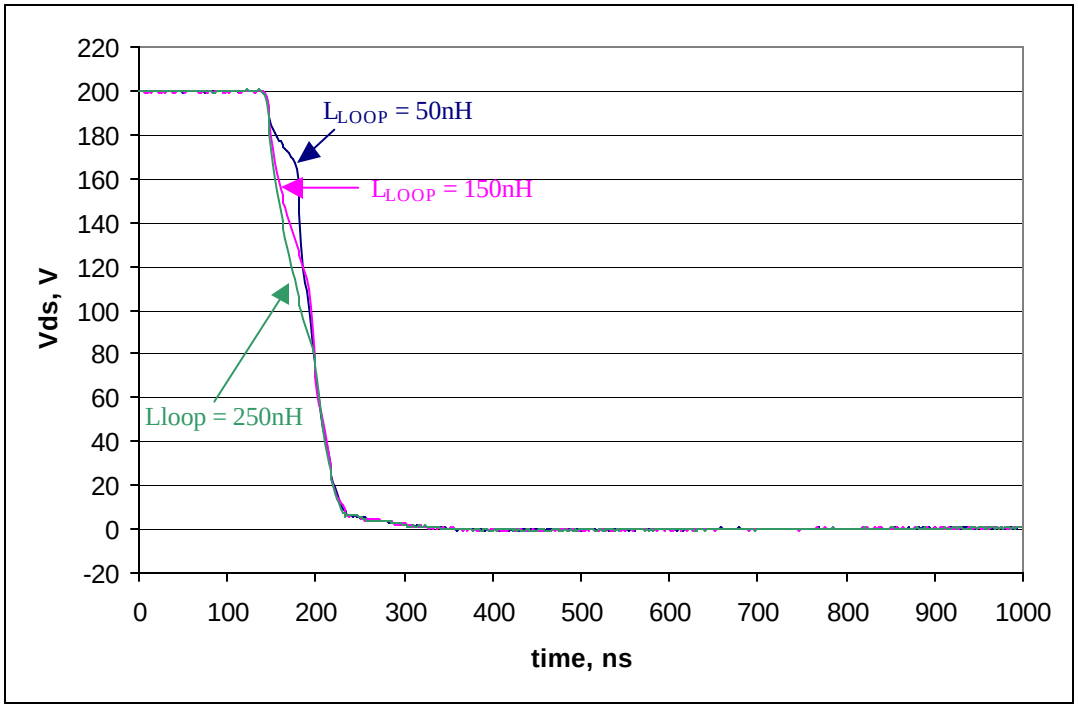

Figure 4.41. V_{ds} for different loop inductances during turn-on.

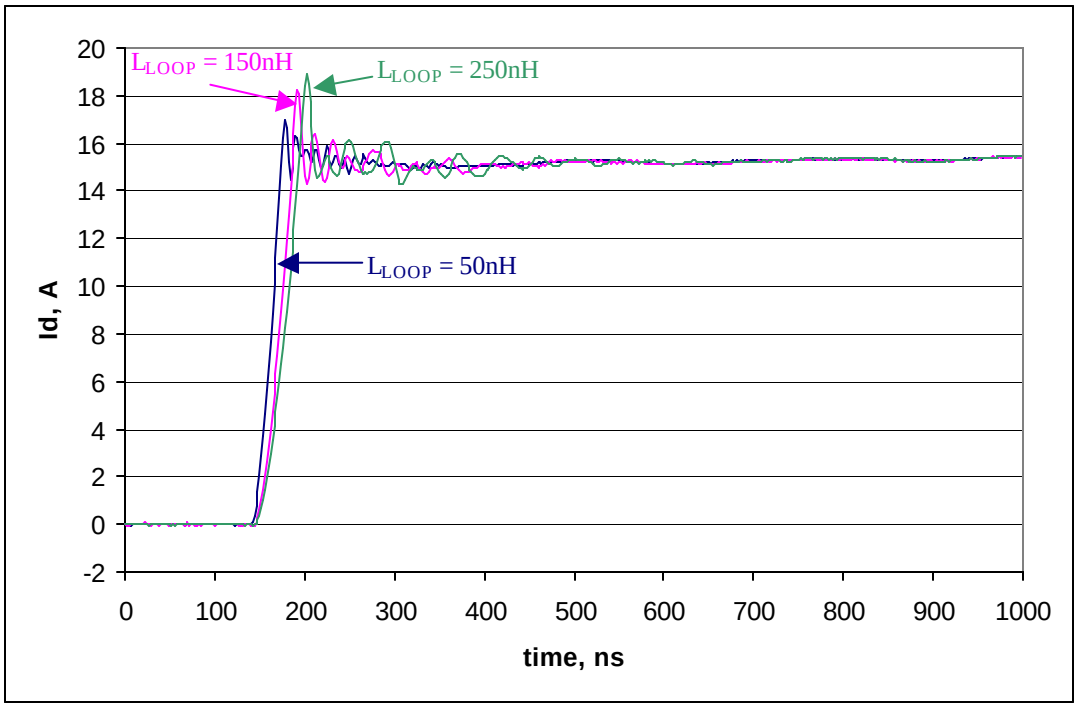

Figure 4.42. I_d for different loop inductances during turn-on.

Figures 4.40 through 4.42 show the gate voltage, drain voltage, and drain current for various values of loop inductance during the turn-off transition while all other parameters have the base values from Table 4.2. The most notable trend is the L*di/dt drain-source's overshoot voltage. In addition, there is a slightly increased current fall time. The result of these two factors will also show increased turn-off energy.

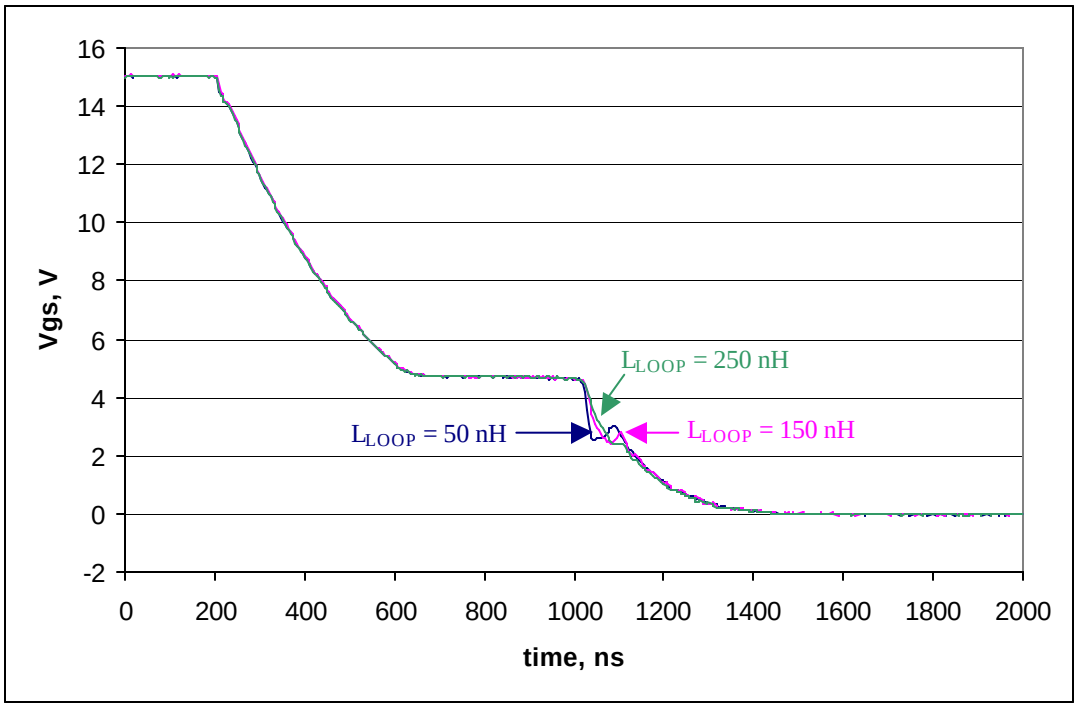

Figure 4.43. V_{gs} for different loop inductances during turn-off.

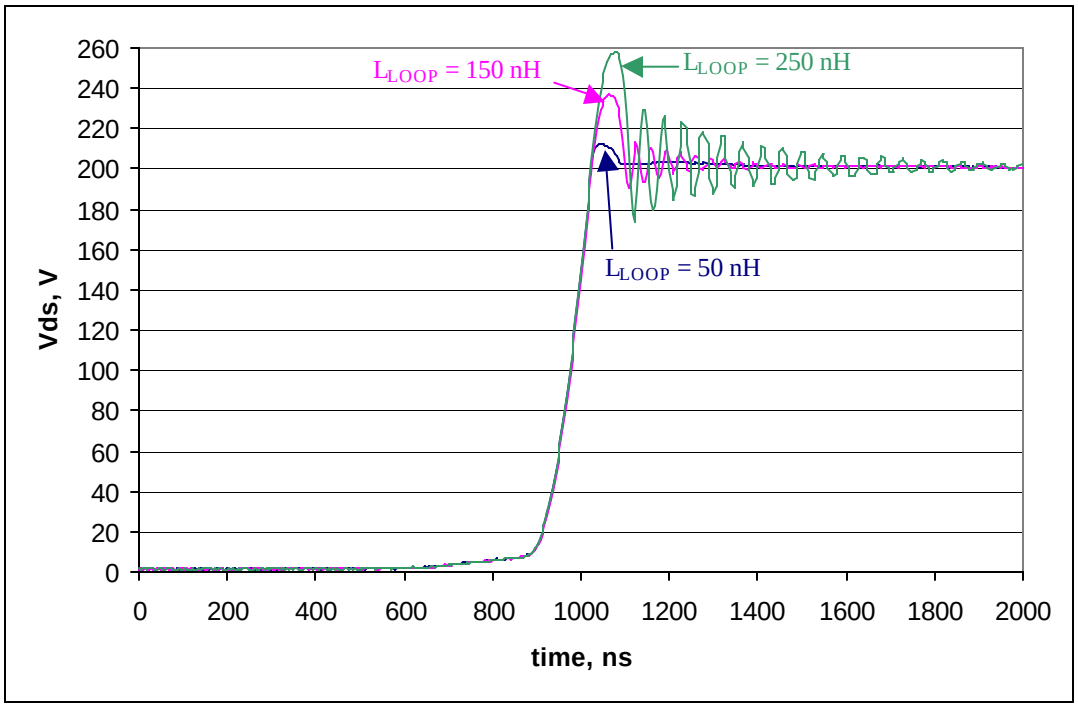

Figure 4.44. V_{ds} for different loop inductances during turn-off.

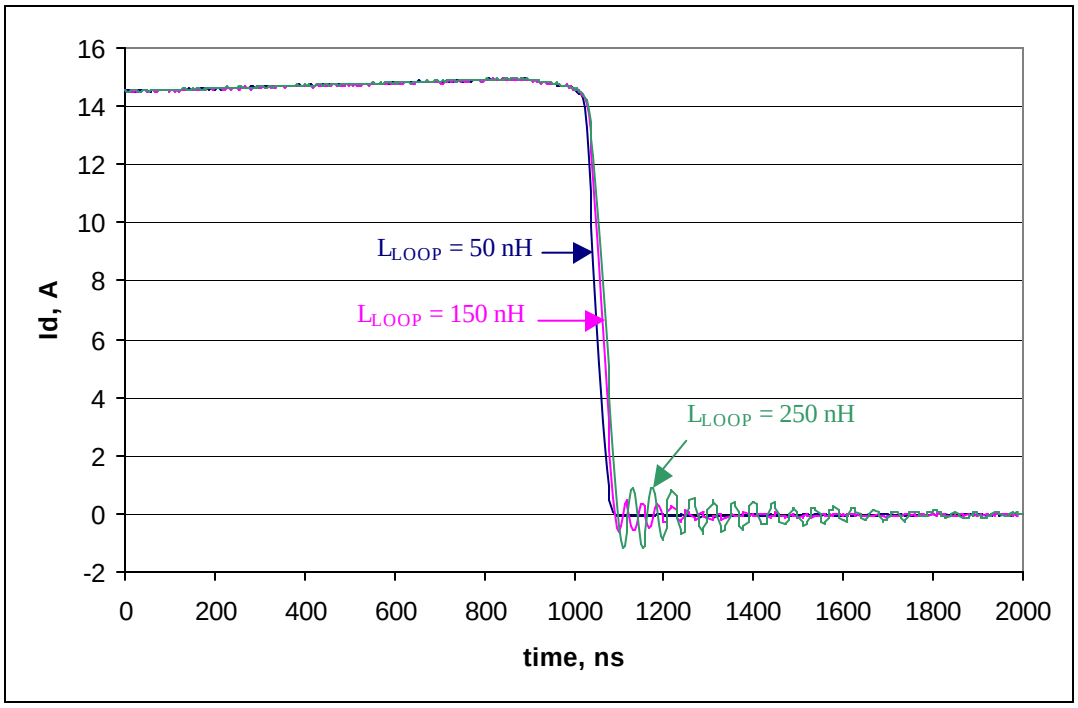

Figure 4.45. I_d for different loop inductances during turn-off.

4.10 Varying junction temperature

From the sensitivity plots and Table 4.3, it is observed that the switching characteristics do not vary greatly over the chosen range of junction temperatures (25 – 100°C). Though the trends were very small, their shapes were undeniably consistent (refer to Appendix D). In other words, the data were not merely random measurement error around a zero-change trend line.

Another note that should be made is that the tests were conducted only for a power MOSFET. While changes in the other varied parameters are expected to show similar trends for IGBTs as for power MOSFETs, the junction temperature is expected to show quite different trends. Increases in junction temperature in an IGBT increases minority carrier lifetime, which leads to lengthier current tail times [33]. The result is that the junction temperature will have significant effects on the turn-off time and losses.

Chapter 5 – Final Tester design

5.1 Introduction

The combined knowledge and data from the previous chapters form the methodology needed to design the power device/module switching characteristics tester. Chapter 2 demonstrated the crucial measurement considerations involved in obtaining accurate switching characteristics data. Chapter 3 introduced the experimental setup for a parametric study that explores the effect of several important circuit parameters on the measured switching characteristics. Chapter 4 gave the results of the parametric study, highlighting the sensitivity of each switching characteristic to the varied parameters and explaining qualitatively the reasons for the noted trends. This chapter provides the guidelines for designing a switching characteristics tester and determining the necessary information to include in a module datasheet. This chapter specifically addresses the following questions:

1) What are the necessary measurement specifications?
2) Which tester parameters need to be specified in the datasheet?
3) At what operating conditions (I_d, V_{bus}, and T_j) should the module be tested at?
4) How should the gate drive parameters (R_g, V_g) be chosen?
5) How should the tester layout be designed?

Though the primary concern in this thesis is extraction of the switching characteristics defined in Chapter 1, verification of module operation under continuous-pulse operation is important. By testing continuous-pulse operation, we can confirm that the module functions properly near rated voltage and current while being heated internally due to power losses. In addition, the final tester design includes power supplies, gate drivers, signal generators, and control circuitry. A basic description of the whole tester is given in section 5.4, and the detailed design of the tester is given in Appendix E. Section 5.5 focuses on the testbed that interfaces the IPEM or device and the board that interfaces the testbed to the rest of the tester.

5.2 Tester Measurement Specifications

From the measured data, it is found that the minimum rise or fall times for both the current and voltage are 10 ns. Of course, this is the measured value rather than the true value. One could argue that if the voltage or current probes used did not have sufficient bandwidth, the measured times may be longer than the actual times. The voltage and current measurements can be dealt with individually.

The voltage probe and oscilloscope combination were specified to have a system bandwidth of 500 MHz. Using Equation 2.2, a signal with a rise time of 5 ns has a rising edge equivalent frequency of 50 MHz. So that both the magnitude and phase of the rising edge are not appreciably distorted, the system bandwidth for measuring this signal should be 500 MHz or greater. The implication here is that since the voltage measurement system bandwidth can faithfully represent signals significantly faster than the one observed, one can trust measurement. As the measured rise time gets closer to 5ns, one should begin to question the correctness of the measurement.

In Chapter 2, it was demonstrated that improvement in voltage measurement could be achieved by reducing the probe tip-to-ground loop. To this end, probe-tip adaptors were used for the parametric study, and they should be used in the final tester design. Note that these adaptors must be physically close to the DUT in order to correctly represent the waveform.

The current measurement is not quite so straightforward. As discussed in Chapter 2, the original shunt used had a high bandwidth specification (400 MHz), but it had significant error even for relatively slow rising edges. The problem seemed to be the small inductance associated with loop around the air gap (see Figure 2.12). A new shunt was implemented which had a bandwidth specification of 2 GHz. Chapter 2 demonstrated that the current measurement could be and was validated using a few key observations from the measured waveform and from the measurement's good agreement with simulation.

5.3 Tester Parameters

Gate drive parameters: R_g, V_g, and gate driver used (gate drive impedance)

The sensitivity analysis of the parametric study showed that the gate drive voltage and resistance dominate the trends of most of the switching characteristics. The gate voltage and resistance will be specified in the IPEM's datasheet. As converter switching frequencies continue to increase, gate resistance values with which devices are tested continue to decrease. Typical R_g values used today are as low as 2Ω [29], which is in a similar range of impedance as the output impedance of many gate driver ICs. For this reason, it is important to also specify the gate driver chip's output impedance in the datasheet. The output impedances of many gate drivers are provided in the chip's datasheet. If this information is not readily available, it can be easily determined as follows:

1) Place a capacitor across the output of the driver with a low value coaxial shunt placed inside the loop for current measurement.
2) Switch the driver on and off, and measure the peak current obtained.
3) The output impedance is the driver output voltage divided by the peak current measured.

Junction Temperature

Though the junction temperature will have significant effects on conduction losses, it was observed to have a minimal effect on the switching characteristics compared to the other parameters. The ultimate conclusion is that it is sufficient to test power MOSFET modules only at room temperature. The conclusion for IGBTs should be quite different. The IGBT's turn-off characteristics are expected to change significantly with temperature junction temperature [33]. The switching characteristics should be tested at room temperature and 100 °C or 125 °C for IGBTs.

Drain Current

From the parametric study, it is observed that the drain current has a significant effect on several of the switching characteristics. In addition, a given converter (and therefore module), could supply a wide range of currents. For these reasons, the IPEM datasheet plots will show the effects of load current on the switching characteristics for currents ranging from 20% to 100% of the device current rating.

Bus Voltage (or voltage across the DUT)

The voltage applied across the device also showed significant effects on the switching characteristics. The operating voltage will change depending on the application, and some applications have the devices operating at different voltages over a line cycle. The conclusion is that for some modules (depending on target applications), the characteristics need to be tested for several voltage values. How many voltages the datasheet provides information for will be dealt with on a case-by-case basis. For modules that are tested with more than one voltage level, one curve showing the trends for changing load current will be given for each voltage level.

Loop Inductance

The loop inductance had a significant influence on current rise times, device stresses, and switching energy. As such, the layout of the tester with respect to this parameter should be given special attention. L_{LOOP} should be made small to ensure that devices do not fail due to voltage overshoot. It should also be kept small so that improvements in module layout can be observed from the switching waveforms. Because this parameter has so much impact, it is important to specify the amount of loop inductance associated with the tester layout. By knowing the relative inductance of the tester and module and the general trends of L_{LOOP} on the switching characteristics, we can draw inferences on the amount of the improvement of one module layout compared to another.

5.4 The Tester

Figure 5.1 below shows the block diagram of the tester. The high voltage DC supply (HVDC) enters the tester through a common-mode choke for the reasons discussed in section 2.4.1. An external programmable signal generator's signals (SigGen) and 120 VAC power (HVAC) also enter the tester and are connected to the backplane. The backplane makes the necessary connections between the other boards. The 120 VAC bus is used to supply two power supply boards. Power Supply 1 provides ±12 V for relay controls and +5 V for logic circuitry on the Control Board. Power Supply 2 provides two +15 V supplies for use on the Gate Driver Board. The Control Board determines what signal continues to the Gate Driver Board. Using switches on the Front Panel, the user can choose between 0-5 V logic and 0-15 V logic and can choose between tests to perform (double-pulse top device, double-pulse bottom device, and continuous-pulse test). Using a switch on the Front Panel, the user can also choose to use one of the load inductors from the Load Board or to use an inductor that they supply. The user-supplied load is connected to the banana plug jacks on the Front Panel. The inductor load current (I_L) is measured at the Load Board using a high bandwidth current transformer (Pearson Model 411). The coaxial output of the current transformer is available at the Front Panel. The Gate Driver board contains two independent gate drivers and is capable of driving a half-bridge. The Power Board and Testbed are described in more detail in section 5.5.

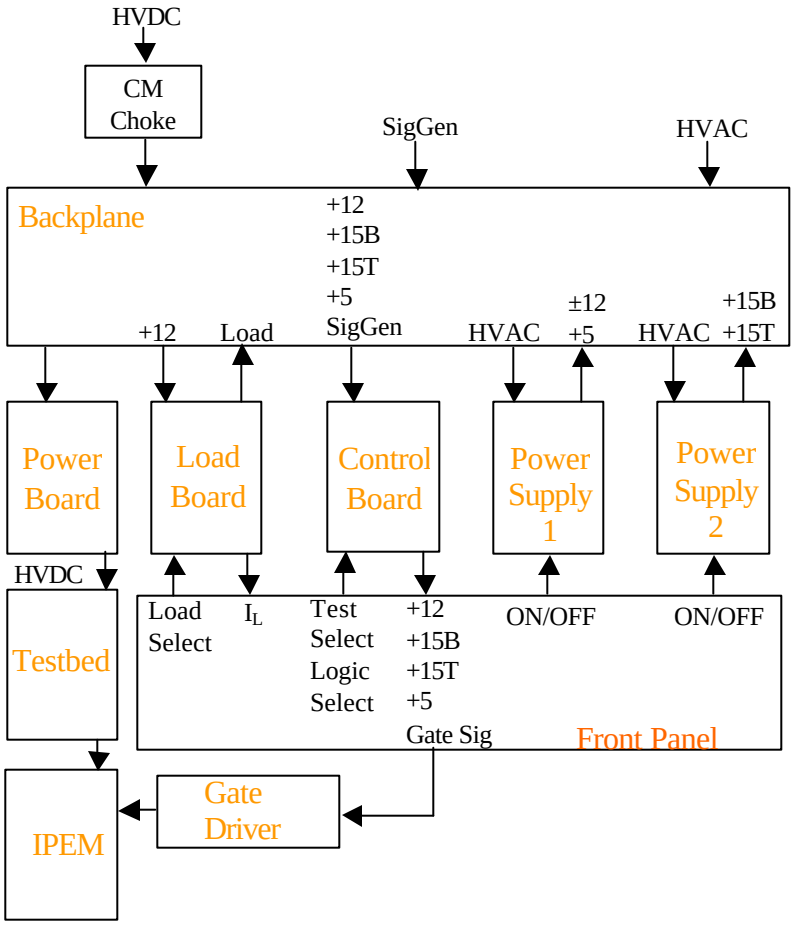

Figure 5.1. Tester block diagram.

5.5 Main Testbed

IPEMs come in a wide variety of topologies, depending on the target applications and the level of integration. The tester designed within this thesis work is intended for half-bridge modules, but also has the proper provisions to be able to test discrete power MOSFETs and IGBTs. Figure 5.2 below shows the topology of the Main Testbed (Testbed and Power Board). If testing a module, pins P, O and N from the module would be connected to the corresponding points of the tester. If testing a discrete power MOSFET or IGBT, the device would be connected across points O and N of the tester. Note the various configurations of the tester that are possible. Table 5.1 gives the

necessary connection schemes for evaluating the top switch, top diode, bottom switch, and bottom diode.

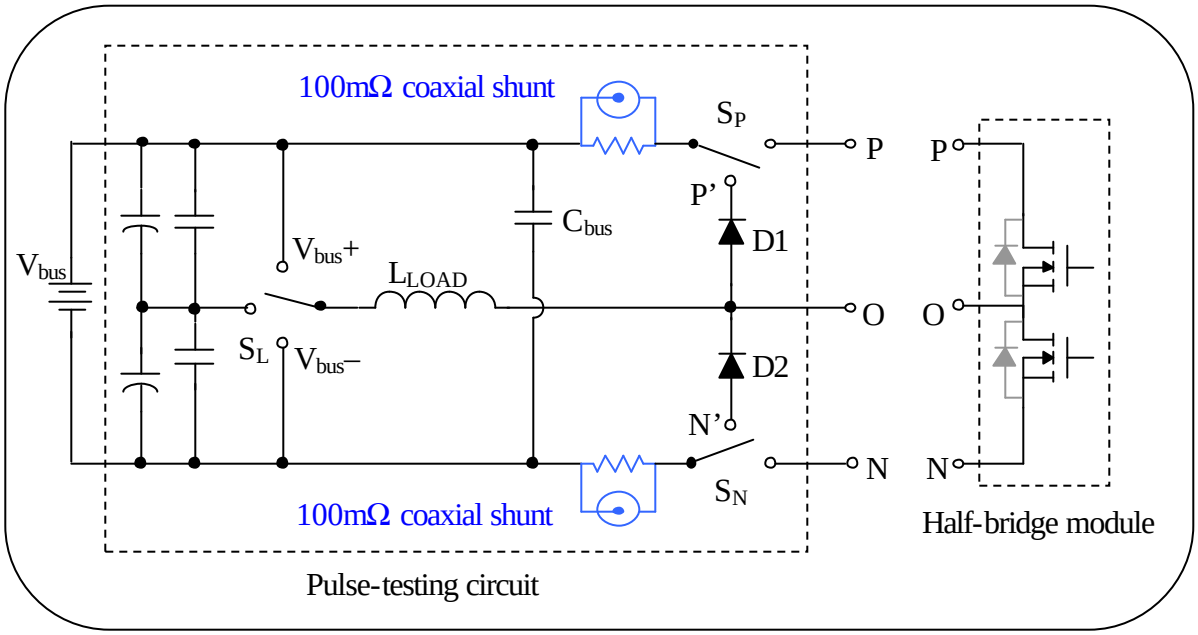

Figure 5.2. Testbed for double-pulse and continuous-pulse testing.

Table 5.1. Tester configurations.

	Top Switch	Top Diode	Bottom Switch	Bottom Diode	Discrete MOSFET	Discrete IGBT
SP	P	P	P'	P	P'	P'
SN	N'	N	N	N	N	N' and N
SL	Vbus-	Vbus+	Vbus+	Vbus-	Vbus+	Vbus+

Figure 5.3 shows the layout of the main testbed. The top two figures show the top and bottom layers of the testbed that interface the IPEM. The pin-outs labeled P, P', O, N, and N' are the same as those of Figure 5.2 above. As this board contains the loop associated with L_{LOOP}, the layout of this board is critical. Note the use of several bus capacitors and that the capacitors are mounted very close to one another. They can be placed so close because adjacent capacitors are mounted on opposite sides of the board. The shunts are placed as close as possible to the bus capacitors, and the diodes are made as near to the shunts as possible while still allowing adjustment of the connection scheme. The clamping screws in conjunction with small PCBs with copper planes are used to make connections as described by Table 5.1. Small shorting clamps are used instead of relays to ensure low inductance connections. Also note that P and N' as well

as P' and N are paired as parallel planes. For most of the double-pulse testing, external SiC Schottky diodes will be used in order to reduce the reverse recovery effect on the switching characteristics. The configurations paired as parallel planes correspond to the use of the external diodes. This is done to reduce the effective parasitic loop inductance. The hole shown is so that the connections between the two circuit boards shown can be made.

Connection between the testbed and IPEM is done using another PCB clamp. This clamp is intended to connect the planes of the testbed to the planes of an adaptor board that is made specifically for the IPEM being tested. The adaptor board/clamp combination is chosen for two reasons. An adaptor board with plane connections will have less parasitic inductance than wire connections, and the adaptor board allows mounting of probe-tip adaptors very near the DUT.

The bottom figure of the three displays the board containing the bulk capacitors, control of inductor connection (S_L), and the interface with the rest of the tester. This board does not contain layout parameters that are critical for switching waveform measurements, so its design can be done more loosely.

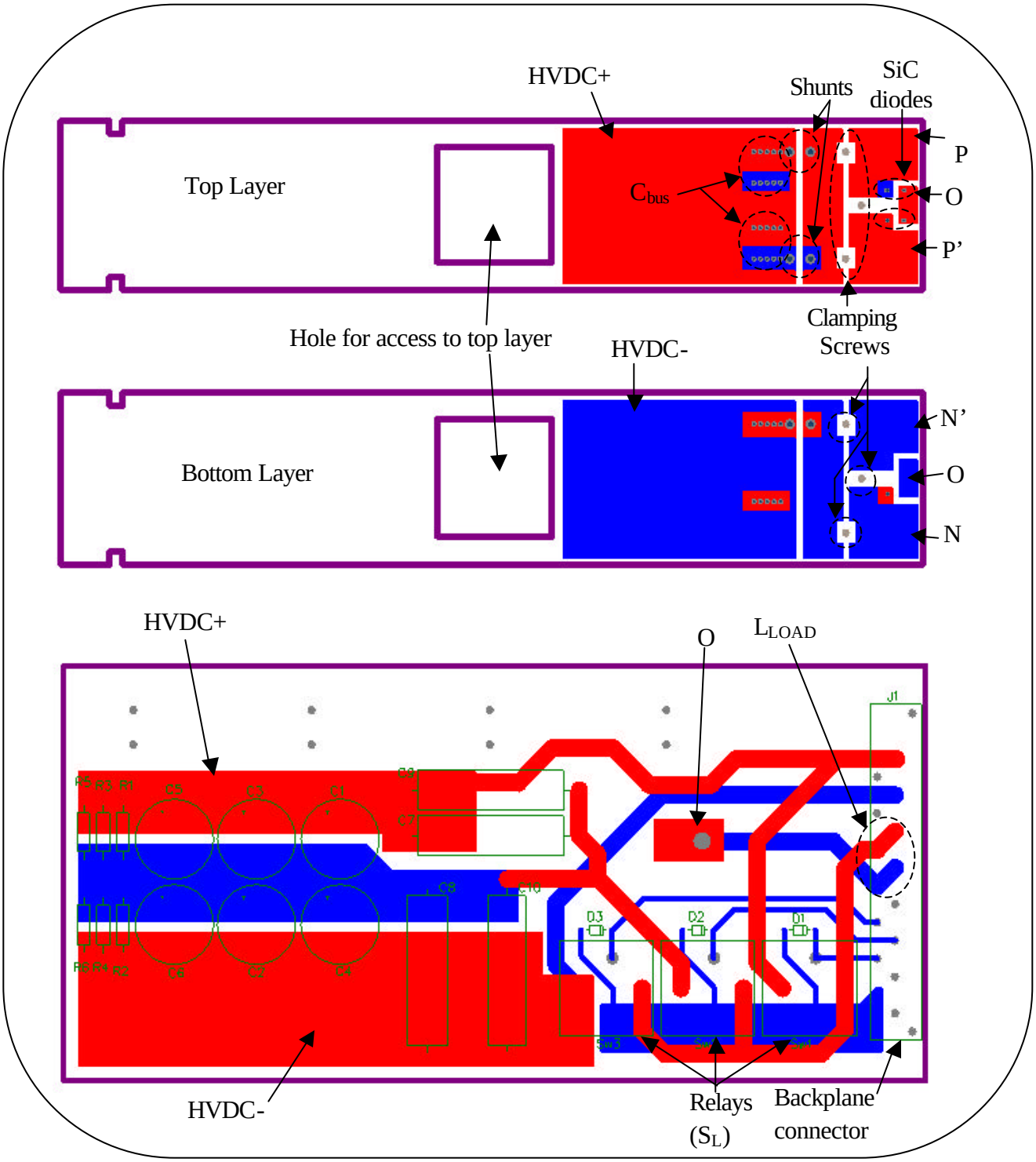

Figure 5.3. Main testbed circuit boards.

Chapter 6 – Conclusions and Future Work

6.1 Conclusions

It has been well established that characterizing an IPEM with respect to its switching characteristics is an important endeavor. For this reason, this thesis has investigated the methods for doing this characterization.

The measurement equipment related problems were addressed. Capacitively-coupled ground loops can be created due to the bus voltage supply's capacitance to earth ground. The consequence of this ground loop manifested as common-mode ringing in the shunt current measurement. The problem is handled using an appropriate common-mode choke. It was found that much of the ringing originally observed from the voltage measurements could be attributed to the probe's tip-to-ground loop inductance. This issue could be solved using probe-tip adaptors that limit the loop to a length barely longer than the tip of the probe and allow direct plugging of the probe into the circuit board.

Several types of voltage and current probes were considered, and it was concluded that the 10X passive, grounded voltage probes and coaxial current shunts were the only set that could adequately measure fast switching waveforms. It was also demonstrated that not all shunts are made equal. The first shunt used showed faster rise times, odd shapes, and much larger current stresses than expected. This was the result of a small amount of inductance formed by the air gap between the concentric cylinders of the coaxial shunt. The problem could be alleviated by using a shunt with larger resistance and a better construction (smaller air gap loop).

A parametric study was performed to determine the sensitivity of the switching characteristics to several circuit parameters, including: gate resistance, gate voltage, bus voltage, drain current, loop inductance, bus capacitance, and junction temperature. By normalizing the varied parameters around their base values and plotting the relative effects of all parameters on a single plot, one can fairly analyze which circuit parameters and operating conditions most affect each characteristic. Overall, it was noted that the gate drive parameters (R_g and V_g) had the greatest effect on most of the switching

characteristics. Loop inductance, bus voltage, and drain current also showed significant changes, while the bus capacitance and junction temperature seemed to have very little effect.

From these sensitivity plots, one can also see some correlation between the effects of the varied parameters. For example, the turn-on switching interval times are significantly reduced by either decreasing R_g or increasing V_g. The conclusion is that it is the gate current (V_g/R_g) that truly determines these switching times. Strong correlation is also noticeable amongst some of the switching characteristics. Note that the shapes of the curves and the sensitivity values in Table 4.3 are very similar for the voltage overshoot (V_{OS}) and the turn-off switching current gradient (di/dt(off)) when the loop inductance is held constant.

Some of the general trends from the parametric study have been known for quite a long time. For instance, knowledgeable engineers understand that increasing gate resistance reduces switching speed and loop inductance has an adverse effect on voltage stress. However, this thesis does more than generalize. The sensitivity plots and Table 4.3 quantify the effects of fore-mentioned parameters in such a way that comparisons can be made and correlations can be deduced. This study is also more complete in that it explores the effects of each parameter on several switching characteristics instead of just one or two characteristics.

Circuit modeling attempts, including layout and component parasitics modeling, were made with fairly good success. The waveforms simulated were very similar to those in measurement and most of the trends from measurement could be duplicated. The simulation circuit proved to be a valuable tool in finding measurement errors. The simulation circuit could also be used to see measurements that cannot be extracted from the real circuit.

To fairly analyze a module's performance and make comparisons amongst designs, it is imperative to use standard test equipment and test procedures. To this end, a hard-switching characteristics tester is designed and the measurement procedure has been demonstrated. From the parametric study and investigation of measurement needs, the following general observations should be noted for the testing of IPEMs:

1) Switching characteristics are very sensitive to the loop inductance. As such, the tester layout should be designed carefully and the parasitic inductance should be specified in the IPEM datasheet.
2) The bandwidth of a measurement must be specified as a system bandwidth.
3) The equivalent frequency of a given signal's rising edge can be calculated to determine if the measurement system bandwidth is questionable or inadequate.
4) The gate driver output impedance should be specified in the datasheet.
5) The gate drive should be connected in such a way as to not increase the source (or emitter) pin parasitic inductance.
6) Probe-tip adaptors should be used to reduce errors in the voltage measurements.
7) The reverse recovery charge of the freewheeling diode can be used to verify the current measurement.

6.2 Suggestions for future work

1) The sensitivity plots in Chapter 4 should be further analyzed. While some conclusions have been drawn from the parametric study, it is believed by this author that many more useful trends and conclusions may be deduced.

2) The choice of where in the drain voltage and drain current waveforms to measure the dv/dt and di/dt (currently measured at 50%) could use further analysis. One of the primary reasons for specifying these values is that these gradients have implications on electromagnetic interference. To improve the meaningfulness of the measurements of dv/dt and di/dt, it would be useful to discern if it is the average gradient, maximum gradient, or other measurement that most lends itself to the analyzing IPEM EMI performance.

3) The work in this thesis deals solely with hard-switching characteristics. However, some modules may be intended for soft-switching operation, or may at least be well suited to a particular soft-switching application. An example may be a ZVS tester such

as shown in Figure 6.1 below. The tester could also be extended for ZCS. In any case, the principles outlined in this thesis for hard-switching could be directly applied to soft-switching testers [34].

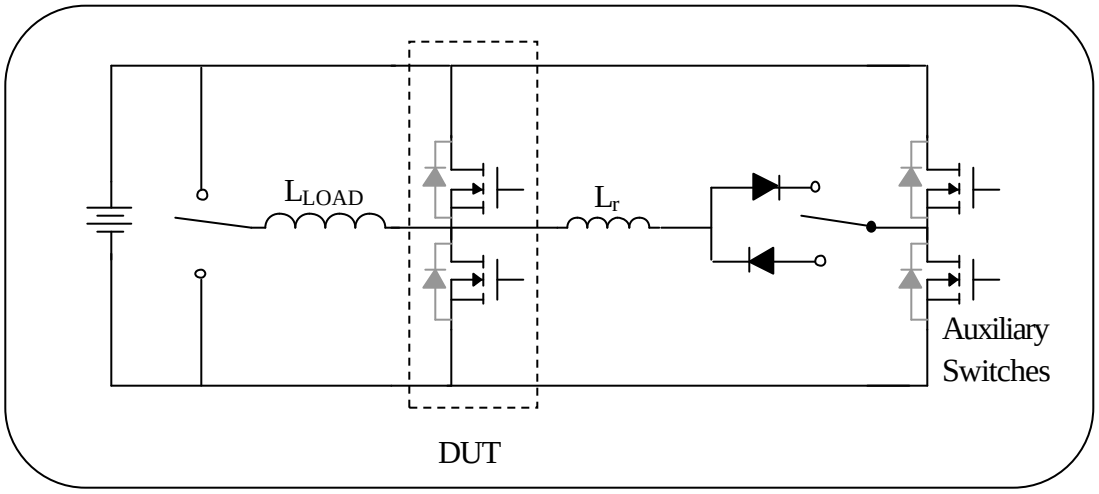

Figure 6.1. ZVS tester circuit.

4) Discrepancies between the simulated and measured results should be studied further. It is believed that the MOSFET capacitance models may be part of the problem. While the simulation model capacitance curves were similar to those from the MOSFET datasheet, they were not the same. Also, the capacitance curves do not extend beyond V_{ds} values greater than 25 V, so it is difficult to tell how well the matching is for higher voltage biases.

5) The tester should be constructed using the information provided in Appendix E and the general guidelines developed in this thesis.

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Appendix A – Pulse-width Distortion and Phase Lag

As mentioned in Chapter 1, the switching delay times can cause considerable pulse-width distortion and phase delay. Figure A.1 below demonstrates these phenomena. The thin trace in the V_{gs} plot is the control signal from the signal generator or processor. The thin lines in the plots of V_{ds} and I_d show the expected pulses if you had perfect switches with no delay. The thick lines show the actual voltages and current. Note from the plots the increased duration of the I_d pulse and the decreased duration of the V_{ds} pulse. This means that the device is actually on longer than expected. This pulse-width distortion may lead to an incorrect voltage or current at the output of the converter. The control loop may or may not be able to compensate for this distortion, depending on how close the duty cycle is to its boundaries. Also, if there are multiple switches in the circuit and a device is on when it is expected to be off, other devices may be turned on prematurely and lead to destruction.

Another notable observation from the figures is that there is a significant phase lag in the actual pulses (V_{ds} and I_d). For turn-on, this phase lag is the result of the delay between the time the gate begins to charge and the time it reaches the device's threshold voltage (the time the current begins to rise). For turn-off, the delay is the time it takes for the gate voltage to fall to the plateau voltage value plus the plateau time. The plateaus are a result of the large capacitance seen by the gate driver when V_{ds} is small [8]. If the phase lag is not modeled in the control design, the converter will have less phase margin than expected. This phenomenon has the ability to cause instability and ultimately cause the destruction of the converter.

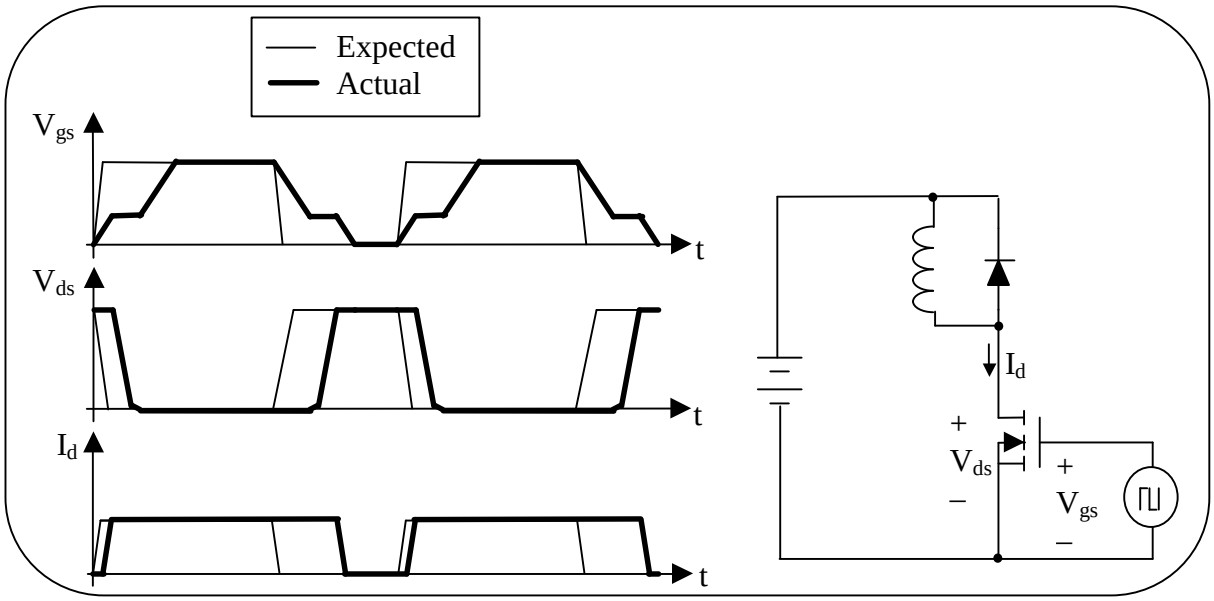


Figure A.1. Example of pulse-width distortion and phase lag.

Appendix B – Equivalent Frequency of a Square-wave Rising Edge

An approximation to the equivalent frequency of a square-wave signal can be determined based on the magnitude and slope, or equivalently the rise time, of the rising edge. This appendix shows how Equation 2.2 was derived. The method begins by finding the equation of a sine-wave that has the same peak-to-peak value and slope at the midpoint (time t = 0 in Figure B.1) as the square-wave in question. An example is shown in Figure B.1.

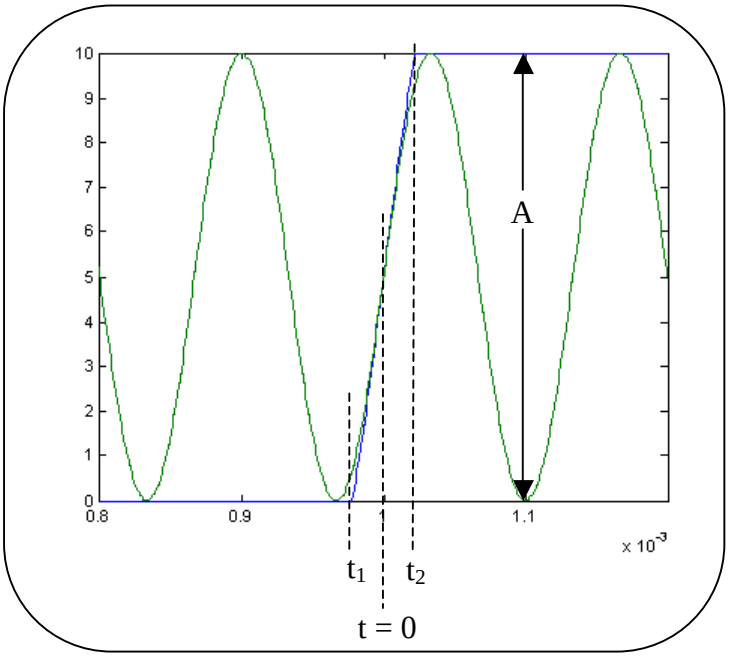


Figure B.1. Using a sine-wave to determine a rising edge's equivalent frequency.

The sine-wave and the line forming the rising edge can be represented by the following equations:

$$\text{Sine-wave:}\quad Y = \frac{A}{2}\sin(wt) + \frac{A}{2} \tag{B.1}$$

$$\text{Line:}\quad Y = mt + \frac{A}{2} \tag{B.2}$$

where m is the slope of the line between times t_1 and t_2. To compare the slopes at time t = 0, take the derivative with respect to time of equations B.1 and B.2 and set t equal to

zero. Since the slopes must be the same, the two resulting derivatives are equated as in Equation B.3.

$$\frac{d}{dt}\left(\frac{A}{2}\sin(wt)+\frac{A}{2}\right)=\frac{d}{dt}\left(mt+\frac{A}{2}\right)$$

$$\frac{A}{2}w\cos(wt)=m$$

$$\text{t} = 0 \quad \Rightarrow \quad \frac{A}{2}w=m \tag{B.3}$$

Replacing ω with 2πf and solving for f, the equivalent frequency is found to be:

$$f=\frac{m}{2p\left(\frac{A}{2}\right)} \tag{B.4}$$

Noting that the rise time (t_r) is 80% of $t_2 - t_1$, the slope m is related to rise time as follows:

$$m=\frac{A}{t_2-t_1}=\frac{A}{0.8t_r} \tag{B.5}$$

Substituting B.5 into B.4, the final result is:

$$f=\frac{0.8}{pt_r}$$

$$f\approx\frac{0.25}{t_r} \tag{B.6}$$

Appendix C – Switching Characteristics Measurement Procedure

C.1 Turn-on Switching Characteristics

The first step is to zoom-in to the gate voltage and drain current as shown below in Figure C.1. From the figure, one can see that the cursors are being used to measure the current turn-on delay time. The current rise time, current turn-on gradient, and current overshoot are also measured at this time. Refer to Chapter 1 for definitions.

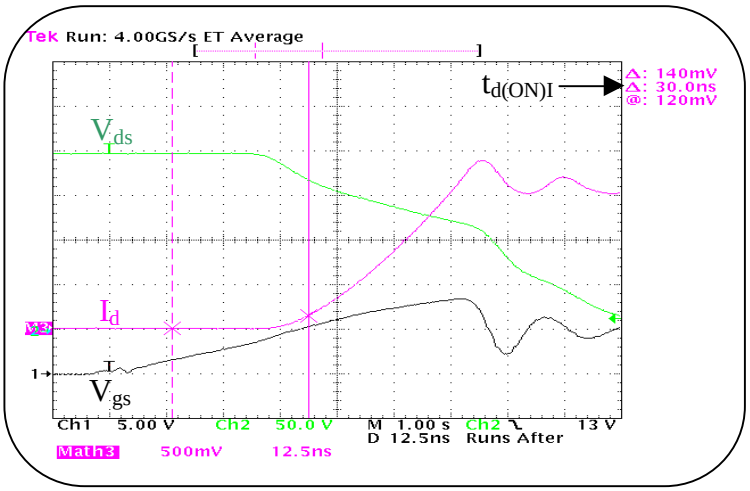


Figure C.1. Measurement of $t_{d(ON)I}$, t_{rI}, di/dt(on), and I_{OS}.

The waveforms are then scrolled to the left. Figure C.2 shows the extraction of the voltage fall time.

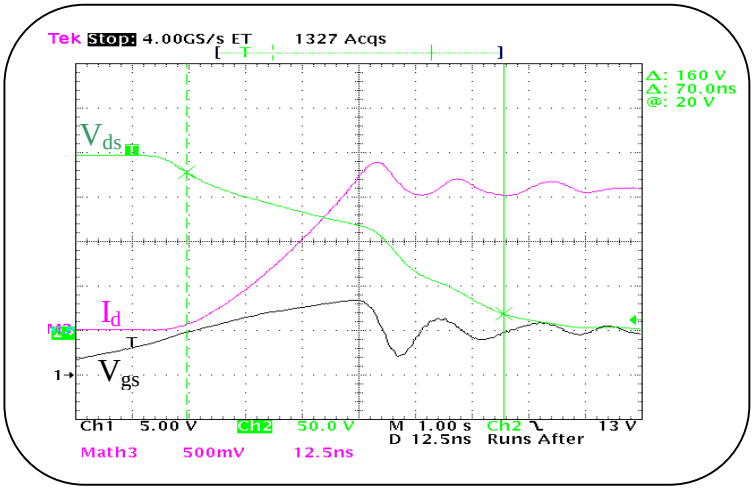


Figure C.2. Measurement of t_{fV}.

The end of the turn-on interval is considered to be when V_{ds} first crosses its saturation level (the steady-state voltage value when the switch is off). To determine the turn-on time, the oscilloscope must be zoomed-in close to the V_{ds} saturation level. Figure C.3 shows the measurement of the turn-on time. The cursor on the right is at the saturation voltage, which is found by aligning a horizontal cursor with steady-state value of V_{ds}.

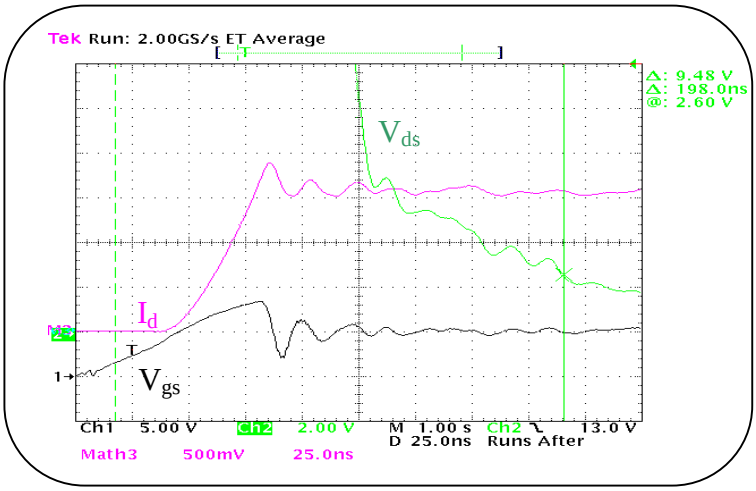


Figure C.3. Measurement of t_{ON}.

To measure the turn-on switching energy loss, one must zoom-out to the entire turn-on interval. Two of the oscilloscope math functions are used. The multiplication function is used to multiply V_{ds} and $-I_d$ (the current is negative because of the orientation of the shunt). The result of this multiplication is then saved as a reference waveform. The oscilloscope's integration function is then used to integrate the reference waveform. The resultant waveform is the negative of the energy. Figure C.4 below shows the measurement of the turn-on energy. The cursors are used to find the change in energy during the turn-on interval. The energy is actually the value shown divided by 0.103 (the value of the shunt). In this case, E_{ON} was approximately 79 μJ.

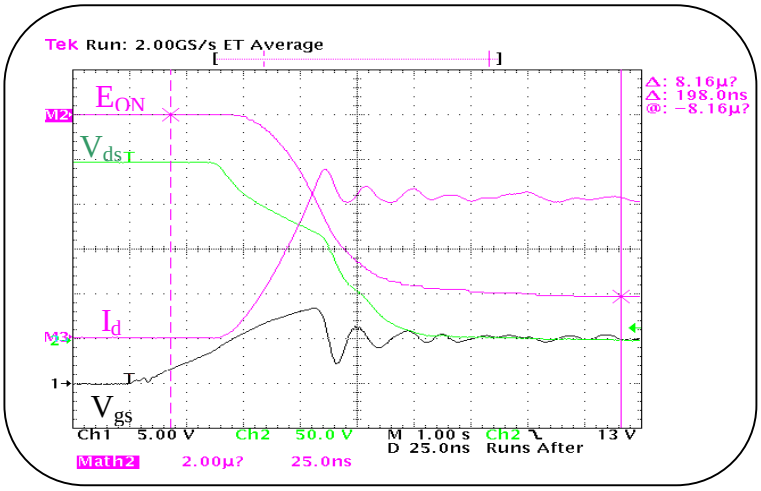


Figure C.4. Measurement of E_{ON}.

C.2 Turn-off Switching Characteristics

The first step is to zoom-in to the gate voltage and drain current as shown below in Figure C.5. From the figure, one can see that the cursors are being used to measure the current turn-off delay time. The turn-off time is also measured at this time.

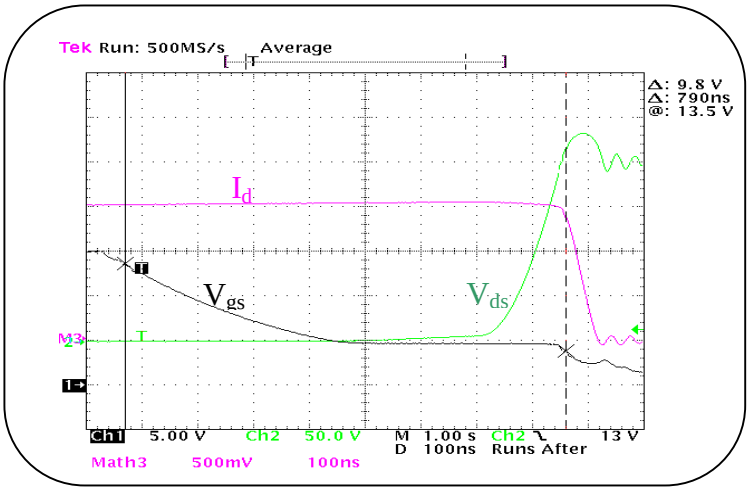


Figure C.5. Measurement of $t_{d(OFF)I}$ and t_{OFF}.

The waveforms are scrolled to the left and zoomed-in, and the voltage rise time, voltage turn-off gradient, voltage overshoot, current fall time, and turn-off current gradient can be measured as in Figure C.6.

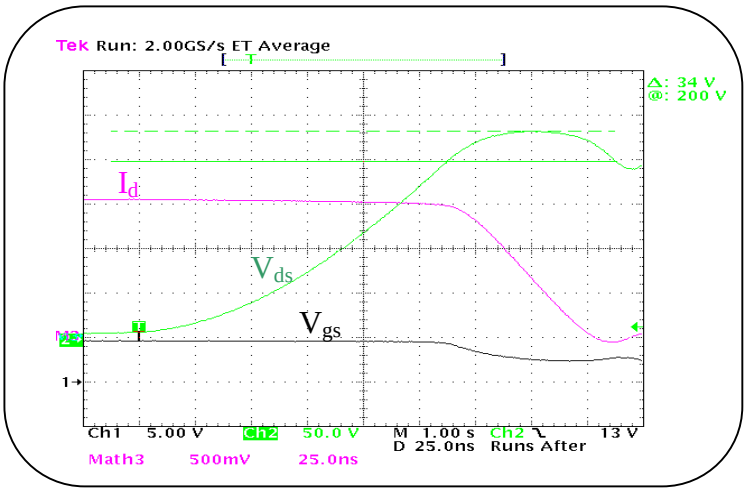


Figure C.6. Measurement of t_{rV}, dv/dt(off), V_{OS}, t_{fI}, and di/dt(off).

To measure the turn-off switching energy loss, one must zoom-out to the entire turn-off interval. The multiplication and integration functions are again used to get the negative of the energy. The cursors are then used to find the change in energy during the turn-off interval. Figure C.7 shows the measurement of the turn-off energy.

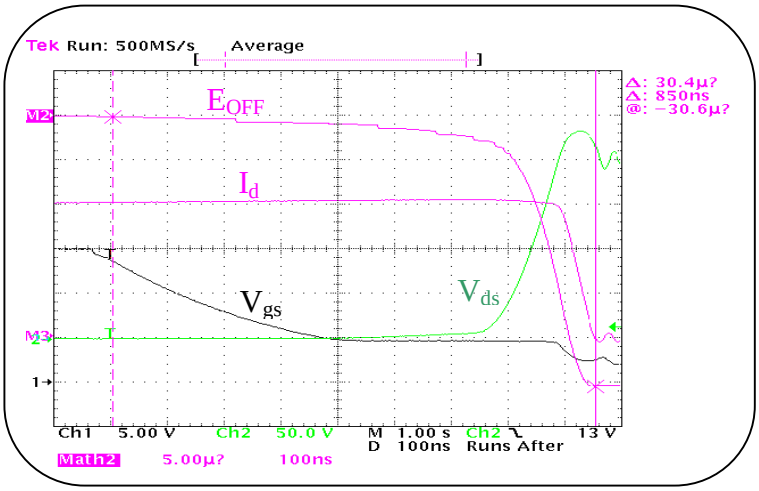
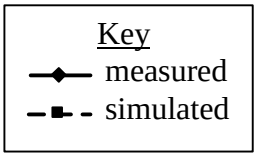


Figure C.7. Measurement of E_{OFF}.

Appendix D – Parametric Study Results

D.1 Switching Characteristics with Changing Gate Resistance (R_g)

The switching characteristics that showed changes with gate resistance are shown in this section. Those switching characteristics not plotted were not sensitive to R_g. The curves shown were fit to the data using Microsoft Excel's trendline function.



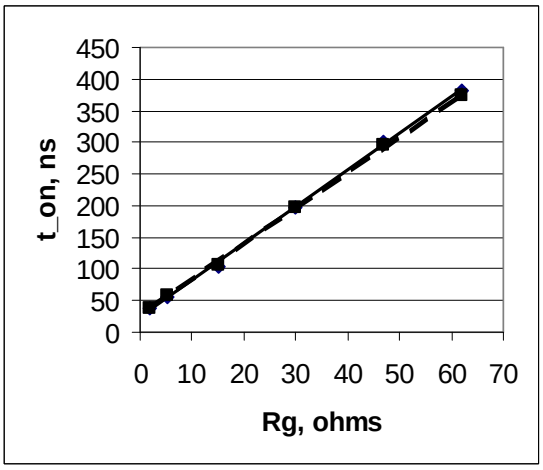


Figure D.1. Turn-on time vs. R_g.

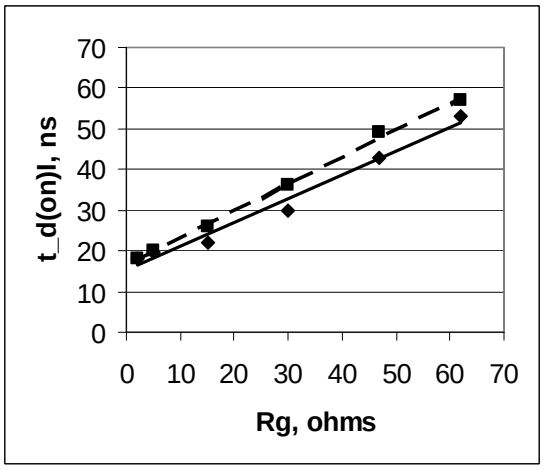


Figure D.2. Current turn-on delay vs. R_g.

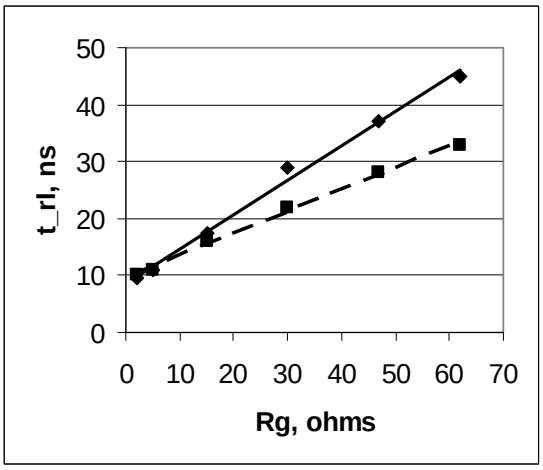


Figure D.3. Current rise time vs R_g.

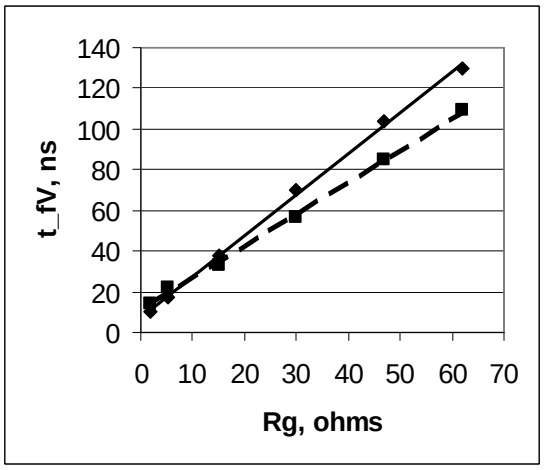
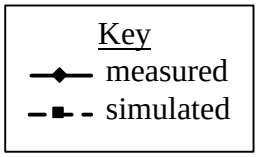


Figure D.4. Voltage fall time vs. R_g.



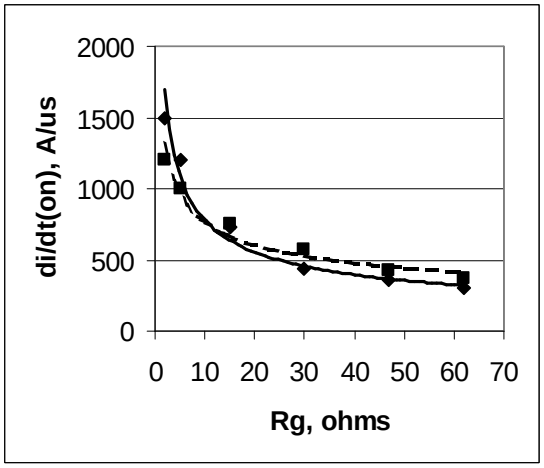


Figure D.5. Turn-on current gradient vs R_g.

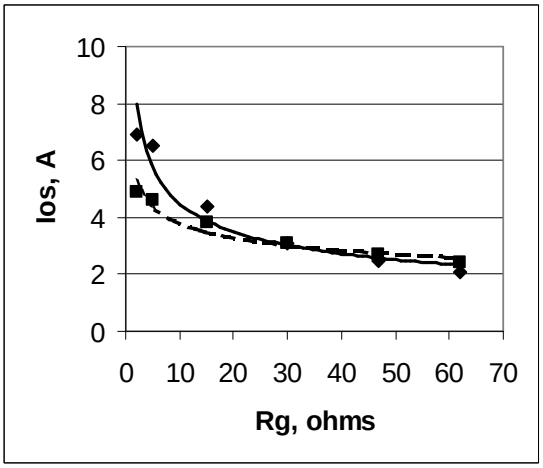


Figure D.6. Current overshoot vs R_g.

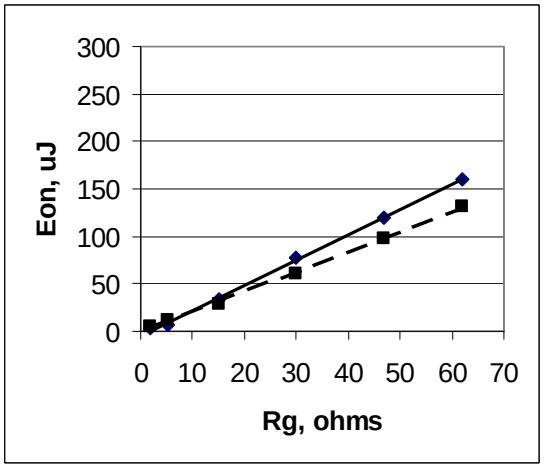


Figure D.7. Turn-on switching energy vs R_g.

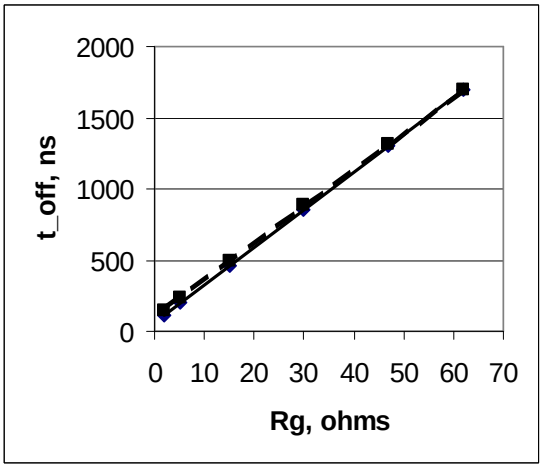


Figure D.8. Turn-off time vs R_g.

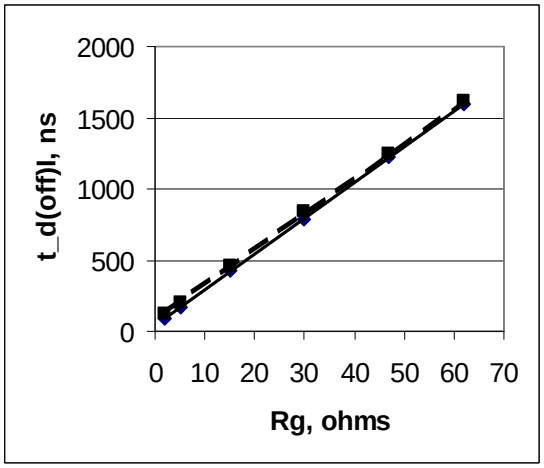
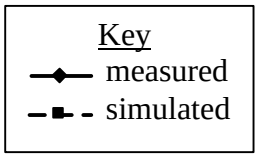


Figure D.9. Current turn-off delay vs R_g.



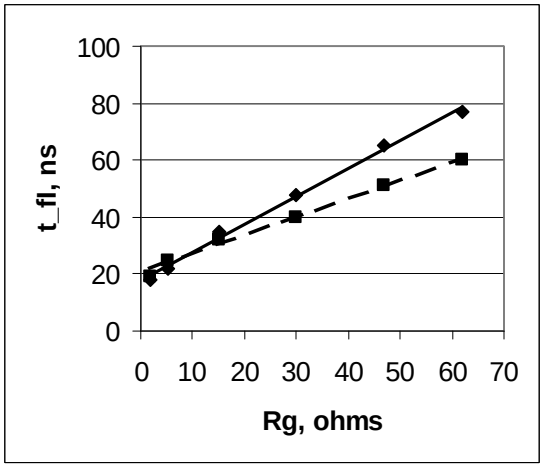


Figure D.10. Current fall time vs R_g.

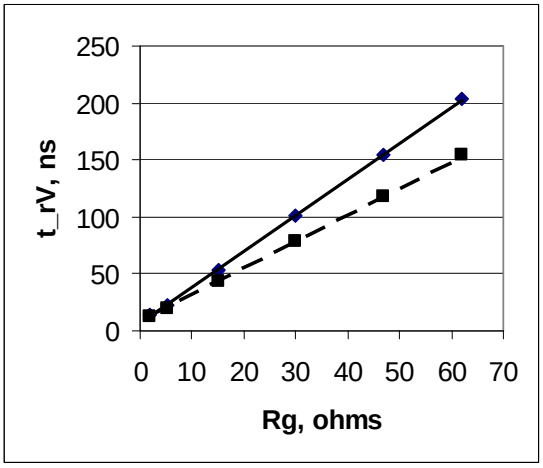


Figure D.11. Voltage rise time vs R_g.

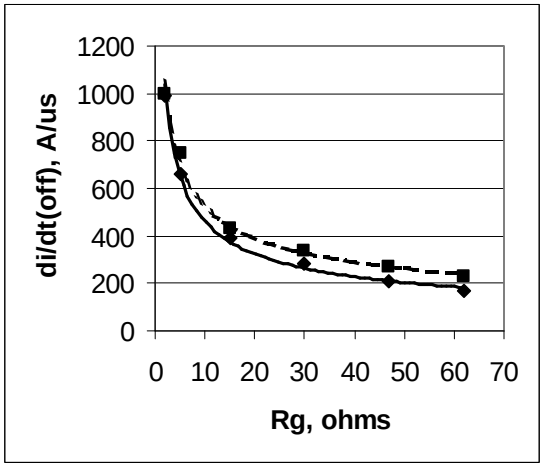


Figure D.12. Turn-off current gradient vs R_g.

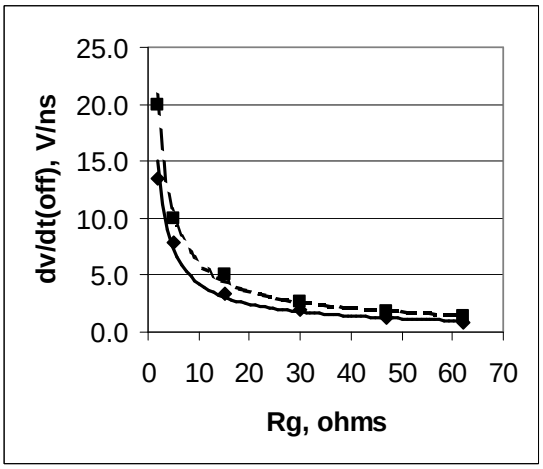


Figure D.13. Turn-off voltage gradient vs R_g.

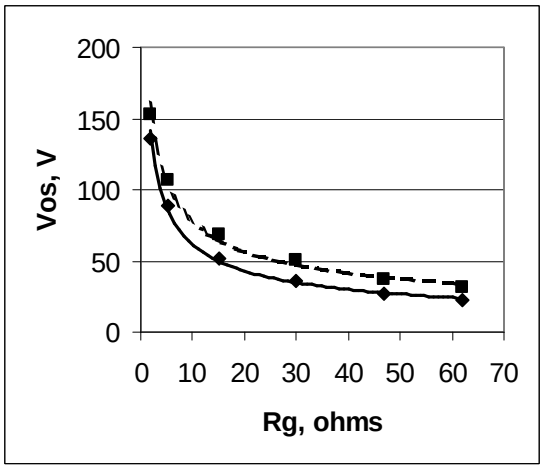


Figure D.14. Voltage overshoot vs R_g.

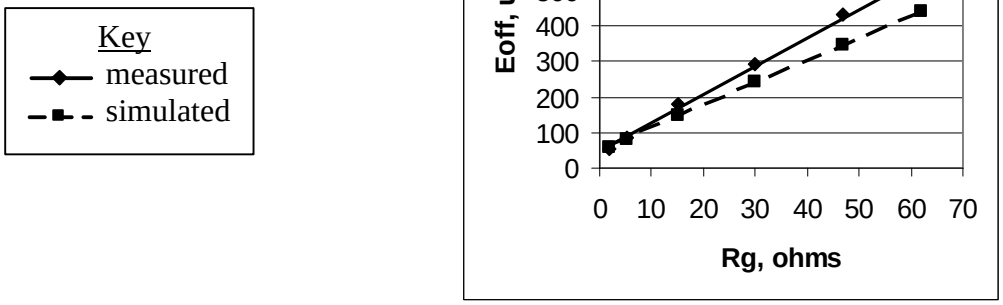


Figure D.15. Turn-off switching energy vs R_g.

D.2 Switching Characteristics with Changing Gate Voltage (V_g)

The switching characteristics that showed changes with gate voltage are shown in this section. Those switching characteristics not plotted were not sensitive to V_g.

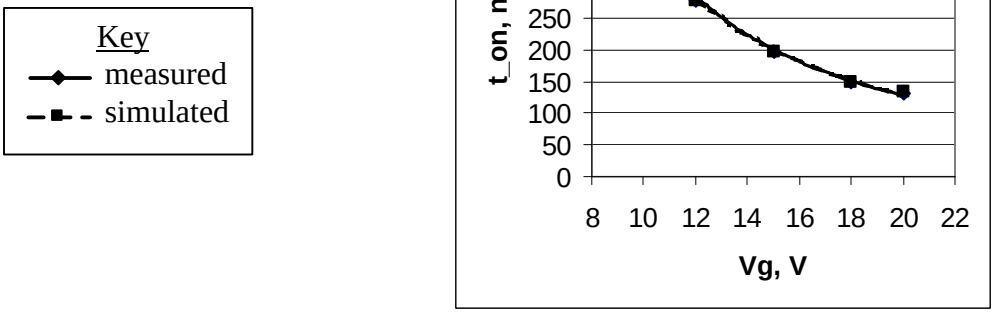
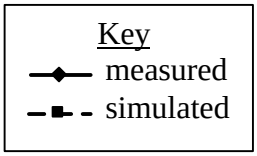


Figure D.16. Turn-on time vs V_g.



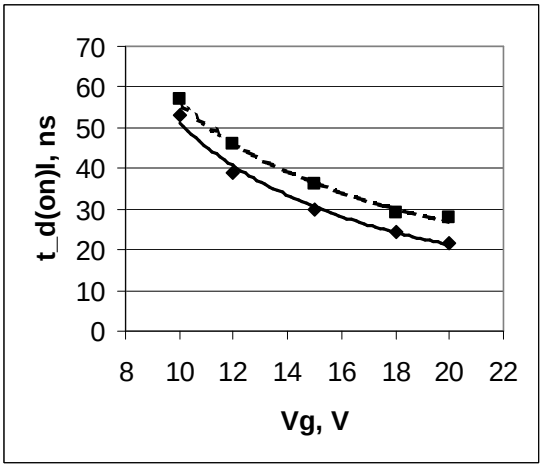


Figure D.17. Current turn-on delay vs V_g.

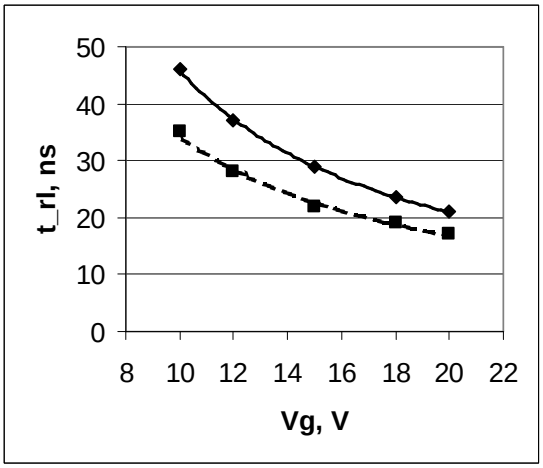


Figure D.18. Current rise time vs V_g.

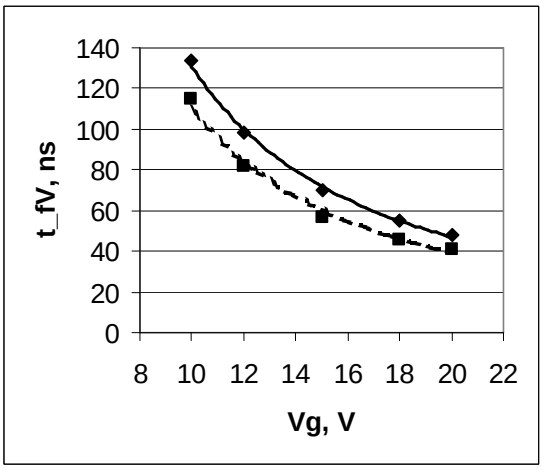


Figure D.19. Voltage fall time vs V_g.

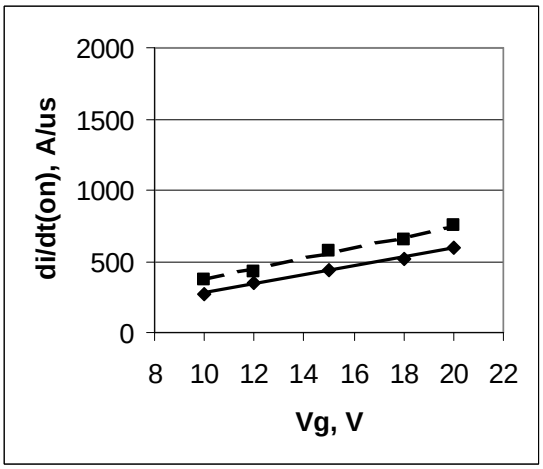


Figure D.20. Turn-on current gradient vs V_g.

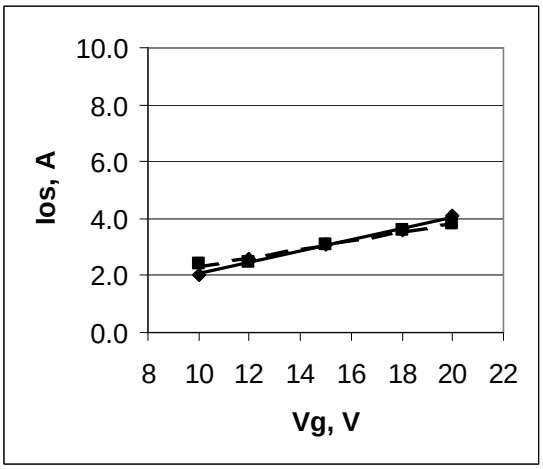
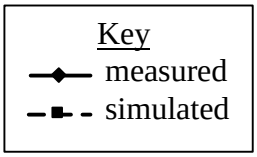


Figure D.21. Current overshoot vs V_g.



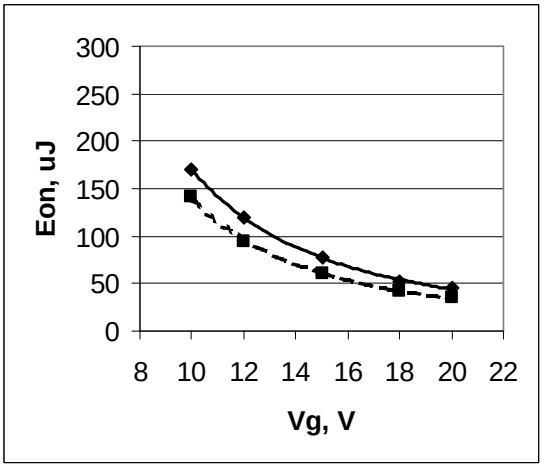


Figure D.22. Turn-on energy vs V_g.

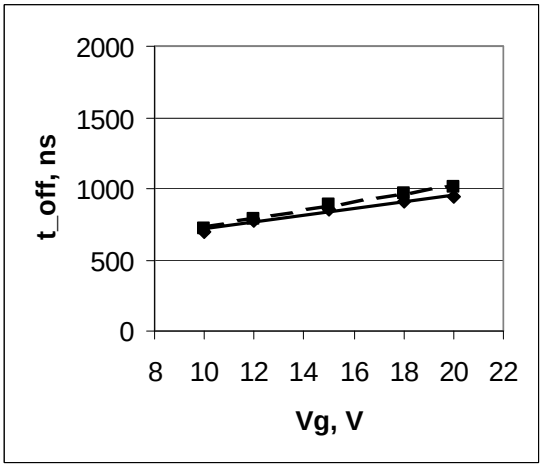


Figure D.23. Turn-off time vs V_g.

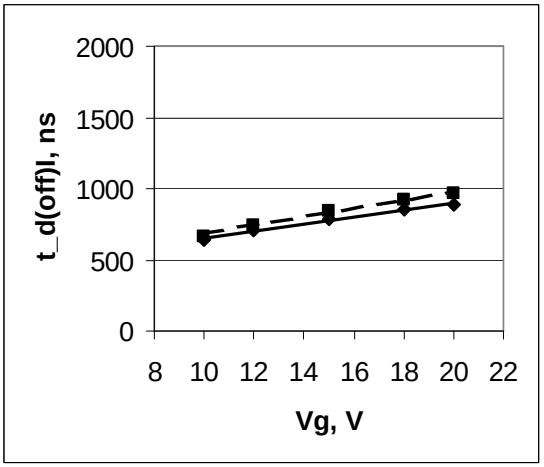


Figure D.24. Current turn-off delay vs V_g.

D.3 Switching Characteristics with Changing Bus Voltage (V_{bus})

The switching characteristics that showed changes with bus voltage are shown in this section. Those switching characteristics not plotted were not sensitive to V_{bus}. The disagreements between measurement and simulation are greater for the data in this section than for the other cases. It is believed by this author that these discrepancies may be caused by differences between the capacitances of the MOSFET simulation model and the real device at higher V_{ds}. The curves in the datasheet for the IXFH26N50 (Figure 3.12) show the capacitances only for V_{ds} less than 25 V.

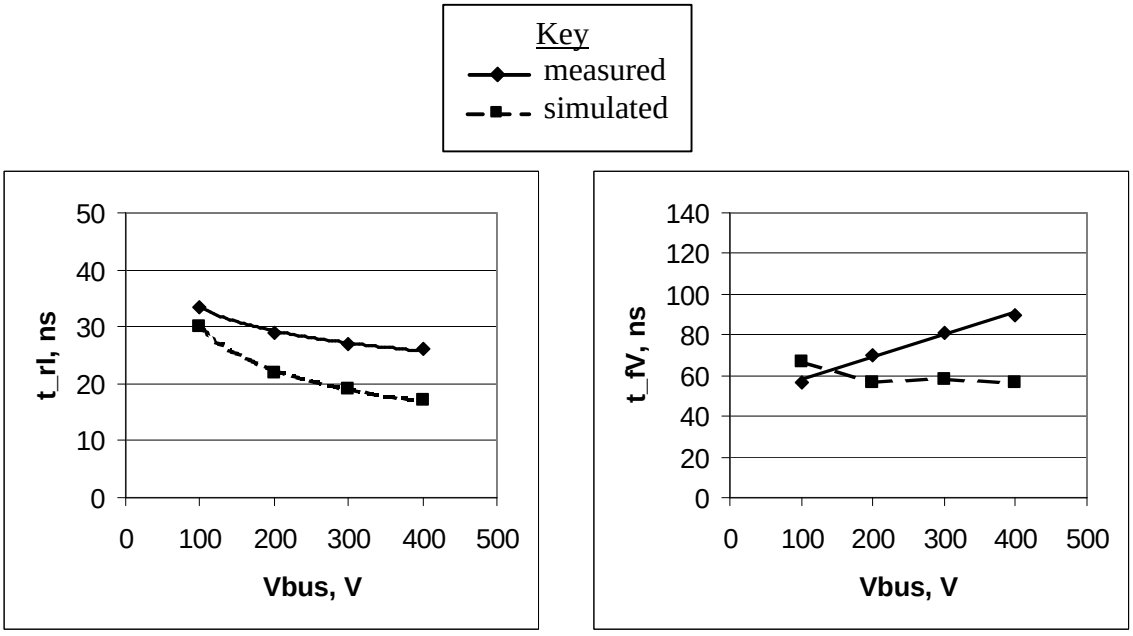


Figure D.25. Current rise time vs V_{bus}.

Figure D.26. Voltage fall time vs. V_{bus}.

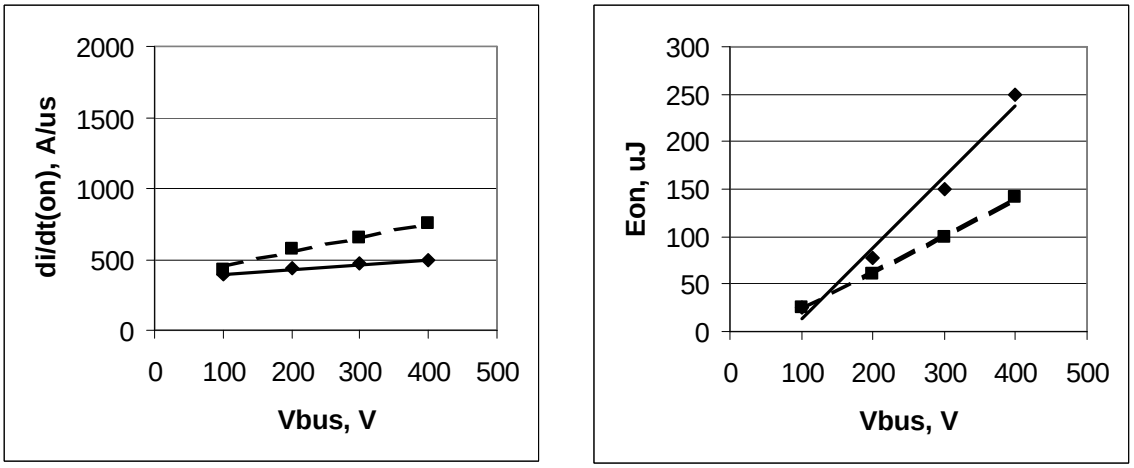
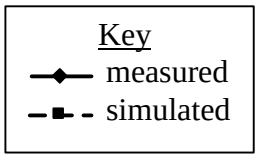


Figure D.27. Turn-on current gradient vs V_{bus}.

Figure D.28. Turn-on switching energy vs V_{bus}.



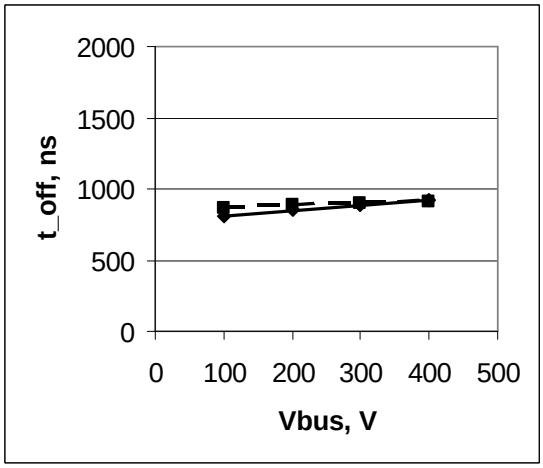


Figure D.29. Turn-off time vs V_{bus}.

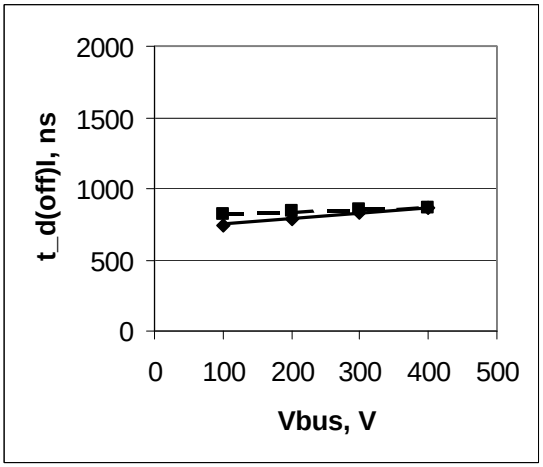


Figure D.30. Current turn-off delay time vs V_{bus}.

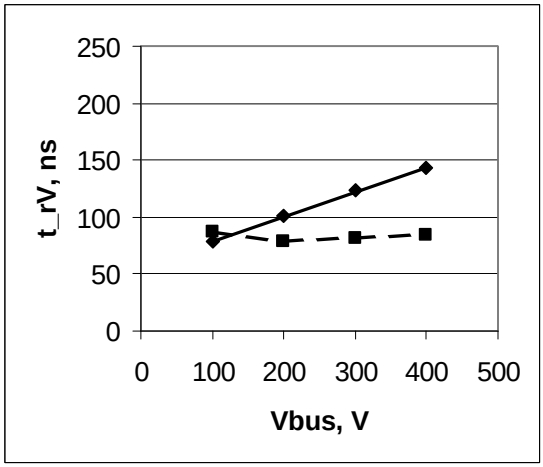


Figure D.31. Voltage rise time vs V_{bus}.

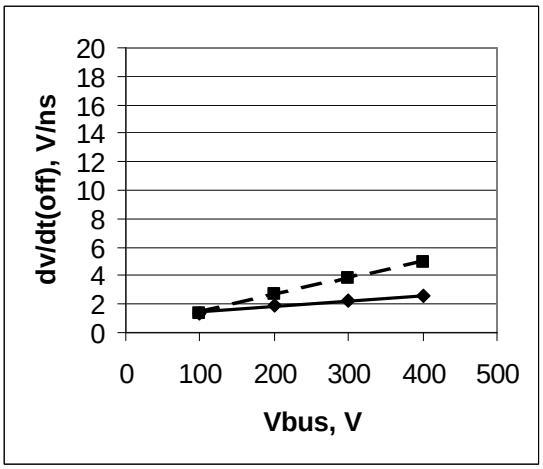


Figure D.32. Turn-off voltage gradient vs V_{bus}.

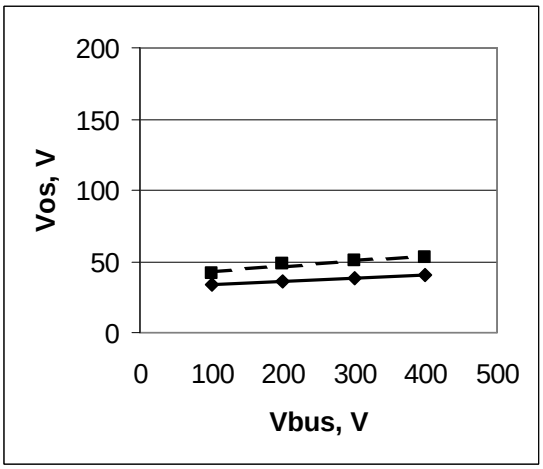


Figure D.33. Voltage overshoot vs V_{bus}.

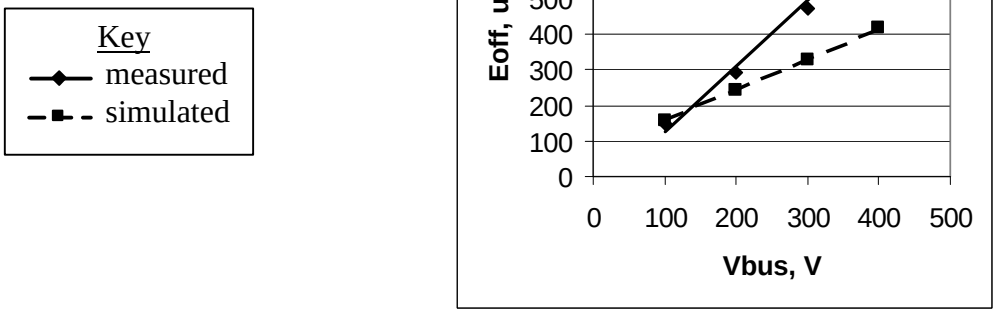


Figure D.34. Turn-off switching energy vs V_{bus}.

D.4 Switching Characteristics with Changing Drain Current (I_d)

The switching characteristics that showed changes with drain current are shown in this section. Those switching characteristics not plotted were not sensitive to I_d.

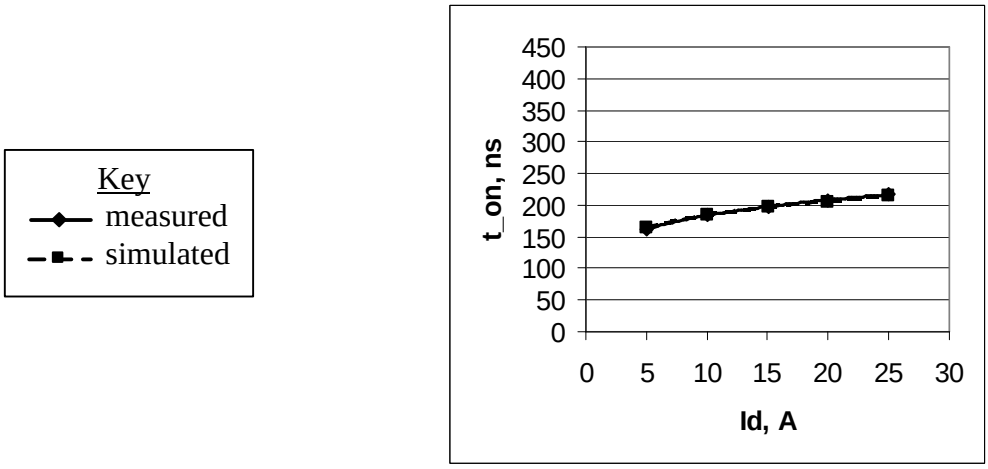
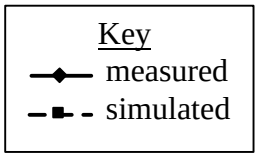


Figure D.35. Turn-on time vs I_d.



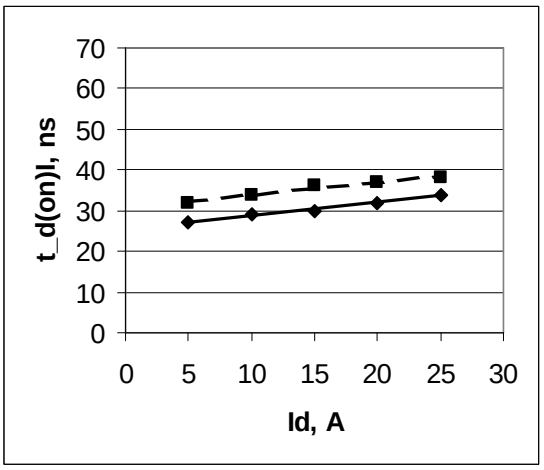


Figure D.36. Current turn-on delay vs I_d.

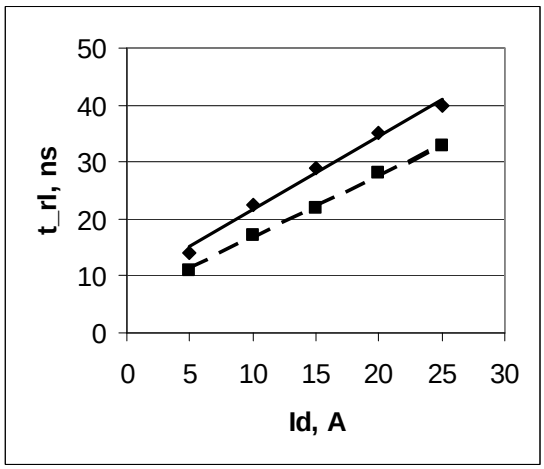


Figure D.37. Current rise time vs I_d.

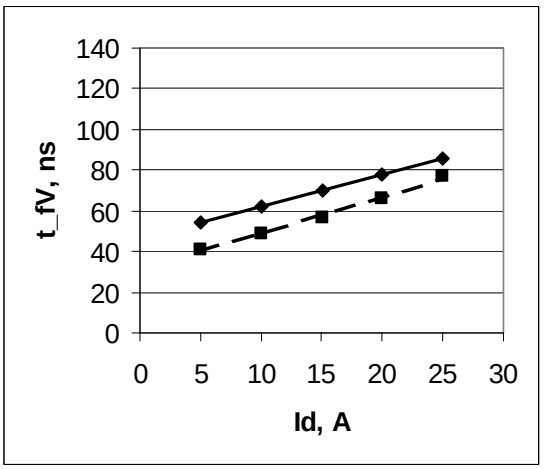


Figure D.38. Voltage fall time vs I_d.

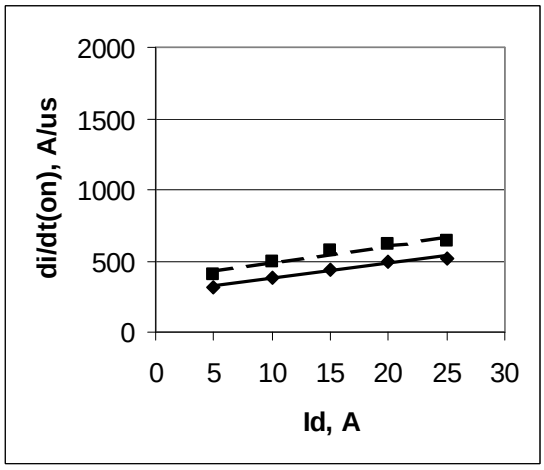


Figure D.39. Turn-on current gradient vs I_d.

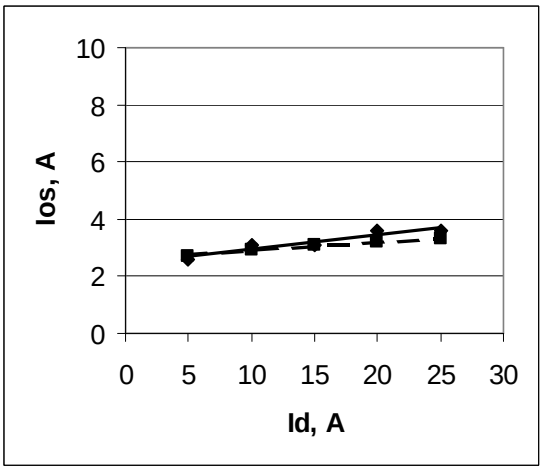
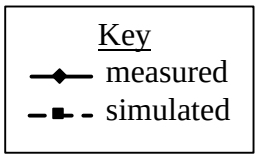


Figure D.40. Current overshoot vs I_d.



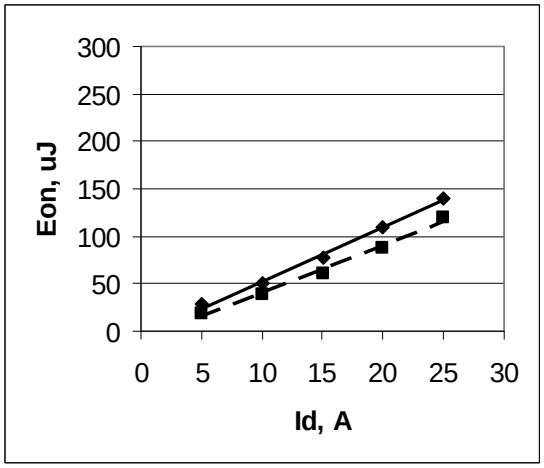


Figure D.41. Turn-on switching energy vs I_d.

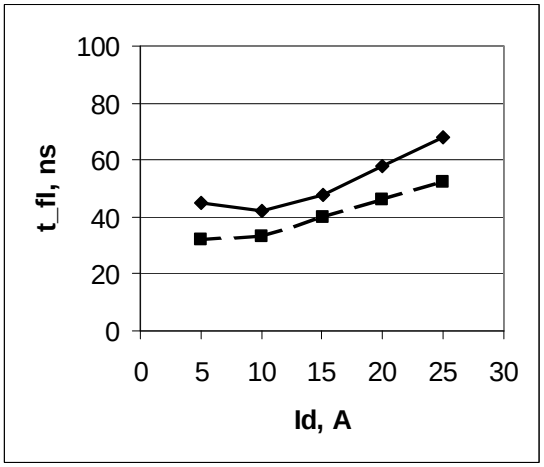


Figure D.42. Current fall time vs I_d.

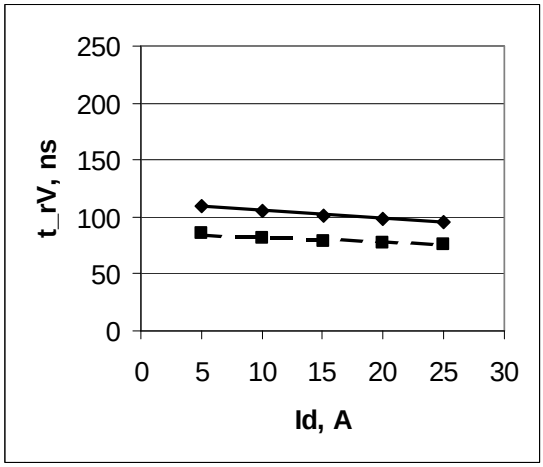


Figure D.43. Voltage rise time vs I_d.

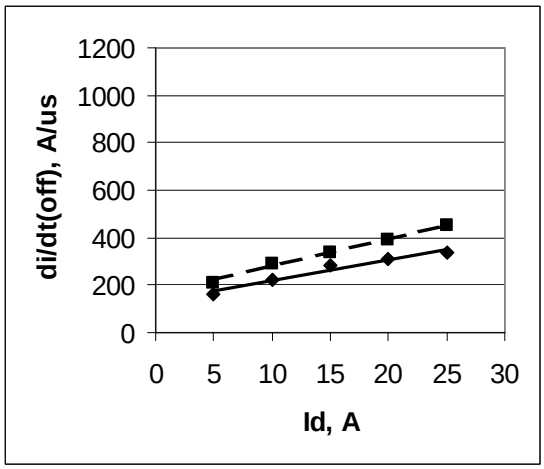


Figure D.44. Turn-off current gradient vs I_d.

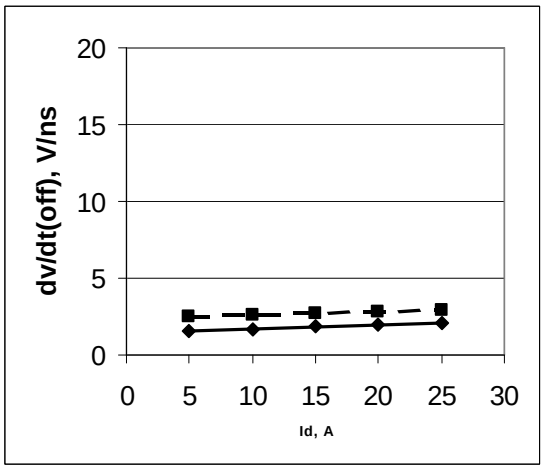


Figure D.45. Turn-off voltage gradient vs I_d.

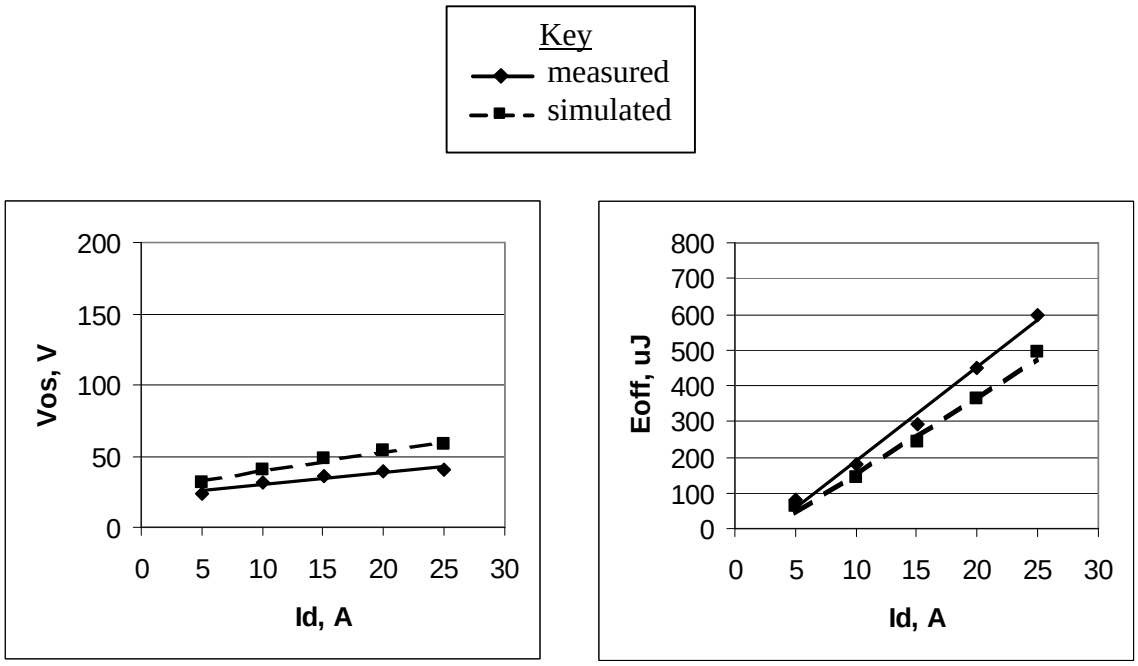


Figure D.46. Voltage overshoot vs I_d.

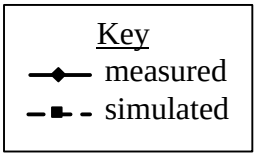
Figure D.47. Turn-off switching energy vs I_d.

D.5 Switching Characteristics with Changing Bus Capacitance (C_{bus})

Over the range chosen (300nF – 900nF), no significant changes in the switching characteristics could be observed. This means that the minimum capacitance of 300nF was still more than enough to adequately provide energy during switching transitions with the rest of the parameters at their base values.

D.6 Switching Characteristics with Changing Loop Inductance (L_{LOOP})

The switching characteristics that showed changes with loop inductance are shown in this section. Those switching characteristics not plotted were not sensitive to L_{LOOP}.



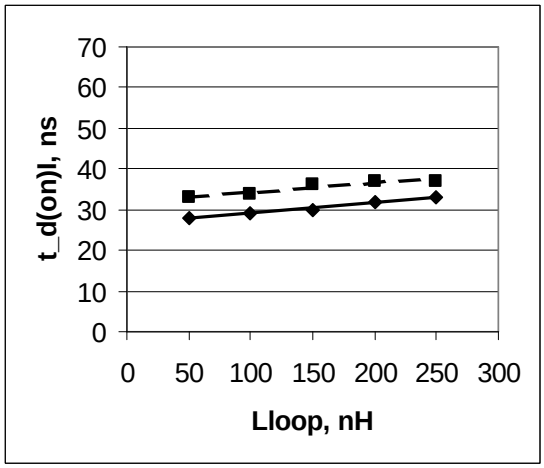


Figure D.48. Current turn-on delay vs L_{LOOP}.

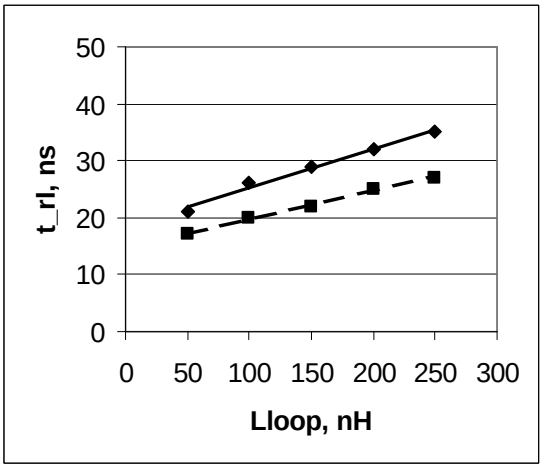


Figure D.49. Current rise time vs L_{LOOP}.

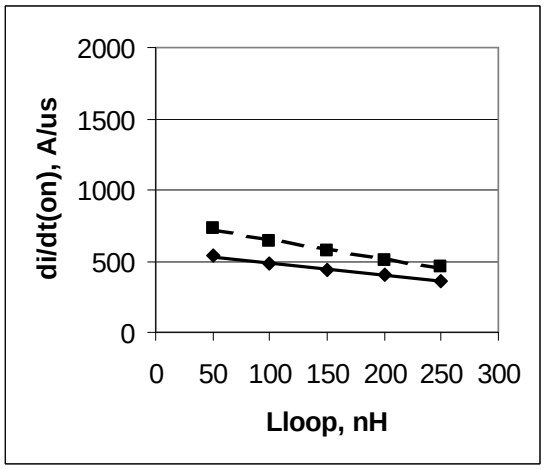


Figure D.50. Turn-on current gradient vs L_{LOOP}.

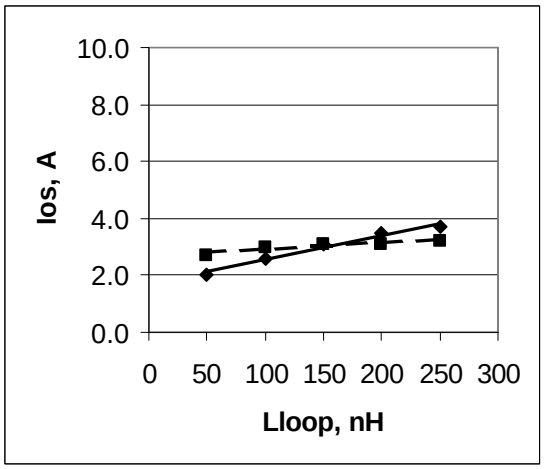
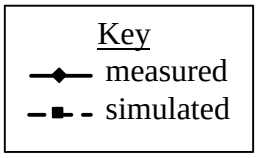


Figure D.51. Current overshoot vs L_{LOOP}.



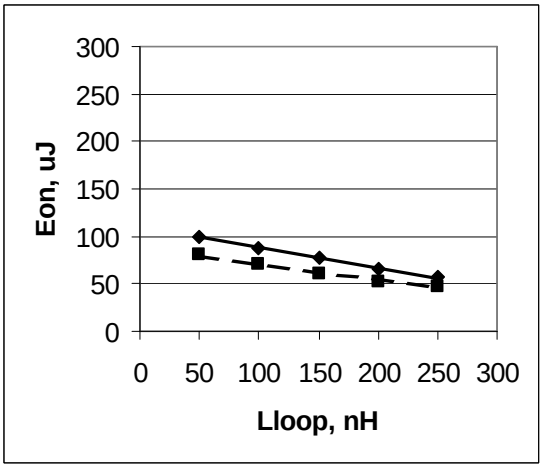


Figure D.52. Turn-on switching energy vs L_{LOOP}.

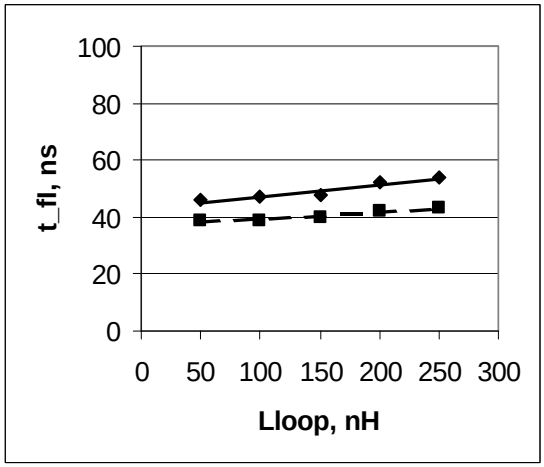


Figure D.53. Current fall time vs L_{LOOP}.

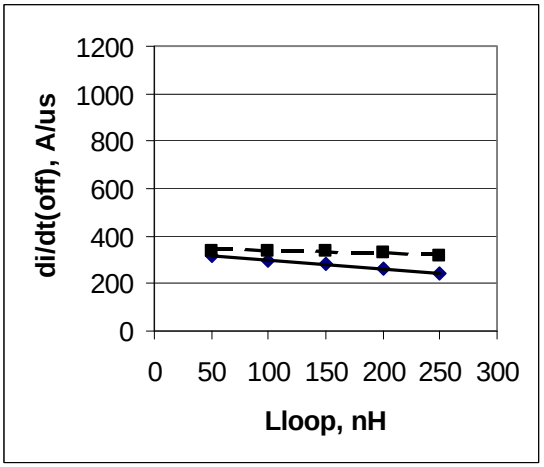


Figure D.54. Turn-off current gradient vs L_{LOOP}.

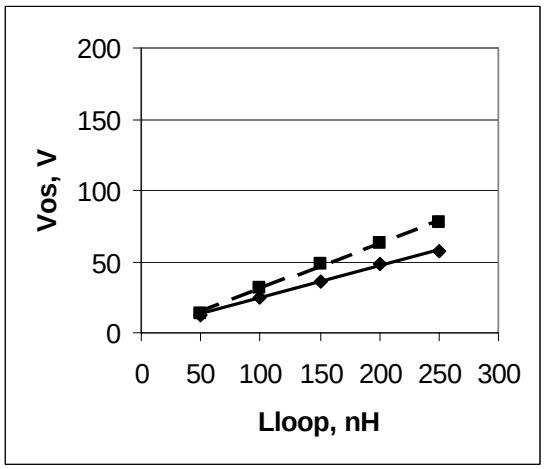


Figure D.55. Voltage overshoot vs L_{LOOP}.

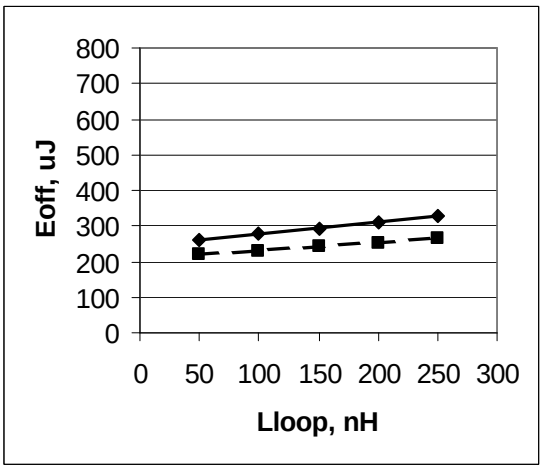


Figure D.56. Turn-off switching energy vs L_{LOOP}.

D.7 Switching Characteristics with Changing Junction Temperature (T_j)

It was observed that the junction temperature has a minimal effect on the switching characteristics compared to the other parameters. However, the trends for the switching characteristics for varying junction temperature consistently increased or decreased. The plots are provided in this section to demonstrate the trends. Note that these plots are not on the same scale as those shown in the previous sections of this appendix. If they were on the same scale, they would appear almost like horizontal lines. The plots below are only the measured data. T_j can be adjusted in the MOSFET simulation model, but time did not permit further simulation.

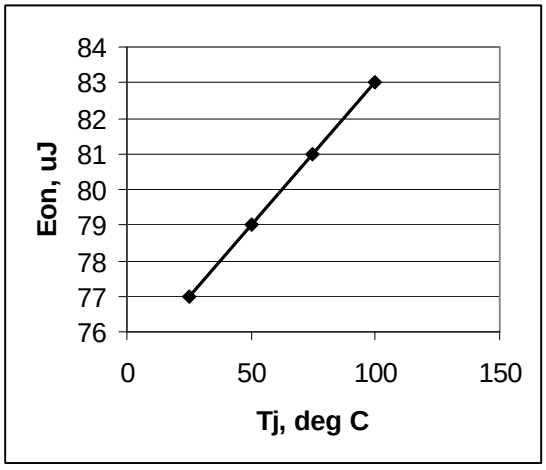


Figure D.57. Turn-on switching energy vs T_j.

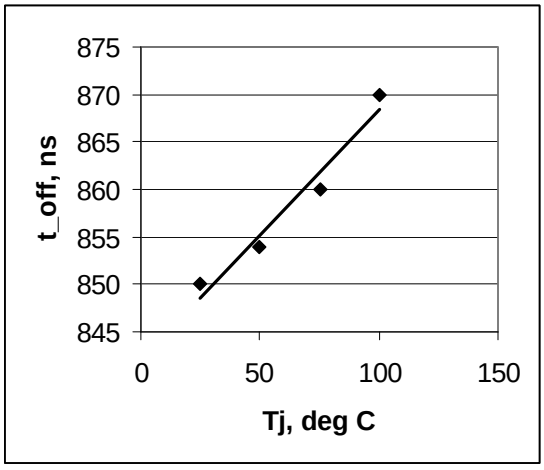


Figure D.58. Turn-off time vs T_j.

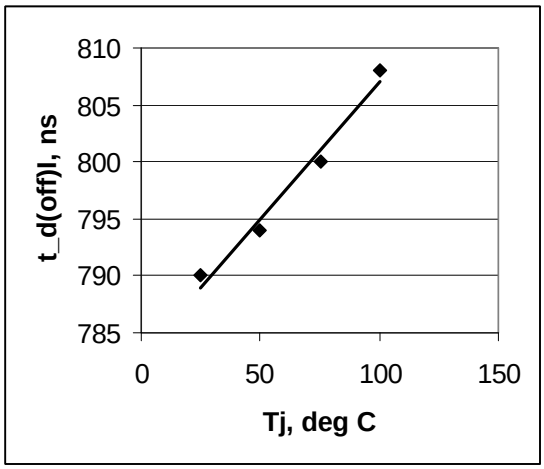


Figure D.59. Current turn-off delay vs T_j.

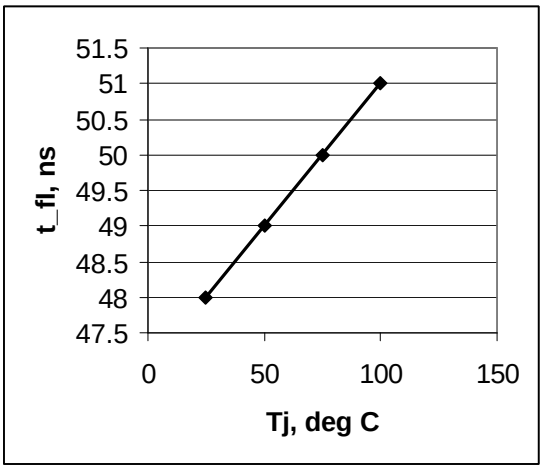


Figure D.60. Current fall time vs T_j.

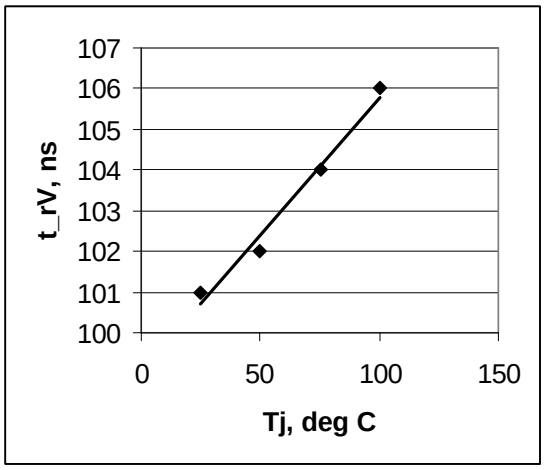


Figure D.61. Voltage rise time vs T_j.

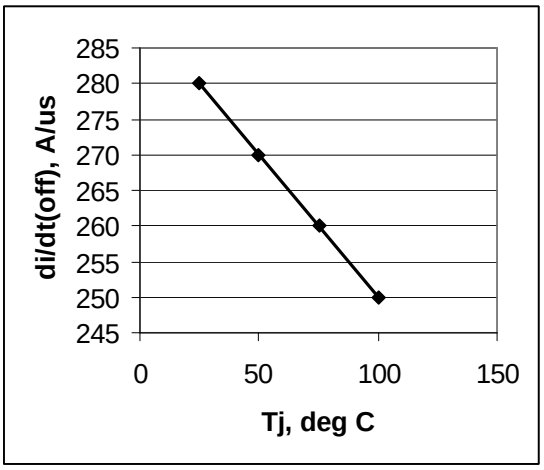


Figure D.62. Turn-off current gradient vs T_j.

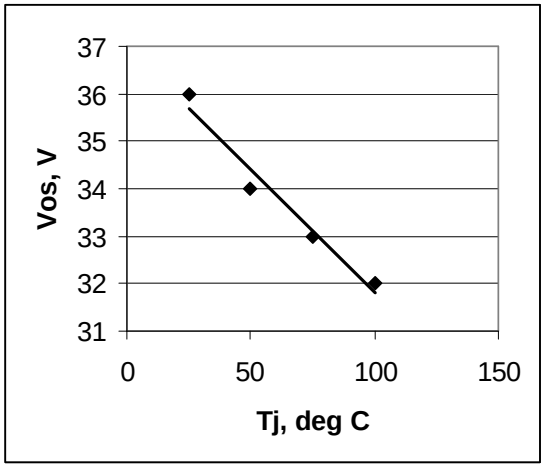


Figure D.63. Voltage overshoot vs T_j.

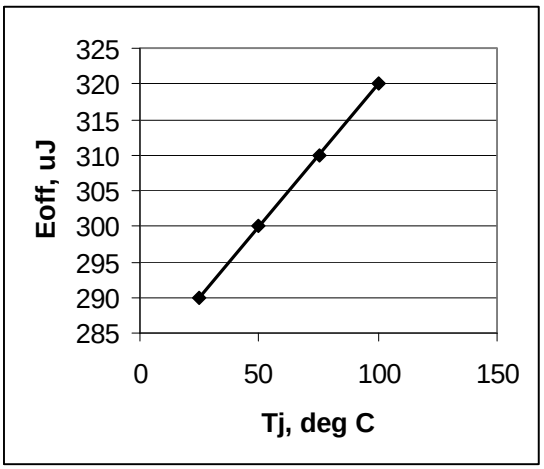


Figure D.64. Turn-off switching energy vs T_j.

Appendix E – Detailed Tester Design

E.1 Introduction

This Appendix gives the detailed design of the switching characteristics tester. The tester consists of eight circuit boards, namely: Testbed, Power Board, Control Board, Gate Driver Board, Load Board, Power Supply Board 1, Power Supply Board 2, and Backplane. A description of the boards' functions, schematic diagram, top and bottom PCB diagrams, component placement diagram, and bill of materials are provided for each board in the next several sections.

E.2 Testbed

The Testbed contains the high frequency capacitors that make up C_{bus}, the coaxial shunts (R_1 and R_2), and the SiC Schottky diodes (D_1 and D_2) shown in Figure E.1 and 5.1. Because this board contains the loop formed by C_{bus} and the power devices, its layout is critical. As described in 5.4, special attention was given to the layout considerations. The primary purpose of this board is to interface to the IPEM being tested. By proper selection of which of the power planes are connected where, the user can choose to use the diodes provided or use diodes from inside the module (perhaps the body diodes if a MOSFET is being tested). For most of the double-pulse testing, diode D_1 or D_2 will be used.

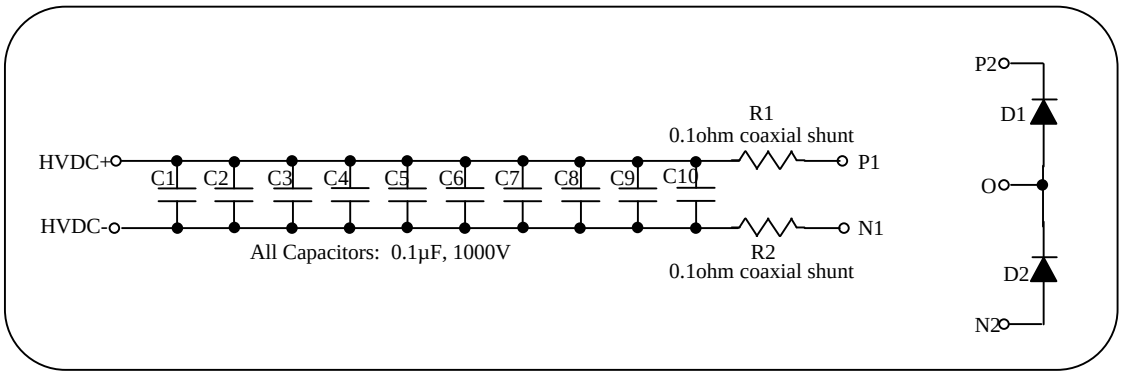


Figure E.1. Testbed schematic.

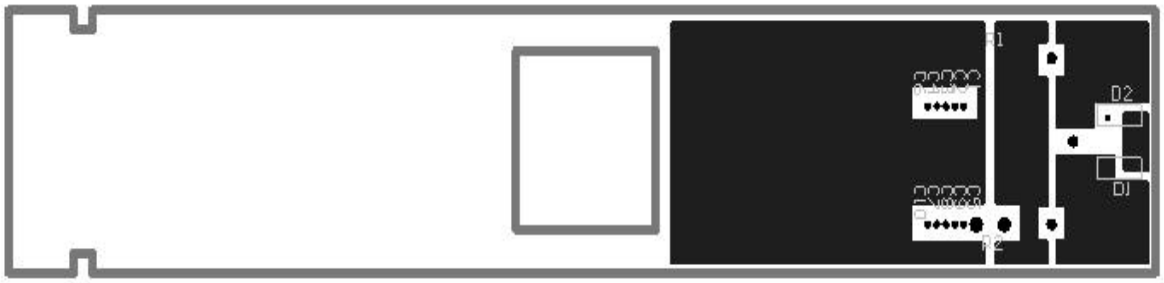


Figure E.2. Testbed top layer.

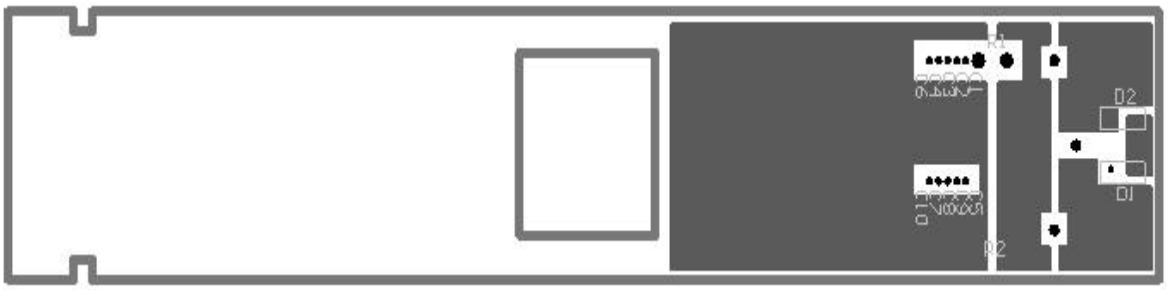


Figure E.3. Testbed bottom layer.

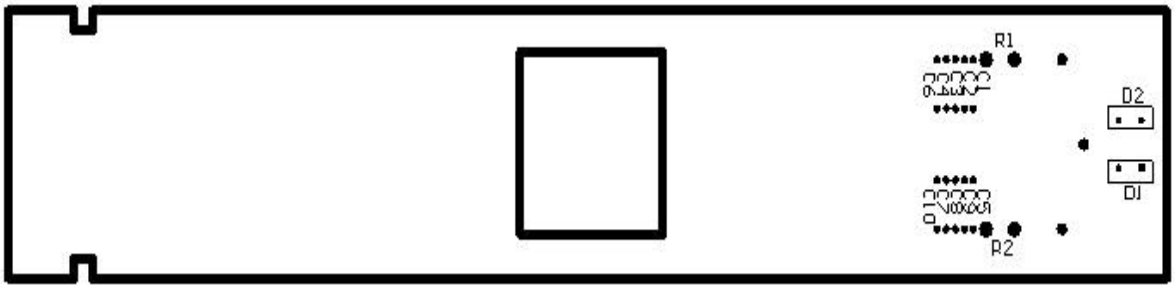


Figure E.4. Testbed component placement diagram.

Table E.1. Testbed bill of materials.

Component	Description	Manufacturer	Part Number	Suggested Distributor
C1 - C10	0.1uF, 1000V ceramic disc capacitor	Vishay	10GAP10	Newark
D1, D2	600 V, 12A SiC Schottky Diode	Infineon	SDT06S60	Infineon
R1, R2	0.1 ohm coaxial shunt	T&M Research	SDN-10	T&M Research

E.3 Power Board

The Power Board contains the bulk capacitors ($C_1 - C_6$) for power storage on the high voltage DC bus. It also has polypropylene capacitors ($C_7 - C_{10}$) to handle the large ripple currents generated during the continuous-pulse testing. Resistors $R_1 - R_6$ are bleeder resistors and should help to balance the voltage across the capacitors. The relays ($Sw_1 - Sw_3$) are controlled via the control signals DPT (double-pulse top), CONT (continuous), and DPB (double-pulse bottom). The relays determine whether the load will be connected to the positive DC bus rail, the negative rail, or the midpoint of the capacitors, depending on which test is performed. Connections to the rest of the tester are made through J_1.

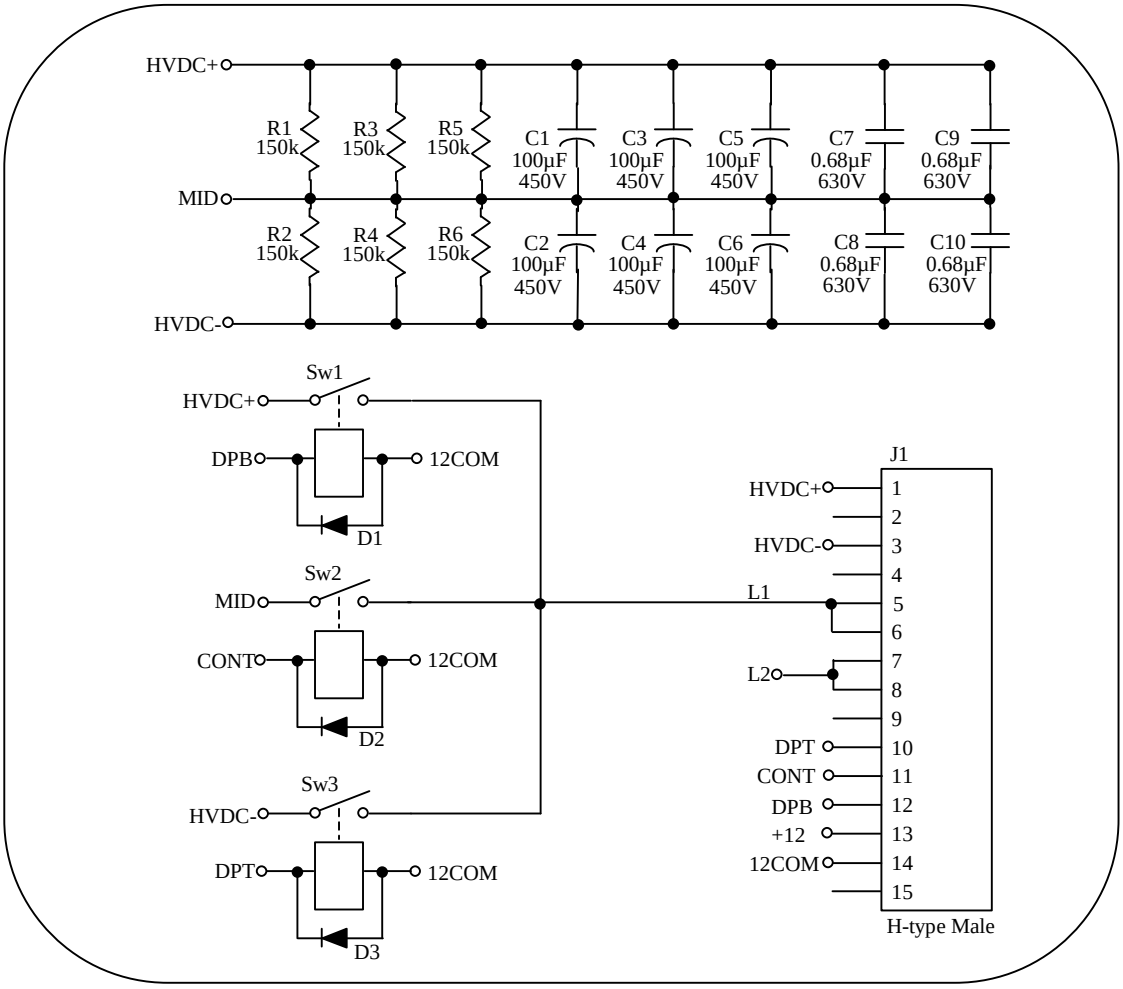


Figure E.5. Power Board schematic.

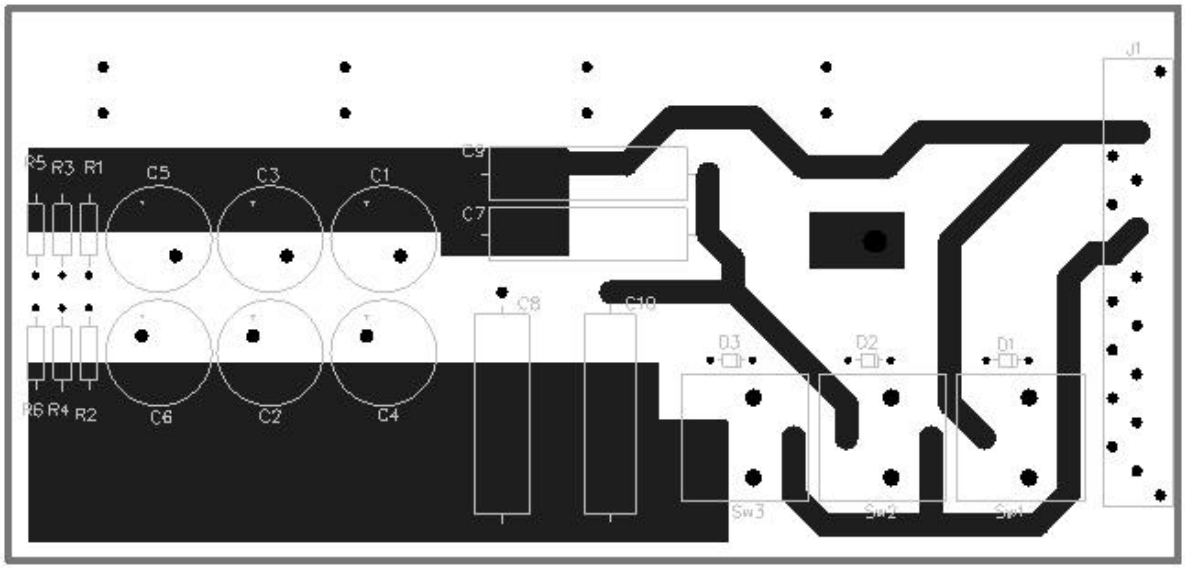


Figure E.6. Power Board top layer.

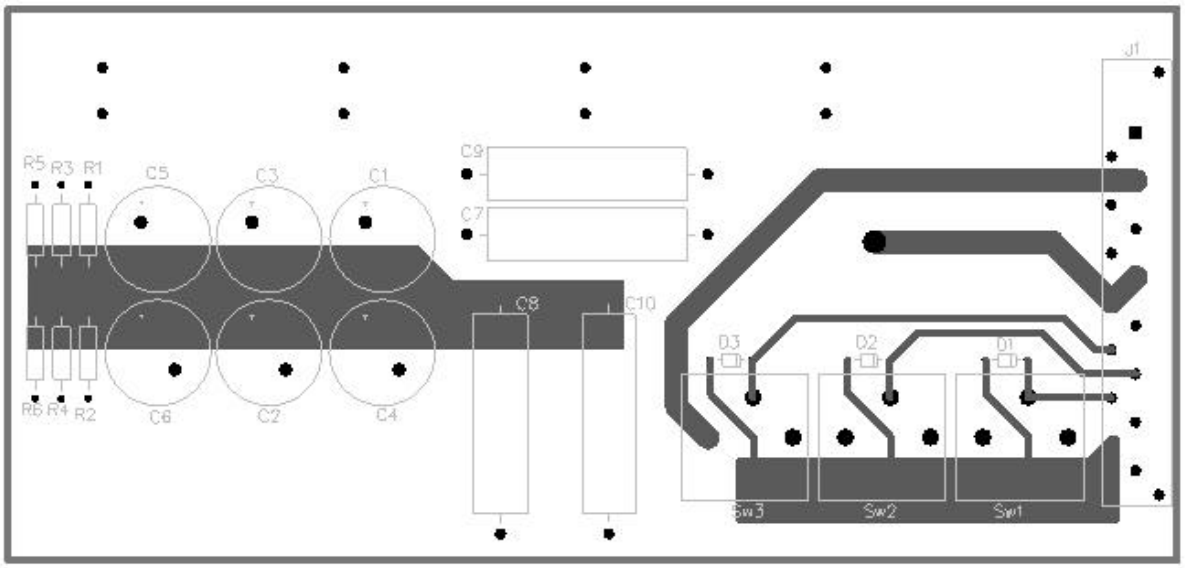


Figure E.7. Power Board bottom layer.

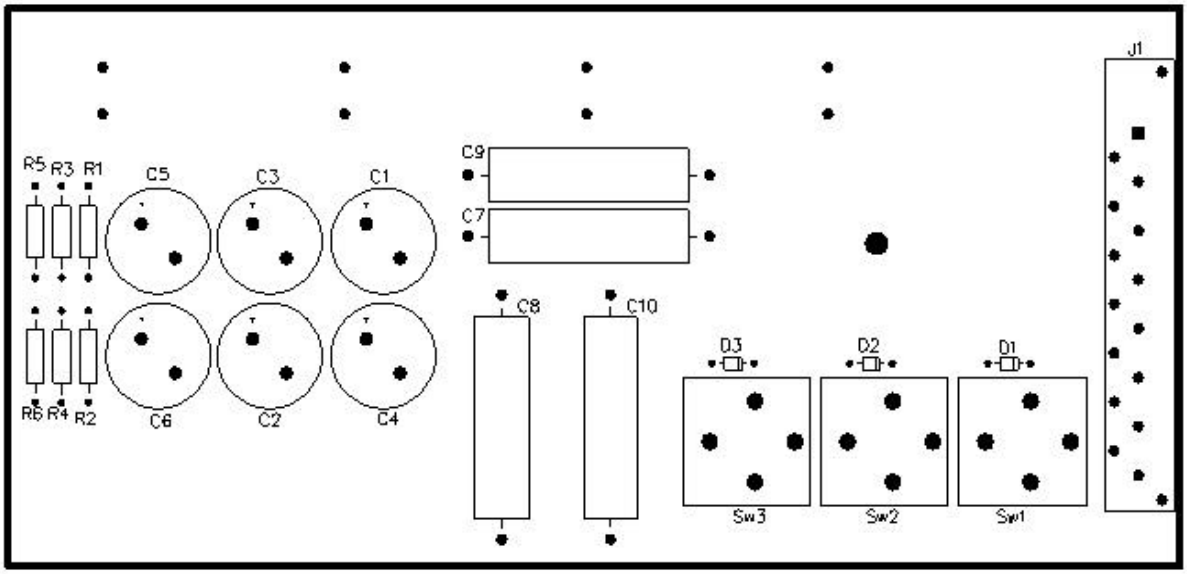


Figure E.8. Power Board component placement diagram.

Table E.2. Power Board bill of materials.

Component	Description	Manufacturer	Man. Part Number	Suggested Distributor
C1-C6	100uF, 450V Aluminum Electrolytic Cap	Panasonic	ECO-S2WB101BA	Digikey
C7-C10	0.68uF, 630V Polypropylene Cap			
D1-D3	100V, 1A rectifier	Gen. Semi.	1N4002	Digikey
J1	Rt. Angle H-type male connector	Harting	09-06-115-2911	Newark
R1-R6	150 kohm, 2W resistor	BC Components	5083NW150K0J12AFX	Digikey
Sw1-Sw3	SPST, 60A relay	P&B / Tyco	VF4-11F13	Digikey

E.4 Control Board

The Control Board is fed the power supply voltages and signals from an external signal generator, and it outputs the voltage supplies and controls signals needed for the gate driver. The input signals are initially sent into an optocoupler (U_1). This optocoupler breaks the ground loop that would otherwise be present due to the fact that both the external signal generator and the oscilloscope are earth grounded. Because the optocoupler inverts the logic, its output is then sent through an inverter (U_2). The optocoupler output is also sent to two inverting buffer chips (U_3 and U_4) to create 0-15 V logic. Using the rocker switch on the tester front panel that connects to J_4 and relays Sw_1 and Sw_2, the user can select between 5 V and 15 V logic. A rotary switch that connects to J_3 is used to select which test will be performed. Depending on the selection, the output of relays Sw3 and Sw_4 will be either ground or a logic signal. The power supplies and signals are fed through J_2 to the front panel to be accessed by the gate driver. Connections to the rest of the tester are made through J_1 to the backplane.

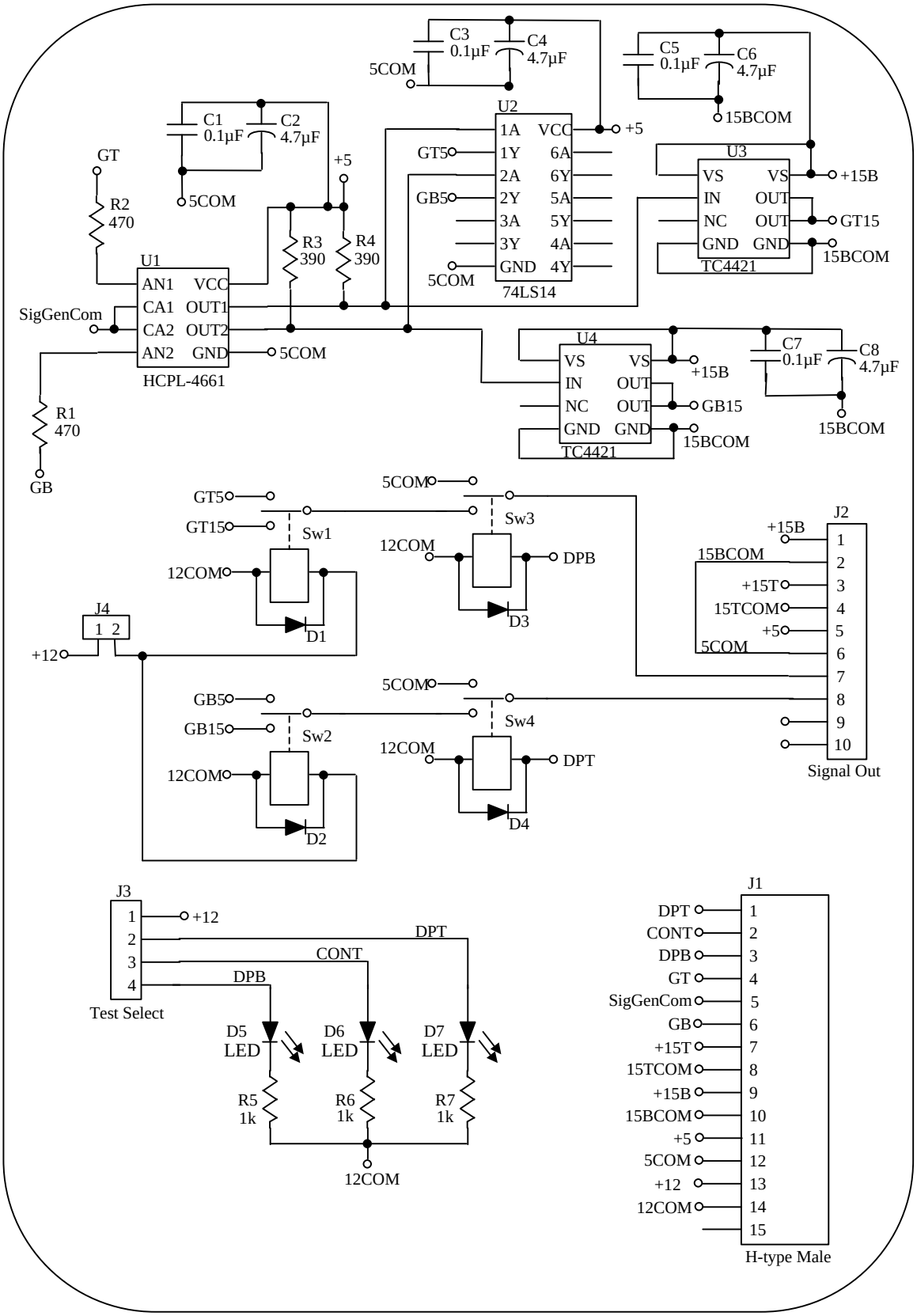


Figure E.9. Control Board schematic.

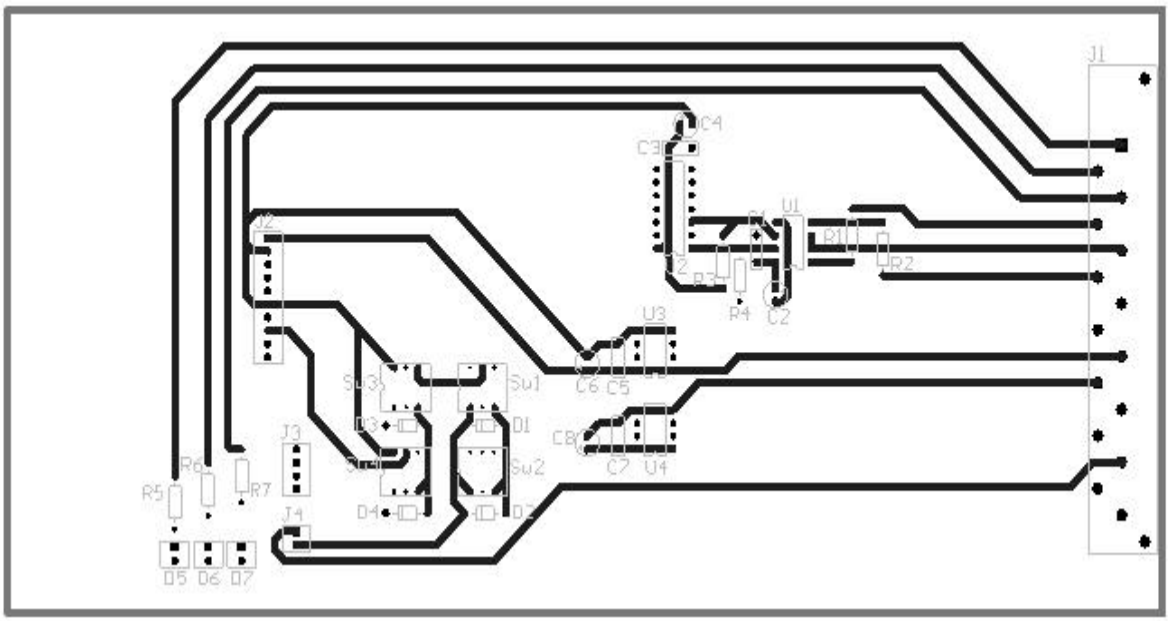


Figure E.10. Control Board top layer.

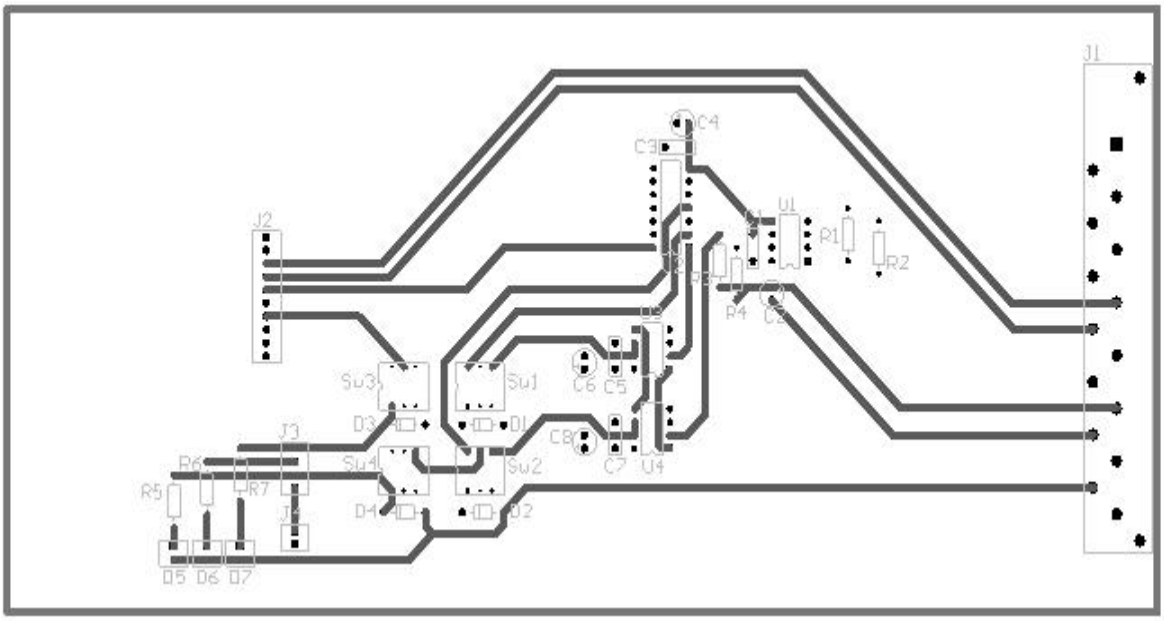


Figure E.11. Control Board bottom layer.

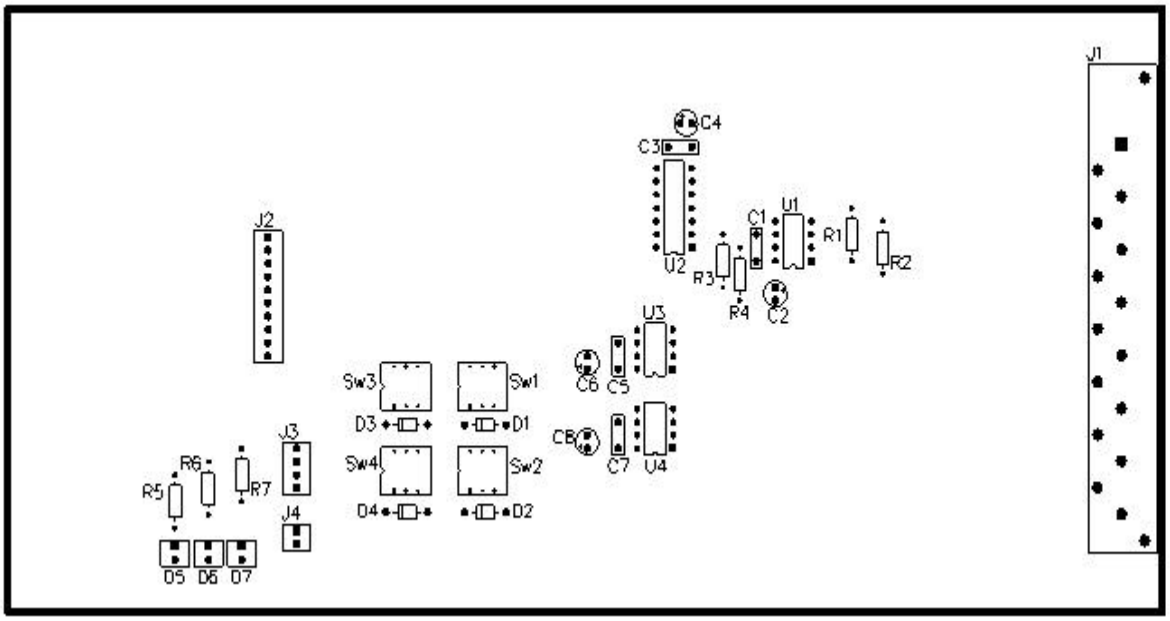


Figure E.12. Control Board component placement.

Table E.3. Control Board bill of materials.

Control Board				
Component	Description	Manufacturer	Man. Part Number	Suggested Distributor
C1,C3,C5,C7	0.1uF, 50V ceramic cap	Kemet	C317C104M5U5CA	Digikey
C2,C4,C6,C8	4.7uF, 35V tantalum cap	Kemet	T350E475K035AS	Digikey
D1-D4	100V, 1A rectifier	Gen. Semi.	1N4002	Digikey
D5-D7,J4	2-pos. straight header	Molex	22-23-2021	Digikey
J1	Rt. Angle H-type male connector	Harting	09-06-115-2911	Newark
J2	10-pos. straight header	Molex	22-23-2101	Digikey
J3	4-pos. straight header	Molex	22-23-2041	Digikey
R1,R2	470 ohm, 0.25 W resistor	Yageo	CFR-25JR-470R	Digikey
R3,R4	390 ohm, 0.25 W resistor	Yageo	CFR-25JR-390R	Digikey
R5-R7	1 kohm, 0.25 W resistor	Yageo	CFR-25JR-1K0	Digikey
Sw1-Sw4	SPDT, 2A relays	NAIS	TK1-12V	Digikey
U1	High CMR dual opto, 8DIP	Agilent	HCPL-4661	Newark
U2	Hex Schmitt-trig inverter, 14DIP	Texas Inst.	SN74LS14N	Digikey
U3,U4	9A low-side gate driver, 8DIP	Microchip	TC4421CPA	Digikey
Front Panel of Control Board				
Component	Description	Manufacturer	Man. Part Number	Suggested Distributor
mate for D5-D7,J4	2-pos. housing	Molex	22-01-3027	Digikey
mate for J2	10-pos. housing	Molex	22-01-3107	Digikey
mate for J3	4-pos. housing	Molex	22-01-3047	Digikey
pins for D5-D7,J2-J4	crimp terminals	Molex	08-50-0114	Digikey
LEDs for D5-D7	Green panel mount LED	Lumex	SSI-LXR4815GD	Digikey
connector for J2	9-pos. male D-Sub connector	AMP	747904-2	Digikey
switch for J3	12-pos. rotary switch	E-Switch	KC-52-A-01-N-L-S	Digikey
switch for J4	Rocker switch	CW Industries	GRS-4011-0076	Digikey

E.5. Gate Driver Board

The Gate Driver Board used contains two isolated drivers. The output buffer chips (U_3 and U_4) are capable of up to 12 A, and are limited to switching frequencies below 300 kHz. R_3 and R_7 will be plugs mounted on the PCB so that the gate resistance can easily be adjusted.

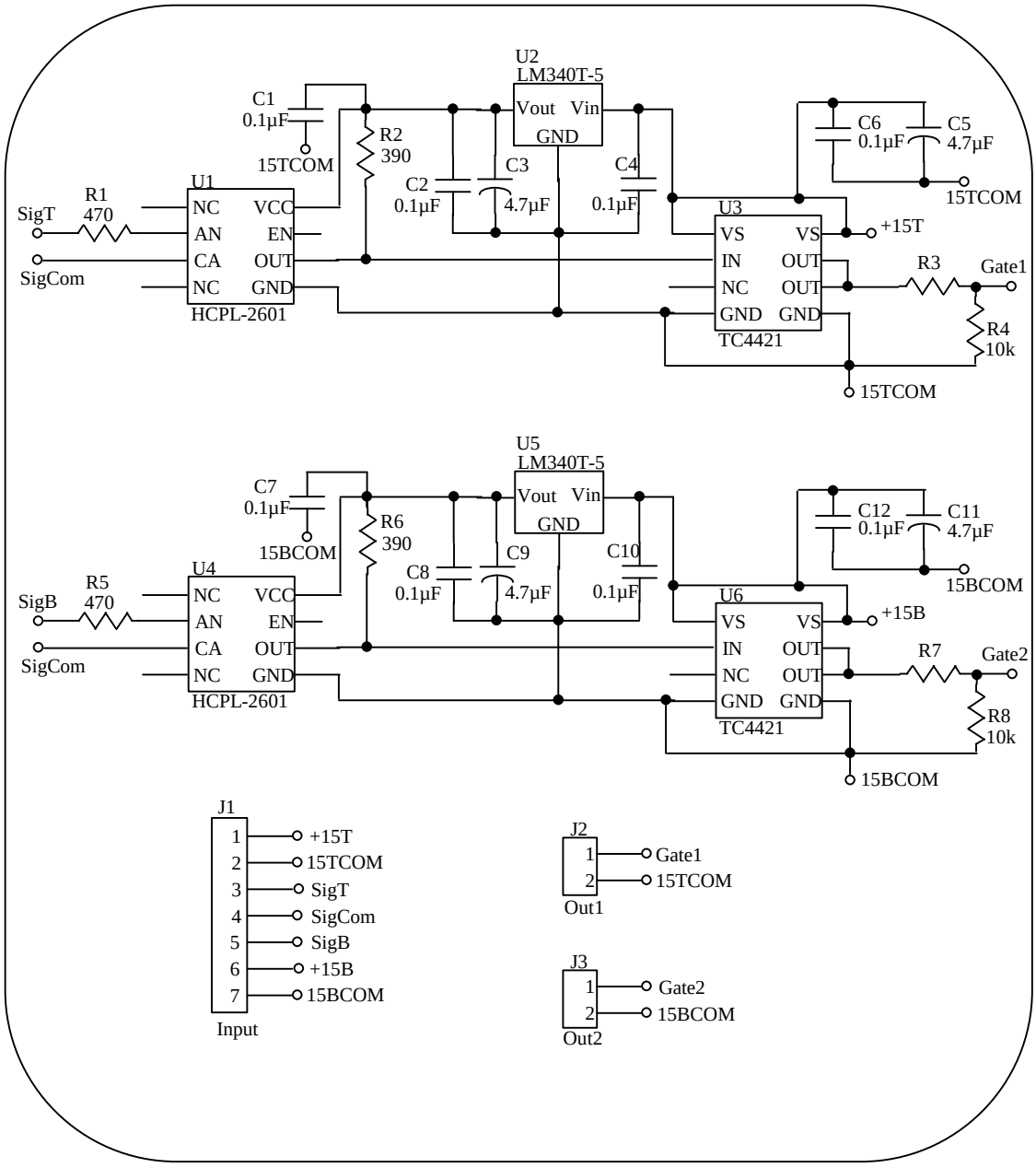


Figure E.13. Gate Driver Board schematic.

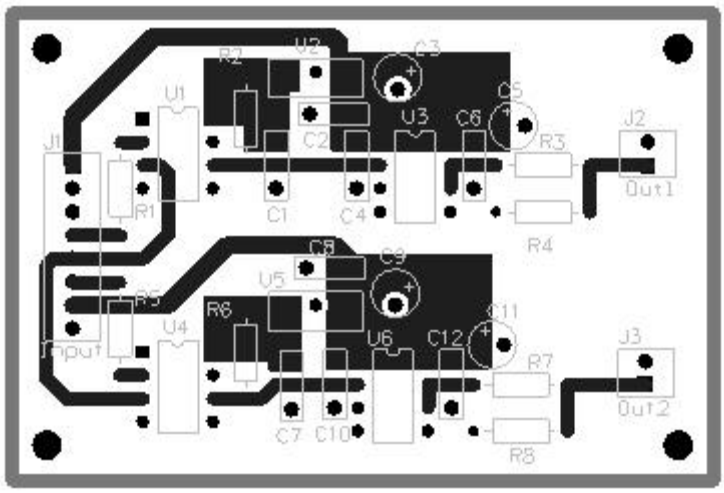


Figure E.14. Gate Driver Board top layer.

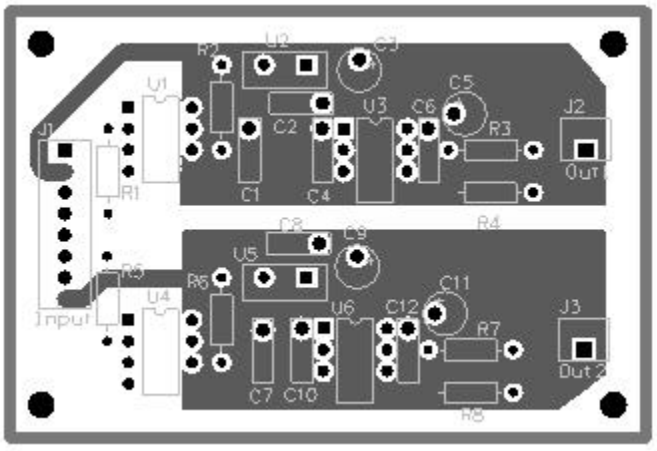


Figure E.15. Gate Driver Board bottom layer.

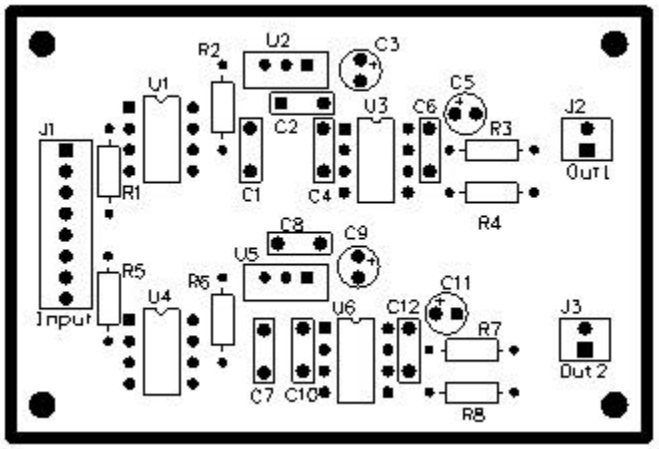


Figure E.16. Gate Driver Board component placement diagram.

Table E.4. Gate Driver Board bill of materials.

Component	Description	Manufacturer	Man. Part Number	Suggested Distributor
C1,C2,C4,C6,C7,C8,C10,C12	0.1uF, 50V ceramic cap	Kemet	C317C104M5U5CA	Digikey
C3,C5,C9,C11	4.7uF, 35V tantalum cap	Kemet	T350E475K035AS	Digikey
J1	7-pos. straight header	Molex	22-23-2071	Digikey
mate for J1	7-pos. housing	Molex	22-01-3077	Digikey
J2,J3	2-pos. straight header	Molex	22-23-2021	Digikey
mate for J2,J3	2-pos. housing	Molex	22-01-3027	Digikey
pins for J1-J3	crimp terminals	Molex	08-50-0114	Digikey
R1,R5	470 ohm, 0.25 W resistor	Yageo	CFR-25JR-470R	Digikey
R2,R6	390 ohm, 0.25 W resistor	Yageo	CFR-25JR-390R	Digikey
R3,R7	homemade from SIP plug			
R4,R8	10 kohm, 0.25 W resistor	Yageo	CFR-25JR-10K	Digikey
U1,U4	high speed opto, 8DIP	Agilent	HCPL-2601	Digikey
U2,U5	5V regulator, TO-220	Nat. Semi.	LM340T-5	Digikey
U3,U6	9A low-side gate driver, 8DIP	Microchip	TC4421CPA	Digikey

E.5 Load Board

The Load Board contains the connections for a 400 µH inductor (J_{3A} and J_{3B}), a 25 µH inductor (J_{4A} and J_{4B}), and an inductor supplied external to the tester by the user (J_{5A} and J_{5B}). A rotary switch connected to J_2 is used to select which inductor will be used. The 400 µH inductor will be used for most of the double-pulse testing, and it can be used for continuous-pulse testing for lower switching frequencies. The peak current through this inductor should be less than 50 A, and the RMS current should be less than 40 A. The 25 µH is useful for MOSFET continuous-pulse testing in the range from 100 – 300 kHz. The current in this inductor should not exceed 30 A peak and 20 A RMS. The inductor is connected to the rest of the tester through the L_1 and L_2 connections that go to the backplane.

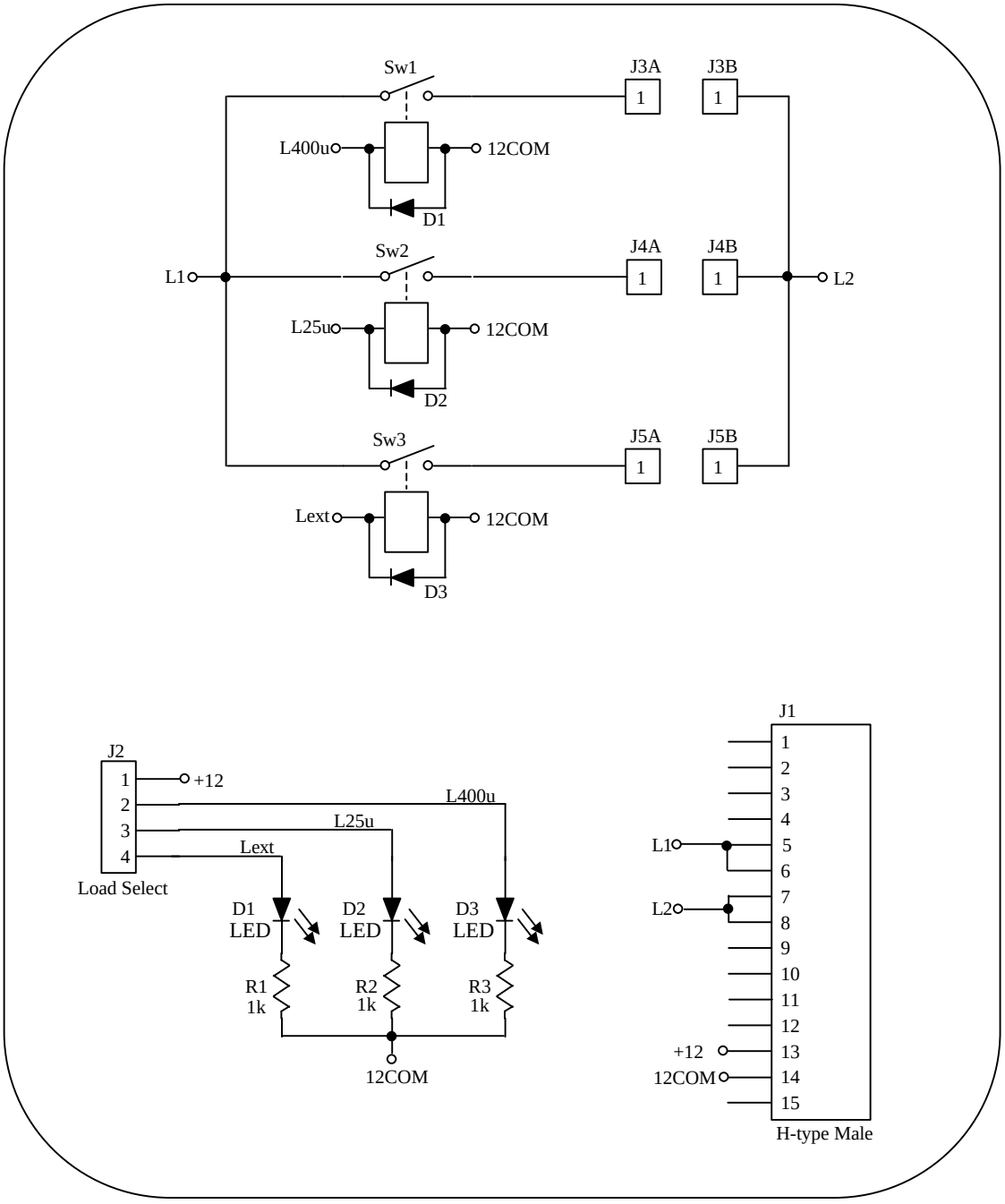


Figure E.17. Load Board schematic.

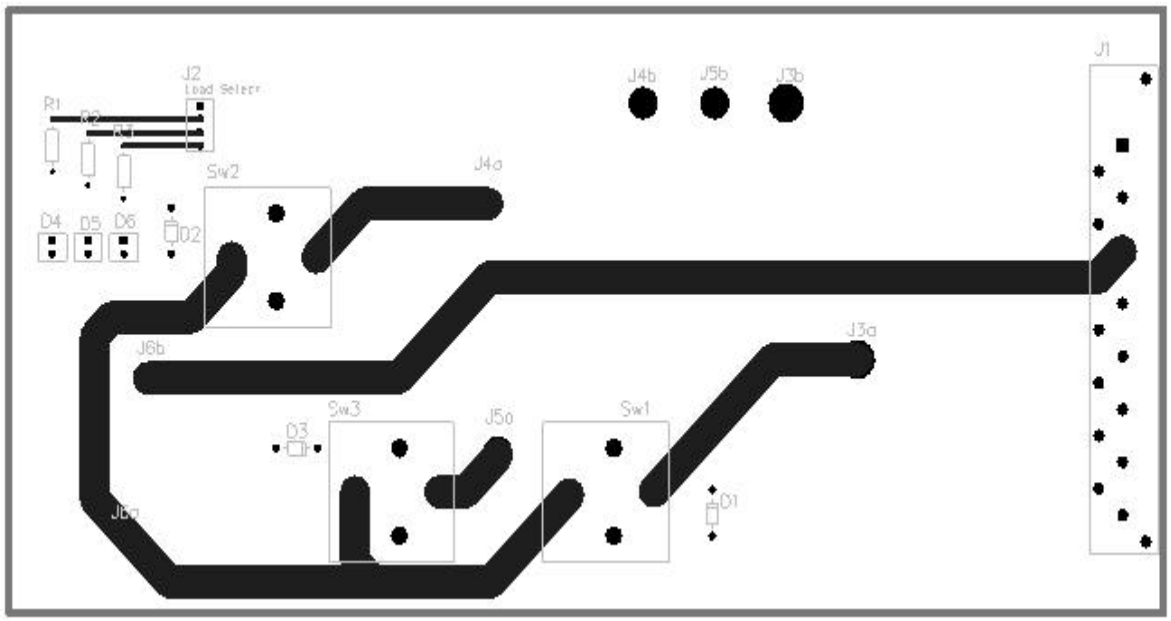


Figure E.18. Load Board top layer.

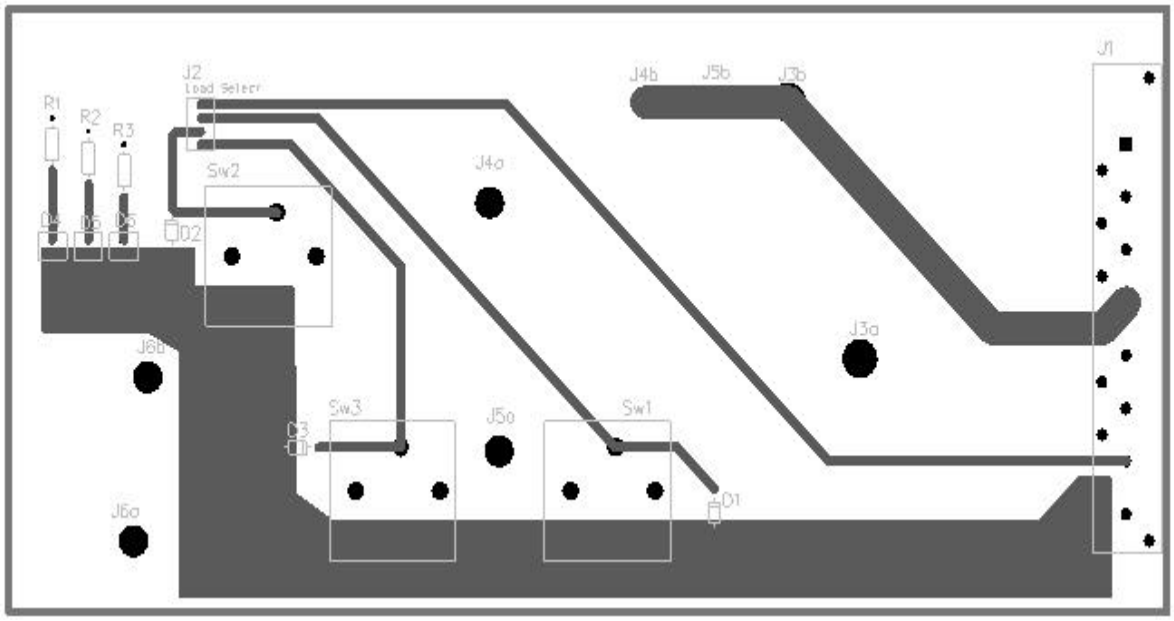


Figure E.19. Load Board bottom layer.

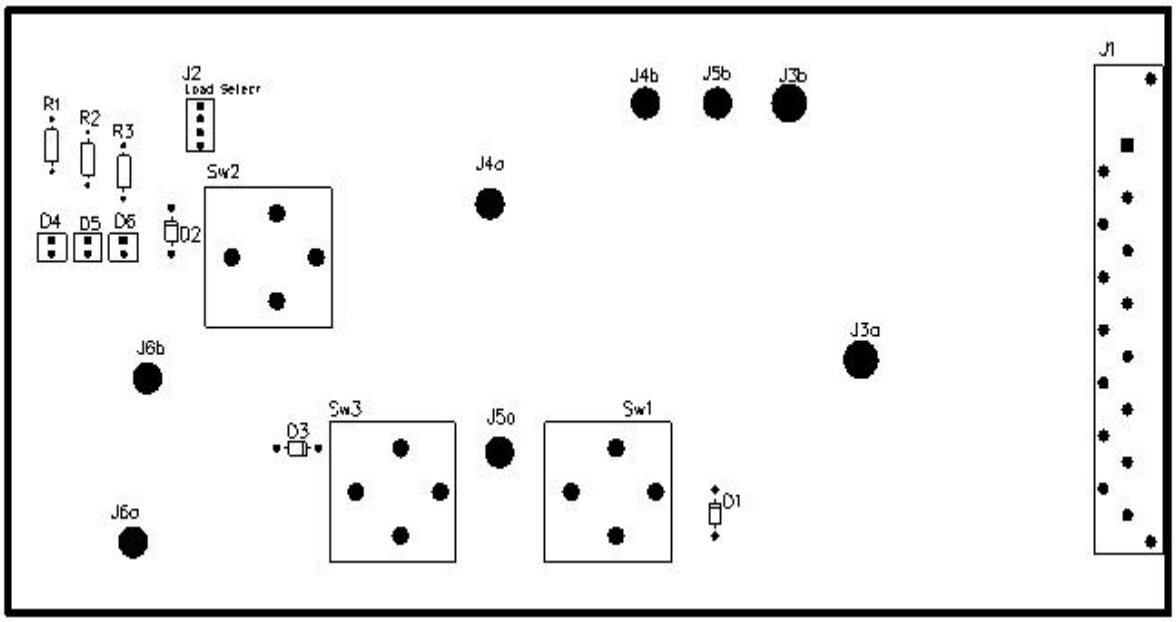


Figure E.20. Load Board component placement diagram.

Table E.5. Load Board bill of materials.

Load Board				
Component	Description	Manufacturer	Man. Part Number	Suggested Distributor
D1-D3	100V, 1A rectifier	Gen. Semi.	1N4002	Digikey
D4-D6	2-pos. straight header	Molex	22-23-2021	Digikey
J1	Rt. Angle H-type male connector	Harting	09-06-115-2911	Newark
J2	4-pos. straight header	Molex	22-23-2041	Digikey
R1-R3	1 kohm, 0.25 W resistor	Yageo	CFR-25JR-1K0	Digikey
Front Panel for Load Board				
Component	Description	Manufacturer	Man. Part Number	Suggested Distributor
mate for D4-D6	2-pos. housing	Molex	22-01-3027	Digikey
LEDs for D4-D6	Green panel mount LED	Lumex	SSI-LXR4815GD	Digikey
mate for J2	4-pos. housing	Molex	22-01-3047	Digikey
pins for D4-D6,J2	crimp terminals	Molex	08-50-0114	Digikey
switch for J2	12-pos. rotary switch	E-Switch	KC-52-A-01-N-L-S	Digikey

E.6 Power Supply Board 1 (±12 V, +5V)

The Power Supply Board 1 accepts 120 VAC and provides ±12 V and +5 V supplies. The +12 V supply is used for relay control in several of the other boards. The +5 V supply is used for the logic circuits on the Control Board and is also fed to the front panel for possible use in future gate drivers. The –12 V supply is a remnant of the original tester design.

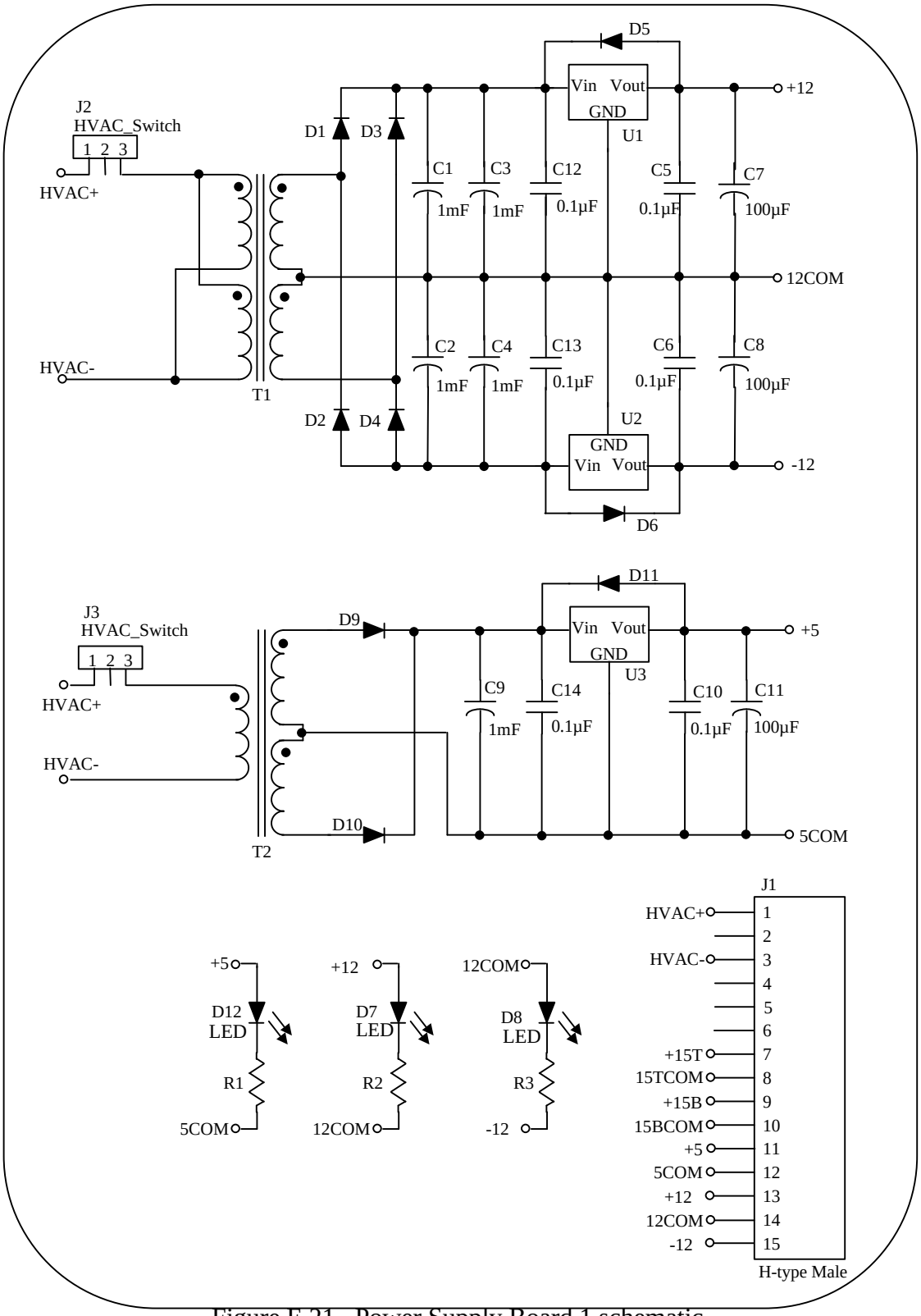


Figure E.21. Power Supply Board 1 schematic.

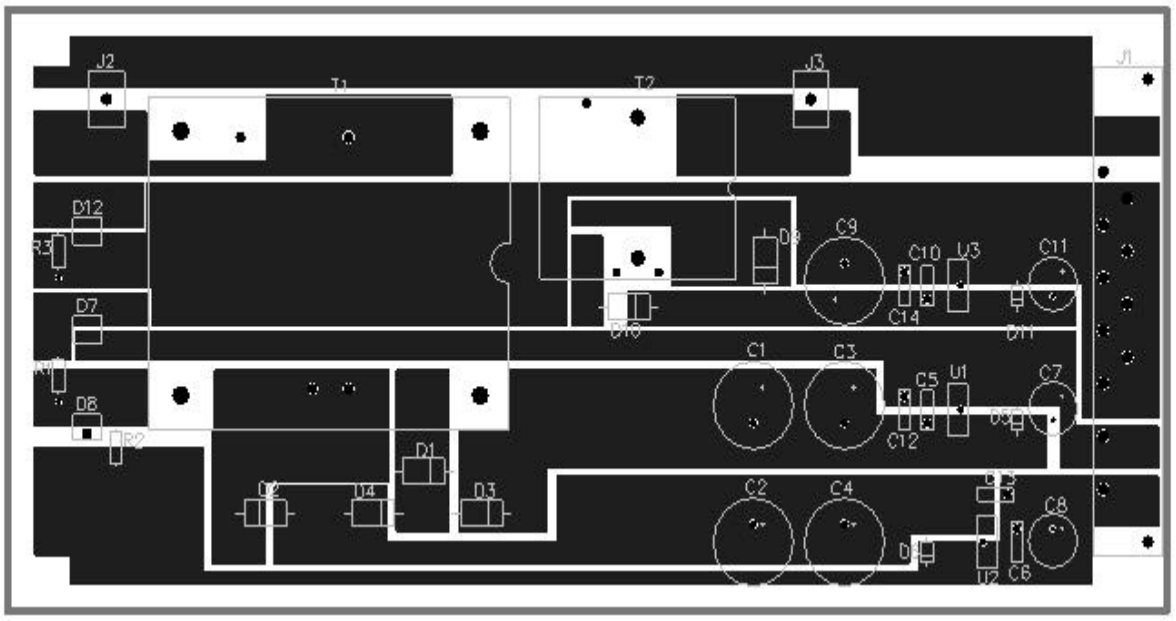


Figure E.22. Power Supply Board 1 top layer.

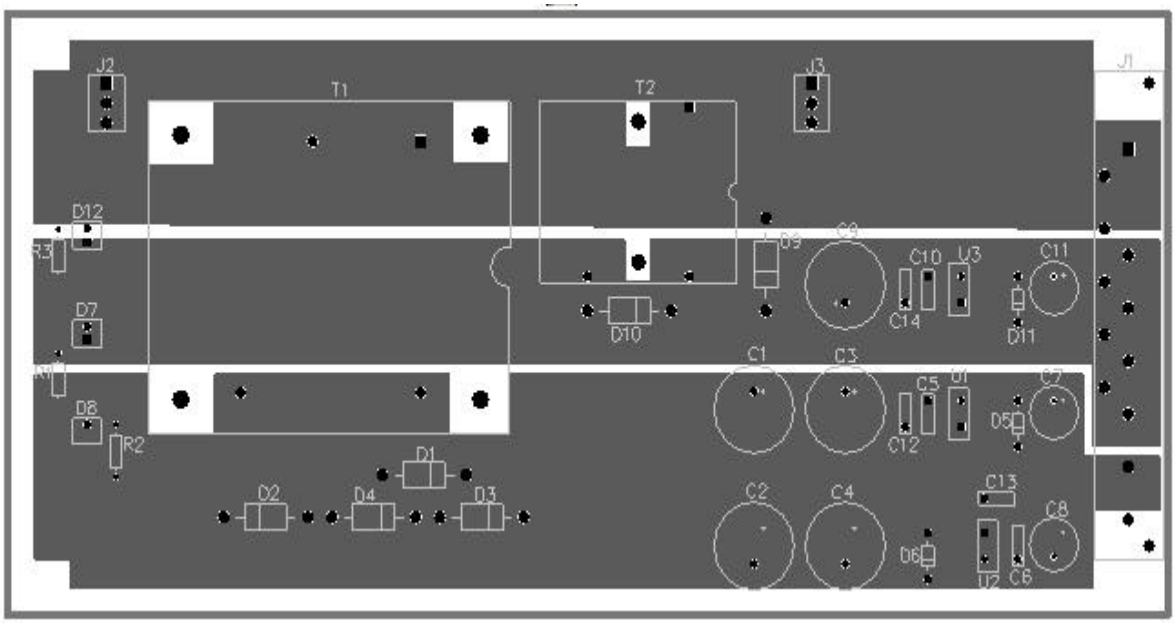


Figure E.23. Power Supply Board 1 bottom layer.

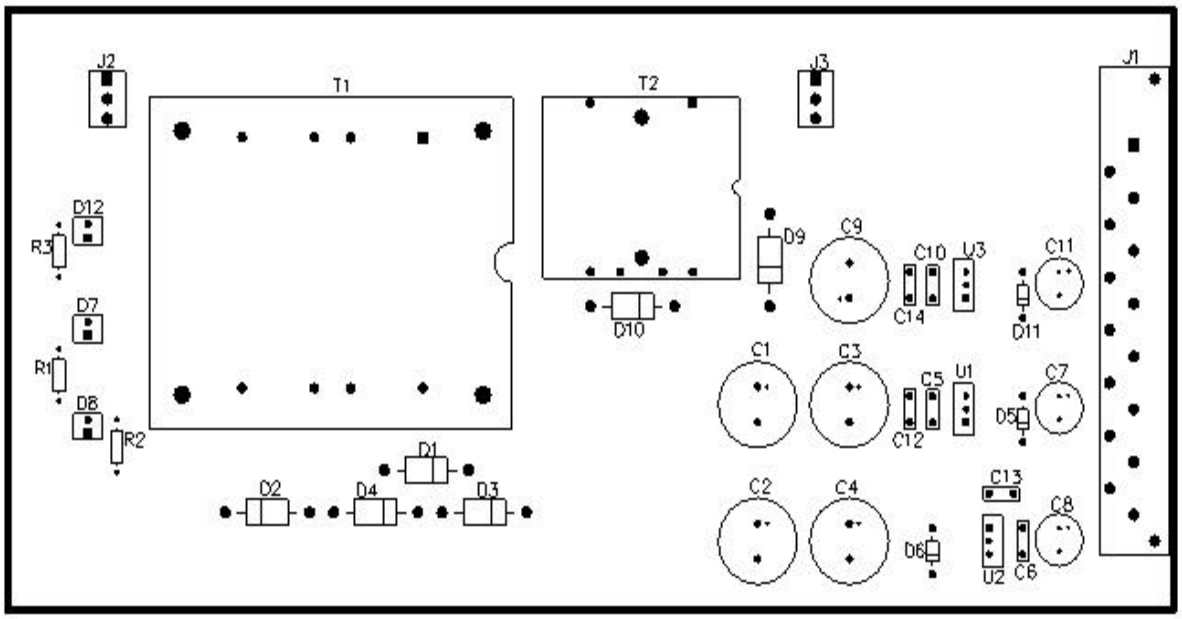


Figure E.24. Power Supply Board 1 component placement diagram.

Table E.6. Power Supply Board 1 bill of materials.

Power Supply 1 Board				
Component	Description	Manufacturer	Man. Part Number	Suggested Distributor
C1-C4,C9	1mF, 50V aluminum electrolytic cap	Panasonic	EEU-FC1H102	Digikey
C5,C6,C10,C12,C13,C14	0.1uF, 50V ceramic cap	Kemet	C317C104M5U5CA	Digikey
C7,C8,C11	100uF, 50V aluminum electrolytic cap	Panasonic	EEU-FC1H101	Digikey
D1-D4,D9,D10	40V, 5A Schottky Diode	Diodes Inc.	SR504	Digikey
D5,D6,D11	100V, 1A rectifier	Gen. Semi.	1N4002	Digikey
D7,D8,D12	2-pos. straight header	Molex	22-23-2021	Digikey
J1	Rt. Angle H-type male connector	Harting	09-06-115-2911	Newark
J2,J3	7A, 3-pos. header	Molex	26-60-4030	Digikey
T1	2 x 18VAC, 56VA transformer	Tamura	PL56-36-130B	Digikey
T2	10VAC, 6VA transformer	Tamura	3FS-420	Digikey
Front Panel for Power Supply 1 Board				
Component	Description	Manufacturer	Man. Part Number	Suggested Distributor
mate for D7,D8,D12	2-pos. housing	Molex	22-01-3047	Digikey
pins for D7,D8,D12	crimp terminals	Molex	08-50-0114	Digikey
LEDs for D7,D8,D12	Green panel mount LED	Lumex	SSI-LXR4815GD	Digikey
mate for J2,J3	7A, 3-pos. housing	Molex	09-50-8031	Digikey
pins for J2,J3	7A crimp terminals	Molex	08-50-0106	Digikey
switch for J2,J3	Rocker switch	CW Industries	GRS-4011-0076	Digikey

E.7 Power Supply Board 2 (+15V, +15V)

The Power Supply Board 2 accepts 120 VAC and produces two isolated +15 V supplies. One of the supplies is currently used in the Control Board to create the 0-15 V

logic, and it is used for one of the gate drivers on the Gate Driver Board. The other +15 V supply is used for the other gate driver.

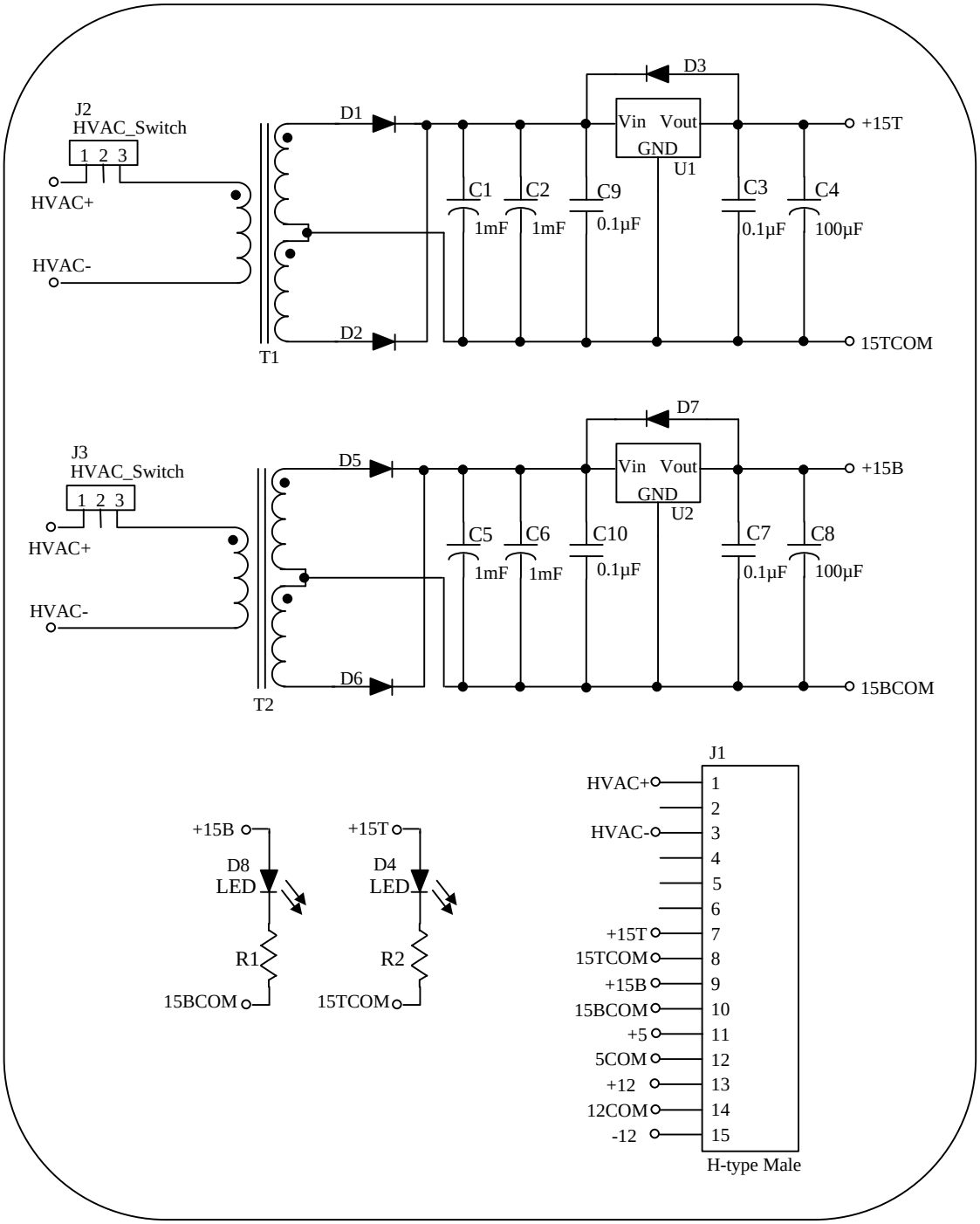


Figure E.25. Power Supply Board 2 schematic.

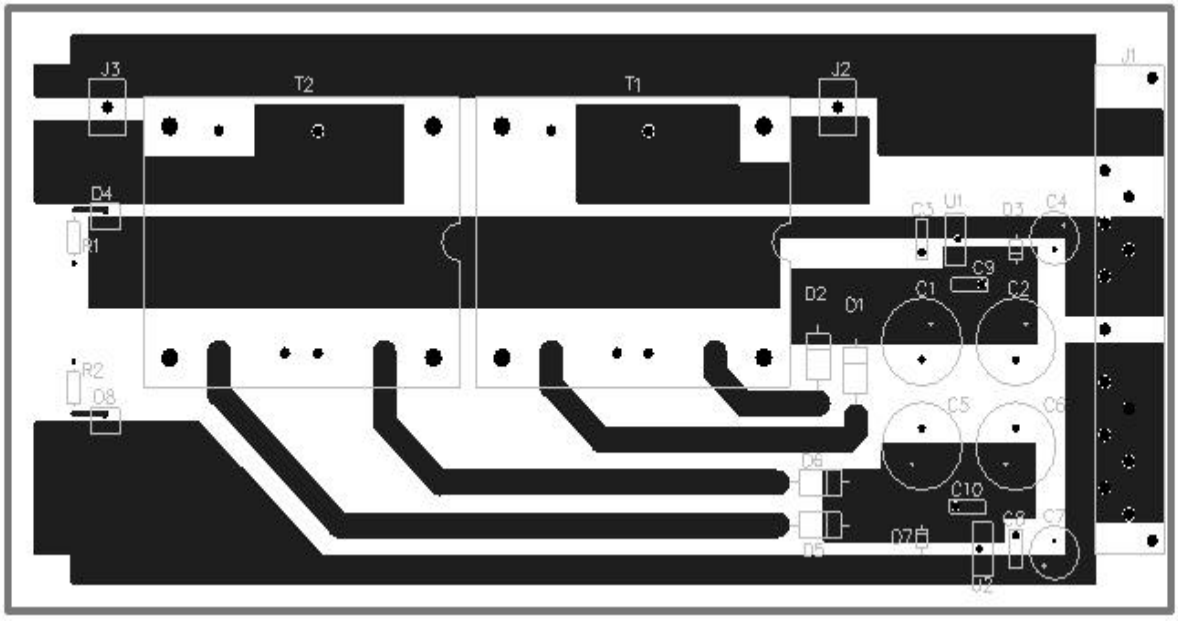


Figure E.26. Power Supply Board 2 top layer.

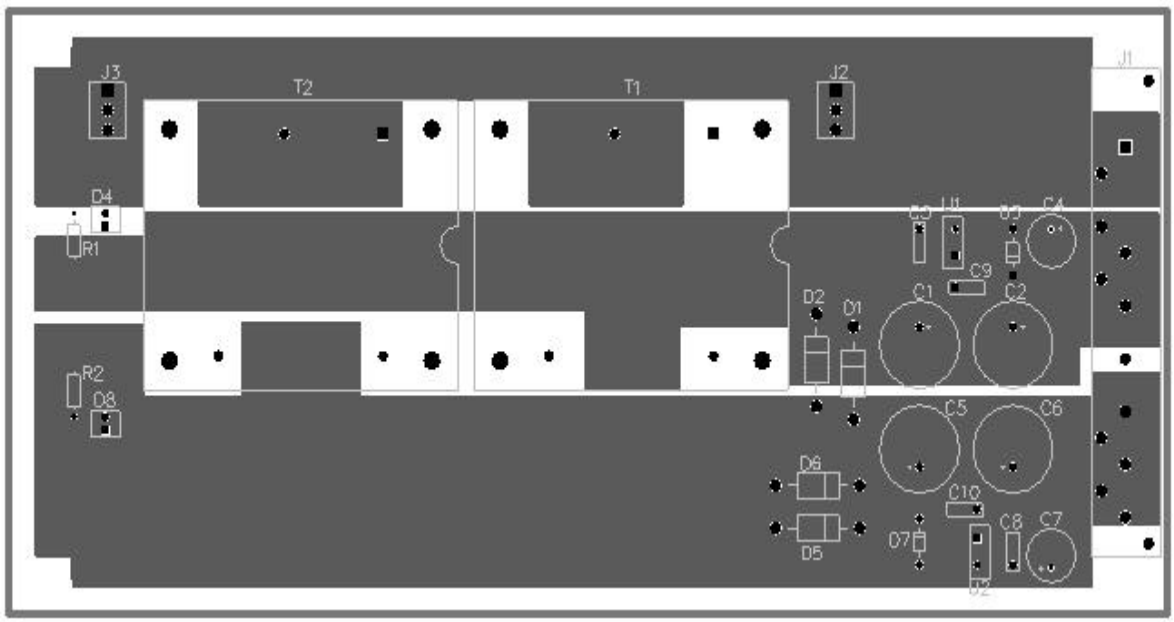


Figure E.27. Power Supply Board 2 bottom layer.

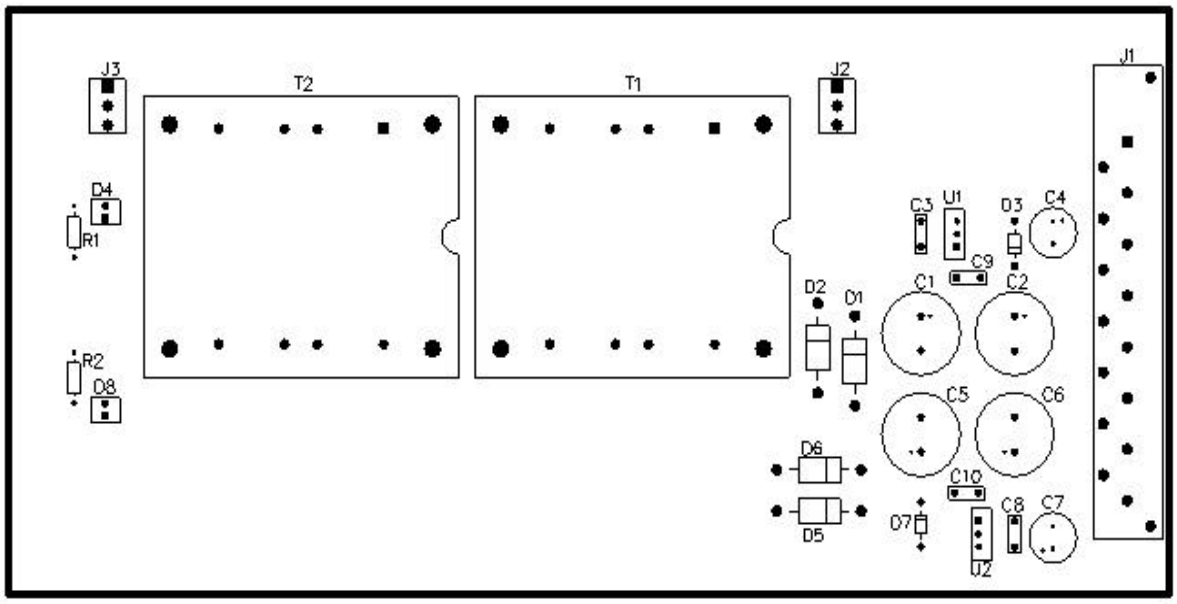


Figure E.28. Power Supply Board 2 component placement diagram.

Table E.7. Power Supply Board 2 bill of materials.

Power Supply 2 Board				
Component	Description	Manufacturer	Man. Part Number	Suggested Distributor
C1,C2,C5,C6	1mF, 50V aluminum electrolytic cap	Panasonic	EEU-FC1H102	Digikey
C3,C7,C9,C10	0.1uF, 50V ceramic cap	Kemet	C317C104M5U5CA	Digikey
C4,C8	100uF, 50V aluminum electrolytic cap	Panasonic	EEU-FC1H101	Digikey
D1,D2,D5,D6	40V, 5A Schottky Diode	Diodes Inc.	SR504	Digikey
D3,D7	100V, 1A rectifier	Gen. Semi.	1N4002	Digikey
D4,D8	2-pos. straight header	Molex	22-23-2021	Digikey
J1	Rt. Angle H-type male connector	Harting	09-06-115-2911	Newark
J2,J3	7A, 3-pos. header	Molex	26-60-4030	Digikey
T1,T2	2 x 18VAC, 30VA transformer	Tamura	PL30-36-130B	Digikey
Front Panel for Power Supply 1 Board				
Component	Description	Manufacturer	Man. Part Number	Suggested Distributor
mate for D4,D8	2-pos. housing	Molex	22-01-3047	Digikey
pins for D4,D8	crimp terminals	Molex	08-50-0114	Digikey
LEDs for D4,D8	Green panel mount LED	Lumex	SSI-LXR4815GD	Digikey
mate for J2,J3	7A, 3-pos. housing	Molex	09-50-8031	Digikey
pins for J2,J3	7A crimp terminals	Molex	08-50-0106	Digikey
switch for J2,J3	Rocker switch	CW Industries	GRS-4011-0076	Digikey

E.9. Backplane

The backplane contains the mating connectors for "J_1" on each of the other boards, and it is used to make the necessary connections between the different boards. It also accepts the DC bus voltage (J_6) that will be applied to the testbed, the 120 VAC input (J_7)

that supplies the power supply boards, and the signals from the signal generator (J_8 and J_9).

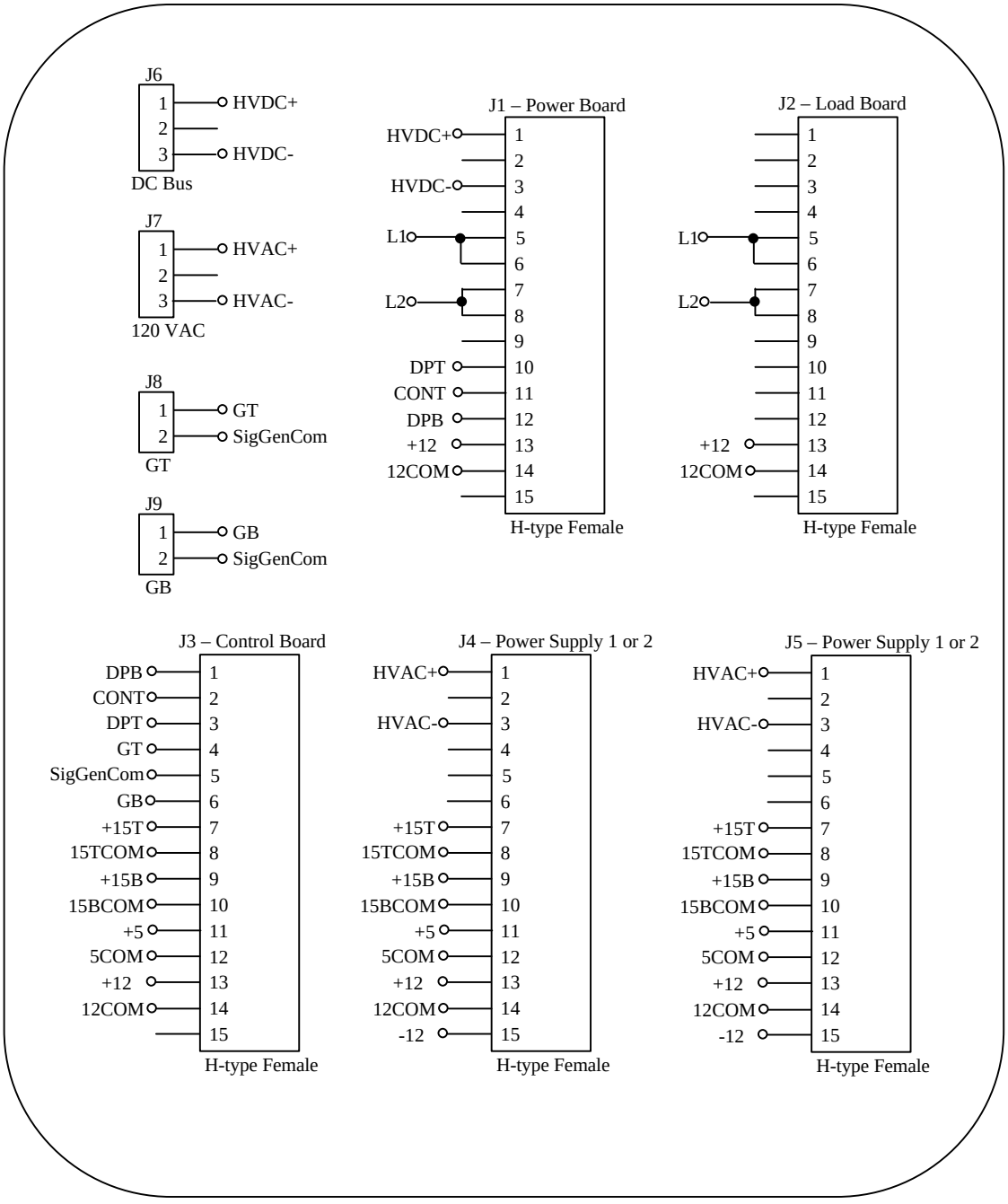


Figure E.29. Backplane Board.

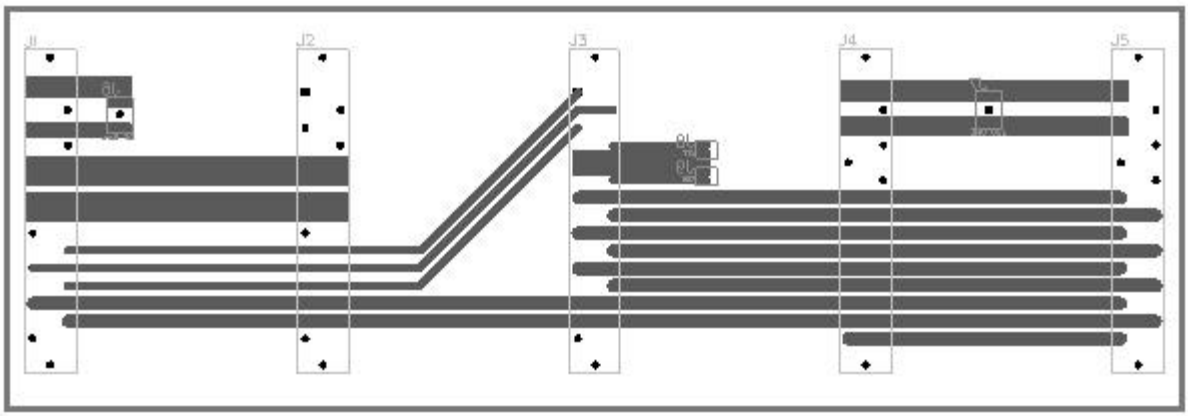


Figure E.30. Backplane bottom layer.

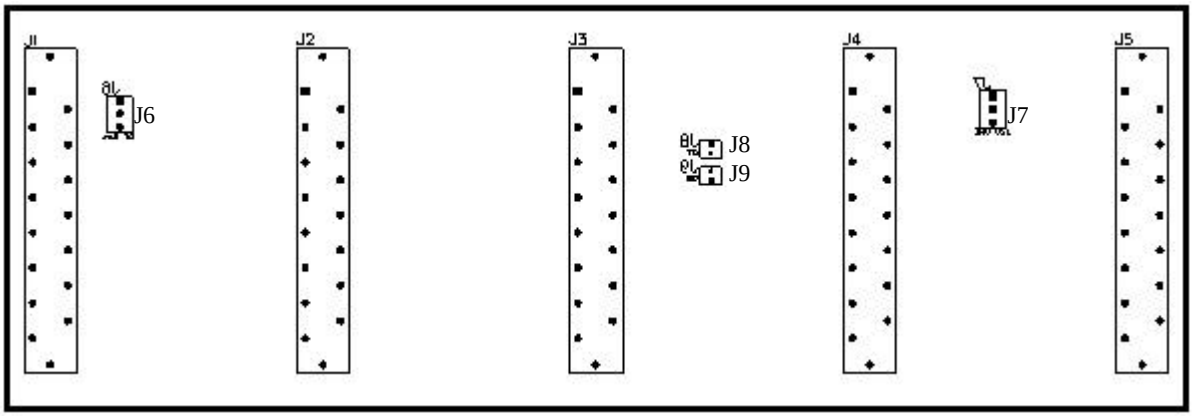


Figure E.31. Backplane component placement diagram.

Table E.8. Backplane bill of materials.

Backplane Board				
Component	Description	Manufacturer	Man. Part Number	Suggested Distributor
J1-J5	H-type female backplane connector	Harting	09-06-215-2821	Newark
J6,J7	7A, 3-pos. header	Molex	26-60-4030	Digikey
J8,J9	2-pos. straight header	Molex	22-23-2021	Digikey
Backplane Board Accessories				
Component	Description	Manufacturer	Man. Part Number	Suggested Distributor
mate for J6,J7	7A, 3-pos. housing	Molex	09-50-8031	Digikey
pins for J6,J7	7A crimp terminals	Molex	08-50-0106	Digikey
mate for J8,J9	2-pos. housing	Molex	22-01-3047	Digikey
pins for J8,J9	crimp terminals	Molex	08-50-0114	Digikey

Vita

Joseph “Brandon” Witcher was born in Newport News, VA on March 29, 1979. He grew up in Gloucester County, VA and graduated from Gloucester High School in June of 1997. Brandon continued his education at Virginia Polytechnic Institute and State University, pursuing a Bachelor of Science degree in Electrical Engineering with a minor in Mathematics. In the fall of 2000, he was admitted to the combined MS/BS program, and he began work as a research assistant for the Center for Power Electronics Systems the following spring. He graduated with his BSEE in May of 2001. He continued his research with CPES concentrating in the switching characterization of Integrated Power Electronics Modules. Upon completion of his Master of Science in Electrical Engineering, Brandon will begin full-time employment with Sandia National Laboratories.