# Improvement of Sigma Voltage Regulator

# — A New Power Architecture

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## (Abstract)

With lower output voltage (lower than 1V) and higher output current (more than 160A) required in the near future, the voltage regulators for the microprocessors, a kind of special power supplies are facing more and more critical challenges to achieve high efficiency and high power density. 90% plus efficiency for CPU VRs is expected from industry not only for the thermal management, but also for saving on electricity costs, especially for the large data-center systems. At the same time, high power density VRs are also desired due to the increasing power consumption of microprocessors as well as the precious space on CPU motherboard.

Current multi-phase Buck VR has its limitation to achieve 90% plus efficiency. With the state of art devices, the single-stage 12V/1.2V 600kHz Buck VR achieves 85% to 86% efficiency at full load condition. In addition, for the future lower output voltage application, the Buck efficiency will drop another 3~4% due to the extreme small duty cycle. From the power density point of view, due to the switching frequency limitation (normally, from 300 kHz to 600 kHz for typical CPU VRs) for acceptable efficiency performance, the multi-phase Buck VR is unable to ensure a small size since it needs bulky output capacitors to meet the challenging transient requirement as well as the output impedance requirement with relatively low bandwidth design.

To attain high efficiency and high power density at the same time, in-series two-stage power architecture was proposed. By cutting the single stage into two and utilizing the low voltage devices, the in-series two stages can achieve around 87% efficiency which is similar as single stage with second-stage operating at 1 MHz for less cost. Compared with the in-series one, the other two-stage power architecture is called "Sigma" architecture which is composed by an unregulated converter (DCX) and a regulated buck converter, with a special connection where the inputs are in series while outputs are paralleled. Through this topology, unlike the in-series two-stage where both two stages deliver the full load power, the power will be distributed between unregulated DCX and regulated Buck. If the unregulated DCX can achieve high efficiency, let most power be handled by it and just small power from buck, the Sigma architecture can achieve high efficiency performance based on this concept.

The design consideration and process had been investigated by CPES previous graduates. By the designed 1.2V/120A Sigma VR circuit, approaching 90% efficiency was achieved which is around 3~4% efficiency higher than state of the art multi-phase Buck VR. However, it is not the optimal design for best efficiency performance, the improvement methods for higher efficiency is deeply considered and the efficiency potential benefit of this special structure will be clarified in this thesis. Besides the efficiency interest, transient performance of Sigma VR is also a challenging issue needed to be addressed. The state of the art Buck VR needs a bunch of output bulk capacitors to meet the stringent output impedance requirement from Intel and those output bulk capacitors occupy too much space in the motherboard. For Sigma architecture, through the

help of the low impedance DCX which can achieve faster current dynamic response, some low voltage bulk capacitors could be replaced by smaller input high voltage capacitors. It is still not clear for us to identify how input capacitor impacts the DCX dynamic current response and how to best choose this impact factor.

This thesis will investigate the faster DCX dynamic current performance of Sigma VR, and explain the dynamic impacts from input capacitors, from control design and from DCX impedance $L_{out}$. The high voltage capacitors could provide energy through low impedance DCX to deal with the transient load with smaller capacitance, resulting less total cost and footprint with conventional Buck solution. Low impedance DCX is also a desire for achieving fast current response for providing a "non-obstacle" path when energy transferring from input capacitors. The control also has the impact to the DCX current response when the bandwidth is higher than certain frequency. The transient benefit will also be discussed from impedance perspective.

In order to improve the efficiency and power density of Sigma VR, several methods are proposed. As a critical component of DCX, the transformer design determines the performance of Sigma VR both to efficiency and power density. By optimizing the transformer design to achieve lower winding loss and smaller leakage inductance, the higher efficiency and faster transient DCX can be obtained. Changing the output capacitors to ceramic ones is helpful when control bandwidth is greater than 100 kHz for both lower cost and smaller footprint. Continually pushing bandwidth can reduce the required output ceramic capacitor number further. In addition, from the study of the loss breakdown, by adjusting the energy ratio of DCX and Buck can achieve higher efficiency based on current

device level. What is more, with the same simple concept of adjusting power ratio of DCX and Buck, with the development of devices in the future as well as higher efficiency DCX, Sigma architecture will be more attractive for future's lower output voltage VR application. And it will also be more efficient considering higher than 12V input bus voltage by letting high efficiency DCX handle more power. Utilizing this characteristic, changing the power system delivery architecture from AC input to the microprocessors, the end to end efficiency could be improved.

**TO MY PARENTS**

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# Chapter 1. Introduction and Background

## 1.1 Evaluation of Microprocessors and Voltage Regulators

The microprocessor, also known as CPU, is widely used in many applications such as computer systems, embedded systems, and handheld devices. Since 1971, when the first microprocessor, Intel's 4-bit 4004 chipset, was released, more and more transistors have been integrated into the microprocessor, following Moore's Law, which indicated that the number of transistors on an integrated circuit doubles roughly every two years. Figure 1-1 shows the historical data of transistor number integrated into Intel's microprocessor [2] . The dual-core processor, which was released in 2006, has more than one billion transistors which had about 1 million times more than the first 4004 microprocessor.

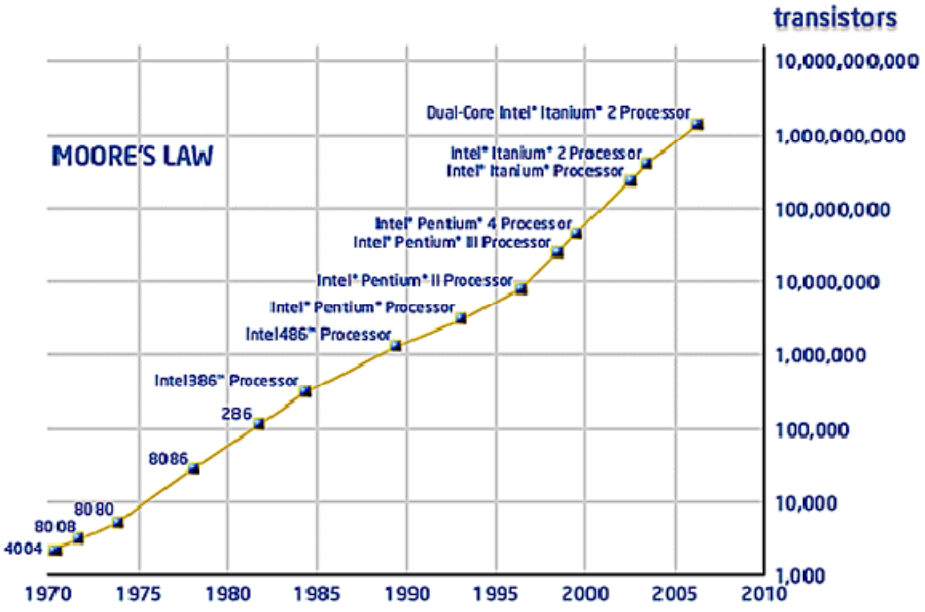



**Figure 1-1 The number of transistor integrated on the die of Intel microprocessor**

The microprocessor can achieve better performance when more transistors are integrated. Figure 1-2 shows the speed of Intel microprocessors using millions of instructions per second (MIPS) [2] . The target of Intel is to build a microprocessor with ten trillion instruction per second (TIPS) by 2015, which is about ten billion times faster than the first 4004 microprocessor.

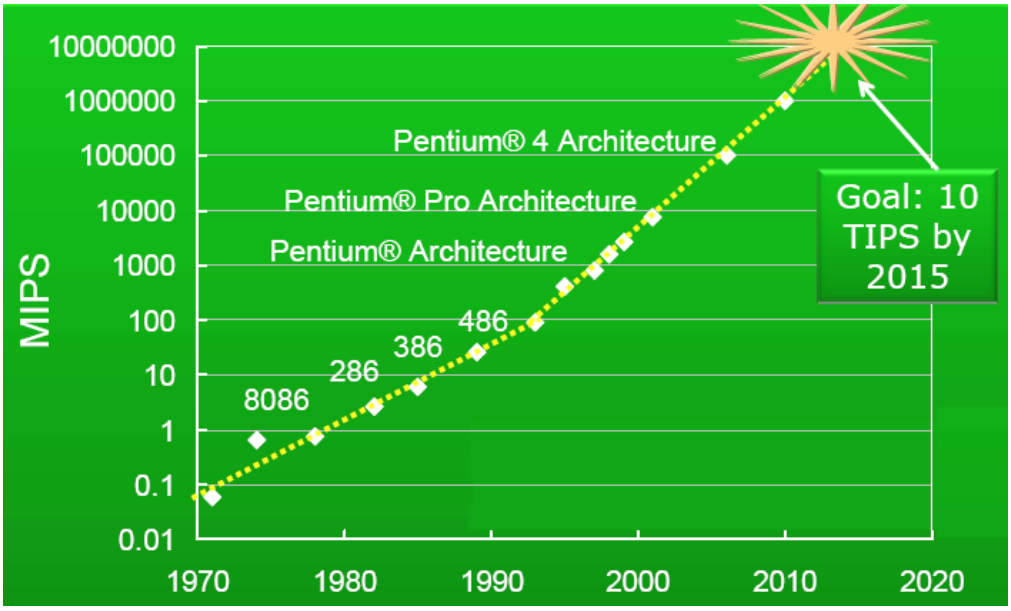



**Figure 1-2 The speed of Inter microprocessors**

Following the Moore's Law trend, higher and higher current is needed from the microprocessor chips because of the increasing number of the transistors. The special power supplies, the voltage regulators of these improving devices are facing stringent thermal management challenge due to such high current requirement. With a single microprocessor, a device's power consumption is roughly proportional to the clock frequency, the total lumped capacitance C of total transistors and the square of the core voltage as following equation $P_{CPU} \propto C \cdot V_{cc}^2 \cdot f$ shows [4] .

$$P_{CPU} \propto C \cdot V_{cc}^2 \cdot f$$

In order to get a higher operating speed, the clock frequency must be higher, but the power consumption increases accordingly. What is more, the scaling of microprocessors will increase the lumped capacitance C, and the power consumption increase as well. This power consumption eventually results in greater heat dissipation, which is a huge challenge for the thermal management of the microprocessors.

Starting in 2005, Intel changed the microprocessor structure from the single core to core multi-processor (CMP). This product uses multiple cores on the die, and includes dual-core and quad-core processors [2] . Assuming the maximum performance of the single core is 1.00x with a power consumption of 1.00x, in order to increase the performance to 1.13x, the clock frequency must be increased by 20% and the supply voltage ($V_{cc}$) should be increased proportionally. The power consumption is increased as 1.73x (=$1.2^3$). Meanwhile, if the clock frequency is reduced by 20%, the supply voltage can be reduced by 20% and the power consumption becomes 0.51x (=$0.8^3$) with 0.87x performance. The dual-core processor uses two under-clocked cores, which increases the performance to 1.73x, with almost the same power consumption. Since the supply voltage is reduced, the processors demand more current. With more cores, the supply voltage is further reduced, and the current becomes higher. Figure 1-3 shows the power roadmap of Intel's microprocessors, which were surveyed in [4] . As can be seen, in the near future around 2014, the CPU core voltage will drop below 1V and the CPU core current demand will be larger than 160A. Facing such a high current and low voltage load, the CPU

voltage regulators are facing critical challenges including achieve high efficiency, high power density at the same time low cost.

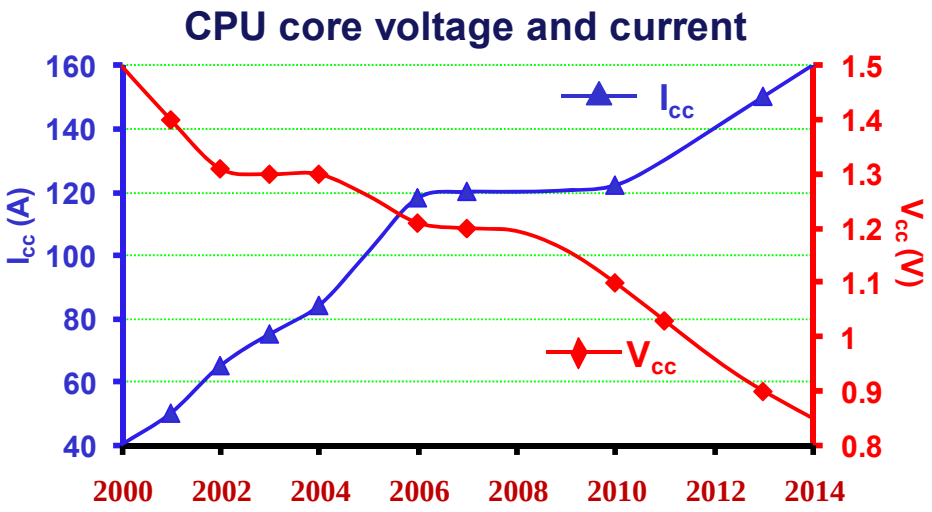



**Figure 1-3 Intel microprocessor's power roadmap**

## 1.2 Challenges for the CPU Voltage Regulators

### *1.2.1 High Efficiency Requirement*

As described in Figure 1-3, with the lower output voltage and higher current demand of the CPUs, the thermal management of this power system will become much more challenging. This problem is even more severe in a data center, where too many CPUs are used for high performance. The cost for powering and cooling the data-center increases much faster than server itself spending due to the high current requirement for CPUs [5] .

Despite of the thermal management, in order to save energy consumption as well as electrical bill, it is important to improve the efficiency of each stage of the power delivery system. Web giant Google™ proposed to improve their entire server power system's

efficiency to 90% [6] . They estimate that if this is deployed in 100 million PCs running for an average of eight hours per day, this new standard would save 40 billion kilowatt-hours over three years, or more than $5 billion at California's energy rates. However, this efficiency target is not that realistic, so they decreased the target to 85%. Assuming the PSU can achieve 95% efficiency, the VR must provide at least 90% efficiency! A similar efficiency requirement is proposed by IBM [7] and Intel [8] .

The interleaving multi-phase Buck VR is the current solution for CPU voltage regulator [9] which is shown in Figure 1-4. By paralleling several synchronous buck converters and phase shifting their drive signals, the interleaving approach can reduce both the input and output current ripples, improve the transient response, and distribute power and heat [10][11].

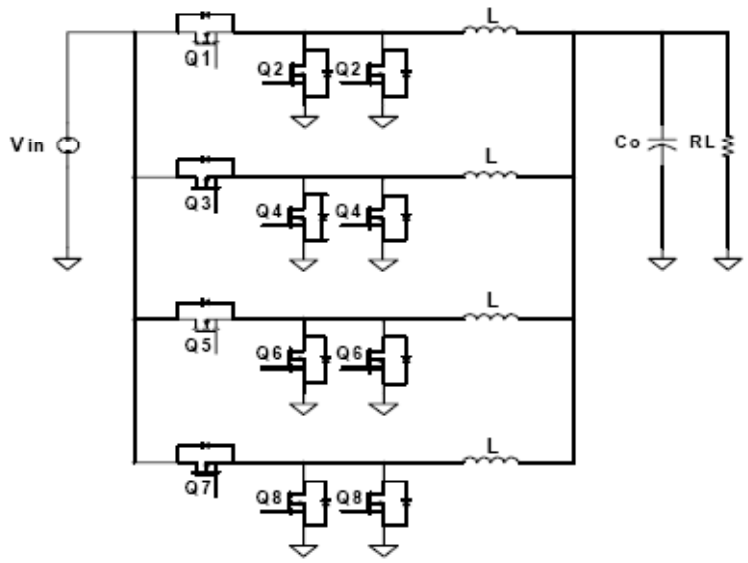



**Figure 1-4 A four-phase interleaving multi-phase Buck VR**

Through the effort from industry, the typical single-stage 12V/1.2V 120A 600 kHz Buck VR efficiency has increased from 75% to 86% at full load. Figure 1-5 shows two

examples of Buck VR efficiency curve, respectively, using Renesas' RJK0305 for top switch and RJK0301 for bottom switch and using the more advanced packaging devices IR's IRF6710 top switch and IRF6795 for bottom switch. Even with the most advanced packaging devices, there is still a 2% gap between the state-of-the-art Buck VR efficiency and the desired efficiency target.

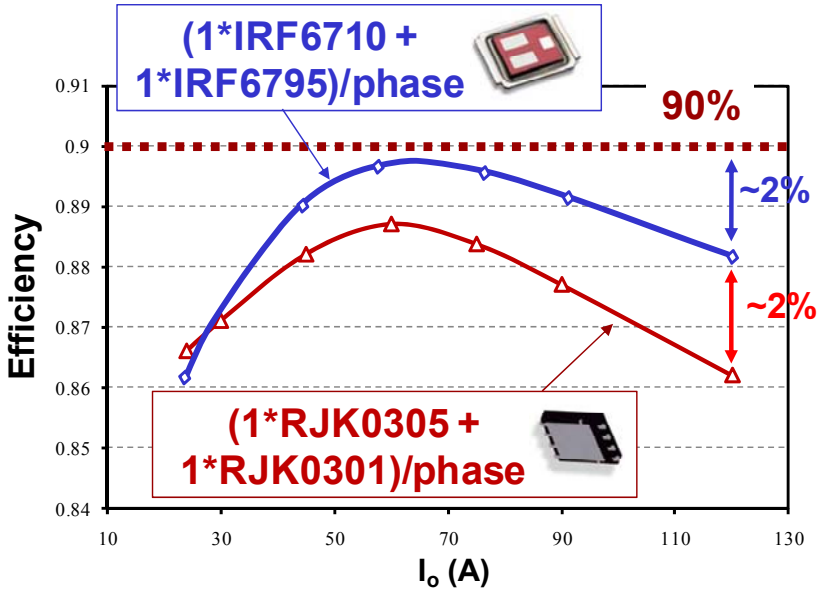



**Figure 1-5 Buck VR efficiency curves with different packaging devices**

The Buck VR efficiency performance becomes even worse for future's lower output voltage application because of the extremely small duty cycle [12]. Assume that the output voltage drops to 0.8V, applying the single stage Buck VR from 12V bus voltage, the duty cycle will be reduced to around 0.07. Using the same devices as mentioned above, the respective efficiency will drop another 3~4% at 120A which is shown in Figure 1-6. Thus, the efficiency target between 90% will be larger for future lower output voltage case.

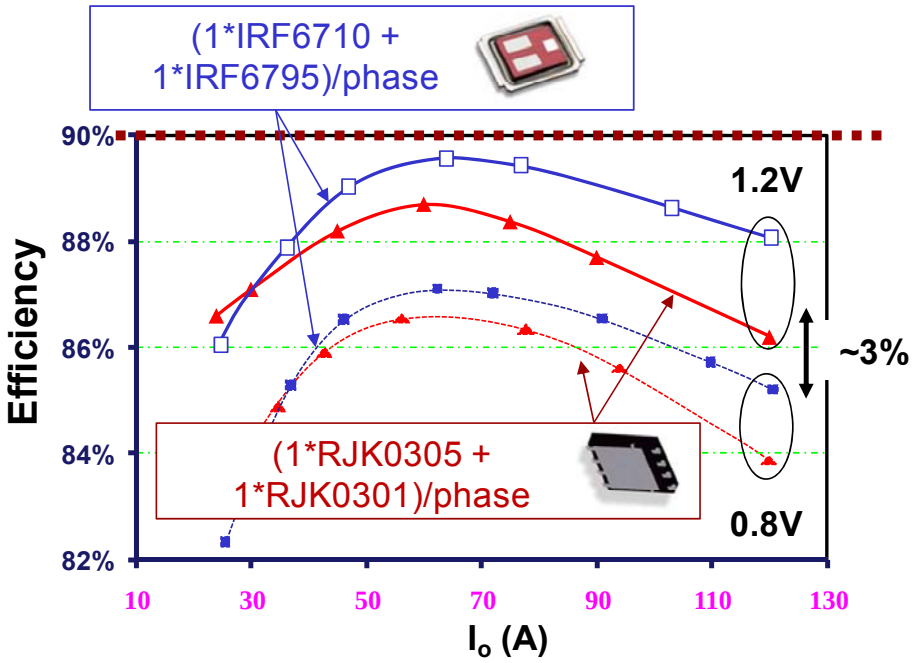



**Figure 1-6 Buck efficiency with lower output voltage**

### *1.2.2 Transient Requirement and CPU Output Capacitors*

Despite of the efficiency requirement, today's VR faces the stringent challenge of a strict transient response requirement. In the Intel VRD 11.0 specification, the maximum current slew rate is 1.9A/ns at the CPU socket [13] [14]. Before talking the transient specification, Figure 1-7 shows the VR output load line from the Intel VRD 11.0 specification which is a special requirement for CPUs. The vertical axis is the VR output voltage deviation from the voltage identification (or VID, which is a code supplied by the processor that determines the reference output voltage), and the horizontal axis is the CPU current ($I_{CC}$). The maximum, typical and minimum load lines are defined by following equations:

$$V_{\max} = VID - R_{LL} \cdot I_{CC}$$
$$V_{typ} = VID - R_{LL} \cdot I_{CC} - TOB$$

$$V_{\min} = VID - R_{LL} \cdot I_{CC} - 2 \cdot TOB$$

Where $R_{LL}$ is the load-line impedance and TOB is the tolerance band. The VR output voltage should be within this load line band for both static and transient operation.

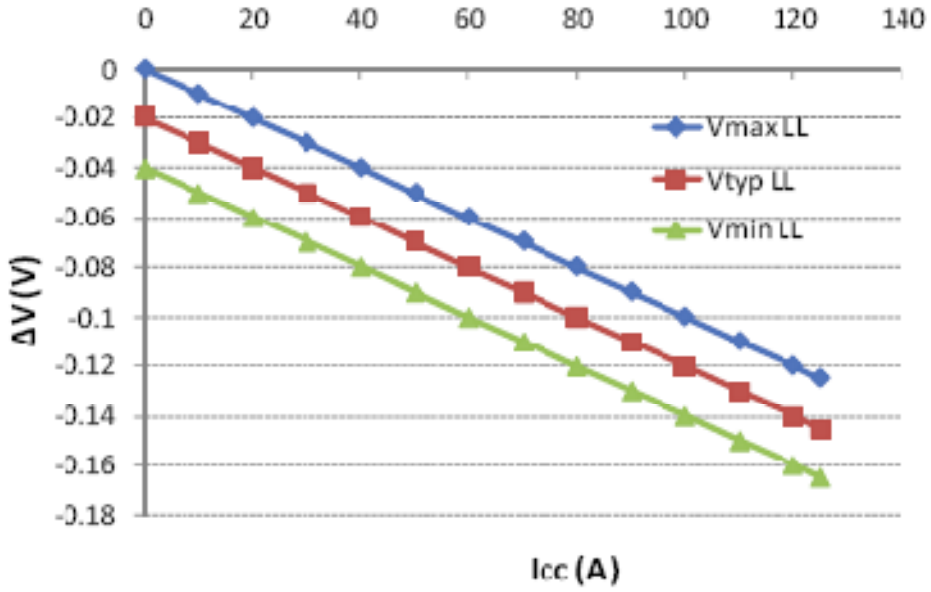



**Figure 1-7 Load-line specifications from Intel VRD 11.0**

Figure 1-8 shows the relationship between the load-line specifications and the time domain waveforms [13]. When the CPU current ($I_o$=$I_{CC}$) is low, the VR output voltage should be high, and when the CPU current is high, the VR output voltage should be low. This is achieved by the VR controller, which is known as the adaptive voltage positioning control (AVP). The VR output must also follow the load line during the transient, with one exception. During the load step-down transient, the VR output voltage can be over $V_{max}$ load line for 25us. This overshoot should not exceed the overshoot reliefs which are VID+50mV in the VRD 11.0 [13] and 11.1 [14] specifications.

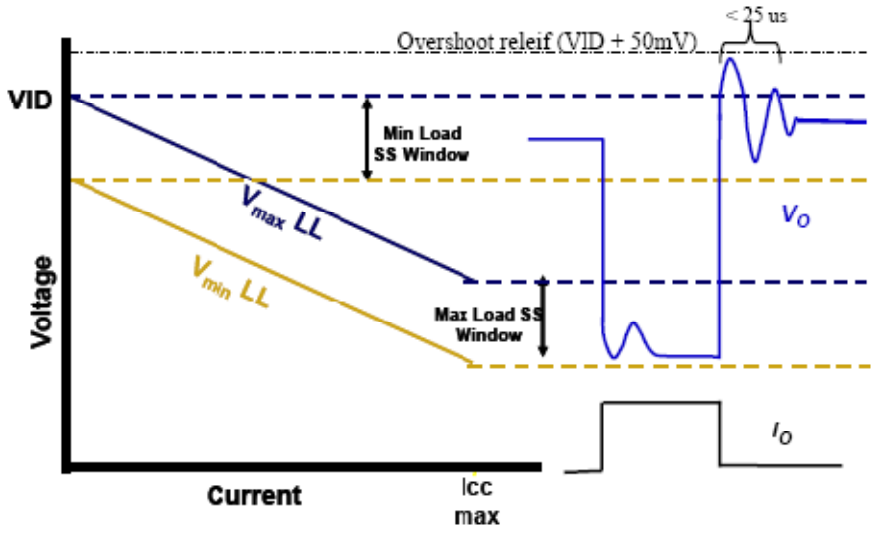



**Figure 1-8 The relationship between the load-line specifications and time domain waveforms**

The voltage overshoots, which cannot meet this specification, will cause higher processor operation temperature and this may result in damage or a reduced processor life span. The processor temperature rise from higher functional voltages may lead to operation at low power states, which directly reduces processor performance. The voltage undershoots may cause system lock-up, "blue screening," or data corruption. These concerns clarify why the CPU output filter capacitors are so important for a processor to operate properly. In order to supply sufficient energy to the processor, sufficient energy storage components, the output capacitors must be placed in different locations in the CPU power delivery path [4][15].

The capacitors closest to the VR are so-called "bulk" capacitors. In most of today's server system, three different bulk capacitors, OS-Con capacitor, SP capacitor and ceramic capacitor are used in different applications. OS-Con capacitors have relatively high profile,

thus it cannot be used in applications in which low profile is required, e.g. laptop computers. Another high-density capacitor called specify polymer capacitor (SPCAP) is now widely used as bulk capacitors in laptop or server computers due to its low profile. Following the bulk capacitors in the power path, multi-layer ceramic capacitor (MLCCs) are used as the decoupling capacitors. The MLCC has even lower ESR and ESL values than the OS-Con capacitors, but the capacitance is small. Because of the small package sizes, these MLCCs are usually located in the socket cavity. So sometimes it is referred as "cavity" capacitors with extremely low ESL. There is also one on-die capacitor to help the transient performance at high current slew-rate.

Figure 1-9 shows a lumped model of the power delivery path of today's microprocessor [15]. The selection of different types of capacitors is an attempt to achieve constant output impedance for the best transient performance.

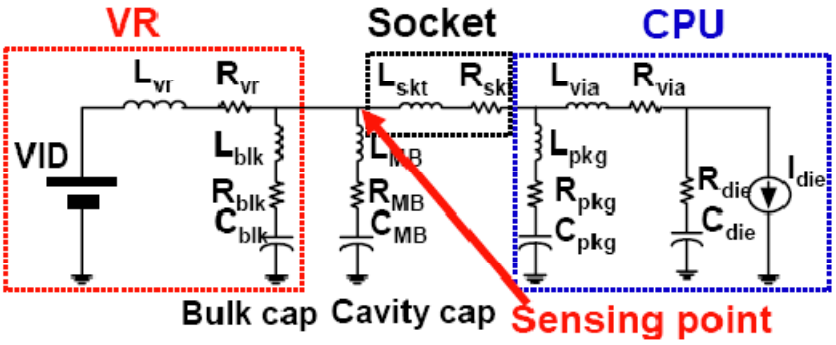
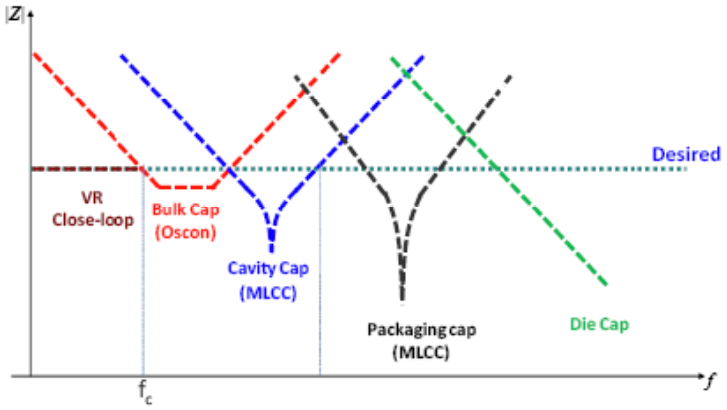


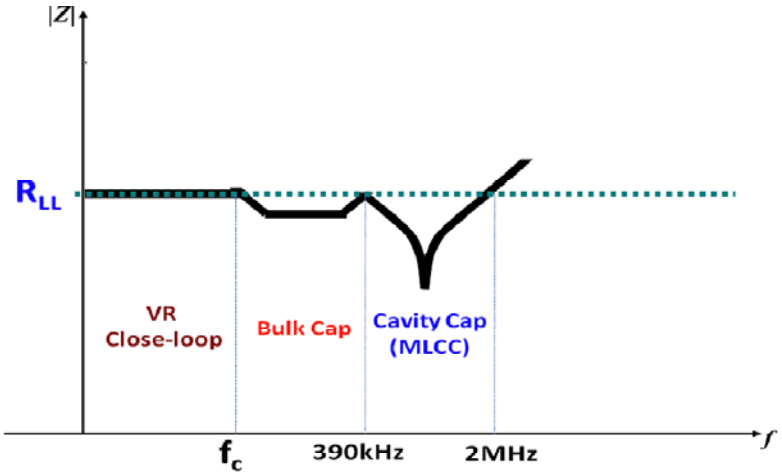

**Figure 1-9 A lumped model of the power delivery path of today's microprocessor**

Figure 1-10 explains this using the constant output impedance concept. Each type of capacitor has a different resonant frequency, so that they can cover a certain range of the frequency to make the overall output impedance lower than the desired impedance, as shown in Figure 1-10 (a). Actually, because the packaging capacitors and die capacitors

are determined by the CPU design and limited by the motherboard design, power engineers cannot do anytime for that, the overall output impedance from the sensing point which neglect the packaging capacitors and die capacitors is more important. As shown in Figure 1-10 (b), the impedance from the sensing point should also achieve constant or lower output impedance than the desired impedance for best dynamic performance.




**(a) Impedances for different decoupling capacitors**




**(b) Impedances requirement from the CPU socket (VR sensing point)**

**Figure 1-10 Constant output impedance for CPU transient requirement**

Since the number of the cavity capacitor is limited by the CPU socket, the maximum number is eighteen 22uF ceramic capacitors with 1206 footprint. As a result, it can only

cover the frequency range from around 390 kHz to 2MHz. Below 390 kHz, bulk capacitors must work with VR to get the desired impedance. For example, assume VR control bandwidth is 50 kHz, which means the impedance below 50 kHz can be taken care by VR close loop. Therefore, there is a gap between VR control bandwidth and the cavity capacitors for 50 kHz to 390 kHz. As a result, if using OS-Con capacitor, ten 560uF OS-Con must be added to fill the gap. If VR control bandwidth can be pushed to 390 kHz, there is no gap between VR impedance and cavity capacitance impedance, which indicate that there is no bulk capacitors required. With different VR control bandwidth, different number of the bulk capacitors should be used, as shown in Figure 1-11.

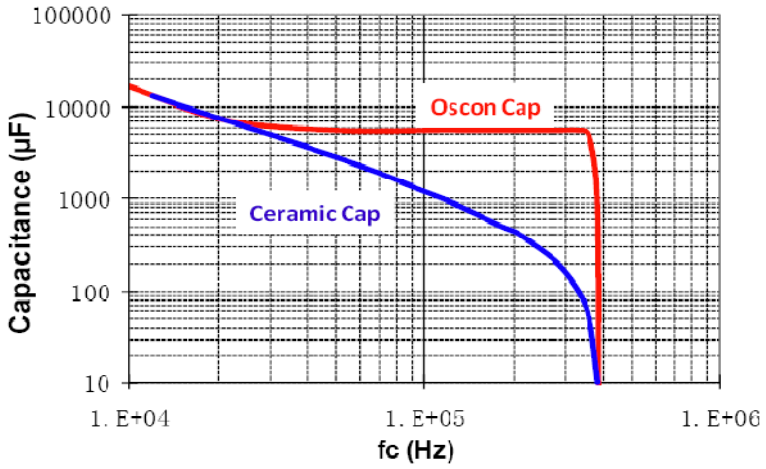



**Figure 1-11 Bulk capacitance vs. VR bandwidth**

From the diagram, a very interesting phenomenon is that within 50 kHz and 390 kHz control bandwidth, capacitance does not change for OS-Con capacitors but gradually changed for ceramic capacitors. The reason is that large ESR of OS-Con capacitors limit the number of the capacitors further reduction with control bandwidth. But for ceramic

capacitors, because the ESR is very small, the peak voltage spike will be just determined by the energy storage which can be controlled by bandwidth [16].

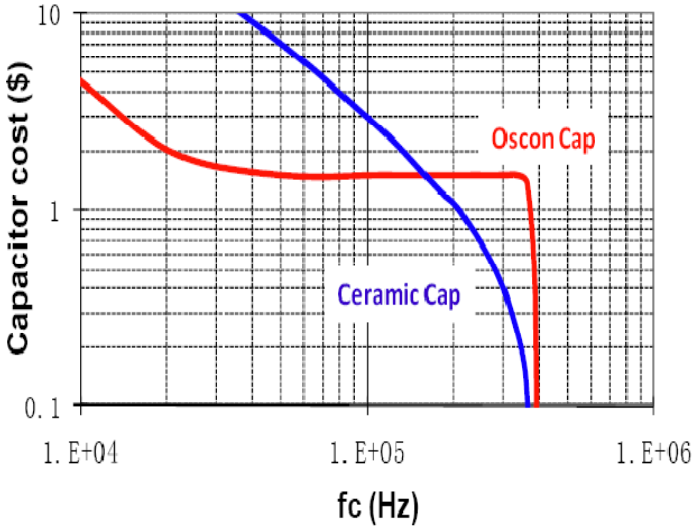



**Figure 1-12 Cost vs. VR bandwidth**

Form Figure 1-12, it can be observed that beyond 150 kHz Buck VR bandwidth, it is better to switch from the OS-Con capacitors to the ceramic capacitors to reduce the footprint while keeping the same cost.

### *1.2.3 High Power Density Requirement*

The power density is increasing by approximately 15% annually for data center system. More servers per rack mean more CPUs, which indicates that the CPU voltage regulators increase correspondingly. It can be calculated that the VR occupies more than 13% of the total motherboard space and there is an example from Intel S5500WB server motherboard shown in Figure 1-13.

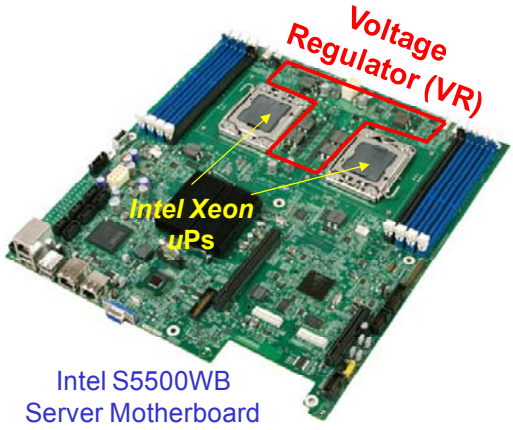



**Figure 1-13 One example with Intel's server motherboard**

To reduce the server size, it is necessary to reduce the VR size. If we perform further calculation, it can be seen that the passive components of the VR, which are the output inductors and output capacitors, are about 60% of the total VR size. So if we want to achieve a high-power-density VR, the passive component size must be reduced.

In the future, since CPU current will continue to increase, more VR phases should be designed to power higher current. With more VR phases, the size of the VR will be further increased. What is more, with lower and lower output voltage, the output voltage spike window is become smaller and smaller in the future which is shown in Figure 1-14 where $R_{LL}$ will be reduced to 0.8mohm. Assume that 100A load current of the microprocessor, than only 80mV voltage transient is permitted. In order to meet the smaller voltage window for future application, more output capacitors should be used for providing more energy buffering. In addition, because of the increasing current slew rate, the impedance requirement would be extended to more broad frequency range which also means that the

decoupling capacitors number is possible to be increased accordingly. The increasing requirement for the output capacitors will reduce the power density of VRs.

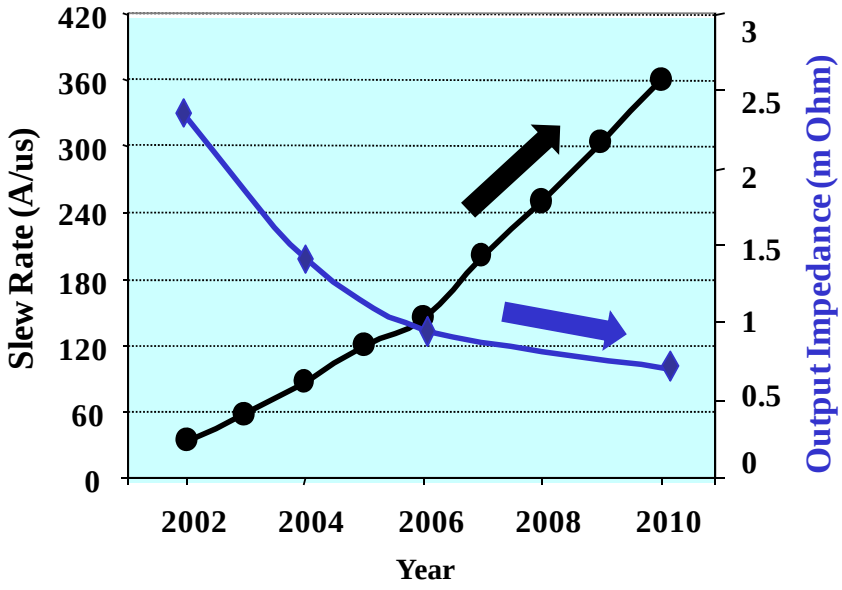



**Figure 1-14 Load Current Slew Rate and $R_{LL}$ for VR**

Figure 1-15 shows an example for using SP capacitor as the output bulk capacitors. Following current solution, assume that 1/6 of 600 kHz switching frequency is designed for the control bandwidth which is around 100 kHz, the number of output capacitors will be doubled for future application, from current 8 SP capacitors to future at least 16 SP capacitors. Both the cost and the footprint of the VR capacitors as well as the total VR will be doubled in the near future. It will result in low power density of the CPU voltage regulator. Besides the output bulk capacitors increasing, the number of the decoupling capacitors will also be increased according to the faster load transient slew rate, which is not shown in this diagram. Anyway, the solution for reducing the passive output capacitors for higher power density should be studied.

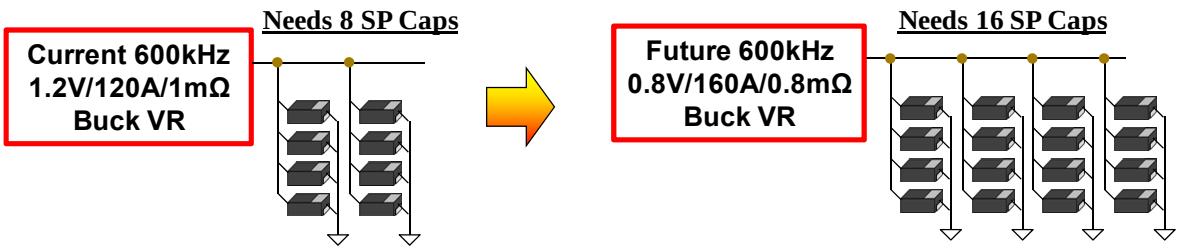



**Figure 1-15 Output Capacitors for Future VR**

## 1.3 Two-Stage VR Solution for High Efficiency and High Power Density

### *1.3.1 In-Series Two-Stage Solution*

In order to achieve both high efficiency and high power density, in-series two-stage concept was proposed [16-20] which is shown in

Figure **1-16**.

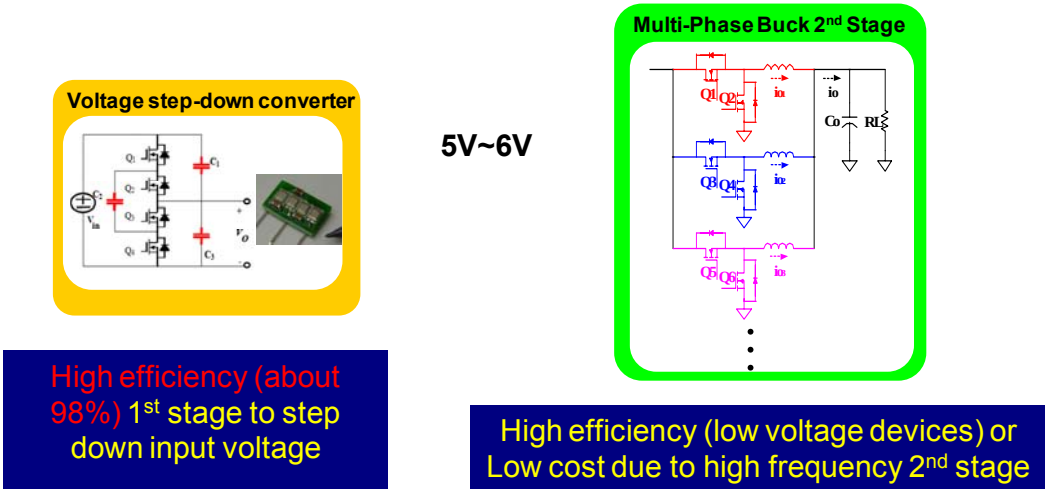



**Figure 1-16 In-Series Two-Stage Structure proposed by CPES**

The in-series two-stage structure plays the "divide and conquer" concept to achieve both high efficiency and high power density or low cost. The first stage can apply very

high efficiency voltage divider which can achieve 98% at full load. It does not require fast transient response for first stage, thus low switching frequency can be designed for high efficiency. The second stage can utilize the low voltage devices for high efficiency or operate at high frequency for low cost, depending on your target. An example of efficiency comparison between single-stage and two-stage specific design is shown in Figure 1-17. Two-stage solution can achieve around 87% with the second stage operating at 1 MHz, while single stage has similar efficiency with switching frequency at 600 kHz. Two-stage solution can achieve both efficiency and less output capacitors compared with the single stage solution.

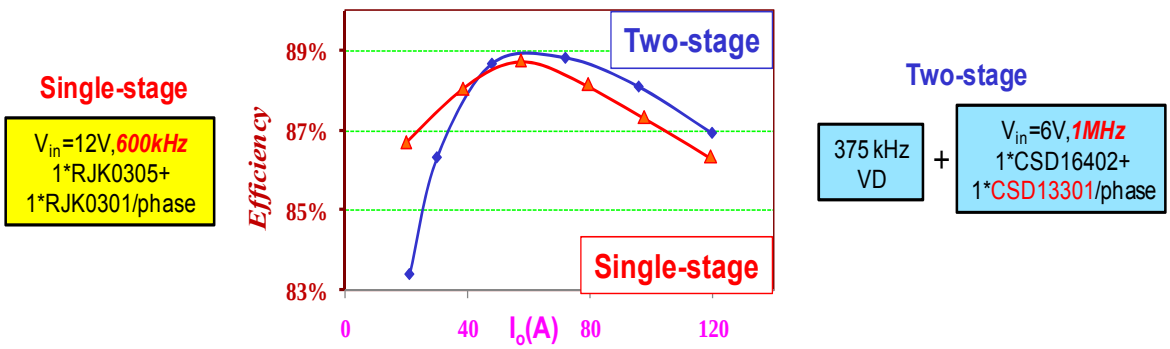



**Figure 1-17 Efficiency comparison between single-stage and two-stage**

Another in series two-stage structure proposed by Vicor [21-22] in Telecom application is shown in Figure 1-18. The basic concept is almost the same as CPES proposed two-stage structure. The only difference is that the second-stage is replaced by an unregulated DCX which is for achieving high efficiency. As commonly known, since the unregulated converter can operate fixed duty cycle modulation, it can be designed at optimal operation point to achieve very small switching loss and achieve higher efficiency

than conventional PWM regulated converter. In Vicor's two-stage, it utilizes the LLC as the topology for the unregulated DCX.

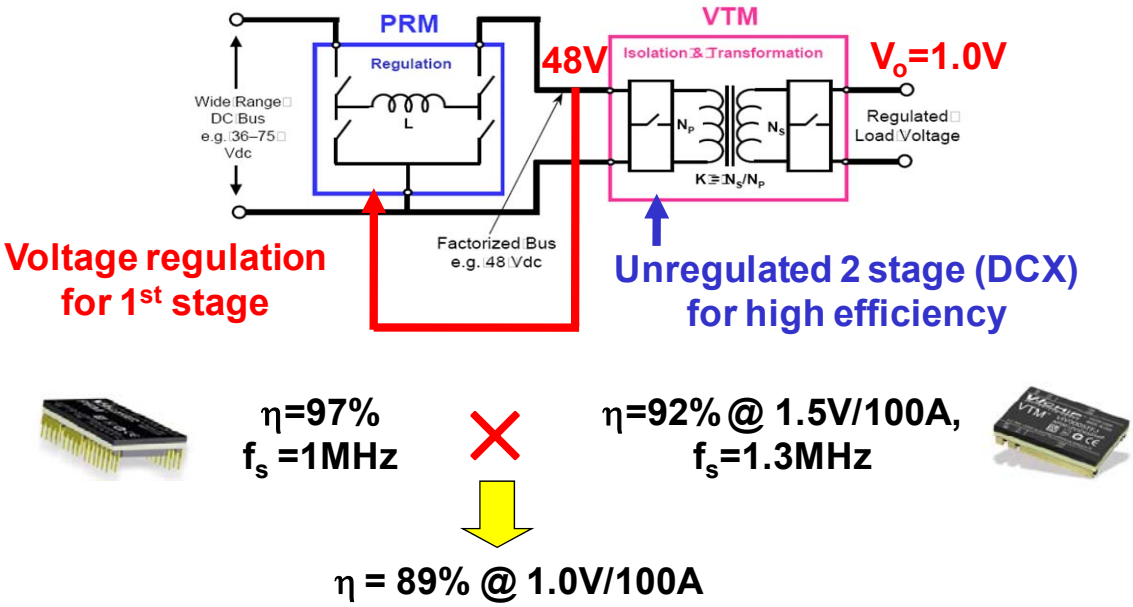



**Figure 1-18 Vicor's Two-Stage Structure**

The typical design of Vicor's product is also shown in Figure 1-18, where both first stage and second stage are using resonant solution. The overall efficiency can achieve around 89% using 1 MHz resonant first stage and 1.3 MHz unregulated second stage.

### *1.3.2 Parallel Two-Stage Solution: Sigma Voltage Regulators*

In-series two-stage structure, since both two stages have to handle the full load power it will decrease the efficiency performance. A more efficiency way to deliver power is that two stages deliver power to the load in parallel and use a high-efficiency unregulated converter to handle most of the power. A parallel-type two-stage approach is proposed, as shown in Figure 1-19 [23] [24]. The input-side of the two converters is in

series and the output sides are in parallel so that the energy can be distributed between them. The energy ratio of these two converters is determined by the input voltage ratio since input current of them is the same. The input voltage of DCX can be controlled by designing appropriate DCX voltage ratio [23].

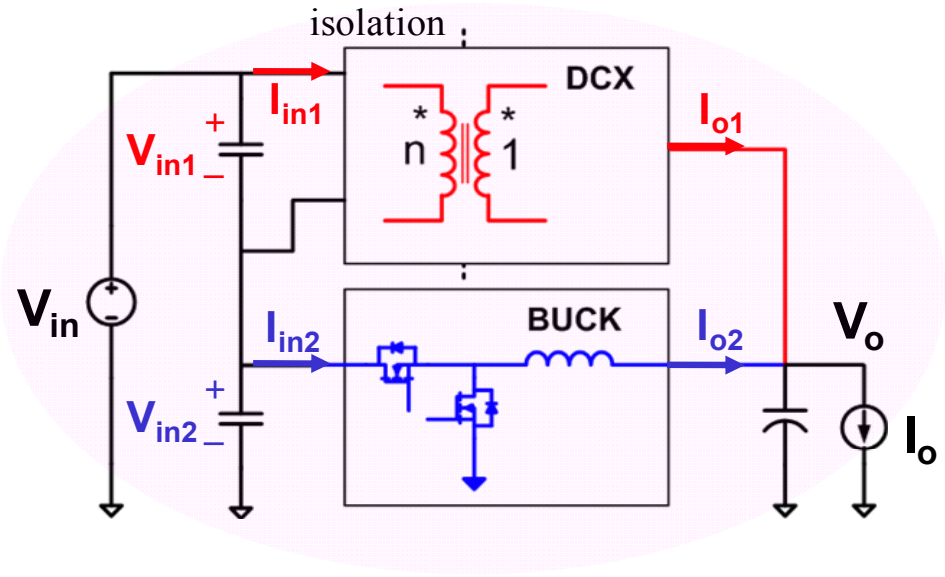



**Figure 1-19 Quasi-Parallel Structure - Sigma Structure**

## 1.4 1.2V/120A Sigma Voltage Regulator Design

Based on the simply concept of Sigma architecture, A 1.2V/120A Sigma VR was designed for efficiency demonstration [15].

The design steps are simply listed as follows:

- Determine the Power Ratio of DCX and Buck

  Considering the input voltage variation which might be change from 10.8V to 13.2V, the Buck input voltage was set to be around 4V for properly operating. The input voltage of DCX is around 8V, thus the transformer turn-

ratio choose to be 6 with consideration of some voltage drop across DCX at full load. Thus, the power ratio of DCX and Buck is set to be 8:4 or 2:1 where DCX will handle 80A current and Buck for 40A.

- Design 40A Buck

  Buck design is relatively easy. We can follow the industry practical design for Buck; two-phase is needed for 40A with each operate for 20A.

- Design the 80A DCX

  Resonant converters are preferred to reduce the switching loss. Two candidates are studied and discussed which is shown in Figure 1-20. For ZVS-QR, the leakage inductor ($L_k$) of the transformer resonates with the output capacitor ($C_o$) to achieve almost ZCS operation. The ZVS-QR has the same devices number as a phase Buck. As a result, it is reasonable to have 20A for this converter. In order to provide 80A, four ZVS-QR DCX converters are needed. Another candidate, the LLC can provide 40A using as the same device number as two-phase Buck and two phase of LLC could be used for 80A DCX solution. These two DCX candidates both can be designed for optimal efficiency operation.

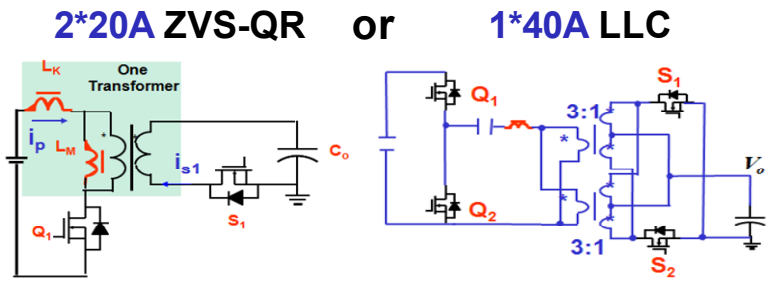



**Figure 1-20 DCX candidates**

Based on the design process, two version of 1.2V/120A Sigma VR is designed. Table 1-1 list the hardware component comparison for 120A Buck, Sigma solution 1 with ZVS-QR DCX and Sigma solution 2 with LLC DCX.

**Table 1-1 Component Comparison**

| | MOSFET | Magnetics | Magnetic Size | Drivers | Controller |
|---|---|---|---|---|---|
| **6-phase Buck** | 12 | 6 | "1" | 12 | Control 6 phase |
| **Sigma VR 1 (ZVS-QR)** | 12 | 7 | "1.2" | 12 | Control 2 phase |
| **Sigma VR 2 (LLC DCX)** | 16 | 6 | "1" | 12 | Control 2 phase |

The 60A Sigma cell is shown in Figure 1-21 with two third of the load power going through DCX and one third from Buck. In the real design, two 60A Sigma cell are paralleled for achieve 120A.

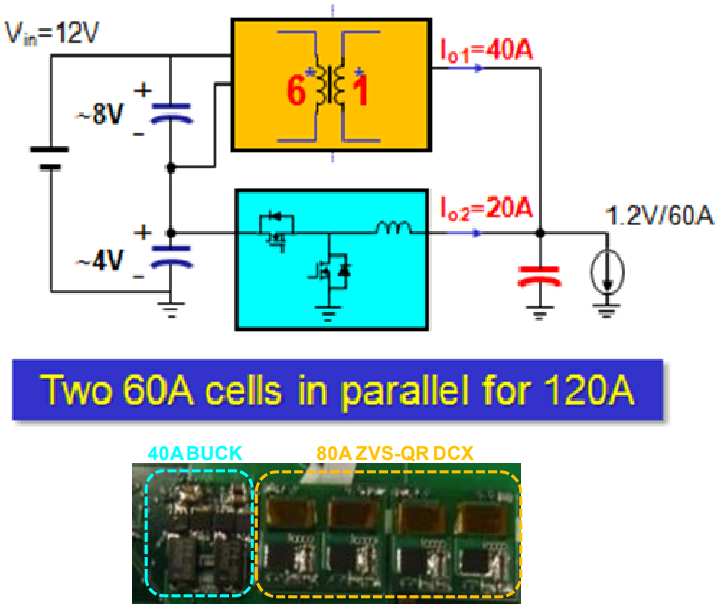



**Figure 1-21 1.2V/120A Sigma VR**

The measured overall efficiency of Sigma VR with the 120A Buck VR is shown in Figure 1-22. Two version Sigma VRs can both achieve around 90% efficiency which is around 3~4% efficiency improvement. It can meet the Intel, IBM and Google's efficiency requirement for VR.

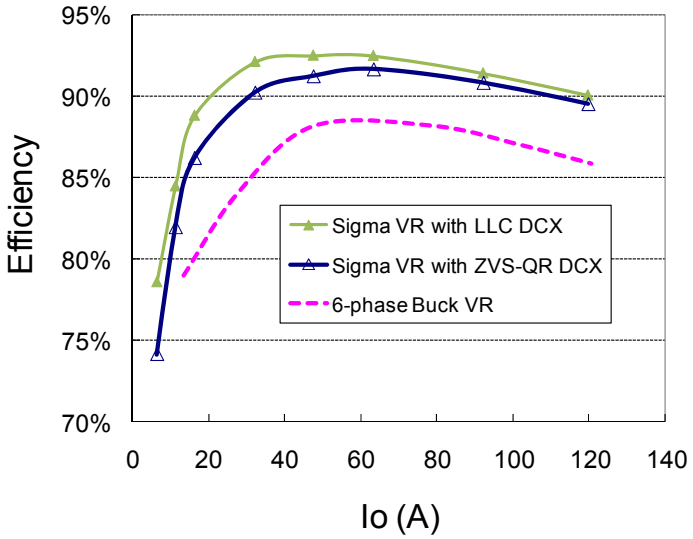
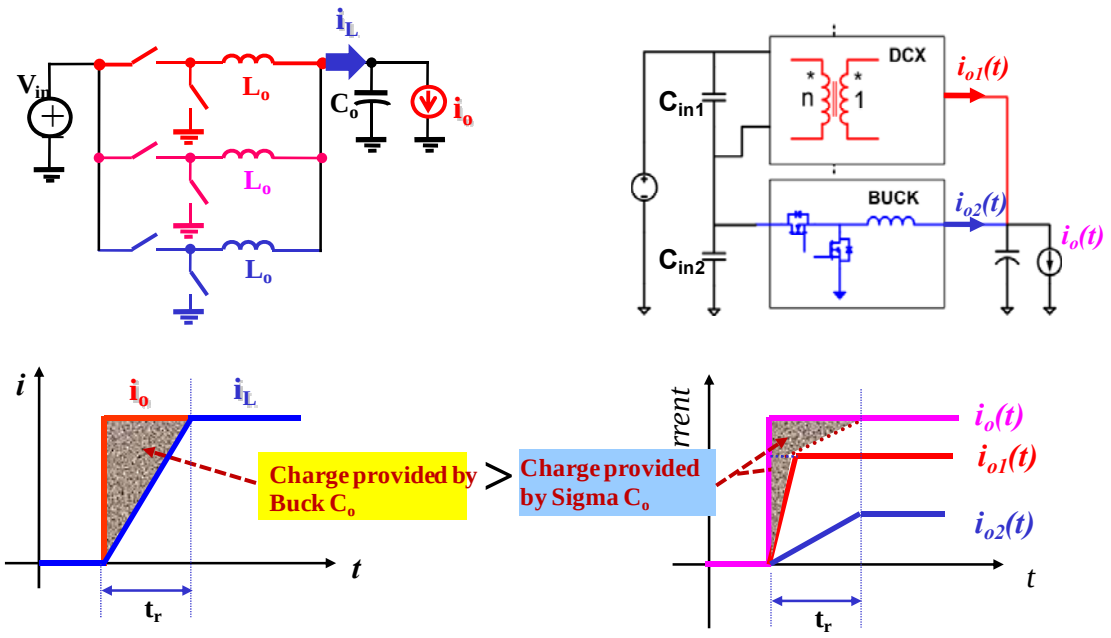



**Figure 1-22 Measured Sigma VR Efficiency**

Besides the efficiency benefit, the transient performance of Sigma VR is also needed to be studied. The faster transient concept of Sigma VR comes from the faster current response from DCX as shown in Figure 1-23. As the diagram shows, when there is a load step changes, for Buck VR, the inductor current slew rate is determined by the control Bandwidth [25][26]. The net charge is provided by the output capacitors which will cause the voltage drop during this transient period. The faster response of the inductor current, keeping the same voltage drop, the output capacitor number can be reduced. That is the reason from time domain why pushing control bandwidth the output capacitor can be reduced. However, in Sigma VR, the low impedance DCX current will have a faster

response than Buck inductor current with the help of input capacitor. So that from the power stage itself, the Sigma architecture will provide total faster current follow speed than Buck VR. And this potential benefit will make sigma VR more attractive from transient dynamic point of view.




**(a) Buck Inductor Current Response** **(b) Current Responses of Sigma VR**

**Figure 1-23 Current Response for Buck VR and Sigma VR**

With the same output capacitors of Buck and Sigma VR, the output voltage spike of Sigma VR will be reduced because the power stage with DCX can provide faster current response to the load current transient compared with Buck VR. On the other hand, if keeping the output voltage spike or voltage drop to be the same, the needed output capacitor number of Sigma VR can be reduced.

With this concept, Sigma VR should be able to achieve output capacitor saving compared with Buck VR. However, there are still several concerns need to be clarified. Is

it always true for Sigma VR that DCX always be faster? What impacts the current response speed of DCX? How DCX impedance will impact the current response speed? Detailed analysis on the transient performance of Sigma VR is necessary especially the transient response of DCX which is essential for output capacitor saving. These all are the related concerned questions for Sigma VR's transient response.

## 1.5 Thesis Objective

This thesis will do detail study of the transient performance and the impedance characteristics of Sigma VR to clarify the output capacitor saving issue. In addition, several improvement methods are discussed for further improving the efficiency and power density performance of Sigma VR.

In Chapter 2, the impedance characteristic and design for Sigma VR is discussed. The impedance reduction of Sigma architecture comes from the high voltage input capacitor's help and the low impedance DCX path. The impact of the input capacitor to the DCX current dynamic response is detailed analyzed. Base on the study of the small-signal-model of Sigma converter, too small or too large input capacitance will have different dynamic issue influence to DCX current response. In order to fully utilize the DCX in Sigma architecture, a suitable input capacitance is necessary. In addition, based on the study of the input capacitor's impact, the optimized input capacitance could be choose and the total capacitor cost and footprint can be compared to show the benefit of Sigma VR. In order to meet Intel's VR impedance specification, the output impedance design of Sigma VR is discussed. With the help of the low impedance DCX, the required output capacitor has the possibility to be reduced. The DCX impedance impacts a lot to the impedance

design. How the impact from the DCX impedance to the output capacitor choosing is also a topic in this chapter.

The efficiency and power density improvement of the Sigma VR is discussed in Chapter 3. As a critical component in DCX, the DCX transformer design not only impact to the efficiency performance but also to the power density issue. The optimization of the DCX transformer is discussed in this chapter, to further reduce the winding loss for improving the efficiency and to future reduce the leakage inductance for improve the DCX dynamic response for higher power density. With current device level, the energy ratio is not optimized one, re-distribution of the energy of DCX and Buck in Sigma VR will also provide us the opportunity to optimize the efficiency performance. Another way to improve the efficiency is possible, which is to reduce the DCX switching frequency. What is more, Sigma VR will be more attractive for future application, because the DCX could handle more power for lower output voltage case.

Chapter 4 is the summary and future opportunity of this new structure is given. Actually, the potential of Sigma architecture has not been fully explored, especially for higher voltage application.

# Chapter 2. Faster Transient Performance and Impedance Reduction of Sigma VR

## 2.1 Introduction

Despite of desired high efficiency performance, to meet the challenging transient requirement is also a critical issue for current and future CPU voltage regulators. Countless research [27-30] and industrial efforts had been made to analyze and improve the VR transient performance.

In this chapter, first, we will review the basic concept of faster DCX current response of Sigma VR and explain why Sigma structure can achieve fast dynamic response to the load transient. From the study of the small-signal-model of Sigma VR, the impact factors for the DCX current response will be studied. Evaluation of these impact parameters is also discussed, including the input capacitors, DCX impedance and control bandwidth of Sigma VR. In addition, following the industry's practice to evaluate the transient performance, from the impedance perspective, reduction of impedance of Sigma VR can be achieved by the high voltage input capacitor and the low impedance DCX. The benefit of the concept of impedance reduction means that if using the same output capacitors, Sigma structure can achieve lower control bandwidth than Buck VR or if the control bandwidth is set to be the same, Sigma VR could achieve output capacitors saving.

Base on the analysis of the faster transient performance and impedance characteristic of sigma VR, a 120A sigma VR is designed for experimental verification. With the less

output capacitor number compared with Buck VR, the designed Sigma VR can achieve both higher efficiency and less output capacitors.

## 2.2 Faster DCX Current Response Sigma VR

The concept of fast transient response of Sigma VR is redrawn and shown in Figure 2-1. Take the load current $i_o(t)$ step up for example, when load current changes from low current to high current, the DCX output current $i_{o1}(s)$ and Buck inductor current $i_{o2}(t)$ will response according to the Sigma power stage natural characteristic. In normal condition, the inductance or impedance of the DCX is much smaller than that of Buck output inductor which means the power path of DCX seems more "clear" than Buck path in Sigma architecture. Therefore, a simply concept that DCX current response will be much faster than Buck inductor current response is proposed [15]. With the faster current response of DCX, the total net charge provide by the output capacitor of Sigma VR is smaller than conventional Buck VR which is the shaded area in Figure 2-1. Sigma power stage inherently response faster, so that utilizing this topology, the requirement from the output capacitors for transient dynamic response can be alleviated.

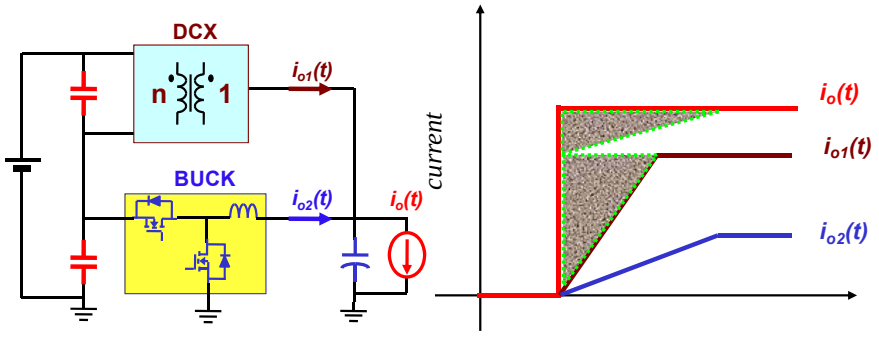



**Figure 2-1 Faster DCX current response of Sigma VR**

However, there is no detail analysis of the faster transient phenomenon. Is it always true that DCX current always respond faster than Buck? What are the impact factors of DCX current response speed? How this factors impact the DCX current? These are all necessary concern needed to be clarified for us to well understand the transient performance of Sigma architecture. In order to understand the DCX current response of Sigma VR, the small-signal-model is established.

### *2.2.1 Small-Signal-Model of Sigma VR*

In order to better understand the Sigma converter dynamic characteristics, especially the DCX current response and to achieve good control design, the small-signal model of Sigma converter and the related transfer functions are necessarily to be studied.

Before the detailed analysis of the small-signal dynamic study, there are some basic concerns about the control issue of sigma converter. As we know, for conventional Buck converter, it is not so hard to understand how the duty cycle regulated the output voltage or the inductor current. However, for Sigma converter, the DCX is unregulated converter, how to achieve the controlling of DCX? Actually, in Sigma converter, it is also easy to understand the Buck duty cycle can control the Buck inductor current. However, not only can it do that, but also it can control the DCX current through the input capacitor coupling. When the duty cycle increases, the average input current of Buck will also increase, the net charge will be withdraw from the input capacitor which will result in the re-distribution of input voltage. The input voltage of DCX will be decreased as well as the DCX current. Thus, we can regard that the Buck duty cycle can also achieve control of DCX current.

#### 2.2.1.1 Average Model of DCX

Before we establish the model of the Sigma converter, it is necessary for us to build the DCX average model first. As we know, the unregulated DCX can be regarded as a DC to DC transformer at steady state. Because there is not duty cycle modulation, small-signal perturbation of duty cycle is eliminated, and the average model of the unregulated DCX is obtained. The inductor-less ZVS-QR [31] is used for our DCX, and the average model [32] is shown in Figure 2-2.

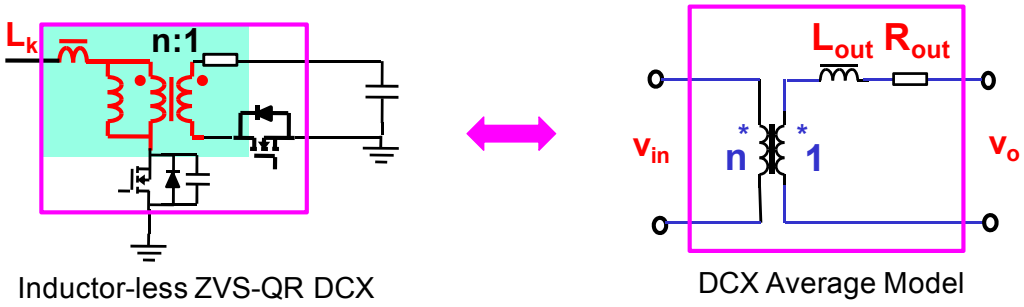



**Figure 2-2 Average model of DCX**

In Figure 2-2, $R_{out}$ is the equivalent output resistance representing the power loss from DCX. $L_{out}$ is the equivalent output inductance representing dynamic behavior of DCX. Some papers [32] and industry documents [22] has detailed analysis on the study of the model of resonant converters. In our case, the respective value of $R_{out}$ and $L_{out}$ of the designed ZVS-QR DCX can be represented as following equations:

$$L_{out} = \frac{\pi^2}{4n^2} \cdot L_k$$

$$R_{out} = \frac{\pi^2}{8} \cdot [R_w + R_{dson\_SR})]$$

Where $L_k$ is the primary side leakage inductance of the DCX transformer, $R_w$ represents the winding resistance and $R_{dson\_SR}$ is the conduction resistance of the output SR. From the equations, the leakage inductance and the winding loss of the DCX transformer is critical to determine the equivalent output impedance of DCX.

#### *2.2.1.2 Small-Signal-Model of Sigma VR*

The small signal model of Sigma VR is established by replacing the DCX average model and Buck three-terminal model into the corresponding position as shown in Figure 2-3. In the diagram, $L_{out}$ and $R_{out}$ are the DCX impedance just mentioned before; $L_o$ is the Buck inductance; DCR is the total resistance of Buck trace resistance, the switch $R_{ds\_on}$ and ESR of Buck inductor; $C_o$ is the output capacitor while $C_{in1}$ and $C_{in2}$ are the input capacitors for DCX and Buck; $R_o$ is the load resistor.

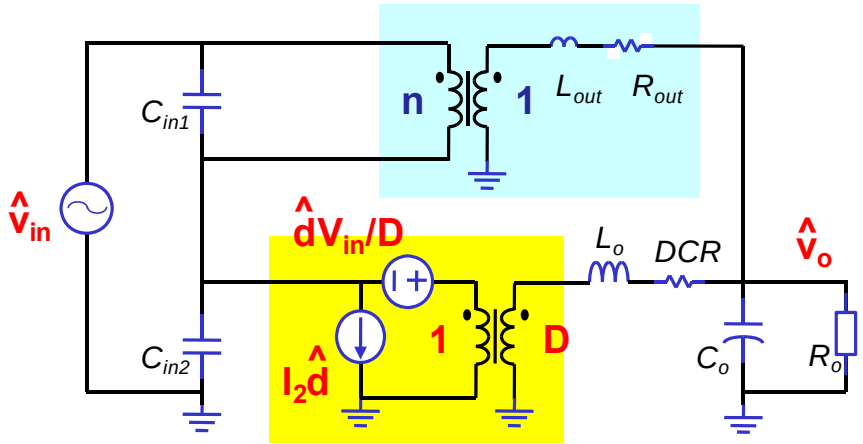



**Figure 2-3 Small-signal-model of Sigma VR**

Form the small-signal-model, the sigma structure is a fourth-order system. There are four system poles existing in Sigma converter. Actually, if the impedance of DCX is ignored, the system could be reduced to a second-order system. However, because we want

to understand the impact from DCX impedance, the four poles, which is actually two pairs of double-pole are both analyzed first.

#### *2.2.1.3 System poles of Sigma VR*

The system poles of sigma structure are just determined by the passive components and the topology structure. By assuming that the DCX $L_{out}$ is much smaller than Buck $L_o$ four poles can be simplified two pair of double-pole. One of the double-pole locates at low frequency range, while the other locates at high frequency.

At low frequency range, because $L_{out}$ is much smaller than Buck inductance, it can be ignored and shorted. Then by reflecting the Buck inductor to the output capacitor side, the low frequency double-pole can be easily derived as following equations:

$$\omega_{Lp} = \frac{1}{\sqrt{(n^2 C_{in} + C_o)\frac{L_o}{(1+nD)^2}}}$$

$$Q_{Lp} = \frac{1}{\omega_{Lp}} \cdot \frac{1}{\frac{L_o}{R_o(1+nD)^2} + (n^2 C_{in} + C_o)(DCR + ESR // R_{out})}$$

The low frequency double-pole can be regarded as the equivalent capacitor which is the output capacitor paralleling with the reflected input capacitor resonating with the equivalent inductor which is $L_o/(1+nD)^2$. The equivalent inductance and capacitance are given as following equations:

$$C_{e\_L} = (n^2 C_{in} + C_o)$$

$$L_{e\_L} = \frac{L_o}{(1+nD)^2}$$

The high frequency approximation can be also made through the same way. At high frequency range, the Buck inductance $L_o$ is much larger than DCX equivalent inductance, so it can be regarded as open circuit. Then the equivalent circuit at high frequency can be easily obtained as well as the high frequency double pole position. The equivalent high frequency capacitance and inductance can be obtained:

$$C_{e\_H} = \frac{n^2 C_{in} \cdot C_o}{n^2 C_{in} + C_o}$$

$$L_{e\_H} = L_{out}$$

The high frequency double pole depends on the DCX $L_{out}$. The position of this high frequency double-pole is important for analysis the current response velocity which will be discussed later. Thus, the resonant frequency and quality factor at high frequency can be determined by following equations:

$$\omega_{Hp} = \frac{1}{\sqrt{\frac{n^2 C_{in} C_o}{n^2 C_{in} + C_o} \cdot L_{out}}}$$

$$Q_{Hp} = \frac{1}{\omega_{Hp}} \cdot \frac{1}{\frac{L_{out}}{R_o} + (\frac{n^2 C_{in} C_o}{n^2 C_{in} + C_o})(R_{out} + ESR)}$$

### *2.2.1.4 $G_{vd}(s)$ of Sigma VR*

Base on the small-signal-model and the system poles analysis above, all the interested transfer functions is derived and simplified which is attached in the Appendix. Here, the transfer function from the duty-cycle to output voltage is given for an example, because it is essential to design the control compensation.

Through derivation and some simplification, the duty-cycle to the output voltage transfer function is:

$$G_{vd}(s)=\frac{\hat{v}_o}{d}=\frac{V_{in}}{(1+n\cdot D)^2}\cdot\frac{(1+\frac{s}{Q_{vd}\cdot\omega_{vd}}+\frac{s^2}{\omega_{vd}^{\ 2}})(1+\frac{s}{\omega_{ESR}})}{(1+\frac{s}{Q_{Lp}\cdot\omega_{Lp}}+\frac{s^2}{\omega_{Lp}^{\ 2}})(1+\frac{s}{Q_{Hp}\cdot\omega_{Hp}}+\frac{s^2}{\omega_{Hp}^{\ 2}})}$$

From the transfer function, we can see that the zero distribution of sigma converter is also different from Buck converter. It has three zero in the power stage including the ESR zero. The other one is a double-zero which is given in:

$$\omega_{z1}=\frac{1}{\sqrt{(n^2C_{in})\cdot(L_{out}/1+nD)}}$$

$$Q_{z1}=\frac{1}{\omega_{z1}}\cdot\frac{(1+nD)^2R_o}{nD(L_o-nDL_{out})}$$

The double-zero is related to the input capacitor and the DCX inductance. It is very interesting that if we choose the input capacitance to be $(D/n)\cdot C_o$, the double-zero will be almost cancelled with the high frequency double pole. An example is shown in Figure 2-4, where we set the input capacitance to be around $(D/n)\cdot C_o$. With the appropriate input capacitance, the compensator design of Sigma converter could be following the Buck converter design guideline. Actually, in the following analysis of choosing input capacitance, the optimal input capacitance happen to be the one where the double-zero will be cancelled with the high frequency double-pole.

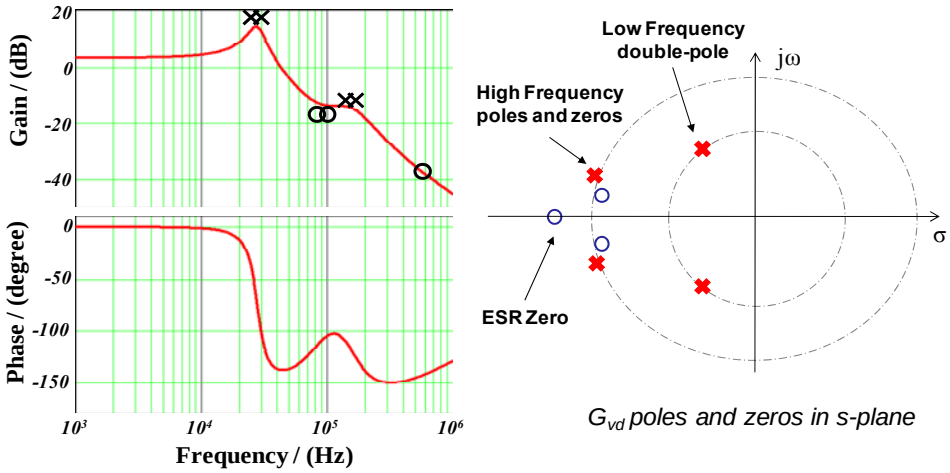



**Figure 2-4 $G_{vd}(s)$ of Sigma VR**

### *2.2.2 Transfer Function - $G_{ii1(s)}$ of Sigma VR*

As we analyzed above, the thing we most care about for Sigma VR is the DCX current response when load transient happens. Thus, the transfer function from DCX current to load current, named $G_{ii1}(s)$ is the most interesting one for us to analyze the response speed of Sigma VR. Following equations also shows the transfer function from Buck inductor current to load current for easily compared with the DCX current response.

$$G_{ii1}(s) = \frac{nD}{1+nD} \cdot \frac{(1+\frac{s}{\omega_{ii1}Q_{ii1}}+\frac{s^2}{\omega_{ii1}^2}) \cdot (1+\frac{s}{\omega_{ESR}})}{\Delta_{Lp} \cdot \Delta_{Hp}}$$

$$G_{ii2}(s) = \frac{1}{1+nD} \cdot \frac{(1+\frac{s}{\omega_{ii2}Q_{ii2}}+\frac{s^2}{\omega_{ii2}^2}) \cdot (1+\frac{s}{\omega_{ESR}})}{\Delta_{Lp} \cdot \Delta_{Hp}}$$

$$\omega_{ESR} = \frac{1}{ESR \cdot C_o} \quad \omega_{ii1} = \frac{1}{\sqrt{nC_{in}\frac{L_o}{D(1+nD)}}} \quad Q_{ii1} = \frac{1}{\omega_{ii1}} \cdot \frac{D(1+nD)}{nC_{in}DCR}$$

$$\omega_{ii2} = \frac{1}{\sqrt{n^2C_{in}\frac{L_{out}}{(1+nD)}}} \quad Q_{ii2} = \frac{1}{\omega_{ii2}} \cdot \frac{(1+nD)}{n^2C_{in}R_{out}}$$

Where $\omega_{ESR}$ is the ESR-zero of the output capacitor, $\omega_{ii1}$ and $\omega_{ii2}$ are the double-zeros in the transfer functions, and $Q_{ii1}$ and $Q_{ii2}$ represent the damping effect that exists in the system.

Take a close look of these two transfer functions, the DC gain of them represents the current ratio between DCX and Buck at steady state. As what we mentioned before, choose appropriate input capacitance, the double-zero of $G_{vd}(s)$ will be cancelled with the high frequency double-pole and $G_{vd}(s)$ is similar to Buck converter. By observing the transfer function of $G_{ii1}(s)$ and $G_{ii2}(s)$, if the capacitance of $C_{in}$ is also set to be $D/n \cdot C_o$, the double-zero of $G_{ii1}(s)$ will also be cancelled by system high frequency double-pole and double-zero of $G_{ii2}(s)$ will be cancelled by system low frequency double poles. This is a very interesting phenomenon of Sigma converter. Thus, the $G_{ii1}(s)$ and $G_{ii2}(s)$ will be simplified as second-order transfer functions. $G_{ii1}(s)$ has the resonant frequency at high frequency double-pole position while $G_{ii2}(s)$ has the resonant frequency at low frequency double-pole position.

Figure 2-5 shows an example of the bode plot of these two transfer functions when choosing appropriate $C_{in}$ value. The system will behavior like a second-order system, $G_{ii1}(s)$ has high frequency double-pole which means it will response much faster than $G_{ii2}(s)$ whose main double-pole is located at low frequency. The circuit parameters are shown as follows:

$V_{in}$=12V, $V_o$=1.2V, n=6, $C_{in}$=88uF, $C_o$=1760uF, $L_{out}$=3nH, $R_{out}$=1.8mΩ, $L_o$=120nH, DCR=2.7mΩ, D=0.3.

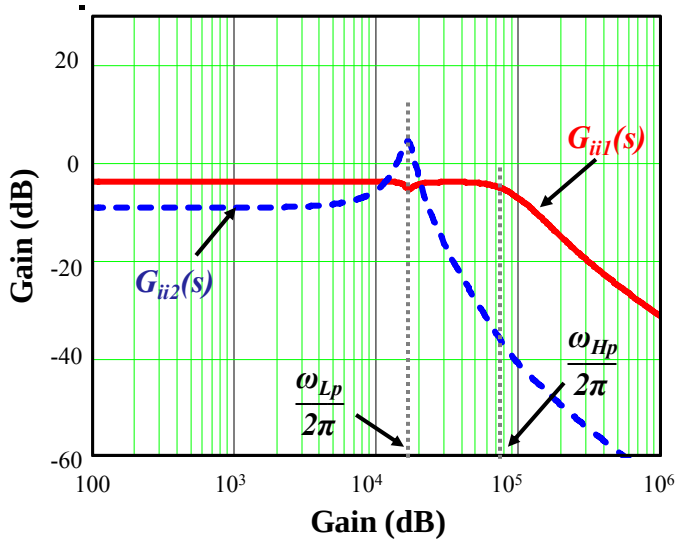
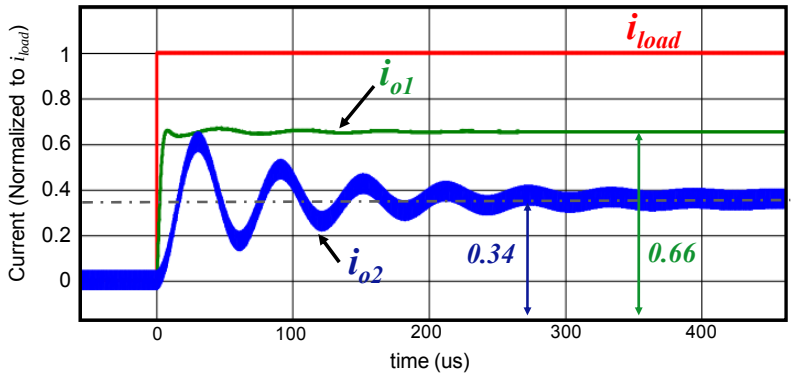
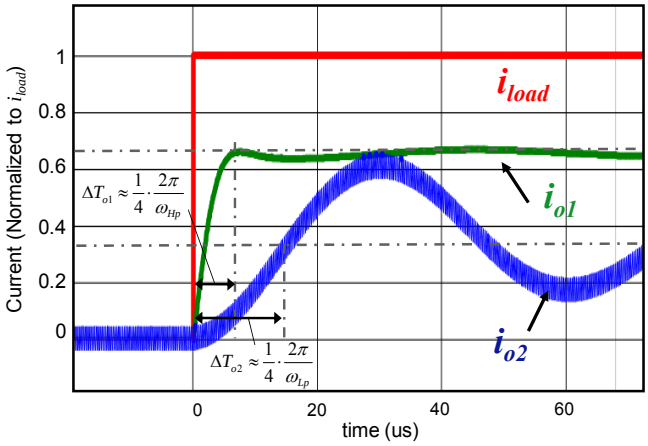



**Figure 2-5 Current transfer functions of $G_{ii1}(s)$ and $G_{ii2}(s)$ of Sigma VR**

From Figure 2-5, the DCX current will response much faster than Buck inductor current when load current step change happens because the resonant frequency of $G_{ii1}(s)$ is higher than $G_{ii2}(s)$. Figure 2-6 shows DCX and Buck current response in open loop of Sigma VR and its zoom-in diagram. When the load current transient happens, the DCX current will response as the high frequency while Buck at low frequency. The steady-state value of the DCX current and Buck current is determined by the power ratio which is discussed at Chapter 1.




**(a) DCX and Buck inductor current response**




**(b) Zoom-in of the current response and rising time**

**Figure 2-6 Current Response of Sigma VR**

Form Figure 2-6(b), the rising time of DCX current is related to the high frequency double-pole, which is determined by $L_{out}$ of DCX and equivalent output capacitance. The rising time of Buck inductor current is related to the low frequency double-pole. The rising time of DCX current and Buck inductor current response are as follows:

$$\Delta T_{o1} \approx \frac{1}{4} \cdot \frac{2\pi}{\omega_{Hp}} = \frac{\pi}{2} \cdot \sqrt{(n^2 C_{in} // C_o) \cdot L_{out}}$$

$$\Delta T_{o2} \approx \frac{1}{4} \cdot \frac{2\pi}{\omega_{Hp}} = \frac{\pi}{2} \cdot \sqrt{(n^2 C_{in} + C_o) \frac{L_o}{(1+nD)^2}}$$

From the above equations, we can see that the rising time of DCX will be much shorter than that of Buck inductor current when $L_{out}$ is much smaller than $L_o$. The above analysis are based on choosing appropriate input capacitance and the open-loop condition, how does the input capacitance and close control loop impact the current slew rate of DCX?

## 2.3 Impact Factors to DCX Current Response

Base on the transfer function of $G_{ii1}(s)$, we can see that the input capacitor $C_{in}$, the DCX impedance $L_{out}$ will both impact the current response of DCX as well as the output capacitor configuration. Another possible impact factor – the control design may also have some effect on it. In this section, the mentioned three impact factors of DCX current response are analyzed and discussed.

### *2.3.1 Input Capacitance Impact and Choosing*

Based on the previous study, we can see that the faster DCX response will give us the benefit of reducing output capacitors. And from the study on the transfer function of $G_{ii1}(s)$ which can be used for analyzing DCX current dynamic response, the DCX current response is related to the choosing of input capacitance. Figure 2-7 shows the open loop simulation current response including DCX current and Buck inductor current with different input capacitance. The load current changes from 0A to 100A. The simulation circuit parameters are shown as following:

$V_{in}$=12V, $V_o$=1.2V, n=6, $C_{in}$=88uF, $C_o$=1760uF, $L_{out}$=3nH, $R_{out}$=1.8mΩ, $L_o$=120nH, DCR=2.7mΩ, D=0.3.

The red curve is the output load current step change, while the blue curve is the DCX output current response and the brown curve is the Buck inductor current response. The green curve is the sum of the DCX and Buck inductor current. From the diagram, we can see that when the input capacitance is very small, the current response of DCX is not faster than Buck current. Increasing the input capacitance a little bit, we can see a faster response

at the beginning of the step change happens from DCX. The reason of the phenomena is that the small input capacitance cannot achieve enough fast current response since the energy stored in the input capacitor is not enough.

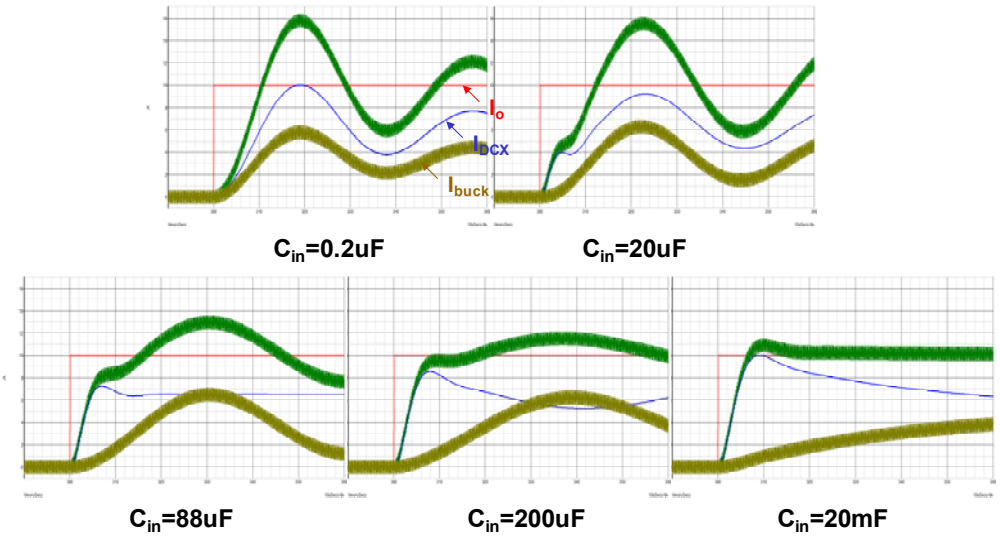



**Figure 2-7 Sigma current response with different $C_{in}$**

When the input capacitance is further increased, it means that the input capacitor can store enough energy at steady state. Thus, when there is the fast current step change at the output side, the energy stored in the input capacitor can provide enough fast transient current response to the output side through low impedance DCX path. That is the benefit and basic concept for the sigma VR's fast transient response. But there is some problem when input capacitance is too large, although the DCX can supply fast current response. The DCX current is uncontrollable by the duty cycle because of the decoupling of the large input capacitor. DCX is uncontrollable, so that it will provide all the dynamic current when the transient happens which will lead to the dynamic current sharing problem between DCX and Buck during transient happens. In summary, if the input capacitance is too small,

the DCX current cannot response faster than Buck, if the input capacitance is too large, the DCX is uncontrollable and dynamic current sharing between DCX and Buck may happen.

To choose appropriate input capacitance, we have to first determine what kind of DCX current response we want. From Figure 2-7, when $C_{in}$=88uF, the DCX current response from 0A to the value which it will operate at steady state. It means the input capacitance has the appropriate energy for DCX to provide the current it should provide, no too small or no too large. The appropriate input capacitance can be derived from the transfer function study of $G_{ii1}(s)$.

From the transfer function of $G_{ii1}(s)$ given before, when the double-zero position equals the low frequency double-pole position, the input capacitance $C_{in}$ will be $(D/n)\cdot C_o$. With the different $C_{in}$ value, the $G_{ii1}(s)$ and its time domain response is given in Figure 2-8. When the input capacitance is lower than $(D/n)\cdot C_o$, there will be a lower step located at high frequency range, which will resulting slower dynamic current response in time domain since the energy in input capacitor is too small. When the input capacitance is higher than $(D/n)\cdot C_o$, there will be a upper step located at high frequency range, which will resulting in larger dynamic current in DCX, since the energy in input capacitor is too large. Only when the input capacitance is around $(D/n)\cdot C_o$, the gain of $G_{ii1}(s)$ will be flat up to the high frequency double-pole position, which will resulting in the appropriate time domain DCX dynamic response which is the optimal choosing of the input capacitance. At the value, the energy store in the input capacitor will not be too large or too small, it just provide the needed energy for Sigma DCX dynamic response. At this condition, we can obtain the appropriate $C_{in}$ capacitance which is $(D/n)\cdot C_o$. Another observation is that, when

input capacitance is chosen to be$(D/n)\cdot C_o$, the transfer function of $G_{vd}(s)$ will be approximately simplified into second-order form, which can follow the compensator design of Buck VR.

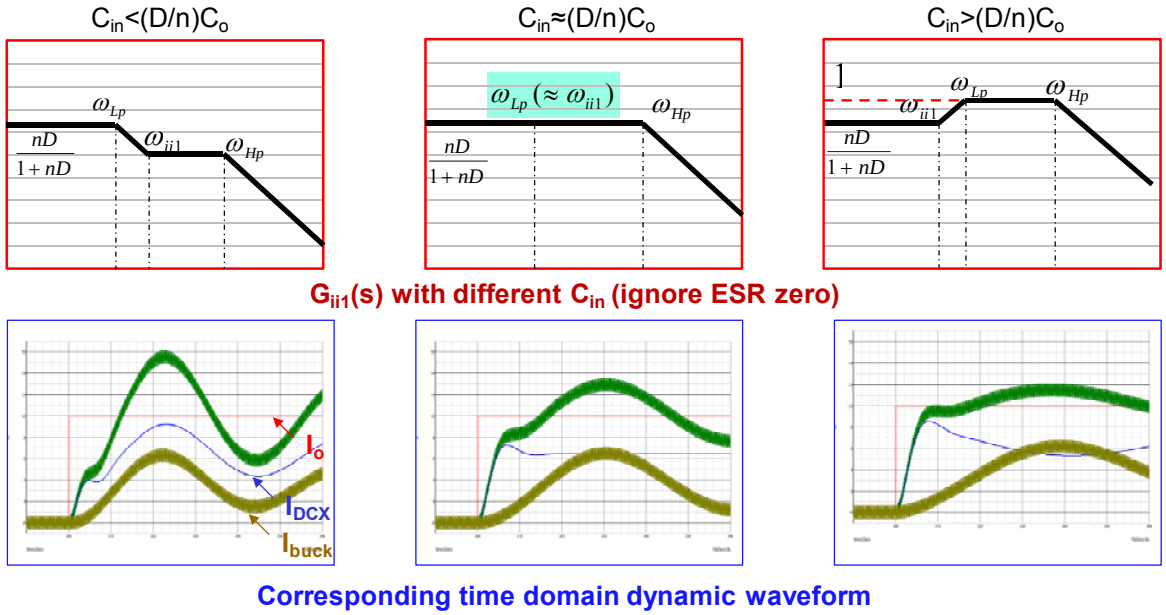



**Figure 2-8 $G_{ii1}(s)$ and time-domain response with different $C_{in}$**

## *2.3.2 DCX Impedance $L_{out}$ Impact*

When the input capacitance is chosen, the transfer function of $G_{ii1}(s)$ can be simplified as the second-order form as shown in the following equation.

$$G_{ii1}(s)=\frac{\hat{i}_{ol}}{\hat{i}_o}\approx\frac{nD}{1+nD}\cdot\frac{(1+\frac{s}{\omega_{ESR}})}{(1+\frac{s}{Q_{pH}\cdot\omega_{pH}}+\frac{s^2}{\omega_{pH}^{\ 2}})}$$

Consequently, the average DCX current will response following the high frequency double-pole which is related to the DCX impedance $L_{out}$. When the $L_{out}$ is large, the high

frequency double-pole position will locate at lower frequency range, while smaller $L_{out}$ value, the double-pole will be pushed to higher frequency.

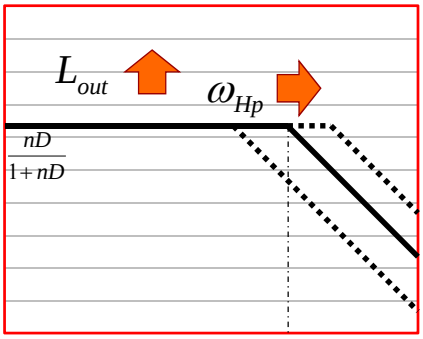



**Figure 2-9 $G_{ii1}(s)$ with different $L_{out}$**

An example of different $L_{out}$ response of DCX current is shown in Figure 2-10. The smaller $L_{out}$, the faster DCX current response can be achieved.

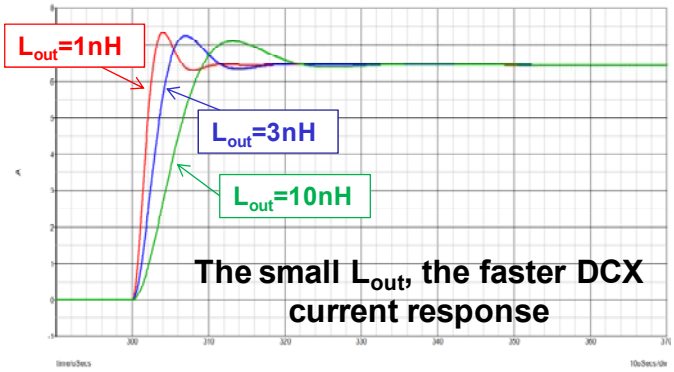



**Figure 2-10 DCX current response with different $L_{out}$**

Actually, in Sigma architecture, the fast dynamic response can be interpreted like special dam preparing for sudden need of water. The input capacitance represents the dam total capacitance, only when the dam stores enough water, the water can be provided fast enough for the people needed. The DCX impedance path is just like the channel which connects the dam and the water faucet of every house. Only when the channel is clear, no

any things block inside, the water could be supplied as fast as possible. The impact of $L_{out}$ for the output capacitor will be also discussed in the next chapter.

### *2.3.3 Control Bandwidth Impact to DCX Current Response*

In Buck VR, the average inductor current slew rate could be controlled by the control bandwidth until the inductance itself limits [25]. The same methodology in [25] is also used to investigate the DCX and Buck inductor current response of Sigma VR. The impact from input capacitor and DCX impedance is discussed, this section will clarify the impact from the control bandwidth.

To make the analysis simple, only the voltage loop is applied for Sigma converter which is shown in Figure 2-11.

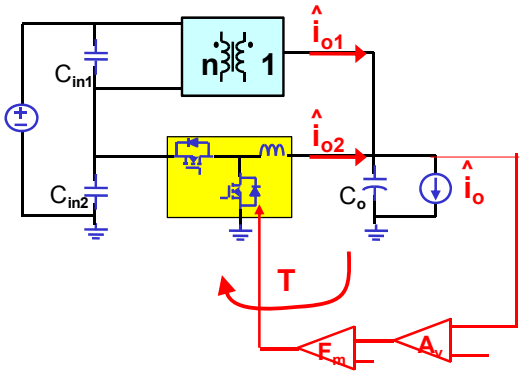



**Figure 2-11 Sigma converter with close voltage loop**

The close loop gain is T which is the product of $G_{vd}(s)$, $F_m$ and $A_v(s)$. With a closed voltage loop, the current transfer functions of $G_{ii1}(s)$ and $G_{ii2}(s)$ are modified to:

$$G_{ii1\_c} = G_{ii1} + G_{id1} \cdot A_v \cdot F_m \cdot \frac{Z_o}{1+T}$$

$$G_{ii2\_c} = G_{ii2} + G_{id2} \cdot A_v \cdot F_m \cdot \frac{Z_o}{1+T}$$

$G_{ii1\_c}(s)$ is the close-loop transfer function from load current to DCX current. $G_{ii2\_c}(s)$ is the close-loop transfer function from load current to Buck inductor current. Through the further mathematic analysis, the respective close-loop transfer function can be simplified into the following equations:

$$G_{ii1\_c} \approx \begin{cases} G_{ii1} & (\omega_c < \omega_{Hp}) \\ \dfrac{1}{1+\dfrac{s}{\omega_c Q}+\dfrac{s}{\omega_c{}^2}} & (\omega_c > \omega_{Hp}) \end{cases}$$

$$G_{ii2\_c} \approx \frac{1+\dfrac{s}{\omega_c}}{1+\dfrac{s}{\omega_c \cdot Q}+\dfrac{s^2}{\omega_c^2}}$$

Where $\omega_c$ is the crossover frequency of the control loop T, the close-loop current transfer function $G_{ii2\_c}(s)$ is related to the control bandwidth which means the buck inductor current will be determined by the close loop bandwidth. The same phenomenon for can be observed in Buck VR. However, for $G_{ii1\_s}(s)$, different control bandwidth design will result in different results. When the control bandwidth the lower than the high frequency double-pole position, the close loop $G_{ii1\_s}(s)$ will keep unchanged which means that the control loop does not impact the dynamic current response of DCX. For the control bandwidth higher than the high frequency double-pole, the close-loop $G_{ii1\_s}(s)$ transfer

function will also be controlled by the bandwidth, however, in this condition, the control bandwidth should be high enough.

A low control bandwidth design example is shown in Figure 2-12. The control bandwidth is designed to be lower than the high frequency double poles. The close loop $G_{ii2\_c}(s)$ has the resonant double-pole which is determined by the control bandwidth. While the close loop $G_{ii1\_c}(s)$ keeps the same as the open loop, which means the control loop does not impact the DCX current response. Actually, the control just function below its bandwidth, it will not affect the higher frequency behavior than it bandwidth so that the DCX current will keep its fast response when control bandwidth is low.

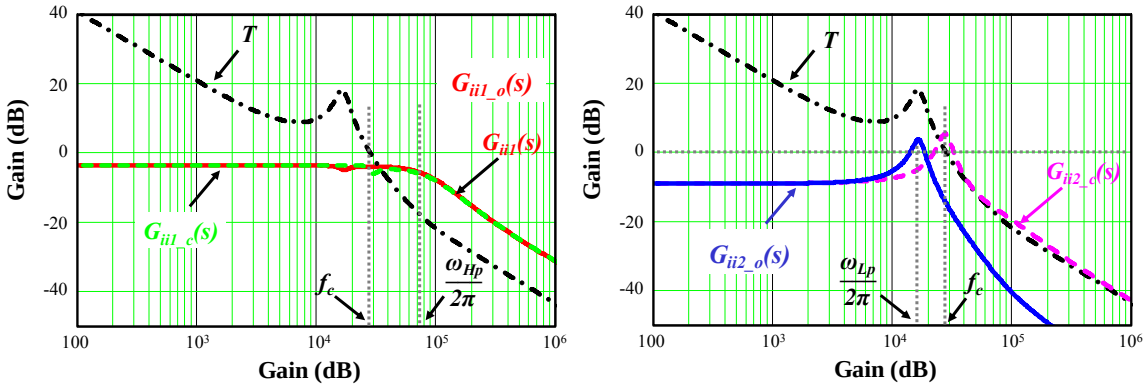



**Figure 2-12 $G_{ii1\_c}(s)$ and $G_{ii2\_c}(s)$ with low control bandwidth design**

Actually, faster DCX current response means less output capacitors can be used. For lower control bandwidth design, because the DCX current is faster than Buck inductor current, so that the more output capacitors could be saved compared with the Buck VR operating at the same control bandwidth.

But for the control bandwidth higher than the high frequency double-pole of Sigma VR, which is shown in Figure 2-13, both Gii1_c(s) and Gii2_c(s) double-pole will be

determined by the control bandwidth. Thus the DCX current and buck inductor current will both be determined by the control. Compared with the Buck VR case with the high control bandwidth design, the benefit of saving output capacitor is limited, because at this condition, the Buck inductor current is as fast as DCX current. This phenomenon will be also observed and discussed from the impedance perspective.

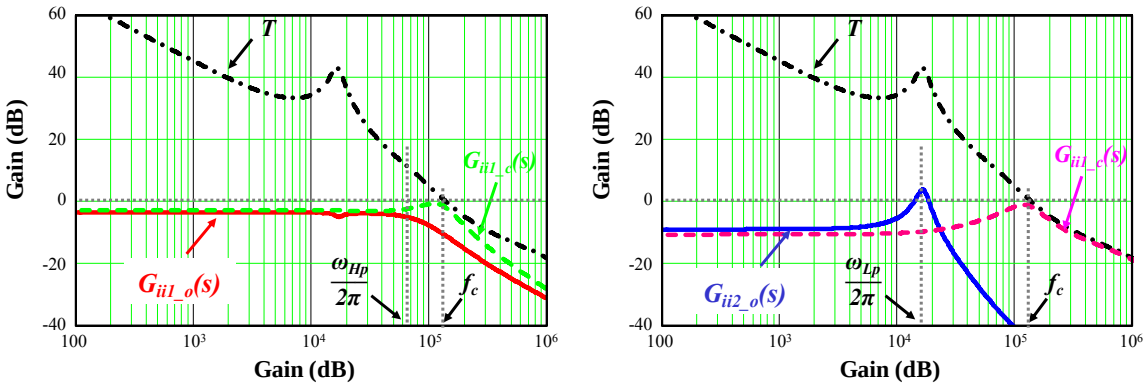



**Figure 2-13 $G_{ii1\_c}(s)$ and $G_{ii2\_c}(s)$ with high control bandwidth design**

From time domain, with the different control bandwidth design, the power stage current response waveforms and the voltage spike waveforms are shown in Figure 2-14. The left diagram is the low control bandwidth design. The Sigma power stage current $i_s(t)$ response faster than $i_B(t)$ which is Buck inductor current at the same control bandwidth. With the same output capacitors, the voltage spike of Sigma VR is smaller than Buck VR. Thus, in low bandwidth design, due to the faster power stage response of Sigma VR, the output capacitors can be saved keeping the same output voltage spike. On the other hand, the right side diagram shows the high control bandwidth design, the Sigma power stage current response the same as the Buck VR inductor current. Actually, at this condition, the control bandwidth determined the current speed as well as the output capacitor

configuration. Thus, the output voltage spike is almost the same between Buck VR and Sigma VR using the same output capacitors.

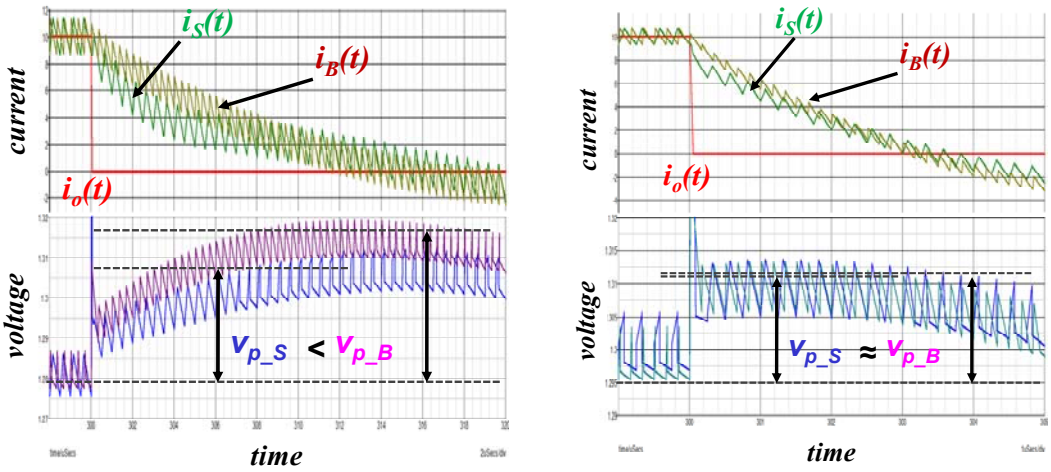



**Figure 2-14 Time domain simulation with low bandwidth and high bandwidth**

## 2.4 Impedance Reduction of Sigma VR

### *2.4.1 Impedance Specification from Intel*

As described before, in order to reduce the number of the output bulk capacitors for lower cost and smaller footprint, the adaptive voltage positioning concept is proposed [29]. With this concept, the whole output voltage tolerance window can be fully utilized for the output voltage transient compared with the tightly regulated condition. Despite the steady state AVP requirement, the load transient requirement is also critical. Evaluation of the transient response of VR can be from time domain or frequency domain. Intel also provides the frequency domain, the impedance specification for VR designer. It is corresponding to the time domain requirement which is re-shown here as well as the impedance requirement in Figure 2-15.

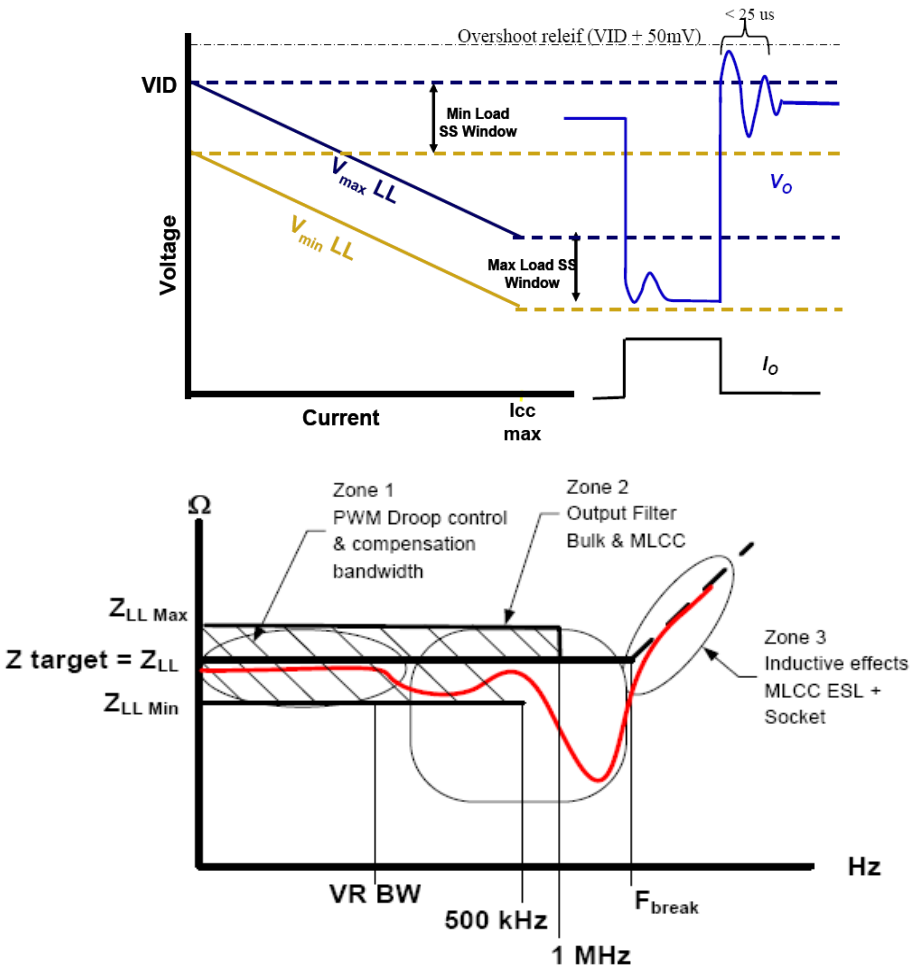



**Figure 2-15 Intel time domain and frequency domain specification for transient**

From Figure 2-15, the close-loop impedance cannot exceed the load line impedance $R_{LL}$ up to 2MHz. Under the control bandwidth, the impedance can be controlled to be constant. Upon the bandwidth up to the frequency where cavity capacitor handles, the bulk capacitors will be used to damp the impedance below the required specification during mid frequency range. Once the impedance specification is met, we can also regard that the time domain transient dynamic requirement is met.

### 2.4.2 Impedance Design of Buck VR

The impedance design of Buck VR is explained very detail in [26] [29] [30]. Active droop control is a good solution to achieve the constant output impedance design for Buck VR. It is composed by two control loops. Figure 2-16 shows the high current bandwidth loop design which is inner loop. By close the high bandwidth current loop, the power stage characteristics is reduced to first order system, since the inductor will behave like a controller current source. Thus, the impedance of Buck VR, which is represented as $Z_{oi\_Buck}$, is just the output capacitor impedance characteristic which is composed by output bulk capacitors and output decoupling capacitors.

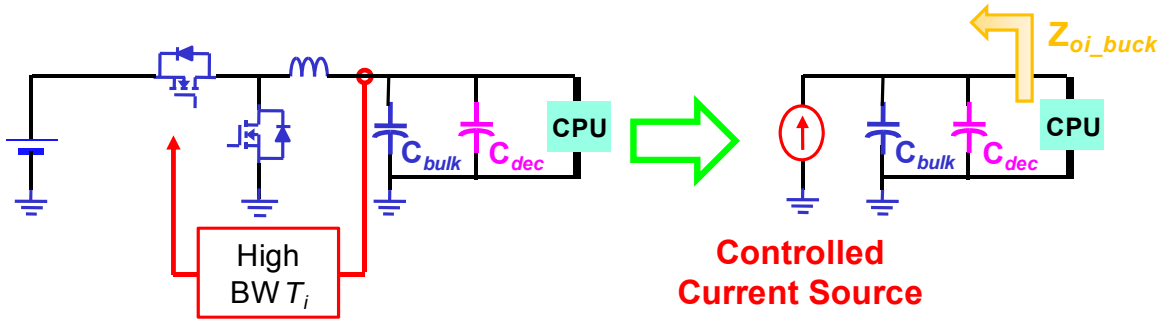



**Figure 2-16 High bandwidth current loop design of Buck VR**

Figure 2-17 shows an example of using 8*330uF SP output bulk capacitors and 18*22uF MLCC output decoupling capacitors. $Z_{oi\_buck}$ is the output impedance of VRM with current loop closed while the voltage loop is open. It is the parallel result of the output bulk capacitors and output decoupling capacitors.

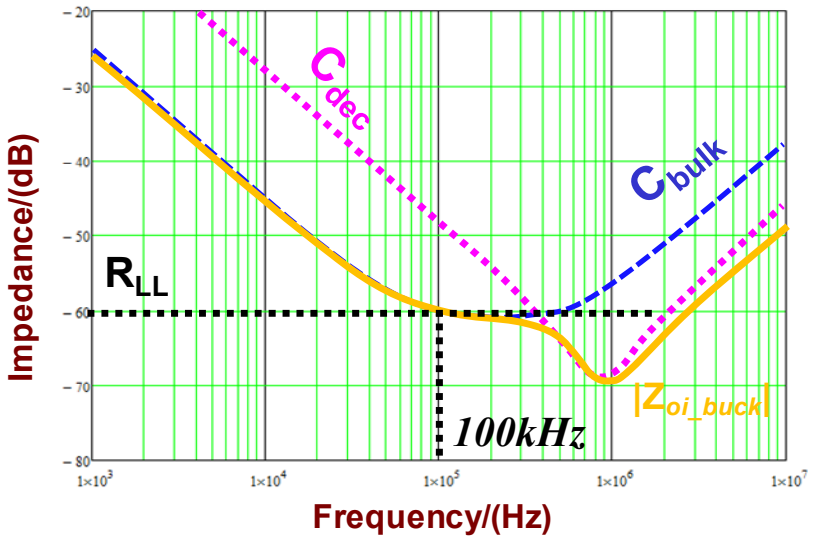



**Figure 2-17 $Z_{oi}(s)$ of Buck VR with high bandwidth current loop**

Close the output control $T_2(s)$, and design the close loop impedance to be constant to meet impedance specification which is shown in Figure 2-19.

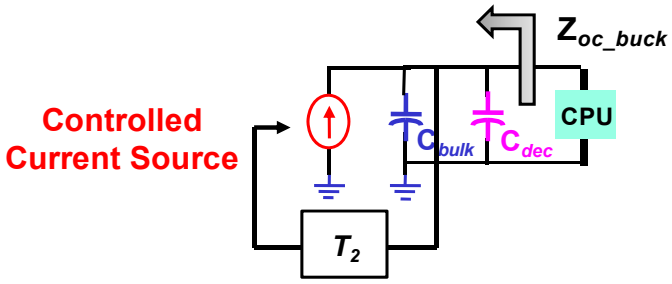



**Figure 2-18 Close outer loop of Buck VR**

With the appropriate design of the $T_2$ loop gain, the impedance under control bandwidth can achieve constant. Beyond control bandwidth, the passive output bulk capacitors and decoupling capacitors will help to meet the impedance requirement. Figure 2-19 shows the closed outer loop impedance $Z_{oc\_buck}$ which can meet the requirement of Intel's impedance specification. With the designed 100 kHz control bandwidth, 8 SP

output capacitors are needed for meeting the requirement. Actually, the control bandwidth is determined by the switching frequency, if the control bandwidth is different the required output capacitor number will also be different.

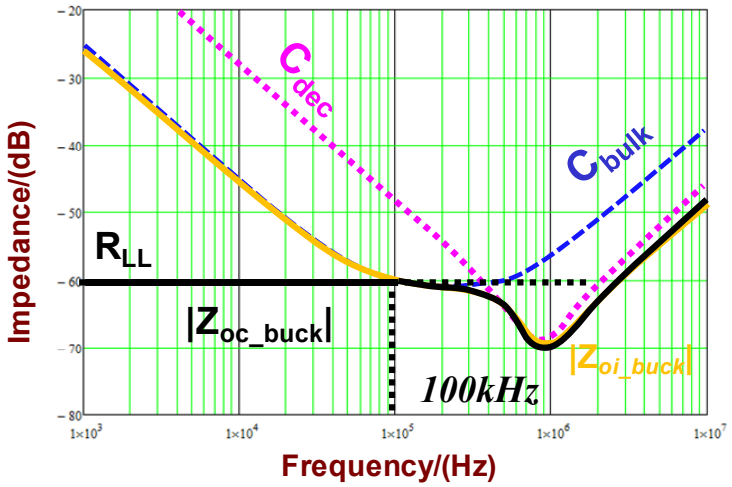



**Figure 2-19 Close loop impedance of Buck VR**

### *2.4.3 Impedance Reduction of Sigma VR*

Following the basic active droop control scheme of Buck VR, the active droop control scheme of Sigma VR can be shown in Figure 2-20. With sensing the Buck inductor current, the control scheme can free the DCX path and it does not need to sense the DCX output current. However, the current sensing coefficient should time the (1+nD) so that the feedback current information can represent the load current to achieve AVP.

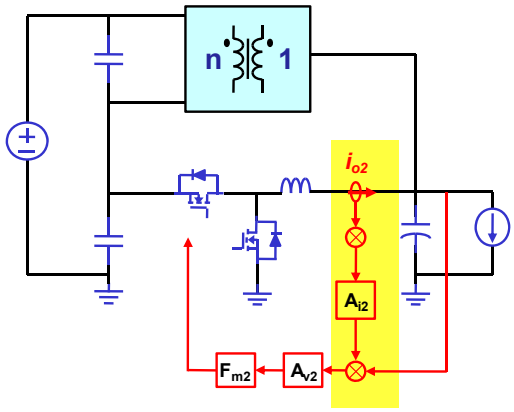



**Figure 2-20 Control scheme of Sigma VR**

Following the design criteria, the high bandwidth current loop is designed firstly. With the high bandwidth current loop, the buck inductor will behave like a controlled current source which is shown in Figure 2-21. For Buck VR, the close-current loop impedance $Z_{oi\_buck}(s)$ is composed by the output capacitors. However for Sigma VR, besides of the output capacitors, the of DCX path impedance $Z_{DCX}(s)$ also contributes to the $Z_{oi\_sigma}(s)$. $Z_{DCX}(s)$ is formed by the input capacitance impedance characteristics plus the DCX impedance which is $L_{out}$ and $R_{out}$. With the help of this impedance, the close-current loop impedance of Sigma VR will be smaller than Buck VR using the same output capacitors as shown in Figure 2-23.

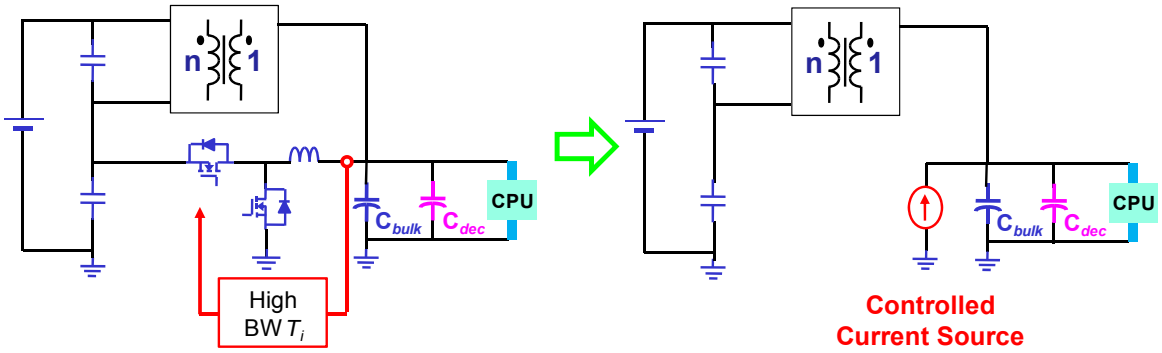



**Figure 2-21 High bandwidth current loop design of Sigma VR**

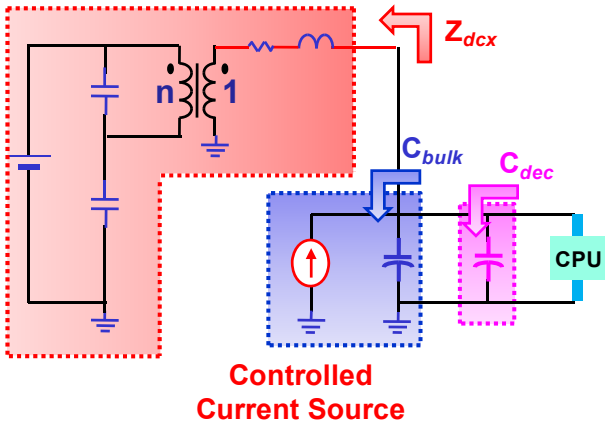



**Figure 2-22 Sigma Impedance with current loop closed and voltage loop open**

Figure 2-23 shows an example of the impedance reduction of Sigma VR. Using the same output bulk capacitors, the impedance of Sigma VR $Z_{oi\_sigma}(s)$ is lower than $Z_{oi\_buck}(s)$ until the DCX impedance $L_{out}$ and $R_{out}$ limits the reduction effect.

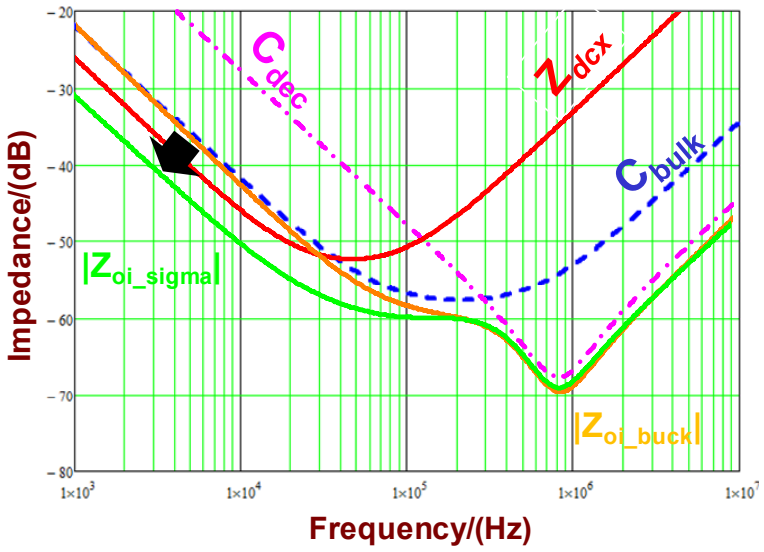



**Figure 2-23 Impedance Reduction by Sigma VR**

From the impedance reduction perspective, the input capacitor impact and the DCX impedance impact can be also observed. Just because of the help of the input capacitor

impedance help during load frequency, the total impedance of Sigma VR can be reduced which also means faster current dynamic response. And because $R_{out}$ and $L_{out}$ limits the impedance reduction effect which also is shown in Figure 2-23, the smaller DCX impedance could achieve more impedance reduction which also means faster dynamic response.

### *2.4.4 Bandwidth Reduction of Sigma VR*

The impedance reduction of Sigma VR brings some benefit from different perspective. On perspective is that if we use the same output capacitors of Buck VR and Sigma VR, with the impedance reduction characteristics, the control bandwidth of Sigma VR can be reduced.

Figure 2-24 shows an example. Both Buck VR and Sigma VR are using 6*330uF SP output capacitors. For Buck VR, the control bandwidth should be around 200 kHz for just 6 SP capacitors. But for Sigma VR, the control bandwidth of 100 kHz is enough which means lower switching frequency and higher efficiency.

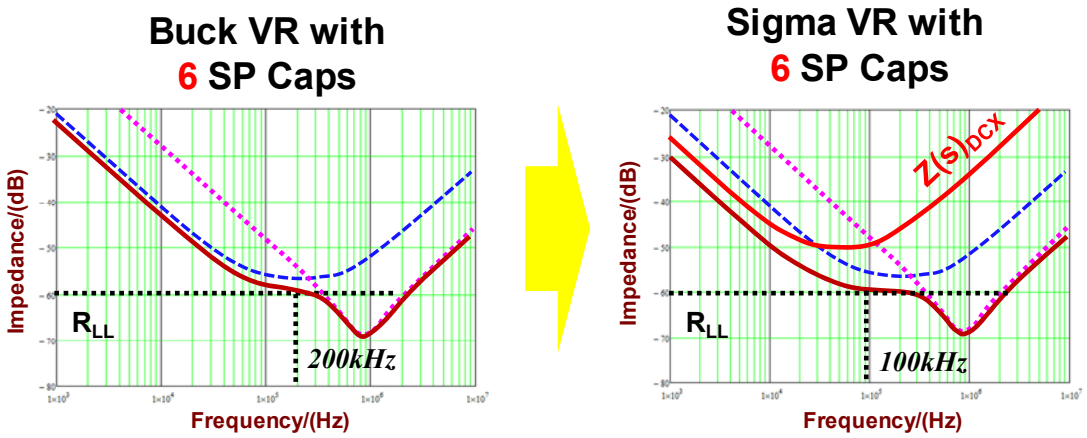



**Figure 2-24 Bandwidth reduction @ same output capacitors**

Actually, from time domain, this phenomenon can also be explained. Because the Sigma VR power stage is faster than Buck VR, it does not need so high bandwidth control for speeding up the power stage current. Thus, the bandwidth could be reduced.

### *2.4.5 Output Bulk Capacitor Saving of Sigma VR*

Another perspective to show the benefit of impedance reduction of Sigma VR is that if we use the same control bandwidth of Buck VR and Sigma VR, the output capacitors of Sigma VR can be reduced compared with Buck VR.

Figure 2-25 shows an example. Both Buck VR and Sigma VR are designed at 100 kHz control bandwidth. For Buck VR, 8 SP capacitors are needed for 100 kHz control bandwidth design. But for Sigma VR, 6 SP capacitors are enough for 100 kHz control bandwidth design.

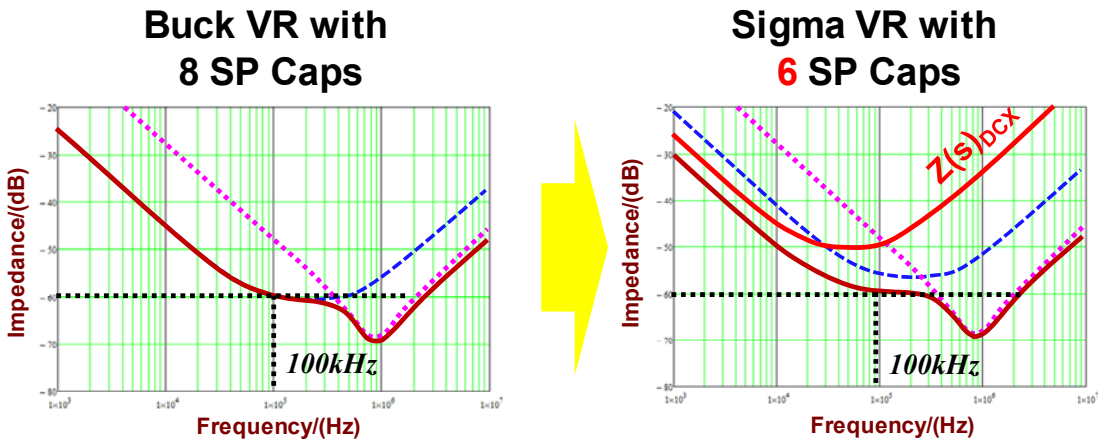



**Figure 2-25 Output capacitors reduction @ same control bandwidth**

Actually, from time domain, this phenomenon can also be explained. Because the Sigma VR power stage is faster than Buck VR with the same control bandwidth, it does not need so many output capacitors for providing transient energy.

## 2.5 Impedance Design of Sigma VR and Experimental Verification

The hardware setup is shown in Figure 2-26 as well as the measured efficiency of 8V input ZVS-QR DCX and 4V input Buck. From the diagram, we can see that the efficiency of ZVS-QR DCX is lower than 4V Buck at full load. The reason is that due to the low output voltage DCX, the RMS current going through transformer and secondary side SR is large, e.g. for 40A DC current, there is around 60A RMS current. In addition, 4V input Buck, because of the lower switching loss, can achieve relatively higher efficiency. Actually, this phenomenon is going to be discussed in the next chapter.

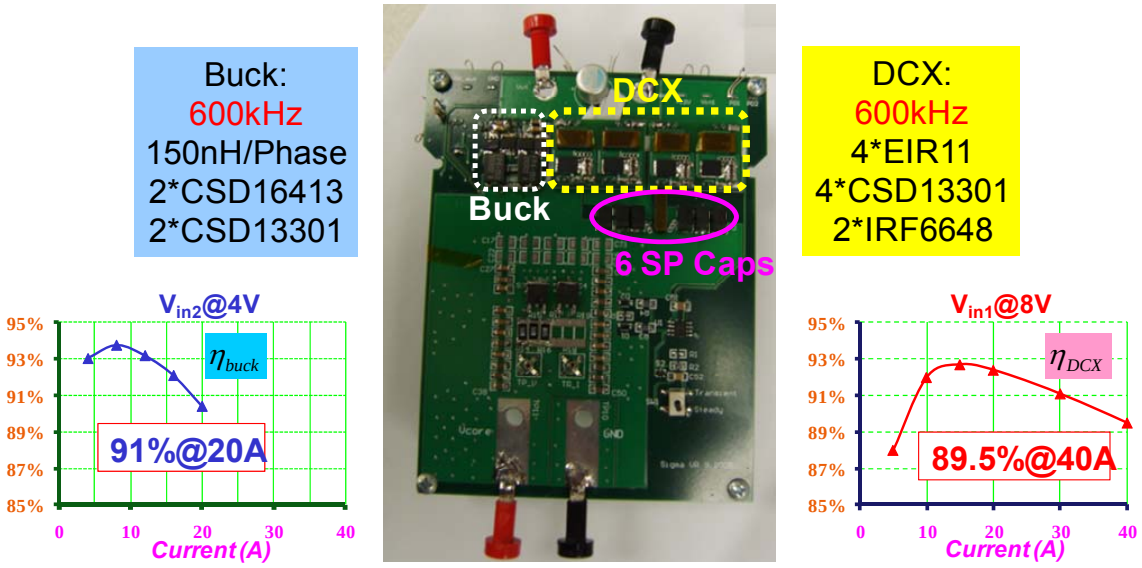



**Figure 2-26 Hardware setup and measured efficiency**

The circuit parameters are shown in Table 2-1. Two 60A Sigma cell is constructed for 120A solution. The energy ratio of DCX and Buck are 2:1, where 2-phase 40A DCX and 2-phase 20A Buck are needed. Both of these two converters are operating at 600 kHz. The 60A Sigma cell efficiency is shown in Figure 2-27 Sigma Overall Efficiency The overall efficiency approaches 90% which can meet the Intel, IBM and Google's efficiency requirement for VR.

**Table 2-1 Circuit Parameters of Sigma VR and 6-Phase Buck VR**

| | Configurations | Devices | Switching frequency | Magnetic components |
|---|---|---|---|---|
| Sigma VR | 2-phase buck and 2-phase DCX | Buck:(RJK0301+ CSD13301) DCX:(IRF6648+ 2*CSD13301) | 600k | 150nH/phase |

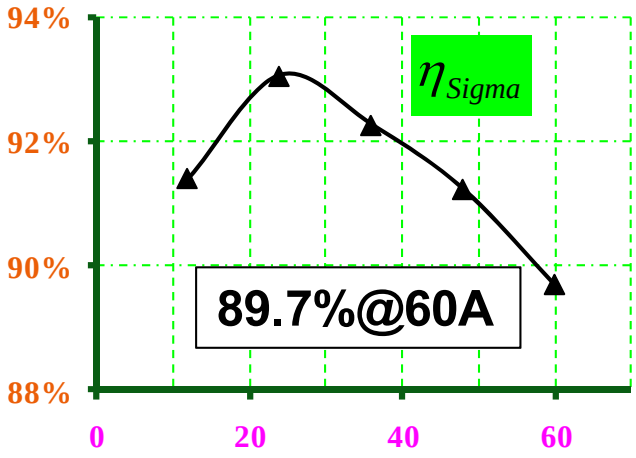



**Figure 2-27 Sigma Overall Efficiency**

For impedance design for transient response, the $R_{out}$ and $L_{out}$ of the designed ZVS-QR DCX is calculated as 1.8mΩ and 3nH by measuring the leakage inductance of the DCX transformer which is shown in Figure 2-29. Based on the impedance value of DCX, design the control bandwidth at 1/6 of the switching frequency, which is around 100 kHz, the required output bulk SP capacitor number is six.

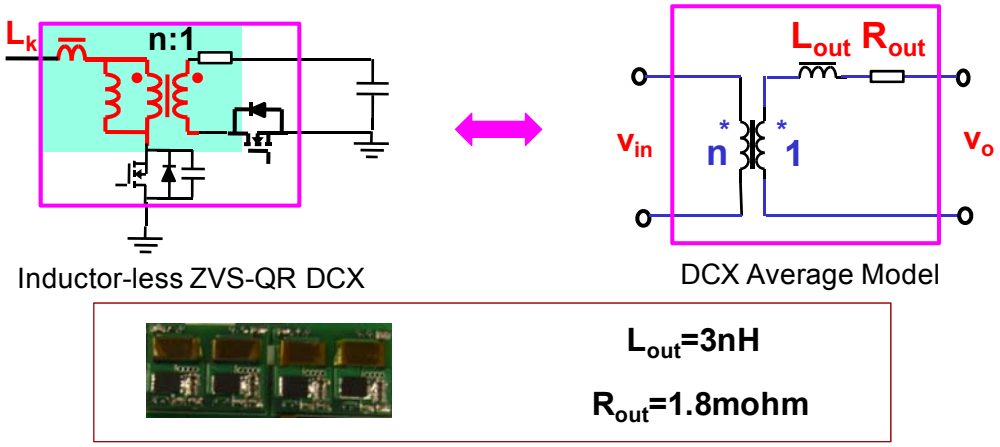



**Figure 2-28 DCX Impedance of the designed circuit**

The impedance final design of the Sigma VR is shown in Figure 2-29, where the impedance can meet the Intel's requirement.

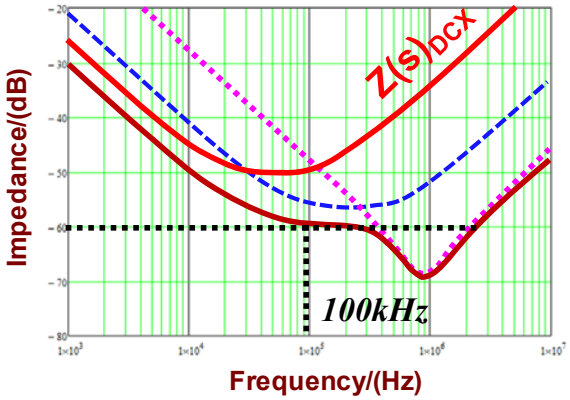



**Figure 2-29 6 SP Capacitors are needed for 100 kHz bandwidth design**

The measured control loop gain is shown in Figure 2-30. The measured control bandwidth is around 100 kHz and the phase margin is around 110 degree.

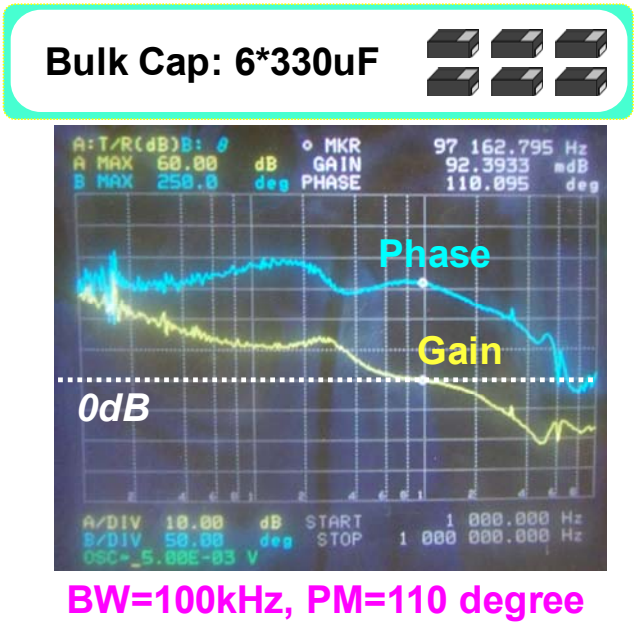



**Figure 2-30 Measured Control Bandwidth**

A 70A load step-up and step-down transient is applied for a transient performance test. The tested step-up and step-down transient response is shown in Figure 2-31. The AVP function is achieved, the also Figure 2-32 which is the zoom-in diagram of transient, the voltage overshoot can meet the VR11.0 specification, which means the impedance meets the requirement.

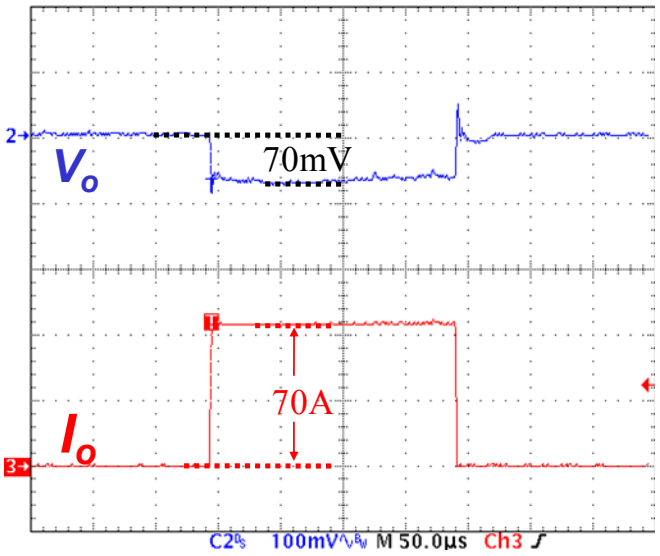



**Figure 2-31 Transient Response of Designed Sigma VR**

From Figure 2-32, the duty cycle increases or decrease immediately when load current step changes. And for the enlarged scale, we can see the step-down voltage has a 45mV voltage spike which is smaller than the 50mV overshoot limitation which can meet Intel's transient specification.

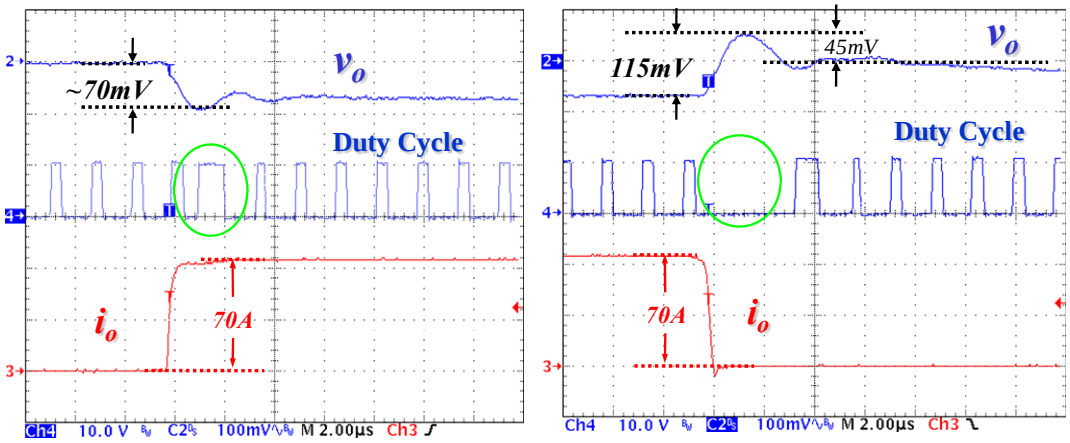



**Figure 2-32 Zoom-in Step-Up and Step-Down Responses**

## 2.6 Summary

This chapter focuses on analyzing the transient performance of Sigma VR. Both from time domain study and from impedance study, the faster transient DCX current response is detailed analyzed.

From the energy transfer point of view, through DCX, the energy can be directly transfers from the input voltage source to the load. From this concept, Sigma converter is going to have faster dynamic response than conventional Buck converter. Any through analyzing the transfer function of $G_{ii1}(s)$ and $G_{ii2}(s)$, we know that is true. The control impact to these two transfer functions, the current response speed of DCX and Buck in Sigma converter is much clearer. When the control bandwidth is low, the DCX current response speed is limited by the equivalent output inductance, while the Buck inductor current response speed is determined by the control bandwidth. Due to the faster DCX current response, the output capacitor has the possibility to be reduced. When the control bandwidth is high, higher than the DCX inductance critical frequency, for $L_{out}$ much smaller than $L_o$ case, both the DCX and Buck current response speed are limited by the control bandwidth. We can also observe this characteristic from the impedance point of view. At last, with our design circuit, the transient experimental result is given.

# Chapter 3. Efficiency and Power Density Improvement of Sigma VR

## 3.1 Introduction

Approximately 90% efficiency was achieved by the designed 1.2V/120A Sigma voltage regulator, and six SP bulk capacitors are needed for meeting the Intel's output impedance and load transient requirement 100 kHz control bandwidth design. Compared with 6 phase Buck VR designed at 100 kHz bandwidth, two SP output bulk capacitor is reduced. Although some benefit can be obtained from this special architecture, however it is not obvious, especially for the output bulk capacitor reduction. This chapter will discuss how to further improve the efficiency and achieve more output capacitor reduction for Sigma VR.

From the efficiency point of view, in the designed circuit, with 2/3 energy ratio for DCX which handles 80A from total 120A load current, and 1/3 from Buck which handles 40A, we can observe that the 4V input buck efficiency at full load is higher than DCX at 80A, which is conflict to the Sigma concept where the DCX is "supposed" to have higher efficiency than regulated Buck from the common sense. Let DCX handling more power is based on the concept of higher efficiency DCX. Based on the current device level, it is not always true. Thus, new power distribution should be considered for higher efficiency. Secondly, just 2 SP capacitors saving were achieved which is not so attractive from power density point of view. How to further reduce the output capacitor cost, footprint and

improve the efficiency performance is a critical issue for Sigma converter to become more attractive. Thus, in this chapter, we will investigate how to further improve the efficiency and power density of Sigma VR, and put the dedicated consideration and deeply thinking of this special architecture design for further efficiency and power density improvement.

By studying the power loss of the designed-Sigma VR, some solutions for reducing the power loss and improve the efficiency performance is proposed. First, as an important component, as well as an important power loss source of DCX, the transformer is needed to be optimized, both for higher efficiency and lower leakage inductance for faster transient response. Actually, based on state of the art device level, the low voltage DCX cannot achieve higher efficiency than 4V Buck at full load, so that the 2 to 1 power ratio between DCX and Buck is not the optimal one for the highest efficiency performance which is shown in Figure 3-1.

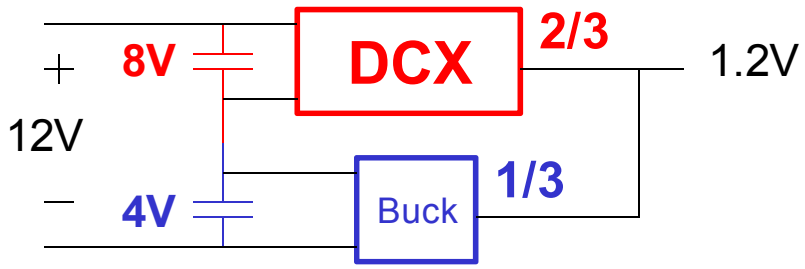



**Figure 3-1 2:1 Power Ratio between DCX and Buck**

The optimized energy distribution is studied in this Chapter for the highest efficiency where Sigma VR can achieve based on the current lever device. The power distribution concept can be applied for future lower output voltage application and high input bus voltage application for Sigma architecture if DCX can achieve high efficiency

performance. From power density point, changing the high-ESR SP capacitors into low-ESR ceramic capacitors gives us opportunity to achieve cost and footprint saving designed at high control bandwidth and pushing the control bandwidth higher can further reduce the output ceramic capacitor number based on the impedance design of Sigma VR. In the next several sections, different ways to improve Sigma VR efficiency and power density performance will be discussed.

## 3.2 DCX Transformer Optimization

As a critical part in Sigma architecture, DCX not only impacts the overall efficiency performance but also impact the transient performance. From the study of the loss breakdown of DCX, the transformer winding conduction contributes a lot to the equivalent resistance $R_{out}$. In addition, as we mentioned above, the DCX equivalent inductance $L_{out}$ is related to the transformer leakage inductance which has a great impact to the transient performance. Thus, the transformer design to reduce $R_{out}$ and $L_{out}$ can improve the efficiency and transient performance of Sigma VR. Actually, Vicor's DCX can achieve very low $R_{out}$ and $L_{out}$ value by highly integrated packaging technology. Figure 3-2 show Vicor's DCX product which converts 48V to 1V. The $R_{out}$ and $L_{out}$ comparison between the DCX from CPES and Vicor is listed in Table 3-1.


**Figure 3-2 CPES DCX vs. Vicor DCX**

**Table 3-1 Comparison between CPES's DCX and Vicor's DCX**

| | CPES | Vicor |
|---|---|---|
| $L_{out}$ | 3nH | 0.3nH |
| $R_{out}$ | 1.8mΩ | 1.1mΩ |

Back to our discrete solution, actually some research on the transformer design to reduce the winding loss and leakage inductance had also been conducted in CPES [35]. The optimization concept, named matrix transformer design can be applied to the Sigma VR DCX transformer design.

Take our 6:1 transformer for example. The original design of this transformer is just simply composed by a six primary winding and one set of secondary winding rounding the same core. By matrix transformer concept, the primary winding could be divided into two in-series 3:1 winding, and the secondary winding could be two set of winding paralleling together. By this new structure, the winding resistance of the transformer could be reduced to half of the original design, as shown in Table 3-2, and the efficiency can be improved. Not only will this structure reduce the winding resistance, but also the leakage inductance of the transformer will be which is reduced by around 50%. Further improvement of this concept can be applied by dividing the primary winding into three 2:1 in-series windings, three set of secondary winding are paralleled. This further reduces the winding resistance as well as the leakage inductance. The designed matrix transformer concept is shown in Figure 3-3, and the designed transformer structure is shown in Figure 3-4.

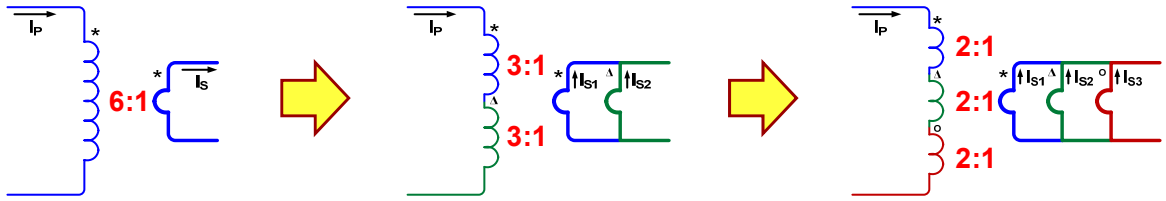



**Figure 3-3 Matrix transformer design**

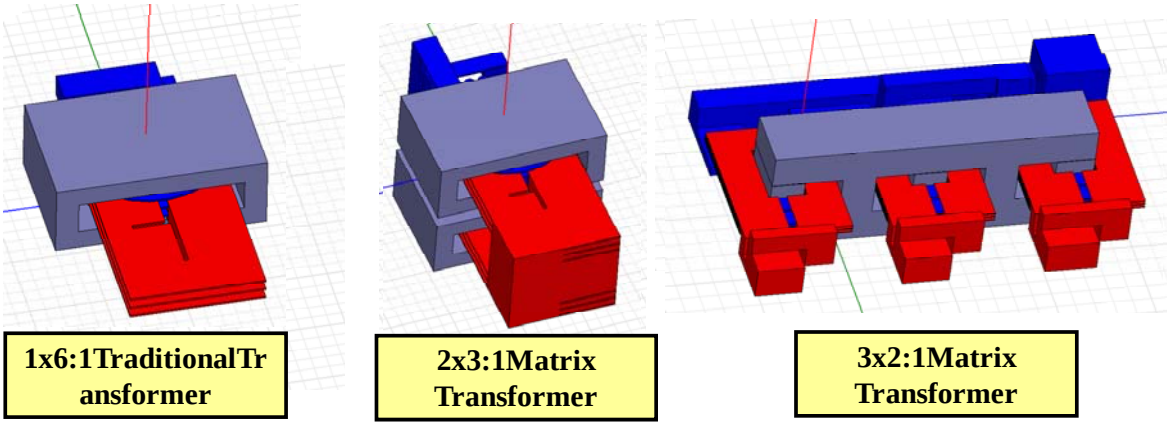



**Figure 3-4 Designed matrix transformer structures**

Through the optimization of the matrix transformer, the equivalent resistance of the transformer and the equivalent leakage inductance is listed in Table 3-2.

**Table 3-2 $R_{out}$ and $L_{out}$ with Different Transformer Design**

| | 1*(6:1) Design | 2*(3:2) Design | 3*(2:1) Design |
|---|---|---|---|
| $R_{out}$ | 1.2mΩ | 0.7mΩ | 0.5mΩ |
| $L_{out}$ | 5nH | 3nH | 1.5nH |

With the smaller $R_{out}$ from 1.2mΩ to 0.5mΩ, the efficiency of the DCX is improved from 88% to 92% which is shown in Figure 3-5. And by handling 2/3 of the total power, this 4% efficiency from DCX will lead to more than 2% efficiency improvement of the Sigma VR overall efficiency.

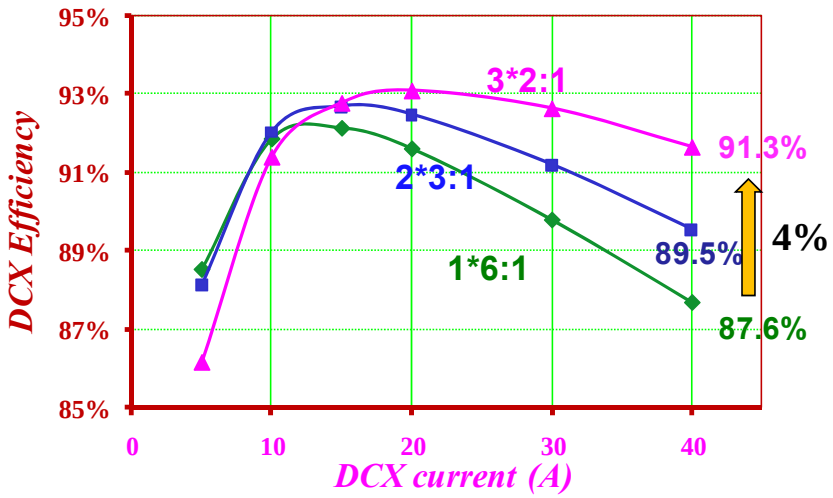



**Figure 3-5 DCX Efficiency with Different Transformer Design**

The reduction of the leakage inductance of the transformer can reduce the required number of the output capacitor. As shown in Figure 3-6, keeping the control bandwidth at 100 kHz, the required SP output capacitor number can be reduced from 7 to 3.

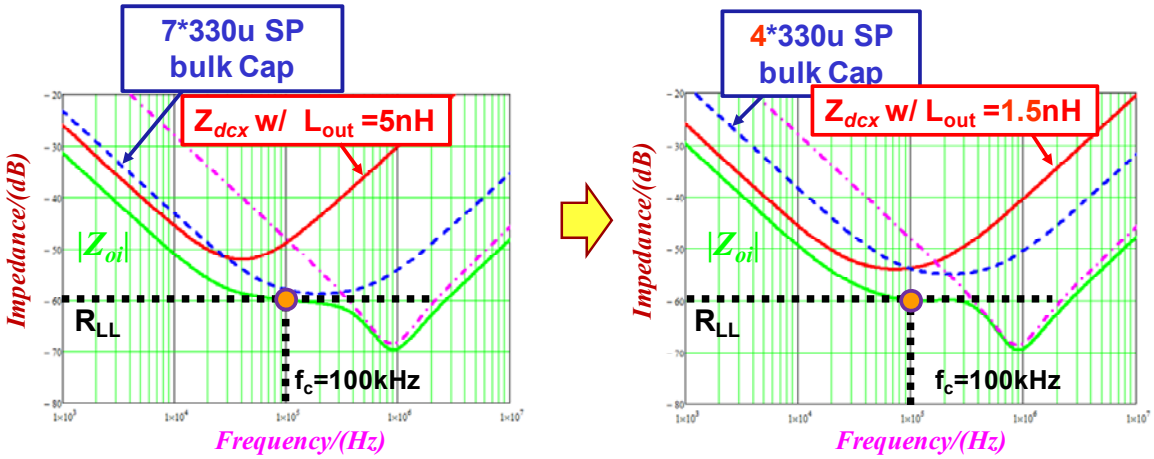



**Figure 3-6 Smaller Lout results in Less Output Ceramic Capacitor**

As mentioned above, Vicor is using more advanced integration technology to achieve even small $R_{out}$ and $L_{out}$. If applying Vicor's DCX in Sigma architecture, the total efficiency can be improved further as well as the required number of output capacitors.

Through the effort of doing this, the sigma structure will become more attractive by applying the high performance DCX.

## 3.3 Pushing Control Bandwidth for Less Ceramic Capacitors

In our discrete solution for the ZVS-QR DCX design, the leakage inductance of the DCX transformer is relatively large. It is around 3nH reflected to the output side. As what we studied before, the DCX impedance $L_{out}$ will impact the DCX current response as well as the output bulk capacitor configuration. The impact of $L_{out}$ to the output capacitor is shown in Figure 3-7. When $L_{out}$ is 3nH, in order to meet the impedance specification at 100 kHz bandwidth design, 6*330u SP capacitors are needed. If $L_{out}$ is reduced to 0.3nH, the number of the SP capacitor can be also reduced to 3. From the impedance perspective, the DCX impedance helps to achieve sigma impedance reduction until $L_{out}$ takes place. When $L_{out}$ is relatively large the impedance reduction is not obvious even the frequency range is low. On the other hand, when $L_{out}$ is small, the impedance reduction effect will be more obvious which can help to reduce the output capacitors.

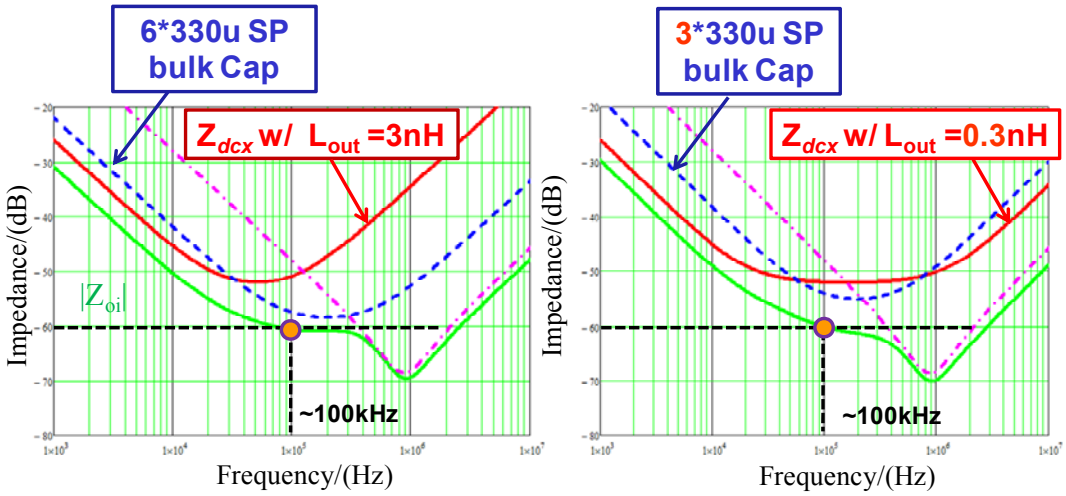



**Figure 3-7 $L_{out}$ Impact to Output Capacitors**

From time domain, the smaller $L_{out}$, the faster current response can be achieved by DCX and the less output capacitors could be used. Figure 3-8, Figure 3-9 and Figure 3-10 show the relationship between the control bandwidth and different output capacitor with different $L_{out}$ value.

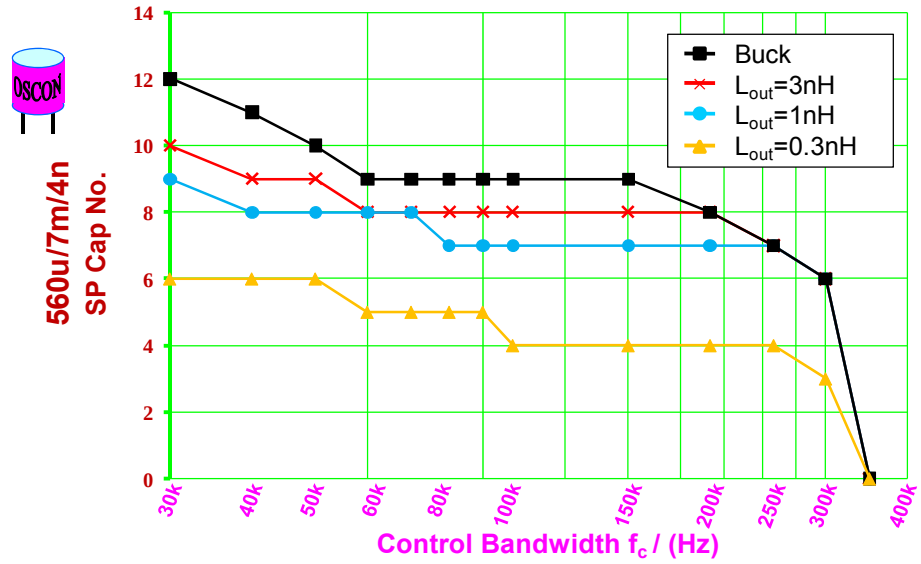



**Figure 3-8 Control bandwidth vs. OS-Con Bulk Caps Number with Different $L_{out}$**

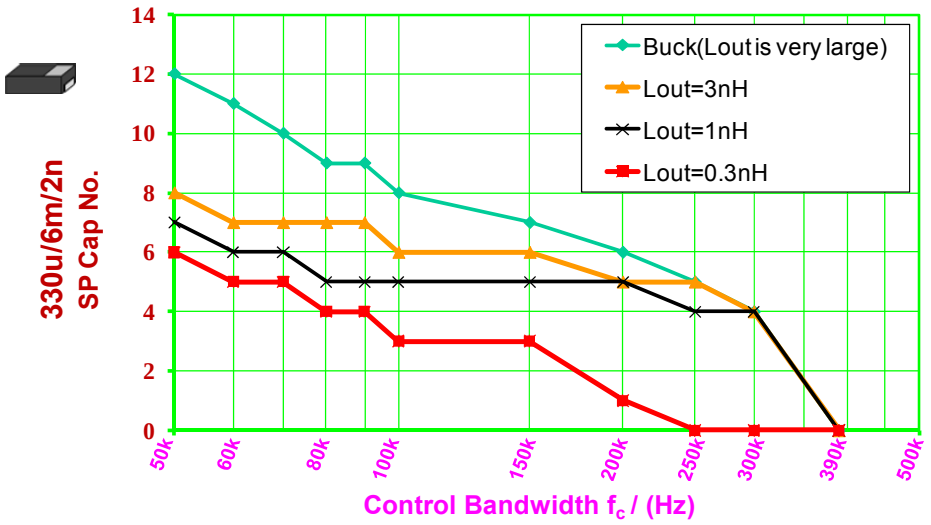



**Figure 3-9 Control Bandwidth vs. SP Bulk Caps Number with Different $L_{out}$**

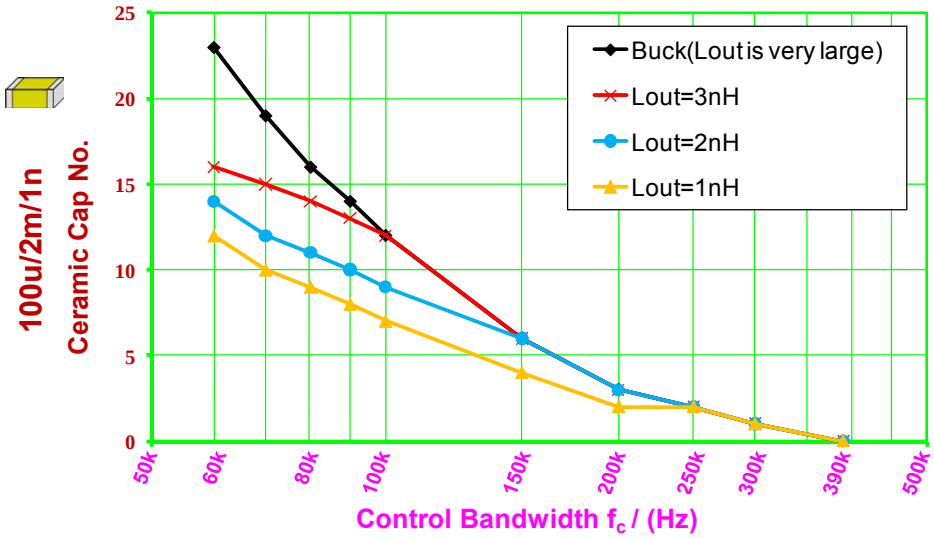



**Figure 3-10 Control Bandwidth vs. Ceramic Bulk Caps Number with Different $L_{out}$**

Using OS-Con and SP capacitor, other than very small $L_{out}$ value, pushing the bandwidth to be high is not helpful to reduce the output capacitor number due to the relatively large ESR during certain concerned frequency bandwidth range. But for the ceramic capacitor, pushing the bandwidth is able to continually reduce the output capacitor number due to the small ESR and the $L_{out}$ value is not so critical for output capacitors.

Figure 3-11 shows that the cost reduction and footprint reduction can be achieved by changing the output bulk capacitor from SP to ceramic capacitor. Below 100 kHz control bandwidth, OS-Con and SP bulk capacitors have the cost benefit compared with the ceramic capacitors. However, beyond 100 kHz, ceramic capacitor begins to show the benefit both from the cost and footprint. Thus, there is a hint that if we want to push the control bandwidth, changing output bulk capacitors to ceramic capacitors is a most cost-effective solution. What is more, due to the low ESR effect, further pushing the control can further reduce the output ceramic bulk capacitor number.

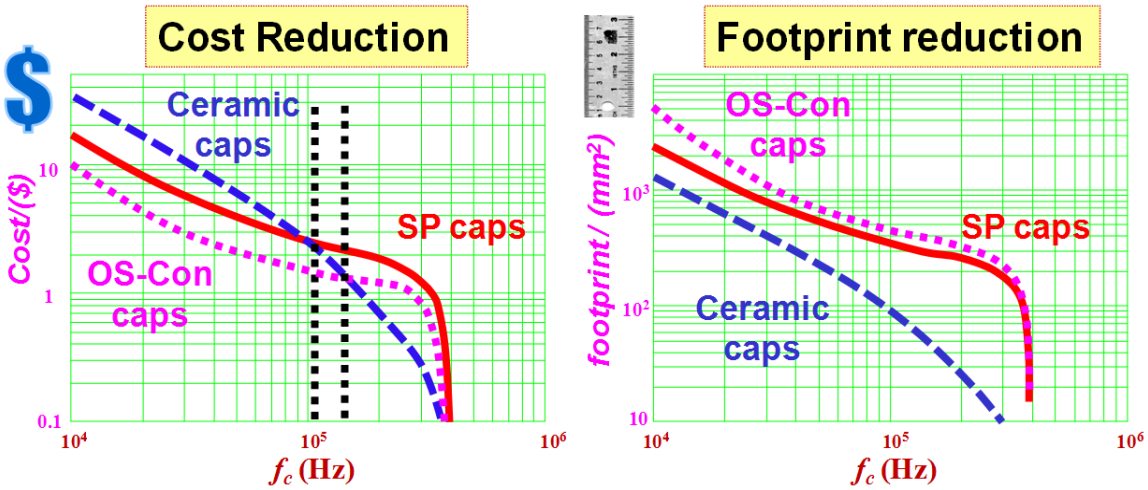



**Figure 3-11 Cost and Footprint Comparison with Different Caps**

Figure 3-132 and Figure 3-13 shows that the benefit of further pushing the control bandwidth for using ceramic bulk capacitors. By pushing the control bandwidth from 100 kHz to 200 kHz could continually reduce the output ceramic capacitor number from 12 to just 3 which cannot be achieved by using other two bulk capacitors. Greater cost and footprint saving can be achieved by further pushing the control bandwidth.

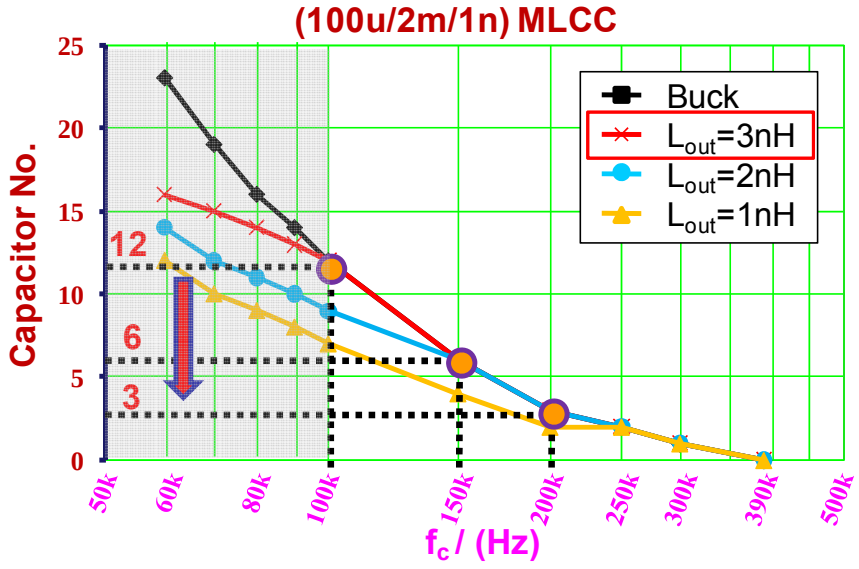



**Figure 3-12 Pushing Bandwidth to Reduce Ceramic Cap**

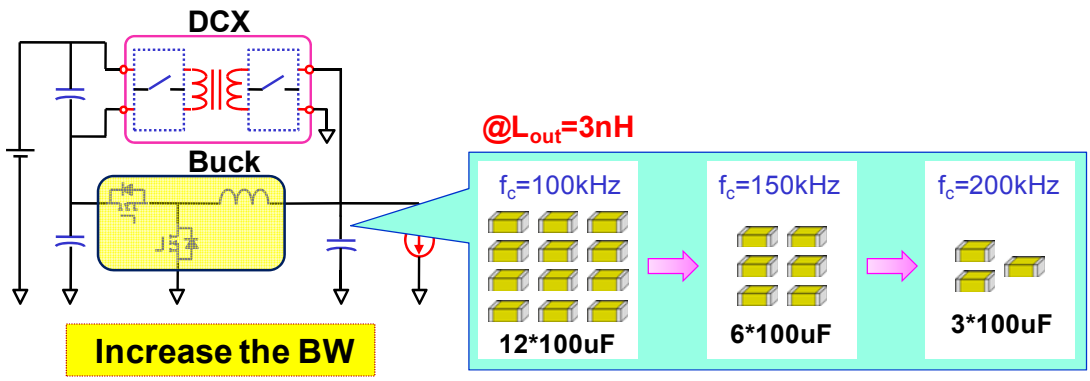



**Figure 3-13 Just 3 100uF Ceramic Caps are needed for 200 kHz Bandwidth**

The experimental result of further pushing the control bandwidth is shown in Figure 3-14. Right hand side is the 100 kHz control bandwidth design, with 12*100uF ceramic capacitors, the transient response can meet specification. The phase margin of the control loop is around 110 degree.

On the left hand side, the control loop bandwidth at 200 kHz is shown with the phase margin at 66 kHz. The 100 kHz bandwidth design and 200 kHz design are both based on the 600 kHz switching frequency, the phase margin is reduced by pushing the control bandwidth. Just 3 output ceramic capacitors are used where 9 ceramic capacitors can be further reduced. The output voltage transient waveform is shown. From the transient response waveform, we can see that around 70mV voltage drop during step-up transient, and 140mV voltage spike during step-down transient, which meet the Intel's transient requirement.

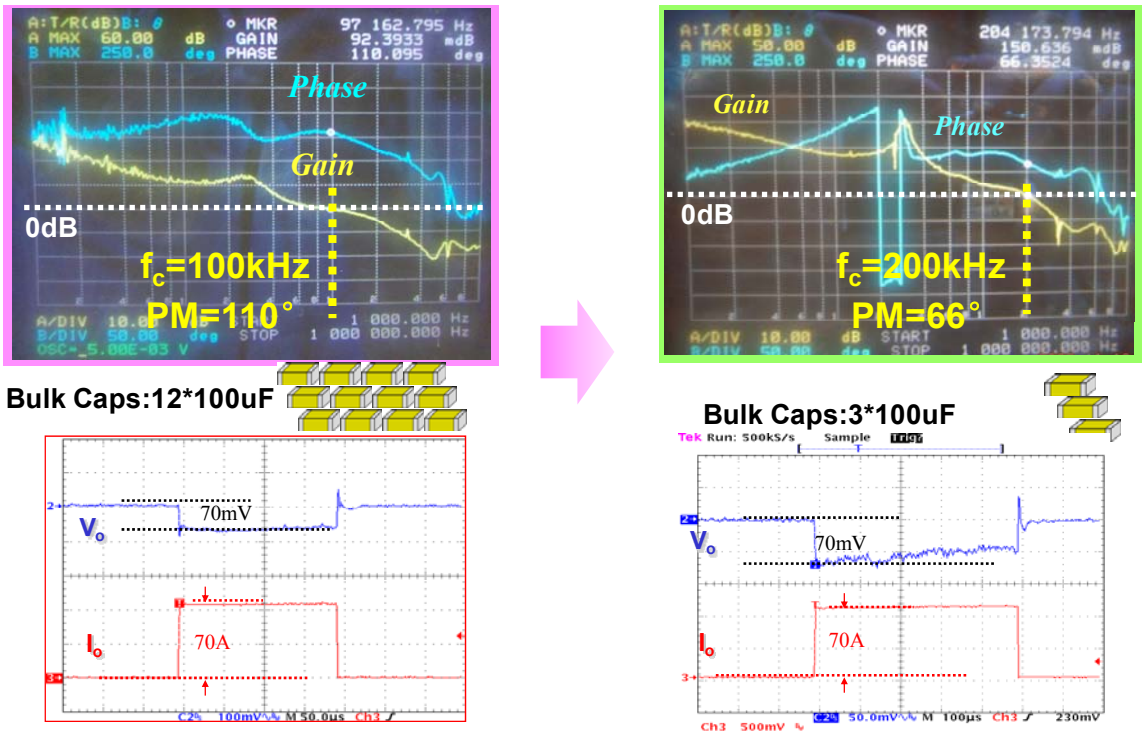



**Figure 3-14 Experimental Result of Reducing Output Caps**

## 3.4 Reducing the DCX Switching Frequency

In Sigma Architecture, reducing the DCX switching frequency is a possible way for further improving the overall efficiency. For conventional Buck, it is not available to reduce switching frequency for higher efficiency while keeping higher control bandwidth for less output capacitors. But for Sigma VR, the control bandwidth is just determined by the regulated Buck's switching frequency. DCX switching frequency will not influence the control bandwidth design. Thus, it is possible for us to change the switching frequency of DCX for even higher efficiency performance. An example of efficiency performance is shown in Figure 3-15 where the DCX switching frequency is reduced from 600 kHz to 300 kHz.

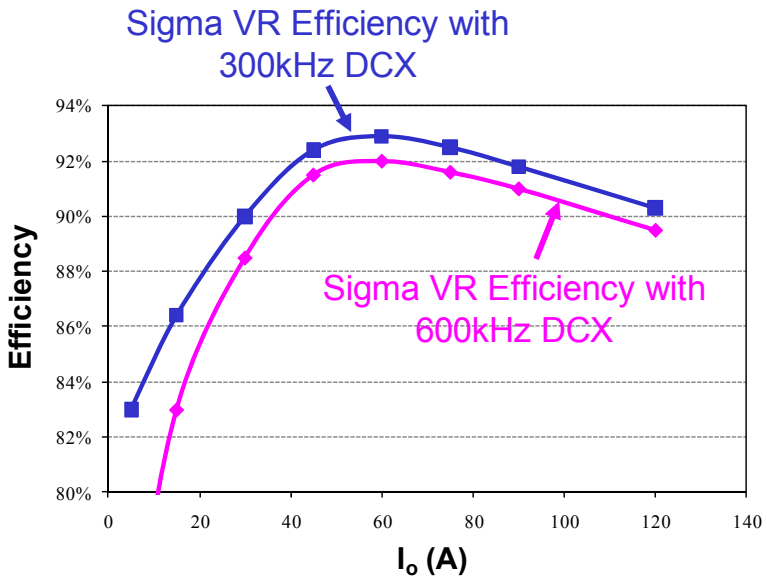



**Figure 3-15 Efficiency Comparison with Different Fs DCX**

Actually, although the efficiency is not so impressive in this design, which is because of the main power loss of ZVS-QR DCX, a specific resonant converter, contributes not too much for the switching loss but for the conduction loss. But if some PWM type DCX is used, the efficiency benefit of reducing switching frequency will be more obvious and more attractive.

## 3.5 Optimal Energy-Distribution of Sigma VR

In our previous design of 1.2V/120A Sigma VR as shown in Figure 3-16, the power ratio of DCX and Buck is around 2:1, where DCX handles 2/3 of the overall current while Buck just for 1/3. As we can observe, the 4V buck efficiency at full load is higher than DCX at full load due to the lower input voltage with the state of the art of devices. Buck is more efficient than DCX, why not transfer some energy from DCX to Buck? It will make

the overall Sigma VR more efficient. Based on this simple concept, re-distribute of the energy between DCX and Buck to achieve optimal efficiency is discussed in this section.

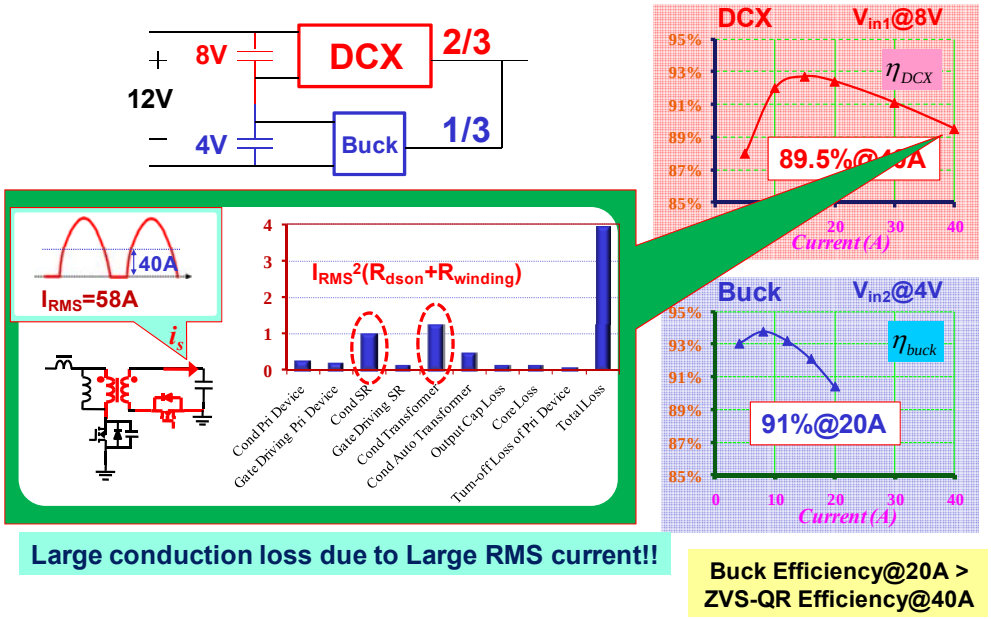



**Figure 3-16 Lower DCX efficiency**

From Figure 3-16, the full load Buck VR achieves around 91% efficiency which is higher than DCX at full load condition. Due to the low input voltage, Buck converter can achieve lower switching loss and lead to higher efficiency. In addition, the reason of the lower efficiency DCX performance is that the huge RMS current going through the winding resistance of DCX transformer and secondary SR. In order to maximize the overall performance, transfer some energy from DCX to Buck maybe useful. We can see that conduction loss from transformer and SR are two main loss of DCX. This results in the lower efficiency performance of DCX.

Based on this consideration, three energy re-distribution cases are considered as shown in Figure 3-17. Case 1 is our original design. In case 2, we increase the energy of

higher efficiency Buck by reducing the energy from DCX. And the energy ratio is set to be 1:1. Further transfer energy from DCX to Buck is the Case 3 condition, where DCX just handle 5/12 of the overall power while Buck handles 7/12 of the total power. Based on the loss calculation, the efficiency performance of these three cases is discussed as following. The same devices are used for these three cases:

For Buck: 600 kHz, 1*IRF6710+2*IRF6797;

For DCX: 600 kHz, 1*IRF6648+2*CSD13301.

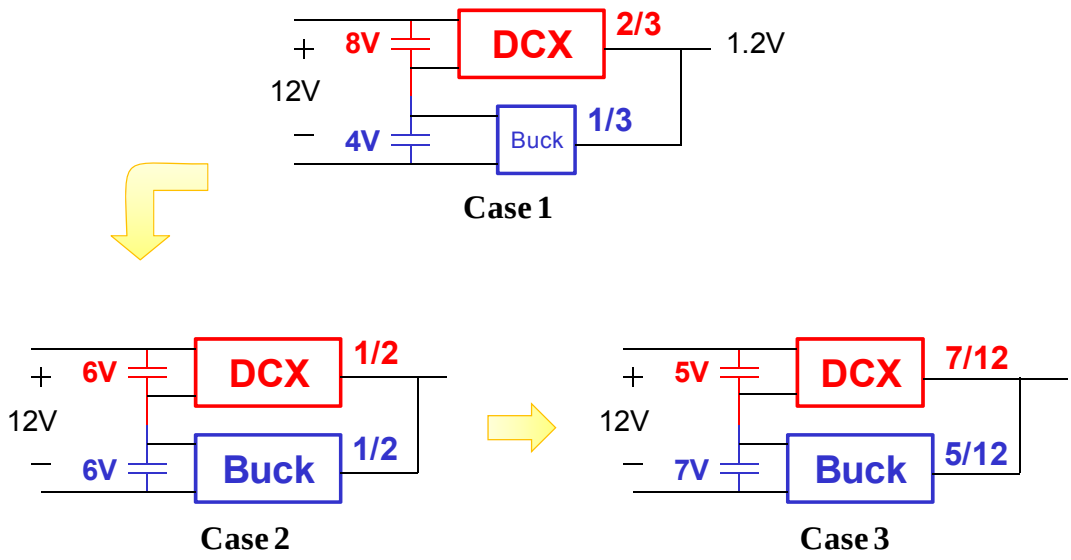



**Figure 3-17 Different Power Ratio Design**

### *3.5.1 Case 1: (2/3) DCX Power and (1/3) Buck Power*

The efficiency performance of the previous design 2:1 power ratio is re-shown again in Figure 3-18. The full load efficiency of 8V DCX is around 89.5% while the 4V Buck full load efficiency is around 91%. By combining these two converters together, the overall efficiency of Sigma VR at full load is around 89.7%.

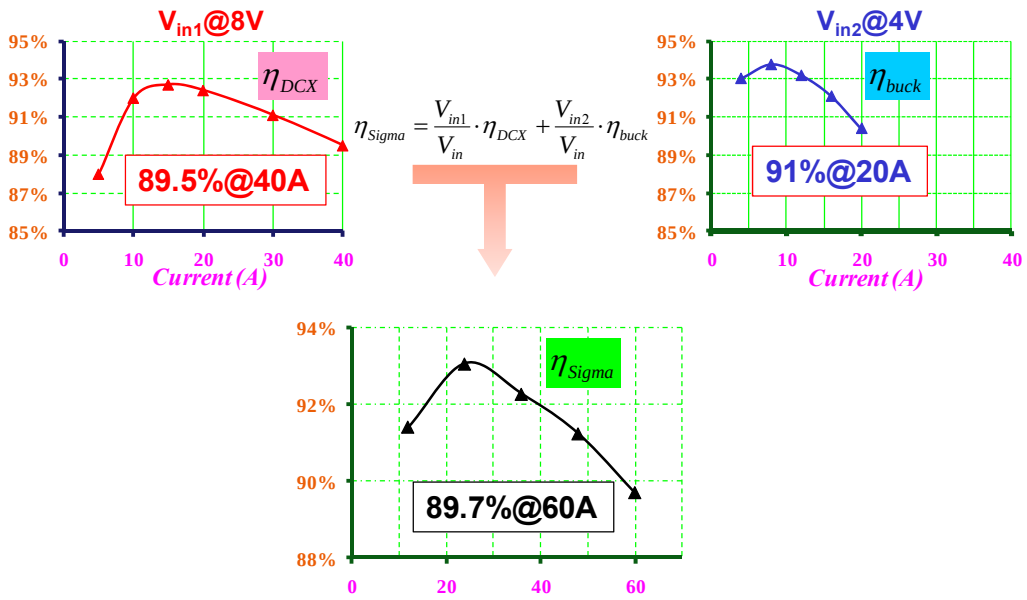



**Figure 3-18 Efficiency Performance of Case 1**

### *3.5.2 Case 2: (1/2) DCX Power and (1/2) Buck Power*

The efficiency performance of 1:1 power ratio of case 2 is shown in Figure 3-19. Due to the lower power and current handling, the DCX efficiency rise from 89.5% to 90.7%. And for Buck converter, because the input voltage is increased as well as the handling power, the efficiency drops from 91% to 89.8%. However, combining these two converters together, the overall efficiency of Sigma VR can achieve 90.7% which is around 1% efficiency improvement.

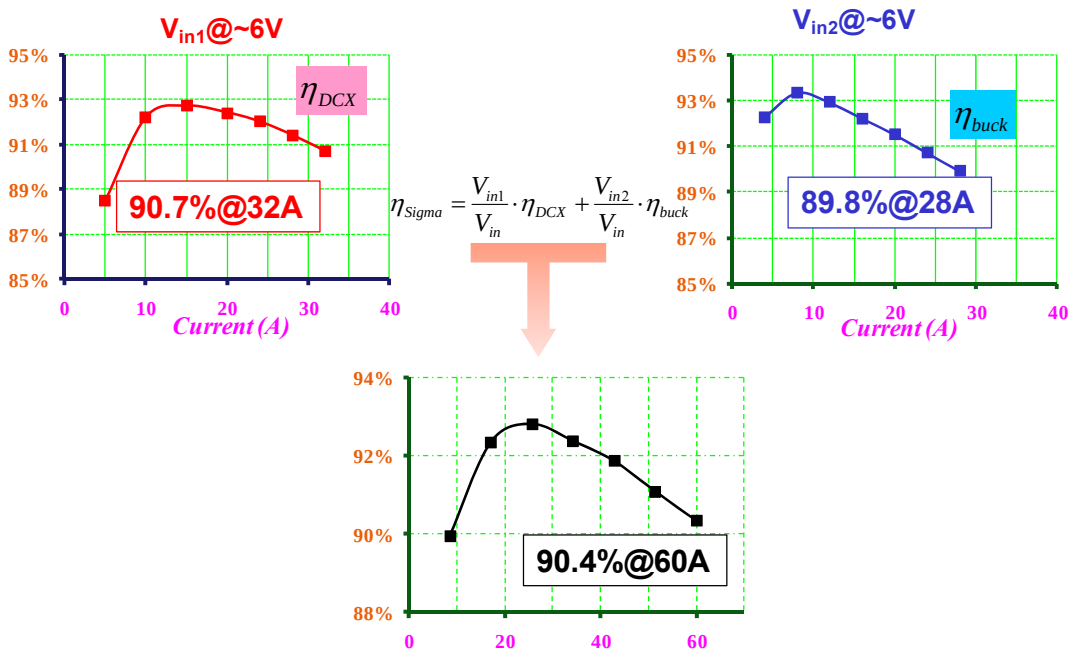



**Figure 3-19 Efficiency Performance of Case 2**

### *3.5.3 Case 3: (5/12) DCX Power and (7/12) Buck Power*

Further transfer the energy from DCX to Buck, the efficiency performance of 5:7 power ratio between DCX and Buck is shown in Figure 3-20. Due to the even lower power and current handling, the DCX efficiency rise again from 90.7% to 91.8%. And for Buck converter, because the input voltage is increased as well as the handling power, the efficiency drop from 89.8% to 88.4%. Although the DCX can achieve higher efficiency, however due to the small portion power handling by it, the overall Sigma VR efficiency drops back from 90.4% to 89.8% again compared with Case 2. There is a trade-off for efficiency performance of DCX and Buck. In order to achieve optimal efficiency, based on different design or choose of DCX and Buck, different power ratio might be more suitable for highest efficiency.

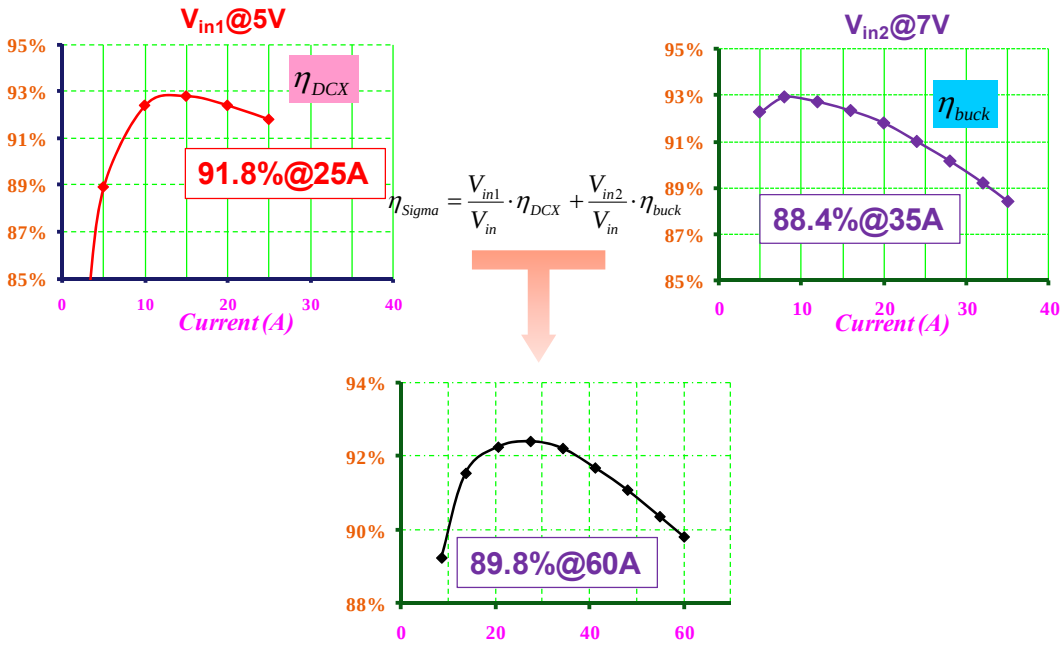



**Figure 3-20 Efficiency Performance of Case 3**

The efficiency comparison of these three cases is shown in Figure 3-21. Based on the current devices level, the highest efficiency can be achieved for around 1:1 power ratio condition where DCX handles half of the overall current and Buck handles another half.

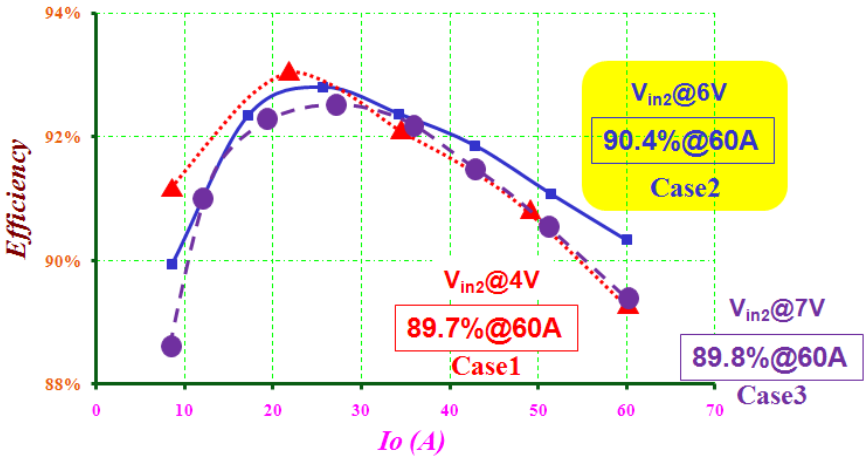



**Figure 3-21 Efficiency for different Power Ratio**

## 3.6 Sigma Architecture of Future VR

According to Intel's roadmap, the CPU output voltage will continue to reduce decreasing in order to reduce the CPU power consumptions. In the near future, the output voltage will drop to sub-1V level. This decreasing output voltage will impact the efficiency performance of current multi-phase Buck solution, using the current devices. For example, using the most advanced packaging devices with DirectFET, the single stage multi-phase Buck efficiency will drop to around 85% at full load with 8 phases for 160A, which is shown in Figure 3-22.

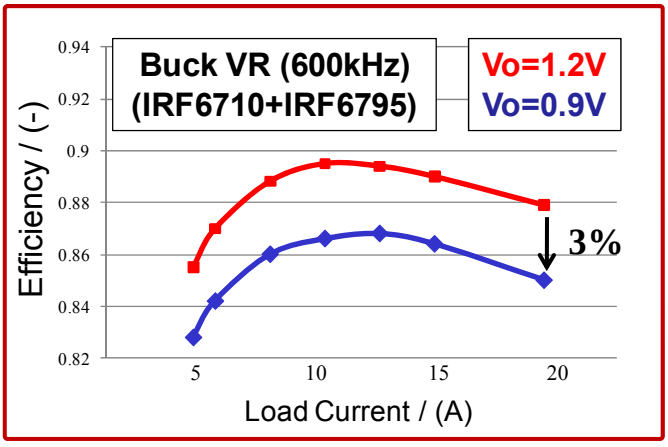
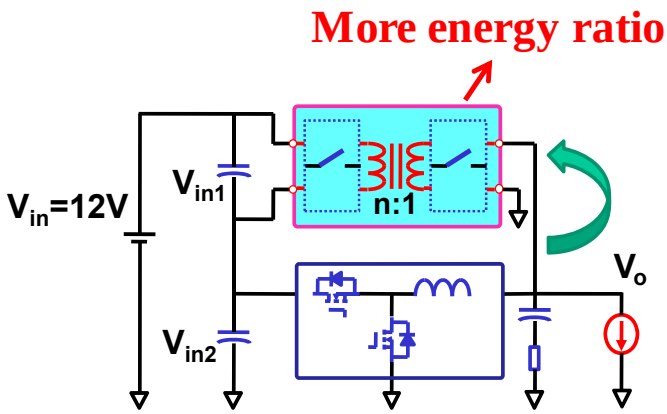



**Figure 3-22 Buck Efficiency with Future Lower Output Voltage**

But for sigma architecture, lower output voltage provides the opportunity for us to change the power ratio of DCX and Buck. It is possible for us to transfer more energy to DCX, if DCX can achieve high efficiency performance, thus the sigma architecture will be more attractive for future lower output voltage application. The basic concept of changing the power ration of sigma VR could be should in Figure 3-23.




| $V_o$/(V) | n | $V_{in1}$/(V) (Energy Ratio) | $V_{in2}$/(V) (Energy Ratio) |
|---|---|---|---|
| 1.2 | 6 | 8 (67%) | 4 (33%) |
| 1.0 | 8 | 9 (75%) | 3 (25%) |
| 0.8 | 11 | 10 (83%) | 2 (17%) |

**Figure 3-23 More Energy Ratio of DCX for Future VR**

As a design example, sigma architecture with 160A/0.9V is proposed. With lower output voltage, it's suitable for us to increasing power ratio of DCX and Buck from 2:1 to 3:1. Two of the Sigma Structures of Figure 3-24 paralleled together to get 160A.

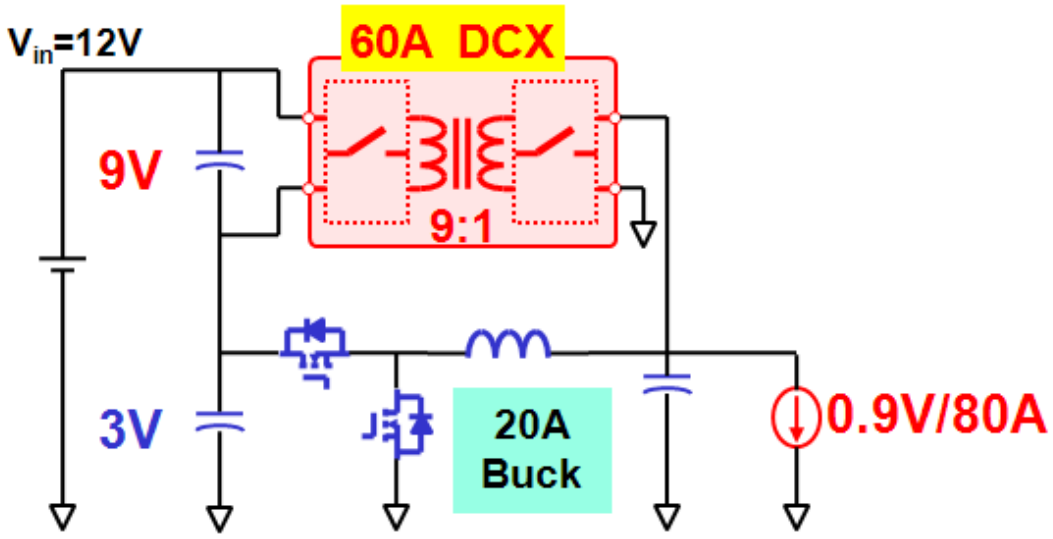



**Figure 3-24 A Design Example for Energy Ratio for Future 0.9V VR**

With this concept, the predicted efficiency for 0.9V Sigma VR efficiency can be also around 89%, compared with the current solution whose efficiency is 85%. There are around 4% efficiency benefits from this new topology.

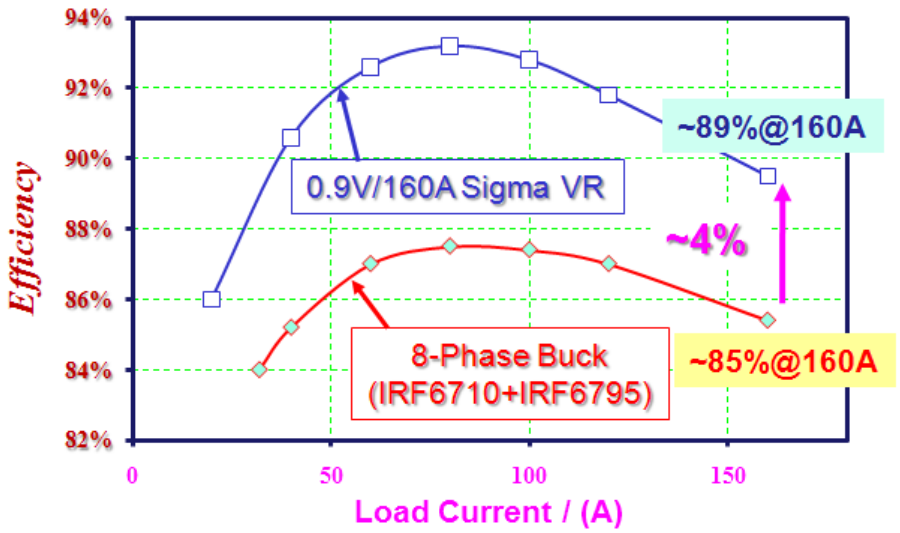



**Figure 3-25 Efficiency Comparison for Future VR Application**

## 3.7 Considering Higher than 12V Bus Voltage

Sigma architecture will be more attractive if DCX can achieve high efficiency. Through the industry's effort on DCX by integration technology, a typical efficiency curve of Vicor's 48V to 1V DCX (also named VTM) is shown in Figure 3-26. Around 92% is achieved for the current range from 70A to 140A. Assume that with the improving technology in the future, the low voltage DCX can also achieve 92% efficiency, thus, the sigma architecture has the opportunity to utilize this high performance DCX.

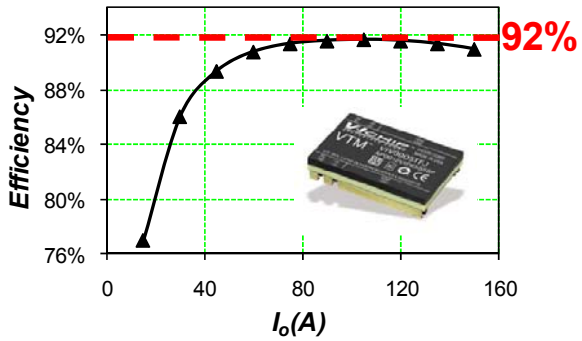



**Figure 3-26 Efficiency for Vicor's DCX**

With the current 12V input bus voltage, the power ratio of DCX and Buck in Sigma architecture will be limited for proper operation. But for potential better performance DCX from industry or future development, the 12V input bus cannot give the best overall performance to Sigma architecture because the power ratio will be limit by this relatively low bus voltage. In order to maximize the power ratio of DCX and let DCX plays more important roles, higher than 12V bus voltage is considered. Higher bus voltage can make DCX handle more power and make DCX determined the overall efficiency performance but also achieving regulation. The concept is shown in Figure 3-27.

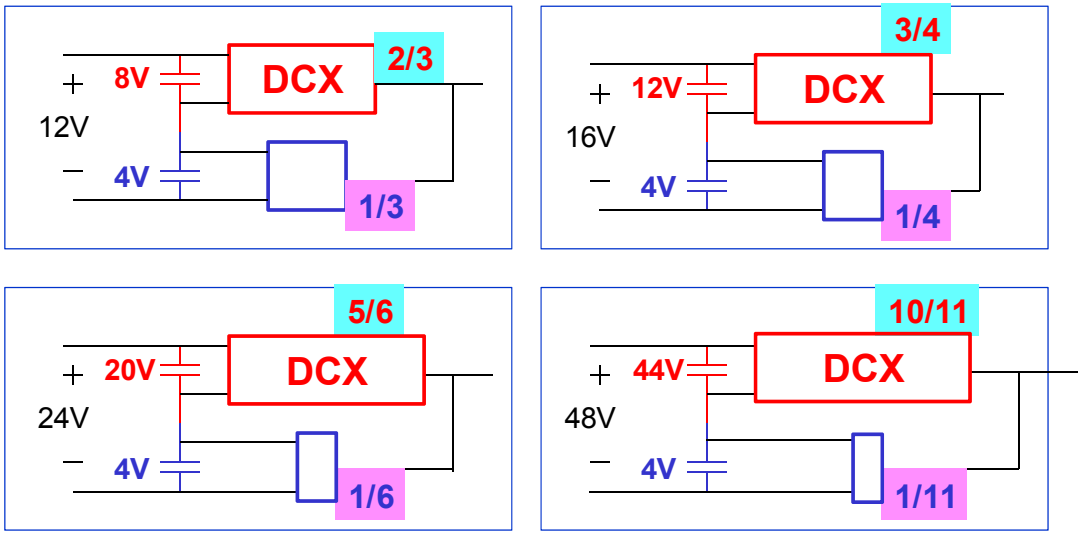



**Figure 3-27 Higher than 12V Bus Voltage**

By increasing the input voltage, the overall sigma efficiency will be mainly determined by DCX, so that the efficiency of overall sigma VR can almost achieve 91-92% range.

Figure 3-28 is a typical power delivery system for microprocessor. The PFC circuit rectifies the 110C AC voltage to 380~400V DC voltage. A DC to DC converter in the

downstream lowers down the 400V DC voltage to 12V voltage bus. The single-stage Buck voltage regulator serves as the POL to transfer the 12V bus voltage to around 1V which is needed by microprocessor. Through this power delivery structure with the typical efficiency shown in Figure 3-28, the end to end system efficiency range is from 77%~81%.

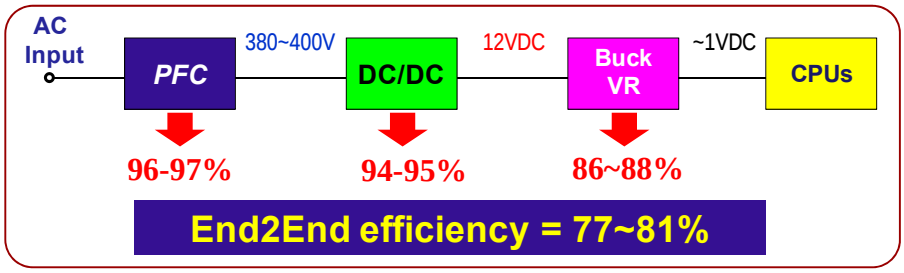



**Figure 3-28 Typical power delivery system for microprocessor**

With the proposed new power delivery system architecture which is shown in Figure 3-29. Changing the 12V bus voltage to 48V bus voltage, and replacing the DC/DC to DCX which convert the high 400V DC voltage to 48V, and replacing the original single stage Buck VR to Sigma VR, the end to end efficiency will be improved. From the diagram, we can see that, due to the high 48V bus voltage. The DCX efficiency can achieve 96%~97%. The 48V Sigma VR will have good efficiency performance which could achieve around 91%~92%. By changing this structure, the end to end efficiency can achieve 84%~87% which is about 6% ~ 7% efficiency improvements.

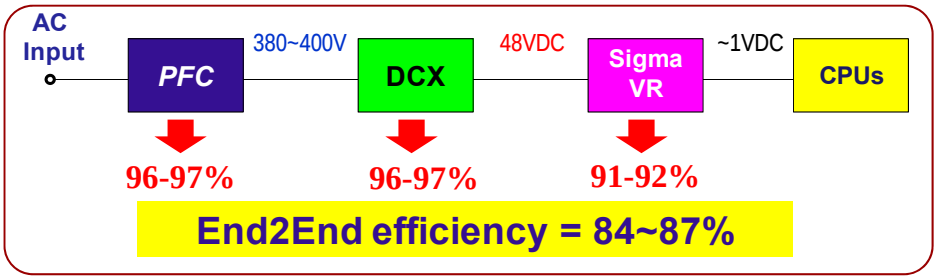



**Figure 3-29 Proposed power delivery system for microprocessor**

# Chapter 4. Summary and Future Work

This thesis mainly focuses on analyzing the DCX current transient response of Sigma VR and the impact factors, from time and impedance domain. Pursuing higher efficiency and higher power density from pre-designed Sigma VR is also one important target of the study. In addition, the potential benefits of Sigma VR to achieve both high efficiency and high power density are investigated.

## 4.1 Transient and Impedance Analysis of Sigma VR

Through the help of DCX and input capacitors, Sigma VR can achieve lower impedance than conventional Buck converter. Thus, using the same capacitors, the control bandwidth could be reduced. Or from another point of view, if designing at the same bandwidth, Sigma VR can achieve output capacitors reduction. Appropriate input capacitance is chosen for provide enough energy from DCX path. What is more, the impedance of DCX limits the energy transit from input to out as well as the benefit of this capacitor reduction characteristic. In this thesis, the factors which impact the transient response of Sigma VR is detailed analyzed.

- ***The Choice of the Input Capacitor***

  The input capacitor plays an important role during Sigma VR load current transient happens. It should provide enough energy for DCX current to response quickly. Otherwise the current will exhaust the energy very quickly and cannot support the output capacitor for transient response. In order to make sure the energy to be enough for at least providing transient current, the input capacitance

cannot be smaller than (D/n) · Co. And in that case, smaller total input capacitor can replace larger output capacitor and maintain the same transient response.

- ***Smaller DCX Impedance is Desired***

  The DCX impedance is a critical factor that will dramatically impact the DCX current response. Although the input capacitor can provide enough energy during transient, large DCX impedance will hinder the faster energy transfer for input side to output side, resulting worse output voltage transient response. The smaller DCX impedance, the faster current response of DCX as well as the higher potential power density could be achieved.

- ***More Attractive for Low Control Bandwidth Application***

  In Sigma VR, the current response of Buck inductor is determined by the control bandwidth, while that of DCX is mainly determined by input capacitor and output impedance of DCX. Compared with conventional Buck VR, the faster current response is more attractive in low control bandwidth application (for desktop or laptop), because the faster DCX current response will gives more benefits.

## 4.2 Efficiency and Power Density Improvement

Based on the previous study of Sigma VR, in order to maximize the performance, some improvements are investigated. They could be listed as following:

- ***Optimization of DCX transformer***

  The DCX performance is mainly impacted by the transformer design, not only for high efficiency but also for high power density. With the more advantaged

matrix transformer design, the DCX $R_{out}$ could be reduced to 1/3 of the original design, resulting in more than 2% efficiency improvement, and the equivalent $L_{out}$ is reduced to around 1/2 of original design and 30% output capacitor saving can be achieved.

- ***Pushing bandwidth to reduce the output ceramic capacitors***

  With the study of the different type of output bulk capacitor's relationship with the control bandwidth, when the bandwidth is greater than 100 kHz, using ceramic capacitor can both achieve cost and footprint saving. And due to the relatively large ESR of OS-Con capacitor and SP capacitors, further pushing the bandwidth higher than 100 kHz cannot greatly reduce the output capacitor number. But if using ceramic capacitor, further pushing the control bandwidth to 200 kHz can continually reduce the output ceramic capacitor from 12 to 3. What is more, if using ceramic capacitor, the impact the DCX $L_{out}$ is not as critical as low control bandwidth case.

- ***Reducing DCX frequency for higher efficiency***

  On the special Sigma architecture, through reducing DCX frequency is possible for improve the efficiency performance. In conventional Buck VR, reducing switching frequency is unavailable for higher efficiency, considering the power density issue. However, sigma architecture provides us an opportunity to do that thing. Although in our design case, the efficiency improvement is not significant due to the specific DCX we chosen, the more attractive aspect comes from this concept by other DCX topologies.

- ***Re-Distribution of DCX and Buck Energy for High Efficiency Performance***

  Based on current device technology, the 4V Buck could achieve higher efficiency at 40A than DCX at 80A based on the designed 2:1 power ratio of these two converters. For the current devices level, re-distribute some energy from DCX to Buck could achieve even higher efficiency. But for the future, with the devices technology increased, with the improved performance of DCX, Sigma concept would become more attractive for future lower output voltage application and higher 12V input bus voltage condition, based on the concept of letting DCX handle more power. By changing the system to 48V bus voltage, the end to end efficiency will be improved about 6%~7%.

## 4.3 Future Work

There are still some remaining works to be done which are related to this thesis:

- ***High Efficiency Low Output Voltage Resonant - DCX***

  Unregulated DCX is commonly regarded as high efficiency solution due to no or very small switching loss because of the resonant behavior. And this concept works very well in higher output voltage case. However, if using this concept in low voltage, such as VR application, although the switching loss could be saved, but the larger conduction loss coming from resonant behavior will harm the efficiency back. How to make DCX efficiency attractive for low output voltage application is important.

- ***High Frequency DCX Transformer Design***

Low impedance DCX is preferred not only for Sigma VR but also for itself. And the transformer is a critical component which determines the efficiency and transient issue of the DCX. Some magnetic integration work may be done to reduce the leakage inductance of DCX.

- ***Sigma VR in Other Application***

  In this dissertation, the major applications are for the server computers. Ideally, sigma VR will be more attractive in high voltage application for transferring energy to DCX. From system point of view, Sigma architecture also has the potential to achieve high efficiency while providing different needed bus voltages to different applications.

# Appendix I

The transfer functions of Sigma converter are listed in this Appendix for reference. The equations are derived and simplified by assuming that the DCX equivalent inductance $L_{out}$ is much smaller than Buck inductance $L_o$ base on the small-signal-model in Figure A-0-1, where $L_{out}$ and $R_{out}$ are the equivalent inductance and resistance of DCX, $L_o$ is the equivalent Buck inductance, DCR includes the $R_{dson}$, inductor ESR and trace resistance. $C_{in1}$ and $C_{in2}$ are input capacitance for DCX and Buck. $C_o$ is the output capacitance. $R_o$ represents the load resistance. D is the steady state duty cycle.

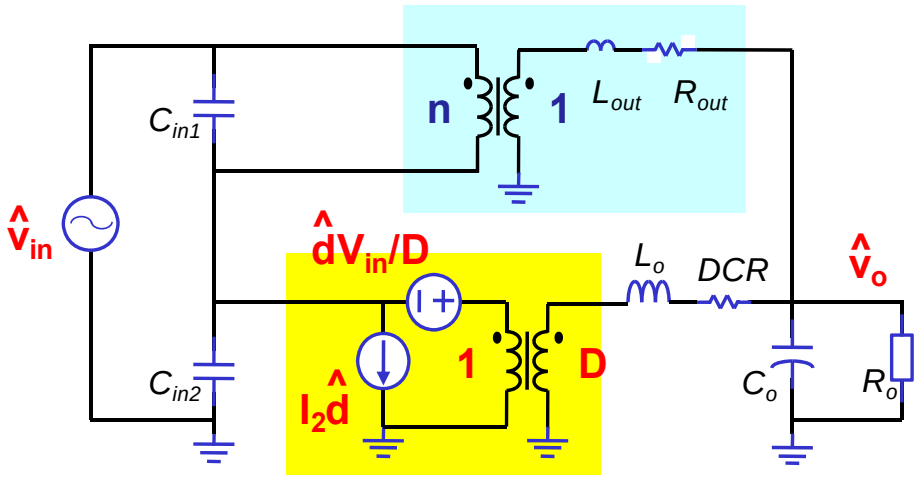



**Figure A-0-1 Small-Signal-Model of Sigma Converter**

**(a) Sigma converter two pairs of double-pole:**

$$\omega_{Lp} = \frac{1}{\sqrt{(n^2 C_{in} + C_o)\dfrac{L_o}{(1+nD)^2}}} \qquad Q_{Lp} = \frac{1}{\omega_{Lp}} \cdot \frac{1}{\dfrac{L_o}{R_o(1+nD)^2} + (n^2 C_{in} + C_o)(DCR + ESR // R_{out})}$$

$$\omega_{Hp} = \frac{1}{\sqrt{(n^2 C_{in} // C_o) L_{out}}} \qquad Q_{Hp} = \frac{1}{\omega_{Hp}} \cdot \frac{1}{\frac{L_{out}}{R_o} + (n^2 C_{in} // C_o)(R_{out} + ESR)}$$

$$\omega_{ESR} = \frac{1}{ESR \cdot C_o}$$

$$\Delta_{Lp} = (1 + \frac{s}{Q_{Lp} \cdot \omega_{Lp}} + \frac{s^2}{\omega_{Lp}^2}) \qquad \Delta_{Hp} = (1 + \frac{s}{Q_{Hp} \cdot \omega_{Hp}} + \frac{s^2}{\omega_{Hp}^2})$$

**(b) Duty cycle to output voltage transfer function:**

$$G_{vd}(s) = \frac{\hat{v}_o}{d} = \frac{V_{in}}{(1 + n \cdot D)^2} \cdot \frac{(1 + \frac{s}{\omega_{vd} \cdot Q_{vd}} + \frac{s^2}{\omega_{vd}^2})(1 + \frac{s}{\omega_{ESR}})}{\Delta_{Lp} \Delta_{Hp}}$$

$$\omega_{vd} = \frac{1}{\sqrt{(n^2 C_{in}) \cdot (\frac{L_{out}}{1 + nD})}} \qquad Q_{vd} = \frac{1}{\omega_{z1}} \cdot \frac{(1 + nD)^2 R_o}{n^2 C_{in} R_{out} R_o (1 + nD) + nD(L_o - nDL_{out})}$$

**(c) Duty cycle to DCX current and Buck inductor current transfer functions:**

$$G_{id1}(s) = \frac{\hat{i}_{o1}}{\hat{d}} = \frac{2nDV_{in}}{(1 + nD)^3 R_o} \cdot \frac{(1 + \frac{s}{\omega_{id1} Q_{id1}} + \frac{s^2}{\omega_{id1}^2})}{\Delta_{Lp} \Delta_{Hp}}$$

$$\omega_{id1} = \frac{1}{\sqrt{\frac{C_{in} L_o}{2 \cdot (1 + nD)}}} \qquad Q_{id1} = \frac{1}{\omega_{id1}} \cdot \frac{1}{\frac{L_o}{2R_o(1 + nD)} + \frac{R_o(DC_o - nC_{in})}{2D}}$$

$$G_{id2}(s) = \frac{\hat{i}_{o2}}{\hat{d}} = \frac{(1 - nD)V_{in}}{(1 + nD)^3 R_o} \cdot \frac{(1 + \frac{s}{\omega_{id2} Q_{id2}} + \frac{s^2}{\omega_{id2}^2})(1 + \frac{s}{\omega_{id2\_2}})}{\Delta_{Lp} \Delta_{Hp}}$$

$$\omega_{id2} = \frac{1}{\sqrt{(n^2 C_{in} // C_o) L_o}} \qquad Q_{id2} = \frac{1}{\omega_{id2}} \cdot \frac{1}{\frac{n^2 L_{out}}{R_o(1 + nD)} + \frac{R_o(DC_o - nC_{in})}{2D}}$$

$$\omega_{id2\_2} = \frac{1-nD}{R_o(n^2C_{in}+C_o)}$$

**(d) Load current to DCX current and Buck inductor current transfer functions:**

$$G_{ii1}(s) = \frac{nD}{1+nD}\cdot\frac{(1+\frac{s}{\omega_{ii1}Q_{ii1}}+\frac{s^2}{\omega_{ii1}^2})\cdot(1+\frac{s}{\omega_{ESR}})}{\Delta_{Lp}\cdot\Delta_{Hp}}$$

$$\omega_{ii1} = \frac{1}{\sqrt{nC_{in}\frac{L_o}{D(1+nD)}}} \qquad Q_{ii1} = \frac{1}{\omega_{ii1}}\cdot\frac{D(1+nD)}{nC_{in}DCR}$$

$$G_{ii2}(s) = \frac{1}{1+nD}\cdot\frac{(1+\frac{s}{\omega_{ii2}Q_{ii2}}+\frac{s^2}{\omega_{ii2}^2})\cdot(1+\frac{s}{\omega_{ESR}})}{\Delta_{Lp}\cdot\Delta_{Hp}}$$

$$\omega_{ii2} = \frac{1}{\sqrt{n^2C_{in}\frac{L_{out}}{(1+nD)}}} \qquad Q_{ii2} = \frac{1}{\omega_{ii2}}\cdot\frac{(1+nD)}{n^2C_{in}R_{out}}$$

**(e) Open-loop impedance seeing from DCX and from Buck inductor:**

$$Z_{o1}(s) = \frac{DCR+n^2D^2R_{out}}{nD(1+nD)}\cdot\frac{(1+\frac{s}{\omega_r})(1+\frac{s}{Q_0\omega_0}+\frac{s^2}{\omega_0^2})}{(1+\frac{s}{Q_1\omega_1}+\frac{s^2}{\omega_1^2})}$$

$$\omega_1 = \frac{1}{\sqrt{\frac{nC_{in}L_o}{D(1+nD)}}} \qquad Q_1 = \frac{1}{DCR}\sqrt{\frac{D(1+nD)L_o}{nC_{in}}}$$

$$Z_{o2}(s) = \frac{DCR+n^2D^2R_{out}}{1+nD}\cdot\frac{(1+\frac{s}{\omega_r})(1+\frac{s}{Q_0\omega_0}+\frac{s^2}{\omega_0^2})}{(1+\frac{s}{Q_2\omega_2}+\frac{s^2}{\omega_2^2})}$$

$$\omega_2 = \frac{1}{\sqrt{\frac{n^2 C_{in} L_{out}}{1+nD}}} \qquad Q_2 = \frac{1}{R_{out}} \sqrt{\frac{(1+nD)L_{out}}{n^2 C_{in}}}$$

$$\omega_0 = \frac{1}{\sqrt{\frac{n^2 C_{in} L_{out} L_o}{L_o + n^2 D^2 L_{out}}}} \qquad Q_0 = \frac{1}{\omega_0} \cdot \frac{(L_o + n^2 D^2 L_{out})^2}{n^2 C_{in}(n^2 D^2 L_{out}^2 DCR + R_{out} L_o^2)} \qquad \omega_r = \frac{DCR + n^2 D^2 R_{out}}{L_o + n^2 D^2 L_{out}}$$

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