DESIGN AND ANALYSIS OF A GRID CONNECTED PHOTOVOLTAIC GENERATION SYSTEM WITH ACTIVE FILTERING FUNCTION.

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Design and Analysis of a Grid Connected Photovoltaic Generation System with Active Filtering Function.

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Abstract

In recent years there has been a growing interest in moving away from large centralized power generation toward distributed energy resources. Solar energy generation presents several benefits for use as a distributed energy resource, especially as a peaking power source. One drawback of solar energy sources is the need for energy storage for the system to be utilized for a significant percentage of the day. One way of avoiding adding energy storage to a solar generation system while still maintaining high system utilization is to design the power conversion subsystem to also provide harmonic and reactive compensation. When the sun is unavailable for generation, the system hardware can still be utilized to correct for harmonic and reactive currents on the distribution system. This system's dual-purpose operation solves both the power generation need, and helps to improve the growing problem of harmonic and reactive pollution of the distribution system.

A control method is proposed for a system that provides approximately 1 kW of solar generation as well as up to 10 kVA of harmonic and reactive compensation simultaneously. The current control for the active was implemented with the synchronous reference frame method. The system and controller was designed and simulated. The harmonic and reactive compensation part of the system was built and tested experimentally. Due to the delay inherent in the control system from the sensors, calculation time, and power stage dynamics, the system was unable to correct for higher order harmonics. To allow the system to correct for all of the harmonics of concern, a hybrid passive - active approach was investigated by placing a set of inductors in series with the AC side of the load. A procedure was developed for properly sizing the inductors based on the harmonic residuals with the compensator in operation.

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Chapter 1. Introduction.

1.1. Motivation.

The motivation for this work was to design a digitally controlled, combination active filter and photovoltaic (PV) generation system. The system will eventually be used to test an experimental fiber optic based current sensor currently under development by Airak, Inc. This work focuses on a proposed control scheme for the dual function system and on the effects of delay on the control of an active filter. The basic system structure, shown as a block diagram in Figure 1.1 consisted of a 0.9 kW PV array with a nominal output voltage of 56 V, interfaced to the 360 V DC link by an isolated full bridge converter.

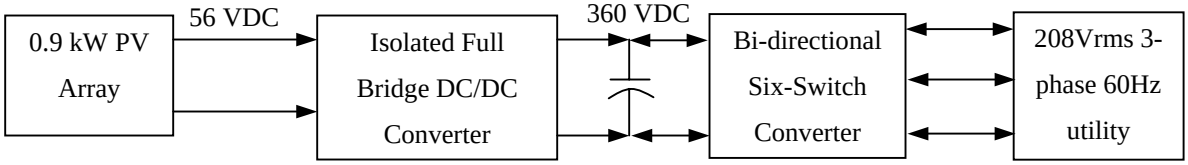


Figure 1.1. PV/Active Filter System Block Diagram.

The DC link was then connected to a bi-directional six-switch converter that would allow the energy generated by the PV array to be sent to the three phase utility grid at 208 V line to line. The bi-directional converter allows the system to provide active filtering capabilities, both during PV generation and when the PV energy is not available. The effective control of an active filter to correct for higher order harmonics requires that the bandwidth of the controller be as high as possible therefore the overall controller delay, which includes sensor delay, is minimized. Because of the importance of delay, this application was chosen as a suitable platform for demonstrating the suitability of the fiber optic sensors to control applications. This work involves the design and analysis of the control scheme for this system, the implementation of the active filter part of the system, and the limitations of active harmonic compensation. The PV portion of the system was not implemented due to a design problem discussed in chapter 3.

1.2. Harmonic Filtering and Reactive Compensation.

Within the last several decades, the vast improvements in semiconductor based devices has led to a number of new power electronic applications including high voltage DC systems,

computer power supplies, and adjustable speed motor drives [2]. While these systems improved existing applications and created new applications, their mode of operation also began to create problems with the power distribution system as their use proliferated. These systems employ diode and thyrister rectifiers on the front end, which draw non-linear currents from the sinusoidal distribution system. The non-linear currents drawn by the rectifiers consist of harmonics of the line frequency and reactive components that distort the line voltage of the distribution system due to the impedance of the distribution lines. In three-phase systems, the non-linear currents can lead to voltage unbalance and excessive currents in the neutral line, which is not designed to carry large currents [2]. As the number of non-linear systems that are attached to a distribution system increases, the effects of the harmonic and reactive "pollution" on the system becomes more evident [3]. The increased current in the neutral lines leads to overheating, insulation damage, and nuisance trips of protection equipment. The distortions caused by the non-linear currents manifest themselves as harmonics in the distribution system voltages. Harmonics in the system voltage can have detrimental effects on sensitive electronic equipment that is connected to the distribution system, such as telecommunications systems, control systems, and computer systems. The harmonic voltages and currents can also cause interference with communications systems through electrostatic and electromagnetic coupling from the transmission lines [3]. These problems have resulted in standards being developed by bodies such as the IEEE and IEC to limit the amount of harmonic current that can be injected into the distribution system based on the type of equipment. Some examples include the IEC International Standard 1000-3-2 that covers equipment limited to less than 16A per phase, and 1000-3-4 that covers equipment limited to between 16 and 75A per phase [4]. Many European governments have begun to adopt these standards as regulations that must be adhered to. Because of these regulations many of the new designs of power electronics systems that convert AC to DC have been designed with a power factor correction (PFC) stage on the front end to limit the amount of harmonic and reactive currents drawn by the equipment. The PFC method corrects the problem at the source, but another method of correcting the problem is to place a large-scale harmonic filter or reactive compensating system at the input to a facility that draws non-linear currents.

Large reactive loads such as the large number of motors at a manufacturing facility draw current that is out of phase with the source voltage. This leads to a higher apparent power, and

added current required to charge and discharge the reactive loads creates I^2R losses in the utility generation equipment and transmission lines. Most utilities charge penalties to commercial customers for drawing excessive reactive currents. To prevent the penalties, manufacturing companies often place reactive compensation equipment at the utility connection to the facility.

1.2.1. Traditional Methods of Harmonic Filtering and Reactive Compensation.

The prevalent method for removing harmonic currents produced by non-linear loads has been to use shunt passive filters placed near the loads. These passive filters are designed as multistage, tuned LC networks with each stage designed to attenuate an expected harmonic. There are several problems associated with this type of filter. One major problem is due to the low source impedance of utility systems; the filter impedance must be low compared to the source impedance at the harmonic frequency. This low impedance requirement for the filter can become size and cost prohibitive [5]. Another drawback to the tuned LC filter approach is that variability in source frequency and harmonic content results in degraded performance of the filter [5]. Finally, passive filters are not ideal and therefore attenuate at all frequencies, which can lead to reduced system voltage at the load.

Historically, the corrective methods for reducing reactive content at the fundamental frequency has been to switch in capacitor banks or use thyristor-controlled reactors at the grid connection to a facility [6]. There are also shortcomings associated with these methods of reactive compensation. First, the reactive components can only be switched in and out of the system in discrete quantities, which inherently limits the controllability of the compensation. A second problem with these methods has been seen in distribution systems under light load conditions, when the compensation networks can resonate with the source impedance and actually introduce harmonics into the system [6].

1.2.2. Power Electronics Based Active Filtering and Static Compensation.

Although advancements in semiconductor device technology have led to an increase of harmonic pollution in distribution systems, they have also provided potential solutions to the problem. With advanced semiconductor switches available that could switch large currents at high frequency and block high voltages, people began to propose switching networks combined with passive storage elements that could dynamically control the impedance seen by the system. The switching frequency of these “active filters” is kept high enough to provide good fidelity at

the lower harmonic frequencies [5] and to allow a wide bandwidth for control of the switching network. These active filters offer solutions to some of the shortcomings of passive compensation. Theoretically a shunt active filter can dynamically adjust the impedance it presents to the system to act as a short circuit to the system at the harmonic frequencies. This would allow the filter to shunt the harmonics and prevent them from feeding back into the utility grid. An active filter system could provide the same compensation capabilities as a much larger bank of tuned LC filters and potentially reduce overall system cost.

For displacement factor compensation the ability to dynamically adjust the impedance over a relatively continuous band gives the switching network approach a much better control over the amount of reactive impedance introduced into the system to cancel the reactive load present in the power system. This method of using a switching network and a passive storage element for fundamental frequency reactive compensation is called static compensation (STATCOM). Since the impedance of the compensator can be adjusted, control can be used to prevent the harmonic production associated with discrete quantity passive approaches.

Due to limitations on switching frequency of power semiconductors at high power levels, the control bandwidth of these active approaches is severely limited which prohibits their use for harmonic cancellation at high powers. Because of this limitation, high power active compensation is limited to displacement factor compensation. At lower power levels, both harmonic and displacement factor compensation can be combined into the same system; that is the approach taken in the system discussed in this work.

1.2.2.a. Active Filter and Static Compensation Topologies.

There are numerous types of active filter topologies found in literature. Although the system discussed in this work used a voltage source inverter (VSI) shunt active filter, several other topologies will be briefly covered in this section. Some of the basic classifications of active filter topologies include series vs. shunt, current source inverter (CSI) vs. voltage source inverter (VSI), and standalone vs. hybrid [6]. The active filter can be connected in shunt with the three phase lines as shown in Figure 1.2. The shunt filter is controlled to draw harmonic currents from the source to compensate for the harmonic currents drawn by nonlinear loads [6]

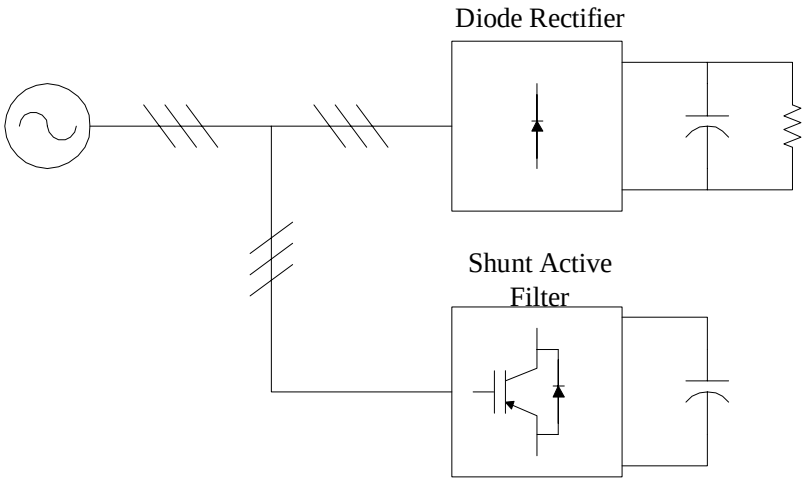


Figure 1.2. Shunt active filter connection.

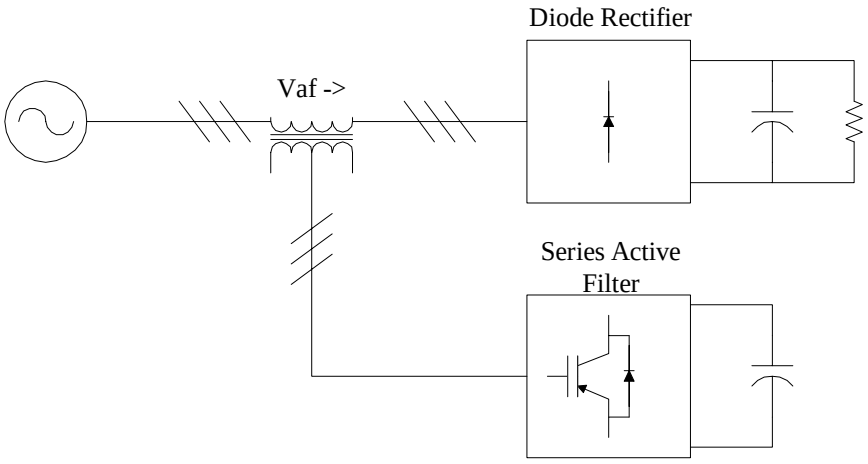


Figure 1.3. Series active filter connection.

The active filter can also be connected in series with the power lines as shown in Figure 1.3. The series active filter injects correcting voltages to the power lines through a matching transformer. Most literatures favor the shunt-connected topology for harmonic current compensation.

The power stage of the topology can be either a CSI or a VSI. Neither of these topologies require an active source to perform the filtering function, but instead use a passive storage element on the DC side of the switching network [5]. The CSI topology uses a switching network fed by a constant current source, so the storage element is an inductor placed in the DC side of the converter. The VSI uses a voltage fed switching network and the passive element is a capacitor across the DC bus. The use of the VSI is currently favored because of

improved efficiency and reduced initial costs [6], but this could change in the future with the increased availability of superconducting coils for use as the storage element in the CSI [7].

Active filters can be operated as standalone units or they can be designed to operate in conjunction with passive filters, called a hybrid topology. The hybrid approach can decrease the size of both the active and passive filters, and this approach is desired in very high power applications [4]. As discussed in chapters 5 and 6, this method may be necessary to meet the harmonic injection standards set in IEC 1000-3-4 for the higher order harmonics.

1.2.2.b. Active Filter Control Strategies.

The active filter relies on the control system to perform the required tasks. The controls of the systems are implemented in three stages: signal conditioning, compensation, and generation of the gating signals for the switching network [2]. The first stage involves the sensing and conditioning of voltages and currents in the system so that they can be used to complete the remainder of the control functions. The second stage is the development of the required compensating signals from the information obtained in the first stage of the controller. There are two basic classifications of the methods that have been developed to accomplish this task, frequency domain techniques and time domain techniques [2]. The final stage of the control scheme involves producing the proper gate signals to the switching network so that the compensating commands from stage two are injected into the power system. There are several methods of performing this task including linear based current or voltage control, sliding mode current control, hysteresis and fuzzy-based current control [2].

Generating the compensating signals can be the most complex part of the control system for an active filter. The literature has given many different methods of calculating the compensating currents or voltages for controlling active filters [2]. Most of the calculation methods are computationally intensive and are therefore very difficult or impossible to implement as an analog controller. With the recent revolutions in DSP speed increase and cost reduction it has become practical to implement these complex calculations in real time digital control systems. The frequency domain methods are especially computationally intensive because they rely on performing Fourier analysis in real time. Because of this increased calculation burden, the literature seems to favor the time domain calculation methods for the compensation calculation stage of the controller. The time required to calculate the

compensating components adds to the overall delay in the control system, decreasing the allowable bandwidth of the controller.

The current control method also has a large impact on the overall bandwidth of the controller. A comparison of some of the methods including the linear rotating reference frame current controller, digital deadbeat current controller, and hysteresis current controller was done in [37]. The results from the comparison showed that the best results were achieved with the hysteresis controller because the delay inherent in the controller was the least. A large number of the control methods proposed for active filters utilize the hysteresis method for the current control, but this method does have some drawbacks. When hysteresis based current control is used, the switching frequency of the converter is not fixed but varies stochastically during the converter operation. This varying switching frequency can lead to difficulty when sizing the output inductors of the active filter and the generation of unwanted resonance on the utility grid.

There are a multitude of different methods that have been proposed for the control of an active filter. Some of the methods combine and or simplify the three steps listed before that are necessary for a control scheme. One example is the Unified Constant Frequency Integration Control method discussed in [36]. This method has a fast response and a constant frequency so the problems with hysteresis are avoided.

1.3. Photovoltaic Power Generation

Along with wind and hydroelectric, photovoltaic (PV) generation or the direct conversion of sunlight into electrical energy is one of the cleanest forms of energy conversion available. When the energy crisis in the seventies was going on, PV generation became very popular as a prospective replacement for fossil fuel electric generation. But, there are several reasons that PV generation has not become a major source of energy. First, the development of low cost, efficient solar cells has been slow. The present large-scale manufactured solar cells are approximately 7 to 17% efficient [9] and cost in the neighborhood of $5000.00 per kW for low volume purchases. This cost does not include the interface equipment that is necessary due to the DC output of the cells. These costs cannot presently compete with large-scale fossil fuel based generation in cost per kW-hr. A second reason for the low use of PV is that power generation in the U. S. has been historically performed in a bulk manner at large centrally located generation plants in the 100 to 1000MW range. Equation (1.1.1) demonstrates one reason why

PV generation is impractical for bulk generation. The energy from the sun at peak insolation is around 1kW/m^2.

$$PV\_array\_area = \frac{power}{power/area \cdot \eta_{pv} \cdot \eta_{Inv}} = \frac{100MW}{1kW/m^2 \cdot 0.17 \cdot 0.96} = 0.61km^2 \qquad (1.1.1)$$

The second efficiency number is due to the losses inherent in the power conversion equipment required to interface the solar cells to the utility grid. This calculation is at peak generation in the middle of a sunny day at the location. To be able to produce 100MW continuously, the facility would have to have a large storage capability and a significantly larger footprint. Equation (1.1.2) shows a simplified estimate of the footprint based on the assumption that the generation capability increases linearly from sunrise to the peak generating point and then decreases linearly to zero at sunset.

$$PV\_array\_area = \frac{\frac{2 \cdot energy\_required}{generation\_time}}{power/area \cdot \eta_{pv} \cdot \eta_{Inv}} = \frac{\frac{2 \cdot 8.64 \cdot 10^{12} J}{39600\sec}}{1kW/m^2 \cdot 0.17 \cdot 0.96} = 2.67km^2 \qquad (1.1.2)$$

The energy required is based on generating 100MW for 24 hrs and the generation time is based on 11 hours of sunlight. Besides requiring large footprints for the solar panels, there are presently numerous technical reasons preventing the feasibility of a PV generation system of this size.

1.3.1. A Move Toward Distributed Energy Generation.

With the present growth rate of energy consumption the world's energy consumption is doubling every 10 years, which will lead to the depletion of the fossil fuel supply in a few hundred years [8]. This will lead to the necessity to begin relying on other forms of energy in the near future. Recently there has been a growing interest in expanding electric generating capacities through the use of distributed energy generation (DEG). DEG consists of placing small (up to tens of megawatts) generation assets around communities and industrial facilities at the distribution level. These generation assets include natural gas micro-turbines, fuel cells, wind, and solar energy sources. DEG offers many advantages to the generation companies and customers alike. The generation company will benefit by not having to sink large sums of

capital into a generation facility that will not produce any return on investment for several years. Another advantage to the utility company is the reduced load on the transmission & distribution (T&D) network. For remote communities that are growing, the long T&D runs are extremely costly to upgrade to a higher capacity [11]. By moving the energy source closer to the end user, losses in T&D lines are reduced [11]. All of the benefits above can be passed on to the end user in the form of lower utility costs. Another benefit to the user would be improved power quality and reliability [11].

PV generation provides a good solution for DEG. PV systems provide the highest power level in the middle of the day, which coincides with the peak power requirements on the utility grid, especially during the summer [12]. Even though PV systems are intermittent resources due to their reliance on the sun shining, the times when the energy available from the sun is at its highest corresponds to the highest demands on the utility grid. This correlation makes PV generation highly suitable as a peaking source.

1.3.2. Issues with Connecting PV Arrays to the Grid.

The major problem that must be overcome when connecting PV arrays to the utility grid is the power conditioning system (PCS) that is required to convert the DC output voltage to 50 or 60Hz AC voltage at the proper level to interface to the utility at the specified distribution level. Converting from DC to AC can be accomplished with line frequency converters or high frequency converters. With the present technology the high frequency converter is the preferred solution because the line frequency converters operate with a poor lagging power factor and introduce harmonic currents on the grid [13]. The high frequency converters can synthesize a good sinusoidal voltage waveform. Also, the control of a high frequency converter allows the system to be operated at a desired power factor. The utility grid tends to have a low voltage at the ends of feeders due to voltage drop from transmitting reactive power. By placing PV generation systems with power factor control close to the end user, the voltage can be brought back to proper levels at the ends of the feeders [13].

The converter control must also have the ability to recognize a utility fault or outage and remove itself from the system. If the converter were to continue to operate as an island generator during an outage, there is a risk that the reclosing of utility breakers for fault clearing would

connect to the unsynchronized system [13]. The converter must be able to protect itself from the large voltage surges that can occur on the utility grid due to lightning strikes.

One common practice when connecting a PV system to the grid is to include a DC/DC converter between the PV array and the input to the DC to AC converter. The DC/DC converter acts as a buffer and allows more freedom in selecting the nominal output voltage of the PV array. There is a risk, when creating a high DC voltage by series connecting a large number of PV cells, of one cell shorting and damaging other cells in the array. Using the DC/DC converter avoids this problem by allowing a low voltage PV array to be interfaced to a high voltage AC system.

1.3.2.a. Maximum Power Point Tracking.

PV cells have a non-linear V-I characteristic that is dependent on solar intensity and cell temperature. This non-linear characteristic makes it difficult to control the output of the PV cells so that the maximum available power is being supplied to the grid [14]. The practice of maximizing the power output of the PV array is known as maximum power point tracking (MPPT). The literature describes many different methods for accomplishing MPPT in a PV system. Some examples of MPPT methods include integration, neural networks, perturbation and observation, and online derivative of power vs. voltage [15].

1.3.2.b. System Utilization.

With a standalone PV system there is usually an energy storage system, normally batteries that are charged during PV operation and provide energy to the loads during hours of darkness or foul weather. This allows the system to provide power at all times if the storage capacity is high enough and the geographic location provides sufficient energy from the sun. With a grid connected PV system, the only reason to have storage capability is to allow the system to act as an uninterruptible power supply to the loads when there is a utility outage. Without storage capability in the system, the excess energy that is produced during daylight hours is simply sold back to the utility. When the sun is not shining, the PV system without storage would sit idle; therefore the overall system utilization would be limited to daylight hours. A common practice to increase system utilization is to design the DC to AC converter control to allow bi-directional power flow and use the converter to provide reactive and harmonic compensation to the grid. This function can continue when the PV generation capability is no longer available, therefore increasing system utilization.

1.4. Conclusion.

The system discussed in section 1.1 was designed for this work and a control scheme was proposed that would control the overall system. The control method for the active filter function was chosen to be a variant of a synchronous reference frame current controller with space vector modulation of the converter switches. Although this method did not provide the best bandwidth for correcting for the higher order harmonics, it did fit well with the proposed control scheme for combining the functions of PV generation and active filtering. The remaining chapters discuss the hardware design and implementation, the control design and simulation, the digital implementation of the control scheme, the experimental results from the active filter testing, and conclusions about the performance and limitations of the control method. Due to the limitations of active filters at correcting for higher order harmonics, there have been several hybrid passive – active filtering methods proposed in the literature. In order to correct for higher order harmonics, inductors were added in series with the AC side of the non-linear load in this system. A procedure has been developed for properly sizing the inductors for the hybrid approach.

Chapter 2. Hardware Design and Implementation.

2.1. System Overview.

Chapter 1 gave a basic overview of the system developed for this work. This chapter describes the hardware used to implement the system. The connection of the system to the utility grid is shown in Figure 2.1 below. The variables assigned to the currents in Figure 2.1 along

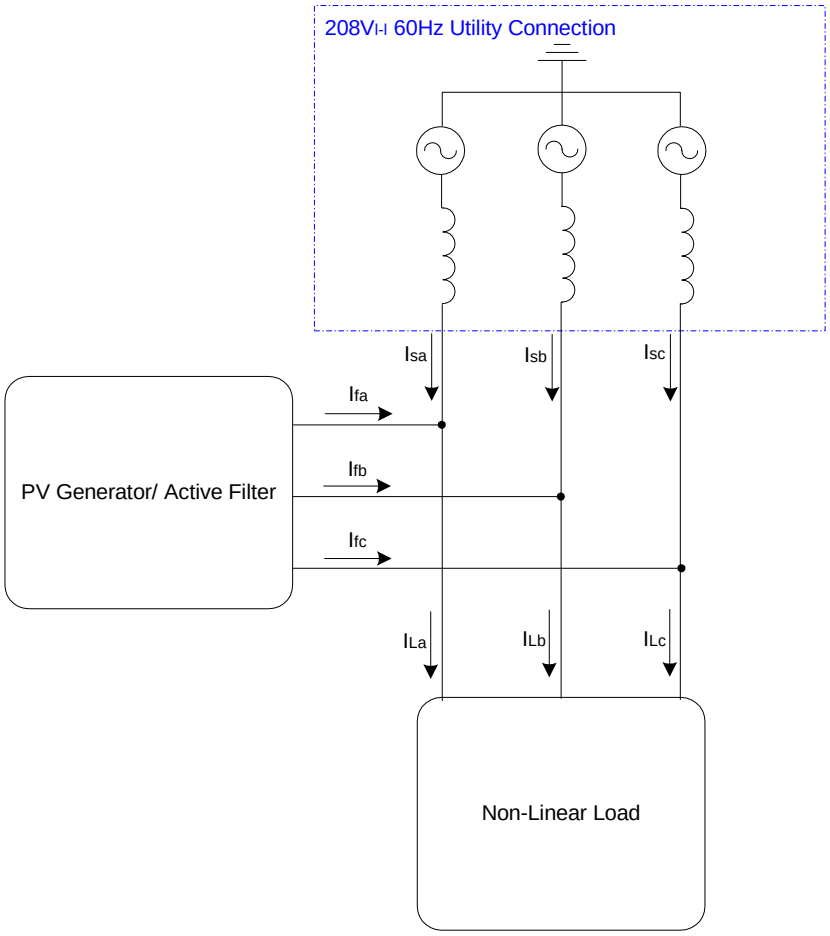


Figure 2.1. Block diagram of system connection to the utility and load.

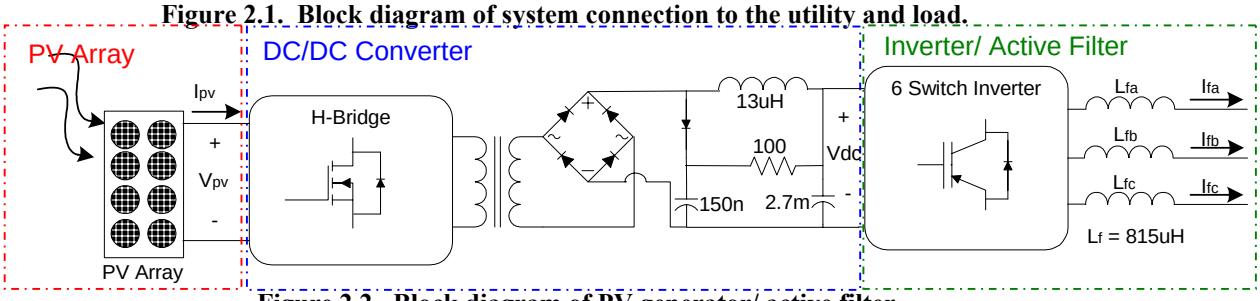


Figure 2.2. Block diagram of PV generator/ active filter.

with the reference directions shown, are used throughout the remainder of this document. Table 2.1 describes the currents shown in Figure 2.1. Figure 2.2 shows a more detailed diagram of the PV generator/ active filter section from Figure 2.1. Again, the voltage and current variables assigned in the figure are used throughout the remaining chapters. Each of the sections outlined in Figure 2.1 are described in detail in the next three sections of this chapter. Section 2.5 describes the hardware used to implement the digital controller for the system.

Table 2.1. System current variables.

Variable	Description
I_{sa}, I_{sb}, I_{sc}	The currents flowing from the source (or utility).
I_{fa}, I_{fb}, I_{fc}	The currents flowing out of the PV/active filter sytem.
I_{La}, I_{Lb}, I_{Lc}	The currents flowing into the load.

2.2. PV array.

The 0.9 kW PV array that was selected for the system consisted of three parallel connections of three Siemens SR100 panels connected in series as shown in Figure 2.3.

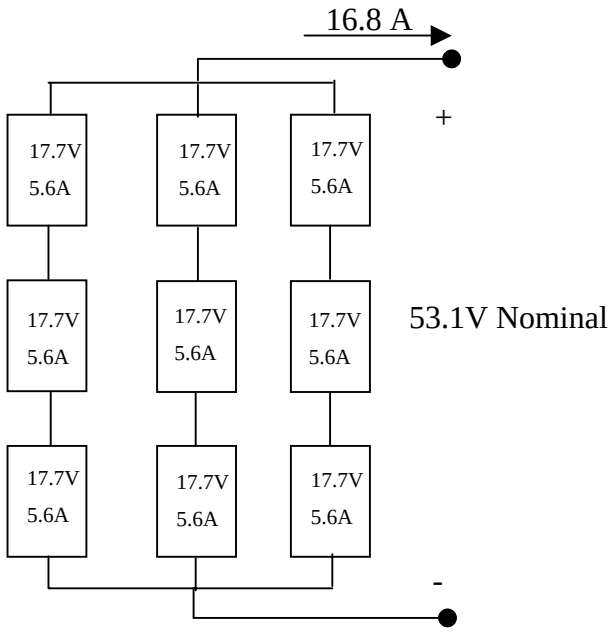


Figure 2.3. PV array connections.

Each of the SR100 solar panels have a maximum power rating of 100W, which occurs at a rated voltage of 17.7V and a rated current of 5.6A. The panels have an open circuit voltage of 22V and a short circuit current of 6.3A. A picture of one of the panels and the V-I curve for each panel is shown in Figure 2.4. As mentioned in section 1.3.3.a the V-I curves have a non-linear shape. It can be seen in the figure below that the curve tends to slide down as the solar intensity decreases, and the curve slides to the left as cell surface temperature increases. In the system

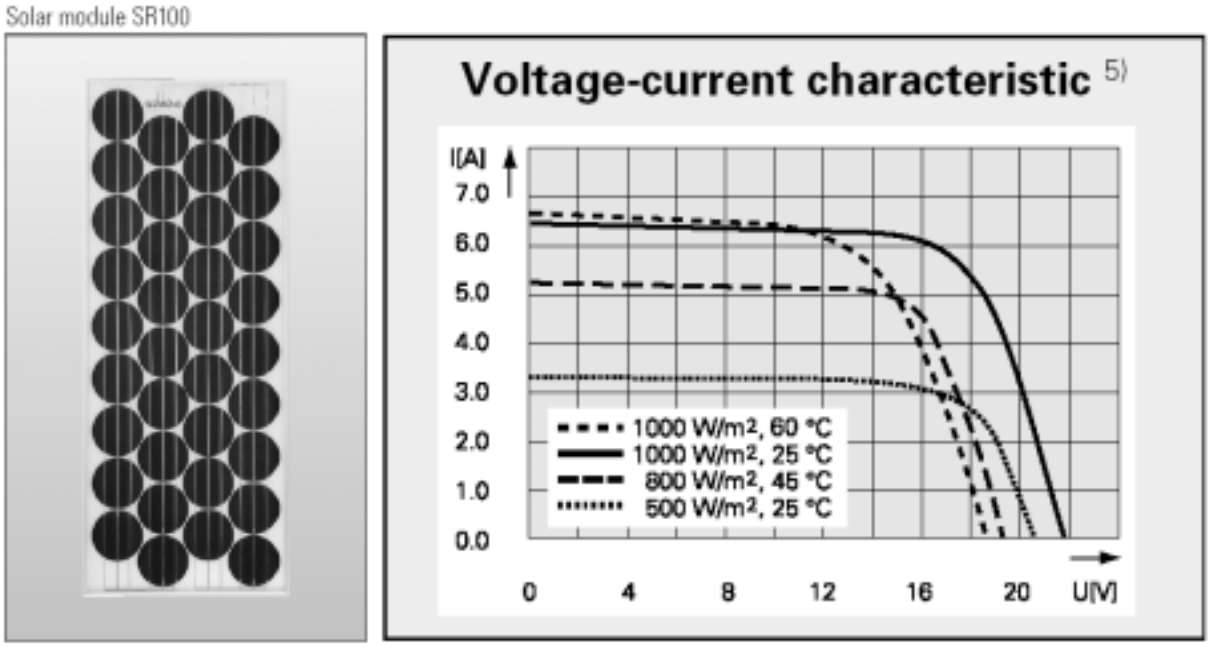


Figure 2.4. Siemens 100W PV panel and V-I curves.

design, the PV array voltage and output current are sensed by LEM voltage and hall current sensors, respectively. The voltage and current variables from the sensors are fed into the digital controller through A/D channels to be used for the MPPT control scheme.

2.3. DC-to-DC Converter.

The DC-to-DC converter power stage selected for the system was originally designed for a project that required the 48V DC nominal output of a fuel cell to be boosted up to a 400V DC link for an inverter. The topology is an isolated full bridge implemented with 100V, 75A MOSFETs (Advanced Power Technologies APT10M19BVR). Figure 2.1 shows the schematic of the converter. The original design was for two 5kW converters operated in parallel to provide 10kW for the inverter stage. In this application the converter only needs to provide 0.9kW, so

only one side of the converter is used. The board designed for the fuel cell application is shown in Figure 2.6 with only one side populated for this application. The capacitor across the

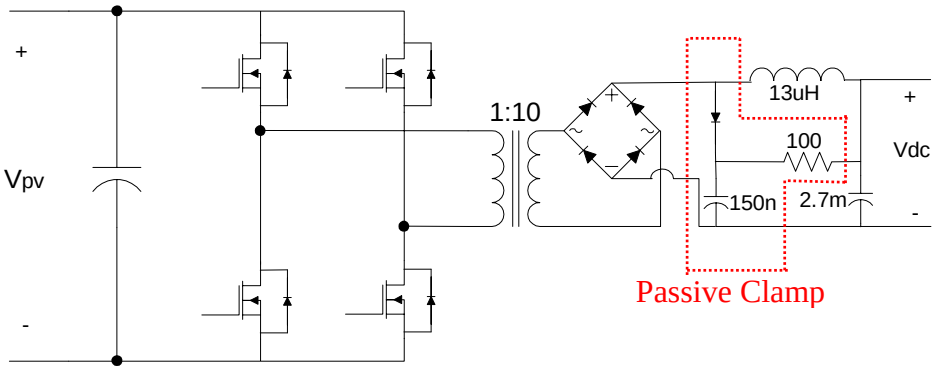


Figure 2.5. DC/DC converter schematic.

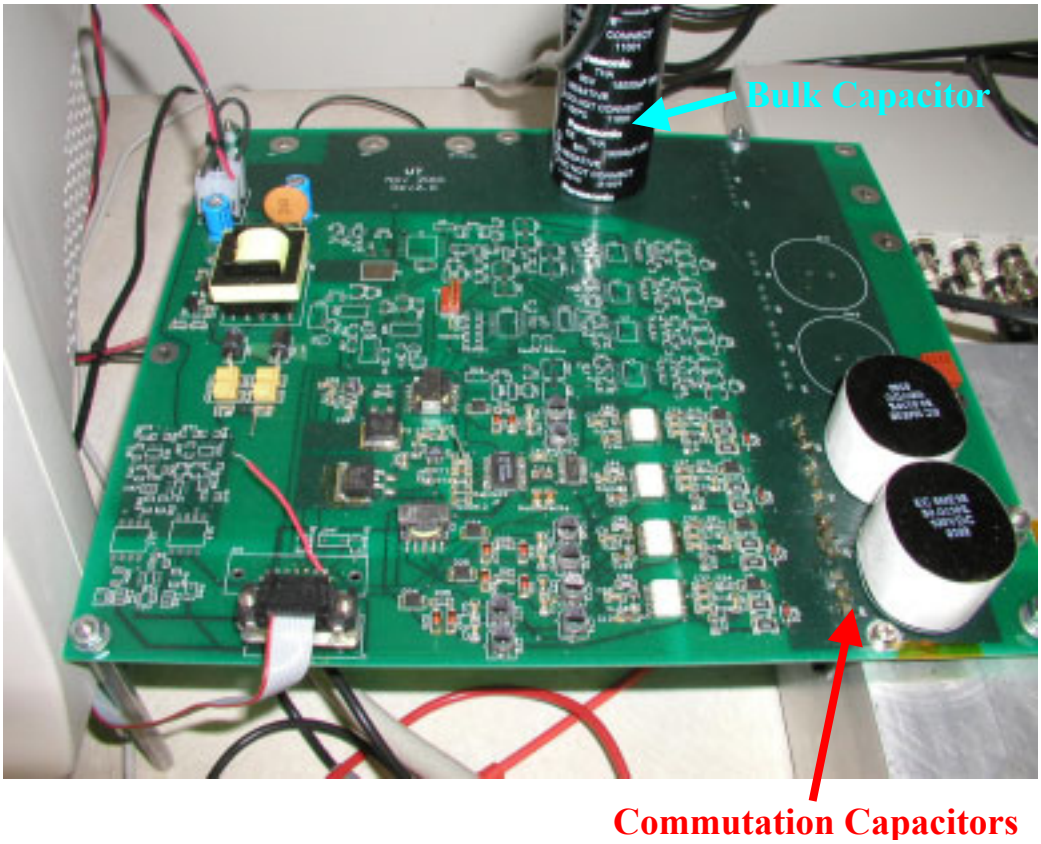


Figure 2.6. DC/DC converter power stage.

input of the converter shown in the schematic is actually three capacitors in the circuit as can be seen in Figure 2.6. The bulk capacitor helps to maintain the dc bus during transients and the commutation capacitors are placed as close to the half bridges as possible to minimize

inductance, so they can prevent the output capacitance of the switches from ringing with the bus inductance during switch commutation.

A TI UC3895 phase shift modulation control chip performs the full bridge switch modulation. The phase shift modulation scheme can provide zero voltage switching by utilizing the energy in the transformer leakage inductance and the output filter inductor [16]. The actual control of the duty cycle of the converter is through a PWM channel from the controller that is passed through a low pass filter to act as a D/A channel and connected to the controller chip.

2.3.1. Gate Drive.

The gate drivers used for the MOSFETs in this converter are the same ones used in the inverter stage so they will only be described here. Figure 2.7 shows a schematic of the gate drive.

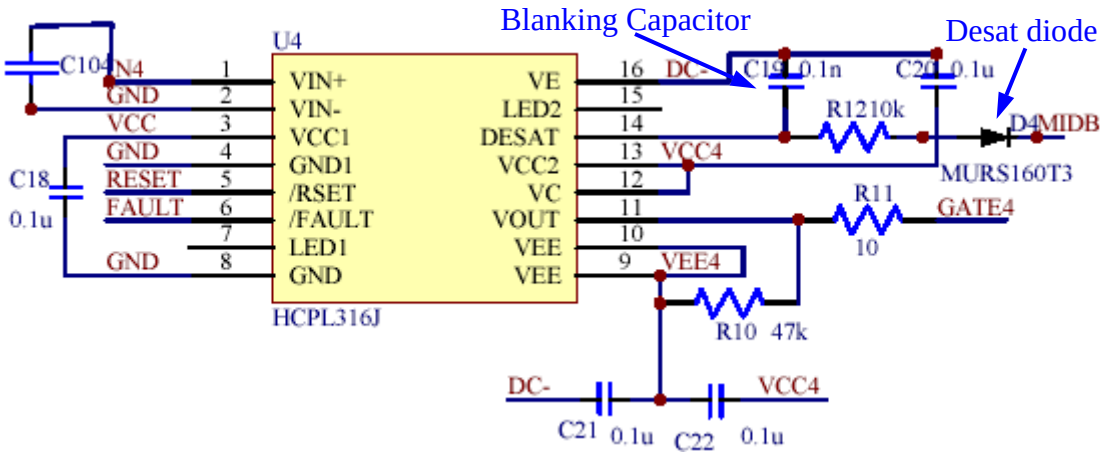


Figure 2.7. Gate drive schematic.

An Agilent HCPL316J optically isolated gate drive chip was used to design the gate drive. The optical isolation of the gate drive IC provides isolation for the devices that are tied to the upper rail and allows all of the devices to be turned off with a negative voltage. In this design the gates of the devices are turned on with +15V and turned off with –5V, which are provided by the flyback power supply shown in Figure 2.8. The power for the gate drive power supply as well as the control circuitry is derived from the input voltage using the auxiliary power supply shown in Figure 2.9. The auxiliary power supply is a flyback that was designed using a Power Integrations Top Switch integrated control and MOSFET IC. The auxiliary power supply also supplies the +5V that is required to run the logic in the gate drive IC. Protection against

overcurrent conditions in each device is provided by the gate drive IC with desaturation protection. The gate drive IC has a constant current source that forces a voltage drop across a resistor and diode that are connected to the collector or drain of the switching device. When the device turns on, the current source charges the blanking capacitor to the voltage across the device plus the voltage drop of the diode and the voltage drop across the resistor. The blanking capacitor charging time gives the device enough time to turn on completely. If the total voltage at the desat pin is above 7V the device is turned off and the gate drive IC feeds back a fault signal to the controller. The gate drive IC will also go into a fault condition if the gate drive power supply voltage drops below 11V. When a fault occurs, the gate drive IC must be reset to run again.

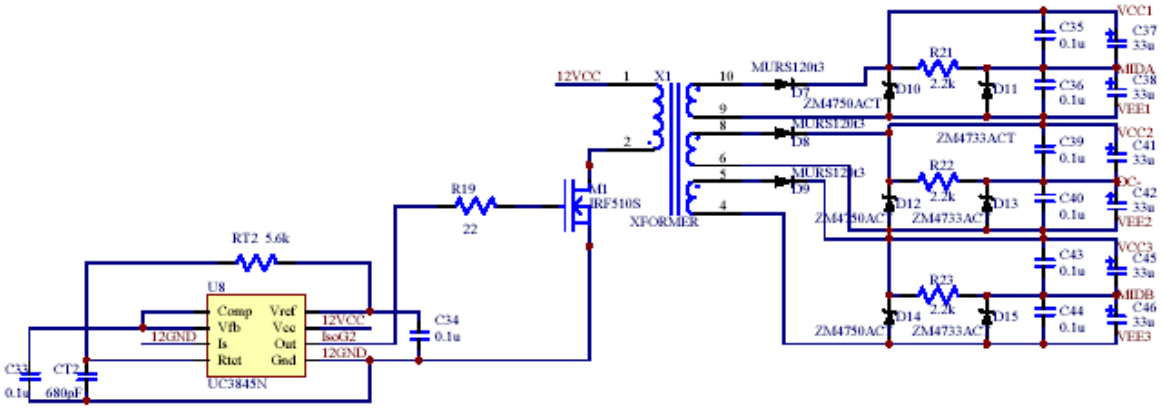


Figure 2.8. Gate drive power supply.

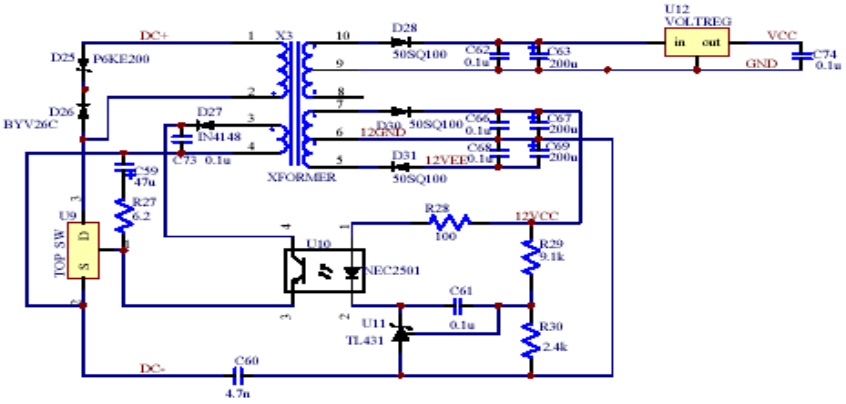


Figure 2.9. Auxiliary power supply.

2.3.2. DC/DC Converter Transformer.

The output of the DC/DC converter must be above 350V so the transformer design boosts the voltage up to this level. The transformer was designed to use an ETD-49 core and has 4 primary windings and 40 secondary windings, giving a turns ratio of 1:10.

2.3.3. Output filter.

The output filter design was based on providing enough capacitance to act as energy storage for the active filter function of the system. The calculation for the size of the DC link capacitor for the active filter is based on controlling the voltage change of the DC link under worst case operating conditions. It is assumed that when the active filter is providing compensation at the fundamental line frequency for displacement power factor (DPF) correction, then the capacitor is charged and discharged twice per line cycle and that the charge and discharge times are even. Based on a charge/discharge balance, the following equation is used to determine the capacitance value for the DC link [17].

$$C_d = \frac{I_{f-rms}\Delta t}{\Delta V_d} = \frac{I_{f-rms}}{4\,f\Delta V_d} = \frac{25}{4(60)(40)} = 2.6mF \qquad (2.1)$$

The change in DC link voltage is high at 40V, but it is assumed that the control loop for the DC link voltage will help to hold a tighter voltage band. A 2.7mF, 450V aluminum electrolytic capacitor was chosen for the DC link of the system.

Based on the proposed controller design that is detailed in Chapter 3, it was desired to have a wide bandwidth for the DC/DC converter output voltage control loop. To help ensure a wide bandwidth was possible for the converter, the resonant point of the output filter was chosen to be 850Hz. This resonant point for the filter resulted in an inductance value of 13uH. The drawback of using this output filter design is that the DC/DC converter will always operate in the discontinuous conduction mode (DCM). By operating in DCM the major benefit of the phase shifted full bridge topology, zero voltage switching, is lost. This trade off was made to allow for the proper operation of the proposed control scheme.

2.3.4. Passive Clamp.

The outlined part in Figure 2.5 is a passive clamp that controls the voltage overshoot that occurs due to a resonance between the capacitance of the rectifier diodes and the leakage inductance of the transformer. The overshoot occurs when the diodes turn off, and requires that the diode voltage rating be increased. When the rectifier diodes turn off the voltage begins to rise and is clamped by the diode to prevent excessive voltages. The size of the clamp capacitor determines how high the voltage will go. After the voltage begins to decrease the clamp capacitor discharges to the nominal DC link voltage through the clamp resistor. About 60% of the clamp energy is dissipated in the resistor and the rest is delivered to the load [18].

2.4. Inverter/ Active Filter.

The power stage for the inverter/active filter part of the system is a 6-switch topology that is rated at 10kVA. Originally designed for another project, the power stage is presently on the fourth revision, and is a well-tested design. As discussed in section 2.3.1, the same gate drive circuit is used in this power stage as the DC/DC converter. The auxiliary power supply is also the same as in the DC/DC converter. International Rectifier IRG4PSC71UD 600V, 60A IGBTs with integrated anti-parallel diodes are used as the power devices in the inverter/active filter power stage. Figure 2.10 shows a schematic representation of the power stage.

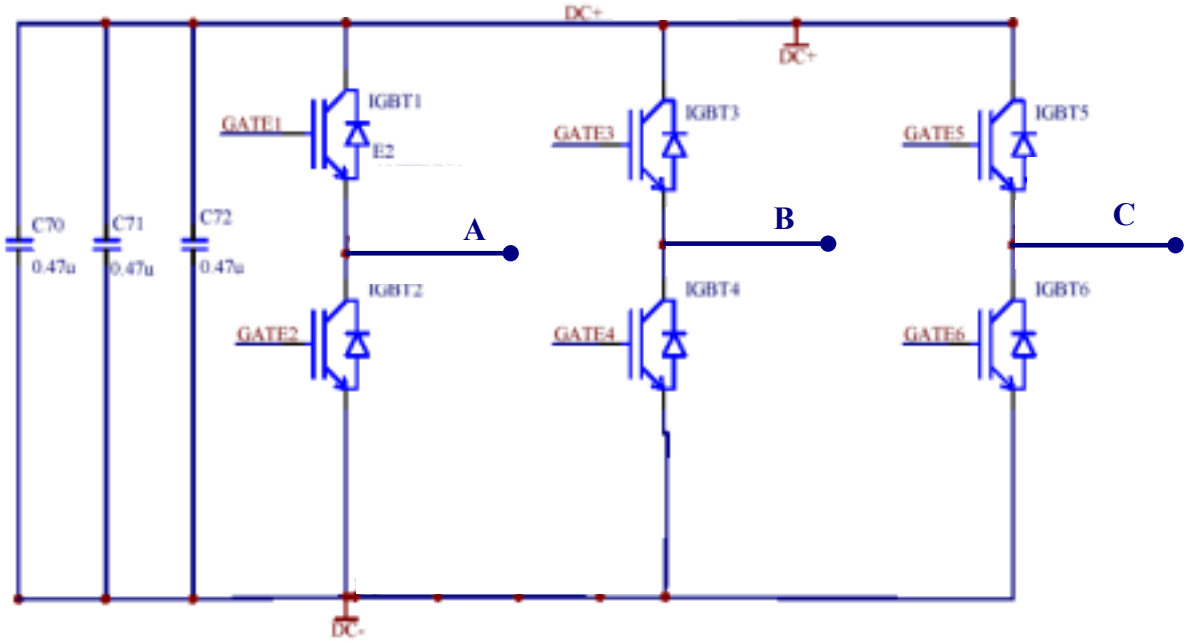


Figure 2.10. Inverter power stage schematic.

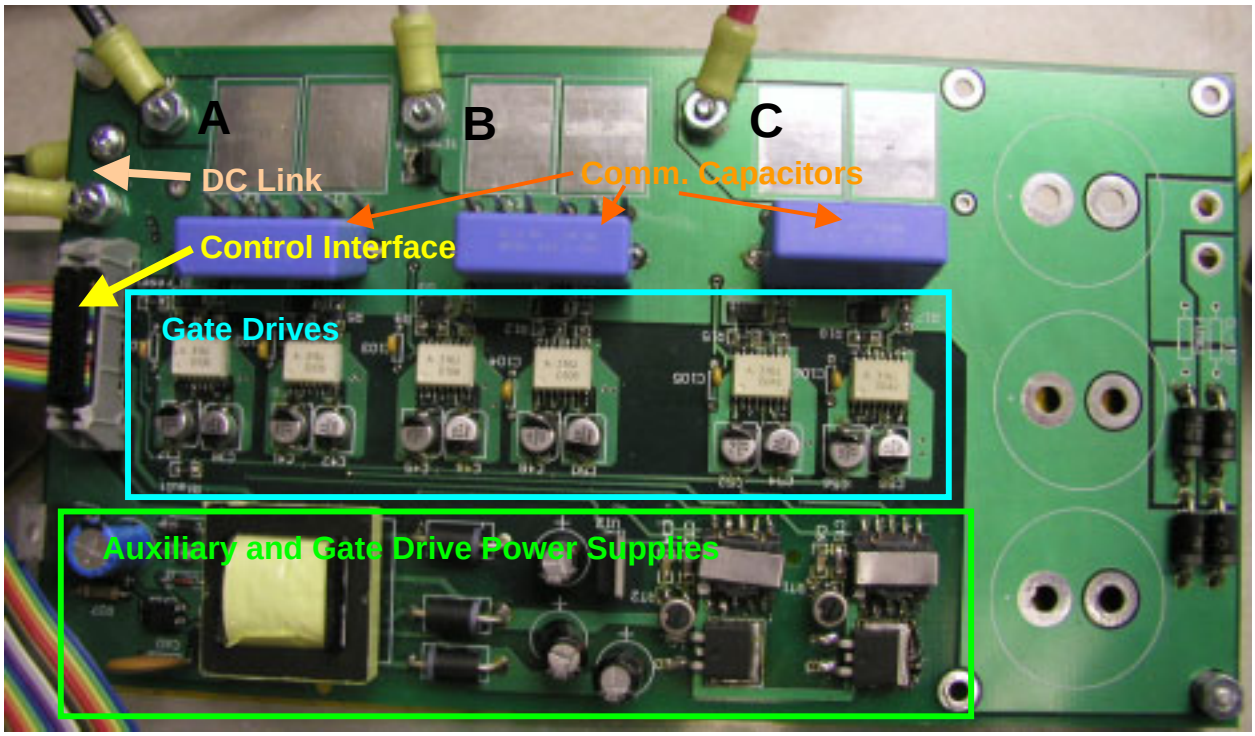


Figure 2.11. Inverter/active filter power stage.

A picture of the upper side of the power stage is shown in Figure 2.11. The PC board has components on both sides and the DC link bus and output buses are integrated into the PC board. The three capacitors shown across the DC link in the schematic are the commutation capacitors that are placed as close to the complementary pairs of power devices as possible to minimize voltage overshoot and ringing on device turn off.

2.4.1. Output Filter Inductors.

Included as part of the inverter/active filter power stage are filter inductors that are placed in series with the three phase outputs of the power stage. The purpose of the inductors is to filter the switching components out of the output currents of the inverter/active filter. The inductor size was designed to limit the current ripple to 2.5A at a switching frequency of 32kHz, a DC link of 360V and a line to line output voltage of 294Vpk [17].

$$L_f = \frac{Vdc - Vab_{pk}}{f_s \cdot \Delta i} = \frac{360 - 294}{32k \cdot 2.5} = 825\text{uH} \qquad (2.2)$$

To size the inductors, first a calculation was done based on the real power that could be flowing from the PV array to the grid, then an assumption was made that the 5th harmonic would be the worst case current for the active filter. Based on a 10kW non-linear load it was assumed that 5kVA of reactive power could be circulated through the active filter [17]. It was then assumed that 60% of the 5kVA would be at the 5th harmonic and the inductors were designed based on that current. Two Magnetics ® MPP 58866-A2 125μ cores are used in each inductor and the windings consist of 54 turns of 3 strands of 17 gauge wire. The measured inductance of the completed inductors is 815uH. Figure 2.12 shows the power stage connected to the output filter inductors.

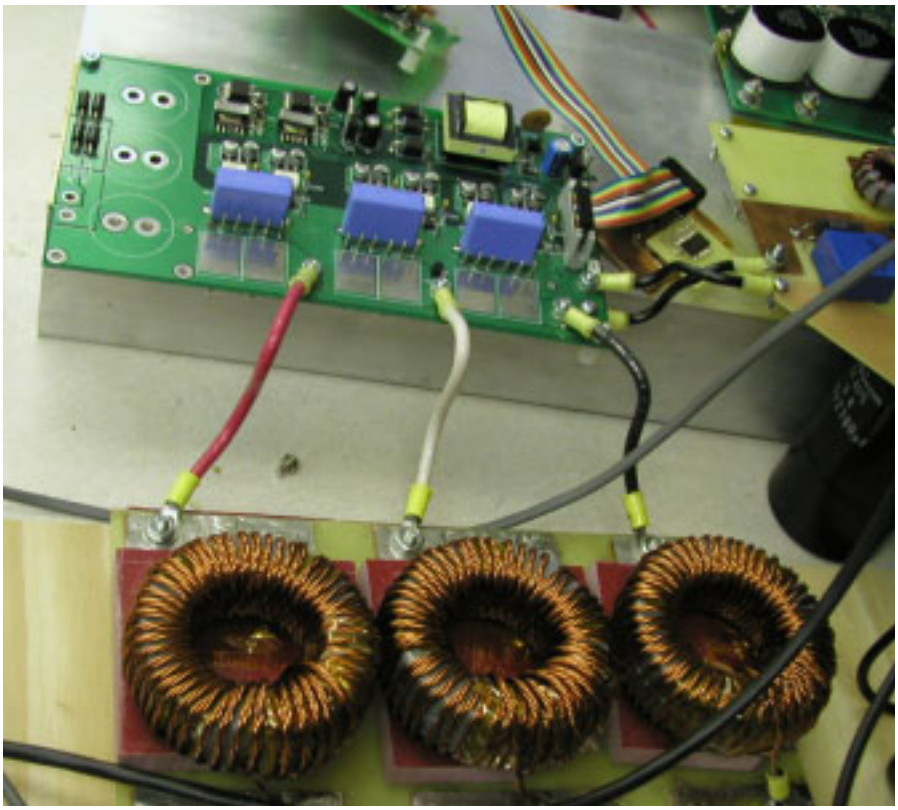


Figure 2.12. Power stage with output filter inductors.

2.5. Controller Hardware.

The controller for the system is based on a high performance Texas Instruments 32 bit floating point DSP. The particular DSP family chosen for the project was designed for

communications applications, and therefore the peripherals included with the DSP do not meet the requirements for a typical power electronics control system. A third party, configurable daughter card was chosen to interface the DSP to the system.

2.5.1. DSP board.

Texas Instrument's TMS320C6701 DSP core was chosen for the controller for this system to ensure that a sufficient amount of processing power was available to not only control the system, but to also provide signal processing for the fiber optic current sensors outputs. The specifications of the DSP core are given below:

DSP core: TMS320C6701

- 32 Bit floating point processor
- 133 MHz maximum clock speed
- 32, 32 bit registers
- 8 independent function units (6 ALU's and 2 MAC's)
- Up to 8 simultaneous 32 bit fixed point instructions per cycle
- Up to 6 simultaneous 32 bit floating point operations per cycle
- Glue-less interface to synchronous and asynchronous memory
- Host port interface
- 2 multi-channel buffered serial ports
- 4 DMA channels

To shorten development time, the evaluation module (EVM) for the TMS320C6XXX family was chosen as the controller board for the system. Texas Instruments builds the EVM and it includes the following features:

EVM module:

- 1 bank of 64K x 32bit 133 MHz SBSRAM memory
- 2 banks of 1M x 32bit 100 MHz SDRAM memory
- Connection to the memory bus via daughter card connector (allows up to 3M more memory)

- Connection to the peripheral interface bus via daughter card connector

The daughter card connectors on the EVM allow third party expansion boards to be easily plugged into the system.

2.5.2. Control Peripheral Daughter Card

A Signalware, Inc. AED-106 daughter card was chosen to provide the necessary peripherals for the control system. Figure 2.13 gives a diagram of the EVM board and the AED-106 and their connections to each other.

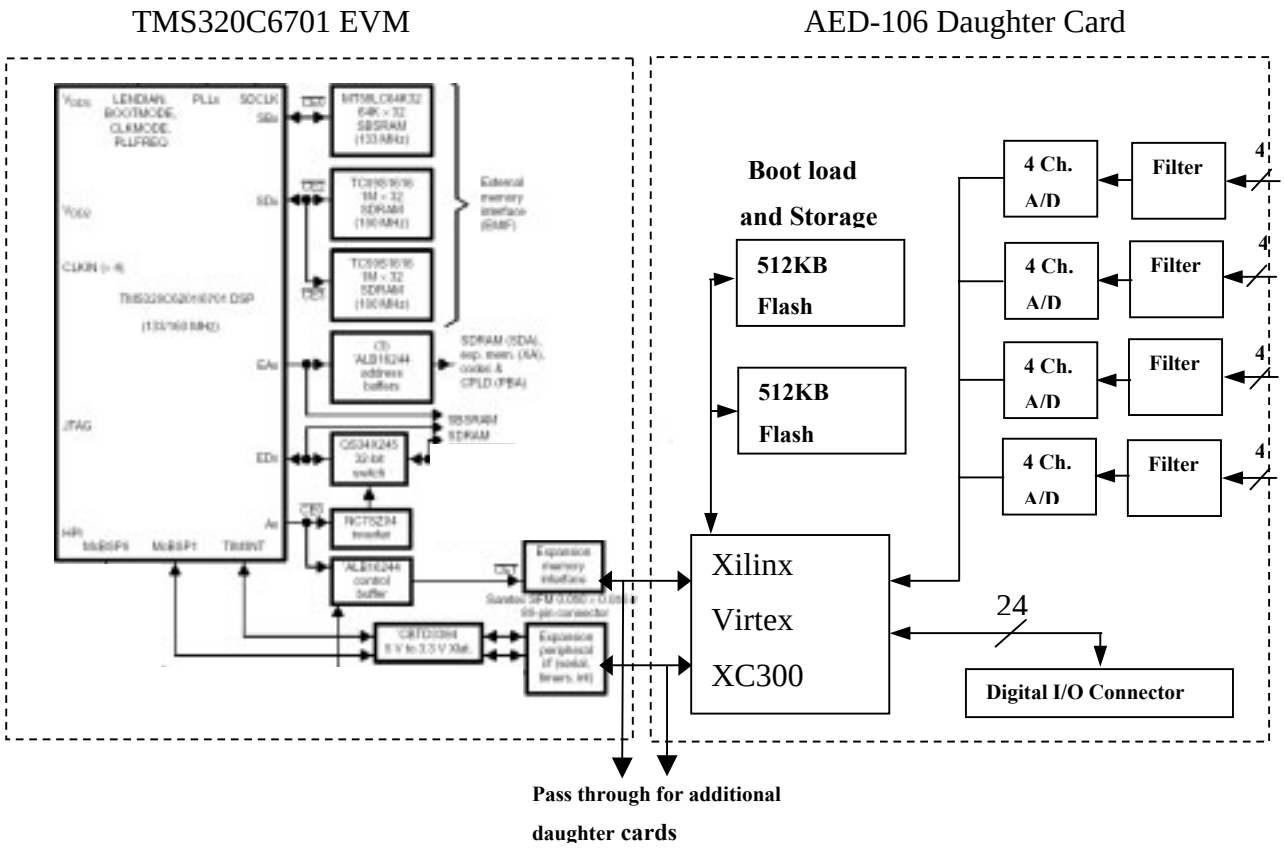


Figure 2.13. Block diagram of EVM and AED-106 boards.

The AED-106 board has the following features:

Daughter card: Signalware Corporation, AED-106

- Xilinx Virtex XCV300 series FPGA for interfacing the memory and peripheral bus from the DSP to peripherals for control applications.
- 2 banks of 512k x 8bit Flash memory for boot loading and program storage.
- 4 THS1206 4 input 12 bit A/D converters, allowing 6 MSPS each.
- High speed (70MHz) amplifiers at the input of each A/D channel for use in a anti-aliasing filter.
- 24 configurable digital I/O lines.

The FPGA on the daughter card allows good flexibility in the controller design. All of the 16 A/D converters are buffered in the FPGA to allow for proper synchronization between the sampling and the transfer to the DSP memory. The FPGA also provides a very flexible digital I/O configuration. In this design, as discussed in Chapter 4, several of the digital I/O pins on the daughter card were used as the PWM channels for the power device gate signals to the inverter. Another digital I/O pin was set up as a PWM channel and passed through an external low pass filter to provide a D/A converter for the control signal to the DC/DC converter control chip. All of the fault signals from the inverter gate drives are ored together to and fed back to one of the digital I/O pins. Another pin is used for the same purpose for the DC/DC converter. Two digital I/O pins are used to provide reset signals to the gate drives on each of the power stages.

2.5.3. A/D Converter Signal Conditioning.

Texas Instruments THS1206 A/D converters are used on the daughter card. These A/D converters have a maximum sampling rate of 6Msamples/sec. at 12-bit resolution. There are 4 A/D chips and each chip has 4 channels that are sampled simultaneously, then the values are converted sequentially by a muxed 12-bit A/D converter and stored in a local buffer before being transferred over a parallel bus to a FIFO buffer in the FPGA. The input voltage range for the A/D converter channels is –1 V to +1 V.

All of the analog signals used in the control system come from either LEM voltage or current sensors. The LEM LV-25, 10-500Vrms voltage sensor is used for all voltage

measurements and the LEM LA-55, 50Arms current sensor is used for all current measurements. Additional channels of the A/D converters are reserved for the Airak, Inc. fiber optic current sensors. The output of the LEM sensors is a current in the 10mA range that is proportional to the measured variable. The conditioning circuits that were designed to interface the LEM sensors to the A/D converters provide a burden resistor to convert the current signal from the sensor to a voltage signal within the input range of the A/D converters. A picture of the conditioning circuits is shown in Figure 2.14. Example schematics of the conditioning circuits are shown in

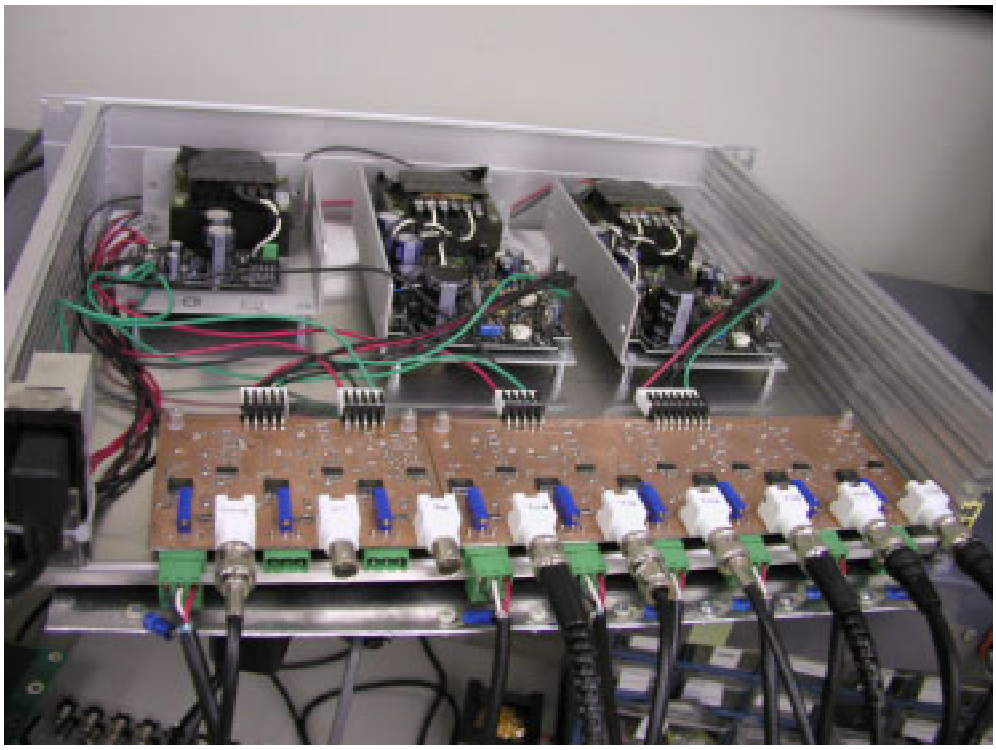


Figure 2.14. Analog signal conditioning circuits.

Figure 2.15. The first circuit schematic is used to measure AC quantities and does not offset the measured signal from zero. To fully utilize the input range of the A/D converters, the DC quantities are offset to –1V as in the second schematic in Figure 2.15. In the signal conditioning circuits an instrumentation amplifier is used to make a differential measurement on the burden resistor. Two LM347 op-amps are used to provide offset for the DC circuits and to allow adjustment of the offset to zero in the AC circuits and to –1V in the DC circuits with a potentiometer. A final op-amp is used in each circuit for a first order low pass, anti-aliasing

filter for the A/D channels. The cutoff of the low pass filters is set at one half of the sampling frequency of the A/D channels. After the signal passes through the anti-aliasing filter, it is connected back to the daughter card through a National Instruments breakout box. The breakout box also provides the connections for the digital I/O.

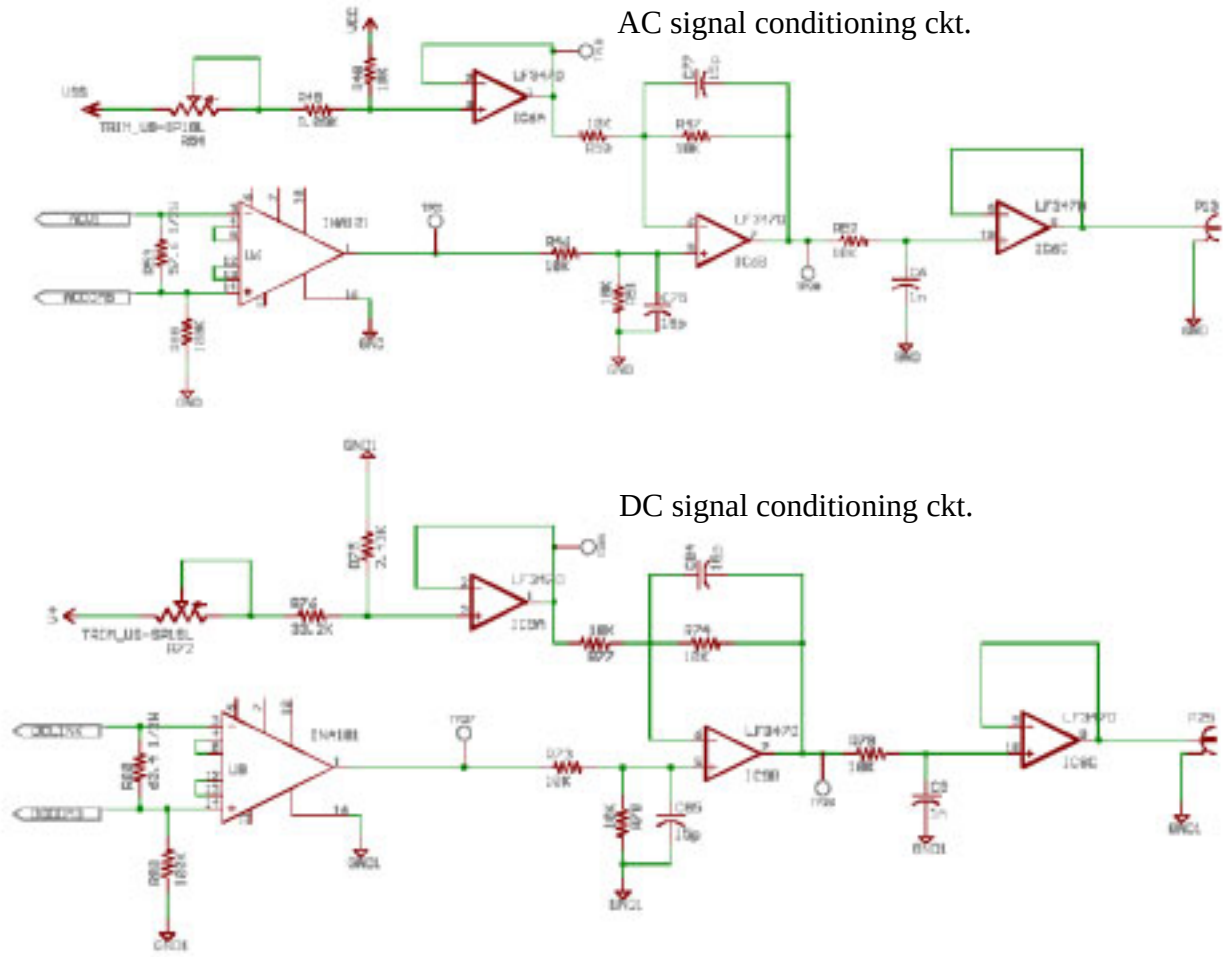


Figure 2.15. Signal conditioning circuit schematics.

2.5.4. Digital Interface.

The digital I/O on the controller are interfaced to the system through a National Instruments breakout box and then through the interface board shown in Figure 2.16. The cable from the breakout box plugs into the large connector on the interface board and the signals are split up to be sent to the inverter/active filter power stage through J2 and the DC/DC converter

through J3 and J4. A second order low-pass filter is placed in series with the PWM signal that controls the duty cycle to the DC/DC converter to form a D/A converter because the controller on the DC/DC converter requires a 0.5V to 3.5V signal for the duty cycle control.

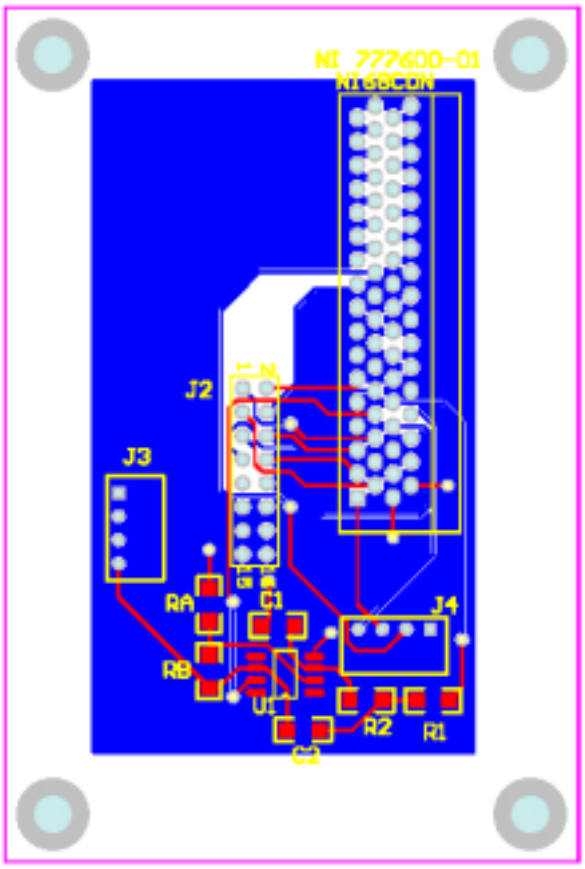


Figure 2.16. Digital interface board.

2.6. Conclusions.

This chapter described the hardware that was designed for the system including the power stages and the controller. Although the implementation of the peripherals in the FPGA can be considered hardware, discussion of their design will be delayed until Chapter 4, which covers the implementation of the controller. The DC/DC converter and the PV array were designed and

built, but due to a design oversight discussed in detail in Chapters 3 and 4 they were not included in the system that was built and tested.

Chapter 3. Controller Design.

3.1. Controller Overview

The system block diagram in Figure 3.1 shows all of the variables required for the proper control of the system.

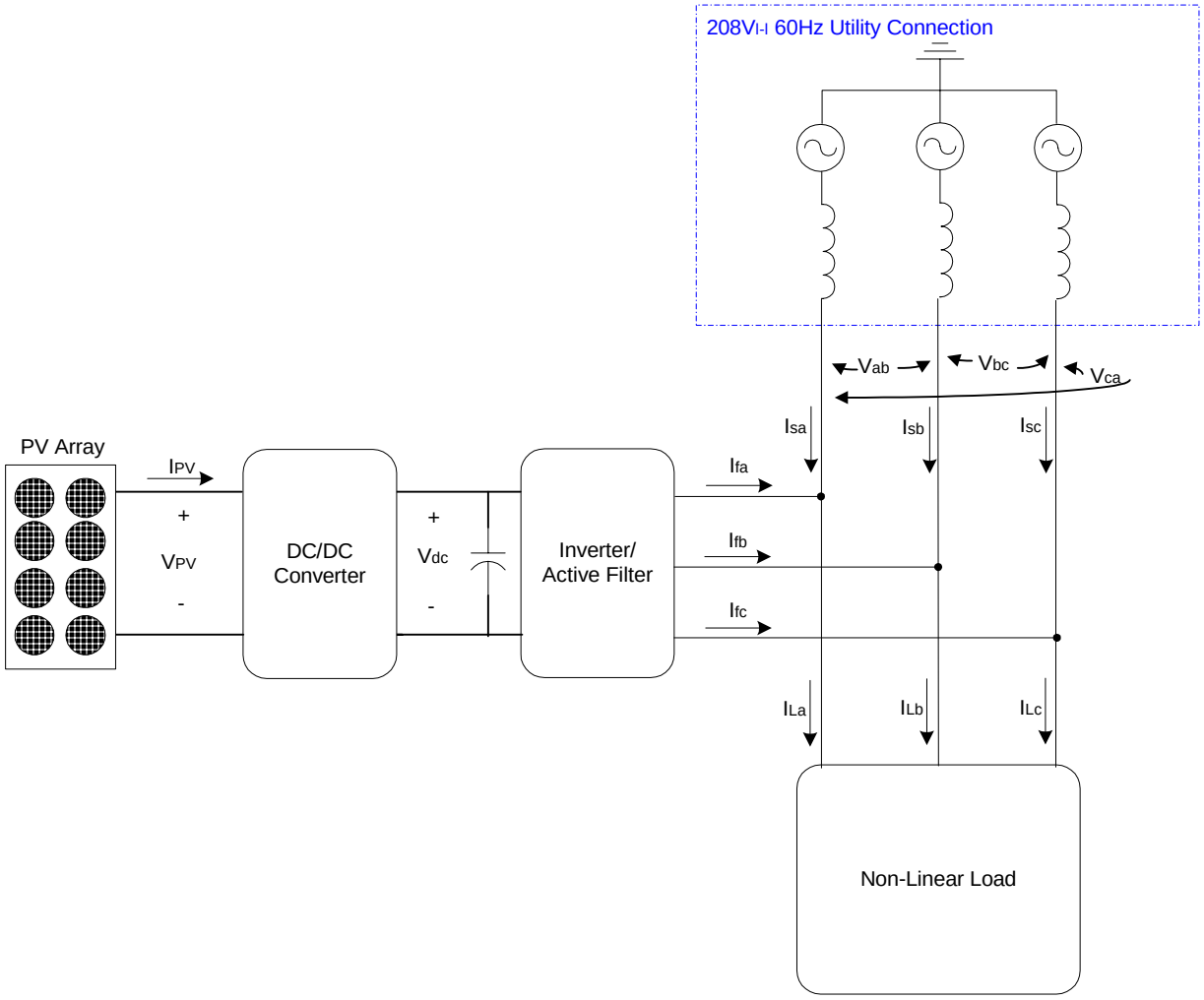


Figure 3.1. System block diagram showing variables of interest.

The sensed variables for the controller are PV array current (I_{PV}), PV array voltage (V_{PV}), DC link voltage (V_{dc}), inverter/active filter output currents (I_{fa}, I_{fb}), load currents (I_{La}, I_{Lb}), and utility voltages (V_{ab}, V_{bc}). Since the three phase sections of the system are three wire, only two of the three variables need to be sensed because the three value must add up to zero. As will be discussed in section 3.4, because of the model used for the inverter/ active filter, all of the three

phase variables are required to be line-to-line values. The utility voltages are measured as line-to-line values and the measured phase currents are converted to line-to-line values using (3.1) - (3.3).

$$i_{ab} = \frac{1}{3}(i_a - i_b) \qquad (3.1)$$

$$i_{bc} = \frac{1}{3}(i_b - i_c) \qquad (3.2)$$

$$i_{ca} = \frac{1}{3}(i_c - i_a) \qquad (3.3)$$

The PV array variables are used to control PV operation at the maximum power point. The DC link voltage, V_{dc} must be controlled to be higher than the peak, line-to-line voltage of the utility connection. To provide the active filtering function, the filter output currents; I_{fa}, I_{fb}, and I_{fc} are controlled to ensure that the utility line currents are sinusoidal and in phase with the line voltage. The filter output currents are also controlled to pass power from the PV array to the load and/or grid. The load currents are used to calculate the correcting currents for the active filtering function. Finally, the utility line voltages are sensed to both, help calculate the correcting currents for the active filter and for synchronizing the system to the utility.

All of the models that were used to develop the control system are outlined in sections 3.2 through 3.5. Section 3.6 gives some conclusions on the controller design.

3.2. PV Array Model.

One of the mistakes made in this work was an improper simplifying assumption about the behavior of the PV array. It was assumed that the behavior would be similar to an ideal voltage source in series with a resistor, and the original controller design was based on that assumption. Later in the design, a more accurate model of the PV array was developed and used in the controller simulations. Section 3.5 discusses the effects of the incorrect model on the overall controller design.

A more accurate model of the PV array was later developed using the datasheet information for the Siemens PV modules that were to be used in the system. The model, described in [20], allows the module manufacturers data to be used to create a model of the

entire array to be used in simulations. The simulation model was implemented as a Mast file for use in the Saber™ simulation package and the listing is shown in Appendix A. An example simulation of the PV array model is shown in Figure 3.2 where a resistive load is swept from a low value to close to a short circuit condition. The model becomes numerically unstable as the load approaches a short circuit and therefore the model cannot be used for simulations that may require short circuit conditions. The waveforms in Figure 3.2 show the voltage source region, the current source region and the transition region where the maximum power point exists. As the power profile shows, the maximum power of the model is 8% lower than the rated power of the actual PV array, but the basic behavior of the array is present.

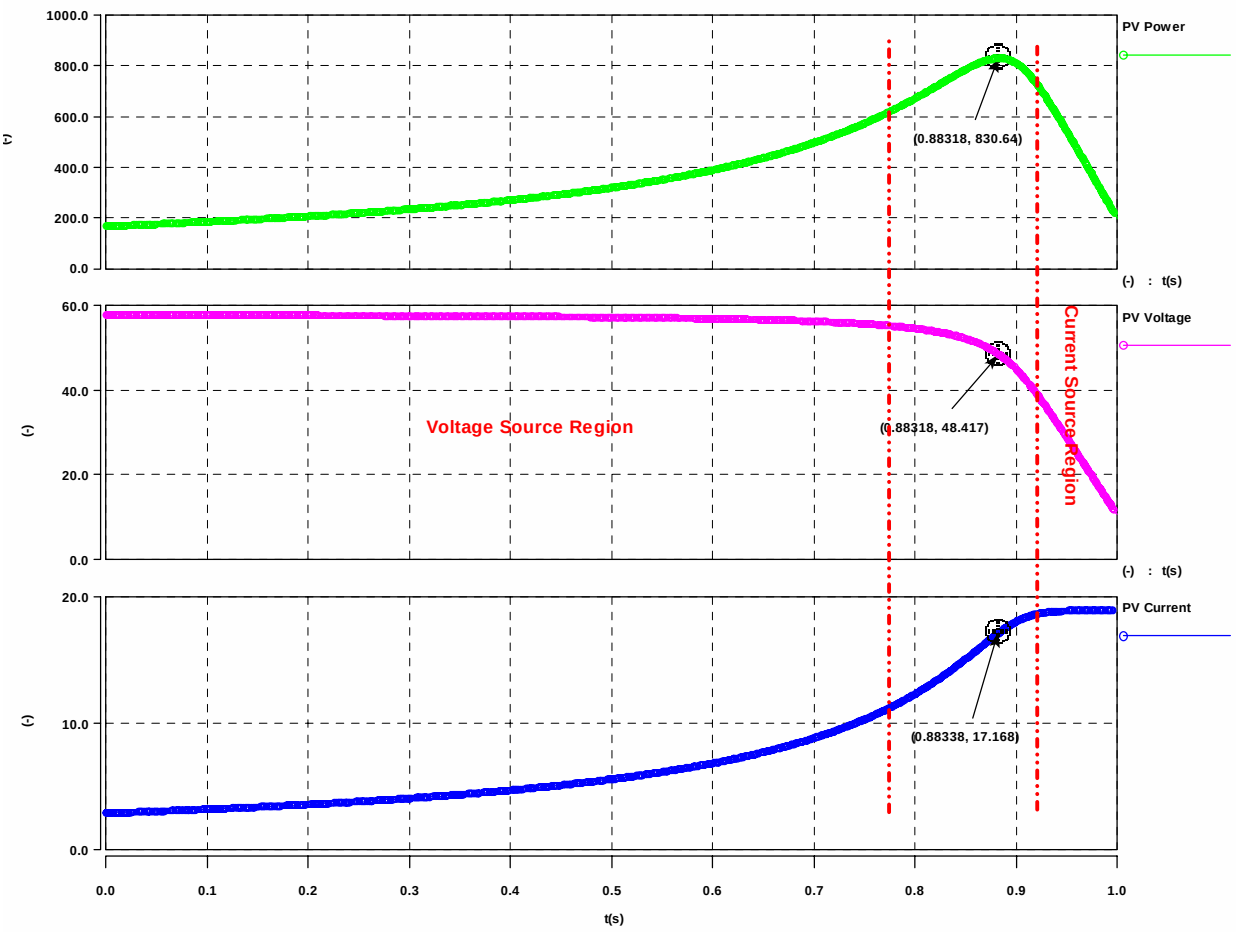


Figure 3.2. Load sweep simulation of the PV array model.

3.3. DC/DC Converter Model and Controller.

At the beginning of the design process an incorrect assumption was made about the behavior of the PV array as discussed in section 3.2 and the DC/DC converter control design was based on that assumption. The control loop for the front end DC-DC converter was developed using Saber. The model for the converter was built in Saber based on the averaged switch model proposed by Tsai [19]. Initial simulations of the converter showed that in the operating range available from the PV array, the converter would always operate in the discontinuous conductions mode. In DCM the averaged switch model includes the switches, transformer, and rectifier, which are represented by the model shown in Figure 3.3 and equations (3.4) through (3.7).

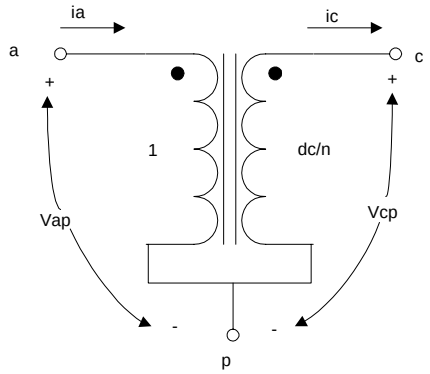


Figure 3.3. ZVS PWM averaged switch model.

$$dc = \frac{d}{d + d2} \qquad (3.4)$$

$$d2 = \frac{2L_f i_c f_r n}{dv_{ap}} \qquad (3.5)$$

$$v_{cp} = \frac{v_{ap} dc}{n} \qquad (3.6)$$

$$i_a = \frac{i_c dc}{n} \qquad (3.7)$$

Where: d = duty cycle

L_f = Filter inductor value

f_r = Output ripple frequency (2*switching frequency)

n = Transformer turns ratio

The Saber model of the averaged switch is shown in Figure 3.4. This model utilized the control modeling components in the Saber parts library to implement equations (3.4) through (3.7). Figure 3.5 shows the simulation schematic of the DC/DC converter. An anti-aliasing filter at 15kHz was placed in the model along with a delay of 1.4 times the sampling period of the system to model the effects of the digital control. The open loop response from control to output voltage is shown in Figure 3.6.

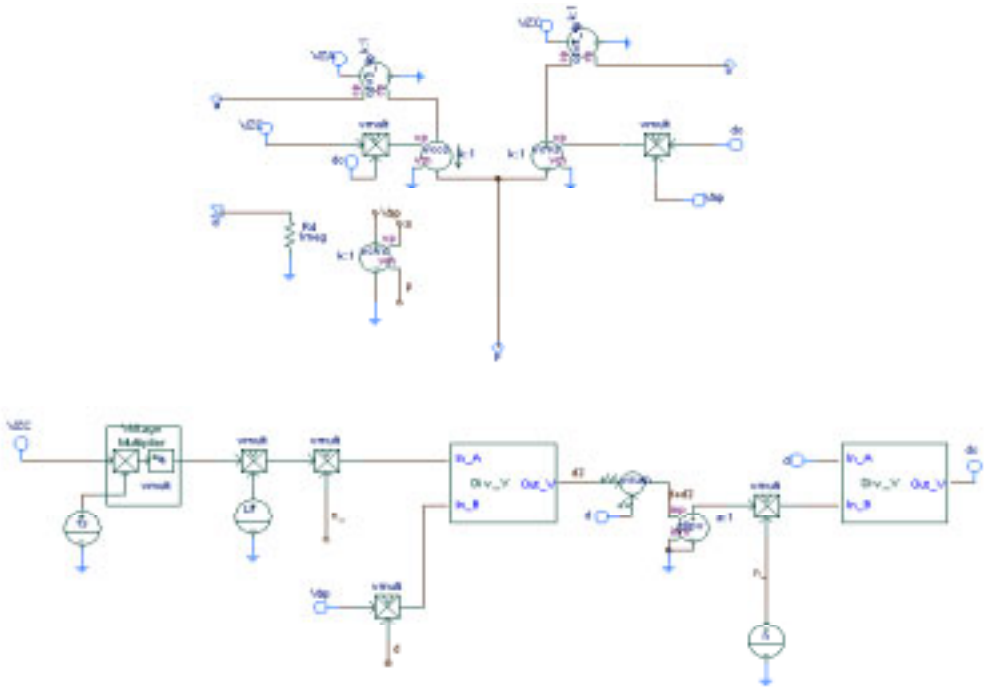


Figure 3.4. Averaged switch simulation model in Saber.

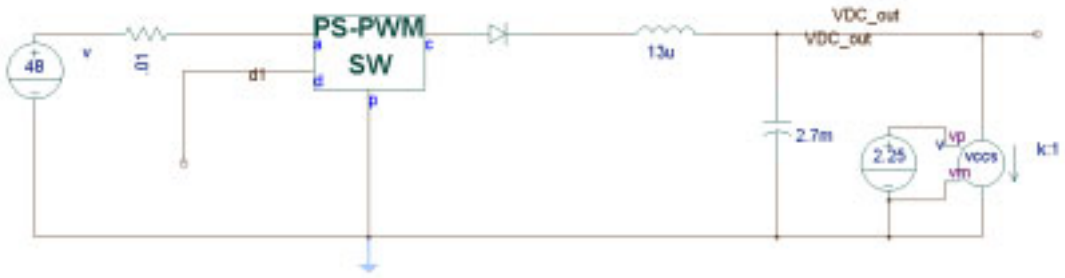


Figure 3.5. Converter simulation schematic.

Because of the complexity of the overall control system, a simple proportional-integral compensator was chosen to close the voltage loop on the DC/DC converter. The integrator ensures that there is no steady state error in the commanded DC link voltage. The voltage loop controls the DC link capacitor voltage, which will also be controlled by the input voltage loop of the active filter. To prevent interaction of these two loops, the bandwidth of the DC/DC converter's voltage loop was designed to be much higher than that of the active filter input voltage loop.

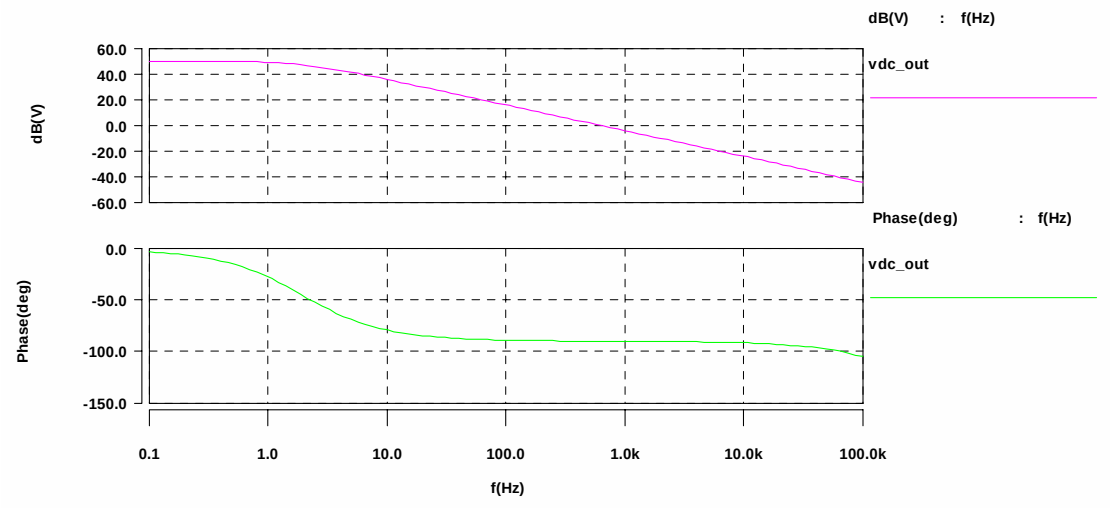


Figure 3.6. Open loop control to output response.

A comparison of the loop response for the two controllers is shown in section 3.5. The loop gain from Saber is shown in Figure 3.7. The gain crosses zero at 1147 Hz with a 65 degree phase margin. The gain margin is 11 dB. The proportional and integral gain constants for the controller are listed in Table 3.1. The closed loop response from control to output is shown in Figure 3.8.

Table 3.1. DC/DC Compensator Constants.

Constant	Value
Kp	0.06
Ki	0.5

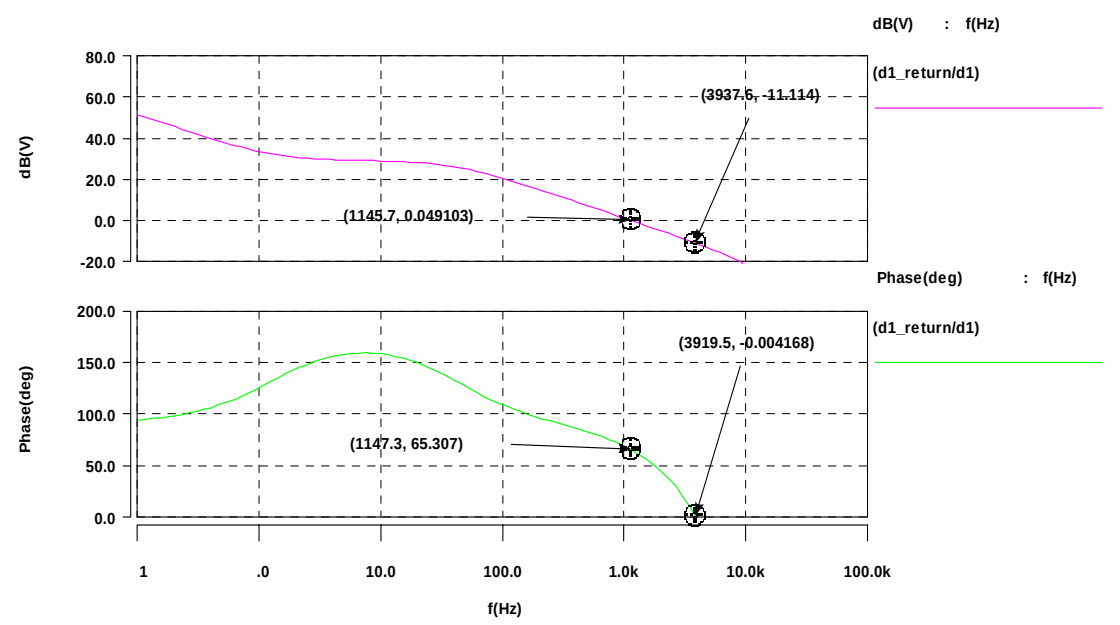


Figure 3.7. Loop gain of the converter with proportional-integral control.

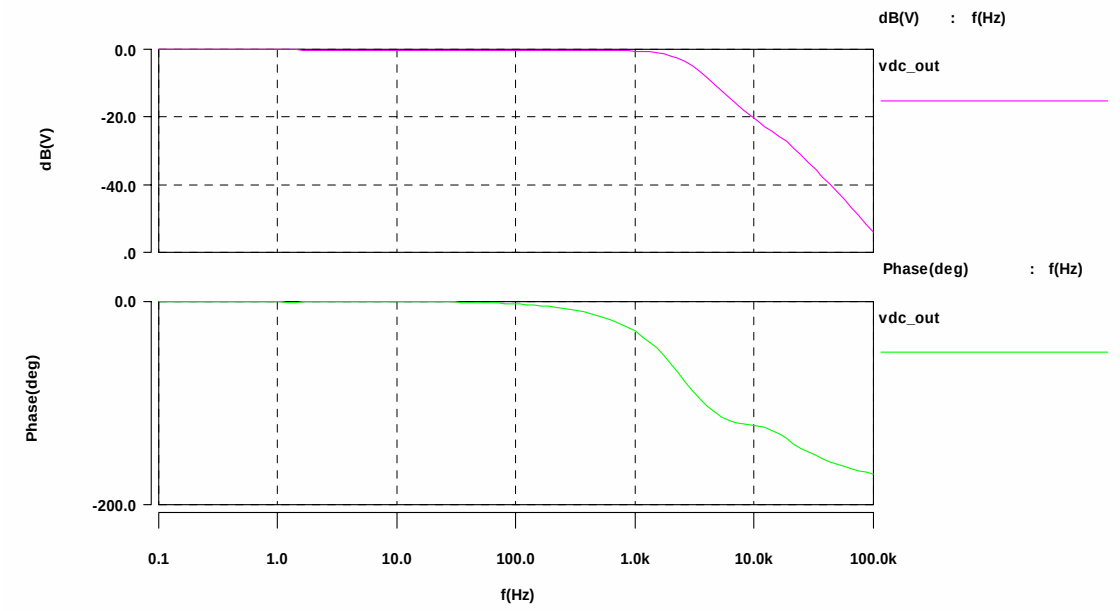


Figure 3.8. Closed loop response from control to output.

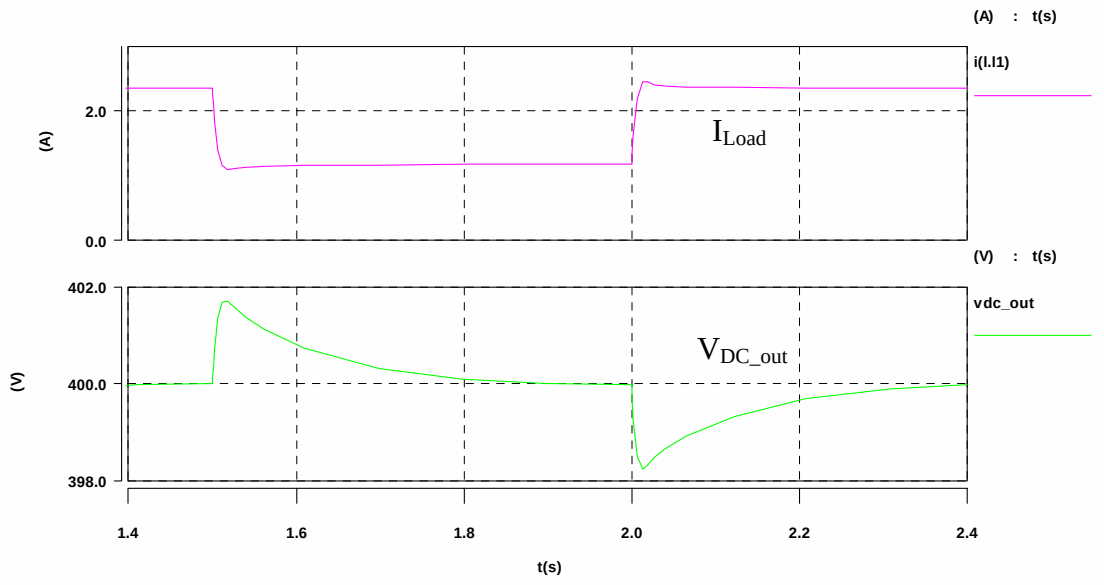


Figure 3.9. Load step from 100% to 50% and back to 100%.

Figure 3.9 shows a load step from 100% to 50% and back to 100%, and it can be seen that the overshoot is less than 2 V. The voltage takes a considerable amount of time to settle back to steady state due to the large capacitor size.

3.4. Inverter/Active Filter Model and Controller.

The inverter/active filter power stage is a six switch current bi-directional converter that consists of a switching network and the filter components. The output filter for this application is comprised of three 815µH inductors. A schematic representation of the power stage model including the energy storage capacitor is shown in Figure 3.10.

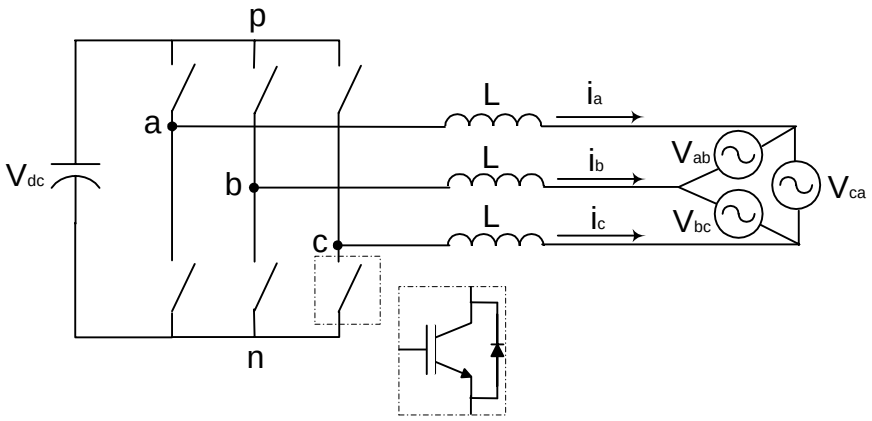


Figure 3.10. Inverter/active filter power stage switching model.

The output of the inverter is connected to the utility grid, which is represented as an ideal, balanced, delta, three phase voltage source. This simplification of the utility grid model is based on a simplifying assumption that the utility voltage is stiff and therefore is unaffected by the converter output currents. Each of the switches in the switching network are IGBTs with anti-parallel diodes to allow current flow in both directions and voltage blocking in one direction. The switching network model is comprised of three single-pole, double-throw switches [21]. In order to insure that the current through the filter inductors is never interrupted, the switches must meet the operating condition based on the switching function defined below [21]:

Switch function definition:

$$s_{jk} = \begin{cases} 1, sw_{jk} closed \\ 0, sw_{jk} closed \end{cases} \quad j = \{a,b,c\}, k = \{p,n\} \qquad (3.8)$$

Switch condition requirements:

$$s_{jp} + s_{jn} = 1,\ j = \{a,b,c\} \qquad (3.9)$$

The switching network is averaged as in [21] to get the circuit shown in Figure 3.11. The line to line currents on the left side of the model are calculated from the line currents on the right side using (3.1) - (3.3). This model was implemented in Saber and the line-to-line three phase variables were transformed into the synchronous reference frame to allow for the controller designs. Since the system is 3-wire, there are no zero-sequence currents and therefore the zero sequence variables are dropped from the model. An example transformation used to place the three phase variables in the dq0 reference frame is shown in (3.10).

$$\begin{bmatrix} i_{fd} \\ i_{fq} \end{bmatrix} = T \cdot \begin{bmatrix} i_{fab} \\ i_{fbc} \\ i_{fca} \end{bmatrix}$$

$$\begin{bmatrix} i_{fd} \\ i_{fq} \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ -\sin(\omega t) & -\sin(\omega t - \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) \end{bmatrix} \cdot \begin{bmatrix} i_{fab} \\ i_{fbc} \\ i_{fca} \end{bmatrix} \quad (3.10)$$

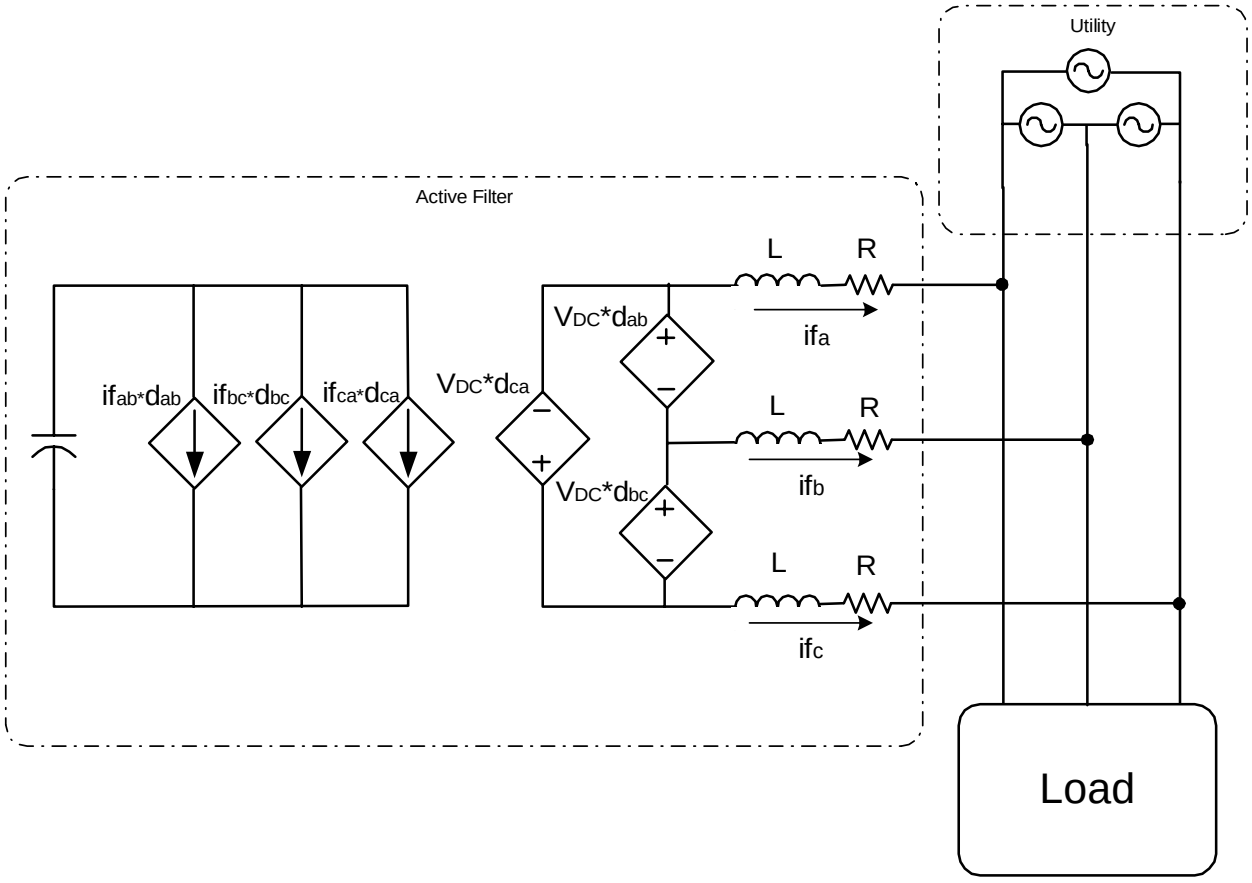


Figure 3.11. Active filter schematic in averaged form.

Linearization around an operating point and the small signal modeling of the converter connected to the utility and load were performed using Saber. Open loop transfer functions from the d-axis control to d-axis current and q-axis current are shown in Figure 3.12. The transfer functions show that the plant shows a first order response with a high gain at lower frequencies

due to the L and R at the filter output. At higher frequencies the phase roll off dominates the response due to the delay added to model the calculation delay and the modulator. There is a strong cross coupling between the d and q axis currents due to the dynamics of the output filter.

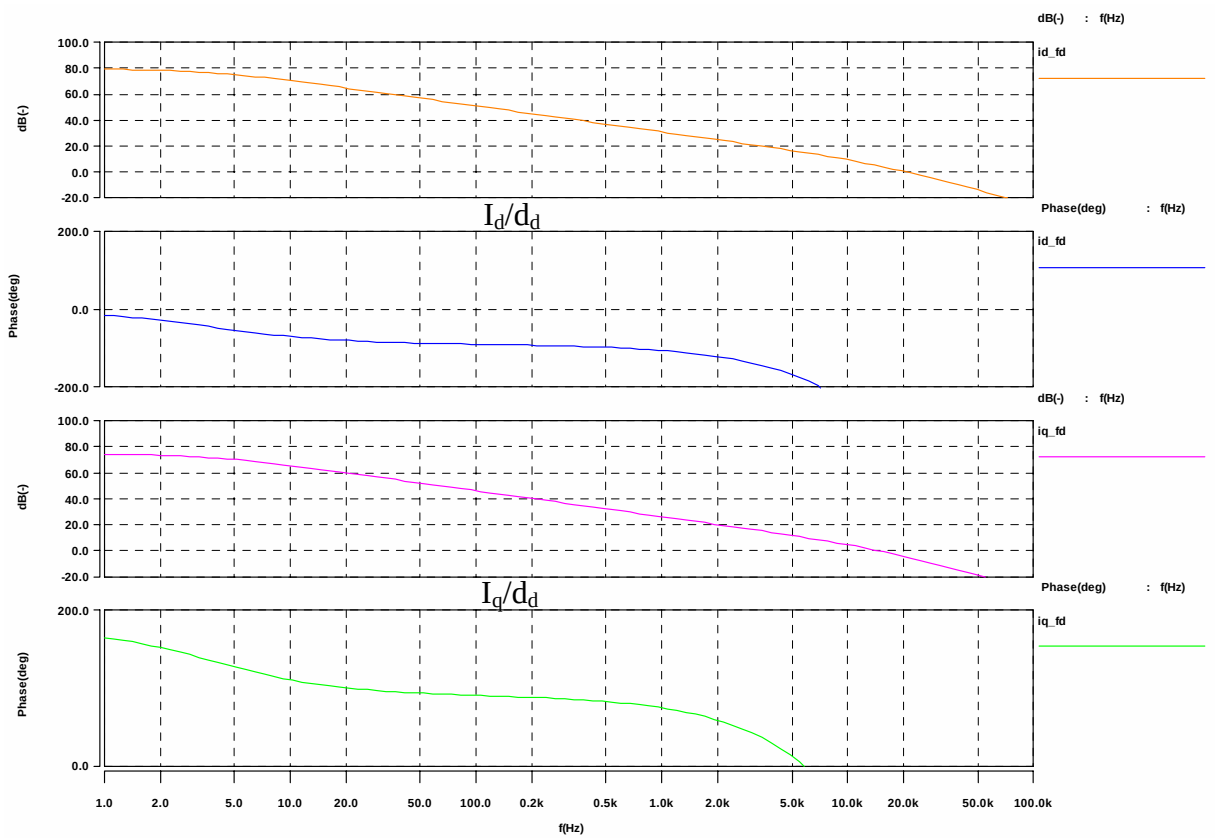


Figure 3.12. Open loop transfer functions id/dd and iq/dd.

The control scheme used for the active filter is based on the method described in [22]. Using the portion of the inverter model in the dq0 reference frame shown in Figure 3.13, the decoupling and cancellation equation for the d and q axis currents is developed and is shown in (3.11), where the u_d and u_q terms are calculated by passing the error of the filter currents and the reference currents in d-q reference frame through PI compensators. Figure 3.14 shows the calculation of the reference currents and the u_d and u_q terms.

$$d_d = \frac{V_d - 3L \cdot \omega \cdot i_{fq} + u_d}{V_{dc}}$$
$$d_q = \frac{V_d + 3L \cdot \omega \cdot i_{fd} + u_q}{V_{dc}} \qquad (3.11)$$

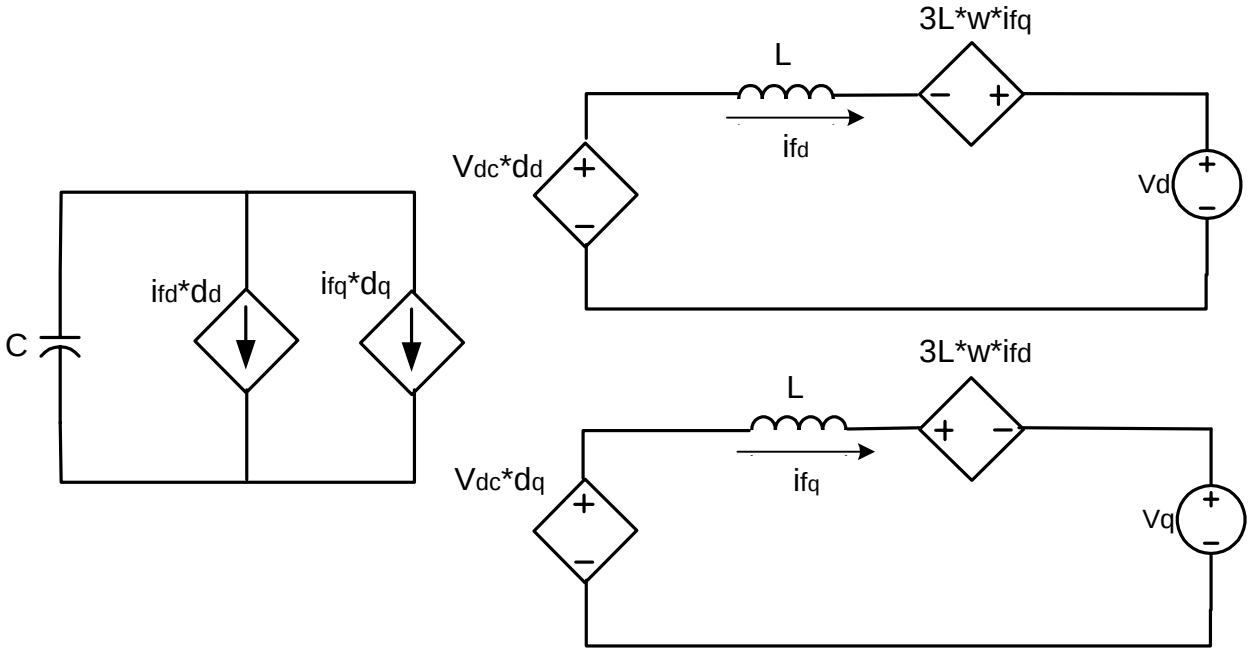


Figure 3.13. Inverter model in dq0 reference frame.

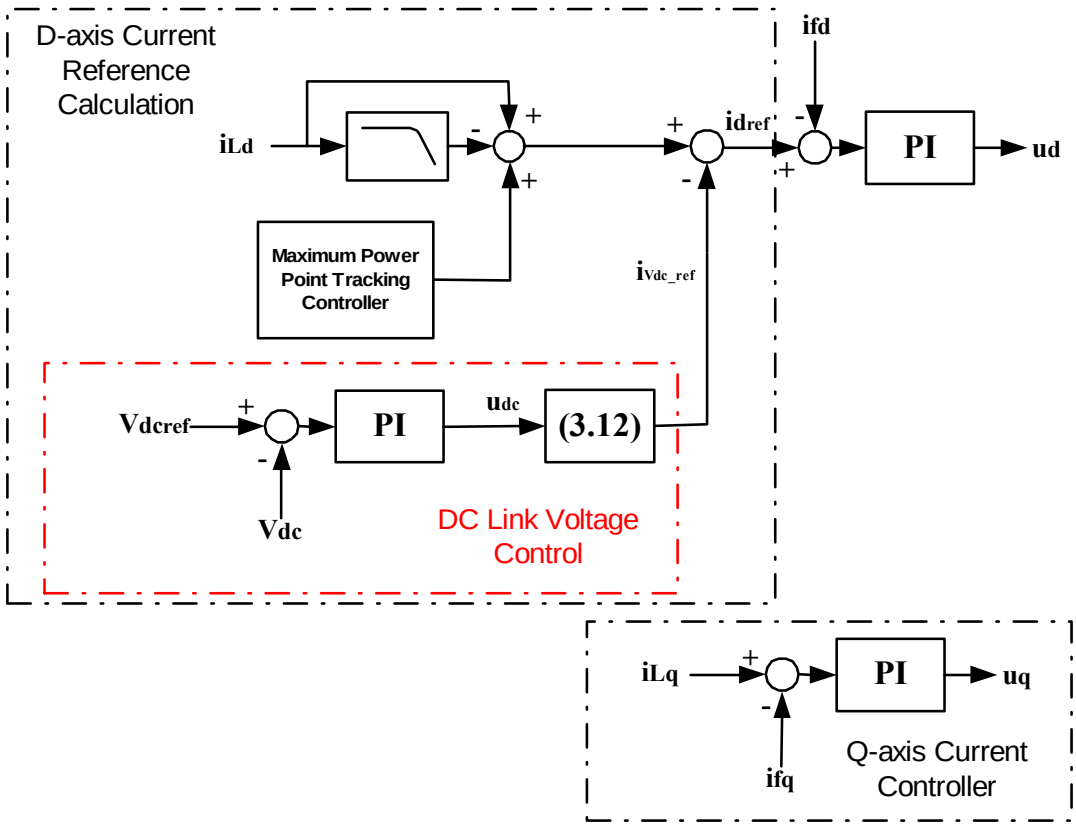


Figure 3.14. Current controllers.

$$i_{Vdc\_ref} = \sqrt{\frac{2}{3}} \cdot \frac{V_{dc}}{V_m} \cdot u_{dc} \qquad (3.12)$$

The q-axis reference current is simply the q-axis load current because the active filter is designed to correct for harmonic currents as well as displacement factor, so the q-axis current is driven to zero by the PI compensator. Calculation of the d-axis reference current is much more complex. First, the d-axis load current is passed through a high pass filter that removes the DC component in the d-q reference frame, which corresponds to the fundamental component of the real power flowing to the load. Next, a command is added back in by the maximum power point controller that corresponds to the real power available from the PV array that is to be passed through the inverter to the load or utility. Finally, the inverter DC link voltage controller calculates a command that is subtracted to maintain the DC link voltage by passing the Vdc error through a PI compensator and (3.12). The inverter DC link voltage controller is discussed in more detail in Section 3.5. The result of the above calculations is the d-axis reference current that is compared to the d-axis filter current and the error is fed through a PI compensator to get the u_d value used by (3.11) to calculate the d-axis duty cycle. The PI compensators for the current loops were adjusted using the average model in Saber to get a large bandwidth with sufficient phase and gain margin. The loop gain plots of the closed q-axis current loop with 10 kW of resistive load are shown in Figure 3.15.

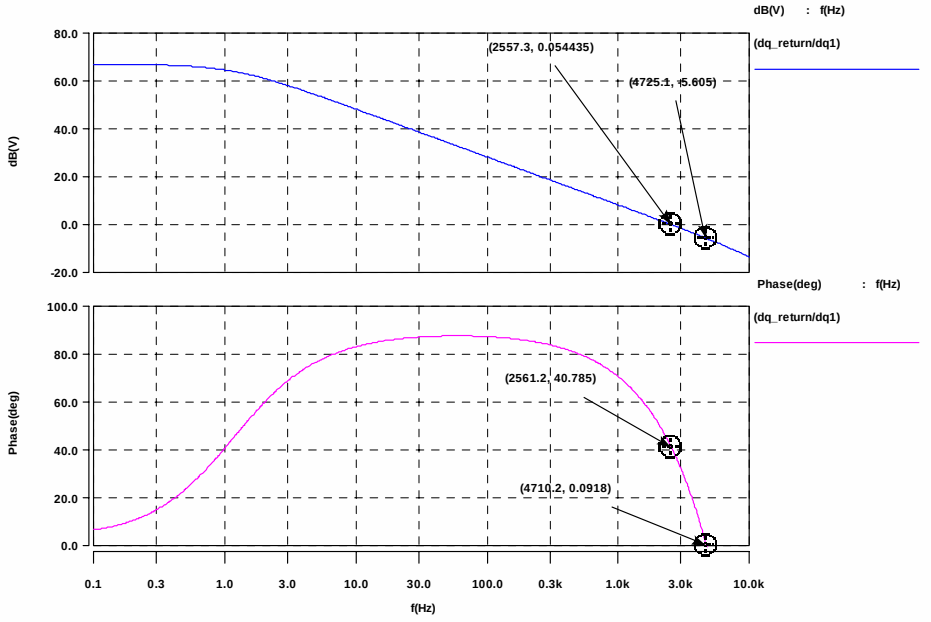


Figure 3.15. Loop gain simulations of d and q axis current controllers.

The phase margin is 40 degrees and the gain margin is 6.8 dB. Current waveforms from a time domain simulation of the active filter with 10 kW of non-linear load on the bus are shown in Figure 3.16.

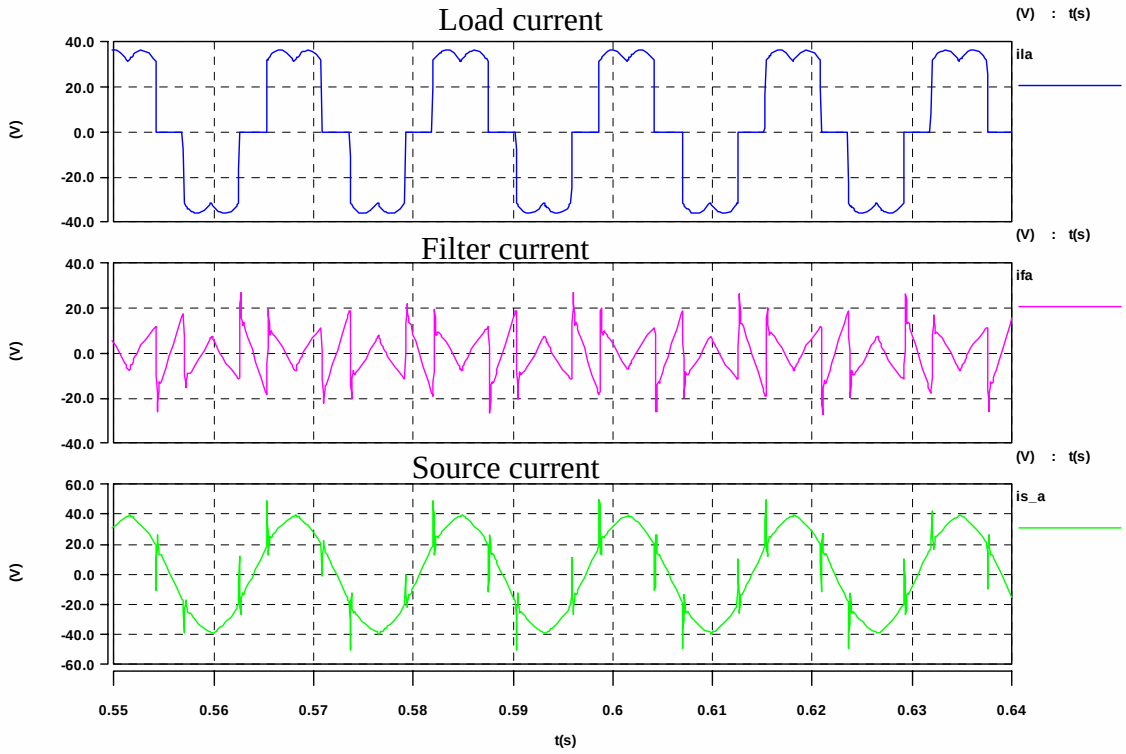


Figure 3.16. Active filter simulation results.

Looking at the source currents from the simulation, spikes remain on the waveform at the times when the load current undergoes a rapid transition. The limited bandwidth of the current controllers prevents the system from properly responding to the rapid current excursions. Figure 3.17 shows a close up of one of the spikes along with the current rise that caused it. The current spike in the source current can be viewed as a transient response of the active filter to the rapid increase in the load current. This issue with the active filter performance is discussed in more detail in section 5.2.

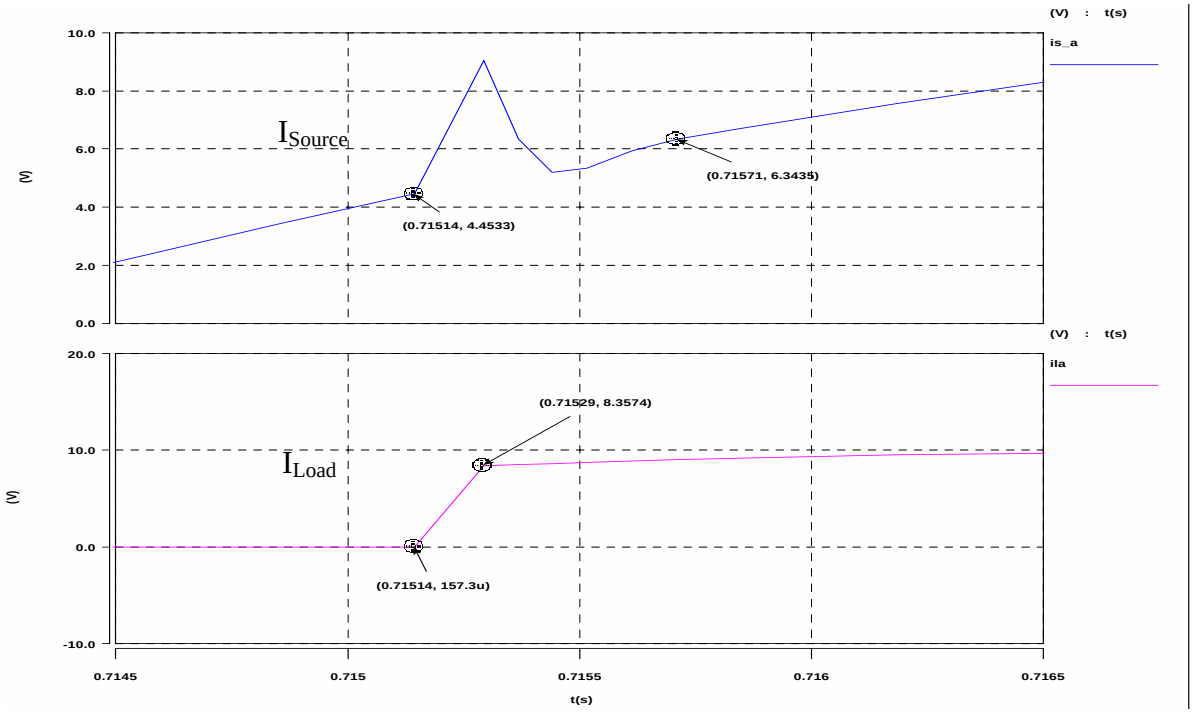


Figure 3.17. Source current spike detail.

3.5. DC-Link Voltage Control Scheme.

A method for controlling the DC link in this system is proposed that has two voltage control loops, the one for the DC/DC converter described in section 3.3 and the inverter voltage loop mentioned in section 3.4. The reason for having two voltage loops is so that when energy from the PV array is no longer available, and the DC/DC converter shuts down, there will still be a controller left to maintain the DC link voltage. To prevent interaction between the two controllers, the bandwidth of the DC/DC converter voltage loop was designed to be high and the inverter DC voltage control loop bandwidth was designed to be at least 10 times lower. The

DC/DC converter voltage loop dominates the inverter voltage loop while the PV array is operational and when the DC/DC converter shuts down the inverter voltage loop takes over control of the DC link voltage. Simulations of the loop gain for the DC/DC voltage loop and the inverter voltage loop show that when the DC/DC converter is in operation, the inverter voltage loop gain is never greater that unity and when the DC/DC converter shuts down the inverter voltage loop gain rises back up to its designed bandwidth. These simulation results are shown in Figures 3.18 through 3.20.

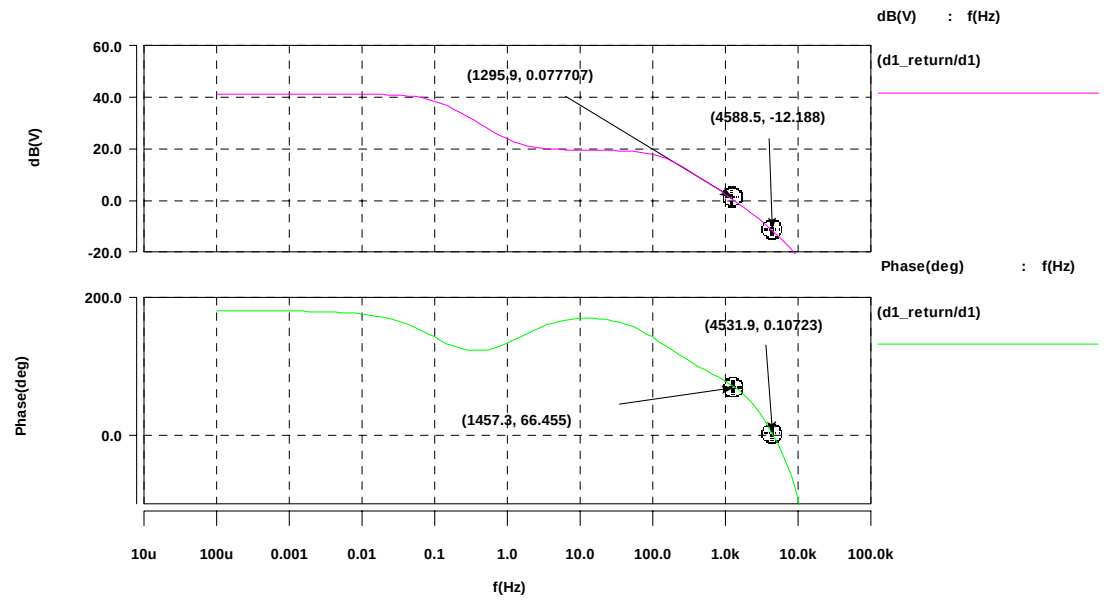


Figure 3.18. DC/DC converter voltage controller loop gain with inverter in operation.

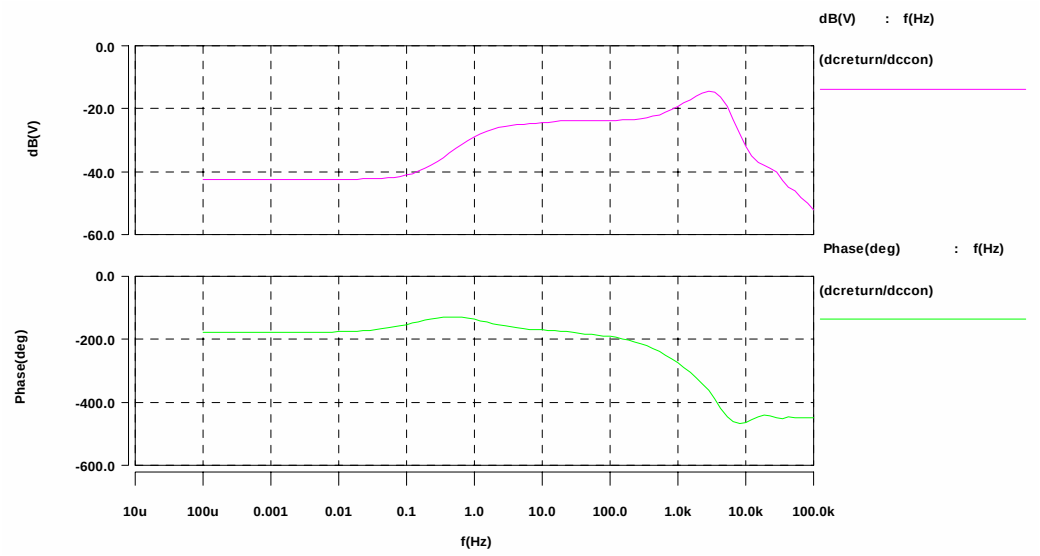


Figure 3.19. Inverter DC voltage controller loop gain with DC/DC converter operating.

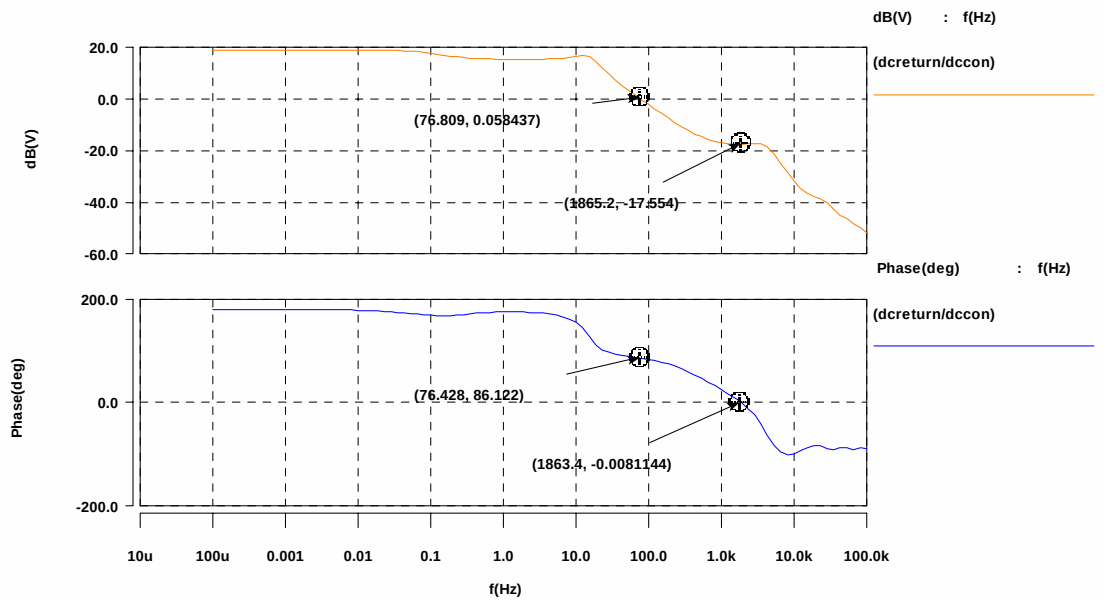


Figure 3.20. Inverter DC voltage controller loop gain with DC/DC converter shut down.

Time domain simulations show that this control scheme works and is stable both with and without the PV array in operation. Figure 3.21 shows a time domain simulation of the system with a load consisting of 5 kW of non-linear load and 2.4 kW of resistive load and the PV array is supplying 1 kW of real power to the system. The Fourier analyses of the current waveforms in Figure 3.21 are shown in Figure 3.22.

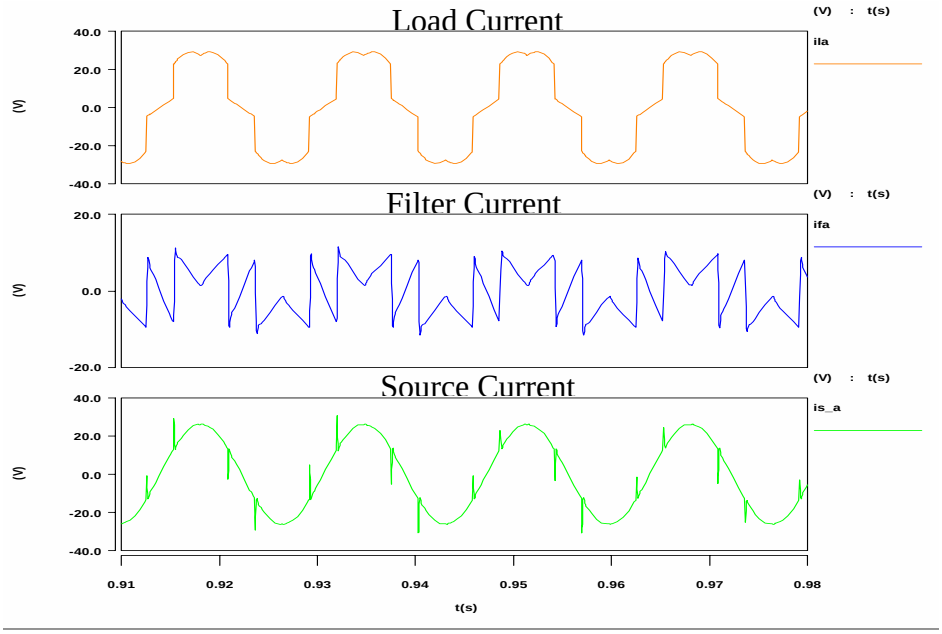


Figure 3.21. Transient analysis at 5 kW non-linear, 2.4 kW resistive load (1 kW from PV array).

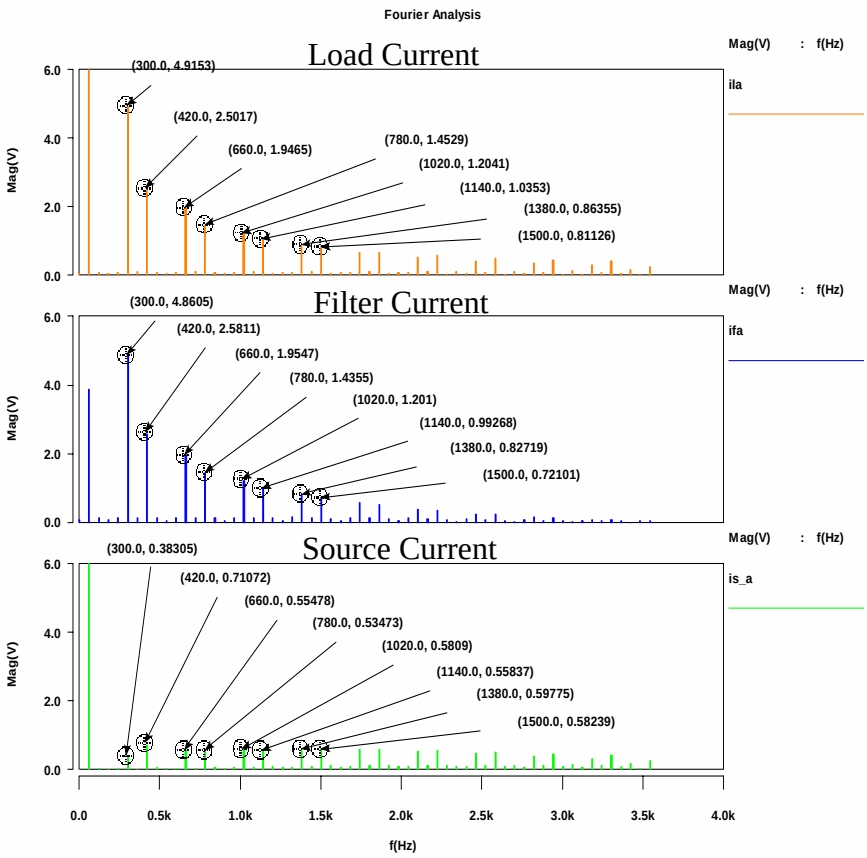


Figure 3.22. Fourier analysis of currents from figure 3.21.

This method of controlling the two functions of the system, (PV generation and active filter), works well with the simplified model of the PV array that was originally used as mentioned in section 3.2. The resistance in series with a voltage source gives a linear V-I curve and the resistance chosen in the original simulations resulted in a relatively stiff voltage source, or a shallow slope in the V-I curve. Figure 3.23 shows a typical V-I curve of a PV array and the normal operating point is at the maximum power point, where the slope is much steeper than in the voltage source region of the array. When the more realistic model of the PV array was introduced into the system simulation the DC/DC converter voltage control bandwidth was greatly decreased by the soft response of the PV array to load changes. The proposed control method relies on the DC/DC converter voltage loop having a large bandwidth compared to the inverter DC voltage control loop, and the loss of bandwidth caused by the soft PV model caused the system to become unstable.

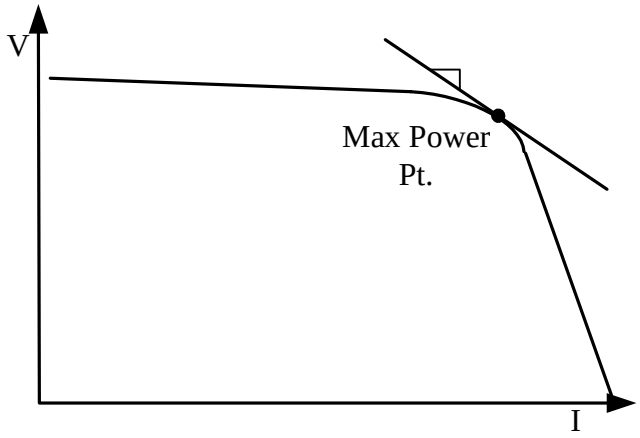


Figure 3.23. Example PV array V-I curve.

Because the DC/DC converter had already been designed when the problem with the model was discovered, the decision was made to not implement the PV array and DC/DC converter in hardware. More work needs to be done to either redesign the DC/DC converter or add a buffer between the PV array and the DC/DC converter to allow the DC/DC converter voltage loop bandwidth to remain high enough for the proposed control scheme to work.

3.6. Conclusion.

This chapter outlined the modeling and development of the control system for the active filter/PV generation system. A method is proposed for controlling both functions of the system by designing both the DC/DC converter and the inverter to have a DC link voltage controller. The DC/DC converter voltage loop is designed to have a much higher bandwidth than the inverter voltage loop, so that when the DC/DC converter is in operation, the inverter voltage control loop response is overridden. The output of the maximum power point tracking controller for the PV array is fed to the inverter d-axis current controller as a current command that is proportional to the power available from the PV array. Since the utility line voltage can be assumed to be constant and the d-axis is aligned with the real power in the controller, a zero frequency current in the d-axis is proportional to the real power flowing through the inverter. The problem of the soft response of the PV array to load changes needs to be resolved to allow for the DC/DC converter to maintain a high control bandwidth for this method to be successfully implemented.

Chapter 4. Controller Implementation.

4.1. Controller Implementation Overview.

This chapter outlines the actual implementation of the controller for the active filter portion of the system. As discussed in Chapter 2, the controller hardware consists of a Texas Instruments 32 bit floating point DSP that is interfaced to the power stage hardware through a configurable analog and digital I/O daughtercard from Signalware, Inc. The daughtercard is configurable using a Xilinx field programmable gate array (FPGA) that allows custom interfacing of the A/D converters and the digital I/O between the DSP and the hardware to be controlled. The daugtercard comes with a framework DSP and FPGA program that provides basic data acquisition and control of the digital I/O. The DSP program is written in C and the FPGA program is a schematic entry program. These programs were altered to meet the requirements of the active filter controller. This chapter details the methods that were used to implement the control algorithms from Chapter 3 into the DSP and FPGA. The C code that implements the control algorithm is listed in Appendix B and the FPGA schematics that were developed for the controller are detailed in the remainder of this chapter.

4.2. Data Acquisition.

All of the variables that need to be measured in order to implement the control algorithm detailed in Chapter 3 are captured using the daughtercard A/D converters. The interface of the A/D converters to the DSP is already implemented in the framework program, and only required that the sampling frequency be altered. As discussed in Chapter 2, the daughtercard A/D converters are capable of a maximum sampling rate of 6 MS/s, but this application required a much lower sampling rate. The switching frequency for the IGBTs in the power stage is 32 kHz, and the sampling frequency is set 4 times this frequency (128 kHz).

The implementation of the data acquisition system transfers the samples from the A/D converter to a FIFO buffer in the FPGA after the 4 channels of the A/D converter have been converted. After 4 samples from each channel are transferred to the FIFO, the FPGA triggers a DMA transfer in the DSP and the sampled data is moved to the DSP memory space for the control program to use. The DSP program structure polls a register to determine when the DMA transfer has completed to call the control algorithm function in the program. When the control

algorithm function is called, it is passed a pointer to the memory location containing the latest set of samples from the A/D converters. At the beginning of the control algorithm function in the controller code, the latest sample from each channel is converted from a fixed-point value to a floating point value and scaled to be in engineering units appropriate for the control algorithms.

4.3. Phase Locked Loop.

Since the control algorithms are implemented in the dq0 reference frame, a sine wave and cosine wave need to be generated that are synchronized to the utility grid voltage to perform the abc to dq0 and the dq0 to abc transformations. A phase locked loop (PLL) is required to perform the synchronization. Software implementations of PLLs were investigated to avoid building additional hardware for the PLL. The first PLL that was implemented in the controller is the Costas Loop [23] [24] [25] [26].

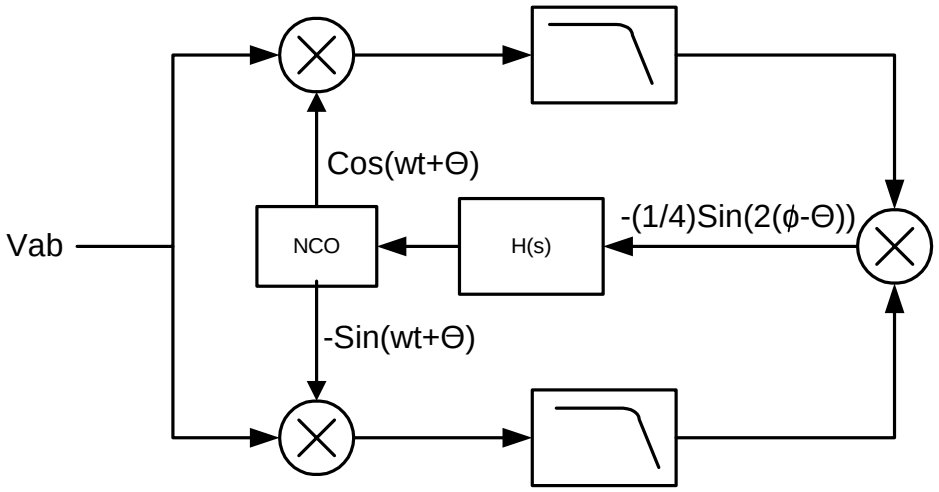


Figure 4.1. Costas Loop block diagram.

Figure 4.1 shows the block diagram of the Costas Loop which takes the voltage between phase A and B as the input to lock the numerically controlled oscillator (NCO) in phase. The NCO generates a cosine and the negative of a sine wave that are mixed with the input waveform. The mixing outputs contain a component that is twice the frequency of the input and a component that is a function of the phase difference between the input waveform and the NCO waveforms. The low pass filters in the upper and lower arm of the Costas Loop remove the two times frequency component. An error term, (-1/4*sin(2(ϕ-θ))), is then developed by mixing the

outputs of the low pass filters. A compensator, H(s), drives the error term to zero by adjusting the frequency of the NCO. The NCO must be started with a frequency that is close to the input frequency to allow the PLL to lock onto the input waveform. This is not a concern in this application because the utility line frequency is very stable.

Simulink was used to model the PLL for the design of the compensator and a simulation is shown in Figure 4.2.

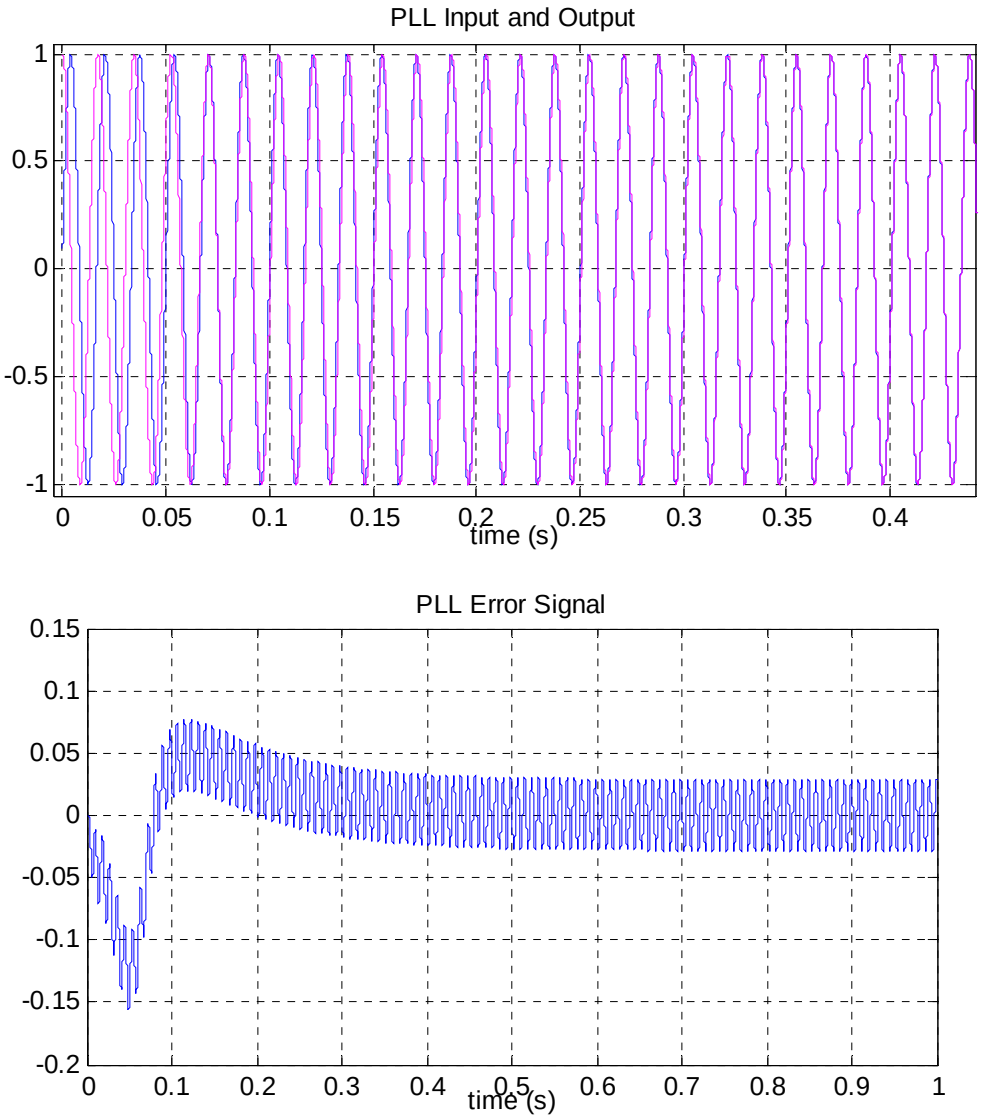


Figure 4.2. Costas Loop simulation.

The PLL locks onto the input in less than 0.4 seconds. The oscillations in the error signal are due to leakage of the 2nd harmonic term through the low pass filters.

The Costas Loop is easily implemented in software and performs well. There is one major drawback to this method of implementing a PLL, the error signal is the sine of the phase difference, which has two stable points. This PLL can lock in phase and 180 degrees out of phase. To get around this problem, the controller waited until the PLL locked on and then checked to see if the NCO was in phase or 180 degrees out of phase with the input waveform. If the PLL locked on out of phase, the NCO was advanced a half cycle and the PLL would be locked in phase. The system start up could then continue after the PLL was properly locked onto the input.

An implementation of a software based PLL was found in the literature that offered advantages in this application, and was used to replace the Costas Loop [27]. Figure 4.3 shows a block diagram of the improved PLL.

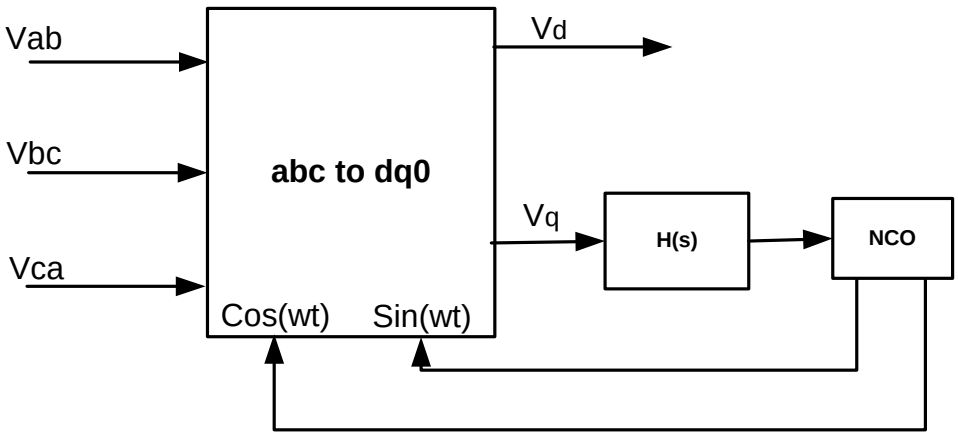


Figure 4.3. dq0 transform based PLL.

The new PLL offers a significant decrease in computational requirements over the Costas Loop. In this application the Vd and Vq are required in the control algorithm so the abc to dq0 transformation in the PLL already existed in the control algorithm. This method also does away with the arm filters in the Costas Loop and the multiplication operations required for mixing the signals. Since the d-axis is the power axis, the compensator drives the Vq value to zero by adjusting the NCO frequency.

The NCO was implemented using techniques outlined by Hagemann, in [28] and [29]. The cosine and sine waves required for the Park's Transformation are implemented with a lookup table. Two lookup tables are used to improve the SNR of the sinusoids, the first table contains 1024 values of the unit sine from 0 to 2π, and the second table contains the slopes between each of the values in the first table. Indexing into the sine table is done with a 20 bit index. The first 10 bits are used to choose the sine value from table one and the second 10 bits are used as the distance between the two sine table values and is multiplied by the slope and added to the sine table value to interpolate between the values. A Matlab m-file was used to generate the sine and slope tables and is included in Appendix C. The PLL compensator output controls the size of the index increment each sampling period to control the frequency of the NCO. The index of the sine table is rolled over when it exceeds 2^{20}.

As mentioned before, both PLL methods perform well, but the dq0 based method is computationally more efficient for this application. Both PLLs will lose synchronization in the event of a large transient on the utility voltage. In order for the system to be protected it must be shut down when the PLL loses synchronization and restarted once the transient has subsided and the PLL has regained synchronization.

4.4. Digital Filter Implementation.

The original controller required several filters, two low pass filters for the Costas Loop and one low pass filter for the d-axis current control. Matlab was used to design the filters directly in the digital domain by specifying the sampling frequency, cutoff frequency, the order and type of filter. The d-axis current controller low pass filter has a 20 Hz cutoff at a sampling frequency of 32568 Hz, and is a 2^{nd} order Butterworth IIR direct form II filter. Figure 4.4 shows a block diagram of the filter implementation and the frequency response of the filter. The code that was used to implement the filter in the controller is in the code listing in Appendix B. As discussed in section 4.3 the Costas Loop was removed from the controller so the associated low-pass filters were not used.

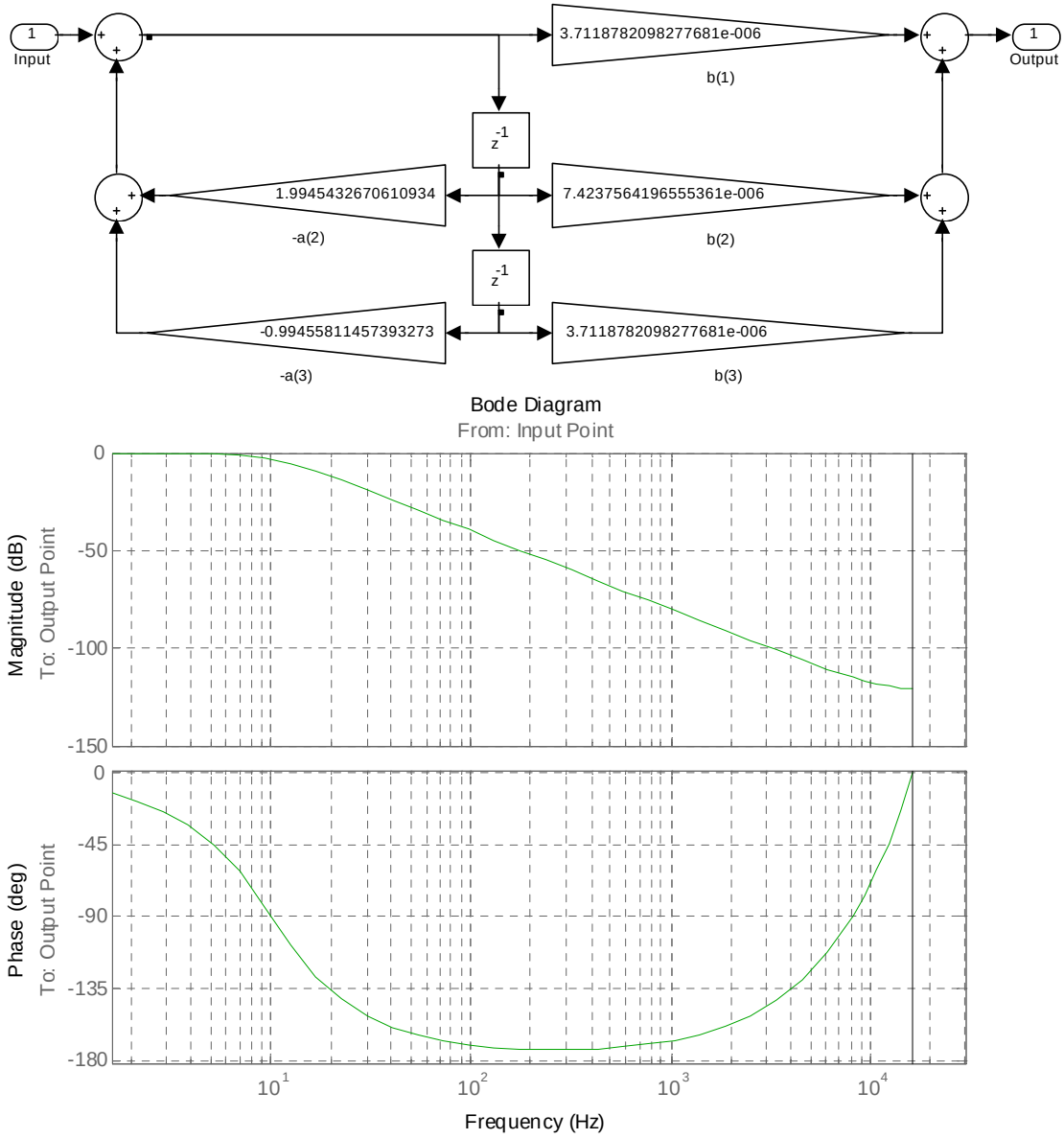


Figure 4.4. D-axis current controller low pass filter implementation and response.

4.5 Proportional Plus Integral Compensators.

The control algorithm for this system uses three proportional plus integral compensators (PI compensators). There are PI compensators in the d-axis and q-axis current controllers and there is a PI compensator controlling the DC link voltage. The coefficients (Kp and Ki) for each of the PI compensators were designed in the s-domain using the simulation of the system in Saber as described in chapter 3. After the design was complete the PI compensators were transformed into the z-domain using the bilinear transform at the sampling frequency. Upper

and lower limits control the maximum and minimum values that the PI compensators can output regardless of the input error and how long the error has existed. In order to prevent the integrators from winding up when the output is at one of the limits, the integrator memory variable is set to the difference between the calculated output of the PI loop and the limit [30]. This nonlinear method of providing anti-windup to the integrators effectively changes the gain of the integral term to prevent the integral term from winding up without completely nulling out its effects. A block diagram of the compensator in the z-domain is shown in Figure 4.5.

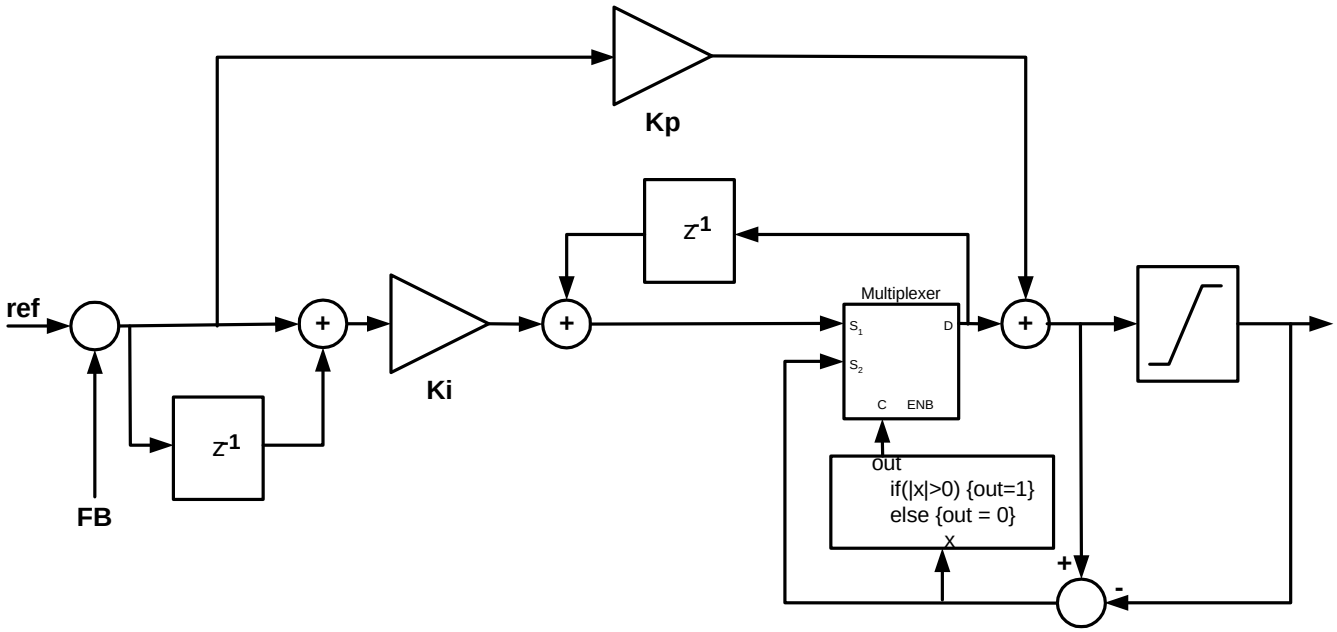


Figure 4.5. Z-domain PI compensator with non-linear anti-windup.

4.6 Space Vector Modulator.

A center aligned space vector modulation scheme is used to control the switches in the active filter power stage. The method implemented in this system has six switch transitions each switching period, looking at two IGBTs as a SPDT switch, therefore all three SPDT switches transition twice each switching period as shown in Figure 4.6. A significant effort was placed on making the SVM implementation computationally efficient in the DSP code. Control of the modulator is through the d and q axis duty cycles determined by the current control loops.

Each orthogonal duty cycle is limited to ±1, but the vector sum of the duty cycles must be limited to a magnitude less than 1. This limiting is done using equation (4.1) to ensure the angle of the control vector is not changed.

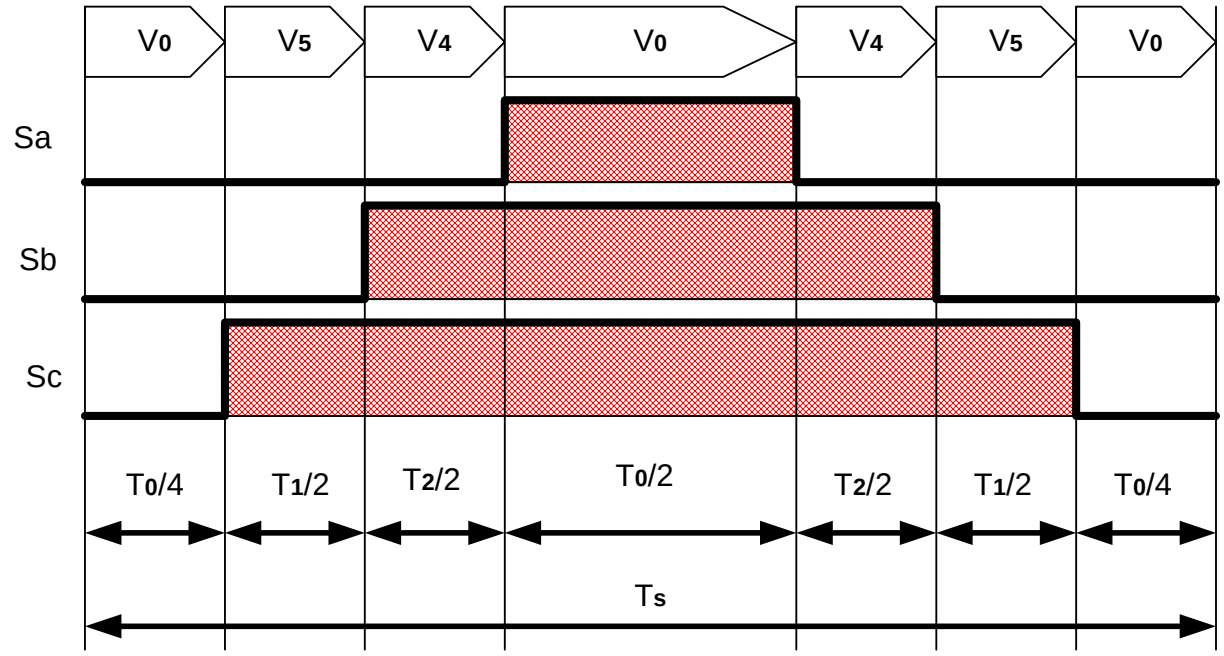
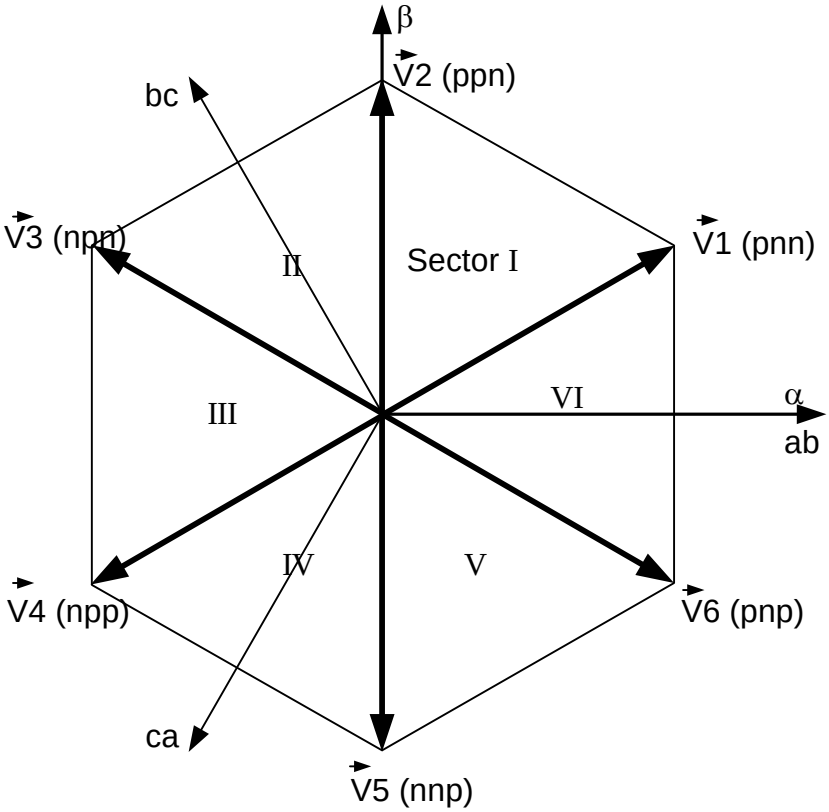


Figure 4.6. Example of one SVM switching cycle switch positions.



Vect.	ρ	θ
V1	$\sqrt{2}\cdot Vdc$	30
V2	$\sqrt{2}\cdot Vdc$	90
V3	$\sqrt{2}\cdot Vdc$	150
V4	$\sqrt{2}\cdot Vdc$	210
V5	$\sqrt{2}\cdot Vdc$	270
V6	$\sqrt{2}\cdot Vdc$	330
V0(ppp)	0	0
V0(nnn)	0	0

Figure 4.7. SVM switching vectors.

$$D_x = \frac{D_x}{\sqrt{D_d^2 + D_q^2}} \qquad (4.1)$$

To prevent doing a square root and a divide in the DSP, which both require numerous instruction cycles, a look up table of the inverse square root of 1 to $\sqrt{2}$ is used to perform (4.1). If the quantity $D_d^2 + D_q^2$ is greater than one, then it is used as the index into the lookup table. Each of the duty cycle components is multiplied by the lookup table entry to scale them back. The same lookup table method that was used for the sinusoids is used here to decrease the granularity of the table with out using an extensive amount of memory for the table.

The next step in the SVM implementation is to transform the d and q axis duty cycles into α,β quantities using the inverse Park's transform. The quadrant of the reference vector is determined using the signs of the α and β quantities. Next, the switching vectors that are used to synthesize the reference vector are determined by using ratios of the α and β lengths to determine which sector within the quadrant the reference vector is located. After the switching vectors are determined, the reference vector is projected onto each switching vector to determine the duty cycle for that switching vector. The sum of the switching vector duty cycles is subtracted from one to determine the amount of time to apply to the zero vectors. Finally, the duty cycles are converted into integer values that are sent to the pulse width modulators in the FPGA for each of the switch poles. This method does not require trigonometric functions to be carried out by the DSP. The C code for this implementation is included in Appendix B.

4.7. Pulse Width Modulator Implementation.

A pulse width modulator (PWM) that is programmed into the FPGA and was designed using schematic entry in Xilinx Foundation Software ® controls the power stage pole switches. The 16 bit registers that are used to control the PWM block are memory mapped into the DSP address space by the decoder shown in Figure 4.8. During initialization, the control code in the DSP writes an integer to the period register that sets the switching period to the value written times 120 ns. When an integer is placed in the dead time register, the dead time is set to the value written times 60 ns. The PWM control register is used to start, stop, and reset the PWM

block. Each switching cycle the control algorithm writes the duty cycles that are calculated by the SVM code to the duty cycle registers for each switch pole in multiples of 120 ns.

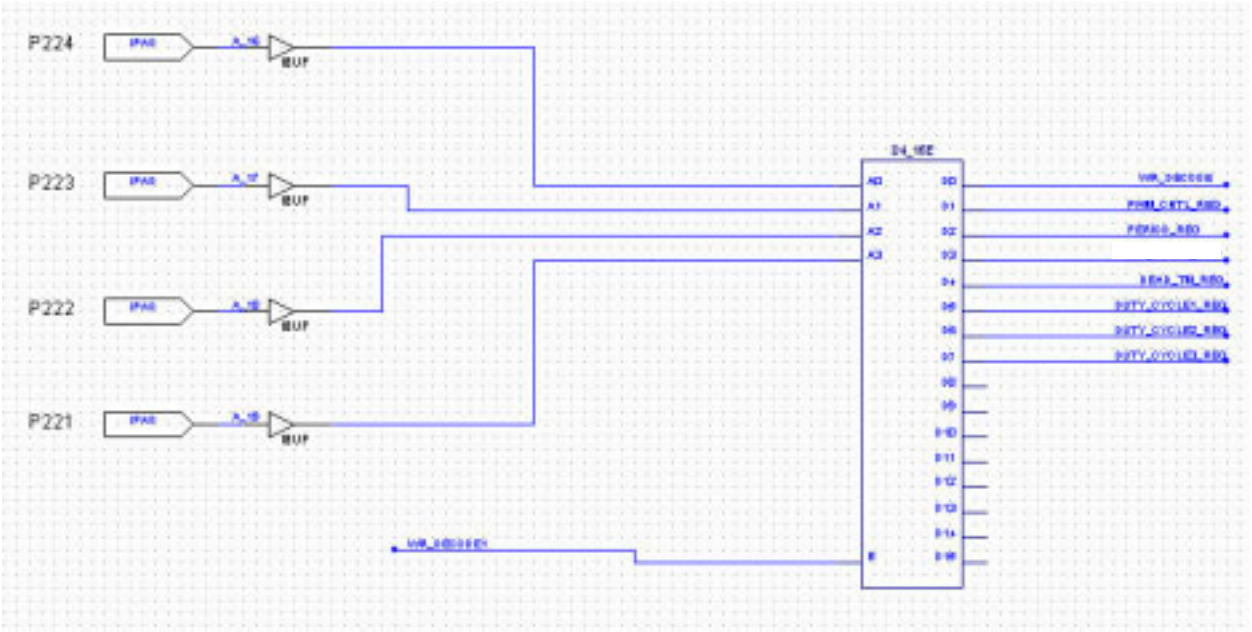


Figure 4.8. PWM control address decoder.

Figure 4.9 shows the triangle generator for the PWM control block. This block controls the switching period of the power stage switches. During initialization, the control register is manipulated to initially load the period value into the counter then the counter is started and begins counting down. When the counter reaches zero the TC output provides a pulse to the CNTR_UP flip-flop clock, which sets its output to one. The CNTR_UP signal causes the counter to begin counting up when it is high. Once the counter value becomes greater than the value held in the period register, the CNTR_UP flip-flop is cleared allowing the counter to begin counting down again. The counter value acts as a digital triangle wave and the CNTR_UP value is a square wave at the switching frequency. This block sets up the timing for the PWM described in the previous paragraph. The clock pulses to the counter are at 33.33 MHz therefore, the counter value changes every 60 ns. A switching period is defined by the counter counting up to the value in the period register and back to zero so the switching period is the value in the period register times 120 ns.

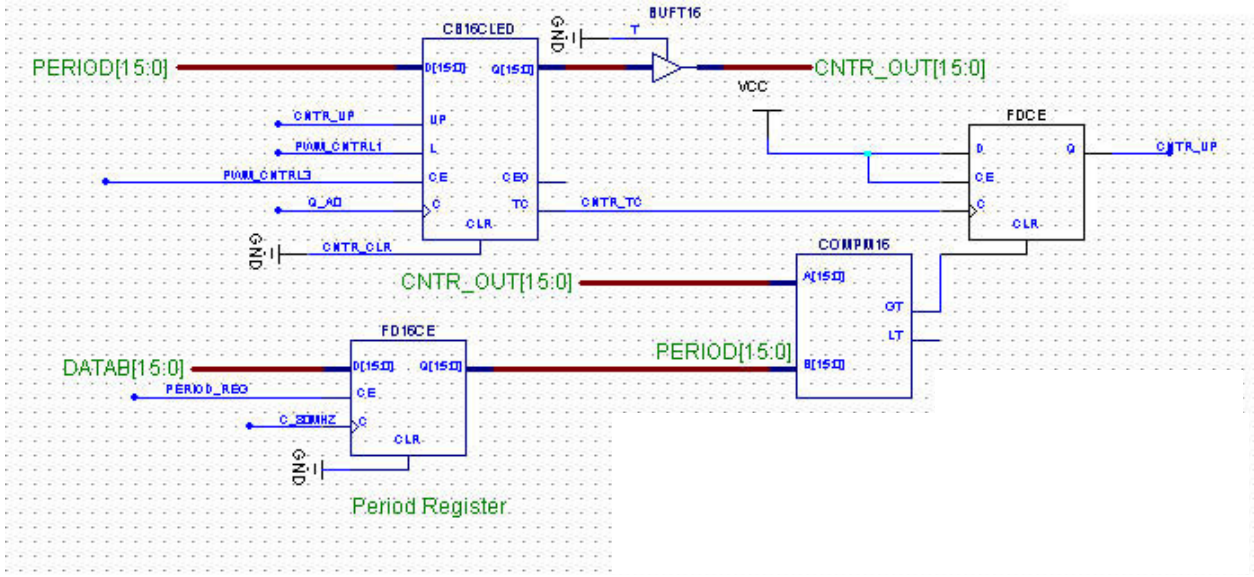


Figure 4.9. PWM digital triangle generator logic.

Figure 4.10 shows the switch controls for one pole of the three-phase power stage. The duty cycle is written to the duty cycle register by the DSP program after the control algorithm has finished running for the latest set of sampled variables. A second register is used to prevent the duty cycle that is used to control the switches from being changed in the middle of a switching period. Once the modulator triangle starts over, the CNTR_UP value clocks the new duty cycle into the second register to be compared to the counter value to change the state of the upper and lower switch in the pole. The upper switch is on while the duty cycle value is greater than the counter value. The dead time is added to the duty cycle value and the lower switch comes on after the upper switch has turned off and the dead time has expired. There are buffer flip-flops on the outputs of the switch control logic to allow for the PWM to be disabled during startup and fault conditions.

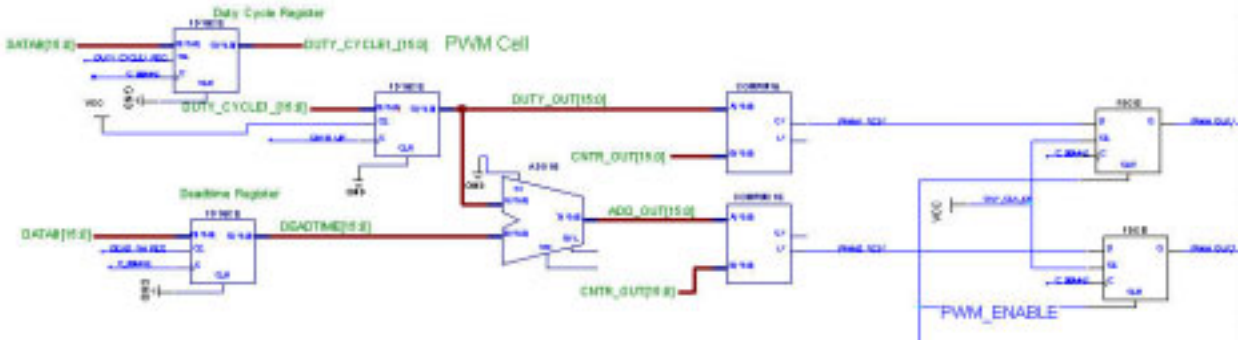


Figure 4.10. PWM switch control for one complementary pole.

The control and protection logic for the PWM generator is shown in Figure 4.11 and Figure 4.12. The PWM control register is used to control the state of the PWM generator. Bit 0 enables the PWM outputs, bit 1 causes the period value to be loaded into the counter during initialization, bit 2 resets PWM lockout from a desat fault, and bit 3 enables the clock for the counter. When a desat fault occurs on one of the gate drives, the PWM outputs are locked out.

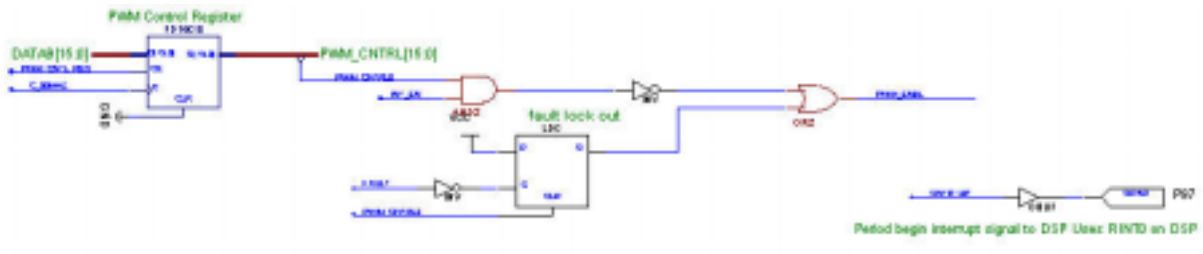


Figure 4.11. PWM control logic.

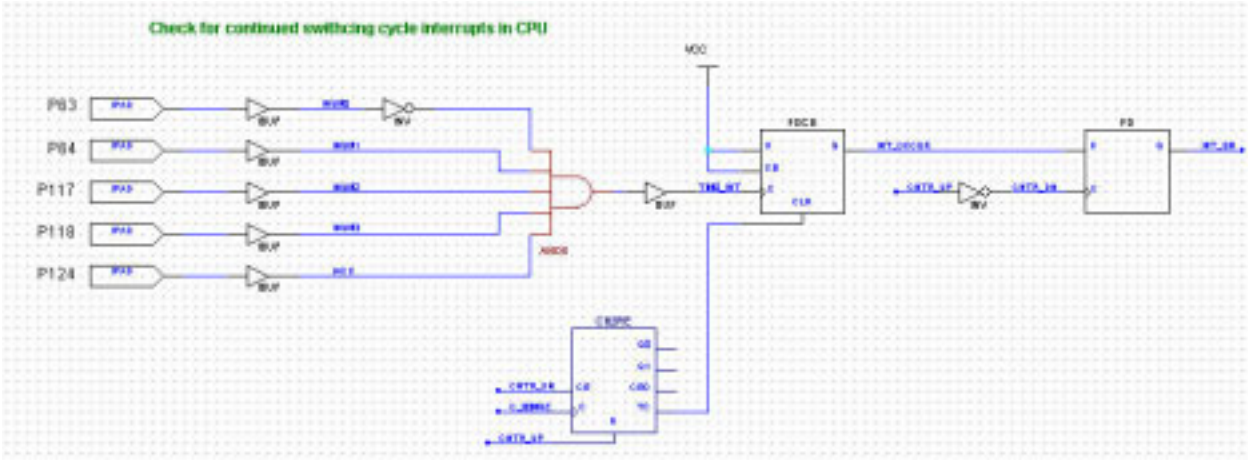


Figure 4.12. PWM watchdog interrupt logic.

The PWM outputs are also disabled if the DSP program stops responding. Each time the CNTR_UP signal transitions from low to high an interrupt is triggered in the DSP. The interrupt does not perform any tasks, but if the DSP does not service the interrupt by the next switching cycle, the logic in Figure 4.12 will lock out the PWM outputs.

4.8. Conclusions.

This chapter outlined the implementation of the control algorithms that were developed for the active filter in chapter 3.

Chapter 5. Experimental Results.

5.1. Active Filter Testing Overview.

After the hardware for the active filter was completed and debugged, several tests were carried out to determine the performance characteristics of the system. This chapter outlines the system tests and the efforts that were performed to improve the system performance. Due to the drawbacks of a stand alone active filter that have been documented in the literature and demonstrated during testing of this system, a method is proposed for designing the supplemental passive component to implement a hybrid-filtering scheme.

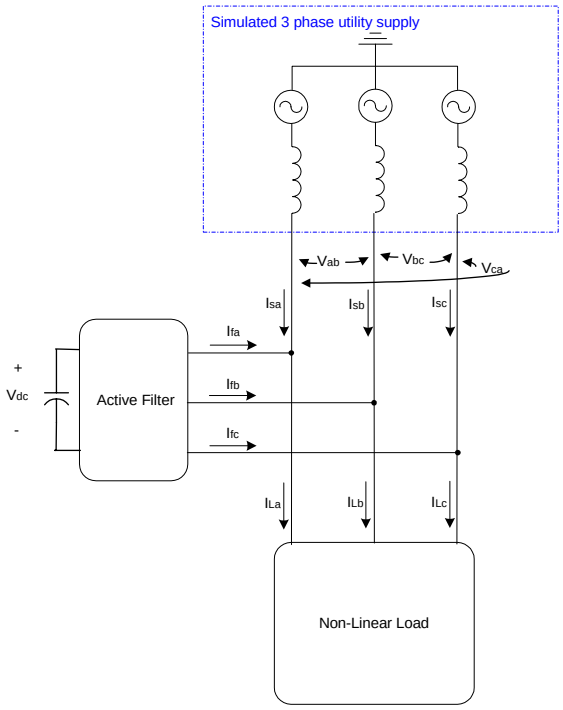


Figure 5.1. Test setup block diagram.

The test setup is shown in Figure 5.1. The non-linear load for the test setup was constructed with a Siemens three-phase full bridge rectifier module feeding an adjustable resistor bank. For safety reasons the system was not connected to the 208 V three phase utility grid. Instead, the grid connection was simulated with the 30 kW linear three phase power supply shown in Figure 5.2. Since the prototype system did not have a soft-charging feature, the power supply allowed slow charging of the DC capacitor prior to system start up. All of the

measurements on the system were performed with a Tektronix 7054 500MHz digital oscilloscope and a Tektronix handheld multimeter.

Figure 5.2. 3 phase power supply.

5.2. Initial Results.

After some hardware and software bugs were removed from the system, the system was tested under varying load conditions. Most of the tests results were recorded as screen captures on the oscilloscope measuring phase A to B voltage, phase A load current, phase A source current, and phase A active filter current. Due to an unresolved problem with the start up transient, the maximum line to line voltage that the system would operate at was 107 Vrms. The Most of the tests were run at 70 Vrms line to line so that the start up transient would not shut the system down. The simulations that were used for comparison to the actual system operation were also run at the 70 Vrms line to line conditions. Figure 5.3 shows two examples of the test results, one at 107 Vrms line to line supplying a 45 Ohm load and one at 100 Vrms line to line supplying a 10 Ohm load.

The spikes that show up in the source current occur at the times when the load current undergoes a high di/dt transient. This deficiency in the ability of the active filter to perform ideal line current compensation is discussed in detail in [31] and [32]. The authors detail the cause of the remaining distortion in the line currents as delay in the active filter control due to sensor

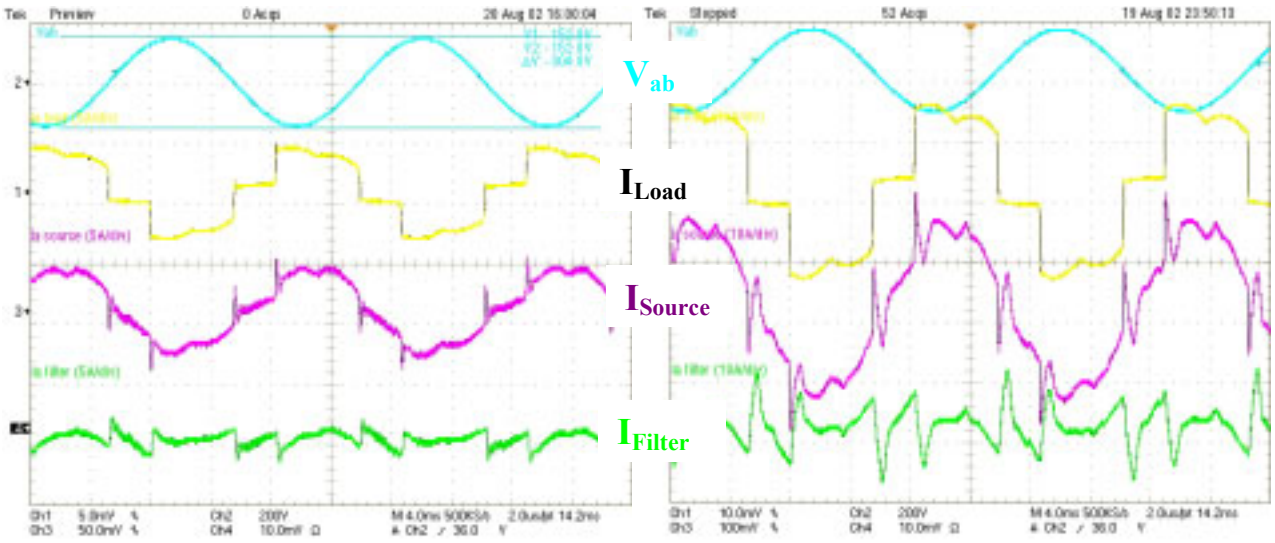


Figure 5.3. Initial test results of active filter operation.

delay, finite reference calculation time, and the dynamic limitations of the converter. Looking at the filtering limitations from a spectral content point of view, since the load current waveform contains such high di/dt sections in the time domain, the spectral content of the waveform is spread out over a wider frequency range. As discussed in [33], for symmetrical trapezoidal waves, where the rise time is much shorter than the period of the waveform, the envelope of the Fourier coefficients that make up the waveform follow the pattern shown in Figure 5.4.

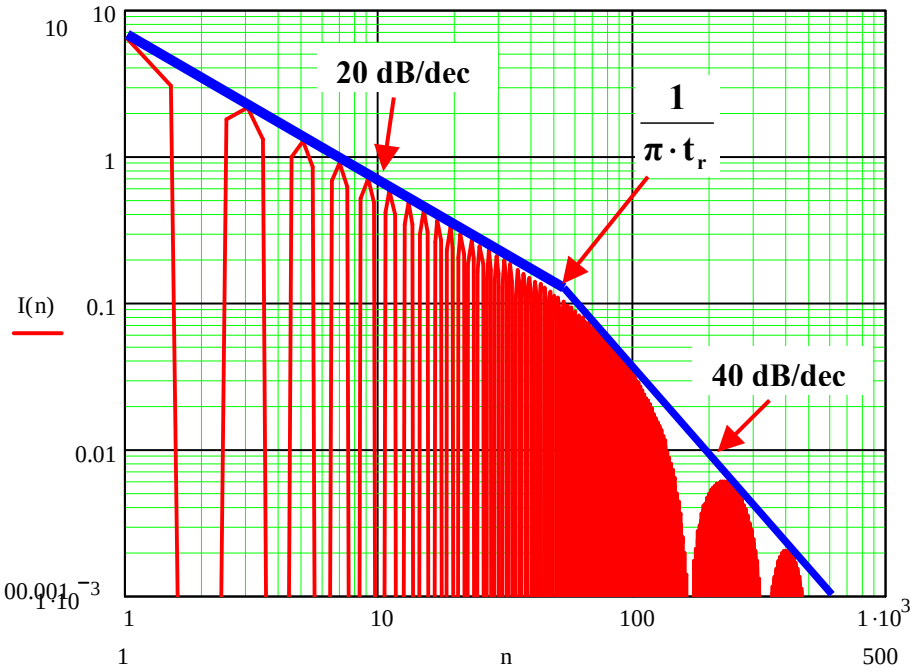


Figure 5.4. Fourier coefficeints of a trapezoidal waveform.

The dominant feature of the envelope to the Fourier coefficients is that the break from decreasing at 20 dB/dec to 40 dB/dec occurs at a frequency defined by the inverse of the rise time of the rapidly changing part of the waveform. This means that the faster the rise time of the waveform, the higher in frequency the 40 dB/dec breakpoint occurs and therefore more waveform energy is contained in higher order harmonics. The load current waveforms in Figure 5.3 have a similar Fourier coefficient envelope to the trapezoidal waveform because the high di/dt sections of the waveform dominate the current waveforms spectral content. The delay in the sensors, control system, and power stage prevents the active filter from being able to properly correct for the high order harmonics contained in the load current.

In the controller simulations discussed in chapter 3, the sensor delay and digital calculation delay were modeled by an ideal transport delay. After tests were performed on the physical system, the delay in the simulation was adjusted to more closely model the system.

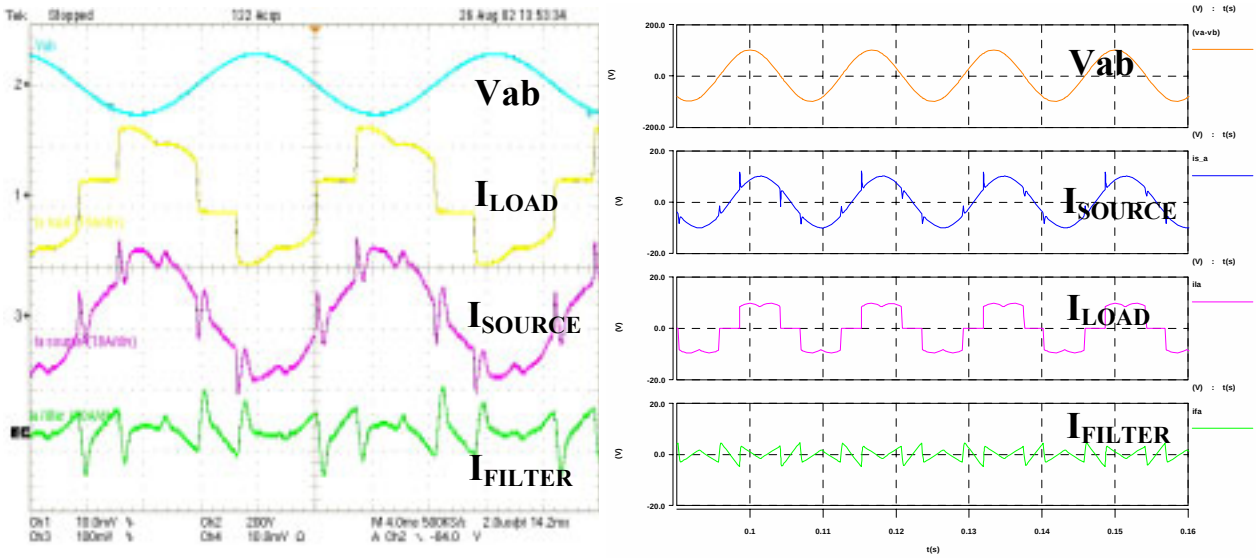


Figure 5.5. Comparison of system operation to simulation.

Figure 5.5 shows a comparison of the system operating with a 10 Ohm load at 70 V_{L-L} RMS and the simulation under the same conditions. The simulation does not have any transport delay in the control system and as can be seen in the comparison, the source current in the simulation is much cleaner and the recovery from the spikes associated with the high di/dt sections of the load current takes less time than in the actual system. Figure 5.6 shows a comparison of three simulations to the system operation where the delay in the simulation was set at 0 switching cycles, 1 switching cycle and 2 switching cycles respectively. The shape of source current

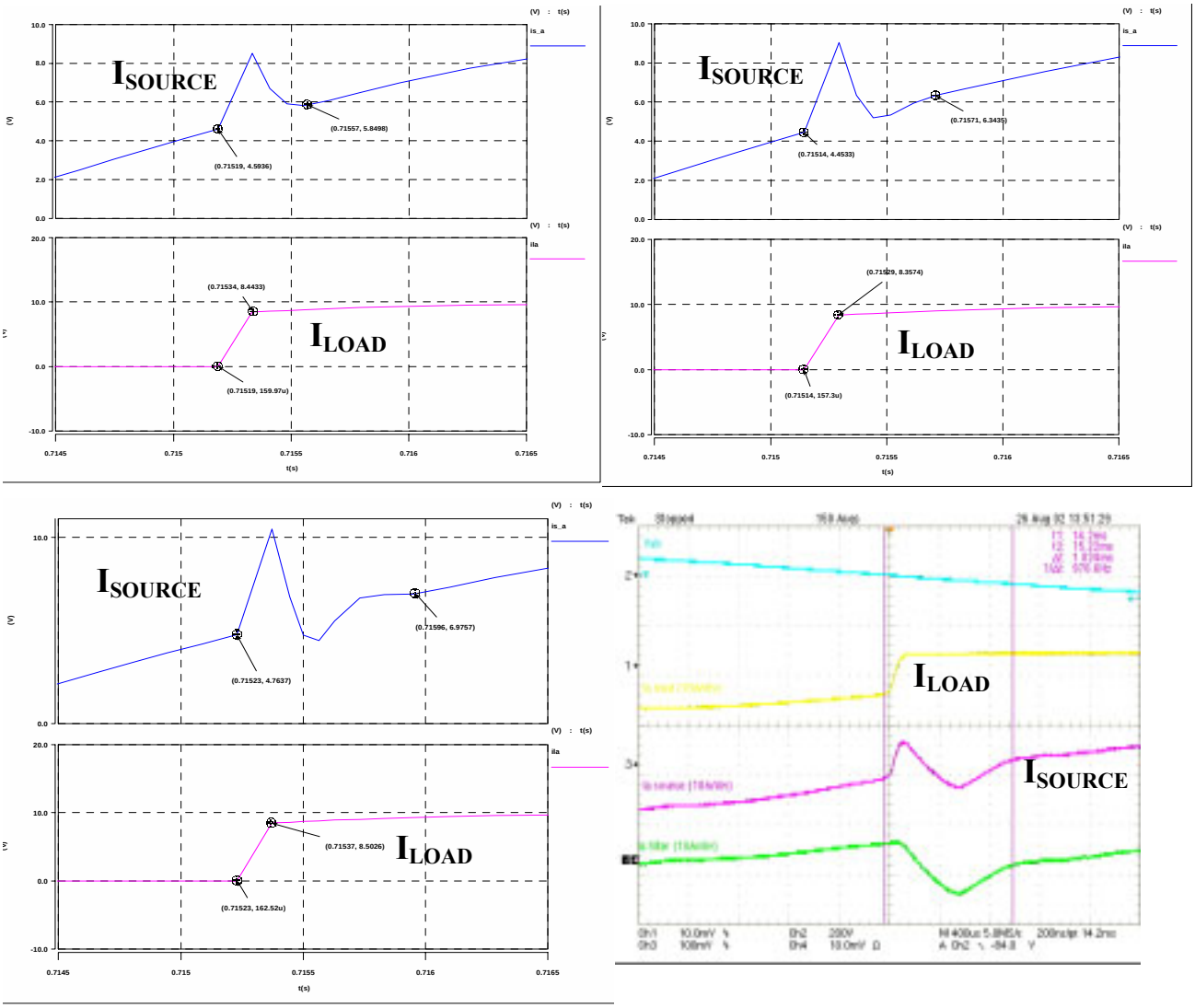


Figure 5.6. Comparison of simulations to system operation.

response to the rapid increase in load current in the oscillograph is close to the shape of the simulation with a delay time of 2 switching periods. The remaining simulations were done with the delay set to slightly below 2 switching periods.

5.3. Adding Prediction to the Controller.

The current controllers for the active filter receive the reference in the d and q axis. Figure 5.7 shows the phase A load current and the q and d axis reference signals that are calculated by the control scheme to correct for the harmonics present in the load current. The shapes of the reference signals can be looked at as a disturbance that the current controllers must follow to more accurately remove the harmonics from the system.

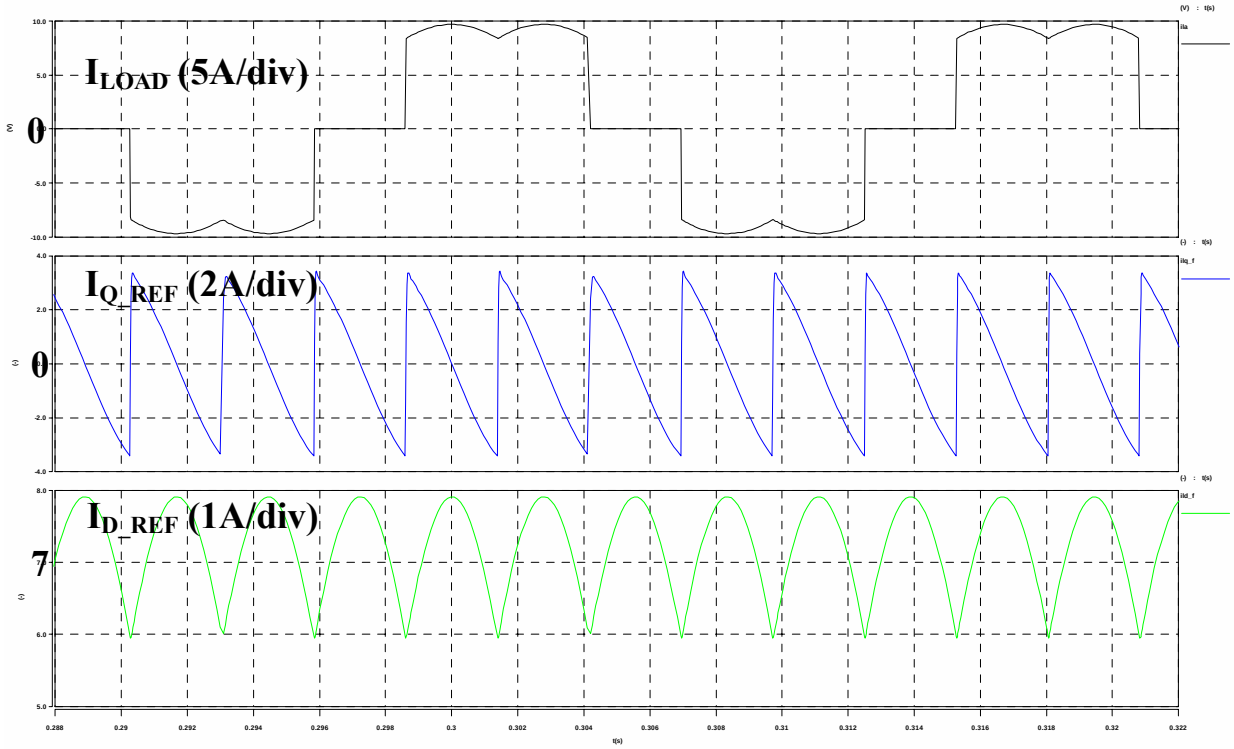


Figure 5.7. Reference signals to current controllers.

The Q axis reference contains very high rate of change disturbances six times per line cycle that coincide with the rectifier diodes turning on. A controller with extremely high bandwidth and a power stage with fast dynamic response would be required to accurately follow this rapid disturbance in the reference signal. One way of improving the active filter performance is to improve the controller response.

As discussed in section 4.2 the system variables used in the reference calculations and the feedback for the control systems were sampled at a rate of 4 times the switching frequency. In the original control implementation the first three values sampled each switching period were discarded and the last value was used for the control calculations. In an effort to improve the response of the current controllers the last 3 samples captured by the data acquisition system were used to calculate a quadratic prediction of where the measured variables were headed prior to feeding them into the reference and controller calculations. This method attempts to decrease the delay in the control system and is therefore analogous to adding zeros to the compensators in the current control loops. The quadratic prediction method used comes from Neville's algorithm which is outlined in [34]. The implementation of the quadratic prediction in the C code is shown in Appendix B. The amount of time the variables were predicted was adjusted in terms of

percentage of a switching period for the tests to find the point were the performance improved the most. Figure 5.8 shows waveforms zoomed in on a high di/dt transient response to show the effect of the quadratic prediction from 0% of a switching period to 50% of a switching period. When the prediction was increased beyond 50% of a switching period, the overshoot would become too severe and saturate the controller causing the system to shut down on over-current.

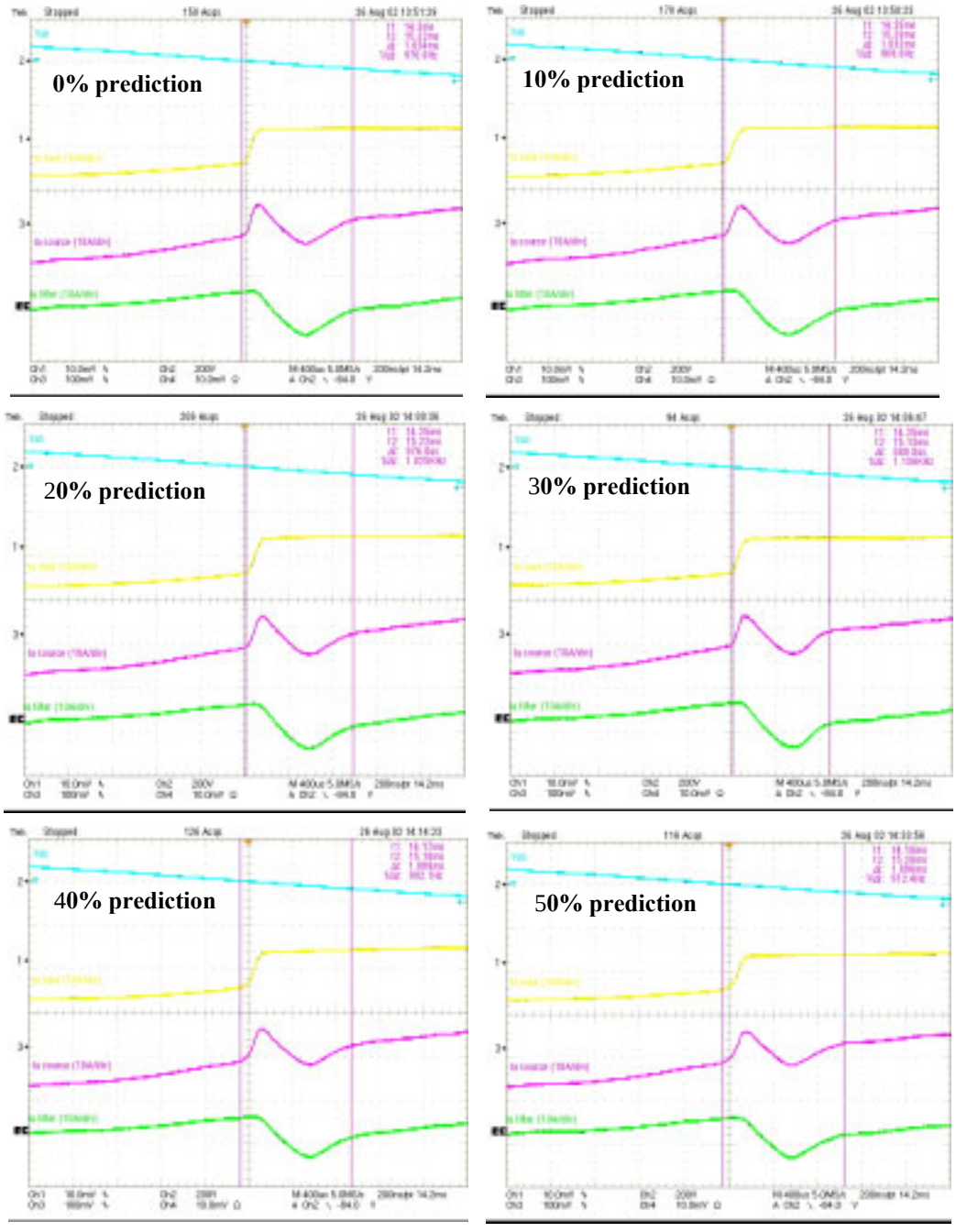


Figure 5.8. Comparison of response with quadratic predition in the controller.

From the experimental results shown in Figure 5.8 the time required for the controller to recover from the high di/dt transient decreases as the prediction amount is increased until 30% prediction and then begins to increase. Based on this empirical result, the prediction time in the controller was set to 30% of a switching period. The addition of the quadratic prediction added some improvement to the performance of the system, but other methods were then investigated to further improve the performance.

5.4. Adding Inductors at the Input of the Load.

As discussed in section 5.2 the short rise time in the load current leads to the spectral content of the current waveforms containing significant energy at higher order harmonics. Since the inherent sensor delay, calculation delay and system dynamic limitations prevent the active filter from effectively correcting for the high order harmonics, another method for improving the situation is to lengthen the rise time of the load current waveforms. As shown in equation (5.1) the frequency where the spectral content begins to drop at 40 dB/dec is inversely proportional to the rise time of the steepest feature in a trapezoidal waveform [33].

$$F_{Knee} = \frac{1}{\pi \cdot t_r} \qquad (5.1)$$

Simulations were performed to show that the load current waveforms have a similar spectral envelope to that shown in Figure 5.4. The rise time of the phase A load current with the original non-linear 10 ohm load is 10 usec as shown in the time domain simulation in Figure 5.9. From equation (5.1), the knee frequency is at 31.8 kHz. The Fourier analysis of the load current in Figure 5.10 shows that the 40 dB/dec break frequency occurs above 10 kHz. In order to slow down the load current rise time, inductors were added in series with the load rectifier on the AC side. First, in the simulation a set of three 150 uH inductors were added and the simulation results are shown in Figure 5.11 and Figure 5.12. The rise time in this case is increased to 240 μs and therefore the knee frequency is calculated to be 1.3 kHz, which closely agrees with the knee frequency shown in Figure 5.12 of around 1 kHz.

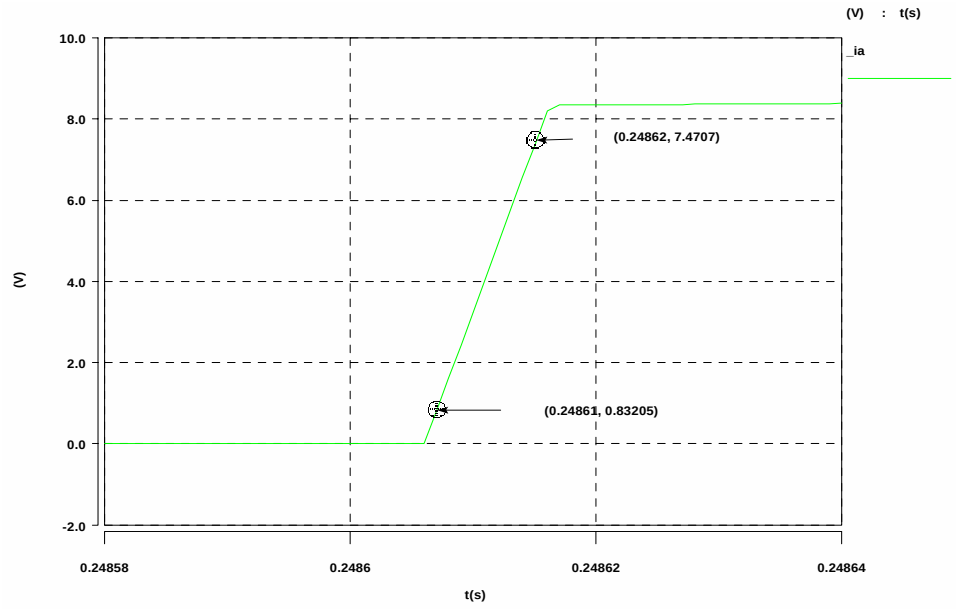


Figure 5.9. Simulation of load current rise time (rectified load).

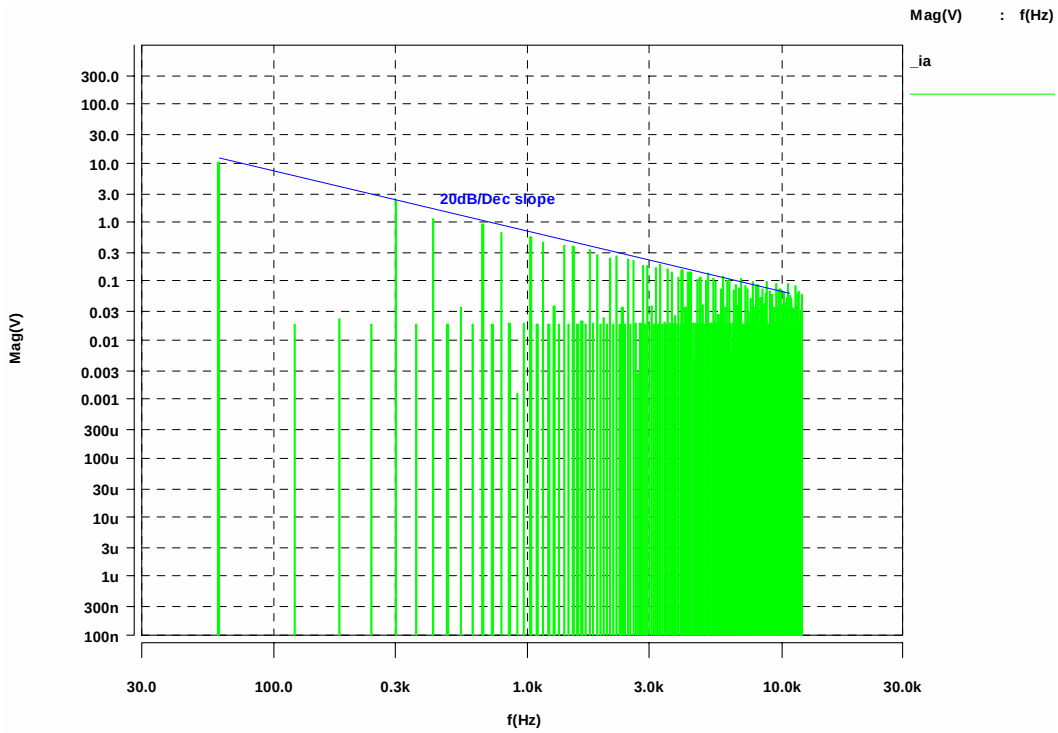


Figure 5.10. Fourier analysis of load current.

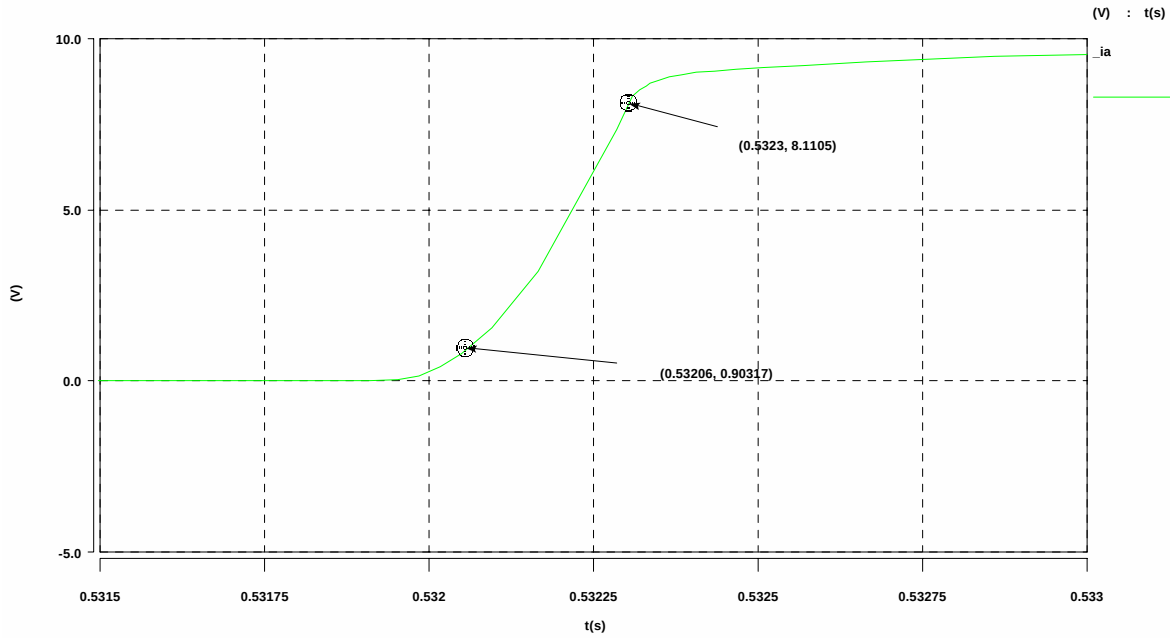


Figure 5.11. Simulation of load current rise time (150 uH inductors in series with load).

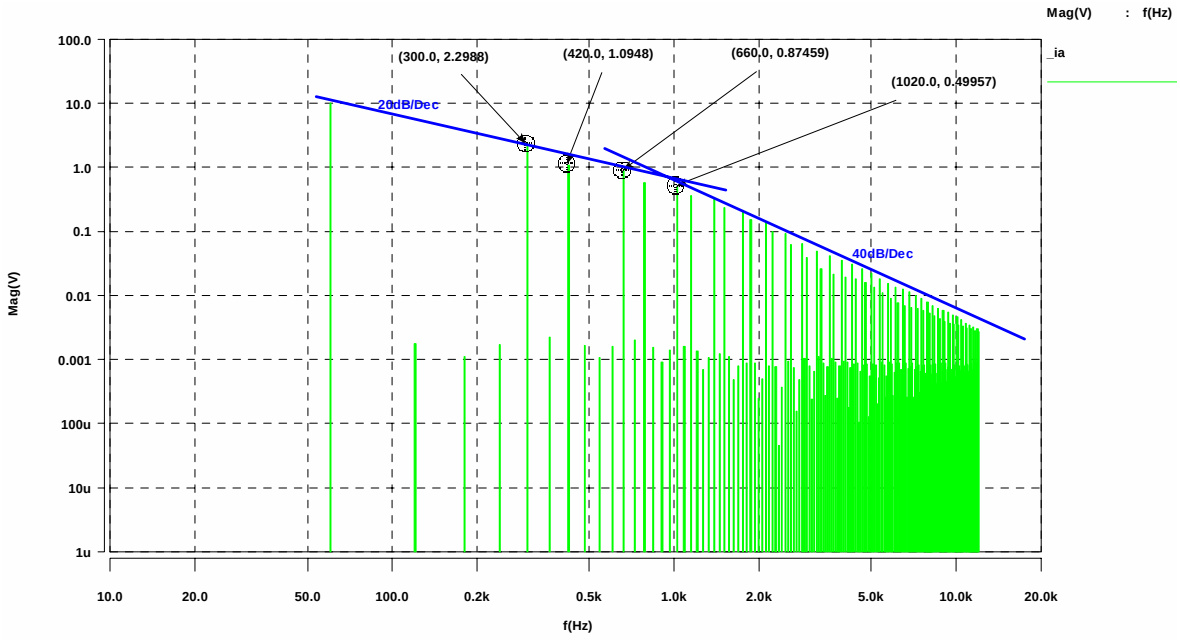


Figure 5.12. Fourier analysis of load current (150 uH inductors in series with load).

Figure 5.13 and Figure 5.14 show the simulation results with 300 uH inductors in series with the load. The rise time is 350 usec so the calculated knee frequency is 900 Hz as compared to the simulation showing around 650 Hz.

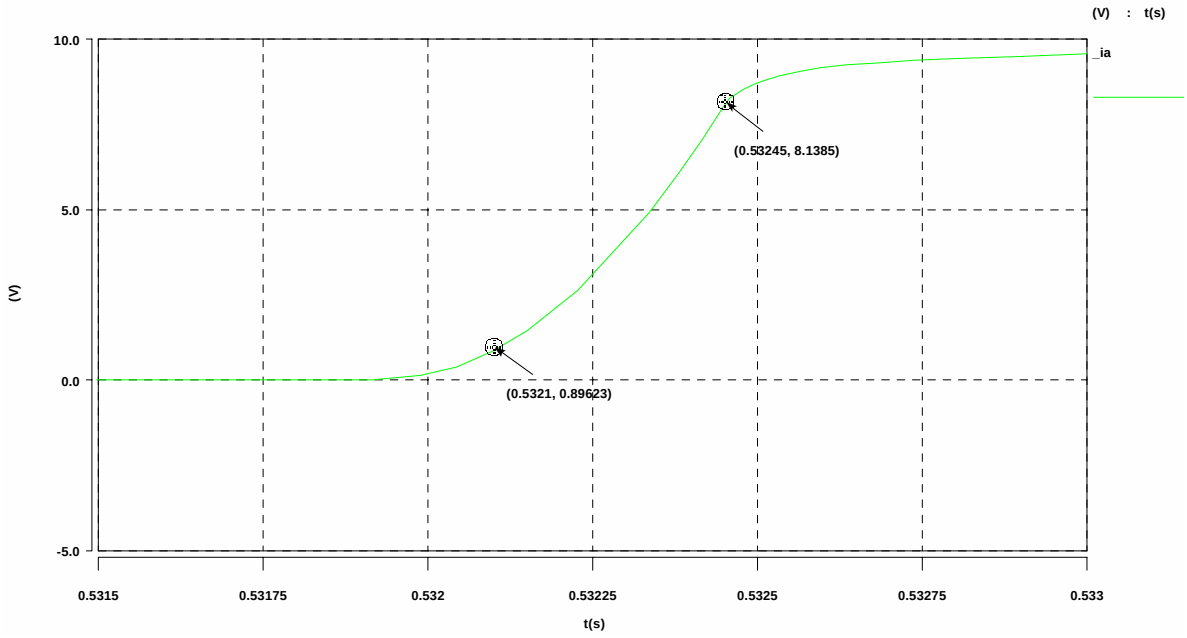


Figure 5.13. Simulation of load current rise time (300 uH inductors in series with load).

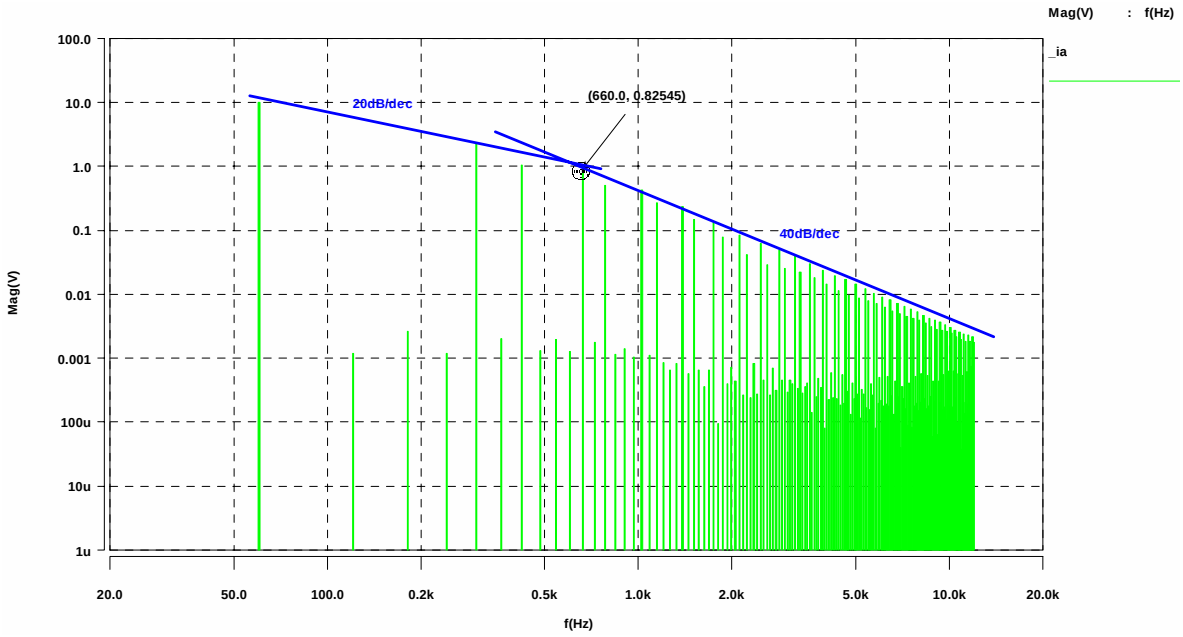


Figure 5.14. Fourier analysis of load current (300 uH inductors in series with load).

The values chosen for the inductors were base on the availability of a 150 uH and 300 uH three phase inductor set for use in the system. Figure 5.15 shows a picture of the 300 uH three-phase inductor used in the tests.

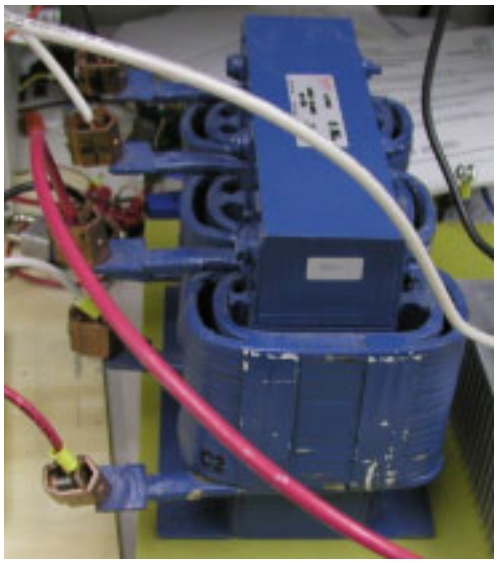


Figure 5.15. 300 uH three phase inductor.

The experimental waveforms showing the difference in the rise time for the system without the inductors and the system with the 300 uH inductors in series with the load are shown in Figure 5.16. In the case where the inductors were present the rise time was nearly 8 times as long as the case without the inductors. The load currents in each of these cases were measured with the oscilloscope and an FFT was performed on them with the results shown in Figure 5.17.

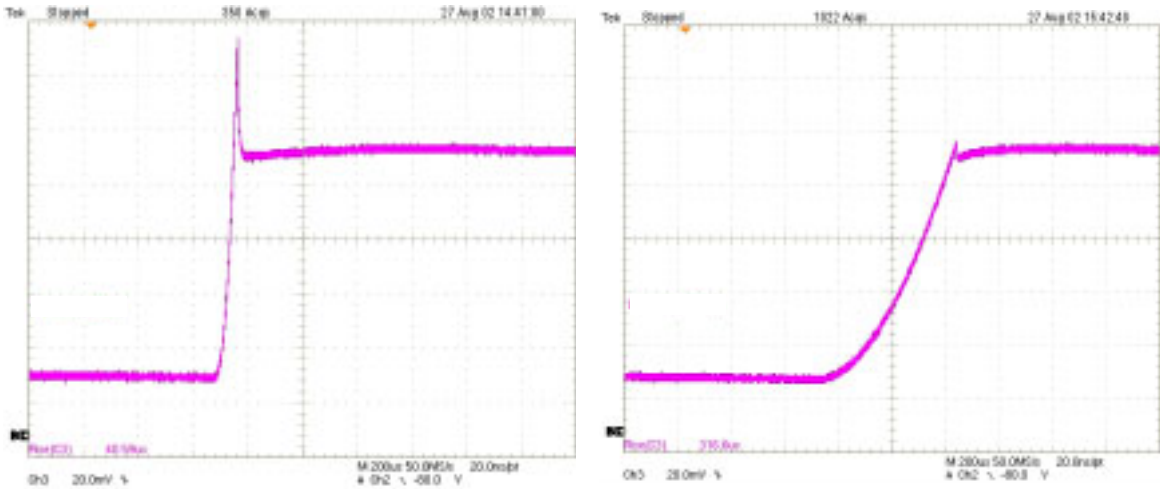


Figure 5.16. Rise time comparison of rectified load current without and with 300 uH inductors.

It can be seen in Figure 5.17 that the load current without the inductors has a knee frequency beyond the measured frequencies and the load current with the inductors has a knee frequency at about 650 Hz which agrees with the simulation results in Figure 5.14. The calculated knee

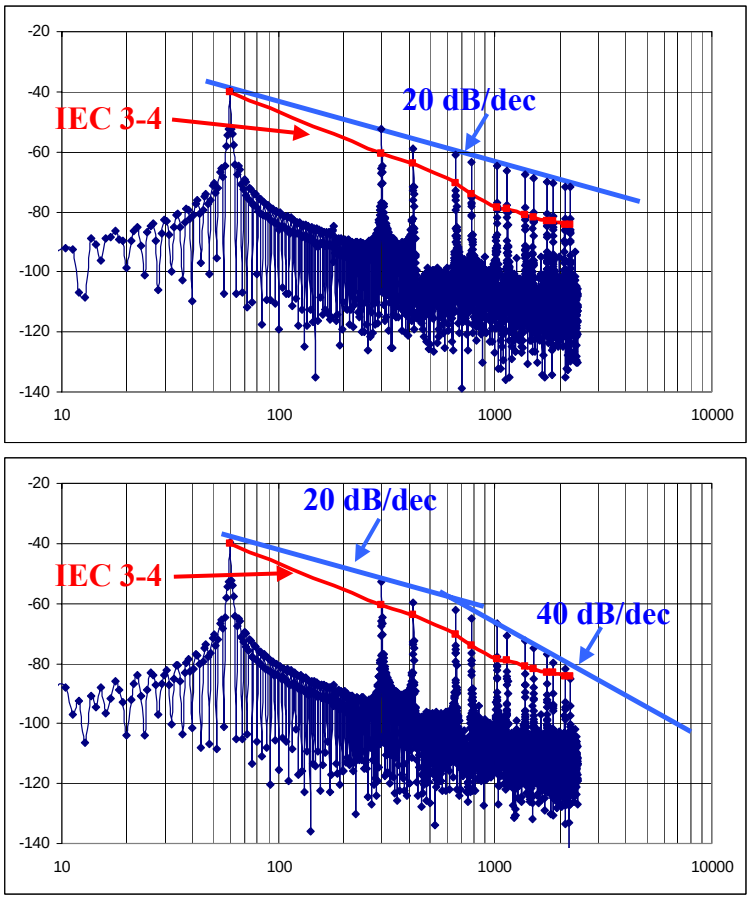


Figure 5.17. Comparison of spectral content of load current without and with 300 uH inductors.

frequency tends to be slightly higher than the measured knee frequency in both the simulations and the system measurements. This discrepancy can be attributed to equation (5.1) being developed from the Fourier analysis of a trapezoidal waveform and is thus only an approximation for the current waveforms seen by the source of this system. The approximation is still close because the high di/dt section of the waveform dominates the spectral content.

Measurements were made on the system both without and with the 300 uH inductors in series with the load and with the active filter running. The FFT of the phase A current is compared to the IEC 3-4 standard in Figure 5.18. It is obvious that the slower rise time in the load current caused by the inductors, allows the system to come closer to meeting the IEC standards. Waveforms from the system operating with the 300 uH inductors are shown in Figure 5.19, where it can be seen that the source current waveform is closer to sinusoidal than in Figure 5.5. The next section outlines a procedure for determining the size for the inductors that will allow the system to meet the IEC 3-4 standards.

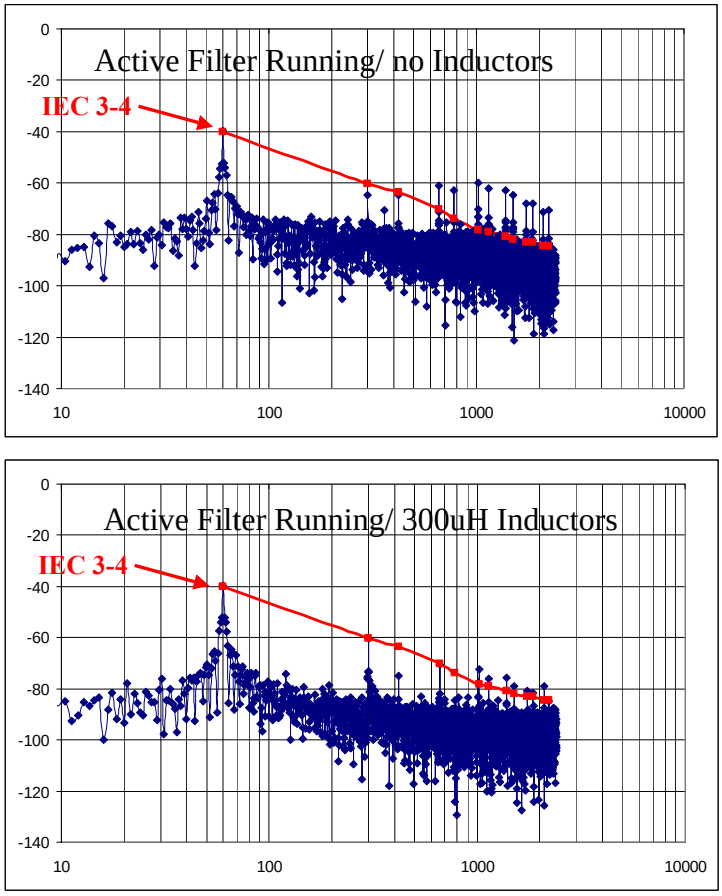


Figure 5.18. Phase A source current FFT compared to IEC 3-4.

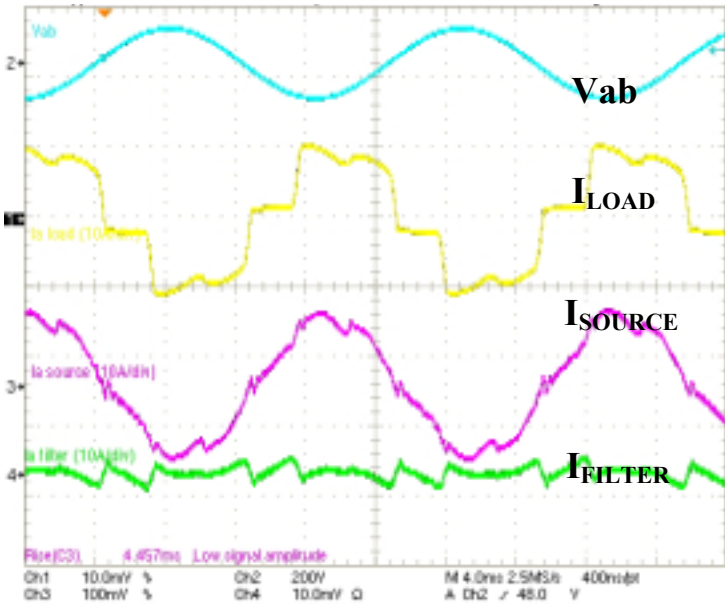


Figure 5.19. System waveforms with 300 uH inductors

5.5. Suggestions for Sizing the Inductors for a Hybrid Approach.

As discussed in the previous section, the addition of inductors in series with the load to decrease the high di/dt of the load current decreases the higher order harmonics. This section outlines a procedure for sizing the inductors based on the performance of the active filter to ensure that the system meets harmonic content standards. The IEC 3-4 standard is used in this procedure, but any standard could be used as long as the allowed magnitude at each harmonic can be expressed as a dB drop from the fundamental. This procedure is based on the EMI filter design procedure outlined in [35]. In the procedure the authors use the fact that the EMI filter has a 40 dB/dec roll off and graphically find the cutoff frequency from the difference between the measured harmonic content and the conducted EMI standards. In the procedure outlined here, the fact that the harmonic content falls off at 40 dB/dec above a frequency defined by the rise time of the current waveform.

The system simulation was used to demonstrate the procedure and is outlined here. First a simulation was run with the active filter running without any inductance added in series with the load and the Fourier analysis of the phase A source current was compared to the IEC 3-4 standard (see Figure 5.20). The active filter corrected up to the 13th harmonic to meet the standard so the inductors needed to be sized to reduce the harmonics above the 13th. Next, the difference between the harmonics and the IEC standard were increased by 3 dB and plotted as in Figure 5.21.

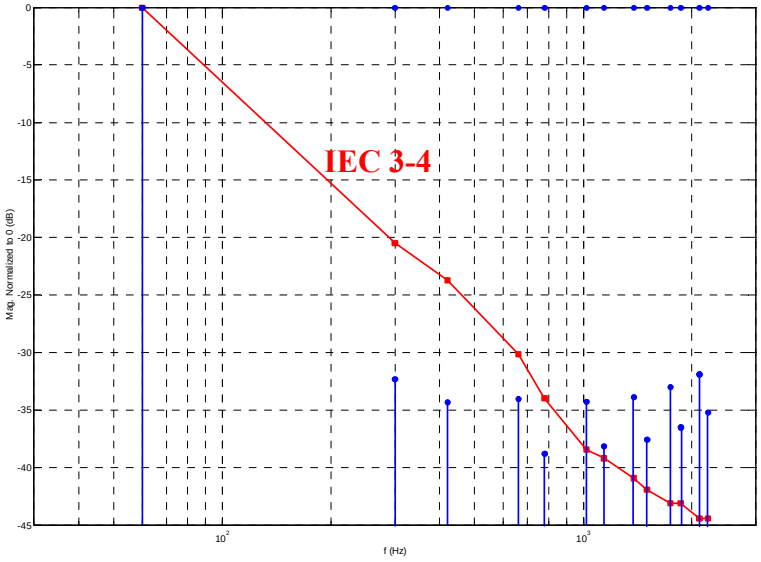


Figure 5.20. Fourier analysis of phase A source current compared to IEC 3-4.

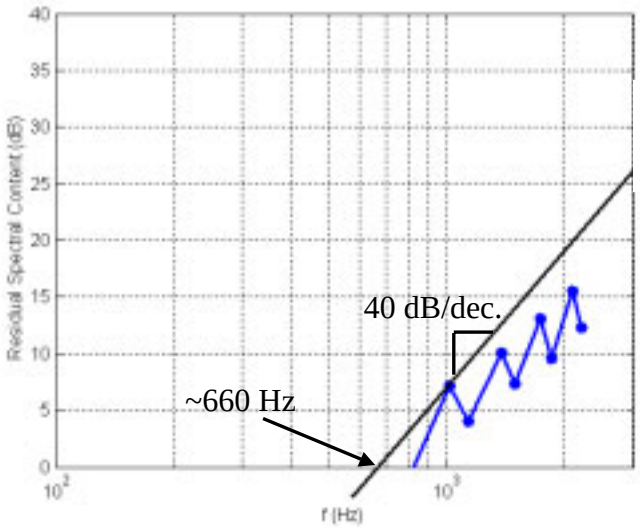


Figure 5.21. Harmonic content minus IEC standard plus 3 dB.

The 3 dB was added to give some margin to the design. Because the harmonic envelope falls off at 40 dB/dec above the knee frequency defined by (5.1), the knee frequency required to decrease the higher order harmonics below the standard can be determined graphically with a 40 dB/dec line. In Figure 5.21, the 40 dB/dec line was moved until it touched the graph of the residual harmonics. The frequency where the 40 dB/dec line crosses the ordinate was then used with (5.1) to calculate the rise time of the high di/dt section of the load current.

$$t_r = \frac{1}{\pi \cdot F_{Knee}} = \frac{1}{\pi \cdot 660} = 480\mu s \qquad (5.2)$$

Using the model of the load, the inductance value was adjusted until the rise time of the high di/dt section of the load current was 480 μs as shown in Figure 5.22. This rise time occurred when the inductance in each leg of the input to the load rectifier was at 500 μH. Figure 5.23 shows the FFT of the phase A load current with the 500 μH inductors in series with the load, where the envelope knee frequency occurs slightly above 500 Hz. As discussed in the previous section, the knee frequency occurs slightly below the frequency predicted by (5.1). Finally, the system was simulated with the active filter running and the 500 μH inductors in the AC side of the load, with the results shown in Figure 5.24.

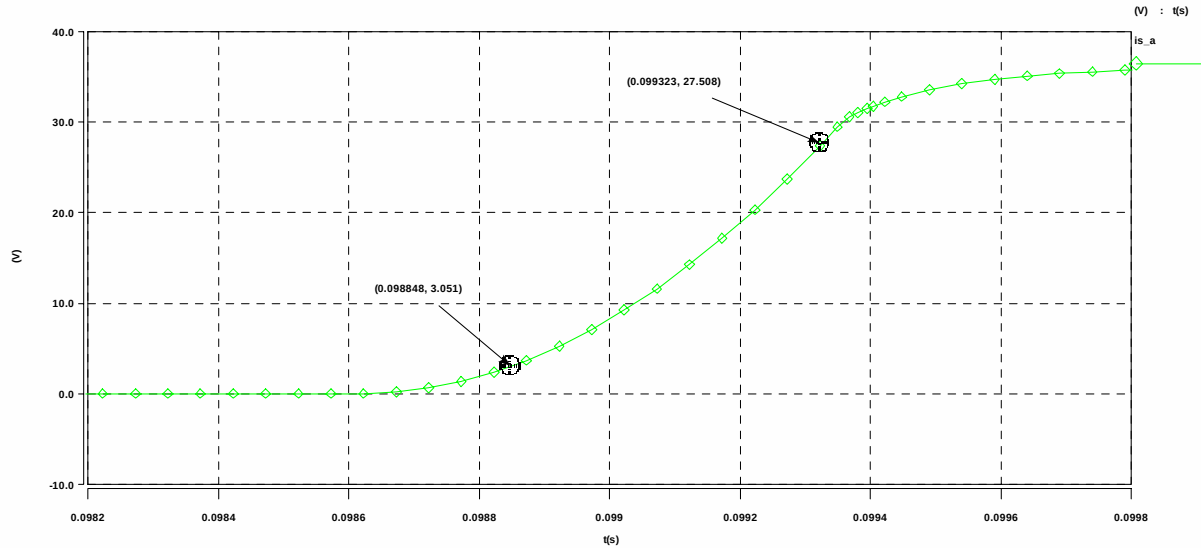


Figure 5.22. Load current rise time with 500 uH inductors.

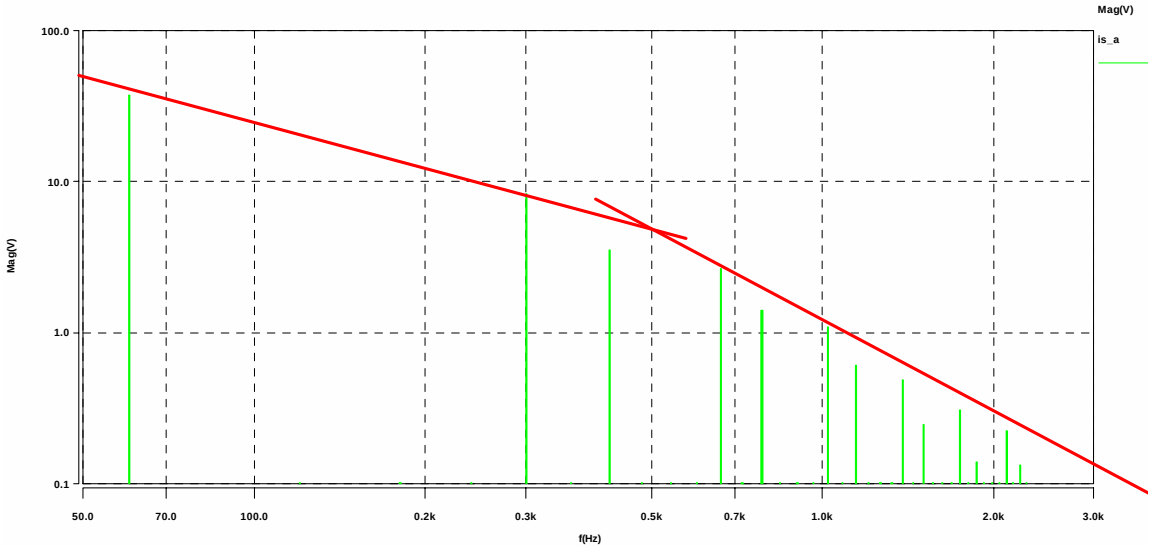


Figure 5.23. FFT of phase A load current with 500 uH inductor in series.

From the simulation results it can be seen that the IEC 3-4 standards are met. As expected from the graphical analysis in Figure 5.21, the 17th harmonic at 1020 Hz is the closest to the standard because the 40 dB/dec line used to size the inductors touches the 17th harmonic. Simulation shows that the procedure is successful at properly sizing the inductors to meet the standard requirements.

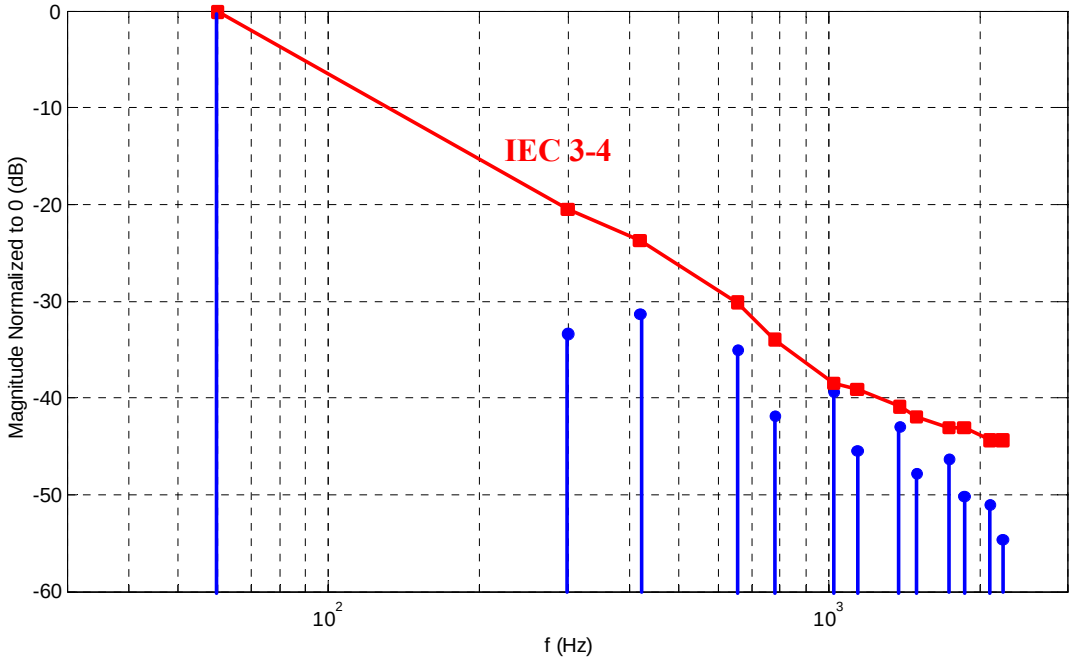


Figure 5.24. FFT of phase A current with filter running and 500 uH inductors.

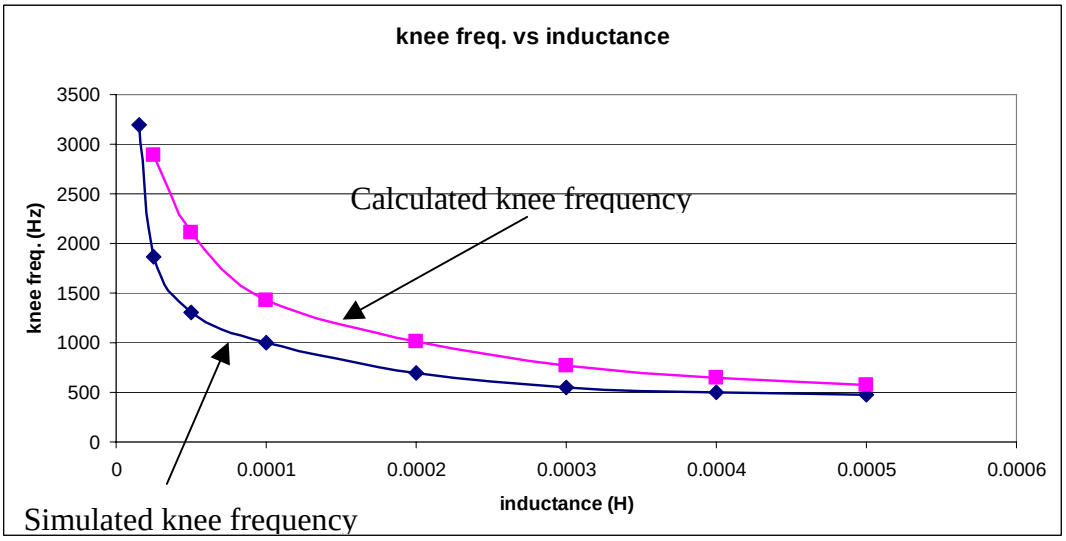


Figure 5.25. Knee frequency vs. inductance.

To show that the knee frequency of the current waveform follows the approximation given by equation (5.1), the knee frequency vs. inductance which was graphically determined in the simulation is compared to the calculated knee frequency based on the current waveform rise time. The results of the comparison are shown in Figure 5.25. The graph shows that the simulated knee frequency is lower but follows a similar shape as the calculated knee frequency.

A summary of the procedure is given below:

1. If the active filter is already built and does not meet the requirements at higher harmonics, measure one source phase current and perform an FFT on the waveform. If the system has not yet been built but an accurate model of the system has been built, simulate the system with the active filter in operation and perform an FFT on one of the source phase currents.
2. Normalize the FFT results to the fundamental component.
3. Place the standard in the same scale as the normalized FFT results and subtract the standard. The positive results are the residual harmonic content.
4. Add 3 dB to the residual for a margin and plot them on a log-log scale.
5. Move a 40 dB/dec line from the left until it just touches the residual plot.
6. The point where the 40 dB/dec line crosses 0 dB is the frequency that should be used in (5.1) to find the rise time of the current waveform.
7. Using a simulation model of the load, adjust the size of the AC side load inductors until the rise time of the phase current matches the result from step 6.
8. verify the results with simulation.

This procedure relies on the approximation of the phase current waveform to a quasi-trapezoidal wave shape, which is true when the current out of the rectifier is close to DC, but as long as the current waveform into the rectifier has a high di/dt section, the approximation should be close.

This procedure has been verified with simulation, but still needs more validation through experiment. The experimental results from section 5.4 shown in Figure 5.18, where the system was tested without and with 300 μH inductors in series with the load, show that the inductors do significantly reduce the higher order harmonics. To show that the procedure is successful, the system needs to be operated with the 500 μH to ensure that the IEC 3-4 standard is actually met as predicted by the simulation.

5.6. Conclusions.

This chapter outlined the experimental tests that were performed to determine the performance of the active filter. The inability of the control system to correct for the higher order harmonic content of the load current due to delay inherent in the sensors and control system and the dynamic limitations of the converter was demonstrated. Two methods for

improving the performance were tested in the system. First, adding quadratic prediction to the reference calculations was used to improve the controller response. This method is equivalent to adding zeros to the compensators in the current loops, but because the system was oversampling the feedback variables, the prediction method was easy to implement. Some improvement to performance was realized with this method, but the high di/dt section of the load current prevented the system from adequately correcting for the higher order harmonics. The second method for improving system performance was the addition of inductors in series with the load on the AC side of the rectifier. This is the normal method for correcting for line current harmonics. The inductors slow down the rise time of the load current, which reduces the amount of harmonic energy at higher frequencies. If inductors were required for the system to meet harmonic current content standards some would argue that there is no need for the added cost and complexity of the active filter, but the active filter reduces the required size of the inductors and also has the ability to significantly improve displacement factor. Finally a method was proposed for sizing the inductors so that the system would meet the IEC 3-4 standard.

Chapter 6. Conclusions and Future Work.

6.1. Conclusions.

The research in this thesis focused on the design of a dual function system that would provide solar generation as well as harmonic and reactive compensation. The proposed control scheme for the simultaneous control of the transfer of energy from the solar array and harmonic and reactive compensation works in simulation as long as the solar array is a stiff source. In reality, when the solar array is controlled at the maximum power point the effective source impedance is high, which led to system instability in the simulation. Because of the stability problem, the solar generation part of the system has not been implemented at this time.

The implementation of the active filter hardware and control software was outlined. Once the system was built and the initial tests were performed it was demonstrated that the bandwidth of the controller limited the ability of the active filter to correct for higher order harmonic content in the load current. Some effort was placed on improving the controller performance, but as the literature points out, the inherent delays in the control system limit the performance of the active filter at higher frequency harmonics. The highest harmonic specified in the IEC 1000-3-4 standard is at 2220 Hz, and in order for an active filter to properly compensate for energy at this frequency, its control bandwidth would have to be significantly higher than this frequency. At higher power levels, bandwidths this high are presently unattainable.

A set of three phase inductors were placed in series with the load on the AC side to limit the rise time of the current, which effectively reduces the spectral energy at higher harmonics. Some arguments could be made that if the active filter must be supplemented by passive compensation to meet the harmonic pollution standards then why expend the effort and cost of using the active filter. The advantages of using the active filter is that the dynamic control of the active filter adjusts the compensation based on the harmonic content at the lower order harmonics where the majority of the energy is concentrated. Also, the active filter can improve the displacement factor, while the inductors alone would degrade the displacement factor in most situations. A procedure was developed for sizing the inductors based on the harmonic content of the load current.

6.2. Future Work.

As discussed in the last section, the proposed control scheme that simultaneously controlled the solar array and the active filter was unsuccessful due to the high effective source impedance of the solar array. The analysis of the system done for this work was not mathematically rigorous, so the interactions between all of the subsystems are not fully understood. The state equations of the system need to be developed to allow a more rigorous analysis of the system behavior. One possible solution for the stability problem is to find a DC/DC topology that would effectively buffer the high source impedance from the input to the inverter section. This may be accomplished by adding a small storage element between the array and the DC/DC converter.

The average model used for the design and comparisons in this work provides a close approximation to the behavior of the real system, so the verification of the inductor sizing procedure through simulation is promising. To gain more confidence in the results of the procedure, some experimental verification needs to be performed.

Appendix A. PV array model

The listing of the PV array model Saber Mast file is given below.

```
#####################################################################
#   PV_array  a model for simulating a PV array
#
#     Takes the output voltage and current as well as solar
#     irradiation and ambient temperature as inputs
#     gives the cell current as the output
#
#####################################################################

template PV_array Vout Ipv test Iout = Rsc,C2,C3,Vctho,m,Ga,Ta

#################################
# Global Variables
#################################
number m = undef
number Rsc = undef
number C2 = undef
number C3 = undef
number Vctho = undef
number Ga = 1000
number Ta = 28

input nu Vout,Ipv

output nu test,Iout

#################################
# Code Block
#################################
{

val nu Nsm,Npm,ec,k,Pcmax,Vcoco,Icsco,Tcco,Gao
val nu C1,Icsc,Tc,Vcoc,Vcth,lnarg,V


#################################
# Calculate required Constants
#################################
values {
            Icsc = 6.3
            V = 56
            Nsm = 108
            Npm = 3
            ec = 1.602177E-19
            k = 1.380658E-23
            Pcmax = 2.778
            Vcoco = 0.611
            Icsco = 6.3
            Tcco = 27
            Gao = 1000
            C1 = Icsco/Gao
            Icsc = C1*Ga
```

```
            Tc = Ta + C2*Ga
            Vcoc = Vcoco + C3*(Tc - Tcco)
            Vcth = (m*k*(273+Tc))/ec
            lnarg = (1-(Ipv/(Npm*Icsc)))
            if(lnarg <= 0) {
                  lnarg = 0.001
                  }
            V = Nsm*Vcth*ln(lnarg)+Vcoc*Nsm-Ipv*Rsc*Nsm/Npm

      }


equations {


      test = lnarg
      Iout = V
}
}
```

Appendix B. Controller Algorithm Code Listing.

```
/*
*************************************************************************
*****
*  Control system constants and variables
*
*************************************************************************
********/
/* Control loop start flag */
int control_flag = 0;
/*  Sine table values */
const int table_length = 1024;                  /* Sine table length */
/* Anti-aliasing filter coefficients */


/* A/D Scaling values and offsets*/
const float VDCscale = 0.1364864;
const float VABscale = 0.1863949;
const float VBCscale = 0.1859921;
const float ILAscale = 0.0263212;
const float ILBscale = 0.0268025;
const float IFAscale = 0.0266357;
const float IFBscale = 0.0269623;
const int VDCreverse = 4096;        /* used to change sign of DC value */
const int VDCoffset = 317;
const int VABoffset = 2004;
const int VBCoffset = 1982;
const int ILAoffset = 1949;
const int ILBoffset = 1964;
const int IFAoffset = 1954;
const int IFBoffset = 1969;

/*  PLL constants  */
const float alpha_pll = .00005;
const float beta_pll = .00000002;         /* PLL control loop coefficients */


/* Control loop constants */
const float sqrt_2_3 = 0.816496580927726032;  /* sqrt(2/3) */
const float one_third = 0.33333333; /* 1/3 */

/*  d-axis low pass filter coefficients */
const float dfilt_a2 = -1.99454326706109;
const float dfilt_a3 = 0.99455811457393;
const float dfilt_b1 = 3.7118782098278E-6;
const float dfilt_b2 = 7.4237564196555E-6;
/* coefficient b3 = b1 */

/* PI controller coefficients */
/*Id and Iq controller coefficients */
const float Idq_KI = 3.838E-6;
const float Idq_KP = 40;

/* Inverter Vdc controller coefficients */
/* Pre-filter coefficients */
```

```
const float Vdc_filt_a2 = 0.82354823329;
const float Vdc_filt_b1 = 0.08822588335;  /* b2 is equal to b1 */

/* PI coefficients */
const float Vdc_KI = 1.535E-5;
const float Vdc_KP = 1;
const float Vdc_upper_limit = 50;
const float Vdc_lower_limit = -50;
const float Vdc_output_scale = 0.0048;

/* Inverter Id and Iq controller coefficients */

const float id_upper_limit = 70;
const float id_lower_limit = -70;
const float iq_upper_limit = 70;
const float iq_lower_limit = -70;
const float three_w_L = 0.3083787348763741;


float Vdc_ref = 100;
const float Vdc_final = 120;
/* Quadratic Predictor future time value */
const float xfuture = 2.3;  /* 2 + the number of samples to predict forward
*/
/* Sample offset used to index into sample set */
const int sample = 16;
/*const float sqrt2_3_120 = sqrt(2.0/3.0)/120.0; */

/*-------------------------------------------*/

/* SVM constants  */

const float one_sqrt3 = 0.5773502691896257645; /* 1/sqrt(3) */
const float two_sqrt3 = 1.1547005383792515290; /* 2/sqrt(3) */
const float sqrt3_2 = 0.86602540378443864676;  /* sqrt(3)/2 */
const float sqrt_3 = 1.73205080756887293527; /* sqrt(3) */
typedef unsigned short SampleRec[48];
/*****************************************************************
   switch_period_int - interrupt service routine for switching cycle
   interupt.
*****************************************************************/
extern interrupt void switch_period_int(void);

int Airak_processing_code(SampleRec sample_row) {
  int ret = 0;
/* This function implements the control algorithms for the active filter */
  static int iteration = 0;
  unsigned int j;
  static int pattern = 0x0000000f;
  static int mask = 0xf0000000;
  static float VAB = 0;             /* Used for initial debugging */
  static int long_index = 0;
  static int lower_index = 0;
  static int upper_index = 0; /* Sine table index values */
  static float cos = 0;             /* Cosine holding variable */
  static float negsin = 0;          /* negative sine holding variable */
  static float sin = 0;         /* dq0 transformation sinusoids */
```

```
  /*  PLL variables */

  static float theta = 0;                       /* PLL increment term  */
  static float PLLerror = 0;              /* PLL error term      */
  static float fn = 0.00185;              /* normalized frequency (first
guess)*/
  static float test=0;                     /* added for debugging */
  static int lockcount = 0;                    /* used for determining PLL
lock status */
  static int start_delay = 0;
  /* Control loop variables */
  /* Sensed values */
  float ifa = 0; float ifb = 0; float ifc = 0;
  float iLa = 0; float iLb = 0; float iLc = 0;
  float Vab = 0; float Vbc = 0; float Vca = 0;
  float ifab = 0; float ifbc = 0; float ifca = 0; /* line to line current
values */
  float iLab = 0; float iLbc = 0; float iLca = 0;
  float Vdc = 0; float VPV = 0; float IPV = 0;


  float ifalpha = 0;
  float ifbeta = 0;
  float ifd = 0;
  float ifq = 0;
  float iLalpha = 0;
  float iLbeta = 0;
  float iLd = 0;
  float iLq = 0;
  float Valpha = 0;
  float Vbeta = 0;
  static float Vd  = 0;
  static float Vq  = 0;                                        /* dq0 control
values */
  static float rec_Vdc = 0;               /*reciprocal of Vdc used in Current
controllers */
  static float Dd = 0;              /* d-axis duty cycle */
  static float Dq = 0;              /* q-axis duty cycle */


  /* d axis filter variables */
  float dfilt_e = 0;
  float dfilt_out = 0;
  static float dfilt_e_1 = 0;
  static float dfilt_e_2 = 0;

  /* Inverter DC voltage controller variables */
  /* pre-filter variables */
  float Vdc_filt_e = 0;
  static float Vdc_filt_e_1 = 0;
  /* PI_loop variables */
  float inv_Vdc_error = 0;
  static float inv_Vdc_error_1 = 0;
  float inv_Vdc_PI_out = 0;
  float inv_Vdc_command = 0;
  static float inv_Vdc_intout = 0;
  float inv_Vdc_Pout = 0;
```

```
  /* Inverter d-axis current controller variables */
  float id_ref = 0;
  float id_error = 0;
  static float id_error_1 = 0;
  float id_PI_out = 0;
  float id_command = 0;
  static float id_intout = 0;
  float id_Pout = 0;

  /* Inverter q-axis current controller variables */

  float iq_error = 0;
  static float iq_error_1 = 0;
  float iq_PI_out = 0;
  float iq_command = 0;
  static float iq_intout = 0;
  float iq_Pout = 0;

  /* SVM Variables */
  float alpha = 0;
  float beta = 0;
  int sect = 1;
  int quadrant = 0;
  float d1 = 0;
  float d2 = 0;
  float d0 = 0;
  int duty_a = 0;
  int duty_b = 0;
  int duty_c = 0;
  float rho = 0;

  /* Quadratic Predictor Variables */
  float P12 = 0;
  float P23 = 0;


  /* debug variables */
  static int test_1 = 0;
  static int test_2 = 0;
  static int test_3 = 0;

  brd_led_enable(APPL_LED);
  /* Read and scale A/D values  */
  /* DC link voltage */
  P12 = (1-xfuture)*sample_row[3] + xfuture*sample_row[3+sample];
  P23 = (2-xfuture)*sample_row[3+sample] + (xfuture-
1)*sample_row[3+2*sample];
  Vdc = 0.5*((2-xfuture)*P12 + xfuture*P23);
  Vdc = VDCreverse - Vdc;
  Vdc = Vdc - VDCoffset;
  if(Vdc < 0) { Vdc = 0; }

  Vdc = Vdc*VDCscale;


  /*if(Vdc > 550.0) { ret = 11;   Check for over voltage on DC bus
```

```
  return ret; }   */

  /* Voltage phase A to B */
  P12 = (1-xfuture)*sample_row[5] + xfuture*sample_row[5+sample];
  P23 = (2-xfuture)*sample_row[5+sample] + (xfuture-
1)*sample_row[5+2*sample];
  Vab = 0.5*((2-xfuture)*P12 + xfuture*P23);
  Vab = Vab - VABoffset;
  Vab = Vab*VABscale;


  /* Voltage phase B to C */
  P12 = (1-xfuture)*sample_row[1] + xfuture*sample_row[1+sample];
  P23 = (2-xfuture)*sample_row[1+sample] + (xfuture-
1)*sample_row[1+2*sample];
  Vbc = 0.5*((2-xfuture)*P12 + xfuture*P23);
  Vbc = Vbc - VBCoffset;
  Vbc = Vbc*VBCscale;


  /* Phase A load current */
  P12 = (1-xfuture)*sample_row[2] + xfuture*sample_row[2+sample];
  P23 = (2-xfuture)*sample_row[2+sample] + (xfuture-
1)*sample_row[2+2*sample];
  iLa = 0.5*((2-xfuture)*P12 + xfuture*P23);
  iLa = iLa - ILAoffset;
  iLa = iLa*ILAscale;


  /* Phase B load current */

  P12 = (1-xfuture)*sample_row[6] + xfuture*sample_row[6+sample];
  P23 = (2-xfuture)*sample_row[6+sample] + (xfuture-
1)*sample_row[6+2*sample];
  iLb = 0.5*((2-xfuture)*P12 + xfuture*P23);
  iLb = iLb - ILBoffset;
  iLb = iLb*ILBscale;


  /*if(iLa > 75.0 || iLa < -75){ ret = 22;  Check for overcurrent*/
 /* return ret; }
  if(iLb > 75.0 || iLb < -75){ ret = 22;  Check for overcurrent
  return ret; }     */

  /* Phase A filter current */
  P12 = (1-xfuture)*sample_row[10] + xfuture*sample_row[10+sample];
  P23 = (2-xfuture)*sample_row[10+sample] + (xfuture-
1)*sample_row[10+2*sample];
  ifa = 0.5*((2-xfuture)*P12 + xfuture*P23);
  ifa = ifa - IFAoffset;
  ifa = ifa*IFAscale;


  /* Phase B filter current */
  P12 = (1-xfuture)*sample_row[14] + xfuture*sample_row[14+sample];
  P23 = (2-xfuture)*sample_row[14+sample] + (xfuture-
1)*sample_row[14+2*sample];
```

```
  ifb = 0.5*((2-xfuture)*P12 + xfuture*P23);
  ifb = ifb - IFBoffset;
  ifb = ifb*IFBscale;


 /* if(ifa > 75.0 || ifa < -75){ ret = 33;  Check for overcurrent */
 /* return ret; }
  if(ifb > 75.0 || ifb < -75){ ret = 33;  Check for overcurrent
  return ret; }         */

  /* Calculate the third phase values */
  Vca = - Vab - Vbc;
  ifc = - ifa - ifb;
  iLc = - iLa - iLb;

  /* Calculate the line to line currents */
  ifab = one_third*(ifa - ifb);
  ifbc = one_third*(ifb - ifc);
  ifca = one_third*(ifc - ifa);
  iLab = one_third*(iLa - iLb);
  iLbc = one_third*(iLb - iLc);
  iLca = one_third*(iLc - iLa);

  /* PLL subroutine  (COSTAS LOOP)*/
  /* scale Vab to be used in costas loop */
  /*VAB = Vab*0.001;    change when testing at high voltage**********!!!!!!*/
  /*upperarm = (VAB)*cos;
  lowerarm = (VAB)*negsin;*/
  /* upper arm filter (40Hz IIR 4th order lowpass) */
  /*upperfilt_e = upperarm - armfilt_a2*upperfilt_e_1 -
armfilt_a3*upperfilt_e_2;
  filtupperarm = armfilt_b1*upperfilt_e + armfilt_b2*upperfilt_e_1 +
armfilt_b1*upperfilt_e_2;
  upperfilt_e_2 = upperfilt_e_1;
  upperfilt_e_1 = upperfilt_e;  */

  /* lower arm filter (40Hz IIR 4th order lowpass) */
  /*lowerfilt_e = lowerarm - armfilt_a2*lowerfilt_e_1 -
armfilt_a3*lowerfilt_e_2;
  filtlowerarm = armfilt_b1*lowerfilt_e + armfilt_b2*lowerfilt_e_1 +
armfilt_b1*lowerfilt_e_2;
  lowerfilt_e_2 = lowerfilt_e_1;
  lowerfilt_e_1 = lowerfilt_e;  */


  /*PLLerror = filtupperarm*filtlowerarm; */
  PLLerror = 0+Vq;
  theta = theta + alpha_pll*PLLerror + fn;
  fn = fn + beta_pll*PLLerror;
  if(theta >= 1) { theta = theta - 1; }
  long_index = (int)(1048575*theta);
  upper_index = ((long_index >> 10));
  lower_index = (long_index & (table_length-1));
  cos = sintable[upper_index] + (slope[upper_index]*lower_index);
  negsin =
sintable[(upper_index+256)&1023]+(slope[(upper_index+256)&1023]*lower_index);
  sin = -negsin;
```

```
/* End of PLL routine */
/* dq transformation on voltage used in PLL */
Valpha = sqrt_2_3*(Vab - 0.5*Vbc - 0.5*Vca);
Vbeta = sqrt_2_3*(sqrt3_2*Vbc - sqrt3_2*Vca);
Vd = Valpha*cos + Vbeta*sin;
Vq = -Valpha*sin + Vbeta*cos;

/* Check for PLL lock and correct phase if necessary */
if(control_flag == 0) {
    if(PLLerror*PLLerror < 6){ lockcount++; }
          if(lockcount > 50000) {
                if(cos > 0.7){
                      /*if(VAB < 0){
                            theta = theta + 0.5;
                            if(theta > 1){    theta = theta - 1; } */
                      control_flag = 1;

                }

          }

}
/* add additional delay to ensure lock */
if(control_flag == 1) {start_delay++;}
if(start_delay > 50000) {control_flag = 2;}
if(control_flag == 2) {
write_32b_reg(get_pwm_cntl_addr(), pwm_cntl_pwmenable);
if(Vdc_ref < Vdc_final){ Vdc_ref = Vdc_ref + 0.00001;}

/* dq transformations */
ifalpha = sqrt_2_3*(ifab - 0.5*ifbc - 0.5*ifca);
ifbeta = sqrt_2_3*(sqrt3_2*ifbc - sqrt3_2*ifca);
ifd = ifalpha*cos + ifbeta*sin;
ifq = -ifalpha*sin + ifbeta*cos;

iLalpha = sqrt_2_3*(iLab - 0.5*iLbc - 0.5*iLca);
iLbeta = sqrt_2_3*(sqrt3_2*iLbc - sqrt3_2*iLca);
iLd = iLalpha*cos + iLbeta*sin;
iLq = -iLalpha*sin + iLbeta*cos;



/* Calculate the d-axis reference current */
/* filter out the 60 hz load component */
dfilt_e = iLd - dfilt_a2*dfilt_e_1 - dfilt_a3*dfilt_e_2;
dfilt_out = dfilt_b1*dfilt_e + dfilt_b2*dfilt_e_1 + dfilt_b1*dfilt_e_2;
dfilt_e_2 = dfilt_e_1;
dfilt_e_1 = dfilt_e;
iLd = iLd - dfilt_out;

/* Inverter DC voltage  PI controller */
/* PI loop pre-filter */
Vdc_filt_e = (Vdc_ref - Vdc) + Vdc_filt_a2*Vdc_filt_e_1;
inv_Vdc_error = Vdc_filt_b1*(Vdc_filt_e + Vdc_filt_e_1);
Vdc_filt_e_1 = Vdc_filt_e;
```

```
  inv_Vdc_intout = inv_Vdc_intout + Vdc_KI*(inv_Vdc_error + inv_Vdc_error_1);
  inv_Vdc_Pout = Vdc_KP*inv_Vdc_error;
  inv_Vdc_error_1 = inv_Vdc_error;
  inv_Vdc_PI_out = inv_Vdc_intout + inv_Vdc_Pout;
  if(inv_Vdc_PI_out > Vdc_upper_limit) { inv_Vdc_intout = inv_Vdc_PI_out -
Vdc_upper_limit;

      inv_Vdc_PI_out = Vdc_upper_limit; }
  if(inv_Vdc_PI_out < Vdc_lower_limit) { inv_Vdc_intout = inv_Vdc_PI_out -
Vdc_lower_limit;

      inv_Vdc_PI_out = Vdc_lower_limit; }
            /* Scale Vdc PI controller output */
  inv_Vdc_command = Vdc_output_scale*Vdc*inv_Vdc_PI_out;
  id_ref = iLd - inv_Vdc_command;
  /* calculate the reciprocal of Vdc for use in current controllers */
  if(Vdc == 0) {rec_Vdc = 1/(Vdc+0.001);}
  else {  rec_Vdc = 1/Vdc; }

  /* Inverter d-axis  PI controller */
  id_error = id_ref - ifd;
  id_intout = id_intout + Idq_KI*(id_error + id_error_1);
  id_Pout = Idq_KP*id_error;
  id_error_1 = id_error;
  id_PI_out = id_intout + id_Pout;
  if(id_PI_out > id_upper_limit) { id_intout = id_PI_out - id_upper_limit;
                                                                  id_PI_out =
id_upper_limit; }
  if(id_PI_out < id_lower_limit) { id_intout = id_PI_out - id_lower_limit;
                                                                  id_PI_out =
id_lower_limit; }
  Dd = (Vd-(three_w_L*ifq) + id_PI_out)*rec_Vdc;
  if(Dd > 1) {Dd = 1;}
  if(Dd < -1) {Dd = -1;}

  iq_error = iLq - ifq;
  iq_intout = iq_intout + Idq_KI*(iq_error + iq_error_1);
  iq_Pout = Idq_KP*iq_error;
  iq_error_1 = iq_error;
  iq_PI_out = iq_intout + iq_Pout;
  if(iq_PI_out > iq_upper_limit) { iq_intout = iq_PI_out - iq_upper_limit;
                                                                  iq_PI_out =
iq_upper_limit; }
  if(iq_PI_out < iq_lower_limit) { iq_intout = iq_PI_out - iq_lower_limit;
                                                                  iq_PI_out =
iq_lower_limit; }
  Dq = (Vq+(three_w_L*ifd) + iq_PI_out)*rec_Vdc;
  if(Dq > 1) {Dq = 1;}
  if(Dq < -1) {Dq = -1;}
  /* SVM calculation block */


  rho = Dd*Dd+Dq*Dq;

  if(rho > 1) {
            long_index = (int)(1048575*(rho-1.0));
            upper_index = ((long_index >> 10));
```

```
            lower_index = (long_index & (table_length-1));
            rho = rsqrt_table[upper_index] +
(rsqrt_slope[upper_index]*lower_index);
            Dd = Dd*rho*0.99;
            Dq = Dq*rho*0.99;
            }
  alpha = Dd*cos - Dq*sin; /* Convert d and q commands to alpha-beta plane */
  beta = Dd*sin + Dq*cos;

  /*add alpha beta limiting code here !!!!!!!!!!!!!*/
  /* determine sector */
  if((alpha*beta) >= 0) {
            quadrant = 13; }
  else { quadrant = 24; }

  if((beta*beta) >= (one_third*(alpha*alpha))) {
            sect = 2; }
  else { sect = 1; }

  if((quadrant == 13) & (alpha > 0)) {
            if(sect == 1) {
                  sect = 1; }
            else { sect = 2;}
            }
  else if((quadrant == 13) & (alpha < 0)) {
            if(sect == 1) {
                  sect = 4; }
            else { sect = 5;}
            }
  else if((quadrant == 24) & (alpha > 0)) {
            if(sect == 1) {
                  sect = 1; }
            else { sect = 6; }
            }
  else if((quadrant == 24) & (alpha < 0)) {
            if(sect == 1) {
                  sect = 4; }
            else { sect = 3; }
            }

  /* Calculate duty cycles */
  if(sect == 1) {
            d1 = sqrt3_2*(alpha*one_sqrt3 - beta);
            d2 = sqrt3_2*(alpha*one_sqrt3 + beta);

            d0 = 1-d1-d2;
            duty_a = (int) ((d1 + d2 + 0.5*d0)*452);
            duty_b = (int) (0.5*d0*452);
            duty_c = (int) ((d1+0.5*d0)*452);
            }
  else if(sect == 2) {
            d1 = alpha;
            d2 = sqrt3_2*(beta - one_sqrt3*alpha);

            d0 = 1-d1-d2;
            duty_a = (int) ((d1 + d2 + 0.5*d0)*452);
            duty_b = (int) ((d2+0.5*d0)*452);
```

```
          duty_c = (int) (0.5*d0*452);
          }
else if(sect == 3) {
          d1 = sqrt3_2*(beta + one_sqrt3*alpha);
          d2 = (-alpha);

          d0 = 1-d1-d2;
          duty_a = (int) ((d1+0.5*d0)*452);
          duty_b = (int) ((d1+d2+0.5*d0)*452);
          duty_c = (int) (0.5*d0*452);
          }
else if(sect == 4) {
          d1 = sqrt3_2*(-alpha*one_sqrt3 + beta);
          d2 = sqrt3_2*(-alpha*one_sqrt3 - beta);

          d0 = 1-d1-d2;
          duty_a = (int) (0.5*d0*452);
          duty_b = (int) ((d1+d2+0.5*d0)*452);
          duty_c = (int) ((d2+0.5*d0)*452);
          }
else if(sect == 5) {
          d1 = (-alpha);
          d2 = sqrt3_2*(-beta + one_sqrt3*alpha);

          d0 = 1-d1-d2;
          duty_a = (int) (0.5*d0*452);
          duty_b = (int) ((d1+0.5*d0)*452);
          duty_c = (int) ((d1+d2+0.5*d0)*452);
          }
else if(sect == 6) {
          d1 = sqrt3_2*(-beta - one_sqrt3*alpha);
          d2 = alpha;

          d0 = 1-d1-d2;
          duty_a = (int) ((d2+0.5*d0)*452);
          duty_b = (int) (0.5*d0*452);
          duty_c = (int) ((d1+d2+0.5*d0)*452);
          }
     /* Added for debugging *****************/
test_1 = (int) ((0.5*Dd+0.5 )*452);
test_2 = (int) ((0.5*Dq + 0.5)*452);
write_32b_reg(get_duty_cycle1_addr(), duty_a);
write_32b_reg(get_duty_cycle2_addr(), duty_b);
write_32b_reg(get_duty_cycle3_addr(), duty_c);
}
/* saving the last row of samples */
for (j=0; j<RECLEN*2; j++)  save_data.uhword[iteration*RECLEN*2+j]
      = sample_row[j];



fpga_io_reg &= mask;
```

```
 /*   if(++iteration >= SAVE_RECORDS) ret = 55;    stops processing
!!!!Removed for testing L.L.*/
/* end of Airak code */
  return ret;
} /* end Airak_processing_code */
```

Appendix C. Sine Table and Square Root Table Generation Code.

```
% Sintable Generation Program
x=linspace(0,2*pi-2*pi/1024,1024);
Sine=sin(x);
plot(Sine)
slope(1) = (Sine(2)-Sine(1))/1024;
for i = 2:1024,
   slope(i-1)=(Sine(i)-Sine(i-1))/1024;
end
slope(1024)=(sin(0)-Sine(1024))/1024;
figure
plot(slope)
fid=fopen('C:\Saber\Sintable.txt','w');
fprintf(fid, 'const float sintable[] = { \n')
for i=1:256,

   fprintf(fid,'%1.8e, %1.8e, %1.8e, %1.8e, \n',...
      Sine((i-1)*4+1),Sine((i-1)*4+2),Sine((i-1)*4+3),...
      Sine((i-1)*4+4));
end
fprintf(fid,'};')
fclose(fid)
fid=fopen('C:\Saber\slopetable.txt','w');
fprintf(fid, 'const float slope[] = { \n')
for i=1:256,

   fprintf(fid,'%1.8e, %1.8e, %1.8e, %1.8e, \n',...
      slope((i-1)*4+1),slope((i-1)*4+2),slope((i-1)*4+3),...
      slope((i-1)*4+4));
end
fprintf(fid,'};')
```

```
fclose(fid)

% M-file to generate a text file containing the lookup table
% of the reciprocal of the square root of the numbers from
% 1 to sqrt(2).
x = linspace(1,(2-1/1024),1024);
y1 = sqrt(x);
y = 1./sqrt(x);
plot(y1);
hold
plot(y);
hold off
slope(1)=((1/sqrt(1+1/1024))-(1/sqrt(1)))/1024;
for i = 2:1024,
   slope(i-1)=(y(i)-y(i-1))/1024;
end
slope(1024) = ((1/sqrt(2)) - (y(1024)))/1024;
figure
plot(slope)
fid=fopen('C:\Saber\rsqrt_table.txt','w');
fprintf(fid, 'const float rsqrt_table[] = { \n')
for i=1:256,

   fprintf(fid,'%1.8e, %1.8e, %1.8e, %1.8e, \n', y((i-1)*4+1),y((i-1)*4+2),y((i-1)*4+3),y((i-
1)*4+4));
end
fprintf(fid,'};')
fclose(fid)
fid=fopen('C:\Saber\rsqrt_slopetable.txt','w');
fprintf(fid, 'const float rsqrt_slope[] = { \n')
for i=1:256,
```

```
    fprintf(fid,'%1.8e, %1.8e, %1.8e, %1.8e, \n', slope((i-1)*4+1),slope((i-1)*4+2),slope((i-1)*4+3),slope((i-1)*4+4));
end
fprintf(fid,'};')
fclose(fid)
```

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Vita

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