Fast Approximation Framework for Timing and Power Analysis of Ultra-Low-Voltage Circuits

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(ABSTRACT)

Ultra-Low-Voltage operation, which can be considered an extreme case of voltage scaling, can greatly reduce the power consumption of circuits. Despite the fact that Ultra-Low-Voltage operation has been proven to be very effective by several successful prototypes in recent years, there is no fast, effective, and comprehensive technique for designers to estimate power and delay of a design operating in the Ultra-Low-Voltage region. While some frameworks and mathematical models exist to estimate power or delay, certain limitations exist, such as being applicable to either power or delay, or within a certain region of transistor operation. This thesis presents a simulation framework that can quickly and accurately characterize a circuit from nominal voltage all the way down into the subthreshold region. The framework uses the nominal frequency and power of a target circuit, which can be obtained using gate-level or transistor-level simulation tools as well as normalized ring oscillator curves to predict delay and power characteristics at lower operating voltages. A specific contribution of this thesis is to introduce a weighted average method, which is a major improvement to a previously published form of this framework. Another contribution is that the amount of process variation in ULV regions of a circuit can be estimated using the proposed framework. The weighted averages framework takes into account the types of gates that are used in the circuit and critical path to give a more accurate power and timing characterization. Despite being many orders of magnitude lower than the nominal voltage, the errors are no greater than 11.27 percent for circuit delay, 16.96 percent for active energy, and 4.86 percent for leakage power for the weighted averages technique. This is in contrast to the original framework which has a maximum error of 39.75, 17.60, and 8.90 percent for circuit delay, active energy, and leakage power, respectively. To validate our framework, a detailed analysis is given in the presence of a variety of design parameters such as fanout, transistor widths, et cetera. In addition, we also validate our framework for a range of sequential benchmark circuits.

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Chapter 1

Introduction

In a vast array of applications such as battery operated smart phones with increasingly more sophisticated features, wearable computers, sensor network processors, and tiny implantable chips that monitor or otherwise aid patients, the power budget is very restricted because the system is running either on a battery or limited scavenged power. The two components of power consumption, active and leakage power, can both be reduced by reducing the supply voltage, a technique called voltage scaling. Because dynamic energy is reduced quadratically, as seen in 4.1 and leakage power is reduced exponentially, as seen in 4.4, more and more applications seek to use this technique than any other to reduce power in a circuit.

Traditional voltage scaling is limited to about half the nominal voltage, the typical voltage at which a circuit is designed to operate. The reason behind this is that some analog-like components of the circuit, such as sense-amplifiers and phase-locked-loops, do not operate properly below the transistor threshold voltage. Moreover, conventional CMOS logic faces extra challenges when operating in Ultra-Low-Voltage, or ULV, such as increased sensitivity to noise and process variation. However, in recent years, several research groups have shown that with a careful and innovative approach, it is possible to have a complete design that operates well below the threshold voltage. Among the reported prototypes are an 8-bit microprocessor operating at 232mV supply, consuming 600fJ per instruction[13], and an FFT processor with a 180mV supply, consuming 155 nJ/FFT[23].

The great power reduction of ULV operation comes at the cost of performance. The reason behind this is that the transistors are not actually switching as usual in the ULV region; instead they operate by modulating the leakage current that passes through them, which is much less than the usual "on" current. Because of the reduced speed of the circuit and the high accuracy required to measure the very small current levels, transistor level simulators such as HSpice take a long time to simulate ULV circuits. Additionally with voltage scaling, a circuit must be simulated across a range of voltages.

When deriving values for power or timing with respect to voltage, closed-form equations such

as the Shockley model are quick but inaccurate and generally only work in certain operating regions. Conversely, simulating a circuit in HSpice will yield accurate results but is time consuming and makes design-space exploration difficult. In this thesis, a simulation framework is presented that provides both a fast and accurate analysis of a gate-level design across a wide range of supply voltages, including the ULV region. The simulation framework is based on the initial framework of [6, 13, 26, 27] but includes a weighted-average methodology that greatly increases the accuracy. Additionally, the effects of process variation are considered and, by using the methodologies presented in this thesis, can be estimated in ULV as well.

The fundamental assumption of the baseline framework discussed in this thesis and [6] is that when delay/energy vs. supply voltage curves are normalized, i.e. the entire curve is divided by the value at nominal voltage, the resulting curve is independent of the underlying circuit. This means that characterizing any circuit across a range of supply voltages simply requires a normalized ring oscillator curve and the frequency or power value at nominal voltage of a target circuit. Despite its simplicity, this framework yields surprisingly accurate results: for a variety of benchmark circuits across a wide range of potential operating voltages, the maximum error was 39.75, 17.60, and 8.90 percent for circuit delay, active energy, and leakage power, respectively. In this thesis, we introduce a weighted-average method, a major improvement that yields large drops in error. With this method, a variety of normalized ring oscillator curves are constructed and are combined using a weighted-average to form a circuit-specific scaling curve. This method reduces the error to no more than 11.27 percent for circuit delay, 16.96 percent for active energy, and 4.86 percent for leakage power. To serve as a baseline, we also compare our framework to the EKV model, which is a single set of closed-form equations that model digital circuits all the way from nominal voltage to the ULV region and demonstrate that the error with our method is significantly lower.

The rest of this thesis is as follows:

- A detailed description of the methods is presented. First an overview of the original framework as well as the proposed weighted average technique is introduced. The potential pitfalls of the two methods are further discussed. Additionally, the applications of this method to account for process variation in timing analysis are also discussed.
- An analysis of the framework is shown in the presence of varying parameters such as fanout, transistor width, and critical path.
- The framework is validated by applying it to standard sequential ISCAS circuits [2]. Additionally, the techniques presented in this thesis are compared to the EKV model to further illustrate the versatility of the method proposed.
- Variations of the proposed frameworks will be presented and applied to standard ISCAS circuits to demonstrate the ease of the method while having increased accuracy.
- The framework is shown to be used to estimate the coefficient of variation of process variation of the ISCAS circuits.

- Finally, it will be shown that the measured results collected from an accurate transistor-level tool, which take several hours to obtain, are very close to the estimated results, which only take a few seconds to obtain.

Chapter 2

Background and Related Work

In recent years, attempts to reduce the supply voltage of a device without compromising performance have been made. For instance, [25] evaluates the delay between user input and computer response to determine the supply voltage range that can be used in the circuit. Another application of ULV devices can be found in [18]. This discusses the use of ULV circuits in real-time applications by finding other techniques to increase the circuit's frequency as well as maintaining circuit reliability. Additionally, [9] discusses varying the effects of voltage scaling by evaluating the device's architecture. This is in contrast to finding a single ideal reduction of supply voltage for the overall circuit because this evaluates the tasks in a given circuit, potential deadlines, as well as CPU cycles. To expand on this technique, [11] takes into account the connections between multiple chips while maintaining a dynamic voltage scaling algorithm for real-time systems.

To further take advantage of voltage scaling, applications can run in the subthreshold region. [20] suggests implementing a variable threshold voltage MOS to compensate for any additional delay that may arise as a result of subthreshold operation, rather than increasing the supply voltage. Similarly, [14] finds an optimal oxide thickness that can further reduce the power of a transistor in subthreshold regions while improving performance. A higher level approach considered can be found in [16] wherein the circuit's timing constraints are compensated for by designing the circuit's architecture for optimal performance. Another approach has been to simply create new types of FETs that are better suited to operate in subthreshold voltages rather than fine-tuning the ones that currently exist. One such device is the Double Gate MOSFET ([8]). This new FET's advantage is that it has a near-ideal subthreshold slope.

So far, idealistic circuits have been discussed, but the effects of process variation on circuits, especially those operating in ULV operation, cannot be ignored. [7] attempts to minimize that with a mathematical model that optimizes a transistor for ULV operation by taking the leakage current and delay into account. Additionally, [3] takes temperature and process variation in ULV operation into account in the voltage regulator that is designed.

It can be seen that voltage scaling is a highly sought-after power reducing technique due to the fact that the power of a circuit is quadratically and exponentially reduced for active and leakage power, respectively. To aid in designing a circuit designed to operate in ULV, one would be inclined to simulate such a circuit using an EDA tool. However, simulation tools that currently exist may take an unreasonably long time to simulate a circuit that is running in the ULV region, which makes designing such circuits more difficult. To avoid these long simulation times, mathematical models can be used. The caveat to this is that they can be cumbersome to use due to variables like threshold voltage, which are not constant and difficult to measure.

Traditionally, a separate set of equations have been used to model the transistors in each mode of operation. A transistor has three main modes of operation, depending on the voltages at the terminals and the threshold voltage of the transistor. *Cutoff Mode*, or *Subthreshold Mode*, is one in which $V_{GS} < V_{TH}$. In theory, the device would not be generating any current in this mode. In actuality, some electrons travel from the source to the drain despite the device being in the "off" mode. With *Triode Mode* and *Saturation Mode*, $V_{GS} > V_{TH}$ and the transistor is on. This means that a channel has been created so that current can flow between the source and drain [21, 24].

Some attempts at fast simulation frameworks have been made through mathematical models. One of the first models that was used was the Shockley diode equation [24]. With improvements in transistor sizing as well as the increased application of ULV devices, more specific equations have been used. However, these models only apply under specific conditions. For instance, [1] is a model for leakage current in ULV regions when transistor stacking is seen. It can be seen that the results from [1] are comparable to the results of the methodology presented in this thesis. Another mathematical model can be found in [5], which presents a model for delay in ULV regions even in variable conditions, such as process variation and transistor stacking. However, these are both mathematical models that only work in ULV regions.

Other methodologies that address the need for versatile power and timing modeling frameworks have been addressed in [10] and [19]. In [10] a modeling framework that can be used to estimate power, area, and timing for multiple core architectures is described. [19] addresses power estimations made without considering potential glitching of a circuit, which can drastically change the power estimation results of a circuit. Despite the versatility of these frameworks, the main advantage that this thesis has over frameworks such as [10] and [19] is that this thesis addresses both super and subthreshold operation of a circuit.

Lastly, the EKV Model presents an estimation technique that can eliminate the need to know which region of operation a transistor is in. By using the EKV model, a single set of equations can cover any region of operation without loss of accuracy [4]. A complete derivation can be found in [4] and an application of the EKV model to digital CMOS circuits can be found in [12]. The details of which will be covered in Chapter 5 but overall, the model's defining parameter is the Inversion Coefficient, IC, which measures the inversion of the transistor

[15]. For this thesis, this will serve as the analytical model for comparison to the frameworks presented.

The method presented in this thesis is more comprehensive in the sense that it not only provides an estimate in superthreshold and subthreshold voltage ranges, but it also provides an estimate of active energy, leakage power, critical path delay, as well as local and global process variation for circuit delay.

Chapter 3

Framework

The fundamental justification of this framework is the assumption that normalized curves for all circuits within a given technology are constant. Using this assumption, a smaller circuit, which can be easily characterized, can be used in order to represent a larger circuit's power, energy, and timing characteristics. With regards to this thesis, a ring oscillator has been used as the characterizable circuit. If normalized curves of the other ring oscillators match the curves of the baseline, then it implies that the circuits scale in the same manner and that the estimated curves of any other circuits can be derived from the baseline using only the nominal frequency and power consumption.

3.1 Basic Framework

Figure 3.1 presents the simulation framework. The idea is to characterize a ring oscillator in a circuit simulation program such as SPICE across a range of supply voltages, then normalize the resulting curves so that they can be applied to other circuits. A ring oscillator is comprised of an odd numbered chain of complimentary gates with the output connected back to the input. The frequency of oscillation is related to the delay of the gates as well as the length of the chain. As the supply voltage of the ring oscillator is reduced, the frequency of oscillation and the power consumption reduce. The supply voltage of a ring oscillator is varied from nominal voltage all the way down to the minimum operating voltage, which is in the ULV region. The resulting frequency and power curves are then normalized by dividing the curve by the value at nominal voltage. These normalized curves can then be used to determine how other circuits respond to supply voltage reduction. All that is needed to characterize an arbitrary design is a fast gate-level design analyzer such as Primetime that can collect power and delay characteristics of a circuit at nominal voltage. As shown in Figure 3.1, these numbers can then be multiplied by the normalized ring oscillator curves, producing curves that model the frequency and power consumption of a design at any voltage.

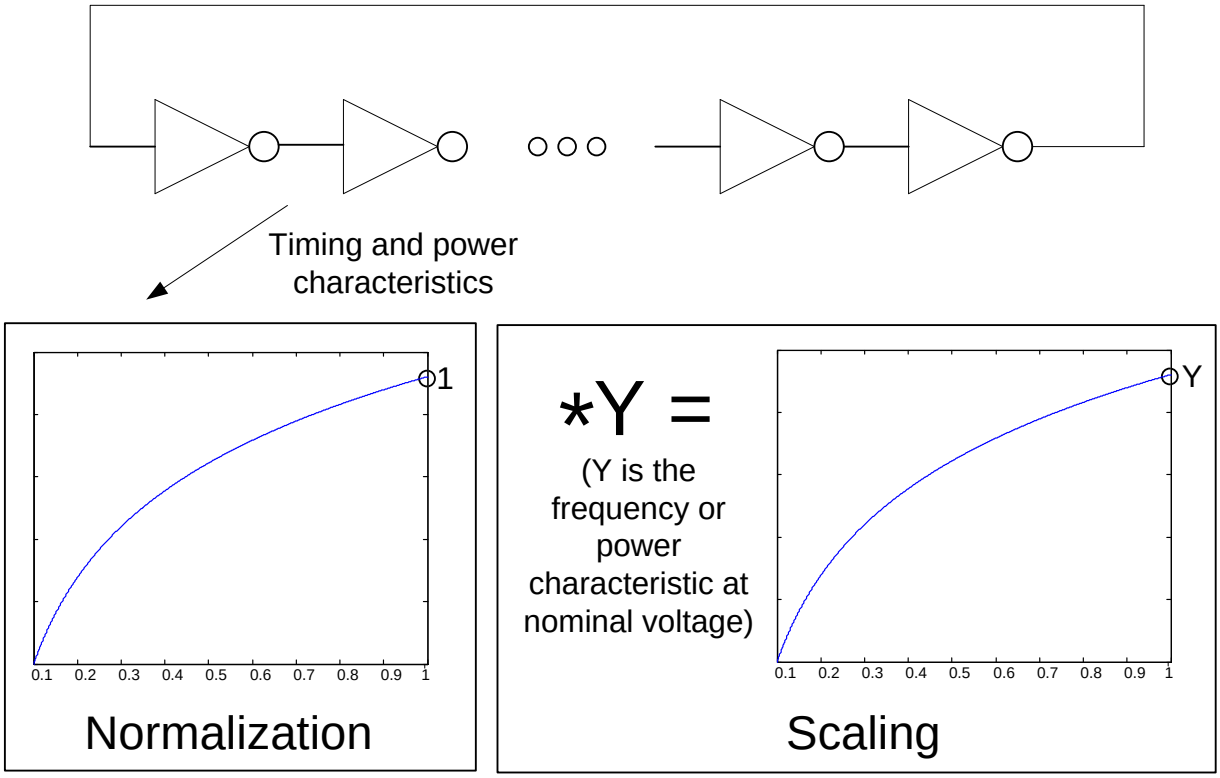

Figure 3.1: Voltage scaling characterization using a normalized ring oscillator

3.2 Weighted Average of Gates and Flip Flops

One of the benefits of the method introduced in Chapter 3.1 is that it it does not require any information about the circuit aside from the power and timing characteristic at nominal voltage. However, this also introduces error such as varying V_{TH}, W, L, et cetera, as can be seen in chapter 4. This is due to the fact that the characteristics of the target, such as the number of combinational and sequential elements of the circuit itself are not considered. Knowing such characteristics allows for a more specific analysis of the target circuit.

This methodology considers the types of components in the entire circuit or critical path when evaluating energy and power or timing, respectively. While the original technique chooses a ring oscillator to normalize, this method specifically chooses the components involved in the target circuit's standard cell library. After normalizing and scaling each component's curves, the ratio of each component found in the circuit is then multiplied to the scaled ring oscillator values to yield the new estimate. This can be seen in Figure 3.2.

Meanwhile, (3.1) shows a mathematical modeling of such an implementation. $Est(V_{DD})$ is the scaled estimation for the target circuit's power or timing values with respect to the

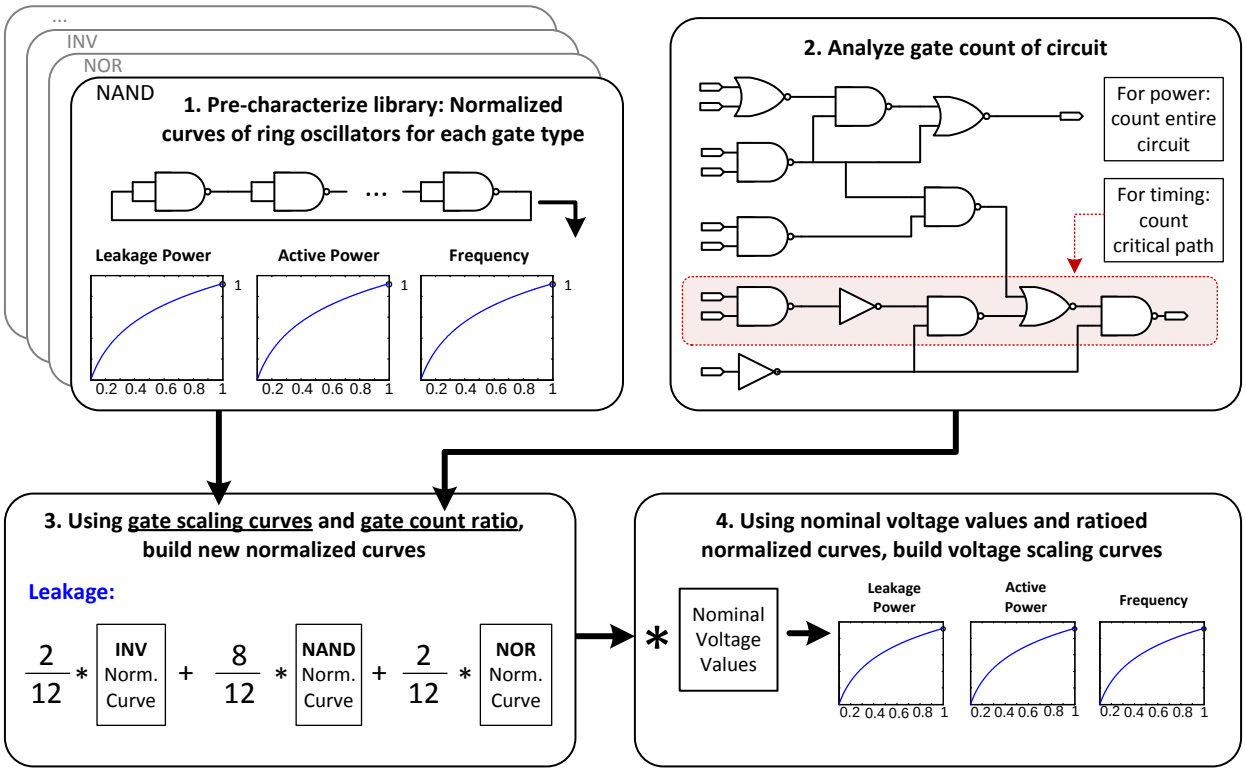

Figure 3.2: Weighted Average Methodology

different components' ratios. K_j is the number of components of type j in either the entire circuit for active energy and leakage power or the critical path for timing delay, N is the total number of components in the target circuit, $S_j(V_{DD})$ is the scaling curve of component type j, and L is the standard cell library.

$$Est(V_{DD}) = \frac{\sum_{\forall j \epsilon L} K_j S_j(V_{DD})}{N} \tag{3.1}$$

The caveat to this proposed method is that a ring oscillator of every gate in the library, or at least those being used in the target circuit, must be characterized in order for this technique to be used. However, once the characterized curves are acquired, any target circuit using that particular technology can be evaluated. This technique, despite the additional steps, is still extremely fast due to the fact that the library analysis is done once. Essentially, once the timing and power analysis of a particular library has been performed, any circuit using that technology and cell library can be quickly evaluated.

3.3 Process Variation

In the same way the base framework performes, this process uses normalization and scaling to estimate the amount of process variation that the circuit may have, which is shown in Figure 3.3. This is done by evaluating the coefficient of variation of a ring oscillator at ULV ranges. The coefficient of variation is the ratio of the standard deviation to the mean. What that means in terms of this framework is the difference in simulation results are divided by the result in the typical corner case. The reasion that the coefficient of variation is used instead of standard deviation is because the mean also changes with every V_{DD}. Therefore, standard deviation alone does not provide an accurate representation of data.

Again, the motivation for using this technique rather than simply simulating the circuit using monte carlo simulations is the time that is saved. In addition to the amount of time it takes to simulate a circuit in the ULV regions, trying to find the process variation of the same circuit would require a monte carlo analysis, which would increase the time the circuit takes to run by the number of monte carlo simulations required. Therefore, this framework has a significant advantage with regards to the time that is saved for a designer.

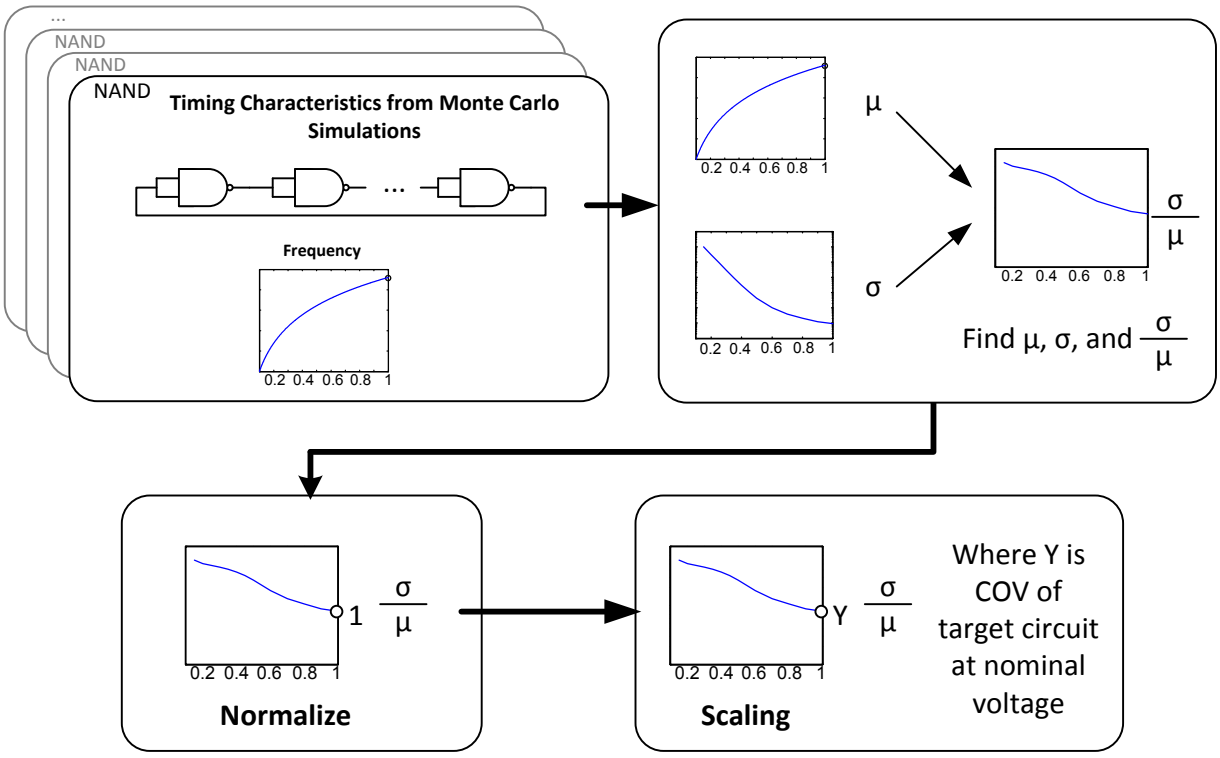

Figure 3.3: Timing Estimate Considering Process Variation

Chapter 4

Analytical Validation

This chapter provides an analytical validation for the framework presented in Chapter 3.1. Later in Chapter 6, we will provide experimental results considering a specific technology with specific circuits. However, this chapter presents an analysis, which allows us to consider the broader case. Additionally, by showing the analytical validation, the sources of error can be more easily identified. To do so, equations that can be applied at any supply voltage, technology, threshold voltage, et cetera, are provided. By normalizing the equations, it can be shown how this process affects the circuit's parameters.

The coefficients of the equations can be broken up into two categories: circuit dependent parameters and circuit independent parameters. Circuit dependent parameters, such as transistor width and load capacitance, vary from circuit to circuit, while circuit independent parameters depend on the process. The simulation framework assumes that the normalized curves of two circuits scale the same way with respect to V_{DD}. This means that after normalizing timing and power, circuit dependent parameters get canceled out and only circuit independent parameters remain (i.e. a normalized ring oscillator curve is identical to a normalized multiplier curve). It will be shown that certain assumptions have to be made in order for this to be true. When these assumptions do not hold, error is introduced into the estimate. The extent of the error will be shown in the experimental validation in chapter 6.

4.1 Active Energy

In this thesis, active energy is considered instead of active power. This way, the frequency variable no longer has to be considered. (4.1) gives a basic equation for the active energy dissipation of a circuit. (4.2) shows (4.1) after normalization to nominal voltage.

$$E_{active}(V_{DD}) = \frac{1}{2} C_L V_{DD}^2 \alpha \tag{4.1}$$

$$S_{Active}(V_{DD}) = \frac{E_{active}(V_{DD})}{E_{active}(V_{Nom})} = \frac{V_{DD}^2}{V_{Nom}^2} \tag{4.2}$$

(4.2) shows that normalization cancels out circuit dependent parameters such as activity factor, α, and load capacitance, C_L, meaning the active energy of a very large circuit with a low activity factor scales the same as a small circuit that is very active with respect to operating voltage.

4.2 Leakage Power

The EKV equations for digital CMOS are based on a circuit dependent parameter known as specific current, I_S, given in (4.3), which is the current when $V_{DS} = V_{GS} = V_{TH}$. The parameters of I_S are subthreshold slope, n, mobility, μ, oxide capacitance, C_{ox}, and thermal voltage, $\phi_t = kT/q$ [12]. (4.4) shows the EKV equation for leakage power where λ_D is the Drain-Induced Barrier Lowering (DIBL) Coefficient and $I_{S,T}$ is the total specific current of the entire circuit.

$$I_S = 2nC_{ox}\mu\frac{W}{L}\phi_t^2 \tag{4.3}$$

$$P_L = V_{DD}I_{S,T}e^{\frac{\lambda_D V_{DD} - V_{TH}}{nV_T}} \tag{4.4}$$

$$S_{Leak}(V_{DD}) = \frac{P_L(V_{DD})}{P_L(V_{Nom})} = \frac{V_{DD}}{V_{Nom}}e^{\lambda_D(V_{DD}-V_{Nom})} \tag{4.5}$$

It is important to note that the parameters in I_S are assumed to be circuit independent, which means that they will be cancelled out during normalization as shown in (4.5). (4.5) shows the equation for leakage current after normalization. DIBL, which is represented as λ_D, is a potential source of error because the framework assumes that λ_D is constant, which is not always the case. Also, (4.4) assumes that V_{TH} is constant. In reality, V_{TH} changes with V_{DD}, W, and L, which is another possible source of error. Additionally, the change in V_{TH} means that there will be a range of I_S due to the fact that the mobility of electrons also changes.

4.3 Timing

The general equation used to find the timing of a critical path, shown in (4.6), can be generalized to the EKV model by defining the drain source current as (4.7). $I_{S,CP}$ is the average specific current of the critical path, K is a fitting parameter, and IC is the inversion coefficient, which is defined in (4.8). The inversion coefficient represents the inversion of a transistor in both subthreshold ($IC < 1$) and superthreshold regions ($IC > 1$) [12].

$$t_d = \frac{C_{CP} V_{DD}}{I_{DS}} \tag{4.6}$$

$$I_{DS} = \frac{I_{S,CP} IC}{K} \tag{4.7}$$

$$IC(V_{DD}) = \ln\left(e^{\frac{V_{DD}(\lambda_D+1)-V_{TH}}{nV_T}} + 1\right)^2 \tag{4.8}$$

$$t_d = \frac{K C_{CP} V_{DD}}{I_{S,CP} IC(V_{DD})} \tag{4.9}$$

$$S_{Timing}(V_{DD}) = \frac{t_d(V_{DD})}{t_d(V_{Nom})} = \frac{V_{DD} IC(V_{Nom})}{V_{Nom} IC(V_{DD})} \tag{4.10}$$

(4.9) shows the EKV equation for delay. Here, C_{CP} represents the total capacitance of the critical path and $I_{S,CP}$ represents the specific current of the critical path, both of which are assumed to be circuit dependent parameters. (4.5) already showed how normalization cancels out circuit dependent parameters when the transistor is in the cutoff region. (4.9) and (4.10) show the effect of normalization on timing. Again, DIBL may lead to some error due to the fact that there may be transistor stacking. Also, the framework once again assumes that V_{TH} is a circuit-independent parameter, whereas in reality, V_{TH} can change with different transistor sizes and supply voltages.

One thing to note is that this chapter considers an analysis from a transistor level. This in turn makes the assumption that the width, length, V_{TH}, stacking, et cetera are the same for every gate, which is an assumption made in Chapter 3.1. In actuality, some of these values will vary and that introduces additional error into the analysis.

4.4 Process Variation

One mathematical model that can be used to estimate the effects of process variation in ULV operation can be found in (4.11). This equation was derived from [17], but certain assumptions were made such as $V_{DS} = V_{GS} = V_{DD}$. However, this is not always the case and will be a source of error with this analysis. In this case, A represents the area, T_{ox} represents the effective oxide thickness, C_{ox} is the oxide capacitance per unit area, E_{ox} is the electric field in the oxide, E_o is a constant around 1.9-2.0 MV/cm and serves as a technology independent parameter [22], E_a is the activation energy, k and T are the Boltzman constant and temperature, respectively.

$$\Delta V_{TH} = A * T_{ox} \sqrt{C_{ox}(V_{DD} - V_{TH})} e^{\frac{E_{ox}}{E_o}} \left(1 - \frac{V_{DD}}{\alpha(V_{DD} - V_{TH})}\right) e^{-\frac{E_a}{kT}} \beta^{0.25} t^{0.25} \tag{4.11}$$

$$\frac{\Delta V_{TH}(V_{DD})}{\Delta V_{TH}(V_{Nom})} = \sqrt{\frac{V_{DD}-V_{TH}}{V_{Nom}-V_{TH}}} e^{\frac{E_o(V_{DD}-V_{Nom})}{T_{ox}}} \frac{(V_{Nom}-V_{TH})(\alpha(V_{DD}-V_{TH})-V_{DD})}{(V_{DD}-V_{TH})(\alpha(V_{Nom}-V_{TH})-V_{Nom})} \quad (4.12)$$

(4.12) shows the normalized equation for this. Most of the circuit independent parameters get cancelled out, except for E_o and the oxide thickness.

Chapter 5

Experimental Methodology

This chapter further discusses the specifics of how the results in Chapter 6 were obtained. To start, variations of the baseline ring oscillator are compared. These variations are those that highlight the potential error sources of this methodology. Then, ISCAS benchmark circuits are used to further verify the validity of this framework by demonstrating its accuracy. The characterization of flip flops are discussed and lastly, process variation of timing delay is also considered, both with local and global process variation.

5.1 Modified Ring Oscillator Analysis

First, to validate the simulation framework, baseline normalized ring oscillator curves were obtained from an 11-stage 2-input NAND ring oscillator with a fanout of one and with transistor lengths and widths from a commercial standard cell library. This was simulated in HSpice and the frequency and power consumption were measured from nominal voltage down to the minimum operating voltage, which has been determined to be 150mV. These baseline curves serve as the foundation of the simulation framework and are used to determine the power and timing of other circuits. Therefore, the effects of results compared to baseline ring oscillators with respect to varying parameters such as load capacitances, stacking, et cetera need to be evaluated. To do so, the baseline's characterized curves are compared to the ring oscillators with varied parameters. These experiments were performed with a 130nm UMC technology library.

5.1.1 Increased Fanout

To evaluate the effects of an increased fanout in a ring oscillator, one can use the baseline ring oscillator and modify this. If the baseline ring oscillator has a fanout of one, then the

modified ring oscillators will have increasing fanouts of two, three, and four. This is achieved by adding additional 2-input NAND gates with the outputs grounded between each stage of the baseline ring oscillator.

5.1.2 Varying Critical Path

To simulate a varying critical path depth, ring oscillators made up of 2-input NAND gates with increasing stages were created. The number of gates in the critical path are 15, 21, 25, and 31. These will be compared to the baseline ring oscillator, which has 11 stages.

5.1.3 Increased Transistor Width

Another parameter that can be varied is the width of a transistor. Several 11-stage ring oscillators with 2-input NAND gates are created wherein the transistor width of each is increased by two to ten times the original width of the baseline ring oscillator's transistors.

5.2 Circuit Analysis

Several ISCAS benchmark circuits were analyzed using the proposed framework as well as the EKV model as a basis for comparison. Pass transistor logic and gates with three or more inputs were excluded because of their poor reliability in the ULV region [27]. The circuits were simulated in SPICE from nominal voltage down to the minimum operating voltage.

5.2.1 Leakage Power

The target circuit's leakage current is measured from V_{DD} values between nominal voltage and 150mV in addition to varying V_{TH} voltages using HSpice. The resulting current values are fitted to a surface plot in MATLAB where V_{DD} and V_{TH} are treated as variables as shown in (5.3). (5.3) is derived by dividing V_{DD} from (4.4) and taking the natural logarithm of both sides. This will yield (5.1) which can be rewritten as (5.2). Finally, (5.3) is simply (5.2) rewritten to make the multivariable nature of the equation more evident. The fitted equation will give the fitting parameters p_0, p_x, and p_y which can be used to find values n and λ_D as seen in (5.4) and (5.5), respectively. p_0 (or $ln(I_S)$), λ_D, and n are then put into (5.1) where the exponential of both sides are taken to yield the final leakage current value estimated by the EKV model. This value is then multplied by V_{DD} to produce the leakage power estimated by the EKV model.

$$ln(I_L) = ln(I_S) + \frac{\lambda_D V_{DD} - V_{TH}}{nV_T} \tag{5.1}$$

$$ln(I_L) = \frac{\lambda_D}{nV_T} V_{DD} - \frac{1}{nV_T} V_{TH} + ln(I_S) \tag{5.2}$$

$$y(V_{DD}, V_{TH}) = p_x V_{DD} + p_y V_{TH} + p_0 \tag{5.3}$$

To obtain values of n and λ_D, (5.4) and (5.5) are used with the parameters derived from (5.3).

$$n = \frac{-1}{p_y V_T} \tag{5.4}$$

$$\lambda_D = p_x n V_T \tag{5.5}$$

The values for p_x, p_y, and p_0 are derived by using the surface fitting tool in MATLAB. p_x and p_y will be used in (5.4) and (5.5) and the exponential of p_0 is used to derive the value of I_S. Using these derived values, (4.4) can be used.

To evaluate leakage power for weighted averages, a chain of gates is made out of the particular type of gates found in the circuit. Leakage power values are collected at multiple supply voltages. After determining the power for each gate, each set of values is normalized and scaled by the power at nominal voltage of the target circuit. Finally, the ratio of each gate's occurrence in the circuit is multiplied by its respective power curve to yield the leakage estimate.

5.2.2 Active Energy

With regards to the EKV model, using (4.1), the variables α and C_L are grouped together into one variable, k. At nominal voltage, the active energy of a particular circuit is measured and set equal to $C_L \alpha$. Knowing the value of $E_{active}(V_{Nom})$ and setting $V_{DD} = V_{Nom}$, the value of k can be derived. Now that the constant k is known, any value of $E_{active}(V_{DD})$ can be estimated using the EKV model.

To evaluate active energy in combinatorial components using the weighted averages technique, a chain of each of the gates found in the standard library is made. Total energy values are collected at V_{DD} values between nominal voltage and 150mV. After determining the total energy for each gate, the leakage energy of the circuit is subtracted from the total to yield the active energy value. Then, each set of values is normalized and scaled to the energy at nominal voltage of the target circuit. Lastly, the ratio of each gate's occurrence in the circuit is multiplied by its respective energy curve to yield the final energy estimate.

5.2.3 Timing

Using the parameters λ_D and n that were generated through 5.2.1, these can be be put into (4.8). In this case, $IC(V_{DD})$ is evaluated at only one V_{TH}. The result of (4.8) is then put into (4.9) where the parameters K, C_{CP}, and $I_{S,CP}$ will be treated as a constant, g. To solve for g, the delay characteristic of a particular circuit is measured with HSpice at varying V_{TH} and V_{DD} levels as shown in (5.6). (5.6) will generate every value of g for each V_{DD} so the geometric mean of g is taken to produce a constant. From this, t_d is found at nominal voltage using HSpice. Now, any value of t_d can be estimated using the EKV model.

$$\frac{KC}{I_S} = \frac{t_d IC}{V_{DD}} \tag{5.6}$$

For the weighted averages estimation's combinational elements, an 11-gate ring oscillator is used to derive the gates' natural frequency. These frequencies are collected at V_{DD} values between nominal voltage and 150mV. These values are normalized and scaled to the frequency of the target circuit at nominal voltage. Finally, the ratio of each gate's occurrence in the critical path of the circuit is multiplied by its respective frequency curve to yield the timing estimate.

5.3 Flip Flops

To characterize the leakage power of a flip flop, a single flip flop's leakage power values are collected at V_{DD} values from nominal voltage to 150mV. The normalized data is then used to estimate the leakage power consumed by the target circuit's flip flops.

Likewise, to evaluate the active energy of a flip flop, a single flip flop's total energy values are collected at V_{DD} values between nominal voltage and 150mV. The leakage power derived previously is converted to energy by multiplying the power by the same period that was used to derive the total energy values. Finally, the single flip flop's leakage values are subtracted from the total values to yield the active energy of a flip flop.

To determine the setup time of a flip flop, the period between the data edge changing and the clock asserting was made larger and larger until the data latched. The critical delay of a sequential circuit is the sum of the combinatorial critical delay and the flip flop setup requirement. The timing experiments shown in 6.2 only look at clock to Q delay rather than evaluating setup time.

5.4 Process Variation for Timing Delay

To account for process variation in a circuit, the same circuits in previous sections are run using Monte Carlo. In this regard, the original framework's approach can be used. In this thesis, both global and local process variation effects are considered. For timing delay, a ring oscillator is run with Monte Carlo at varying supply voltages. This will yield a multitude of results for which the standard deviation, or σ, will be derived for the circuit. In previous sections, tests were performed using the typical corner of operation, so those results will be used as the mean, or μ of our analysis. To get the coefficient of variation, the σ is divided by μ for each V_{DD}.

Now that the coefficient of variation has been calculated, the same process of normalization and circuit characterization can be applied. That is, the coefficient of variation of the ring oscillator can be normalized and then the coefficient of variation of the target circuit at nominal voltage can be multiplied by the normalized circuit to yield the approximate coefficient of variation for the target circuit. Essentially, the coefficient of variation curves of the timing values are analagous to the timing values themselves with regards to process variation considerations and circuit characterization estimations, respectively.

Chapter 6

Results

6.1 Modified Circuit Parameter Analysis

To demonstrate that this technique is accurate even with varying circuit parameters, this chapter shows three examples of the baseline ring oscillator being modified either through circuit dependent parameters (such as varying critical path) or circuit independent parameters (such as transistor width) and compared to the original baseline ring oscillator for leakage power, active energy, and timing delay.

Figures 6.1 through 6.3 show the effects of varying ring oscillator lengths. The idea is to essentially simulate varying critical path lengths. The results seem to suggest that active energy is the parameter most heavily affected by a varying critical path. Timing delay error is also affected, but the error is less than 0.5 percent for a 31 gate ring oscillator, so this error is negligible. Leakage power is also virtually unaffected by the change in lengths. The errors from active energy can be attributed to second order effects that have not been considered in the analytical discussion.

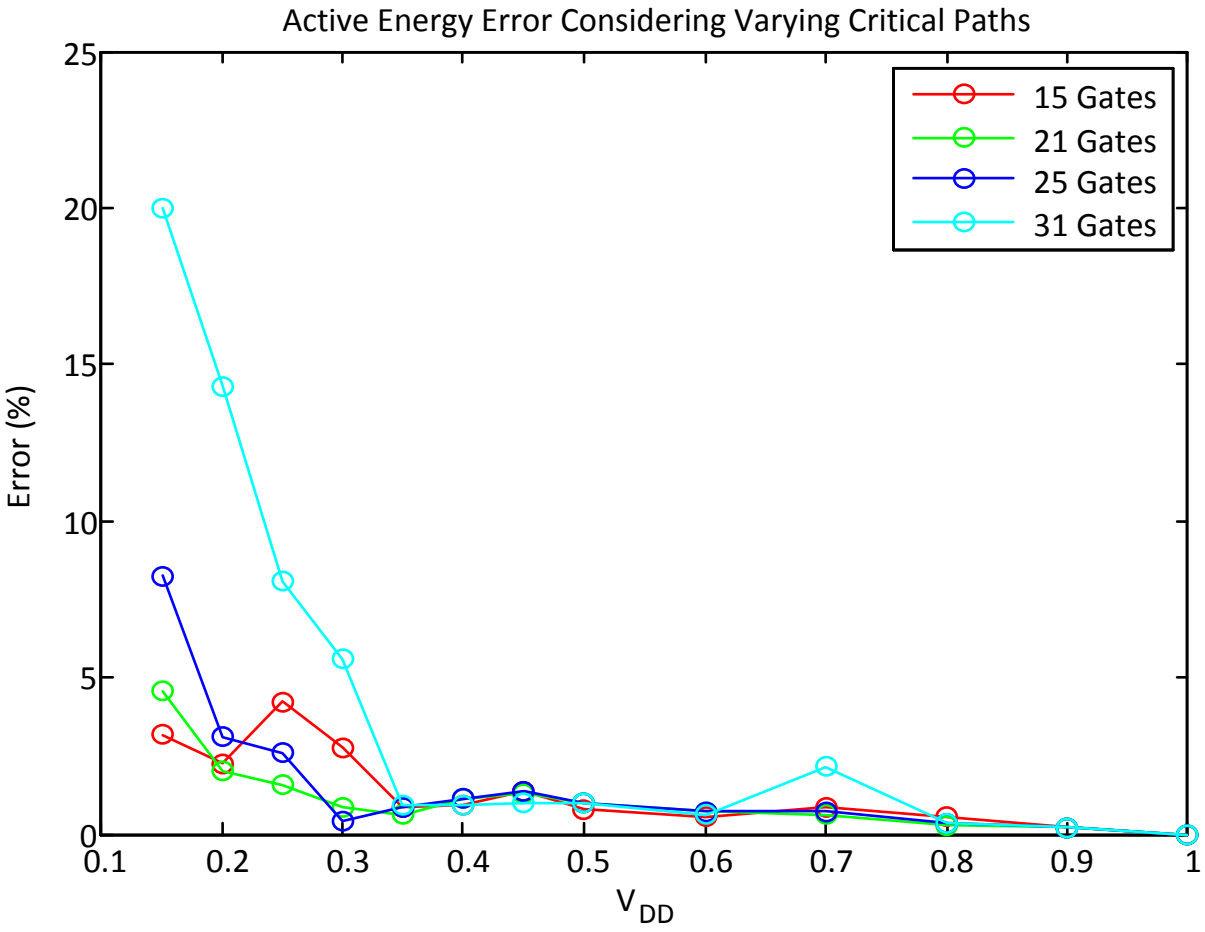

Figure 6.1: The effect of a varying critical path length on active energy

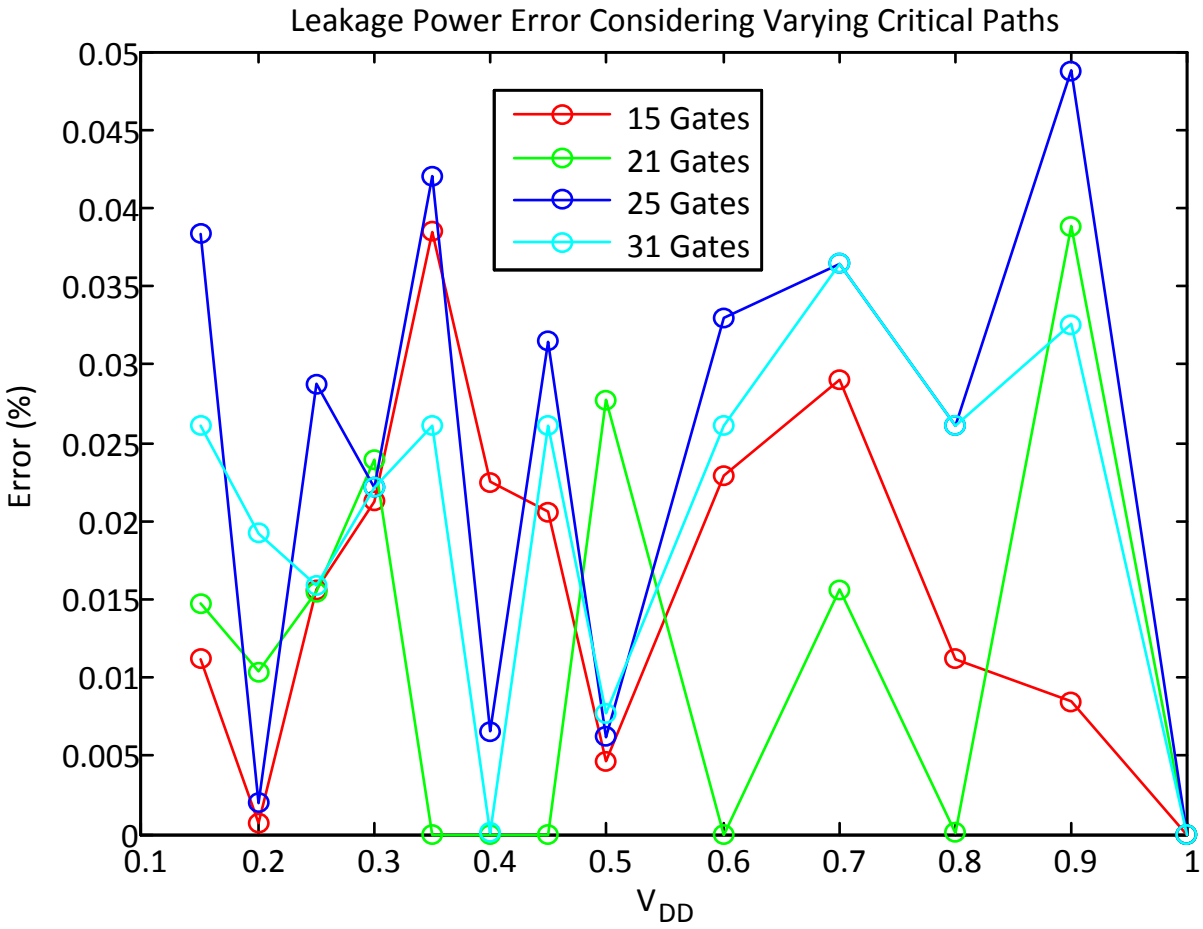

Figure 6.2: The effect of a varying critical path length on leakage power

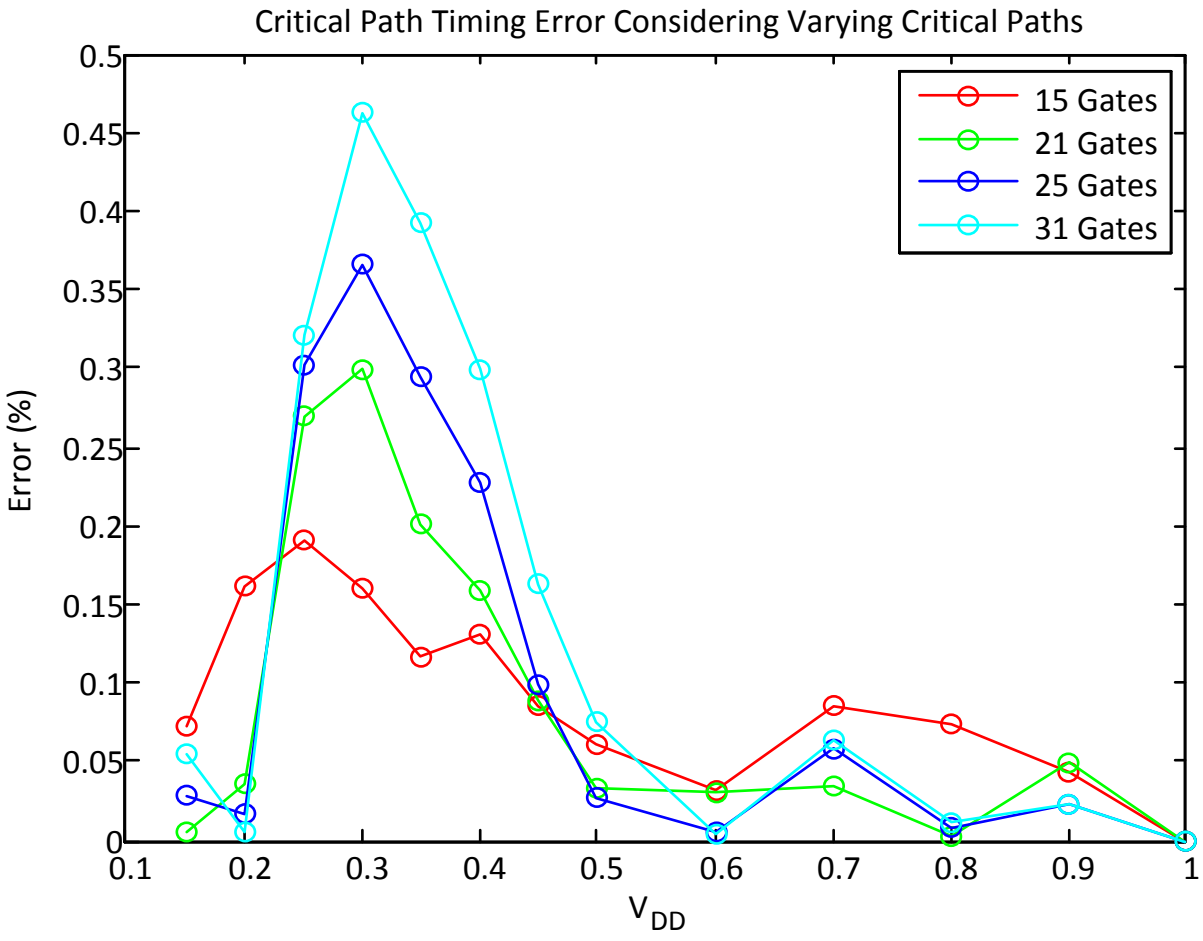

Figure 6.3: The effect of a varying critical path length on timing delay

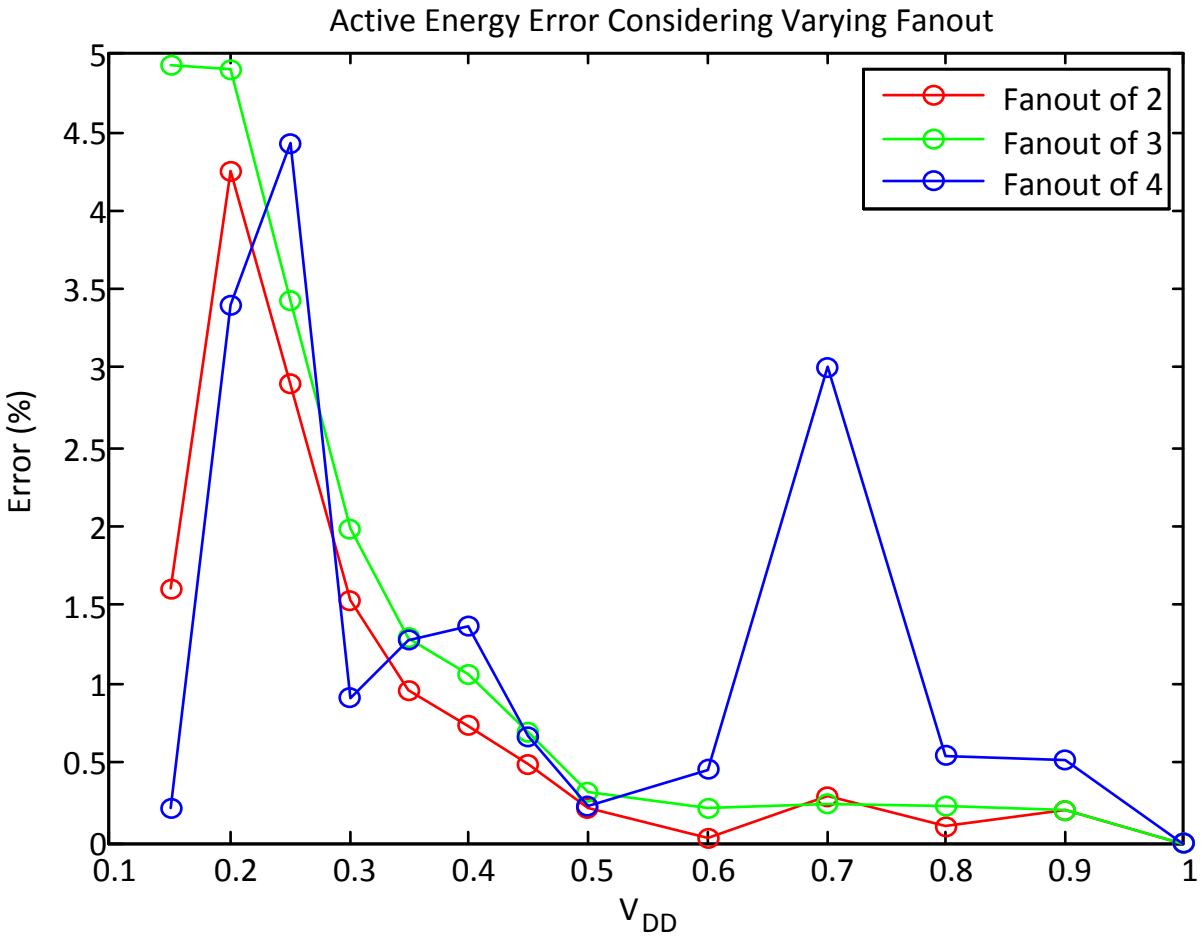

Figure 6.4: The effect of varying fanouts on active energy

Figures 6.4 through 6.6 show the effects of increasing fanout from the base ring oscillator. This test considers varying load capacitances in a circuit. Overall, for active energy, there are variations, but overall, after normalization, the general shape of the active curve, regardless of fanout level, remains the same. The leakage power error curve is virtually unaffected by fanout as well. The only parameter that is affected by an increasing fanout is timing delay. The error for this increases as the fanout increases as well, most likely due to a second order delay not discussed in the analytical section.

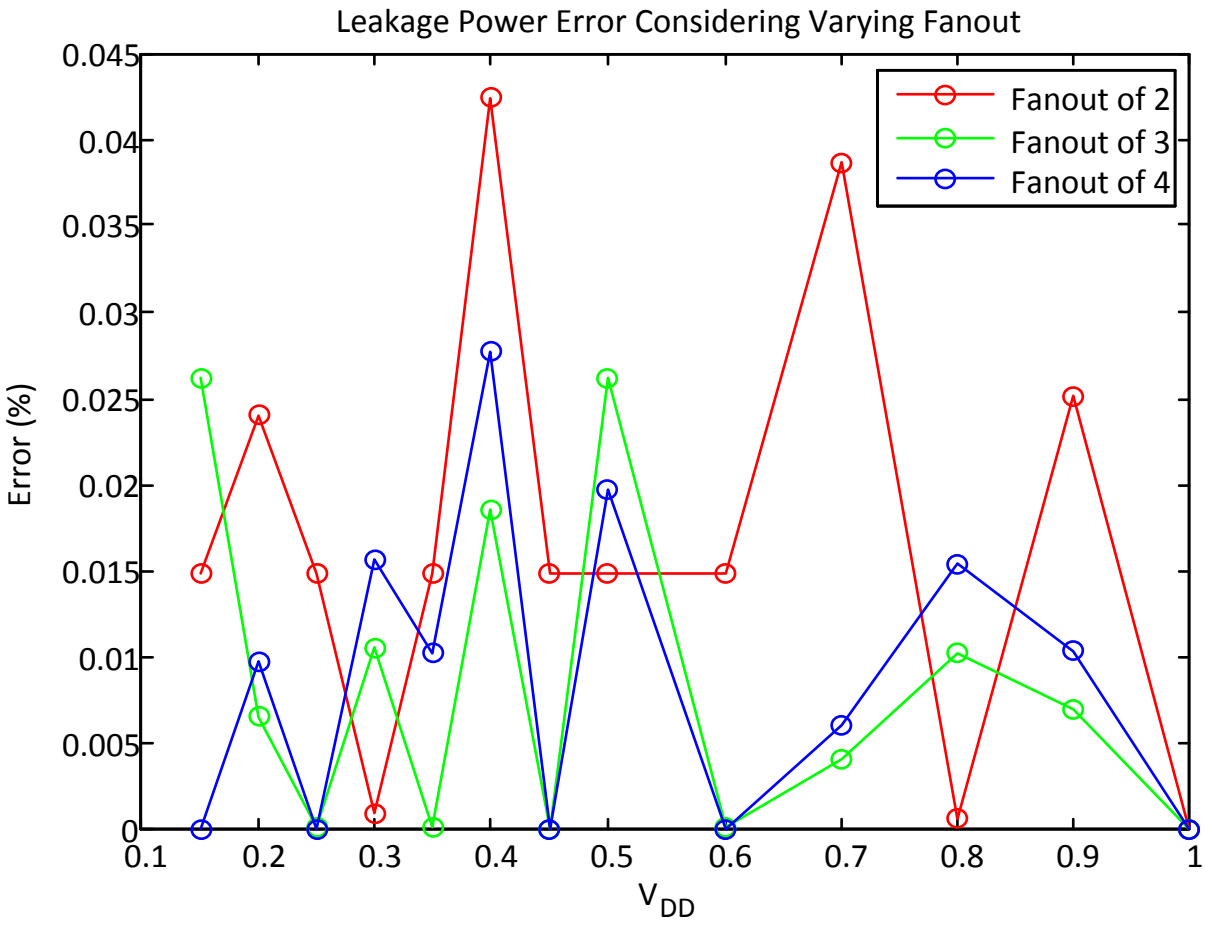

Figure 6.5: The effect of varying fanouts on leakage power

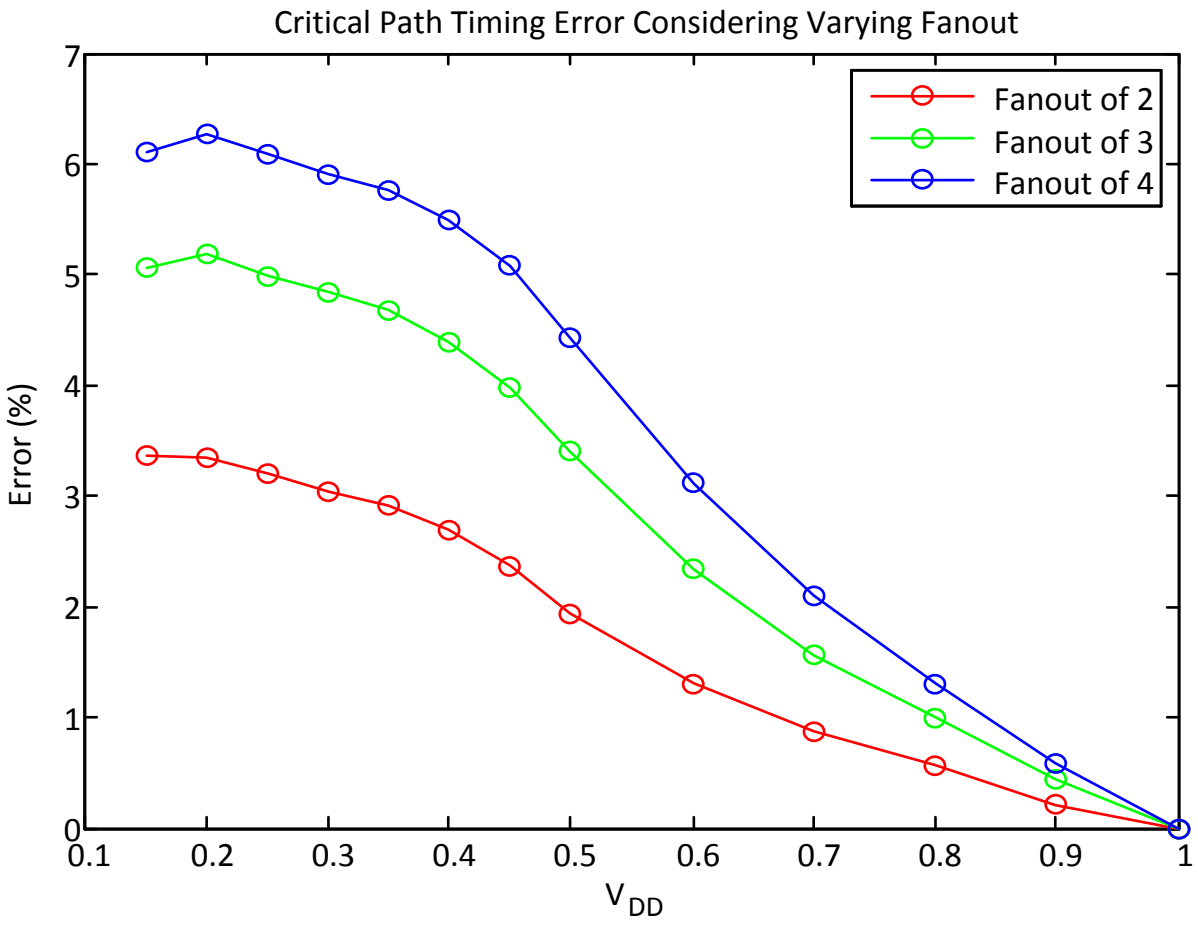

Figure 6.6: The effect of varying fanouts on timing delay

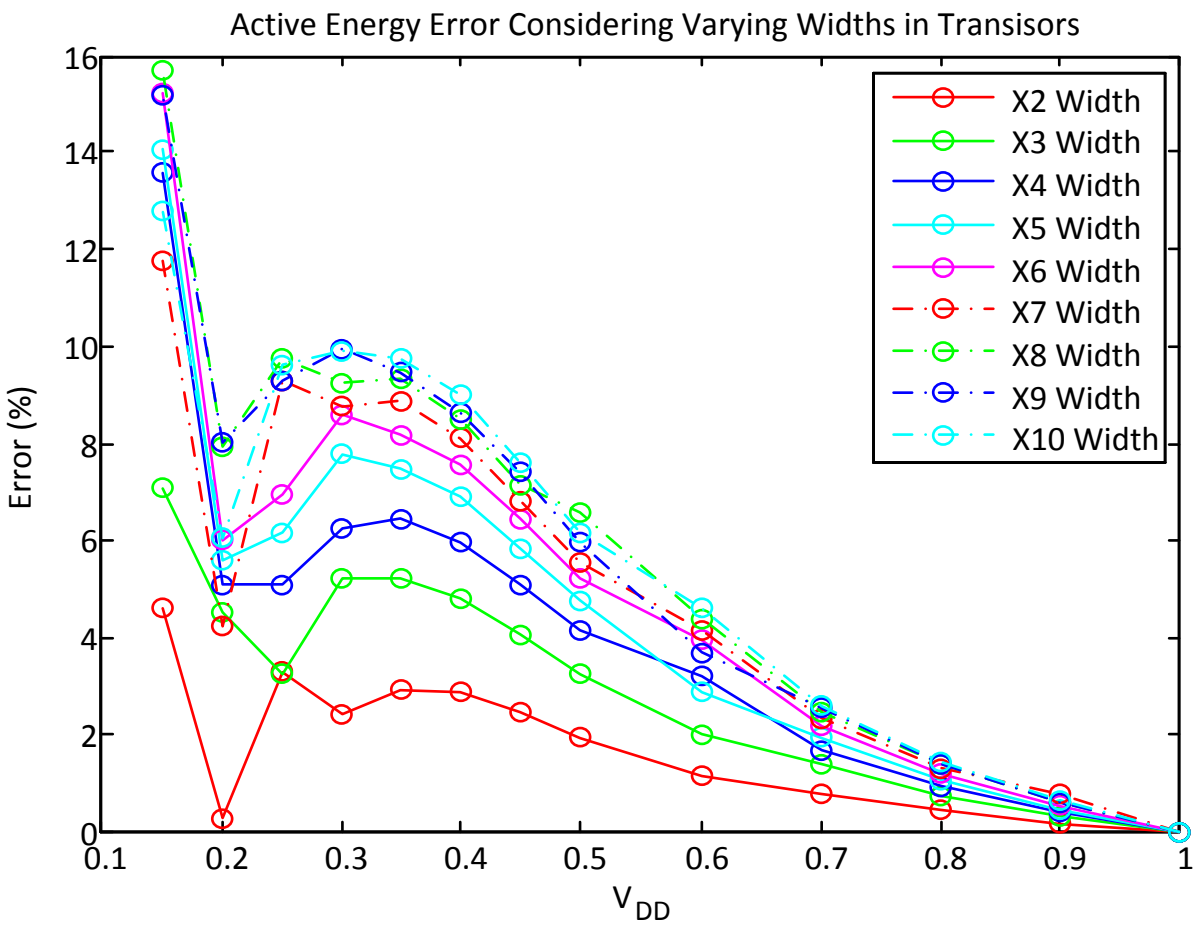

Figure 6.7: The effect of varying transistor widths on active energy

Figures 6.7 through 6.9 show the effect of increasing widths in transistors. Not surprisingly, the active energy error increases as the width of the transistor increases. Likewise, the leakage power's error also increases as the transistor width increases. Possibly the most significant error comes in from timing error, which increases substantially. Again, these errors can be attributed to the fact that tools such as HSpice use more complex algorithms than the ones considered in this thesis. Because of this, there are additional effects incurred than expected.

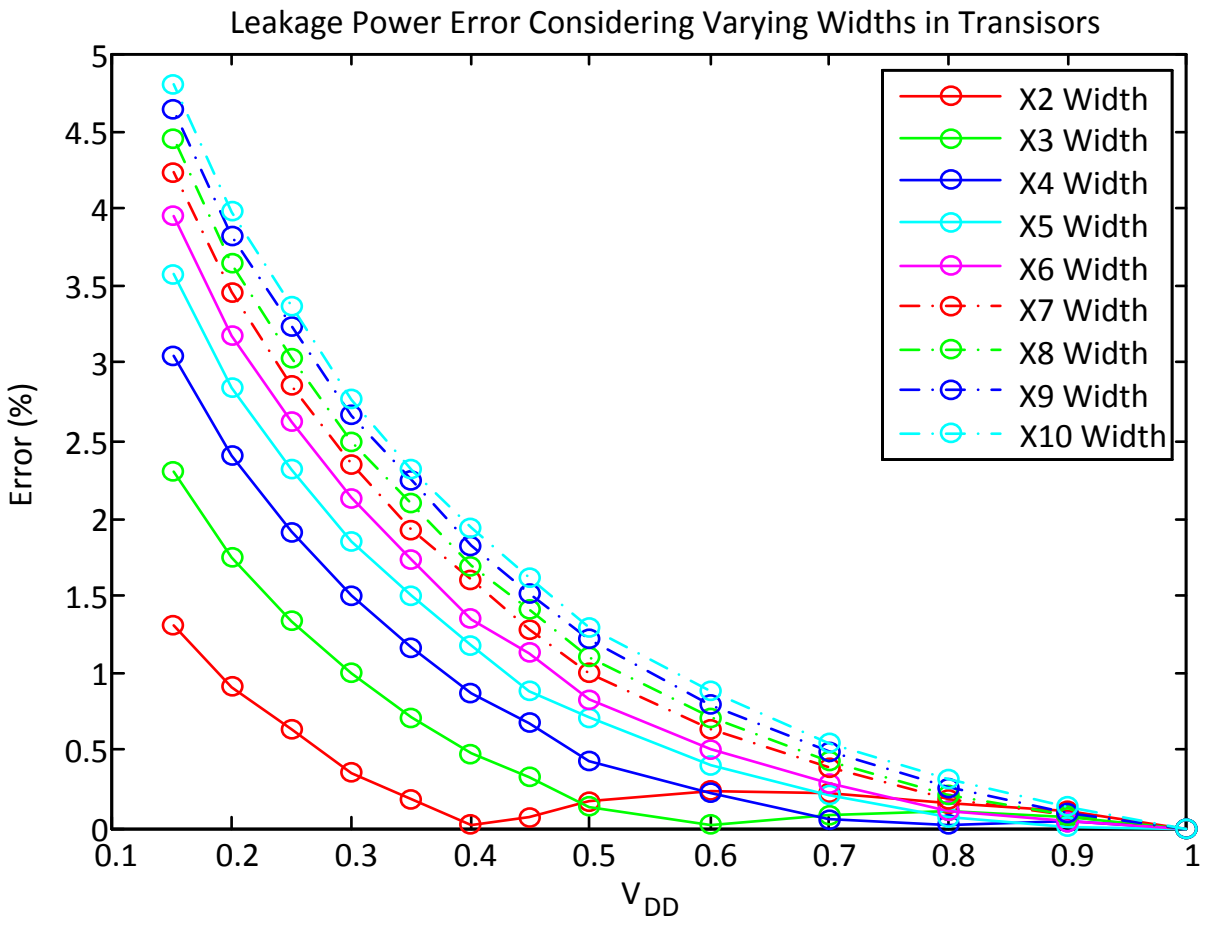

Figure 6.8: The effect of varying transistor widths on leakage power

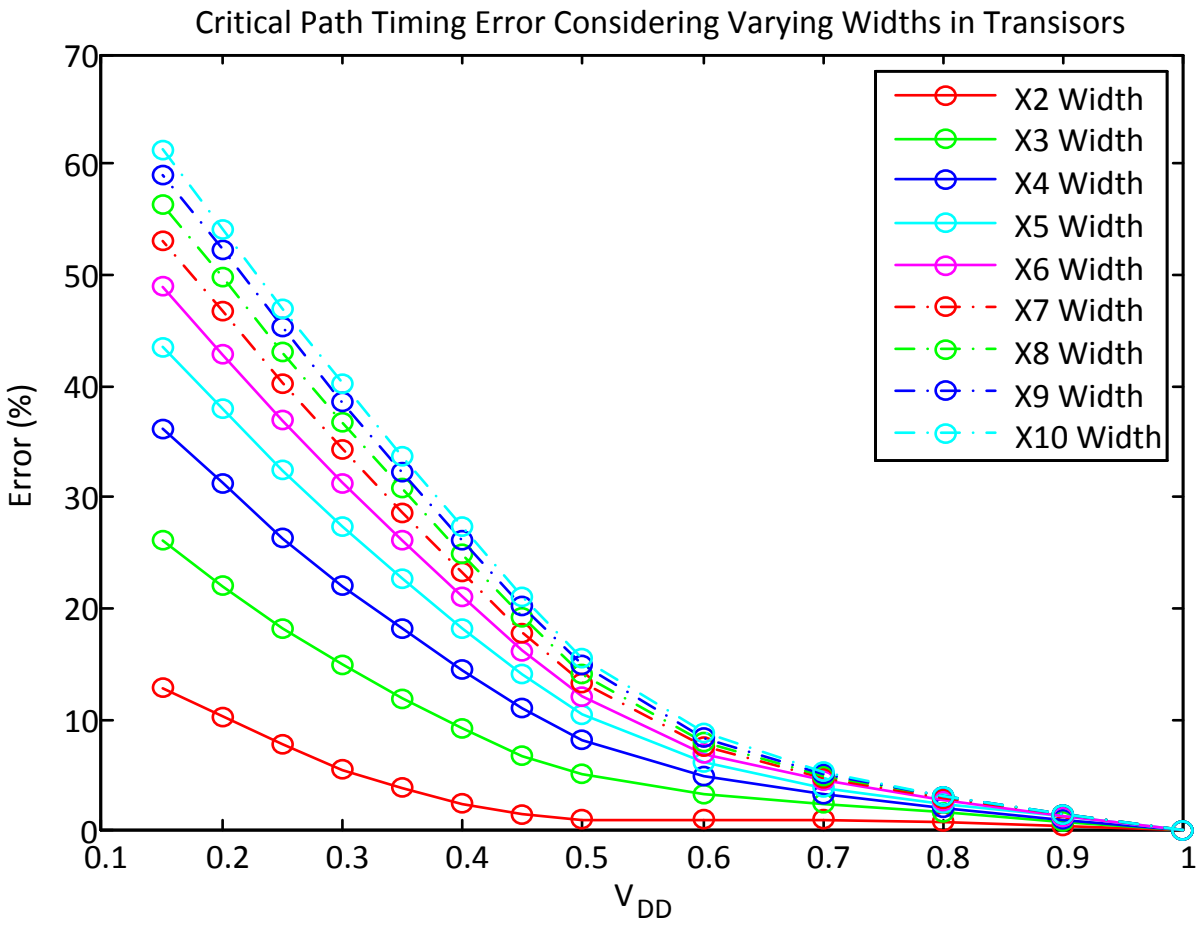

Figure 6.9: The effect of varying transistor widths on timing delay

6.2 Benchmark Circuit Test

This section tests the proposed frameworks against standard ISCAS circuits. This is to show that this method works for sequential circuits, which prove to be the most difficult to create estimation models for. Table 6.1 shows the maximum error for each circuit active energy, leakage power, and timing delay using the NAND estimate, weighted averages, and the EKV model's estimation techniques. One common trend that is found is that, overall, the weighted averages estimation is the best technique for estimation, followed by the NAND estimation technique, and lastly the EKV model's estimation. Another notable trend is that, for timing estimation, the EKV model performes poorly in the subthreshold regions. In fact, Table 6.1 does not even consider the highest two errors for the EKV model when evaluating the maximum error to give a more fair analysis of the models.

Figures 6.10 through 6.12 show s27's errors. Figure 6.13 shows 6.12 zoomed to capture the majority of the points in the analysis.

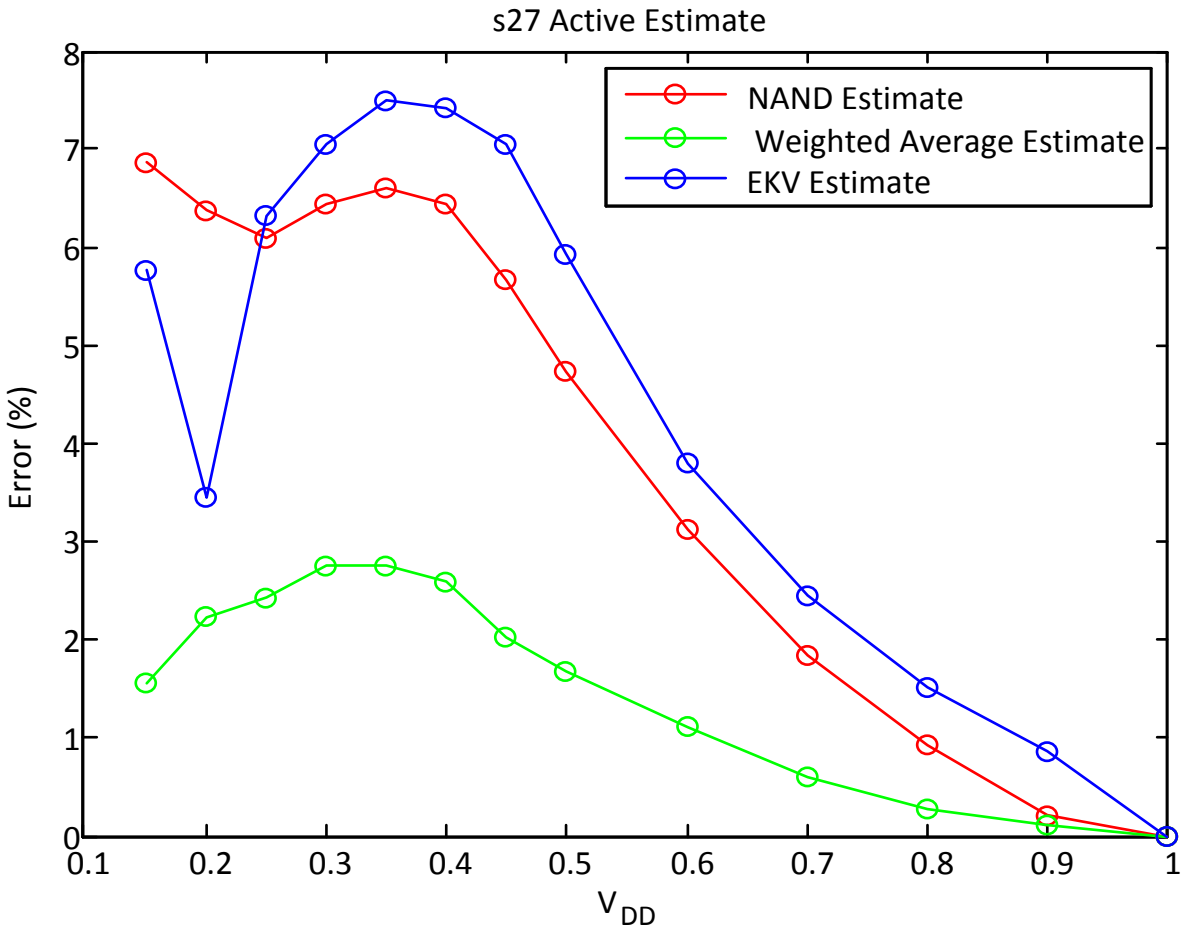

Figure 6.10: Active energy error for s27 with NAND, Weighted Average, and EKV estimates

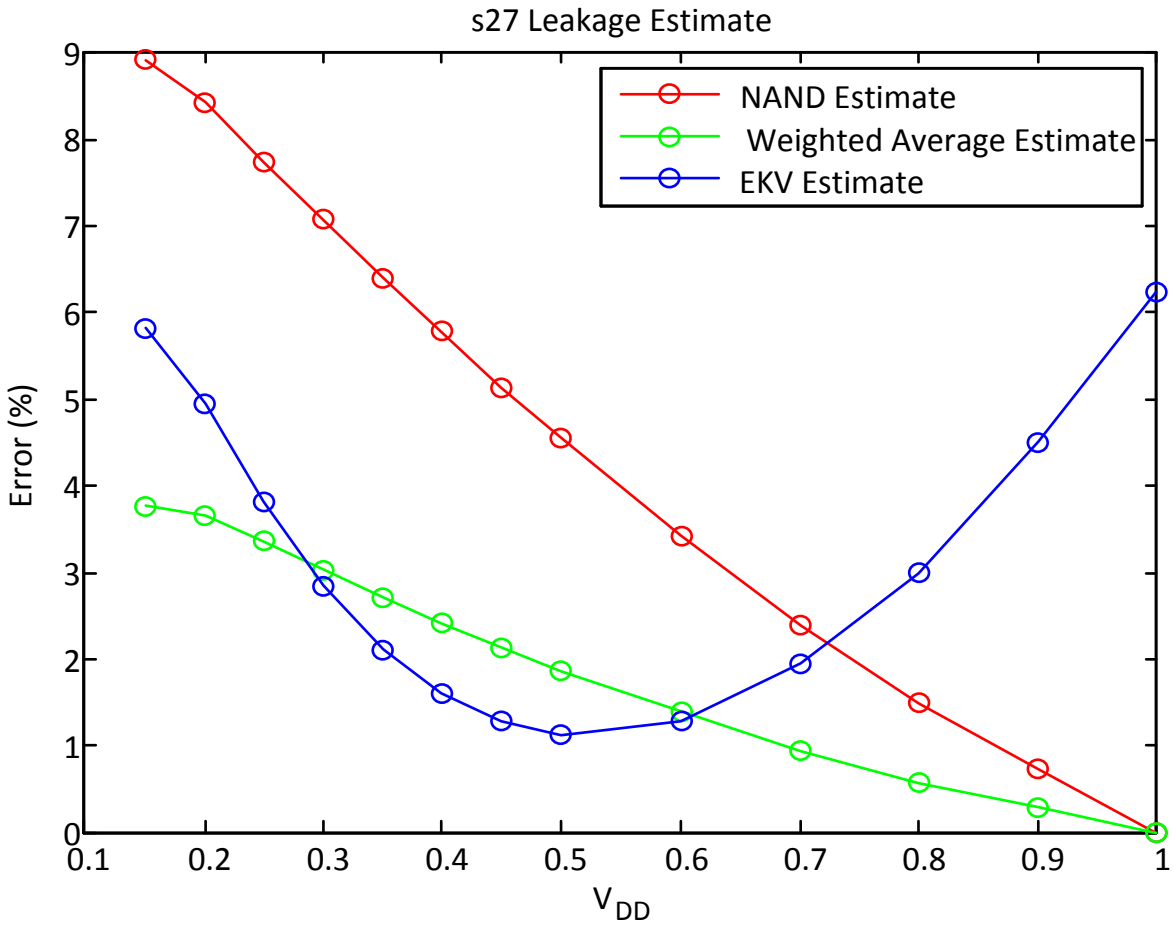

Figure 6.11: Leakage power error for s27 with NAND, Weighted Average, and EKV estimates

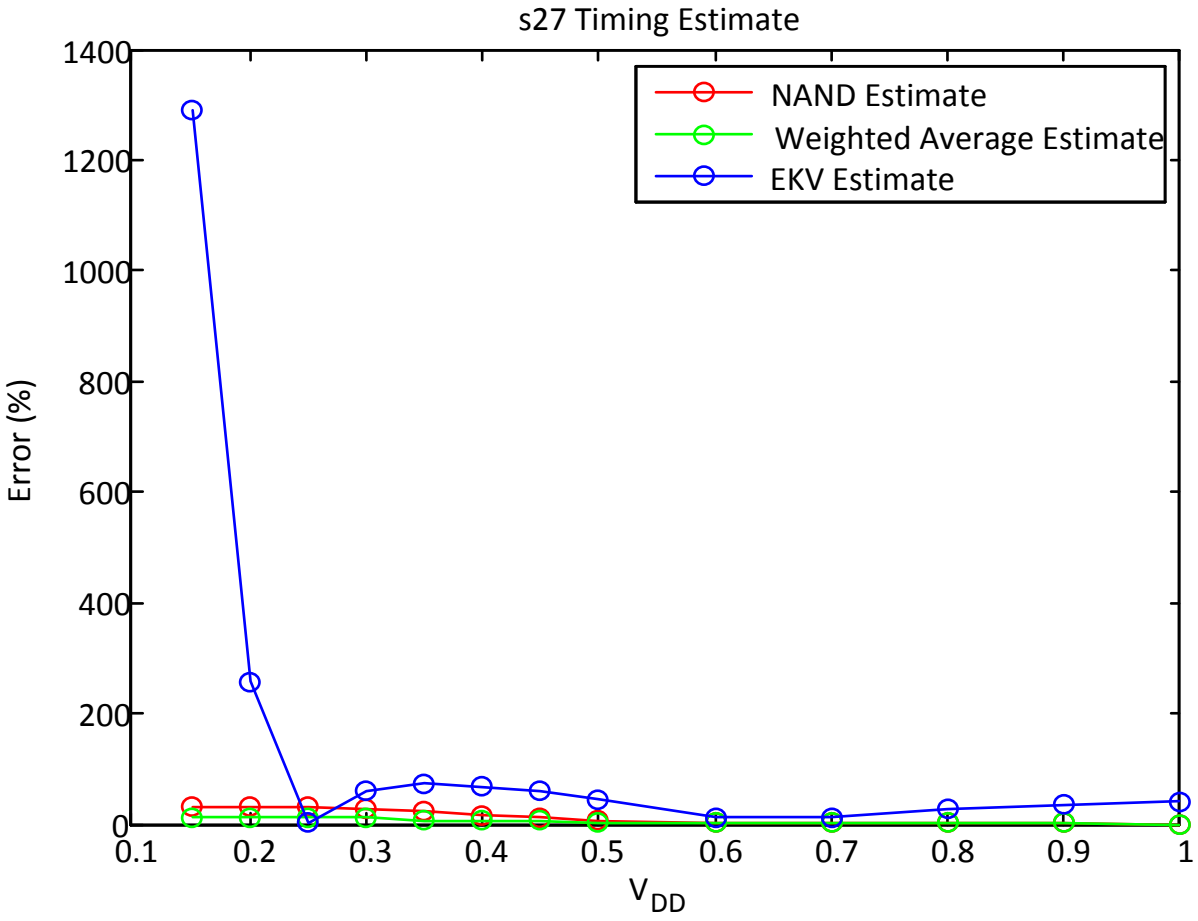

Figure 6.12: Timing delay error for s27 with NAND, Weighted Average, and EKV estimates

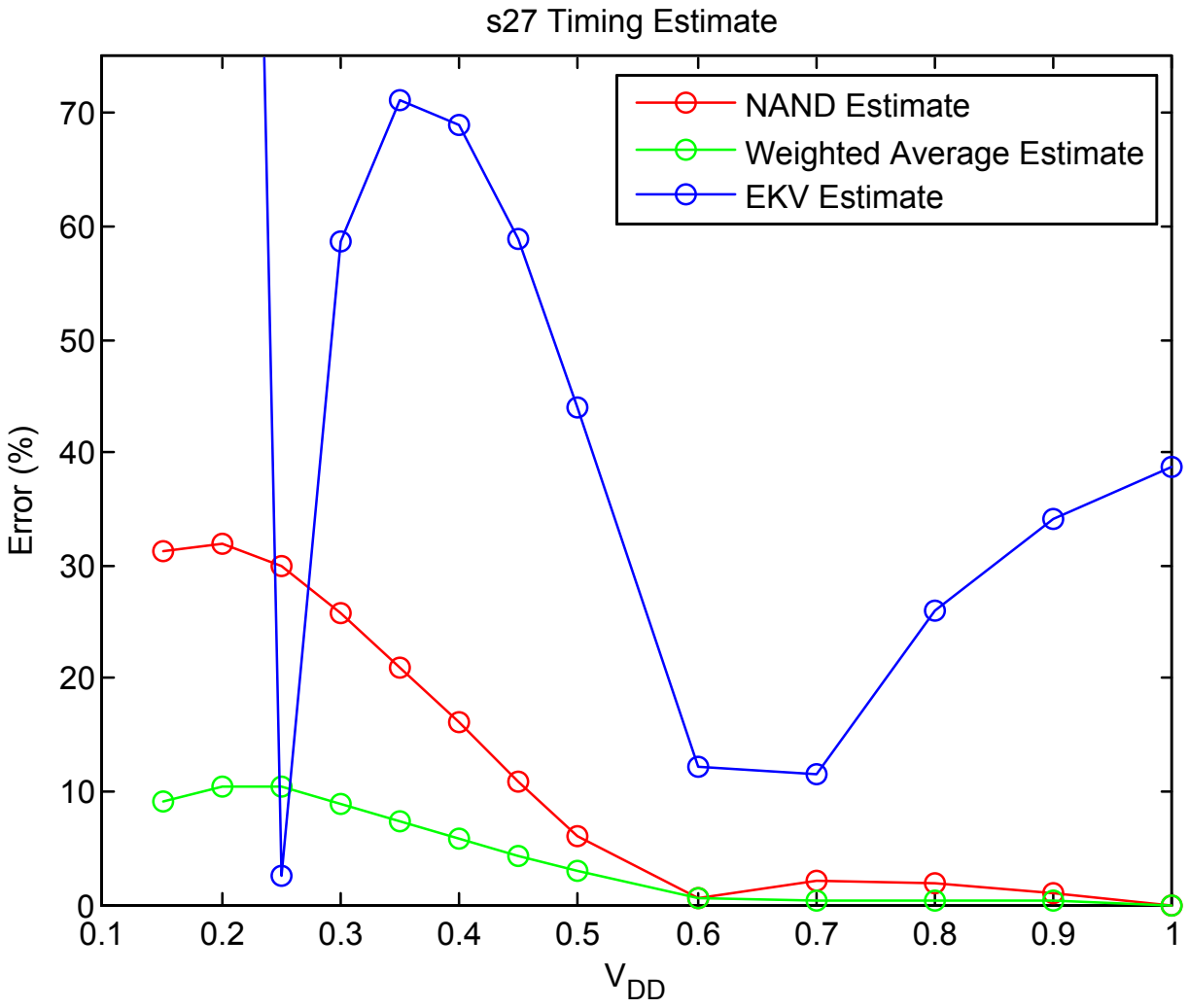

Figure 6.13: Timing delay error for s27 with NAND, Weighted Average, and EKV estimates

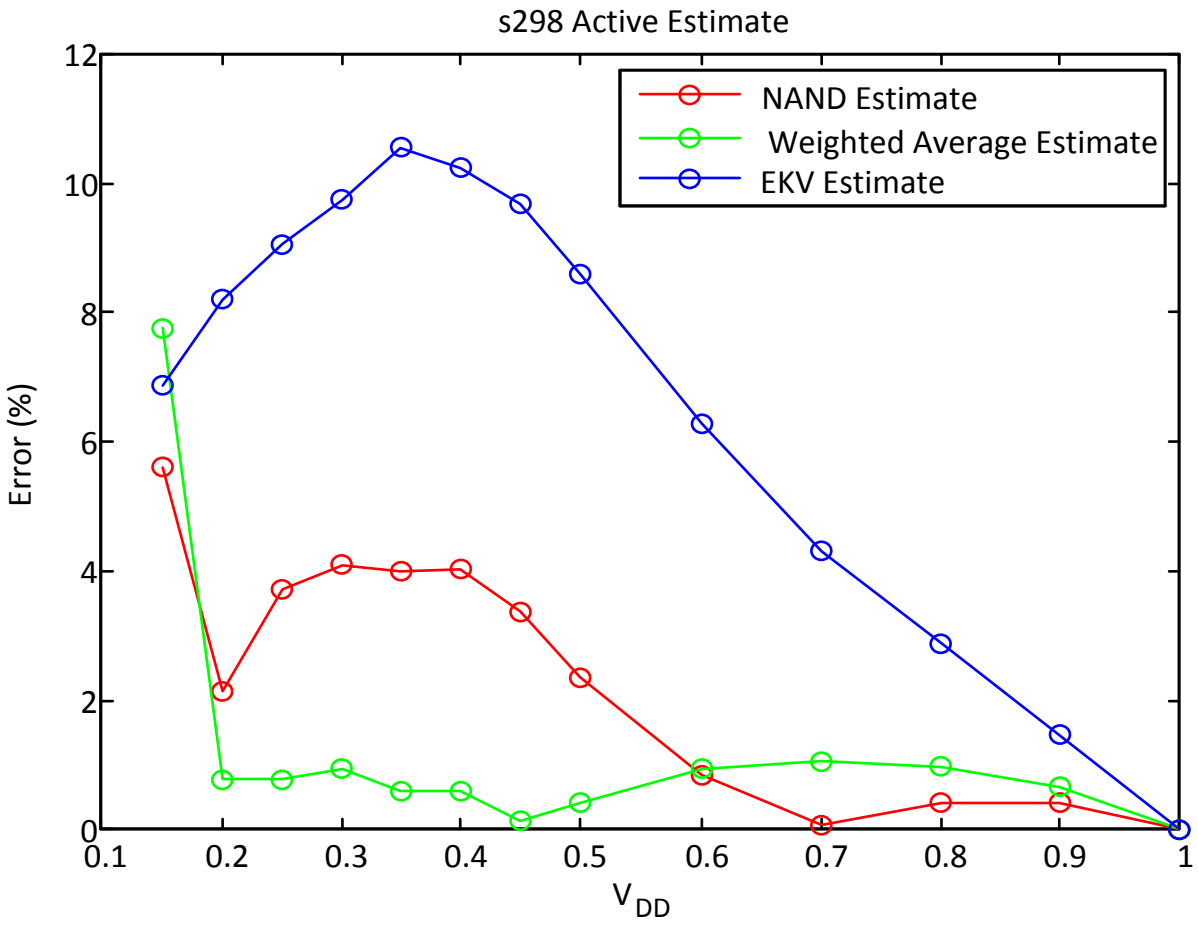

Figure 6.14: Active energy error for s298 with NAND, Weighted Average, and EKV estimates

Figures 6.14 through 6.16 show s298's errors. Figure 6.17 shows 6.16 zoomed to capture the majority of the points in the analysis.

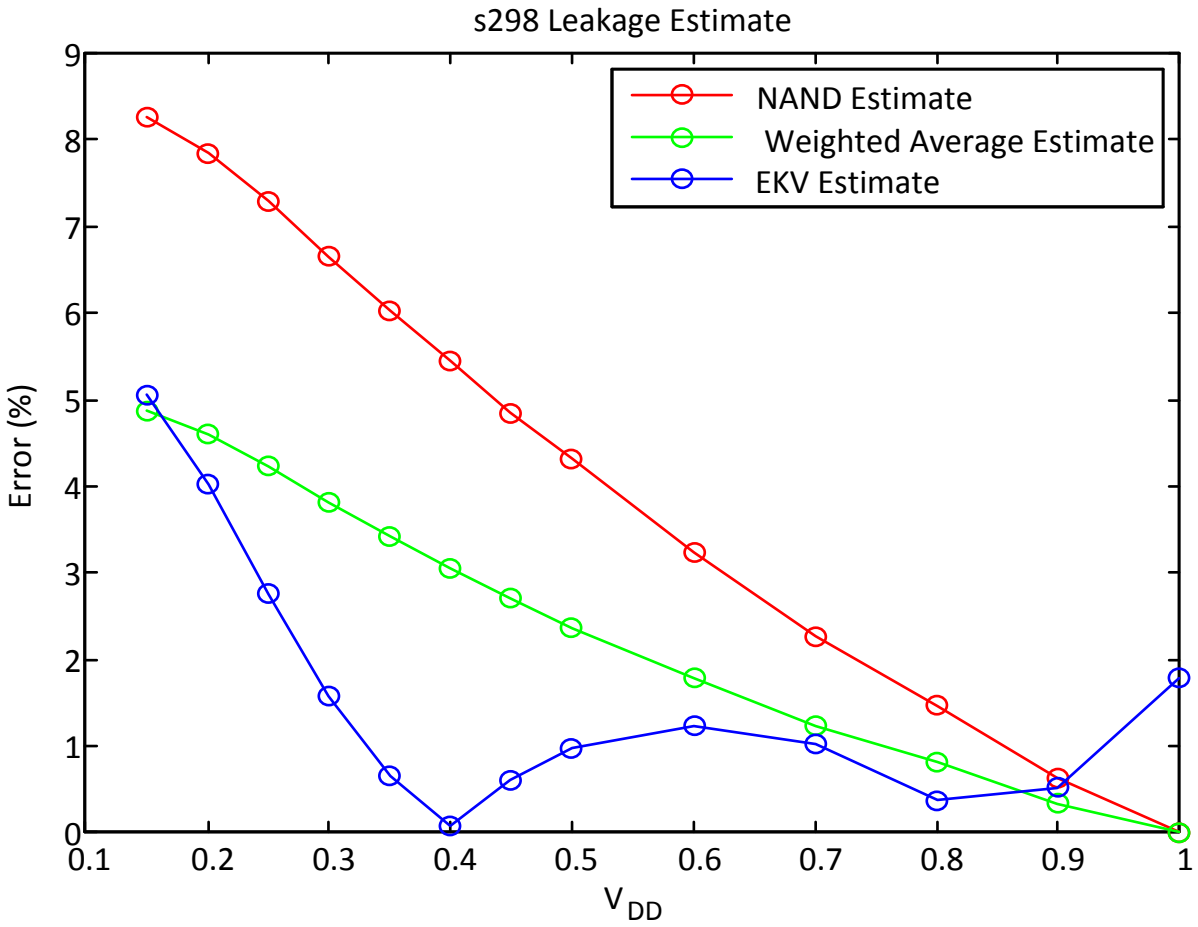

Figure 6.15: Leakage power error for s298 with NAND, Weighted Average, and EKV estimates

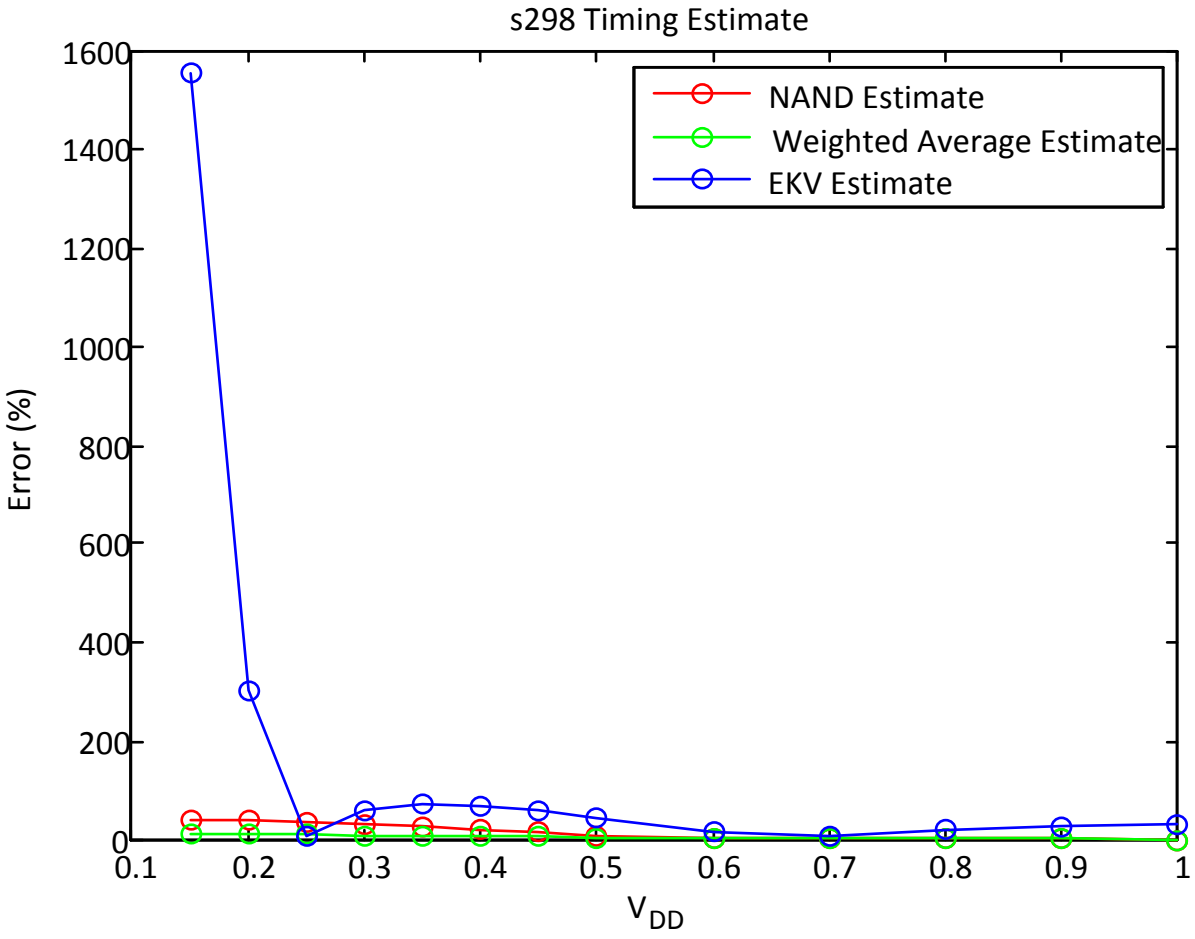

Figure 6.16: Timing delay error for s298 with NAND, Weighted Average, and EKV estimates

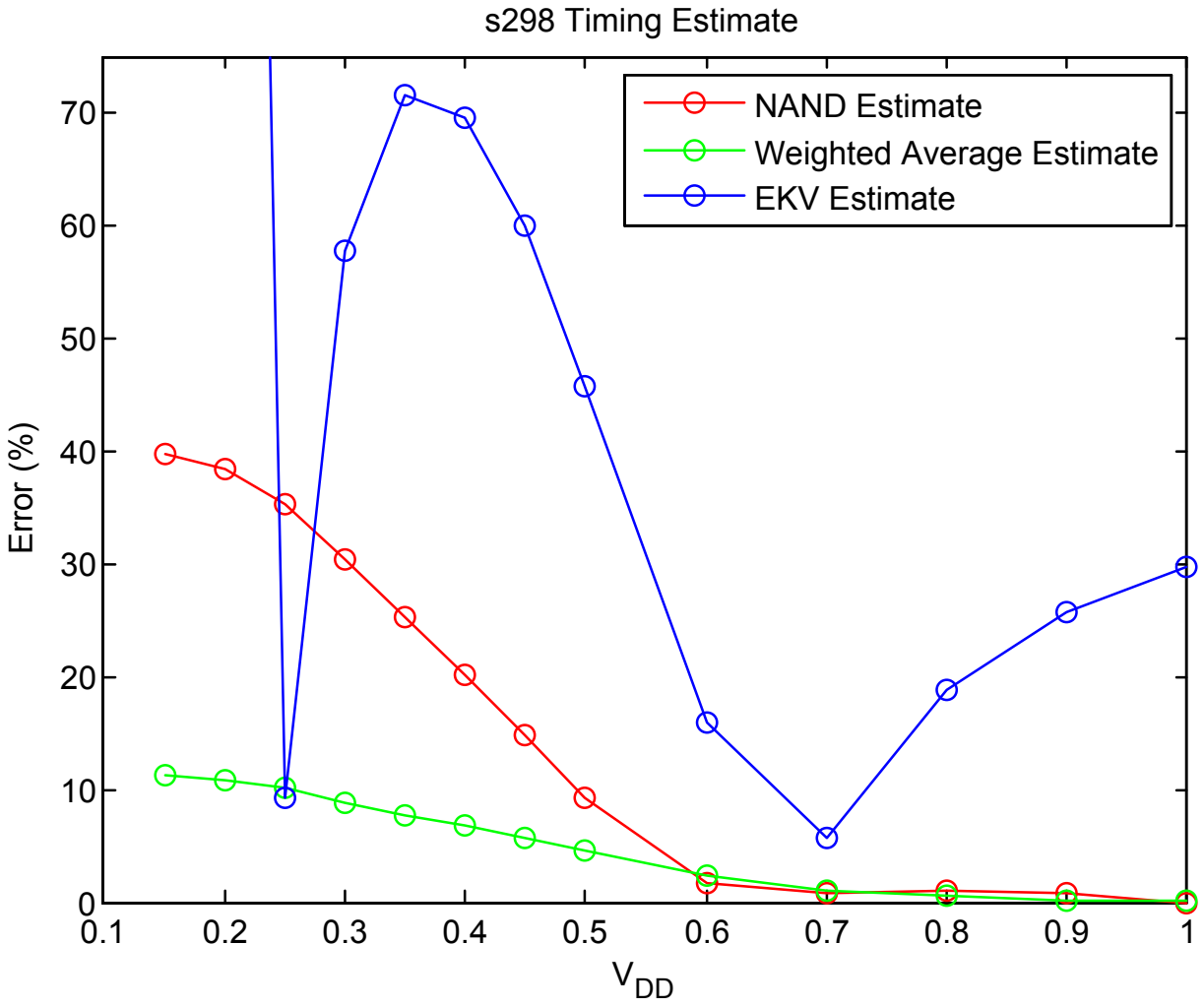

Figure 6.17: Timing delay error for s298 with NAND, Weighted Average, and EKV estimates

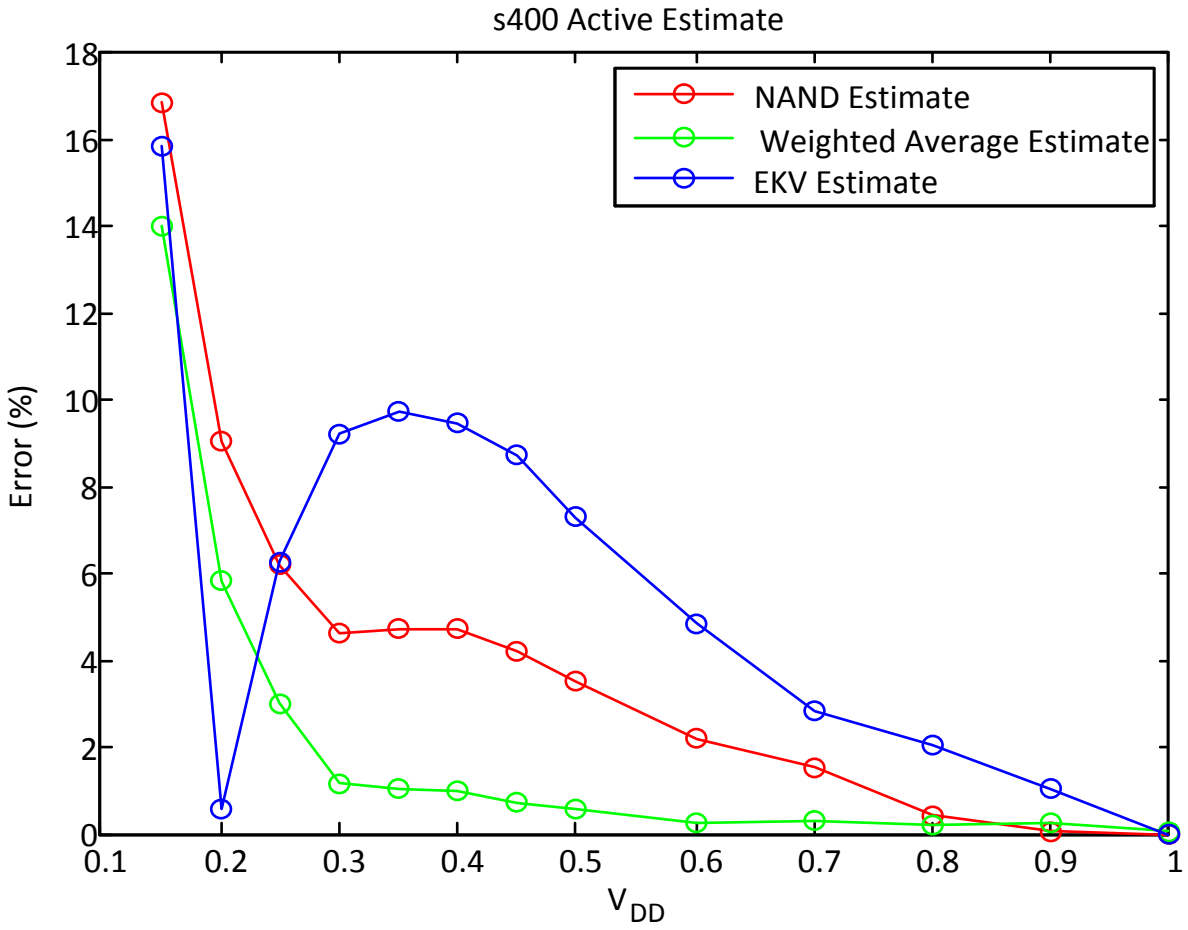

Figure 6.18: Active energy error for s400 with NAND, Weighted Average, and EKV estimates

Figures 6.18 through 6.20 show s400's errors. Figure 6.21 shows 6.20 zoomed to capture the majority of the points in the analysis.

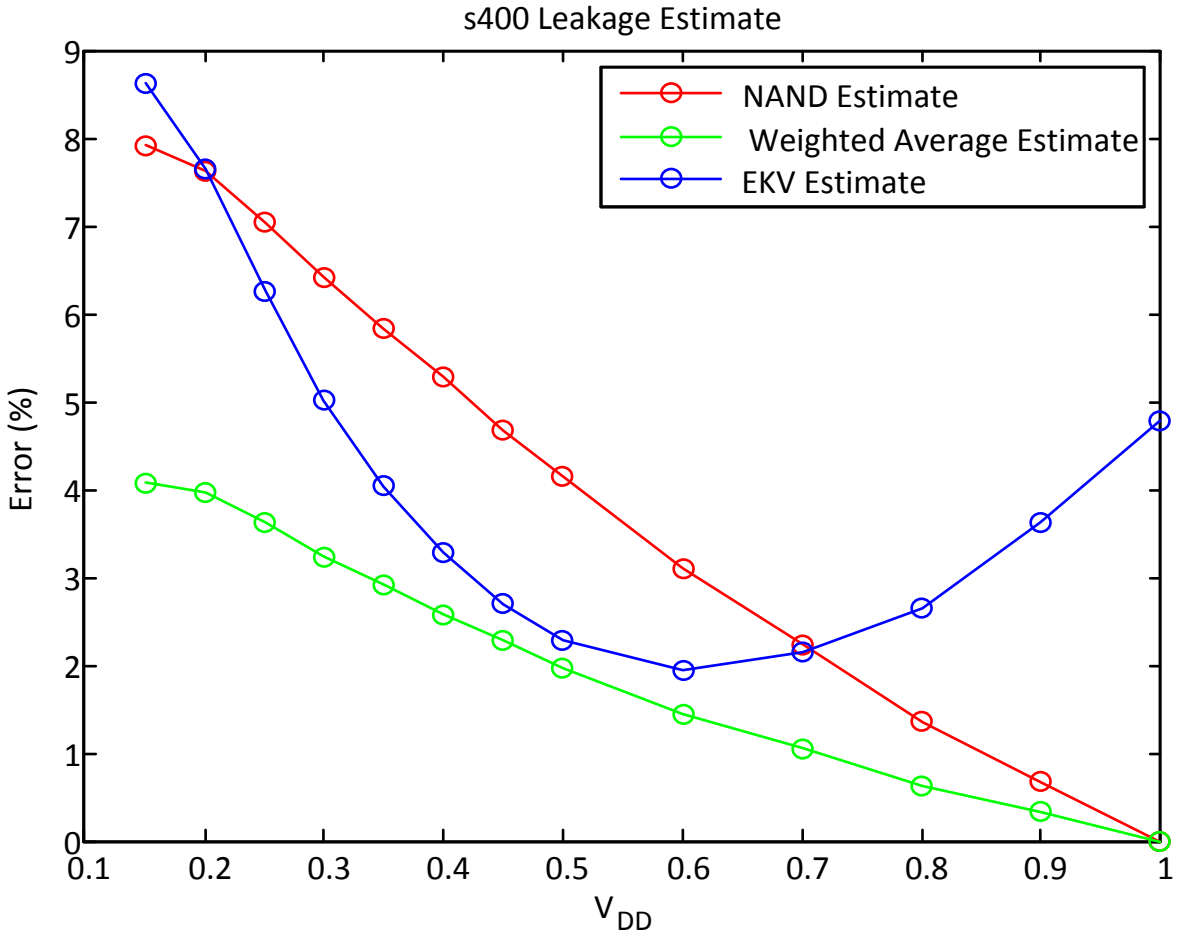

Figure 6.19: Leakage power error for s400 with NAND, Weighted Average, and EKV estimates

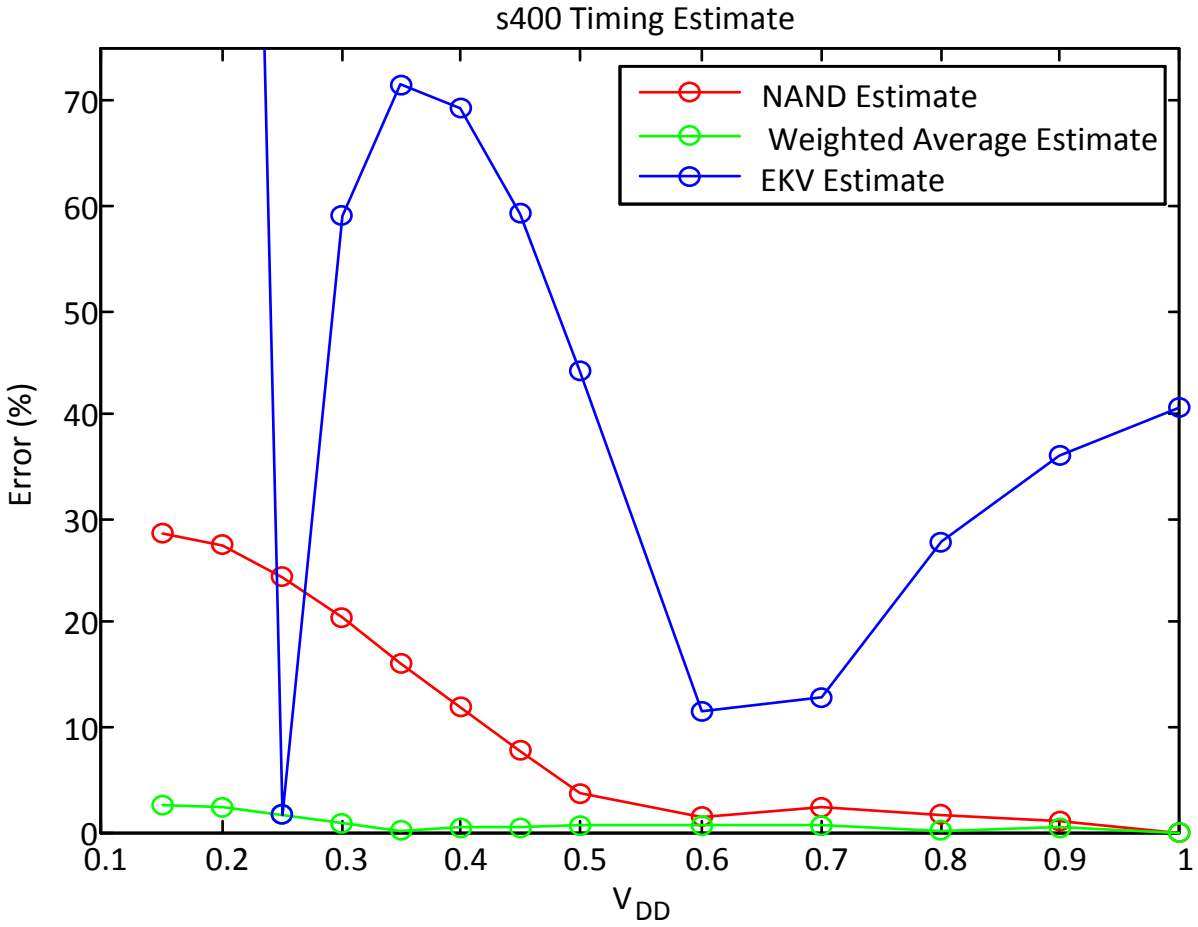

Figure 6.20: Timing delay error for s400 with NAND, Weighted Average, and EKV estimates

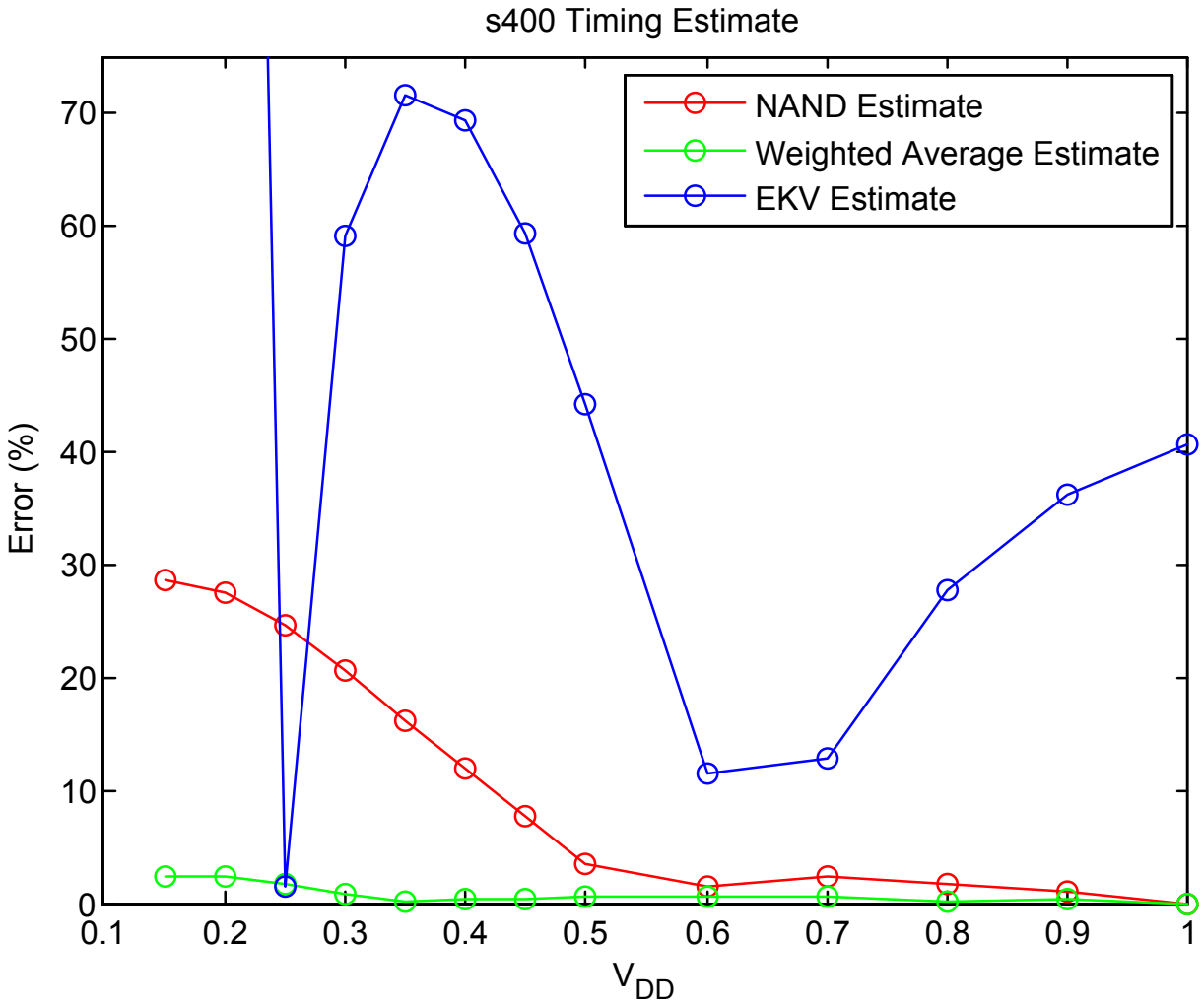

Figure 6.21: Timing delay error for s400 with NAND, Weighted Average, and EKV estimates

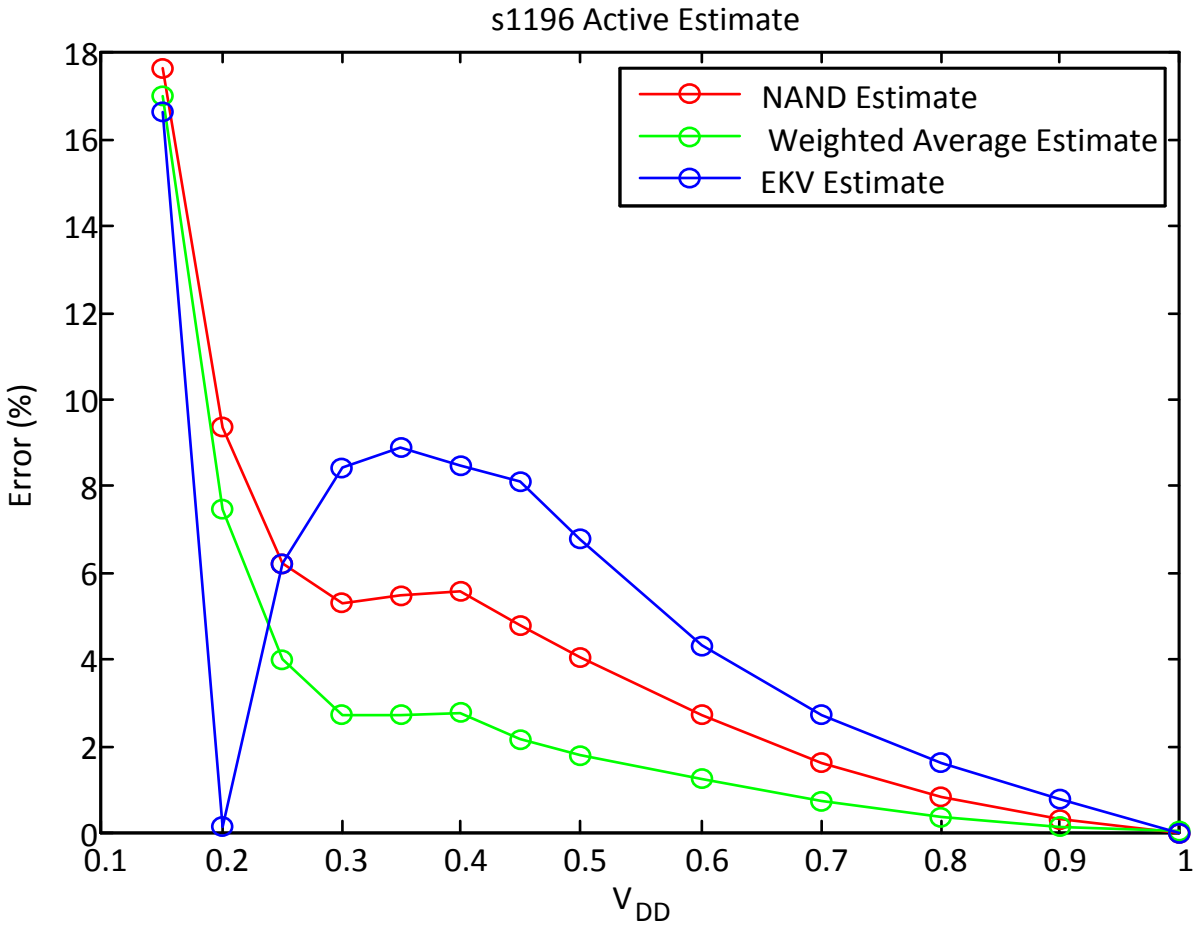

Figure 6.22: Active energy error for s1196 with NAND, Weighted Average, and EKV estimates

Figures 6.22 through 6.24 show s1196's errors. For timing, the error of the NAND estimation technique versus the weighted average estimation technique is about the same due to the fact that the majority of the critical path for s1196 is NAND gates. Figure 6.25 shows 6.24 zoomed to capture the majority of the points in the analysis.

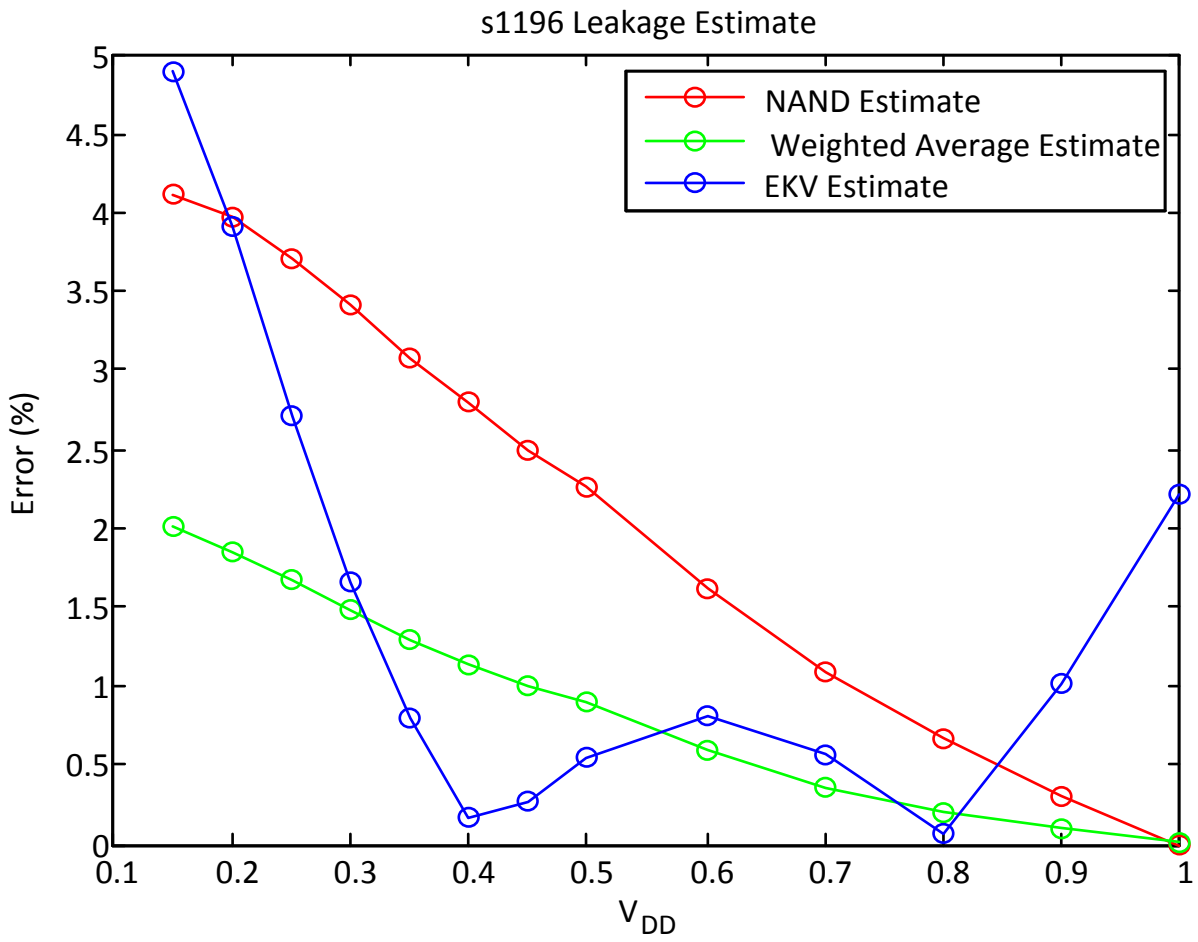

Figure 6.23: Leakage power error for s1196 with NAND, Weighted Average, and EKV estimates

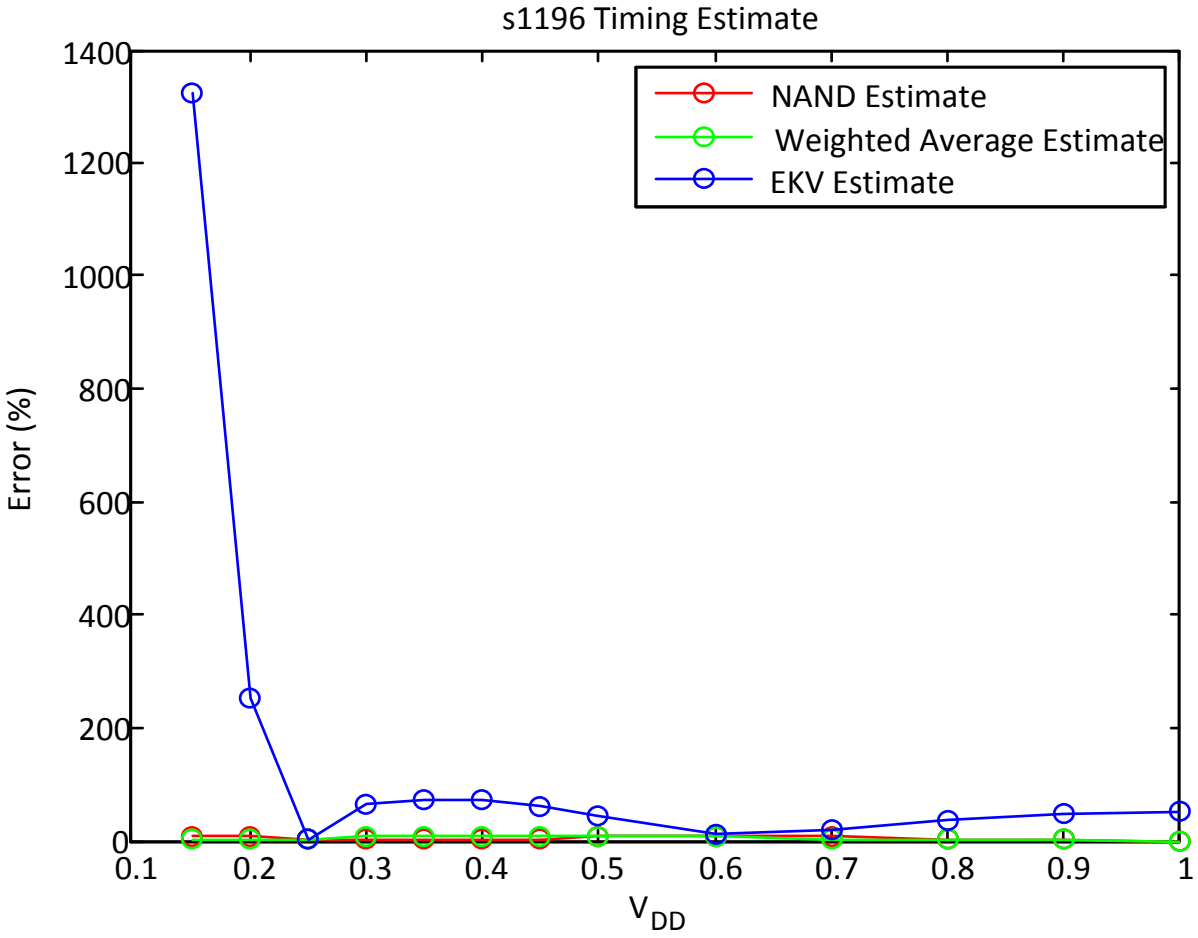

Figure 6.24: Timing delay error for s1196 with NAND, Weighted Average, and EKV estimates

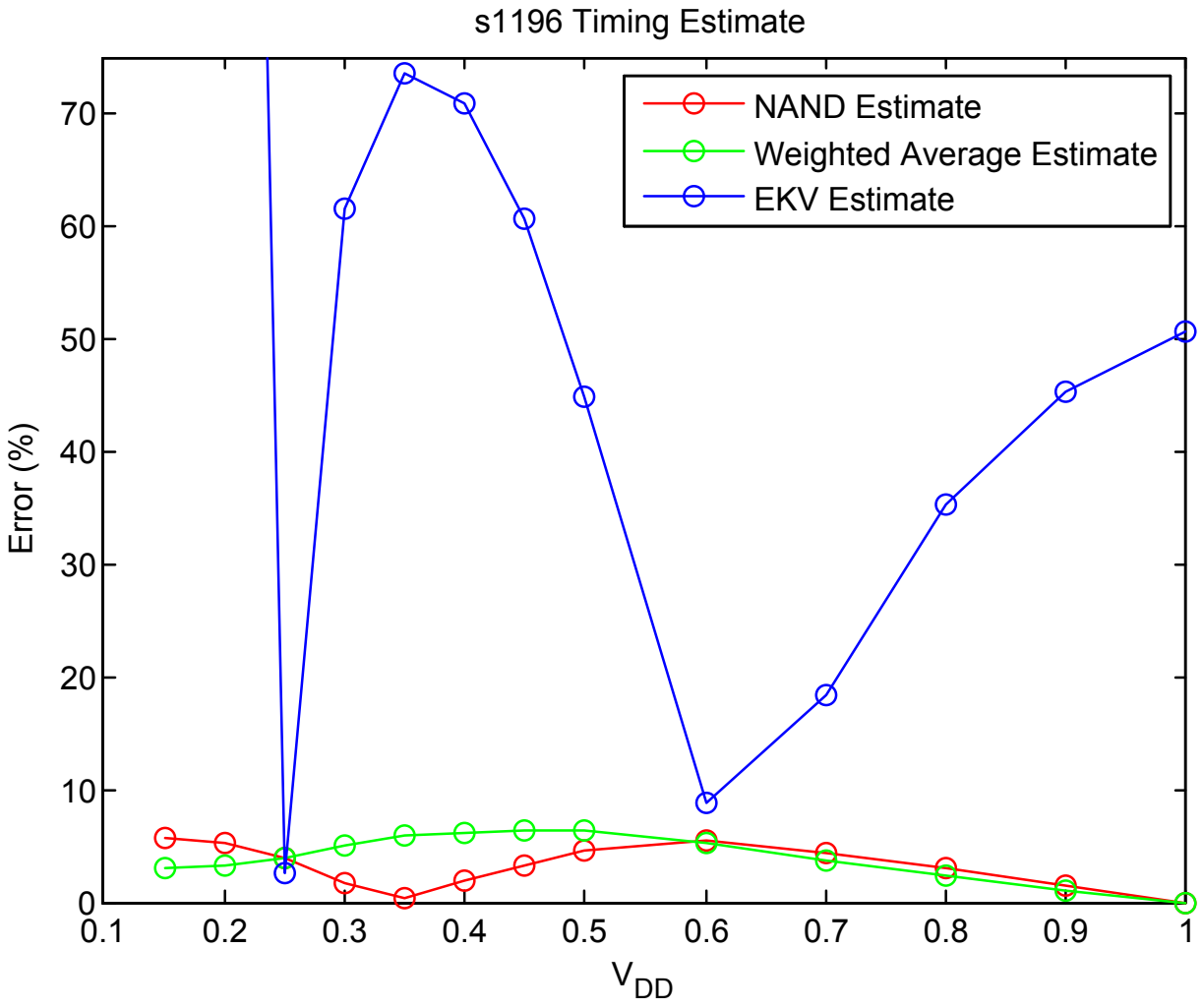

Figure 6.25: Timing delay error for s1196 with NAND, Weighted Average, and EKV estimates

Table 6.1: Maximum Error Rates for Different Circuits using Variations of the Framework ($0.25V < V_{DD} < 1.0V$ for Circuit Delay)

Circuit	**Leakage Power**			**Active Energy**			**Circuit Delay**		
	NAND Estimate	Weighted Average	EKV Modeling	NAND Estimate	Weighted Average	EKV Modeling	NAND Estimate	Weighted Average	EKV Modeling
s27	8.9024	3.7446	6.2243	6.8758	2.7478	7.4984	31.8854	10.5059	71.2
s298	8.2410	4.8639	5.0385	5.6080	7.7266	10.5306	39.7480	11.2690	71.5
s400	7.9035	4.0641	8.6278	16.8047	13.9939	15.8102	28.5790	2.4462	71.6
s1196	4.1156	2.0091	4.8869	17.5994	16.9633	16.6144	5.6754	6.2736	73.5

To illustrate the significance of the accuracy of this methodology, Table 6.1 provides a more comprehensive look by showing the absolute value of the maximum error with the estimation methodologies for various circuits. Note that Table 6.1's circuit delay data only shows the maximum error from a V_{DD} range of 0.25V to 1.0V for the EVK data due to the fact that the EKV model for timing is not highly accurate, especially in the ULV region. The error between the benchmark and the estimations derived through the methodologies illustrated in this thesis are minimal considering the framework only uses nominal values and at the lowest voltage, the circuits are more than 1000 times slower. Another consideration is that it took several hours to simulate each circuit across the range of voltages in SPICE, while the simulation framework took only seconds to obtain an estimate.

The general trend observed is that the EKV model has the worst estimation performance and the weighted averages technique has the best performance. Considering leakage power estimates, there was not a significant improvement in the weighted average estimate versus the NAND gate estimate. However, these two methods showed a noticeable improvement over the EKV model's estimation. With active power, the improvement the weighted average method has over the NAND estimate and the EKV model is slightly more distinct. However, the big gains come in with timing estimation. The EKV model does not fit the overall curve of the baseline very well, so the EKV model for timing is going to vastly over or underestimate the timing characteristic of a circuit. The NAND estimation method for timing is a significant improvement over the EKV model, but it still lacks some of the precision desired. The weighted average methodology, on the other hand, is usually at least twice as accurate, which is a marked improvement over the NAND estimation technique.

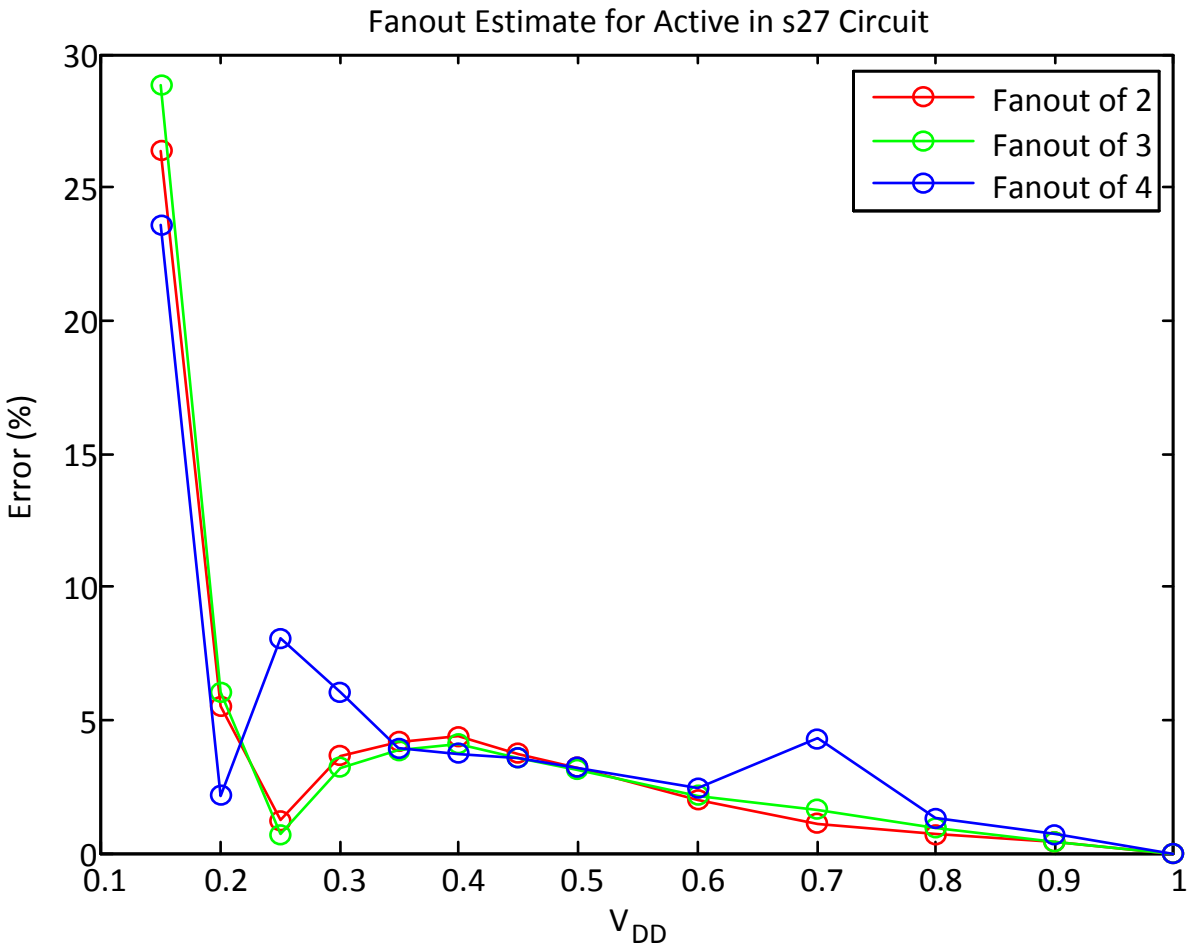

Figure 6.26: The effect of an increasing fanout as the base for estimating s27's active energy

6.2.1 Varying Base Ring Oscillator Test

For the experiments performed so far in this thesis, ring oscillators with a fanout of one have been used. This section considers what may happen to errors in active energy, leakage power, and timing delay if a more realistic ring oscillator base was used instead. Ring oscillators comprised of NAND gates with fanout of 2, 3, and 4 are evaluated as the new ring oscillator base. The following graphs will show that the amount of error does not change significantly after varying the baseline oscillator. Moreover, none of the oscillators outperforms all others for various circuits.

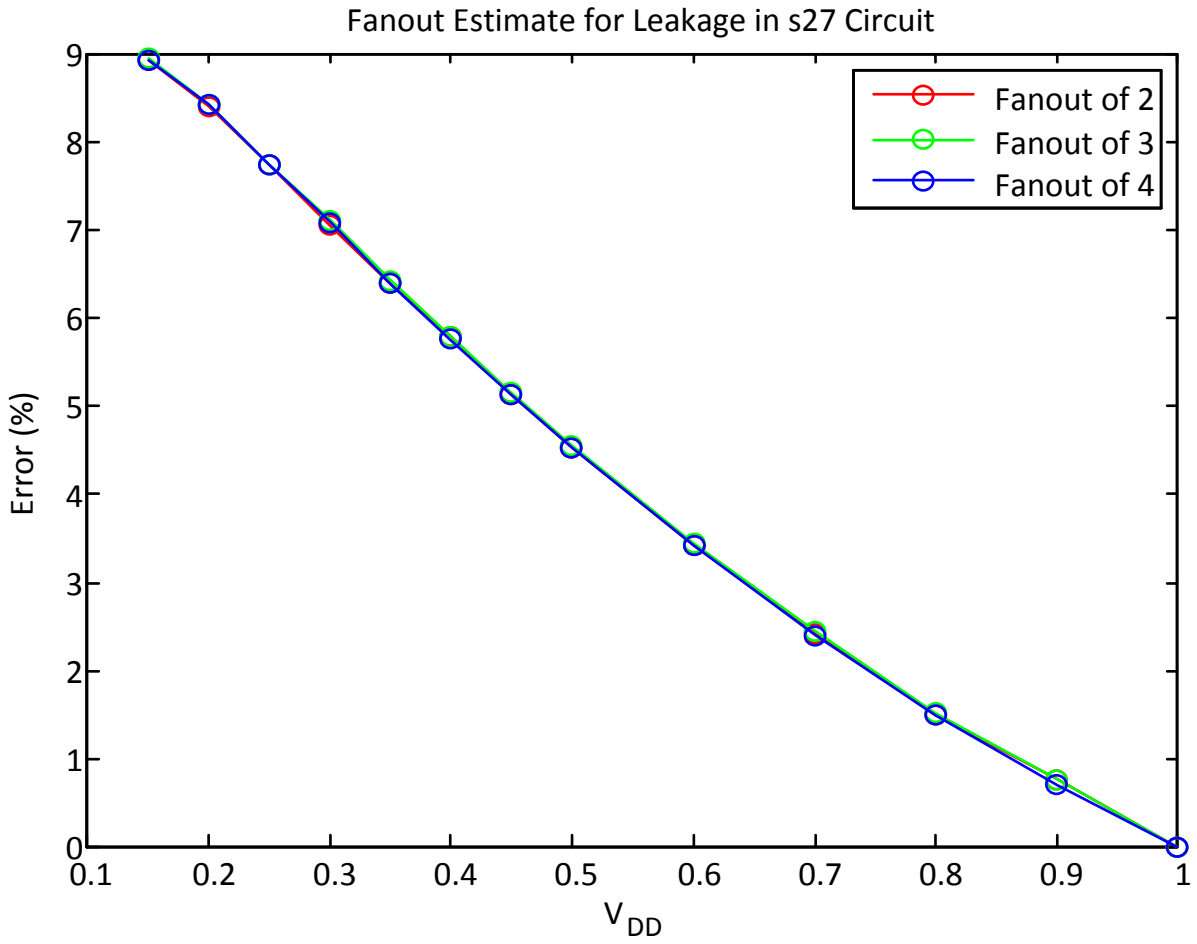

Figure 6.27: The effect of an increasing fanout as the base for estimating s27's leakage power

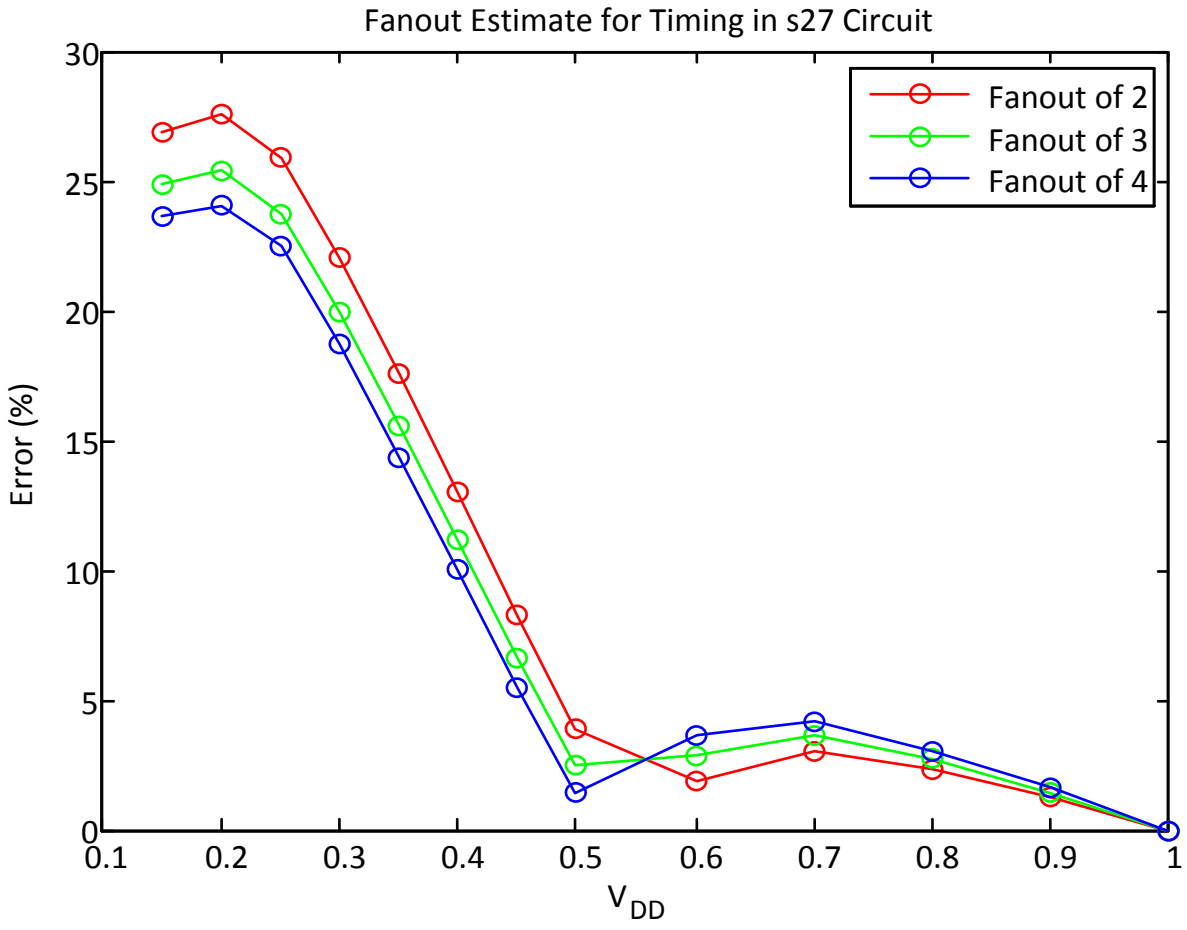

Figure 6.28: The effect of an increasing fanout as the base for estimating s27's timing delay

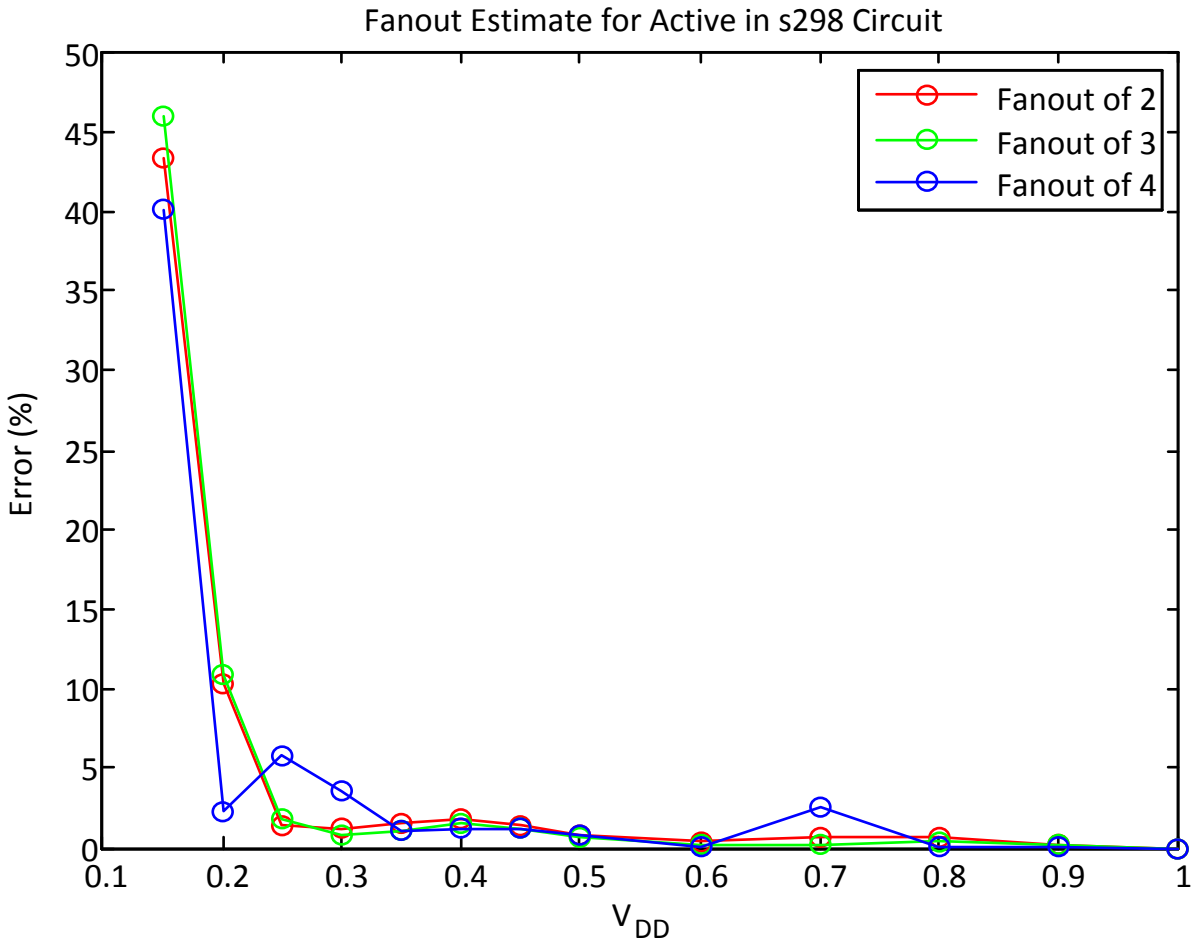

Figure 6.29: The effect of an increasing fanout as the base for estimating s298's active energy

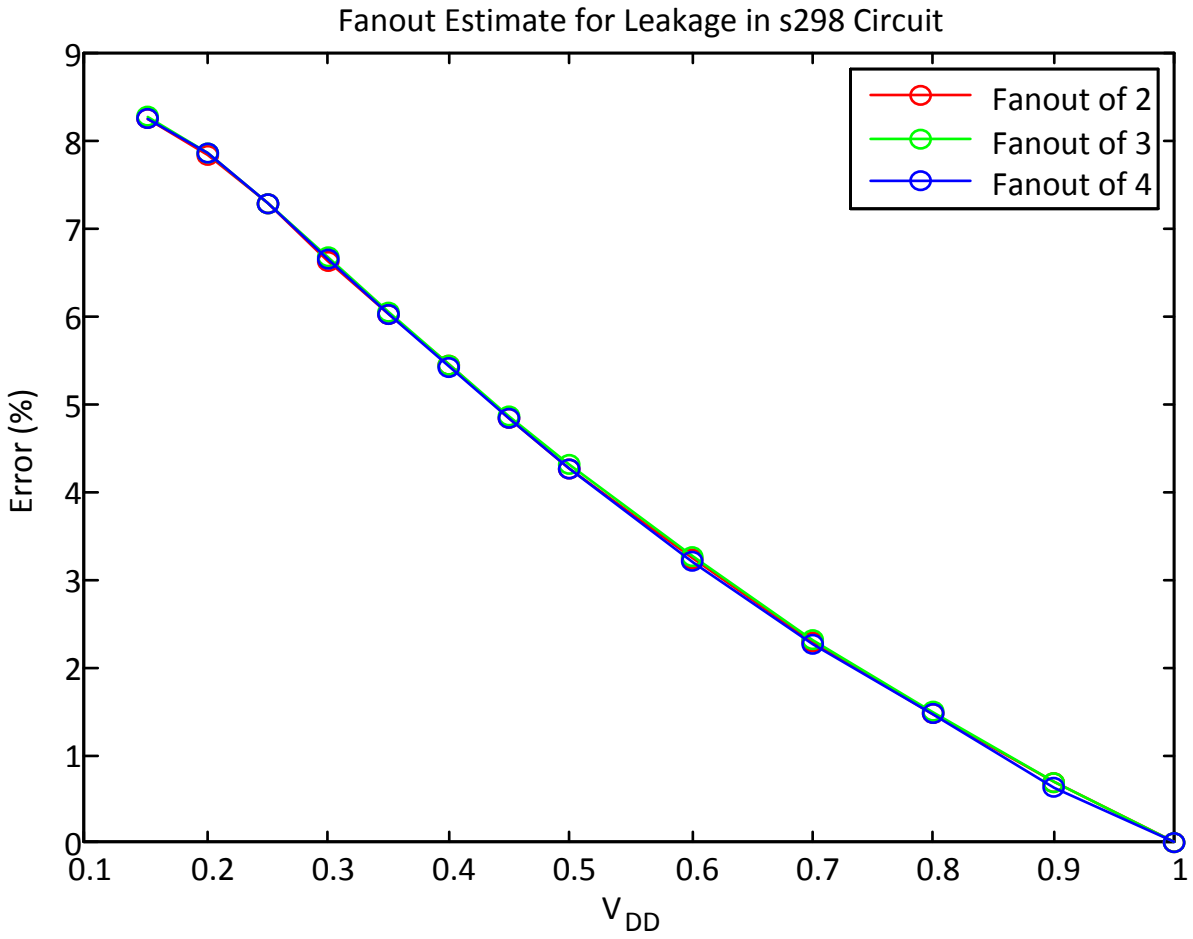

Figure 6.30: The effect of an increasing fanout as the base for estimating s298's leakage power

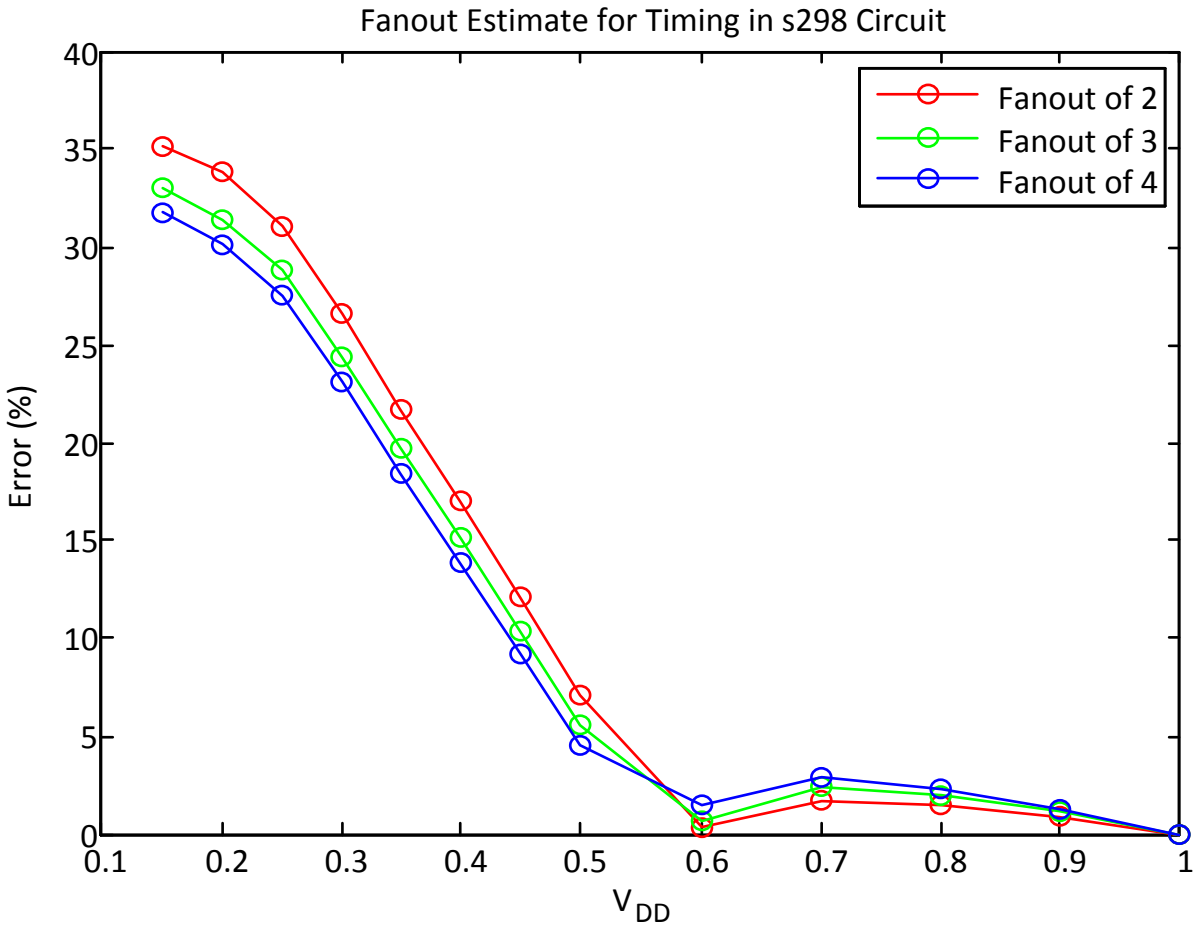

Figure 6.31: The effect of an increasing fanout as the base for estimating s298's timing delay

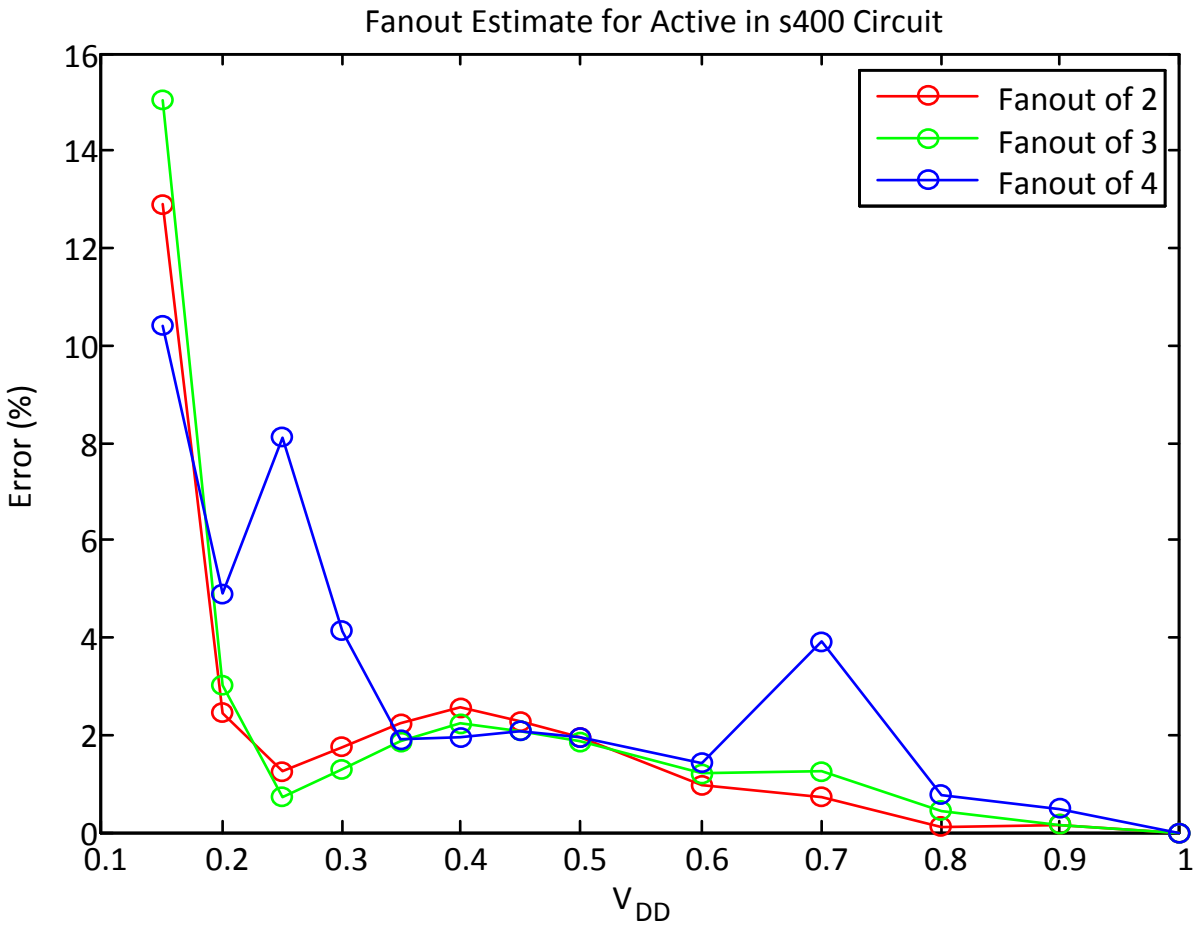

Figure 6.32: The effect of an increasing fanout as the base for estimating s400's active energy

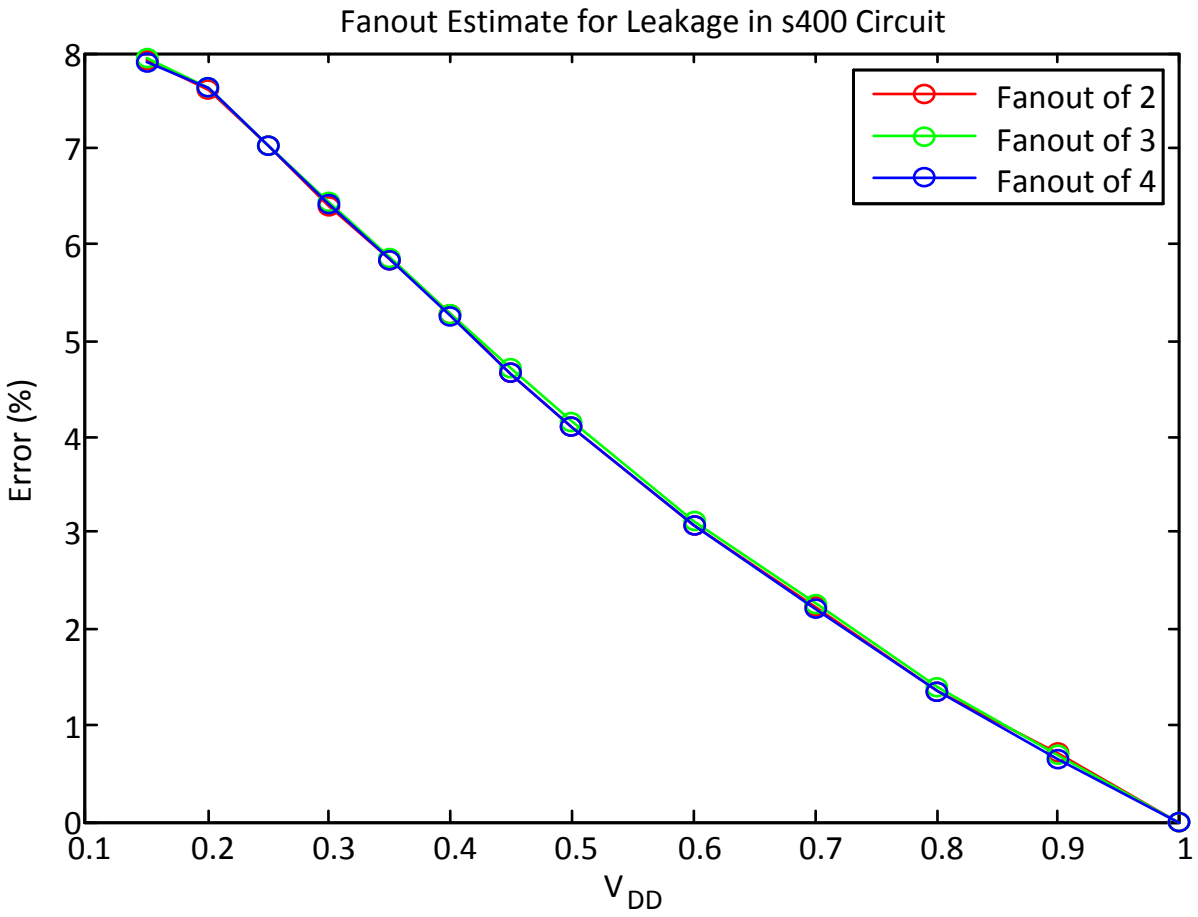

Figure 6.33: The effect of an increasing fanout as the base for estimating s400's leakage power

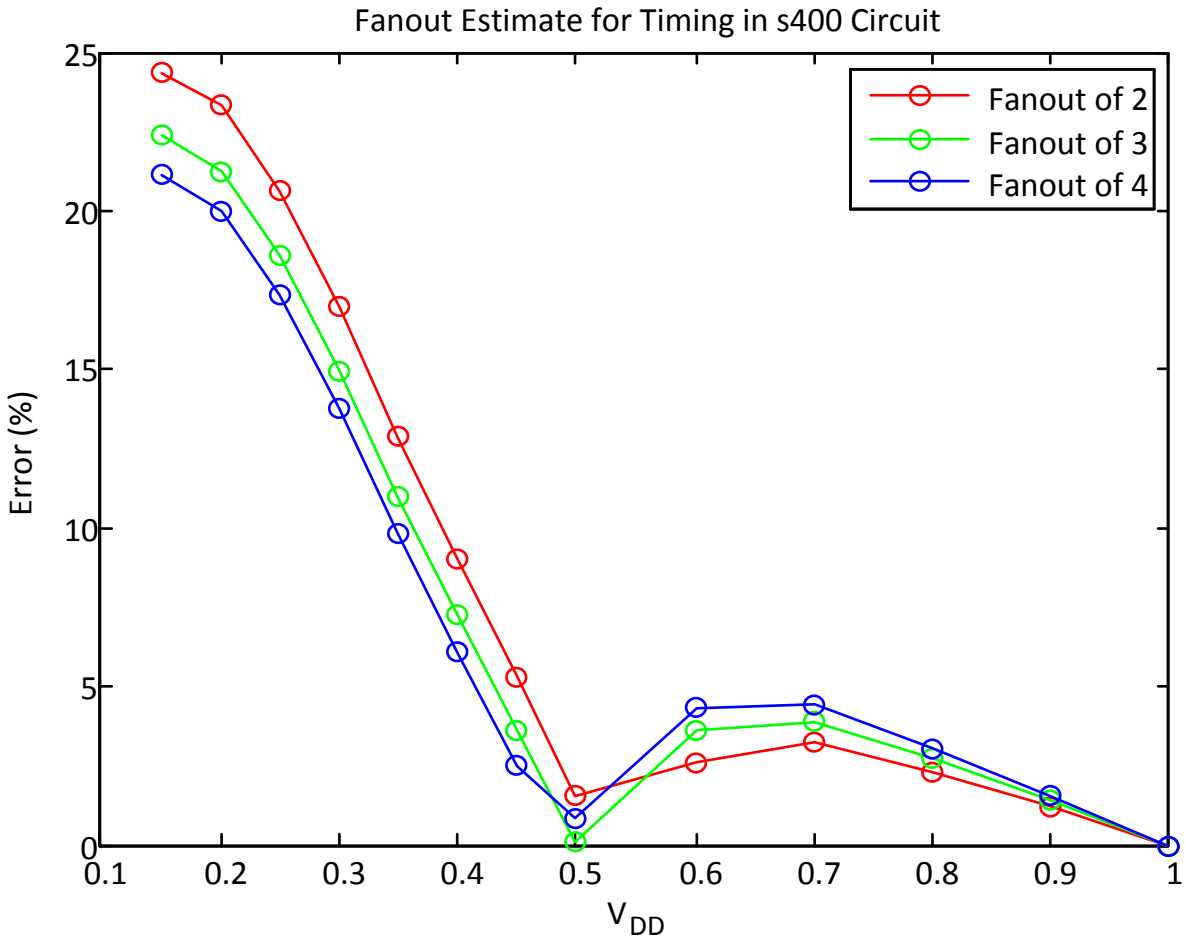

Figure 6.34: The effect of an increasing fanout as the base for estimating s400's timing delay

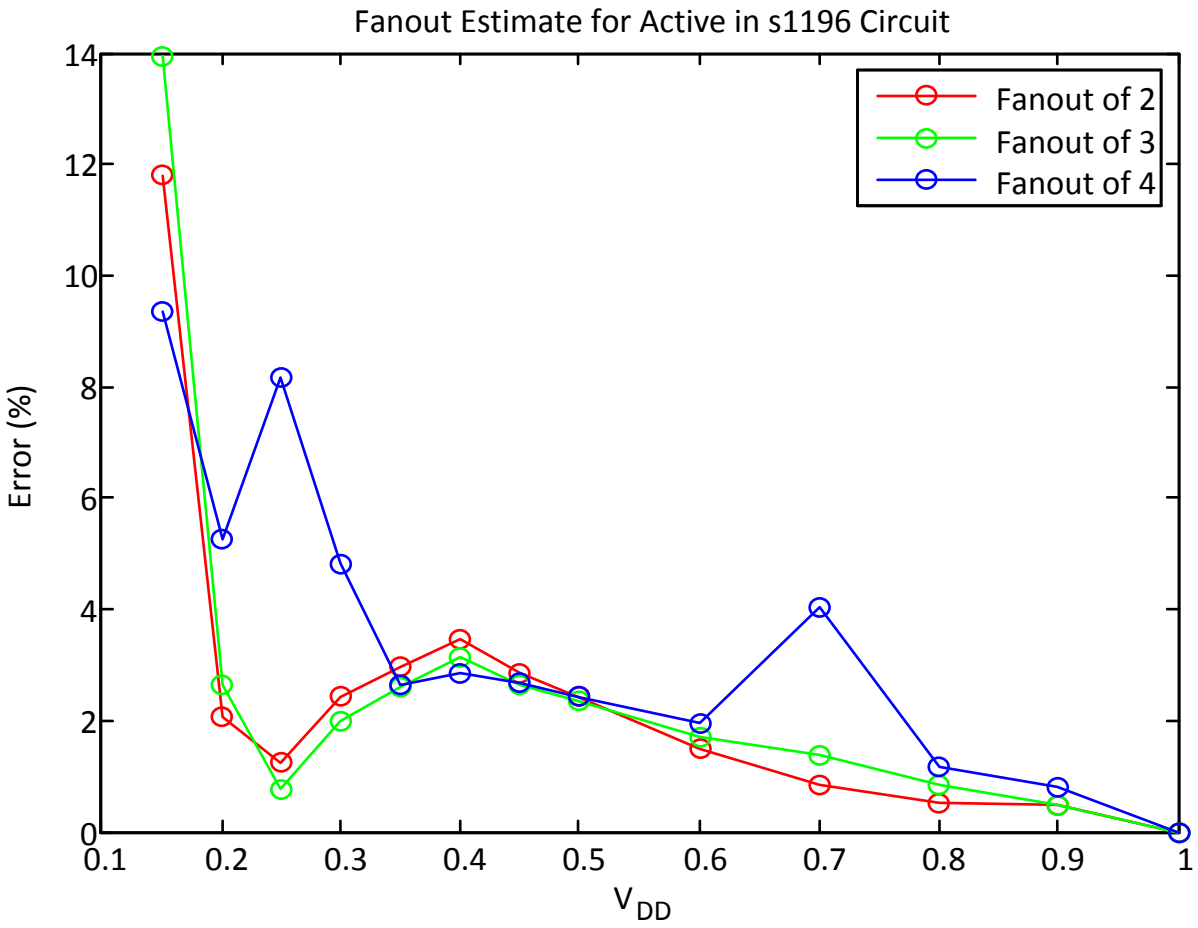

Figure 6.35: The effect of an increasing fanout as the base for estimating s1196's active energy

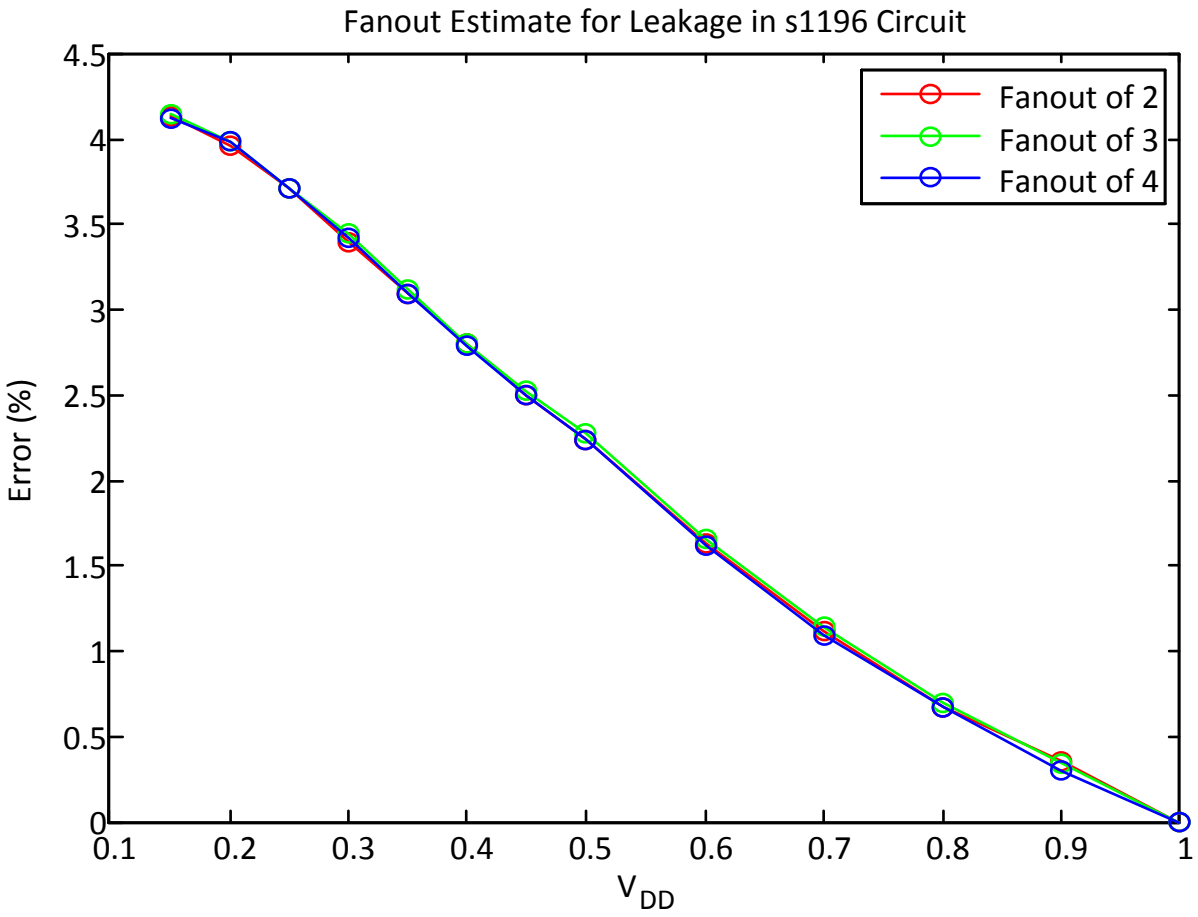

Figure 6.36: The effect of an increasing fanout as the base for estimating s1196's leakage power

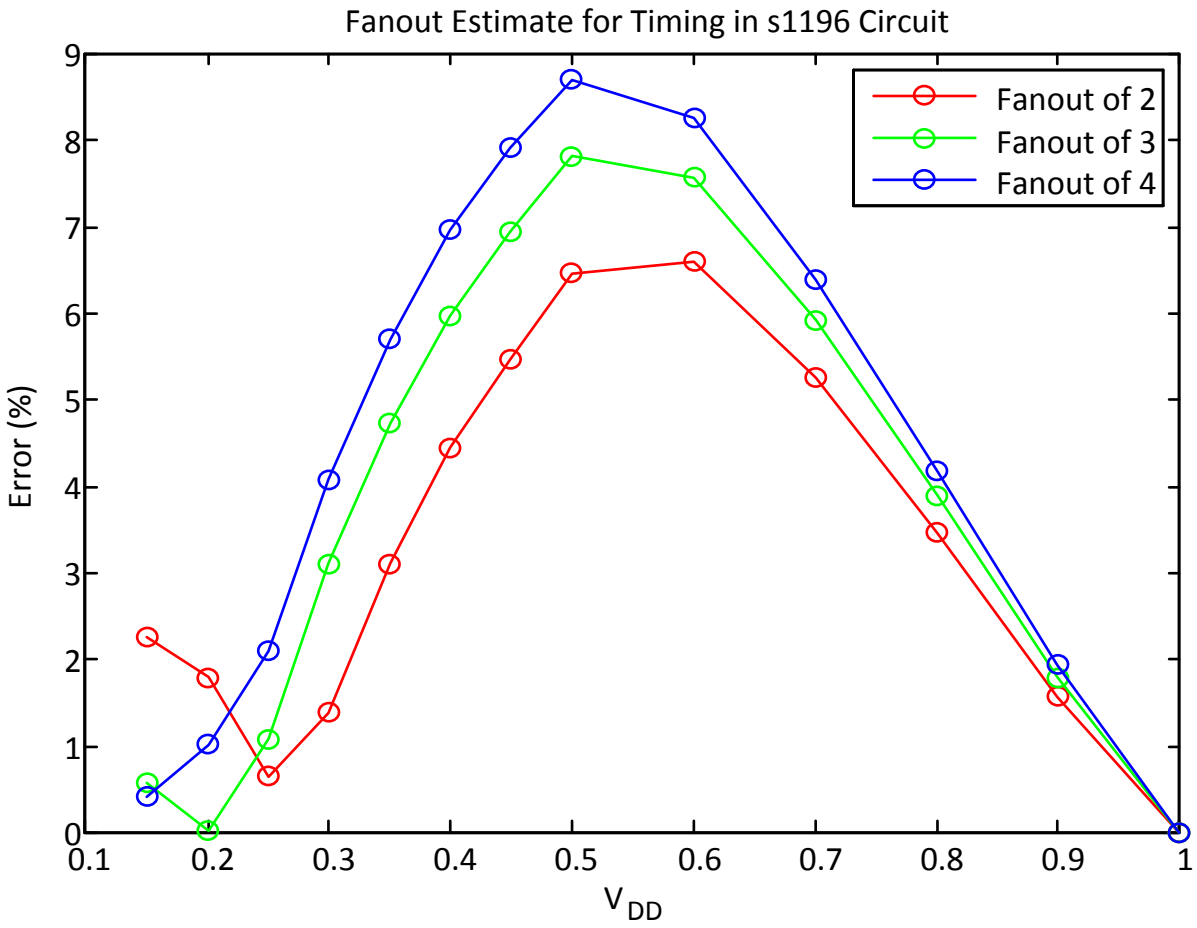

Figure 6.37: The effect of an increasing fanout as the base for estimating s1196's timing delay

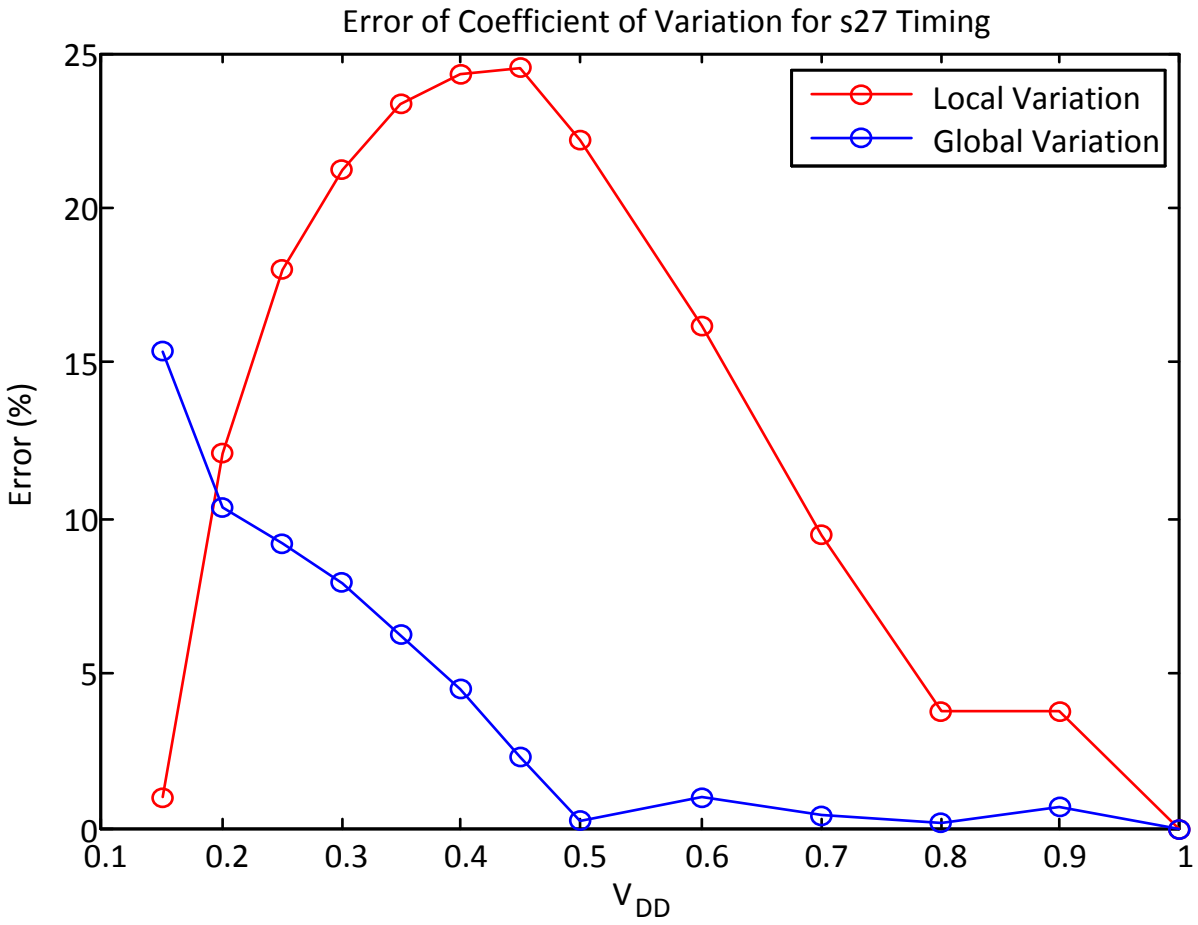

Figure 6.38: Error for coefficient of variation for timing delay in s27

6.3 Process Variation Consideration for Timing Delay

This section covers the estimation of local and global process variation using the methods described in this thesis. Because timing delay seems to be the most critical with regards to estimation methods, this thesis will focus on the effects of process variation on timing delay. Figures 6.38 to 6.41 show the error of the effects of local and global process variation on timing analysis.

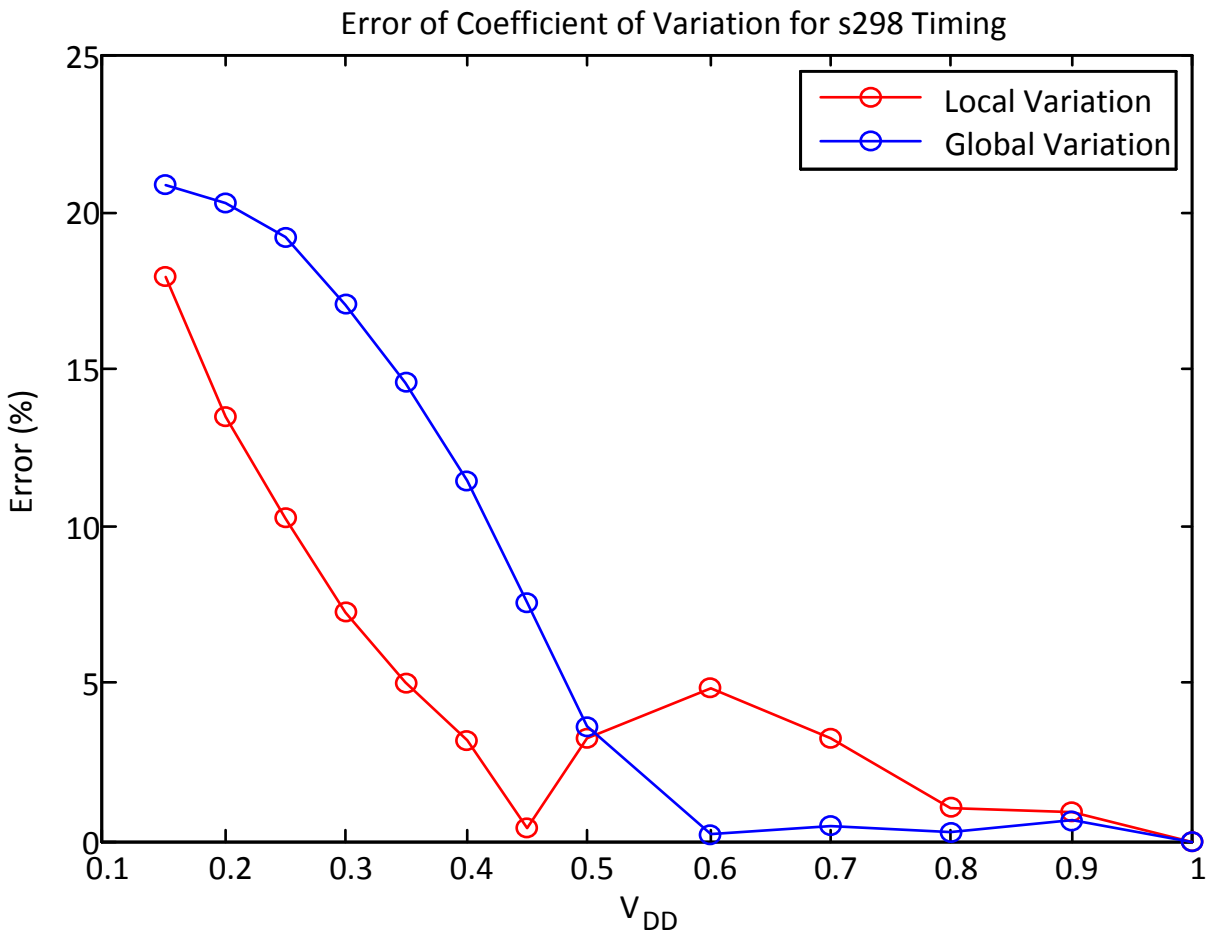

Figure 6.39: Error for coefficient of variation for timing delay in s298

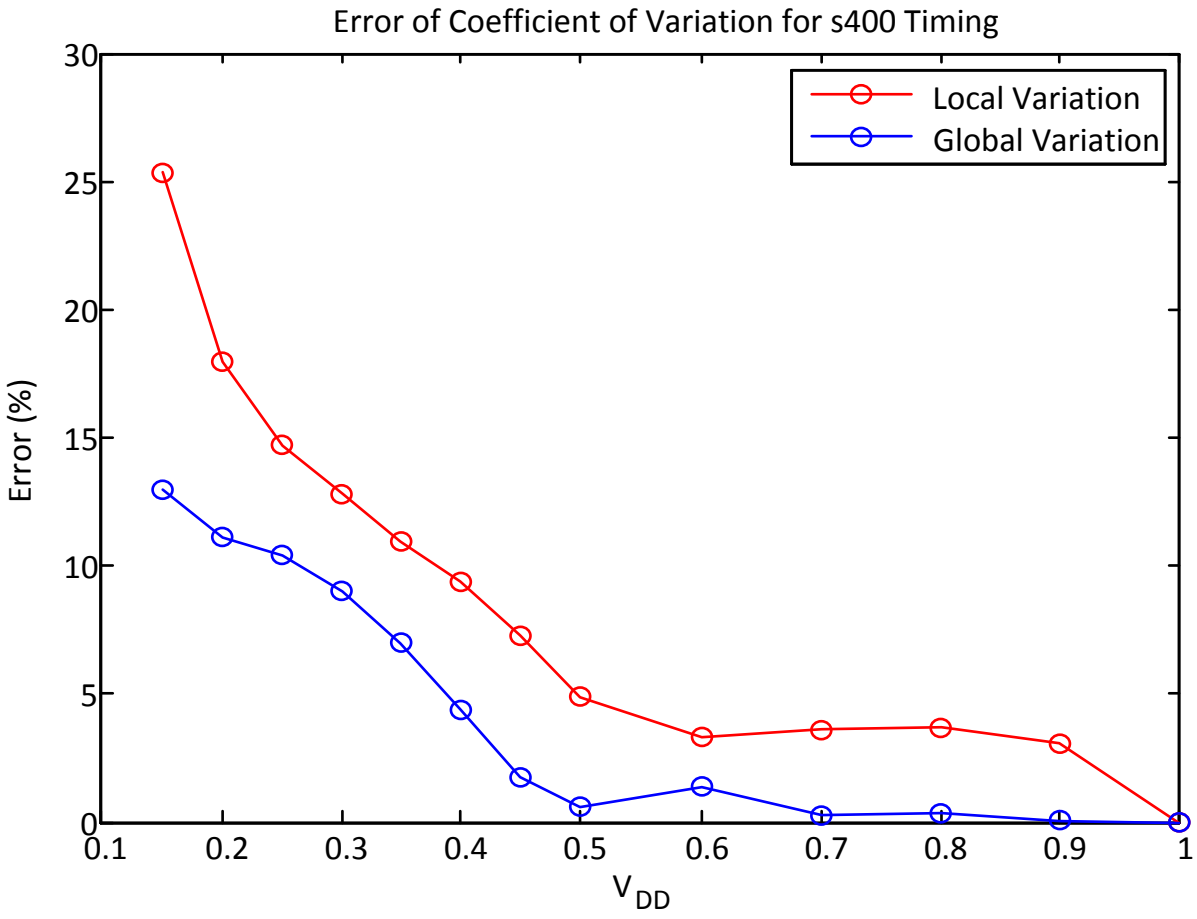

Figure 6.40: Error for coefficient of variation for timing delay in s400

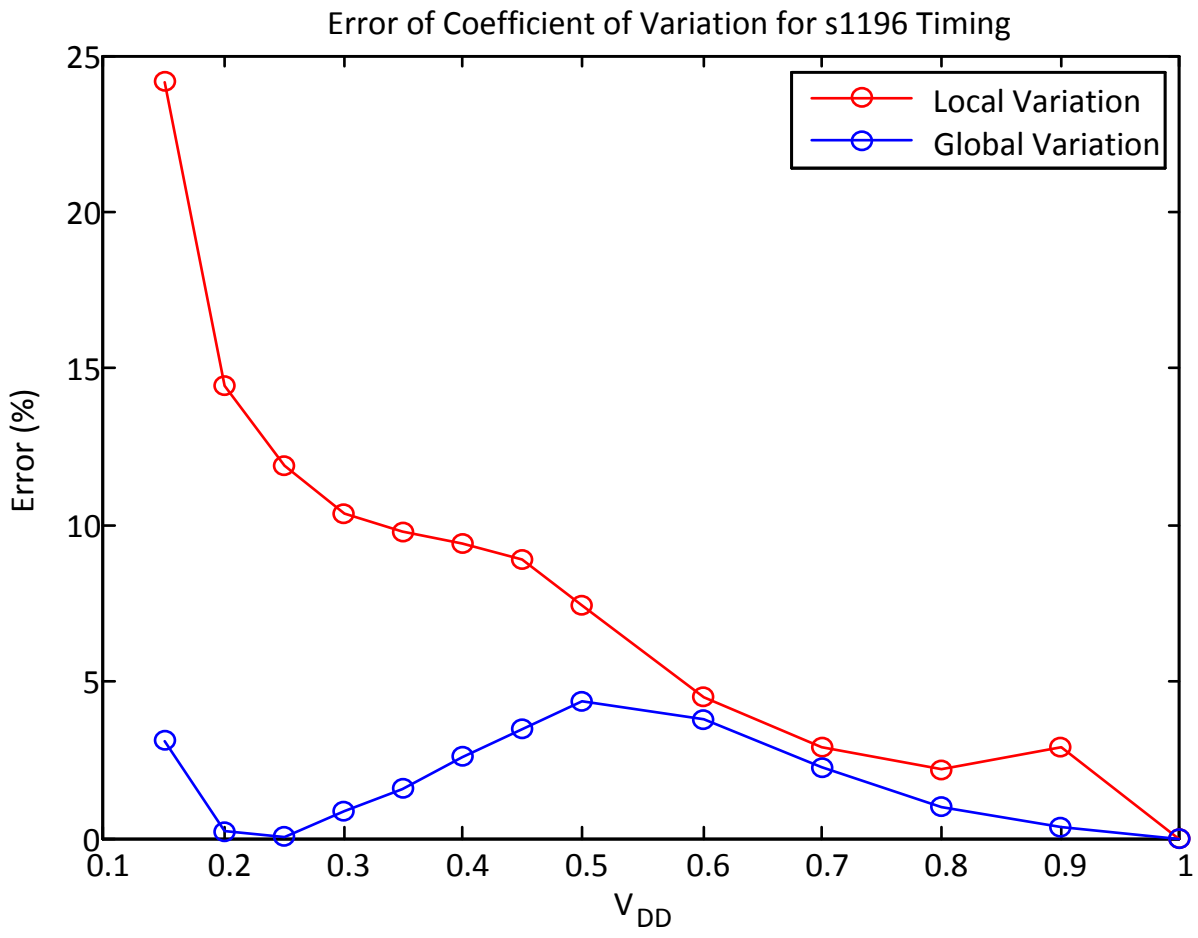

Figure 6.41: Error for coefficient of variation for timing delay in s1196

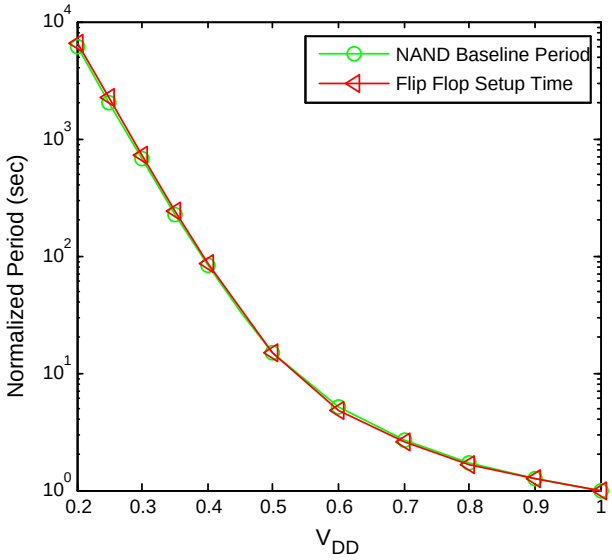

Figure 6.42: Baseline timing curve and normalized flip-flop setup requirement

6.4 Setup time Considerations

The simulation frameworks can also be used with sequential circuits. Figure 6.42 shows the baseline timing curve along with the normalized setup requirement of a flip flop. Because both of these normalized curves scale identically with a decreasing supply voltage, the framework can be used to estimate the critical delay of a sequential circuit. Hold times are not shown because as the supply voltage decreases, the hold requirement decreases. The delay to the flip flop increases with a reduces supply voltage, so as long as a circuit does not violate hold times at nominal voltage, it will not violate hold times and reduced voltages.

Chapter 7

Conclusion

This thesis presented a framework to quickly characterize the frequency and power consumption of a circuit across a wide range of voltages, including the ULV region. One problem with simulating circuits with low supply voltages is that transistor level simulations can take a long time due to the increased simulation time and accuracy requirements for the ULV region. The simulation framework addresses this issue by using only the nominal frequency and power of a circuit and multiplying them with normalized ring oscillator curves. Additionally, the framework presented is not a mathematical model, so many parameters that may be unknown in the target circuit are not needed. The framework was tested against a number of circuits that are both sequential as well as combinational. Despite the differences in order of magnitude with respect to frequency and power in different operating voltages, the estimates were accurate and only took a couple of seconds to obtain, while the HSpice simulations took many hours to complete. This technique proved to be even more accurate than the EKV Model, which is currently the standard methodology for estimating the frequency and power characteristics of a given circuit. Additionally, this thesis considers process variation and gives an example of using this framework to estimate the coefficient of variation. The speed and accuracy of this framework makes it useful for many applications including architectural comparisons, minimum energy point determination, and design space exploration.

Appendix A

Cell Measurements in Various Operating Corners

Table A.1: NAND Gate Measurements in Various Operating Corners

V_{DD}	**Active Energy**			**Leakage Power**			**Timing Delay**		
	Slow Corner	Typical Corner	Fast Corner	Slow Corner	Typical Corner	Fast Corner	Slow Corner	Typical Corner	Fast Corner
1	7.344e-14	7.765e-14	8.130e-14	1.108e-10	5.569e-10	3.278e-09	1.553e-09	1.160e-09	9.166e-10
0.9	5.899e-14	6.223e-14	6.511e-14	8.872e-11	4.449e-10	2.618e-09	2.050e-09	1.449e-09	1.097e-09
0.8	4.561e-14	4.851e-14	5.082e-14	6.993e-11	3.503e-10	2.062e-09	3.016e-09	1.949e-09	1.383e-09
0.7	3.410e-14	3.646e-14	3.832e-14	5.402e-11	2.708e-10	1.594e-09	5.407e-09	2.974e-09	1.894e-09
0.6	2.432e-14	2.609e-14	2.758e-14	4.064e-11	2.044e-10	1.205e-09	1.415e-08	5.752e-09	3.003e-09
0.5	1.627e-14	1.747e-14	1.856e-14	2.951e-11	1.494e-10	8.820e-10	6.753e-08	1.747e-08	6.324e-09
0.45	1.310e-14	1.387e-14	1.472e-14	2.471e-11	1.257e-10	7.429e-10	1.819e-07	3.858e-08	1.099e-08
0.4	1.032e-14	1.083e-14	1.139e-14	2.038e-11	1.043e-10	6.172e-10	5.341e-07	9.844e-08	2.241e-08
0.35	7.928e-15	8.288e-15	8.575e-15	1.649e-11	8.509e-11	5.040e-10	1.658e-06	2.778e-07	5.334e-08
0.3	5.878e-15	6.156e-15	6.298e-15	1.303e-11	6.783e-11	4.025e-10	5.309e-06	8.332e-07	1.425e-07
0.25	4.116e-15	4.392e-15	4.477e-15	9.961e-12	5.244e-11	3.118e-10	1.706e-05	2.571e-06	4.064e-07
0.2	2.657e-15	3.047e-15	3.087e-15	7.268e-12	3.880e-11	2.311e-10	5.345e-05	7.877e-06	1.183e-06
0.15	1.534e-15	2.239e-15	2.197e-15	4.932e-12	2.676e-11	1.598e-10	1.586e-04	2.311e-05	3.369e-06

Table A.2: NOR Gate Measurements in Various Operating Corners

V_{DD}	**Active Energy**			**Leakage Power**			**Timing Delay**		
	Slow Corner	Typical Corner	Fast Corner	Slow Corner	Typical Corner	Fast Corner	Slow Corner	Typical Corner	Fast Corner
1	5.732e-14	5.941e-14	6.212e-14	2.207e-10	1.043e-09	5.369e-09	2.278e-09	1.668e-09	1.292e-09
0.9	4.615e-14	4.774e-14	4.970e-14	1.770e-10	8.402e-10	4.290e-09	3.080e-09	2.128e-09	1.579e-09
0.8	3.614e-14	3.742e-14	3.883e-14	1.396e-10	6.669e-10	3.376e-09	4.640e-09	2.926e-09	2.034e-09
0.7	2.742e-14	2.836e-14	2.939e-14	1.079e-10	5.194e-10	2.607e-09	8.397e-09	4.540e-09	2.839e-09
0.6	1.976e-14	2.051e-14	2.132e-14	8.119e-11	3.950e-10	1.964e-09	2.101e-08	8.691e-09	4.537e-09
0.5	1.345e-14	1.393e-14	1.452e-14	5.898e-11	2.907e-10	1.432e-09	8.766e-08	2.411e-08	9.204e-09
0.45	1.085e-14	1.115e-14	1.162e-14	4.941e-11	2.455e-10	1.203e-09	2.185e-07	4.900e-08	1.512e-08
0.4	8.567e-15	8.730e-15	9.040e-15	4.077e-11	2.044e-10	9.972e-10	5.972e-07	1.143e-07	2.826e-08
0.35	6.564e-15	6.659e-15	6.841e-15	3.302e-11	1.673e-10	8.121e-10	1.737e-06	2.973e-07	6.081e-08
0.3	4.816e-15	4.895e-15	5.020e-15	2.612e-11	1.339e-10	6.467e-10	5.255e-06	8.296e-07	1.479e-07
0.25	3.312e-15	3.395e-15	3.558e-15	2.002e-11	1.041e-10	4.998e-10	1.608e-05	2.409e-06	3.900e-07
0.2	2.044e-15	2.164e-15	2.462e-15	1.469e-11	7.761e-11	3.704e-10	4.832e-05	7.040e-06	1.068e-06
0.15	9.848e-16	1.185e-15	1.776e-15	1.011e-11	5.456e-11	2.580e-10	1.382e-04	1.994e-05	2.920e-06

Table A.3: INV Gate Measurements in Various Operating Corners

V_{DD}	**Active Energy**			**Leakage Power**			**Timing Delay**		
	Slow Corner	Typical Corner	Fast Corner	Slow Corner	Typical Corner	Fast Corner	Slow Corner	Typical Corner	Fast Corner
1	3.987e-14	4.127e-14	4.295e-14	5.538e-11	2.784e-10	1.639e-09	1.097e-09	8.001e-10	6.170e-10
0.9	3.217e-14	3.330e-14	3.449e-14	4.436e-11	2.224e-10	1.309e-09	1.451e-09	9.990e-10	7.388e-10
0.8	2.518e-14	2.604e-14	2.702e-14	3.497e-11	1.751e-10	1.031e-09	2.143e-09	1.348e-09	9.309e-10
0.7	1.896e-14	1.971e-14	2.047e-14	2.701e-11	1.354e-10	7.972e-10	3.787e-09	2.035e-09	1.267e-09
0.6	1.363e-14	1.424e-14	1.485e-14	2.032e-11	1.022e-10	6.024e-10	9.641e-09	3.833e-09	1.980e-09
0.5	9.261e-15	9.641e-15	1.011e-14	1.476e-11	7.472e-11	4.410e-10	4.447e-08	1.100e-08	3.963e-09
0.45	7.441e-15	7.699e-15	8.061e-15	1.236e-11	6.287e-11	3.714e-10	1.182e-07	2.345e-08	6.575e-09
0.4	5.871e-15	6.020e-15	6.263e-15	1.019e-11	5.217e-11	3.086e-10	3.404e-07	5.815e-08	1.266e-08
0.35	4.499e-15	4.598e-15	4.727e-15	8.248e-12	4.254e-11	2.520e-10	1.037e-06	1.596e-07	2.866e-08
0.3	3.310e-15	3.403e-15	3.464e-15	6.515e-12	3.392e-11	2.012e-10	3.259e-06	4.662e-07	7.352e-08
0.25	2.307e-15	2.431e-15	2.461e-15	4.981e-12	2.622e-11	1.559e-10	1.032e-05	1.405e-06	2.027e-07
0.2	1.494e-15	1.712e-15	1.729e-15	3.634e-12	1.940e-11	1.156e-10	3.219e-05	4.261e-06	5.780e-07
0.15	8.764e-16	1.298e-15	1.306e-15	2.466e-12	1.338e-11	7.992e-11	9.599e-05	1.257e-05	1.643e-06

Table A.4: DFF Measurements in Various Operating Corners

V_{DD}	**Active Energy**			**Leakage Power**		
	Slow Corner	Typical Corner	Fast Corner	Slow Corner	Typical Corner	Fast Corner
1	6.299e-14	6.448e-14	6.653e-14	1.242e-10	5.936e-10	3.882e-09
0.9	5.081e-14	5.186e-14	5.326e-14	9.998e-11	4.759e-10	3.110e-09
0.8	3.987e-14	4.070e-14	4.165e-14	7.903e-11	3.756e-10	2.454e-09
0.7	3.023e-14	3.090e-14	3.159e-14	6.109e-11	2.908e-10	1.900e-09
0.6	2.192e-14	2.243e-14	2.296e-14	4.587e-11	2.195e-10	1.435e-09
0.5	1.502e-14	1.533e-14	1.571e-14	3.314e-11	1.602e-10	1.050e-09
0.45	1.213e-14	1.231e-14	1.260e-14	2.763e-11	1.346e-10	8.832e-10
0.4	9.594e-15	9.679e-15	9.861e-15	2.266e-11	1.115e-10	7.328e-10
0.35	7.353e-15	7.405e-15	7.492e-15	1.821e-11	9.073e-11	5.975e-10
0.3	5.399e-15	5.454e-15	5.494e-15	1.426e-11	7.214e-11	4.763e-10
0.25	3.713e-15	3.797e-15	3.845e-15	1.080e-11	5.562e-11	3.684e-10
0.2	2.265e-15	2.427e-15	2.526e-15	7.793e-12	4.109e-11	2.731e-10
0.15	1.020e-15	1.343e-15	1.545e-15	5.257e-12	2.850e-11	1.901e-10

Appendix B

Target Circuit Values

Table B.1: s27 Measurements in Various Operating Corners

V_{DD}	**Active Energy**			**Leakage Power**			**Timing Delay**		
	Slow Corner	Typical Corner	Fast Corner	Slow Corner	Typical Corner	Fast Corner	Slow Corner	Typical Corner	Fast Corner
1	1.349e-13	1.391e-13	1.449e-13	5.428e-10	2.486e-09	1.512e-08	5.202e-10	3.797e-10	2.933e-10
0.9	1.063e-13	1.117e-13	1.160e-13	4.364e-10	1.992e-09	1.211e-08	6.920e-10	4.793e-10	3.543e-10
0.8	8.334e-14	8.772e-14	9.062e-14	3.448e-10	1.573e-09	9.553e-09	1.029e-09	6.495e-10	4.490e-10
0.7	6.364e-14	6.654e-14	6.867e-14	2.665e-10	1.218e-09	7.395e-09	1.849e-09	9.946e-10	6.189e-10
0.6	4.620e-14	4.825e-14	4.991e-14	2.002e-10	9.202e-10	5.587e-09	4.660e-09	1.894e-09	9.807e-10
0.5	3.166e-14	3.284e-14	3.411e-14	1.448e-10	6.726e-10	4.086e-09	2.076e-08	5.397e-09	1.995e-09
0.45	2.560e-14	2.632e-14	2.734e-14	1.208e-10	5.656e-10	3.438e-09	5.385e-08	1.139e-08	3.324e-09
0.4	2.024e-14	2.072e-14	2.136e-14	9.923e-11	4.690e-10	2.853e-09	1.534e-07	2.776e-08	6.400e-09
0.35	1.557e-14	1.585e-14	1.620e-14	7.989e-11	3.821e-10	2.326e-09	4.600e-07	7.516e-08	1.434e-08
0.3	1.135e-14	1.170e-14	1.187e-14	6.271e-11	3.043e-10	1.855e-09	1.426e-06	2.168e-07	3.648e-08
0.25	7.742e-15	8.179e-15	8.411e-15	4.760e-11	2.351e-10	1.435e-09	4.473e-06	6.477e-07	1.000e-07
0.2	4.729e-15	5.379e-15	5.749e-15	3.449e-11	1.741e-10	1.064e-09	1.380e-05	1.955e-06	2.837e-07
0.15	2.110e-15	3.322e-15	3.980e-15	2.337e-11	1.212e-10	7.414e-10	4.132e-05	5.766e-06	8.121e-07

Table B.2: s298 Measurements in Various Operating Corners

V_{DD}	**Active Energy**			**Leakage Power**			**Timing Delay**		
	Slow Corner	Typical Corner	Fast Corner	Slow Corner	Typical Corner	Fast Corner	Slow Corner	Typical Corner	Fast Corner
1	1.362e-12	1.418e-12	1.490e-12	3.248e-09	1.591e-08	9.507e-08	1.364e-09	1.008e-09	7.830e-10
0.9	1.091e-12	1.132e-12	1.186e-12	2.614e-09	1.276e-08	7.619e-08	1.820e-09	1.268e-09	9.436e-10
0.8	8.488e-13	8.821e-13	9.203e-13	2.071e-09	1.007e-08	6.016e-08	2.682e-09	1.710e-09	1.194e-09
0.7	6.359e-13	6.660e-13	6.923e-13	1.605e-09	7.805e-09	4.662e-08	4.765e-09	2.606e-09	1.640e-09
0.6	4.596e-13	4.803e-13	4.997e-13	1.211e-09	5.900e-09	3.527e-08	1.200e-08	4.917e-09	2.567e-09
0.5	3.148e-13	3.264e-13	3.395e-13	8.798e-10	4.315e-09	2.584e-08	5.361e-08	1.391e-08	5.142e-09
0.45	2.536e-13	2.618e-13	2.721e-13	7.361e-10	3.630e-09	2.176e-08	1.399e-07	2.922e-08	8.490e-09
0.4	2.008e-13	2.058e-13	2.121e-13	6.069e-10	3.011e-09	1.808e-08	3.982e-07	7.117e-08	1.622e-08
0.35	1.544e-13	1.571e-13	1.527e-13	4.904e-10	2.454e-09	1.476e-08	1.196e-06	1.927e-07	3.620e-08
0.3	1.138e-13	1.163e-13	1.129e-13	3.868e-10	1.955e-09	1.178e-08	3.722e-06	5.551e-07	9.149e-08
0.25	7.546e-14	8.127e-14	7.992e-14	2.951e-10	1.511e-09	9.131e-09	1.166e-05	1.652e-06	2.496e-07
0.2	4.673e-14	5.242e-14	5.469e-14	2.153e-10	1.120e-09	6.785e-09	3.580e-05	4.950e-06	7.022e-07
0.15	2.375e-14	2.985e-14	3.422e-14	1.470e-10	7.804e-10	4.739e-09	1.053e-04	1.437e-05	1.964e-06

Table B.3: s400 Measurements in Various Operating Corners

V_{DD}	**Active Energy**			**Leakage Power**			**Timing Delay**		
	Slow Corner	Typical Corner	Fast Corner	Slow Corner	Typical Corner	Fast Corner	Slow Corner	Typical Corner	Fast Corner
1	6.842e-13	7.110e-13	7.439e-13	4.881e-09	2.325e-08	1.355e-07	1.434e-09	1.052e-09	8.121e-10
0.9	5.496e-13	5.700e-13	5.947e-13	3.926e-09	1.864e-08	1.085e-07	1.910e-09	1.327e-09	9.812e-10
0.8	4.234e-13	4.461e-13	4.644e-13	3.108e-09	1.473e-08	8.569e-08	2.840e-09	1.799e-09	1.250e-09
0.7	3.296e-13	3.388e-13	3.516e-13	2.406e-09	1.141e-08	6.640e-08	5.087e-09	2.763e-09	1.724e-09
0.6	2.287e-13	2.442e-13	2.549e-13	1.815e-09	8.633e-09	5.023e-08	1.298e-08	5.288e-09	2.733e-09
0.5	1.578e-13	1.657e-13	1.736e-13	1.316e-09	6.315e-09	3.679e-08	5.831e-08	1.530e-08	5.603e-09
0.45	1.284e-13	1.325e-13	1.388e-13	1.100e-09	5.312e-09	3.098e-08	1.522e-07	3.247e-08	9.431e-09
0.4	1.019e-13	1.039e-13	1.081e-13	9.068e-10	4.407e-09	2.572e-08	4.330e-07	7.973e-08	1.839e-08
0.35	7.772e-14	7.940e-14	8.189e-14	7.322e-10	3.592e-09	2.099e-08	1.305e-06	2.168e-07	4.169e-08
0.3	5.729e-14	5.862e-14	6.030e-14	5.776e-10	2.863e-09	1.675e-08	4.065e-06	6.268e-07	1.065e-07
0.25	3.971e-14	4.183e-14	4.288e-14	4.405e-10	2.213e-09	1.297e-08	1.275e-05	1.873e-06	2.922e-07
0.2	2.493e-14	2.829e-14	2.993e-14	3.215e-10	1.640e-09	9.629e-09	3.905e-05	5.603e-06	8.260e-07
0.15	1.255e-14	1.900e-14	2.194e-14	2.204e-10	1.144e-09	6.720e-09	1.145e-04	1.630e-05	2.328e-06

Table B.4: s1196 Measurements in Various Operating Corners

V_{DD}	**Active Energy**			**Leakage Power**			**Timing Delay**		
	Slow Corner	Typical Corner	Fast Corner	Slow Corner	Typical Corner	Fast Corner	Slow Corner	Typical Corner	Fast Corner
1	5.926e-13	6.133e-13	6.437e-13	1.051e-08	4.877e-08	3.429e-07	1.408e-09	1.037e-09	8.014e-10
0.9	4.652e-13	4.931e-13	5.147e-13	8.485e-09	3.924e-08	2.755e-07	1.886e-09	1.313e-09	9.722e-10
0.8	3.728e-13	3.863e-13	4.018e-13	6.740e-09	3.111e-08	2.182e-07	2.820e-09	1.795e-09	1.247e-09
0.7	2.778e-13	2.926e-13	3.043e-13	5.239e-09	2.420e-08	1.697e-07	5.118e-09	2.781e-09	1.737e-09
0.6	2.005e-13	2.118e-13	2.208e-13	3.957e-09	1.837e-08	1.289e-07	1.343e-08	5.435e-09	2.798e-09
0.5	1.380e-13	1.436e-13	1.505e-13	2.885e-09	1.349e-08	9.480e-08	6.302e-08	1.638e-08	5.915e-09
0.45	1.111e-13	1.149e-13	1.204e-13	2.423e-09	1.138e-08	8.004e-08	1.671e-07	3.564e-08	1.021e-08
0.4	8.838e-14	9.049e-14	9.391e-14	2.004e-09	9.466e-09	6.664e-08	4.845e-07	8.964e-08	2.052e-08
0.35	6.777e-14	6.902e-14	7.107e-14	1.626e-09	7.736e-09	5.455e-08	1.477e-06	2.490e-07	4.798e-08
0.3	4.967e-14	5.092e-14	5.234e-14	1.285e-09	6.180e-09	4.366e-08	4.657e-06	7.330e-07	1.256e-07
0.25	3.453e-14	3.610e-14	3.751e-14	9.845e-10	4.791e-09	3.392e-08	1.469e-05	2.213e-06	3.515e-07
0.2	2.173e-14	2.449e-14	2.680e-14	7.221e-10	3.561e-09	2.527e-08	4.519e-05	6.694e-06	1.009e-06
0.15	1.091e-14	1.655e-14	2.054e-14	4.960e-10	2.487e-09	1.769e-08	1.323e-04	1.955e-05	2.890e-06

Appendix C

Ring Oscillator Variation Experiments

Table C.1: NAND Active Energy Gate Measurements with Varying Critical Path Lengths

	Active Energy			
V_{DD}	15 cells	21 cells	25 cells	31 cells
1	1.057e-13	1.499e-13	1.793e-13	2.232e-13
0.9	8.459e-14	1.200e-13	1.435e-13	1.787e-13
0.8	6.578e-14	9.357e-14	1.119e-13	1.393e-13
0.7	4.944e-14	7.029e-14	8.401e-14	1.031e-13
0.6	3.576e-14	5.064e-14	6.054e-14	7.541e-14
0.5	2.391e-14	3.385e-14	4.047e-14	5.040e-14
0.45	1.890e-14	2.681e-14	3.205e-14	4.003e-14
0.4	1.481e-14	2.095e-14	2.507e-14	3.128e-14
0.35	1.132e-14	1.610e-14	1.921e-14	2.390e-14
0.3	8.636e-15	1.181e-14	1.419e-14	1.679e-14
0.25	6.093e-15	8.408e-15	1.016e-14	1.138e-14
0.2	3.711e-15	5.248e-15	5.940e-15	6.607e-15
0.15	1.137e-15	1.561e-15	1.736e-15	1.714e-15

Table C.2: NAND Leakage Power Gate Measurements with Varying Critical Path Lengths

	Leakage Power			
V_{DD}	15 cells	21 cells	25 cells	31 cells
1	8.938e-10	1.277e-09	1.532e-09	1.915e-09
0.9	7.214e-10	1.031e-09	1.237e-09	1.546e-09
0.8	5.740e-10	8.200e-10	9.840e-10	1.230e-09
0.7	4.485e-10	6.407e-10	7.688e-10	9.610e-10
0.6	3.422e-10	4.888e-10	5.866e-10	7.332e-10
0.5	2.528e-10	3.611e-10	4.333e-10	5.417e-10
0.45	2.138e-10	3.054e-10	3.665e-10	4.581e-10
0.4	1.783e-10	2.548e-10	3.057e-10	3.821e-10
0.35	1.462e-10	2.088e-10	2.506e-10	3.132e-10
0.3	1.171e-10	1.673e-10	2.008e-10	2.510e-10
0.25	9.106e-11	1.301e-10	1.561e-10	1.951e-10
0.2	6.785e-11	9.693e-11	1.163e-10	1.454e-10
0.15	4.746e-11	6.781e-11	8.137e-11	1.017e-10

Table C.3: NAND Timing Delay Gate Measurements with Varying Critical Path Lengths

	Timing			
V_{DD}	15 cells	21 cells	25 cells	31 cells
1	1.582e-09	2.217e-09	2.640e-09	3.275e-09
0.9	1.977e-09	2.768e-09	3.297e-09	4.090e-09
0.8	2.660e-09	3.725e-09	4.436e-09	5.502e-09
0.7	4.058e-09	5.684e-09	6.770e-09	8.399e-09
0.6	7.847e-09	1.099e-08	1.309e-08	1.624e-08
0.5	2.384e-08	3.340e-08	3.977e-08	4.936e-08
0.45	5.266e-08	7.380e-08	8.789e-08	1.091e-07
0.4	1.344e-07	1.884e-07	2.245e-07	2.787e-07
0.35	3.793e-07	5.320e-07	6.341e-07	7.874e-07
0.3	1.138e-06	1.597e-06	1.903e-06	2.363e-06
0.25	3.513e-06	4.927e-06	5.869e-06	7.282e-06
0.2	1.076e-05	1.506e-05	1.793e-05	2.224e-05
0.15	3.154e-05	4.417e-05	5.258e-05	6.521e-05

Table C.4: NAND Gate Measurements with Varying Fanouts

	Active Energy			**Leakage Power**			**Timing Delay**		
V_{DD}	FO 2	FO 3	FO 4	FO 2	FO 3	FO 4	FO 2	FO 3	FO 4
1	1.652e-13	2.533e-13	3.415e-13	1.277e-09	1.915e-09	2.554e-09	1.875e-09	2.607e-09	3.346e-09
0.9	1.322e-13	2.027e-13	2.724e-13	1.031e-09	1.546e-09	2.061e-09	2.337e-09	3.242e-09	4.155e-09
0.8	1.035e-13	1.582e-13	2.126e-13	8.200e-10	1.230e-09	1.640e-09	3.133e-09	4.337e-09	5.550e-09
0.7	7.816e-14	1.192e-13	1.564e-13	6.407e-10	9.610e-10	1.281e-09	4.764e-09	6.578e-09	8.400e-09
0.6	5.619e-14	8.596e-14	1.156e-13	4.888e-10	7.332e-10	9.775e-10	9.178e-09	1.263e-08	1.609e-08
0.5	3.775e-14	5.794e-14	7.803e-14	3.611e-10	5.417e-10	7.222e-10	2.770e-08	3.797e-08	4.825e-08
0.45	3.008e-14	4.621e-14	6.228e-14	3.054e-10	4.581e-10	6.108e-10	6.092e-08	8.338e-08	1.059e-07
0.4	2.353e-14	3.620e-14	4.895e-14	2.548e-10	3.821e-10	5.095e-10	1.549e-07	2.119e-07	2.691e-07
0.35	1.803e-14	2.774e-14	3.739e-14	2.088e-10	3.132e-10	4.176e-10	4.363e-07	5.964e-07	7.576e-07
0.3	1.333e-14	2.054e-14	2.690e-14	1.673e-10	2.510e-10	3.347e-10	1.307e-06	1.786e-06	2.269e-06
0.25	9.405e-15	1.450e-14	1.807e-14	1.301e-10	1.951e-10	2.602e-10	4.027e-06	5.504e-06	6.991e-06
0.2	5.973e-15	9.238e-15	1.140e-14	9.693e-11	1.454e-10	1.939e-10	1.232e-05	1.683e-05	2.138e-05
0.15	2.089e-15	3.447e-15	4.286e-15	6.781e-11	1.017e-10	1.356e-10	3.614e-05	4.943e-05	6.282e-05

Table C.5: NAND Gate Active Energy Measurements with Varying Transistor Widths

	Active Energy								
V_{DD}	X2	X3	X4	X5	X6	X7	X8	X9	X10
1	6.262e-14	8.659e-14	1.103e-13	1.339e-13	1.575e-13	1.811e-13	2.046e-13	2.282e-13	2.518e-13
0.9	5.014e-14	6.924e-14	8.808e-14	1.068e-13	1.256e-13	1.444e-13	1.632e-13	1.819e-13	2.007e-13
0.8	3.901e-14	5.381e-14	6.841e-14	8.291e-14	9.739e-14	1.119e-13	1.264e-13	1.409e-13	1.554e-13
0.7	2.931e-14	4.029e-14	5.115e-14	6.193e-14	7.269e-14	8.346e-14	9.422e-14	1.050e-13	1.157e-13
0.6	2.094e-14	2.870e-14	3.659e-14	4.393e-14	5.189e-14	5.911e-14	6.719e-14	7.482e-14	8.246e-14
0.5	1.401e-14	1.913e-14	2.416e-14	2.915e-14	3.415e-14	3.914e-14	4.413e-14	4.912e-14	5.410e-14
0.45	1.109e-14	1.510e-14	1.904e-14	2.295e-14	2.685e-14	3.077e-14	3.466e-14	3.856e-14	4.246e-14
0.4	8.641e-15	1.174e-14	1.478e-14	1.780e-14	2.082e-14	2.382e-14	2.684e-14	2.986e-14	3.285e-14
0.35	6.658e-15	9.043e-15	1.139e-14	1.370e-14	1.603e-14	1.833e-14	2.065e-14	2.297e-14	2.532e-14
0.3	5.041e-15	6.857e-15	8.693e-15	1.044e-14	1.222e-14	1.400e-14	1.579e-14	1.758e-14	1.938e-14
0.25	3.993e-15	5.386e-15	6.849e-15	8.316e-15	9.793e-15	1.124e-14	1.261e-14	1.405e-14	1.550e-14
0.2	3.190e-15	4.918e-15	5.860e-15	7.258e-15	8.876e-15	1.033e-14	8.167e-15	9.230e-15	1.470e-14
0.15	3.270e-15	4.931e-15	6.751e-15	8.586e-15	1.065e-14	1.228e-14	1.436e-14	1.614e-14	1.772e-14

Table C.6: NAND Gate Leakage Power Measurements with Varying Transistor Widths

	Leakage Power								
V_{DD}	X2	X3	X4	X5	X6	X7	X8	X9	X10
1	1.672e-09	2.775e-09	3.897e-09	5.027e-09	6.160e-09	7.294e-09	8.430e-09	9.566e-09	1.070e-08
0.9	1.348e-09	2.238e-09	3.144e-09	4.057e-09	4.973e-09	5.891e-09	6.809e-09	7.728e-09	8.648e-09
0.8	1.072e-09	1.780e-09	2.502e-09	3.230e-09	3.960e-09	4.692e-09	5.425e-09	6.158e-09	6.892e-09
0.7	8.368e-10	1.391e-09	1.956e-09	2.527e-09	3.099e-09	3.673e-09	4.247e-09	4.822e-09	5.397e-09
0.6	6.385e-10	1.062e-09	1.495e-09	1.932e-09	2.370e-09	2.810e-09	3.250e-09	3.691e-09	4.132e-09
0.5	4.721e-10	7.860e-10	1.107e-09	1.432e-09	1.757e-09	2.084e-09	2.411e-09	2.739e-09	3.066e-09
0.45	3.996e-10	6.658e-10	9.383e-10	1.213e-09	1.490e-09	1.767e-09	2.045e-09	2.323e-09	2.601e-09
0.4	3.337e-10	5.563e-10	7.844e-10	1.015e-09	1.246e-09	1.479e-09	1.711e-09	1.944e-09	2.177e-09
0.35	2.739e-10	4.570e-10	6.447e-10	8.344e-10	1.025e-09	1.216e-09	1.408e-09	1.600e-09	1.791e-09
0.3	2.199e-10	3.673e-10	5.184e-10	6.712e-10	8.248e-10	9.788e-10	1.133e-09	1.288e-09	1.442e-09
0.25	1.714e-10	2.865e-10	4.047e-10	5.242e-10	6.444e-10	7.649e-10	8.856e-10	1.007e-09	1.128e-09
0.2	1.281e-10	2.144e-10	3.031e-10	3.928e-10	4.830e-10	5.735e-10	6.642e-10	7.550e-10	8.459e-10
0.15	8.995e-11	1.508e-10	2.134e-10	2.768e-10	3.405e-10	4.044e-10	4.684e-10	5.326e-10	5.968e-10

Table C.7: NAND Gate Timing Delay Measurements with Varying Transistor Widths

	Timing Delay								
V_{DD}	X2	X3	X4	X5	X6	X7	X8	X9	X10
1	1.013e-09	1.235e-09	1.778e-09	1.243e-08	2.203e-08	4.954e-08	6.509e-07	1.320e-06	3.376e-06
0.9	9.751e-10	1.216e-09	5.752e-09	1.140e-08	2.133e-08	4.868e-08	5.421e-07	1.245e-06	3.286e-06
0.8	9.500e-10	1.202e-09	4.700e-09	1.077e-08	2.080e-08	2.778e-07	4.818e-07	1.193e-06	3.215e-06
0.7	9.320e-10	1.190e-09	4.163e-09	1.035e-08	2.040e-08	2.206e-07	4.450e-07	1.154e-06	2.311e-05
0.6	9.184e-10	2.973e-09	3.870e-09	1.005e-08	2.008e-08	1.856e-07	4.209e-07	1.124e-06	1.688e-05
0.5	9.078e-10	2.429e-09	3.689e-09	9.831e-09	9.842e-08	1.660e-07	4.038e-07	1.101e-06	1.369e-05
0.45	8.995e-10	2.171e-09	3.569e-09	9.662e-09	7.922e-08	1.540e-07	3.913e-07	7.877e-06	1.198e-05
0.4	1.949e-09	2.033e-09	3.484e-09	9.526e-09	6.737e-08	1.461e-07	3.817e-07	5.895e-06	1.096e-05
0.35	1.596e-09	1.947e-09	3.421e-09	3.858e-08	6.072e-08	1.406e-07	3.741e-07	4.818e-06	1.029e-05
0.3	1.434e-09	1.890e-09	3.371e-09	3.136e-08	5.664e-08	1.364e-07	2.571e-06	4.235e-06	9.830e-06
0.25	1.349e-09	1.850e-09	3.332e-09	2.699e-08	5.395e-08	1.333e-07	1.969e-06	3.883e-06	9.488e-06
0.2	1.295e-09	1.820e-09	1.747e-08	2.454e-08	5.204e-08	1.308e-07	1.624e-06	3.654e-06	9.228e-06
0.15	1.261e-09	1.797e-09	1.428e-08	2.303e-08	5.063e-08	8.331e-07	1.435e-06	3.494e-06	9.021e-06

Appendix D

Process Variation Experiments

Table D.1: NAND Gate Timing Delay Measurements with Local Process Variation

V_{DD}	Timing Delay									
1	1.160e-09	1.169e-09	1.151e-09	1.149e-09	1.160e-09	1.148e-09	1.172e-09	1.169e-09	1.152e-09	1.180e-09
	1.150e-09	1.148e-09	1.141e-09	1.168e-09	1.184e-09	1.153e-09	1.158e-09	1.158e-09	1.165e-09	1.168e-09
	1.179e-09	1.152e-09	1.158e-09	1.169e-09	1.173e-09	1.167e-09	1.164e-09	1.170e-09	1.154e-09	1.153e-09
	1.156e-09	1.155e-09	1.151e-09	1.146e-09	1.172e-09	1.152e-09	1.166e-09	1.163e-09	1.167e-09	1.164e-09
0.9	1.450e-09	1.462e-09	1.436e-09	1.435e-09	1.450e-09	1.432e-09	1.466e-09	1.464e-09	1.439e-09	1.476e-09
	1.436e-09	1.433e-09	1.422e-09	1.462e-09	1.483e-09	1.440e-09	1.448e-09	1.448e-09	1.459e-09	1.462e-09
	1.478e-09	1.439e-09	1.446e-09	1.462e-09	1.469e-09	1.460e-09	1.456e-09	1.465e-09	1.439e-09	1.440e-09
	1.443e-09	1.441e-09	1.438e-09	1.431e-09	1.468e-09	1.440e-09	1.457e-09	1.454e-09	1.460e-09	1.454e-09
0.8	1.951e-09	1.972e-09	1.927e-09	1.928e-09	1.951e-09	1.920e-09	1.975e-09	1.975e-09	1.937e-09	1.991e-09
	1.929e-09	1.925e-09	1.905e-09	1.972e-09	2.002e-09	1.937e-09	1.952e-09	1.950e-09	1.969e-09	1.972e-09
	2.000e-09	1.934e-09	1.944e-09	1.971e-09	1.983e-09	1.970e-09	1.962e-09	1.978e-09	1.931e-09	1.936e-09
	1.941e-09	1.936e-09	1.932e-09	1.923e-09	1.981e-09	1.938e-09	1.962e-09	1.958e-09	1.969e-09	1.953e-09
0.7	2.979e-09	3.023e-09	2.931e-09	2.939e-09	2.978e-09	2.913e-09	3.023e-09	3.031e-09	2.958e-09	3.055e-09
	2.940e-09	2.936e-09	2.889e-09	3.023e-09	3.075e-09	2.958e-09	2.992e-09	2.986e-09	3.023e-09	3.027e-09
	3.084e-09	2.950e-09	2.965e-09	3.018e-09	3.046e-09	3.022e-09	3.004e-09	3.037e-09	2.935e-09	2.955e-09
	2.961e-09	2.950e-09	2.944e-09	2.934e-09	3.044e-09	2.960e-09	3.000e-09	2.996e-09	3.019e-09	2.974e-09
0.6	5.779e-09	5.917e-09	5.644e-09	5.681e-09	5.774e-09	5.586e-09	5.882e-09	5.940e-09	5.751e-09	5.982e-09
	5.676e-09	5.685e-09	5.530e-09	5.911e-09	6.030e-09	5.734e-09	5.854e-09	5.830e-09	5.927e-09	5.935e-09
	6.093e-09	5.719e-09	5.738e-09	5.882e-09	5.977e-09	5.925e-09	5.853e-09	5.952e-09	5.635e-09	5.728e-09
	5.743e-09	5.705e-09	5.688e-09	5.689e-09	5.981e-09	5.742e-09	5.834e-09	5.844e-09	5.904e-09	5.735e-09
0.5	1.770e-08	1.844e-08	1.707e-08	1.726e-08	1.766e-08	1.674e-08	1.807e-08	1.855e-08	1.774e-08	1.866e-08
	1.721e-08	1.740e-08	1.654e-08	1.833e-08	1.877e-08	1.750e-08	1.822e-08	1.813e-08	1.851e-08	1.853e-08
	1.927e-08	1.754e-08	1.749e-08	1.811e-08	1.865e-08	1.854e-08	1.803e-08	1.852e-08	1.691e-08	1.751e-08
	1.762e-08	1.743e-08	1.727e-08	1.748e-08	1.877e-08	1.755e-08	1.793e-08	1.811e-08	1.833e-08	1.736e-08
0.45	3.928e-08	4.137e-08	3.766e-08	3.815e-08	3.918e-08	3.674e-08	4.015e-08	4.167e-08	3.962e-08	4.191e-08
	3.799e-08	3.867e-08	3.625e-08	4.097e-08	4.204e-08	3.876e-08	4.086e-08	4.064e-08	4.155e-08	4.159e-08
	4.356e-08	3.904e-08	3.875e-08	4.028e-08	4.182e-08	4.170e-08	4.015e-08	4.146e-08	3.709e-08	3.885e-08
	3.922e-08	3.869e-08	3.813e-08	3.896e-08	4.228e-08	3.888e-08	3.989e-08	4.052e-08	4.100e-08	3.830e-08
0.4	1.006e-07	1.070e-07	9.604e-08	9.739e-08	1.004e-07	9.326e-08	1.030e-07	1.078e-07	1.021e-07	1.085e-07
	9.689e-08	9.923e-08	9.188e-08	1.056e-07	1.085e-07	9.906e-08	1.056e-07	1.050e-07	1.075e-07	1.076e-07
	1.133e-07	1.003e-07	9.916e-08	1.033e-07	1.081e-07	1.080e-07	1.031e-07	1.069e-07	9.410e-08	9.954e-08
	1.008e-07	9.919e-08	9.724e-08	1.002e-07	1.097e-07	9.942e-08	1.024e-07	1.044e-07	1.057e-07	9.768e-08
0.35	2.846e-07	3.048e-07	2.708e-07	2.747e-07	2.843e-07	2.621e-07	2.917e-07	3.075e-07	2.904e-07	3.092e-07
	2.733e-07	2.812e-07	2.578e-07	3.000e-07	3.085e-07	2.796e-07	3.009e-07	2.991e-07	3.068e-07	3.066e-07
	3.243e-07	2.847e-07	2.806e-07	2.924e-07	3.075e-07	3.082e-07	2.926e-07	3.039e-07	2.644e-07	2.816e-07
	2.861e-07	2.811e-07	2.740e-07	2.845e-07	3.133e-07	2.809e-07	2.905e-07	2.965e-07	3.006e-07	2.756e-07
0.3	8.544e-07	9.202e-07	8.114e-07	8.233e-07	8.546e-07	7.837e-07	8.774e-07	9.298e-07	8.760e-07	9.345e-07
	8.192e-07	8.456e-07	7.693e-07	9.043e-07	9.305e-07	8.380e-07	9.087e-07	9.029e-07	9.277e-07	9.262e-07
	9.828e-07	8.578e-07	8.434e-07	8.785e-07	9.282e-07	9.317e-07	8.813e-07	9.163e-07	7.905e-07	8.458e-07
	8.622e-07	8.456e-07	8.204e-07	8.571e-07	9.484e-07	8.428e-07	8.746e-07	8.924e-07	9.068e-07	8.265e-07
0.25	2.637e-06	2.850e-06	2.501e-06	2.538e-06	2.639e-06	2.411e-06	2.713e-06	2.883e-06	2.710e-06	2.896e-06
	2.525e-06	2.612e-06	2.364e-06	2.800e-06	2.880e-06	2.585e-06	2.814e-06	2.794e-06	2.876e-06	2.870e-06
	3.052e-06	2.653e-06	2.605e-06	2.712e-06	2.875e-06	2.887e-06	2.726e-06	2.836e-06	2.433e-06	2.611e-06
	2.667e-06	2.611e-06	2.528e-06	2.650e-06	2.943e-06	2.601e-06	2.705e-06	2.757e-06	2.806e-06	2.550e-06
0.2	8.084e-06	8.741e-06	7.658e-06	7.776e-06	8.085e-06	7.372e-06	8.323e-06	8.849e-06	8.300e-06	8.888e-06
	7.727e-06	8.003e-06	7.229e-06	8.596e-06	8.842e-06	7.924e-06	8.629e-06	8.562e-06	8.821e-06	8.806e-06
	9.381e-06	8.132e-06	7.979e-06	8.312e-06	8.828e-06	8.857e-06	8.362e-06	8.707e-06	7.440e-06	8.002e-06
	8.181e-06	7.987e-06	7.745e-06	8.117e-06	9.043e-06	7.976e-06	8.297e-06	8.451e-06	8.603e-06	7.817e-06
0.15	2.377e-05	2.566e-05	2.248e-05	2.284e-05	2.376e-05	2.160e-05	2.451e-05	2.599e-05	2.435e-05	2.613e-05
	2.268e-05	2.348e-05	2.121e-05	2.529e-05	2.604e-05	2.332e-05	2.528e-05	2.514e-05	2.588e-05	2.587e-05
	2.759e-05	2.389e-05	2.343e-05	2.441e-05	2.600e-05	2.603e-05	2.456e-05	2.561e-05	2.184e-05	2.351e-05
	2.411e-05	2.338e-05	2.278e-05	2.380e-05	2.669e-05	2.353e-05	2.439e-05	2.485e-05	2.524e-05	2.302e-05

Table D.2: NAND Gate Timing Delay Measurements with Global Process Variation

V_{DD}	Timing Delay									
1	1.130e-09	1.223e-09	1.172e-09	1.187e-09	1.160e-09	1.099e-09	1.159e-09	1.099e-09	1.171e-09	1.260e-09
	1.159e-09	1.232e-09	1.270e-09	1.170e-09	1.201e-09	1.122e-09	1.184e-09	1.172e-09	1.146e-09	1.208e-09
	1.179e-09	1.234e-09	1.185e-09	1.174e-09	1.115e-09	1.159e-09	1.138e-09	1.178e-09	1.163e-09	1.107e-09
	1.218e-09	1.217e-09	1.161e-09	1.143e-09	1.130e-09	1.092e-09	1.127e-09	1.131e-09	1.179e-09	1.175e-09
0.9	1.403e-09	1.547e-09	1.470e-09	1.488e-09	1.450e-09	1.359e-09	1.449e-09	1.358e-09	1.470e-09	1.594e-09
	1.453e-09	1.561e-09	1.614e-09	1.464e-09	1.501e-09	1.393e-09	1.491e-09	1.471e-09	1.435e-09	1.522e-09
	1.479e-09	1.562e-09	1.487e-09	1.471e-09	1.384e-09	1.447e-09	1.422e-09	1.479e-09	1.455e-09	1.376e-09
	1.534e-09	1.532e-09	1.449e-09	1.428e-09	1.401e-09	1.351e-09	1.404e-09	1.404e-09	1.475e-09	1.466e-09
0.8	1.868e-09	2.123e-09	1.991e-09	2.011e-09	1.954e-09	1.801e-09	1.947e-09	1.796e-09	1.991e-09	2.184e-09
	1.963e-09	2.146e-09	2.228e-09	1.972e-09	2.021e-09	1.857e-09	2.029e-09	1.992e-09	1.937e-09	2.076e-09
	2.004e-09	2.142e-09	2.014e-09	1.987e-09	1.847e-09	1.943e-09	1.914e-09	2.003e-09	1.962e-09	1.839e-09
	2.092e-09	2.086e-09	1.945e-09	1.922e-09	1.865e-09	1.789e-09	1.880e-09	1.871e-09	1.990e-09	1.966e-09
0.7	2.799e-09	3.356e-09	3.075e-09	3.092e-09	2.991e-09	2.682e-09	2.968e-09	2.657e-09	3.080e-09	3.442e-09
	3.017e-09	3.396e-09	3.557e-09	3.023e-09	3.081e-09	2.797e-09	3.164e-09	3.076e-09	2.985e-09	3.246e-09
	3.096e-09	3.385e-09	3.108e-09	3.057e-09	2.790e-09	2.959e-09	2.928e-09	3.089e-09	3.013e-09	2.780e-09
	3.264e-09	3.253e-09	2.960e-09	2.946e-09	2.794e-09	2.658e-09	2.848e-09	2.807e-09	3.058e-09	2.984e-09
0.6	5.234e-09	6.947e-09	6.089e-09	6.070e-09	5.826e-09	4.978e-09	5.728e-09	4.843e-09	6.143e-09	7.072e-09
	5.899e-09	7.029e-09	7.486e-09	5.921e-09	5.943e-09	5.307e-09	6.389e-09	6.094e-09	5.934e-09	6.593e-09
	6.139e-09	7.002e-09	6.141e-09	6.017e-09	5.360e-09	5.724e-09	5.709e-09	6.082e-09	5.940e-09	5.313e-09
	6.575e-09	6.575e-09	5.696e-09	5.801e-09	5.226e-09	4.895e-09	5.457e-09	5.264e-09	6.009e-09	5.708e-09
0.5	1.494e-08	2.361e-08	1.927e-08	1.887e-08	1.796e-08	1.420e-08	1.732e-08	1.319e-08	1.987e-08	2.377e-08
	1.810e-08	2.374e-08	2.608e-08	1.857e-08	1.789e-08	1.581e-08	2.094e-08	1.934e-08	1.925e-08	2.185e-08
	1.949e-08	2.387e-08	1.933e-08	1.889e-08	1.652e-08	1.751e-08	1.773e-08	1.891e-08	1.894e-08	1.600e-08
	2.129e-08	2.161e-08	1.712e-08	1.855e-08	1.499e-08	1.366e-08	1.640e-08	1.514e-08	1.887e-08	1.698e-08
0.45	3.177e-08	5.518e-08	4.348e-08	4.215e-08	4.004e-08	3.041e-08	3.815e-08	2.726e-08	4.555e-08	5.529e-08
	4.002e-08	5.521e-08	6.161e-08	4.188e-08	3.925e-08	3.473e-08	4.818e-08	4.375e-08	4.433e-08	5.060e-08
	4.406e-08	5.599e-08	4.349e-08	4.248e-08	3.712e-08	3.894e-08	3.973e-08	4.214e-08	4.312e-08	3.535e-08
	4.853e-08	4.986e-08	3.754e-08	4.241e-08	3.205e-08	2.872e-08	3.606e-08	3.243e-08	4.256e-08	3.703e-08
0.4	7.849e-08	1.467e-07	1.127e-07	1.084e-07	1.031e-07	7.590e-08	9.710e-08	6.579e-08	1.198e-07	1.465e-07
	1.017e-07	1.457e-07	1.647e-07	1.089e-07	9.947e-08	8.844e-08	1.269e-07	1.136e-07	1.171e-07	1.341e-07
	1.144e-07	1.495e-07	1.126e-07	1.098e-07	9.623e-08	1.001e-07	1.027e-07	1.079e-07	1.127e-07	9.049e-08
	1.263e-07	1.318e-07	9.518e-08	1.113e-07	7.980e-08	7.043e-08	9.175e-08	8.068e-08	1.106e-07	9.347e-08
0.35	2.160e-07	4.240e-07	3.210e-07	3.066e-07	2.930e-07	2.115e-07	2.734e-07	1.785e-07	3.459e-07	4.233e-07
	2.838e-07	4.179e-07	4.769e-07	3.116e-07	2.789e-07	2.496e-07	3.662e-07	3.243e-07	3.389e-07	3.887e-07
	3.264e-07	4.347e-07	3.210e-07	3.121e-07	2.747e-07	2.848e-07	2.926e-07	3.039e-07	3.231e-07	2.566e-07
	3.590e-07	3.814e-07	2.668e-07	3.205e-07	2.218e-07	1.934e-07	2.584e-07	2.235e-07	3.170e-07	2.614e-07
0.3	6.354e-07	1.291e-06	9.680e-07	9.199e-07	8.844e-07	6.300e-07	8.184e-07	5.206e-07	1.054e-06	1.288e-06
	8.402e-07	1.263e-06	1.453e-06	9.442e-07	8.318e-07	7.492e-07	1.115e-06	9.789e-07	1.033e-06	1.189e-06
	9.854e-07	1.330e-06	9.698e-07	9.386e-07	8.278e-07	8.601e-07	8.834e-07	9.077e-07	9.764e-07	7.729e-07
	1.079e-06	1.166e-06	7.962e-07	9.721e-07	6.593e-07	5.696e-07	7.732e-07	6.616e-07	9.628e-07	7.782e-07
0.25	1.935e-06	4.015e-06	2.997e-06	2.838e-06	2.742e-06	1.935e-06	2.519e-06	1.578e-06	3.280e-06	4.008e-06
	2.565e-06	3.911e-06	4.528e-06	2.927e-06	2.557e-06	2.307e-06	3.476e-06	3.027e-06	3.203e-06	3.717e-06
	3.048e-06	4.159e-06	3.009e-06	2.891e-06	2.540e-06	2.668e-06	2.731e-06	2.793e-06	3.006e-06	2.388e-06
	3.333e-06	3.648e-06	2.452e-06	3.003e-06	2.026e-06	1.736e-06	2.377e-06	2.025e-06	2.997e-06	2.388e-06
0.2	5.897e-06	1.236e-05	9.205e-06	8.704e-06	8.440e-06	5.903e-06	7.701e-06	4.795e-06	1.006e-05	1.233e-05
	7.813e-06	1.202e-05	1.399e-05	8.960e-06	7.825e-06	7.028e-06	1.071e-05	9.272e-06	9.748e-06	1.148e-05
	9.331e-06	1.284e-05	9.262e-06	8.808e-06	7.670e-06	8.206e-06	8.338e-06	8.568e-06	9.104e-06	7.298e-06
	1.025e-05	1.129e-05	7.539e-06	9.124e-06	6.213e-06	5.285e-06	7.244e-06	6.193e-06	9.226e-06	7.292e-06
0.15	1.735e-05	3.640e-05	2.711e-05	2.562e-05	2.491e-05	1.725e-05	2.260e-05	1.409e-05	2.950e-05	3.632e-05
	2.297e-05	3.551e-05	4.147e-05	2.622e-05	2.305e-05	2.051e-05	3.154e-05	2.722e-05	2.832e-05	3.388e-05
	2.735e-05	3.791e-05	2.735e-05	2.567e-05	2.236e-05	2.419e-05	2.433e-05	2.533e-05	2.637e-05	2.136e-05
	3.044e-05	3.340e-05	2.234e-05	2.648e-05	1.838e-05	1.553e-05	2.116e-05	1.826e-05	2.715e-05	2.143e-05

Table D.3: s27 Timing Delay Measurements with Local Process Variation

V_{DD}	Timing Delay									
1	3.767e-10	3.848e-10	3.763e-10	3.764e-10	3.831e-10	3.687e-10	3.788e-10	3.754e-10	3.840e-10	4.068e-10
	3.769e-10	3.845e-10	3.908e-10	3.830e-10	3.861e-10	3.721e-10	3.808e-10	3.759e-10	3.814e-10	3.767e-10
	3.769e-10	3.884e-10	3.820e-10	3.904e-10	3.759e-10	3.832e-10	3.890e-10	3.900e-10	3.944e-10	3.957e-10
	3.743e-10	3.662e-10	3.816e-10	3.936e-10	3.689e-10	4.057e-10	3.921e-10	3.792e-10	3.747e-10	3.802e-10
0.9	4.759e-10	4.874e-10	4.749e-10	4.734e-10	4.848e-10	4.650e-10	4.769e-10	4.704e-10	4.860e-10	5.209e-10
	4.759e-10	4.859e-10	4.946e-10	4.808e-10	4.855e-10	4.673e-10	4.832e-10	4.785e-10	4.793e-10	4.762e-10
	4.753e-10	4.879e-10	4.836e-10	4.943e-10	4.742e-10	4.860e-10	4.907e-10	4.925e-10	5.002e-10	5.004e-10
	4.738e-10	4.611e-10	4.817e-10	4.977e-10	4.658e-10	5.146e-10	4.935e-10	4.764e-10	4.719e-10	4.783e-10
0.8	6.520e-10	6.699e-10	6.457e-10	6.418e-10	6.629e-10	6.302e-10	6.454e-10	6.323e-10	6.622e-10	7.163e-10
	6.448e-10	6.628e-10	6.750e-10	6.542e-10	6.664e-10	6.364e-10	6.591e-10	6.452e-10	6.533e-10	6.438e-10
	6.447e-10	6.673e-10	6.575e-10	6.782e-10	6.433e-10	6.649e-10	6.718e-10	6.722e-10	6.825e-10	6.853e-10
	6.395e-10	6.246e-10	6.570e-10	6.810e-10	6.243e-10	7.110e-10	6.719e-10	6.480e-10	6.367e-10	6.550e-10
0.7	9.963e-10	1.034e-09	9.839e-10	9.780e-10	1.018e-09	9.562e-10	9.852e-10	9.704e-10	1.013e-09	1.125e-09
	9.944e-10	1.024e-09	1.040e-09	9.968e-10	1.016e-09	9.645e-10	1.007e-09	9.980e-10	1.010e-09	9.804e-10
	9.909e-10	1.040e-09	1.020e-09	1.052e-09	9.820e-10	1.036e-09	1.041e-09	1.030e-09	1.057e-09	1.063e-09
	9.910e-10	9.555e-10	1.005e-09	1.057e-09	9.421e-10	1.103e-09	1.035e-09	9.892e-10	9.709e-10	1.002e-09
0.6	1.926e-09	1.997e-09	1.864e-09	1.858e-09	1.952e-09	1.801e-09	1.854e-09	1.827e-09	1.940e-09	2.262e-09
	1.904e-09	1.983e-09	2.020e-09	1.895e-09	1.962e-09	1.833e-09	1.928e-09	1.896e-09	1.934e-09	1.865e-09
	1.883e-09	2.006e-09	1.972e-09	2.033e-09	1.875e-09	2.019e-09	2.008e-09	1.962e-09	2.049e-09	2.070e-09
	1.901e-09	1.806e-09	1.919e-09	2.052e-09	1.762e-09	2.178e-09	2.004e-09	1.883e-09	1.819e-09	1.925e-09
0.5	5.646e-09	5.866e-09	5.321e-09	5.314e-09	5.659e-09	5.034e-09	5.191e-09	5.148e-09	5.569e-09	7.092e-09
	5.522e-09	5.836e-09	5.945e-09	5.377e-09	5.708e-09	5.243e-09	5.592e-09	5.465e-09	5.588e-09	5.351e-09
	5.377e-09	6.052e-09	5.815e-09	5.980e-09	5.390e-09	6.054e-09	5.894e-09	5.635e-09	6.078e-09	6.175e-09
	5.501e-09	5.169e-09	5.548e-09	6.117e-09	4.894e-09	6.662e-09	5.896e-09	5.424e-09	5.115e-09	5.611e-09
0.45	1.216e-08	1.256e-08	1.114e-08	1.121e-08	1.198e-08	1.054e-08	1.082e-08	1.073e-08	1.173e-08	1.573e-08
	1.181e-08	1.250e-08	1.272e-08	1.133e-08	1.218e-08	1.110e-08	1.189e-08	1.159e-08	1.180e-08	1.128e-08
	1.136e-08	1.321e-08	1.245e-08	1.278e-08	1.147e-08	1.309e-08	1.256e-08	1.194e-08	1.311e-08	1.332e-08
	1.173e-08	1.101e-08	1.173e-08	1.323e-08	1.017e-08	1.463e-08	1.265e-08	1.155e-08	1.068e-08	1.196e-08
0.4	3.001e-08	3.104e-08	2.717e-08	2.750e-08	2.937e-08	2.555e-08	2.613e-08	2.612e-08	2.850e-08	4.011e-08
	2.906e-08	3.104e-08	3.129e-08	2.766e-08	3.022e-08	2.729e-08	2.933e-08	2.843e-08	2.873e-08	2.744e-08
	2.760e-08	3.317e-08	3.075e-08	3.166e-08	2.826e-08	3.266e-08	3.089e-08	2.925e-08	3.292e-08	3.308e-08
	2.889e-08	2.685e-08	2.880e-08	3.307e-08	2.443e-08	3.700e-08	3.139e-08	2.849e-08	2.577e-08	2.952e-08
0.35	8.139e-08	8.501e-08	7.380e-08	7.460e-08	7.999e-08	6.853e-08	7.027e-08	7.077e-08	7.687e-08	1.129e-07
	7.963e-08	8.506e-08	8.516e-08	7.544e-08	8.363e-08	7.426e-08	8.039e-08	7.719e-08	7.802e-08	7.404e-08
	7.473e-08	9.206e-08	8.376e-08	8.685e-08	7.753e-08	8.973e-08	8.448e-08	7.938e-08	9.124e-08	9.114e-08
	7.913e-08	7.306e-08	7.844e-08	9.178e-08	6.570e-08	1.028e-07	8.584e-08	7.820e-08	6.951e-08	8.080e-08
0.3	2.362e-07	2.495e-07	2.124e-07	2.151e-07	2.315e-07	1.964e-07	2.028e-07	2.049e-07	2.217e-07	3.367e-07
	2.322e-07	2.472e-07	2.454e-07	2.199e-07	2.458e-07	2.143e-07	2.334e-07	2.232e-07	2.257e-07	2.132e-07
	2.147e-07	2.727e-07	2.438e-07	2.542e-07	2.269e-07	2.612e-07	2.467e-07	2.293e-07	2.690e-07	2.674e-07
	2.299e-07	2.114e-07	2.276e-07	2.703e-07	1.890e-07	3.037e-07	2.505e-07	2.278e-07	2.010e-07	2.360e-07
0.25	7.044e-07	7.550e-07	6.343e-07	6.415e-07	6.971e-07	5.807e-07	6.061e-07	6.100e-07	6.611e-07	1.035e-06
	6.994e-07	7.432e-07	7.299e-07	6.650e-07	7.470e-07	6.384e-07	7.022e-07	6.653e-07	6.746e-07	6.372e-07
	6.410e-07	8.267e-07	7.331e-07	7.686e-07	6.890e-07	7.868e-07	7.418e-07	6.873e-07	8.171e-07	8.082e-07
	6.936e-07	6.301e-07	6.845e-07	8.273e-07	5.646e-07	9.235e-07	7.533e-07	6.907e-07	5.964e-07	7.124e-07
0.2	2.122e-06	2.297e-06	1.907e-06	1.917e-06	2.106e-06	1.735e-06	1.826e-06	1.829e-06	1.997e-06	3.222e-06
	2.108e-06	2.245e-06	2.182e-06	2.020e-06	2.279e-06	1.913e-06	2.117e-06	2.010e-06	2.033e-06	1.910e-06
	1.928e-06	2.547e-06	2.222e-06	2.336e-06	2.097e-06	2.385e-06	2.259e-06	2.070e-06	2.500e-06	2.474e-06
	2.108e-06	1.884e-06	2.076e-06	2.529e-06	1.695e-06	2.832e-06	2.283e-06	2.110e-06	1.795e-06	2.156e-06
0.15	6.312e-06	6.901e-06	5.573e-06	5.566e-06	6.234e-06	5.011e-06	5.433e-06	5.275e-06	5.957e-06	1.016e-05
	6.242e-06	6.699e-06	6.385e-06	6.025e-06	6.762e-06	5.616e-06	6.216e-06	5.984e-06	6.063e-06	5.611e-06
	5.776e-06	7.874e-06	6.670e-06	7.009e-06	6.300e-06	7.108e-06	6.928e-06	6.211e-06	7.567e-06	7.465e-06
	6.315e-06	5.478e-06	6.263e-06	7.720e-06	5.011e-06	8.652e-06	6.778e-06	6.389e-06	5.220e-06	6.410e-06

Table D.4: s27 Timing Delay Measurements with Global Process Variation

V_{DD}	Timing Delay									
1	3.733e-10	4.082e-10	3.675e-10	3.884e-10	3.937e-10	3.565e-10	3.954e-10	3.723e-10	3.736e-10	4.017e-10
	3.594e-10	3.812e-10	4.033e-10	3.781e-10	3.899e-10	3.620e-10	3.728e-10	4.137e-10	3.735e-10	3.646e-10
	3.881e-10	4.141e-10	3.523e-10	3.758e-10	3.770e-10	4.216e-10	3.704e-10	3.591e-10	3.895e-10	4.226e-10
	3.728e-10	3.465e-10	3.833e-10	3.961e-10	3.949e-10	4.092e-10	3.880e-10	3.870e-10	3.875e-10	3.922e-10
0.9	4.695e-10	5.196e-10	4.612e-10	4.907e-10	5.039e-10	4.444e-10	5.016e-10	4.672e-10	4.704e-10	5.176e-10
	4.484e-10	4.826e-10	5.132e-10	4.774e-10	4.924e-10	4.527e-10	4.725e-10	5.310e-10	4.739e-10	4.564e-10
	4.937e-10	5.313e-10	4.406e-10	4.753e-10	4.763e-10	5.404e-10	4.654e-10	4.504e-10	4.950e-10	5.429e-10
	4.690e-10	4.341e-10	4.842e-10	5.028e-10	5.014e-10	5.286e-10	4.882e-10	4.892e-10	4.929e-10	4.978e-10
0.8	6.411e-10	7.284e-10	6.216e-10	6.768e-10	6.917e-10	5.910e-10	6.882e-10	6.347e-10	6.422e-10	7.158e-10
	6.008e-10	6.525e-10	7.119e-10	6.458e-10	6.741e-10	6.037e-10	6.373e-10	7.407e-10	6.395e-10	6.168e-10
	6.771e-10	7.329e-10	5.883e-10	6.438e-10	6.401e-10	7.546e-10	6.311e-10	6.010e-10	6.713e-10	7.622e-10
	6.366e-10	5.772e-10	6.614e-10	6.880e-10	6.933e-10	7.314e-10	6.682e-10	6.636e-10	6.719e-10	6.821e-10
0.7	9.788e-10	1.156e-09	9.356e-10	1.052e-09	1.093e-09	8.742e-10	1.072e-09	9.686e-10	9.753e-10	1.138e-09
	8.967e-10	1.004e-09	1.123e-09	9.759e-10	1.035e-09	9.112e-10	9.695e-10	1.183e-09	9.744e-10	9.348e-10
	1.053e-09	1.170e-09	8.781e-10	9.825e-10	9.794e-10	1.222e-09	9.549e-10	8.999e-10	1.031e-09	1.231e-09
	9.766e-10	8.565e-10	1.019e-09	1.075e-09	1.091e-09	1.168e-09	1.036e-09	1.025e-09	1.040e-09	1.073e-09
0.6	1.854e-09	2.344e-09	1.741e-09	2.074e-09	2.188e-09	1.578e-09	2.125e-09	1.852e-09	1.835e-09	2.311e-09
	1.639e-09	1.946e-09	2.261e-09	1.854e-09	2.004e-09	1.683e-09	1.816e-09	2.434e-09	1.853e-09	1.739e-09
	2.064e-09	2.389e-09	1.595e-09	1.857e-09	1.847e-09	2.549e-09	1.786e-09	1.627e-09	1.982e-09	2.569e-09
	1.857e-09	1.546e-09	1.991e-09	2.122e-09	2.177e-09	2.402e-09	2.018e-09	1.969e-09	1.997e-09	2.118e-09
0.5	5.269e-09	7.543e-09	4.745e-09	6.323e-09	7.000e-09	4.083e-09	6.411e-09	5.287e-09	5.162e-09	7.465e-09
	4.401e-09	5.711e-09	7.080e-09	5.295e-09	5.974e-09	4.682e-09	5.077e-09	7.834e-09	5.292e-09	4.776e-09
	6.218e-09	7.708e-09	4.253e-09	5.242e-09	5.216e-09	8.492e-09	4.948e-09	4.292e-09	5.775e-09	8.575e-09
	5.308e-09	4.029e-09	5.950e-09	6.671e-09	6.691e-09	7.995e-09	5.965e-09	5.743e-09	5.809e-09	6.438e-09
0.45	1.104e-08	1.688e-08	9.761e-09	1.388e-08	1.587e-08	8.086e-09	1.388e-08	1.117e-08	1.073e-08	1.682e-08
	8.962e-09	1.233e-08	1.568e-08	1.123e-08	1.303e-08	9.861e-09	1.061e-08	1.759e-08	1.117e-08	9.851e-09
	1.353e-08	1.747e-08	8.645e-09	1.097e-08	1.100e-08	1.946e-08	1.023e-08	8.621e-09	1.242e-08	1.971e-08
	1.120e-08	8.016e-09	1.298e-08	1.508e-08	1.466e-08	1.855e-08	1.284e-08	1.228e-08	1.246e-08	1.402e-08
0.4	2.671e-08	4.290e-08	2.329e-08	3.493e-08	4.144e-08	1.866e-08	3.463e-08	2.727e-08	2.572e-08	4.334e-08
	2.135e-08	3.062e-08	3.977e-08	2.783e-08	3.287e-08	2.422e-08	2.575e-08	4.476e-08	2.749e-08	2.363e-08
	3.363e-08	4.505e-08	2.048e-08	2.661e-08	2.693e-08	5.034e-08	2.459e-08	2.021e-08	3.083e-08	5.120e-08
	2.767e-08	1.866e-08	3.270e-08	3.941e-08	3.695e-08	4.919e-08	3.162e-08	3.036e-08	3.059e-08	3.505e-08
0.35	7.146e-08	1.182e-07	6.232e-08	9.649e-08	1.188e-07	4.869e-08	9.512e-08	7.349e-08	6.885e-08	1.218e-07
	5.742e-08	8.460e-08	1.103e-07	7.679e-08	9.209e-08	6.680e-08	6.999e-08	1.238e-07	7.517e-08	6.353e-08
	9.196e-08	1.272e-07	5.481e-08	7.183e-08	7.403e-08	1.405e-07	6.603e-08	5.325e-08	8.538e-08	1.448e-07
	7.558e-08	4.865e-08	9.076e-08	1.138e-07	1.015e-07	1.428e-07	8.608e-08	8.328e-08	8.360e-08	9.670e-08
0.3	2.034e-07	3.452e-07	1.792e-07	2.819e-07	3.607e-07	1.367e-07	2.784e-07	2.094e-07	1.962e-07	3.605e-07
	1.660e-07	2.481e-07	3.230e-07	2.272e-07	2.735e-07	1.958e-07	2.032e-07	3.623e-07	2.200e-07	1.836e-07
	2.673e-07	3.775e-07	1.568e-07	2.067e-07	2.189e-07	4.135e-07	1.905e-07	1.514e-07	2.512e-07	4.295e-07
	2.204e-07	1.373e-07	2.674e-07	3.480e-07	2.962e-07	4.345e-07	2.465e-07	2.418e-07	2.424e-07	2.824e-07
0.25	6.020e-07	1.031e-06	5.330e-07	8.484e-07	1.124e-06	4.014e-07	8.408e-07	6.182e-07	5.805e-07	1.099e-06
	5.000e-07	7.507e-07	9.706e-07	6.950e-07	8.353e-07	5.939e-07	6.119e-07	1.077e-06	6.684e-07	5.478e-07
	8.052e-07	1.156e-06	4.701e-07	6.184e-07	6.684e-07	1.250e-06	5.703e-07	4.468e-07	7.639e-07	1.307e-06
	6.673e-07	4.044e-07	8.115e-07	1.087e-06	8.896e-07	1.351e-06	7.307e-07	7.279e-07	7.256e-07	8.517e-07
0.2	1.791e-06	3.079e-06	1.606e-06	2.553e-06	3.507e-06	1.189e-06	2.559e-06	1.832e-06	1.732e-06	3.371e-06
	1.516e-06	2.268e-06	2.921e-06	2.129e-06	2.544e-06	1.797e-06	1.854e-06	3.252e-06	2.032e-06	1.658e-06
	2.436e-06	3.549e-06	1.416e-06	1.864e-06	2.047e-06	3.772e-06	1.739e-06	1.344e-06	2.338e-06	3.974e-06
	2.029e-06	1.205e-06	2.475e-06	3.422e-06	2.679e-06	4.199e-06	2.155e-06	2.201e-06	2.193e-06	2.585e-06
0.15	5.313e-06	8.945e-06	4.738e-06	7.523e-06	1.092e-05	3.475e-06	7.674e-06	5.297e-06	5.091e-06	1.029e-05
	4.567e-06	6.746e-06	8.741e-06	6.473e-06	7.643e-06	5.378e-06	5.518e-06	9.464e-06	6.148e-06	4.954e-06
	7.404e-06	1.090e-05	4.264e-06	5.506e-06	6.199e-06	1.128e-05	5.250e-06	3.995e-06	7.034e-06	1.199e-05
	6.066e-06	3.563e-06	7.540e-06	1.132e-05	8.400e-06	1.334e-05	6.203e-06	6.599e-06	6.422e-06	7.698e-06

Table D.5: s298 Timing Delay Measurements with Local Process Variation

V_{DD}	Timing Delay									
1	1.008e-09	9.978e-10	1.013e-09	1.001e-09	1.016e-09	1.002e-09	1.023e-09	1.004e-09	1.018e-09	1.027e-09
	1.021e-09	9.750e-10	1.001e-09	1.017e-09	9.989e-10	1.018e-09	9.954e-10	1.004e-09	1.005e-09	1.046e-09
	1.000e-09	9.965e-10	1.011e-09	1.008e-09	1.022e-09	9.970e-10	1.011e-09	9.863e-10	1.000e-09	9.941e-10
	1.010e-09	1.007e-09	1.007e-09	1.012e-09	1.043e-09	1.019e-09	1.005e-09	1.013e-09	9.716e-10	9.769e-10
0.9	1.272e-09	1.256e-09	1.275e-09	1.263e-09	1.282e-09	1.262e-09	1.292e-09	1.261e-09	1.283e-09	1.296e-09
	1.284e-09	1.225e-09	1.260e-09	1.280e-09	1.257e-09	1.283e-09	1.252e-09	1.264e-09	1.263e-09	1.326e-09
	1.258e-09	1.251e-09	1.275e-09	1.266e-09	1.289e-09	1.255e-09	1.274e-09	1.239e-09	1.260e-09	1.250e-09
	1.268e-09	1.270e-09	1.273e-09	1.274e-09	1.317e-09	1.281e-09	1.264e-09	1.277e-09	1.215e-09	1.223e-09
0.8	1.721e-09	1.697e-09	1.728e-09	1.709e-09	1.735e-09	1.699e-09	1.758e-09	1.706e-09	1.743e-09	1.757e-09
	1.738e-09	1.644e-09	1.703e-09	1.728e-09	1.694e-09	1.737e-09	1.685e-09	1.707e-09	1.711e-09	1.816e-09
	1.700e-09	1.688e-09	1.729e-09	1.711e-09	1.753e-09	1.695e-09	1.723e-09	1.668e-09	1.706e-09	1.687e-09
	1.714e-09	1.722e-09	1.727e-09	1.725e-09	1.792e-09	1.729e-09	1.713e-09	1.725e-09	1.631e-09	1.645e-09
0.7	2.632e-09	2.586e-09	2.641e-09	2.608e-09	2.657e-09	2.591e-09	2.708e-09	2.596e-09	2.679e-09	2.699e-09
	2.651e-09	2.489e-09	2.594e-09	2.631e-09	2.569e-09	2.646e-09	2.557e-09	2.601e-09	2.619e-09	2.815e-09
	2.588e-09	2.568e-09	2.654e-09	2.606e-09	2.693e-09	2.569e-09	2.635e-09	2.513e-09	2.607e-09	2.580e-09
	2.606e-09	2.637e-09	2.653e-09	2.624e-09	2.759e-09	2.638e-09	2.613e-09	2.621e-09	2.455e-09	2.484e-09
0.6	4.989e-09	4.907e-09	5.057e-09	4.964e-09	5.094e-09	4.895e-09	5.243e-09	4.911e-09	5.141e-09	5.186e-09
	5.027e-09	4.650e-09	4.909e-09	4.959e-09	4.840e-09	5.041e-09	4.819e-09	4.925e-09	5.011e-09	5.544e-09
	4.896e-09	4.839e-09	5.077e-09	4.940e-09	5.190e-09	4.825e-09	5.003e-09	4.685e-09	4.985e-09	4.903e-09
	4.923e-09	5.051e-09	5.121e-09	4.965e-09	5.327e-09	4.986e-09	4.981e-09	4.944e-09	4.553e-09	4.628e-09
0.5	1.428e-08	1.410e-08	1.464e-08	1.428e-08	1.492e-08	1.386e-08	1.557e-08	1.396e-08	1.506e-08	1.528e-08
	1.431e-08	1.295e-08	1.402e-08	1.404e-08	1.366e-08	1.448e-08	1.369e-08	1.404e-08	1.455e-08	1.715e-08
	1.389e-08	1.376e-08	1.474e-08	1.434e-08	1.534e-08	1.351e-08	1.433e-08	1.293e-08	1.436e-08	1.410e-08
	1.400e-08	1.479e-08	1.510e-08	1.423e-08	1.572e-08	1.422e-08	1.436e-08	1.406e-08	1.248e-08	1.300e-08
0.45	3.028e-08	3.005e-08	3.124e-08	3.035e-08	3.217e-08	2.911e-08	3.372e-08	2.947e-08	3.240e-08	3.311e-08
	3.018e-08	2.690e-08	2.972e-08	2.943e-08	2.873e-08	3.079e-08	2.896e-08	2.967e-08	3.113e-08	3.827e-08
	2.920e-08	2.905e-08	3.147e-08	3.076e-08	3.313e-08	2.818e-08	3.040e-08	2.673e-08	3.049e-08	2.993e-08
	2.951e-08	3.167e-08	3.252e-08	3.018e-08	3.393e-08	3.012e-08	3.056e-08	2.970e-08	2.570e-08	2.749e-08
0.4	7.436e-08	7.419e-08	7.692e-08	7.450e-08	8.048e-08	7.102e-08	8.413e-08	7.188e-08	8.086e-08	8.287e-08
	7.404e-08	6.488e-08	7.309e-08	7.146e-08	7.022e-08	7.593e-08	7.108e-08	7.263e-08	7.682e-08	9.812e-08
	7.146e-08	7.121e-08	7.761e-08	7.695e-08	8.243e-08	6.819e-08	7.481e-08	6.416e-08	7.476e-08	7.348e-08
	7.197e-08	7.849e-08	8.122e-08	7.425e-08	8.449e-08	7.426e-08	7.520e-08	7.300e-08	6.155e-08	6.739e-08
0.35	2.017e-07	2.032e-07	2.102e-07	2.024e-07	2.221e-07	1.920e-07	2.310e-07	1.944e-07	2.228e-07	2.287e-07
	2.009e-07	1.744e-07	1.991e-07	1.931e-07	1.905e-07	2.076e-07	1.941e-07	1.971e-07	2.099e-07	2.757e-07
	1.937e-07	1.933e-07	2.117e-07	2.130e-07	2.259e-07	1.838e-07	2.047e-07	1.712e-07	2.019e-07	1.999e-07
	1.946e-07	2.151e-07	2.237e-07	2.032e-07	2.328e-07	2.033e-07	2.048e-07	1.992e-07	1.639e-07	1.837e-07
0.3	5.826e-07	5.909e-07	6.082e-07	5.804e-07	6.509e-07	5.521e-07	6.717e-07	5.575e-07	6.522e-07	6.669e-07
	5.779e-07	4.974e-07	5.764e-07	5.527e-07	5.503e-07	6.032e-07	5.620e-07	5.682e-07	6.085e-07	8.214e-07
	5.606e-07	5.599e-07	6.130e-07	6.254e-07	6.536e-07	5.272e-07	5.943e-07	4.873e-07	5.780e-07	5.776e-07
	5.586e-07	6.230e-07	6.536e-07	5.892e-07	6.800e-07	5.909e-07	5.922e-07	5.788e-07	4.638e-07	5.332e-07
0.25	1.742e-06	1.777e-06	1.820e-06	1.725e-06	1.964e-06	1.640e-06	2.008e-06	1.652e-06	1.975e-06	2.007e-06
	1.721e-06	1.468e-06	1.726e-06	1.646e-06	1.645e-06	1.815e-06	1.685e-06	1.695e-06	1.822e-06	2.522e-06
	1.680e-06	1.680e-06	1.834e-06	1.896e-06	1.953e-06	1.568e-06	1.786e-06	1.435e-06	1.714e-06	1.729e-06
	1.661e-06	1.862e-06	1.978e-06	1.774e-06	2.050e-06	1.779e-06	1.769e-06	1.738e-06	1.363e-06	1.607e-06
0.2	5.237e-06	5.331e-06	5.488e-06	5.122e-06	5.931e-06	4.898e-06	6.008e-06	4.916e-06	6.000e-06	6.034e-06
	5.144e-06	4.371e-06	5.180e-06	4.915e-06	4.923e-06	5.469e-06	5.066e-06	5.086e-06	5.474e-06	7.721e-06
	5.060e-06	5.065e-06	5.514e-06	5.748e-06	5.839e-06	4.691e-06	5.392e-06	4.243e-06	5.109e-06	5.199e-06
	4.969e-06	5.586e-06	5.996e-06	5.373e-06	6.198e-06	5.362e-06	5.296e-06	5.241e-06	4.019e-06	4.831e-06
0.15	1.535e-05	1.542e-05	1.630e-05	1.484e-05	1.722e-05	1.416e-05	1.732e-05	1.412e-05	1.780e-05	1.739e-05
	1.482e-05	1.265e-05	1.501e-05	1.429e-05	1.412e-05	1.600e-05	1.478e-05	1.487e-05	1.612e-05	2.304e-05
	1.492e-05	1.485e-05	1.627e-05	1.691e-05	1.679e-05	1.360e-05	1.580e-05	1.212e-05	1.479e-05	1.528e-05
	1.450e-05	1.625e-05	1.764e-05	1.584e-05	1.832e-05	1.577e-05	1.535e-05	1.529e-05	1.144e-05	1.415e-05

Table D.6: s298 Timing Delay Measurements with Global Process Variation

V_{DD}	Timing Delay									
1	9.833e-10	1.027e-09	1.019e-09	9.639e-10	1.037e-09	1.003e-09	9.986e-10	1.004e-09	9.937e-10	1.018e-09
	1.123e-09	9.146e-10	9.585e-10	1.061e-09	1.064e-09	1.047e-09	1.059e-09	1.023e-09	9.644e-10	1.107e-09
	9.946e-10	9.838e-10	1.041e-09	9.650e-10	9.921e-10	9.883e-10	9.610e-10	1.040e-09	1.017e-09	9.755e-10
	1.030e-09	1.004e-09	9.953e-10	9.590e-10	1.020e-09	9.644e-10	9.818e-10	1.007e-09	9.664e-10	1.045e-09
0.9	1.235e-09	1.300e-09	1.290e-09	1.207e-09	1.312e-09	1.261e-09	1.256e-09	1.256e-09	1.245e-09	1.279e-09
	1.439e-09	1.132e-09	1.199e-09	1.348e-09	1.353e-09	1.333e-09	1.344e-09	1.292e-09	1.204e-09	1.415e-09
	1.247e-09	1.233e-09	1.323e-09	1.199e-09	1.246e-09	1.238e-09	1.199e-09	1.321e-09	1.283e-09	1.225e-09
	1.301e-09	1.268e-09	1.257e-09	1.190e-09	1.281e-09	1.200e-09	1.229e-09	1.263e-09	1.213e-09	1.331e-09
0.8	1.657e-09	1.776e-09	1.756e-09	1.621e-09	1.783e-09	1.705e-09	1.694e-09	1.689e-09	1.672e-09	1.732e-09
	2.003e-09	1.494e-09	1.609e-09	1.841e-09	1.852e-09	1.823e-09	1.846e-09	1.749e-09	1.617e-09	1.957e-09
	1.678e-09	1.661e-09	1.809e-09	1.597e-09	1.684e-09	1.663e-09	1.597e-09	1.807e-09	1.746e-09	1.655e-09
	1.762e-09	1.728e-09	1.708e-09	1.573e-09	1.724e-09	1.590e-09	1.654e-09	1.701e-09	1.631e-09	1.833e-09
0.7	2.503e-09	2.770e-09	2.713e-09	2.438e-09	2.753e-09	2.595e-09	2.577e-09	2.551e-09	2.529e-09	2.629e-09
	3.196e-09	2.180e-09	2.415e-09	2.871e-09	2.899e-09	2.838e-09	2.886e-09	2.681e-09	2.434e-09	3.110e-09
	2.541e-09	2.516e-09	2.815e-09	2.379e-09	2.555e-09	2.507e-09	2.381e-09	2.810e-09	2.676e-09	2.508e-09
	2.694e-09	2.660e-09	2.620e-09	2.321e-09	2.613e-09	2.352e-09	2.491e-09	2.567e-09	2.470e-09	2.868e-09
0.6	4.651e-09	5.470e-09	5.275e-09	4.510e-09	5.331e-09	4.894e-09	4.883e-09	4.770e-09	4.750e-09	4.982e-09
	6.623e-09	3.844e-09	4.466e-09	5.625e-09	5.770e-09	5.603e-09	5.773e-09	5.146e-09	4.486e-09	6.433e-09
	4.747e-09	4.714e-09	5.552e-09	4.373e-09	4.823e-09	4.633e-09	4.336e-09	5.521e-09	5.140e-09	4.699e-09
	5.154e-09	5.123e-09	5.027e-09	4.128e-09	4.933e-09	4.213e-09	4.646e-09	4.785e-09	4.618e-09	5.748e-09
0.5	1.287e-08	1.725e-08	1.580e-08	1.236e-08	1.589e-08	1.389e-08	1.397e-08	1.347e-08	1.358e-08	1.423e-08
	2.176e-08	9.632e-09	1.224e-08	1.706e-08	1.808e-08	1.718e-08	1.813e-08	1.497e-08	1.222e-08	2.206e-08
	1.329e-08	1.321e-08	1.713e-08	1.206e-08	1.370e-08	1.265e-08	1.150e-08	1.674e-08	1.498e-08	1.315e-08
	1.493e-08	1.520e-08	1.466e-08	1.057e-08	1.417e-08	1.095e-08	1.283e-08	1.334e-08	1.286e-08	1.818e-08
0.45	2.657e-08	3.894e-08	3.417e-08	2.541e-08	3.455e-08	2.925e-08	2.968e-08	2.854e-08	2.903e-08	3.020e-08
	4.980e-08	1.875e-08	2.521e-08	3.728e-08	4.053e-08	3.803e-08	4.046e-08	3.206e-08	2.516e-08	5.228e-08
	2.787e-08	2.762e-08	3.811e-08	2.547e-08	2.894e-08	2.602e-08	2.329e-08	3.644e-08	3.202e-08	2.741e-08
	3.185e-08	3.284e-08	3.127e-08	2.094e-08	3.043e-08	2.210e-08	2.658e-08	2.788e-08	2.680e-08	4.087e-08
0.4	6.353e-08	1.013e-07	8.486e-08	6.059e-08	8.676e-08	7.156e-08	7.325e-08	7.069e-08	7.257e-08	7.409e-08
	1.292e-07	4.291e-08	6.049e-08	9.337e-08	1.045e-07	9.698e-08	1.032e-07	7.931e-08	5.999e-08	1.414e-07
	6.812e-08	6.705e-08	9.750e-08	6.295e-08	7.077e-08	6.229e-08	5.509e-08	9.089e-08	7.891e-08	6.620e-08
	7.849e-08	8.159e-08	7.669e-08	4.858e-08	7.606e-08	5.237e-08	6.362e-08	6.783e-08	6.457e-08	1.052e-07
0.35	1.692e-07	2.894e-07	2.318e-07	1.601e-07	2.395e-07	1.944e-07	2.007e-07	1.948e-07	2.030e-07	2.015e-07
	3.623e-07	1.114e-07	1.614e-07	2.552e-07	2.956e-07	2.716e-07	2.878e-07	2.167e-07	1.594e-07	4.148e-07
	1.856e-07	1.806e-07	2.747e-07	1.739e-07	1.926e-07	1.667e-07	1.470e-07	2.483e-07	2.148e-07	1.775e-07
	2.134e-07	2.232e-07	2.070e-07	1.278e-07	2.109e-07	1.402e-07	1.697e-07	1.846e-07	1.728e-07	2.955e-07
0.3	4.793e-07	8.698e-07	6.666e-07	4.495e-07	6.985e-07	5.616e-07	5.837e-07	5.735e-07	6.052e-07	5.792e-07
	1.064e-06	3.134e-07	4.591e-07	7.361e-07	8.805e-07	8.045e-07	8.408e-07	6.274e-07	4.507e-07	1.272e-06
	5.412e-07	5.201e-07	8.177e-07	5.133e-07	5.557e-07	4.766e-07	4.218e-07	7.130e-07	6.196e-07	5.053e-07
	6.146e-07	6.446e-07	5.919e-07	3.620e-07	6.230e-07	4.042e-07	4.824e-07	5.353e-07	4.907e-07	8.725e-07
0.25	1.409e-06	2.677e-06	1.979e-06	1.305e-06	2.106e-06	1.675e-06	1.750e-06	1.737e-06	1.863e-06	1.732e-06
	3.193e-06	9.220e-07	1.352e-06	2.183e-06	2.683e-06	2.455e-06	2.530e-06	1.879e-06	1.324e-06	3.977e-06
	1.633e-06	1.552e-06	2.500e-06	1.561e-06	1.658e-06	1.415e-06	1.257e-06	2.107e-06	1.840e-06	1.495e-06
	1.834e-06	1.923e-06	1.747e-06	1.072e-06	1.895e-06	1.212e-06	1.418e-06	1.610e-06	1.441e-06	2.642e-06
0.2	4.176e-06	8.154e-06	5.928e-06	3.812e-06	6.324e-06	5.016e-06	5.253e-06	5.268e-06	5.748e-06	5.161e-06
	9.549e-06	2.745e-06	4.020e-06	6.488e-06	8.102e-06	7.466e-06	7.588e-06	5.643e-06	3.922e-06	1.232e-05
	4.962e-06	4.665e-06	7.635e-06	4.747e-06	4.969e-06	4.221e-06	3.785e-06	6.231e-06	5.513e-06	4.441e-06
	5.489e-06	5.737e-06	5.191e-06	3.211e-06	5.758e-06	3.659e-06	4.195e-06	4.873e-06	4.253e-06	7.962e-06
0.15	1.210e-05	2.360e-05	1.756e-05	1.082e-05	1.836e-05	1.455e-05	1.518e-05	1.540e-05	1.751e-05	1.482e-05
	2.737e-05	8.005e-06	1.158e-05	1.861e-05	2.325e-05	2.195e-05	2.201e-05	1.654e-05	1.144e-05	3.690e-05
	1.475e-05	1.369e-05	2.279e-05	1.395e-05	1.431e-05	1.224e-05	1.107e-05	1.773e-05	1.606e-05	1.295e-05
	1.601e-05	1.668e-05	1.502e-05	9.455e-06	1.708e-05	1.074e-05	1.209e-05	1.424e-05	1.205e-05	2.325e-05

Table D.7: s400 Timing Delay Measurements with Local Process Variation

V_{DD}	Timing Delay									
1	1.045e-09	1.067e-09	1.061e-09	1.033e-09	1.056e-09	1.063e-09	1.053e-09	1.039e-09	1.045e-09	1.040e-09
	1.043e-09	1.069e-09	1.048e-09	1.062e-09	1.055e-09	1.039e-09	1.063e-09	1.077e-09	1.068e-09	1.051e-09
	1.024e-09	1.077e-09	1.051e-09	1.069e-09	1.061e-09	1.035e-09	1.048e-09	1.053e-09	1.043e-09	1.046e-09
	1.045e-09	1.061e-09	1.061e-09	1.079e-09	1.036e-09	1.048e-09	1.060e-09	1.045e-09	1.056e-09	1.046e-09
0.9	1.317e-09	1.350e-09	1.340e-09	1.300e-09	1.334e-09	1.342e-09	1.330e-09	1.311e-09	1.318e-09	1.310e-09
	1.316e-09	1.351e-09	1.324e-09	1.344e-09	1.334e-09	1.307e-09	1.346e-09	1.364e-09	1.354e-09	1.324e-09
	1.286e-09	1.367e-09	1.326e-09	1.354e-09	1.342e-09	1.302e-09	1.319e-09	1.333e-09	1.314e-09	1.316e-09
	1.318e-09	1.341e-09	1.343e-09	1.366e-09	1.307e-09	1.323e-09	1.340e-09	1.320e-09	1.335e-09	1.321e-09
0.8	1.783e-09	1.836e-09	1.824e-09	1.762e-09	1.813e-09	1.826e-09	1.806e-09	1.777e-09	1.786e-09	1.774e-09
	1.785e-09	1.840e-09	1.796e-09	1.828e-09	1.816e-09	1.772e-09	1.830e-09	1.864e-09	1.851e-09	1.797e-09
	1.731e-09	1.869e-09	1.803e-09	1.846e-09	1.826e-09	1.758e-09	1.789e-09	1.819e-09	1.779e-09	1.784e-09
	1.791e-09	1.823e-09	1.830e-09	1.868e-09	1.773e-09	1.798e-09	1.825e-09	1.796e-09	1.819e-09	1.793e-09
0.7	2.726e-09	2.832e-09	2.809e-09	2.701e-09	2.782e-09	2.803e-09	2.768e-09	2.722e-09	2.728e-09	2.705e-09
	2.739e-09	2.832e-09	2.762e-09	2.819e-09	2.790e-09	2.708e-09	2.817e-09	2.891e-09	2.878e-09	2.756e-09
	2.629e-09	2.912e-09	2.774e-09	2.855e-09	2.808e-09	2.670e-09	2.730e-09	2.815e-09	2.717e-09	2.734e-09
	2.742e-09	2.804e-09	2.826e-09	2.888e-09	2.714e-09	2.769e-09	2.811e-09	2.769e-09	2.802e-09	2.751e-09
0.6	5.192e-09	5.487e-09	5.426e-09	5.148e-09	5.367e-09	5.396e-09	5.309e-09	5.221e-09	5.201e-09	5.128e-09
	5.242e-09	5.476e-09	5.284e-09	5.451e-09	5.392e-09	5.161e-09	5.447e-09	5.656e-09	5.662e-09	5.286e-09
	4.929e-09	5.742e-09	5.361e-09	5.549e-09	5.415e-09	5.052e-09	5.197e-09	5.477e-09	5.148e-09	5.222e-09
	5.251e-09	5.400e-09	5.480e-09	5.615e-09	5.176e-09	5.328e-09	5.433e-09	5.353e-09	5.399e-09	5.274e-09
0.5	1.495e-08	1.618e-08	1.607e-08	1.488e-08	1.580e-08	1.574e-08	1.531e-08	1.523e-08	1.494e-08	1.464e-08
	1.517e-08	1.616e-08	1.537e-08	1.610e-08	1.590e-08	1.494e-08	1.608e-08	1.711e-08	1.740e-08	1.542e-08
	1.379e-08	1.764e-08	1.593e-08	1.650e-08	1.586e-08	1.429e-08	1.495e-08	1.645e-08	1.464e-08	1.510e-08
	1.519e-08	1.580e-08	1.628e-08	1.674e-08	1.487e-08	1.573e-08	1.607e-08	1.583e-08	1.576e-08	1.527e-08
0.45	3.180e-08	3.481e-08	3.471e-08	3.160e-08	3.401e-08	3.364e-08	3.245e-08	3.253e-08	3.161e-08	3.082e-08
	3.225e-08	3.482e-08	3.284e-08	3.471e-08	3.425e-08	3.190e-08	3.458e-08	3.751e-08	3.848e-08	3.293e-08
	2.882e-08	3.889e-08	3.453e-08	3.569e-08	3.406e-08	2.994e-08	3.176e-08	3.569e-08	3.083e-08	3.210e-08
	3.234e-08	3.390e-08	3.522e-08	3.616e-08	3.146e-08	3.392e-08	3.455e-08	3.419e-08	3.363e-08	3.248e-08
0.4	7.817e-08	8.636e-08	8.663e-08	7.755e-08	8.439e-08	8.288e-08	7.948e-08	8.036e-08	7.740e-08	7.510e-08
	7.901e-08	8.653e-08	8.091e-08	8.620e-08	8.502e-08	7.857e-08	8.591e-08	9.446e-08	9.802e-08	8.135e-08
	6.980e-08	9.853e-08	8.628e-08	8.895e-08	8.431e-08	7.264e-08	7.795e-08	8.923e-08	7.506e-08	7.868e-08
	7.948e-08	8.374e-08	8.766e-08	9.009e-08	7.701e-08	8.438e-08	8.575e-08	8.507e-08	8.273e-08	7.971e-08
0.35	2.131e-07	2.364e-07	2.386e-07	2.109e-07	2.315e-07	2.257e-07	2.152e-07	2.196e-07	2.102e-07	2.032e-07
	2.143e-07	2.378e-07	2.210e-07	2.372e-07	2.331e-07	2.141e-07	2.362e-07	2.619e-07	2.747e-07	2.220e-07
	1.884e-07	2.749e-07	2.386e-07	2.440e-07	2.314e-07	1.961e-07	2.126e-07	2.465e-07	2.031e-07	2.143e-07
	2.164e-07	2.292e-07	2.412e-07	2.473e-07	2.093e-07	2.323e-07	2.350e-07	2.334e-07	2.249e-07	2.164e-07
0.3	6.171e-07	6.847e-07	6.981e-07	6.099e-07	6.751e-07	6.535e-07	6.191e-07	6.361e-07	6.081e-07	5.868e-07
	6.186e-07	6.957e-07	6.434e-07	6.921e-07	6.775e-07	6.211e-07	6.898e-07	7.700e-07	8.156e-07	6.436e-07
	5.424e-07	8.121e-07	6.997e-07	7.125e-07	6.728e-07	5.609e-07	6.157e-07	7.220e-07	5.867e-07	6.198e-07
	6.269e-07	6.681e-07	7.047e-07	7.206e-07	6.073e-07	6.797e-07	6.850e-07	6.802e-07	6.510e-07	6.259e-07
0.25	1.844e-06	2.054e-06	2.104e-06	1.824e-06	2.028e-06	1.949e-06	1.846e-06	1.901e-06	1.818e-06	1.754e-06
	1.840e-06	2.096e-06	1.931e-06	2.082e-06	2.034e-06	1.859e-06	2.079e-06	2.337e-06	2.486e-06	1.926e-06
	1.616e-06	2.466e-06	2.109e-06	2.146e-06	2.027e-06	1.662e-06	1.840e-06	2.173e-06	1.753e-06	1.853e-06
	1.875e-06	2.008e-06	2.122e-06	2.162e-06	1.820e-06	2.050e-06	2.058e-06	2.044e-06	1.946e-06	1.865e-06
0.2	5.486e-06	6.152e-06	6.325e-06	5.456e-06	6.087e-06	5.813e-06	5.484e-06	5.658e-06	5.444e-06	5.249e-06
	5.467e-06	6.322e-06	5.783e-06	6.265e-06	6.105e-06	5.553e-06	6.251e-06	7.110e-06	7.558e-06	5.747e-06
	4.812e-06	7.481e-06	6.359e-06	6.470e-06	6.103e-06	4.924e-06	5.508e-06	6.530e-06	5.235e-06	5.544e-06
	5.607e-06	6.030e-06	6.389e-06	6.475e-06	5.463e-06	6.168e-06	6.207e-06	6.130e-06	5.833e-06	5.585e-06
0.15		1.795e-05	1.844e-05	1.618e-05	1.781e-05	1.695e-05	1.575e-05	1.631e-05	1.584e-05	1.528e-05
	1.561e-05	1.867e-05	1.665e-05	1.825e-05	1.781e-05	1.615e-05	1.829e-05	2.150e-05	2.278e-05	1.667e-05
	1.379e-05	2.231e-05	1.873e-05	1.893e-05	1.795e-05	1.408e-05	1.616e-05	1.922e-05	1.518e-05	1.625e-05
	1.635e-05	1.752e-05	1.876e-05	1.887e-05	1.597e-05	1.809e-05	1.851e-05	1.797e-05	1.702e-05	1.627e-05

Table D.8: s400 Timing Delay Measurements with Global Process Variation

V_{DD}	Timing Delay									
1	1.018e-09	1.006e-09	1.066e-09	1.038e-09	1.077e-09	1.085e-09	1.049e-09	9.580e-10	1.023e-09	1.016e-09
	1.093e-09	1.060e-09	1.000e-09	1.022e-09	1.081e-09	9.839e-10	1.111e-09	1.079e-09	1.078e-09	1.074e-09
	1.015e-09	1.060e-09	1.036e-09	1.066e-09	1.083e-09	1.034e-09	1.083e-09	1.091e-09	9.650e-10	1.056e-09
	1.016e-09	1.055e-09	1.064e-09	1.145e-09	1.051e-09	1.102e-09	1.056e-09	1.032e-09	1.084e-09	1.087e-09
0.9	1.277e-09	1.261e-09	1.349e-09	1.315e-09	1.364e-09	1.381e-09	1.318e-09	1.186e-09	1.287e-09	1.273e-09
	1.389e-09	1.336e-09	1.253e-09	1.281e-09	1.373e-09	1.226e-09	1.417e-09	1.367e-09	1.365e-09	1.363e-09
	1.274e-09	1.341e-09	1.305e-09	1.350e-09	1.373e-09	1.300e-09	1.370e-09	1.388e-09	1.201e-09	1.336e-09
	1.274e-09	1.329e-09	1.352e-09	1.470e-09	1.327e-09	1.401e-09	1.330e-09	1.299e-09	1.372e-09	1.377e-09
0.8	1.716e-09	1.694e-09	1.836e-09	1.794e-09	1.861e-09	1.897e-09	1.779e-09	1.572e-09	1.735e-09	1.714e-09
	1.910e-09	1.814e-09	1.675e-09	1.723e-09	1.881e-09	1.632e-09	1.957e-09	1.871e-09	1.872e-09	1.867e-09
	1.716e-09	1.823e-09	1.772e-09	1.841e-09	1.873e-09	1.755e-09	1.866e-09	1.911e-09	1.592e-09	1.819e-09
	1.716e-09	1.803e-09	1.850e-09	2.049e-09	1.805e-09	1.930e-09	1.803e-09	1.758e-09	1.874e-09	1.886e-09
0.7	2.589e-09	2.550e-09	2.833e-09	2.776e-09	2.879e-09	2.975e-09	2.708e-09	2.317e-09	2.627e-09	2.592e-09
	2.979e-09	2.781e-09	2.513e-09	2.599e-09	2.930e-09	2.422e-09	3.096e-09	2.904e-09	2.923e-09	2.917e-09
	2.593e-09	2.809e-09	2.721e-09	2.852e-09	2.899e-09	2.677e-09	2.881e-09	3.019e-09	2.345e-09	2.812e-09
	2.594e-09	2.757e-09	2.878e-09	3.283e-09	2.786e-09	3.040e-09	2.765e-09	2.688e-09	2.906e-09	2.930e-09
0.6	4.809e-09	4.719e-09	5.492e-09	5.418e-09	5.617e-09	5.926e-09	5.125e-09	4.168e-09	4.926e-09	4.838e-09
	5.911e-09	5.318e-09	4.611e-09	4.849e-09	5.794e-09	4.389e-09	6.273e-09	5.688e-09	5.863e-09	5.770e-09
	4.852e-09	5.467e-09	5.232e-09	5.555e-09	5.647e-09	5.080e-09	5.582e-09	6.103e-09	4.163e-09	5.457e-09
	4.848e-09	5.284e-09	5.667e-09	6.831e-09	5.398e-09	6.156e-09	5.300e-09	5.115e-09	5.649e-09	5.742e-09
0.5	1.320e-08	1.292e-08	1.639e-08	1.620e-08	1.703e-08	1.844e-08	1.473e-08	1.116e-08	1.375e-08	1.346e-08
	1.816e-08	1.542e-08	1.236e-08	1.354e-08	1.770e-08	1.164e-08	2.000e-08	1.715e-08	1.907e-08	1.778e-08
	1.351e-08	1.656e-08	1.551e-08	1.664e-08	1.687e-08	1.473e-08	1.654e-08	1.972e-08	1.048e-08	1.615e-08
	1.351e-08	1.541e-08	1.722e-08	2.294e-08	1.592e-08	1.991e-08	1.534e-08	1.477e-08	1.682e-08	1.733e-08
0.45	2.715e-08	2.647e-08	3.564e-08	3.512e-08	3.739e-08	4.095e-08	3.139e-08	2.291e-08	2.868e-08	2.802e-08
	3.989e-08	3.281e-08	2.509e-08	2.832e-08	3.875e-08	2.359e-08	4.485e-08	3.736e-08	4.400e-08	3.919e-08
	2.820e-08	3.649e-08	3.366e-08	3.610e-08	3.652e-08	3.153e-08	3.568e-08	4.476e-08	2.037e-08	3.474e-08
	2.819e-08	3.314e-08	3.767e-08	5.299e-08	3.426e-08	4.530e-08	3.257e-08	3.139e-08	3.631e-08	3.783e-08
0.4	6.464e-08	6.284e-08	8.954e-08	8.742e-08	9.447e-08	1.042e-07	7.762e-08	5.518e-08	6.936e-08	6.767e-08
	1.004e-07	8.091e-08	5.906e-08	6.896e-08	9.695e-08	5.586e-08	1.149e-07	9.346e-08	1.165e-07	9.895e-08
	6.829e-08	9.257e-08	8.438e-08	9.048e-08	9.127e-08	7.817e-08	8.845e-08	1.163e-07	4.621e-08	8.588e-08
	6.824e-08	8.263e-08	9.420e-08	1.391e-07	8.529e-08	1.179e-07	7.997e-08	7.714e-08	9.028e-08	9.492e-08
0.35	1.718e-07	1.664e-07	2.476e-07	2.394e-07	2.628e-07	2.899e-07	2.131e-07	1.492e-07	1.866e-07	1.827e-07
	2.771e-07	2.215e-07	1.563e-07	1.879e-07	2.657e-07	1.484e-07	3.214e-07	2.569e-07	3.370e-07	2.748e-07
	1.844e-07	2.590e-07	2.344e-07	2.497e-07	2.517e-07	2.148e-07	2.424e-07	3.308e-07	1.187e-07	2.343e-07
	1.844e-07	2.284e-07	2.596e-07	3.967e-07	2.345e-07	3.361e-07	2.172e-07	2.101e-07	2.478e-07	2.624e-07
0.3	4.870e-07	4.700e-07	7.265e-07	6.943e-07	7.767e-07	8.532e-07	6.231e-07	4.325e-07	5.378e-07	5.289e-07
	8.088e-07	6.454e-07	4.440e-07	5.488e-07	7.691e-07	4.249e-07	9.490e-07	7.488e-07	1.023e-06	8.063e-07
	5.321e-07	7.679e-07	6.908e-07	7.315e-07	7.355e-07	6.279e-07	7.018e-07	9.901e-07	3.311e-07	6.755e-07
	5.322e-07	6.713e-07	7.568e-07	1.186e-06	6.868e-07	1.008e-06	6.285e-07	6.102e-07	7.215e-07	7.672e-07
0.25	1.428e-06	1.376e-06	2.195e-06	2.076e-06	2.355e-06	2.576e-06	1.879e-06	1.292e-06	1.600e-06	1.586e-06
	2.424e-06	1.945e-06	1.310e-06	1.655e-06	2.293e-06	1.261e-06	2.874e-06	2.253e-06	3.156e-06	2.427e-06
	1.588e-06	2.329e-06	2.092e-06	2.209e-06	2.218e-06	1.892e-06	2.099e-06	3.025e-06	9.629e-07	2.012e-06
	1.586e-06	2.035e-06	2.275e-06	3.625e-06	2.076e-06	3.088e-06	1.879e-06	1.825e-06	2.172e-06	2.313e-06
0.2	4.214e-06	4.063e-06	6.597e-06	6.223e-06	7.139e-06	7.756e-06	5.624e-06	3.837e-06	4.781e-06	4.769e-06
	7.205e-06	5.852e-06	3.887e-06	5.000e-06	6.830e-06	3.747e-06	8.673e-06	6.809e-06	9.640e-06	7.260e-06
	4.734e-06	7.034e-06	6.325e-06	6.671e-06	6.685e-06	5.656e-06	6.278e-06	9.165e-06	2.828e-06	6.011e-06
	4.736e-06	6.132e-06	6.820e-06	1.096e-05	6.274e-06	9.367e-06	5.661e-06	5.463e-06	6.530e-06	6.966e-06
0.15		1.170e-05	1.920e-05	1.836e-05	2.104e-05	2.276e-05	1.622e-05	1.120e-05	1.390e-05	1.398e-05
	2.061e-05	1.728e-05	1.114e-05	1.467e-05	1.986e-05	1.092e-05	2.535e-05	2.050e-05	2.959e-05	2.097e-05
	1.360e-05	2.101e-05	1.872e-05	1.954e-05	1.963e-05	1.626e-05	1.839e-05	2.715e-05	8.139e-06	1.753e-05
	1.378e-05	1.777e-05	2.000e-05	3.201e-05	1.846e-05	2.768e-05	1.686e-05	1.604e-05	1.914e-05	2.038e-05

Table D.9: s1196 Timing Delay Measurements with Local Process Variation

V_{DD}	Timing Delay									
1	1.038e-09	1.041e-09	1.049e-09	1.044e-09	1.040e-09	1.038e-09	1.007e-09	1.023e-09	1.028e-09	1.039e-09
	1.041e-09	1.071e-09	1.046e-09	1.061e-09	1.047e-09	1.046e-09	1.047e-09	1.035e-09	1.041e-09	1.050e-09
	1.058e-09	1.029e-09	1.032e-09	1.043e-09	1.027e-09	1.034e-09	1.023e-09	1.043e-09	1.023e-09	1.057e-09
	1.022e-09	1.028e-09	1.042e-09	1.030e-09	1.013e-09	1.041e-09	1.039e-09	1.030e-09	1.059e-09	1.040e-09
0.9	1.316e-09	1.321e-09	1.336e-09	1.328e-09	1.322e-09	1.317e-09	1.274e-09	1.295e-09	1.302e-09	1.316e-09
	1.321e-09	1.368e-09	1.330e-09	1.350e-09	1.334e-09	1.327e-09	1.330e-09	1.310e-09	1.321e-09	1.337e-09
	1.347e-09	1.304e-09	1.308e-09	1.323e-09	1.300e-09	1.312e-09	1.294e-09	1.326e-09	1.292e-09	1.341e-09
	1.292e-09	1.303e-09	1.322e-09	1.304e-09	1.281e-09	1.320e-09	1.318e-09	1.303e-09	1.345e-09	1.320e-09
0.8	1.800e-09	1.804e-09	1.839e-09	1.822e-09	1.813e-09	1.800e-09	1.731e-09	1.766e-09	1.784e-09	1.800e-09
	1.810e-09	1.884e-09	1.822e-09	1.851e-09	1.835e-09	1.821e-09	1.815e-09	1.791e-09	1.808e-09	1.840e-09
	1.850e-09	1.780e-09	1.789e-09	1.810e-09	1.774e-09	1.792e-09	1.764e-09	1.816e-09	1.760e-09	1.847e-09
	1.766e-09	1.779e-09	1.806e-09	1.786e-09	1.740e-09	1.802e-09	1.800e-09	1.786e-09	1.848e-09	1.811e-09
0.7	2.798e-09	2.789e-09	2.879e-09	2.858e-09	2.820e-09	2.793e-09	2.661e-09	2.725e-09	2.772e-09	2.787e-09
	2.811e-09	2.959e-09	2.843e-09	2.891e-09	2.873e-09	2.838e-09	2.816e-09	2.774e-09	2.800e-09	2.893e-09
	2.896e-09	2.759e-09	2.767e-09	2.813e-09	2.746e-09	2.780e-09	2.724e-09	2.832e-09	2.708e-09	2.889e-09
	2.735e-09	2.754e-09	2.804e-09	2.777e-09	2.673e-09	2.789e-09	2.785e-09	2.761e-09	2.886e-09	2.819e-09
0.6	5.501e-09	5.457e-09	5.771e-09	5.689e-09	5.583e-09	5.466e-09	5.143e-09	5.299e-09	5.440e-09	5.453e-09
	5.512e-09	5.939e-09	5.636e-09	5.749e-09	5.761e-09	5.630e-09	5.493e-09	5.416e-09	5.506e-09	5.839e-09
	5.760e-09	5.394e-09	5.406e-09	5.530e-09	5.350e-09	5.441e-09	5.306e-09	5.581e-09	5.223e-09	5.773e-09
	5.360e-09	5.382e-09	5.513e-09	5.445e-09	5.130e-09	5.445e-09	5.432e-09	5.390e-09	5.733e-09	5.574e-09
0.5	1.680e-08	1.644e-08	1.819e-08	1.779e-08	1.720e-08	1.664e-08	1.525e-08	1.583e-08	1.659e-08	1.651e-08
	1.671e-08	1.875e-08	1.751e-08	1.787e-08	1.824e-08	1.753e-08	1.650e-08	1.635e-08	1.670e-08	1.894e-08
	1.796e-08	1.633e-08	1.618e-08	1.693e-08	1.605e-08	1.644e-08	1.587e-08	1.711e-08	1.555e-08	1.811e-08
	1.631e-08	1.625e-08	1.679e-08	1.659e-08	1.499e-08	1.639e-08	1.631e-08	1.612e-08	1.780e-08	1.727e-08
0.45	3.696e-08	3.591e-08	4.072e-08	3.966e-08	3.796e-08	3.659e-08	3.307e-08	3.437e-08	3.648e-08	3.612e-08
	3.657e-08	4.200e-08	3.892e-08	3.966e-08	4.092e-08	3.908e-08	3.586e-08	3.583e-08	3.661e-08	4.311e-08
	3.994e-08	3.572e-08	3.514e-08	3.729e-08	3.493e-08	3.595e-08	3.445e-08	3.774e-08	3.373e-08	4.050e-08
	3.590e-08	3.549e-08	3.694e-08	3.645e-08	3.209e-08	3.596e-08	3.553e-08	3.503e-08	3.951e-08	3.828e-08
0.4	9.356e-08	9.042e-08	1.047e-07	1.013e-07	9.677e-08	9.259e-08	8.275e-08	8.638e-08	9.231e-08	9.117e-08
	9.203e-08	1.077e-07	9.934e-08	1.012e-07	1.053e-07	1.000e-07	8.991e-08	9.053e-08	9.229e-08	1.124e-07
	1.018e-07	9.027e-08	8.795e-08	9.472e-08	8.759e-08	9.062e-08	8.640e-08	9.565e-08	8.475e-08	1.040e-07
	9.091e-08	8.927e-08	9.346e-08	9.238e-08	7.952e-08	9.091e-08	8.909e-08	8.773e-08	1.010e-07	9.813e-08
0.35	2.611e-07	2.513e-07	2.956e-07	2.849e-07	2.713e-07	2.589e-07	2.294e-07	2.398e-07	2.578e-07	2.538e-07
	2.552e-07	3.035e-07	2.790e-07	2.833e-07	2.972e-07	2.814e-07	2.489e-07	2.525e-07	2.562e-07	3.214e-07
	2.852e-07	2.514e-07	2.424e-07	2.654e-07	2.430e-07	2.517e-07	2.391e-07	2.668e-07	2.356e-07	2.934e-07
	2.539e-07	2.481e-07	2.607e-07	2.580e-07	2.185e-07	2.538e-07	2.475e-07	2.427e-07	2.834e-07	2.758e-07
0.3	7.696e-07	7.386e-07	8.818e-07	8.474e-07	8.035e-07	7.655e-07	6.747e-07	7.053e-07	7.607e-07	7.475e-07
	7.493e-07	9.020e-07	8.278e-07	8.390e-07	8.854e-07	8.350e-07	7.286e-07	7.440e-07	7.515e-07	9.639e-07
	8.442e-07	7.404e-07	7.063e-07	7.854e-07	7.137e-07	7.418e-07	7.005e-07	7.880e-07	6.951e-07	8.757e-07
	7.508e-07	7.296e-07	7.685e-07	7.618e-07	6.383e-07	7.484e-07	7.256e-07	7.100e-07	8.424e-07	8.215e-07
0.25	2.329e-06	2.233e-06	2.698e-06	2.591e-06	2.449e-06	2.329e-06	2.036e-06	2.140e-06	2.303e-06	2.264e-06
	2.260e-06	2.758e-06	2.524e-06	2.552e-06	2.702e-06	2.547e-06	2.201e-06	2.257e-06	2.271e-06	2.969e-06
	2.564e-06	2.245e-06	2.122e-06	2.390e-06	2.162e-06	2.256e-06	2.120e-06	2.397e-06	2.107e-06	2.682e-06
	2.275e-06	2.207e-06	2.333e-06	2.307e-06	1.919e-06	2.271e-06	2.199e-06	2.145e-06	2.569e-06	2.506e-06
0.2	7.005e-06	6.723e-06	8.200e-06	7.919e-06	7.432e-06	7.083e-06	6.140e-06	6.472e-06	6.959e-06	6.836e-06
	6.820e-06	8.414e-06	7.672e-06	7.727e-06	8.237e-06	7.704e-06	6.637e-06	6.815e-06	6.830e-06	9.110e-06
	7.780e-06	6.786e-06	6.369e-06	7.212e-06	6.527e-06	6.829e-06	6.410e-06	7.262e-06	6.353e-06	8.176e-06
	6.873e-06	6.667e-06	7.048e-06	6.951e-06	5.766e-06	6.871e-06	6.618e-06	6.473e-06	7.817e-06	7.605e-06
0.15	2.023e-05	1.960e-05	2.428e-05	2.393e-05	2.202e-05	2.092e-05	1.789e-05	1.899e-05	2.040e-05	2.000e-05
	2.010e-05	2.522e-05	2.281e-05	2.281e-05	2.480e-05	2.278e-05	1.941e-05	1.998e-05	1.978e-05	2.823e-05
	2.306e-05	1.993e-05	1.845e-05	2.106e-05	1.907e-05	2.013e-05	1.885e-05	2.144e-05	1.859e-05	2.438e-05
	2.006e-05	1.937e-05	2.063e-05	2.020e-05	1.674e-05	2.023e-05	1.942e-05	1.901e-05	2.341e-05	2.251e-05

Table D.10: s1196 Timing Delay Measurements with Global Process Variation

V_{DD}	Timing Delay									
1	1.008e-09	9.994e-10	1.084e-09	1.037e-09	1.023e-09	1.036e-09	9.554e-10	1.021e-09	1.030e-09	1.085e-09
	1.040e-09	1.093e-09	1.033e-09	1.105e-09	9.970e-10	1.036e-09	1.045e-09	1.013e-09	9.818e-10	1.075e-09
	1.069e-09	1.047e-09	9.704e-10	1.059e-09	9.418e-10	9.894e-10	1.062e-09	1.054e-09	1.079e-09	1.091e-09
	9.571e-10	1.079e-09	1.043e-09	1.042e-09	1.054e-09	9.683e-10	1.074e-09	1.007e-09	1.048e-09	1.016e-09
0.9	1.270e-09	1.258e-09	1.393e-09	1.319e-09	1.299e-09	1.314e-09	1.196e-09	1.291e-09	1.304e-09	1.386e-09
	1.318e-09	1.401e-09	1.313e-09	1.414e-09	1.255e-09	1.310e-09	1.324e-09	1.279e-09	1.237e-09	1.375e-09
	1.363e-09	1.334e-09	1.218e-09	1.346e-09	1.175e-09	1.245e-09	1.361e-09	1.341e-09	1.377e-09	1.398e-09
	1.201e-09	1.381e-09	1.327e-09	1.326e-09	1.339e-09	1.213e-09	1.373e-09	1.271e-09	1.329e-09	1.284e-09
0.8	1.722e-09	1.697e-09	1.942e-09	1.812e-09	1.774e-09	1.799e-09	1.601e-09	1.756e-09	1.788e-09	1.913e-09
	1.804e-09	1.942e-09	1.796e-09	1.958e-09	1.704e-09	1.794e-09	1.805e-09	1.742e-09	1.670e-09	1.902e-09
	1.884e-09	1.838e-09	1.639e-09	1.852e-09	1.566e-09	1.682e-09	1.887e-09	1.844e-09	1.897e-09	1.944e-09
	1.616e-09	1.914e-09	1.820e-09	1.824e-09	1.836e-09	1.623e-09	1.905e-09	1.732e-09	1.815e-09	1.745e-09
0.7	2.632e-09	2.581e-09	3.110e-09	2.833e-09	2.750e-09	2.808e-09	2.399e-09	2.698e-09	2.783e-09	3.016e-09
	2.801e-09	3.086e-09	2.788e-09	3.104e-09	2.610e-09	2.791e-09	2.782e-09	2.677e-09	2.539e-09	3.022e-09
	2.962e-09	2.894e-09	2.481e-09	2.901e-09	2.324e-09	2.549e-09	2.999e-09	2.884e-09	2.993e-09	3.101e-09
	2.438e-09	3.042e-09	2.838e-09	2.853e-09	2.857e-09	2.434e-09	3.029e-09	2.657e-09	2.818e-09	2.685e-09
0.6	5.018e-09	4.872e-09	6.467e-09	5.623e-09	5.382e-09	5.617e-09	4.407e-09	5.183e-09	5.483e-09	6.082e-09
	5.529e-09	6.320e-09	5.482e-09	6.358e-09	5.028e-09	5.538e-09	5.400e-09	5.136e-09	4.797e-09	6.226e-09
	5.968e-09	5.865e-09	4.655e-09	5.865e-09	4.206e-09	4.776e-09	6.146e-09	5.735e-09	6.039e-09	6.433e-09
	4.552e-09	6.222e-09	5.600e-09	5.661e-09	5.630e-09	4.476e-09	6.193e-09	5.101e-09	5.514e-09	5.178e-09
0.5	1.448e-08	1.385e-08	2.162e-08	1.743e-08	1.630e-08	1.828e-08	1.198e-08	1.510e-08	1.701e-08	1.931e-08
	1.712e-08	2.055e-08	1.670e-08	2.083e-08	1.510e-08	1.749e-08	1.607e-08	1.494e-08	1.368e-08	2.089e-08
	1.885e-08	1.905e-08	1.321e-08	1.911e-08	1.104e-08	1.335e-08	2.005e-08	1.785e-08	1.943e-08	2.150e-08
	1.274e-08	2.022e-08	1.723e-08	1.754e-08	1.726e-08	1.213e-08	2.019e-08	1.485e-08	1.663e-08	1.525e-08
0.45	3.070e-08	2.929e-08	4.966e-08	3.854e-08	3.569e-08	4.216e-08	2.454e-08	3.232e-08	3.790e-08	4.321e-08
	3.805e-08	4.668e-08	3.660e-08	4.755e-08	3.315e-08	3.949e-08	3.491e-08	3.188e-08	2.897e-08	4.854e-08
	4.199e-08	4.361e-08	2.810e-08	4.386e-08	2.219e-08	2.776e-08	4.568e-08	3.966e-08	4.406e-08	4.974e-08
	2.672e-08	4.591e-08	3.795e-08	3.875e-08	3.812e-08	2.497e-08	4.591e-08	3.167e-08	3.630e-08	3.296e-08
0.4	7.540e-08	7.202e-08	1.293e-07	9.804e-08	9.027e-08	1.117e-07	5.849e-08	7.983e-08	9.704e-08	1.110e-07
	9.745e-08	1.207e-07	9.222e-08	1.239e-07	8.401e-08	1.025e-07	8.761e-08	7.851e-08	7.123e-08	1.284e-07
	1.067e-07	1.143e-07	6.956e-08	1.151e-07	5.206e-08	6.693e-08	1.185e-07	1.014e-07	1.143e-07	1.307e-07
	6.510e-08	1.184e-07	9.613e-08	9.827e-08	9.692e-08	5.991e-08	1.191e-07	7.809e-08	9.142e-08	8.239e-08
0.35	2.050e-07	1.971e-07	3.652e-07	2.735e-07	2.516e-07	3.245e-07	1.566e-07	2.175e-07	2.745e-07	3.108e-07
	2.746e-07	3.406e-07	2.559e-07	3.525e-07	2.352e-07	2.916e-07	2.431e-07	2.132e-07	1.947e-07	3.710e-07
	2.943e-07	3.271e-07	1.924e-07	3.300e-07	1.381e-07	1.799e-07	3.357e-07	2.847e-07	3.242e-07	3.748e-07
	1.774e-07	3.326e-07	2.676e-07	2.731e-07	2.712e-07	1.609e-07	3.368e-07	2.136e-07	2.541e-07	2.281e-07
0.3	5.910e-07	5.753e-07	1.081e-06	8.066e-07	7.435e-07	9.897e-07	4.482e-07	6.303e-07	8.170e-07	9.171e-07
	8.192e-07	1.011e-06	7.512e-07	1.053e-06	6.985e-07	8.755e-07	7.158e-07	6.146e-07	5.678e-07	1.122e-06
	8.558e-07	9.839e-07	5.676e-07	9.926e-07	3.939e-07	5.165e-07	9.999e-07	8.468e-07	9.725e-07	1.129e-06
	5.152e-07	9.803e-07	7.885e-07	8.005e-07	8.039e-07	4.631e-07	1.002e-06	6.210e-07	7.492e-07	6.710e-07
0.25	1.761e-06	1.736e-06	3.277e-06	2.449e-06	2.258e-06	3.066e-06	1.330e-06	1.882e-06	2.493e-06	2.779e-06
	2.511e-06	3.088e-06	2.271e-06	3.222e-06	2.129e-06	2.684e-06	2.169e-06	1.831e-06	1.706e-06	3.465e-06
	2.558e-06	3.019e-06	1.724e-06	3.037e-06	1.173e-06	1.537e-06	3.044e-06	2.588e-06	2.968e-06	3.470e-06
	1.547e-06	2.965e-06	2.385e-06	2.408e-06	2.448e-06	1.380e-06	3.051e-06	1.860e-06	2.276e-06	2.036e-06
0.2	5.241e-06	5.240e-06	9.872e-06	7.451e-06	6.852e-06	9.427e-06	3.967e-06	5.634e-06	7.540e-06	8.383e-06
	7.653e-06	9.398e-06	6.867e-06	9.786e-06	6.497e-06	8.168e-06	6.548e-06	5.470e-06	5.113e-06	1.065e-05
	7.649e-06	9.181e-06	5.237e-06	9.154e-06	3.496e-06	4.595e-06	9.245e-06	7.878e-06	8.989e-06	1.062e-05
	4.646e-06	8.897e-06	7.177e-06	7.214e-06	7.410e-06	4.124e-06	9.237e-06	5.590e-06	6.908e-06	6.172e-06
0.15	1.507e-05	1.534e-05	2.903e-05	2.242e-05	2.030e-05	2.916e-05	1.151e-05	1.641e-05	2.232e-05	2.459e-05
	2.284e-05	2.807e-05	2.035e-05	2.889e-05	2.005e-05	2.449e-05	1.923e-05	1.594e-05	1.483e-05	3.314e-05
	2.254e-05	2.717e-05	1.554e-05	2.703e-05	1.021e-05	1.341e-05	2.728e-05	2.334e-05	2.621e-05	3.162e-05
	1.352e-05	2.574e-05	2.101e-05	2.085e-05	2.162e-05	1.207e-05	2.710e-05	1.638e-05	2.062e-05	1.823e-05

Appendix E

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