

A Hybrid DSP and FPGA System for Software Defined Radio Applications

Volodymyr S. Podosinov

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partial fulfillment of the requirements for the degree of

Master of Science
In
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Dr. Majid Manteghi, Chair
Dr. William Davis, Member
Dr. Patrick Schaumont, Member

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Description of item under review for fair use: Figure 2.2: Input connector of the COM-2001 DAC [7]

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Description of item under review for fair use: Figure 2.3: Wiring and prototyping board for the TMS320C6455 DSK [34]

Report generated on: 04-21-2011 at : 12:46:24

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Description of item under review for fair use: Table 2.1: External memory (EMIF) expansion connector pinout [5]

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Factor 4

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Description of item under review for fair use: Figure 2.5: Timing Diagram for the EMIF interface in the writing mode [13]

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Factor 3

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Factor 4

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Description of item under review for fair use: Figure 3.2: Direct down-converter used in the project [8]

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Factor 2

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Your consideration of the amount and substantiality of your use of the copyrighted work weighs: *in favor of fair use*

Factor 4

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Description of item under review for fair use: Figure 3.3: Output of the COM-3002B receiver module [8]

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Description of item under review for fair use: Figure 3.7: DC blocking filter block diagram [4]

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Factor 2

Your consideration of the nature of the copyrighted work you used weighs: *in favor of fair use*

Factor 3

Your consideration of the amount and substantiality of your use of the copyrighted work weighs: *in favor of fair use*

Factor 4

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Description of item under review for fair use: Table 3.4: Host Port Interface (HPI) external connector pinout [5]

Report generated on: 04-21-2011 at : 12:56:16

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Factor 2

Your consideration of the nature of the copyrighted work you used weighs: *in favor of fair use*

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Your consideration of the amount and substantiality of your use of the copyrighted work weighs: *in favor of fair use*

Factor 4

Your consideration of the effect or potential effect on the market after your use of the copyrighted work weighs: *against fair use*

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Description of item under review for fair use: Figure 3.19: HPI strobe control logic [16]

Report generated on: 04-21-2011 at : 12:56:52

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Factor 2

Your consideration of the nature of the copyrighted work you used weighs: *in favor of fair use*

Factor 3

Your consideration of the amount and substantiality of your use of the copyrighted work weighs: *in favor of fair use*

Factor 4

Your consideration of the effect or potential effect on the market after your use of the copyrighted work weighs: *against fair use*

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Description of item under review for fair use: Table 3.5: Access type based on control signal value [16]

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Factor 1

Your consideration of the purpose and character of your use of the copyright work weighs: *in favor of fair use*

Factor 2

Your consideration of the nature of the copyrighted work you used weighs: *in favor of fair use*

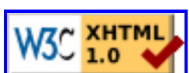
Factor 3

Your consideration of the amount and substantiality of your use of the copyrighted work weighs: *in favor of fair use*

Factor 4

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Description of item under review for fair use: Figure 3.20: HPI interface DMA logic [16]

Report generated on: 04-21-2011 at : 12:59:46

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Factor 2

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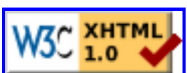
Factor 3

Your consideration of the amount and substantiality of your use of the copyrighted work weighs: *in favor of fair use*

Factor 4

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Description of item under review for fair use: Figure 3.21: HPI interface write timing diagram [16]

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Description of item under review for fair use: Figure 4.4: TMS320C6455 DSK Memory Map [5]

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Description of item under review for fair use: Table 4.1: Partial TMS320C6455 internal memory map [23]

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Description of item under review for fair use: Table 4.8: Configuration switched for different DSP boot options [5]

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Description of item under review for fair use: Figure 4.21: Diagram of how FlashBurn works [33]

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