DOUBLE-SIDED LIQUID COOLING FOR POWER SEMICONDUCTOR DEVICES USING EMBEDDED POWER TECHNOLOGY

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ABSTRACT

Power electronics is a constantly growing and demanding technical field. Consumer demand and developing technologies have made the improvement of power density a primary emphasis of research for this area. Power semiconductors present some of the major challenges for increasing system level power density due to high loss density and interconnection requirements. Advanced cooling schemes, such as double-sided, forced liquid convection or multi-phase flow, can be implemented with non-wire bond packaging to improve thermal management while maintaining proper electrical performance. Embedded power is one such packaging technology, which provides a compact structure for interface of power semiconductor to fluid flow.

The objective of this work was to identify the potential of implementing embedded power packaging with double-sided forced liquid convection. Physics based, electro-thermal models were first used to predict the improvement in heat transfer of double-sided, forced liquid convection with embedded power packaging over single-sided liquid cooled wire bond based packaging. A liquid module test bed was designed and constructed based on the electro-thermal models, which could be interfaced with high power MOSFET based samples implementing various packaging technologies. Experiments were used to verify the model predictions and identify practical limitations of high flow rate, double-sided liquid cooling with embedded power. An improvement of 45% to 60% in total junction to case thermal resistance is shown for embedded power packaging with double-sided liquid cooling for water flow rates between 0.25 and 4.5 gal/min.

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1 INTRODUCTION

1.1 Motivation for Improved Power Semiconductor Thermal Management

Semiconductor based power converters are essential for efficient power delivery and use for countless applications in the world. Technology, specifically related to electronics, has advanced rapidly in recent decades and consumer requirements for electronic systems have become more and more demanding. These developments have sparked the need for higher efficiency and higher power density power converters. As the power density requirements grow for power conversion system, effective thermal management design for power electronic components becomes more critical [1].

High power density packaging of power semiconductor devices presents some of the greatest thermal design challenges. Power semiconductor devices typically have the greatest quantity of power loss in a power conversion system [1]. This issue is made even more complicated since semiconductors have a limited amount of surface area to interface with heat removal systems. Electrical interconnection requirements complicate this matter twofold. Advanced cooling techniques involving forced liquid convection or phase change can help meet loss density requirements for current and future semiconductor devices [2]. These advanced cooling techniques can improve power density greatly if they can be interfaced properly with the semiconductor device packaging technology.

1.2 Cooling Schemes Review

There are many examples of cooling schemes for semiconductor based systems and individual semiconductor device. These cooling schemes can be placed into four areas of heat transfer including conduction, convection, phase change, and radiation heat transfer [3]. It is important to understand the potential of each heat transfer method and also identify the effectiveness for each in a particular electronics application.

Conduction heat transfer is present in all semiconductor cooling schemes due to electrical and mechanical interconnection requirements for semiconductor chips. Conduction is also considered in thermal management design for heat spreading and

thermal energy storage. Heat transfer via conduction can not be considered alone since thermal energy from power loss is normally exchanged or removed to the environment. This heat removal requires convection, radiation or a combination of these heat transfer methods. Phase change can also be implemented with convection to remove a greater amount of heat. These heat transfer methods are compared approximately in Figure 1.1, which shows the heat transfer coefficient range for various cooling media and schemes [2-3].

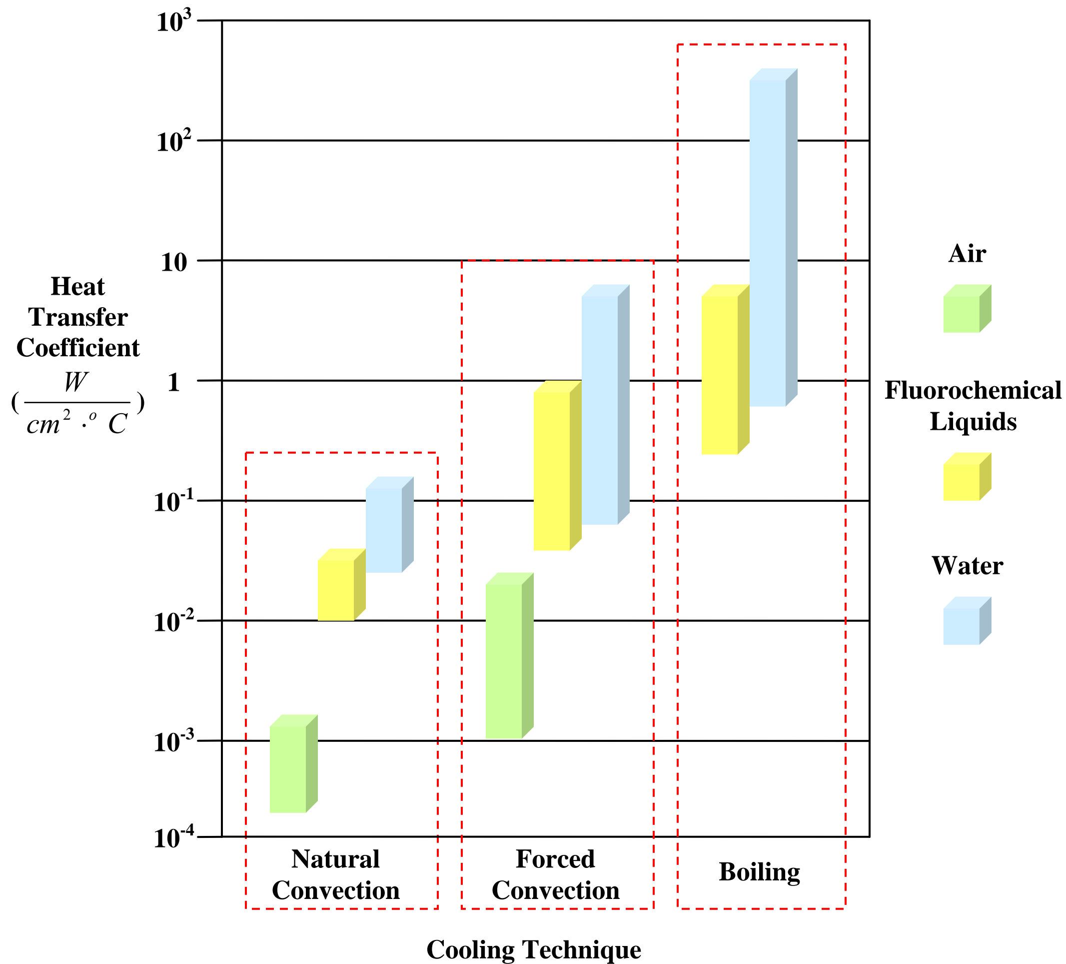


Figure 1.1 Heat transfer coefficient for various heat transfer methods and cooling fluids

Figure 1.1 shows the potential of forced liquid convection and phase change heat transfer methods for combating the high loss density of power semiconductor devices. These cooling techniques will provide the lowest temperature rise for high surface heat flux. The interface of these advanced electronics cooling schemes to power

semiconductors should be considered to effectively cool while providing high power density.

1.3 Power Semiconductor Thermal Management Survey

There has been a considerable amount of research on thermal management of power semiconductors. This research includes investigations on advanced cooling for typical power device packaging technology, which uses wire bonds. Most of these studies cover cooling schemes for the non-wire bond side of the device, while a few cover cooling of the top side of the device. Few, if any, sources mention double-sided cooling with wire bond packaging, but this is not impossible. Some research effort has been placed on improved thermal management using non-wire bond packaging technologies. These packaging technologies use flip chip technology or other alternate interconnection methods to replace wire bonds. This allows for easier interface to advanced cooling schemes. This section presents a survey of state of the art advanced cooling schemes and power semiconductor packaging.

1.3.1 Wire Bond Packaging and Cooling

Previous efforts to interface advanced cooling schemes with power semiconductor devices are primarily driven by device packaging containing wire bond interconnects [1]. A cross section of a typical wire bond package is shown in Figure 1.2. In these schemes, semiconductors are usually interfaced with cooling mechanisms on the non-wire bond side of the package. The wire bond side is normally avoided for electrical isolation and wire bond reliability concerns. Some efforts have been made to improve the removal of heat through the wire bond side of MOSFET and IGBT packages by using advanced cooling techniques such as spray cooling.

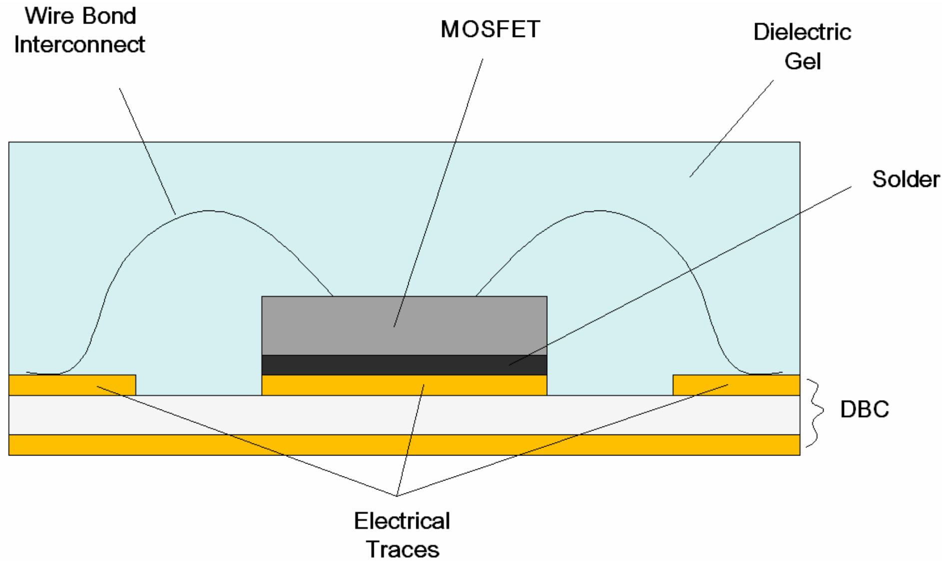


Figure 1.2 Cross section of typical wire bond package

One effort to improve heat transfer for wire bonded MOSFETs is to integrate liquid cooling under the semiconductor device in a power electronics module package [4]. This MOSFET based module uses an integrated fluid channel under the copper base plate, which the semiconductor die are directly soldered to. The devices in this package are therefore not electrically isolated from the coolant, so de-ionized water is used as the cooling media in the module. Figure 1.3 shows a simple representation for this cooling package. This structure improves thermal management of the semiconductor device by reducing the thermal resistance between the chip and fluid compared to a system with a module on a liquid cold plate. Thermal resistance was calculated based on experimental results to be between 0.02 to 0.01 ^{o}C/W for a flow rate range of 0.4 to 1.8 gal/min with a 1300 W loss from a dual switch MOSFET module. A maximum pressure drop was found to be approximately 200 mbar.

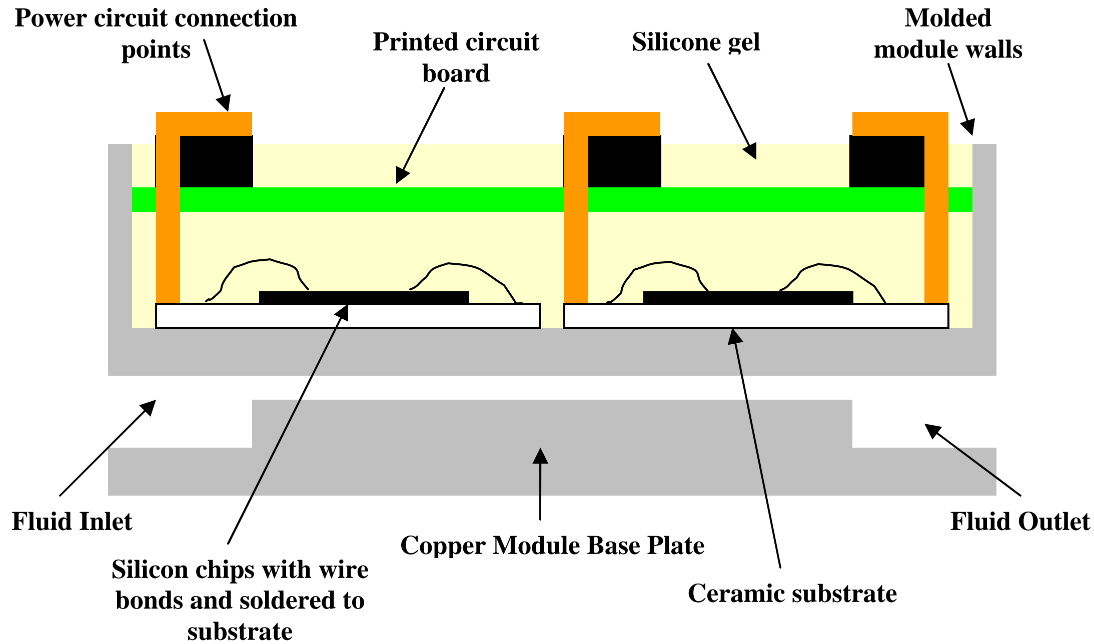


Figure 1.3 Conceptual drawing of an integrated liquid cooling in a high power MOSFET module

An improved thermal management scheme was demonstrated for an insulated gate bipolar transistor (IGBT) by using integrated single- and two- phase micro heat sinks [5]. It was mentioned that the micro scale cooling system could actually be implemented in the semiconductor itself, but this is not demonstrated since metallization is applied on the wafer for chip connections. As an alternative, micro heat sinks were place directly under the power semiconductor die. This micro structure can be used with single phase fluid flow to greatly reduce thermal resistance between the device and fluid. Thermal resistance was found to be approximately 0.1 ^{o}C/W for single phase water flow of 0.4 gal/min, 31 mbar pressure drop and 300 W device loss. A similar thermal resistance was found for multiphase flow, but with a flow rate of 0.007 gal/min and 2.7 mbar pressure drop. Figure 1.4 shows a conceptual drawing of the micro cooling structure for an IGBT device. A similar study with micro channels was performed for a group of IGBTs [6]. Single phase flow provides improved cooling performance due to a reduction in thermal resistance and can be implemented on the system level while remaining compact.

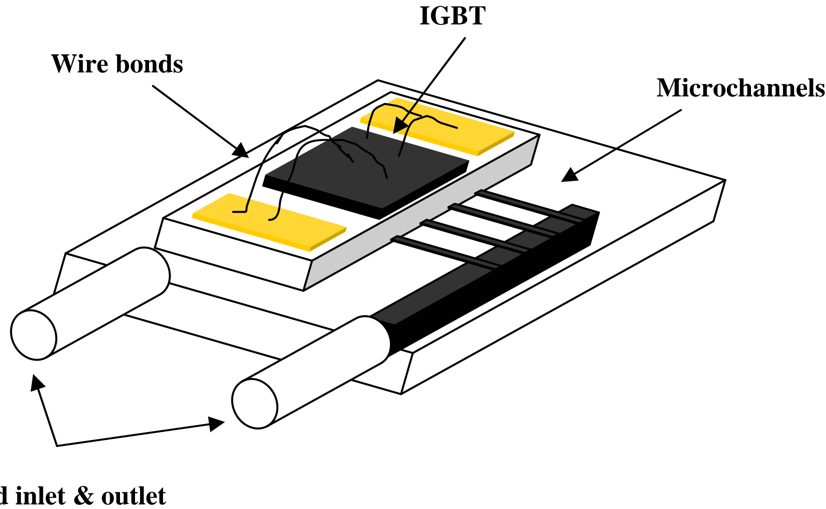


Figure 1.4 Conceptual drawing of an IGBT and integrated micro structure for single- and two-phase cooling

An advanced liquid cooled base plate can also improve thermal performance for IGBTs [7]. Multiple IGBTs are placed on a metal matrix composite (MMC) base plate. This base plate has been enhanced by using a pin pattern to increase surface area and promote turbulent flow. This structure reduces junction to fluid thermal resistance and provided a more uniform temperature across all of the devices. This package design gave a thermal resistance of 0.047 ^{o}C/W for a flow rate range of 0.8 to 4.2 gal/min, a 39 mbar pressure drop, and 800 W device loss.

A micro jet array was also demonstrated to cool a power MOSFET device [8]. This cooling structure is applied to the bottom side of the MOSFET and utilizes air rather than a liquid. The cooling structure was created by assembling 4 etched layers of silicon using epoxy. A micro structure is included to enhance the heat transfer at the stagnation region for each jet plume in a jet array. A detailed analysis of heat transfer for a micro jet array reported heat flux capability greater than 15 W/m^2 [9]. A conceptual drawing of the jet array cooling structure is shown in Figure 1.5.

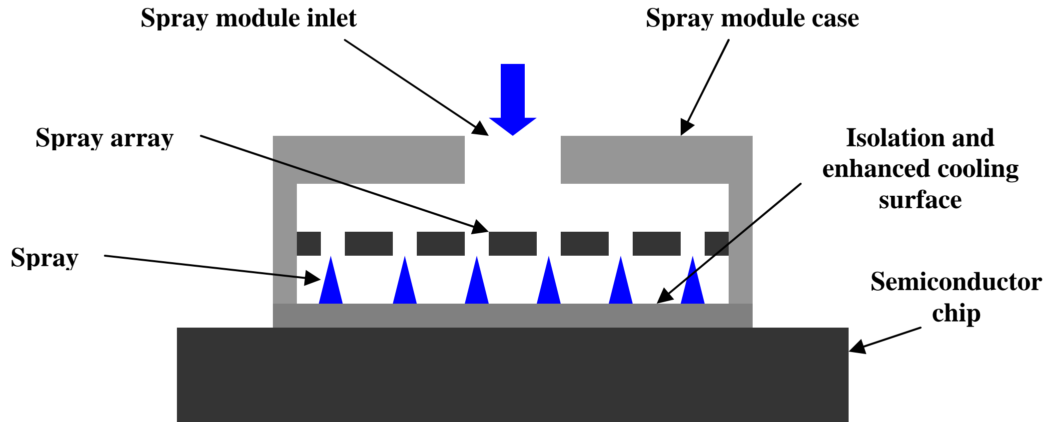


Figure 1.5 Structure of an air micro jet array for a power MOSFET

A more aggressive effort was made for wire bond packaging by implementing spray cooling [10]. Water spray was applied directly over an entire three phase motor drive system. Parylene was used to insulate the wire bonds and the chips themselves. This cooling method greatly improved thermal management for the semiconductors. A thermal resistance for the IGBTs in this system is estimated to be 0.05 ^{o}C/W for spray flow rates range of 0.05 to 0.34 gal/min and a system power loss of 670 W.

1.3.2 Non-Wire Bond Packaging and Cooling

Alternative non-wire bond power device packaging can provide a better opportunity to interface both sides of the semiconductor device with advanced cooling schemes. These non-wire bond packaging techniques include low temperature joining, flip chip solder balls interconnection technology, power overlay technology, DirectFET^{TM}, press pack technology, and embedded power technology [11-18]. Design complexity, cooling efficiency, electrical isolation and power density must be considered for each case when interfacing the device package with advanced double-sided cooling schemes.

Low temperature joining techniques have been used to connect IGBT devices to Direct Bond Copper (DBC) in order to achieve double-sided liquid cooling [9]. This technique increases cooling performance, but electrical isolation via DBC adds thermal resistance [11]. Figure 1.6 shows a cross section of the double-sided cooling structure

with power semiconductors. This package design gave a thermal resistance of 0.087 ^{o}C/W for a flow rate of 1.6 gal/min.

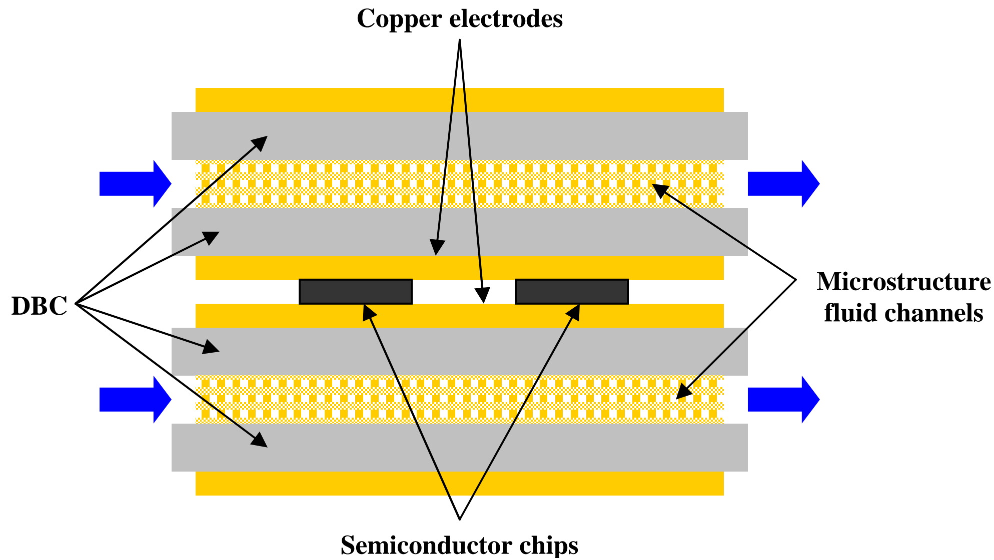


Figure 1.6 Cross section of power semiconductors connected to DBC using low temperature joining techniques (microstructures were formed between DBC pieces to create cooling fluid channels)

Flip chip solder ball interconnection technology can be used to eliminate cooling interface issues related to wire bonds, but electrical isolation requirements also limit the efficiency of the cooling system [12]. Micro channels are integrated directly in the package to provide double-sided cooling. The interface between the device and DBC via solder balls as well as the use of DBC as isolation between the device and heat sinks greatly reduces the heat transfer from the chip. This cooling and package configuration provides a thermal resistance of 0.09 to 0.12 ^{o}C/W for a flow rate range of 0.2 to 2 gal/min. Figure 1.7 shows a cross section of the structure.

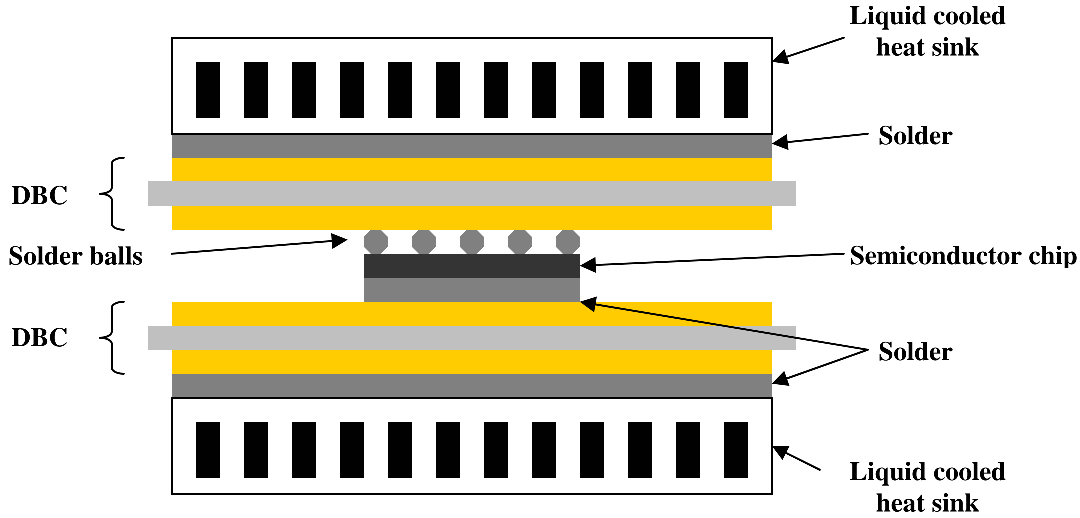


Figure 1.7 Cross section of a double–sided micro channel package for IGBTs using flip chip interconnection

Various other interconnection methods eliminate wire bonds and can interface with double-sided cooling. Most have been demonstrated with conduction and air cooling schemes, while most have not been implemented with advanced cooling schemes such as forced liquid convection or phase change. Power overlay technology is one such technology that could possibly be implemented in an advanced double-side cooling configuration [13]. Electrical isolation and mechanical structure would have to be considered when implementing this technology with liquid systems.

DirectFET™ by International Rectifier is a very promising packaging technology for low power devices on a single chip scale [14]. DirectFET™ boast double-sided cooling as a primary benefit of the package. Underfill is helpful in the implementation of this device and could be necessary to prevent non-dielectric fluid flow under the chip for some advanced cooling schemes cooling. As higher power devices are produced with this technology more advanced cooling schemes will most certainly be explored. A cross section of a DirectFET™ is shown in Figure 1.8.

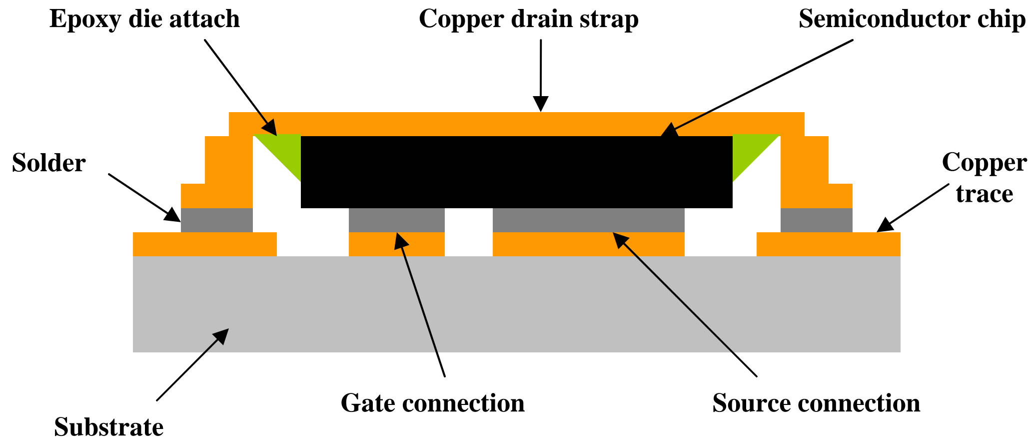


Figure 1.8 Cross section of a DirectFET™ device

Press-pack semiconductor packaging technology can also allow advanced double-side cooling schemes [15]. This example uses evaporators on both sides of the semiconductors. This method is promising for applications that use press-pack technology. Figure 1.9 shows the cross section of the press-pack and double-sided multiphase cooling structure.

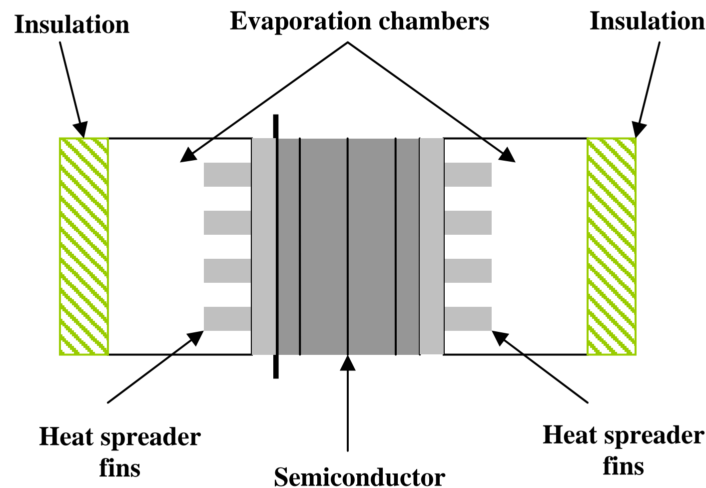


Figure 1.9 Cross section of a press pack semiconductor package with double-sided multiphase cooling channels

Double-sided cooling for embedded power has been explored for standard cooling techniques including conduction and forced air convection [16-18]. Planar metallization with a copper strap rather than wire bonds were used for electrical connection and heat

transfer through the top side of a MOSFET [17]. The copper strap does not provide a major improvement since the conduction path from the top of the semiconductor chip through the strap is long. This structure has some similarity to the DirectFET™ design.

A more direct cooling approach is shown by using DBC and heat sinks attached to the top side metallization of an embedded power package [18]. This scheme reduced thermal resistance between the device and cooling media, but a more advanced cooling scheme could improve heat transfer even greater. Figure 1.10 shows a cross section of embedded power configured for double-sided air cooling.

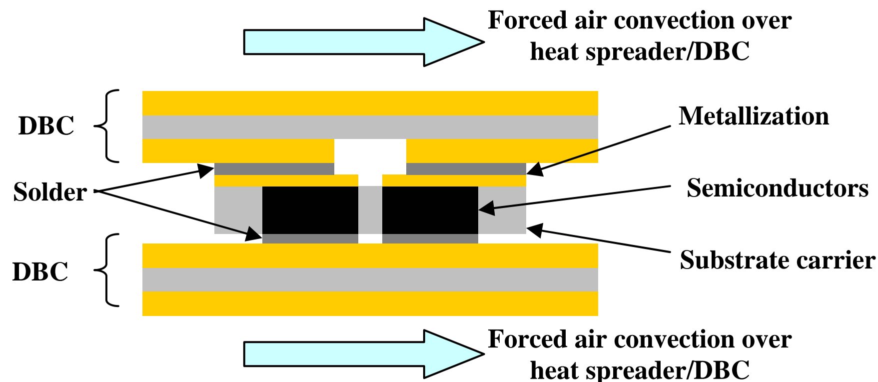


Figure 1.10 Cross section of embedded power with double-sided air cooling

A summary of cooling and packaging technologies previously explored can be seen in Table 1.1. Some packaging technologies, such as DirectFET™, press pack, and power overlay, are not included in Table 1.1 since advanced cooling schemes have not been reported with these technologies. From the survey it is easy to notice many research avenues for advanced cooling and packaging for power semiconductor devices. Both single- and multi-phase forced liquid cooling techniques have been explored for wire bond packaging. Non-wire bond packaging has been used to implement double-sided air and liquid cooling. Micro channels or micro structures are often utilized with liquid or air cooling for wire bond and non-wire bond packaging. High flow rate liquid convection has been used with several packaging technologies, but not embedded power. Higher velocity, forced liquid convection close to or directly on both sides of a power semiconductor in embedded power technology is new and reasonable area of study.

Table 1.1 Summary of cooling and packaging technologies explored for power semiconductor components and systems

Interconnect and packaging technology [Reference]	Type of cooling	Number of cooling sides	Total package thermal resistance (C/W)	Flow rate	Device & Cooling Area	Device Loss (W)
Wire bond module with liquid cooled base plate [4]	Forced liquid convection	1	0.02-0.01	0.4-1.8 gal/min	12 APT 20M38DVR 200V MOSFETS	1300
Wire bond module with microchannels [5]	Forced liquid convection	1	0.1	0.4 gal/min	1 SIEMENS 1600 V, 50 A IGBT (14x14 mm)	300
Wire bond module with microchannels [5]	Multiphase forced convection	1	0.1	0.007 gal/min	1 SIEMENS 1600 V, 50 A IGBT (14x14 mm)	300
Wire bond module with microchannels [6]	Forced liquid convection	1	0.09-0.11	1.9-4.4 gal/min	2 IGBT on Cu heat spreader (51x19 mm)	300
Wire bond module with liquid cooled MCM base plate [7]	Forced liquid convection	1	0.047	0.8-4.2 gal/min	12 IGBT (9.5x9.5 mm) and 12 diodes (7x7mm)	800
Wire bond system [10]	Water spray convection	1	0.05	0.05-0.34 gal/min	3-phase IGBT module (Eupec BSM50GD120DN2)	670
Low temperature joining of DBC with microchannels [11]	Forced liquid convection	2	0.087	1.6 gal/min	1 IGBT (12x12mm)	900
Flip chip solder ball module [12]	Forced liquid convection	2	0.12-0.09	0.2-2 gal/min	1 IGBT (11.8x11.8mm)	300
Embedded power [16]	Forced air convection	1	2-3	0.0094 m^3/s	2 MOSFET (8.8x7.1mm) on Cu spreader (2x3.5cm)	6-9
Embedded power with copper strap [17]	Thermo-electric cooler	2	0.55		1 MOSFET	19
Embedded power [18]	Forced air convection	2	14.07	0.05 m^3/s	1 MOSFET (8.8x7.1mm)	1.4
Embedded power with double-side DBC[18]	Forced air convection	2	11.29	0.05 m^3/s	1 MOSFET (8.8x7.1mm)	1.86
Embedded power with double-side DBCand heat spreaders[18]	Forced air convection	2	5.38	0.05 m^3/s	1 MOSFET (8.8x7.1mm)	1.8

1.4 Embedded Power Technology with Forced Liquid Convection

Embedded power technology is an advanced packaging technology with a structure favorable for interface to advanced cooling schemes. The basic structure and construction details for embedded power are defined by Liang [16]. Figure 1.11 shows an example of a power factor correction (PFC) integrated power electronics module using embedded power technology with a CoolMos^{TM} and SiC Schottky diodes. This module shows the possible improvement to power density of an active power stage for a power converter. Embedded power technology may provide other benefits, including improved electrical performance and system manufacturing ability.

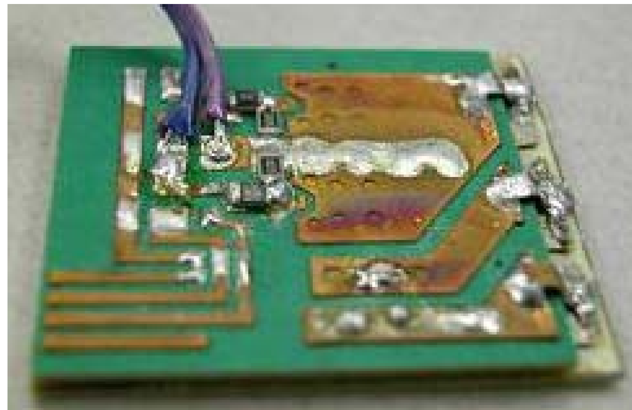


Figure 1.11. Power factor correction (PFC) integrated power electronics module using embedded power technology with a CoolMos^{TM} and SiC schottky diodes

This device packaging technology can easily envisage single or double-sided conductive cooling since wire bonds are eliminated [16-18]. Table 1.1 gives expected thermal resistances for different cooling configurations. An alternate and more advanced cooling method, such as forced liquid convection, can be applied in a similar manner by interfacing the device package with a module or larger package to contain and control fluid flow directly across top and bottom side interconnects. Figure 1.12 shows a cross section of this proposed interface of the embedded power package with a forced liquid cooling system.

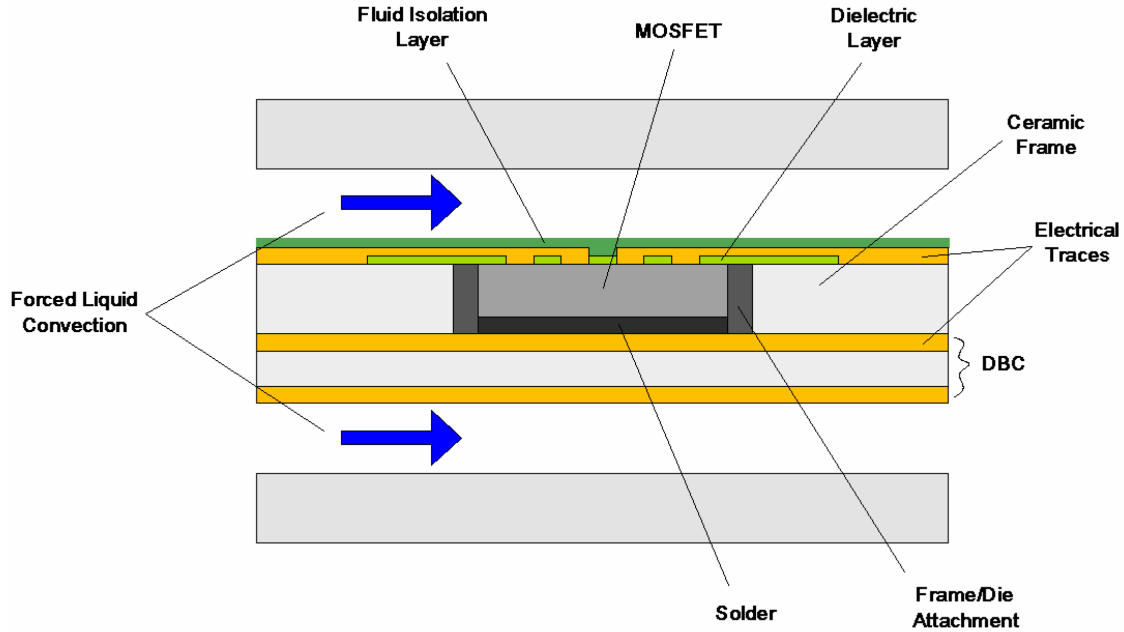


Figure 1.12 Cross section of typical embedded power technology structure with proposed double-sided liquid cooling

1.5 Objectives

A state of the art survey of thermal management and packaging schemes for power semiconductor devices quickly shows that a double-sided, high flow rate cooled embedded power package is a value topic to explore. Wire bond packaging and advanced cooling schemes have been explored thoroughly, but cooling potential is usually limited by single-side cooling. Non-wire bond packaging provides the opportunity for advanced double-sided cooling. Micro channels and micro structures have been implemented with both types of packaging and show promise when higher flow rates can be achieved. The goal of this thesis is to identify the potential of embedded power with double-sided, high flow rate forced liquid convection using a liquid cooling test bed.

Chapter 2 will present the development of a physics based electro-thermal model, which is used to predict the improvements provided by embedded power technology with double-sided forced liquid convection. Chapter 3 will discuss the design, development, and results of an experimental study used to verify thermal modeling predictions as well as explore practical issues of implementing double-sided liquid cooling with embedded power packaging. Finally, chapter 4 gives some conclusions and topics for future work.

2 THERMAL MODELING

Thermal modeling was considered as the next research tool after reviewing the state of art technology related to advance cooling schemes for power semiconductors. Several thermal modeling techniques were available, including finite difference techniques using Mathematica or Matlab, finite element software such as ANSYS, IDEAS or Flotherm, and physics based electro-thermal modeling using Saber or other electrical simulation software. A quick simulation method was preferred and electro-thermal modeling would provide this while being accurate. Physics based electro-thermal models were used to help predict the improvement provided by double-sided forced liquid convection with embedded power technology in comparison to single-sided forced liquid convection. The remainder of this chapter gives a description of the physics based electro-thermal modeling technique used, an example of electro-thermal modeling applied to embedded power, and a comparison of embedded power with double-sided forced liquid convection to a wire bond package with single-sided forced liquid convection.

2.1 Physics Based Electro-Thermal Modeling Background

Physics based electro-thermal models can be constructed simply and then simulated in electrical simulation software such as Saber. The construction of an electro-thermal model for a power semiconductor package with forced liquid cooling requires several elements to represent the forms of heat transfer. These elements include the thermal resistance of solid materials, the thermal capacitance of solid materials, and the thermal resistance of heat transfer via forced liquid convection. These elements are placed in a Cauer RC electrical circuit similar to the circuit example shown in Figure 2.1 [19-20]. Current sources represent heat flux boundary conditions while voltage sources represent temperature boundary conditions. Voltage and current values therefore represent temperature and heat flux values.

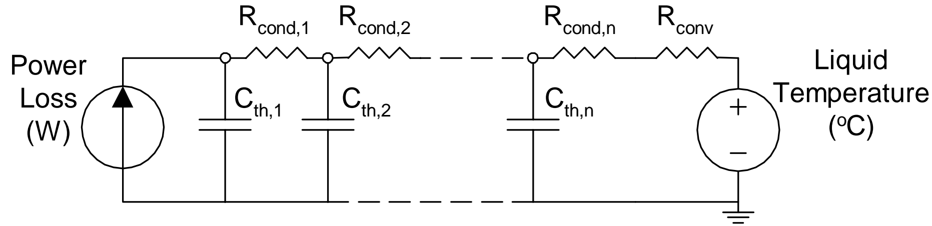


Figure 2.1 Cauer RC electro-thermal simulation circuit example

To simplify the development of each of these electro-thermal components, several key assumptions were made. One dimensional heat transfer is assumed to greatly reduce the complexity of the model. This assumption is reasonable since a semiconductor device has a considerably greater area versus height. Thermal capacitances can be eliminated in the model when only studying steady state thermal conditions. Interfacial thermal resistance between solid materials is also neglected. This assumption is necessary since interfaces are difficult to characterize and control. Solid material properties and fluid properties were considered to be constant since these properties change very little over the temperature range expected, 25 ^{o}C to 150 ^{o}C. Heat transfer through forced liquid convection is also assumed to be the only form of heat removal from the semiconductor device. This is hard to control in most experimental cases, but heat transfer through high velocity fluid convection is considered to dominate most other forms of heat transfer encountered. This can be confirmed easily for the most likely case by comparing the range of forced water convection thermal resistance to the thermal resistance range of natural air convection from Figure 1.1. Fluid flow is considered to be fully developed and in the turbulent flow regime with $3000<Re_D<5x10^6$. This assumption is reasonable for high velocity fluid flow and can be checked by calculating the Reynolds number. The following two sections describe the construction of conduction based thermal resistance and convection thermal resistance.

2.1.1 Conduction Heat Transfer Modeling

Electro-thermal model components for conduction heat transfer are simple to create in comparison to convection based thermal resistance. Conduction based thermal resistance can be calculated based on equation 1.1 [21].

$$R_{conduction} = \frac{L}{kA_s} \tag{1.1}$$

A_s is the area of the device, while L is the thickness of each layer of material under the device. Solid material thermal conductivity is defined by k.

2.1.2 Convection Heat Transfer Modeling

Convection thermal resistance can be extremely complicated to formulate. This is due to combining fluid mechanics and heat transfer, which are both complex subjects. The assumptions mentioned previously help to reduce the formulation and simulation difficulties for convection heat transfer. A convection thermal resistance can be found from equations 1.2 through 1.4 [21].

$$R_{convection} = \frac{1}{hA_s} \tag{1.2}$$

$$h = \frac{Nu_D D_h}{k_f} \tag{1.3}$$

$$D_h = \frac{4A_c}{P} \tag{1.4}$$

D_h is the hydraulic diameter in the cooling chamber, A_c is the cross sectional area of fluid flow, and P is the perimeter of rectangular flow area. Fluid thermal conductivity is defined by k_f. The Nusselt number, Nu_D, is a function of the Reynolds number, which is defined by equation 1.5 [21].

$$\mathrm{Re}_D = \frac{\rho u_m D_h}{\mu} \tag{1.5}$$

Fluid density and viscosity are defined by ρ and μ, respectively. An average Reynolds number can be calculated by finding a mean velocity, u_m, in the cooling region. The mean velocity in the cooling region is calculated from using equation 1.6 assuming a fluid flow rate, F is known.

$$u_m = \frac{F}{A_c} \tag{1.6}$$

It was assumed that the flow in the cooling region is in the turbulent regime with $3000<\mathrm{Re}_D<5\ \mathrm{x}10^6$. Based on this assumption, Nu_D can be found for fully developed turbulent flow through a rectangular duct from the correlation proposed by Gnielinski, which is given by equations 1.7 and 1.8 [21].

$$Nu_D = \frac{(f/8)(\mathrm{Re}_D - 1000)\mathrm{Pr}}{1+12.7(f/8)^{1/2}(\mathrm{Pr}^{2/3}-1)} \tag{1.7}$$

$$f = (0.79\ln \mathrm{Re}_D - 1.64)^{-2} \tag{1.8}$$

These equations are valid for fluid properties and flow conditions such that $3000<\mathrm{Re}_D<5\ \mathrm{x}10^6$ and $0.5<\mathrm{Pr}<2000$. The Prandtl number, Pr, can be calculated based on equation 1.9, where c_p is specific heat of the fluid [21].

$$\mathrm{Pr} = \frac{c_p \mu}{k_f} \tag{1.9}$$

2.2 Package Structure and Thermal Models

The following sections describe the packaging structures under study and their thermal models.

2.2.1 Embedded Power Package

A completed example of embedded power with CoolMOS™ and SiC schottky diodes for power factor correction applications was shown in Figure 1.11. A detailed cross section of a similar package with a single MOSFET is shown in Figure 2.2. Design and construction details are described by Liang [16]. As described in a previous section, this package can be interfaced with forced liquid convection using a liquid module to contain and control fluid flow over the top and bottom side of the embedded power package. Direct fluid flow requires a thin insulation layer to be applied to the gate/source

side of the MOSFET for electrical insulation and to prevent degradation of the chip interconnections by mechanical abrasion. Enthone® DSR-3241 liquid photoimageable solder mask is a reasonable material to use for this purpose, but other materials including sputtered silicon nitride, sputtered aluminum nitride, or chemical vapor deposited parylene may be better candidates for even greater heat transfer [22]. This insulation layer could also be eliminated if a dielectric fluid was used, but mechanical abrasion of the copper traces and the semiconductor chip would still need to be considered. DBC and solder are used as a drain interconnection. This DBC/solder interconnect also acts as isolation and mechanical support, but could be replaced by a planar metallization interconnection similar to the top side to further improve heat transfer.

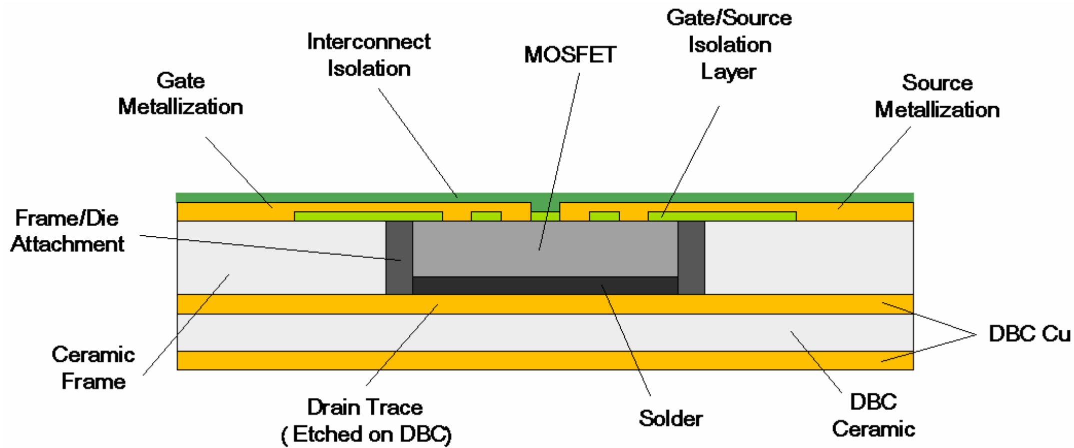


Figure 2.2 Cross section of embedded power technology with DBC base

A one dimensional, physics based electro-thermal model can be constructed for an embedded power package by first identifying the loss or heat source, which in this case is a single MOSFET device, Advanced Power Technology (APT) APT60M75DFLL, with dimensions of 11.9 mm x 16.5 mm x 0.254 mm [23]. Next, all solid material layers should be identified and their thicknesses and material properties recorded. This information can be used to calculate thermal resistance using equation 1.1. The material properties and thermal resistances of all solid layers in the embedded power package are shown in Table 2.1.

Table 2.1 Thermal resistance values for embedded power technology

	L	***k***	A_s	R_{th}
	m	$\frac{W}{mK}$	m^2	$\frac{W}{C}$
Bottom half of silicon chip	0.000127	118	0.000196	0.0457
Solder	0.0004	57	0.000196	0.0357
DBC copper	0.0006096	380	0.000196	0.0082
DBC ceramic	0.000635	26	0.000196	0.1242
Top half of silicon chip	0.000127	118	0.000196	0.0457
Copper connections	0.0000508	380	6.735x10^{-5}	0.002
Screen printed dielectric	0.0000508	0.3942	1.291x10^{-4}	0.9979
Electroplated copper	0.0000762	380	0.000196	0.001
Solder mask insulation	0.00002	0.08368	0.000196	1.5448

Convection thermal resistance can be calculated based on equations 1.3 through 1.10. A fluid flow range between 0 and 10 gal/min with water in a rectangular duct with flow cross section dimensions 42 mm x 5 mm was assumed. Fluid properties are summarized in Table 2.1 and fluid velocity versus flow rate for this cross sectional area is shown in Figure 2.3. The Reynolds number versus flow rate is shown in Figure 2.4. A red line was added at F≈0.6 gal/min, which gives a Reynolds around 3000, the lower limit of the turbulent convection correlation given in equation 1.7. Figure 2.5 through Figure 2.7 show the friction factor, the Nusselt number, and the convection heat transfer coefficient versus flow rate. Figure 2.8 gives the convection thermal resistance for a single side of a chip. The lower limit of the convection model is depicted with a red line in appropriate graphs.

Table 2.2. Thermal and flow properties of water at 25°C

	ρ	μ	k_f	c_p	**Pr**
Water	$1000\,\frac{kg}{m^3}$	$855\text{x}10^{-6}\,\frac{N \cdot s}{m^2}$	$613\text{x}10^{-3}\,\frac{W}{mK}$	$4.179\,\frac{kJ}{kg \cdot K}$	5.83

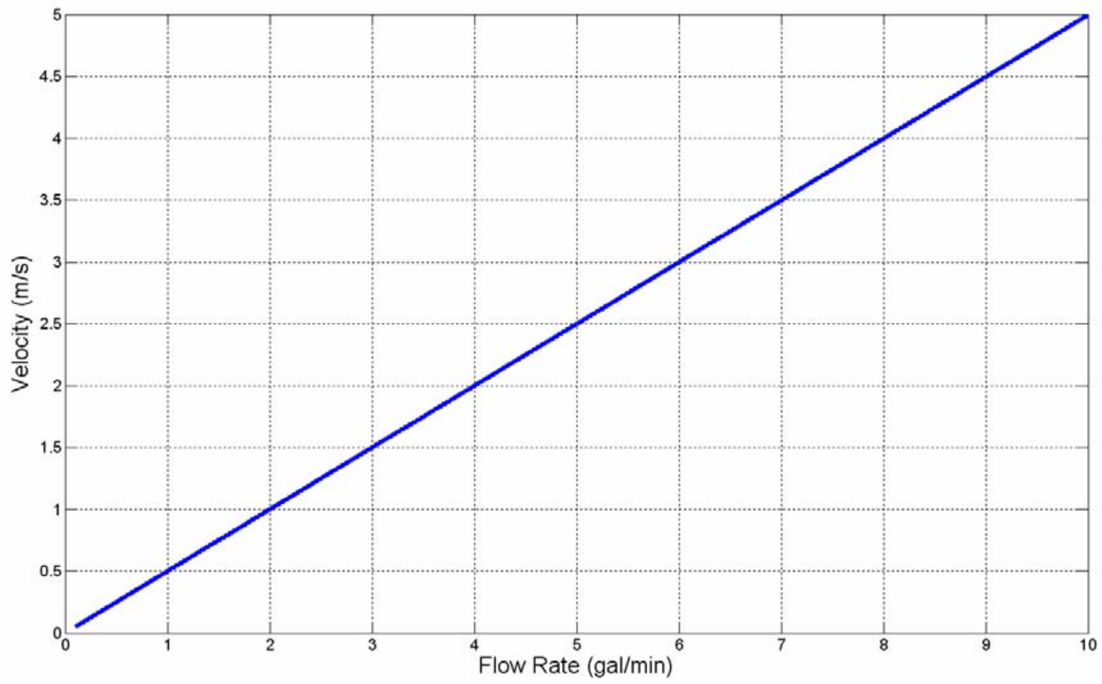


Figure 2.3 Fluid velocity, u_m versus flow rate, F

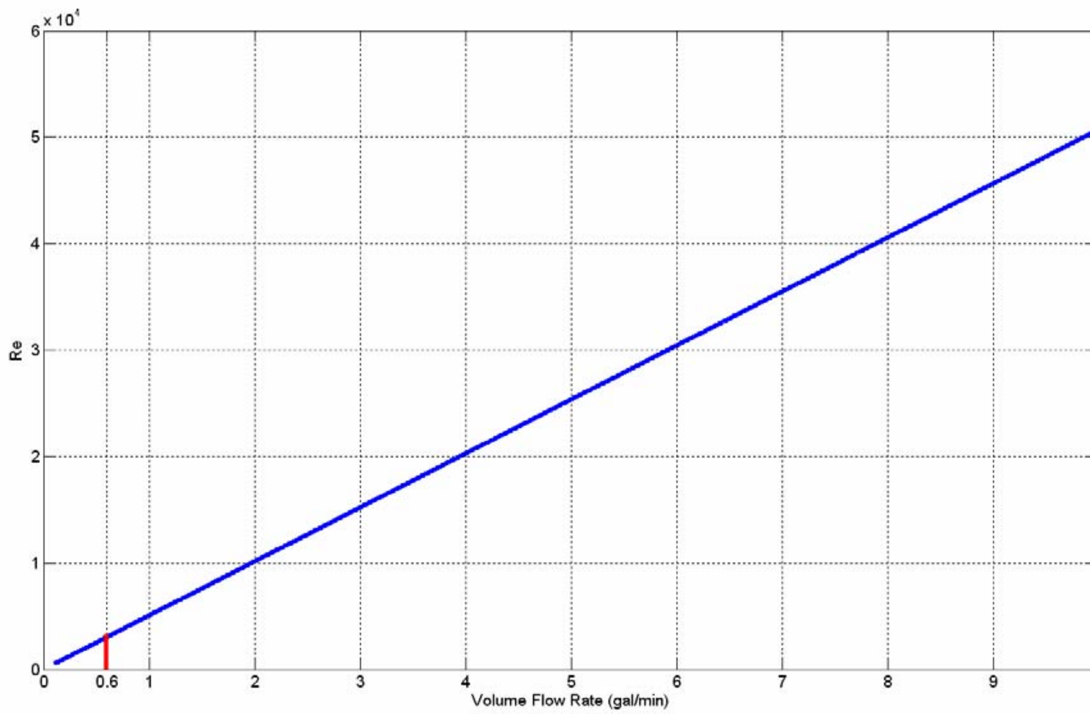


Figure 2.4 Reynolds number, Re_D versus flow rate, F

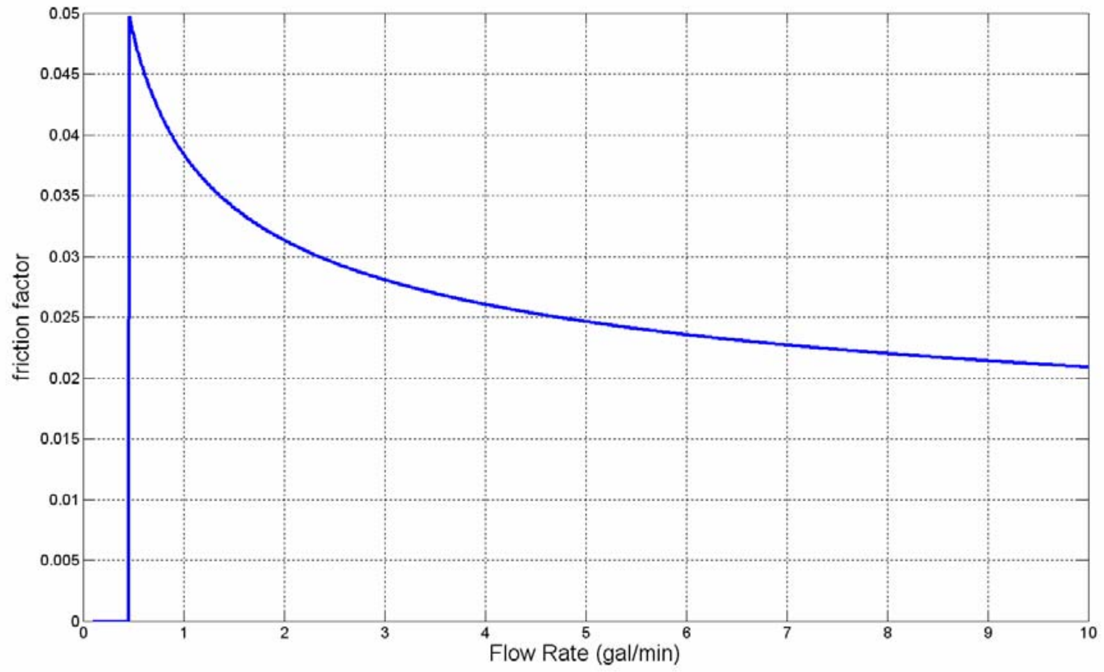


Figure 2.5 Friction factor, *f* versus flow rate, *F*

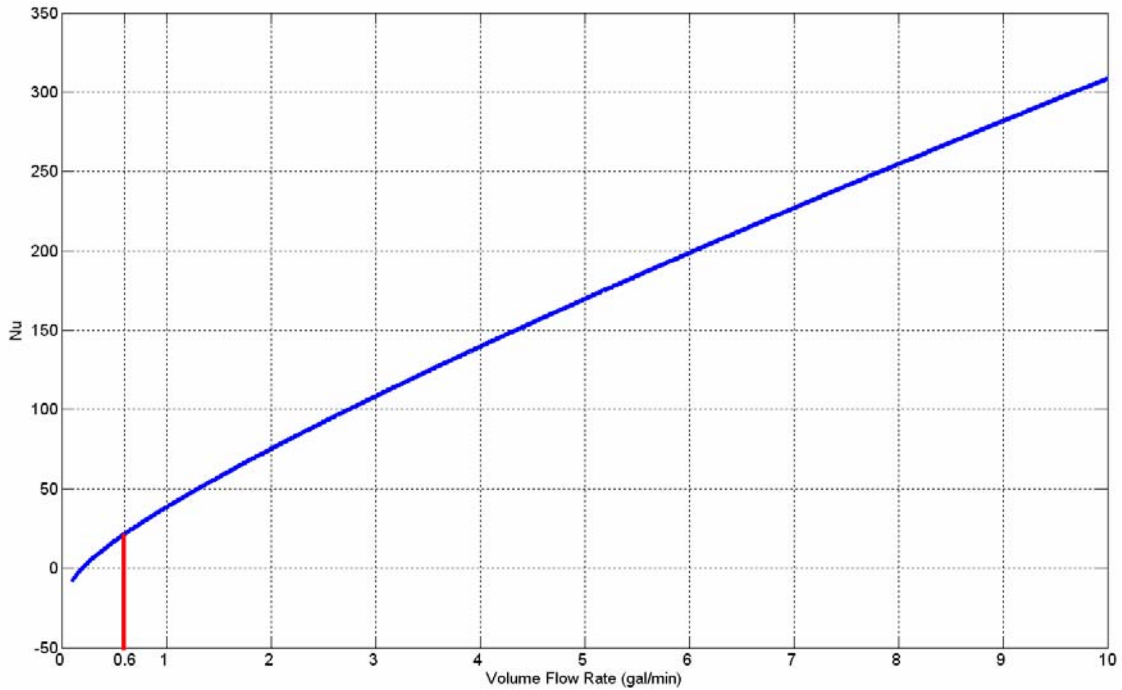


Figure 2.6 Nusselt number, Nu_D versus flow rate, *F*

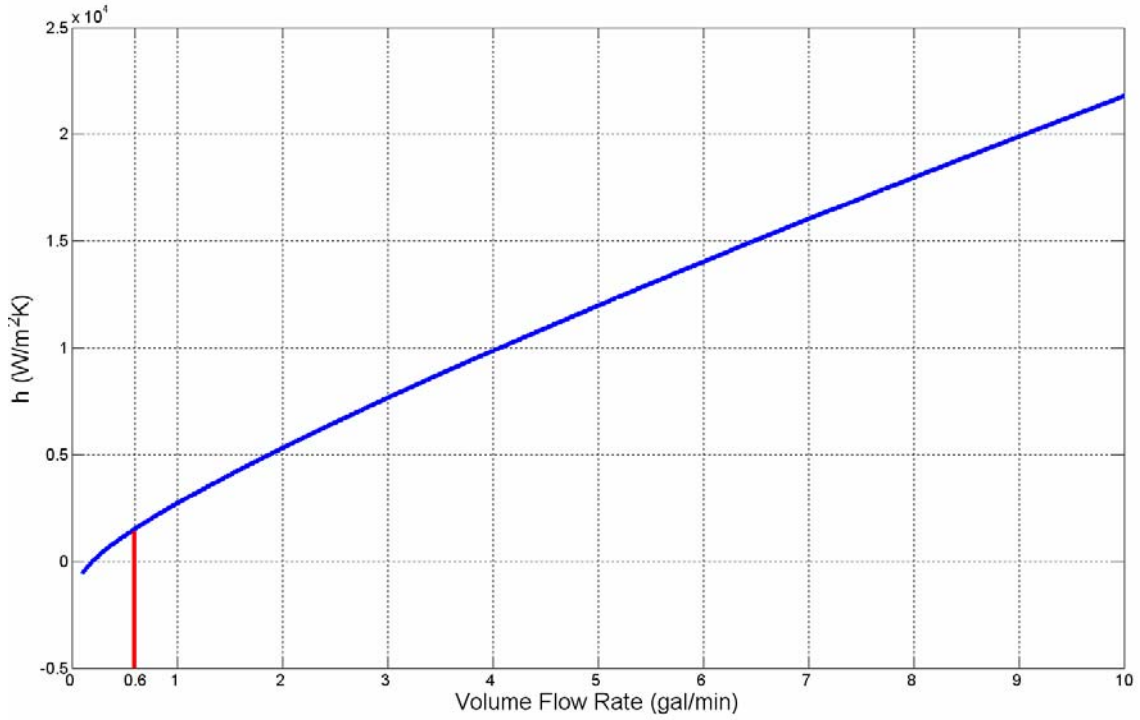


Figure 2.7 Convection heat transfer coefficient, *h* versus flow rate, *F*

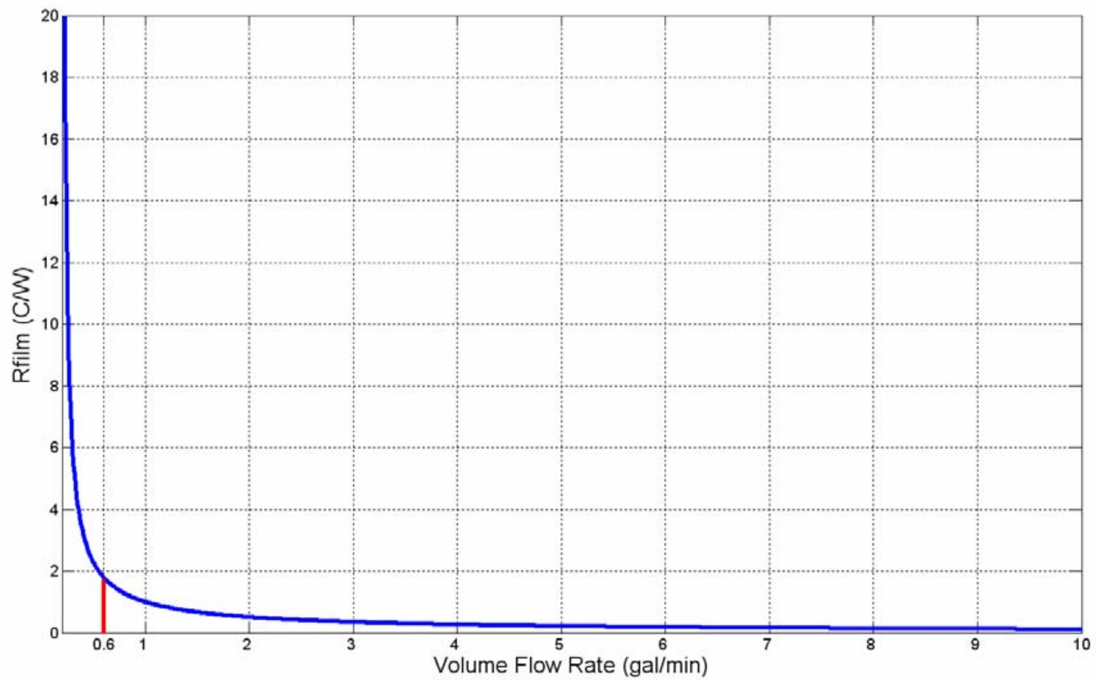


Figure 2.8 Convection thermal resistance, $R_{convection}$ versus flow rate, *F*

A thermal model for embedded power with a single APT APT60M75DFLL MOSFET and a water flow rate between 0 and 10 gal/min can now be constructed as shown in Figure 2.9. The MOSFET power loss can be defined as a single current source and fluid temperature can be set by a voltage source.

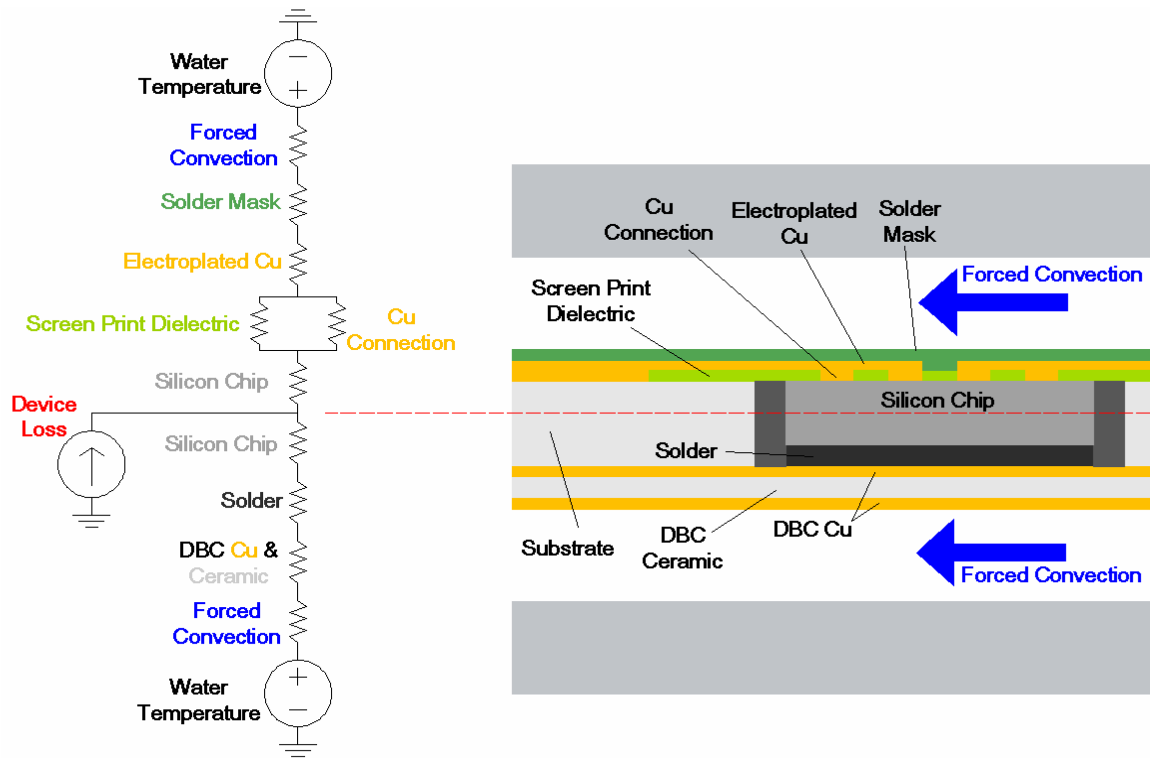


Figure 2.9. Thermal model for embedded power with double-sided forced liquid convection

2.2.2 Wire Bond Package

A wire bond based package with single-side forced liquid convection was chosen to compare to the high fluid flow rate cooled embedded power package. A cross section of a wire bond based package with single-sided liquid cooling is shown in Figure 2.10. A protective silicone based, dielectric gel is typically placed on the top side of a wire bond device. This gel is considered as an electrical and thermal insulator, so heat can only pass through the bottom side of the device through the DBC. This heat transfer path is assumed to be the same as the bottom side of the embedded power case. The wire bond package solid layers and their respective properties and thermal components are shown in

Table 2.3. The convection thermal resistance found previously for the embedded power case with a water flow rate of 0 to 10 gal/min is used with the wire bond package.

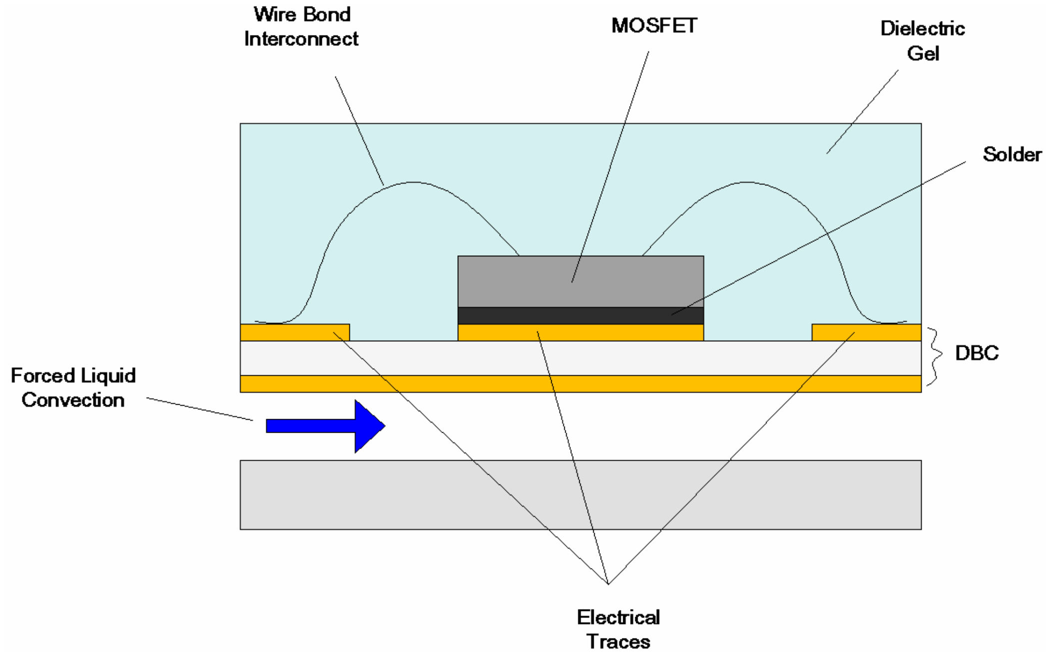


Figure 2.10 Cross section of wire bond package with single-sided liquid cooling

Table 2.3 Thermal resistance values for wire bond packaging

	L	k	A_s	R_{th}
	m	$\frac{W}{mK}$	m^2	$\frac{W}{C}$
Bottom half of silicon chip	0.000127	118	0.000196	0.0457
Solder	0.0004	57	0.000196	0.0357
DBC copper	0.0006096	380	0.000196	0.0082
DBC ceramic	0.000635	26	0.000196	0.1242

A thermal model for a wire bond package with a single APT APT60M75DFLL MOSFET and a water flow rate between 0 and 10 gal/min can now be constructed as shown in Figure 2.11.

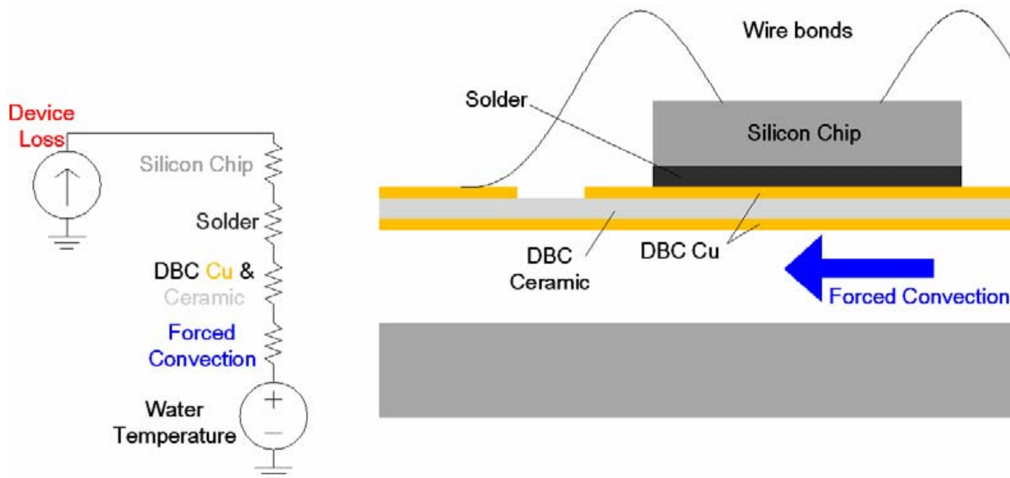


Figure 2.11 Thermal model for a wire bond package with single-sided forced liquid convection

2.3 Thermal Modeling Results

The thermal models for the embedded power and wire bond packages were compared to predict the improvements of high velocity double-side forced liquid convection. Total junction to case thermal resistance can be found by adding conduction thermal resistance to convection thermal resistance. These resistances are shown versus flow rate in Figure 2.12. The total junction to case thermal resistance versus flow rate is shown in Figure 2.13. The percentage improvement provided by double-sided cooling over single-sided cooling is shown in Figure 2.14. This plot shows approximately 48% improvement at low flow rates and 20% improvement at high flow rates for double-side cooled embedded power packaging versus single-side cooled wire bond packaging.

This improvement is due to the additional heat removal path of the embedded power package. The improvement decreases with flow rate because the bottom side total thermal resistance of the embedded power is used for the wire bond thermal model. Therefore the wire bond total package thermal resistance approaches that of the embedded power package at high flow rates. The top side and bottom side of the device contribute differently to the overall efficiency of double-sided cooling due to different solid layers above and below the device in embedded power technology. This can be seen clearly in Figure 2.12. Alternate insulation materials may make the top-side cooling more effective. It can be predicted that a 300 W semiconductor device loss can be

achieved with this MOSFET in embedded power with high flow rate cooling while keeping the device below its maximum junction temperature of 150 ^{o}C.

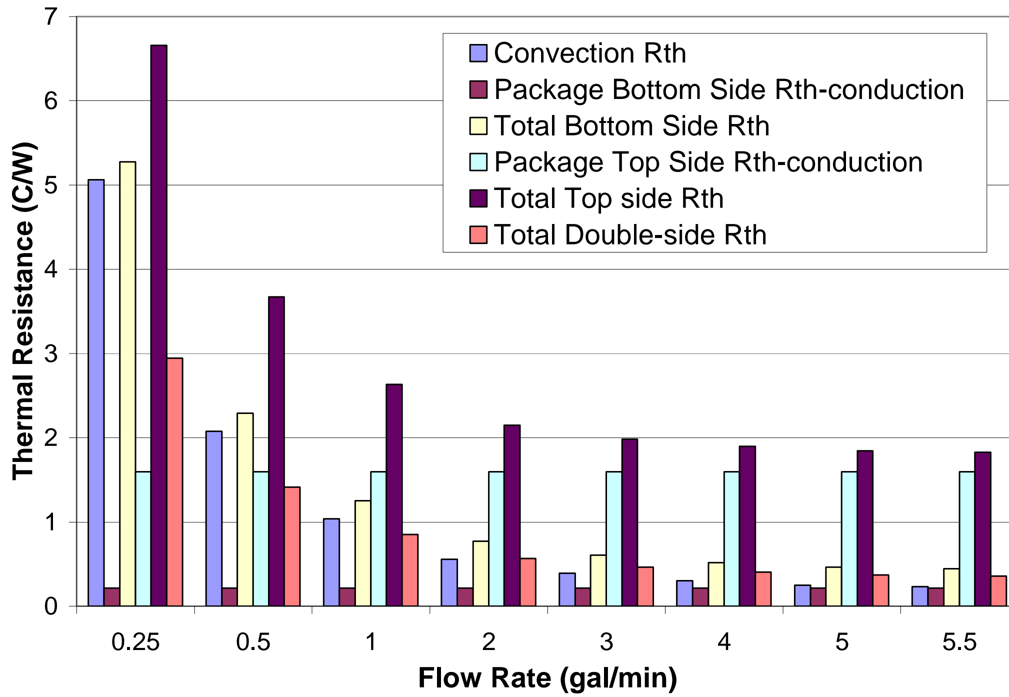


Figure 2.12 Comparison of conduction and convection thermal resistances found from thermal modeling

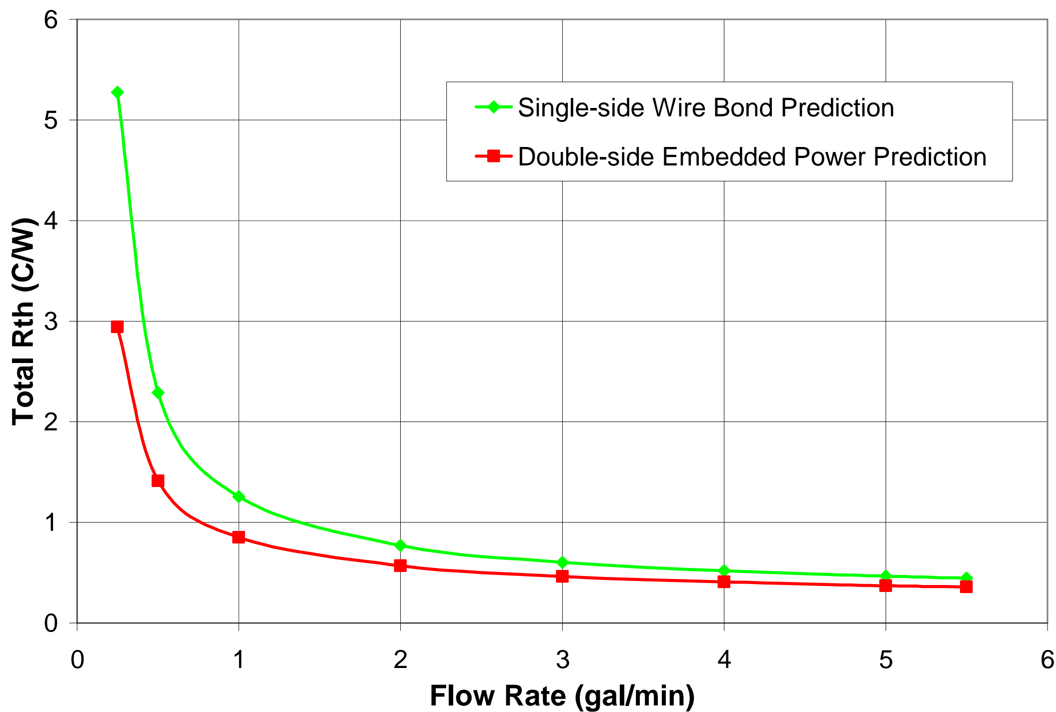


Figure 2.13 Predicted total junction to case thermal resistance comparison for double-side cooled embedded power packaging and single-side cooled wire bond packaging versus flow rate

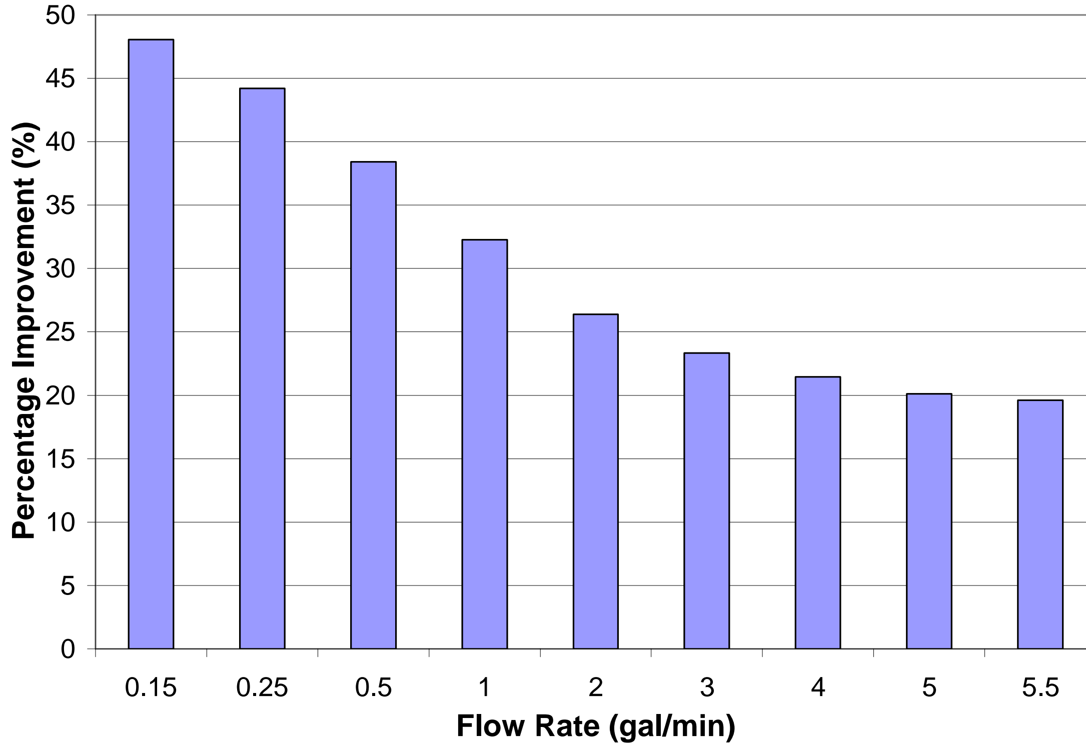


Figure 2.14 Predicted percentage improvement provided by double-sided cooling over single-sided cooling

2.4 Thermal Modeling Summary

Thermal modeling helps show the potential of double-sided forced liquid convection with embedded power versus a wire bond package with single-sided forced liquid convection. One dimensional, physics based electro-thermal models provide a quick and accurate modeling method. An improvement of approximately 48% for low flow rates and 20% for high flow rates is predicted for thermal resistance of the double-side cooled embedded power package compared to the single-side cooled wire bond package for planar water flow rate between 0 and 5.5 gal/min. Maximum temperature rise for a power semiconductor can be significantly reduced due to this reduction in overall thermal resistance. The cooling potential for high flow rates in conjunction to double-sided heat transfer is clearly shown.

3 EXPERIMENTAL VERIFICATION

Experimental verification can verify the potential predicted in thermal modeling for double-sided, high velocity, forced convection with embedded power technology. Experimenting with embedded power and liquid cooling also helps identify design issues and future work for the implementation of a similar system in a commercial or military application. A test bed for liquid cooling of power semiconductors is also developed from this experimentation and can be applied to future semiconductor package designs.

This chapter presents the design and construction details for experimental analysis of high velocity, liquid-cooled power semiconductor packaging. A liquid module test bed was created to interface power semiconductor packaging technologies to high velocity fluid flow. A MOSFET based embedded power package and a wire bond package were designed and constructed to mimic the package cases reviewed in thermal modeling and allow attachment to the liquid module test bed. Design challenges are reviewed and experimental results are given. Thermal modeling results are also compared to experimental results to analyze the overall prediction quality.

3.1 Liquid Module Test Bed

A packaging structure is required to interface cooling fluid to the power semiconductor packaging. This packaging structure contains the fluid while controlling its direction over the semiconductor devices. A liquid module test bed was designed to handle a fluid range of 0 to 6 gal/min and provide planar flow over the packaging structures studied with thermal modeling. Future liquid module designs could incorporate perpendicular flow types, such as spray cooling or jet impingement, by adding connections and fluid distribution channels through the bottom of the modules in the cooling region. The cross sectional flow region was designed with dimensions similar to those assumed in thermal modeling while the length of the cooling region was chosen to allow reasonable sample cooling area. It was desired to create a module, which would allow for quick and easy change of samples without destroying the module or semiconductor package. This is achieved by employing a substrate frame, which can be permanently attached to the semiconductor package via a sealing adhesive, and a viton o-

ring seal to attach this frame to the liquid module. O-ring material choice and gland design details can be found in from Erik's technical documentation on o-rings [24]. The liquid module and sample frame were drawn in Autocad as shown in Figure A.1.

The final pieces were manufactured in multipurpose 6061 alloy Aluminum by Metal Processing Inc. in Radford, Virginia and are shown in Figure 3.1. Aluminum was chosen due to its excellent machining qualities, strength and light weight. The sample frame design causes some bowing to appear after machining. This was ignored assuming pressure applied by the liquid module would flatten the frame and provide a good seal. Future designs should consider this by choosing an alternate material or defining a specific machining method. The liquid module has a powdered finish and the substrate frame has a polished finish to improve the seal between these pieces around the o-ring. Brass pipe compression fittings are used to attach round pipe to the module ends allowing connection to a fluid system. Bolts are used to connect the pieces of the package and apply pressure. These bolts can also be used to connect the package to a testing bench or converter case. Figure 3.2 and Figure 3.3 show the liquid module test bed in single-side and double-side test configuration, respectively.

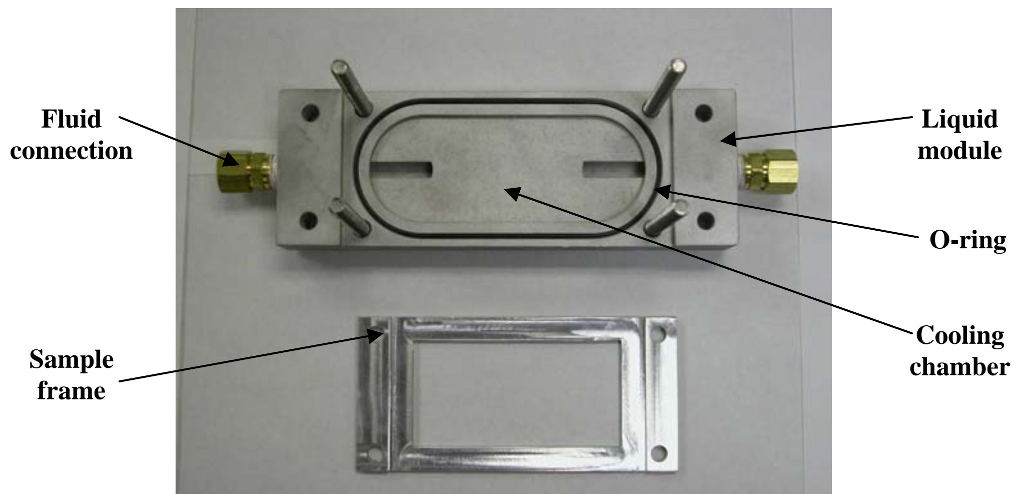


Figure 3.1 Liquid module test bed and sample frame

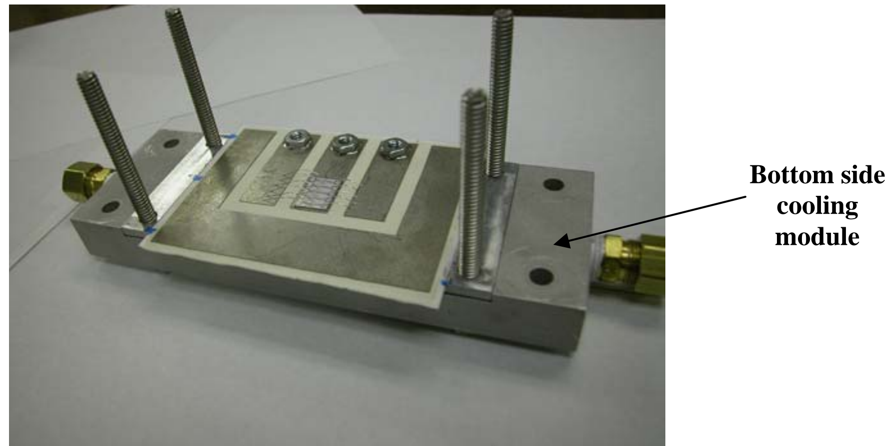
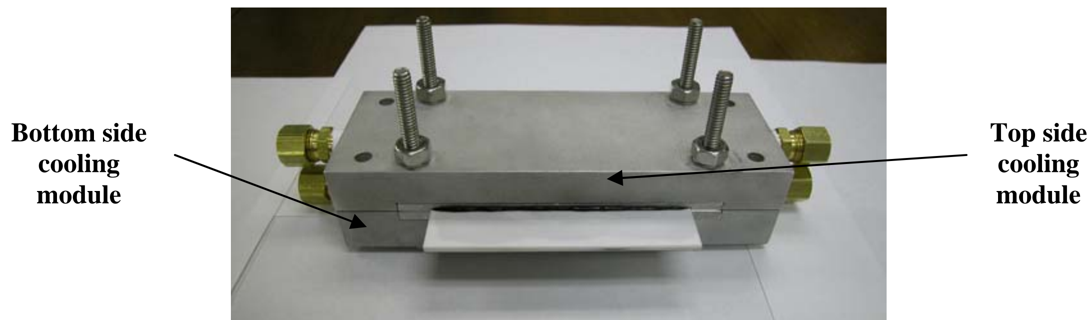


Figure 3.2 Liquid module in single-side cooling test configuration



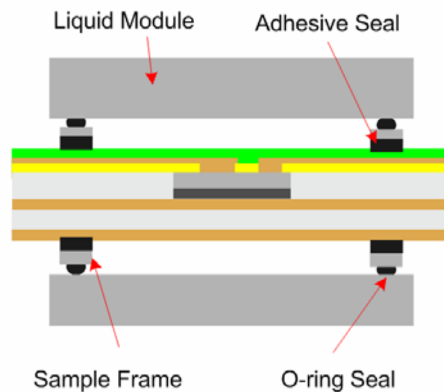


Figure 3.3 Picture and cross section of liquid module test bed in double-side cooling test configuration

3.2 MOSFET for Experimental Verification

A MOSFET based package was chosen for experimental verification to more closely represent a power converter semiconductor package. Other components like diodes and resistors could also be used to explore the potential of double-side cooled

embedded power packaging, but each have advantages and disadvantages for research, which must be considered. High power chip resistors that have similar thickness and footprint to high power, power semiconductors are not available as standard commercial products. Power diodes could have been implemented rather than MOSFETs, but a working power MOSFET sample could eventually be placed directly in a switching power converter system. Using a MOSFET rather than other components is much more useful in order to explore practical design and manufacturing issues for a switching power semiconductor in an embedded power package with high velocity fluid flow.

The MOSFET chosen for experimental verification is APT60M75DFLL by Advanced Power Technology and was previously used for the thermal modeling example in section 2.2 [23]. A picture of the bare FREDFET is shown in Figure 3.4. The die dimensions, gate structure, and source structure are available from Advanced Power Technology [25]. The die has titanium-nickel-silver (Ti-Ni-Ag) metallization on the backside or drain, which can handle most solders [25]. Key characteristics can be taken from the datasheet for its discrete counterpart and are listed in Table 3.1 [23]. Low voltage forward characteristics for this FREDFET can also be obtained from the device datasheet and are used to determine the device power loss range possible with different gate to source voltage V_{GS}, drain current I_D, and drain-to-source voltage V_{DS}.

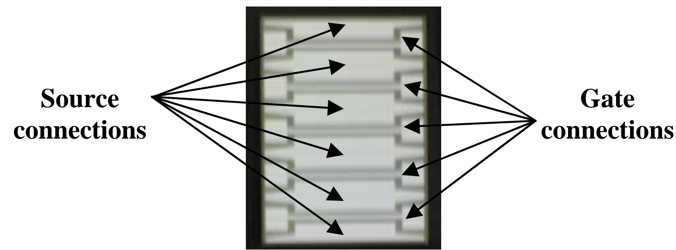


Figure 3.4 APT APT60M75DFLL FREDFET device

Table 3.1 APT APT60M75DFLL FREDFET key parameters

	V_{DS}	I_D	$V_{GS(th)}$	$R_{DS(on)}$	$T_{J(max)}$
APT60M75DFLL FREDFET	600V	73A	3V to 5V	0.075Ω	150°C

3.3 Embedded Power Package

3.3.1 Embedded Power Package Design

An embedded power package using APT60M75DFLL by Advanced Power Technology was designed for liquid cooling testing. The cooling area of the liquid module defines the area allowed for power semiconductor devices to be mounted. It was chosen to use four FREDFETs by APT to improve yield in case any of the semiconductor die are damaged during manufacturing steps. These chips are placed in a diamond formation to make electrical connection simpler and to ensure the chips are close to the center of the cooling region. Each chip can be connected to external circuitry separately through electrical connectors outside the cooling region. This requires that the substrate be wider than the cooling region. Future connection could be half bridge, full bridge, or multiple levels. A solder joint to a DBC substrate is used for the drain connection. DBC provides insulation from non-dielectric fluid and protection against abrasion caused by fluid flow. The DBC also acts as mechanical support for the high pressure flow. Type k thermocouples from Omega Engineering Inc. are attached next to each drain pad to monitor chip temperature [26]. Solder mask is used to insulate the top side gate and source traces. This layer also helps prevent mechanical degradation of electrical traces and the semiconductor chips. Silicone based gel is used between the DBC and substrate carrier to provide mechanical support for the sample frame. The dielectric layer design and trace layout design are shown in Figure B.2 and Figure B.3.

3.3.2 Embedded Power Package Construction

This section describes the steps to construct the MOSFET based embedded power package for double-sided liquid cooling. The basic process is described by Liang [16]. All major steps are discussed while some minor steps, such as equipment use and sample cleaning, are not. An outline of the complete process is given in Appendix C.

After first creating a conceptual design via hand drawings, a finalized design should be created in Autocad. Key information to finalize completely are the substrate laser cutting pattern, dielectric screen print pattern, metallization electrical trace pattern, and DBC electrical trace pattern. These patterns are shown in Figure B.1 through Figure

B.4. The first step after completing the design phase is to laser cut the substrate carrier. 99.6% alumina, Al_2O_3, with the dimensions 101.6 mm x 101.6 mm x 0.635 mm, from Accumet Engineering Corporation was used in this sample [27]. The laser cut pattern in Figure B.1 is then used to cut the substrate. Care was taken by using a low laser power settings and multiple runs to reduce heating and therefore avoid breaking substrates. Figure 3.5 shows an uncut substrate and cut substrate. Extra holes were cut for pressure relief and screw connectors, but weren't used in this version. After cutting, the sample was mechanical cleaned using a diamond file, then wet cleaned using acetone, isopropyl alcohol, and de-ionized water, and allowed to dry completely.

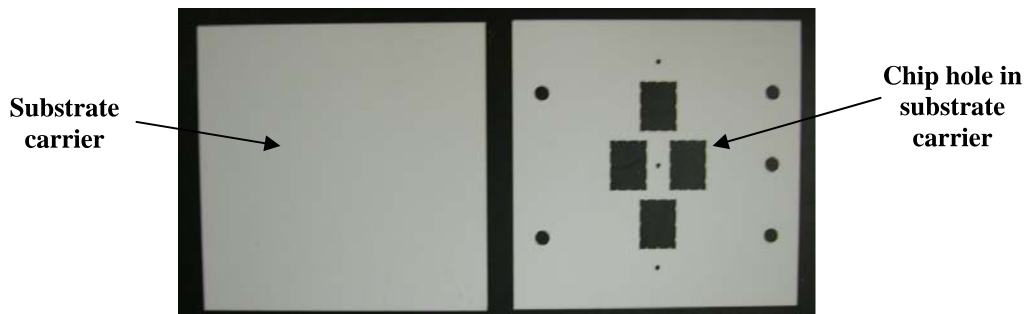


Figure 3.5 Uncut and laser cut alumina substrate for semiconductor die placement

The semiconductor die were placed in the substrate carrier. This steps requires extreme care to not damage the semiconductor via static charge or mechanical abuse. Kapton tape is first placed on the top side of the substrate over the hole where chips and/or epoxy will be placed. The chips are then carefully placed in their respective holes with their gate and source patterns touching the Kapton tape. This is done using a suction cup system. The chip drains and top side are then pressed using the suction cup system to remove air bubbles seen through the Kapton. This is important to prevent epoxy flow onto the top of the chip. Die attach epoxy, EP3AOHT from Master Bond Inc., is then applied around the chip via a syringe [28]. This epoxy can be heated slightly to improve its viscosity for uniform application. Voids are stamped out of the epoxy by using a tweezers or needle point to ensure good adhesion between the chip and substrate and more epoxy is added if needed. The voids can be viewed by holding the sample up to a light and looking though the epoxy. After epoxy application is complete, the epoxy

should be baked and the allowed to cool. Figure 3.6 shows bottom and top views of the chips in the substrate carrier post epoxy bake.

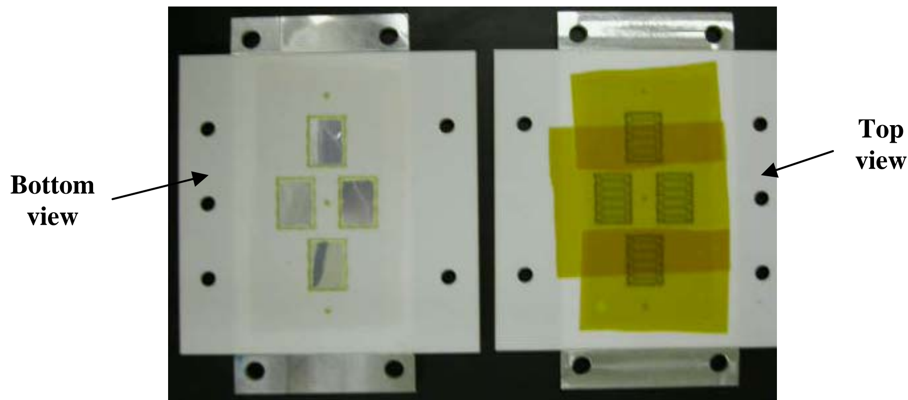


Figure 3.6 Top and bottom views of die attachment to alumina substrate carrier

Top side dielectric application is required to isolate gate and source pads. This dielectric can be applied using screen printing or photolithography methods depending on the isolation requirement between the gate and source, source and drain, and gate and drain. Screen printing was chosen for this case due to previous experience and higher dielectric strength. The screen print material used is EPO-TEK 600 from Epoxy Technology and the dielectric screen print pattern is shown in Figure B.2 [29]. The screens were constructed by Sefar Printing Solutions, Inc. The Kapton tape is removed from the previous step and a wet clean with acetone, isopropyl alcohol, and de-ionized water is then performed to remove residue left by the tape. Screen printing is then performed on the substrate after firmly securing the substrate and checking alignment. EPO-TEK 600 can be heated slightly to improve viscosity for application. The screen printed sample is then baked. Figure 3.7 shows the sample after screen printing and baking.

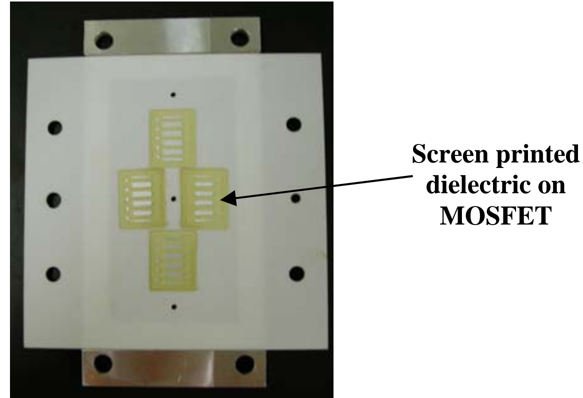


Figure 3.7 Screen printed dielectric layer over top of MOSFET chips

A smooth solid layer is then applied over the screen printed pattern to help with adhesion of thin film metals in future steps. Enthone® DSR-3241 liquid photoimageable solder mask is used for this and will also add to the dielectric strength of the system between MOSFET connection points [30]. The solder mask is mixed and applied by spin coating. The material is then pre-cured and developed using photolithography steps. The solder mask is put through a final bake after developing. The photolithography pattern is identical to the pattern used for screen printing in Figure B.2. A sample after solder mask application and the photolithography transparency used for this step is shown in Figure 3.8.

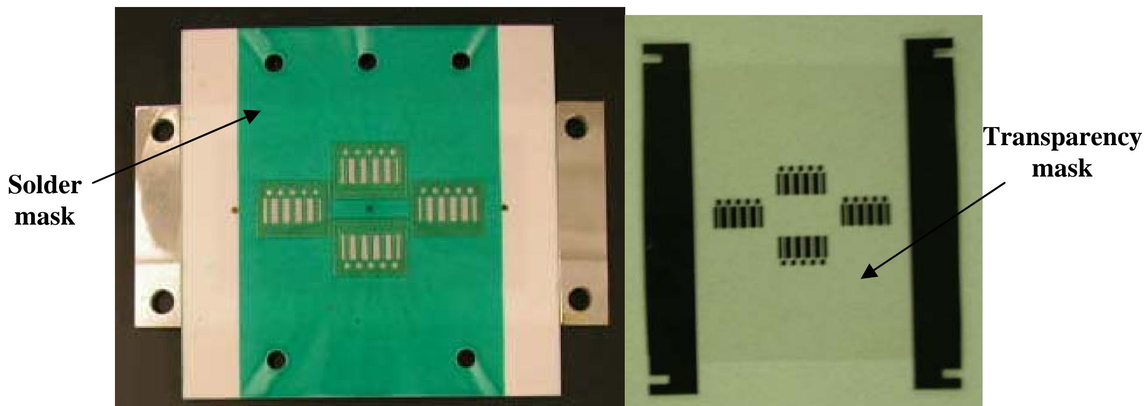


Figure 3.8 Solder mask layer for sputtering and photolithography transparency

Proper application of thin film metal interconnects is critical for the success of an embedded power sample. Physical vapor deposition (PVD) or sputtering is used to apply titanium and copper thin films on the gate and source side of the sample. A complete and

thorough description of PVD and related issues such as sample preparation and plasma cleaning can be found in the Handbook of Physical Vapor Deposition (PVD) Processing [31]. The sample is first put through a wet clean process using acetone, isopropyl alcohol, and de-ionized water and then put through an ex-situ plasma clean process. In-situ plasma cleaning should be implemented in the future to improve deposition quality. The embedded power structure is then put in a PVD chamber where thin film metals are applied. Titanium is used as an adhesion layer for copper, which provides electrical connection. Figure 3.9 shows the sample after titanium and copper were deposited.

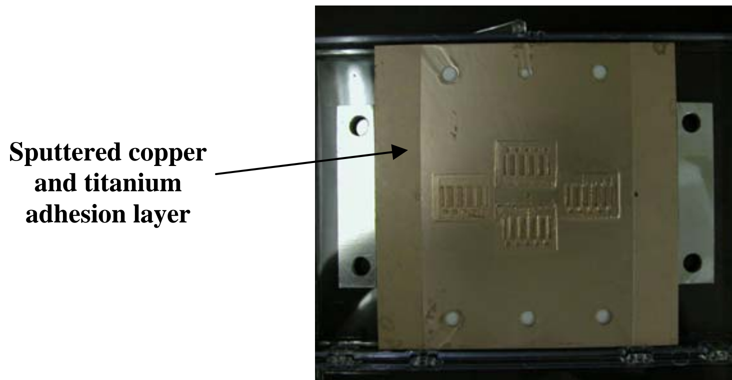


Figure 3.9 Physical vapor deposited (PVD) thin film titanium and copper for electrical interconnects

The next step is to prepare the sample for copper electroplating. A wet clean process using acetone, isopropyl alcohol, and de-ionized water is performed carefully to not remove the previously deposited thin film metals. Photrak EPT240/1694 photoimageable etch resist is then applied where thick film copper is not desired via spin coating. The material is then pre-cured and developed using photolithography steps. The trace pattern is shown in Figure B.3 and the corresponding photolithography transparency is shown in Figure 3.10. A ring around the edge of the sample is left open to attach to the electroplating fixture. Figure 3.10 shows the sample after this process is complete.

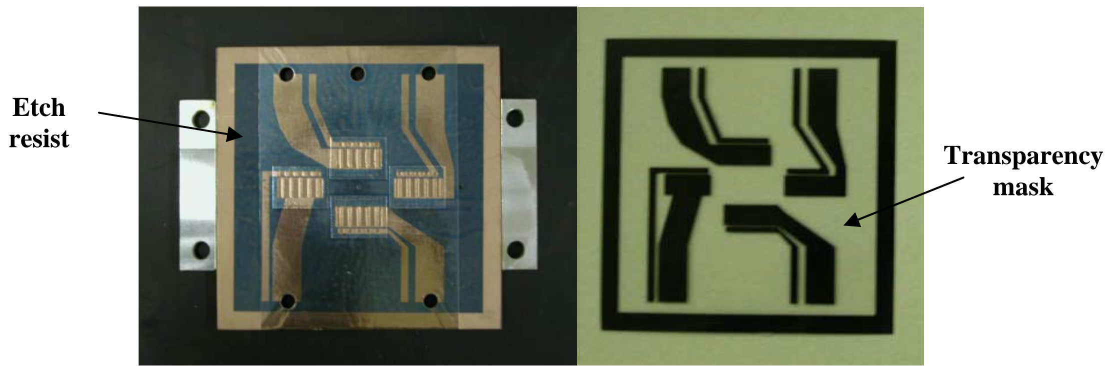


Figure 3.10 Photo mask for copper electroplating and photolithography transparency

Electroplating is challenging step to perfect, but is essential in constructing a working embedded power sample. An electroplate frame used to provide electrical connection to the sample is first created using a board router and plated circuit board. The sample is then attached to the frame using Kapton. The contact point and back side of the substrate should be completely sealed to avoid damaging the chip or thin film metallization. The sample is then electroplated in Techni Copper RR copper solution for roughly three hours at approximately 550 mA to achieve 0.0762 mm of copper [32]. The copper anode can also be taped to provide roughly half of the visible area of the embedded power sample, which will improve the electroplating results. Figure 3.11 shows the electroplate frame, top side of sample in frame, bottom side of sample in frame, and electroplate station. The sample is then removed from the electroplate station and frame. The tape is removed and the sample is rinsed using de-ionized water. The plated embedded power sample can be seen in Figure 3.12. Some of the thin film copper has been etched near the frame contact point. This could be avoided with better sealing.

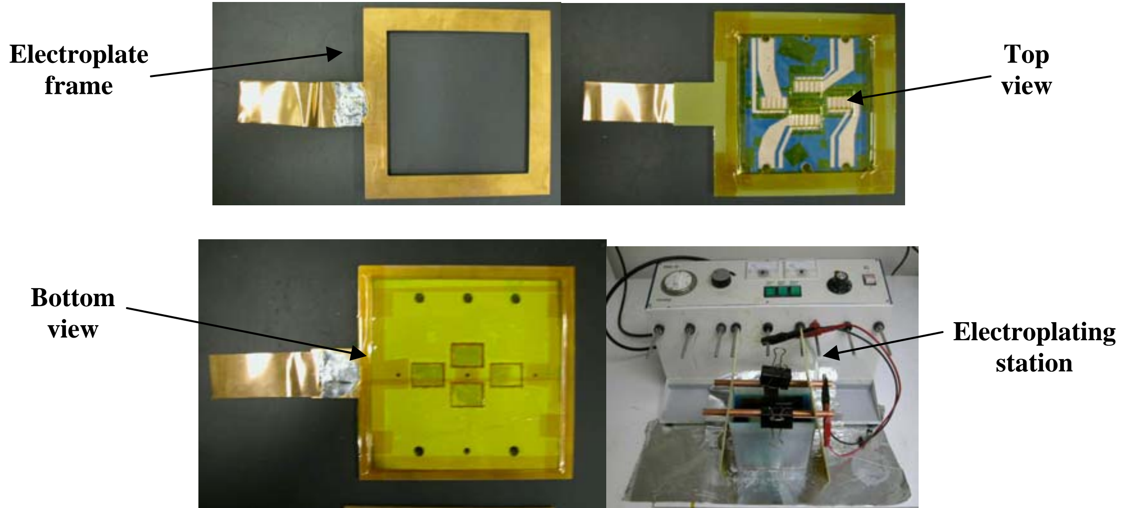


Figure 3.11 Copper electroplate frame, top and bottom views of sample in electroplate frame, and electroplating station

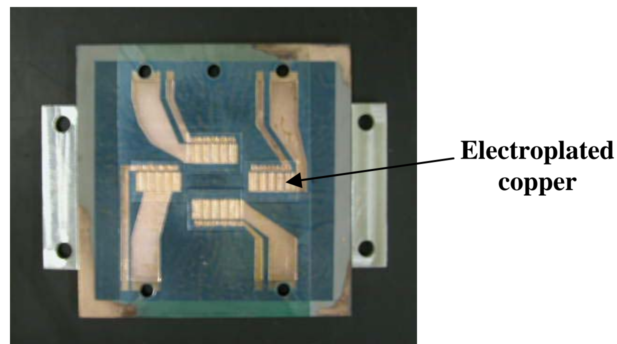


Figure 3.12 Embedded power sample after copper electroplating

After electroplating, the photoimageable etch resist can be removed by soaking the sample in acetone. The unwanted thin film copper can then be removed using copper micro etch, PC200-10 Etchant-SP [33]. This will remove some electroplated copper. Care should be taken to not touch the sample since the MOSFETs will no longer be directly shorted. The sample can then be wet cleaned using acetone, isopropyl alcohol, and de-ionized water. Figure 3.13 shows the sample before PVD copper etch.

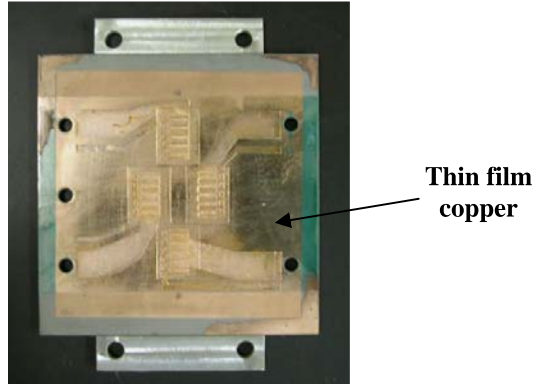


Figure 3.13 Embedded power sample before PVD thin film copper etch

A similar process is used to remove the unwanted thin film titanium. The sample is soaked in titanium etchant for several minutes [34]. Extreme care should be taken to not touch the sample since the MOSFETs will no longer be shorted. Figure 3.14 shows the sample before PVD titanium etch. The sample should be wet cleaned using acetone, isopropyl alcohol, and de-ionized water after all unwanted titanium is removed. The embedded power sample with completed gate and source interconnects is shown in Figure 3.15.

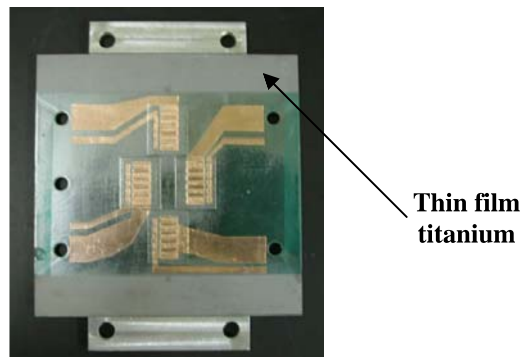


Figure 3.14 Embedded power sample after PVD thin film copper etch

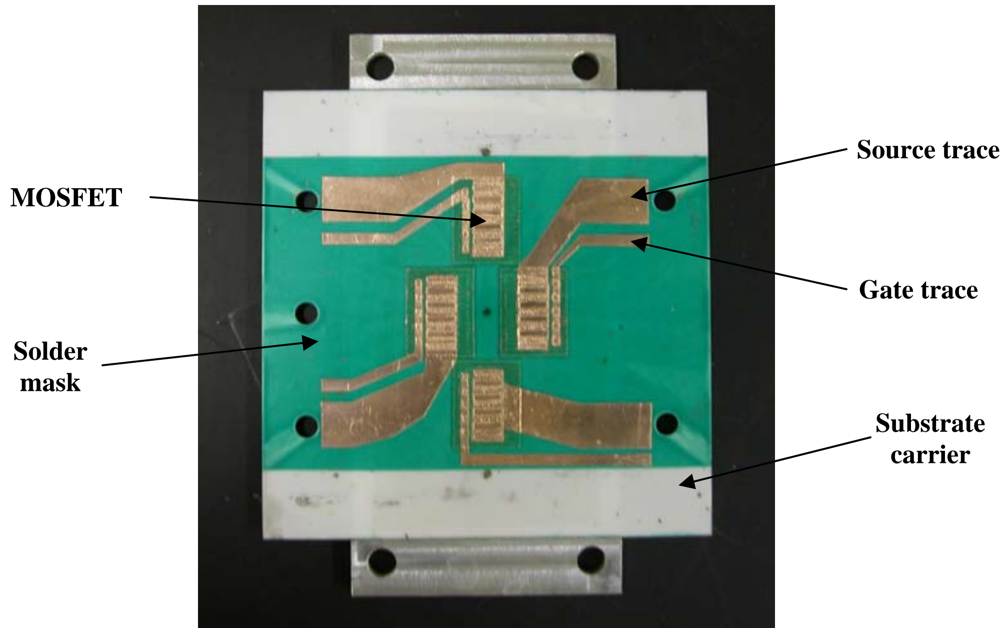


Figure 3.15 Embedded power structure after PVD thin film titanium etch

At this point, the construction of the DBC will be presented. Other steps, such as top side insulation application, can be completed in parallel. Nickel plated, alumina DBC is chosen for the base of the embedded power structure. The DBC substrate is first etched and cut to meet the sample frame dimensions. Some over hang is left to have drain pads outside the embedded power sample. Photoimageable etch resist is then applied to create the drain trace pattern via spin coating and cured as described in previous steps. The DBC drain pattern is shown in Figure B.4. The back side of the DBC is taped with Kapton tape to prevent any etching. A bench top etcher is then used etch the DBC substrate. Figure 3.16 shows the initial nickel plated alumina DBC substrate and photomask pattern on the DBC. Thermocouples were carefully taped next to each drain pad. EP3AOHT from Master Bond was used to secure the measurement point of each thermocouple. The thermocouples and epoxy should have a height less than or equivalent to that of the DBC drain traces. The DBC after etching and after thermocouple attachment is shown in Figure 3.17.

Figure 3.16 DBC and photo masked pattern on DBC

Figure 3.17 Drain pattern on DBC and DBC base with thermocouples

After creating the DBC base, the embedded power substrate carrier with chips can be attached. This is done using solder paste and a reflow belt. Kapton is placed over the DBC substrate and rectangles are cut in the tape for the drain pads. This will help unwanted solder flow and connection of drains. $Sn_{43}Pb_{43}Bi_{14}$ solder paste from EFD is then generously applied to the drain pads on the DBC and on the drain of each chip [35]. A thin copper shim with an area equal to that of the die and a thickness of 0.254 mm is then placed on the paste on each chip drain. The shim can be pushed slightly to remove voids in the paste. Additional solder paste is the applied on the visible part of the shim. Figure 3.18 shows the embedded power at various solder paste application stages. The sample should then be reflowed following the temperature patterns described by EFD's Reflow Profiling Guide [36]. Pressure can be applied on the top side of the device to

ensure proper alignment during reflow. A small solder dot should be place in a visible area on the top of sample to monitor the solder paste state to ensure proper contact between the DBC and chips. A sample after the drain solder paste connection steps is shown in Figure 3.19.

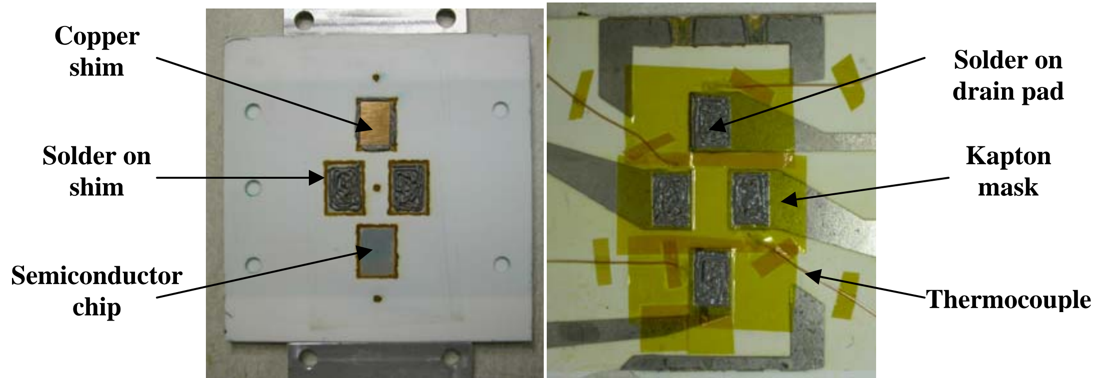


Figure 3.18 Bottom side of chips showing MOSFET drain, solder paste, and copper shim; Solder paste on DBC drain pads

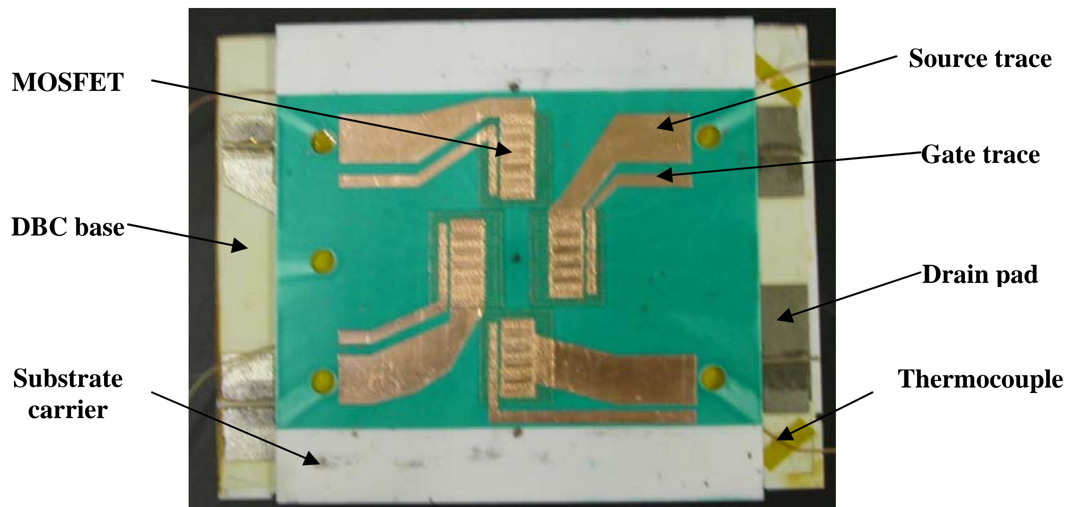


Figure 3.19 DBC based embedded power package with thermocouples

Electrical connectors can be attached next with a lower melting point solder paste. Brass nuts for the drain and source and copper strips for the gate were used for this sample. The sample is placed on a hot plate and heated to slightly below the melting point of the solder paste in use. The paste and connecters are then a placed on the sample. A solder iron is used to locally heat the connector and solder. Care should be taken to not over heat any portion of the sample using the solder iron. A sample with connectors

attached and the hot plate used to attach them are shown in Figure 3.20. At this point, each MOSFET can be tested.

Figure 3.20 Attachment of electrical connectors via solder paste and hot plate

Top side insulation can be applied before attaching the DBC substrate or after. If done before attaching the DBC, the sample is considerably smaller and easier to handle making spin coating possible. In this case, Enthone® DSR-3241 liquid photoimageable solder mask was applied after DBC and electrical connecter attachment. The solder mask was brushed on generously, but smoothly. It was then directly baked for final curing. Figure 3.21 shows the sample with solder mask applied.

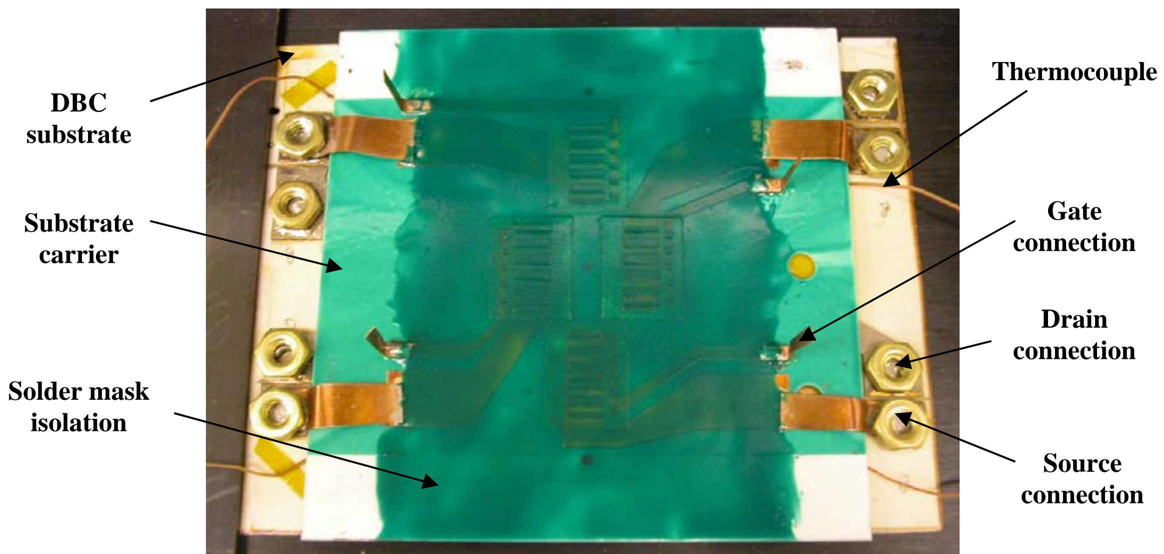


Figure 3.21 Solder mask insulation for top side of embedded power sample

General Electric RTV dielectric silicone gel, RTV6166, is added between the DBC and substrate to add mechanical support for the application of the substrate frame

[37]. Tape is applied around the edges leaving some holes to pour gel. The silicone gel is then mixed and poured into the sample while holding it vertical. The sample is carefully placed flat in a container after allowing the material to cure slightly. The sample is left to cure for 24 hours.

The final step is to apply the sample frames, so the sample can be attached to the liquid module for testing. Mega Black O.E.M. high temperature silicone gasket maker is applied to each frame generously and allowed to pre-cure for three to five minutes [38]. The bottom and top frame are then attached to the sample. The frames can be marked to aid in alignment. The frames should be pressed slightly to spread the silicone adhesive, so a small bead can be seen on the inside of the frame. The entire sample should then be placed in the liquid module with o-rings in the double-side configuration. The test bed should then be tightened to final testing configuration where no gaps can be seen between the sample frame and liquid module. The silicone should then be allowed to cure for 48 hours. Figure 3.22 shows the embedded power structure with sample frames.

The total sample height is critical, but hard to control. The first attempt to create a double-side cooled embedded power sample failed during initial test after tightening the liquid module screws to ensure no leaks around the o-ring. This pressure caused the substrate carrier to crack slightly as seen in Figure 3.23. Future designs should include better mechanical support for the substrate carrier and DBC where the sample frames apply pressure. Silicone gel is too soft after curing, so future version should use epoxy and/or an alumina shim as support. Cracks were sealed by applying a thin layer of clear epoxy.

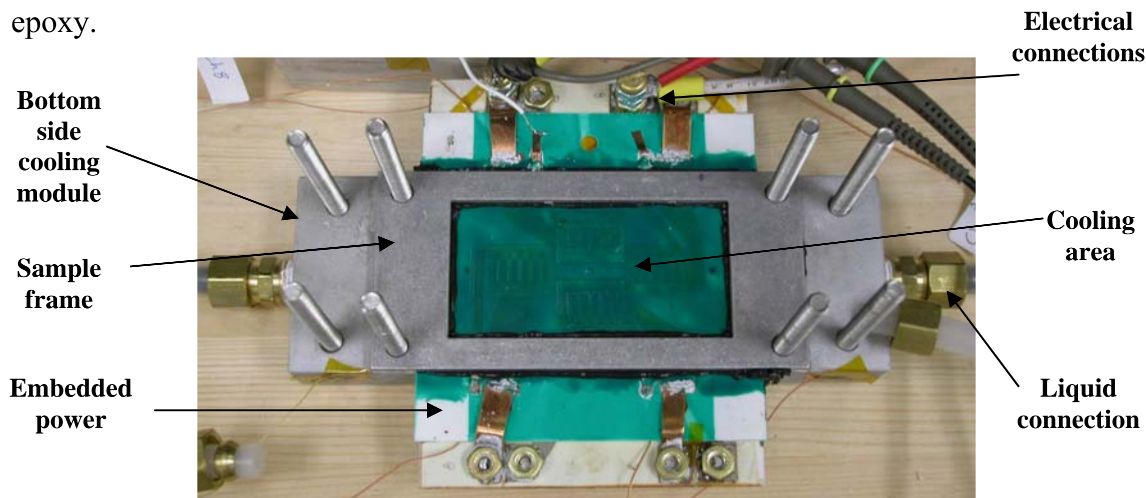


Figure 3.22 Completed embedded power sample attached to sample frames via silicone adhesive

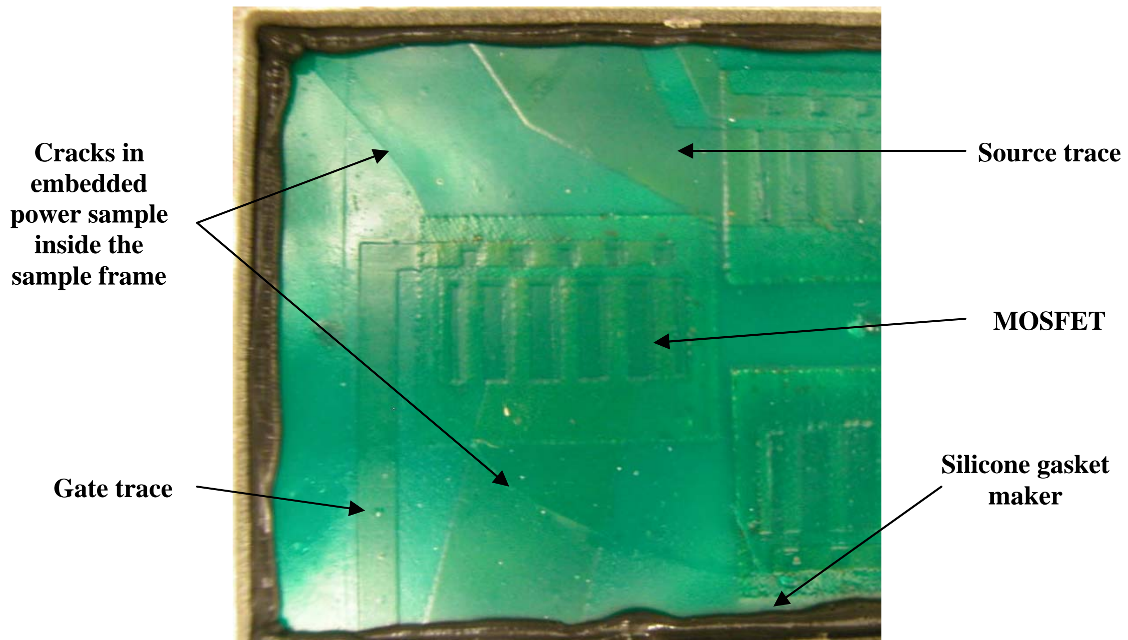


Figure 3.23 Cracked embedded power sample from a lack of support under the sample frames

The final configuration of the liquid module with the MOSFET based embedded power sample for double-sided cooling test is shown in Figure 3.24. This section has presented the embedded power package design and explained the key construction steps required to make the test sample.

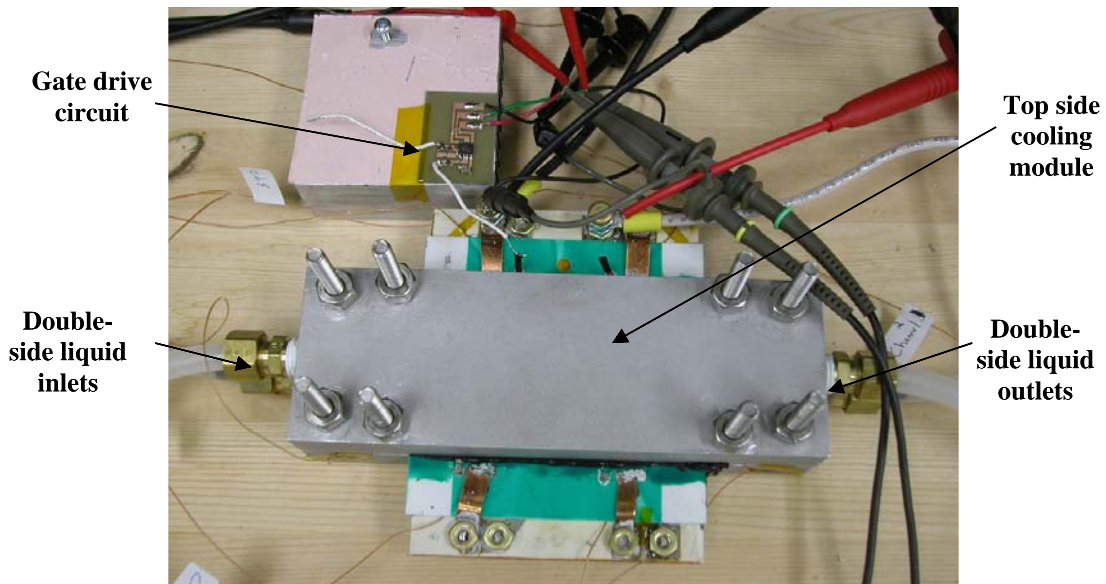


Figure 3.24 Embedded power sample connected to liquid module for double-sided cooling test

3.4 Wire Bond Package

3.4.1 Wire Bond Package Design

A wire bond based package was designed and constructed to compare to the embedded power package with liquid cooling. This package uses a single APT60M75DFLL FREDFET. Wire bond manufacturing experience is greater, so multiple chips were not placed on the same substrate. The chip is placed on a nickel plated, alumina DBC similar to the base for the embedded power sample. Electrical connection was kept simple and the trace design is shown in Figure D.1. Brass nuts are used to connect the gate, drain, and source. A type k thermocouple is attached with Kapton tape and epoxy directly to the top side of the device for device temperature monitoring.

3.4.2 Wire Bond Package Construction

This section describes the steps to construct the MOSFET based wire bond package for single-sided liquid cooling, which is considerably less complicated in design and less difficult to manufacturer. Many of the process steps are similar to procedures performed to construct the embedded power sample. All major steps are discussed while some minor steps, such as equipment use and sample cleaning, are not. An outline of the complete process is given in Appendix E.

After creating a conceptual design via hand drawings, a finalized wire bond package design should be created in Autocad. This entails creating a DBC trace pattern. This pattern is shown in Figure D.1. The first step after finalizing the design is to cut and etch the DBC base. This is similar to what was done for the embedded power base shown in Figure 3.16. The next step is to solder the drain side of the chip to the drain pad on the DBC substrate. The substrate is taped with Kapton and a rectangle cut out for the drain pad. $Sn_{43}Pb_{43}Bi_{14}$ solder paste is then applied to the drain pad and the chip is placed with a suction cup holder. At this point, electrical connectors are also applied with the same solder paste. The sample is then reflowed as described by EFD's Reflow Profiling Guide [36]. Wire bonds are applied using a manual ultrasonic wire bonding machine. All gate and source pads must be bonded to fully utilize the device.

A type k thermocouple from Omega Engineering Inc. was attached to the top side of the chip. A small piece of Kapton tape was place on the chip to electrically isolate the thermocouple and epoxy was place on the top of the measurement point to insulate it from the environment. The device can now be tested to check operation. General Electric RTV dielectric silicone gel, RTV6166, could be applied over the top of the device as a better insulator, but this was omitted for this version to reduce processing time. The package is then attached to a sample frame as described for the embedded power except only a single frame and liquid module is required. Figure 3.25 shows the completed wire bond sample and Figure 3.26 shows the sample attached to the liquid module for single-sided cooling test. This section has presented the wire bond package design and explained the key construction steps required to make the test sample.

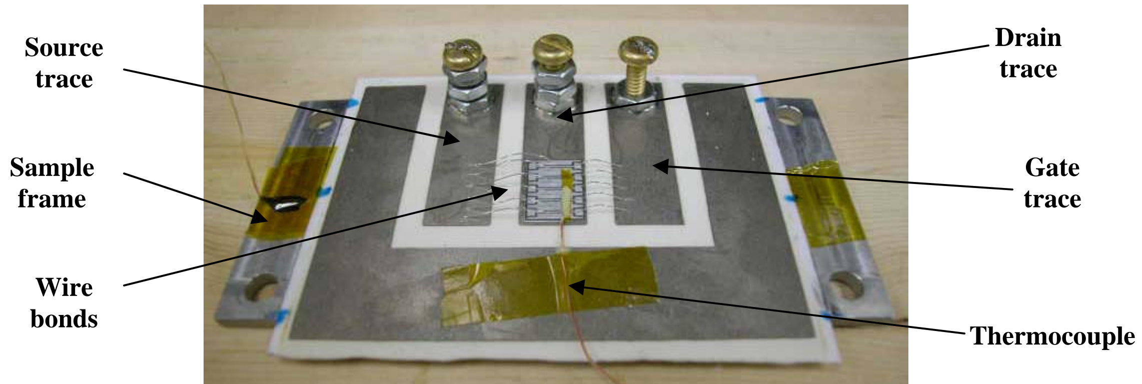


Figure 3.25 MOSFET based wire bond package with thermocouples attached to sample frame via silicone adhesive

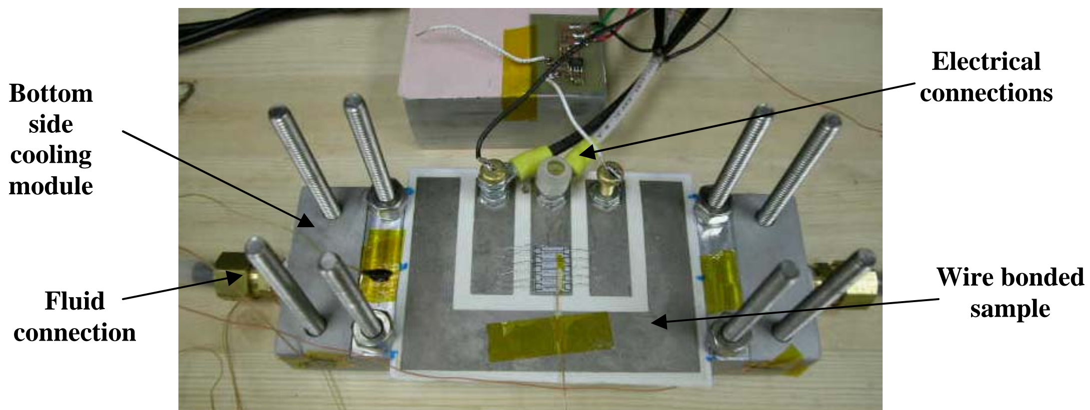


Figure 3.26 Wire bond package connected to liquid module for single-sided testing

3.5 Experimental Setup

This section provides the details of the experimental setup and testing procedures. The experimental setup has two key parts, electrical system and fluid system. The electrical system contains the MOSFET power loss circuit as well as all monitoring and recording equipment. The fluid system includes the fluid process/control and fluid monitoring equipment. A schematic for the complete testing system is shown in Figure 3.27 and picture of the test bench is shown in Figure 3.28.

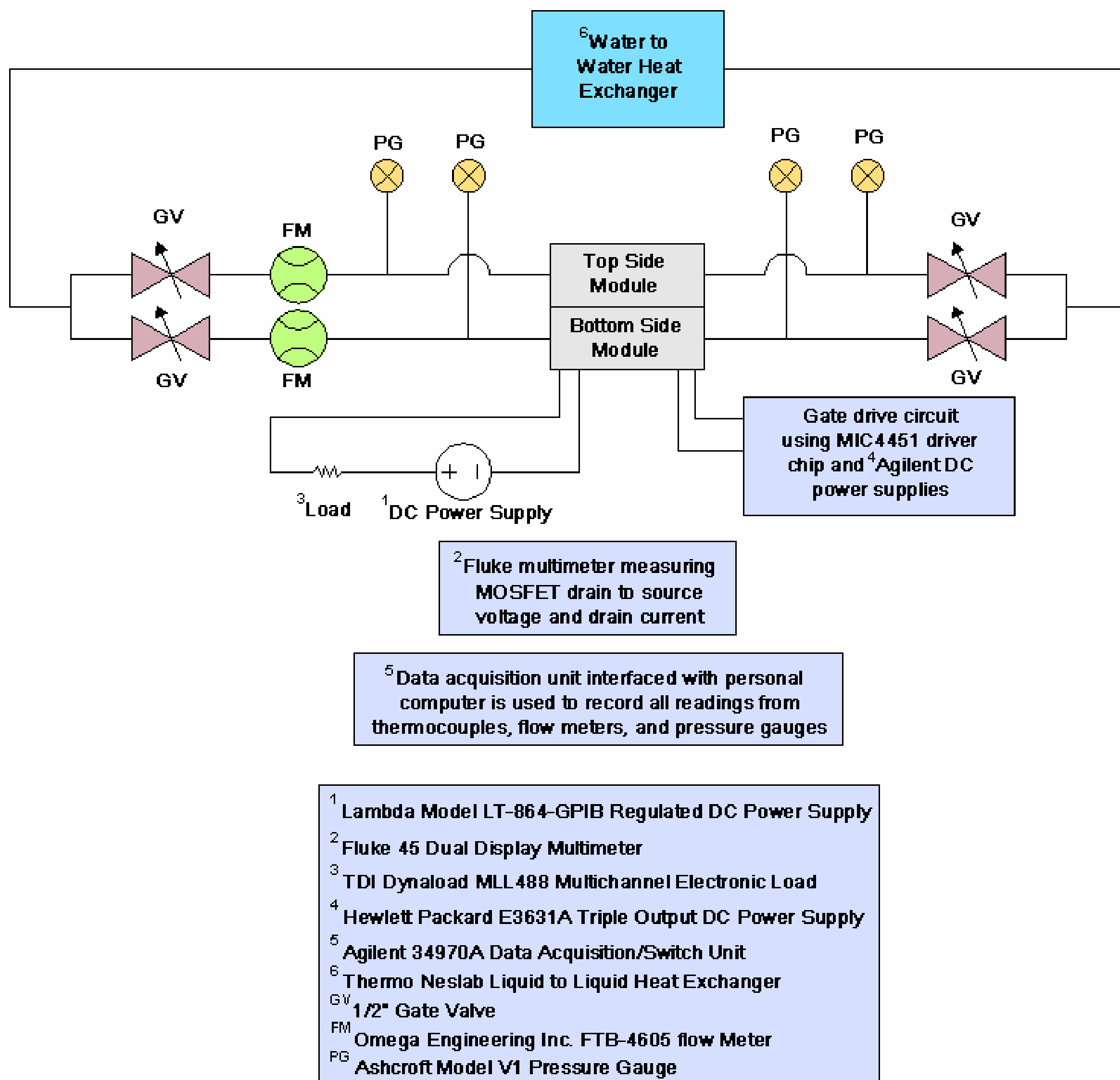


Figure 3.27 Test configuration schematic

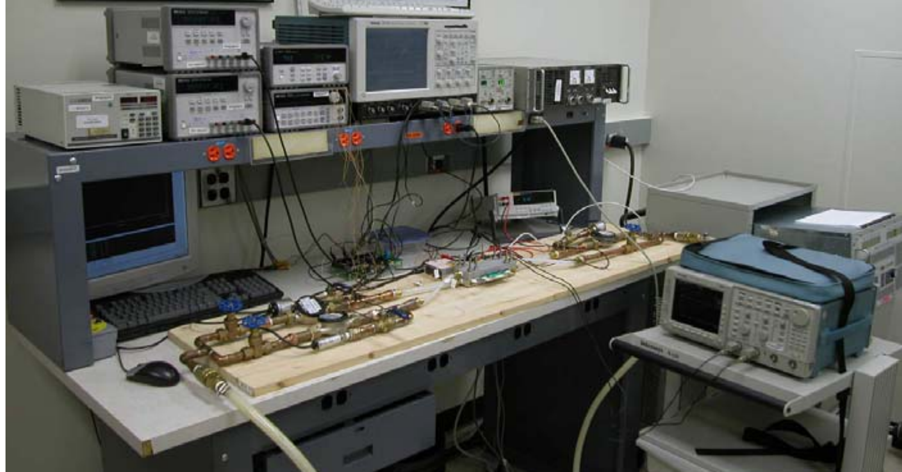


Figure 3.28 Picture of test bench

The electrical test system fairly simple in design, but has many components. The actual MOSFET power loss circuit is made up of a Lambda Model LT-864-GPIB Regulated DC power supply as a power source, TDI Dynaload MLL488 Multichannel Electronic Load for current regulation, and the MOSFET under test as the load or heat source in the cooling region. These components are in series as shown in Figure 3.27. The MOSFET is controlled and driven with a simple MIC4451 drive chip. The drive circuit is given in the MIC4451 datasheet and is shown in Figure 3.29 [39]. A Hewlett Packard E3631A Triple Output DC power supply is used to power and switch the gate drive circuit on or off, which turns the MOSFET on or off. With this electrical circuit, steady state and transient test can be performed. V_{GS}, V_{DS}, and I_D are monitored with a Fluke 45 Dual Display Multimeter. Measured values for V_{DS} and I_D are used to calculate the power loss of the MOSFET. A V_{GS} value can be chosen from the forward characteristics and the power loss can be estimated from V_{DS} and I_D values before performing a test. All thermocouples are attached to an Agilent 34970A Data Acquisition/Switch Unit and are monitored and recorded through Desktop Bench Logger on a personal computer.

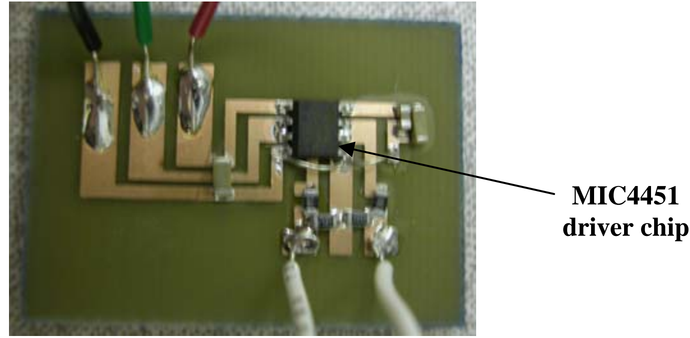


Figure 3.29 Picture of MIC4452 MOSFET driver circuit

The fluid system is also fairly simple in design. Plastic tubes are used to connect liquid module to fluid measurement and control equipment. This connection and the surrounding fluid apparatus are shown in Figure 3.30. Gate valves are used to control the fluid flow rate and isolate modules if necessary. Omega Engineering Inc. 4600 series flow meters are used to measure the flow rate into the input side of the module and Ashcroft V1 pressure gauges are present to monitor the pressure drop across the module. These meters interface with an oscilloscope where the flow rate and pressure can be calculated from pulse frequency and DC voltage magnitude, respectively [40-41]. A Thermo Neslab de-ionized water to facility water heat exchanger is used to pump the fluid and control fluid temperature. Thermocouples are attached to the inlet and outlet pipes as well as the module to monitor temperatures other than the device temperature. The inlet pipe temperature also serves as a comparative point of the temperature displayed by the liquid-to-liquid heat exchanger.

Figure 3.30 Fluid measurement and control system

Steady state thermal test were performed by turning the fluid system on to a desired flow rate. The device electrical circuit is then turned on with the gate drive signal turned on last. The power loss is then slowly increased to a desired value. The steady state temperature is then recorded. Flow rate and loss values are increased in increments to analyze the potential of each packaging technology and cooling configuration.

3.6 Liquid Module and Sample Design Test

Before performing actual thermal test, the liquid module had to be tested to confirm its operation under high flow rates and pressure drop. The o-ring design is tested first by place a clear piece of lexan plastic in the liquid module over the o-ring in place of the sample frame as shown in Figure 3.31. Fluid test were then performed from 0 to 6 gal/min and confirmed that no leaks were present around the o-ring.

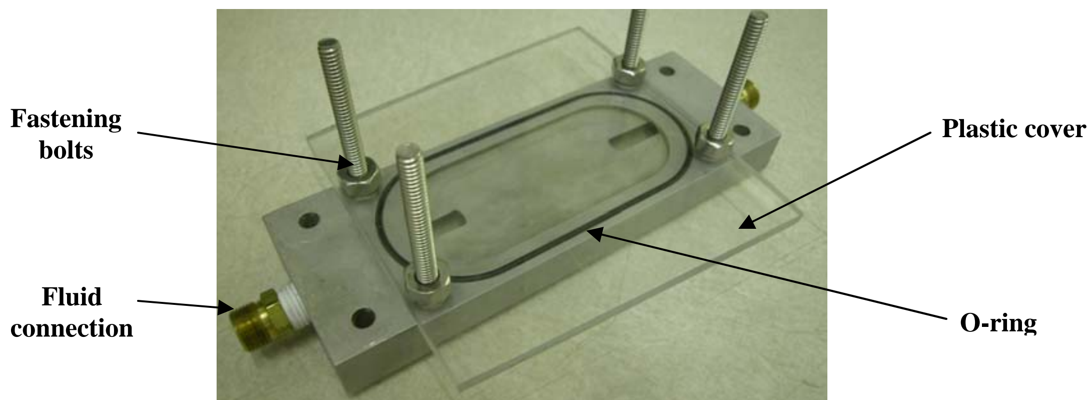


Figure 3.31 O-ring test configuration via clear lexan plastic

The glue seal between the package and sample frame was tested also. This was done by gluing a clear piece of lexan plastic on the frame rather than a specific semiconductor package. This test configuration is shown in Figure 3.32 and flow test was performed in a similar manner as was described for the o-ring test. The first material used, Master Bond EP3AOHT, failed under high flow rates. From closer inspection of the sample, which is shown in Figure 3.33, it can be determined that this epoxy did not adhere well to the polished sample frame. Mega Black O.E.M. high temperature silicone gasket maker was then tried and passed flow and pressure test. This test sample is shown in Figure 3.34.

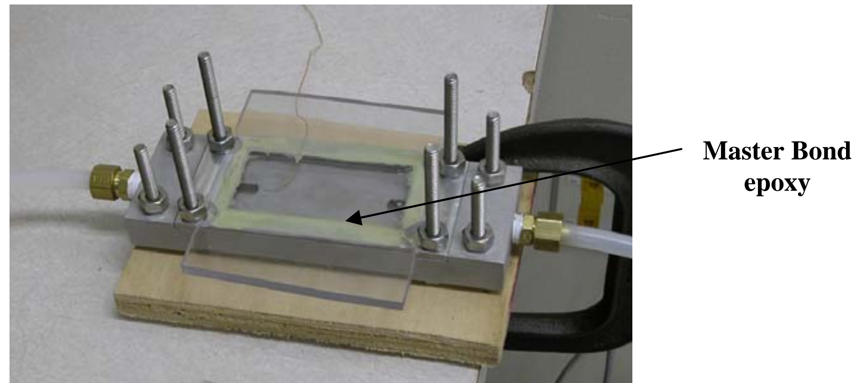


Figure 3.32 Sample frame adhesive test configuration using Master Bond EP3AOHT

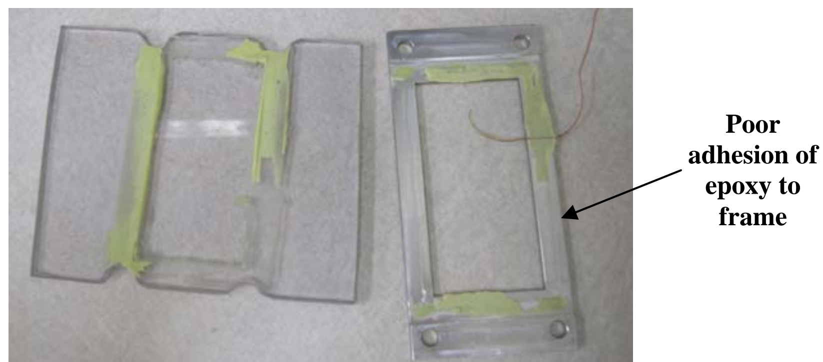


Figure 3.33 Failed frame adhesion with Master Bond EP3AOHT after initial pressure test

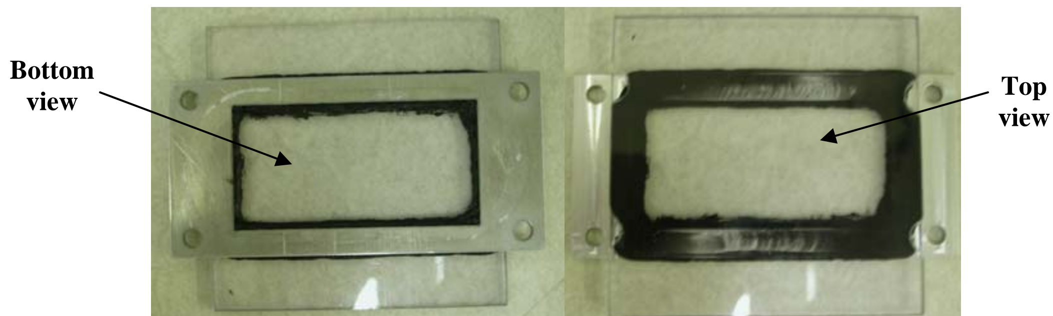


Figure 3.34 Mega Black O.E.M. high temperature silicone gasket maker test sample

Before proceeding with thermal test, a single module was characterized by recording the inlet pressure, outlet pressure, and pressure drop versus flow rate as shown in Figure 3.35. For the double-side case, the total pressure drop would be half the pressure drop for a single module. The module has very high pressure drop at high flow rates, which implies a large amount of force on the sample. This could be a future

limitation of this cooling system, especially for single-side cooling situations. Force should be equivalent and offsetting for the double-side cooling case with equal pressure drop on each side of the package. Pressure relief holes could be added in the sample to compensate for uneven pressure between the sides of a sample.

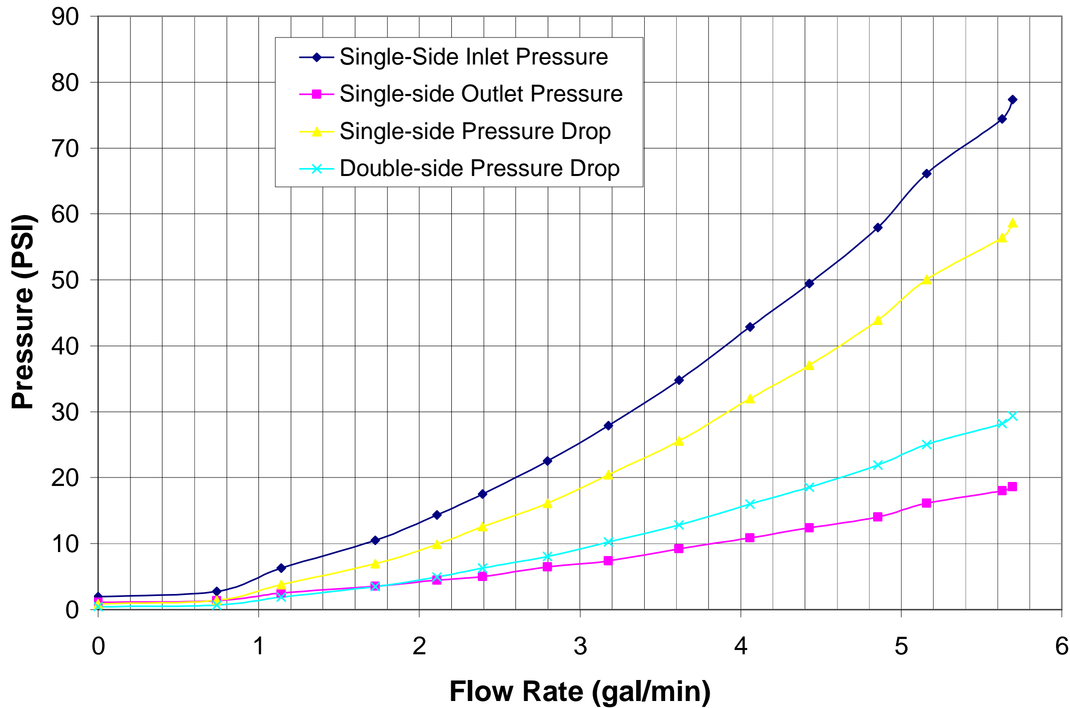


Figure 3.35 Pressure drop analysis for the liquid module test bed: pressure versus fluid flow rate

3.7 Experimental Results

In this section steady state thermal results from experiments are presented and compared for embedded power with double-sided liquid cooling and a wire bond package with single-sided liquid cooling. Experimental results are also compared to thermal modeling results found previously. The results of a parametric study are shown to address any error between the model predictions and experimental results. The de-ionized water temperature at the inlet was set to 25°C and monitored during all test.

3.7.1 Experimental Results and Analysis

Steady state thermal results show the potential of each package with forced liquid convection. Junction to case thermal resistance or total thermal resistance from the

device to the moving coolant is used to analyze the overall performance of each package. This thermal resistance is calculated by dividing the device temperature rise by the power loss. The temperature rise is found by subtracting the fluid temperature from the device temperature. Figure 3.36 shows total thermal resistance versus module flow rate for the wire bond package and single-sided cooling. Multiple curves are given for various device losses between 10 and 100 W, which shows that power loss and temperature rise are linearly related. It can also be seen that flow rate has a large effect on thermal resistance, which suggest the degree of turbulence changes greatly with flow rate. Maximum flow rate was limited to approximately 5.5 gal/min due to the pumping power available from the heat exchanger system. Figure 3.37 shows a similar plot for the embedded power package for device loss values between 5 and 300 W. The flow rate was limited to roughly 4.5 gal/min by minor leaks noticed between the DBC substrate and substrate carrier. These leaks imply that the epoxy used to fill cracks in the substrate carrier, shown in Figure 3.23, failed at higher flow rates. This plot shows the effect of the parallel cooling paths above and below the MOSFET chip in embedded power.

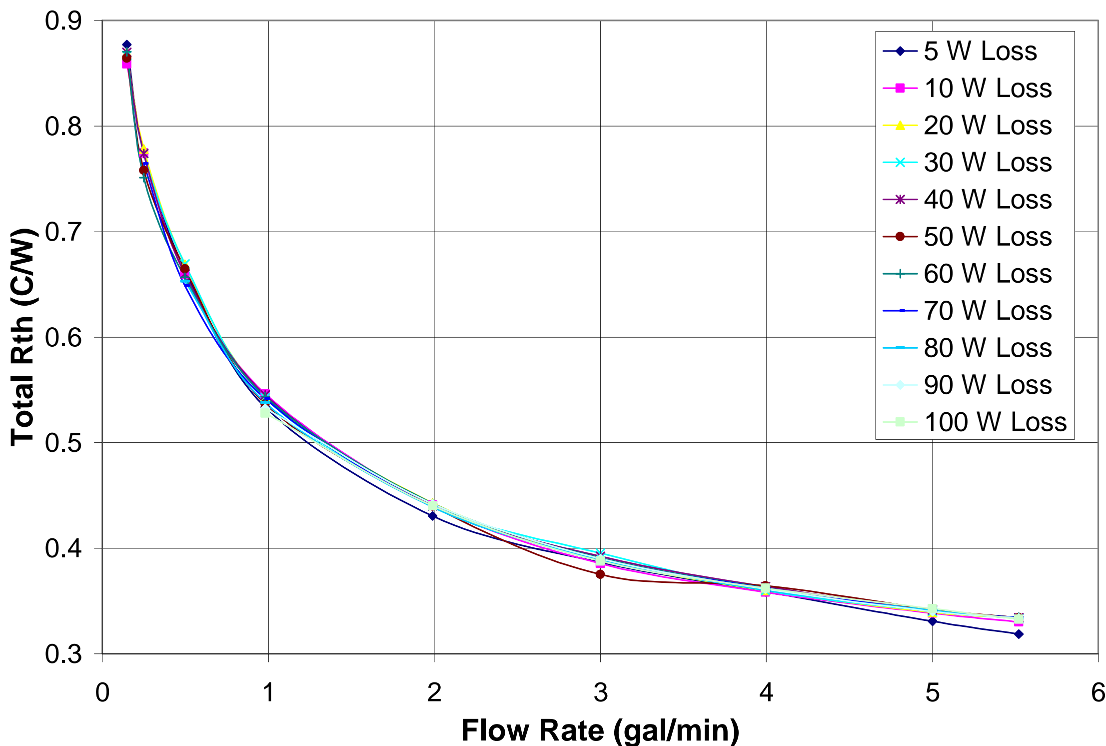


Figure 3.36 Junction to case (total) thermal resistance versus flow rate for the wire bond package with single-side forced liquid convection and various device power loss

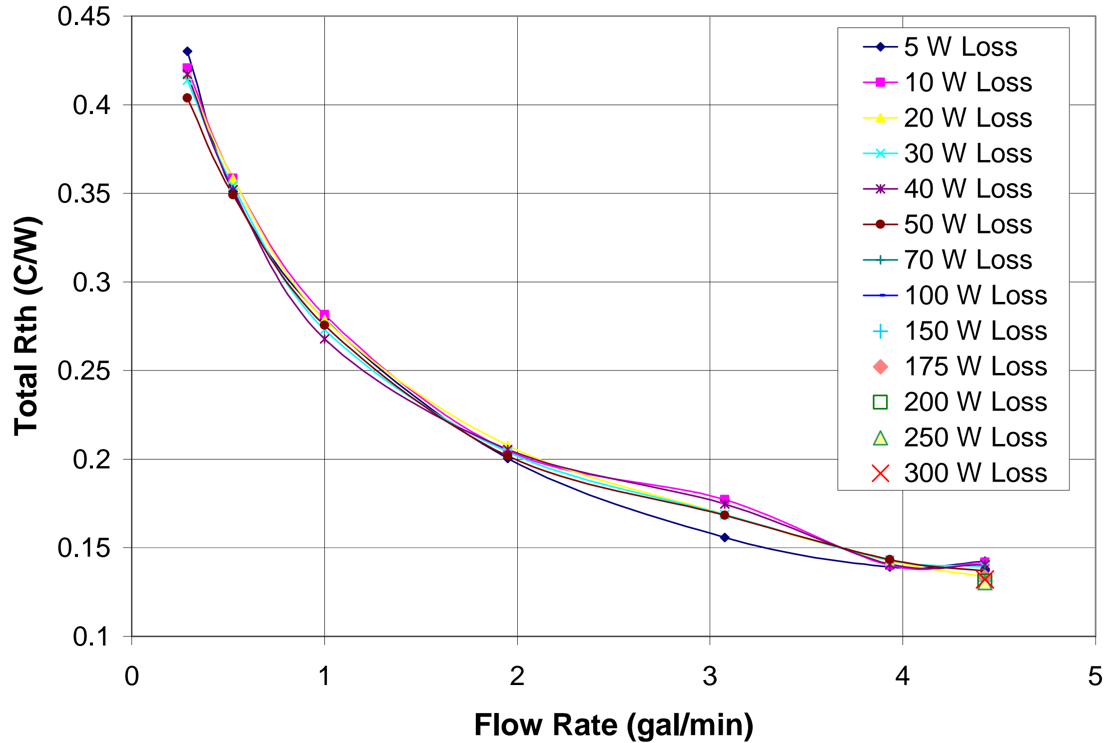


Figure 3.37 Junction to case (total) thermal resistance versus flow rate for the embedded power package with double-side forced liquid convection and various device power loss

The wire bond package with single-sided liquid cooling is compared to embedded power with double-sided liquid cooling configurations in Figure 3.38. The total thermal resistances shown in this plot are the average of their respective curves in Figure 3.36 and Figure 3.37. The percentage improvement in thermal resistance and percentage difference between the single-side and double-side test flow rate are summarized in Figure 3.39. The double-side cooling with embedded power gives approximately 45% to 60% improvement over single-side cooling with a wire bond package. The improvement provided by double-sided cooling, which is made possible with the use of embedded power packaging, is clearly shown. Differences in measured flow rate for the single-side and double-side cases are most prevalent at lower flow rates, which could relate to the precision of control allowed by the gate valves or the measuring limit of the flow meters.

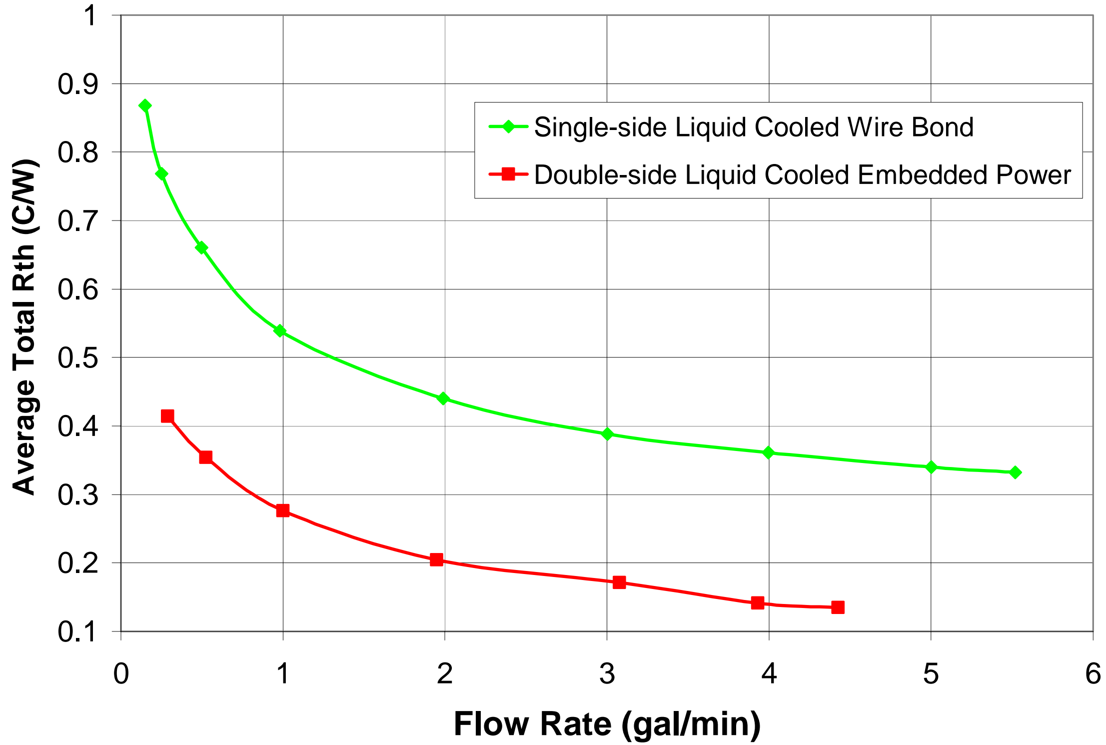


Figure 3.38 Comparison of total thermal resistance for embedded power with double-sided liquid cooling and a wire bond package with single-sided liquid cooling (R_{thavg} from average of R_{th} from different loss)

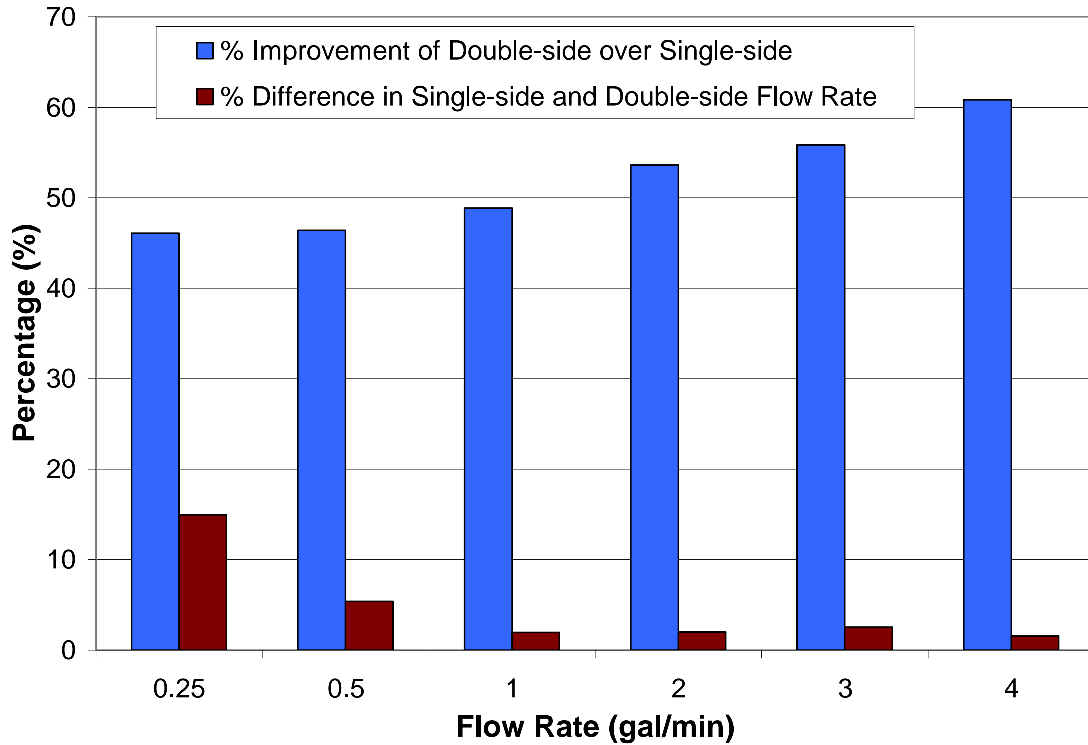


Figure 3.39 Percentage improvement in thermal resistance from double-side cooled embedded power over single-side cooling and percentage difference of measured flow rates

3.7.2 Comparison of Thermal Modeling Predictions to Experimental Results

This section presents a comparison of the thermal modeling predictions created previously to the experimental results. Figure 3.40 compares the experimental and model based total package thermal resistance for each case studied. The model provided an initial understanding of the trends related to double-sided forced liquid convection cooling interfaced with embedded power, but the error is significant between the actual modeling and experimental results.

Many factors could cause error between the model and experimental results including the assumptions of one dimensional heat transfer, neglecting interfacial thermal resistance, constant properties, and fully develop turbulent flow. Measurement error for power loss, temperature values, and geometry could also add to error. Using an average velocity in the convection correlation could be major factor that reduces the prediction ability of the physics based electro-thermal modeling technique for forced convection. Not to mention, the fluid velocity used in the convection correlation is calculated based on a known round inlet tube velocity and using conservation laws to estimate the velocity in the rectangular cooling region.

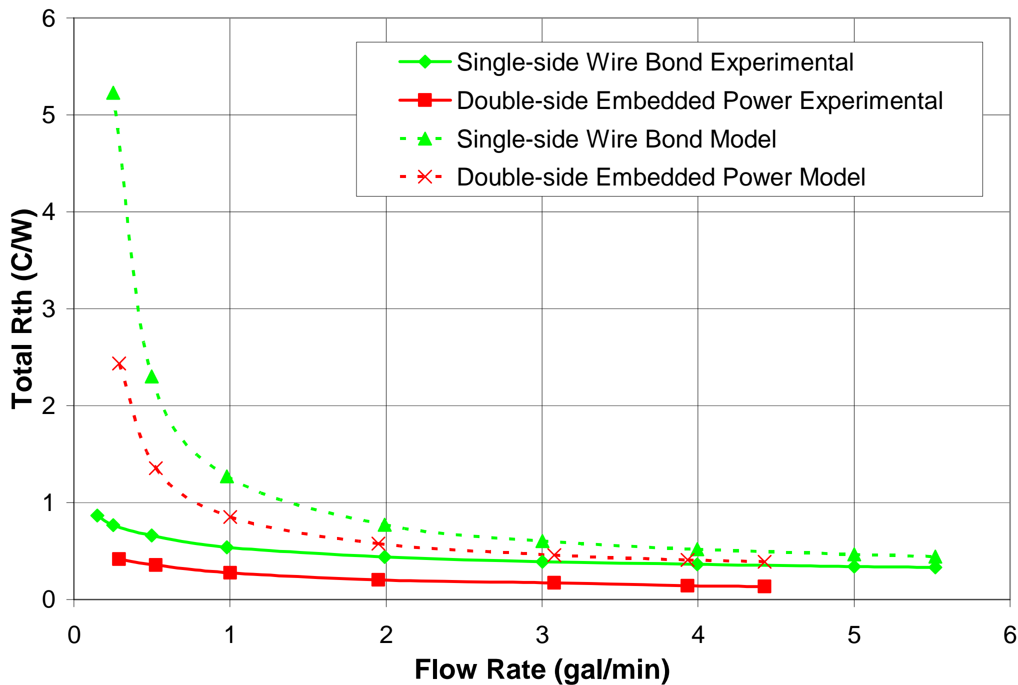


Figure 3.40 Junction to case (total) thermal resistance comparison of electro-thermal models to average experimental results

A parametric analysis of the one dimensional, physics based electro-thermal models can provide some understanding of the possible sources for error. Figure 3.41 shows the parallel relationship between the top and bottom side heat paths. This relationship is evident in Figure 2.12, where the total top side thermal resistance is much greater than the bottom side heat path. The top side resistance limits the double side thermal resistance for this package design. A more detailed look at the components of the top and bottom side thermal resistances is required to determine possible sources for modeling error.

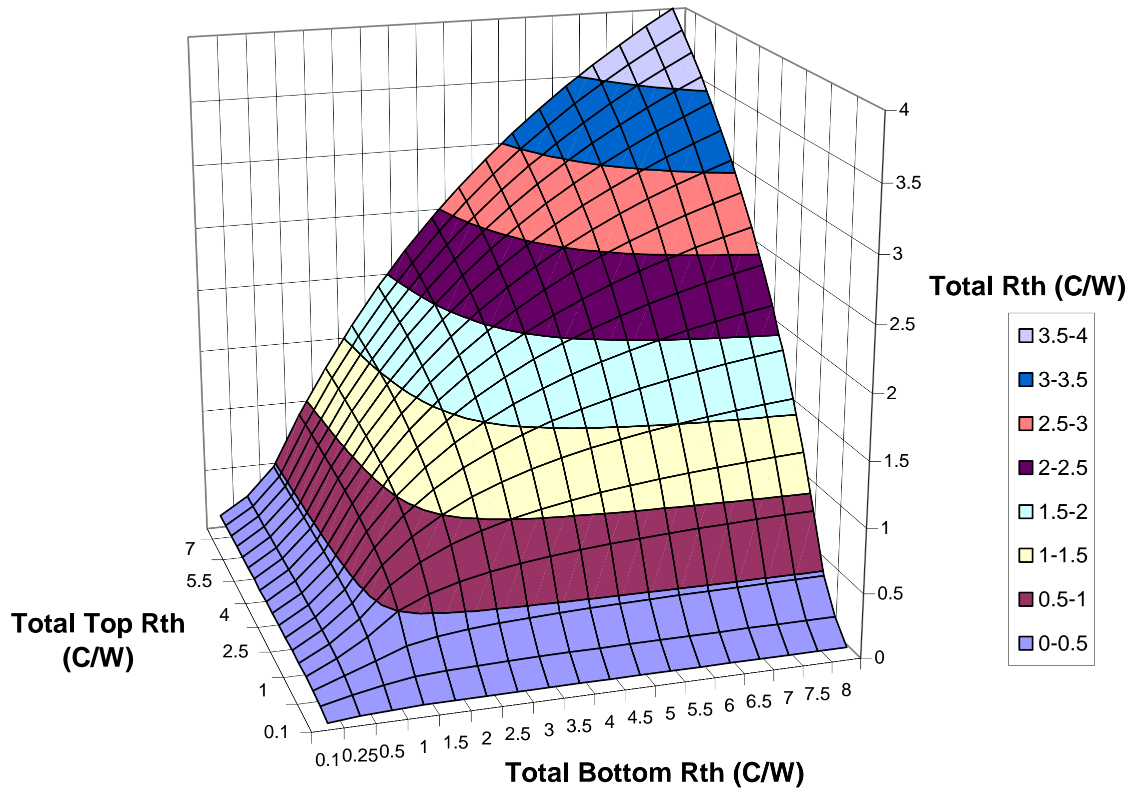


Figure 3.41 Total package thermal resistance vs. total top thermal resistance vs. total bottom thermal resistance

The sensitivity of the total double-side package resistance to top and bottom side conduction thermal resistance is shown in Figure 3.42 and Figure 3.43, respectively. From these plots, it is apparent that a variance in top side conduction resistance has a slightly greater effect on the total package thermal resistance over the entire flow rate range. Comparisons of the specific conduction thermal resistance components for top and bottom side conduction are given in Figure 3.44 and Figure 3.45. The largest thermal

resistance components, solder mask insulation and screen printed dielectric, are parts of the top side conduction resistance. These components could lead to large error if they are not correctly modeled. Figure 3.46 and Figure 3.47 show the sensitivity of the solder mask insulation and screen printed dielectric to changes in cooling area and material thickness. The solder mask insulation is highly dependent on the thickness and cooling area, while the screen printed dielectric is far more sensitive to material thickness. Modeling error related to cooling area is possible since heat transfer is a three dimensional phenomena. Thermal energy could easily spread as it propagates from the semiconductor chip to the flowing fluid. Error due to material thickness could also be present since there are limits to controlling some layers thicknesses during sample construction and measuring internal layers.

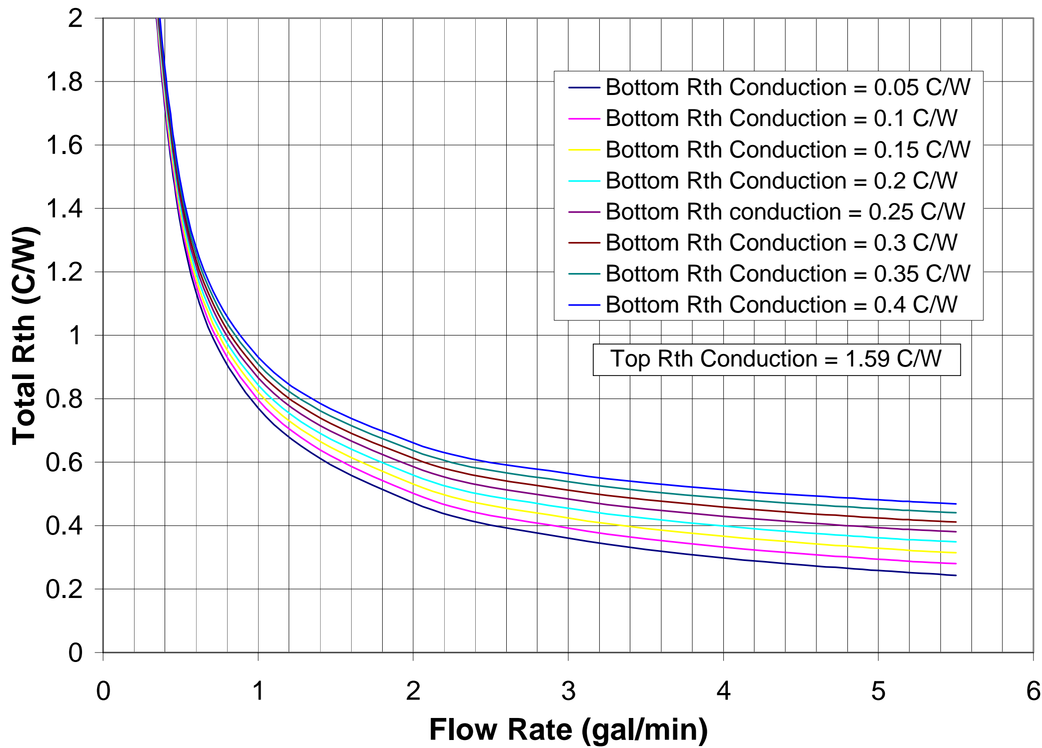


Figure 3.42 Total package thermal resistance vs. flow rate for various bottom side conduction thermal resistance values

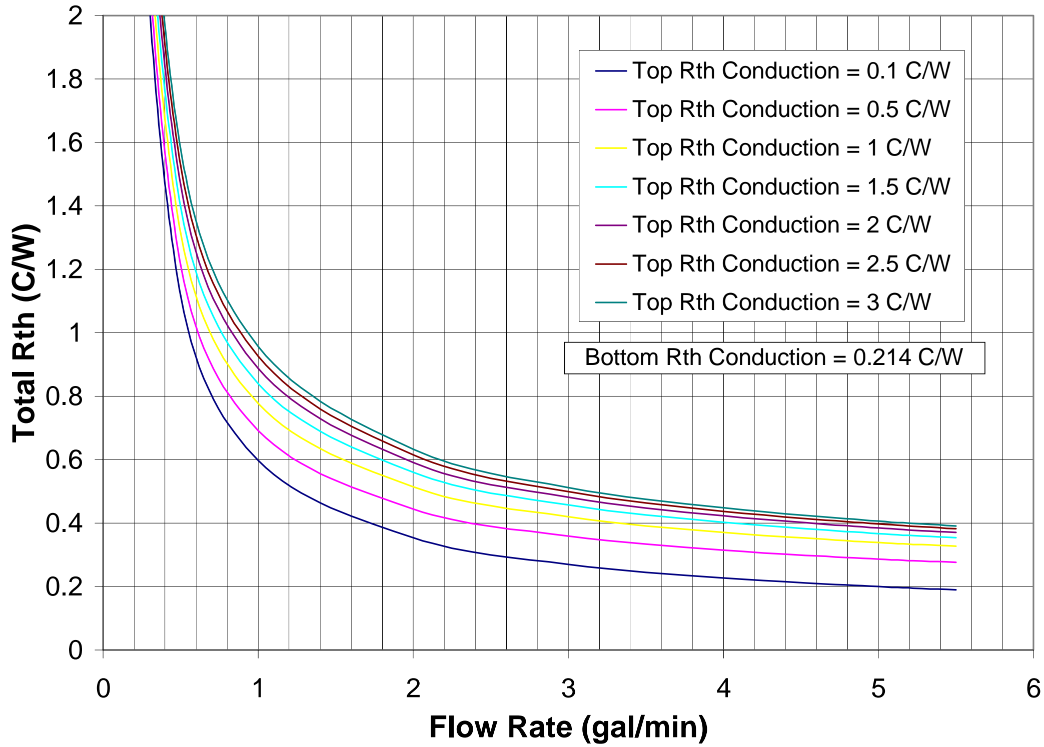


Figure 3.43 Total package thermal resistance vs. flow rate for various top side conduction thermal resistance values

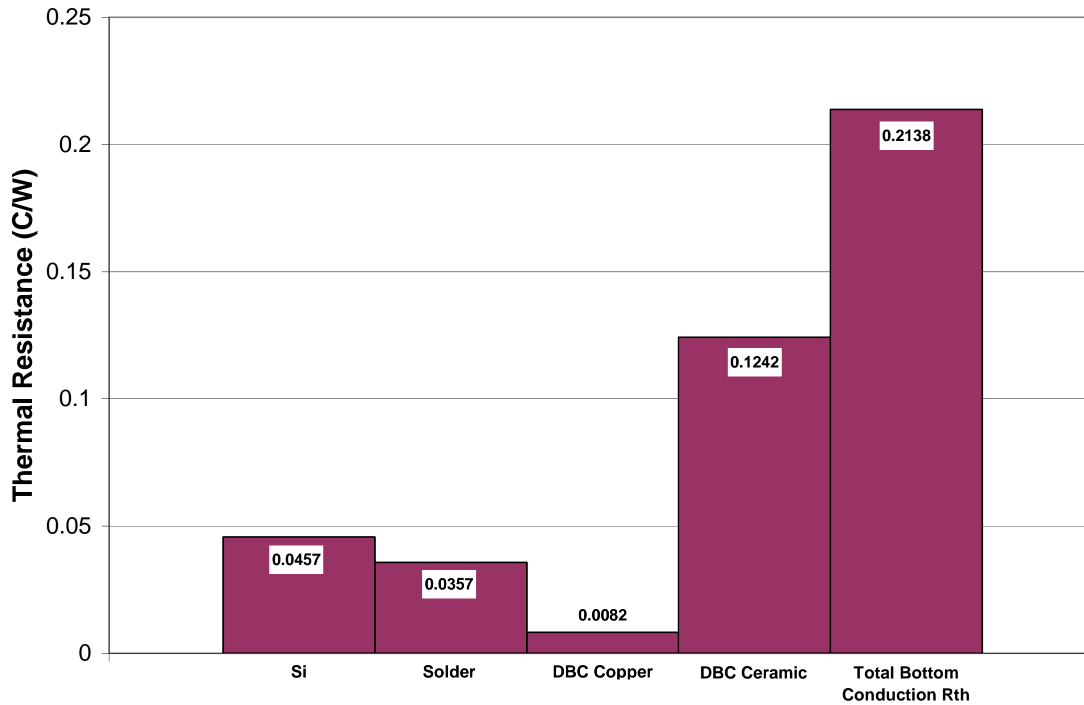


Figure 3.44 Comparison of bottom side conduction thermal resistance components

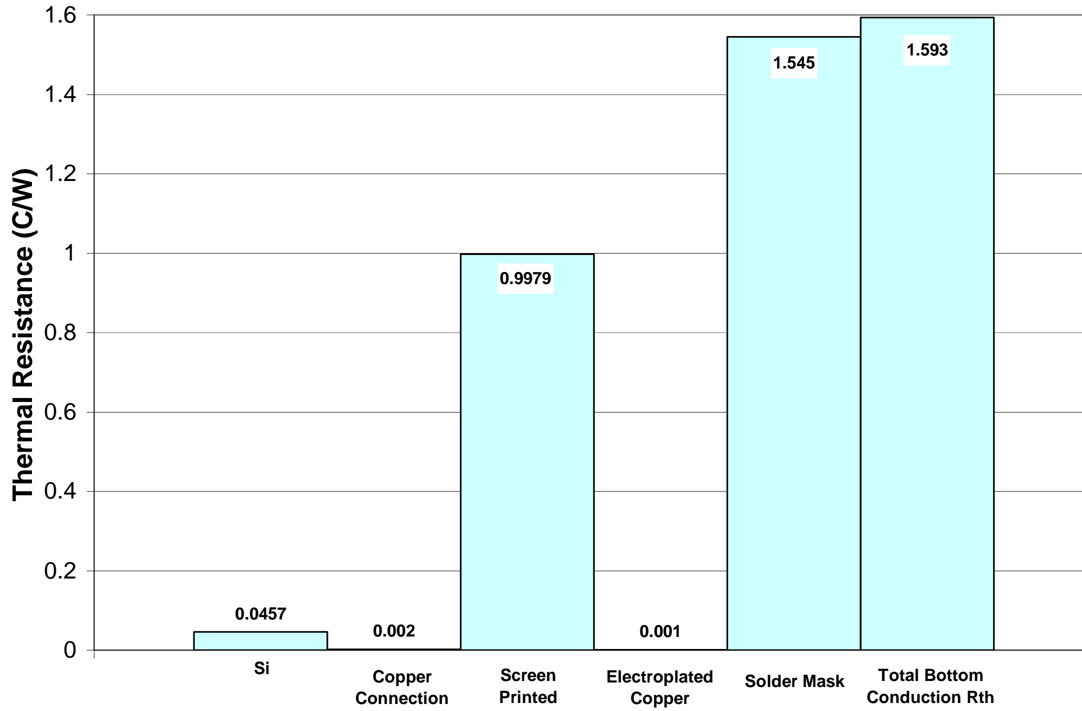


Figure 3.45 Comparison of top side conduction thermal resistance components

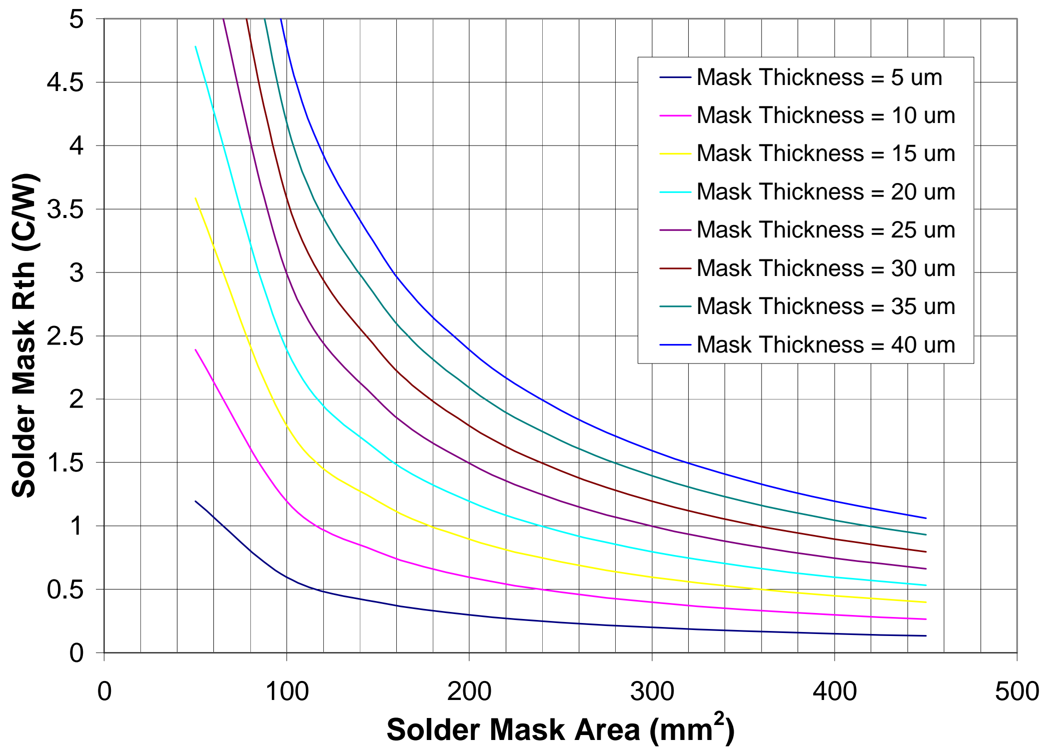


Figure 3.46 Solder mask thermal resistance vs. solder mask area for various solder mask thicknesses

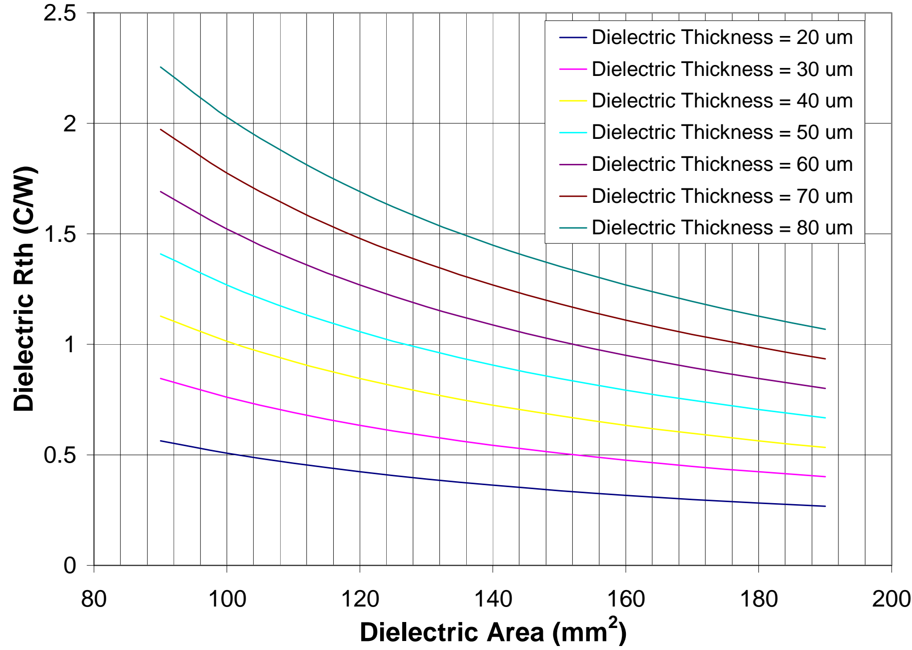


Figure 3.47 Screen printed dielectric thermal resistance vs. dielectric area for various dielectric thicknesses

Similar sources of error related to the conduction portion of the model can also be considered from these plots. Interfacial resistances were neglected since they are hard to characterize and can often be avoided during construction of the package. If a large thermal resistance interface existed in the package it would have a similar affect as the larger conduction components. This could be ruled out since the model predicts a higher overall thermal resistance than found experimentally. Material thermal conductivity could also have an affect on resistance if conductivity changes greatly with temperature. The thermal conductivity was assumed to be constant for each material in the package. This assumption was made since the package material conductivities do not change drastically over the temperature range experienced in the package and solving complexity is greatly reduced.

The convection portion of the model could be considered to be more complicated than the conduction part. The convection resistance model may also be subject to greater error since the flow was assumed to be fully developed and turbulent between two plates. An average velocity was also predicted from the inlet velocity from the round inlet tube. These assumptions neglect the affects of the inlet, outlet, and walls of liquid module, which could greatly change the flow field in the cooling region around the semiconductor

package. This would cause error in the local Reynolds numbers throughout the cooling region. The convection correlation is also limited in its range of application, specifically related to the Prandtl and Reynolds numbers. This might explain the extreme error between the model predictions and experimental results at lower flow rates, since this region exceeds the lower Reynolds limit of the correlation.

The overall affect of the convection thermal resistance on the total bottom, top, and double-side thermal resistances is shown in Figure 3.48. As expected, the convection thermal resistance is linearly related to the total package thermal resistances. This plot also shows that the range of convection thermal resistances found with this model causes a relatively large change in total package resistances. The derivation of the convection thermal resistance, given in section 2.1.2, shows its relationship to the Nusselt number and cooling area. The dependence of the total package resistances and convection resistance on the Nusselt number is shown in Figure 3.49. All of these resistances change greatly for lower Nusselt numbers.

The Nusselt number is related to the friction factor, Reynolds number, and Prandtl number. The relationship of these components to convection thermal resistance are shown in Figure 3.50 through Figure 3.52. Higher friction factors cause a large change in thermal resistance, which corresponds to the trends predicted for changes in the Nusselt and Reynolds numbers. Both high friction factors and low Nusselt numbers occur at low Reynolds or low fluid velocities. This implies that the model would be very sensitive to differences between the model correlation and experimental conditions at lower flow rates.

The study of the convection model implies that the experiment may not correctly mimic the conditions used to create the correlation. The model shows a considerably larger thermal resistance at low flow rates compared to experimental results. A higher Nusselt number could exist at lower flow rates due to the structure of the package and liquid module, which would correspond to a greater degree of turbulence and therefore heat transfer over the entire flow rate range.

The relationship between the fluid properties and convection model is apparent in Figure 3.51 and Figure 3.52 by reviewing the Prandtl number. Higher Prandtl numbers lead to lower and more constant thermal resistance over the flow rate range. A Prandtl

number for water at 25°C was assumed for this model since the flow rate was relatively high.

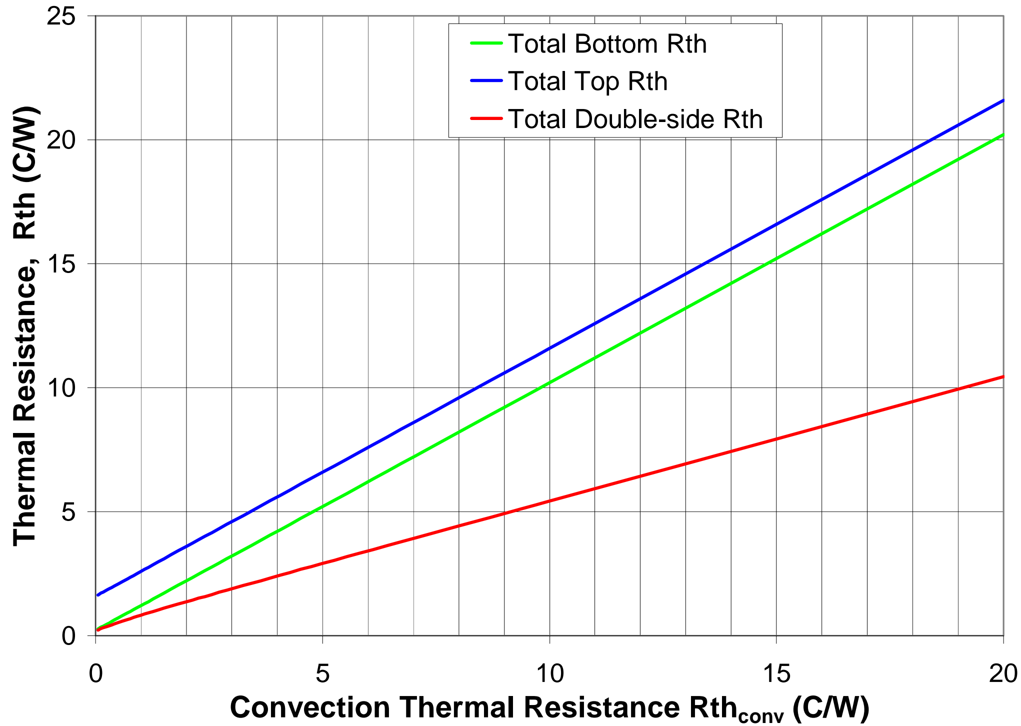


Figure 3.48 Total top, bottom, and double-side thermal resistance vs. convection thermal resistance

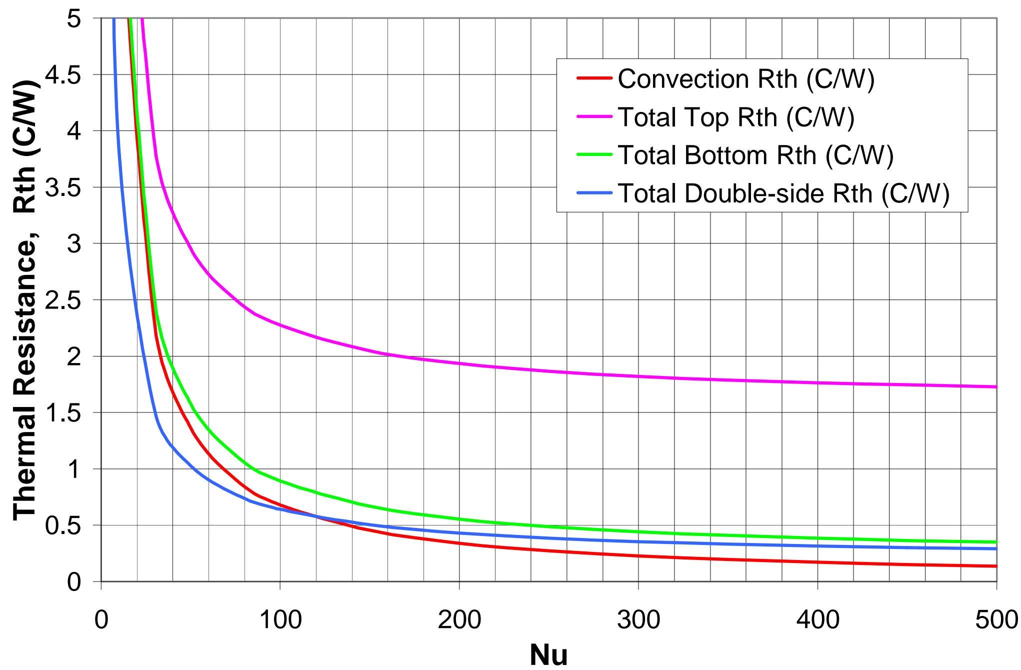


Figure 3.49 Convection, total top, total bottom, and total double-side thermal resistance vs. Nusselt number, Nu

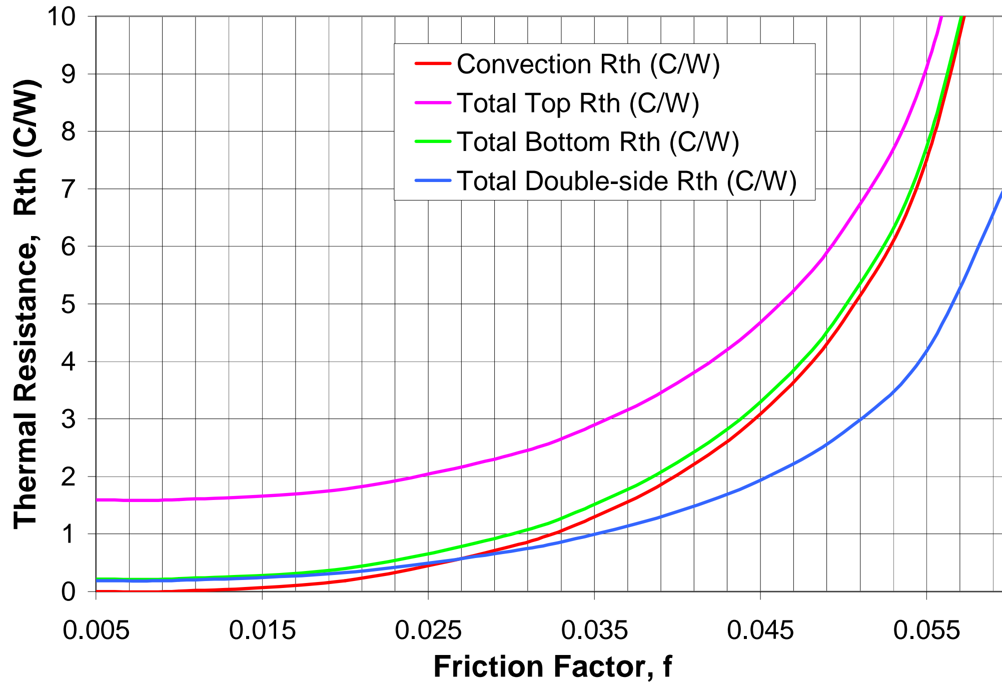


Figure 3.50 Convection, total top, total bottom, and total double-side thermal resistance vs. friction factor, f

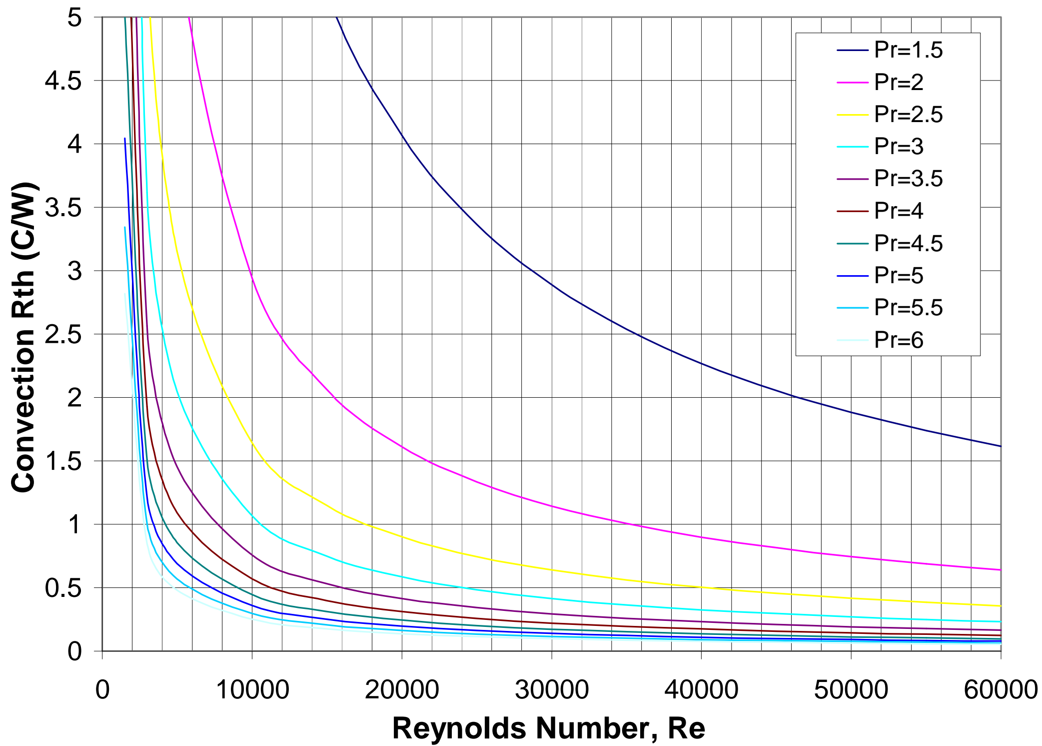


Figure 3.51 Convection thermal resistance vs. Reynolds number, Re, for various Prandtl numbers, Pr

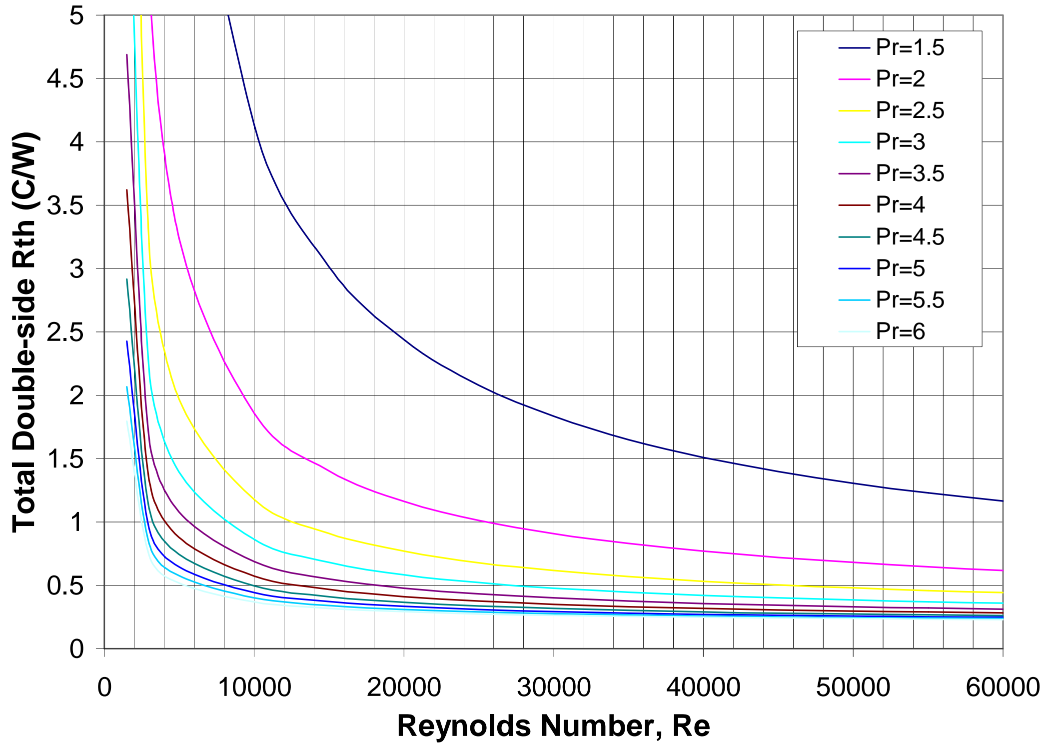


Figure 3.52 Total package thermal resistance vs. Reynolds number, Re, for various Prandtl numbers, Pr

The convection thermal resistance is highly dependent on the cooling area as shown for the conduction portion of the model. Figure 3.53 and Figure 3.54 show the affect of varying the cooling area or chip size. A drastic increase in heat transfer is noticed as the cooling area increases. The increase in cooling area also makes the model less sensitive to changes in flow rate over the flow rate range except in the lower region. As stated for conduction, increased cooling area might be more realistic to true heat transfer through materials and the environment. The hydraulic diameter could also be a source of error even though the dimensions of the module are well characterized. The hydraulic diameter calculation for a non-circular tube inherently provides an average solution for the Reynolds number and heat transfer coefficient since convection heat transfer varies drastically along the perimeter of the structure and approaches zero in the corners. The hydraulic diameter is linearly related to the Reynolds number and convection coefficient, which are described in the previous plots.

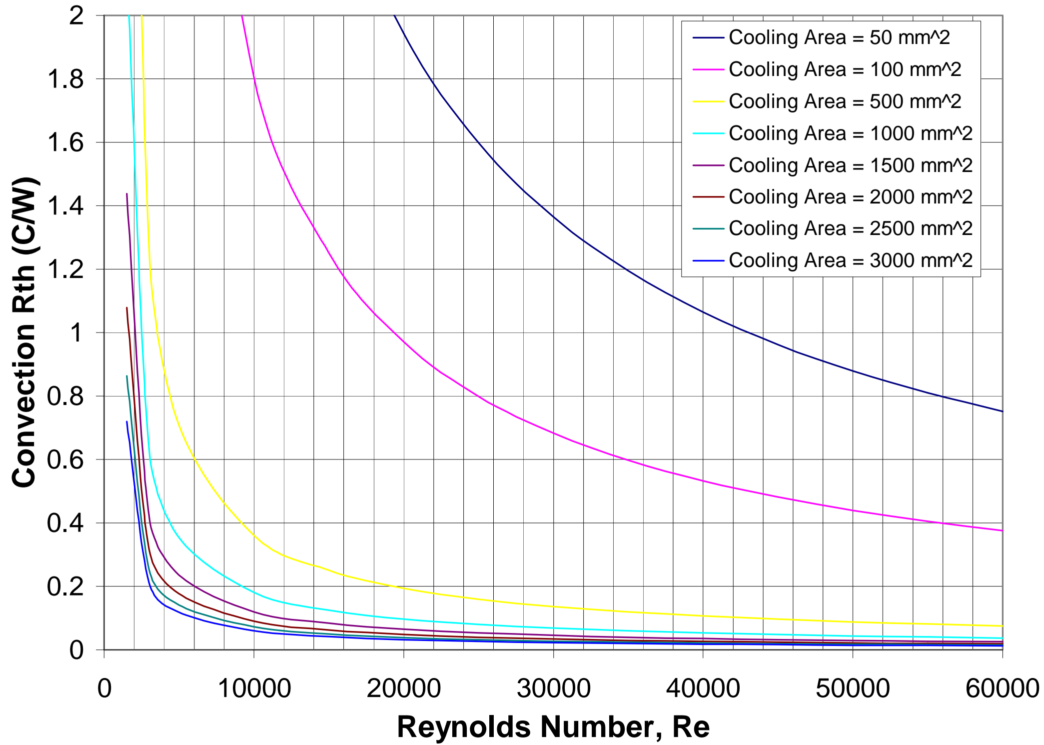


Figure 3.53 Convection thermal resistance vs. Reynolds number, Re, for various cooling areas

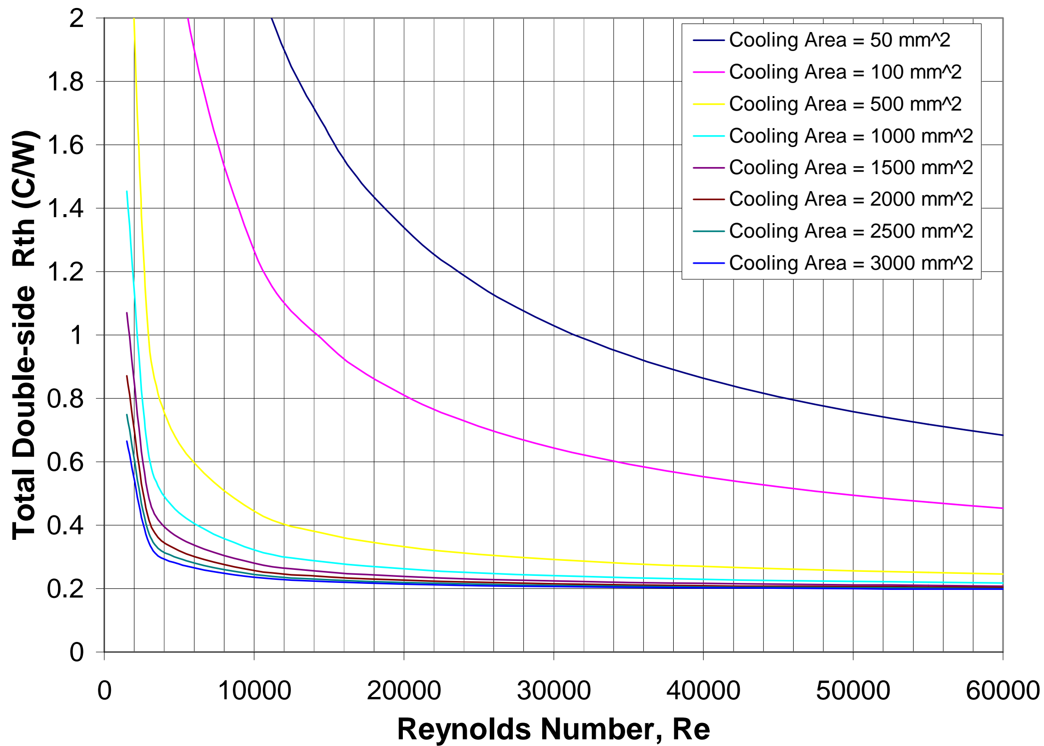


Figure 3.54 Total package thermal resistance vs. Reynolds number, Re, for various cooling areas

Overall, the model fulfilled its purpose as a quick tool to analyze the potential for high flow rate, double-sided forced liquid cooling with embedded power technology. The parametric analysis shows that there exist several factors that could lead to error between model predictions and experimental results. These factors include the material properties, conduction layer thicknesses, flow field assumptions, and multiple dimension heat transfer. These items could be studied further through more detailed modeling and experiments to determine their true weight in the system. More advanced software tools involving finite element analysis and computational fluid dynamics would be required to create an accurate and robust model of the liquid cooling system.

4 CONCLUSIONS AND FUTURE RESEARCH

4.1 Conclusions

The research reported in this thesis has focused on advanced forced liquid convection and its interface to power semiconductor packaging. Embedded power technology packaging allows double-side, high velocity forced convection cooling. This advanced thermal management cooling scheme can help improve semiconductor performance and power density by providing a considerably lower thermal resistance while not effecting electrical performance.

Traditional power semiconductor packaging, including wire bond based packaging, is limited in thermal performance since the wire bond side of the device is difficult to interface with advanced cooling schemes such as jet impingement or other forced liquid convection cooling schemes. Phase change and spray cooling schemes have been explored for the wire bond side of the power semiconductor and show very promising results [4-10]. Researchers have explored alternate packaging technologies to attempt to double the device cooling area or halve the loss density while eliminating concerns about dimensioning electrical performance or effecting reliability that is present for top side cooled wire bond device packaging. These packaging technologies include power overlay technology, DirectFET^{TM}, press pack technology, embedded power, and flip chip solder ball interconnects [11-18]. Design complexity, cooling efficiency, electrical isolation and power density must be considered for each case when interfacing the device package with advanced double-sided cooling schemes.

One dimensional physics based electro-thermal models were constructed to explore the potential of double-sided force liquid convection with embedded power package. Thermal modeling results showed that embedded power with double-sided forced liquid cooling reduces thermal resistance considerably in steady state thermal conditions compared to a wire bond package with single-sided liquid cooling.

A liquid module test bed was constructed to verify predictions by the physics based electro-thermal models for double and single-sided liquid cooling with wire bond and embedded power packaging technologies. Sealing material choice was shown to be

critical for a reliable fluid system design. Mechanical design for interfacing the embedded power with the test bed was also found to be extremely important. The overall strength and reliability of the embedded power package must be understood in order to allow proper operation of the cooling system for the life of the semiconductors.

Experimental results for single-sided liquid cooling with wire bond packaging and double-sided liquid cooling with embedded power packaging follow the trends predicted in modeling. A 45% to 60% improvement is shown by double-side liquid cooled embedded power. An analysis of the models shows possible sources of error between the model and experimental findings. These sources include flow field assumptions, one dimensional heat transfer, material properties, and material geometry. Further investigation using finite element analysis and computational fluid dynamic software would be required to improve the model prediction capability.

The interface between semiconductor device packaging and its cooling system will determine the overall power density of a power electronic system and its application. Embedded Power technology can provide a large thermal improvement while maintaining electrical functionality by interfacing the package with an advanced cooling scheme, such as high flow rate, forced liquid convection.

4.2 Direction of Future Research

Research in the areas of thermal management and semiconductor packaging is an open ended field. The research presented in this thesis shows great promise for a single packaging technology, embedded power, and a single cooling method, high velocity planar forced liquid convection. Future work should include a more detailed study of packaging technologies and cooling schemes. Commercial wire bond device packaging could be experimentally studied in addition to emerging alternate packaging technologies such as DirectFET™. Certain packaging technologies may lend themselves to single device cooling while others allow high power density, system level cooling. Other advanced cooling schemes, such as jet impingement, spray cooling, phase change and convective/phase change, could be studied with several modifications to this test bed. These cooling schemes could have fewer design or operation penalties versus high velocity planar convection.

Alternate embedded power designs and their potential for high power systems with enhanced thermal management schemes could also be explored experimentally with this test bed. The replacement of wire bonds and solder interconnects with planar metallization minimizes the conduction thermal resistance above and below the semiconductor device. The package has the potential to improve thermal performance further by directly applying fluid on both sides of a power semiconductor device. Mechanical design issues, such as pressure effects on chip attachment and mechanical abrasion of traces due to fluid flow, would then most likely out weigh many common electrical considerations in importance.

Improved thermal modeling techniques would be valuable for power electronics packaging design and understanding different thermal management schemes. Computational fluid dynamic and finite element base heat transfer software could be used to develop a correlation for convection heat transfer through the liquid module test bed. Alternate materials in the semiconductor package, such as aluminum nitride substrate carrier, aluminum nitride DBC, diamond heat spreaders, microstructures, and thin film insulation, could also be studied using simulation tools and then confirmed experimentally.

Appendix A Liquid Module Autocad Drawings

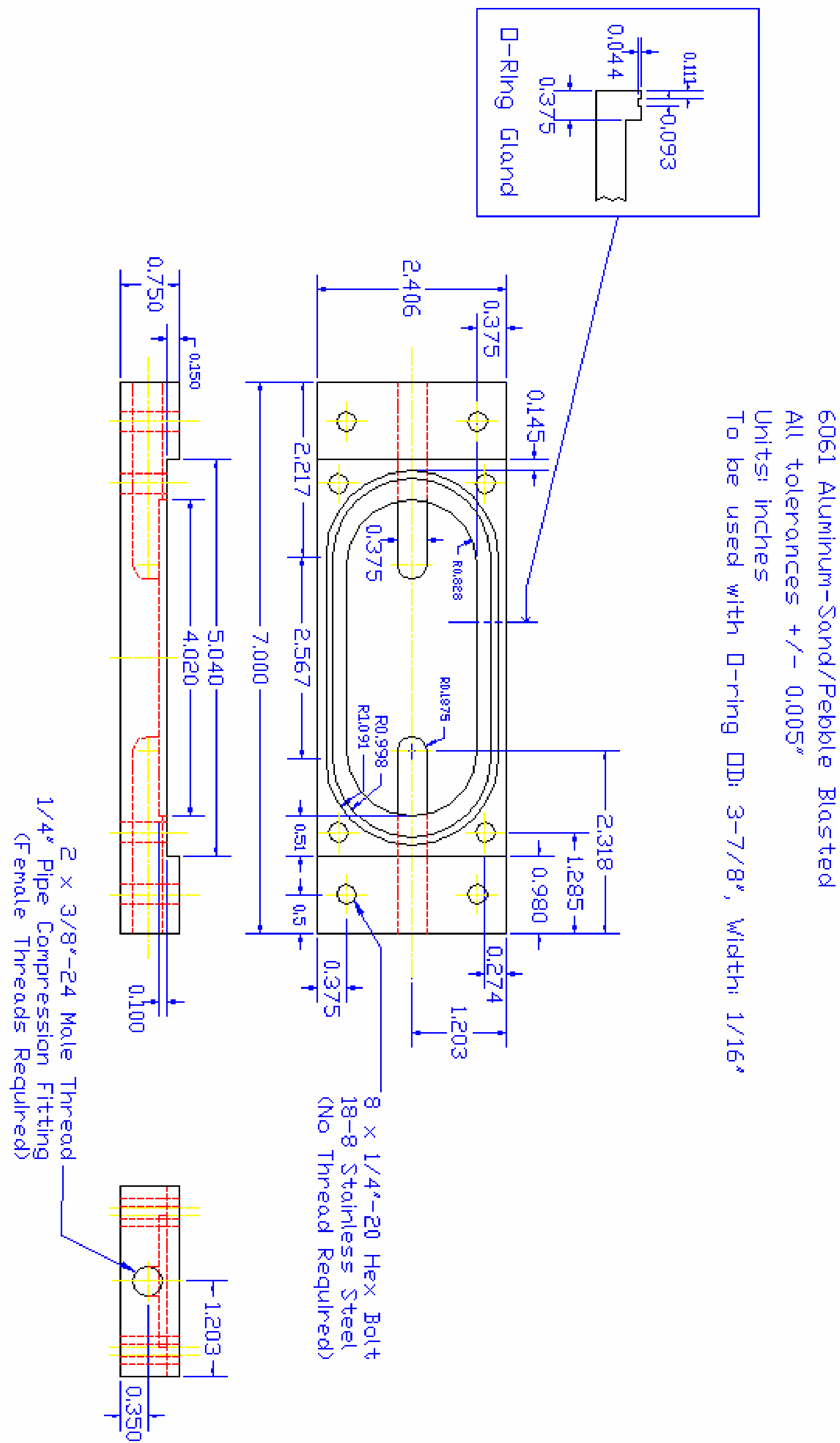


Figure A.1 Liquid module test bed design

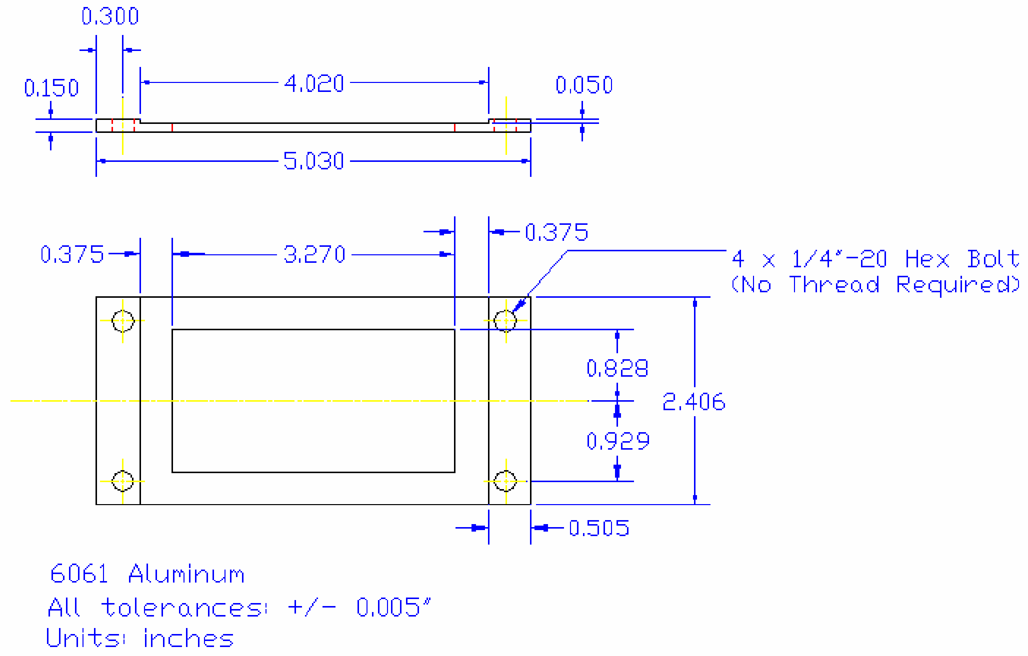


Figure A.2 Sample frame design

Appendix B Embedded Power Package Autocad Drawings

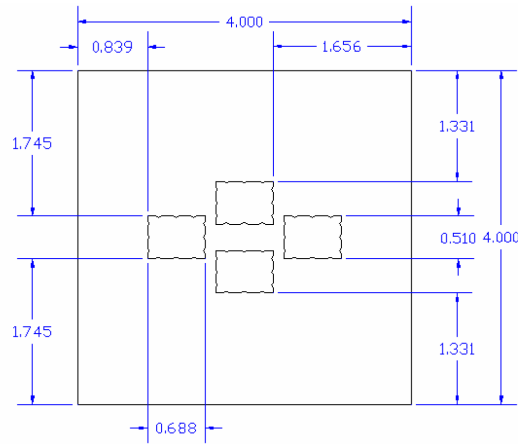


Figure B.1 Substrate carrier laser cut out pattern for the embedded power package

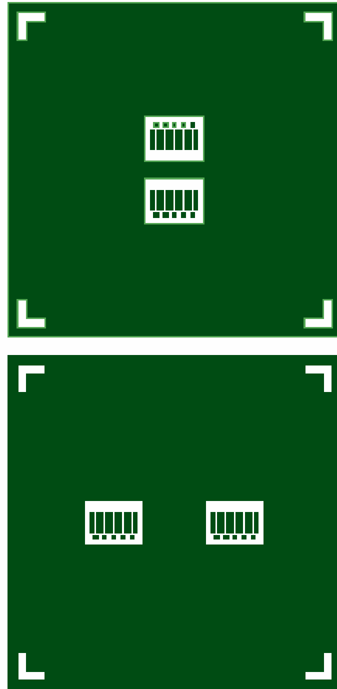


Figure B.2 Drawing of screen printing dielectric layer design for the embedded power package

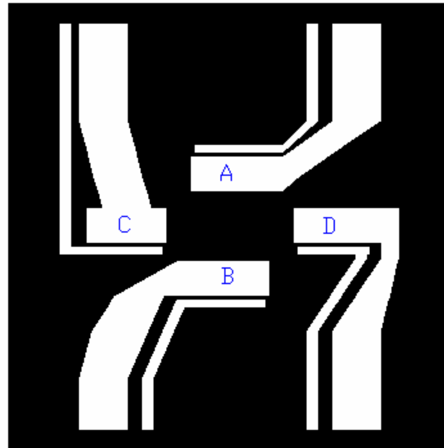


Figure B.3 Drawing of trace layout design for the embedded power package

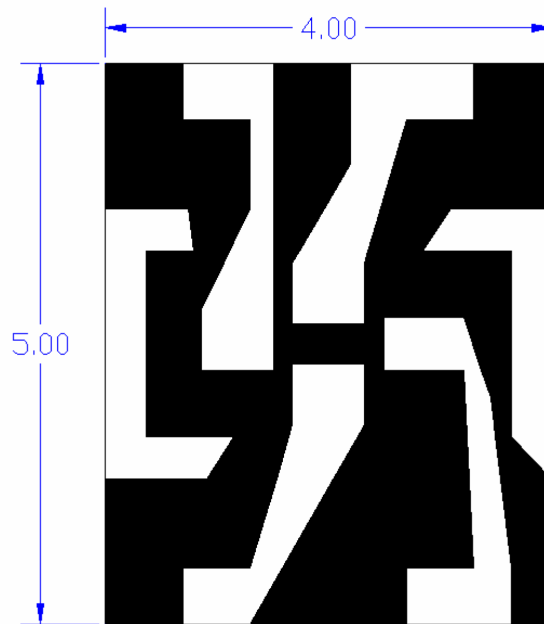


Figure B.4 DBC drain trace design for the embedded power package

Appendix C Embedded Power Package Construction Outline

Embedded Power Sample Construction Steps

1) Create design in Autocad
2) Create Autocad and obtain screen for screen printing for gate and source isolation (for FETS)
3) Create Autocad and transparency matching screen printing design for solder mask application
4) Create Autocad and transparency for Cu trace pattern (show areas where Cu is wanted)
5) Create Autocad and transparency for DBC drain pattern if being used
6) Create Autocad for substrate die cut
7) Clean substrate using acetone, alcohol, DI water
8) Cut substrate for embedding die using laser
9) Clean substrate after laser cutting using diamond file, acetone, alcohol, and DI water
10) Embed chips using Master Bond EP3AOHT
    a. Apply kapton on metallization side of substrate carrier (make sure flat)
    b. Place chips in substrate carrier on kapton and apply epoxy around chips
    c. Check for voids using light
    d. Stamp voids out using needle or tweezers and add more epoxy if necessary
    e. Cure embedding polymer (1 ^{o}C/min up to 150 ^{o}C, bake for 15 minutes) in lab oven
    f. Allow to cool and remove from oven
11) Screen print dielectric (EPO-TEK 600)
    a. Make sure screens are clean with acetone and alcohol and dry with forced air
    b. Mount screen
    c. Screen print first pattern
    d. Cure screen print material (1 ^{o}C/min up to 150 ^{o}C, bake for 60 minutes, 1 ^{o}C/min up 200 ^{o}C bake for 30 minutes) in lab oven
    e. Allow to cool and remove from oven
    f. Mount screen second screen if applicable
    g. Screen print second pattern
    h. Cure screen print material (1 ^{o}C/min up to 150 ^{o}C, bake for 60 minutes, 1 ^{o}C/min up 200 ^{o}C bake for 30 minutes) in lab oven
    i. Clean screens using acetone and alcohol, dry screens using forced air
    j. Allow to cool and remove from oven
12) Dielectric reinforcement/sputtered layer
    a. Mix Enthone DSR-3241 liquid photoimageable solder mask, 4 parts to 1 by weight
    b. Apply solder mask extremely thin using spatula (no air bubbles)
    c. Spin coat solder mask (800 RPM for 15 sec, $\geq$2000 RPM for 40 sec)
    d. Cure for 20 minutes at 85 ^{o}C or until no longer sticky then allow to cool
    e. Repeat if doing double side metallization
    f. Attach transparency(ies) matching screen print design
    g. Expose to UV light for 10 minutes (can repeat second time) then allow to cool and remove transparency(ies)
    h. Develop solder mask in D4000 developer solution with brush (20:1, DI Water: D4000)
    i. Rinse sample with water
    j. Cure outside dark room in oven (1 ^{o}C up to 160 ^{o}C, bake for 30 minutes)
    k. Allow to cool and remove from oven
13) Sputter (thin metallization application)
    a. Clean sample – acetone, alcohol, DI water and/or plasma (dry) clean
    b. Sputter Ti (10 to 15 minutes)
    c. Sputter Cu (twice) (15 minutes each allowing to cool for 15 minutes in-between)
    d. Remove sample and repeat if double side is required
14) Apply photo mask for Cu electroplating
    a. Apply Photrak EPT240/1694 photoimageable etch resist (blue) thin using spatula (no air bubbles)

b. Spin coat mask (800 RPM for 15 sec, ≥2000 RPM for 40 sec)
c. Cure for 20 minutes at 85 °C or until no longer sticky then allow to cool
d. Repeat for other side if doing double side metallization
e. Attach transparency(ies) for Cu electroplating (CU trace pattern)
f. Expose to UV light for 10 minutes then allow to cool (can repeat second time) and remove transparency(ies)
g. Develop solder mask in D4000 developer solution with brush (20:1, DI Water: D4000)
h. Rinse sample with DI water

15) Cu electroplating (thick film traces)
  a. Attach electroplating frame
    i. Kapton sample very carefully (plating solution is acid based and will etch sputtered Cu contacts, wire or Cu sheet can be soldered as an alternative)
  b. Attach anode(s) (Cu target) to plating system in solution
    i. Tape anode(s) so that anode is roughly ¾ to ½ the area of the sample to achieve more uniform plating
  c. Dip sample in plating solution, Techni Copper RR, several times to clean surface
  d. Attach sample to plating system
  e. Plate at the following rate 20mA/cm^2 for 1 hour to achieve 1 mil
    i. My case: 533 mA for 3 hour for roughly 3 mil for single side metallization case
    ii. check sample and voltage drop through out process (roughly every 15 to 30 minutes)
  f. Remove sample from plating solution and rinse with DI water and dry with forced air
  g. Remove frame very carefully
  h. If satisfied with plating remove photo mask with acetone and rinse with DI water and dry with forced air

16) Thin film Cu and Ti etch
  a. Cu micro etch
    i. Mix 16.9 gram water to 1 gram PC200-10 Etchant-SP (Sodium Persulate-Oxidizer) by Injectorall Electronics Corp (powder)
      1. Or ½ lb powder to 1 gal water
    ii. Remove sputtered Cu using Cu micro etch and brush
    iii. Rinse with DI water
  b. Ti etch
    i. Mix 20 parts water to 1 part Ti etch TFT (Hydrofluric acid based) (can use less water or more water depending on desired etch rate)
    ii. Remove sputtered Ti with Ti etch
    iii. Clean with acetone, alcohol, and DI water

17) Chip Protection (Optional)
  a. Solder a 20kΩ to 50kΩ surface mount resistor between the gate and source trace of each chip for protection

18) DBC construction (if being used)
  a. Etch DBC in order to cut to proper dimensions using bench top etcher
    i. Use kapton for etch resist
  b. Cut with laser
  c. Create DBC pattern
    i. Apply Photrak EPT240/1694 photoimageable etch resist (blue) thin using spatula (no air bubbles) (can use kapton for backside resist)
    ii. Spin coat mask if possible (800 RPM for 15 sec, 2000 RPM for 40 sec)
    iii. Cure for 20 minutes at 85 °C or until no longer sticky then allow to cool
    iv. Attach transparency for DBC pattern
    v. Expose to UV light for 10 minutes (can repeat second time) then allow to cool and remove transparency
    vi. Develop solder mask in D4000 developer solution with brush (20:1, DI Water: D4000)
    vii. Rinse sample with water
    viii. Etch using bench top etcher

ix. Once Cu completely removed, remove photomask using acetone
x. Clean DBC with acetone, alcohol, and DI water (can also perform a light acid clean to clean ceramic)

d. Attach thermocouples under drain pads on DBC
i. Create thermocouples using thermocouple welder in lab (Type K insulated) and check functionality with data acquisition unit
ii. Attach thermocouples with kapton away from exposed measurement points
iii. Apply Masterbond EP3AOHT under and above exposed couple measurement point
1. Make sure couples are flat and epoxy is not higher than drain pad
iv. Cure embedding polymer (1 ^{o}C up to 150 ^{o}C, bake for 15 minutes) in lab oven
v. Allow to cool and remove from oven
vi. Check functionality of couples using solder iron on pad and data acquisition unit

19) Attach DBC to embedded chips if not creating double side metallization sample
a. Place a considerable amount of standard solder paste (www.efdsolder.com $Sn_{43}Pb_{43}Bi_{14}$-163°C) on each drain pad and drain side of chips (try to fill greater than 15 mil x chip area of volume)
b. Place a 5 to 10 mil thickness of flat (use hydraulic press to insure flatness) Cu strip on solder paste on drain of chip (Cu strip should be cut to match the chip size)
i. Alternate technique: Place multiple solder balls in paste on drain pads along with Cu or instead of Cu strip if desired (~15 balls for my APT FREDFET)
c. Place substrate carrier with chips on DBC
d. Attach any other structure using solder paste to top of embedded power sample
e. Reflow sample 50°C, 100°C (preheat), 150°C, 160°C (soak), 195°C (reflow), 150°C 50°C (cool down) speed 2 to 10

20) Check chip(s) functionality
21) Insulation application (if dielectric fluid not being used)
a. Can apply high temperature parylene if leads are taped for best thermal performance
b. Solder mask as easy alternate
i. Mix Enthone DSR-3241 liquid photoimageable solder mask, 4 parts to 1 by weight
ii. Apply solder mask extremely thin using spatula (no air bubbles)
iii. Spin coat solder mask if possible (800 RPM for 15 sec, 2000 RPM for 40 sec)
iv. Cure for 20 minutes at 85 ^{o}C or until no longer sticky then allow to cool
v. Repeat if doing double side metallization
vi. Expose to UV light for 10 minutes (can repeat second time) then allow to cool and remove transparency(ies)
vii. Develop solder mask in D4000 developer solution with brush (20:1, DI Water: D4000)
viii. Rinse sample with DI water
ix. Cure outside dark room in oven (1 ^{o}C up to 160 ^{o}C, bake for 30 minutes)
x. Allow to cool and remove from oven
xi. Clean with acetone, alcohol, and DI water

22) Attach connection points via solder or solder paste with hotplate and solder iron (careful about overheating pads, may peal off)
23) Check functionality of chips
24) Attach cooling frames using silicon gasket sealer
25) Check functionality of chips
26) Begin testing

Appendix D Wire Bond Package Autocad Drawings

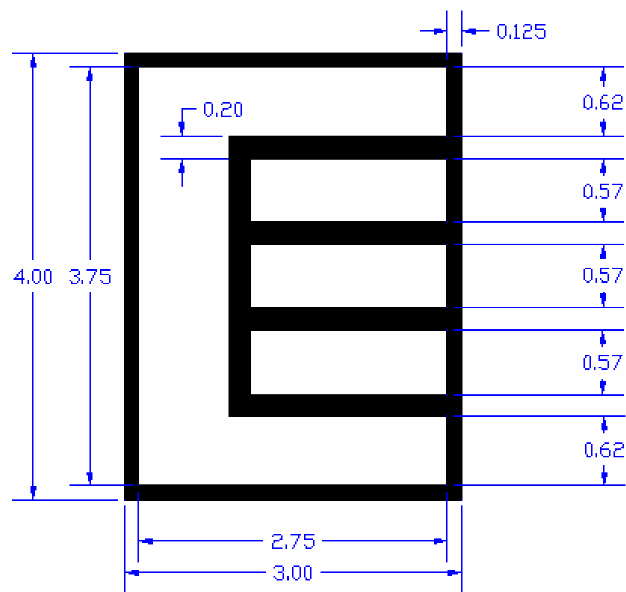


Figure D.1 DBC trace design for wire bond package

Appendix E Wire Bond Package Construction Outline

Wire Bond Sample Construction Steps

1) Create design in Autocad
2) Create Autocad and transparency for DBC trace pattern
3) Create Autocad for DBC cutting/etching if required
4) Clean substrate using acetone, alcohol, DI water
5) DBC construction (if being used)
    a. Etch DBC in order to cut to proper dimensions using bench top etcher
        i. Use kapton for etch resist
    b. Cut with laser
    c. Create DBC pattern
        i. Apply Photrak EPT240/1694 photoimageable etch resist (blue) thin using spatula (no air bubbles) (can use kapton for backside resist)
        ii. Spin coat mask if possible (800 RPM for 15 sec, 2000 RPM for 40 sec)
        iii. Cure for 20 minutes at 85 ^{o}C or until no longer sticky then allow to cool
        iv. Attach transparency for DBC pattern
        v. Expose to UV light for 10 minutes (can repeat second time) then allow to cool and remove transparency
        vi. Develop solder mask in D4000 developer solution with brush (20:1, DI Water: D4000)
        vii. Rinse sample with water
        viii. Etch using bench top etcher
        ix. Once Cu completely removed, remove photomask using acetone
        x. Clean DBC with acetone, alcohol, and DI water (can also perform a light acid clean to clean ceramic)
6) Attach the MOSFET to the DBC substrate
    a. Apply kapton over the DBC pattern and cut out rectangles for the drain pads
    b. Place a considerable amount of standard solder paste (www.efdsolder.com $Sn_{43}Pb_{43}Bi_{14}$-163°C)
    c. Attach any other structure using solder paste to the DBC using the same solder paste
    d. Reflow sample 50°C, 100°C (preheat), 150°C, 160°C (soak), 195°C (reflow), 150°C 50°C (cool down) speed 2 to 10
    e. Allow the sample to cool
7) Attach wire bonds to the gate and source pads on the chip and DBC using an ultrasonic wire bonder
8) Check functionality of chips
9) Attach cooling frames using silicone gasket sealer
10) Check functionality of chips
11) Begin testing

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VITA

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