Design and Prototyping of a Wireless Data Transceiver in the 900MHz ISM Band

Benjamin M. Grady

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Dr. Charles W. Bostian, Chairman
Dr. Dennis G. Sweeney
Dr. Tim Pratt

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Design and Prototyping of a Wireless Data Transceiver in the 900MHz ISM Band

By

Benjamin M. Grady

Committee Chairman: Dr. Charles W. Bostian

(Abstract)

The Communications industry is currently involved in a wireless revolution. Consequently, there is a need for a wide variety of wireless solutions to replace existing wired systems. The major systems, such as cellular and satellite, are costly to put in place and require a low BER (bit error rate) to be successful for their real-time applications. In contrast to this are those systems that can tolerate a higher BER as a trade off for cost (<$50.00) and complexity. A typical application for these lower cost systems is monitoring non-critical data that is not required to be delivered real-time.

The work presented here focused on designing, building and testing a Proof of Concept Prototype (POCP) for a low-cost wireless data link (WDL). In a typical WDL application, problems arise when too large a data rate attempts to travel the allotted channel bandwidth in the frequency band of interest. Also, limitations imposed by current radio transceiver technology tend to limit WDL design. The existing sponsor's wired system operates at a 9600 Baud, and presented the opposite problem: the data rate was too low for the RF Microdevices RF2905 used for the POCP. This challenge necessitated the development of a low-cost encoding scheme using standard digital logic gates in place of more costly Manchester Encoding. For the digital logic encoding scheme to work, the crystal oscillators had to be modified. This resolved the problem with the low frequency limitations of the RF2905 phase locked-loop. In addition, the polled, asynchronous, and unbalanced RS485 connections of the wired system had to be adapted to interface with the single-ended data connections of the WDL. Finally, the successful design of a timing scheme, using standard TTL components and balanced to unbalanced drivers, resolved the interface problems resulting in a low-cost WDL designed to operate with an existing wired system without requiring modifications to that system. The WDL is transparent in connection and operation and can be inserted without disrupting the current wired system.

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Table of Contents

List of Figures

List of Tables

Chapter 1 Introduction

The Communications industry is currently involved in a wireless revolution. Consequently, there is a need for a wide variety of wireless solutions to replace existing wired systems. The major systems, such as cellular and satellite, are costly to put in place and require a low BER (bit error rate) to be successful for their real-time applications. In contrast to this are those systems that can tolerate a higher BER as a trade off for cost and complexity. A typical application for these lower cost systems is monitoring non-critical data that is not required to be delivered real-time.

The sponsor of the project described here designed and built an electric power sub-measurement system to monitor power consumption at breaker panels. It is to be installed in customers' businesses, factories, shopping malls, and other facilities. The system gathers power information (complex voltage, current, power factor, etc.) and transmits it back to the sponsor for storage. Using the World Wide Web (WWW), customers can query the database for information regarding their power consumption. An example of the usefulness of this data is monitoring air conditioner units located on a roof. If one unit tends to draw more power then the others, the customer may want to have the unit checked. Presently the system uses a RS485 wired, balanced line to connect multiple units together at a single customer site. The sponsor wishes to replace this with a wireless connection.

This thesis describes the design and testing of a Proof of Concept Prototype (POCP) for the low-cost Wireless Data Link (WDL). Low cost is defined here as less than $50.00 per unit. The WDL for this project consists of three main parts: the RF transceiver, the digital interface (DIF), and a data source. The transceiver is a slightly modified RF Micro Devices (RFMD) 2905-evaluation board, while the DIF is a custom designed circuit board that contains the encoding and interface circuitry. The data source is either a computer, or the sponsor's monitoring unit (SMU). The data protocol is asynchronous RS232 standard with parameters N81 (no parity, 8 data bits, one stop bit) at 9600 BAUD. The data encoding/decoding scheme, performance testing of the encoding/decoding scheme, transmitter/receiver operation, and system propagation testing are detailed in the thesis.

1.1 Statement of the Problem

The basic data acquisition system consists of a single master and several slave units (Figure 1.1). The individual units are connected via an RS485 bus.

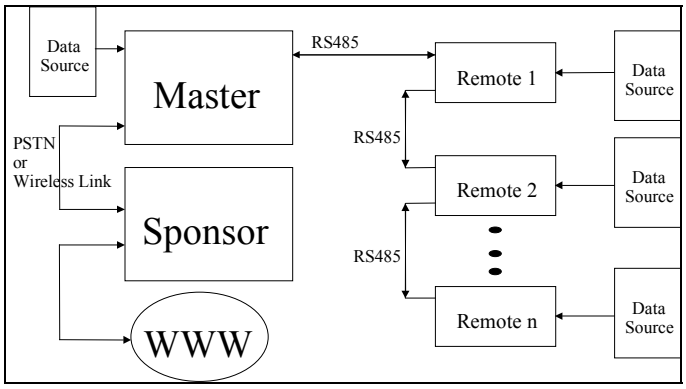


Figure 1.1 Wired Data Acquisition System

During operation, the master polls each slave for data; the slave responds with the requested data, and the master sends the data to a central database for storage. The data can then be accessed via the WWW and queried for detailed reports regarding the measured parameters. The task was to remove the RS485 wire link and replace it with a wireless component. The replacement had to be low-cost and transparent to the existing system.

From the sponsor's point of view, the WDL had to meet three criteria; sell for less than $50, require no design changes to the current SMU, and be usable in either the United States or Europe. From the design point of view these requirements affected the decision making process for the POCP. This thesis describes the steps taken and obstacles overcome in order to design the WDL POCP according to the sponsor's specifications. The main tasks accomplished were:

- Selected an operating frequency and modulation type
- Located parts that would meet the requirements for both cost and design
- Modified the parts to work with the sub-measurement system
- Built the WDL POCP
- Tested the system on the bench and in the field

1.2 Contributions to Knowledge

RF transceiver manufacturers, such as RF Microdevices, are primarily concerned that their parts meet specifications during laboratory and production tests. It is up to the end user to implement and test components in real world applications. Consequently, manufacturers have very little information on the performance of their components when used for their designed purpose. In addition, the implications of the design limitations of the components are not explored to any detailed depth. The work described here has addressed these problems, and as a result, has produced several contributions to knowledge.

The RF Microdeveices RF2905 was implemented in a WDL to be used in a commercial application. The data rate of the application was lower than could be handled by the RF2905, which required the development of an encoder/decoder to overcome this problem. Although Manchester Encoding is suggested in the RF2905 data sheet, cost constraints required the development of a lower cost method that does not require synchronization. Digital Logic Encoding (DLOC) uses standard TTL logic gates and timers at a cost of less than $1.00 per unit, as compared to Manchester Encoding (cost > $15.00). The system was tested with both DLOC and Manchester Encoding. It was found that the low-cost encoding scheme worked as well as, and in many cases better than, Manchester Encoding for the WDL. In addition, performance of the RF2905 was measured during use both in buildings and outdoors, which gives valuable feedback to the manufacturer as to its actual performance compared to verification and production line testing.

Chapter 2 WDL Specifications

The WDL provides all the functions associated with Layer 1 (physical layer) of the ISO/OSI Seven Layer model. The physical layer is responsible for providing the physical transmission, coding, modulation and other tasks that establish and maintain the channel. In basic terms the WDL receives baseband data from the transmitting SMU and passes baseband data to the receiving SMU. This fulfills the requirement of being transparent to the current wired system. Table 2.1 shows the WDL specifications as determined by conceptual analysis and preliminary system design. Chapter 2 describes the selection process from which these specifications were derived.

2.1 Radio Channel

The radio channel link between multiple slaves and a single master data unit is half-duplex. Half-duplex, or simplex, means that only one unit transmits at a time; therefore data cannot be passed in both directions at the same time. This type of configuration lends itself well to polling, the application where a master requests data from each remote unit, which responds in turn. Half duplex reduces the complexity of the transceiver and therefore reduces the cost.

Table 2.1 Radio Channel Specifications

Operating Frequency (ISM unlicensed band)	TX 905.663 MHz RX 916.360 MHz
IF Frequency	10.7 MHz
TX Power	+10 or –10 dBm (selectable)
Modulation	FSK (frequency Shift Keying)
FSK Deviation-Mode 1	85kHz
FSK Deviation-Mode 2	85kHz for data 1, none for data 0
Data Encoding-Mode 1	Manchester Encoding (43.2kHz)
Data Encoding-Mode 2	Modified AMI
Data Rate	43.2kHz
DC Power	+12V to +24V
DC Current	120mA typical (in TX mode)

The SMUs are to be deployed throughout the world and the sponsor required that the WDL operate in an unlicensed frequency band. The initial deployment of the SMU is in the United States (US); thus the requirement was reduced to US unlicensed frequencies for which components were readily available. A final restriction was that the radio channel component(s) had to be purchased from RF Micro Devices (RFMD). Based on these criteria, it was determined that the RF2905 was the best available component. This component is a receiver and transmitter on a single chip (transceiver) that operates in either the 915MHz US or the 400MHz and 868MHz European unlicensed bands. For the physical layer to be low-cost, it was determined that no microprocessor, and as little additional circuitry as possible, were to be incorporated into the WDL. This defined that the transmission layer use non-coherent modulation, which the RF2905 provided in the form of frequency shift keying (FSK). The RF2905 was ordered as an evaluation board because it has all the external circuitry required for using the component in the 900MHz band. To operate the transceiver, the user selects the configuration with jumpers, and supplies power and data at the appropriate levels.

The exact transmit and receive frequencies are a function of the reference crystal (on the evaluation board) and the dual modulus/dual divide prescaller (128/129 or 64/64) in the RF2905 transceiver [2]. Setting the prescaller to 128 with reference crystal frequencies of 7.07549MHz and 7.15909MHz, a transmit frequency of 905.663MHz, and a receive frequency of 916.363MHz, are obtained. The IF filter used on the evaluation board has a center frequency of 10.7MHz and a bandwidth of 180kHz, which determined the maximum frequency deviation possible for the POCP. The 915MHz ISM band imposes a limitation of 10dBm (10mW) for the maximum transmitted power, and the transceiver has a 20 dB power control range, which can reduce the transmitter output power to –10dBm. Using a quarter wave whip antenna (gain of 0dB) the transmitter power is then equal to the radiated power.

2.2 Encoding Schemes

For FSK, the modulation rate must be greater than the phase locked loop bandwidth (PLL). If the PLL bandwidth is too wide, long strings of zeros or ones can be tracked out by the PLL, resulting in error [1]. For the RF 2905 evaluation board, it

was determined that the PLL bandwidth could not be made low enough to overcome the problem; therefore the data rate had to be increased.

2.2.1 Manchester Encoder

Manchester encoding is one way to increase the data rate without bit-stuffing. Bit stuffing is the process of adding bits to the data stream in order to ensure that no long strings of ones or zeros are sent to the modulator. Manchester encoding generates two symbols for each bit transmitted, therefore ensuring transitions during long one or zero strings. Two main problems exist with Manchester encoding; the necessary hardware is expensive (around $15.00/chip) and synchronization between the transmitter and receiver is required.

Manchester Encoding is used to convert non-return to zero (NRZ) data to return to zero (RTZ) data, thus ensuring a transition for each data bit. When using NRZ the signal does not return to a zero state before each data one in a sequence; the signal stays high for the complete period of all consecutive ones. For Manchester encoding the direction of the transition indicates the binary data value. A logic-0 is defined as a low-to-high transition in the middle of the bit period and a logic-1 is a high-to-low transition. Figure. 2.1 shows the timing diagram relationship for the two schemes.

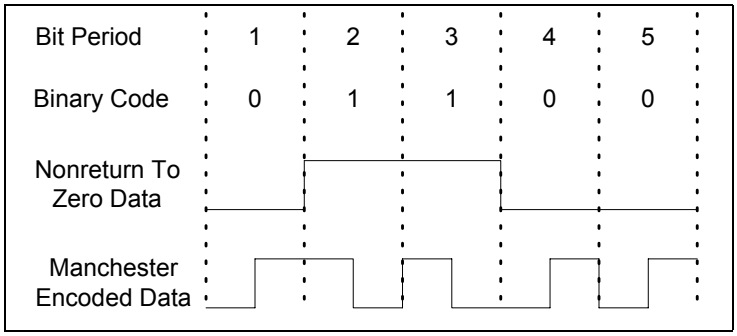


Figure 2.1 Manchester Encoder

Manchester is the standard encoding scheme used for the 802.11 wired LAN systems and has a data rate of 10 Mbits/second, which exceeds the transceiver maximum modulation frequency of 2 MHz. This caused a problem with locating a usable

component since most manufactures produce components to run at the 802.11 rates and they cannot be changed by the user. Harris Semiconductor designed the HD6409 to operate at a user-selected data rate set by selection of the clock input. In addition, the Harris part was one of the lowest cost Manchester encoder/decoder components evaluated. For these reasons the DH6409 was selected for the POCP.

The data rate is determined by the setting of the HD6409 clock, and the peak deviation for the FSK transceiver is determined by the peak amplitude of the data signal driving the RF2905 modulator. The baseband data from the SMU is 9600 baud and the HD6409 is used to sample that data. The minimal sample rate to satisfy the Nyquist criteria is 19.2kHz. Trial and error showed that a four times oversampling rate, or a 38.4kHz clock, produced acceptable results in a wired test. Increasing the sample rate beyond this value did not increase the performance of the link. Using a crystal already on hand resulted in a sampling rate of 43.2kHz. For an IF bandwidth of 180kHz the peak deviation cannot exceed one-half the bandwidth, or 90kHz. This is shown using Carson's rule.

$$B_{IF} = 2(\Delta f_{pk} + f_{\max})$$

Setting B_{IF} to 180kHz and f_{max} to 43.2kHz results in Δf_{pk} being 46.8kHz which is well within the IF filter specifications [6].

2.2.2 Digital Logic Encoder

Due to the high cost to the Manchester Encoder, an alternative encoding scheme was desired. Alternate Mark Inversion (AMI) is a synchronous encoding technique that uses bipolar pulses to represent logic one and no symbol for logic zero [5]. A low-cost derivative of this uses standard logic gates and timers, here referred to as Digital Logic Encoding (DLOC). DLOC is similar to AMI except that AMI is synchronous, and uses bipolar pulses to represent logic one. DLOC is non-synchronous, and uses unipolar pulses at the sampling frequency to represent logic one. The sampling frequency (43.2kHz) was maintained so the two encoding schemes could be compared. Figure 2.2 shows how AMI and DLOC differ for logic one and are the same for logic zero.

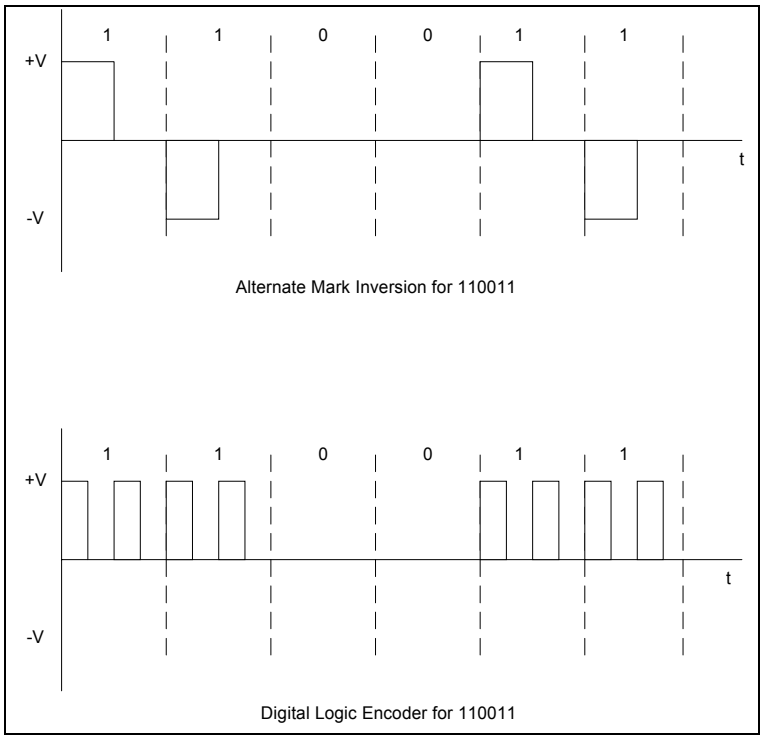


Figure 2.2 AMI/DLOC timing

Chapter 3 WDL Detailed Design

The complete WDL consists of three main parts: the digital interface (DIF), an RF transceiver and a data source. The DIF board is custom designed, and contains the encoding/decoding circuitry and electronics to interface the data unit with the transceiver. A modified RFMD 2905 is used for the transceiver, and the sponsor supplied the data source.

3.1 Digital Interface Board

The DIF board provides an interface between the SMU and the RF2905 transceiver. The three main functions are:

- Using the TX/RX (transmit/receive) control line from the SMU to set the DIF board and RF2905 in the proper mode of operation (TX/RX).
- In transmit mode, receiving data from the monitoring unit, encoding the data, perform level adjustment, and send the data to the transceiver for transmission.
- In receive mode, decoding the received data and sending it to the monitoring unit.

The design of the DIF board was completed in two stages. The first stage (initial design) consisted of construction of the SMU interface circuitry, TX/RX control, and Manchester encoder circuitry. The second stage was to add the DLOC circuitry and associated jumpers to select the mode of operation.

3.1.1 TXON and TXOFF Delay

In an RS485 application, the data is transmitted without any precursor. This works well for wired systems, but when a half-duplex wireless link is added, delays are required for the transceiver to change from TX to RX or vice-versa. The delay allows time for the RF2905 reference crystal oscillator and PLL to settle when the transceiver is switched from RX to TX or TX to RX, and for synchronization, when using Manchester Encoding. Two time delays are used in the SMU software and are configured through

the COM port using a standard PC terminal program. The TXON delay is the amount of time between the SMU setting the TX_RX_CTRL line high (transmit) and sending the data to the DIF board. The TXOFF delay is the amount of time between the SMU sending the data to the DIF board and setting the TX_RX_CTRL line low (receive). Table 3.1 shows the settings that were found to be best for the RF2905 evaluation board.

Table 3.1 Software Delay

Delay Parameter	Delay in ms
TXON	50
TXOFF	10

3.1.2 Stage One - Interface Electronics and Manchester Encoder

The SMU was scheduled for production before the decision was made to incorporate a wireless system. Consequently, no major hardware modifications could be made to the SMU to accommodate a transceiver, only slight software changes. The transceiver connection had to be transparent. This meant that the monitoring units could be connected via either a wired or wireless link. The SMUs did not require reconfiguration, and operated the same in both situations. A block diagram of the interface and Manchester encoder connections is shown in Figure 3.1.

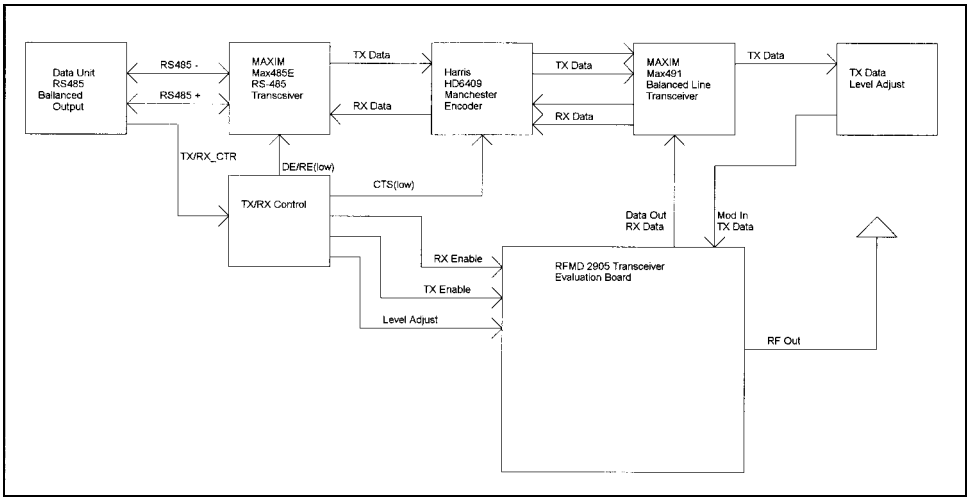


Figure 3.1 Detailed Block Diagram

The first challenge was converting the data from balanced RS485 to a single-ended, unbalanced line. A Maxim Max 491 (half-duplex RS485 to serial converter), was selected for this purpose. Another interface problem was that the WDL required a TX/RX control line and delays (TXON TXOFF), but they did not exist for the RS485 link. The control line is needed to select the mode of operation of the DIF board and transceiver as either transmit or receive. In addition, the RF2905 needs time for the PLL to lock when the state is changed from transmit to receive or vice-versa. The sponsor's existing system had an extra output pin that was used for a control line that could be configured for the delay using software (Chapter 3.1.1).

The Manchester Encoder circuit was included in this stage of design. The implementation required very little design work except for the 555-timer delay circuit: timing and synchronization are already incorporated in the HD6409 integrated circuit. To demonstrate operation of the transceiver in the Manchester mode, a detailed description of a complete cycle of a master's request for data and the slave's response follows. While reading the description, the parts layout in Appendix B, the schematic in Appendix A, and the timing diagram in Figure 3.4 should be referenced.

Upon initialization, both the master and slave WDL units are in RX (receive) mode due to the low setting of the TX_RX_CTRL line. When the master requests data from the slave, it sets the TX_RX_CTRL line high. Component U4 (74123 timer) is triggered, and outputs a 30ms DELAY pulse. The high on the TX_RX_CTRL line switches the RF2905 to TX mode, and the U1 (Max 485) RE and DE line is pulled low to set the RS485 line driver/receiver into receive mode. The 30ms delay allows time for the transceiver to settle before any data is transmitted. When the delay pulse ends, the CTS line on the U2 (HD6409 Manchester Encoder/Decoder) goes low and the synchronization sequence begins (Figure 3.2). See the Harris HD6409 data sheet for more details.

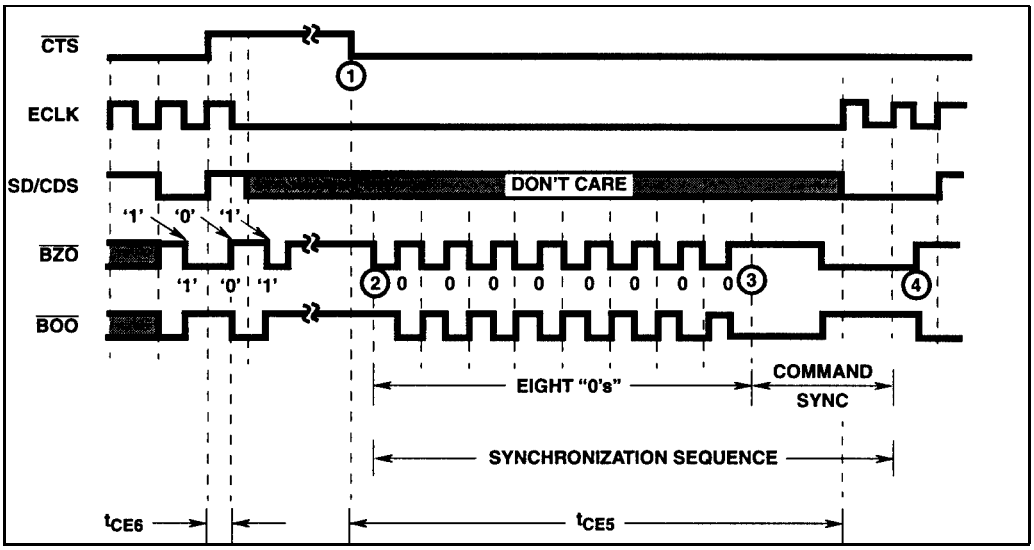


Figure 3.2 Manchester Synchronization Sequence

The delay pulse length (30ms) plus the synchronization sequence time are less than the TXON delay (50ms), thus ensuring that the data from the SMU is sent after the synchronization sequence. The SMU data is received by U1, converted from RS485 to single-ended, and input into U2 on the SD/CDS pin, where it is sampled at 43.2KHz by U2 and converted to Manchester Encoded data. This data is then output on the BOO and BZO lines and converted to a single-ended line by U3. The amplitude of the data is adjusted by R11 and connected to the Modulation Input of the RF2905, where it modulates the VCO carrier frequency with ±50KHz deviation. After the data has been transmitted and after a TXOFF delay of 10 milliseconds, the master returns to receive (RX) mode to wait for a reply from the slave.

The slave unit in receive mode is waiting for a request for data. As the master transmits, the slave is receiving and the detected signal is taken from the DATA_OUT pin on the RF2905, passed through U3 (pin DI) and converted to a balanced line (U3 Y Z) that is connected to U2 (BOI and BZI). The slave U2 (HD6409 Manchester Encoder/Decoder) first synchronizes with U2 (master) using the synchronization sequence. Once synchronized, the received data can be properly decoded. Figure 3.3 shows UDI (unipolar data input) instead of the bipolar input, but the concept is exactly the same.

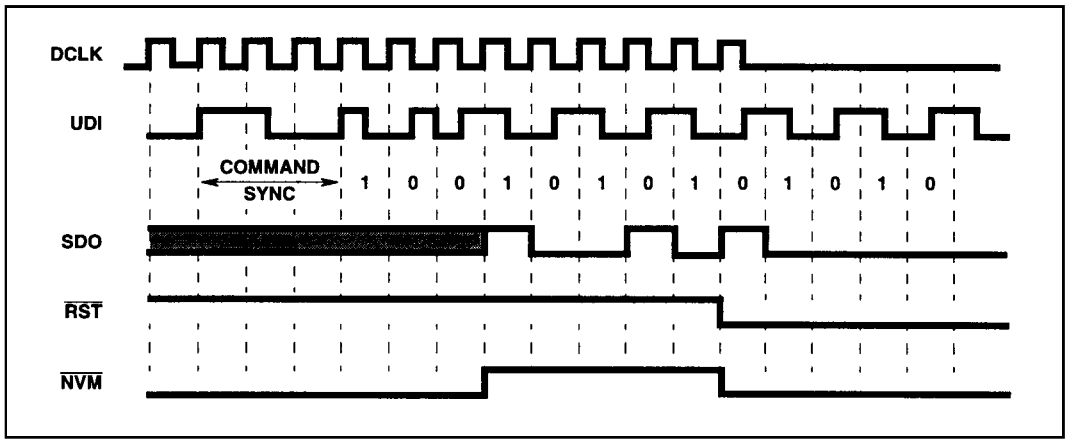


Figure 3.3 Manchester Decoder Sequence

The decoded data is sent out U2 (SDO) to U1 where it is converted to RS485 and transmitted to the slave data unit which decodes the request for data. If the requested slave address matches the slave address, the slave replies. The reply sequence follows the same process as the request for data sequence, except the slave now transmits the data while the master receives.

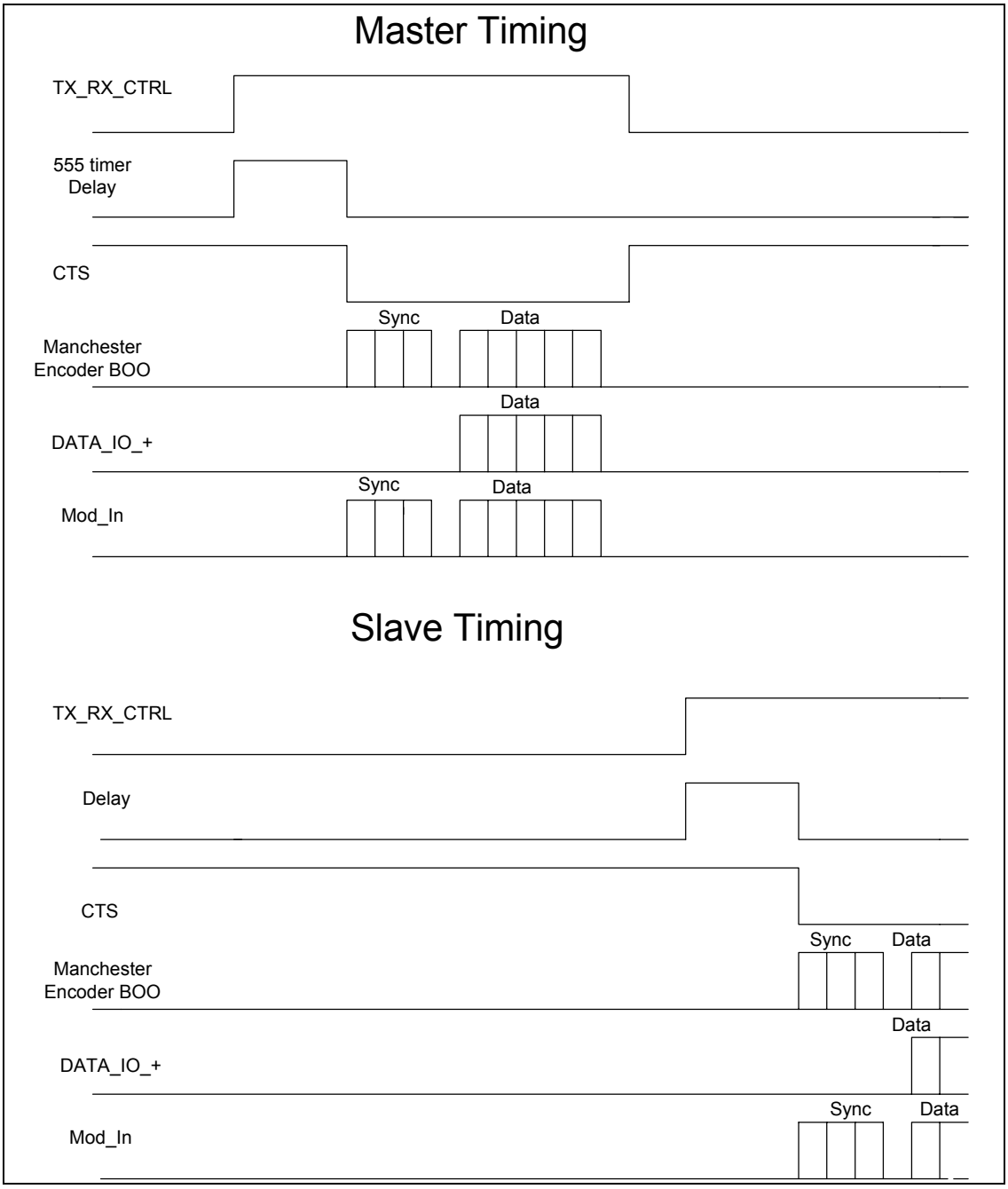


Figure 3.4 Master/Slave Timing Sequence

3.1.3 Stage Two DLOC

When comparing two different circuits for performance issues, it is best to change only one thing at a time, making is simple to conclude the cause of increase or decrease in performance. In keeping with this strategy, the clock output from the Manchester Encoder was used as the clock for the DLOC, thus keeping the sampling

rate the same. In Figure 3.5, one input to the AND gate is the data, while the other is a clock. When the data to be transmitted is high, the AND gate output is the clock, and, when the data is low, the output is low. To decode the data a TTL one-shot, configured to be re-triggerable, with a pulse width slightly longer than the sampling clock, is employed. When the sampled data input to the one-shot is a "1", consisting of N clock pulses, it triggers and continues to re-trigger the one-shot, resulting in an output "1" of length N clock pulses. The addition of up to one pulse width can occur to the output "1" data, thus extending its width to be greater than the transmitted data (Figure 3.6).

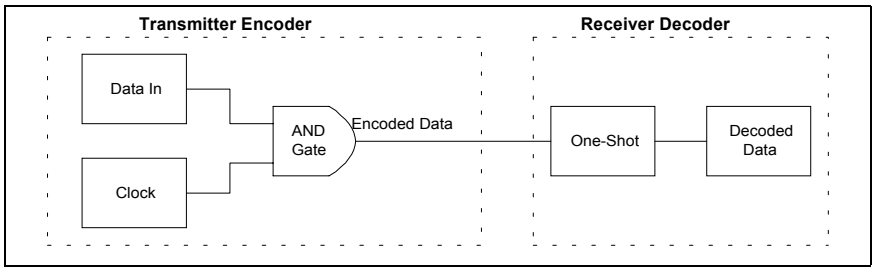


Figure 3.5 DLOC Block Diagram

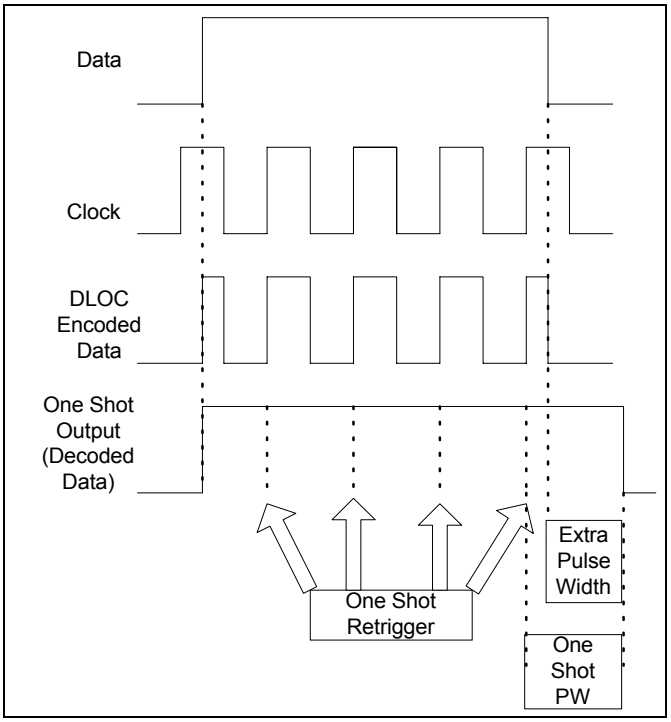


Figure 3.6 DLOC Decoder Timing

Verification of the digital portion of the DLOC was done with Microsim Psipce®. The circuit was simulated as shown in Figure 3.7. Two simulations were performed, one with the data and clock synchronized, and one with them un-synchronized. The plots in Figures 3.8 and 3.9 show the results of the simulation. Both plots are for an input data stream of "101010….". For both cases the decoded data matches, with the exception of the extra pulse width of ≈ 15µs. For the 9600-BAUD asynchronous communications this "jitter" does not seem to have any effect on the wired or wireless digital communications. For the un-synchronized simulation, the decoded data was correct with the "jitter" still around 15µs.

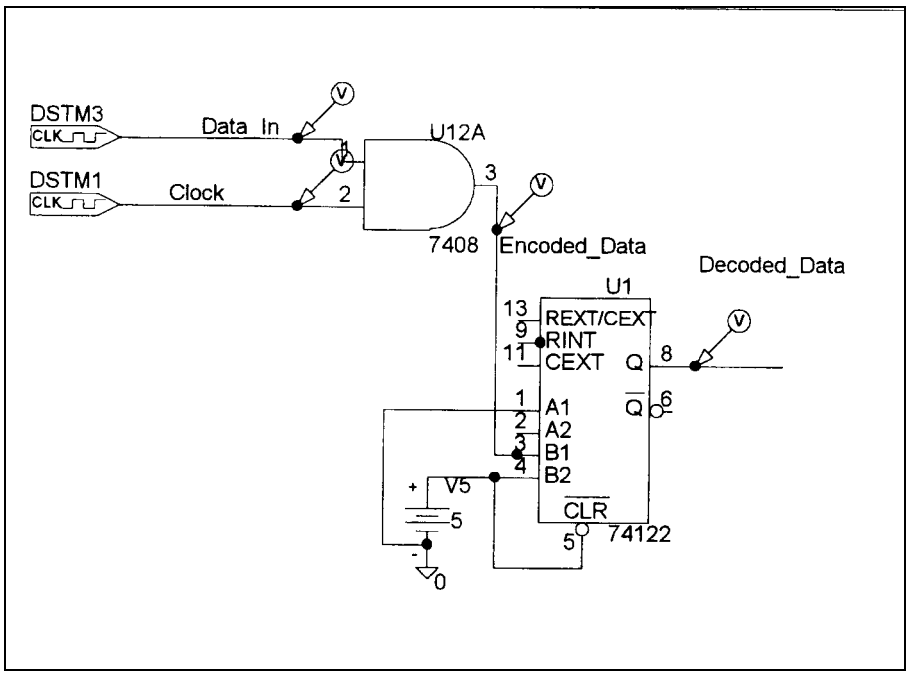


Figure 3.7 DLOC Simulation Circuit

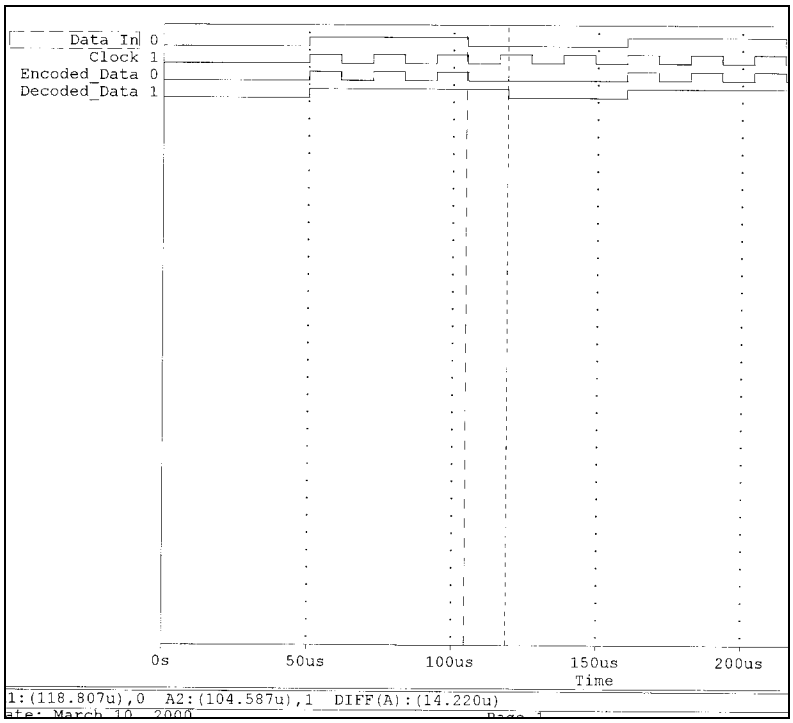


Figure 3.8 DLOC Simulation Results (Synchronized)

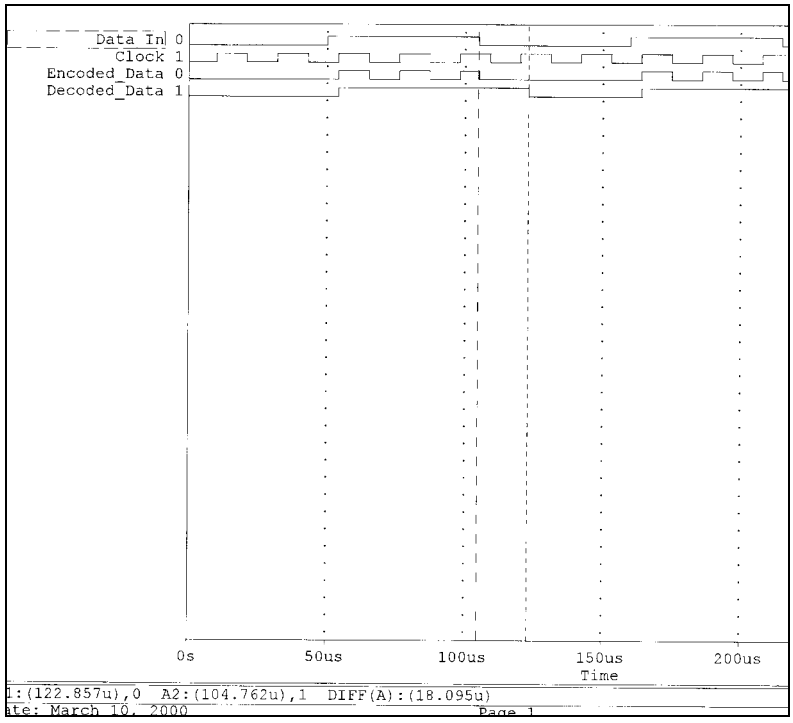


Figure 3.9 DLOC Simulation Results (Unsynchronized)

To implement the DLOC in conjunction with Manchester Encoding, logic gates and jumpers were added to the DIF board. Figure 3.10 shows the additional circuitry for the DLOC; a complete schematic appears in Appendix A.

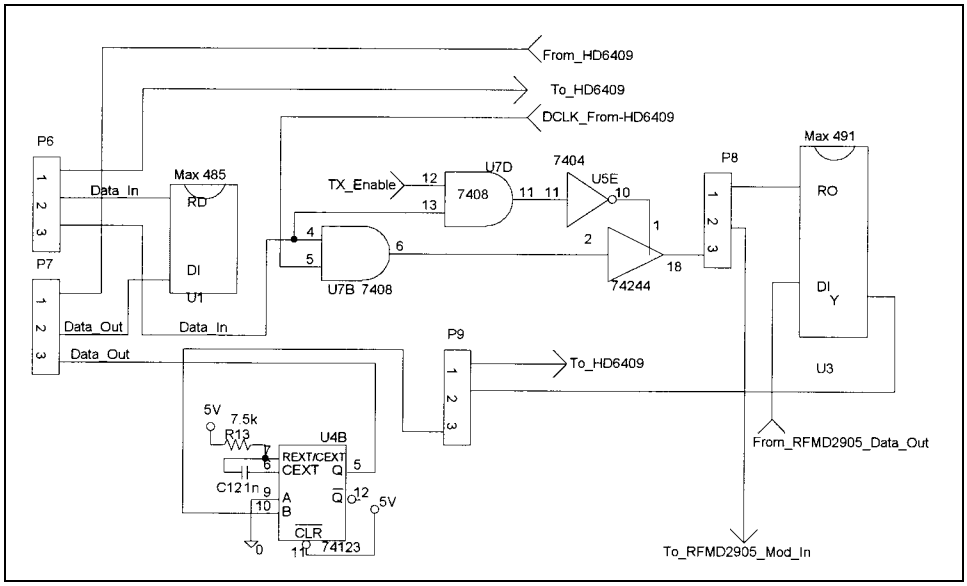


Figure 3.10 DLOC Circuit Implementation Schematic

To explain the DLOC operation, a description of the transmit data path is detailed here, referencing the schematic in Appendix A. The delay and TX/RX Control work the same as the Manchester Encoder (except that there is no synchronization sequence) and therefore will not be explained again. The data from the SMU is converted from a balanced to a single-ended line by U1, and sent to one input of AND gate U7B, while the decoder clock (DCLK/U2), used as the sampling clock, is connected to the other input. The AND gate samples the data at the clock frequency of 44.205KHz, and the sampled data is passed through U10, a tri-state buffer. ANDing the data with the TX_ENABLE line and inverting controls the buffer state, high impedance or buffer, results in the sampled data being passed when the data and TX_ENABLE are high. When the data is low the buffer is high impedance; i.e., no data is passed. R11 is used to adjust the level of the data into the VCO to obtain the proper frequency deviation of the carrier. A data high is transmitted using FSK with a deviation of 85KHz, while an undeviated carrier represents a data low. In addition, R14 and R15 apply a DC bias such that when the data is low (U10 high impedance), a fixed voltage is applied to the VCO

(modulator), thus only a carrier is transmitted. Figure 3.11 shows the clock in the upper trace and the sampled data in the lower trace. The DC offset during a data low is noticeable in the lower trace.

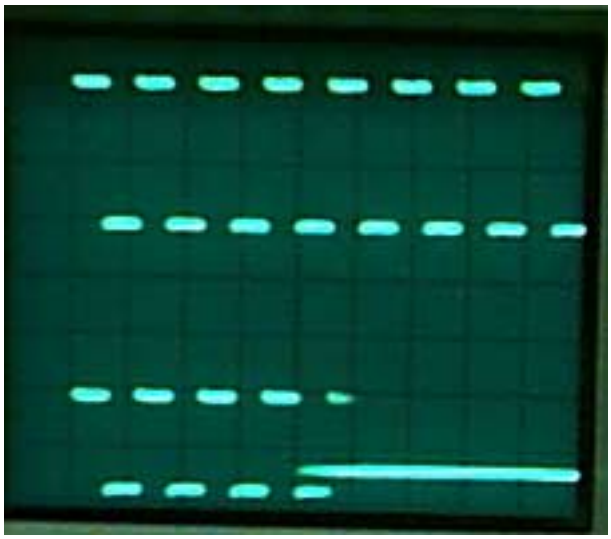


Figure 3.11 Clock and Sampled Data

The receive path begins with the Data Out from the RFMD2905 being driven into the balanced line driver U3. The positive signal (Y) from U3 is connected to the timer U4B, which is configured to be re-triggerable. The pulse width of the one-shot is 25μs, which is slightly longer than the clock frequency of 44.205KHz (22.62 μs). When a string of pulses is received, corresponding to a transmitted data of "1", the one shot is triggered and continues to be re-triggered until the pulses end. The Q output of the one shot is a high as long as it is being re-triggered resulting in a "1". This detected "1" is close to the transmitted "1" with a maximum error of one pulse width of 25μs. Since the data rate from the SMU is fixed at 9600 BAUD, the higher the sampling clock the smaller the error. When a "0" is transmitted, only the carrier is received and the Data Out is low. A constant low does not trigger or re-trigger the one shot, and the Q output goes low. The one shot output is connected to line driver U1 that transmits the data to the SMU.

3.1.4 Jumpers

In order to test the WDL using both encoding schemes, several jumpers had to be included on the DIF board. Table 3.2 details the jumpers and their settings. Jumpers P3 and P4 provide control of the transceiver unit, while jumpers P6-P9 are used to select the mode of operation. As an example, to set the unit to DLOC mode, jump pins 2-3 on jumpers P6-P9 and to set to Manchester Encoder mode, jump pins 1-2 on jumpers P6-P9.

Table 3.2 DIF Board Jumper Configurations

Jumper	Settings
P3-TX Level Adjust	*jump 1 to 2*=Max RF power output (≈ +10dBm) *jump 2 to 3*=Min RF power output (≈ -10dBm)
P4-TX/RX pull-up resistor	*jump 1 to 2*= TX_RX_CTRL grounded, WDL in RX mode if data unit *jump 2 to 3*= TX_RX_CTRL pulled high, use this configuration when WDL connected to data unit and to put WDL in TX mode when data unit not connected.
P6-Receive Data From U1	*jump 1 to 2*=Manchester Encoder *jump 2 to 3*=DLOC
P7-Transmit Data to U1	*jump 1 to 2*=Manchester Encoder *jump 2 to 3*=DLOC
P8-Transmit Data to RFMD2905	*jump 1 to 2*=Manchester Encoder *jump 2 to 3*=DLOC
P9-Positive Channel of receive data from U3	*jump 1 to 2*=Manchester Encoder *jump 2 to 3*=To DLOC

3.2 RFMD 2905 Evaluation Board

A RFMD2905 transceiver evaluation board provides the system's RF channel. The RF2905 was selected because it is designed for use in the 900MHz ISM band using FSK modulation. Several minor modifications were required to the evaluation board to complete the WDL.

3.2.1 Jumpers

The RF2905 evaluation board comes with several I/O (input/output) pins, which enable the user to configure the transceiver for different modes of operation, as well as to control some functions of the RF integrated circuit (RFIC). To decrease the number of connections between the DIF and evaluation board, a single mode of operation was selected and jumpers were added to maintain this setting. Figure 3.12 shows the physical jumpers and Table 3.3 details the operational state.

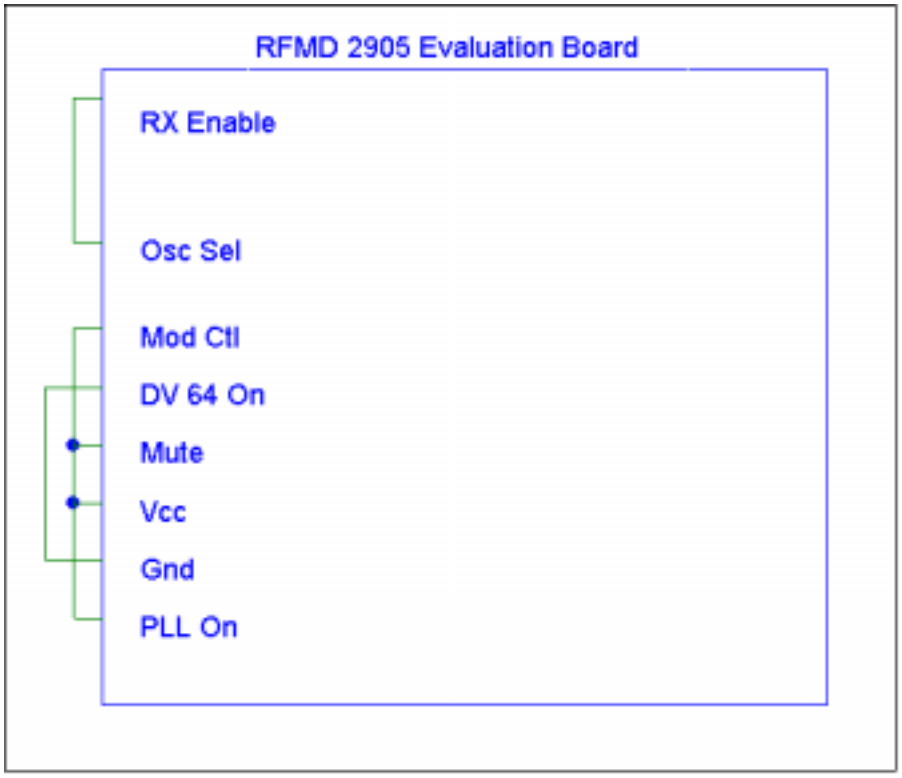


Figure 3.12 RF2905 Evaluation Board Jumpers

Table 3.3 RF2905 Evaluation Board Configuration

RF 2905 Function	Description as Configured
RX Enable	Receiver enable-=Follows the RX enable line from the interface board RX Enable>2.0V = Receive enable RX Enable<1.0V = Receive disable
Osc Sel	Selects the proper oscillator for RX and TX. Follows the RX enable line Osc Sel>2.0V=Ref osc 2,RX Osc Sel<2.0V=Ref osc 1,TX
Mod Ctl	Selects the prescaler modulus. Connected to Vcc to select 128 divisor
DV64 On	Select prescaler divisor(64/65 or 128/129) Connected ground to select 128/129
Mute	Mutes Data Out. Connected to Vcc to select Data Out on (not muted)
PLL On	Enable phase locked loop. Connected to Vcc to keep PLL enabled.

3.2.2 Crystal Oscillator Modifications

Recall that DLOC transmits a FSK signal for a data one, and a carrier only for a data zero. A data zero means that the VCO is at its free running frequency determined by the crystal, its external components, and the PLL. Depending on the transmitter/receiver pair, the transmitter's free-running frequency could be detected by the receiver as either a data high, data low, or somewhere in the transition region. To correct this problem, the crystal oscillator frequency either of the transmitter, receiver, or both, had to be adjusted. Since the extent of the problem depends on the TX/RX pair, a single unit was labeled as the master and the two others as slaves, to make the adjustments easier.

Figure 3.13 shows the RF2905 evaluation board schematic having 0 ohm resistors (R1 and R2) to ground from the TX and RX reference crystals. By replacing the resistors with either capacitance or inductance, the crystals' free running frequency could be increased or decreased without degrading the performance of the circuit.

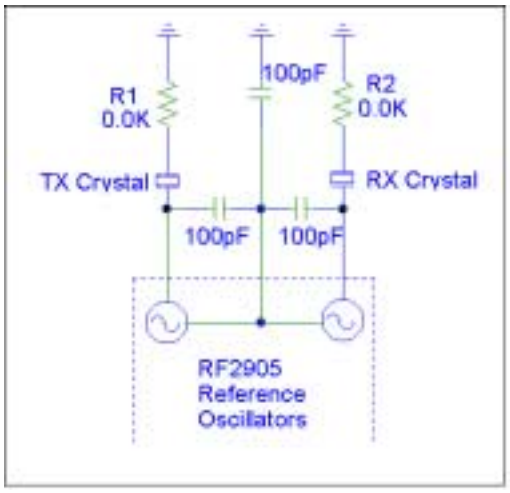


Figure 3.13 RF2905 Crystal Oscillator

Two measurements were required to determine the evaluation board modifications. These were (a) the transmitter frequency of each unit and (b) the receive frequency range for which the detector produced a low, high or transitional output. Measurement of the transmitter frequency was accomplished by connecting the RF2905 RF output to an HP8594E Spectrum Analyzer and using the frequency marker counter function. To determining the detector output range a HP8648C Signal Generator set to –70dBm (RF output) was connected to each transceiver evaluation board in receive mode. Tuning the signal generator frequency across the receive band and monitoring the RF2905 Data Out port produced the data in Table 3.4.

Table 3.4 Data High/Low Frequency Before Modifications

WDL	Transmit	RX Freq (MHz)				
Function	**Freq(MHz)**	**Data Out High Range**		**Transition Region**	**Data Out Low Range**	
Master	905.6494	905.4075	905.5945	905.5950-905.6325	905.6330	905.7450
Slave-1	905.6253	905.4550	905.6060	605.6065-905.6355	905.6360	905.7445
Slave-2	905.6162	905.4680	905.6480	905.6585-905.6675	905.6680	905.7680

By comparing the master TX Frequency with the Data Out (High or Low*)* range of each slave, one can see that a master transmitted carrier would produce a low data out for slave-1. The data would be in the transition region, and thus would produce neither a good low nor a good high output for slave-2. Comparing each slave TX frequency with the master RX frequency, it can be seen that the master RX detected data output from both slave units is in the transition region. Trial and error was used to determine the exact component values required for each evaluation board. Table 3.5 details the modifications required to produce the TX frequency change and RX frequency range shift.

Table 3.5 Crystal Oscillator Modifications

Crystal Oscillator Modifications		
WDL	TX Crystal	RX Crystal
Function	7.075945MHz	7.14159 MHz
Master-1	None	None
Slave-2	150pF	None
Slave-3	4.7uH	None

The modified evaluation boards were again tested to verify test results (Table 3.6). Comparing the TX and RX frequencies verifies that a carrier transmitted from the master to any slave, and from any slave to the master, produces a low detected data output. The changes are specific to each evaluation board and POCP, but this frequency offset can be designed into the circuit for a production unit.

Table 3.6 Data High/Low Frequencies After Modifications

WDL	Transmit	RX Freq (MHz)				
Function	**Freq(MHz)**	**Data Out High Range**		**Transition Region**	**Data Out Low Range**	
Master-1	905.6494	905.4075	905.5945	905.5950-905.6325	905.6330	905.7450
Slave-2	905.6380	905.4480	905.6080	905.6085-905.6325	905.6330	905.7430
Slave-3	905.6394	905.4395	905.6195	905.6200-905.6390	905.6395	905.7345

Chapter 4 WDL Operation and Verification

Once the WDL was designed and built, the operation and verification of the POCP was performed. Testing of the WDL was an ongoing process during system development. All stages of testing will not be discussed in the thesis; only testing that impacts its use will be presented. The testing was done in stages to ensure that each individual circuit operated correctly before testing the complete WDL.

4.1 Connection and Start Up

Since these are POCP units they have not been designed for mass production and require manual control and configuration for the start up procedure. In order for the WDL to work correctly the following procedure must be followed for connection to the SMU:

1. Turn off the SMU and WDL units.
2. Jump pins 2-3 on P4 on the WDL (see Table 3.2).
3. Connect the Universal Serial Bus (USB) and TX/RX CTRL lines from the SMU to the WDL unit.
4. Turn on the SMU.
5. Wait for the initial opening message to be displayed on the monitoring unit. At this time turn on the WDL unit.

This procedure must be followed to ensure that the WDL is not turned on while in the transmit mode. If turned on in the TX mode, data will be driving the modulation input (VCO) and the RF2905 may not be able to lock to the correct TX frequency.

In addition, each unit is matched with respect to the RF2905, the DIF board, and the enclosure. All individual sub-units are marked with the same serial number so that they can be kept together as a single unit when assembled. Failure to do this will alter the transmitter deviation controlled by the modulation-input level from the DIF board. If this occurs, the modulation level will then have to be readjusted as described in Modulation Level Adjustment, Chapter 4.2. The modulation level will also have to be adjusted when switching between the two modes of operation, DLOC or Manchester.

4.2 Modulation Level Adjustment

Resistor R11, labeled Mod Level on the outside of the enclosure, adjusts the modulation level. The following procedure is recommended to adjust the level for a two-unit set up:

1. Set the unit to be adjusted in TX mode by disconnecting the TX/RX control line and jump P3 from pins 2 to 3. Check to be sure that the TX ON light is lit.
2. On the receive WDL unit, disconnect the data unit and jump P3 from 1 to 2. Connect an oscilloscope to P1_3 (data out).
3. While adjusting R11, monitor the scope to obtain the best square wave possible.
4. Reverse the unit's roles (TX/RX) and repeat steps 1-3.

4.3 WDL Verification

Verification of the WDL was performed in five stages.

- Stage one: Produced a table of the receiver's received signal strength indicator voltage, versus received power.
- Stage Two: Tested the Manchester Encoder without the RF2905
- Stage three: Tested the complete WDL using the Manchester Encoding scheme via a wired RF connection
- Stage four: Tested the DLOC without the RF2905
- Stage five: Tested the complete WDL using the DLOC via a wired RF connection

A counter in the master SMU displays the number of requests for data (TX) and the number of times the requested data is received from the slave (RX). Since a one-for-one request and response is counted, the probability that the requested data will be received can be determined. This data can be used in conjunction with the RSSI measurement to determine the reliability of the link based on RSSI.

4.3.1 Received Signal Strength Indicator (RSSI)

The RSSI signal from the RF2905 gives an indication, in the form of a voltage, as to the strength of the received signal in dBm. In order to evaluate the performance of the WDL, a table and plot of voltage versus received power was developed. The RF2905 evaluation boards come with this data, but it is for a CW (continuos wave) mode of operation. The test was done while transmitting data to obtain a better correlation between the RSSI and radio link performance. A wired (coaxial) set up was used for the testing to reduce the probability of outside interference (Figure 4.1). Switchable attenuators were used between the transmitter and receiver to adjust the received power level and create the table.

To get accurate data the test setup must first be calibrated. Calibration consists of measuring and recording the losses in the coax cable (Table 4.3), as well as the actual loss inserted by the attenuator for each selection (Table 4.1). This was required since the attenuators had not been calibrated in five or more years. In addition, the actual transmitter power levels were measured and recorded (Table 4.2).

Table 4.1 Attenuator Calibration

	Attenuator Calibration Data			
	KAY 341C Attenuator			
TE464520			**TE464520**	
Selected Atten	**Measured**		**Selected Atten**	**Measured**
dB	dB		dB	dB
1	0.7		1	1.35
2	2.45		2	2.07
3	2.84		3	3.13
5	4.95		5	5.03
10	9.68		10	9.59
20	20.23		20	19.58
Insertion Loss	0.38		Insertion Loss	0.63

Table 4.2 Transceiver Output Power

Measured Output Power of WDL				
WDL-1	**Pout dB**		**WDL-2**	**Pout dB**
Pout Max	8.32		Pout Max	7.1
Pout Min	-10.34		Pout Min	-10.85

Table 4.3 Test Cable Loss

Test Cable Loss (dB)	
Power Input	**7.1**
Atten Loss	-0.38
Pout out	6.11
Cable Loss	0.61

With calibration complete, the RSSI table (Table 4.4) was obtained using one RF2905 as the transmitter and one as the receiver. Although there will be slight deviation in the RSSI readings for different evaluation boards, this effect is minimal, and all boards' RSSI will be assumed equal for the testing purposes.

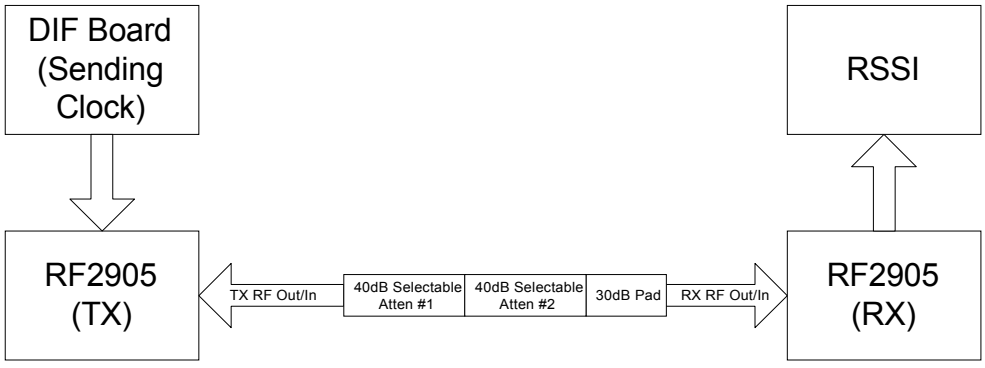


Figure 4.1 Cabled RF Test

Table 4.4 Manchester RSSI Calibration

	Received Power vs RSSI				
	Transmitting Manchester Clock				
	TX WDL 002 Min Pout				
	Fixed Attenuation				
		30			
	RX WDL 001				
Atten #1 (dB)	Atten #2 (dB)	Cable Loss (dB)	Total Atten (dB)	Received Power (dBm)	RSSI (V)
0	0	0.61	30.61	-40.95	2.499
4.95	0	0.61	35.56	-45.9	2.375
9.68	0	0.61	40.29	-50.63	2.233
14.63	0	0.61	45.24	-55.58	2.145
20.23	0	0.61	50.84	-61.18	2.061
25.18	0	0.61	55.79	-66.13	1.914
29.91	0	0.61	60.52	-70.86	1.687
34.86	0	0.61	65.47	-75.81	1.448
34.86	5.03	0.61	70.5	-80.84	1.288
34.86	9.59	0.61	75.06	-85.4	1.204
34.86	14.62	0.61	80.09	-90.43	1.095
34.86	19.58	0.61	85.05	-95.39	0.947
34.86	24.61	0.61	90.08	-100.42	0.723
34.86	29.17	0.61	94.64	-104.98	0.65
34.86	34.2	0.61	99.67	-110.01	0.608

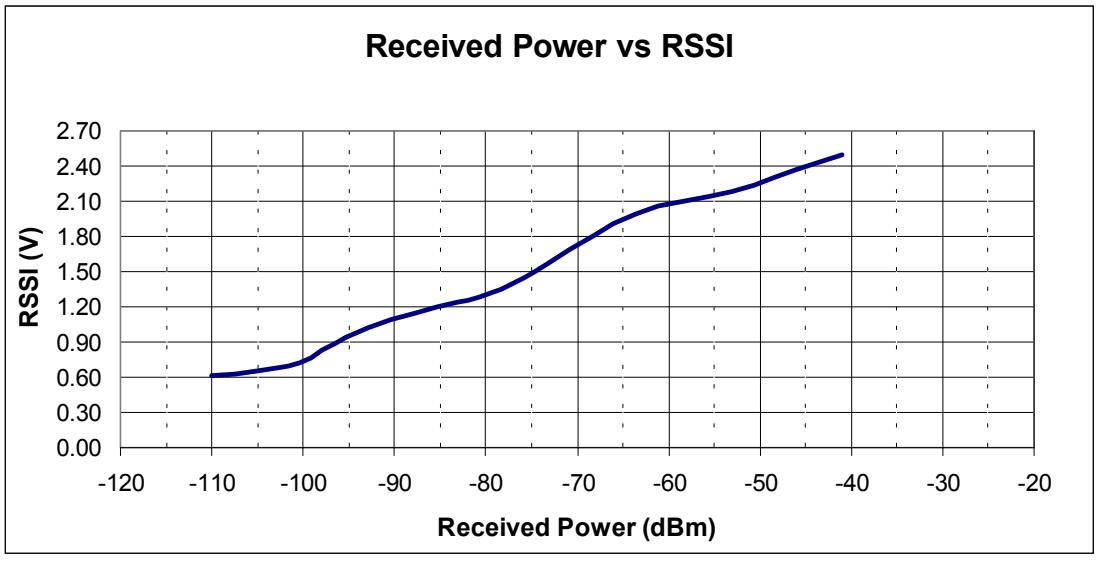


Figure 4.2 Manchester RSSI Calibration

4.3.2 Digital Circuit Verification-Manchester Encoder

The unique use of the Manchester Encoder to sample the incoming asynchronous data was tested in a wired system to ensure that no problems exist with the concept. To prove that the Manchester encoding worked correctly, the transceivers were not incorporated into the system. Two SMUs were connected through DIF boards and the DIF boards were connected via a wire to transfer the encoded data (Figure 4.3). The system was allowed to run overnight, resulting in 6315 requests for data (TX) and 6313 replies (RX), which yields a probability of 0.9997 (99.97%) that the requested data will be received.

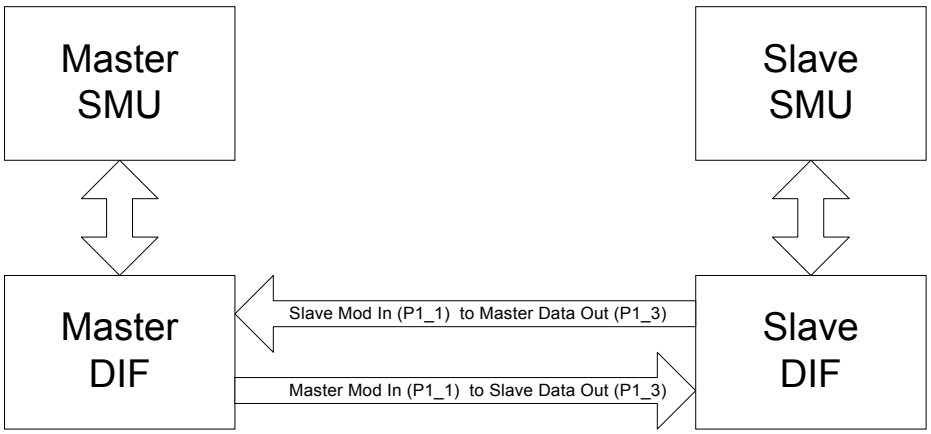


Figure 4.3 DIF Board Verification

4.3.3 Complete Transceiver-Manchester Encoder

With the encoding scheme circuit verified, the transceiver was added. The system was then subjected to further testing (Figure 4.4). Testing consisted of allowing 10 requests for data and recording the number of replies. The attenuation was then increased, and the test was repeated to obtain the data in Table 4.5. From the graph (Figure 4.5) it can be seen that a successful data transfer of 100% (probability of 1.0) occurred until a received power level of –85dBm was reached, which translated to an RSSI of around 1.2 volts (Figure 4.6). This relationship between the probability, received power, and RSSI can be used to determine the usable range of the WDL.

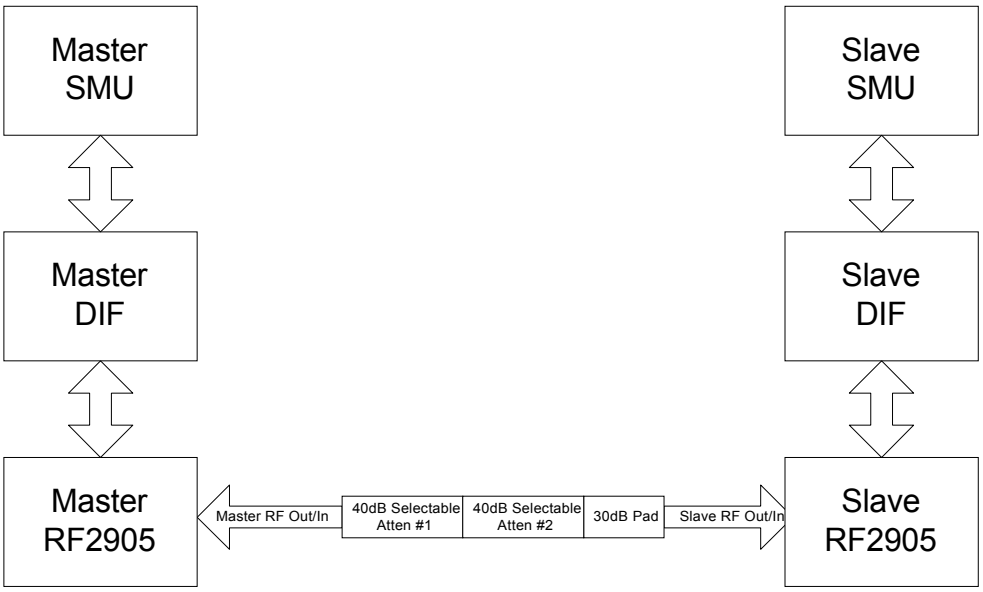


Figure 4.4 Manchester WDL Cabled Test

Table 4.5 Manchester Probability of Error

		Received Power vs Bit Error						
		Transmitting Manchester Data						
		TX=WDL S#002 Min Pout						
		Fixed Attenuation (dB)						
			30					
		RX=WDL S#001						ND=No Data
Atten #1	**Atten #2**	**Cable Loss**	**Total**			**Received**		
(dB)	**(dB)**	**(dB)**	**Atten (dB)**	**TX**	**RX**	**Poewr (dBm)**	**Prob**	**RSSI(V)**
0	0	0.61	30.61	10	10	-40.95	1.00	2.49
4.95	0	0.61	35.56	10	10	-45.90	1.00	2.38
9.68	0	0.61	40.29	10	10	-50.63	1.00	2.23
14.63	0	0.61	45.24	10	10	-55.58	1.00	2.14
20.23	0	0.61	50.84	10	10	-61.18	1.00	2.06
25.18	0	0.61	55.79	10	10	-66.13	1.00	1.91
29.91	0	0.61	60.52	10	10	-70.86	1.00	1.68
34.86	0	0.61	65.47	10	10	-75.81	1.00	1.45
34.86	5.03	0.61	70.5	10	10	-80.84	1.00	1.28
34.86	9.59	0.61	75.06	10	10	-85.40	1.00	1.20
34.86	14.62	0.61	80.09	10	8	-90.43	0.80	1.09
34.86	15.97	0.61	81.44	10	8	-91.78	0.80	ND
34.86	16.69	0.61	82.16	10	7	-92.50	0.70	ND
34.86	17.75	0.61	83.22	10	7	-93.56	0.70	ND
34.86	19.1	0.61	84.57	10	6	-94.91	0.60	ND
34.86	19.58	0.61	85.05	10	0	-95.39	0.00	0.95
34.86	24.61	0.61	90.08	10	0	-100.42	0.00	ND
34.86	29.17	0.61	94.64	10	0	-104.98	0.00	0.65
34.86	34.2	0.61	99.67	10	0	-110.01	0.00	0.60

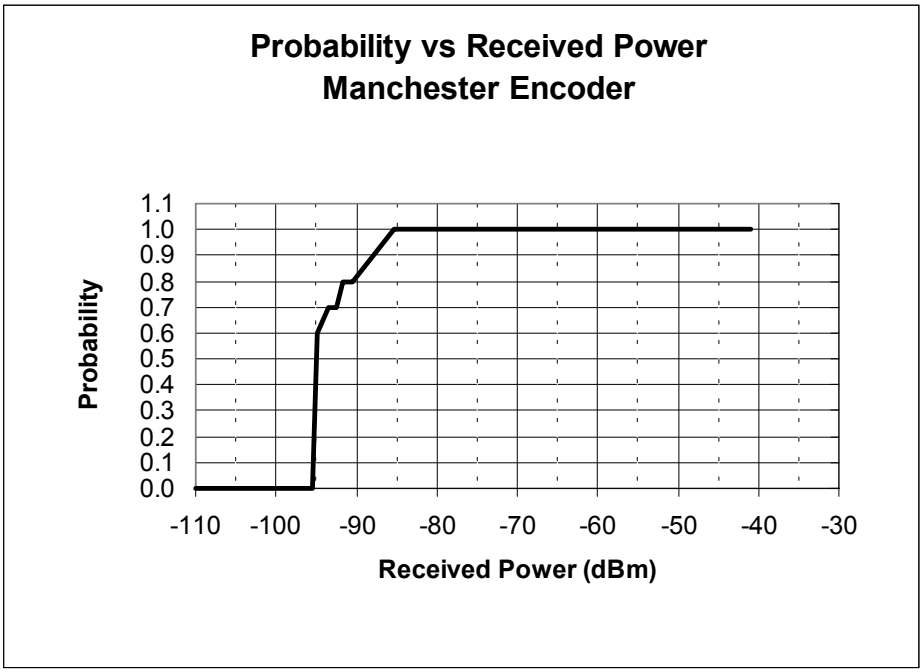


Figure 4.5 Manchester Probability of Error

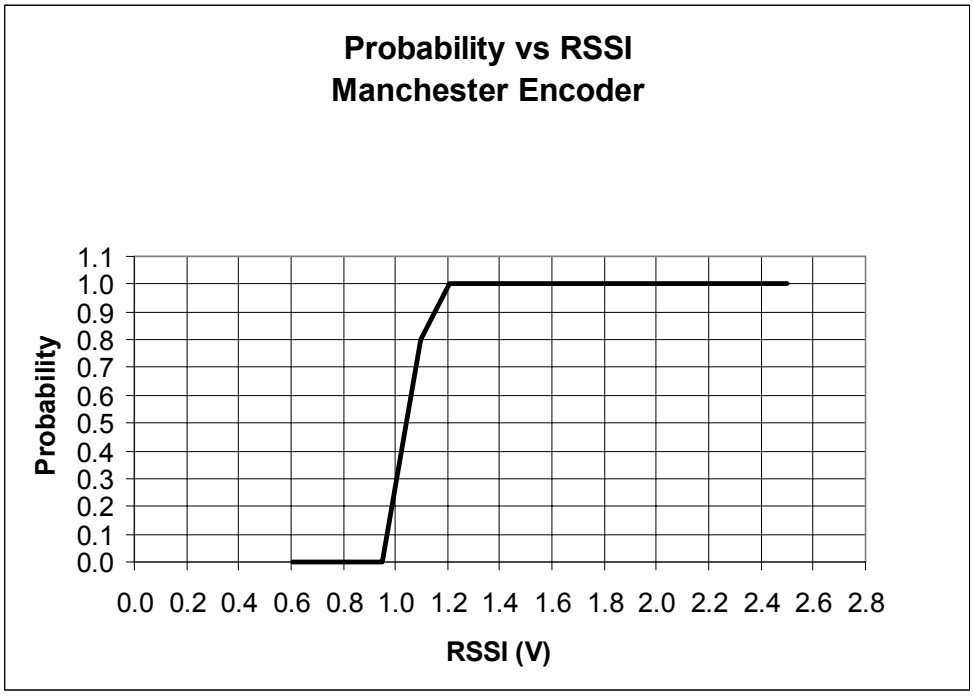


Figure 4.6 Manchester RSSI vs Probability of Error

4.3.4 Digital Circuit-DLOC

The SMUs and DIFs, configured for DLOC, were connected as shown in Figure 4.3 and the system was allowed to run overnight. There were 6,694 requests for data, and 6,678 successful replies, yielding a probability of 0.997 (99. 7%) that there will be successful data transfer.

4.3.5 Complete Transceiver-DLOC

Before connecting the transceivers to the SMU, a verification process using computer generated data was employed. This was necessary, because the SMU transmits a data packet that is difficult to capture on an oscilloscope. For comparision purposes both the the transmitted and received data need to be captured. The computer transmits a continuous stream of data from a file that can then be monitored at both ends (TX-RX) to ensure proper operation of the DLOC. A shareware program, COMHEX, was used to send the data stream. COMHEX is a DOS based program that allows the user to create a ASCII hex data file and send it out the serial port of a personel conputer. Figure 4.7 shows the interconnection for testing. The computer and a B&B Electronics 485TBLED RS232 to RS485 converter were used in place of the SMU during testing.

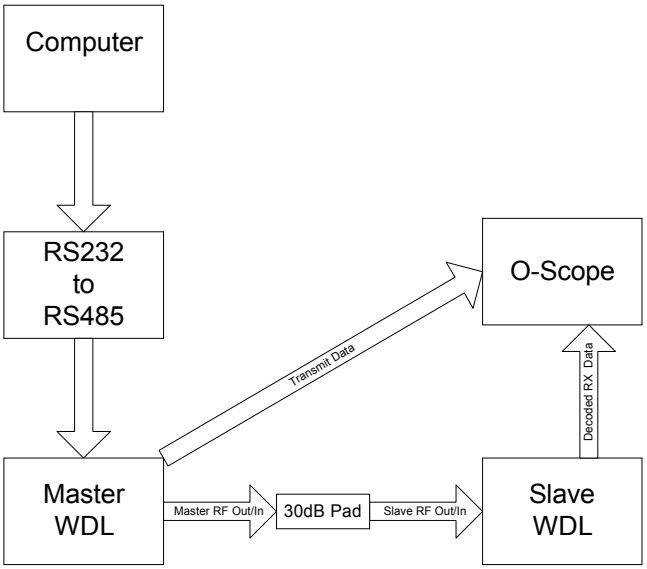


Figure 4.7 DLOC Verification Test Setup

For testing purposes data files consisting of the SMU's request for data sequence, all 0's and all 1's were created. The "0" and "1" files were to test the extreme limits of the DLOC, while the request for data sequence was a real world data stream. Figures 4.8 and 4.9 show the transmitted data in the upper trace and the received data in the lower trace. The right hand portion shows the same signal expanded in time so that the pulse width differences are noticeable. Figure 4.10 is the SMU's request for data sequence. In all three cases, the encoded transmitted data and decoded received data were equal.

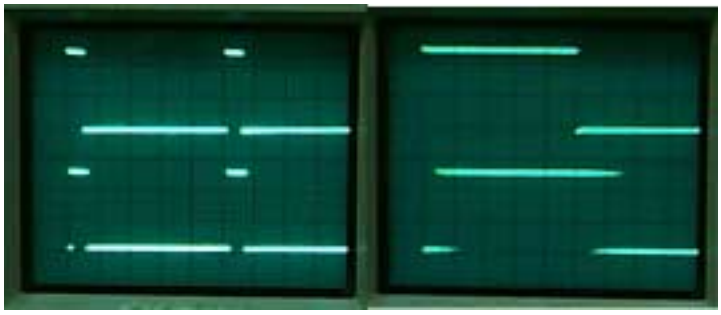


Figure 4.8 Test Data-Sending all zeros

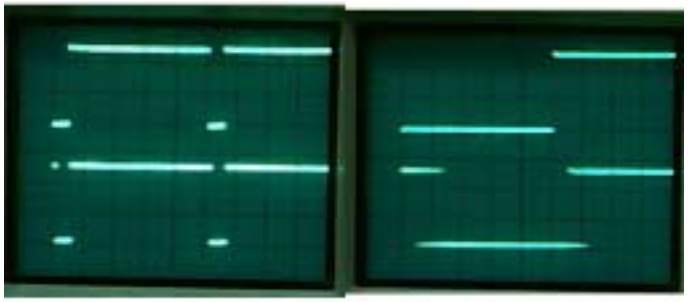


Figure 4.9 Test Data-Sending all ones

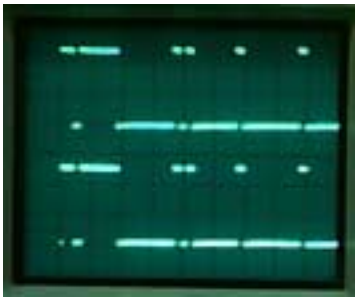


Figure 4.10 Test Data- Sending request for data sequence

Connecting the system on the lab bench as shown in Figure 4.11, the system was allowed to run overnight with a result of 6,386 requests and 5,745 successful replies. A probability of successful data transfer of 0.899 (89.9%) was obtained.

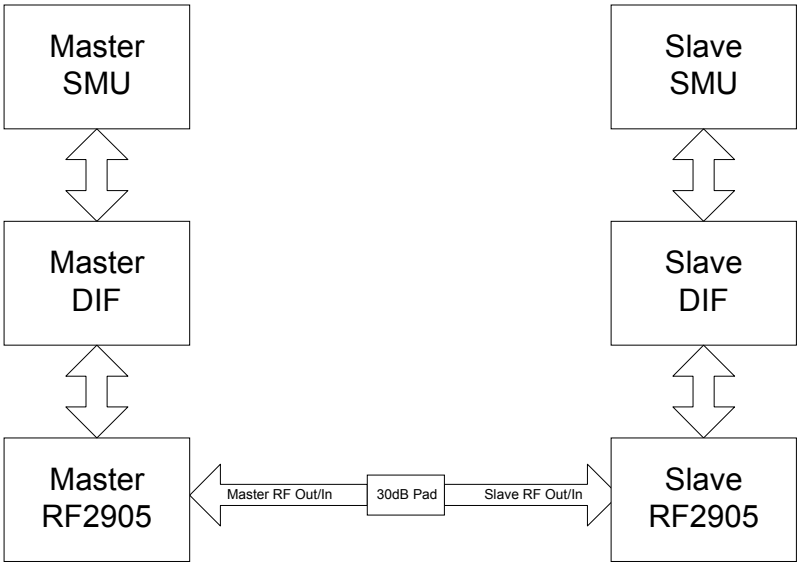


Figure 4.11 WDL Cabled RF Test Setup

A second wired test determined the sensitivity of the receiver with respect to data errors. The test setup in Figure 4.4 was used with the DIF boards set to DLOC mode; the test results are shown in Table 4.6. Figures 4.12 and 4.13 graphically show the results of the test. Performance of the DLOC shows the probability dropping from 1.0 at a received power of –78dBm and an RSSI of 1.4V.

Table 4.6 Transmitted Power vs Probability of Error

		Transmitted Power vs Bit Error						
			DLOC Data					
			TX=WDC S#001 Min Pout					
			Fixed Attenuation					
			20					
			RX=WDC 002					ND=No Data
Atten #1 (dB)	**Atten #2 (dB)**	**Cable Loss (dB)**	**Total Atten(dB)**	**TX**	**RX**	**Received Power (dBm)**	**Prob**	**RSSI(V)**
0	0	0.61	20.61	10	10	-30.95	1.00	
4.95	0	0.61	25.56	10	10	-35.90	1.00	
9.68	0	0.61	30.29	10	10	-40.63	1.00	2.49
14.63	0	0.61	35.24	10	10	-45.58	1.00	2.38
20.23	0	0.61	40.84	10	10	-51.18	1.00	2.23
25.18	0	0.61	45.79	10	10	-56.13	1.00	2.14
29.91	0	0.61	50.52	10	10	-60.86	1.00	2.06
34.86	0	0.61	55.47	10	10	-65.81	1.00	1.91
40.52	0	0.61	61.13	10	10	-71.47	1.00	1.68
40.52	5.03	0.61	66.16	10	10	-76.50	1.00	1.45
40.52	9.59	0.61	70.72	10	9	-81.06	0.90	1.28
40.52	14.62	0.61	75.75	10	7	-86.09	0.70	1.2
40.52	19.58	0.61	80.71	10	1	-91.05	0.10	ND
40.52	24.61	0.61	85.74	10	0	-96.08	0.00	0.95
40.52	27	0.61	88.13	10	0	-98.47	0.00	ND
40.52	29	0.61	90.13	10	0	-100.47	0.00	ND
40.52	31	0.61	92.13	10	0	-102.47	0.00	ND
40.52	33	0.61	94.13	10	0	-104.47	0.00	0.65
40.52	35	0.61	96.13	10	0	-106.47	0.00	ND
40.52	37	0.61	98.13	10	0	-108.47	0.00	0.6

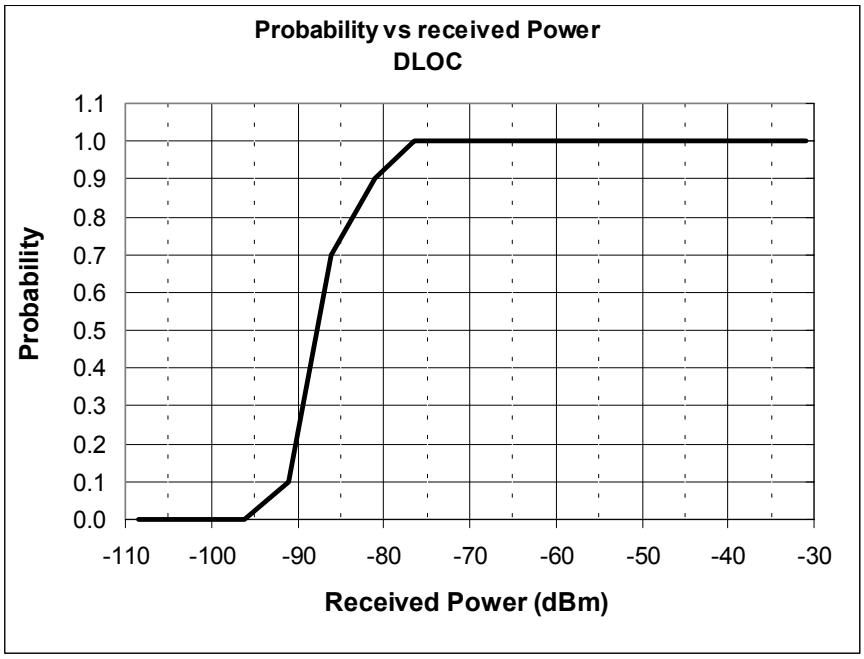


Figure 4.12 Probability vs. Received Power

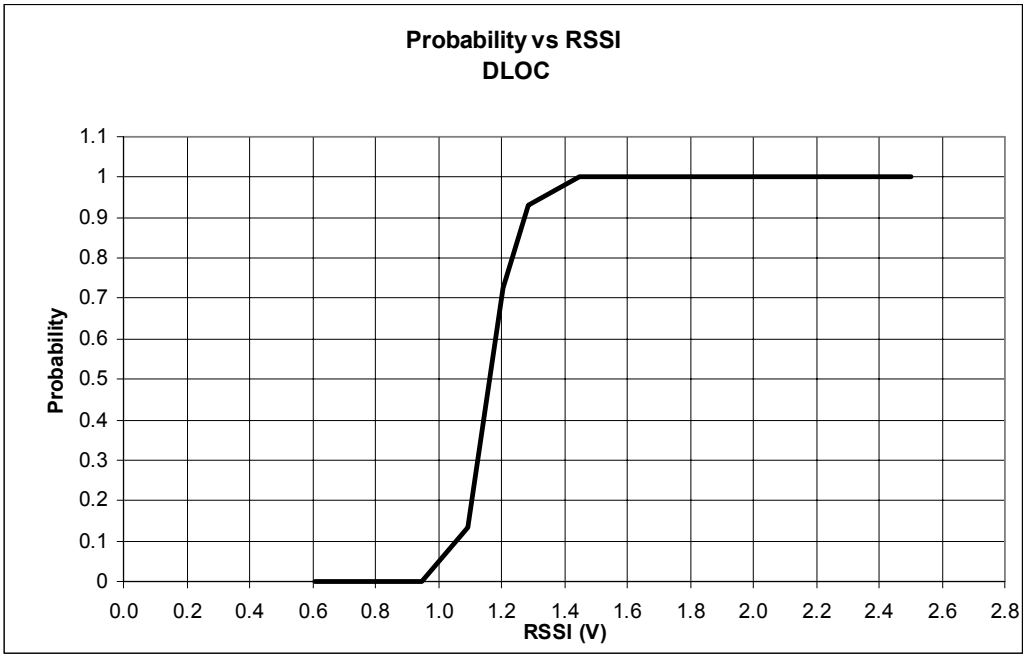


Figure 4.13 Probability vs. RSSI

Chapter 5 Propagation Testing

Chapter 5 details the indoor and outdoor propagation testing of the WDL. Indoor testing was performed in Whittemore Hall and Squires Student Center. Outdoor testing was done in the Whittemore Hall parking lot and surrounding campus. All testing was performed at Virginia Polytechnic Institute and State University (Virginia Tech/Blacksburg campus).

5.1 Whittemore Hall

Whittemore Hall provides a real world harsh environment for propagation testing. It is a six-story building made of concrete and steel. The structure has two elevators and offices and labs occupy 90% of the interior space. Since this is one of the electrical engineering buildings, other labs doing radio frequency and microwave work could potentially cause interference.

5.1.1Manchester Encoder

For testing, the TX power level was set to maximum (around +10dBm). A single slave unit was placed in the CWT lab (fourth floor) and the master unit moved to various positions on the fourth, fifth, and sixth floors (Figures 5.1-5.3). The master was set to poll the slave for data every 10 seconds. The system was left to run from twenty minutes to two hours and the TX/RX numbers and RSSI voltage were recorded. From these numbers the probability for each location was calculated.

Table 5.1 Whittemore Hall Manchester Encoder

Manchester Encoder	
4th, 5th and 6th Floors	
Probability	RSSI(V)
0.0000	0.658
0.0000	0.730
0.4262	1.150
0.4301	0.900
0.0483	0.863
0.6069	1.300
0.6100	0.865
0.6223	1.060
0.6927	1.200
0.8473	2.159
0.8514	1.311
0.9258	1.580
0.9321	1.500

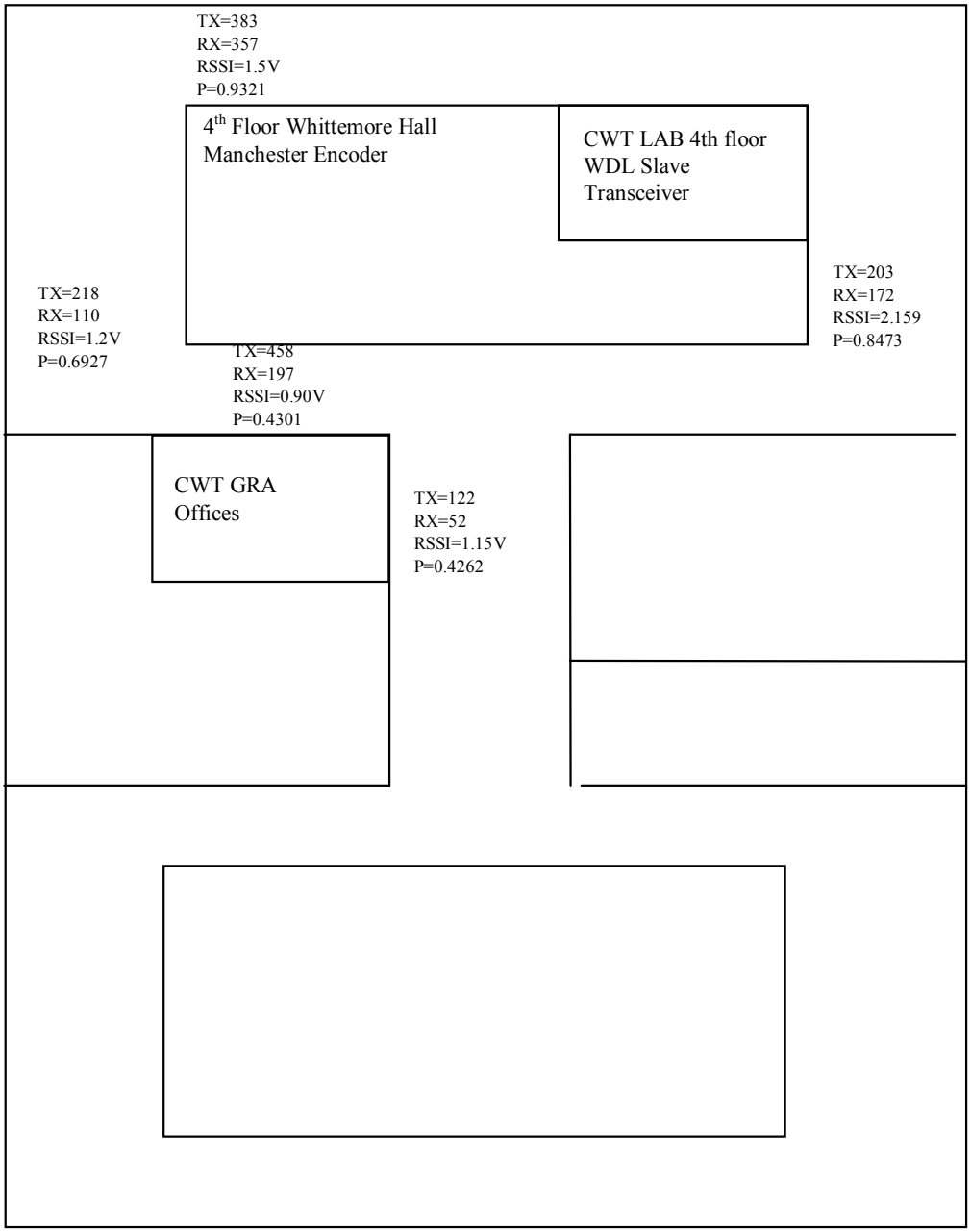


Figure 5.1 Fourth floor Whittemore Hall

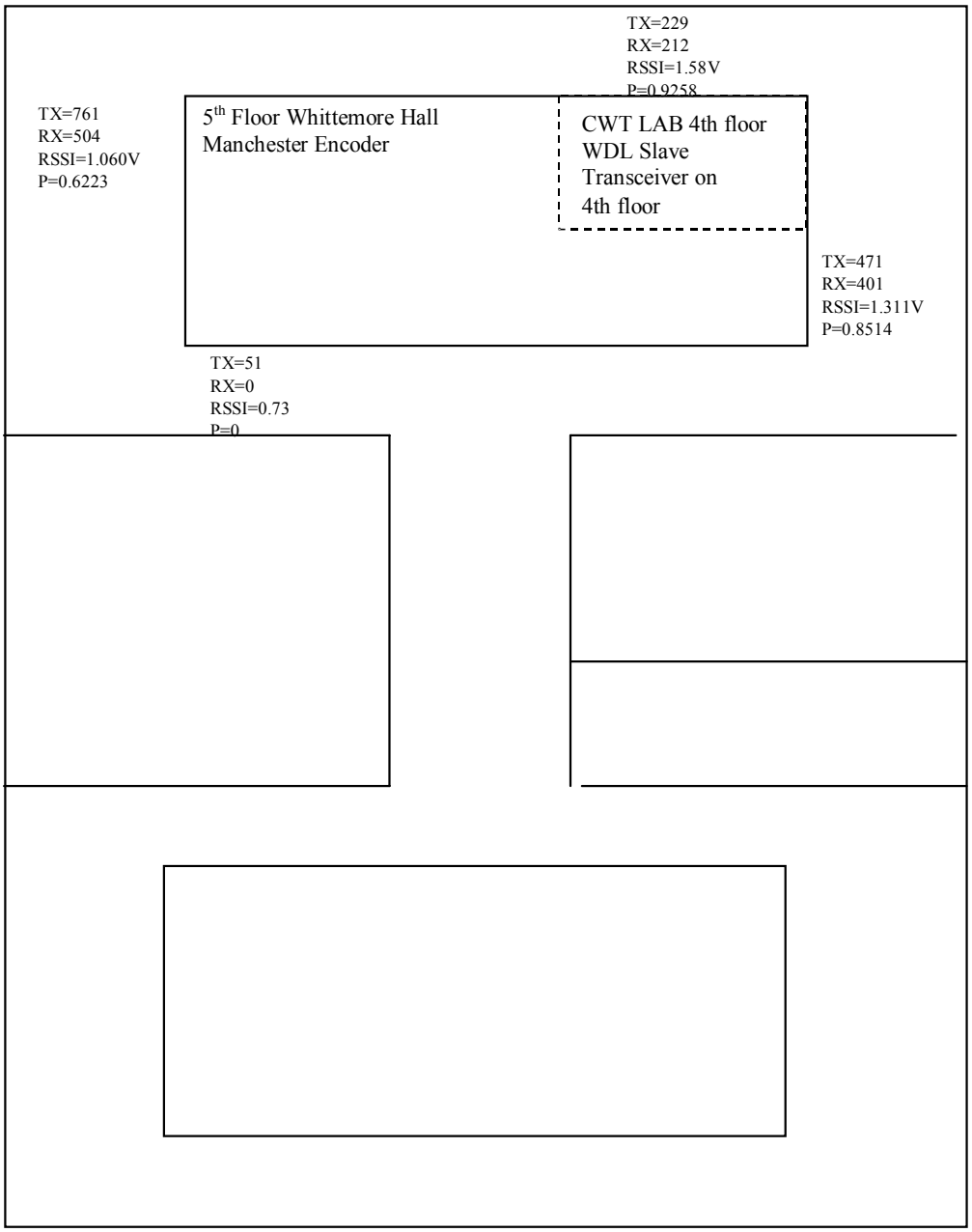


Figure 5.2 Fifth floor Whittemore Hall

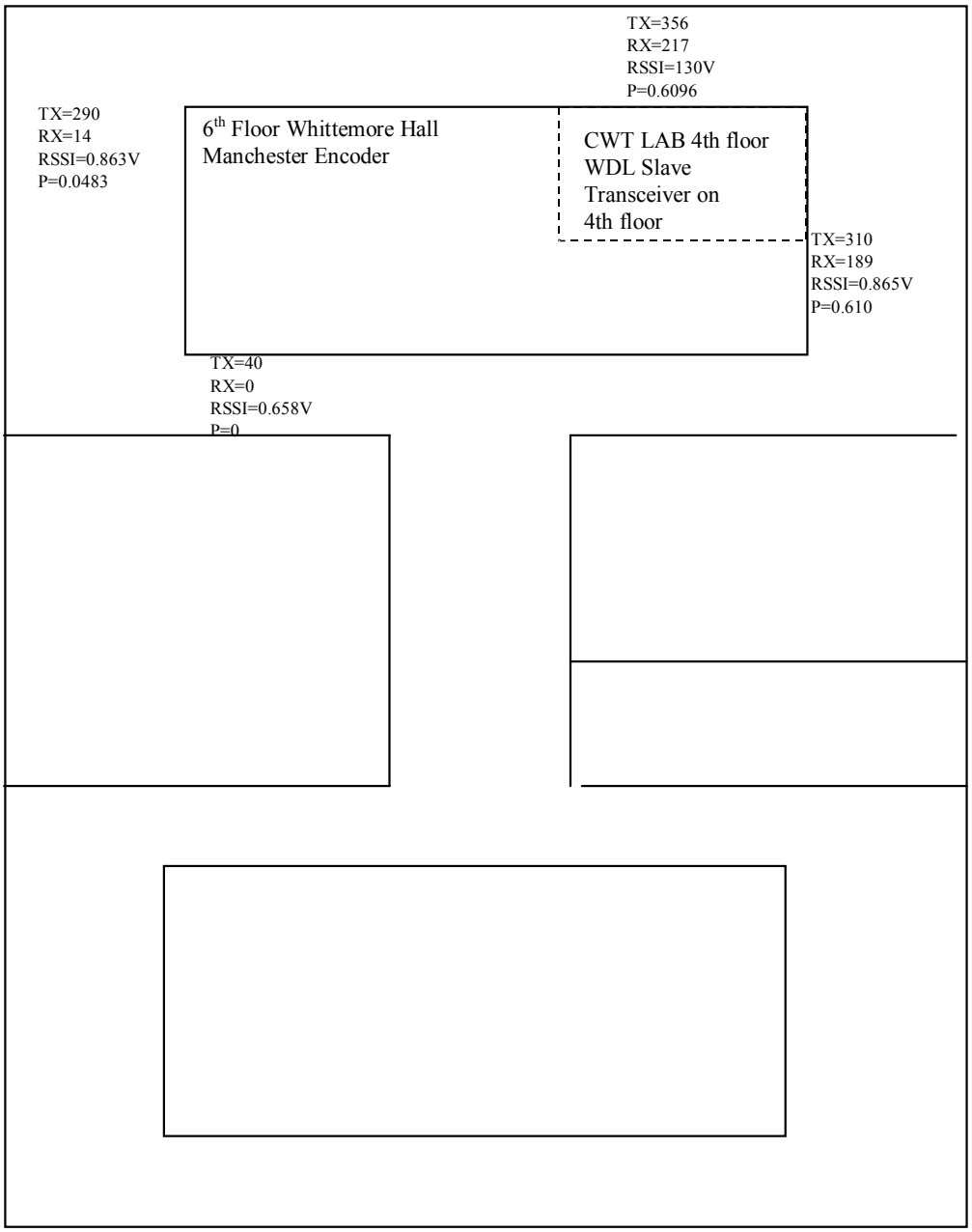


Figure 5.3 Sixth floor Whittemore Hall

A second propagation test in Whittemore Hall, similar to the wired coaxial test, was performed to obtain data on the repeatability of the link. As with the previous test the slave WDL was placed in the fourth floor lab, but the master was positioned in various locations only on the fourth floor. The fifth and sixth floors were assumed to have similar correlation with the previous long-term test. At each location the master

was allowed ten requests for data (TX), and the number of correct responses (RX) was recorded. This was done four times per location to ensure that the data was repeatable and the probability taken to be the average of the test (Table 5.2). Figure 5.4 shows the details and locations of the test.

Table 5.2 Whittemore Hall fourth floor only

Manchester Encoder	
4th Floor Only	
Probability	RSSI(V)
0.0000	0.900
0.6250	1.284
0.6250	1.350
0.8500	1.489
0.8500	2.075
0.9000	1.730
0.9000	2.240

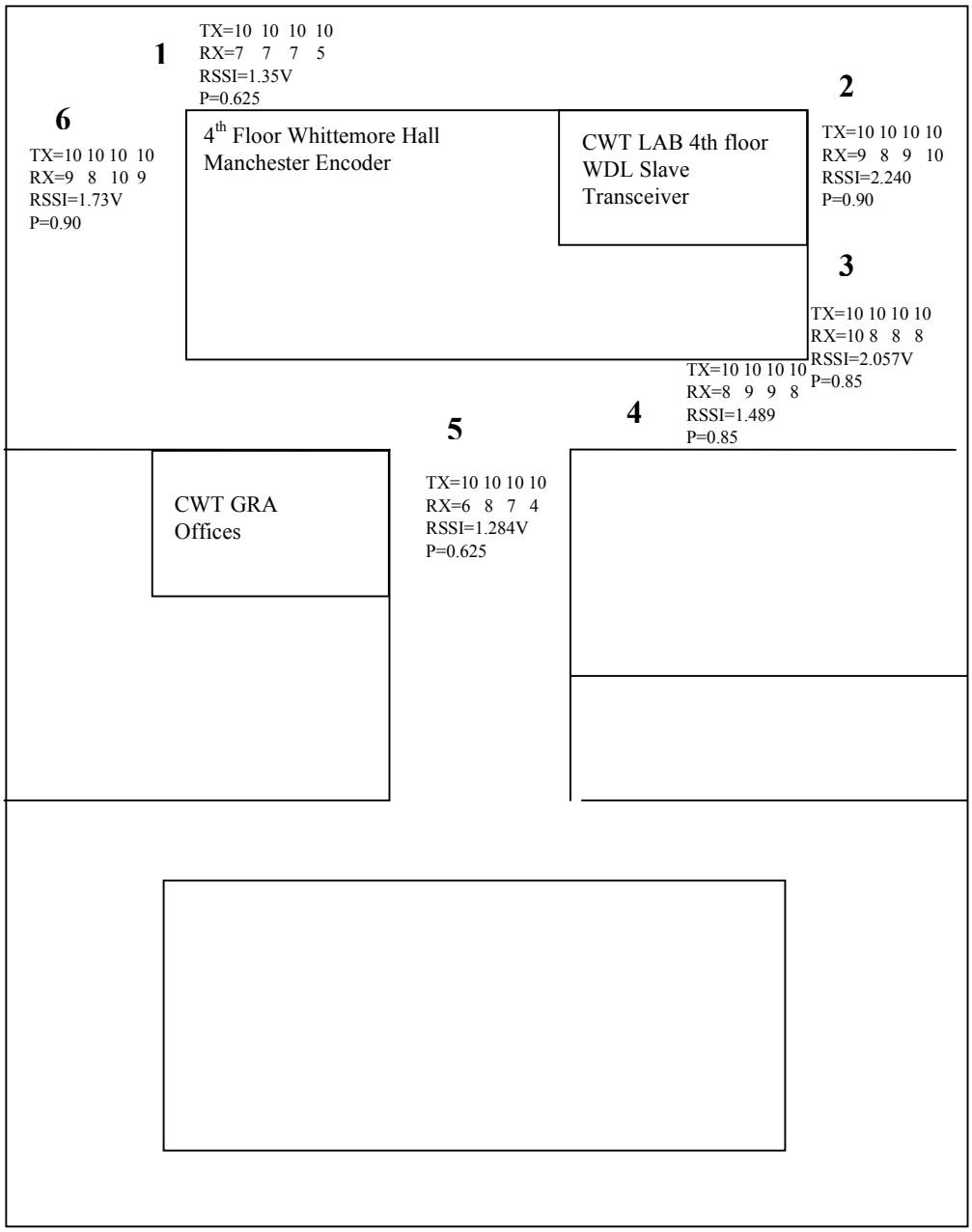


Figure 5.4 Manchester-Fourth floor Whittemore Hall

5.1.2 DLOC

To determine how well the DLOC scheme worked, the Whittemore Hall (fourth floor only) propagation test was performed. In order to compare the two encoding schemes, the test locations were kept as close to the Manchester Encoder locations as possible. Figure 5.5 shows the locations and Table 5.3 display the test results.

Table 5.3 DLOC Fourth floor Whittemore Hall

	DLOC	
Location	Prob	RSSI(V)
1	0.775	1.35
2	0.850	2.24
3	0.875	2.06
4	0.700	1.49
5	0.775	1.28
6	0.750	1.73

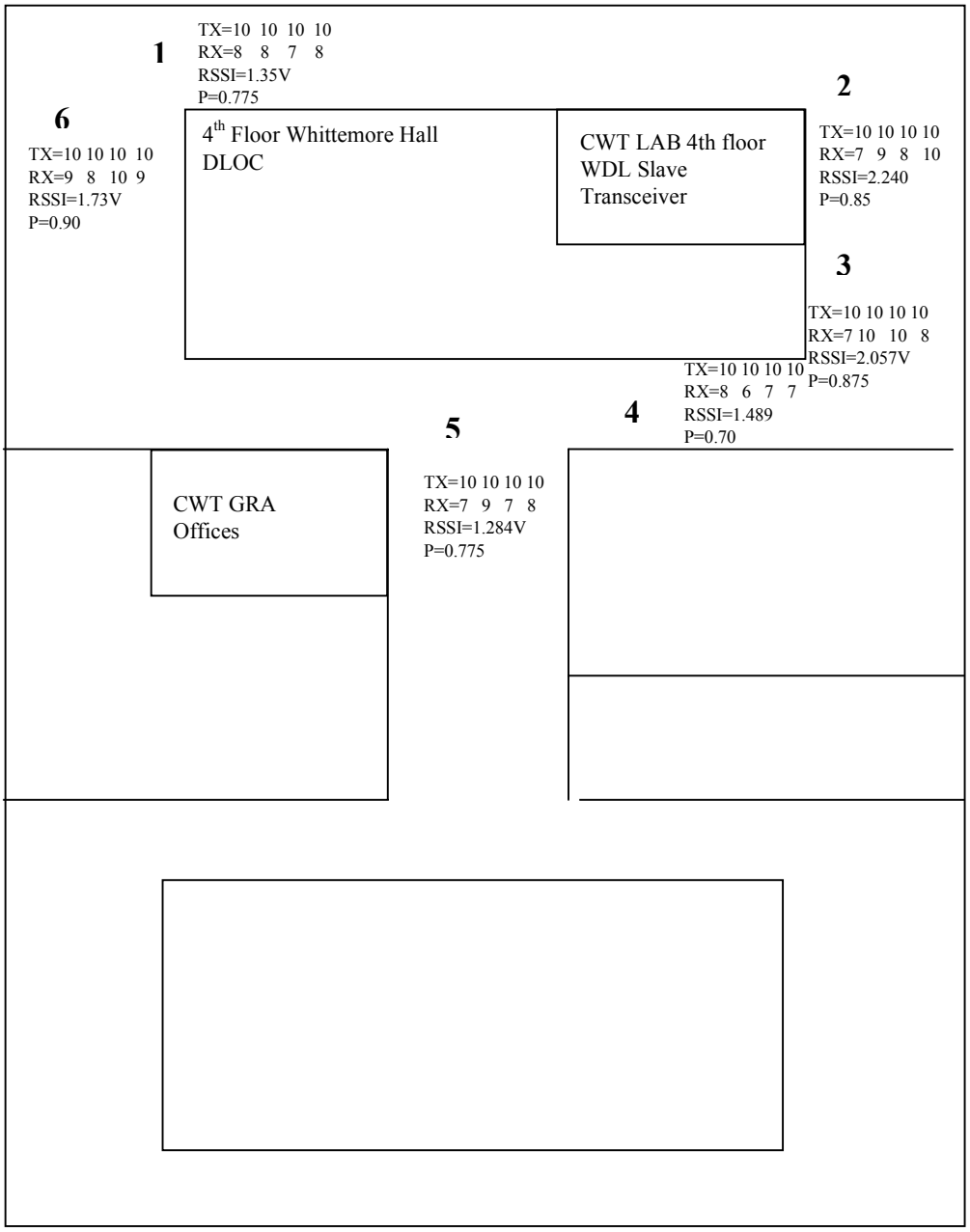


Figure 5.5 DLOC-Fourth floor Whittemore Hall

5.1.3 Whittemore Hall Summary

The probability versus the RSSI for all Whittemore Hall tests is shown in Figure 5.6. ME-1 and ME-2 stand for the fourth floor results for the two Manchester Encoder tests. From this data a general conclusion can be drawn that for the either type of

encoding scheme, an RSSI voltage of 1.25V or greater is required to obtain greater than a 50% probability of successful data transfer.

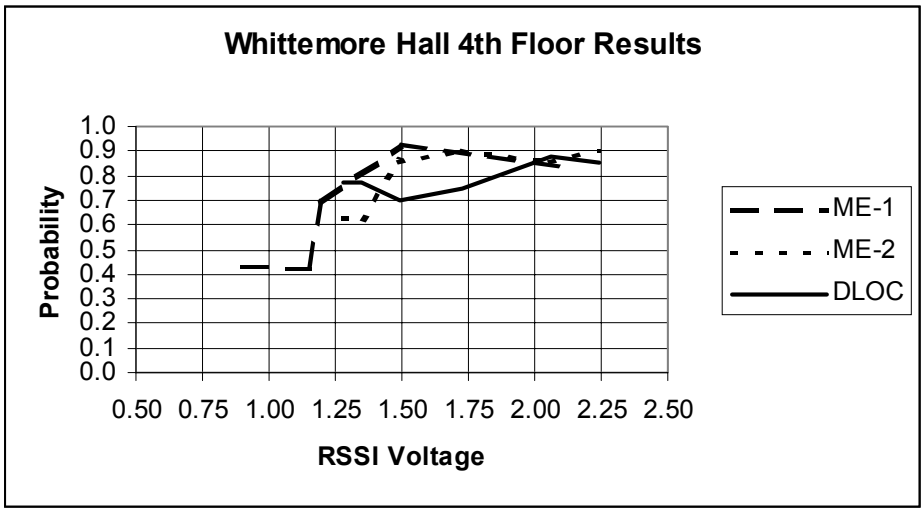


Figure 5.6 Whittemore Hall fourth floor results

Since each test location for the ME-2 and DLOC test were the same, the received power and RSSI remained the same. Using this data a comparison of the two encoding schemes was graphed. Figure 5.7 shows that on the average the two schemes work equally well at each location.

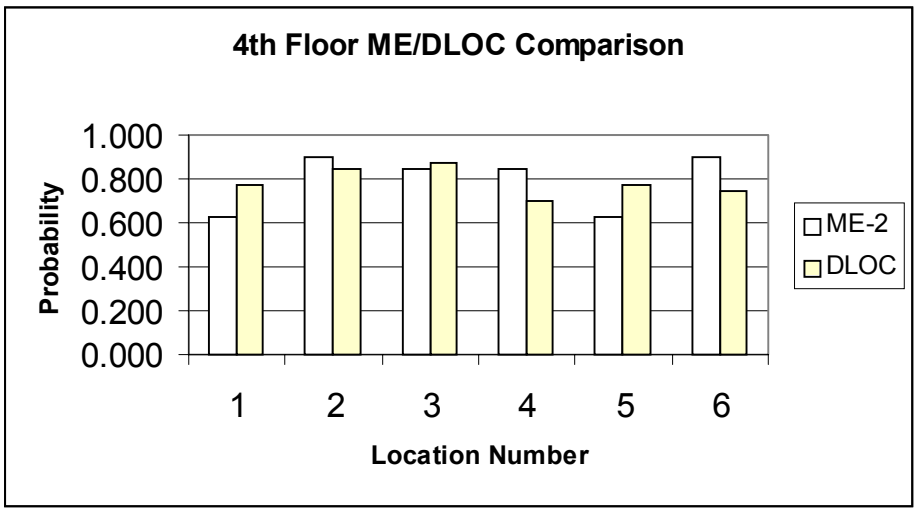


Figure 5.7 Whittemore Hall fourth floor comparison

5.2 Squires Student Center

A real world operating environment was determined to be a shopping mall with multiple floors. Requests were made of several local malls for the use of their facilities with no success. The Squires Student Center on the Virginia Tech campus was chosen due to its similarity to a mall environment. The student center has three floors with an open space connecting all three as well as halls extending off of the main area on each floor. For this test, only the DLOC encoding scheme was employed. Previous results have shown that the DLOC works as well as and in some cases better than the Manchester Encoder. In addition, with cost being the main driving factor, the DLOC is the preferred design. Setup for the test consisted of placing a slave unit on the first floor and having the master as the mobile transceiver, which was moved to various locations on all floors.

5.2.1 DLOC Testing

The transceivers were configured for maximum output power. At each location several tests of ten requests for data were done to ensure that the link was repeatable. Figures 5.9, 5.10 and 5.11 show the location of each unit and the associated measurements. Measurements include received power (Pwr), RSSI voltage, and the probability of a successful data transfer. Table 5.4 and Figure 5.8 present the results for comparison.

From the data and figures it can be seen that a significant portion of the student center could be covered with a probability greater than 50% with an RSSI of 1.30V or larger. These results concur with the Whittemore Hall indoor test for probability and RSSI.

Table 5.4 Squires Student Center Probability-DLOC

Location	RSSI (volts)	Rcvd Power (dBm)	Prob	Floor
1	1.75	-68.937	0.550	1
2	1.55	-73.087	0.850	1
3	1.50	-74.123	0.900	1
4	0.74	-99.428	0.000	1
5	1.02	-93.450	0.000	1
6	1.38	-77.338	0.600	2
7	1.44	-75.452	0.600	2
8	1.26	-81.750	0.350	2
9	1.40	-76.709	0.900	2
10	1.15	-87.282	0.000	2
11	1.35	-78.281	0.700	3
12	1.10	-89.589	0.100	3
13	1.35	-78.281	0.450	3

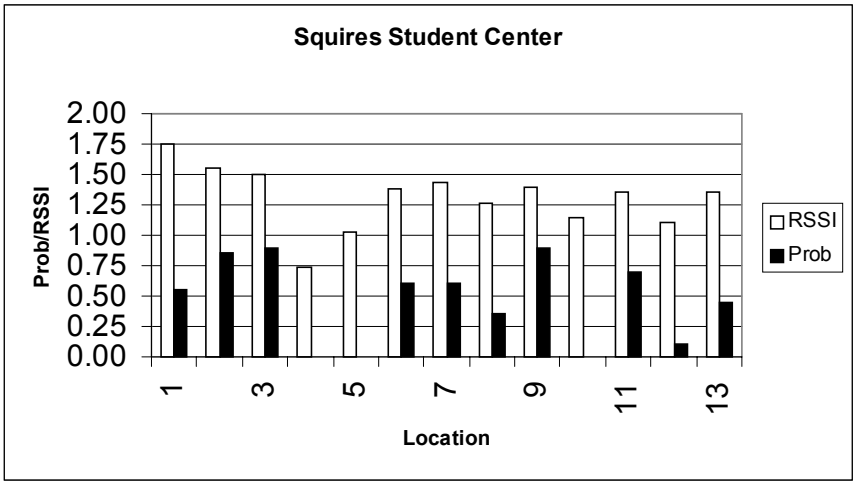


Figure 5.8 Squires Student Center-DLOC

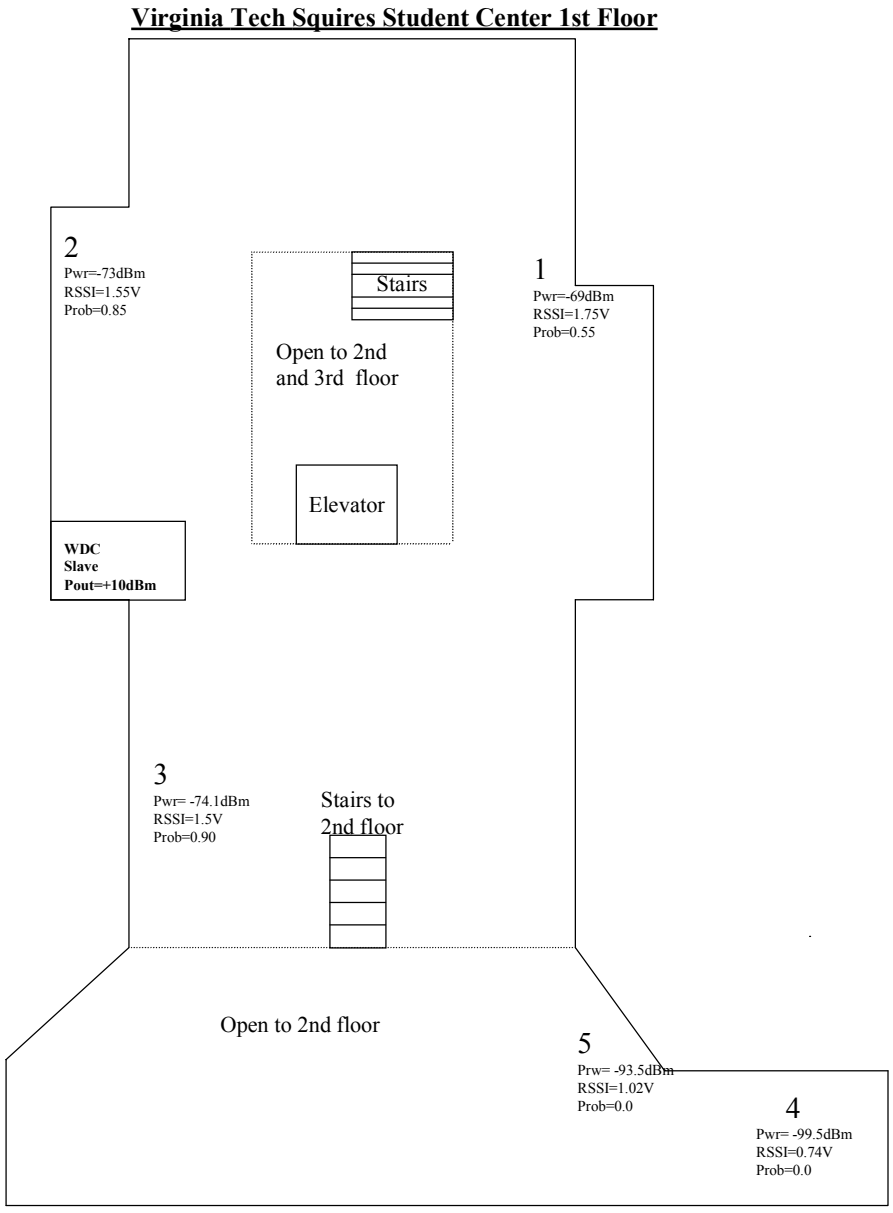


Figure 5.9 First floor Squires Student Center

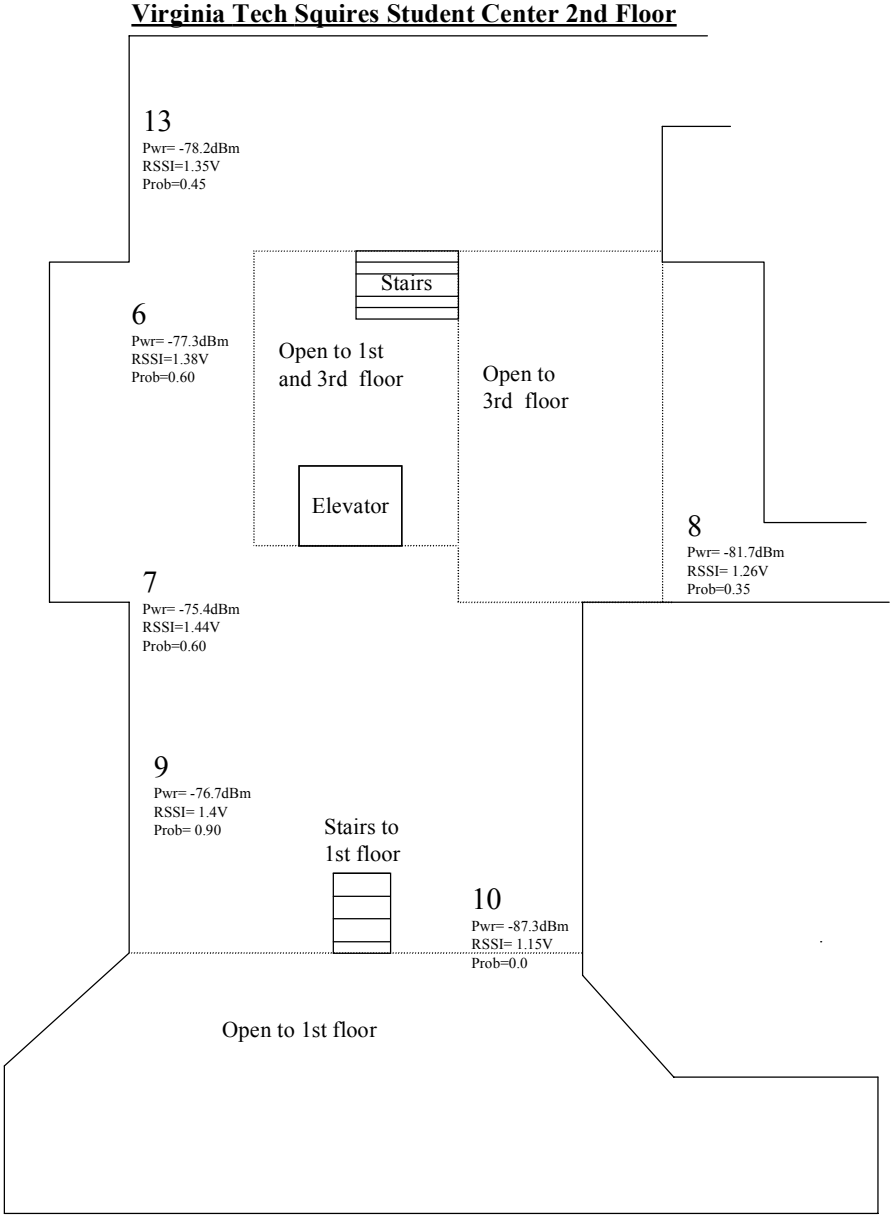


Figure 5.10 Second floor Squires Student Center

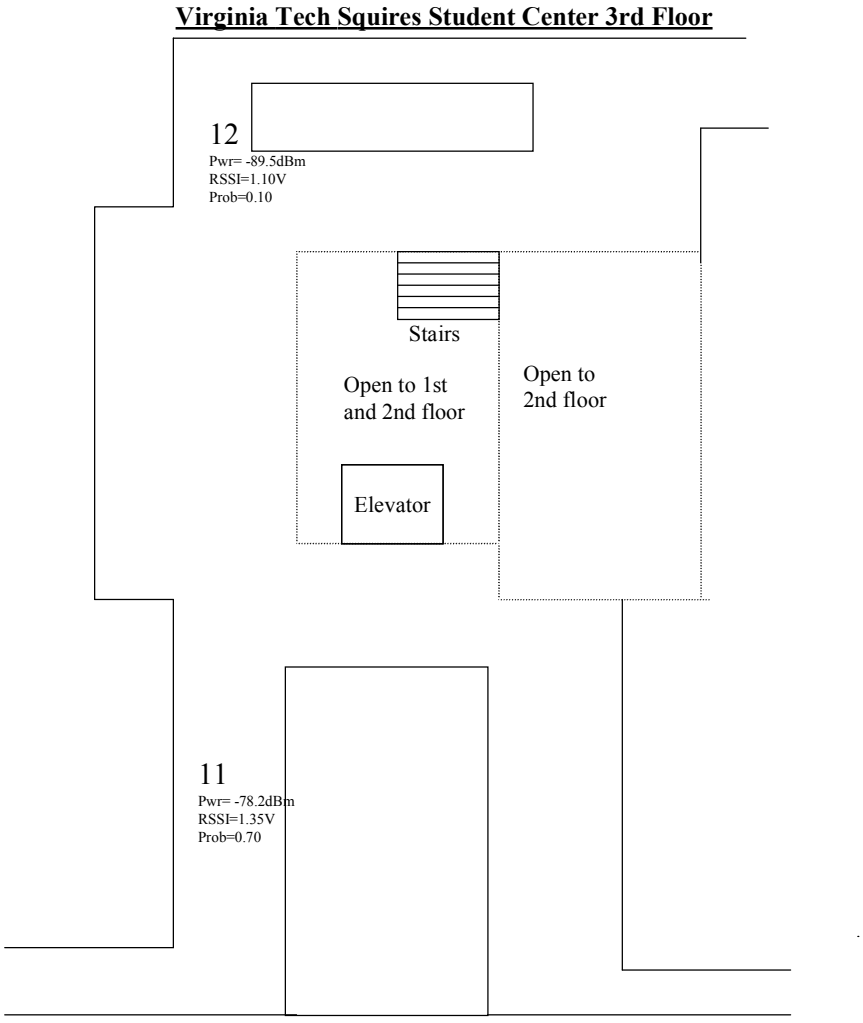


Figure 5.11 Third floor Squires Student Center

5.3 Outdoor Testing

Two outdoor propagation tests were performed to remove distance limits imposed by buildings. Test one was conducted in the Whittemore Hall parking lot, keeping the master and slave WDL in line-of-sight. The slave was placed on the third

floor balcony and the master moved around the parking lot. A second test, allowing for greater distance between the transceivers, was conducted from the roof top antenna range on Whittemore Hall to various locations around the campus.

5.3.1 Whittemore Hall Parking Lot-Master in Car

For the test a slave unit was positioned on the third floor balcony of Whittemore Hall, while the master unit was placed in a car (physically in the car at window height) and moved about the parking lot. This process was done two times to get the data for RSSI, Manchester Encoder, and DLOC. Line of sight was maintained for both tests, which required some slight position adjustment for each encoding scheme due to changing parking lot conditions.

Table 5.5 Parking lot-Master in car-DLOC

		Manchester		Distance
Location	RSSI(V)	Encoder	DLOC	Meters
1	1.330	0.575	0.466	342.647
2	1.750	0.833	0.879	131.194
3	1.750	0.066	0.525	205.313
4	1.400	0.966	0.700	198.66
5	1.260	0.000	0.330	331.638
6	1.450	0.000	0.566	194.718
7	1.550	0.833	0.825	54.017
8	1.470	0.375	0.700	142.557

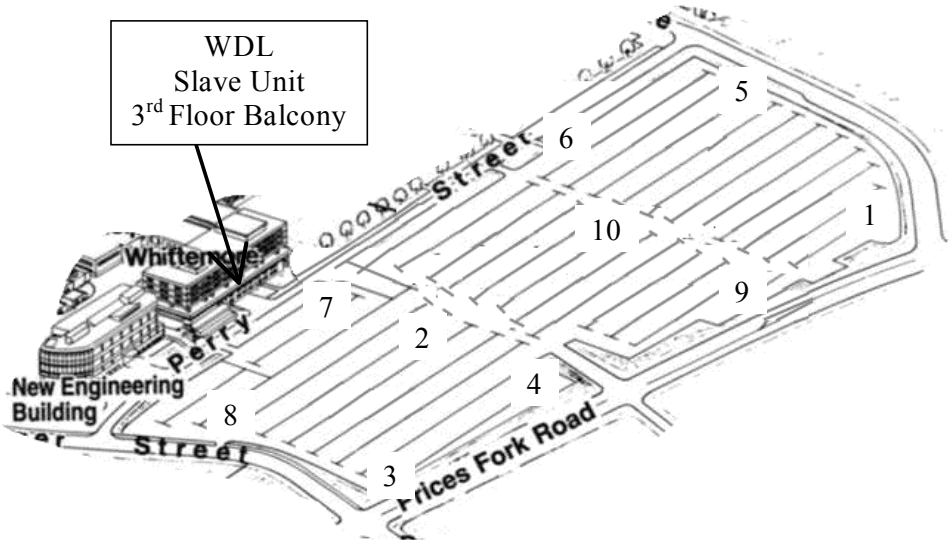


Figure 5.12 Whittemore Hall parking lot test locations

The success rates were fairly close when both encoding schemes worked properly. However, there were two positions (5,6) where the Manchester scheme was unable to transfer data correctly. In position three, two out of thirty requests resulted in a proper reply from the slave, which was a probability of 0.066 and should be considered as zero. The problem in these positions is most likely due to timing errors with the Manchester Encoders; the TX and RX clocks may not have been synchronizing. The RSSI voltage compared to the probability is consistent with the indoor test, where it was determined that an RSSI of greater than 1.25V was needed to get a 50% or better success rate. Position one had an RSSI of 1.33V and an average probability of 0.51; while position seven had an RSSI of 1.55V and an average probability of 0.83.

5.3.2 Whittmore Hall Parking Lot-Master On Car Roof

Placing the master WDL on the roof of the car, the test was repeated to determine if the transceiver's position inside the car had any significant effects on the radio link (Table 5.6). The DLOC scheme worked significantly better in all test locations where a reply was received, but the overall test results were worse than the "in car" test. Locations 3 and 8 produced no successful data transfers for the "on roof" test, while the "in car" test results were greater than 50% for both locations for the DLOC.

Table 5.6 Parking lot-Master on car roof-DLOC

		Manchester		Distance
Location	RSSI(V)	Encoder	DLOC	Meters
1	1.34	0.566	0.866	342.647
2	1.56	0.000	0.100	131.194
3	1.9	0.000	0.033	205.313
4	1.78	0.625	0.850	198.668
5	1.16	0.033	0.300	331.638
6	1.45	0.800	0.966	194.718
7	2.02	0.625	0.933	54.017
8	1.48	0.000	0.033	142.557
9	1.46	0.000	0.000	270.004
10	1.49	0.000	0.000	226.198

It is not known if the degradation in performance is due to the master or the slave WDL. The software in the slave unit does not count the number of requests received; therefore, it is difficult to determine at which end the problem exists. The assumption is that the master WDL received multi-path signals during the reply from the slave unit, thus causing the data to be corrupted. It is suspect that the cause of this was the metal roof of the car; it may have acted as a reflector, causing multi-path signals at the master antenna. Furthermore, the only change to the test setup was placing the master on the car roof. The location of the slave unit was not changed, so the problem would not have been with the slave unit.

5.3.3 Whittemore Hall Roof Top

From the rooftop, the line of sight distance between the master and slave units was greatly increased. The actual distances were not measured, but an estimate was done to better evaluate the performance of the radio link. A WDL set to transmit the clock was positioned on the corner of the building such that there were no obstructions in front of or behind the transceiver. A unit in receive mode was placed in a car and moved to several locations around the Virginia Tech campus. Time permitted only an RSSI measurement, but several locations were near those used for the “In Car” test, and the RSSI measurements were within a few tenths of a volt. This allows the conclusion to be drawn that all other RSSI measurements of the clock signal are accurate. Figures 5.13 and Table 5.7 detail the test locations and measurements.

From Table 5.7 it can be seen that the critical RSSI voltage (around 1.3V/ 50% probability) can be obtained from a distance no greater than 1200 feet (365m).

Table 5.7 Whittemore Hall roof top RSSI

			Estimated
Loc. #	Location Detail	RSSI (V)	Meters
1	Metered spaces in front of Whittemore Hall	1.530	91.46
2	Corner of Perry St. & W Campus Dr.	1.350	365.84
3	Corner of w Campus Dr. & Prices Fork Rd.	1.300	396.33
4	VT Parking lot on turner St.	1.297	304.87
5	Four Points Hotel Parking Lot	0.900	762.18
	(Corner of Prices Fork Dr. & University City Blvd.)		
6	Corner of Mcbryde Dr. & Prices Fork Dr.	1.550	274.38
7	Corner of Kesley Ls. & Toms Creek Rd.	0.840	640.23
8	Corner of Winston & Toms Creek	1.275	548.77
9	Corner of Prices Fork & Toms Creek	1.450	243.90
10	Corner of Prices Fork & Main St.	0.950	640.23
11	Tech Village Center Parking Lot (Spot closest to VT)	1.200	579.25
12	Corner of Duck Pond Dr. & Oak Ln	1.246	579.25
13	Corner of Duck Pond Dr. & Smithfield Dr.	0.860	609.74
14	Corner of Duck Pond Dr. & W Campus Dr.	1.350	426.82

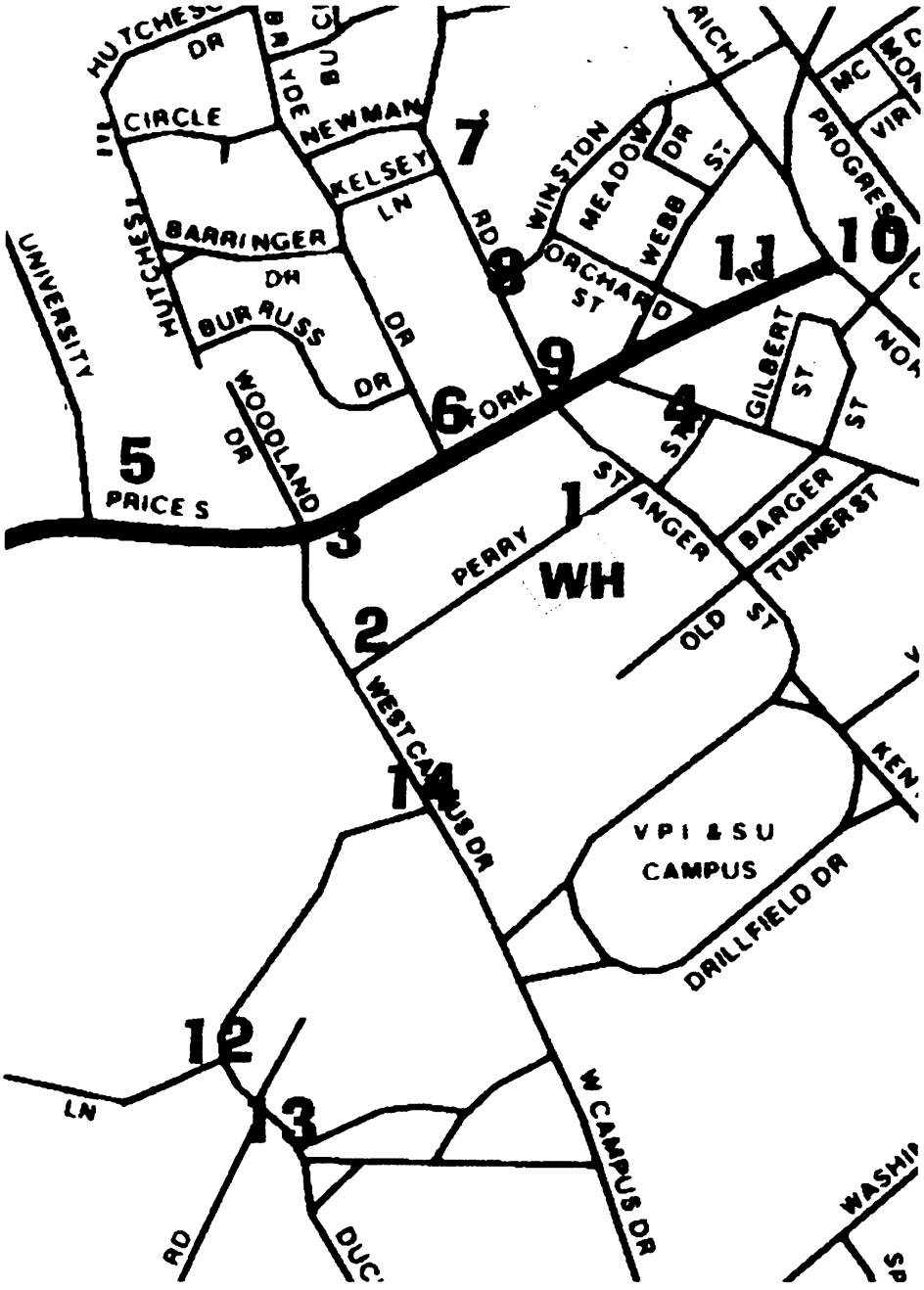


Figure 5.13 Roof top test locations

5.4 Verification of Propagation Testing

Indoor path loss varies as a function of the type of building and the material that the signal must pass through from transmitter to receiver. This is a topic of continuing research, which has resulted in many different indoor path loss models. One recent model used measured results to determine a new mean distance exponent used in the Friis transmission equation, and a standard deviation (sigma) for various building types and propagation paths [7].

Several of the test locations used to determine the distance exponent and sigma were similar to the WDL test locations. Using the values for these locations, correlation between the model and WDL measured path loss is verified (Table 5.8). In both cases the WDL received power for the stated distances was –75dBm.

Table 5.8 Propagation Path Loss Verification

Whittemore Single Floor			**Squires Single Floor**	
Similar to "Same Floor Building #1"			Similar to "West Wing 5th floor	
Freq	914MHz		Freq	914MHz
Pt(dBm)	8		Pt(dBm)	8
Distance(m)	18.3		Distance(m)	60.0
PL(d0)	31.7		PL(d0)	31.7
N	3.3		N	2.7
PL(d)	73.0		PL(d)	79.4
sigma	11.2		sigma	8.1
Pr(dBm)	-76.2		Pr(dBm)	-79.5

Chapter 6 Production Costs Estimate

One of the goals of this project was to keep the production cost less than $50.00 per unit for the WDL. A production cost of $36.50 per unit, plus a number of one time engineering charges, was realized by working with a local circuit board manufacturer. As the lowest-cost design, the DLOC was the only scheme for which estimates were obtained. The first step to obtaining the targeted cost was to reduce the POCP parts list in Appendix C, to a production list in Appendix D. All parts required only for the POCP were removed to produce a minimum parts list for production. The production parts list was passed on to the circuit board manufacture to obtain a quote (Table 6.1).

Table 6.1 Production Cost Estimates

	Qty	Cost Ea.
WDL Communications Board	1000	$36.50
Estimates of one time Engineering Charges		
NRE for Machine Set Up	1	$400-$650
Solder Paste Stencils	1	$500.00
Board Set Up/Tooling Chg's	1	$500-$1000
Bare Board Electrical Test	1	$400-$700

Chapter 7 Summary and Conclusions

The WDL system consists of three main parts: the RF transceiver board, the data encoder/decoder, and the digital interface (DIF) board. The DIF board is a custom designed board that contains the encoder/decoder, while the transceiver is a slightly modified evaluation board from RF Micro Devices (RFMD). FSK (frequency shift keying) modulation was chosen due to its low complexity, ease of implementation and low cost.

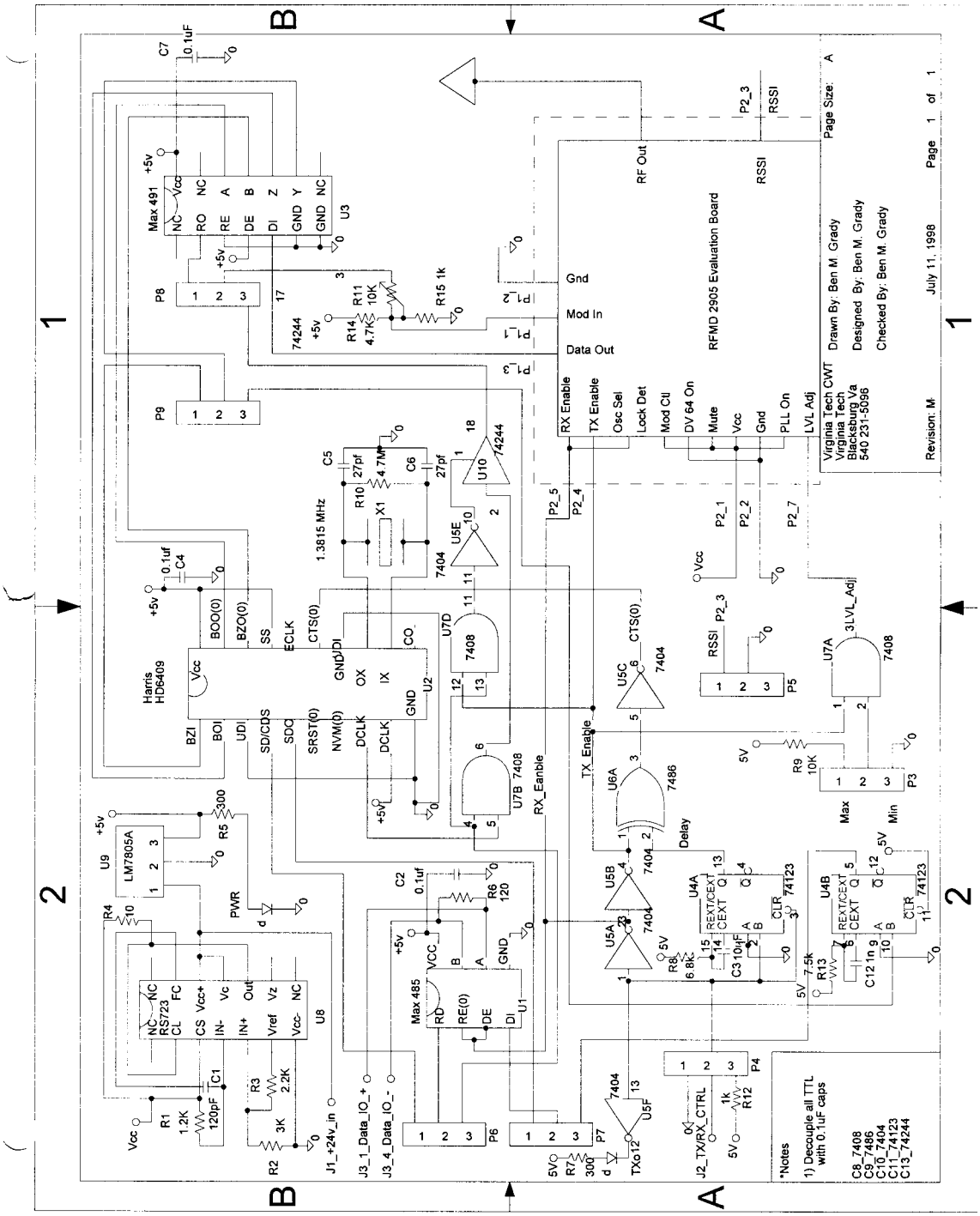
The designed system was tested in the laboratory, indoor, and outdoor settings to determine usability. Based on the test data, two tools were deemed reliable to determine the expected data error rate. One is the RSSI (received signal strength indication) measurement, which is related to the received power, and the other is repeated measurement of the propagation path using the actual system with test data. In the laboratory an RSSI voltage around 1.20V (received power –85dBm) was determined to yield a 50% probability of a successful data transfer in an ideal link. When taking into account RF propagation issues such as multi-path, the RSSI voltage does not provide a reliable measure of probability. The second test provided a more reliable result, since it used repeated test data transmissions to determine the error rate. Consequently, the characteristics of each individual link can be taken into account.

Results of the tests in Whittemore Hall and Squires Student Center gave two real-world indoor environments for comparison. For propagation on a single floor, an RSSI voltage of 1.50V (receiver power –75dBm) should yield a probability of at least 0.75 for a straight-line distance of approximately 60 feet in Whittemore Hall. The straight-line path under worst-case conditions is through a concrete wall and several interior rooms, one of which is the equipment room for the air handler. For the less harsh environment of Squires, an RSSI of 1.50V should yield a probability of 0.85 for a range no greater than 200 feet. Between floor propagation in Squires showed that by staying within the main open area on all floors, a probability of at least 0.5 could be obtained with an RSSI of 1.4V or greater. When the RSSI dropped below 1.20V (received RF levels lower than –83dBm), the probability was zero. This data corresponds with the cabled receiver sensitivity test. At levels approaching 1.25V (-80dBm), the probability dropped from one.

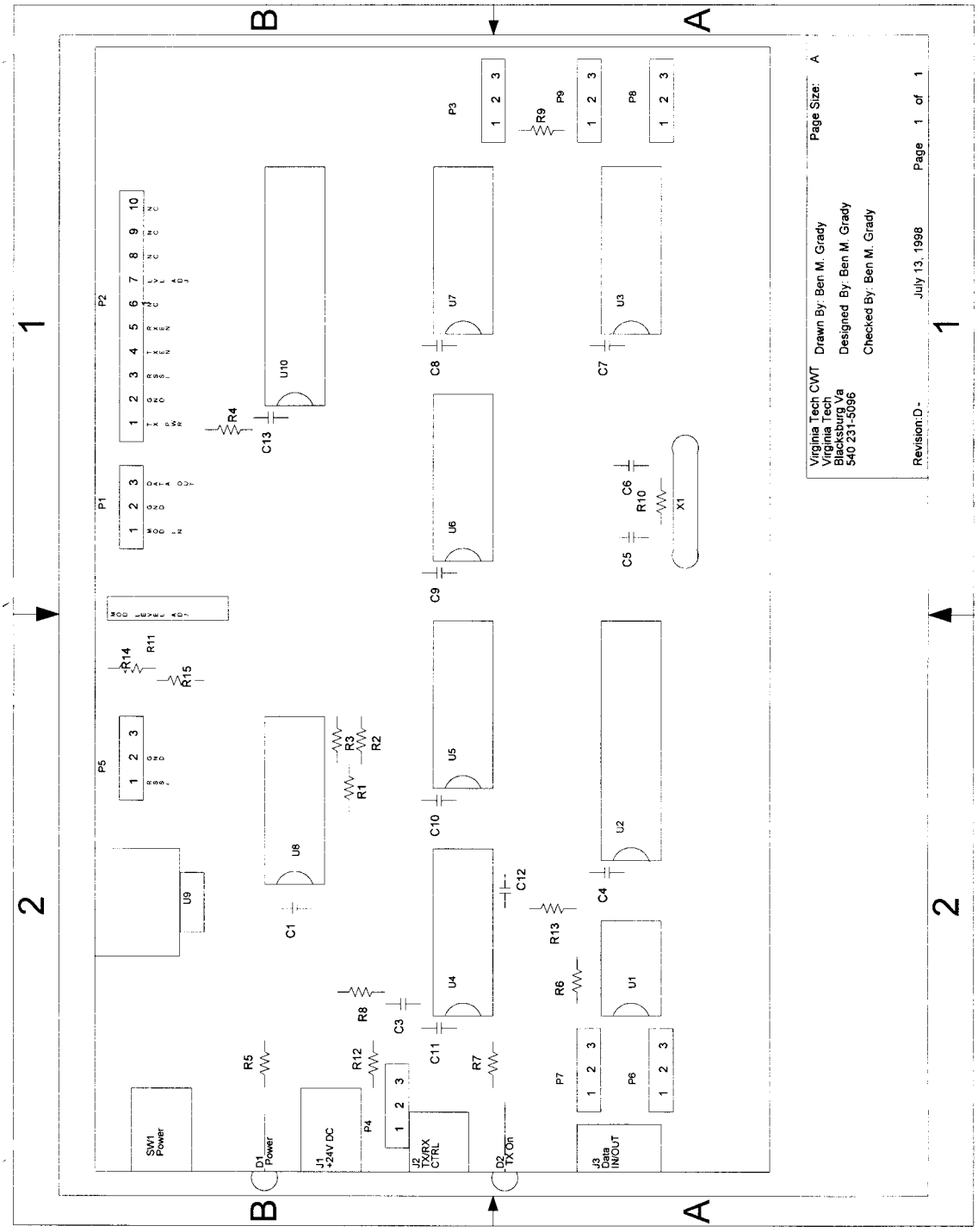
Removing the constraints of an enclosed building, two outdoor propagation tests were performed from Whittemore Hall at Virginia Tech. These test were done LOS (line-of-sight), which means the transmitter and receiver antennas were able to "see" one another. The tests were from the 6th floor rooftop antenna range to several locations on and off campus, and from the 3rd floor balcony to locations in the Whittemore Hall parking lot. Due to the time of year, leaves on the trees obscured the LOS paths for several of the 6th floor tests. In addition, time constraints only allowed RSSI measurements for the 6th floor testing. To cover the whole Whittemore Hall parking lot from the 3rd floor balcony (maximum distance 1200 ft), a RSSI voltage of at least 1.3V (received power –78dBm) is required for a probability of no less than 0.5. By moving the transmitter from the 3rd to the 6th floor, the LOS range was able to extend. Although actual data transmission testing was not possible, it was determined that distances greater than approximately 1200ft (365m) produced an RSSI close to the critical value of 1.3V for a probability of 0.5, as determined from the parking lot test. This RSSI corresponds to a received power of –80dBm, and is the low end of receiver sensitivity for data transfer as found in the cabled bench test. Any slight change in the propagation path characteristics or radio position could push the received power into the zero probability area.

The general conclusion for the WDL is, that for most operating environments, a RSSI of 1.4V would yield at least 50% probability of successful data transfer. This RSSI corresponds to a received power lever of –75 dBm, and a LOS distance of 300m or 1000ft.

Appendix A Schmetic



Appendix B Parts Layout



Appendix C-POCP Parts List

WDL POCP PARTS LIST

Parts Required for One WDL Transciever

Part	Qty	Manufacture	Part #	Description	Vendor	Part #	Price ea	Total
J3	1	Amp	787616-1	Series A 90 deg USB Con.	Newark		$ -	$ -
J1	1	Radio Shack	274-1565A	Coaxial Power Jack	Radio Shack	274-1567A	$ 0.85	$ 0.85
J2	1	Radio Shack	274-247	Phono Jack	Radio Shack	274-247	$ 0.90	$ 0.90
P1	1	Radio Shack	274-1567A	Coaxial Power Plug	Radio Shack	274-1567A	$ 0.95	$ 0.95
P2	1	Radio Shack	274-289C	Phono Plug	Radio Shack	274-289C	$ 0.85	$ 0.85
	1	Radio Shack	276-1318	Stand Offs	Radio Shack	276-1318	$ 2.19	$ 2.19
	1	Centurion	EXC-902-SM	Antenna Tuf Duck	Centurion	EXC-902-SM	$ -	$ -
	1	Radio Shack	276-1368	T220 Heat Sink	Radio Shack	276-1368	$ 1.49	$ 1.49
	1	Radio Shack	276-1373	T220 Heat Sink Mounting Kit	Radio Shack	276-1373	$ 1.39	$ 1.39
	1	RFMD	2905	915MHz Transceiver	RFMD	RFMD2905	$ -	$ -
	1	Vector	8001	Prototype board	Newark	38F1249	$ 31.40	$ 31.40
	1	Amp	621745-1	Series A USB Cable	Newark	83F1114	$ 9.09	$ 9.09
	3	Amp	87499-5	3 pin AMPMODU Header Con.	Newark	90F7736	$ 0.78	$ 2.34
	1	Amp	1-87499-7	10 pin AMPMODU Header Con.	Newark	90F4896	$ 0.89	$ 0.89
	14	Amp	87756-7	Header Pins receptacle	Newark	90F5084	$ 0.21	$ 2.94
P1,P2,P3,P4,P5	1	Amp	4-103321-0	Verticle Single Row Header	Newark	90F3988	$ 1.52	$ 1.52
	1	Radio Shack	11907656	Project Box	Radio Shack	11907656	$ 3.69	$ 3.69
U2	1	Harris	HD3-6409-9	Manchester Encoder/Decoder	Hamilton Halmark	DH3-6409-9	$ 15.80	$ 15.80
U1	1	Maxim	Max485ECPA	RS-485/RS-422 Transceiver	Digikey		$ 2.00	$ 2.00
U3	1	Maxim	Max491ECPA	RS-491/RS-422 Transceiver	Digikey		$ 2.00	$ 2.00
U6	1	Radio Shack	7486	XOR Gate	Radio Shack		$ 1.00	$ 1.00
U5	1	Radio Shack	7404	Invertor	Radio Shack		$ 1.00	$ 1.00
U4	1	Radio Shack	74123	One Shot	Radio Shack		$ 1.00	$ 1.00
U7	1	Radio Shack	7408	AND Gate	Radio Shack		$ 1.00	$ 1.00
U8	1	Radio Shack	276-1740	723 Adj Voltage Reg	Radio Shack	276-1740	$ 0.99	$ 0.99
U9	1	Radio Shack	276-1770A	7805 +5V reg	Radio Shack	276-1770A	$ 1.49	$ 1.49
	4	Radio Shack		14 pin dip socket	Radio Shack		$ 0.30	$ 1.20
	1	Radio Shack		16 pin dip socket	Radio Shack		$ 0.30	$ 0.30
	1	Radio Shack		20 pin dip socket	Radio Shack		$ 0.30	$ 0.30
	1	Augat	508-AG12D	Machined 8 pin dip socket	Newark	14F3301	$ 0.97	$ 0.97
	1			SMA(M)-SMA(M) 90 deg				$ -
SW1	1	Radio Shack	275-612	SPST switch	Radio Shack	275-612	$ 2.89	$ 2.89
D1,D2	2			LEDS			$ -	$ -
R1	1			1.2K				$ -
R2	1			3K				$ -
R3	1			2.2K				$ -
R4	1			10				$ -
R5	1			300				$ -
R6	1			120				$ -
R7	1			300				$ -
R8	1			10K(varies for timming delay)				$ -
R9	1			10K				$ -
R10	1			4.7M				$ -
R11	1			10K multiturn				
R12	1			1K				
C1	1			10uF				$ -
C2	1			0.1uF				$ -
C3	1			10uF				$ -
C4	1			0.1uF				$ -
C5	1			27pF				$ -
C6	1			27pF				$ -
C7	1			0.1uF				$ -
C8	1			0.1uF				$ -
C9	1			0.1uF				$ -
C10	1			0.1uF				$ -
C11	1			0.1uF				$ -
TOTAL								**$ 92.43**

Appendix D-Production Parts List

Digital Interface Board

Part	Qty	Manufacture	Part #	Description
U9	1	Texas Instruments	UA78M05KC	3 terminal 5V regulator
U2	1	Texas Instruments	NE555D	555 timer
	1	Texas Instruments	TL317D	1.2-32Volt Adjustable Reg
U1	1	Maxim	Max485ECPA	RS-485/RS-422 Transceiver
U3	1	Maxim	Max491ECPA	RS-491/RS-422 Transceiver
U5	1	Texas Instruments	SN74LS04D	Invertor
U4	1	Texas Instruments	SN74LS123D	One Shot
U7	1	Texas Instruments	SN74LS08D	AND Gate
U8	1	Texas Instruments	SN74LS244DW	Tri state buffer
R4	1		5% 1/10W	10
R5	1		5% 1/10W	300
R6	1		5% 1/10W	120
R7	1		5% 1/10W	300
R8	1		5% 1/10W	10K selectable
R9	1		5% 1/10W	10K
R11	1		5% 1/10W	10K selectable
R12	1		5% 1/10W	1K
R13	1		5% 1/10W	7.5k
R14	1		5% 1/10W	4.7k
R15	1		5% 1/10W	1K
R16	1		5% 1/10W	
R17	1		5% 1/10W	
C1	1		10% 35V	120pF
C2	1		10% 35V	0.1uF
C7	1		10% 35V	0.1uF
C8	1		10% 35V	0.1uF
C9	1		10% 35V	0.1uF
C10	1		10% 35V	0.1uF
C11	1		10% 35V	0.1uF
C12	1		10% 35V	
C13	1		10% 35V	
C14	1		10% 35V	

Transceiver

Parts required for a single RFMD 2905 evaluation board as obtained from RFMD

Part	Qty	Manufacture	Description/	Notes
			Part #	
Capacitors	28			
Inductors	5			
Resistors	7			
Tantalum Capacit	1		4.7uF for Vcc (5V)	
Varactor (diode)	1		SMV1233-011	
Crystals	1		7.15909MHz	83.5 KHz apart for the 10.7MHz II
	1		7.07549MHz	
FM Discriminator	1		CDF107B-A0	
10.7 MHz IF filters	2	Murata	CEFC10.8MD11	
RF2905	1	RFMD	Transceiver/RF2905	

Appendix E-WDL Pictures

References

[1] Nadler, A. J. "RF Silicon Transceiver Family Targets ISM Band Low-power Wireless Data Communications." Applied Microwave and Wireless April 1998; 68-76

[2] RF Micro Devices, RF2905 Data Sheet, Rev B9 991108

[3] RF Microdevices, Application Note TA0028, "Silicon Transceiver Family for Low-Power Wireless Communications"

[4] Harris Semiconductor, HD-6409/883 CMOS Manchester Encoder-Decoder, March 1997.

[5] Tomasi, Wayne. Advanced Electronic Communications System. Englewood Cliffs, NJ. Prentice-Hall, 1987, 199-201.

[6] Couch, Leon W. II, Digital and Analog Communication Systems, Upper Saddle River, NJ. Prentice-Hall, 1997, 341-343.

[7] Scott, Seidel Y., Rappaport, Theodore S. "914 MHz Path Loss Prediction Models for Indoor Wireless Communications in Multifloored Buildings" IEEE Transactions on Antennas and Propagation, Vol. 40, No. 2, February 1992, pp. 207-217.

Vita

The author, Benjamin M. Grady, was born in Lynchburg, Virginia in 1965. He received an Associates Degree in Electronics Technology in 1987 after which he spent 3 years servicing and installing general aviation Avionics. In 1990 he enrolled in the Old Dominion University Electrical Engineering Technology program and was selected to participate in the NASA/ODU Microwave Technology Program. The main focus of the program was to design and build a 4.3GHz radiometer for laboratory testing. Upon graduating in 1992, he continued to work at NASA Langley Research Center to complete the laboratory radiometer. From 1995 to 1997 he was a Product Support Engineer at Ericsson with the main focus on the PCS1900 cellular base stations. In 1997 he enrolled in the Masters degree program at Virginia Polytechnic Institute and State University and completed his degree in May 2000. After graduation he will be working at the Naval Surface Warfare Center in Dahlgren Virginia in the Pulsed Power Electronic Counter Measure group focusing on RF systems.