A Fully Monolithic 2.5 GHz LC Voltage Controlled Oscillator in 0.35 μm CMOS Technology

by

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(ABSTRACT)

The explosive growth in wireless communications has led to an increased demand for wireless products that are cheaper, smaller, and lower power. Recently there has been an increased interest in using CMOS, a traditional digital and low frequency analog IC technology, to implement RF components such as mixers, voltage controlled oscillators (VCOs), and low noise amplifiers (LNAs). Future mass-market RF links, such as BlueTooth, will require the potentially low-cost single-chip solutions that CMOS can provide. In order for such single-chip solutions to be realized, RF circuits must be designed that can operate in the presence of noisy digital circuitry. The voltage controlled oscillator (VCO), an important building block for RF systems, is particularly sensitive when exposed to an electrically noisy environment. In addition, CMOS implementations of VCOs have been hampered by the lack of high-quality integrated inductors.

This thesis focuses on the design of a fully integrated 2.5 GHz LC CMOS VCO. The circuit is intended as a vehicle for future mixed RF/digital noise characterization. The circuit was implemented in a 0.35 μm single poly, 4 metal, 3.3 V, CMOS process available through MOSIS. The oscillator uses a complementary negative transconductance topology. This oscillator circuit is analyzed as a negative-resistance oscillator. Monolithic inductors are designed using full-wave electromagnetic field solver software. The design of an "inversion-mode" MOS (I-MOS) tuning varactor is presented,

along with a discussion of the effects of varactor nonlinearity on VCO performance. I-MOS varactors are shown to have substantially improved tuning range (and tuning curve linearity) over conventional MOS varactors. Practical issues pertaining to CMOS VCO circuit design, layout, and testing are also discussed. The characterization of the VCO and the integrated passives is presented. The VCO achieves a best-case phase noise of -106.7 dBc/Hz at 100 kHz offset from a center frequency of 2.73 GHz. The tuning range is 425 MHz (17%). The circuit consumes 9 mA from a 3.3 V supply. This represents excellent performance for CMOS oscillator designs reported at this frequency. Finally, several recommendations for improvements in oscillator performance and characterization are discussed.

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Chapter 1

Introduction

1.1 Background

The explosive growth in wireless communications has led to an increased demand for wireless products that are cheaper, smaller, and require lower power. Unlike the computer industry, where performance has nearly doubled annually since the mid 1960's[1], improvements in RF and analog circuits have been much slower. A major reason for the rapid advancement of digital performance has been that improvements in device technology—specifically the ever decreasing minimum feature size of Complementary Metal-Oxide-Semiconductor (CMOS) technology—has translated directly into performance gains. On the other hand, radio frequency (RF) components have typically been fabricated in technologies such as Gallium Arsenide (GaAs) and Silicon Bipolar, which yield better RF performance. These traditional RF processes have not benefited from improvements in device technology as quickly as their digital brethren.

Recently there has been an increased interest in using CMOS, a traditional digital

[1] The often quoted Moore's law postulates that digital device technology should approximately double in density and speed every 18 months.

and low frequency analog IC technology, to implement RF components such as mixers, voltage control oscillators (VCOs), and low noise amplifiers (LNAs) [3],[4]. The reasoning behind this research movement is obvious—digital CMOS circuits can be fabricated in extremely high volume on eight or twelve inch wafers at a relatively low cost per die. If suitable RF performance can be achieved in CMOS then wireless products could benefit from the same economy of scale that has propelled the PC industry from 20 MHz 80386 processors to 1.5GHz Pentiums during the last 10 years[2]. The potential for higher levels of integration in CMOS is tremendous. If digital and RF functionality can be combined on a single CMOS die, then the total cost of designing a wireless product could also be reduced.

CMOS has not been a very good technology for RF designs for a number of reasons [5]. While one could argue that sub-micron PMOS and NMOS devices themselves have reasonable RF characteristics (high f_t and f_{max}, Fig. 1.1), the low resistivity silicon substrates used in CMOS create a number of problems for RF circuits. Recent generations of CMOS technology have utilized a thin layer of epitaxial, high resistivity silicon for the active layer, grown on thick low resistivity bulk wafers to prevent latch-up[3]. This low resistivity substrate makes it difficult to isolate portions of the circuit from each other. Low resistivity substrates also compromise the quality of integrated passives, particularly integrated inductors. The p+ substrate of a typical digital CMOS process may have a resistivity as low as $0.01\,\Omega \cdot \mathrm{cm}$. These lossy substrates combined with low quality aluminum interconnects have limited the quality factor (Q) of inductors on silicon to less than 5. The bulk conductivity of aluminum is approximately $3.54 \times 10^7\,\mathrm{S/m}$ which is fairly high; however when alu-

[2]It is the belief of the author that Moore's law is a self-fulfilling prophecy. Fierce competition and consumer demand has forced companies to sink billions of dollars into digital semiconductor research, which has resulted in consistent improvements in the technology. Had a similar amount of research energy been devoted to an alternate technology it is likely that a similar gains would have been realized.

[3]Latch-up is a device failure that may occur in CMOS circuits when short pulses turn on a parasitic silicon controlled rectifier that exists across the substrate between devices. This phenomenon is discussed in [6].

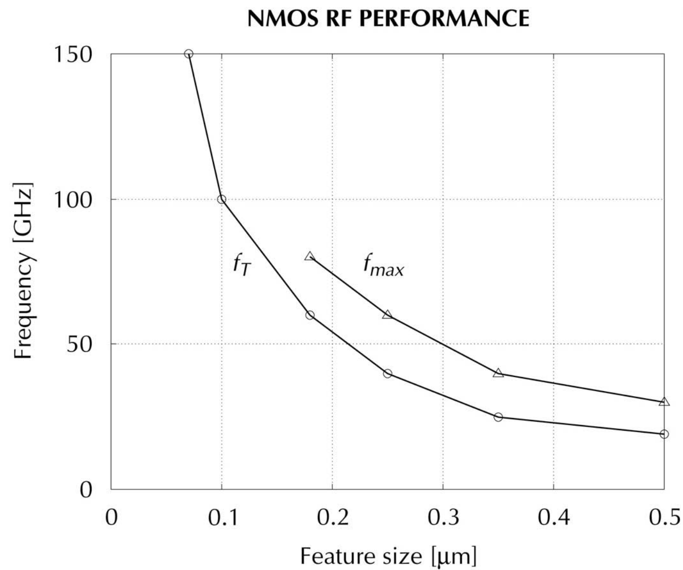


Figure 1.1: NMOS f_t and f_{max} versus feature size [1].

minum is deposited as a thin film its conductivity is much lower than this. Copper and gold metalizations do not suffer from large deviations between their bulk and thin film conductivities. The tradeoffs between CMOS, Silicon Bipolar, GaAs, and other technologies for RFIC applications are discussed at length in [5].

While the on-chip passive elements are likely to improve with lower resistivity copper interconnects, and high resistivity substrates may be utilized if circuits are carefully laid out to prevent latch-up, isolation will likely remain an important issue. If high density digital VLSI and RF circuits are to coexist in the same IC environment then the RF circuits will have to tolerate noise generated by the digital circuitry. This digital noise is typically large since the digital circuitry will have large amplitude swings (rail to rail in most logic circuits). It will most likely be strongest at harmonics (nf_{clk}) and sub-harmonics ($\frac{f_{clk}}{n}$) of the digital clock frequencies. Much of this noise arises from the currents that are necessary to charge the input capacitances of the various CMOS logic gates.

One circuit that may be noticeably degraded by the presence of digital switching noise is the voltage controlled oscillator (VCO). VCOs are critical components for signal

generation and frequency selection (i.e. the local oscillator) in RF transceivers. In addition, low jitter VCOs are important for the generation of clock signals in digital systems (Jitter is essential the time domain expression of phase noise.). VCOs are very sensitive to noise because they are free running, autonomous, systems[4]. Any noise coupled into the oscillator circuit can be amplitude or frequency modulated and appear on the noise skirts of the oscillator, compromising its spectral purity. For this reason the VCO is an excellent circuit to use as a test vehicle for investigating the effects of noise coupling in mixed digital/RF circuits. The investigation of these mixed-signal noise coupling issues was a primary motivation behind the design of the VCO presented in this thesis. However, the design of a CMOS oscillator with an integrated tank circuit is a significant effort unto itself, and it is to that goal that this thesis will be directed.

1.2 Recent work on LC CMOS VCO's

In this section a brief overview of recently reported CMOS VCOs will be presented. Many of the design issues and methods presented in these works will be discussed in detail in later chapters.

A number of LC CMOS VCO's have been reported recently in the literature. Craninckx and Steyaert presented a very complete treatment of VCOs based on both planar spiral inductors and bond wire inductors in [7]. This work also utilized Leeson's equation [8] to predict the phase noise of these oscillators. In [9], Lee and Hajimiri presented a comprehensive analysis of the phase noise of oscillators, which is applicable to both ring and LC oscillators. Their phase noise model is the first model to correctly account for the time-variant nature of oscillator circuits. They draw a number of interesting conclusions that may help designers reduce flicker ($\frac{1}{f}$) noise

[4]Even when frequency or phase locked in a control loop, noise in the loop will still modulate the VCO output

upconversion that is problematic in CMOS VCOs. Vora and Larson presented a 2 GHz VCO in [10], analyzing their design using both the linear methods of Leeson and the linear time-variant method of Hajimiri and Lee. Herzel et al, presented a CMOS VCO using MOS[5] varactor tuning and predicted its phase noise using linear methods [11]. Andreani and Mattisson presented a 2.4 GHz VCO using MOS varactors in [12] as well as a detailed analysis of the MOS varactor quality factor. Andreani also presents a comparison of VCO tuning with MOS varactors and junction varactors in [13].

Table 1.1 summarizes the performance of various monolithic LC CMOS VCOs that have been recently reported. The figure of merit (FOM) in this table results from normalizing the center frequency, phase noise offset, and power consumption so that each VCO can be objectively compared. This FOM is defined in [19] as:

$$VCO_{FOM} = \mathcal{L}(f_{offset}) - 20\,log\left(\frac{f_{osc}}{f_{offset}}\right) + 10\,log\left(\frac{P_{diss}}{1\,mW}\right), \tag{1.1}$$

where, $\mathcal{L}(f_{offset})$ is the phase noise at offset, f_{offset} with a center frequency of f_{osc} and an oscillator power consumption of P_{diss}. The units of this FOM are the same as phase noise: dBc/Hz. Lower (more negative) figures of merit represent better oscillator noise performance. This FOM does overlook some other oscillator parameters which are important such as output power, tuning range, and die area. However, since these parameters are not always reported in the literature it is difficult to present a complete comparison.

1.3 Overview of Thesis

This thesis follows in chronological order the design, implementation, and finally testing of the LC CMOS VCO circuit that is the focus of this work. Chapter 2 presents

[5] MOS varactors are a CMOS alternative to pn junction diode varactors that have been traditionally used. Varactors will be discussed in Chapter 4.

Table 1.1: Recently reported fully monolithic LC CMOS VCOs.

Reference	Tech. (μm)	f_o (GHz)	Phase Noise (dBc/Hz)	Tuning Range (MHz)	power (mW)	Voltage (V)	FOM (dBc/Hz)
Hajimiri [14]	0.25	1.8	-121 @ 600 kHz	?	6	1.5	-182.8
Craninckx [2]	0.7	1.8	-116 @ 600kHz	250	6	1.5	-177.8
Vora [10]	0.6	2	-103 @ 100 kHz	?	22	?	-175.6
Park [15]	0.5	0.9	-110 @ 200 kHz	126	6.6	3.3	-174.9
Herzel [11]	0.25	1.9	-100 @ 100 kHz	250	15	2.5	-173.8
Andreani [12]	0.8	2.4	-118 @ 1 MHz	350	22.5	2.5	-172.1
Razavi [16]	0.6	1.8	-100 @ 500 kHz	120	7.59	3.3	-162.3
Wong [17]	0.35	2	-87 @ 100 kHz	?	22.5	3	-159.5
Lam [18]	0.35	2.6	-110 @ 5 MHz	320	13	2.5	-153.2

a thorough analysis of the CMOS $-G_M$ oscillator. Chapter 3 explores the design of spiral inductors on a lossy CMOS substrate. Chapter 4 briefly surveys various topologies for varactors in CMOS and presents the design of a PMOS inversion mode varactor. Chapter 5 presents the final VCO design and its implementation in a 0.35 μm single-poly, 4-metal, digital CMOS process. Chapter 6 presents measurement results for the fabricated VCO. Chapter 7 concludes the thesis by comparing the results of this project with other fully integrated VCOs and suggesting a number of ideas for future work.

Chapter 2

$-G_M$ Oscillator Theory

In this chapter the theory of operation of CMOS negative transconductance ($-G_M$) oscillators will be presented. The material presented here provides the background that is necessary to understand the tank circuit and oscillator designs that are presented in the following chapters. Various $-G_M$ topologies are presented, and the complementary $-G_M$ topology used in this thesis is discussed in detail. The complementary $-G_M$ oscillator is treated as both an analog and a digital circuit providing a unique design perspective. Limitations of this topology and the calculation of its phase noise is also discussed.

2.1 Background

All LC oscillators can be represented as a simple feedback network as shown in Figure 2.1(a). The conditions for oscillation to occur are known as the Barkhausen criteria. These conditions require that the gain around the feedback loop equal unity and the total phase shift around the loop equal zero or some multiple of 360°. When these conditions are satisfied, a signal at the input of the gain stage will be amplified and

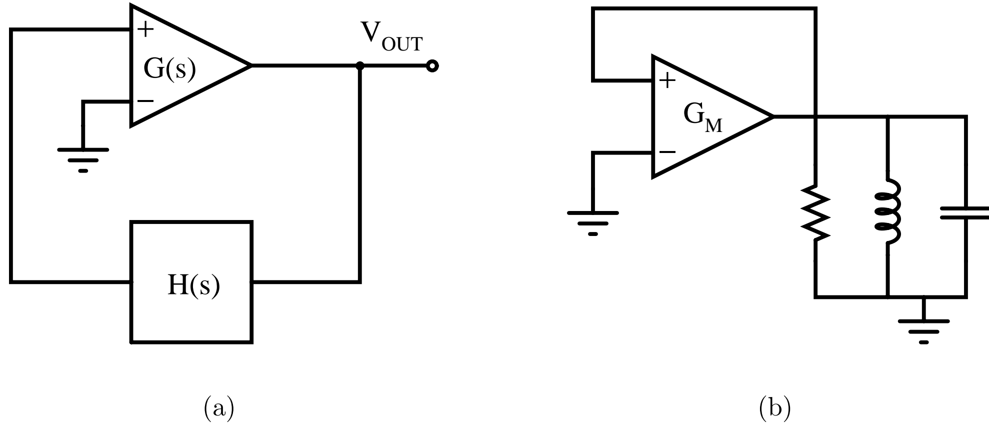


Figure 2.1: Feedback Oscillator Models. (a) Feedback Loop. (b) Transconductor.

returned back to the input in phase resulting in a self-sustaining signal. This feedback loop viewpoint is very useful for the analysis of LC oscillators and has been widely used to predict their behavior. This approach has been especially useful in describing the operation of traditional oscillators (based on single active devices) such as the Colpitts, Hartley, and Pierce oscillators.

An alternate way to describe the operation of oscillators involves the concept of *negative resistance*. Figure 2.1(b) shows a model of a simple negative resistance LC oscillator. In this figure the active device is a simple transconductance (G_M) amplifier connected in positive feedback to an LC tank circuit. It is straightforward to show that the tank circuit sees a negative resistance of -$\frac{1}{G_M}$ looking back into the transconductor output. It can be shown that if the Barkhausen criteria are satisfied this negative resistance will exactly cancel the equivalent parallel resistance of the tank circuit [20]. This makes sense because the active device must add enough energy to the circuit to cancel the total losses of the tank circuit—otherwise the circuit would simply behave as an underdamped system. Negative resistance oscillators have the property that they continue to generate a negative resistance when the tank circuit is removed. On the other hand, removing the tank circuit from a feedback oscillator breaks the feedback loop that creates the negative resistance and a negative resistance cannot be

measured [20]. Although both representations are equivalent, the negative resistance viewpoint will be utilized for the oscillator analyses of this thesis.

It is possible to implement an oscillator in CMOS technology using single active devices in traditional topologies such as the Hartley or Colpitts. However most recent implementations of CMOS LC oscillators have utilized a differential topology. Differential topologies are advantageous in integrated circuits, since they are less susceptible to supply noise that is often present in on-chip power rails. Furthermore, many integrated RF systems would benefit from the use of a differential local oscillator (LO) since typical integrated mixers are doubly-balanced Gilbert Cell topologies. In these case, the use of a differential oscillator eliminates the need for single-ended to differential conversion circuitry. The most popular differential oscillator topologies are the $-G_M$ oscillators, which utilize two cross-coupled transconductors (FETs) to produce a negative resistance similar to the transconductor of Figure 2.1(b).

2.2 $-G_M$ Oscillator Topologies

In order to understand the operation of the *complementary* $-G_M$ oscillator presented in this thesis, it is helpful to first examine its NMOS-only and PMOS-only counterparts. Figure 2.2 shows a simple NMOS $-G_M$ oscillator topology. The DC analysis of this circuit is simple since the inductors may be replaced by short circuits. The DC bias point is defined by $V_{GS} = V_{DD}$ and $V_{DS} = V_{DD}$. Assuming the NMOS devices to be long channel FETs (for conceptual purposes only, short channel devices are actually used in the final design), and neglecting the body effect, the drain current can be written as:

$$I_{DS} = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L} \right) (V_{GS} - V_{th})^2, \tag{2.1}$$

where μ_n is the surface mobility of the electrons in the NMOS channel, C_{ox} is the oxide capacitance per unit area, and V_{th} is the device threshold voltage. Thus the

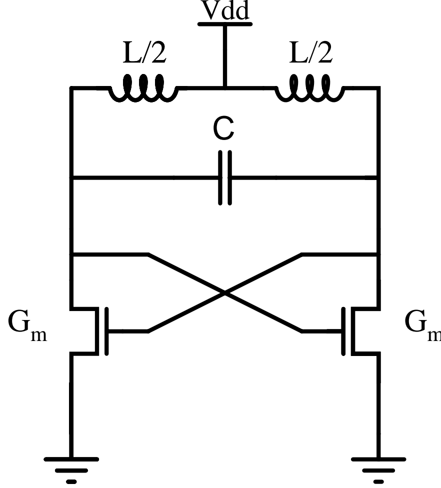


Figure 2.2: Simple NMOS $-G_M$ oscillator.

quiescent bias current $I_{DS(Q)}$ is easily calculated. In order to demonstrate how this circuit develops a negative resistance the FETs are replaced with their small signal models (Fig. 2.3). This is a low frequency equivalent circuit since the input capacitance of the FET has been ignored (this simplification will be justified later). The transconductance for a MOSFET is defined as:

$$G_M = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{Qpoint} = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{th}). \tag{2.2}$$

The input resistance seen looking into the cross coupled NMOS transistors can therefore be shown to be -$\frac{2}{G_M}$ (a full derivation of this negative resistance circuit is shown in Appendix A). In order for the circuit of Figure 2.2 to oscillate, the *magnitude* of this negative resistance must be *smaller* than the parallel resistance of the tank circuit.

$$\frac{2}{G_M} > R_p \tag{2.3}$$

The ratio of negative resistance, $\frac{2}{G_M}$, to the equivalent parallel resistance, R_p, is referred to as the *startup safety factor*. Integrated oscillators are usually designed with a startup safety factor of at least 2. It should be noted that this excess negative

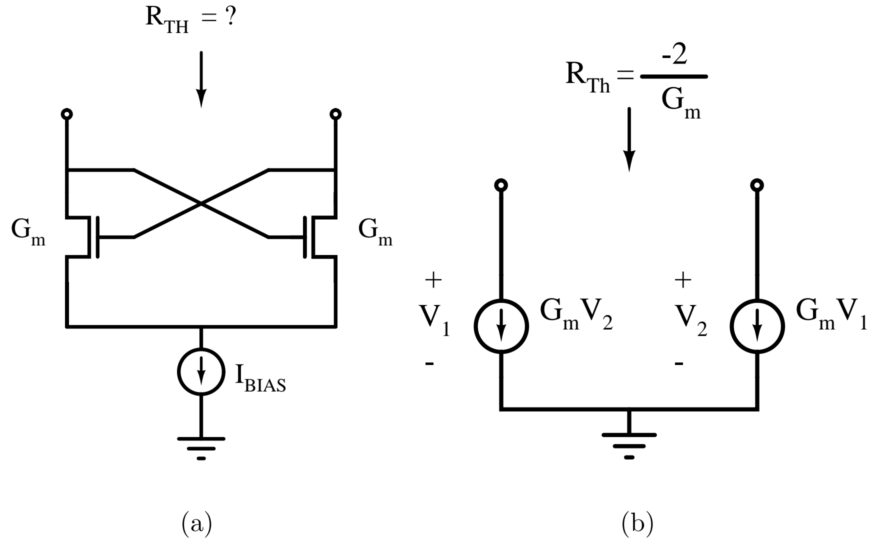


Figure 2.3: Cross coupled NFETs and DC equivalent circuit. (a) Cross coupled NFETs. (b) Small signal model of cross coupled NFETs.

resistance does not result in an exponentially growing oscillation amplitude since nonlinear effects ultimately limit the maximum voltage swing.

Four different topologies for $-G_M$ oscillators are shown in Figure 2.4. Figure 2.4(b) shows a PMOS implementation that is similar to the NMOS oscillator already discussed [shown again in Fig. 2.4(a)]. The analysis of this circuit is nearly identical, except for polarity differences. However, since the mobility of holes (μ_p) is lower than electrons, and the magnitude of the threshold of PMOS devices ($|V_{th}|$) is usually higher than NMOS devices, the PMOS devices will need to be roughly twice the size of the NMOS devices.

In the simple NMOS oscillator the DC bias was set by the supply voltage, since V_{GS} and V_{DS} were both equal to V_{DD}; thus, by Equation 2.2, the transconductance is defined solely by the size of the devices. This severely limits the flexibility of the circuit since the negative resistance is effectively controlled by the power supply voltage. Varying the negative resistance will also vary the oscillation amplitude. This is an extremely important fact since the phase noise performance (discussed in Sec.

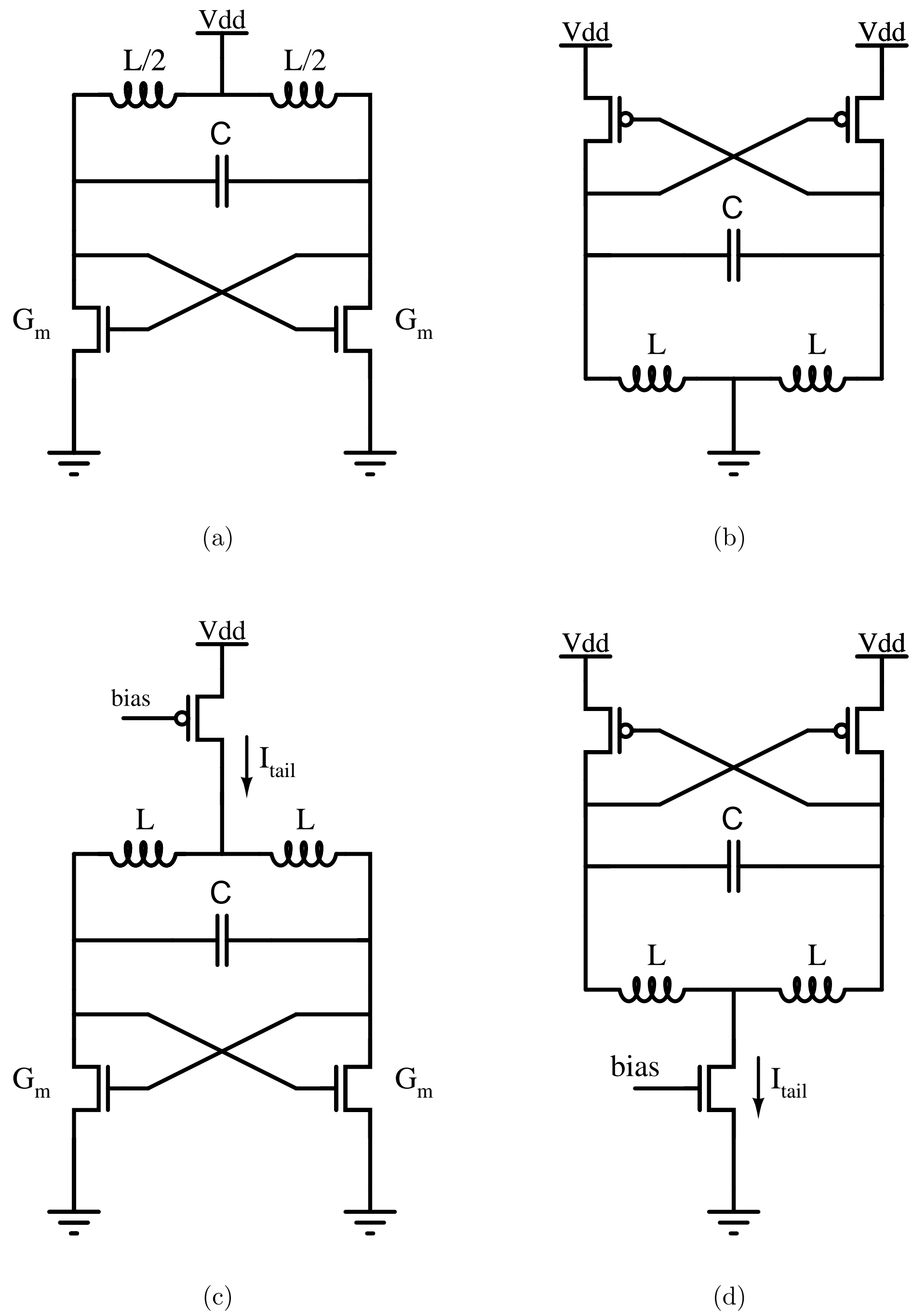


Figure 2.4: PMOS and NMOS $-G_M$ oscillators.

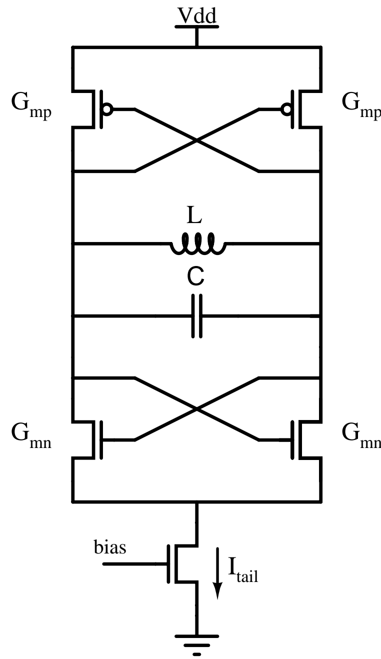


Figure 2.5: CMOS $-G_M$ Oscillator

2.6) of the oscillator depends directly on the oscillation amplitude. For these reasons it is desirable to have a means of controlling the negative resistance; this may be achieved by limiting the supply current. Figures 2.4(c) and 2.4(d) show the NMOS and PMOS versions of this circuit with a FET current mirror that can be used to control the bias current, and therefore the negative resistance of the circuit. The bias current that flows through the mirror device is referred to as the *tail current*. The value of this tail current also sets the total power dissipation of the oscillator. Having a means of controlling the bias current allows the designer to make the best compromise between phase noise and power dissipation. However in some cases it may be advantageous to eliminate the tail current source entirely since it will contribute device noise to the circuit.

The *complementary* $-G_M$ oscillator circuit is the result of using both PMOS and NMOS cross coupled pairs in parallel to generate the negative resistance. Figure 2.5 shows a simple CMOS $-G_M$ oscillator. Since the same bias current flows through both

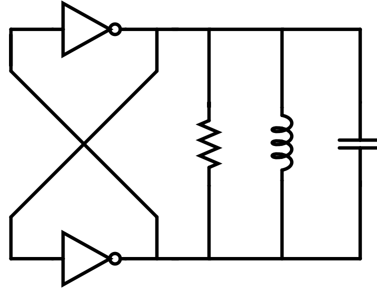


Figure 2.6: Cross coupled inverters

the PMOS and NMOS devices, the negative resistance can be twice as large for the same power consumption. Viewing the negative resistances generated by the PMOS and NMOS devices in the manner discussed above, the total negative resistance of this circuit is the parallel combination of the two individual cross-coupled FET circuits. Thus, the negative resistance is given by:

$$R_{negative} = \frac{-2}{G_{Mn} + G_{Mp}}. \tag{2.4}$$

It turns out that the left and right sides of this complementary $-G_M$ oscillator are identical to the structure of a CMOS inverter. This provides a very intuitive way to understand the operation of the complementary VCO. Figure 2.6 shows this circuit redrawn as a pair of cross-coupled inverters shunted with a tank circuit[1]. At DC the outputs of the inverters are shorted to their inputs through the inductor creating negative feedback which drives the inverters toward their switching points (usually near $\frac{V_{DD}}{2}$). A typical inverter transfer characteristic is shown in Figure 2.7. In this circuit the output of the inverter is forced to be equal to its input. At this bias point an inverter will operate as a high gain inverting linear amplifier rather than as a digital switch. However, at the resonant frequency of the tank circuit the positive feedback of the cross coupled inverters satisfies the necessary conditions for oscillation. It is also instructive to note the similarity between this circuit and the Pierce crystal oscillator,

[1]Digital designers will recognize these cross-coupled inverters as a latch. In digital systems the positive feedback creates memory, which is the foundation of sequential logic. Here the idea is the same but both the NMOS and PMOS devices operate in saturation.

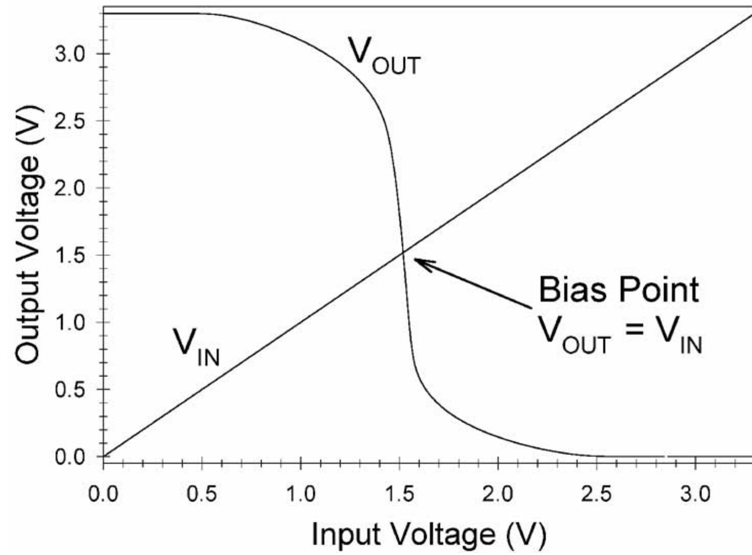


Figure 2.7: Inverter bias point.

which has often been used to generate accurate digital clock signals (Fig. 2.8). In the Pierce oscillator circuit the crystal acts as an inductance that resonates with the capacitors of the feedback π-network. Replacing the crystal with an inductor, and combining two of these circuits anti-parallel, yields the circuit of Figure 2.9(a). Combining the parallel inductors and capacitors of this circuit reduces it to the circuit of Figure 2.9(b). Recall that, since the circuit of Figure 2.6 is differential, the tank circuit elements can be split into grounded single ended elements by exploiting the virtual ground along the axis of symmetry in the circuit. Because of this virtual ground there is an equivalence between the single ended capacitors in the circuit of Figure 2.9(b) and the differential tank capacitance of Figure 2.6.

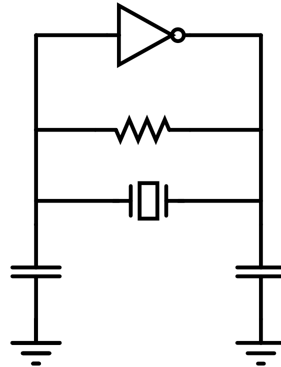
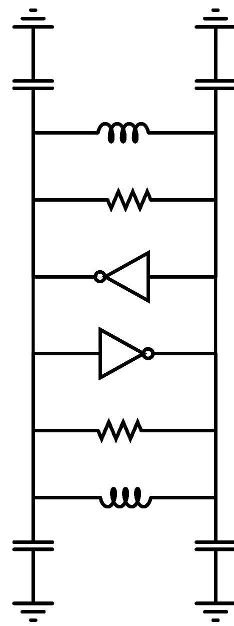
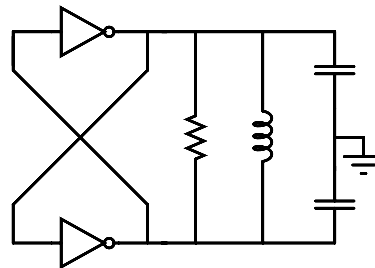


Figure 2.8: Pierce crystal oscillator.



(a) Anti-parallel



(b) Simplified Circuit

Figure 2.9: The complementary $-G_M$ oscillator as a Pierce oscillator.

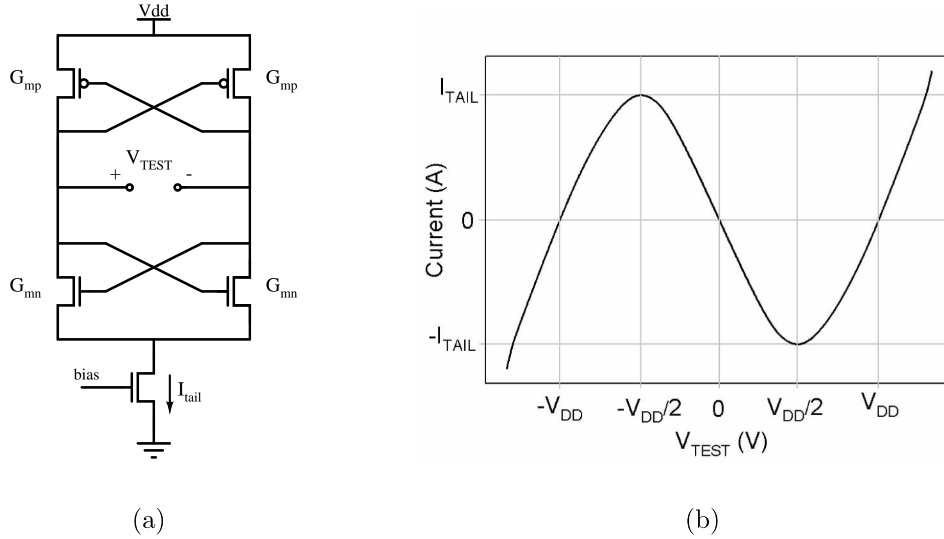


Figure 2.10: De-embedded nonlinearity. (a) Test circuit. (b) I-V characteristic.

2.3 Analysis of The Complementary $-G_M$ Oscillator

While the prior discussion gives a conceptual understanding of the operation of the complementary $-G_M$ oscillator, analyzing it as a negative resistance circuit is more useful for design purposes. To help understand the operation of this circuit the entire active portion of this circuit can be de-embedded as a simple static nonlinear I-V characteristic. This can only be done in simulation since, in reality, the negative resistance will try to sink power into the DC source (However, if a positive resistance is shunted across the negative resistance then the negative resistance can be de-embedded from the measurement of a positive resistance.). Figure 2.10(a) shows the test circuit that was used to de-embed the I-V characteristic shown in Figure 2.10(b). For differential voltages near zero the I-V characteristic has a negative slope, and thus exhibits a negative resistance. The negative resistance region extends from $-\frac{V_{DD}}{2}$ to $\frac{V_{DD}}{2}$, which is $3.3\,V$ for the work in this thesis. This simple nonlinear I-V curve can be used to simulate the $-G_M$ oscillator. Figure 2.11 shows a simple lossy

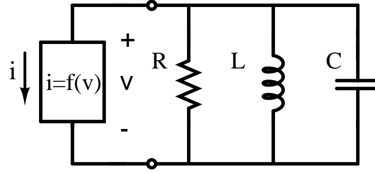


Figure 2.11: Ideal nonlinear oscillator circuit

tank circuit in parallel with a device having this nonlinear characteristic. This circuit can be simulated directly in a traditional (e.g. SPICE) circuit simulator if a suitable nonlinear voltage controlled current source is available. However, since this is a simple parallel circuit, the formulation of a differential equation is straightforward. Standard circuit analysis techniques yield:

$$\begin{aligned}
&\text{by KCL at the top node:} && 0 = f(v) + \frac{v}{R} + i_L + C\frac{dv}{dt} \\
&\text{the inductor voltage is:} && v = L\frac{di_L}{dt} \\
&\text{rearranging the first expression:} && i_L = -f(v) - \frac{v}{R} - C\frac{dv}{dt} \\
&\text{differentiating this expression} && \frac{di_L}{dt} = -\frac{d}{dt}f(v) - \frac{1}{R}\frac{dv}{dt} - C\frac{d^2v}{dt^2} \\
&\text{thus the inductor voltage is:} && v = -L\frac{d}{dt}f(v) - \frac{L}{R}\frac{dv}{dt} - LC\frac{d^2v}{dt^2} \\
&\text{rearranging the terms:} && LC\frac{d^2v}{dt^2} + \frac{L}{R}\frac{dv}{dt} + L\frac{d}{dt}f(v) + v = 0
\end{aligned} \tag{2.5}$$

This equation completely describes the oscillator, where $i = f(v)$ is the de-embedded nonlinearity. The circuit in Figure 2.11 was simulated using Spectre [21] and Equation 2.5 was solved using Mathematica [22]. A derivation of the relationship between oscillator amplitude and the parallel resistance is included in Appendix B. It is important to note that this model represents the *static* or DC nonlinearity of the circuit. Ideal capacitances can be added to the tank circuit to account for the parasitics of the device; However, it should be noted that the parasitic capacitances of the tank

are also nonlinear themselves[2]. Nevertheless this simple de-embedded nonlinear I-V curve does an excellent job of predicting the circuit behavior, and is extremely fast since computationally intensive BSIM3v3[3] [23] MOSFET equations are not evaluated with each iteration. The simulator need only compute the value of the function $f(v)$ and its derivatives for each iteration.

2.4 Frequency Limitations of $-G_M$ Oscillators

In the preceding analysis the parasitic resistances and capacitances of the MOSFETs were ignored. The parasitic capacitances of the gate-to-source region, C_{gs}, and the gate-to-drain region, C_{gd}, can be represented as a single capacitor in parallel with the tank capacitance. Figure 2.12 illustrates how C_{gd} appears directly in parallel with the tank circuit. The other parasitic capacitors can also be represented in parallel with the tank if a virtual ground is assumed. The net effect of these capacitances together will be to tune the oscillator to a lower frequency. This must be accounted for in the design if a specific center frequency is desired.

A more important effect of these parasitic capacitances is that they decrease the oscillator tuning range. This is because these capacitances are fixed, yet they contribute significantly to the total tank capacitance, leaving only a small portion of this capacitance for frequency tuning. Figure 2.13 shows a representation of the tank circuit with the varactor capacitance and the parasitic capacitance in parallel. The oscillation frequency is determined by the resonant frequency of the tank circuit :

$$f_o = \frac{1}{2\pi\sqrt{L(C_{parasitic} + C_{varactor})}} \tag{2.6}$$

As $C_{parasitic}$ becomes large relative to $C_{varactor}$ the oscillation frequency becomes less

[2] Indeed, the voltage dependence of the MOS capacitance will be used later to design a varactor for tuning the oscillator frequency

[3] "BSIM3 is a physics-based, accurate, scalable, robustic and predictive MOSFET SPICE model for circuit simulation and CMOS technology development." [23]

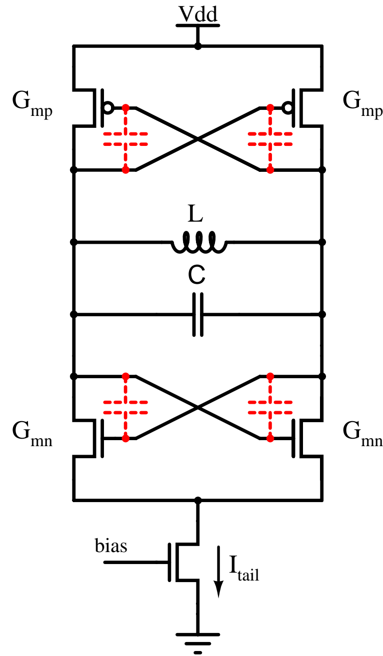


Figure 2.12: C_{gd} in parallel with tank circuit.

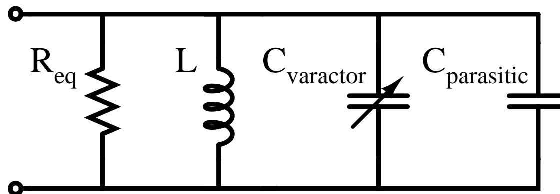


Figure 2.13: Tank circuit with parasitic capacitance in parallel

variable. The tuning range of an oscillator is often expressed as a ratio that is defined as:

$$\text{Tuning Range} = \frac{f_{max} - f_{min}}{f_{center}} = 2 \times \frac{f_{max} - f_{min}}{f_{max} + f_{min}} \tag{2.7}$$

Where f_{max}, f_{min}, and f_{center} are the maximum, minimum, and center frequencies respectively. If the varactor can tune from C_{min} to C_{max}, by combining Equations 2.6 and 2.7 and factoring out the common terms, the tuning range can expressed as:

$$\text{Tuning Range} = 2 \times \frac{\frac{1}{\sqrt{C_{parasitic}+C_{min}}} - \frac{1}{\sqrt{C_{parasitic}+C_{max}}}}{\frac{1}{\sqrt{C_{parasitic}+C_{min}}} + \frac{1}{\sqrt{C_{parasitic}+C_{max}}}} \tag{2.8}$$

It can be shown that the largest tuning range will be achieved when $C_{parasitic}$ is very small. This is a very important tradeoff in $-G_M$ oscillator design. Increasing the device size will increase the negative resistance yielding a large amplitude oscillation, but larger devices will have correspondingly larger parasitic capacitances. This tradeoff between device size and tuning range will dominate the design of the oscillator.

The discussion of Section 2.3 also ignored the impact of gate resistance. While the gate resistance of a properly designed MOSFET can be made very small by using multiple fingers (i.e. devices in parallel), it is important to understand that it is the gate resistance that is responsible for the upper frequency limit of the $-G_M$ circuit[4]. If there is a resistance in series with the gate capacitance of the cross coupled FETs then the negative resistance will have a low pass frequency characteristic. Figure 2.14 shows a simple small-signal MOSFET model with gate resistance (R_g) and the gate-to-source capacitance (C_{gs}) added. C_{gd} is ignored since it can be lumped into the tank circuit. The input admittance of a cross coupled FET pair using this small-signal model is given by (derived in Appendix A):

$$Y_{IN} = \frac{1}{2}\left(\frac{C_{gs} j\omega - 1}{1 + R_g C_{gs} j\omega}\right). \tag{2.9}$$

[4]The highest oscillation frequency for *any* active device is defined as f_{max}, the unilateral *power* gain frequency. f_{max} depends on device size, whereas f_t, the unity *current* gain frequency is independent of device size [24].

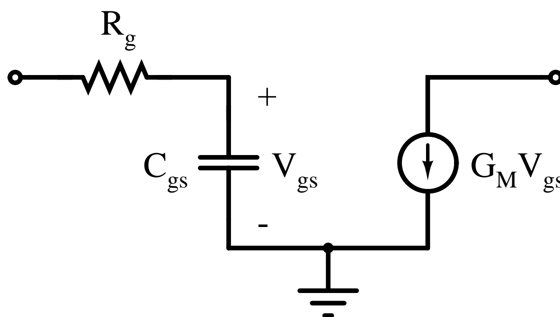


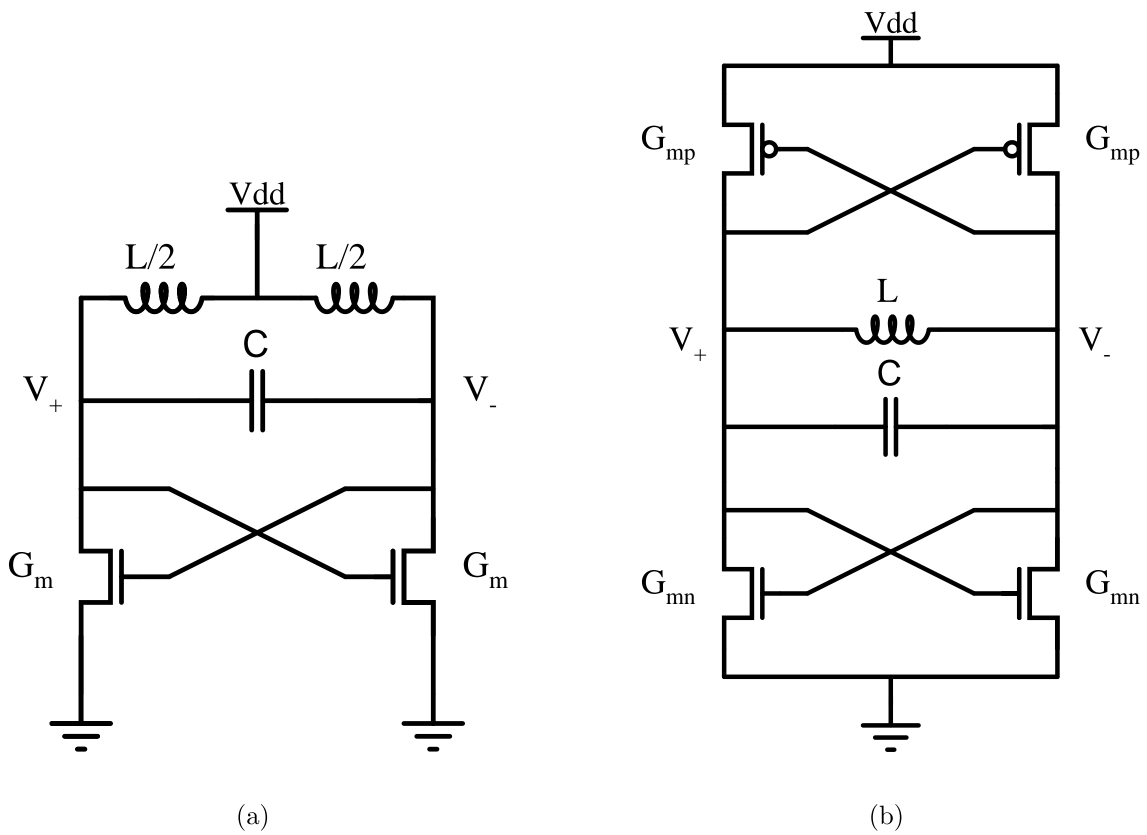
Figure 2.14: High frequency MOSFET model.

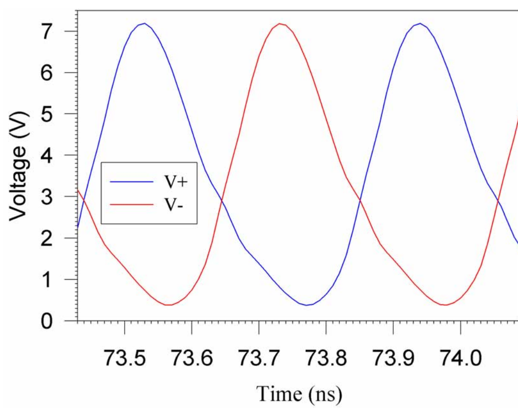
The input admittance contains a pole created by R_G and C_{GS}, which will tend to increase the magnitude of the negative resistance at higher frequencies. In most cases this pole will be well above 10 GHz, even for a poorly designed FET. However, this can still be a factor since the negative resistance will begin rolling off at frequencies lower than this pole frequency (recall that a pole represents a half power point, not a sharp transition frequency). In order to minimize the effect of this high frequency rolloff, the FETs must be laid out to minimize parasitic gate resistances. The gate resistance of a FET can be reduced significantly by using multiple fingers. Details on how this can be achieved for the circuits in this thesis are discussed in Chapter 5. Because the gate resistance of a MOSFET can be made very small, it can be advantageous to use MOS devices rather than BJTs in $-G_M$ oscillators. The high frequency limit would be much lower for a BJT VCO since the base resistance of BJTs is quite large [7]. However, a number of other important factors have made most BJT oscillator designs superior to those implemented in CMOS.

2.5 Advantages and Disadvantages of the Complementary $-G_M$ Oscillator

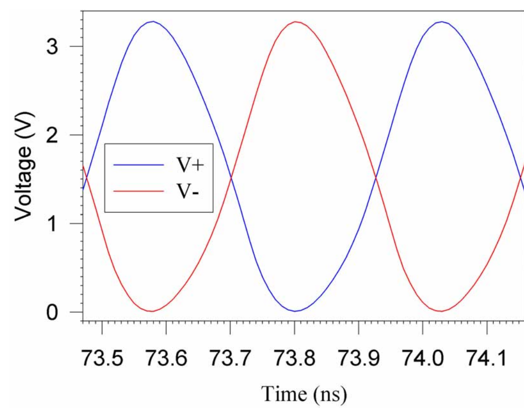
One important difference between the complementary $-G_M$ oscillator and its NMOS-only or PMOS-only counterparts is that in the complementary version, the differential voltage swing is limited to the supply voltage. This limitation is not present in the NMOS-only or PMOS-only versions. Figure 2.15 shows the output waveforms of an NMOS-only and a complementary $-G_M$ oscillator. In both cases the Q of the tank circuit is assumed to be high so that the oscillation amplitude overdrives the FETs. In the case of the NMOS only circuit the AC voltage at the drain of the transistors swings above V_{DD}. In the complementary circuit a similar voltage excursion is impossible since the PMOS transistors would be driven into cutoff, shutting off the bias current needed by the NMOS devices. Recall from Section 2.3 that the negative resistance of the complementary oscillator extends from $-\frac{V_{DD}}{2}$ to $\frac{V_{DD}}{2}$; thus, in the complementary oscillator, the maximum differential oscillation amplitude is approximately equal to V_{DD}. Therefore, the complementary oscillator is amplitude limited by both the supply voltage and the tail current source. On the other hand, the PMOS-only or NMOS-only versions are limited only by the bias current. Typically this is not a severe limitation for fully integrated CMOS VCO designs; since, for reasonably sized devices, the low quality factor of the tank will likely limit the oscillation amplitude long before supply voltage headroom becomes a concern. It should be noted that the distortion seen in the NMOS-only [Fig. 2.15(c)] waveform is typically not a problem since the output of the oscillator is typically limited to a square wave, either by logic or in the switching stage of an integrated mixer.

One slight advantage of the complementary topology is its ease of implementation as a pair of cross coupled inverters. For use in a digital system, the active part of the circuit could be implemented using existing inverter layout cells, although this is not likely





(c)



(d)

Figure 2.15: Amplitude limiting of NMOS and CMOS oscillators. (a) NMOS only oscillator. (b) Complementary oscillator. (c) NMOS only waveforms. (d) Complementary waveforms.

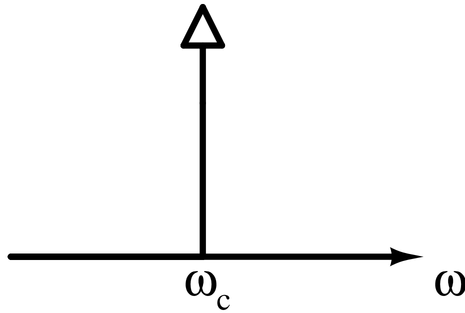


Figure 2.16: Ideal oscillator output spectrum

to result in an optimal design. In addition, the output voltages of the complementary oscillator are already at logic level (i.e. DC level = $\frac{V_{DD}}{2}$ with rail-to-rail swings) and interfacing to standard CMOS logic is straightforward. The complementary structure has also been shown to be advantageous for minimizing the upconversion of 1/f noise into near-carrier phase noise [9]. This is highly important in CMOS oscillator design since MOS transistors typically have a much higher 1/f noise corner than do BJTs. It is for these reasons, along with the elegant simplicity of the cross coupled structure presented in Sections 2.2 and 2.3, that the complementary $-G_M$ topology was chosen.

2.6 Oscillator Phase Noise

The most important characteristic of an RF oscillator is its frequency stability. An ideal oscillator would have a frequency spectrum that consists of a unit impulse centered at the output frequency (Fig. 2.16). In the time domain, such an oscillator would have an output voltage with the following form:

$$V_{out}(t) = A\,sin(\omega_0 t + \theta). \tag{2.10}$$

However, real oscillators are implemented with physical devices with inherent noise. This device noise manifests itself in both the amplitude and phase of the oscillator

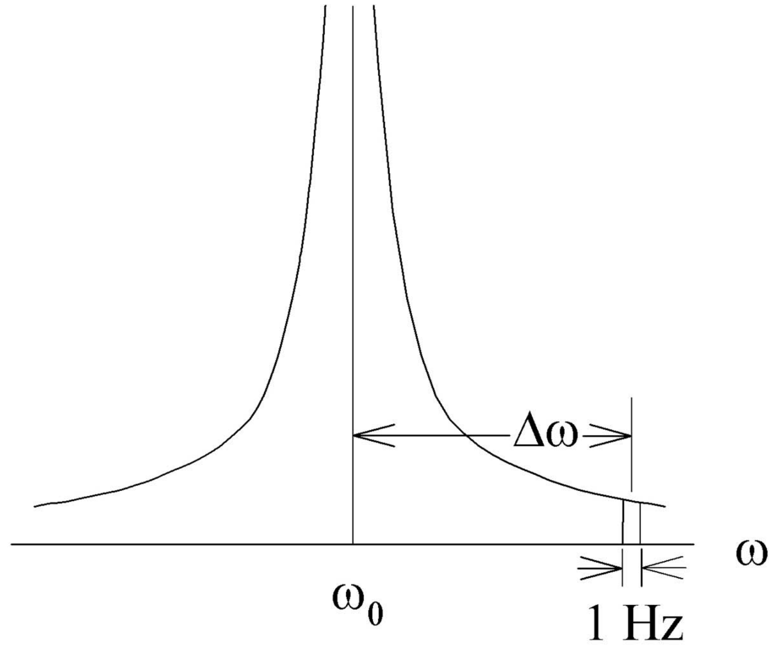


Figure 2.17: Phase noise in oscillator output spectrum

output such that the output of a practical oscillator is:

$$V_{out}(t) = A(t)\, sin(\omega_0 t + \theta(t)). \tag{2.11}$$

Since $A(t)$ and $\theta(t)$ are now functions of time, the frequency spectrum of V_{out} will contain noise sidebands near the oscillation frequency. Most oscillators have an inherent nonlinear limiting mechanism that attenuates $A(t)$. For example, the tail current and supply voltage limiting discussed in Section 2.5 limit the amplitude in the NMOS and CMOS $-G_M$ oscillators. In many RF systems the output of an oscillator is amplitude limited before it is used as an input to a mixer. When a waveform is amplitude limited some of the AM noise $[A(t)]$ that is present is converted to phase noise. For these reasons, only phase noise is usually considered.

Phase noise is quantified by considering the noise power (relative to the carrier power) in a $1\,Hz$ bandwidth at an offset $\Delta\omega$ from the carrier frequency (Fig. 2.17). The single-sided spectral noise density is defined by:

$$\mathcal{L}\{\Delta\omega\} = 10\, log\left(\frac{\text{Noise power at } (\omega_0 + \Delta\omega) \text{ in 1 Hz Bandwidth}}{\text{carrier power}}\right), \tag{2.12}$$

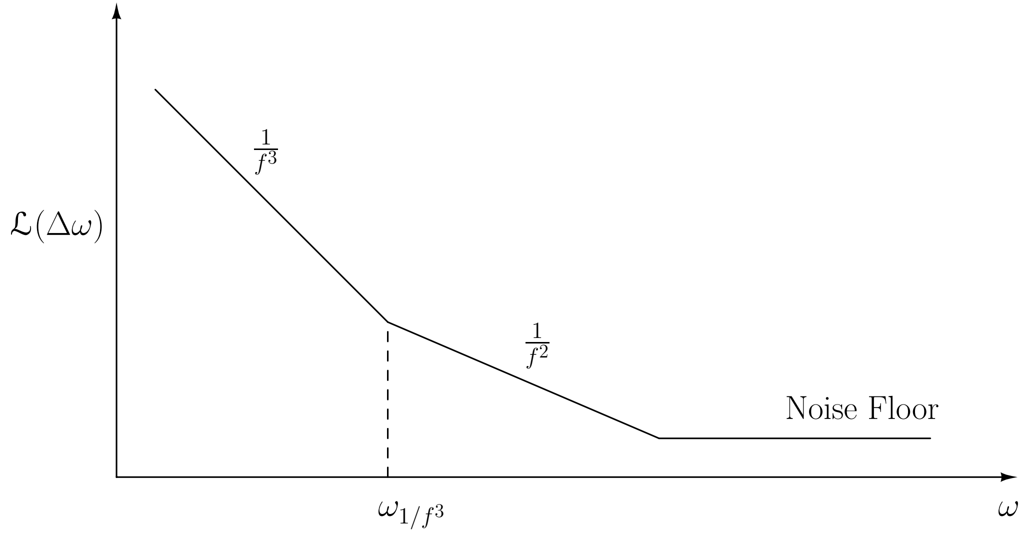


Figure 2.18: Typical oscillator phase noise spectrum

where the units are decibels below the carrier per Hertz (dBc/Hz). The phase noise of a typical oscillator versus offset frequency, $\Delta\omega$, is shown on a logarithmic frequency scale in Figure 2.18.

The phase noise of oscillators has been studied widely in the literature [8],[10],[25],[26]. A linear time invariant model for phase noise was presented by Leeson in [8] and was expanded upon in [7]. This model predicts the phase noise to be:

$$\mathcal{L}\{\Delta\omega\} = 10\,log\left\{\frac{2FkT}{P_s}\cdot\left[1+\left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right]\cdot\left(1+\frac{\omega_{1/f^3}}{\Delta\omega}\right)\right\}, \tag{2.13}$$

where F is the device excess noise factor, k is Boltzman's constant, T is the absolute temperature, P_s is the average power dissipated in the resonator, Q_L is the loaded quality factor of the resonator, and ω_{1/f^3} is the corner frequency between the $1/f^3$ and $1/f^2$ regions, shown in Figure 2.18 [9]. F and ω_{1/f^3} are empirical parameters which are seldom known during the initial design of an oscillator. F represents noise contributed by the active devices in the oscillator. This equation can correctly model all three regions of the typical phase noise characteristic shown in Figure 2.18 if F and ω_{1/f^3} are accurately known. However this is not often the case for the circuit designer, since F does not include nonlinear frequency conversion effects, and ω_{1/f^3}

is typically not the same as the device $1/f$ noise corner. Accurate predictions of phase noise using Leeson's equations have been limited to relatively high Q, discrete oscillator designs. A key problem with Leeson's equation is that this model assumes that oscillators are linear, time-invariant (LTI) systems, which in practice is never the case [25].

A more accurate time domain model has been proposed by Hajimiri and Lee in [9]. This model more accurately accounts for all the processes involved in converting device noise into phase noise. The linear time variant (LTV) phase noise model is able to account for the upconversion of $1/f$ device noise into low offset phase noise (i.e. $1/f^3$, etc). The time variant model also more accurately models the noise folding that translates noise at harmonics of the oscillation frequency into the phase noise skirts of the fundamental frequency. The LTV phase noise model introduces the concept of the impulse sensitivity function (ISF), $\Gamma(\omega_0\tau)$, which expresses the phase change introduced into an oscillator as a function of the time in the oscillation the impulse is introduced. Using this approach Hajimiri and Lee show that the upconversion of $1/f$ noise can be minimized by minimizing the DC coefficient C_0 of $\Gamma(\omega_0\tau)$. In the case of an LC oscillator, $\Gamma(\omega_0\tau)$ depends on the *symmetry* of the waveform. The conclusion drawn in [9] is that the complementary $-G_M$ oscillator can suppress the upconversion of $1/f$ noise, since it can be designed to create a more symmetrical output waveform than non-complementary designs. Recall from Figure 2.15 that the NMOS-only oscillator has a quite asymmetric waveform.

While the LTV phase noise model is generally believed to be the most accurate method reported for determining the phase noise of an oscillator, it is not very straightforward to implement in practice. The difficulty lies in the calculation of $\Gamma(\omega_0\tau)$, which must be calculated and minimized for each node of the circuit. In addition, accurate noise models for CMOS devices are often unavailable to RF designers.

To simplify matters in this work, phase noise is predicted using the simple expression

[7]:

$$\mathcal{L}\{\Delta\omega\} = \frac{kTR_{eff}[1+A]\left(\frac{\omega_0}{\Delta\omega}\right)^2}{V_A^2/2}, \tag{2.14}$$

where R_{eff} is the equivalent series resistance, V_A is the peak voltage amplitude across the tank circuit, and A is the excess noise factor which is set equal to the oscillator startup safety factor (the ratio of equivalent parallel resistance to the negative resistance). The reason for setting A equal to the startup safety factor is intuitive: if $A = 0$ the active devices contribute no noise to the oscillator; if $A = 1$ the active and passive devices contribute equal amounts of noise. By setting A equal to the startup safety factor, the active devices contribute proportionally more more noise than the passives. R_{eff} is not a physical resistance component, but rather a way of representing the total loaded quality factor of the tank circuit. This expression is therefore equivalent to Leeson's basic equations. A derivation of this expression is found in [7]. This model enabled straightforward hand calculations of phase noise (in the $\frac{1}{f^2}$ region) during the design phase.

Chapter 3

Inductor Design

3.1 Background

An important quantity in the characterization of resonant tank circuits is the quality factor (Q), which is defined as:

$$Q = 2\pi \frac{\text{maximum energy stored}}{\text{energy dissipated per cycle}}. \tag{3.1}$$

The resonator Q will strongly influence both the phase noise and the power consumption of an oscillator. The inductor in an LC oscillator is usually the most critical circuit element in the design—typically, the Q of the inductor dominates the total Q of the tank circuit. In addition, the tuning range of a VCO is strongly affected by the self-resonant frequency (f_{sr}) of an inductor. The self resonant frequency is that frequency at which capacitive parasitics result in a zero net reactance; beyond this frequency the inductor becomes capacitive.

Traditionally, inductors have been incorporated as discrete components located off-chip (often as small surface mount parts). While off-chip inductors can have extremely good performance, it is desirable to eliminate as many discrete components as possible. This reduces the board-level complexity and component count, which in turn

leads to a direct reduction in cost. As an alternative to off-chip inductors, some RF integrated circuits have utilized bonding wires as hybrid inductors [7],[27]. While bonding wires can have a relatively high Q (on the order of 50), they can also suffer from large variations in inductance value since wire bonding is a mechanical process that cannot be as tightly controlled as a photolithographic processes.

Monolithic inductors fabricated as simple planar spirals are now widely used on GaAs substrates with Q's in the range of 10-20. The inductance of a monolithic inductor is defined solely by its geometry. Modern photolithographic processes provide extremely tight geometric tolerances. For this reason monolithic inductors have very small variations in their performance.

Unlike standard Si technologies, GaAs processes are more conducive to the fabrication of monolithic inductors since the GaAs substrate is a nearly perfect insulator ($\rho \cong 10^8\,\Omega \cdot cm$) and the metalization used is often thick electroplated gold ($\sigma \cong 4.1 \times 10^7\,S/m$). Silicon substrates have a resistivity that varies from $10 - 100\,\Omega \cdot cm$ for Bipolar and BiCMOS to as low as $0.01\,\Omega{\cdot}cm$ on some digital CMOS processes. Furthermore, the metalization has traditionally been aluminum which has a low thin-film conductivity (although copper has appeared recently as an alternative interconnect metal [28],[29]). Monolithic inductors are becoming popular for BiCMOS technologies, especially the newer SiGe processes which are tailored for RF design [30]. However, these processes are still more costly than the standard digital CMOS process. The dream of many RFIC designers is to be able to leverage the same economies of scale that have supported Moore's law for nearly two and a half decades for the realization of RF systems. For this reason, much recent effort has been focused on the problem of fabricating RF inductors in CMOS processes. In this chapter monolithic inductor design in a generic[1] digital CMOS process is explored.

[1]generic = low-resistivity substrate, single layer of poly, strict adherence to DRC rules, and no extra post-processing steps.

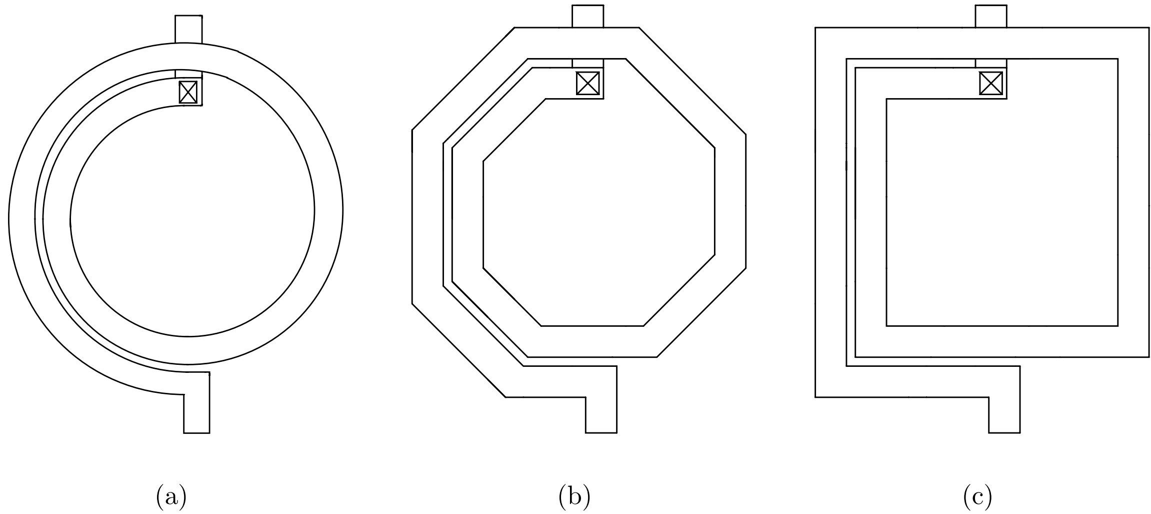


Figure 3.1: Spiral inductor geometries: (a) circular spiral. (b) octagonal spiral (c) square spiral.

3.2 Inductor Geometries

There are many ways to lay out a planar spiral inductor. The optimum structure is a circular spiral. This structure [Fig. 3.1(a)] places the largest amount of conductor in the smallest possible area, reducing the series resistance (R_s) of the spiral. This structure, however, is not often used because it is not supported by many mask generation systems. Many of these systems are able to only generate Manhattan (Manhattan style layouts only contain structures with 90 degree angles, like the streets of Manhattan, NY.) geometries (and possibly 45° angles as well). While the curved metal traces can be approximated in a step-wise fashion, a simpler solution is to approximate the circle with a polygon. Figure 3.1(b) shows an octagonal spiral that only requires the mask maker to generate 45° angles in addition to the standard Manhattan geometries. This structure has a Q that is slightly lower than the circular structure, but is much easier to layout. For the CMOS process used in this thesis non-Manhattan-style shapes are allowed but not recommended. For this reason the standard square spiral structure of Figure 3.1(c) was chosen. The square spiral structure does not have the

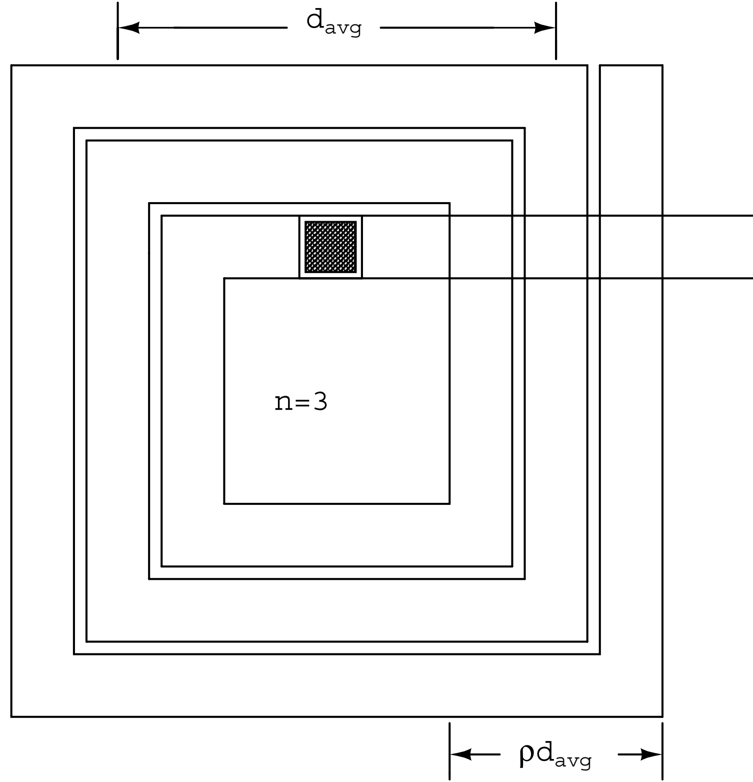


Figure 3.2: Parameters for Equation 3.2.

best performance but it is one of the easiest structures to lay out and simulate.

The square spiral inductor has been studied extensively in [29],[31],[32]. The following recently published expression has demonstrated good accuracy for predicting the inductance of a square spiral [33]:

$$L = \frac{2\mu_0 n^2 d_{avg}}{\pi}\left[\ln\left(\frac{2.067}{\rho}\right) + 0.178\rho + 0.125\rho^2\right], \tag{3.2}$$

where n is the number of turns in the spiral, and the parameters d_{avg}, and ρ are defined in Figure 3.2. μ_0 is the permeability of free space, d_{avg} represents the average diameter of the spiral, and ρ represents the percentage of the inductor area that is filled by turns. Equation 3.2 is based on a current sheet approximation of the spiral structure, and is valid only for square spirals[2]. Predicting parameters such as inductor

[2]Reference [33] also presents a range of expressions that are valid for other geometries.

Q and Self Resonant Frequency (f_{sr}) generally cannot be done with a simple formula. These parameters are usually obtained through simulation.

3.3 Losses in spiral inductors

There are several sources of loss in a spiral inductor. The most obvious loss mechanism is the series winding resistance, R_s. The interconnect metal used in most CMOS processes is aluminum. Depending on the metalization thickness and particular alloy used, the sheet resistivity can be anywhere from 30-70 $m\Omega/\Box$. The DC resistance of the spiral is easily calculated as the product of this sheet resistance and the number of squares in the spiral. However, at higher frequencies the resistance of the spiral increases due to the skin effect and current crowding at the corners of the spiral.

As mentioned above, the introduction of copper metalization and thick upper-level interconnect have yielded improvements in the maximum inductor Qs that have been reported in CMOS [29]. In addition, multiple levels of metalization may be strapped together to create a spiral with a lower DC winding resistance [34]. However, substrate losses ultimately remain the limiting factor even when the conductivity of the spiral windings is no longer an issue. Since the silicon substrate is neither a perfect conductor nor insulator there are resulting losses in the reactive fields that surround the windings of the spiral.

Figure 3.3 shows the losses due to the electric fields in the inductor structure. In a CMOS process the windings of the spiral are separated from the substrate by a thin layer of silicon dioxide (SiO_2). This creates a capacitance between the spiral and the surface of the substrate. In most digital CMOS processes, this substrate is heavily doped p+ material and is tied to ground potential. Thus, the substrate appears as a grounded resistor in series with this capacitance. This substrate capacitance has two detrimental effects in a circuit: (1) it allows RF currents to interact with the substrate,

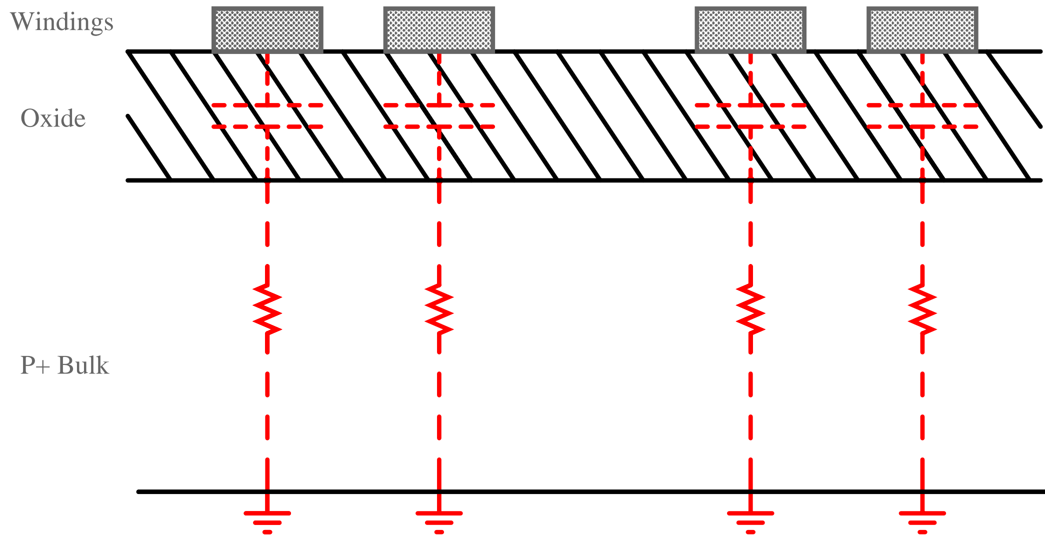


Figure 3.3: Electric field (capacitive) losses.

lowering the Q of the circuit; (2) it increases parasitic capacitances, reducing the self resonant frequency (f_{sr}). This capacitance can be reduced by decreasing the area occupied by the inductor traces, but this in turn will increase the series resistance of the inductor. This is an important tradeoff, since wide traces are generally used in inductors on silicon to overcome the low thin-film conductivity of the metalization. This also limits the feasibility of creating arbitrarily large valued inductances.

Figure 3.4 shows the losses due to the magnetic field in the inductor structure. The magnetic field $\vec{B}(t)$ extends around the windings of the spiral and into the substrate. Faraday's Law states that this time-varying magnetic field will induce an electric field in the substrate. This field will force an *image current* to flow in the substrate in the opposite direction of the current in the winding directly above it. These image currents can account for 50 percent or more of the losses in a CMOS inductor [7]. This effect can also be thought of as a parasitic transformer, where the substrate represents an unwanted secondary winding. Larger inductors will have magnetic fields that penetrate deeper into the substrate, and will therefore suffer from higher substrate losses. This effect is in opposition to the goal of limiting series resistance

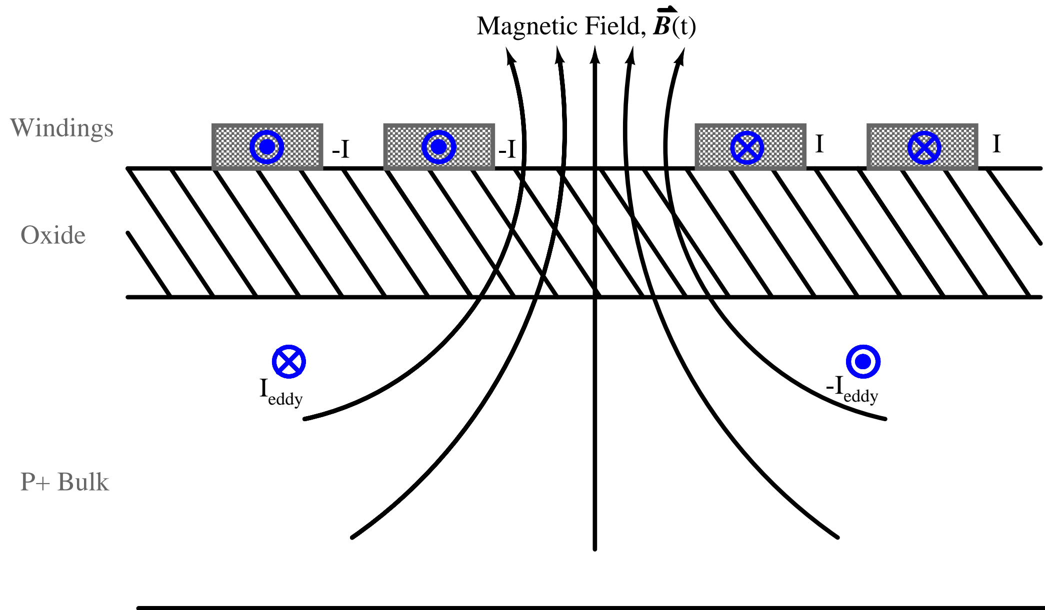


Figure 3.4: Magnetic field (inductive) losses.

with wide spiral traces. The substrate effects could be avoided by utilizing a post processing step to etch the substrate away under the inductor [35], however for this research no non-standard processing steps were used. Using such exotic processing steps would defeat the purpose of implementing an RF circuit in a *standard* digital CMOS process.

The magnetic field will not only penetrate into the substrate but also into the other windings of the coil, further increasing the loss [7]. Figure 3.5 shows the eddy currents that are generated in the center of a winding. This effect causes the inner turns of the inductor to contribute much more loss to the inductor while having a minimal impact on the actual inductance. This phenomenon is sometimes referred to as "current crowding" [2],[36]. In [2] a 9 turn inductor was simulated using a finite-element field solver. It was found that the resistance of the outer turn at 2 GHz was 18% higher than its DC value; however, the resistance of the inner turn at 2 GHz increased by 480% over its DC value. For this reason spiral inductors on silicon typically utilize "hollow" centers in order to increase their Q [7].

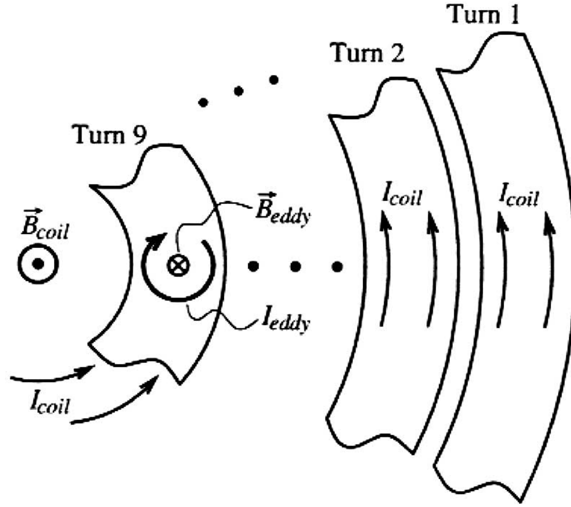


Figure 3.5: Eddy currents in the spiral windings [2].

3.4 Inductor Circuit Models

A circuit model for a monolithic inductor on a low-resistivity substrate is shown in Figure 3.6 [32]. This model includes circuit elements that model the loss mechanisms that were discussed in Section 3.3. This circuit accurately models inductors on low resistivity silicon substrates since it includes the effect of the magnetic eddy currents. The magnetic substrate loss is represented in this model as an ideal transformer coupled to the resistor, $R_{sub(m)}$.

Some confusion exists in the literature regarding how the quality factor (Q) and inductance (L) of a monolithic inductor should be defined, particularly with regard to differential (balanced) versus single-ended (unbalanced) implementations. Typically, the inductance of a monolithic inductor is calculated by converting measured or simulated S-parameters into Y-parameters. These Y-parameters are then used to extract the value of L and Q. In cases where one side of the inductor is grounded (i.e. single-ended or unbalanced), L is often defined as:

$$L = Im\left(\frac{\frac{1}{Y_{11}}}{2\pi f}\right). \tag{3.3}$$

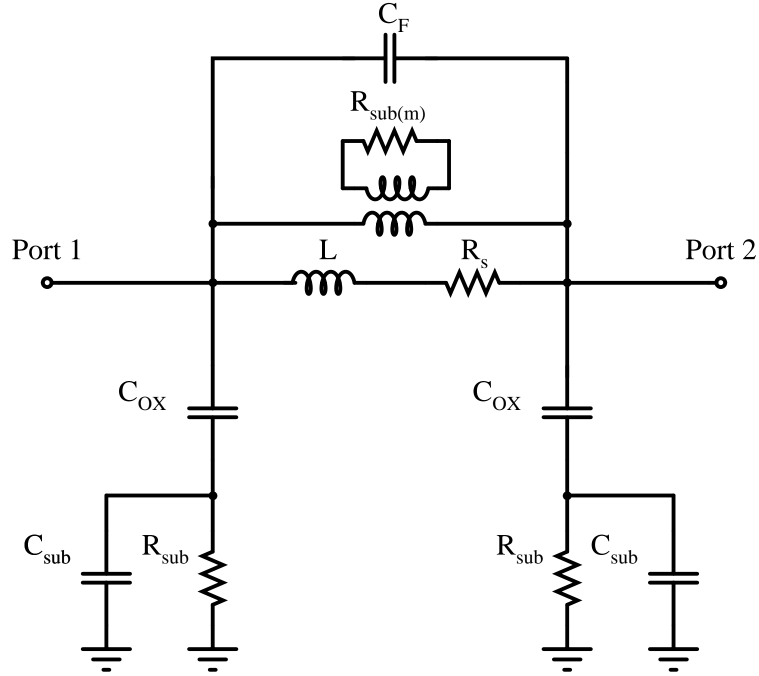


Figure 3.6: Spiral inductor lumped circuit model.

In other cases where the inductor is used differentially (i.e. balanced), L is often defined as [32],[37],[31]:

$$L = Im\left(\frac{\frac{1}{Y_{12}}}{2\pi f}\right) \tag{3.4}$$

Depending upon the inductor application either of these expressions may be acceptable.

To understand the difference between the above definitions it is helpful to look at the π equivalent of a two-port network (Fig. 3.7). This circuit model expresses the two-port Y-parameters as admittances in a π network. For a passive reciprocal network, $Y_{12} = Y_{21}$. If the network is symmetric, $Y_{11} = Y_{22}$. To define inductance and quality factor, this π model must be reduced to a single element (i.e. an inductance in series or parallel with a resistance). For the case of a simple series element $R + jX$:

$$L = \frac{X}{(2\pi f)} \tag{3.5}$$

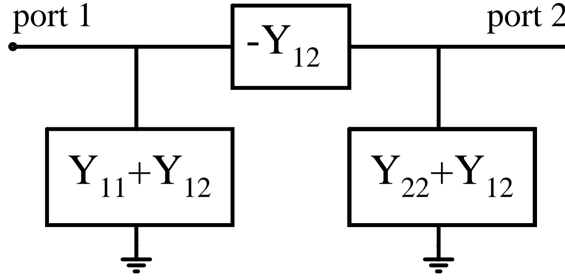


Figure 3.7: π equivalent circuit for a two-port network.

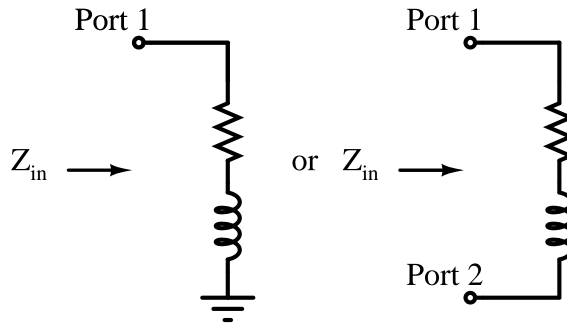


Figure 3.8: Two methods of reducing π-network.

and

$$Q = \frac{X}{R}. \tag{3.6}$$

There are two simple methods of reducing the π-circuit to the series element, $R + jX$ (Fig. 3.8). If port 2 of the π-circuit is grounded, the $Y_{22}+Y_{12}$ element is bypassed and the circuit looking *into* port 1 reduces to the admittance Y_{11} connected to ground (since admittances in parallel add, Y_{12} is eliminated). Converting admittance to impedance, $R + jX$ becomes:

$$R + jX = \frac{1}{Y_{11}}. \tag{3.7}$$

If this assumption is valid, then L and Q may be defined using:

$$L = Im\left(\frac{\frac{1}{Y_{11}}}{2\pi f}\right). \tag{3.8}$$

and

$$Q = \frac{Im(\frac{1}{Y_{11}})}{Re(\frac{1}{Y_{11}})}. \tag{3.9}$$

This method is valid if the inductor will be used in a circuit where one terminal of the inductor is connected to AC ground. This is often the case in many RF circuits, particularly in LNAs and mixers, where inductors are used for degeneration or loading. This method is also equivalent to taking one-port S-parameter measurements with one terminal of the inductor grounded, and converting the measured reflection coefficent, Γ, into an input impedance. Using this approach with port 2 grounded yields:

$$\Gamma_1 = S_{11} - \frac{S_{12}S_{21}}{1 + S_{22}}. \tag{3.10}$$

The series impedance is then given by:

$$R + jX = Z_{in} = Z_0 \frac{1 + \Gamma_1}{1 - \Gamma_1}, \tag{3.11}$$

which is equivalent to Equation 3.7.

On the other hand, if the inductor will be used in a differential configuration (i.e. neither port is at AC ground potential) a different approach is required. The *floating* impedance, $R + jX$, seen *between* ports 1 and 2 of the π-network is:

$$R + jX = \left(-\frac{1}{Y_{12}}\right) \Big\| \left(\frac{1}{Y_{11} + Y_{12}} + \frac{1}{Y_{22} + Y_{12}}\right) = \frac{Y_{11} + Y_{22} + 2Y_{12}}{Y_{11}Y_{22} - Y_{12}^2}. \tag{3.12}$$

Since in this case, the shunt elements $Y_{11} + Y_{12}$ and $Y_{11} + Y_{12}$ of the π network are the parasitic capacitances to ground (perhaps in series with a substrate resistance, see Fig. 3.6), they are often ignored (particularly in technologies using insulating substrates) and L is calculated using Equation 3.4 [32],[37]. The impedance calculated in Equation 3.12 is referred to as *floating* since it ignores the ground connection in the equivalent circuit. This is valid, since if the inductor is connected in this manner, the ground as represented in Figure 3.7 is no longer explicit and exists only as a *virtual ground*. Inductors connected in this manner are often referred to as *floating* or *differential* and L and Q can be defined as:

$$L = Im\left(\frac{\frac{1}{Y_{12}}}{2\pi f}\right) \tag{3.13}$$

$$Q = \frac{Im(\frac{1}{Y_{12}})}{Re(\frac{1}{Y_{12}})}. \tag{3.14}$$

In most cases the differential Q measured using this method will be slightly higher (3-5 percent) than in the grounded one port case. If the shunt elements $Y_{11} + Y_{12}$ and $Y_{11} + Y_{12}$ are not negligible (as is the case in standard CMOS) it is more accurate to use Equation 3.12 in conjunction with Equations 3.5 and 3.6 to calculate L and Q rather than Equations 3.13 and 3.14.

In this thesis both methods of reporting L and Q are used. Although the total tank inductance is floating, it will actually be implemented as two identical inductors in series. While, the total tank inductance uses the differential inductor definitions, each individual inductor is considered using the simplified one port approach. Where not explicitly stated, subsequent references to L and Q in this thesis should be considered to follow this convention.

3.5 Inductor Simulation

Although the inductance value can be computed using Equation 3.2, or other similar expressions found in the literature, it is difficult, if not impossible, to accurately predict analytically the losses associated with a spiral inductor. This necessitates the use of electromagnetic field solvers. Initially the inductors in this project were simulated using the freeware program ASITIC [38], However, it was found that this program underestimated the magnetic substrate eddy current effects. More accurate simulations were obtained using Sonnet EM [39]. Sonnet EM is a planar full-wave EM solver (method-of-moments) package that can accurately calculate the fields and currents of a planar structure such as a spiral inductor. Sonnet EM accurately calculates the fields in the substrate and the dielectric, but does not account for the effects of the finite metal thickness. 2D and 2.5D planar simulators such as Sonnet EM assume the conductive layers to be infinitesimally thin, with a finite sheet resistivity. Thus,

the capacitance between the spiral windings and the eddy currents in the windings are not modeled. In order to achieve the most accurate simulation possible a full 3-D finite-element simulation must be done. Programs such as Agilent HFSS [40] can be used to do this at the expense of long simulation times. Such complete simulations were not done in this thesis.

These electromagnetic field solvers report their simulation results in S-parameters. These results can then be numerically fitted to the circuit model of Figure 3.6. However, a number of the component values in this circuit model vary with frequency (both the skin effect and the substrate losses vary with frequency). For this reason it may be desirable to simulate circuits with inductors by directly using the S-parameter data extracted from the field solver. Advanced circuit simulators such as Spectre can accept S-parameters directly and use a convolution based method to perform transient time-domain simulations [21],[41]. Both methods were used in this thesis; the latter method is much slower because it is computationally intensive to evaluate S-parameters in the time domain. On the other hand, frequency-domain simulators using techniques such as harmonic balance work well with S-parameter files; however, for oscillator design a time-domain approach is preferred.

3.6 Final inductor design

The inductors for this project were designed primarily by iteration. Originally 2.5 GHz was the desired frequency of operation and most of the simulations were focused on obtaining oscillation near this frequency. However, the goal of this project was not as much to design an oscillator for a specific frequency range, but rather to implement a benchmark oscillator that could be used explore mixed-signal noise effects. Since a tank circuit with C=1 pF and L=4 nH resonated near 2.5GHz, this was the chosen starting point for the design. The ASITIC inductor simulation tool was used initially

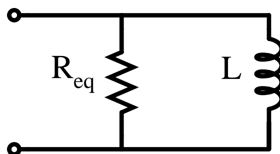


Figure 3.9: Simple parallel RL inductor model.

to calculate the inductance and quality factor of a variety of structures; Sonnet EM was used for the final comparison of various structures. It was found from the literature [7],[9],[12], that the outside diameter of a $4-6\,nH$ spiral inductor in CMOS technology is typically in the range $200-300\,\mu m$. This was used as a guideline for most of the inductor geometries that were explored.

During the inductor design, the tradeoff between inductor size and oscillator current drain also served as a guideline. Large valued inductors will reduce current drain in the oscillator. This happens because larger inductors have larger equivalent parallel resistances. If the inductor is modeled as an ideal inductance with a shunt resistor R_{eq} (Fig. 3.9) then:

$$R_{eq} = Q2\pi f_o L. \tag{3.15}$$

Larger values of R_{eq} are desirable because the active portion of the circuit will be required to generate less negative resistance to sustain oscillation and thus consume less current. However, as L is increased, its self-resonant frequency decreases because its parasitic capacitances also increase. Larger inductances will also decrease the oscillator tuning range. This occurs because a smaller tank capacitance is required to achieve the desired oscillation frequency. As the tank capacitance becomes smaller, it gets swamped out by the parasitic capacitances. As was discussed earlier, larger area inductors will also have an increased substrate loss, since their magnetic fields penetrate deeper into the substrate. All these factors must be considered when designing the inductor. The feasibility of using a larger inductor is limited by the parasitics that will be associated with the active circuitry and the varactor tuning element.

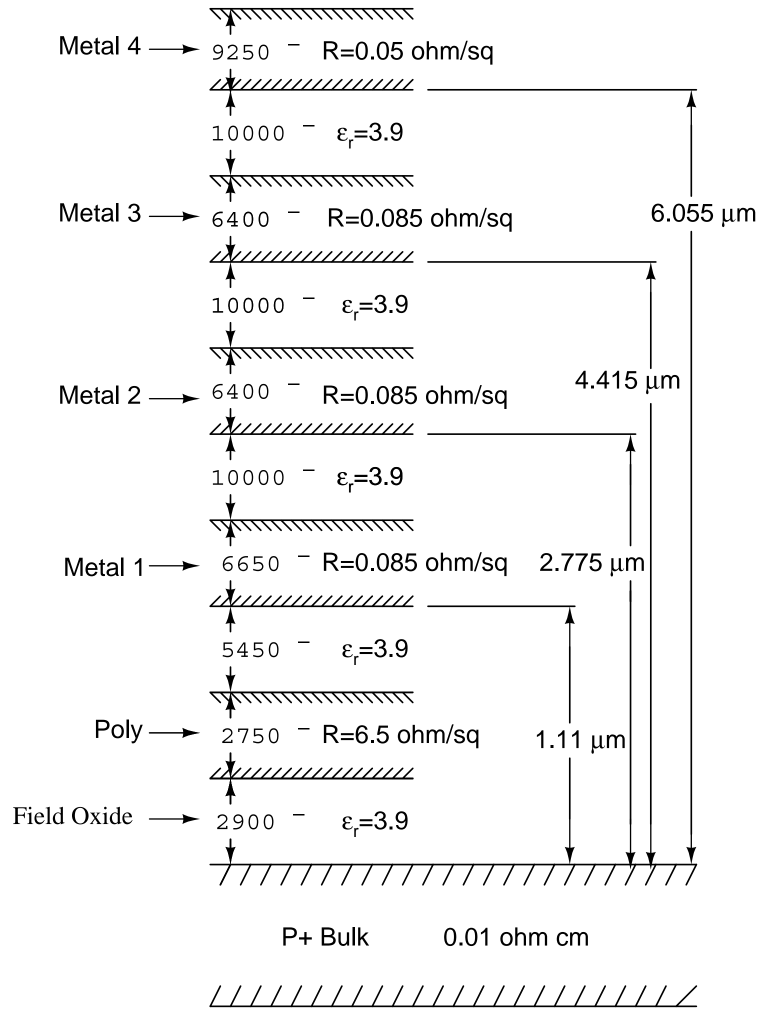


Figure 3.10: CMOS process layer stack-up.

The CMOS process used for this design is a $0.35\,\mu m$ single-poly, 4-metal process available through MOSIS[3]. The vertical dimensions of the process layers are shown in Figure 3.10. The metalization thicknesses and dielectric thicknesses are known accurately, but the substrate parameters are not disclosed by MOSIS. Consequently, the substrate resistivity was assumed to be $0.01\,\Omega \cdot cm$ as this appears to be a typical value for modern digital CMOS processes [7],[37],[42]. The p+ substrate was assumed to be $1500\,\mu m$ thick throughout the design . Although this is an unreason-

[3]MOSIS is a low-cost prototyping and small-volume production service for VLSI circuit development.

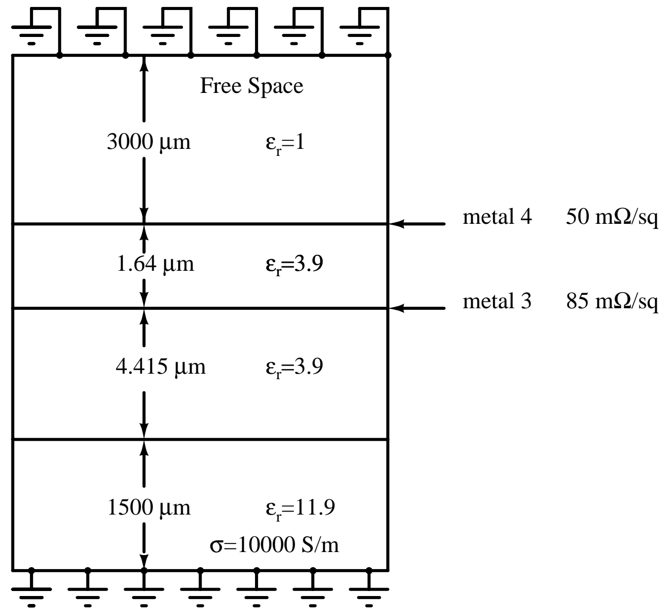


Figure 3.11: Simplified layer data for Sonnet EM simulations.

ably large thickness for a 0.35 μm CMOS process manufactured on 8 inch wafers (the wafer size and thickness were unknown during the design phase), it is a conservative value for simulation purposes. Many CMOS processes have substrates as thin as 650 μm. Typically 8 inch wafers are 725 μm thick [43]. Sonnet simulations showed that thicker substrates yielded lower Qs. When simulations were conducted using a 650 μm substrate the resulting inductance was nearly identical to simulations on 1500 μm substrates and the Q was less than 1 percent higher.

Figure 3.11 shows simplified layer parameters used in the Sonnet EM simulations of the inductors. Only the uppermost metalization layer (metal-4) was used for the inductor (metal-3 was used as a crossover). More complicated structures involving multiple levels of metal were avoided due to the difficulty of simulating such a structure. Sonnet simulates these metal layers as zero thickness layers (with a given sheet resistivity) between the dielectric layers. The area above the inductor is assumed to be free space, but the entire structure is surrounded by a grounded PEC (perfect electrical conductor) cavity. The thickness of the free space layer was chosen to be

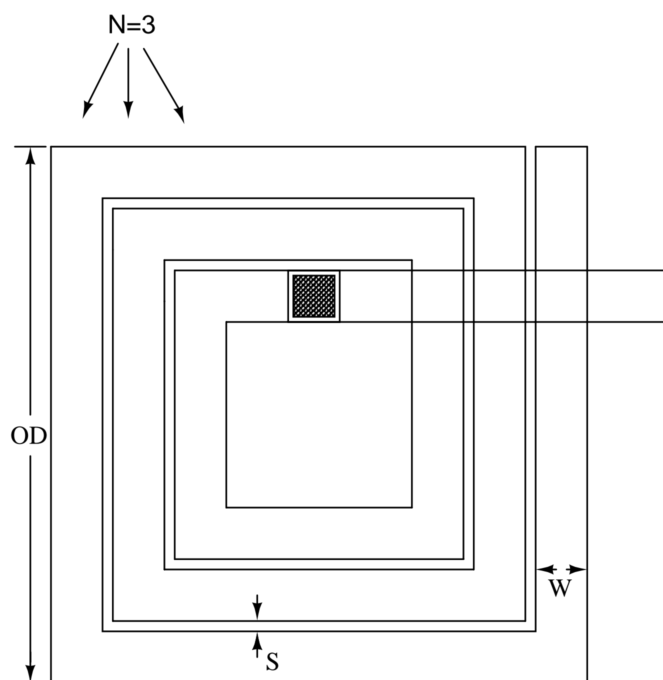


Figure 3.12: Design variables for square spiral inductor.

large so that the effects of image currents in the PEC cavity of the simulation were insignificant.

A square spiral with the four relevant design variables is shown in Figure 3.12. The two port S-parameters were simulated for this structure, over the frequency range of 0.1-10.1 GHz. A variety of inductor structures were studied with outside diameters (OD) varying from $150 - 300\mu m$, tracewidths (W) from $10 - 25\mu m$, and an interwinding spacing (S) of $2\,\mu m$. Figures 3.13 and 3.14 show the inductance and Q versus frequency for a variety of inductors that were simulated. These graphs show samples from the large number of structures that were evaluated. The suitability of these inductors for use in the complementary $-G_M$ oscillator was determined by calculating their equivalent parallel resistance (Eq. 3.15). Some of the inductor designs yielded higher Qs, but due to their low inductance values yielded unacceptably low R_{eq}. Figure 3.15 shows a plot of R_{eq} versus frequency for the same set of inductors. Although some improvement in Q appears to be available by using large tracewidths

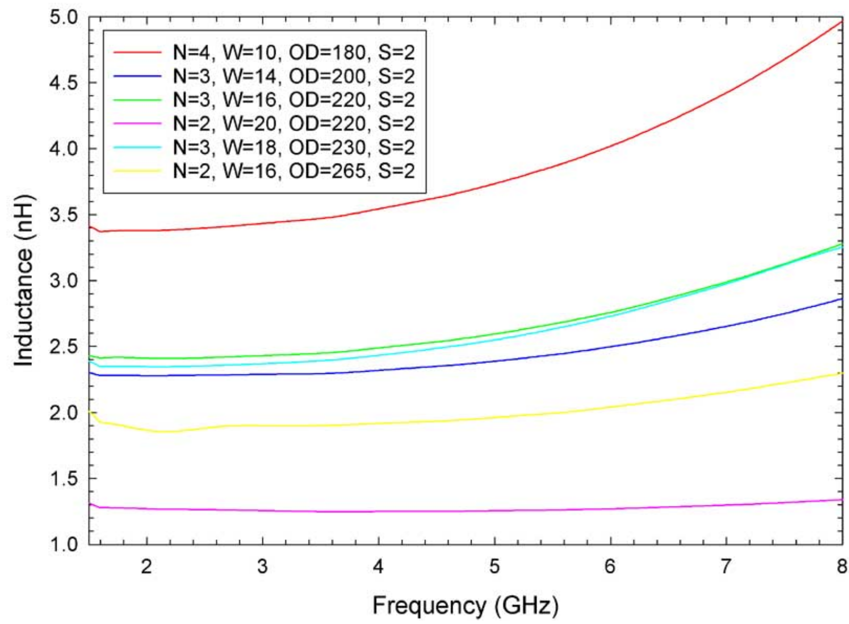


Figure 3.13: Inductance (single-ended) versus frequency for a variety of dimensions (in μm).

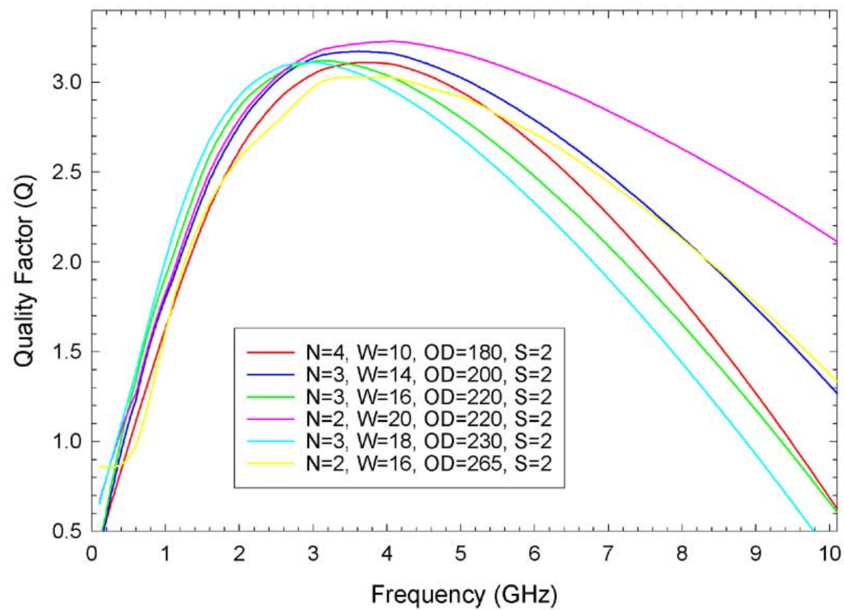


Figure 3.14: Quality factor (single-ended) versus frequency for a variety of dimensions (in μm).

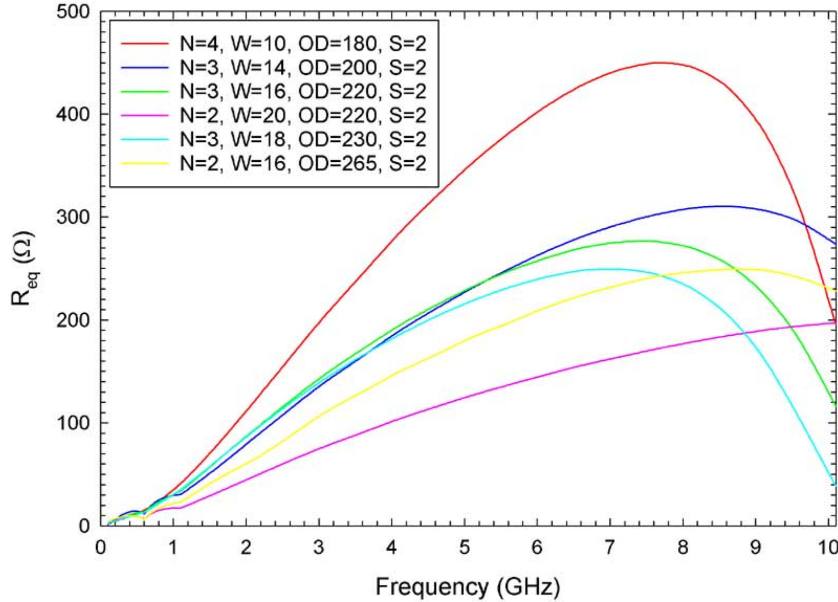


Figure 3.15: R_{eq} versus frequency for a variety of dimensions (in μm).

($W > 18\,\mu m$) and large inductor structures ($OD > 240\,\mu m$) these large geometries were avoided, because the author had doubts about the accuracy of planar, 2.5D, simulations on such large structures. Since Sonnet EM is a planar solver, it cannot simulate some 3D effects such as current crowding that might become important with large spirals. To minimize the impact of these large geometry effects, a smaller structure was chosen.

The final inductor design that was selected was a three turn spiral, with $OD = 220\,\mu m$, $W = 16\,\mu m$, and $S = 2\,\mu m$. This inductor has an inductance of 2.42 nH and a Q of 3.06 at 2.5 GHz (calculated using Eq. 3.7). This inductor represents a compromise between all the design tradeoffs. The total tank circuit inductance was implemented by connecting two inductors in series as shown in Figure 3.16. This is done so that the differential oscillator will see a symmetric reactive load. Simulations predicted a Q=3.1 and L=4.59 nH at 2.5 GHz, for this dual inductor structure. Graphs showing Q, L, and R_{eq} are shown in Figures 3.17, 3.18, and 3.19 respectively

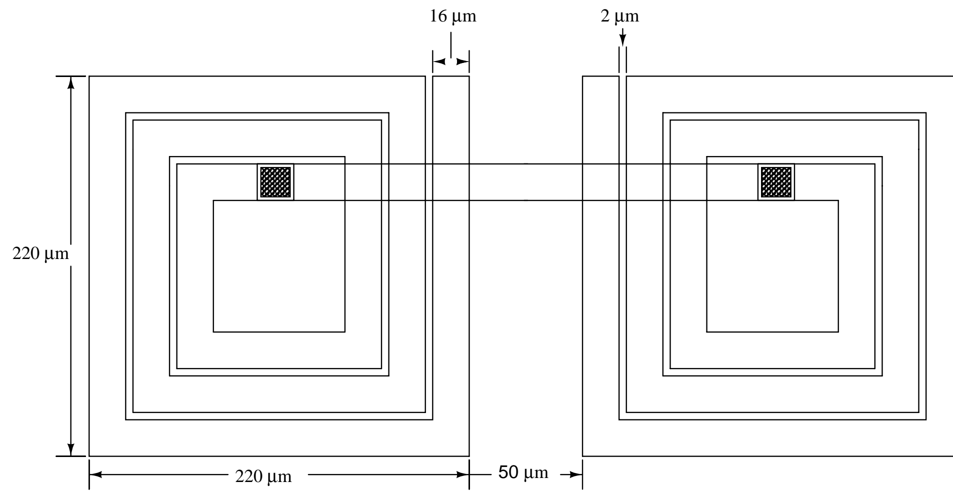


Figure 3.16: Series connected tank circuit inductor and dimensions

(this is a floating inductor, i.e. Eq. 3.12 applies).

The S-parameters and π-model of this inductor were used in simulations to design the oscillator. The inductor design that has been presented was the result of a number of iterations after simulations of the overall oscillator were considered. In the next chapter the other half of the tank circuit, the varactor, will be presented.

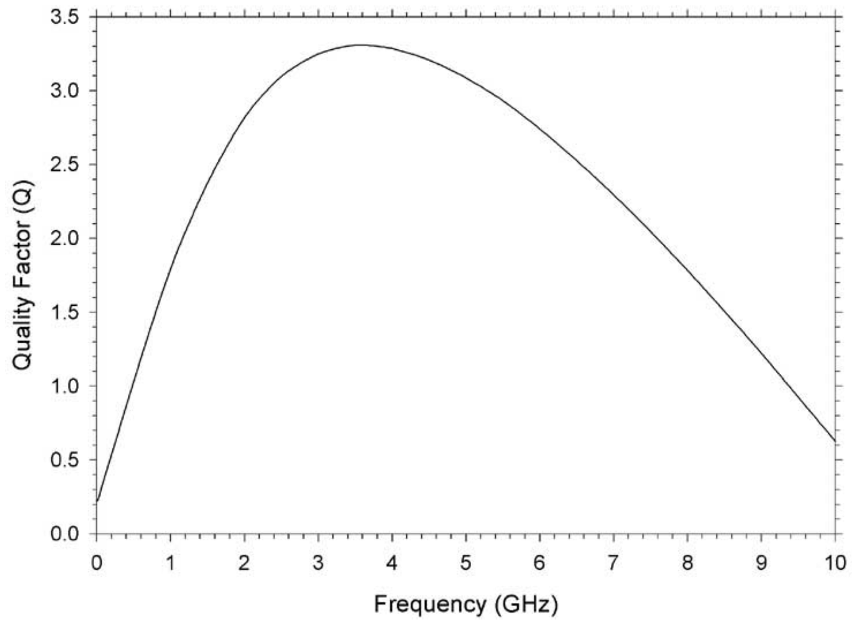


Figure 3.17: Dual inductor quality factor (differential) versus frequency.

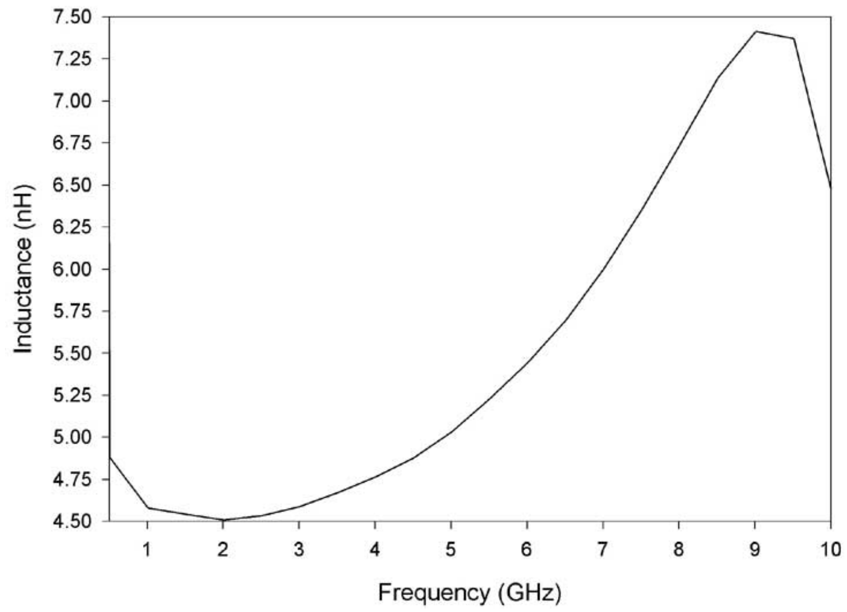


Figure 3.18: Dual inductor inductance (differential) versus frequency.

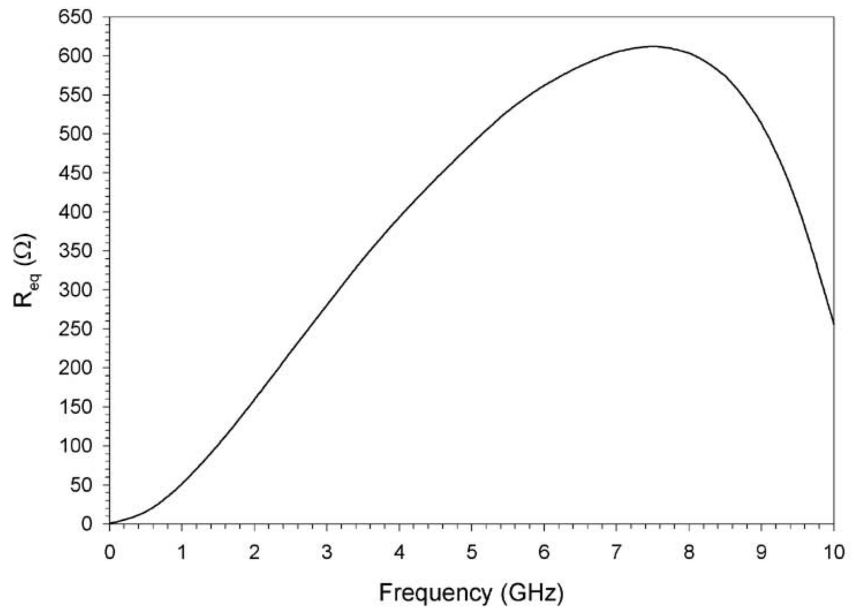


Figure 3.19: Dual inductor R_{eq} versus frequency.

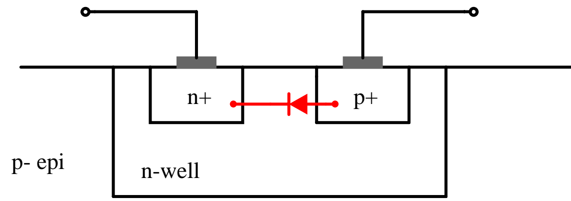
Chapter 4

Varactor Design

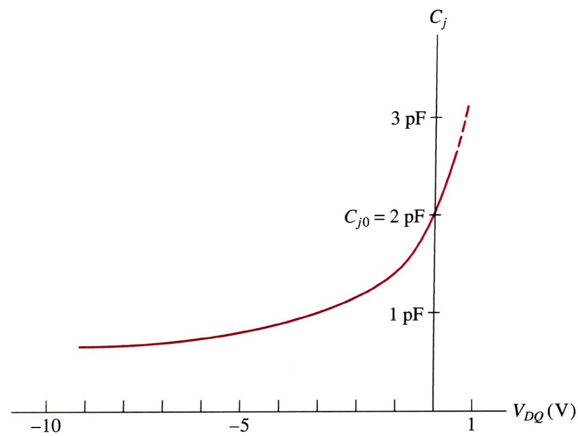
4.1 Background

Although the quality factor of the tank circuit will be dominated by the inductor, the design of the varactor is also critical. If the varactor is not carefully designed its series resistance could significantly lower the overall Q of the tank circuit, adversely impacting the phase noise of the oscillator

Traditionally, discrete VCO implementations have used junction varactor diodes. These diodes are operated under reverse bias and are designed to enhance the variability of their depletion capacitance with reverse bias voltage. In a monolithic environment RF designers are much more restricted in the choice of tuning elements. The junction diodes that are available in a standard silicon CMOS process are not optimized for use as varactors; still, many monolithic LC oscillators have used such diodes as tuning elements [2],[7],[13]. In a typical n-well CMOS process there are three junction diode structures available: n+/p- bulk, p+/n-well, and n-well/p- bulk. The only suitable choice for a junction varactor diode is the p+/n-well junction. Since the p- bulk is typically connected to ground, the other structures would require a



(a)



(b)

Figure 4.1: CMOS P-N junction varactor. (a) p+/n-well varactor diode cross section. (b) Typical depletion capacitance versus voltage characteristic [44].

negative bias voltage in order to be reverse biased. The p+/n-well structure also has a lower series resistance due to the higher n-well doping level compared to the p- bulk. Figure 4.1 shows this structure and its capacitance versus voltage (C-V) characteristic. A p+/n-well structure can typically have a quality factor of 20 or better. One disadvantage of junction varactors is that they can become forward biased by large amplitude voltage swings.

4.2 MOS varactor structures

In this work a MOS capacitor, rather than a junction diode, was used for the tuning element of the VCO. The MOS capacitor operates in a similar manner as a simple parallel plate capacitor. In this case the plates of the capacitor are formed by the polysilicon gate and the channel of a MOSFET. The capacitance of this MOS device varies non-linearly as the DC gate bias of the MOSFET is varied through accumulation, depletion and inversion. Therefore a structure which is always present in a CMOS process can be used as the tuning element of an oscillator. This section will briefly examine three types of MOS capacitors that are suitable for use as varactors. Figure 4.2 shows the cross sections and corresponding C-V characteristic for each of these structures. Each structure shown is similar to a PMOS transistor situated in an n-well; however, these devices could also be implemented as NMOS devices in the p- bulk as well. However, PMOS is preferred because the bulk terminal of an n-well can be biased at a variable voltage (in an n-well process), whereas the p- bulk of an NMOS device must be at ground potential.

Different variations on the basic MOS structure have been explored in order to realize varactors with the highest possible quality factor [45]. The first structure [Fig. 4.2(a)] consists of a PMOS transistor with the drain, source and bulk connected together (D=S=B) to form one node of the capacitor, and with the polysilicon gate as the other node. This structure has a capacitance that varies non-monotonically[1], since the device can operate in inversion, depletion, and accumulation [24],[45]. Figure 4.2(b) shows the DC tuning curve of this structure. The maximum capacitance in both inversion and accumulation is approximated by C_{ox}, which can be calculated from the device dimensions as a simple parallel plate capacitor. If fringing effects are

[1] A function that is not strictly increasing or decreasing (i.e. a function that has a local minimum or maximum)

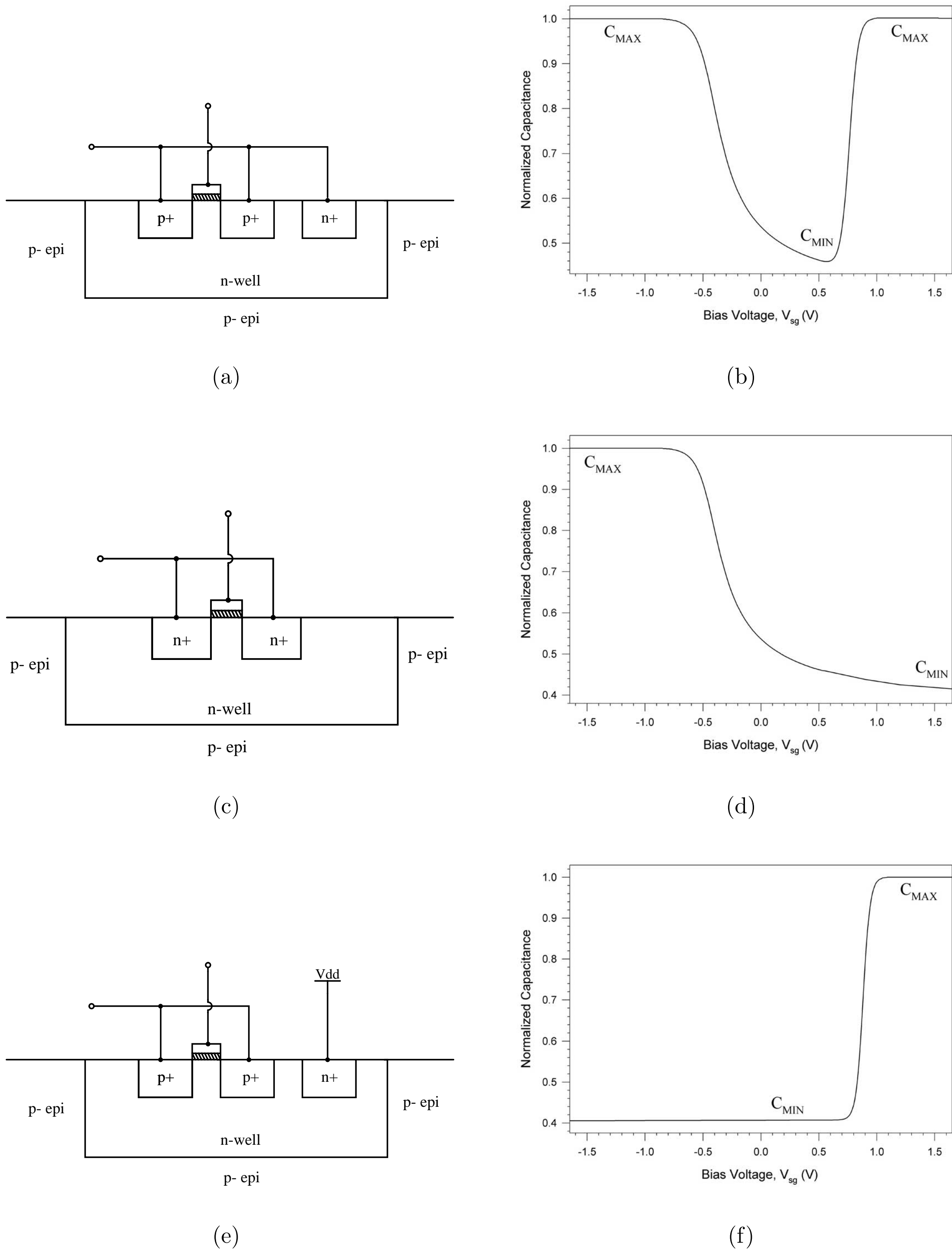


Figure 4.2: MOS capacitor structures. (a) D=S=B structure. (b) D=S=B C-V curve. (c) Accumulation mode structure. (d) Accumulation mode C-V curve. (e) Inversion mode structure. (f) Inversion mode C-V curve.

neglected:

$$C_{ox} = \frac{3.9\varepsilon_0 WL}{t_{ox}} \tag{4.1}$$

where t_{ox} is the gate oxide thickness and is approximately 76Å in this process. If a MOS varactor is to be used as the tuning element of an oscillator (as in this thesis), then the nonmonotonic characteristic of Figure 4.2(b) can be problematic as will be seen in section 4.4.

The C-V curves shown in Figure 4.2 are the DC or small signal characteristics. These curves characterize the capacitance versus voltage for a very small signal superimposed onto the DC bias voltage, V_{gs}. If the signal voltage applied across the device is large (as in a VCO), then the instantaneous value of the capacitance changes throughout the signal period. The effective capacitance seen by the large signal will be the weighted average of the small signal capacitance over a single period. Because of this "averaging" effect the *RF* frequency versus tuning voltage and the DC small-signal tuning curve (shown here) will not be equivalent. The effect of this large signal averaging is to fill in the local minimum of Figure 4.2(b), degrading the tuning range of the oscillator. This large signal averaging effect will be discussed further in Section 4.4

MOS capacitors may also be designed to operate in accumulation mode. Figure 4.2(c) shows the structure of an accumulation mode (A-MOS) capacitor. This structure departs somewhat from the standard PMOS transistor, since it replaces the p+ diffusions of the drain and source with n+ regions. This suppresses the injection of minority carriers (holes) into the channel and prevents it from inverting. The use of n+ regions also obviates the need for n+ ohmic contacts to bias the n-Well, so this structure can be smaller than the other MOS capacitors. Since this device works in accumulation and depletion only, the capacitance characteristic shown in Figure 4.2(d) results. While still nonlinear, the curve is now monotonic. However this structure has a number of drawbacks. Since this structure is no longer a MOS transistor,

its characteristics are not represented in the device models supplied by the vendor (e.g. BSIM3v3 [23]). In order to simulate the behavior of this structure, a device simulator such as Medici[2] must be used, requiring detailed knowledge of process parameters such as doping concentrations. At the time of this writing MOSIS does not supply their customers with this data.

The third option is the inversion mode MOS capacitor [Fig. 4.2(e)]. This structure is identical to a MOSFET. The drain and source are shorted together to form one capacitor terminal while the polysilicon gate forms the other. However, the bulk (n-well) of this structure is connected to the highest voltage available in the circuit, V_{DD}. Since the n-well connection of the device is always at a higher or equal potential with respect to the gate, the device can only operate in inversion. This yields the DC C-V characteristic shown in Figure 4.2(f). This characteristic is also nonlinear and monotonic, but the transition from C_{min} to C_{max} is very sharp. While this characteristic suggests an extremely large tuning gain in the oscillator, it should be noted that the oscillator will tune to the frequency determined by the large signal *average* capacitance (see Section 4.4). The capacitances of the D=S=B and Inversion mode capacitors are both supported by the BSIM3v3 models. An additional benefit of the inversion mode structure is that its n-well connection is tied to V_{DD} rather than a tuning voltage, and therefore the device is less vulnerable to latch-up[3]. For these reasons, inversion mode varactors (I-MOS) are used in this thesis.

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[2]Medici is a registered trademark of Avant! Corporation

[3]Latch-up is a critical failure mechanism that can occur in CMOS circuits when high frequency pulses turn on a parasitic silicon controlled rectifier existing across the substrate between V_{DD} and ground [6].

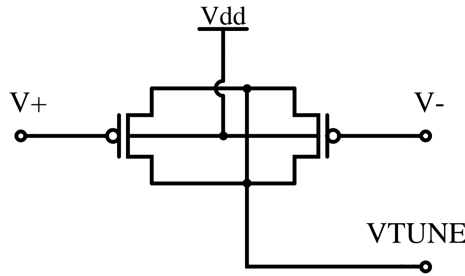


Figure 4.3: Series varactor connection

4.3 Varactor Design and Layout

The MOS varactor design was tightly coupled to the overall LC tank circuit design and the design of the complete oscillator. As was stated in Section 3.6, the starting point for this design was a tank circuit with C=1 pF and L=4 nH which resonates near 2.5GHz. The total tank capacitance is formed by the combination of the variable tuning capacitance (varactors) and parasitic capacitances associated with the circuit layout, including the inductors.

The tuning capacitance is implemented in a differential fashion by connecting two identical PMOS varactors in series (Fig. 4.3). Therefore, the tank varactor capacitance is half the value of the individual varactors. If the circuit is properly balanced, connecting the tuning capacitors in series creates a virtual ground at the common node. The tuning voltage can be applied at this node through a resistor. Because of the virtual ground, the differential varactor connection does not require AC currents to flow into the bulk. Therefore, this connection makes the circuit insensitive to parasitic capacitances from the p+ diffusions to the n-well and from the n-well to the p-substrate.

When the additional parasitics of the oscillator (tank circuit and actives) circuit were considered, it was decided to design each varactor for a maximum capacitance of approximately 1pF yielding a maximum total tank capacitance of 0.5pF. The parasitics of the circuit provide the other half of the tank capacitance. The varactor must be

simulated carefully since BSIM3v3 models do not correctly predict the quality factor of MOS capacitors. For example, using Equation 4.1, a 1 pF capacitor could conceivably be implemented in this process using a PMOS transistor that is 14.8 μm in length and width. However, such an implementation would have very poor performance since the resistance of the channel (R_{ch}) and the gate (R_g) would be excessive. BSIM3v3 and most other MOSFET models predict an infinite Q even with a badly thought out device geometry, since the models do not account for channel resistance when the drain and source are shorted. Furthermore, the resistance of the polysilicon gate and the device contacts are not accounted for in the device models.

During the initial design of the oscillator it was assumed that the varactor would have a quality factor of approximately 30. The varactor was actually designed while the oscillator circuit was being laid out. The layout geometry of a MOS capacitor determines its Q. The Q of a capacitor with a series resistance is defined by:

$$Q = \frac{1}{\omega_0 R_s C}. \tag{4.2}$$

The series resistance of an inversion mode PMOS Capacitor will include the combination of the gate resistance, the contacts to polysilicon and diffusion, and the resistance of the inverted channel. To a first approximation the resistance of the inverted channel, R_{ch}, and the gate, R_g, can be considered in series with the MOS capacitor. However the situation is far more complicated than this simple treatment. R_{ch} depends directly on the conductivity of the inversion layer of the MOS structure, which is bias voltage dependent. A complete analysis must also consider the *distributed* nature of the MOS structure. When the MOS gate and channel are considered as an RC transmission line, and the gate is contacted on both ends of the channel, the intrinsic gate resistance is given by [4]:

$$R_g = \frac{1}{12}\frac{W}{L} R_{poly,\square}. \tag{4.3}$$

This expression is valid only for the polysilicon over the active region of a device. Extrinsic resistances such as those of contacts and polysilicon extending from the

device to the contacts, and metal interconnects must be added to this expression. An expression for the series resistance of an accumulation mode varactor is developed in [46]. This expression was modified slightly ($R_{nw,\square}$ the n-well sheet resistivity was replaced by $R_{ch,\square}$ the inversion layer sheet resistivity.) to reflect its use in an inversion mode device:

$$R_s = \frac{1}{12} \times \frac{1}{N} \times \left(R_{ch,\square} \times \frac{L}{W} + R_{poly,\square} \times \frac{W}{L} \right). \tag{4.4}$$

where $R_{ch,\square}$ is set equal to the sheet resistance of the channel in the triode region [12] and N is the number of gate fingers. $R_{ch,\square}$ is not given explicitly in the MOSFET models or design data, but it can be estimated from the MOSFET models using:

$$R_{ch,\square} = \frac{1}{\left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{V_{DS}=0}} \times \frac{W}{L} = \frac{1}{\mu_n C_{ox}(V_{GS} - V_{th})}. \tag{4.5}$$

Since V_{GS} varies with the oscillation voltage, the resistance of the channel will not be constant. In order to obtain an estimate for $R_{ch,\square}$, $V_{GS} - V_{th}$ can be set to $\frac{V_{DD}}{2}$.

During the tank circuit design phase, Equation 4.4 was simply used as a guideline. The gate resistance was estimated to ensure that the design led to a reasonable Q. Since $R_{ch,\square} \gg R_{poly,\square}$, Equation 4.4 indicates that L should be minimized to reduce the series resistance. For this reason the process minimum channel length was utilized. On the other hand, using the minimum channel width would result in a device with an excessive number of fingers with large associated parasitic capacitances, compromising the tuning range. In addition, for small devices, the series resistance will be dominated by the contact resistances, since small devices can only support a single contact rather than the preferred larger array of contacts [47]. Consequently, the MOS varactors for the VCO design were realized using the minimum gate length allowed in the process (0.35 μm). The width of each channel was chosen to be 3.3 μm, which represents a compromise between quality factor, varactor size, and parasitics. Each of the two series varactors consists of 4 parallel devices with 40 fingers each (Fig 4.4). Therefore, the overall device is a 160 finger transistor, with $W = 3.3\mu m$ and $L = 0.35\mu m$. Using Equation 4.1, C_{MAX} would equal approximately $0.84pF$; however, the overlap and

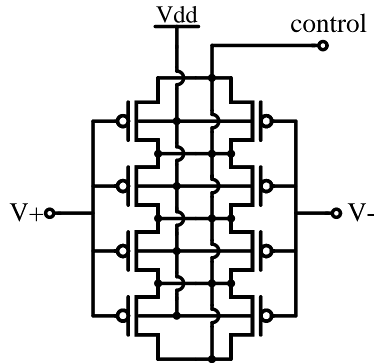


Figure 4.4: Varactor implementation schematic.

fringing effects on each finger cause the actual capacitance to be about 30 percent larger. Figure 4.5 shows the layout of the varactor along with a detailed view of the gate and contact arrangement. Notice that the gate polysilicon is contacted on each end of the device. Also notice that in order to further reduce the resistance of the polysilicon contacts two rows of contacts are used. The contacts are placed as close together as possible. In the available process (and many other sub-micron silicon processes), vias and contacts may only be of a fixed size and must be separated by minimum distance. The $3.3\mu m$ channel width does increase the gate resistance of each device, but the wider device allows the placement of 4 diffusion contacts on the source and drain of each finger. The entire structure is placed in a common n-well, and n+ ohmic bulk contacts connect the n-well to V_{DD} between each 40-finger-section of the varactor. The control voltage and the n-well bias enter the structure in the center on the first two metal levels; the tank circuit is connected on the outer edges by metal 2 fingers that run down each row of poly contacts.

Figure 4.7 shows a plot of the simulated total varactor capacitance (i.e. the series combination of Fig. 4.3) versus the control voltage. This C-V curve was generated using a transient simulation in Spectre. A 2.5GHz, 10mV signal was applied across the varactor and the displacement current[4] through the device was measured (Fig.

[4]Because the BSIM3v3 models do not model the gate resistance or the channel resistance (when

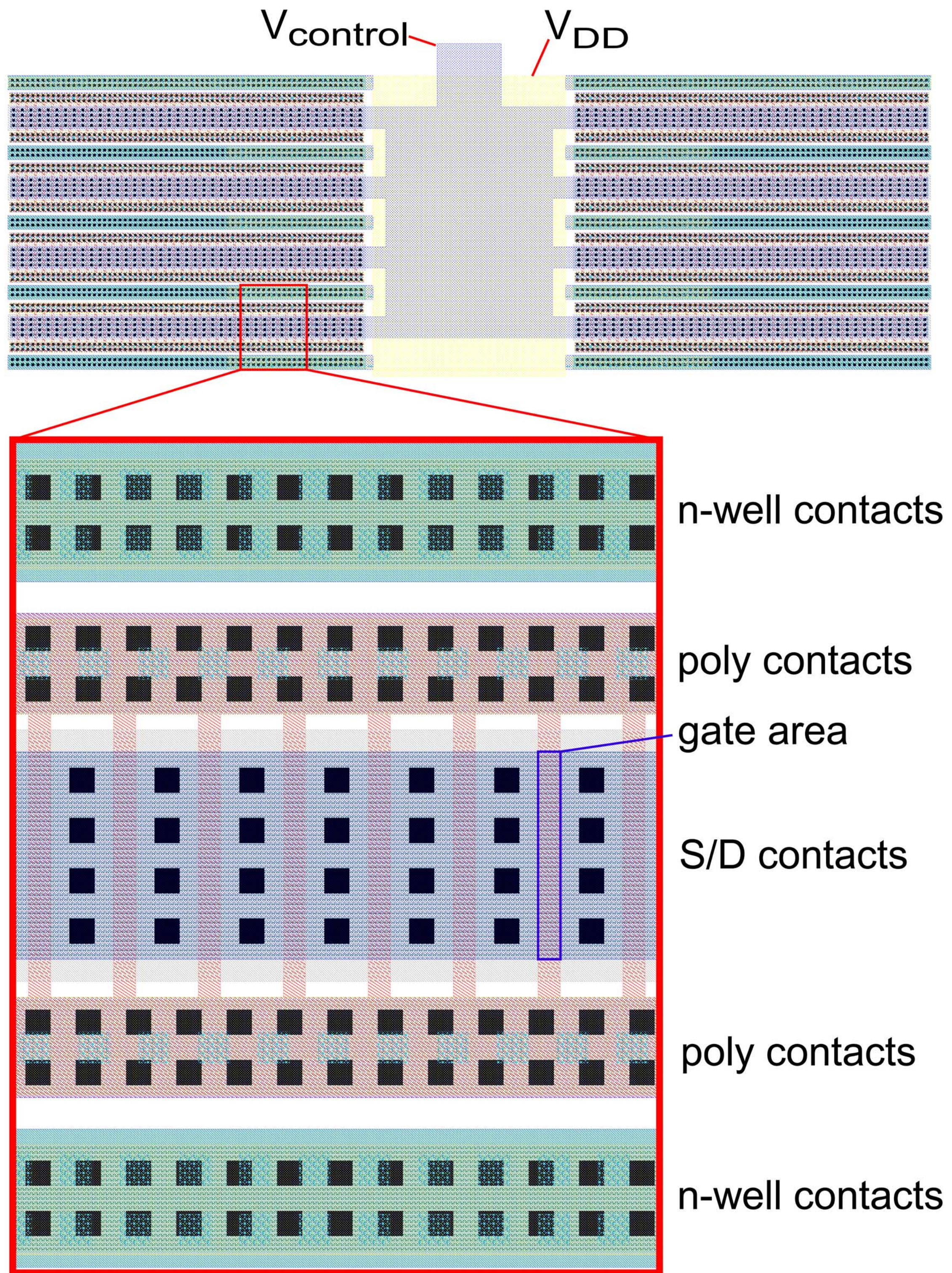


Figure 4.5: Varactor layout with detailed view of gate and contact arrangement. Contacts are shown as solid black squares in the various regions.

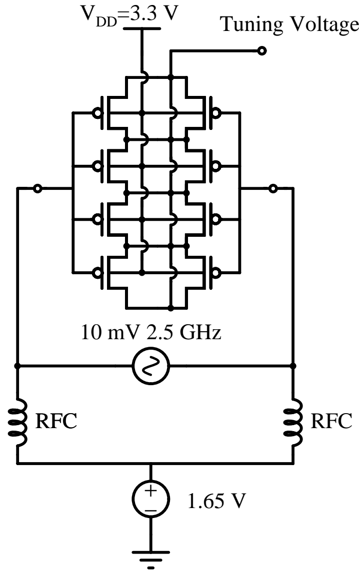


Figure 4.6: Circuit used to measure total tank circuit varactor capacitance versus tuning voltage.

4.6). The DC voltage at the gates of the varactor is set to $\frac{V_{DD}}{2} = 1.65$ since this is close to the actual DC operating voltage at the tank circuit nodes in the complementary $-G_M$ oscillator (see Sect. 2.2). The tuning voltage was varied over a number of simulation runs and the capacitance was calculated from the displacement current through the varactors for each run.

The relevant contact and sheet resistances necessary to calculate the Q of this structure are given in Table 4.1. $R_{ch,\square}$ was calculated by doing a DC sweep in simulation, since short channel devices deviate somewhat from Equation 4.5. Using $V_{GS} = 1.65V$ for simplicity, $R_{ch,\square} \approx 57000$, (quite large, but recall that this is the resistance of the very thin inversion layer of the device at $V_{DS} = 0$). $V_{GS} = \frac{V_{DD}}{2}$ was chosen since it represents an average operating point for the varactor. During actual operation V_{GS} will swing between $V_{GS} = 0$ and $V_{GS} = V_{DD}$ over an oscillation cycle. This causes the varactor to operate in both strong and weak inversion. Using Equation 4.4 for

the drain and source are shorted) it is assumed that the current into the gate terminal of the varactors is in quadrature with the applied voltage (i.e. the device appears purely capacitive). Thus the capacitance is easily calculated as the ratio $C = \frac{1}{2\pi f} \frac{|I|}{|V|}$.

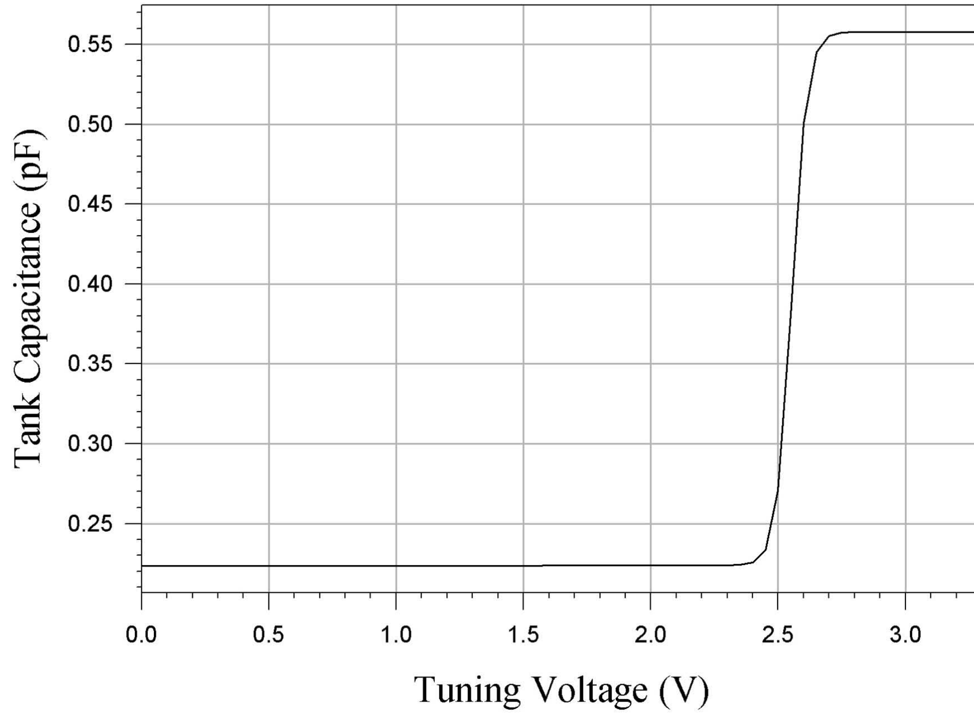


Figure 4.7: Simulated total tank circuit varactor capacitance versus tuning voltage

Table 4.1: Sheet and contact resistances for a 0.35μm process

$R_{poly,\square}$	6.3
$R_{P+,\square}$	2.6
$R_{Metal1,\square}$	0.07
$R_{M1-Poly}$	4.7
R_{M1-P+}	4.1
R_{M1-M2}	1.4

each varactor, R_s was calculated to be 3.18Ω. Considering the total tank varactor, the total series resistance would be 6.36Ω. From Figure 4.7 the varactor capacitance varies from 0.223 pF to 0.558 pF. If the tuning range extends from 2.3 GHz to 2.8 GHz (as was expected from simulations), Equation 4.2 predicts that the Q of the varactor will vary from 19.5 to 40.1, respectively.

4.4 Large-Signal Effects

As was stated earlier the oscillator responds to the *average* capacitance rather than to the exact value on the DC C-V curve. Since the AC voltage across the varactors (in a $-G_M$ oscillator, Fig. 2.5) will be large relative to the voltage required to transition from C_{min} to C_{max} the tuning curve of the VCO will be significantly more linear than the small-signal (DC) C-V plot of the varactors themselves. Furthermore, larger tank voltages will result in more "smoothing" and the tuning curve will become more linear. For very small tank amplitudes the tuning curve becomes more nonlinear and approaches the shape of the small signal C-V curve in the limit as the tank amplitude approaches zero (for this reason the C-V curve of Figure 4.7 was measured using a 10 mV signal). In this section a numerical analysis of the effects of a large-signal applied to a nonlinear MOS varactor is presented.

The small-signal C-V characteristic for *half* of the tank circuit varactor is shown in Figure 4.8. This C-V plot was extracted using the test circuit shown in Figure 4.9. The C-V measurement method is similar to that used in Section 4.3 to generated Figure 4.7. The only difference is that here only a single varactor (half the tank varactor) is considered.

This C-V curve follows a hyperbolic tangent trend and was fitted to the following expression.

$$C(v) = 7.66844 \times 10^{-13} + 3.24339 \times 10^{-13} \tanh(17v - 43.01) \tag{4.6}$$

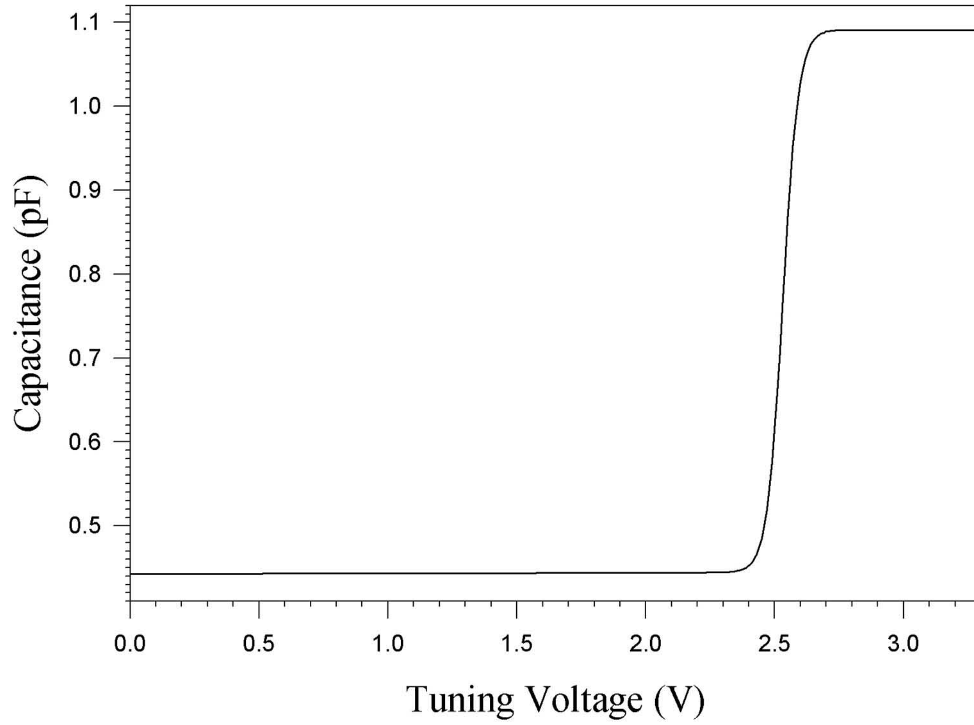


Figure 4.8: Varactor tuning characteristic

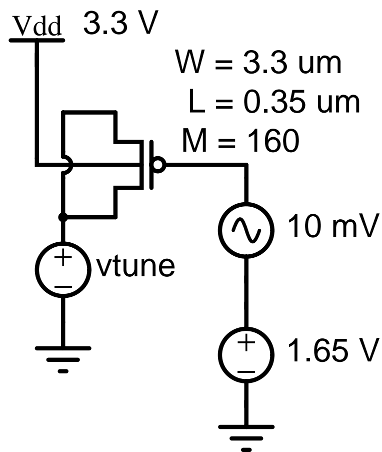


Figure 4.9: Varactor C-V test circuit

Since this capacitance is highly nonlinear the meaning of *large-signal average capacitance* must be rigorously defined. From nonlinear network theory the current into a voltage controlled capacitance is defined as [48]:

$$i = C(v(t))\frac{dv}{dt} \tag{4.7}$$

If it is assumed that the oscillator output is nearly sinusoidal, (a good assumption for the complementary oscillator of this thesis) at frequency f_o, then the average capacitance is:

$$C_{AVG} = \frac{\text{rms}(i)|_{f_o}}{\text{rms}\left(\frac{dv}{dt}\right)\Big|_{f_o}} \tag{4.8}$$

where, $\text{rms}(x(t))$ is the root-mean-square of the periodic signal $x(t)$ with period T. Current components that exist at harmonics of f_o, are of not considered since they are strongly attenuated by the tank circuit inductor and will only distort the output waveform slightly. If a signal:

$$v(t) = A\,\sin(\omega_0 t) + B, \tag{4.9}$$

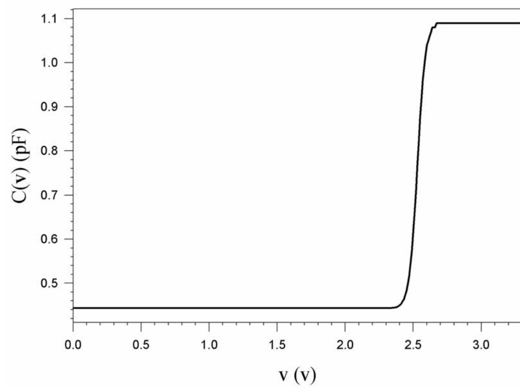
where B represents the DC tuning voltage applied to the varactor and A represents the voltage amplitude, is applied to the circuit, the current i can be calculated using Equation 4.7. Figure 4.10 shows how the nonlinear capacitance results in a highly distorted current waveform. Figure 4.10(c) clearly shows that the nonlinear capacitance establishes the oscillator as a linear *time-variant* system. This is true because the tank capacitance is now a function of time (i.e. it is a function of a time dependent voltage).

The fundamental frequency rms current, $\text{rms}(i_c)|_{f_o}$, can be calculated by determining the Fourier series coefficient a_1 using:

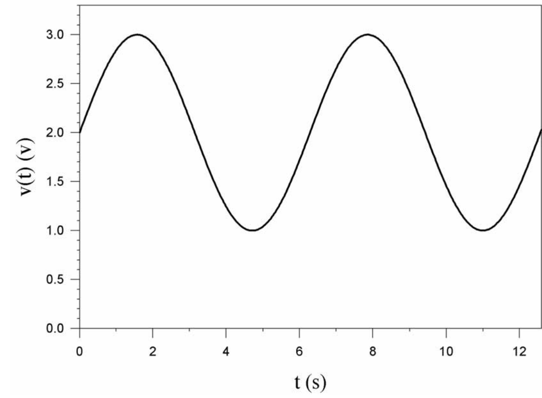
$$a_n = \frac{1}{\sqrt{2}}\frac{2}{T}\int_0^T i(t)\cos(n\omega_o t)dt. \tag{4.10}$$

This equation is a mathematical way of discarding the higher order harmonics, yielding the fundamental rms current.Combining Equations 4.7, 4.8 and 4.9 yields:

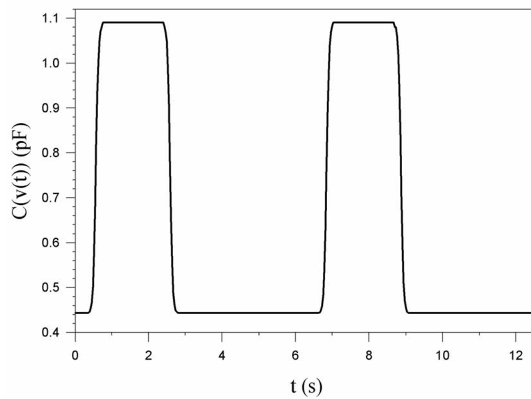
$$C_{AVG} = \frac{\omega_0}{\pi}\int_0^{\frac{2\pi}{\omega_0}} \Big[C\left[A\sin(\omega_0 t) + B\right]\,\cos(\omega_0 t)\Big]\cos(\omega_0 t)dt \tag{4.11}$$



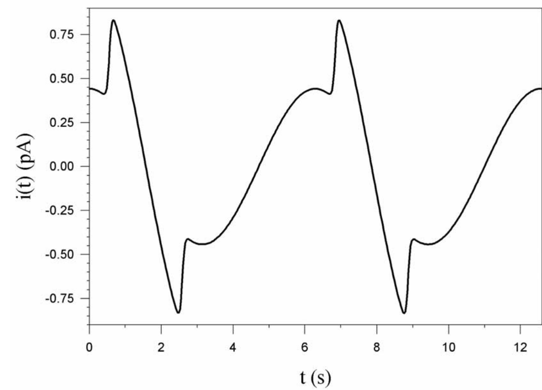
(a)



(b)



(c)



(d)

Figure 4.10: Time domain effect of nonlinear capacitance. (a) $C(v)$. (b) $v(t)$. (c) $C(v(t))$. (d) $i(t) = C(v(t))\frac{\partial v(t)}{\partial t}$.

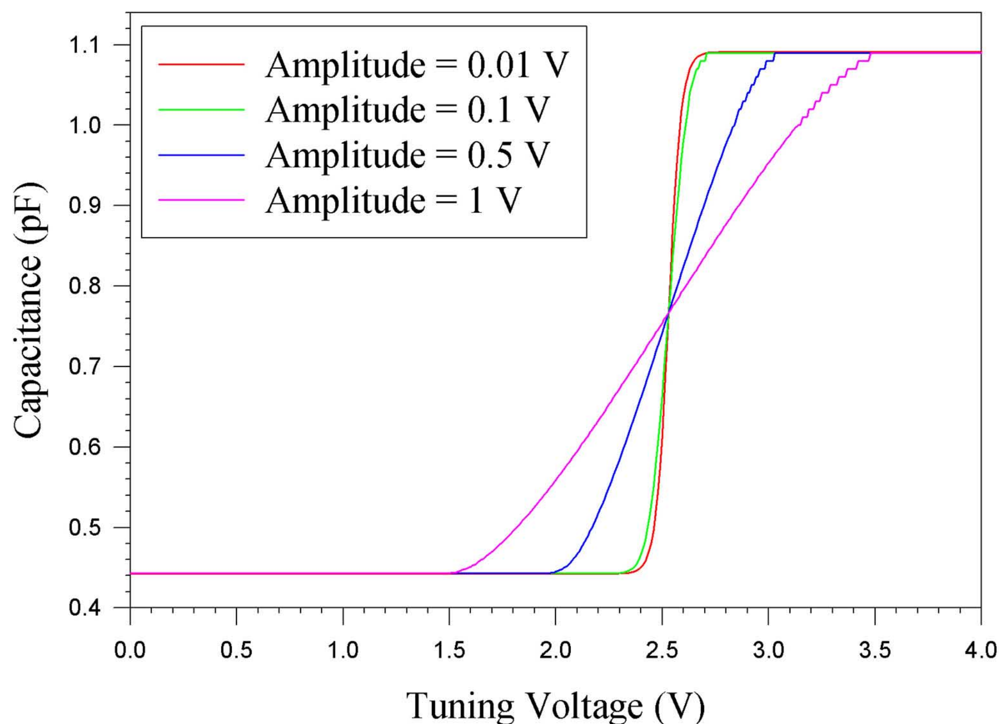


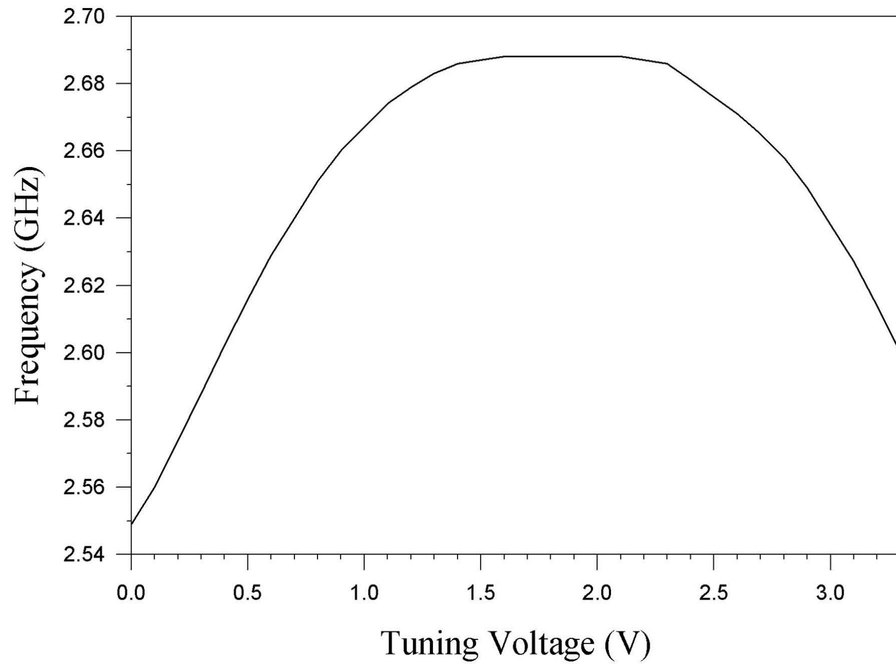
Figure 4.11: C_{AVG} vs. tuning voltage for various amplitudes.

It might be tempting to avoid this complicated development and calculate C_{AVG} as $mean(C(v(t)))$; however, this would be incorrect. Equation 4.11 averages only the fundamental frequency components which agrees with oscillator circuit simulations. Equation 4.11 was integrated numerically using Mathematica [22]. Figure 4.11 shows C_{AVG} versus voltage for various voltage amplitudes. Notice that as the amplitude becomes larger, the linear region of the characteristic becomes wider. The tuning curve of the VCO is determined by these large-signal average capacitance plots.

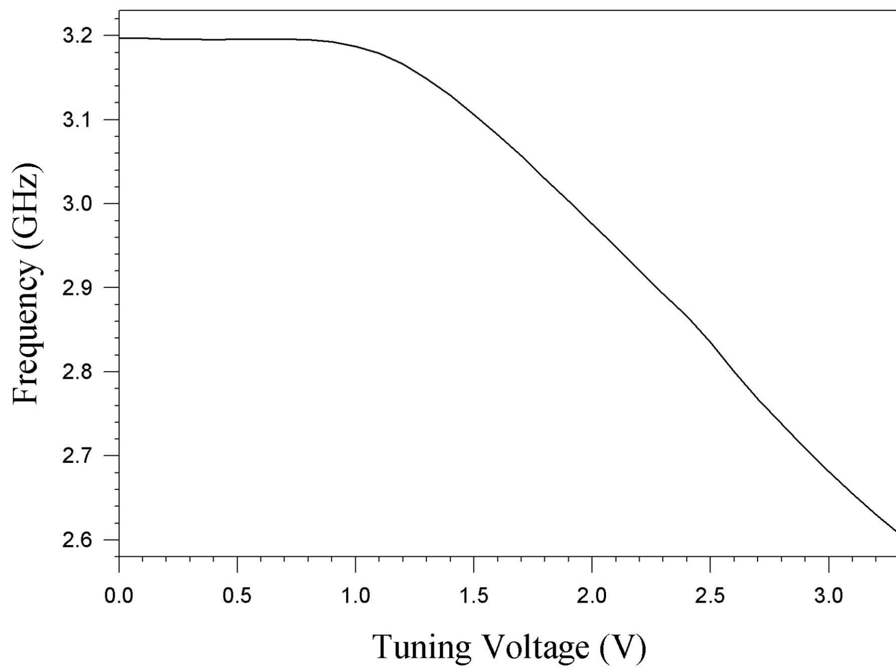
This linearizing effect of the large signal amplitude on the tuning curve is one reason why the D=S=B varactor is such a poor choice for a tuning element. Although the $\frac{C_{MAX}}{C_{MIN}}$ ratios of the D=S=B and I-MOS varactors are similar, the nonmonotonicity of the D=S=B device hampers its tuning range since its large signal average capacitance never gets as low as C_{MIN}. Figure 4.12 shows the tuning curves of two simple $-G_M$

VCOs (see Fig. 2.5) that have the same varactor dimensions, but with one implemented using D=S=B and the other using I-MOS. In each case the Q of the tank circuit is high and the voltage amplitude at the varactor gate terminals is $\approx \frac{V_{DD}}{2}$. Notice that the tuning range of the D=S=B is only 0.14 GHz (5.3%) whereas the I-MOS has a tuning range of 0.6 GHz (20.7%). Furthermore, the maximum operating frequency of the D=S=B oscillator is lower than the I-MOS oscillator

Another large signal effect observed during the design of this VCO was that of harmonic currents flowing into the tuning node. The tank circuit voltage across the nonlinearity of the varactor will generate even-order harmonic currents. However, since the VCO is implemented as a differential structure, these even-order currents are suppressed from flowing into the tank circuit. It was observed during the oscillator design that these even order currents have a tendency to flow into the tuning voltage node. When an ideal voltage source was connected to the tuning node of the varactors this led to considerable distortion in the simulated output signal. This may be because the harmonic currents are reflected back into the oscillator circuit by the ideal voltage source. It was discovered that placing a resistor between the tuning node and the tuning voltage suppressed the level of these harmonics that appeared in the output waveforms. This effect is not fully understood at this time and represents a possible area for future work since these harmonic currents may have a considerable impact on the output phase noise of the oscillator.



(a)



(b)

Figure 4.12: Simulated MOS capacitor VCO tuning curves. (a) D=S=B VCO tuning curve. (b) I-MOS VCO tuning curve.

Chapter 5

Oscillator Design and Implementation

5.1 Background

In the two previous chapters the design of both a monolithic inductor and a PMOS varactor are presented. In this chapter these components are integrated into the overall design of the $-G_M$ oscillator. Layout and implementation issues of the VCO circuit are discussed. Although the inductor and varactor designs were presented in sequential chapters, it is important to appreciate that the design process of an integrated oscillator will often not proceed in such a linear fashion. The impact of the individual components on the circuit as a whole must be considered during their design. This often requires the designer to retreat and make changes to components after having apparently moved on in the design process. In any non-trivial design there are an infinite number of possiblities[1], and often many design decisions are the

[1] A unique treatment of the problem of oscillator design optimization has been presented in [49] and [50]. The authors of these works attempt to reduce the design of an optimal oscillator to simple mathematics, using linear and geometric programming. If such attempts succeed, maybe all circuit

result of a nonlinear trial and error process. The oscillator designed for this thesis is no exception. In that spirit, the reader is encouraged to reference the previous chapters often while reading this chapter.

Three different versions of the $-G_M$ oscillator were fabricated on the project test chip. These variants will be discussed in detail in the following sections. In addition to the oscillators, a number of test structures were fabricated so that the performance of the circuit components could measured individually.

5.2 Oscillator Design

The theory of operation of the $-G_M$ oscillator was discussed at length in Chapter 2. The starting point for the oscillator design in this thesis was the simplified circuit shown in Figure 5.1. This oscillator circuit is tuned by a simple RLC tank with a $Q \approx 2.4$ (at this point the monolithic inductor had not yet been designed; Q=2.4 was considered a worst-case estimate). This circuit was simulated with various PMOS and NMOS device sizes. The transconductances of the devices, $G_{M(nmos)}$ and $G_{M(pmos)}$ were chosen to be equal so that the DC voltage at each side of the tank (V_{out+} and V_{out-}) is maintained at approximately $\frac{V_{DD}}{2}$. This situation is desirable since it allows the output of the oscillator to directly drive into a buffering CMOS inverter, or be converted to a logic signal for use as a digital clock signal. Biasing this node at $\frac{V_{DD}}{2}$ allows the oscillator waveform to be very symmetric since the positive and negative halves (V+ and V- in Fig. 2.15(d)) of the waveform will have the same amount of headroom. The symmetry of this circuit topology has been reported to result in a lower 1/f noise corner frequency, which is important for low close-in phase noise performance [9]. For the simple circuit shown, G_M must be at least 6.7 mS in order to overcome the parallel resistance, $R_p = 150\,\Omega$. $G_{M(nmos)} = G_{M(pmos)} = 10\,mS$ was

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designers should start job hunting!

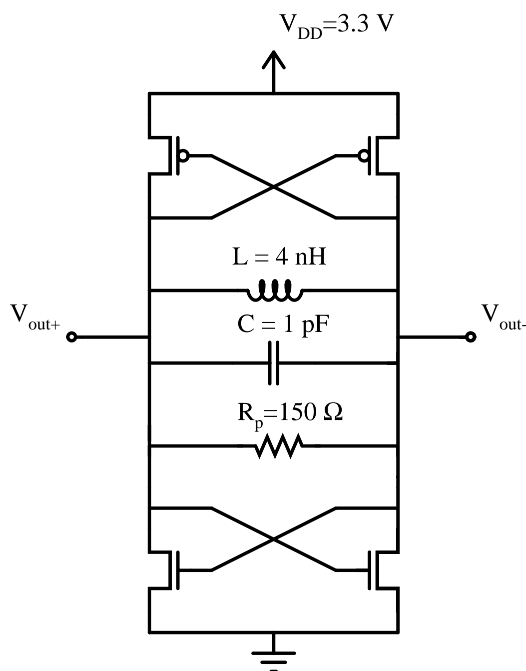

Figure 5.1: Starting point of the VCO design.

chosen, such that the oscillator would still function as long as $R_p > 100$. This gives an oscillator start-up safety factor of 1.5, which is relatively low. However, recall that the assumed Q of 2.4 is also a worst case scenario.

The MOS devices were implemented using the minimum gate length allowed in this process ($0.35\,\mu m$). Because G_M is proportional to $\frac{W}{L}$, using the smallest allowable gate length (L) implies that a small device width (W) can be utilized. This minimizes the gate area ($W \times L$) and thus the gate capacitance. One important drawback of the complementary $-G_M$ structure is that in order to set $G_{M(nmos)} = G_{M(pmos)}$, the PMOS devices must be approximately twice the size of the NMOS devices[2]. In order to realize $G_M = 10\,mS$, $W = 112\,\mu m$ and $W = 54\,\mu m$ were chosen for the PMOS and NMOS devices, respectively.

The circuit of Figure 5.1 is biased directly by the power supply voltage since this is the only way to control the drain currents of the devices. In order to have more

[2]Due to the lower mobility and higher threshold voltage for p-channel devices.

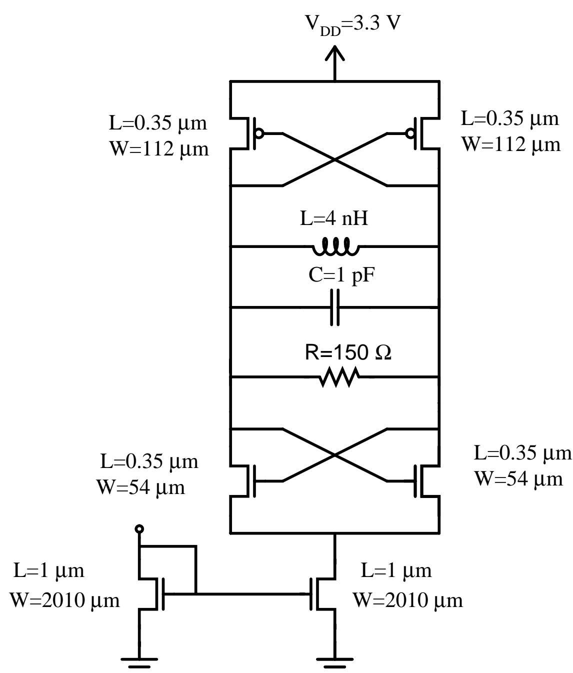

Figure 5.2: Oscillator with tail current control and device sizes.

control over the bias point of the oscillator, a tail current control device was added to the circuit. This tail current control device was implemented as a simple NMOS current mirror. Figure 5.2 shows the circuit with this simple modification. The $\frac{W}{L}$ ratio of this tail current mirror was chosen to be large so that it effectively presents a short circuit directly to ground (less $\approx 80mV$ of headroom) when its gate voltage is high ($V_{gs} \gg V_{th}$), reverting the circuit back to Figure 5.1 ($L = 1\,\mu m$ for layout purposes). This tail current device can alter the voltage swing across the tank circuit of the oscillator. Since the negative resistance presented to the tank circuit can be varied by changing this current, the actual equivalent parallel resistance (R_p) of the resonator can be experimentally determined by finding the lowest bias current at which the circuit will oscillate. At this bias point: $R_{negative} = R_p$.

The simplified tank circuit shown in Figure 5.2 was then implemented with the PMOS varactor and the spiral inductor models from Chapters 3 and 4 for more accurate simulations. The PMOS varactor model used is shown in Figure 5.3. The structure

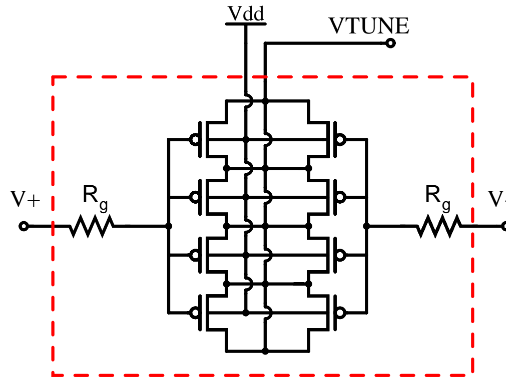

Figure 5.3: Varactor model.

of this model and the calculation of its series gate resistance have been discussed in Chapter 4. The spiral inductor can be simulated using either a π-network (which is valid over a small frequency range), or with S-parameter data. Spectre allows transient simulations on networks that include elements defined by S-parameters with a part called *nport*, which references a S-parameter data file. The nominal values of these reactive components are L=4.67nH ($Q \approx 3.0$) and C=0.22pF-0.56pF ($Q \approx 30$). The detailed design of these tank elements was presented in Chapters 3 and 4. Additional tank capacitance results from the parasitics of the devices and the layout.

Since extracting the oscillator output signal directly into $50\,\Omega$ test equipment would severely load the oscillator (with only $100\,\Omega$ of negative resistance it would probably not oscillate at all), the output of the oscillator must be presented with a high impedance (i.e. the loaded Q and the unloaded Q must be nearly equal). This was achieved using two different approaches. The first approach involved using a resistive divider to extract the signal. In this case a $1\,k\Omega$ polysilicon resistor was fabricated in series with each of the outputs. Since the $50\,\Omega$ load presented by the test equipment appears in series with this $1\,k\Omega$ resistance, each output node is only loaded by $1.05\,k\Omega$; thus, the tank circuit sees a parallel load of $2.1\,k\Omega$. For the simple circuit shown earlier ($R_p = 150\,\Omega$), the parallel resistance would be $150\,\Omega||2050\,\Omega = 140\,\Omega$. The corresponding Q at 2.5 GHz decreases from 2.4 to 2.2. However, this approach

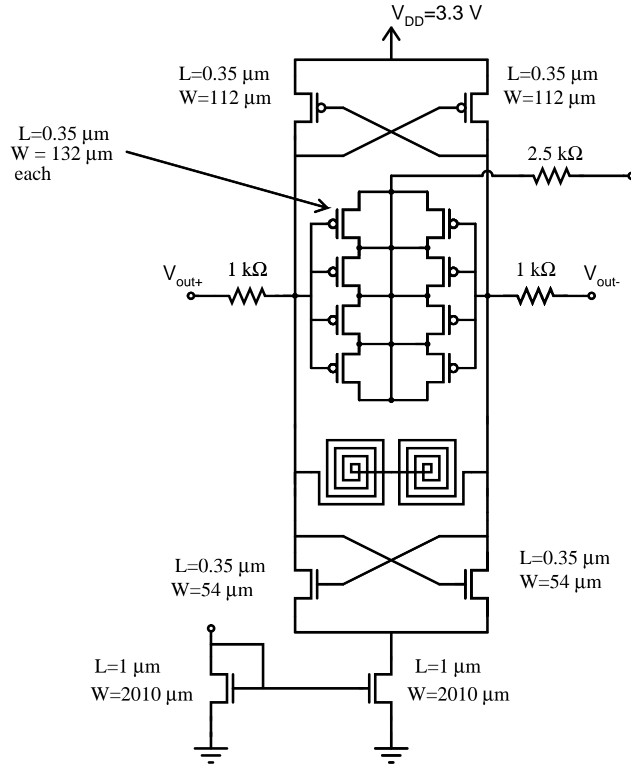

Figure 5.4: Complete unbuffered VCO design (Oscillator #1).

reduces the output power available to the test equipment significantly. If the voltage swing at the oscillator outputs (V_{out+} or V_{out-}) is 1 V-peak, then the voltage into the 50 Ω test equipment is $\approx$ 50 mV-peak or -16dBm. However, since phase noise is a relative measurement, such a low output power does not necessarily present a problem because the noise floor of the spectrum analyzer is quite low. This method of extracting the oscillator signal will be referred to in this thesis as the *unbuffered* case. The complete unbuffered VCO design (oscillator #1) is shown in Figure 5.4. Although the Q of the resonator is reduced somewhat, this approach was available as a fallback in the event that the active buffering methods did not operate as designed.

The other approach for presenting a high impedance to the oscillator output was through the use of an active buffer circuit. Since the complementary $-G_M$ circuit

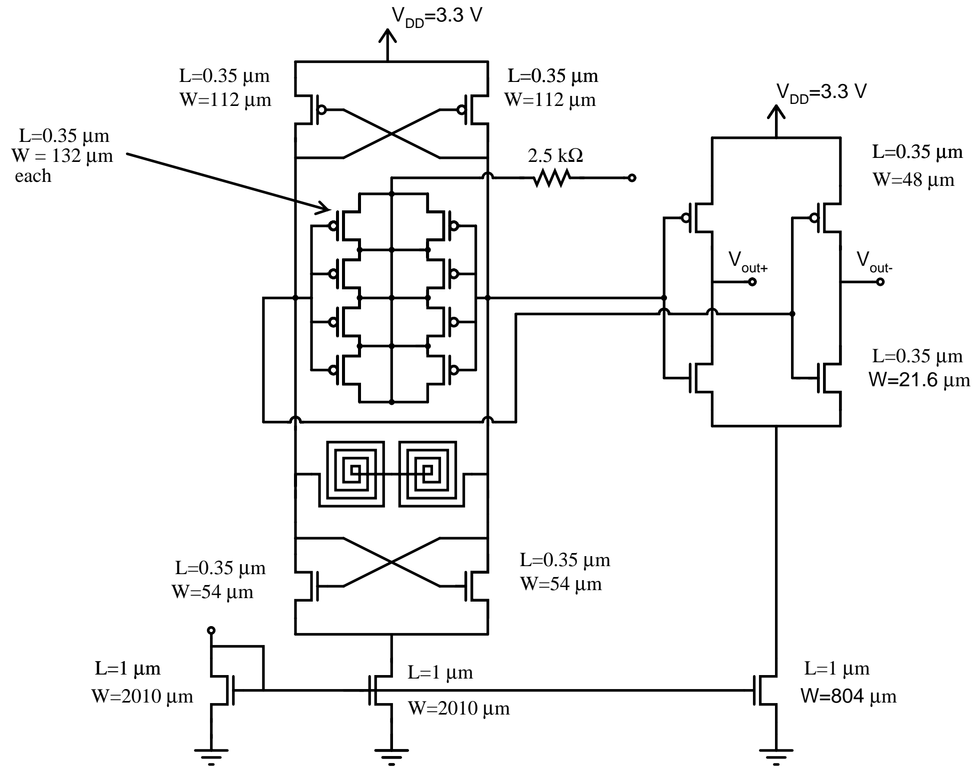

Figure 5.5: Complete buffered VCO design (Oscillator #2).

outputs are already at logic levels, the oscillator can directly drive into a CMOS inverter. The dimensions of the inverter devices can be chosen such that the switching point of the inverter is the same as the DC level of the oscillator outputs. This maximizes the gain available from the inverter. Since the DC level of the oscillator output will vary with the bias current, the inverting buffers must be designed to adjust to this voltage change. To address this, a current control device tied to the same mirror reference device as the VCO core itself was placed below the inverters. The second of the three fabricated oscillators was buffered in this manner (oscillator #2) and is shown in Figure 5.5. This circuit is identical to Figure 5.4 except that the output series resistors are replaced with CMOS inverters. Although the inverters present a high resistance to the tank circuit, their reactance is significant because of their gate capacitance. Each presents a capacitance of approximately 0.05 pF, which lowers the tuned frequency slightly. The small size of these inverters does not

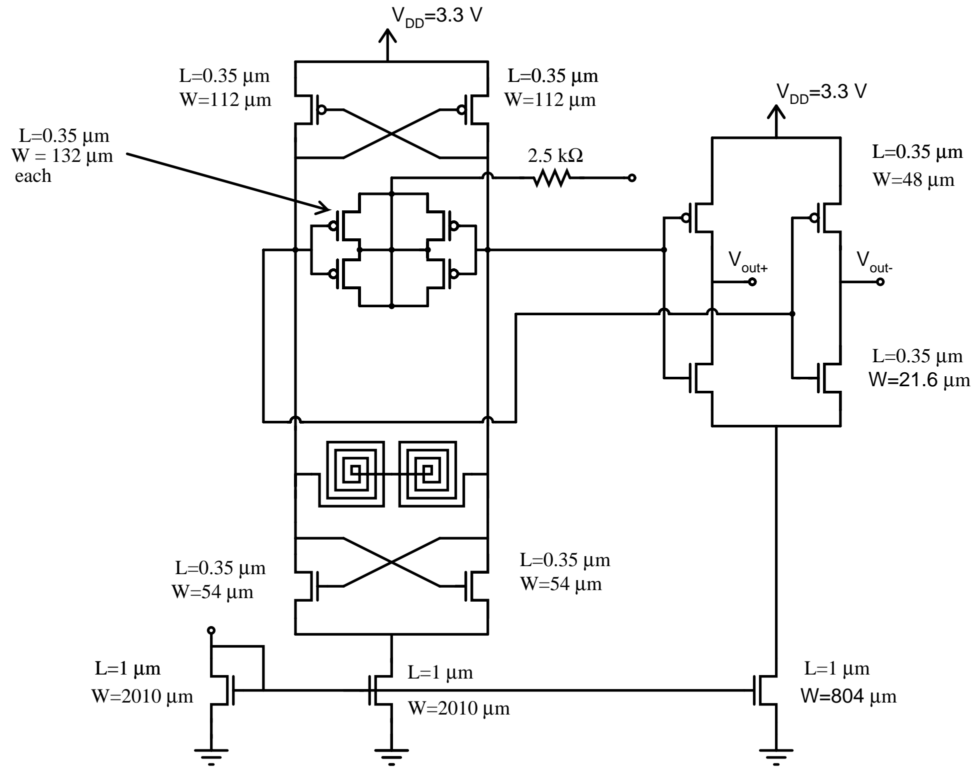

Figure 5.6: Complete re-tuned VCO design (oscillator #3).

allow them to drive a $50\,\Omega$ load rail-to-rail as typical logic inverters should. They do, however, act as amplifiers. Simulations show that these inverters can provide an output amplitude of 200 mV-peak into a $50\,\Omega$ load ($\approx -4\,dBm$).

Due to concerns about the accuracy of the inductor simulation [in particular, the Q versus frequency characteristic (Fig. 3.17 was a concern to the limitations of the planar (2.5D) EM simulation software that was used], a third version of the $-G_M$ oscillator was implemented. In order to ensure high oscillation amplitude and low phase noise, it is good practice to design an oscillator to operate near the peak Q of the resonator. If the peak Q occurs at a higher frequency than predicted the varactor may not provide enough tuning range to reach this frequency. The third oscillator (oscillator #3) addresses this possibility by implementing the varactor with exactly half the size of the varactor in the previous two designs (Fig. 5.6). This simple change

allows this circuit to oscillate at a frequency several hundred MHz higher than the original design. This *re-tuned* oscillator was implemented with a buffer identical to the one used in the second oscillator design. However, the tuning range of this VCO is lower because the variable capacitance (varactor), is now a much smaller fraction of the overall tank capacitance.

5.3 Oscillator Simulations

The oscillators of this thesis were simulated using Spectre. Spectre is a SPICE-like software package integrated into the Cadence IC design system [51]. All of the simulations performed during the design phase used the MOSIS extracted parameters for the January 2000 run of the TSMC[3] $0.35\,\mu m$ process. Although, TSMC provides binned[4] and corner[5] device models that are more accurate, the extracted BSIM3v3 parameters supplied by MOSIS were found to be sufficient early in the design phase. The MOSIS parameters used in designing these oscillators (and those extracted for the run on which the test chip was actually fabricated) are provided for reference in Appendix C.

Figure 5.7 shows the unbuffered oscillator as simulated in Spectre. The varactor is modeled as shown earlier with the series resistance calculated in Section 4.3 added as an extrinsic element. The "dual" inductor is modeled as a Spectre *nport* part that references an S-parameter data file. The inductor was simulated in Sonnet EM from 0.1-10.1 GHz to produce this S-parameter file. The control voltage, tail current bias, and power supply are all simulated as ideal voltage sources. The active devices in the negative resistance circuit have also been modified to reflect the actual layouts.

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[3] Taiwan Semiconductor Manufacturing Company

[4] "binning" involves defining a different device model for different ranges of device size in order to obtain a better fit over the range of device sizes available.

[5] Device "corner" refers to the worst case statistical variation of device parameters that are allowed in a given process.

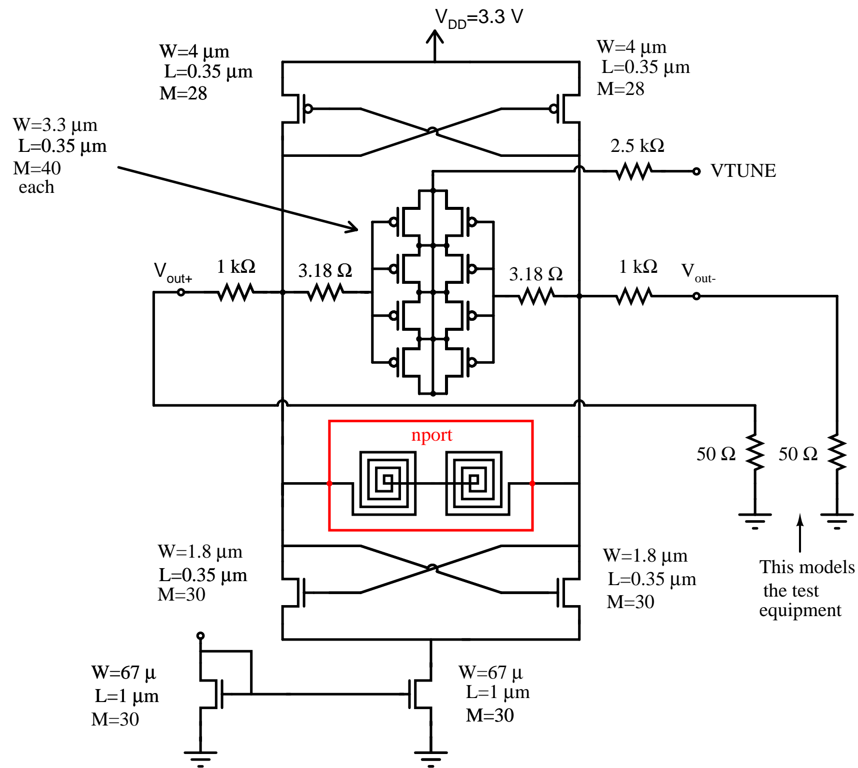


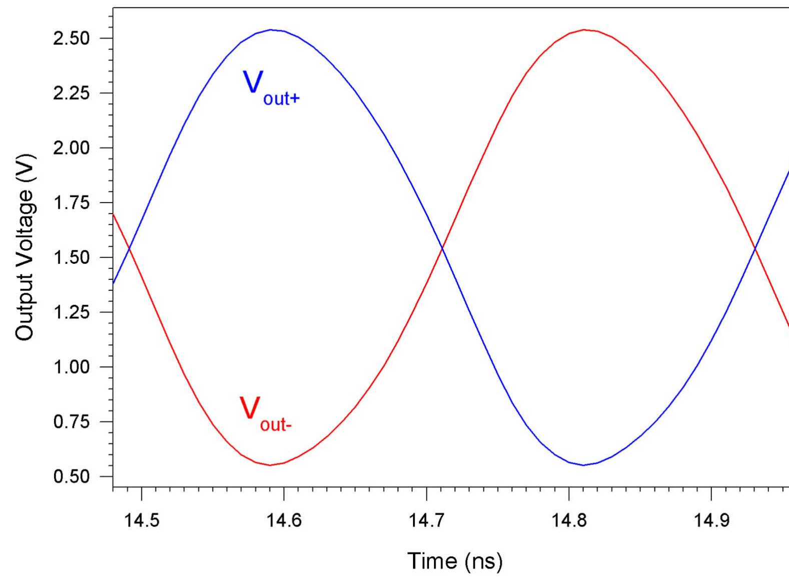
Figure 5.7: Simulated oscillator circuit. M = multiplicity factor used to simulated multi-finger devices.

Large devices are laid out as a number of smaller devices in parallel. The device multiplicity, m, represents the number of devices in parallel.

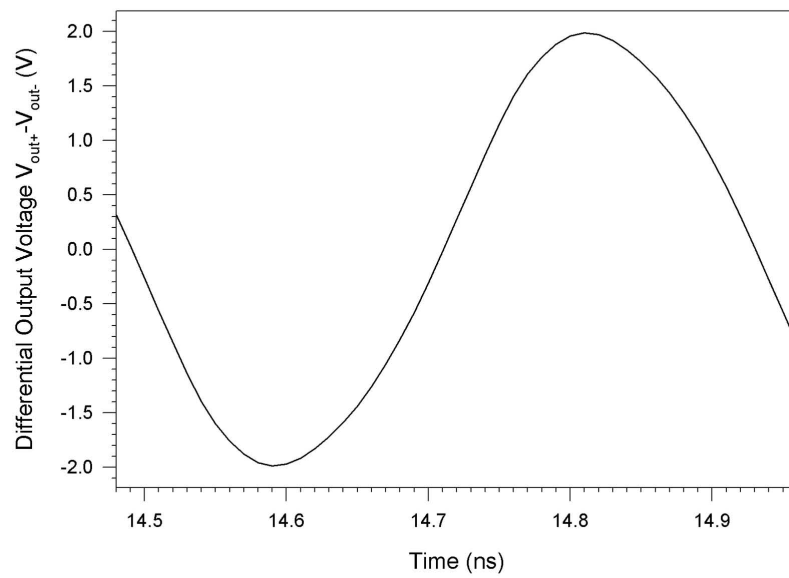
In order to simulate oscillator circuits, the tank circuit must be perturbed by a small transient. In reality noise that is present in the circuit should be sufficient to ensure oscillator startup. However, in simulation a piece-wise-linear current source in parallel with the tank circuit generates a short current pulse to trigger the oscillation. The maximum transient time step used was 0.01 ns. The maximum time-step must be much less than the oscillator signal period to ensure valid simulation results. The circuit shown in Figure 5.7 was simulated primarily to obtain the oscillation amplitude and the oscillation frequency. Figure 5.8 shows the steady state outputs of the oscillator at the low end of the tuning range (VTUNE = 3.3 V)—the waveforms are nearly sinusoidal. Figure 5.9 shows the simulated tuning curve of the oscillator. The predicted tuning range is 590 MHz (23%). The amplitude of the oscillations did not vary significantly over the tuning range. Simulations predict that this oscillator draws 12.4 mA at a supply voltage of 3.3V.

While these transient simulations are useful for evaluating key oscillator parameters, they tell the designer very little about the phase noise performance of the circuit. As was discussed in Section 2.6, phase noise predictions are always difficult. The Spectre circuit simulator can simulate phase noise, using a periodic steady-state (shooting method) approach. However, accurate simulations ultimately depend on accurate models. In this case, adequate noise models for the devices were not available. To accurately simulate the phase noise of the $-G_M$ oscillator, both the thermal noise and flicker (1/f) noise of the MOSFETs would need to be correctly modeled. A significant disadvantage to using digital CMOS to achieve RF functionality is the lack of noise models for the MOS devices.

In order to have some idea of the expected phase noise of the oscillator, the method of [7] was used (Sec. 2.6). Using Equation 2.14 the phase noise of the oscillator can be



(a)



(b)

Figure 5.8: Simulated oscillator output voltages: (a) single-ended outputs; (b) differential output.

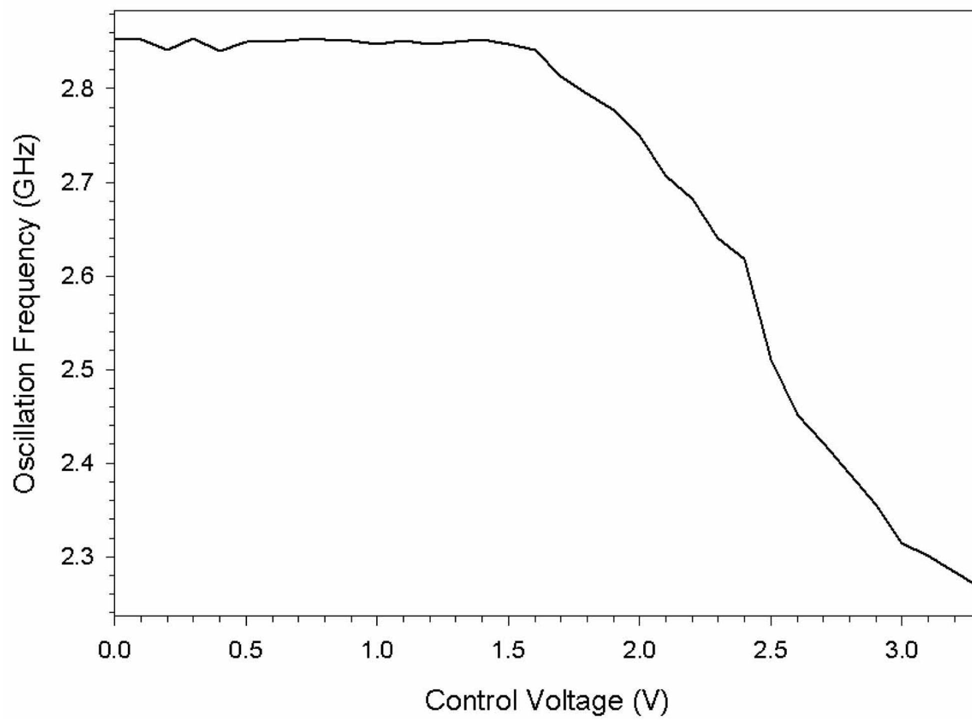


Figure 5.9: Simulated oscillator tuning characteristic. Tuning range: 590 MHz (23%).

predicted. From the preceding simulations, The peak differential voltage amplitude, V_A, is 2 V. For this simple analysis, $f_o = 2.5\,GHz$ is assumed. At this frequency the Q of the inductor is 3.1 (Sec. 3.6). The varactor Q is estimated to be 30 (Sec. 4.3). The total tank circuit quality factor can therefore be computed as:

$$Q_{tank} = \frac{1}{\frac{1}{Q_{varactor}} + \frac{1}{Q_{inductor}}} = \frac{1}{\frac{1}{30} + \frac{1}{3.1}} = 2.81. \tag{5.1}$$

Thus R_{eff} can be calculated,

$$R_{eff} = \frac{2\pi f_0 L}{Q_{tank}} = \frac{2\pi\,(2.5 \times 10^9)\,(4.59 \times 10^{-9})}{2.81} = 25.66\,\Omega \tag{5.2}$$

The excess noise factor A is typically set equal to the oscillator startup safety factor, which can be calculated as the ratio of the equivalent parallel resistance, R_{eq}, to the negative resistance generated by the circuit. R_{eq} is given by:

$$R_{eq} = Q_{tank} 2\pi f_o L = (2.81)\,(2\pi)\,(2.5 \times 10^9)\,(4.59 \times 10^{-9}) = 203\,\Omega. \tag{5.3}$$

Simulations have shown that the generated negative resistance is $\approx -104\,\Omega$, thus $A = 1.95$. After substituting these values into Equation 2.14, the expected phase noise can be predicted:

$$\mathcal{L}\{100\,kHz\} = \frac{(1.38 \times 10^{-23})\,(290)\,(25.66)\,[1 + 1.95]\left(\frac{2.5\times10^9}{100\times10^3}\right)^2}{\frac{2.0^2}{2}} = -100.2\,dBc/Hz. \tag{5.4}$$

When compared with recently published VCOs (Table 1.1), this appeared to be a reasonable result.

5.4 Test Chip Layout

All three versions of the VCO discussed in the preceding section were implemented in TSMC's 0.35 μm single-poly 4-metal (1P4M) process (available through MOSIS). The layout tool used was Cadence Virtuoso Layout Editor [52]. Circuit layout was

somewhat hampered by the lack of an industrial quality Cadence design kit for the TSMC 0.35 μm process. An available design kit was the Canadian Microelectronics Corporation (CMC)[6] CMOSP35v3.0 design kit. This design kit included the capability to design rule check (DRC) the circuit layout. However, this design kit was tailored for an older (2-poly, 3-metal, 2P3M) version of the TSMC 0.35 μm process. Although newer design kits are available from CMC, these were not available to MOSIS or the author due to licensing issues. Therefore the CMOSP35v3.0 design kit was locally modified to suit the needs of this project by adding the necessary code to support the 1P4M process. Although the design kit originally included code that allowed the circuit netlist to be extracted from layout for simulation, this functionality was not achieved in the locally modified version.

The test chip was not fabricated with the intent of packaging the die. For all measurements, a Cascade[7] probe station was to be used to directly probe the die. Microprobing the die, rather than having it bondwired to a package allows the designer much more flexibility in the placement of bond pads on the test chip. Since clearance between bondwires was not a concern in this case, most of the strict rules for bondpad placement could be ignored. For example, this permitted the placement of bondpads in the interior of the layout rather than just at the edges, allowing the die area to be more fully utilized. However, one of the drawbacks to microprobing[8] is that the number of simultaneous inputs and outputs is limited.

When laying out a circuit for microprobing, the *pitch* of the probe pads must match that of the probes. Pitch is defined as the distance between the centers of adjacent probe pads. Since all available probes had a pitch of 150 μm, and a layout for 100 μm

[6]Canadian Microelectronics Corporation (CMC) is a not-for-profit organization established in 1984 to provide industrial microelectronic technologies to Canadian universities/educational institutions (similar to the US MOSIS and European CMP).

[7]Cascade Microtech, Inc.

[8]Although, there are specialized probe cards and membrane probes available that do permit a large number of probe connections, such specialized probe fixtures were not available.

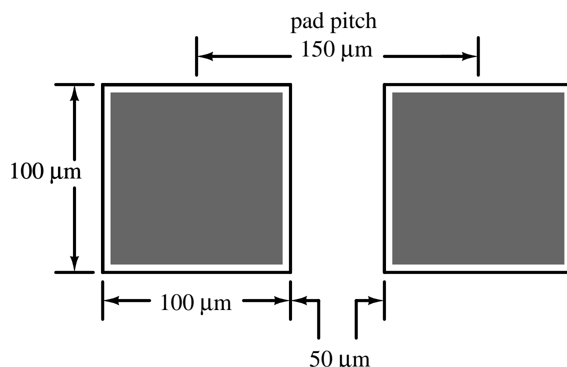


Figure 5.10: Probepad structure.

square bond pads was readily available, it was decided to use 100 μm pads with a spacing of 50 μm. Figure 5.10 shows this arrangement. The bondpads used were modified from bond pad layout cells included in the CMOSP35v3.0 design kit. The bond pads in this design kit were tailored for use as digital I/O pads and included digital buffering circuitry as well as ESD[9] protection structures. Because the pads used in this project are for RF/DC signals, this additional circuitry was removed from the pad structures. ESD protection was deemed unnecessary since the die was to be microprobed. In addition, the bondpad was modified for the 4-metal process.

Figure 5.11 shows the layout of the unbuffered version of the oscillator (corresponding to Fig. 5.4). The four pads at the top of the layout are the DC bias connections: IBIAS, GND, VDD, and VTUNE. The bottom four pads are in a GSSG (ground-signal-signal-ground) configuration; the differential RF output of the VCO is extracted through the two signal pads (V_{out+} and V_{out-}). The buffered and retuned VCOs are laid out in the same configuration, with their respective modifications. The die area of the unbuffered VCO including the bond pads is 550 $\mu m \times 700\,\mu m$.

Figure 5.11 also highlights the different structures that make up the VCO. The varactor and inductor have already been discussed in the preceding chapters. The resistors are implemented using polysilicon over n-well. The resistance of a rectangle of poly

[9]Electro-Static Discharge.

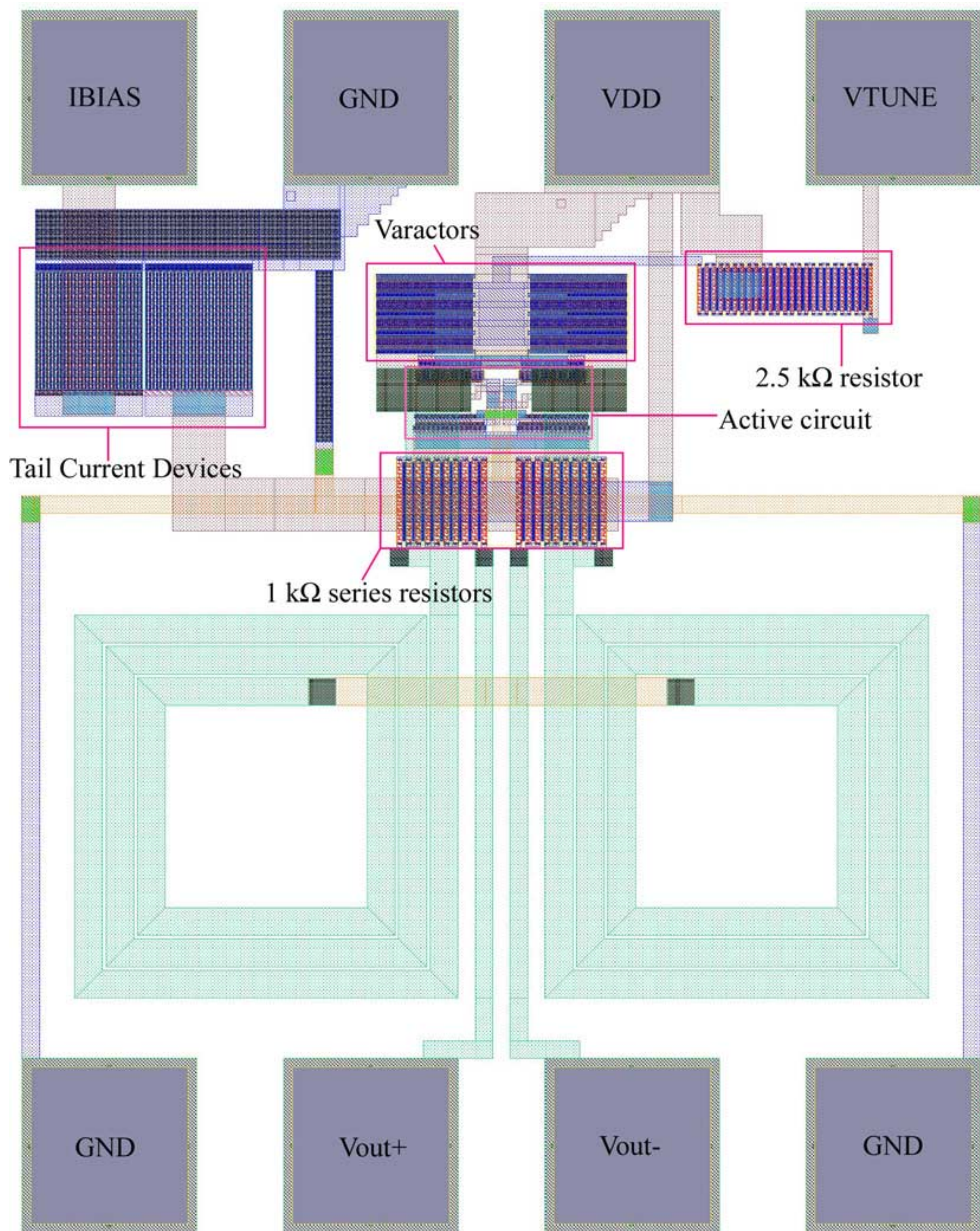


Figure 5.11: Unbuffered Oscillator (VCO #1).

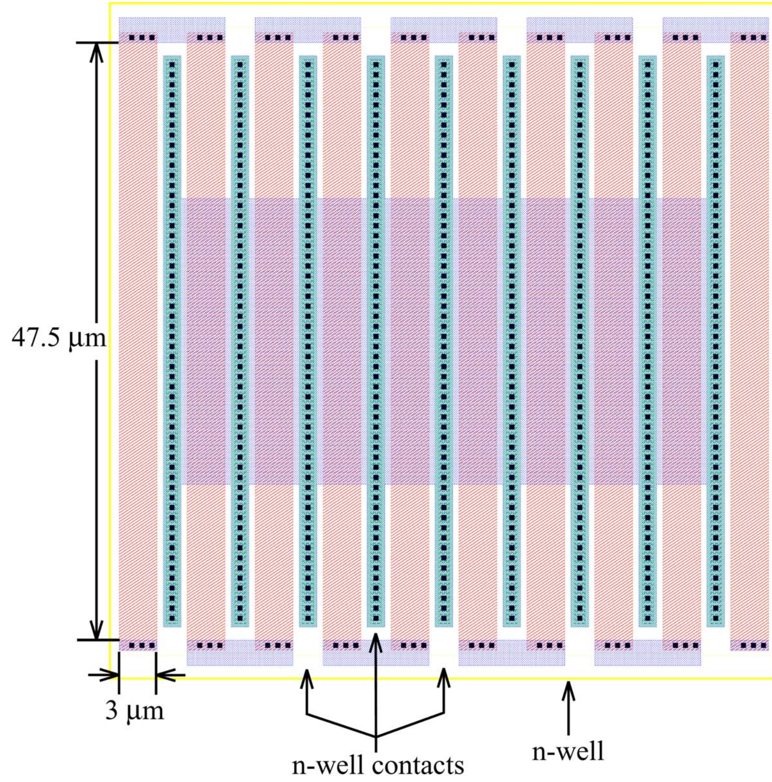


Figure 5.12: Layout of $1\,k\Omega$ resistor.

is determined by:

$$R_{poly} = \frac{L}{W}\,R_{poly,\square}, \tag{5.5}$$

where W and L are the width and length of the rectangle and $R_{poly,\square}$ is the polysilicon sheet resistivity (in this process $R_{poly,\square} = 6.3\,\Omega/\square$). Figure 5.12 shows the structure of the $1\,k\Omega$ series resistors. The resistor is implemented as 10, $100\,\Omega$ segments. Each $100\,\Omega$ segment is implemented as a $47.5\,\mu m \times 3\,\mu m$ rectangle. The n-well area under the poly segments is connected to V_{DD}. The $2.5\,k\Omega$ resistor in the is implemented using a similar structure. For this application the exact values of these resistors is not critical.

In order to completely characterize the VCOs, a variety of on-chip test structures were also fabricated. These test structures allow the performance of the individual components of the VCO to be isolated. In particular, the tank circuit inductor (Fig.

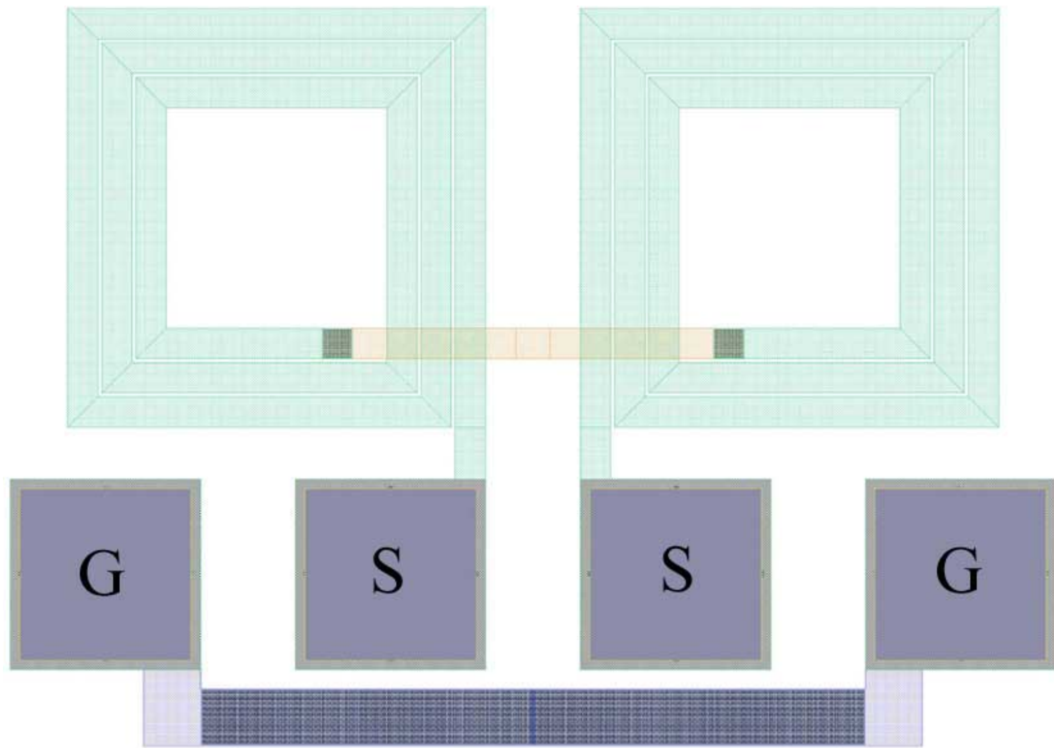


Figure 5.13: Inductor test structure.

5.13), the varactor (Fig. 5.14), and the active portion of the VCO (Fig. 5.15) were laid out as isolated components connected directly to probe pads. The aforementioned arrangement of GSSG pads was used for each test structure. Open circuit and short circuit calibration structures were also implemented (Figs. 5.16 and 5.17). These two structures enable the de-embedding of the pad characteristics. Using these structures the Q of the inductor and varactor can be measured accurately. In addition, the negative resistance supplied by the active devices can be directly determined.

The TSMC 0.35 μm process, as well as many other sub-micron processes, has a number of design rules that require a minimum layer density on each interconnect layer. The 1P4M process requires that each metal layer cover at least 30 percent of the layout area, and that polysilicon cover at least 15 percent of the layout area. These density rules are enforced for every 1 mm^2 of the layout. These rules are required

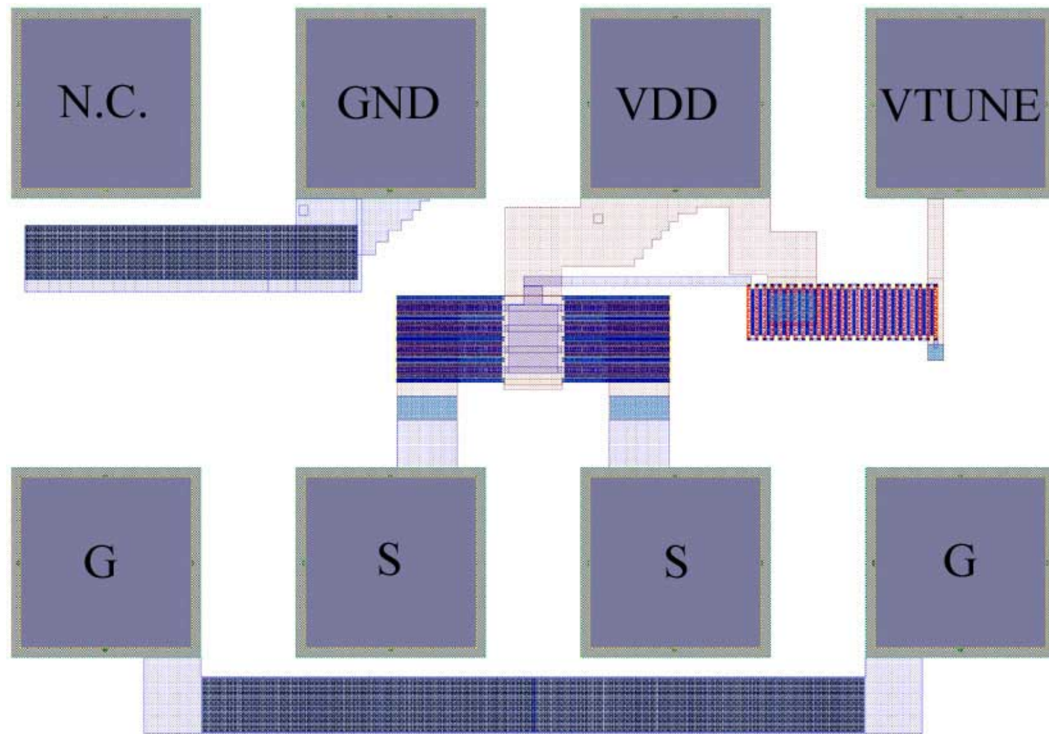


Figure 5.14: Varactor test structure.

to maintain the planarity of the wafers during fabrication (for CMP[10] steps) and are easily satisfied for most digital designs. If the layout does not meet these density requirements, MOSIS will by default fill the open areas of the layout with a passive fill pattern. For RF designs this is *not* acceptable. The layout area around the inductors must be free of any other metal structures so that undesired eddy currents (which would degrade the quality factor) are not generated. For this project large strips of metal (1-4) and polysilicon sandwiches were placed in the layout as area fill. This area fill was connected to the substrate so that it would not remain floating in order to avoid ESD (electro-static discharge) problems.

The complete test chip includes the 3 VCO's, the test structures mentioned above, area fill, and a few additional test structures. It also contains 4 ring oscillators that will be used for future mixed-signal measurements. The complete test chip is shown

[10]Chemical/Mechanical Polishing.

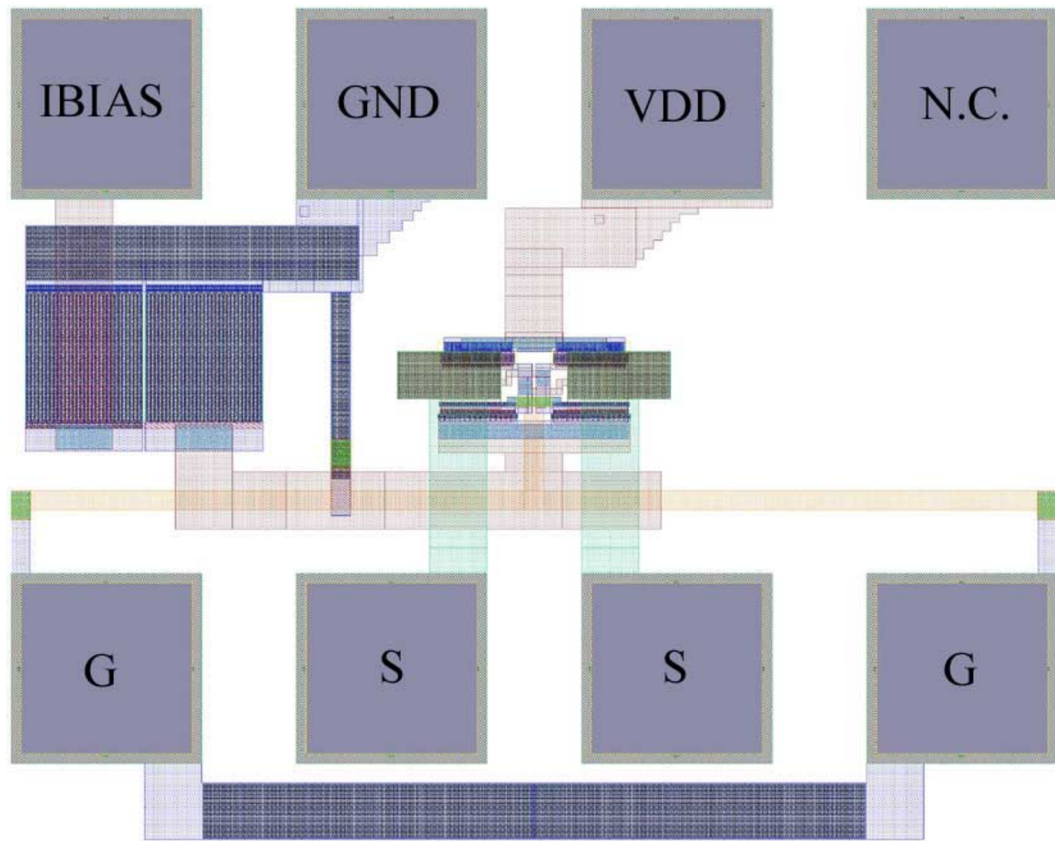


Figure 5.15: Active circuit test structure.

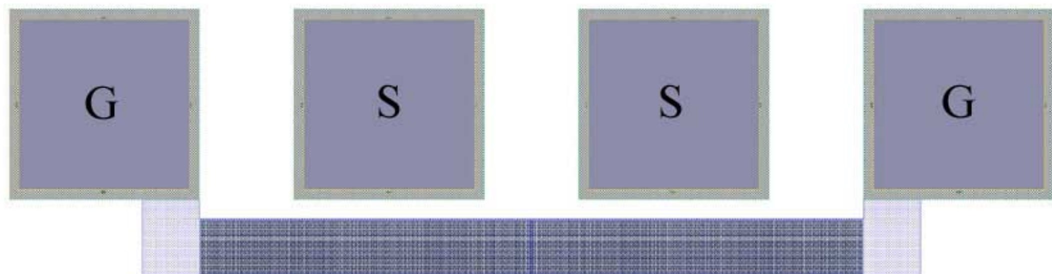


Figure 5.16: Open circuit bondpad test structure.

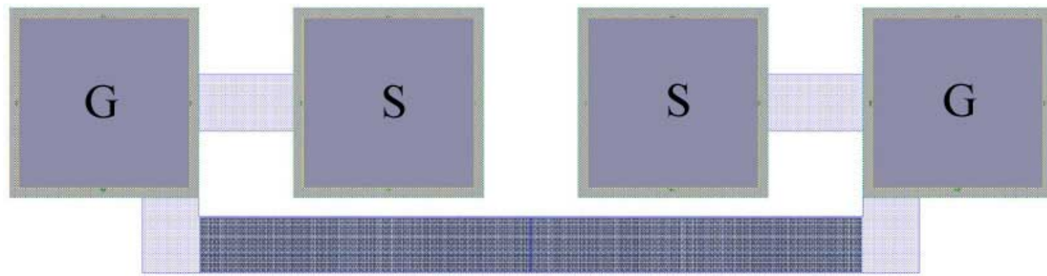


Figure 5.17: Short circuit bondpad test structure.

in Figure 5.18 with the different structures labeled. The overall dimensions of the chip are $2600\,\mu m \times 2050\,\mu m$. The test chip layout was submitted to MOSIS for the Aug. 14, 2000 run of the TSMC 1P4M $0.35\,\mu m$ process.

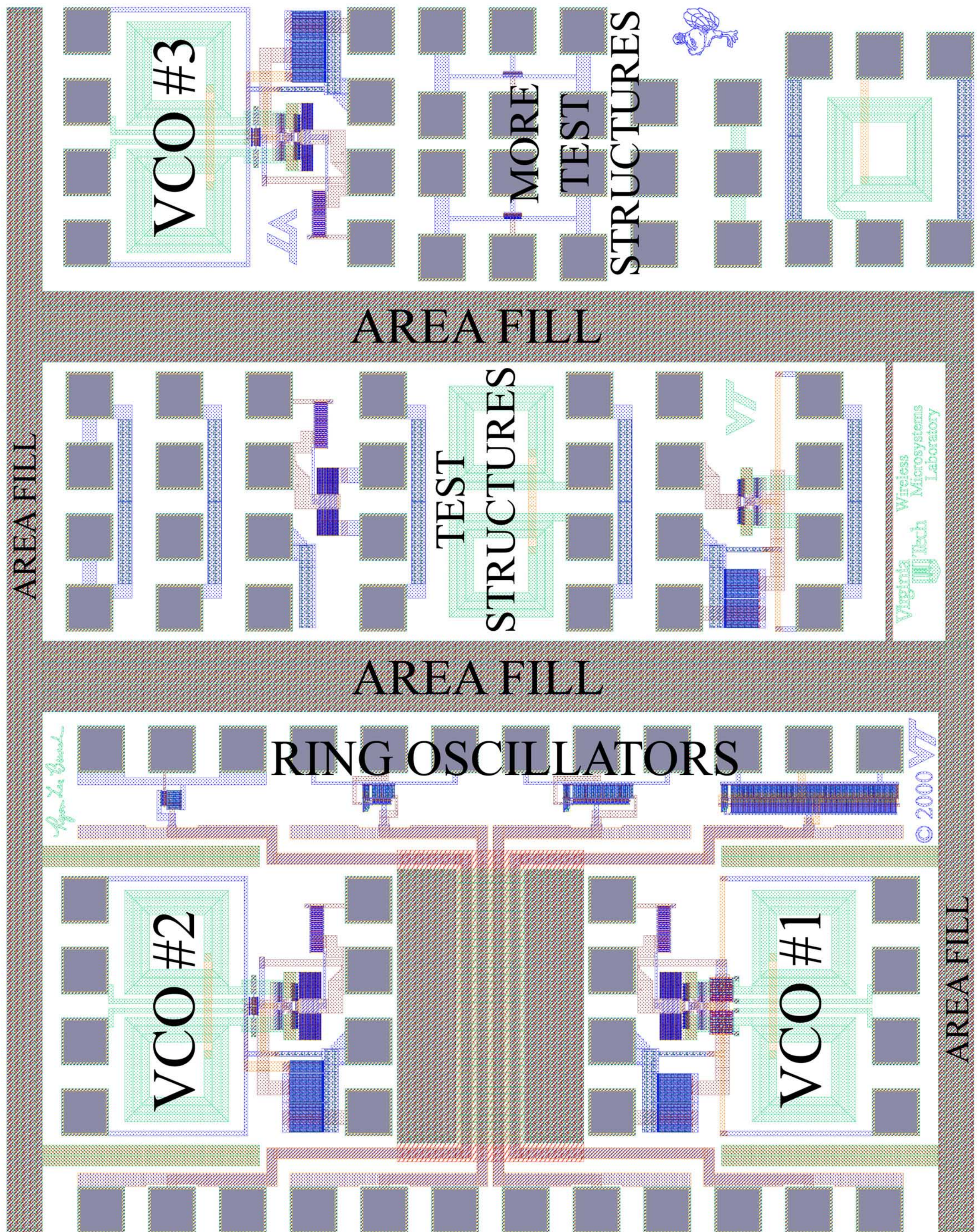


Figure 5.18: Complete test chip.

Chapter 6

Measured Results

This chapter presents the full characterization of the VCOs and test structures on the fabricated CMOS die. First, the performance of the passive test structures are discussed; then the detailed oscillator measurements are presented.

The test chips were received from MOSIS as loose unpackaged die. A photograph of the fabricated test chip is shown in Figure 6.1. The MOSIS layout overhead is clearly visible at the left and at the top of the photograph.

The measurements presented here were made using a Cascade on-wafer probe station. In order to facilitate probing, the die were attached to gold plated carrier substrates using conductive silver epoxy. These substrates provided sufficient surface area for the probe station chuck vacuum to be effective, and also improved mechanical characteristics during handling. Figure 6.2 shows a photograph of a mounted die on the probe station chuck with probes in contact.

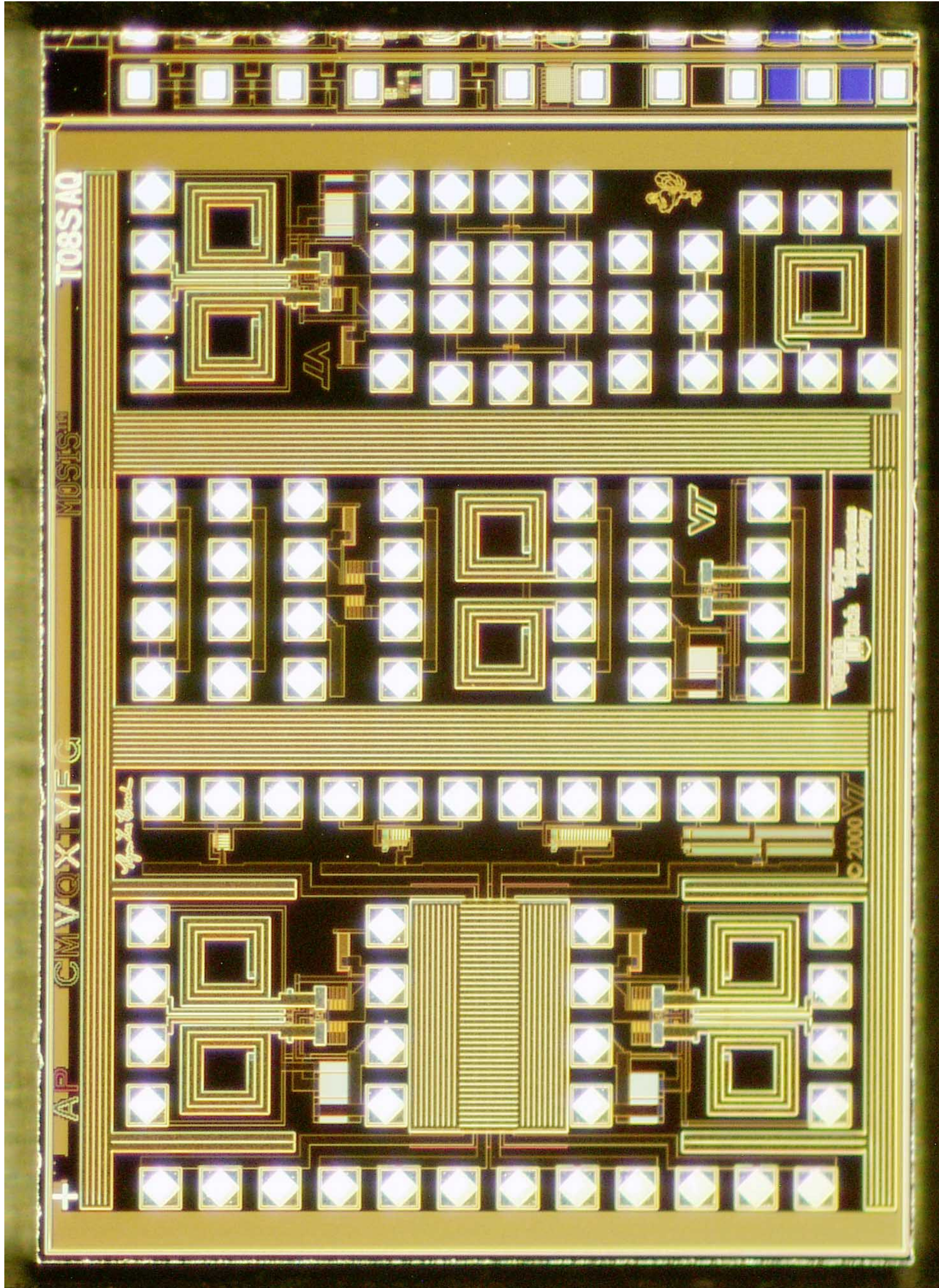


Figure 6.1: Fabricated CMOS test chip.

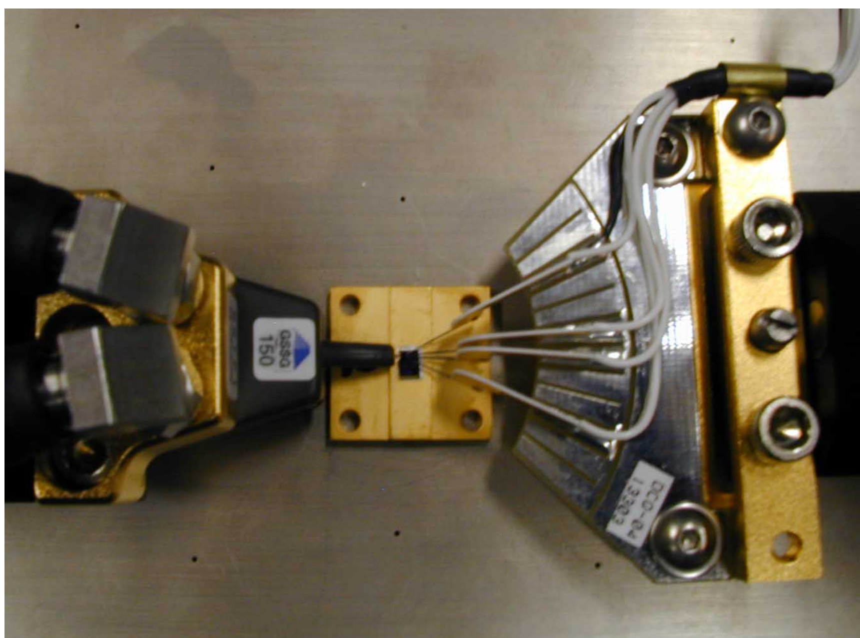


Figure 6.2: Carrier substrate with probes contacting the test chip.

6.1 One Port Test Structure Measurements

The test chip included a number of test structures (as discussed in Section 5.4) to facilitate comparisons with simulation and correlation with overall oscillator performance.

In order to measure the inductor and varactor characteristics, a *differential* one-port measurement method was used (Fig. 6.3). Bias tees were necessary to bias the gate of the varactor; for inductor measurements the DC port of the tees were left open. The GSSG probe head has two independent coaxial connections; in order to make a one-port differential measurement the independent connections feed the -3 dB ports of a 180° hybrid coupler (in this case an Anaren 3A0200 1.3-2.6 GHz 180° hybrid was used). The signal from the difference port (Δ) is then fed into the network analyzer. This method is effectively the same as using a balun transformer to convert a differential signal into a single ended signal. However, no suitable balun was available for the frequency range of interest. The network analyzer was calibrated to cancel

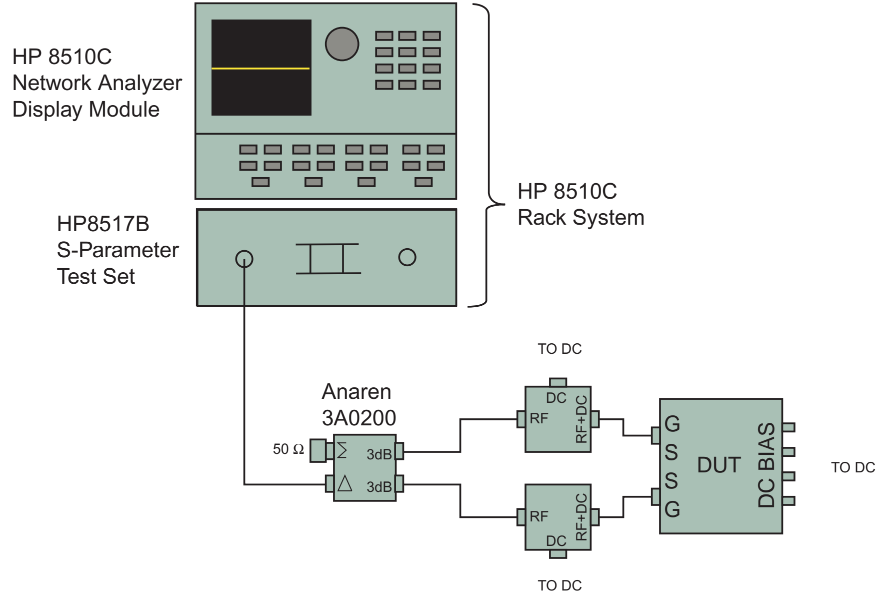


Figure 6.3: Differential single port test setup.

the loss in the cables, bias tees, hybrid coupler, and probes by performing a one-port short-open-load (SOL) calibration procedure using an impedance standard substrate. For this calibration the impedance standards were connected between the signal pads of the GSSG probe. The reference impedance of the analyzer was set equal to the DC resistance of the load standard which was measured using a multimeter prior to the calibration. The calibrated one-port measurements yielded values of S_{11} vs. frequency, which are easily converted into input impedances or admittances. Since the CMOS substrate is much more lossy than the calibration substrate, the effect of the CMOS bond pads must be de-embedded. In this case the effect of the bond pads was modeled as a shunt element (Fig. 6.4). Thus, the input admittance of the device under test can be calculated as:

$$Y_{DUT} = Y_{measured} - Y_{pads}, \tag{6.1}$$

where the Y parameters are calculated from the measured S-parameters using:

$$Y_{in} = Y_0 \frac{1 - S_{11}}{1 + S_{11}}. \tag{6.2}$$

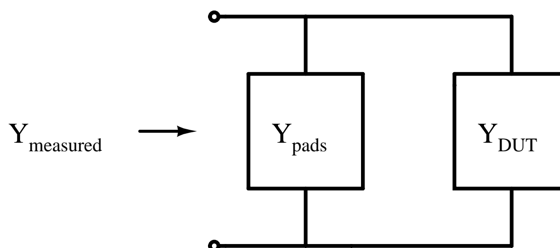


Figure 6.4: Bond pads as a shunt element.

The one port measurement method utilized here treats the inductor as a balanced differential element and is equivalent to the floating or differential inductor definitions discussed earlier (Sec. 3.4). One issue with the measurements here is the limited frequency range of the 180° hybrid used. However, this frequency range does cover enough of the oscillator tuning range to provide useful insight.

6.2 Inductor Measurement

S_{11} vs. frequency of the inductor test structure (Fig. 5.13) was measured using the one-port method described above. The data represents the average of 9 independent measurements. Figure 6.5 shows the de-embedded inductor input impedance versus frequency. The corresponding quality factor and inductance vs. frequency are shown in Figures 6.6 and 6.7 respectively.At 2.5 GHz the measured inductance and quality factor of the inductor are 4.49 nH and 2.88 respectively, compared to the simulated values of 4.59 nH and 3.1. The inductance is only slightly lower, but the quality factor is lower by a relatively significant amount. This may be because only planar 2.5D simulations were performed, neglecting some important parasitic effects as discussed in Section 3.5. In addition, the exact value of the CMOS substrate resistivity is still unknown. Comparing the measured results in Figure 6.6 to the simulated results in Figure 3.17, the expected trend of an increasing Q with frequency is observed. However, the relatively narrow-band coupler did not allow a broader band response

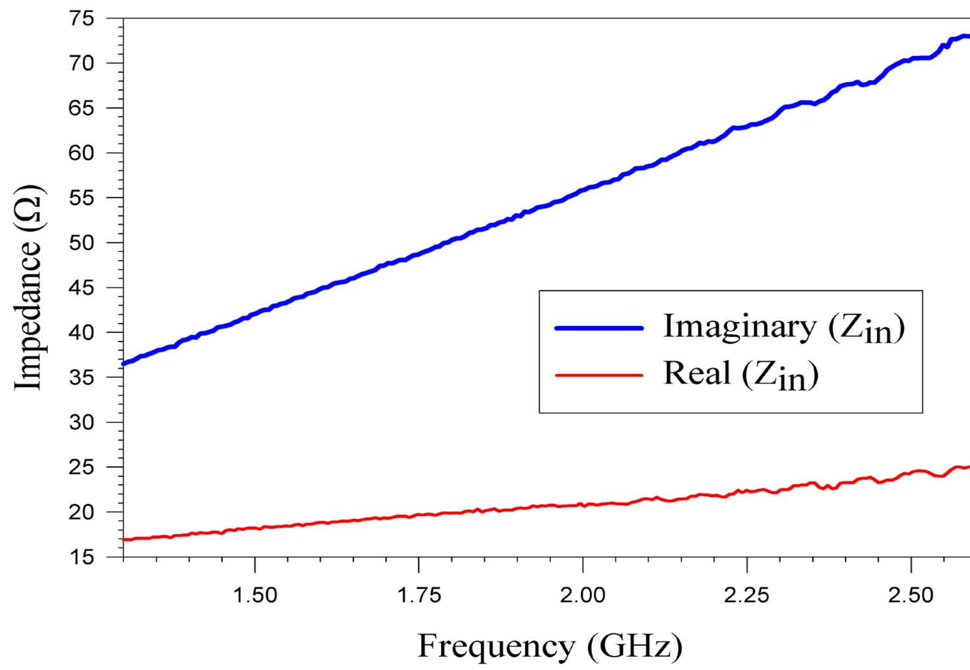


Figure 6.5: Measured differential tank inductor input impedance.

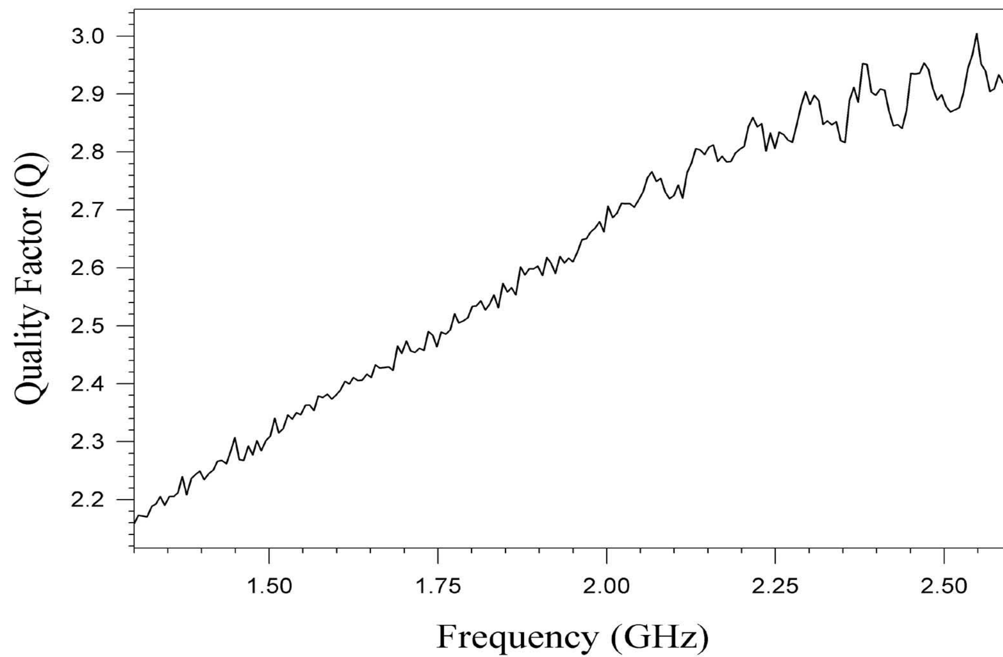


Figure 6.6: Measured differential tank inductor quality factor.

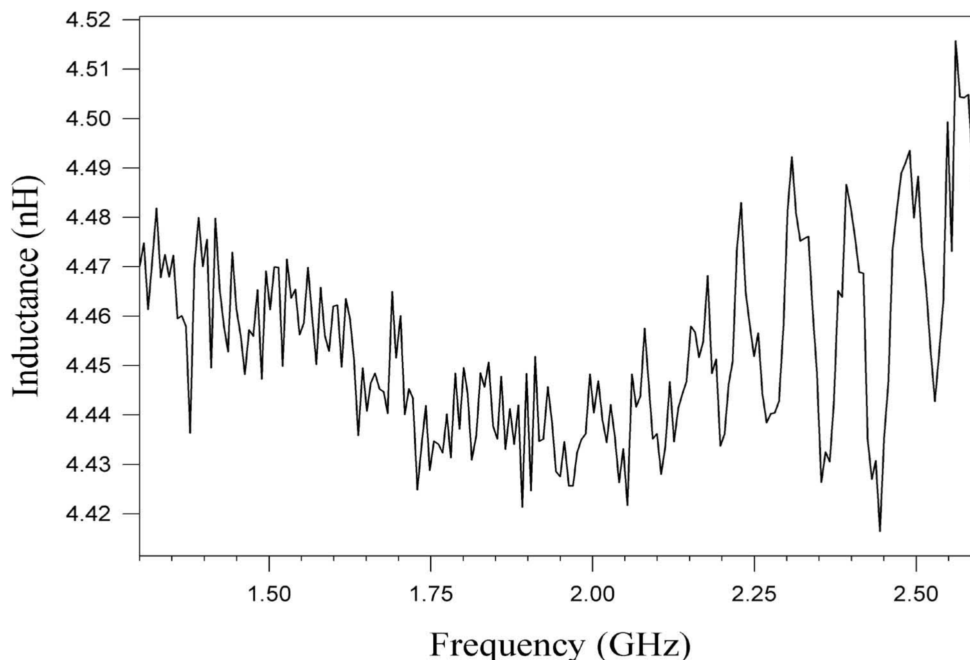


Figure 6.7: Measured differential tank inductor inductance.

to be measured. The data points in these graphs have a high degree of variability at the high end of the frequency range (near 2.6 GHz). This effect was noticed throughout all the one port measurements and may be a characteristic of the hybrid coupler used. The DC resistance of the inductor was measured to be approximately $10\,\Omega$; this value was somewhat lower than expected and is a result of the actual sheet resistivity for metal 4 in this fabrication run (see Appendix C) being lower than the value used in the Sonnet simulations ($0.03\Omega/\square$ as opposed to $0.05\Omega/\square$). This leads to the conclusion that the inductor Q is dominated by the substrate effects.

6.3 Varactor Measurements

S_{11} vs. frequency of the tank circuit varactor test structure was also measured using a similar one-port test configuration. Measurements on the varactor are complicated

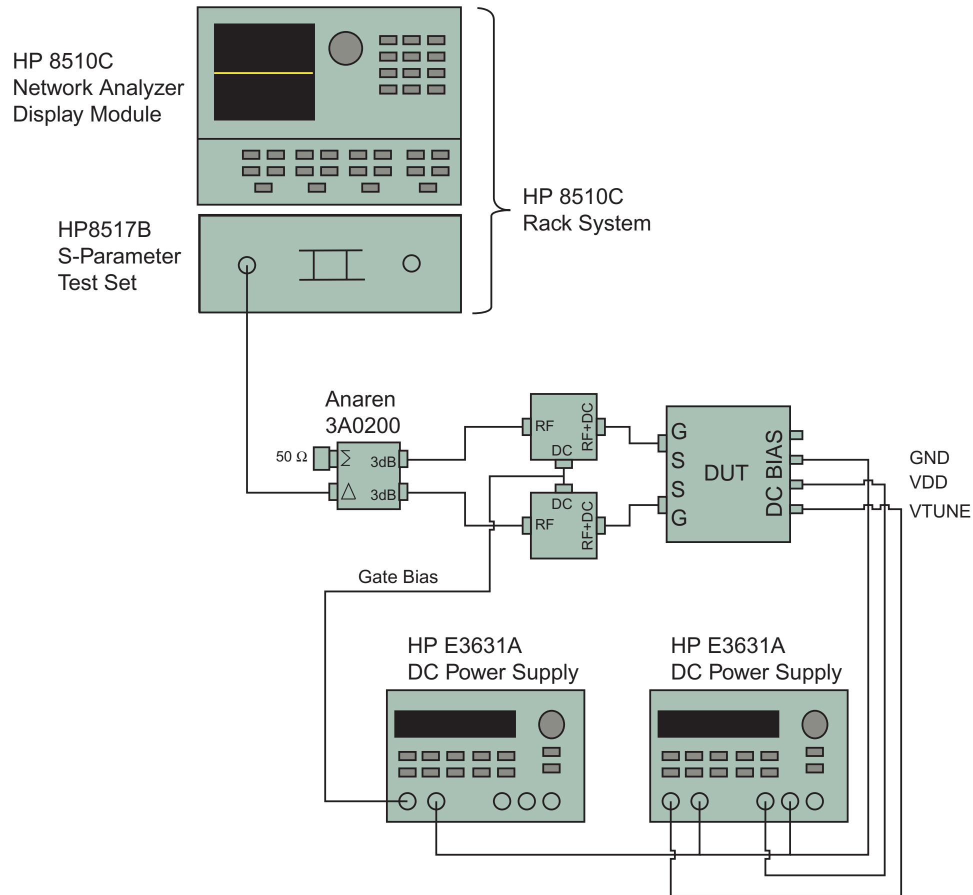


Figure 6.8: Varactor test setup.

by the DC bias requirements. Since the DC voltage at the gate of the varactors (V_g) is around $\frac{V_{DD}}{2} = 1.65\,V$ during normal oscillator operation, the DC gate voltage on the varactor test structure is set to $1.65\,V$ during measurements. Figure 6.8 shows the test setup. The bias tees are used to supply $1.65\,V$ to the gates of the varactor, and the DC probe is used to bias the varactor (i.e. it supplies V_{DD}, GND, and V_{TUNE}). The varactor input impedance was measured versus frequency for tuning voltages from 0 to $3.3\,V$. The capacitance of the varactor does not show any significant change versus frequency. This was expected since the capacitance of the varactor acts as a simple parallel plate capacitor. At the frequencies involved distributed effects are negligible.

The measured tuning curve of the varactor is shown in Figure 6.9. The capacitance

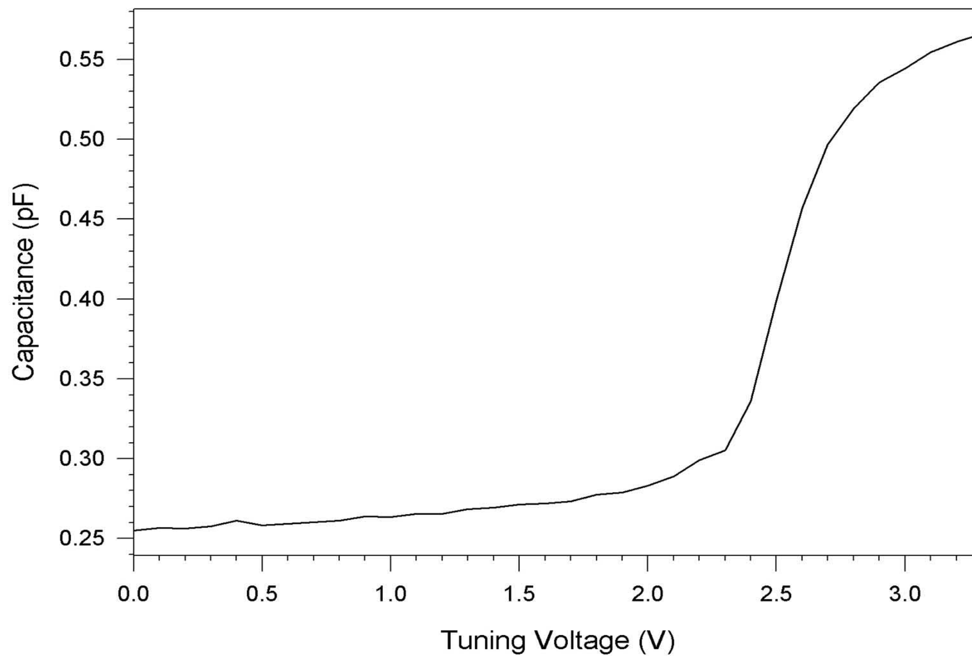


Figure 6.9: Measured varactor small signal capacitance versus tuning voltage.

values shown in this figure are the average of the capacitance from 1.3-2.6 GHz. This averaging has little effect on the overall curve since the capacitance varies only a few percent over this frequency range. The curve shown in Figure 6.9 matches reasonably well with the simulated results shown in Figure 4.7. However, the measured $C_{MIN} - C_{MAX}$ transition is not as steep because the voltage amplitude of the network analyzer source is high enough to result in the nonlinear effects discussed in Section 4.4. An attempt was made to utilize the VNA's internal port attenuation to lower the voltage amplitude in order to more accurately measure the abrupt small-signal tuning curve. However, at low signal levels the one port calibration became inaccurate as the losses in the hybrid coupler became dominant.

For tuning voltages near zero, the quality factor of the varactor was too high to measure since the resistive part of the measured input impedance is very small (below the noise floor of the measurement) and the plot of its Q versus frequency characteristic

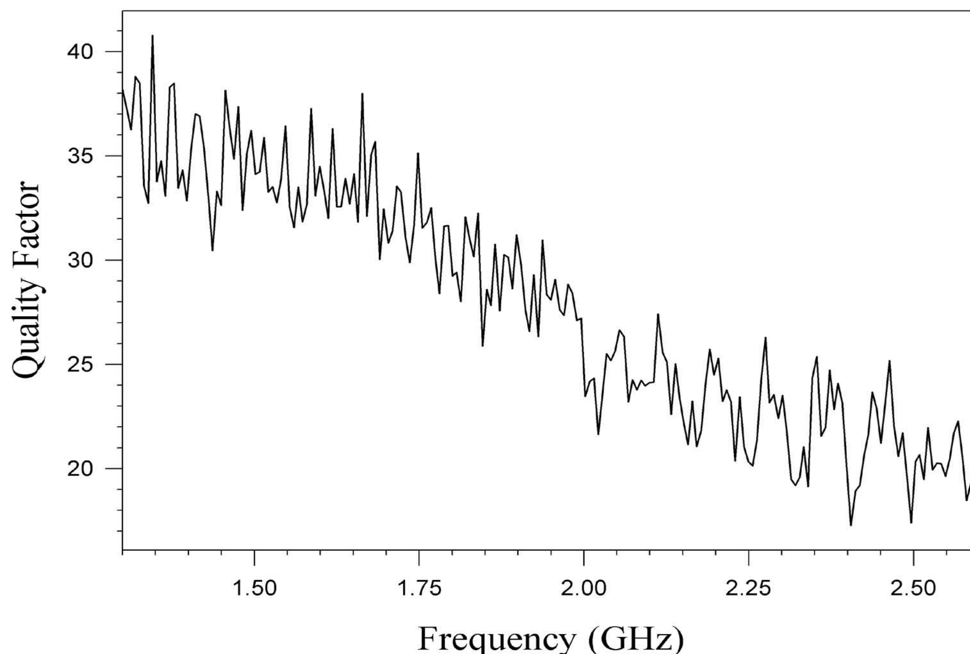


Figure 6.10: De-embedded varactor Q versus frequency, $V_{TUNE} = 3.3\,V$, $V_g = 1.65$.

becomes very erratic. The series resistance is small for low tuning voltages since the channel of the varactor is strongly inverted (i.e. $R_{ch,\square}$ is low). However, the quality factor is well over 100 at nearly every frequency point. For tuning voltages near $V_{DD} = 3.3\,V$ the quality factor was much lower. At this operating point the channel of the varactor is no longer strongly inverted (i.e. $R_{ch,\square}$ is high). Figure 6.10 shows a plot of the varactor quality factor versus frequency for $V_{TUNE} = 3.3\,V$. The quality factors shown in this figure are in the same range as predicted in Section 4.3.

6.4 Negative Resistance Circuit Measurements

The final test structure that was measured was the *tankless* active portion of the VCO. This structure was fabricated so that the negative resistance characteristic presented to the tank circuit by the active devices could be characterized. Although there are

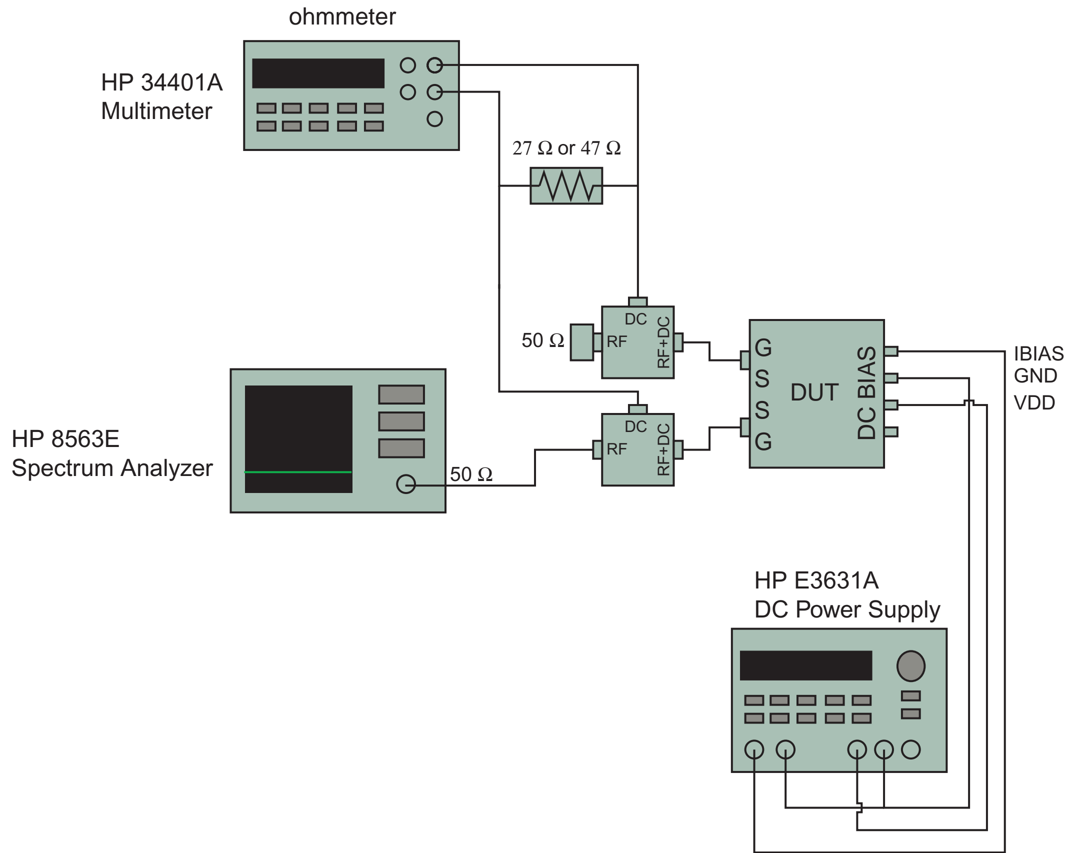


Figure 6.11: Negative resistance measurement configuration.

methods for directly measuring this negative resistance at RF, only the static (DC) nonlinear I-V curve has been measured at the time of this writing.

The maximum negative resistance generated by the active circuit is approximately $-100\,\Omega$. This negative resistance cannot be measured directly using the test equipment available; however, if a positive resistance less than $100\,\Omega$ is placed in parallel with this negative resistance then their parallel combination becomes positive. In order to measure the DC negative resistance, the measurement configuration shown in Figure 6.11 was used. The DC bias tees allow the outputs of the tankless VCO to see an AC termination of $50\,\Omega$ (This prevents RF oscillations.). One side of the differential output is connected to the $50\,\Omega$ input of a spectrum analyzer, while the other side is connected to a $50\,\Omega$ precision termination. Having one terminal con-

Table 6.1: Negative resistance for 27 Ω resistor.

$I_{tail}\,(mA)$	$R_{test}\,(\Omega)$	$R_{measured}\,(\Omega)$	$R_{negative}\,(\Omega)$
1.0	29.053	32.803	-254.1
1.5	29.047	33.79	-206.9
10	29.047	39.23	-111.9

Table 6.2: Negative resistance for 47 Ω resistor.

$I_{tail}\,(mA)$	$R_{test}\,(\Omega)$	$R_{measured}\,(\Omega)$	$R_{negative}\,(\Omega)$
1.0	51.1	63.463	-262.3
1.5	51.1	67.24	-212.9
10	50.75	94.5	-109.62

nected to the spectrum analyzer is helpful since the stability of the circuit can be visually verified. For this measurement the output spectrum should remain flat, since oscillations will disturb the measurement. Using the DC output of the bias tees, a resistor can be placed in parallel with the negative resistance. If this resistance is measured with an ohmmeter it will appear larger than its actual value. The negative resistance can be calculated as:

$$R_{negative} = \frac{R_{test} R_{measured}}{R_{test} - R_{measured}}, \tag{6.3}$$

where R_{test} is the value of the resistor placed in parallel with the VCO negative resistance, $R_{measured}$ is the parallel combination measured by the ohmmeter, and $R_{negative}$ is the negative resistance generated by the active circuitry. Two standard 10 percent resistors were used for R_{test}. Tables 6.1 and 6.2 show the results for the two resistors. At 10 mA, the maximum bias current of the active circuit for $V_{DD} = 3.3\,V$, these results show that the maximum negative resistance is approximately $-110\,\Omega$. This agrees well with the simulated value of $-104\,\Omega$. The negative resistance was also measured at 1.0 mA and 1.5 mA since these currents were measured to be the conditions of impending oscillation for $V_{TUNE} = 0$ (f_{max}) and $V_{TUNE} = 3.3$ (f_{min}),

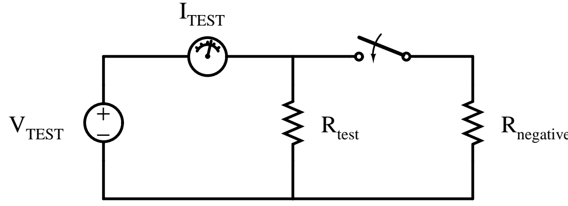


Figure 6.12: Circuit for Equation 6.4.

respectively. Oscillation occurs at lower bias currents for higher frequencies since the equivalent parallel resistance, R_{eq}, is larger at higher frequencies. Therefore, these measurements also give an indication of total tank circuit Q seen by the active circuit of the oscillator, assuming that the negative resistance at DC is approximately equal to the negative resistance at RF (a valid assumption if $R_g C_{gs}$ is small, see Appendix A).

The I-V characteristic of the tankless VCO can be measured by connecting a voltage source across the test resistor and measuring the current versus voltage with the active circuit both off and on as shown in Figure 6.12. The current through the negative resistance (using the passive sign convention) can then be calculated as:

$$I_{TEST} = I_{TEST(ON)} - I_{TEST(OFF)} \tag{6.4}$$

where $I_{TEST(OFF)}$ is the current supplied the voltage source when the active circuit is disconnected, and $I_{TEST(ON)}$ is the current supplied by the voltage source when the active circuit is operating. Figure 6.13 shows the measurement setup used to measure the I-V curve shown in Figure 6.14. The measured I-V characteristic has the shape that was expected from the simulated results.

6.5 Oscillator Measurements

All three oscillator circuits were measured on-chip using the Cascade probe station. A GSSG probe was used to extract the differential signal. A 4 contact DC probe was

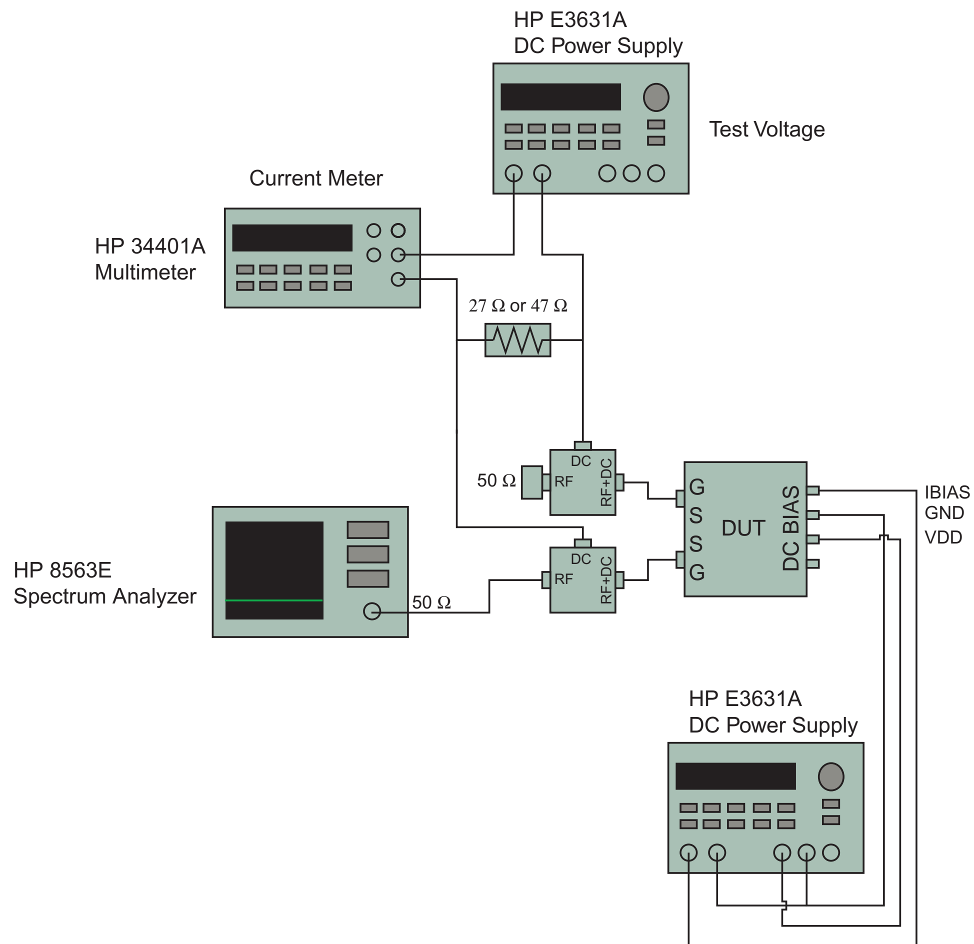


Figure 6.13: I-V characteristic measurement method.

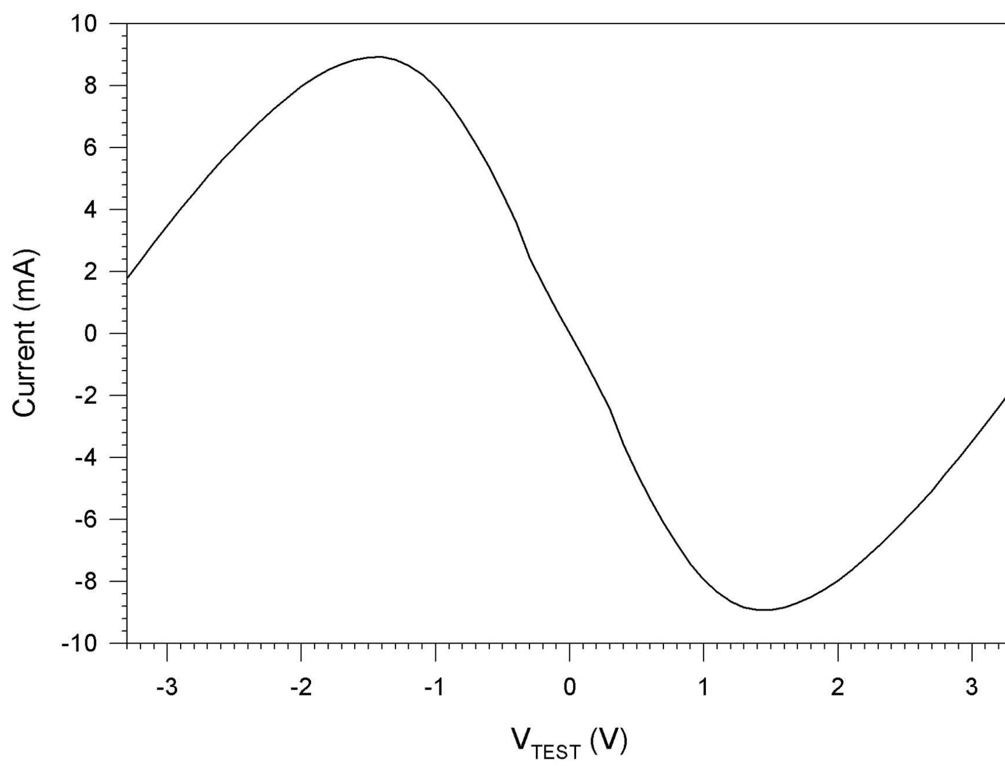


Figure 6.14: Measured I-V characteristic of the negative resistance circuit.

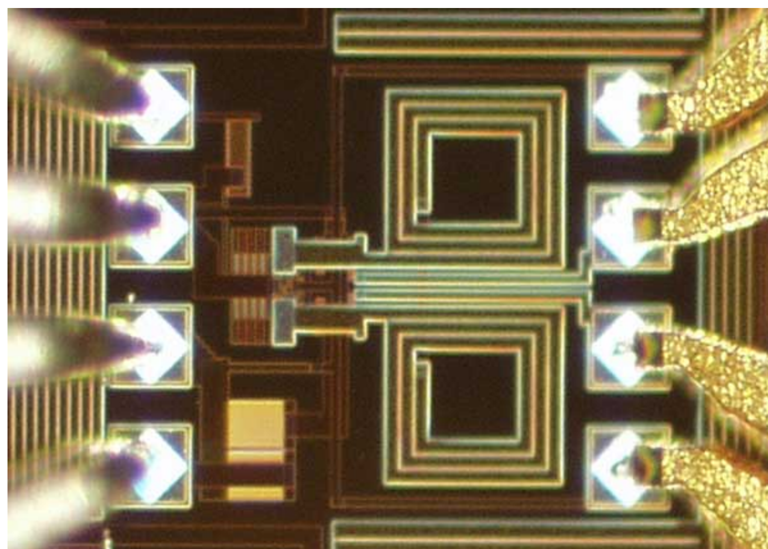


Figure 6.15: Fabricated CMOS VCO with probes in contact. The RF GSSG probe is at the right and the DC probe is at the left.

used to supply bias voltages as described in Section 5.4. Figure 6.15 shows the probes contacting an oscillator circuit. The current I_{BIAS} is supplied by a voltage source. In the case of the unbuffered oscillator, when this voltage is greater than 1 V, the current drawn by the VCO saturates (i.e. the tail current control transistor acts like a short circuit) and no longer increases with increasing voltage. Oscillator measurements were primarily made under this condition, since it represents the highest possible negative resistance inside the circuit and therefore the highest possible oscillation amplitude.

Although the output of the oscillator is differential, the measurements presented here were single-ended, with a $50\,\Omega$ precision load terminating one half of the differential port, while the other port was connected to the $50\,\Omega$ input of the spectrum analyzer. This differs from the one port measurement methods that utilized a hybrid coupler.

During the testing of the oscillators, a number of RF interference problems were encountered. The probe station and supporting vibration control table act as a low frequency antenna, picking up interference from the environment. Because the probe station is physically large, and the DC probe does not present a very good RF ground,

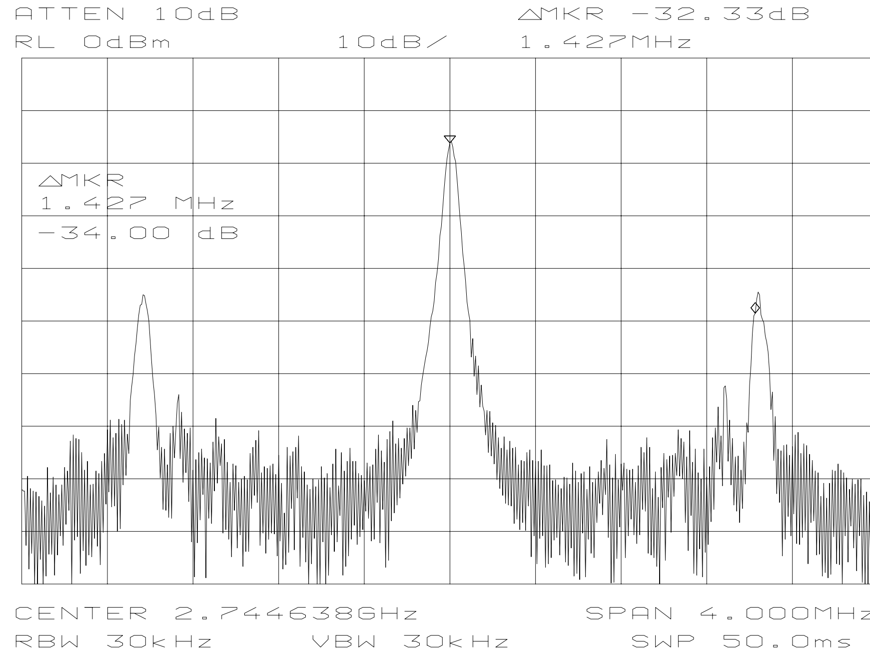


Figure 6.16: Sidebands created by local AM radio stations. The large sideband at 1.43MHz offset is caused by WKEX Blacksburg broadcasting at 1430 kHz.

it was not possible to avoid low frequency interference such as that from local AM radio stations. When RF signals are present on the bias lines of the VCO, particularly the I_{BIAS} terminal, they are mixed into the phase noise skirt of the oscillator. Figure 6.16 shows the sidebands created by a local AM radio station (WKEX 1430 kHz). It was also discovered that a nearby computer monitor was generating interference. Figure 6.17 shows 100 kHz sidebands that appeared when this monitor was operating. It was also found that much of this external interference feeds through the ground connections of the power supplies and other measurement equipment. To avoid these effects as much as possible, all phase noise measurements were ultimately performed while biasing the circuit with batteries (6.18). This is not uncommon for measurements on a free running oscillator[1]. Using batteries, a cleaner output spectrum was obtained (Fig. 6.19).

[1]The motive behind designing this oscillator was to create a vehicle for quantifying the noise effects on VCOs in an on chip environment. It was proposed in Chapter 1 that a VCO should be very sensitive to injected noise. Perhaps the author designed too much of a good thing.

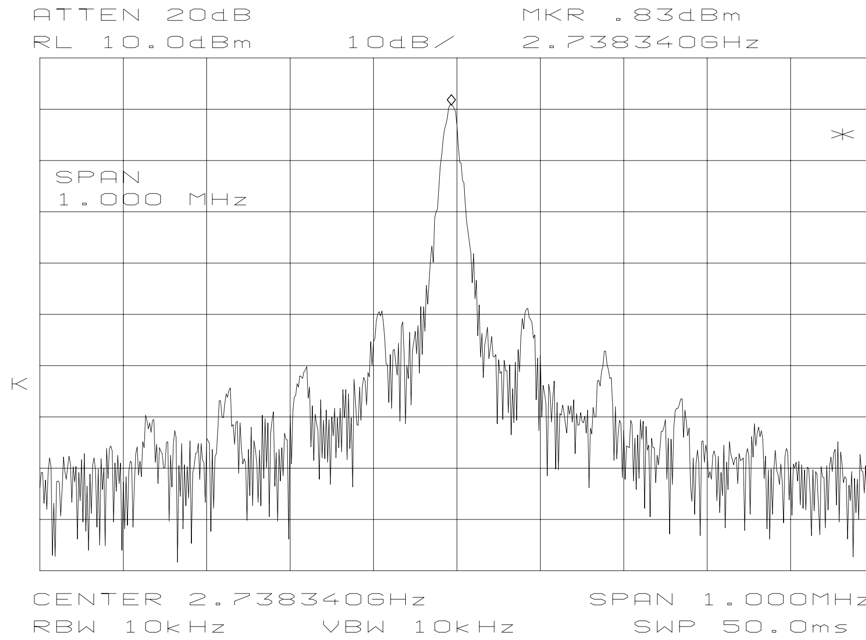


Figure 6.17: 100 kHz sidebands created by refresh rate of nearby computer monitor.

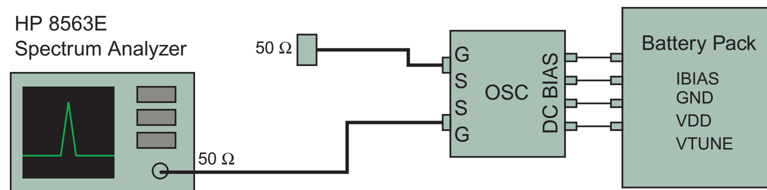


Figure 6.18: Single-ended oscillator measurement setup.

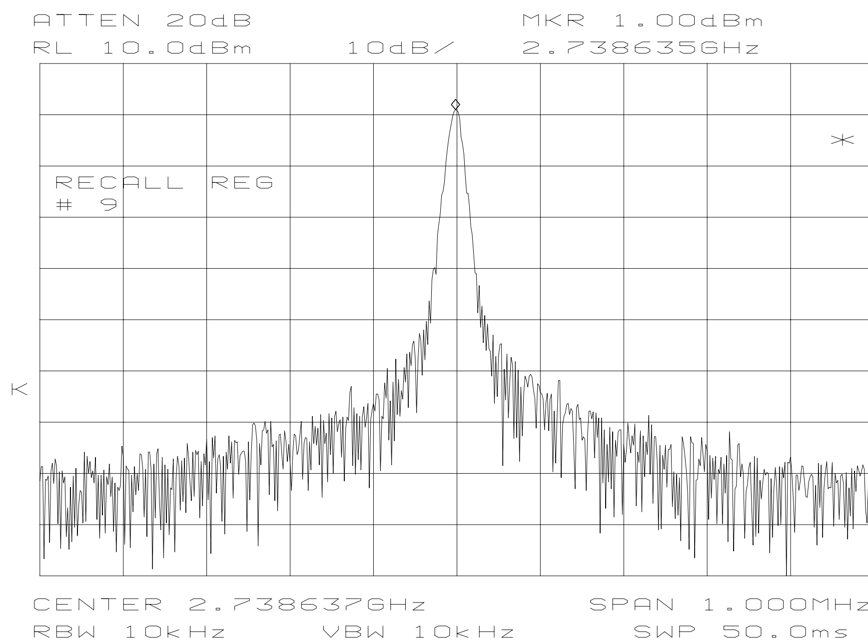


Figure 6.19: Output spectrum of VCO when biased with batteries

Recall from Section 5.2 that 3 different VCOs were fabricated. The "unbuffered" VCO (VCO #1) used series resistors to mitigate the effect of the 50 Ω measurement equipment on the loaded Q of the tank circuit. The "buffered" VCO (VCO #2) was identical except that active buffers (inverters) were used in place of the series resistors. Finally, a "retuned" VCO (VCO #3) was implemented using the same active buffering scheme, but with a varactor half the size of the varactors in the first 2 oscillators. In the following discussion these oscillators are referred to as VCO #1, VCO #2, and VCO #3.

The tuning curve of each VCO was measured by stepping the tuning voltage, V_{TUNE}, and measuring the resultant output frequency with the spectrum analyzer. These tuning curves were measured at the maximum tail bias current, 10 mA. Figures 6.20 and 6.21 show the tuning curves of VCO #1 and VCO #3 respectively. The tuning curves of VCO #2 and VCO #1 differ only slightly, since the buffers only add a very small parasitic capacitance to the tank circuit. For this reason only the tuning curve of VCO #1 is shown. All three VCO tuning curves display a linear

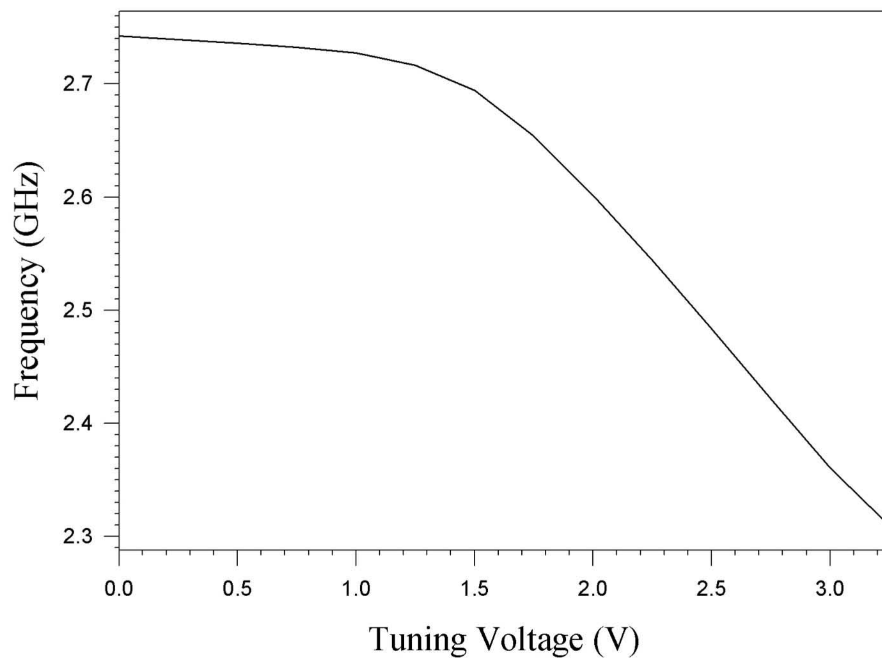


Figure 6.20: Measured unbuffered VCO (VCO #1) tuning curve.

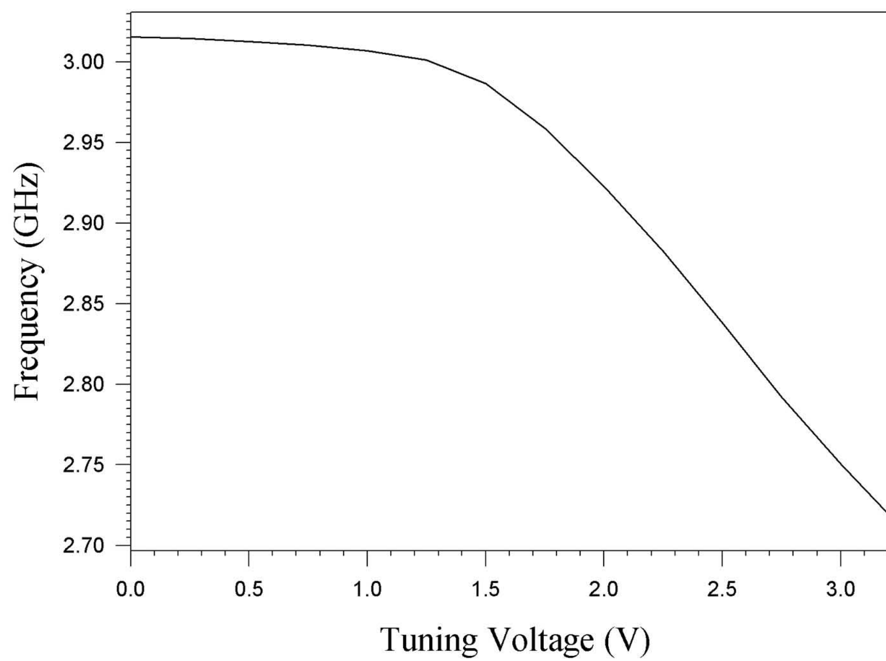


Figure 6.21: Measured retuned VCO (VCO #3) tuning curve.

tuning characteristic centered near 2.4 V. The tuning sensitivities of the VCOs are 235 MHz/V for VCO #1 and VCO #2, and 182 MHz/V for VCO #3. These tuning curves compare favorably with the simulated results (see Fig. 5.9). The tuning range of VCO #1 and VCO #2 is 17.1%; simulations predicted 23%. The tuning range is probably lower than predicted due to parasitic capacitances. The tuning range of VCO #3 is 10.6%. VCO #3 has a smaller tuning range since its varactor is smaller; therefore, the tunable portion of the tank capacitance is smaller, while the parasitic portion of the tank capacitance remains the same.

The phase noise was measured with an HP 8563E spectrum analyzer, with the HP 85671A phase noise add-on utility installed[2]. Some of these measurements are somewhat inaccurate due to the tendency of the oscillator to slowly drift in frequency. The manual for the 85671A phase noise utility states, *"A signal with a constant drift rate will have a repeatable, but incorrect, phase noise plot."*[53]. This occurs because the oscillator spectrum can shift in frequency between the measurement of the carrier power and the measurement of the noise power at a particular offset frequency. However, the oscillator does not drift significantly at some points on the tuning curve and the drift rate is slow enough so that trends may be observed. The oscillators tend to drift more at frequencies where the tuning gain is high. The measurement accuracy of the phase noise utility is $\pm 2.5\,dB$, and the repeatability is specified as $\pm 1.5\,dB$ for smoothed data. With this in mind, the reader is cautioned that more accurate phase noise measurements would require a more complicated measurement method. The measured data does however show some general trends.

Phase noise was measured at a range of points on the tuning curves, in an effort to find the optimal phase noise of the oscillators. The phase noise was measured 5 times at each operating point and the average is reported here. The lowest phase noise was achieved with VCO #2 at low tuning voltages (high frequencies). VCO #2 with

[2]Both are products of Hewlett Packard, Inc. now Agilent Technologies, Inc.

$V_{TUNE} = 0.5V$ (2.73 GHz) has an output phase noise of $-106.7\,dBc/Hz$ at $100\,kHz$ offset. The oscillator and buffers draw a total of 13.933 mA from a 3.3 V supply. From similar measurements on VCO #1 it is observed that the oscillator core is drawing 9mA of current at this operating point. Therefore the oscillator power consumption at this point is 29.7 mW. Using Equation 1.1 the figure of merit for this oscillator can be calculated to be -180.7 dBc/Hz, which is state-of-the-art compared with other published designs (Table 1.1). This is, however, the best-case measurement and the oscillator does not perform as well across the entire tuning range.

During the course of these measurements, it was noticed that VCO #1 has a much more stable output and does not drift as much as the other oscillators. VCOs #2 and #3 appear to be sensitive to any disturbance in the test setup. Touching the RF cables carrying the oscillator output away from the probes sometimes caused erratic frequency hops. The reasons for this are currently unclear but are presumed to be the result of a flawed buffer implementation. One possibility is that an imbalance in the switching point of the buffers causes some feedback that intermittently detunes the oscillator.

A log plot of the phase noise of VCO #1 is shown in Figure 6.22. The phase noise measurements on VCO #1 are considered more accurate than the other oscillators because it does not drift significantly during the measurement. The phase noise of VCO #1 versus tuning voltage is shown in Figure 6.23. This graph shows that the phase noise performance of the oscillator degrades where the *tuning sensitivity* ($\frac{df}{dv}$) is highest. A likely reason for this is that, at high tuning sensitivities, noise on the varactor control line is converted into frequency (and thus phase) variations in the oscillator output.

The single-ended output power of the VCOs was also measured (note: the loss of the measurement cables was not calibrated out of the measurements; power at the port of the VCO is estimated to be 1 dB higher). For VCO #2 and VCO #3, the output

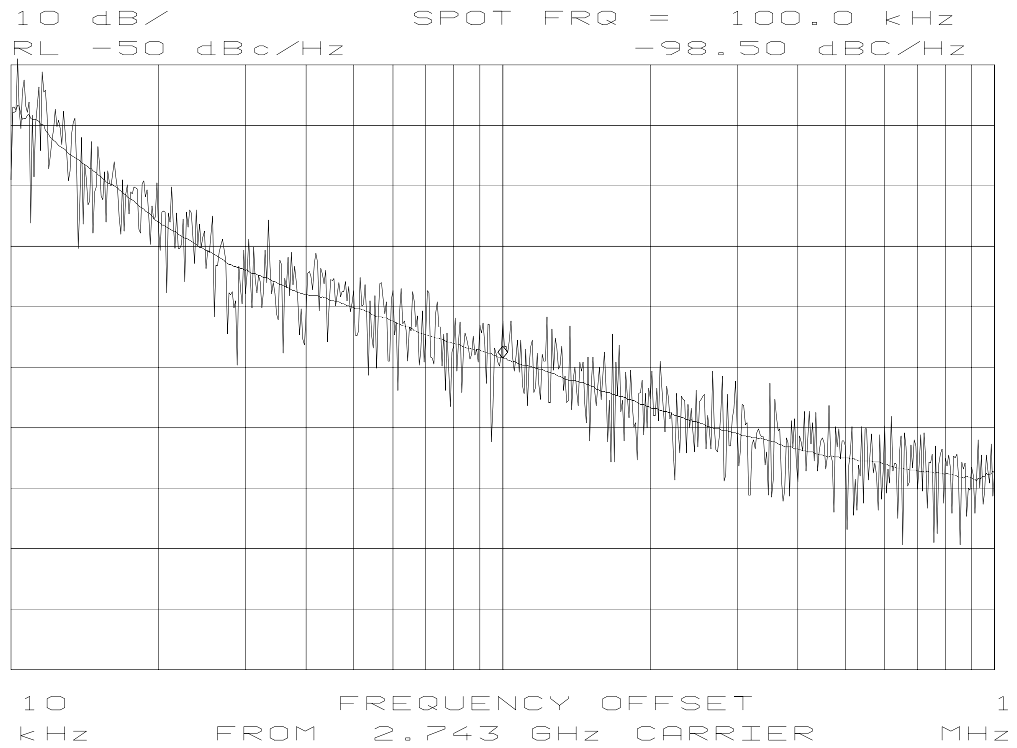


Figure 6.22: Unbuffered (VCO #1) VCO phase noise versus frequency. $V_{TUNE} = 0\,V$. $I_{BIAS} = 10\,mA$.

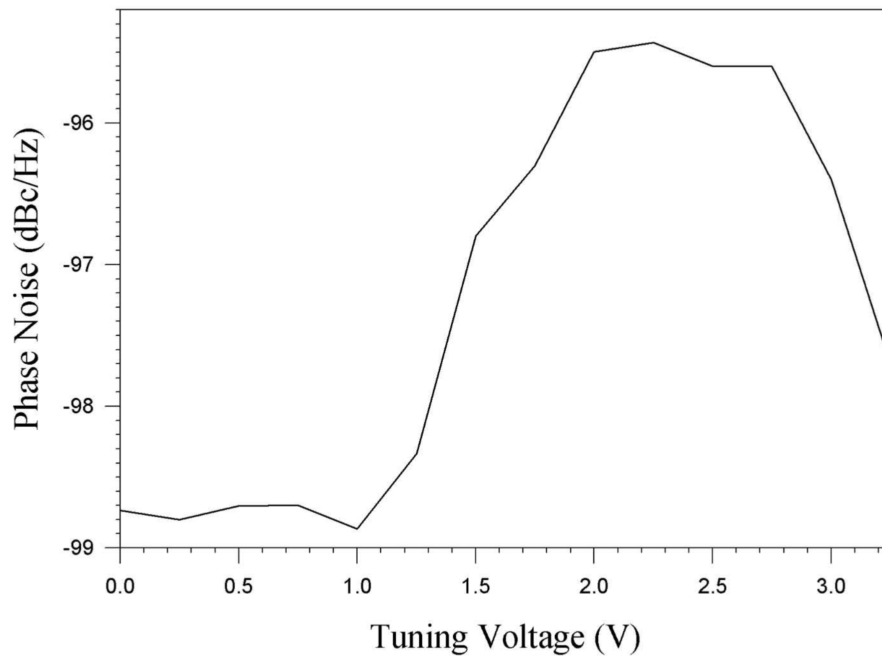


Figure 6.23: Measured phase noise versus tuning voltage for unbuffered (VCO #1) VCO.

power is near 0dBm and does not vary significantly over the tuning range since the limiting effect of the buffers tends to override any differences in the amplitudes of the oscillator waveforms. However, VCO #1 does show an interesting trend. Figure 6.24 shows the output power of VCO #1 versus tuning voltage. Notice that the output power is higher at higher output frequencies (lower tuning voltages). This most likely occurs because the Q of the inductor is higher at higher frequencies. In addition, the equivalent parallel resistance of the inductor will be higher at higher frequencies. Both these effects will cause the oscillation amplitude to be larger at higher frequencies.

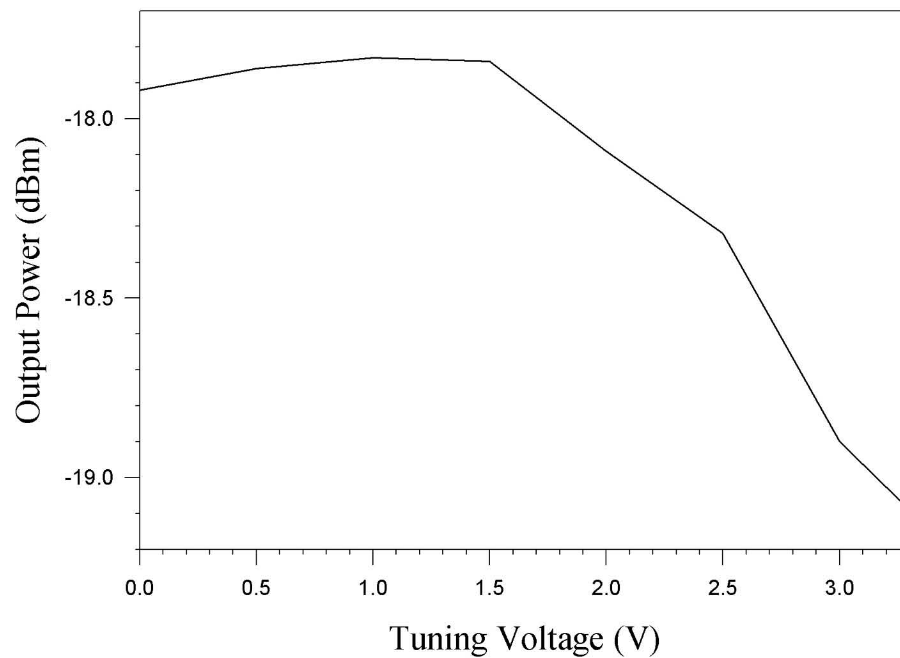


Figure 6.24: Measured single-ended output power of unbuffered (VCO #1) VCO versus tuning voltage.

Chapter 7

Conclusions and Future Work

This chapter concludes the research work presented in this thesis. The goal of this research was to create a vehicle that would be useful in quantifying the effects of mixed-signal and digital noise on an RF system. This is motivated by the desire to realize a wireless system-on-a-chip; in this case RF and digital components will have to coexist without excessive mutual interference. To this end an RF VCO was implemented in a digital CMOS process technology. Integrated into a PLL, this VCO could possibly serve as the local oscillator for wireless applications near 2.4-2.5 GHz, such as Bluetooth, 802.11 WLAN, or unlicensed ISM applications. In each of these applications, the low cost provided by a fully integrated CMOS solution is very attractive.

7.1 Conclusions

The lowest phase noise for the VCOs presented in this thesis was achieved with the buffered VCO; $-106.7\,dBc/Hz$ at $100kHz$ offset was achieved at an output frequency of 2.73 GHz. At this operating point the VCO core (not including the buffers) draws

9 mA from a 3.3 V supply (29.7 mW). The following figure-of-merit was presented in Section 1.2 as a means of comparing different VCOs:

$$VCO_{FOM} = \mathfrak{L}(f_{offset}) - 20\ \log\left(\frac{f_{osc}}{f_{offset}}\right) + 10\ \log\left(\frac{P_{diss}}{1\,mW}\right) \tag{7.1}$$

For the conditions above this becomes:

$$VCO_{FOM} = -106.7 - 20\ \log\left(\frac{2.73 \times 10^9}{100 \times 10^3}\right) + 10\ \log(29.7) = -180.7 \tag{7.2}$$

The low phase noise of this buffered oscillator may be overly optimistic, however, since the output frequency tends to drift during phase noise measurements. The phase noise utility on the spectrum analyzer attempts to track the frequency of the oscillator; however, depending on the direction of the frequency drift the measured phase noise will either be higher or lower than it actually is. The buffered oscillators had a tendency to drift more than the unbuffered oscillator. For this reason the author has more confidence in the phase noise measurements of the unbuffered oscillator. The best phase noise achieved by the unbuffered VCO was approximately $-98.9\,dBc/Hz$ at $100\,kHz$ offset with an output frequency of $2.7274\,GHz$. The current consumption is 9 mA. Using Equation 7.1:

$$VCO_{FOM} = -98.9 - 20\ \log\left(\frac{2.7274 \times 10^9}{100 \times 10^3}\right) + 10\ \log(29.7) = -172.9 \tag{7.3}$$

Revisiting Table 1.1 this work can be compared to other LC CMOS VCOs. Table 7.1 shows the best case phase noises from the buffered and unbuffered oscillators compared with recently reported CMOS LC VCOs. The result from the buffered version is excellent and only the work by Hajimiri et al demonstrates better performance [14]. The unbuffered oscillator has a FOM that is more average. Realistically, the performance that could be achieved by this oscillator design with a proper buffering scheme probably lies somewhere between these two results. It is worth noting that the phase noise performance of this CMOS VCO is already competitive with a commercial part, the MAX2750, implemented in a bipolar technology [54]. At the time of this writing the VCO in [54] is the only monolithic VCO in the 2.4 GHz frequency range that is commercially available.

Table 7.1: Comparison of this work and reported fully monolithic LC CMOS VCOs.

Reference	Tech. (μm)	f_o (GHz)	Phase Noise (dBc/Hz)	Tuning Range (MHz)	power (mW)	Voltage (V)	FOM (dBc/Hz)
Hajimiri[14]	0.25	1.8	-121 @ 600 kHz	?	6	1.5	-182.8
This work (buffered)	0.35	2.73	-106.7 @ 100 kHz	425	29.7	3.3	-180.7
Craninckx[2]	0.7	1.8	-116 @ 600kHz	250	6	1.5	-177.8
Vora [10]	0.6	2	-103 @ 100 kHz	?	22	?	-175.6
Park [15]	0.5	0.9	-110 @ 200 kHz	126	6.6	3.3	-174.9
Herzel [11]	0.25	1.9	-100 @ 100 kHz	250	15	2.5	-173.8
This work (unbuffered)	0.35	2.7274	-98.9 @ 100 kHz	433	29.7	3.3	-172.9
Andreani [12]	0.8	2.4	-118 @ 1 MHz	350	22.5	2.5	-172.1
Razavi [16]	0.6	1.8	-100 @ 500 kHz	120	7.59	3.3	-162.3
Wong[17]	0.35	2	-87 @ 100 kHz	?	22.5	3	-159.5
Lam [18]	0.35	2.6	-110 @ 5 MHz	320	13	2.5	-153.2

7.2 Future Work

During the course of this work a number of unresolved questions regarding design issues were raised. Addressing these concerns is a possible area for future work.

The most pressing issue with the VCO design is the more accurate measurement of its phase noise. Phase noise measurements on a free running oscillator are tricky because the carrier frequency can drift while the power at the desired offset is being measured. Since the entire oscillator spectrum drifts with the carrier this can lead to incorrect results. This presents a significant problem for the HP 85671A phase noise utility used for the measurements presented in this thesis. Accurate measurements of the phase noise of a free running VCO can be obtained by using a dedicated phase noise measurement system, such as the Agilent 3048A or the Aeroflex Comstron PN9000. However, these systems are prohibitively expensive; a more cost-effective approach might involve setting up a system to manually perform phase noise measurements in the same manner that these commercial instruments use. There are two well known methods for measuring the phase noise of a free running VCO that might be suitable here [55],[56].

The first method involves locking a clean reference oscillator to the output frequency of the free running VCO (Fig. 7.1). The two synchronized signals are then phase-detected and low-pass filtered. This filtered signal can then be measured using an audio frequency spectrum analyzer. If the loop bandwidth of the PLL is set lower than the desired phase noise offset then the phase noise can be measured. The phase noise at an offset f_m will be proportional to the output power at f_m measured by the audio frequency spectrum analyzer.

The second method involves dividing the signal into two equal signals, delaying one signal path, and phase detecting (Fig. 7.2). The delay line decorrelates the noise in the two halves of the signal such that the output noise at f_m is 3 dB higher than

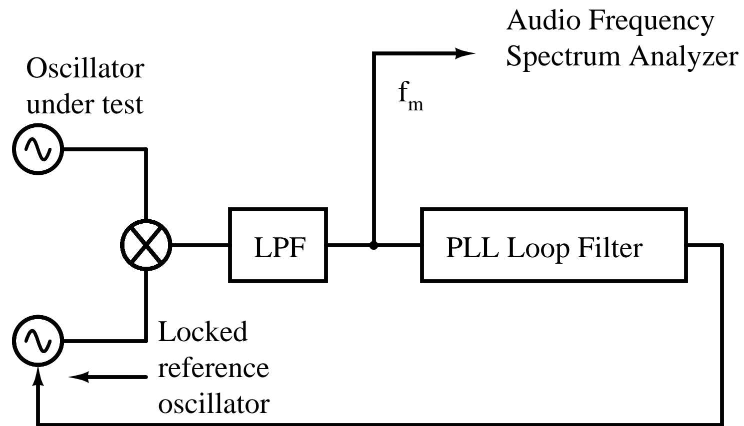


Figure 7.1: Phase noise measurement using the PLL method.

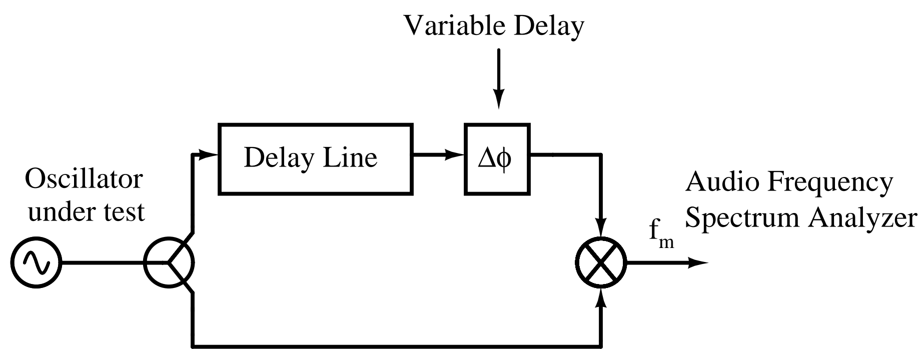


Figure 7.2: Phase noise measurement using the delay line method.

the actual phase noise. A long delay is required to measure low frequency offsets. A long length (300 m) of coaxial cable could be used, but its loss would have to be compensated using an amplifier. If this is unsuitable, a fiber optic delay line might be used [57].

Both these phase noise measurement methods would require significant calibration. These methods should yield much more reliable results since they both address the signal tracking problem.

The accuracy of the phase noise measurement on the unbuffered VCO might also be improved if an LNA is inserted between the measurement equipment and the oscillator output. The low signal level of the unbuffered VCO ($\approx -18\,dBm$) may lead to errors due to the dynamic range limitation of the phase noise utility.

Finally, there are a number of design suggestions that should be considered in any future revisions of this oscillator design:

- The problem of measuring the phase noise of the free running VCO is significant and is not likely to be resolved if a dedicated phase noise measurement system is not available. An alternative solution involves integrating the VCO into a wideband PLL on-chip. The VCO could be locked to a low frequency (10-100 MHz) source with a wide loop bandwidth such that the phase noise of the VCO would be dominant. The only significant design challenge would be designing an appropriate frequency divider.

- The phase noise of the VCO would likely be improved if the tail current control device had been PMOS rather than NMOS. This is because PMOS devices have lower 1/f noise than NMOS devices.

- As was mentioned in the measurements chapter, the output frequency tends to drift in the buffered oscillators; the design of these buffers should therefore be carefully scrutinized. A simple source-follower might have been just as adequate

without creating frequency stability problems.

- The current mirroring between the IBIAS input device and the tail current control transistors does not work well because the device gate length was chosen too small. Although this is not a serious concern since the current can still be controlled, an accurate current mirror would have been helpful during measurements.

- RF interference coupled into the test setup was a significant problem, especially the upconversion of WKEX, AM 1430, and the refresh signals of nearby computer monitors. In a realistic environment these interference sources would not be as problematic since a packaged part would not likely see the large metal structures that the microprobed die was exposed to in the lab. Four of the VCO test chips from the fabrication run were packaged into small MLF-20 packages (only the unbuffered oscillator was wirebonded) with the intent of mounting them on a small test board for phase noise measurements, but this has not yet been completed.

- Some on-chip bias and power supply decoupling should be considered to clean up the power supply and bias lines. Simple capacitor connected NMOS transistors could be used.

- Both the passive elements, the inductor and the varactor, could be the subject of extensive optimization. The varactor might be more accurately simulated using a device simulator such as Medici. Similarly a full 3D EM simulation of the inductor might yield more insight than the 2D simulations provided by Sonnet EM. Furthermore, the inductor used in this work was a simple single-layer spiral. A multi-layer spiral composed of two metalization layers "strapped together" with vias might lower the series resistance of the inductor.

- For the purposes of measuring the passive test structures with a 1-port cali-

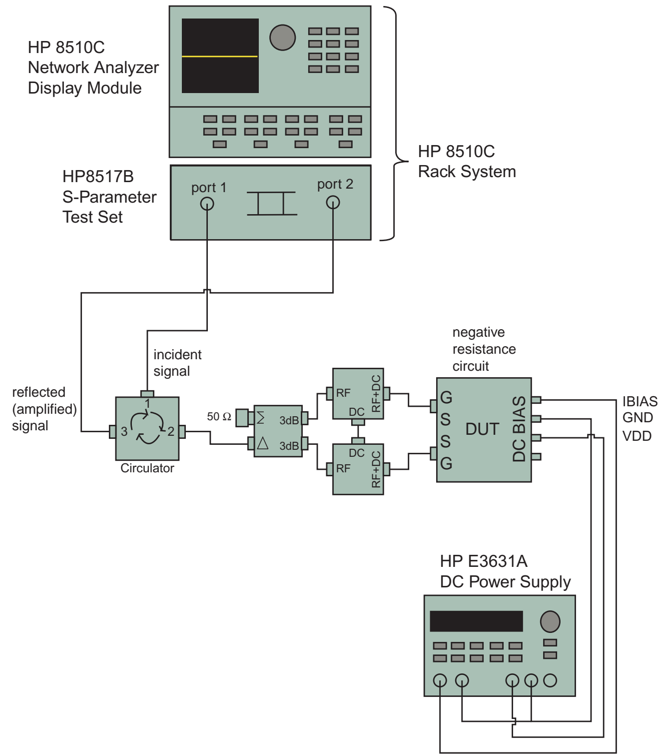


Figure 7.3: RF negative resistance measurement using a circulator.

bration, the necessary test structures (open, short, and load) could be designed directly onto the fabricated test chip. The value of the load resistance could then be measured at DC and used as the characteristic impedance for 1-port measurements.

- The RF negative resistance could be measured using a circulator as shown in Figure 7.3. In this configuration the device is connected as a negative resistance amplifier. The negative resistance could be de-embedded from the measured value of S_{21}.

- The extraction of the device parasitics should be examined in more detail. The extraction deck that was used was written for the 2P3M TSMC process and the author attempted to modify it for the 1P4M process. However, the results seriously overestimated the device parasitic capacitances. The lack of a good

design flow from schematics through layout hampered the quality of this work.

The suggestions above should improve the performance of the VCO designed in this work. The ultimate goal of this research is to characterize the effects of mixed-signal digital noise on the performance of RF VCOs. In that respect there is much work left to be done. Hopefully the work presented here provides a unique look at CMOS LC oscillator design, as well as providing a test vehicle to facilitate that future research.

Appendix A

Derivation of Negative Resistance of Cross Coupled FETs

A.1 Low Frequency Model

This section describes how two cross coupled FETs yield a negative resistance ($-\frac{2}{G_M}$). Figure A.1 below shows two cross coupled NMOS FETs and a small signal low frequency equivalent circuit:

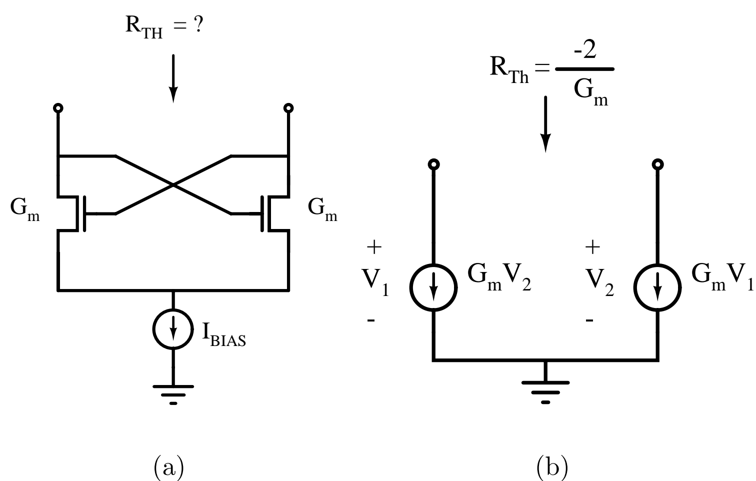


Figure A.1: Cross coupled NFETs and DC equivalent circuit.

The parasitic capacitances and other second order effects are ignored here for sim-

plicity. For convenience we redraw this circuit in Figure A.2:

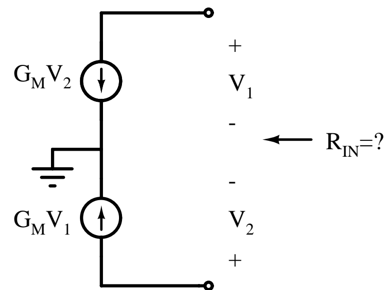


Figure A.2: Redrawn circuit

Recall from circuit theory that the Thévenin input resistance of a circuit can be calculated by applying a test source. Figure A.3 shows this circuit with a test voltage source V_{TEST} applied:

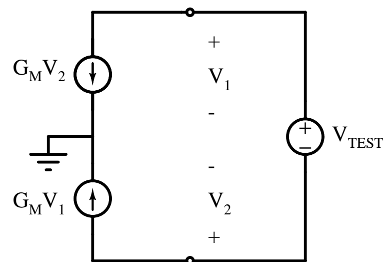


Figure A.3: Test Source

To facilitate the calculation it is helpful to break up V_{TEST} into two sources, each with a voltage equal to $\frac{V_{TEST}}{2}$:

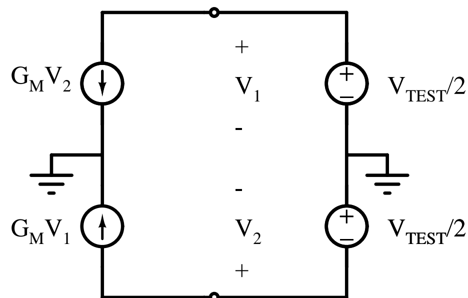


Figure A.4:

Now the input resistance seen by V_{TEST} can be calculated as:

$$R_{TH} = \frac{V_{TEST}}{G_M V_2}$$

By inspection it can be seen that:

$$V_2 = -\frac{V_{TEST}}{2}$$

Therefore:

$$R_{TH} = \frac{V_{TEST}}{G_M \left(-\frac{V_{TEST}}{2}\right)} = -\frac{2}{G_M}$$

A.2 High Frequency Model

Adding the gate parasitics (R_g and C_{gs}) of the MOS devices to figure A.4 only makes the development slightly more complicated. Figure A.5 shows the equivalent circuit with the gate resistance, R_g, and the gate to source capacitance, C_{gs}, included:

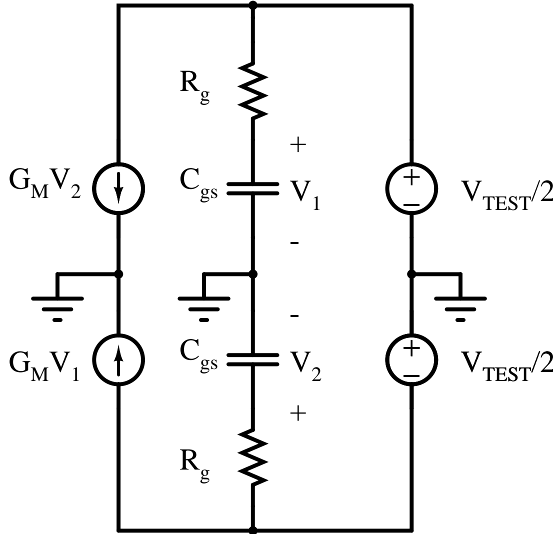


Figure A.5:

The input impedance of this structure can be calculated in the frequency domain in

a similar manner as was done for the low frequency case:

$$Z_{TH} = \frac{V_{TEST}}{I_{TEST}}$$

By KCL:

$$I_{TEST} = G_M V_2 + \frac{\frac{V_{TEST}}{2}}{R_g + \frac{1}{j\omega C_{gs}}}$$

Replacing C_{gs} with its complex impedance, V_2 can be calculated:

$$V_2 = -\frac{V_{TEST}}{2}\left(\frac{\frac{1}{j\omega C_{gs}}}{R_g + \frac{1}{j\omega C_{gs}}}\right)$$

Therefore:

$$I_{TEST} = (G_M) \cdot \left(-\frac{V_{TEST}}{2}\right) \cdot \left(\frac{\frac{1}{j\omega C_{gs}}}{R_g + \frac{1}{j\omega C_{gs}}}\right) + \frac{\frac{V_{TEST}}{2}}{R_g + \frac{1}{j\omega C_{gs}}}$$

Simplifying:

$$I_{TEST} = \left(\frac{V_{TEST}}{2}\right) \cdot \left(\frac{1}{R_g + \frac{1}{j\omega C_{gs}}}\right) \cdot \left(1 - \frac{G_M}{j\omega C_{gs}}\right)$$

Now it is straightforward to find Z_{IN}

$$Z_{TH} = \frac{1}{\left(\frac{1}{2}\right) \cdot \left(\frac{1}{R_g + \frac{1}{j\omega C_{gs}}}\right) \cdot \left(1 - \frac{G_M}{j\omega C_{gs}}\right)}$$

simplified:

$$Z_{TH} = 2\left(\frac{1 + R_g C_{gs} j\omega}{C_{gs} j\omega - G_M}\right)$$

Clearly if $C_{gs} = 0$ then $Z_{TH} = -\frac{2}{G_M}$. If $R_g = 0$ then the negative resistance, $-\frac{2}{G_M}$, appears in parallel with a capacitor equal to $\frac{C_{gs}}{2}$:

$$Z_{TH} = -\frac{2}{G_M} \| \frac{1}{\frac{C_{gs}}{2} j\omega}.$$

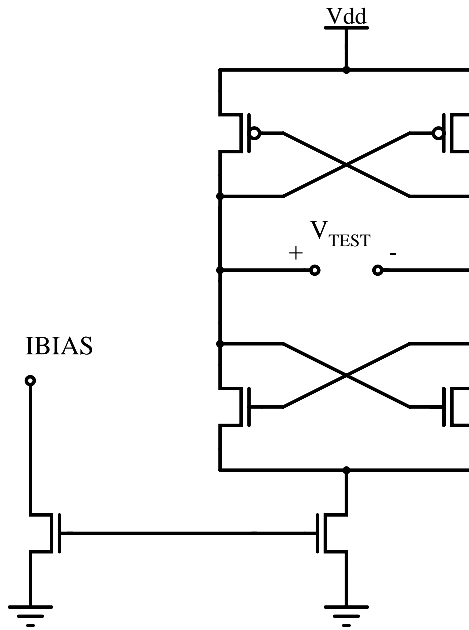
Appendix B

Solution of Nonlinear Differential Oscillator Equation

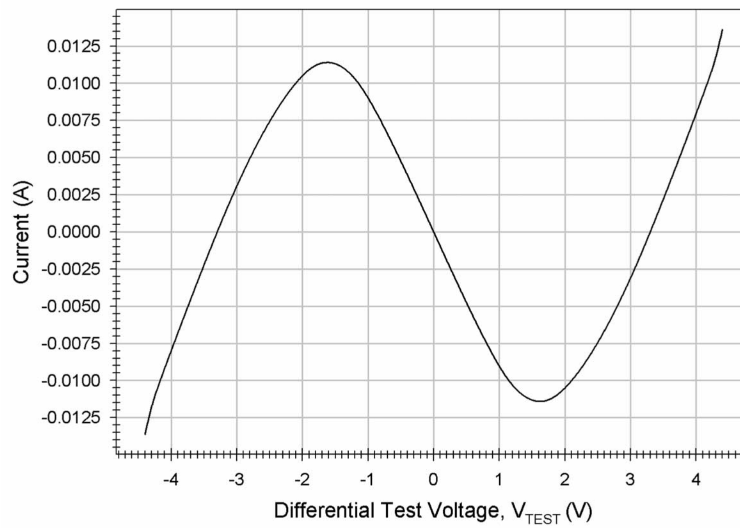
In this appendix the output voltage amplitude of the complementary $-G_M$ oscillator is calculated as a function of the tank circuit parallel resistance, R (In this appendix all references to R refer to a parallel RLC circuit). Recall from Chapter 2 that the nonlinear I-V characteristic of the active circuit can be extracted by replacing the tank circuit with a DC source and plotting the current through this test source as a function of its voltage. The test circuit and resulting I-V curve are shown in Figure B.1. Mathematica [22] was then used to find a least-squares curve fit to this nonlinearity. The odd symmetry of the curve indicates that only odd-order terms are necessary. The following polynomial was obtained using 8 odd order terms:

$$\begin{aligned} f(v) &= -0.00959646\,v + 0.000115714\,v^3 + 0.000589498\,v^5 \\ &\quad - 0.000131705\,v^7 + 0.0000140351\,v^9 - 8.07038\times 10^{-7}\,v^{11} \\ &\quad + 2.39369\times 10^{-8}\,v^{13} - 2.86388\times 10^{-10}\,v^{15}. \end{aligned} \quad \text{(B.1)}$$

An RLC circuit shunted by the nonlinearity $i = f(v)$ was used to model the complementary $-G_M$ oscillator (Fig. B.2). This circuit has a response that is determined



(a) Test circuit for measuring $i = f(v)$.



(b) Nonlinear Resistance I-V characteristic, $i = f(v)$.

Figure B.1: Test circuit and extracted I-V curve.

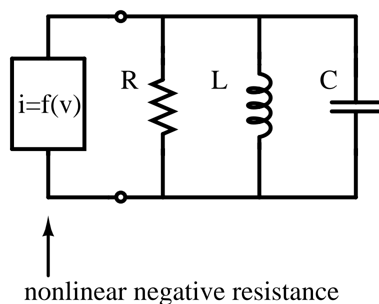


Figure B.2: RLC model of $-G_M$ oscillator.

by solving the following differential equation:

$$LC\frac{d^2v}{dt^2} + \frac{L}{R}\frac{dv}{dt} + L\frac{d}{dt}f(v) + v = 0 \tag{B.2}$$

The solution to equation B.2 is assumed to be sinusoidal to simplify this calculation:

$$v(t) = A\,Sin(\omega t). \tag{B.3}$$

This assumption is justified since even in low Q LC oscillators the harmonics are typically well out of the passband of the resonator. In addition, low oscillation amplitudes will force this circuit to operate on the nearly linear portion of the I-V curve. Even in a high Q oscillator the output voltage will be nearly sinusoidal because of the filtering effect of the tank circuit, although the current waveform into the nonlinear element may become very distorted.

Substituting Equation B.3 into B.2 and truncating the higher order harmonics allows the differential equation to be solved (This is harmonic balance with a single tone). The result of this substitution (using Mathematica) is:

$$\begin{aligned}
&A\,\cos(\omega t) - L\,C\,A\,\omega^2\,\cos(\omega t) + 0.00959646\,L\,A\,\omega\,\sin(\omega t)\\
&- 0.0000867858\,L\,A^3\,\omega\,\sin(\omega t) - 0.000368436\,L\,A^5\,\omega\,\sin(\omega t)\\
&+ 0.0000720264\,L\,A^7\,\omega\,\sin(\omega t) - 6.9079\times10^{-6}\,L\,A^9\,\omega\,\sin(\omega t)\\
&+ 3.64113\times10^{-7}\,L\,A^{11}\,\omega\,\sin(\omega t) - 1.00283\times10^{-8}\,L\,A^{13}\,\omega\,\sin(\omega t)\\
&+ 1.12482\times10^{-10}\,L\,A^{15}\,\omega\,\sin(\omega t) - \frac{L\,A\,\omega\,\sin(\omega t)}{R}\\
&+ \text{Higher Order Terms} = 0
\end{aligned} \tag{B.4}$$

Now since the sine and cosine functions are orthogonal we can solve for their coefficients independently. Solving the coefficients of the cosine terms yields:

$$\begin{aligned} A - A\,L\,C\,\omega^2 &= 0 \\ \omega &= \frac{1}{\sqrt{LC}}. \end{aligned} \tag{B.5}$$

This is the well known resonant frequency of an LC circuit. Solving the sine coefficients yields:

$$\begin{aligned} &0.00959646\,L\,A\,\omega - 0.0000867858\,L\,A^3\,\omega - 0.000368436\,L\,A^5\,\omega \\ &+ 0.0000720264\,L\,A^7\,\omega - 6.9079 \times 10^{-6}\,L\,A^9\,\omega + 3.64113 \times 10^{-7}\,L\,A^{11}\,\omega \\ &- 1.00283 \times 10^{-8}\,L\,A^{13}\,\omega + 1.12482 \times 10^{-10}\,L\,A^{15}\,\omega - \frac{L\,A\,\omega}{R} = 0 \end{aligned} \tag{B.6}$$

Further simplification yields:

$$\begin{aligned} &0.00959646 - 0.0000867858\,A^2 - 0.000368436\,A^4 \\ &+ 0.0000720264\,A^6 - 6.9079 \times 10^{-6}\,A^8 + 3.64113 \times 10^{-7}\,A^{10} \\ &- 1.00283 \times 10^{-8}\,A^{12} + 1.12482 \times 10^{-10}\,A^{14} = \frac{1}{R} \end{aligned} \tag{B.7}$$

This expression gives insight into the operation of the oscillator by relating the peak (differential) oscillation amplitude A to the equivalent parallel resistance of the tank circuit. Equation B.7 can be considered a simple energy balance. The resistance of the tank circuit, R, during steady state oscillation, will be equal to the large signal average negative resistance of the active circuit. This negative resistance represents the power delivered by the active circuit as the sinusoidal waveform sweeps through the nonlinearity, $i = f(v)$. While equation B.7 could be solved numerically, it is more useful to plot R as a function of A and evaluate it graphically as shown in figure B.3. This allows the designer to quickly see how the amplitude and parallel resistance of the tank circuit are related.

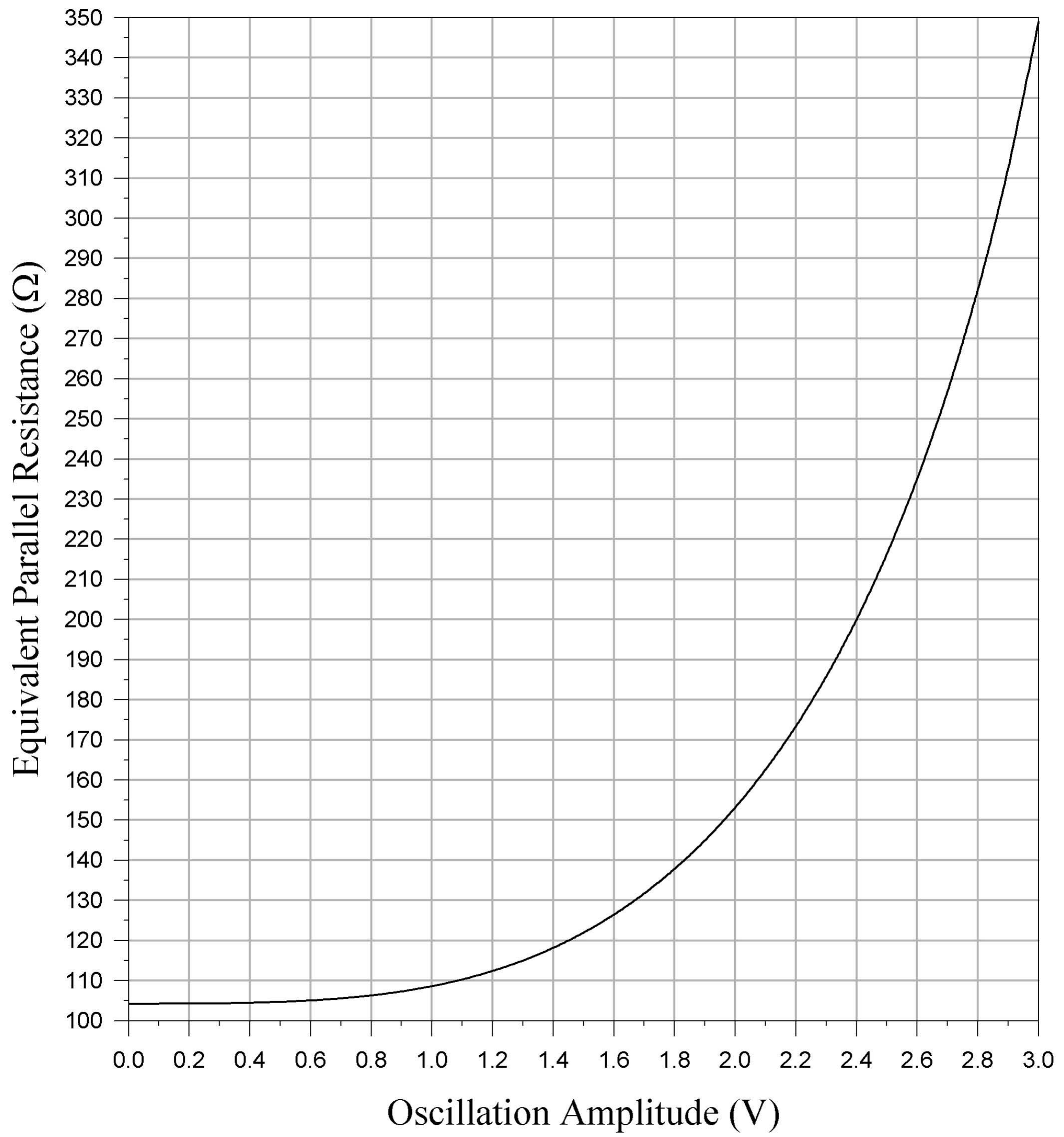


Figure B.3: Equivalent parallel resistance versus oscillation amplitude.

Appendix C

TSMC 0.35 μm 1P4M Device Parameters Extracted by MOSIS

C.1 January 2000 MOSIS Parameters

The following data was extracted by MOSIS for their January 10, 2000 run of the TSMC 0.35 μm process[1] [58]. These are the parameters and the BSIM3v3 device models that were used during the design of the oscillators.

```
                         MOSIS PARAMETRIC TEST RESULTS

        RUN: N9CQ (1P4M)                                      VENDOR: TSMC
   TECHNOLOGY: SCN035                                FEATURE SIZE: 0.35 microns


INTRODUCTION: This report contains the lot average results obtained by MOSIS
              from measurements of MOSIS test structures on each wafer of
              this fabrication lot. SPICE parameters obtained from similar
              measurements on a selected wafer are also attached.

COMMENTS: TSMC 0352P4M.


TRANSISTOR PARAMETERS     W/L       N-CHANNEL P-CHANNEL  UNITS
```

[1] The data in this appendix (as well as data for any other past MOSIS run) is available from: `http://www.mosis.org/Technical/Testdata/menu-testdata.html`

MINIMUM	0.6/0.4			
Vth		0.58	-0.81	volts
SHORT	20.0/0.4			
Idss		492	-223	uA/um
Vth		0.62	-0.80	volts
Vpt		9.2	-9.8	volts
WIDE	20.0/0.4			
Ids0		0.4	-0.2	pA/um
LARGE	50.0/50.0			
Vth		0.55	-0.77	volts
Vjbkd		8.2	-8.8	volts
Ijlk		-36.7	-3.7	pA
Gamma		0.62	0.35	V^0.5
K' (Uo*Cox/2)		68.9	-29.6	uA/V^2

COMMENTS: Poly bias varies with design technology. To account for mask and etch bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology		XL
SCN3M_SUBM (lambda=0.20)		-0.02
	thick oxide	-0.06
TSMC35		0.03
	thick oxide	0.04
SCN3M (lambda=0.25)		-0.12
	thick oxide	-0.06

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	MTL1	MTL2	MTL3	UNITS
Sheet Resistance	3.5	2.7	5.9		0.07	0.07	0.07	ohms/sq
Width Variation (measured - drawn)	-0.00	0.09	0.03		0.16	-0.02	-0.01	microns
Contact Resistance	4.5	4.0	4.7			1.02	1.43	ohms
Gate Oxide Thickness	76							angstrom

PROCESS PARAMETERS	MTL4	N\PLY	N_WELL	UNITS
Sheet Resistance	0.04	1080	1023	ohms/sq
Width Variation (measured - drawn)	0.17			microns
Contact Resistance	1.78			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	MTL1	MTL2	MTL3	MTL4	N_WELL	UNITS
Area (substrate)	1068	1393	111		30	15	7	11	59	aF/um^2
Area (N+active)			4591		39	18	12	10		aF/um^2
Area (P+active)			4584							aF/um^2
Area (poly)					57	16	9	7		aF/um^2
Area (poly2)					144					aF/um^2
Area (metal1)						36	14	8		aF/um^2
Area (metal2)							35	13		aF/um^2
Area (metal3)								33		aF/um^2
Fringe (substrate)	400	435			48	44	51	15		aF/um
Fringe (poly)					72	39	29	24		aF/um
Fringe (metal1)						61	36	27		aF/um
Fringe (metal2)							59	36		aF/um

```
 Fringe (metal3)                                                    55         aF/um
 Overlap (N+active)                    295                                     aF/um
 Overlap (P+active)                    277                                     aF/um

CIRCUIT PARAMETERS                           UNITS
 Inverters                    K
  Vinv                       1.0       1.24  volts
  Vinv                       1.5       1.37  volts
  Vol (100 uA)               2.0       0.16  volts
  Voh (100 uA)               2.0       3.01  volts
  Vinv                       2.0       1.47  volts
  Gain                       2.0     -18.76
 Ring Oscillator Freq.
  DIV256 (31-stg,3.3V)               200.30  MHz
 Ring Oscillator Power
  DIV256 (31-stg,3.3V)                 0.14  uW/MHz/gate

COMMENTS: SUBMICRON
```

```
 N9CQ SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Mar 14/00
* LOT: n9cq                  WAF: 10
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                                LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 7.6E-9
+XJ      = 1E-7           NCH     = 2.3579E17      VTH0    = 0.5027514
+K1      = 0.5359893      K2      = 0.0258172      K3      = 24.6606744
+K3B     = 1.4055348      W0      = 5.355464E-6    NLX     = 2.404522E-9
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = -0.120252      DVT1    = 3.084588E-3    DVT2    = 0.470688
+U0      = 417.429294     UA      = -1.40534E-13   UB      = 1.355832E-18
+UC      = 2.939828E-11   VSAT    = 1.208882E5     A0      = 0.9319916
+AGS     = 0.1686015      B0      = 1.288356E-6    B1      = 5E-6
+KETA    = 0.0105706      A1      = 0              A2      = 1
+RDSW    = 1.103044E3     PRWG    = 1.750872E-3    PRWB    = -0.0916512
+WR      = 1              WINT    = 6.910593E-8    LINT    = 1.993462E-8
+XL      = -2E-8          XW      = 0              DWG     = 1.047524E-9
+DWB     = 1.084571E-8    VOFF    = -0.0906265     NFACTOR = 0.6164962
+CIT     = 0              CDSC    = 5.145568E-6    CDSCD   = 0
+CDSCB   = 0              ETA0    = 4.63499E-3     ETAB    = -9.189583E-4
+DSUB    = 0.1150044      PCLM    = 0.7703416      PDIBLC1 = 0.3438859
+PDIBLC2 = 8.526878E-3    PDIBLCB = 0.0845601      DROUT   = 0.6859339
+PSCBE1  = 7.23225E9      PSCBE2  = 5.005586E-10   PVAG    = 0.4108257
+DELTA   = 0.01           MOBMOD  = 1              PRT     = 0
+UTE     = -1.5           KT1     = -0.11          KT1L    = 0
+KT2     = 0.022          UA1     = 4.31E-9        UB1     = -7.61E-18
+UC1     = -5.6E-11       AT      = 3.3E4          WL      = 0
+WLN     = 1              WW      = -1.22182E-15   WWN     = 1.1837
+WWL     = 0              LL      = 0              LLN     = 1
+LW      = 0              LWN     = 1              LWL     = 0
+CAPMOD  = 2              XPART   = 0.4            CGDO    = 2.95E-10
+CGSO    = 2.95E-10       CGBO    = 1E-11          CJ      = 1.08158E-3
+PB      = 0.7719669      MJ      = 0.3252096      CJSW    = 3.480034E-10
+PBSW    = 0.99           MJSW    = 0.1576976      PVTH0   = -0.0122678
+PRDSW   = -93.3365259    PK2     = -3.470912E-3   WKETA   = -3.503848E-3
+LKETA   = -0.0105386      )
*
.MODEL CMOSP PMOS (                                LEVEL   = 49
```

```
+VERSION = 3.1            TNOM     = 27             TOX      = 7.6E-9
+XJ      = 1E-7           NCH      = 8.52E16        VTH0     = -0.6821549
+K1      = 0.4197546      K2       = -6.11453E-3    K3       = 35.791795
+K3B     = -2.796173      W0       = 1.990794E-6    NLX      = 4.309814E-7
+DVT0W   = 0              DVT1W    = 0              DVT2W    = 0
+DVT0    = 1.134781       DVT1     = 0.3272645      DVT2     = -1.051562E-3
+U0      = 141.3184274    UA       = 1.024889E-10   UB       = 1.354611E-18
+UC      = -3.30244E-11   VSAT     = 1.6171E5       A0       = 0.6693235
+AGS     = 0.2959248      B0       = 2.86196E-6     B1       = 5E-6
+KETA    = -6.382387E-3   A1       = 0              A2       = 1
+RDSW    = 3.44286E3      PRWG     = -0.0626736     PRWB     = 0.0981315
+WR      = 1              WINT     = 5.340142E-8    LINT     = 1.410986E-9
+XL      = -2E-8          XW       = 0              DWG      = -4.209302E-9
+DWB     = 1.12145E-8     VOFF     = -0.1154702     NFACTOR = 2
+CIT     = 0              CDSC     = 0              CDSCD    = 0
+CDSCB   = 4.724734E-5    ETA0     = 0.0115959      ETAB     = 2.08259E-4
+DSUB    = 0.2766226      PCLM     = 7.8965744      PDIBLC1 = 1.97648E-3
+PDIBLC2 = 8.825766E-3    PDIBLCB = 2.37472E-3     DROUT    = 0.4321935
+PSCBE1  = 3.010835E10    PSCBE2   = 7.998967E-10   PVAG     = 15
+DELTA   = 0.01           MOBMOD   = 1              PRT      = 0
+UTE     = -1.5           KT1      = -0.11          KT1L     = 0
+KT2     = 0.022          UA1      = 4.31E-9        UB1      = -7.61E-18
+UC1     = -5.6E-11       AT       = 3.3E4          WL       = 0
+WLN     = 1              WW       = -5.22182E-16   WWN      = 1.195
+WWL     = 0              LL       = 0              LLN      = 1
+LW      = 0              LWN      = 1              LWL      = 0
+CAPMOD  = 2              XPART    = 0.4            CGDO     = 2.77E-10
+CGSO    = 2.77E-10       CGBO     = 1E-11          CJ       = 1.417679E-3
+PB      = 0.99           MJ       = 0.5636812      CJSW     = 4.292884E-10
+PBSW    = 0.99           MJSW     = 0.3497357      PVTH0    = 0.0116448
+PRDSW   = -58.3059685    PK2      = 1.654991E-3    WKETA    = -6.310553E-4
+LKETA   = 1.189744E-3     )
*
```

C.2 August 2000 MOSIS parameters

The following data was extracted by MOSIS for their August 14, 2000 run of the TSMC 0.35 μm process. This is run on which the test chip of this thesis was fabricated.

```
                         MOSIS PARAMETRIC TEST RESULTS

          RUN: T08S (1P4M)                                   VENDOR: TSMC
   TECHNOLOGY: SCN035                                  FEATURE SIZE: 0.35 microns


INTRODUCTION: This report contains the lot average results obtained by MOSIS
              from measurements of MOSIS test structures on each wafer of
              this fabrication lot. SPICE parameters obtained from similar
              measurements on a selected wafer are also attached.
```

COMMENTS: TSMC 035

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.6/0.4			
Vth		0.59	-0.77	volts
SHORT	20.0/0.4			
Idss		474	-230	uA/um
Vth		0.63	-0.76	volts
Vpt		9.5	-9.6	volts
WIDE	20.0/0.4			
Ids0		0.2	-0.2	pA/um
LARGE	50.0/50.0			
Vth		0.55	-0.76	volts
Vjbkd		8.4	-8.8	volts
Ijlk		-21.8	-2.0	pA
Gamma		0.63	0.35	V^0.5
K' (Uo*Cox/2)		90.2	-33.0	uA/V^2
Low-field Mobility		423.17	154.82	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask and etch bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology		XL
SCN4M_SUBM (lambda=0.20)		-0.02
	thick oxide	-0.06
TSMC35		0.03
	thick oxide	0.04
SCN4M (lambda=0.25)		-0.12
	thick oxide	-0.06

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	MTL1	MTL2	MTL3	UNITS
Sheet Resistance	3.4	2.6	6.3		0.07	0.08	0.07	ohms/sq
Width Variation (measured - drawn)	0.06	0.12	0.07		0.09	-0.07	-0.09	microns
Contact Resistance	4.7	4.1	4.7			1.40	1.29	ohms
Gate Oxide Thickness	81							angstrom

PROCESS PARAMETERS	MTL4	N+BLK	N\PLY	N_WELL	UNITS
Sheet Resistance	0.03	88.9	1075	1018	ohms/sq
Width Variation (measured - drawn)	0.28				microns
Contact Resistance	1.44				ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	MTL1	MTL2	MTL3	MTL4	N_WELL	UNITS
Area (substrate)	1016	1352	108	29	13	6	10	60	aF/um^2
Area (N+active)			4429	38	17	12	10		aF/um^2

```
 Area (P+active)                      4440                                   aF/um^2
 Area (poly)                                 53   16    9    7          aF/um^2
 Area (metal1)                                    32   14    9          aF/um^2
 Area (metal2)                                         38   14          aF/um^2
 Area (metal3)                                              37          aF/um^2
 Fringe (substrate)     315     416          36   37   44   11          aF/um
 Fringe (poly)                               69   38   29   25          aF/um
 Fringe (metal1)                                  57   35   27          aF/um
 Fringe (metal2)                                       58   37          aF/um
 Fringe (metal3)                                            58          aF/um
 Overlap (N+active)                    274                              aF/um
 Overlap (P+active)                    311                              aF/um
```

```
CIRCUIT PARAMETERS                              UNITS
 Inverters                      K
  Vinv                        1.0       1.28  volts
  Vinv                        1.5       1.40  volts
  Vol (100 uA)                2.0       0.26  volts
  Voh (100 uA)                2.0       2.87  volts
  Vinv                        2.0       1.50  volts
  Gain                        2.0     -19.98
 Ring Oscillator Freq.
  DIV256 (31-stg,3.3V)                184.02  MHz
 Ring Oscillator Power
  DIV256 (31-stg,3.3V)                  0.14  uW/MHz/gate

COMMENTS: SUBMICRON
```

```
 T08S SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Nov 13/00
* LOT: T08S                  WAF: 103
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                                LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 8.1E-9
+XJ      = 1E-7           NCH     = 2.2E17         VTH0    = 0.5169068
+K1      = 0.5551284      K2      = 0.0247147      K3      = 1E-3
+K3B     = 5.7031543      W0      = 5E-5           NLX     = 2.226795E-7
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 2.9823324      DVT1    = 0.8849715      DVT2    = -0.2059247
+U0      = 421.5071635    UA      = -4.90693E-13   UB      = 1.418415E-18
+UC      = 3.065945E-11   VSAT    = 1.662044E5     A0      = 1.2159231
+AGS     = 0.1478168      B0      = 5.92974E-7     B1      = 5E-6
+KETA    = 9.900943E-3    A1      = 0              A2      = 0.4174418
+RDSW    = 825.2124432    PRWG    = 0.0124291      PRWB    = -0.0912541
+WR      = 1              WINT    = 9.131257E-8    LINT    = 1.501905E-8
+XL      = -2E-8          XW      = 0              DWG     = -2.663403E-9
+DWB     = 9.799988E-9    VOFF    = -0.0777288     NFACTOR = 1.2505668
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 0.029673       ETAB    = 2.902442E-6
+DSUB    = 0.3184477      PCLM    = 1.3055529      PDIBLC1 = 0.9407465
+PDIBLC2 = 6.620126E-3    PDIBLCB = 0.1            DROUT   = 1
+PSCBE1  = 7.209753E9     PSCBE2  = 5E-10          PVAG    = 0
+DELTA   = 0.01           RSH     = 3.4            MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
```

```
+WL      = 0             WLN     = 1             WW      = -1.22182E-15
+WWN     = 1.1907        WWL     = 0             LL      = 0
+LLN     = 1             LW      = 0             LWN     = 1
+LWL     = 0             CAPMOD  = 2             XPART   = 0.4
+CGDO    = 2.74E-10      CGSO    = 2.74E-10      CGBO    = 1E-12
+CJ      = 1.023782E-3   PB      = 0.7868484     MJ      = 0.3237206
+CJSW    = 3.019021E-10  PBSW    = 0.99          MJSW    = 0.1347617
+CF      = 0             PVTH0   = -0.0191777    PRDSW   = -85.4483848
+PK2     = 6.530421E-4   WKETA   = -6.682303E-3  LKETA   = -9.721488E-3   )
*
.MODEL CMOSP PMOS (                              LEVEL   = 49
+VERSION = 3.1           TNOM    = 27            TOX     = 8.1E-9
+XJ      = 1E-7          NCH     = 8.52E16       VTH0    = -0.6992912
+K1      = 0.4396488     K2      = -0.0181007    K3      = 44.6318077
+K3B     = -5            W0      = 4.019537E-6   NLX     = 1.974877E-7
+DVT0W   = 0             DVT1W   = 0             DVT2W   = 0
+DVT0    = 1.4812718     DVT1    = 0.5133197     DVT2    = -6.692767E-3
+U0      = 151.5559517   UA      = 1E-10         UB      = 1.702681E-18
+UC      = -3.19487E-11  VSAT    = 2E5           A0      = 0.8082448
+AGS     = 0.3032618     B0      = 2.432768E-6   B1      = 5E-6
+KETA    = -4.138844E-3  A1      = 8.401321E-4   A2      = 0.5337971
+RDSW    = 2.68101E3     PRWG    = -0.0600015    PRWB    = 5.205337E-3
+WR      = 1             WINT    = 8.058704E-8   LINT    = -3.125706E-9
+XL      = -2E-8         XW      = 0             DWG     = -9.298651E-9
+DWB     = 1.10411E-8    VOFF    = -0.1075986    NFACTOR = 1.989503
+CIT     = 0             CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0             ETA0    = 0.0560929     ETAB    = 4.307915E-3
+DSUB    = 0.4782723     PCLM    = 6.2373142     PDIBLC1 = 9.665571E-3
+PDIBLC2 = 2.242382E-3   PDIBLCB = 7.103885E-3   DROUT   = 0.0919911
+PSCBE1  = 2.446742E10   PSCBE2  = 6.500325E-10  PVAG    = 15
+DELTA   = 0.01          RSH     = 2.6           MOBMOD  = 1
+PRT     = 0             UTE     = -1.5          KT1     = -0.11
+KT1L    = 0             KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0             WLN     = 1             WW      = -5.22182E-16
+WWN     = 1.215         WWL     = 0             LL      = 0
+LLN     = 1             LW      = 0             LWN     = 1
+LWL     = 0             CAPMOD  = 2             XPART   = 0.4
+CGDO    = 3.11E-10      CGSO    = 3.11E-10      CGBO    = 1E-12
+CJ      = 1.36545E-3    PB      = 0.99          MJ      = 0.5667335
+CJSW    = 4.015042E-10  PBSW    = 0.99          MJSW    = 0.3468404
+CF      = 0             PVTH0   = 0.0099919     PRDSW   = -71.4646976
+PK2     = 8.455564E-4   WKETA   = -2.342639E-4  LKETA   = -3.593741E-3   )
*
```

REFERENCES

[1] Troels Emil Kolding, "Review of RF CMOS Performance and Future Process Innovations," Technical Report R98-1014, Aalborg University, RFIC Integrated Systems & Circuits (RISC) group, Aalborg, Denmark, Oct. 1998, ISSN 0908-1224.

[2] Jan Craninckx and Michiel S. J. Steyaert, "A 1.8-GHz Low-Phase-Noise CMOS VCO Using Optimized Hollow Spiral Inductors," *IEEE Journal of Solid State Circuits*, vol. 32, no. 5, pp. 736–744, May 1997.

[3] Thomas H. Lee, "CMOS RF: No Longer an Oxymoron," in *IEEE GaAs Integrated Circuit Symposium Digest*, 1997, pp. 244–247.

[4] Tajinder Manku, "Microwave CMOS - Devices and Circuits," in *Proceedings of the IEEE Custom Integrated Circuits Conference*, 1998, pp. 59–66.

[5] Lawrence E. Larson, "Integrated Circuit Technology Options for RFIC's—Present Status and Future Directions," *IEEE Journal of Solid State Circuits*, vol. 33, no. 3, pp. 387–399, March 1998.

[6] David Johns and Ken Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, Inc., New York, 1997.

[7] J. Craninckx and M. Steyaert, *Wireless CMOS Frequency Synthesizer Design*, Kluwer Academic Publishers, Norwell, MA, 1998.

[8] D. B. Leeson, "A Simple Model of Feedback Oscillator Noise Spectrum," *Proceedings of the IEEE*, vol. 54, pp. 329–330, feb 1966.

[9] Thomas H. Lee and Ali Hajimiri, *The Design of Low Noise Oscillators*, Kluwer Academic Publishers, Norwell, MA, 1999.

[10] Sameer Vora and Lawrence E. Larson, "Noise Power Optimization of Monolithic CMOS VCOs," in *IEEE Radio Frequency Integrated Circuits Symposium Digest*, 1999, pp. 167–170.

[11] Frank Herzel, Michael Pierschel, Peter Weger, and Marc Tiebout, "Phase Noise in a Differential CMOS Voltage-Controlled Oscillator for RF Applications," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 47, no. 1, pp. 11–15, Jan. 2000.

[12] Pietro Andreani and Sven Mattisson, "A 2.4-GHz CMOS Monolithic VCO with an MOS Varactor," *Analog Integrated Circuits and Signal Processing*, vol. 22, no. 1, pp. 17–24, Jan. 2000.

[13] Pietro Andreani, "A Comparison between Two 1.8GHz CMOS VCOs Tuned by Different Varactors," in *Proc. 22nd Eur. Solid-State Cir. Conf. (ESSCIRC)*, 1998, pp. 380–383.

[14] Ali Hajimiri and Thomas H. Lee, "Design Issues in CMOS Differential LC Oscillators," *IEEE Journal of Solid State Circuits*, vol. 34, no. 5, pp. 717–724, May 1999.

[15] Byeong-Ha Park and Phillip E. Allen, "Low-Power, Low-Phase-Noise CMOS Voltage-Controlled-Oscillator with Integrated LC Resonator," in *IEEE International Symposium on Circuits and Systems Proceedings*, 1998, vol. 4, pp. 421–424.

[16] Behzad Razavi, "A 1.8GHz CMOS Voltage-Controlled Oscillator," in *IEEE International Solid State Circuits Conference Digest*, 1997, pp. 388–389.

[17] Wallace Ming Yip Wong, Ping Shing Hui, Zhiheng Chen, Keqiang Shen, Jack Lau, Philip C. H. Chan, and Ping-Keung Ko, "A Wide Tuning Range Gated Varactor," *IEEE Journal of Solid State Circuits*, vol. 35, no. 5, pp. 773–779, May 2000.

[18] Christopher Lam and Behzad Razavi, "A 2.6GHz/5.2GHz CMOS Voltage-Controlled Oscillator," in *IEEE International Solid State Circuits Conference Digest*, 1999, pp. 402–403.

[19] P. G. M. Baltus, A. G. Wagemans, R. Dekker, A. Hoogstraate, H. Maas, A. Tombeur, and J. van Sinderen, "A 3.5mW 2.5GHz Diversity Receiver and a 1.2mW 3.6GHz VCO in Silicon-On-Anything," *IEEE Journal of Solid State Circuits*, vol. 33, no. 12, pp. 2074–2080, Dec. 1998.

[20] Irving M. Gottlieb, *Understanding Oscillators*, Howard W. Sams, Indianapolis, IN, 1971.

[21] Cadence Design Systems, Inc., Sunnyvale, CA, *Spectre 4.4.3*, 1998.

[22] Wolfram Research, Inc., Champaign, IL, *Mathematica 4.02*, 1999.

[23] University of California, Berkeley, Berkeley, CA, *BSim3v3*, 1999, `http://www-device.eecs.berkeley.edu/~bsim3/`.

[24] Yuan Taur and Tak H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, New York, NY, 1998.

[25] Ali Hajimiri and Thomas H. Lee, "A General Theory of Phase Noise in Electrical Oscillators," *IEEE Journal of Solid State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.

[26] Konstantin A. Kouznetsov and Robert G. Meyer, "Phase Noise in LC Oscillators," *IEEE Journal of Solid State Circuits*, vol. 35, no. 8, pp. 1244–1248, Aug. 2000.

[27] C.-M. Hung and Kenneth K. O, "A Packaged 1.1-GHz CMOS VCO with Phase Noise of -126 dBc/Hz at a 600-kHz Offset," *Journal of Solid State Circuits*, vol. 35, no. 1, pp. 100–103, jan 2000.

[28] Joachim N. Burghartz, Daniel C. Edelstein, Keith A. Jenkins, and Young H. Kwark, "Spiral Inductors and Transmission Lines in Silicon Technology Using Copper-Damascene Interconnects and Low-Loss Substrates," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 10, pp. 1961–1968, oct 1997.

[29] Joachim N. Burghartz, D.C. Edelstein, Mehmet Soyuer, H. A. Ainspan, and Keith A. Jenkins, "RF Circuit Design Aspects of Spiral Inductors on Silicon," *IEEE Journal of Solid State Circuits*, vol. 33, no. 12, pp. 2028–2034, dec 1998.

[30] Rainer Götzfried, Frank Beisswanger, and Stephan Gerlach, "Design of RF Integrated Circuits Using SiGe Bipolar Technology," *IEEE Journal of Solid State Circuits*, vol. 33, no. 9, pp. 1417–1422, sept 1998.

[31] Yorgos K. Koutsoyannopoulos and Yannis Papananos, "Systematic Analysis and Modeling of Integrated Inductors and Transformers in RF IC Design," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 47, no. 8, pp. 699–713, Aug 2000.

[32] Paolo Arcioni, Rinaldo Castello, Luca Perregrini, Enrico Sacchi, and Francesco Svelto, "An Innovative Modelization of Loss Mechanism in Silicon Integrated Inductors," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 46, no. 12, pp. 1453–1460, Dec. 1999.

[33] Sunderarajan S. Mohan, Maria del Mar Hershenson, Stephen P. Boyd, and Thomas H. Lee, "Simple Accurate Expressions for Planar Spiral Inductances," *IEEE Journal of Solid State Circuits*, vol. 34, no. 10, pp. 1419–1424, Oct 1999.

[34] Joachim N. Burghartz, Mehment Soyuer, and Keith A. Jenkins, "Microwave Inductors and Capacitors in Standard Multilevel Interconnect Silicon Technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 44, no. 1, pp. 100–104, Jan. 1996.

[35] J. Y.-C. Chang, Asad A. Abidi, and Michael Gaitan, "Large Suspended Inductors on Silicon and Their Use in a 2-μm CMOS RF Amplifier," *IEEE Electron Device Letters*, vol. 14, no. 5, pp. 246–248, May 1993.

[36] William B. Kuhn, "Approximate Analytical Modeling of Current Crowding Effects in Multi-Turn Spiral Inductors," in *IEEE Radio Frequency Integrated Circuits Symposium Digest*, 2000, pp. 271–274.

[37] R. B. Andersen, T. Jørgensen, S. Laursen, and T. E. Kolding, "EM-Simulation of Planar Inductor Performance for Epitaxial Silicon Processes," in *Proceedings of the 18th NORCHIP Conference*, Nov. 2000, pp. 96–101.

[38] Ali M. Niknejad, *ASITIC: Analysis and Simulation of Spiral Inductors and Transformers for ICs*, University of California, Berkeley, `http://formosa.eecs.berkeley.edu/~niknejad/asitic.html`, 2000.

[39] Sonnet USA, Inc., Liverpool, NY, *Sonnet em Suite*, 1999.

[40] Agilent Technologies, Inc., Palo Alto, CA, *Agilent HFSS Designer*, 2000.

[41] Boris Troyanovsky, Norman Chang, and Dick Dowell, "Integration of Transient S-Parameter Simulation into HPSpice," Tech. Rep. HPL-95-61, Hewlett Packard Labs, May 1995.

[42] Paolo Arcioni, Rinaldo Castello, Luca Perregrini, and Enrico Sacchi, "Modeling of Metal and Substrate Losses in CMOS and BiCMOS Inductors for RFICs," *Microwave Journal*, vol. 42, pp. 62–74, Aug. 1999.

[43] James D. Plummer, Michael D. Deal, and Peter B. Griffin, *Silicon VLSI Technology*, Prentice Hall, Upper Saddle River, NJ, 2000.

[44] Allan R. Hambley, *Electronics: a top down approach to computer-aided circuit design*, Macmillan Publishing Company, New York, 1994.

[45] Pietro Andreani and Sven Mattisson, "On the Use of MOS Varactors in RF VCO's," *IEEE Journal of Solid State Circuits*, vol. 35, no. 6, pp. 905–910, June 2000.

[46] Chih-Ming Hung, Yo-Chuol Ho, I-Chang Wu, and Kenneth O, "High-Q Capacitors Implemented in a CMOS Process for Low-Power Wireless Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 5, pp. 505–511, May 1998.

[47] Taiwan Semiconductor Manufacturing Company Ltd., *TSMC 0.35UM LOGIC SILICIDE 3.3V/5V DESIGN RULE*, June 1999.

[48] Leo O. Chua, *Introduction to nonlinear network theory*, McGraw-Hill, New York, 1969.

[49] Donhee Ham and Ali Hajimiri, "Design and Optimization of A Low Noise 2.4GHz CMOS VCO With Integrated LC Tank and MOSCAP Tuning," in *IEEE International Symposium on Circuits and Systems Proceedings*, May 2000, pp. I–331–I–334.

[50] Maria del Mar Hershenson, Ali Hajimiri, Sunderarajan S. Mohan, Stephen P. Boyd, and Thomas H. Lee, "Design and optimization of LC oscillators," in *IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers*, 1999, pp. 65–69.

[51] Cadence Design Systems, Inc., Sunnyvale, CA, *Cadence Analog Design Environment*, 1998.

[52] Cadence Design Systems, Inc., Sunnyvale, CA, *Virtuoso Layout Editor 4.4.3*, 1998.

[53] Hewlett-Packard Company, Santa Rosa, CA, *User's Guide: HP 85671A Phase Noise Utility*, 1994.

[54] Maxim Integrated Products, Inc., Sunnyvale, CA, *MAX2750 Data Sheet: 2.4GHz Monolithic Voltage-Controlled Oscillators*, Oct. 2000.

[55] Wenzel Associates, Inc., Austin, Texas, *Techniques for Measuring Phase Noise*, `http://www.wenzel.com/documents/measuringphasenoise.htm`.

[56] Aeroflex Incorporated, Plainview, New York, *APPLICATION NOTE #1: Phase Noise Theory and Measurement*, March 1995.

[57] Lucent Technologies Inc. now Agere Systems, Allentown, PA, *Data Sheet: 5000-Series Fiber-Optic Delay Line*, Aug. 2000.

[58] Information Sciences Institute, University of Southern California, Marina del Rey, CA, *MOSIS*, `http://www.mosis.org/`.

VITA

Ryan Lee Bunch was born on May 25, 1977 in Suffolk Virginia, the peanut capital of the world. He grew up on the very rural southern edge of Suffolk, just a few miles from the Virginia/Carolina state line. After graduating from Lakeland High School his interest in electronics led him to Virginia Tech to study electrical engineering. He received his Bachelor of Science, Magna Cum Laude, in May, 1999.

During the Summers of 1998 and 1999 Ryan was employed as an analog circuit designer by IBM in Raleigh, NC. There he participated in the development of an Ethernet transceiver and a 2.5 Gb/s serial link. In August, 1999 Ryan returned to Virginia Tech to pursue graduate studies in Electrical Engineering.

Ryan will have completed the requirements for the degree of Master of Science in Electrical Engineering in April, 2001. After graduation, he will join RF Micro Devices in Greensboro, NC as a Design Engineer.