Investigation of High-Input-Voltage Non-Isolated Voltage Regulator Modules Topology Candidates

By

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(ABSTRACT)

Since the early 80s, the computer industry has undergone great expansion. Processors are becoming faster and more powerful. Power management issues in computing systems are becoming more complex and challenging. An evolution began when the high-performance Pentium processor was driven by a non-standard, less-than-5V power supply, instead of drawing its power from the 5V plane on the system board. A so-called Voltage Regulator Module (VRM), is put close to the processor in order to provide the power as quickly as possible. Nowadays, for desktop and workstation applications, VRM input voltage has moved to the 12V output of the silver box. In the meantime, microprocessors will run at very low voltage (below 1V), will consume up to 100A of current, and will have dynamics of about 400A/us.

This work presents an investigation of three 12V VRM topologies: the synchronous buck converter, the tapped-inductor buck converter and the active-clamp couple-buck converter. The limitations of today's synchronous buck approach are identified. The extreme duty cycle of the current topology makes it difficult to design an efficient VRM with decent transient response

The tapped-inductor buck and the active-clamp couple-buck converters are discussed as solutions. The transient response and efficiency of each type of converter are compared. Ripple cancellation is also addressed. The analytical and experimental results are presented: The tapped-inductor buck can improve the efficiency, but suffers a voltage spike, which nullifies its candidacy; the active-clamp couple-buck converter can improve the efficiency while maintaining good transient response, and it is therefore a good candidate for 12V VRMs.

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Chapter 1.

Introduction

The purpose of this work is to develop 12V-input, high-current voltage regulator modules for future generations of microprocessors.

1.1. Background

Since the early 80s, computer industry has experienced rapid expansion. Processors are becoming faster and more powerful. Accordingly, their power consumption has increased dramatically. An evolution began when the high-performance Pentium processor was driven by a non-standard, less-than-5V power supply, instead of drawing its power from the 5V plane on the system board. In order to provide the power as quick as possible, a so-called Voltage Regulator Module (VRM), was put close to the processor. In the past, VRMs basically drew power from the 5V output of the silver box. Nowadays, for desktop and workstation applications, VRM input voltage has moved to the 12V output of the silver box. And for server applications, the 48V VRM is emerging as a standard practice.

VRM design faces a great challenge in terms of keeping pace with the fast development of processors. Fig. 2.1 shows the Intel roadmap of voltage and current of the CPU load for VRMs. Future microprocessors will run at very low voltage (below 1V), will consume up to 100A of current, and will have fast dynamics of about 400A/us [1][2][3].

Today's 12V VRMs use the multi-phase interleaving synchronous buck converter [4][5][6][7][8][9][10]. Due to the very low output voltage, the buck converter has a very small duty cycle, which could even be smaller than 0.1 in the future. This extreme duty cycle makes it difficult to design an efficient converter with decent transient response. Also, the extreme duty cycle introduces some obstacles in current sensing and control, especially as the switching frequency increases in the future.

This work addresses these issues, focusing especially on the investigation of alternative topologies for 12V VRMs.

1.2. Thesis Outline

In Chapter 2, the state-of-the-art conventional VRM — the multi-phase interleaving synchronous buck converter — will be discussed. The critical inductance concept will be introduced as a guideline for the trade-off between efficiency and transient response. Penalties resulting from the extreme duty cycle will be identified. Experimental results will be presented. This topology will be used as a benchmark for the comparison of alternative topologies.

In Chapter 3, an improved topology — the tapped-inductor buck — will be presented. Critical inductance analysis of the tapped-inductor buck indicates that with a properly designed turns ratio, transient response does not suffer, and meanwhile higher efficiency can be achieved due to the extended duty cycle. Experimental results will be provided. Dynamic issues of the tapped-inductor buck will also be addressed. However, a detrimental voltage spike shows up in this topology thus its use is contraindicated.

In Chapter 4, the active-clamp couple-buck converter will be introduced. This topology solves the voltage spike issue of the tapped-inductor buck topology. Critical inductance analysis shows that with a properly designed turns ratio, the transient response is not impaired. On the other hand, the extended duty cycle improves efficiency, as verified by experimental results. The dynamic performance of the active-clamp couple-buck converter will also be addressed.

Chapter 2.

High-Input-Voltage Non-Isolated VRM

— The Multi-Phase Interleaving Buck VRM

In the area of low-voltage high-current applications with highly dynamic loads, such as voltage regulator modules (VRMs) for microprocessors, the synchronous buck converter is widely used. As the power demand for microprocessors increases steadily, the VRMs are required to work at a higher input voltage (12V). Meanwhile, the future generation of microprocessors will require a logic voltage lower than 1V and a significantly increased current, as shown in Fig. 2.1 [1][2][3]. This higher current load, together with the increase in slew rate, will cause a significant voltage deviation during the transient response. Power management issues in computing systems are becoming more complex and challenging. Tab.2.1 shows the specifications for present and future VRMs.

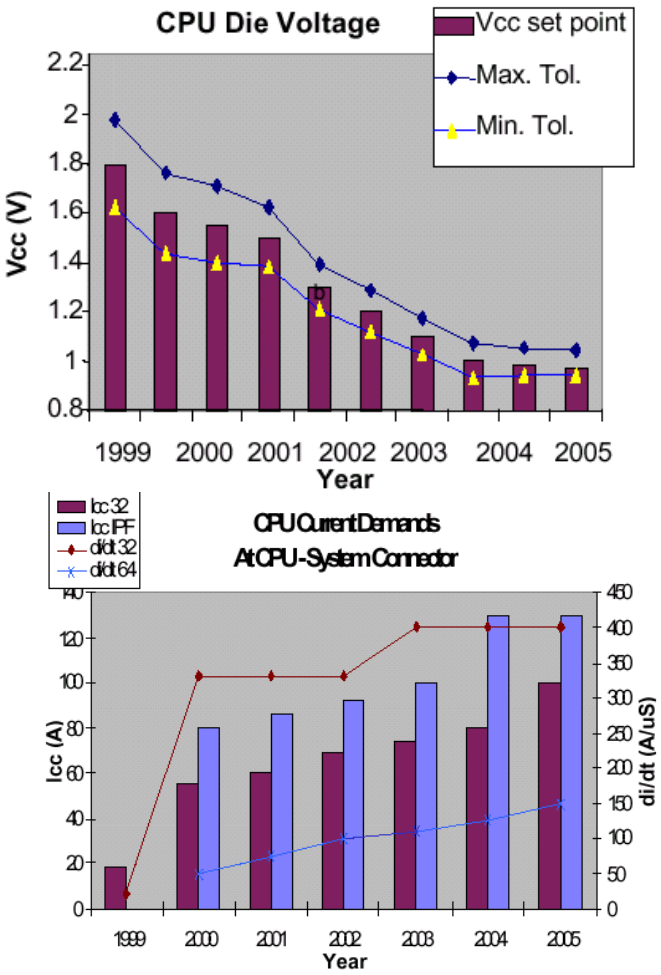


Fig. 2.1 Intel roadmap of the CPU load voltage and current.

Tab.2.1 Specifications for present VRMs

VRM 9.0

Current	60A
Voltage	1.7V
Slew rate	50A/μs
Voltage tolerance	70mV
Efficiency	>80%
Size	3.8×1.95×0.5 $inch^3$

2.1. Critical Inductance [28]

The majority of today's non-isolated input VRMs use the multi-phase interleaving synchronous rectifier buck topology shown in Fig. 2.2 [4][5][6][7][8][9][10].

The small-signal model of a multi-phase interleaving buck can be simplified as a single-phase buck converter [11][28], as shown in Fig. 2.3. The equivalent inductance in the simplified model is *1/n* of the inductance in each phase. The equivalent switching frequency of the simplified model is *n* times the switching frequency in each phase. So the multi-phase interleaving buck converter can be analyzed in the same way as a single-phase buck converter.

The greatest challenge in VRM design is to meet the stringent transient response requirement. The processor load of the VRM has a high current step change with high di/dt, especially when the CPU experiences changes between sleep mode and active mode or changes caused by the software. Generally speaking, the VRM output inductor current slew rate is much lower than the load current slew rate, as shown in Fig. 2.4 (a). Therefore, the output capacitor has to provide some energy in additional to the inductor current to power the load. The voltage drop across the VRM output capacitor occurs due to the unbalanced charges between the current flowing into the capacitor and that flowing out of it. It is straightforward that increasing the VRM output inductor current slew rate reduces the unbalanced charges. Via this approach the VRM transient response can be improved. This can be verified by simulation. Fig. 2.4 (b) explains this concept: When the VRM inductor current slew rate increases from I_L to I_L', the VRM transient output voltage spikes can be much reduced from, V_o to V_o'.

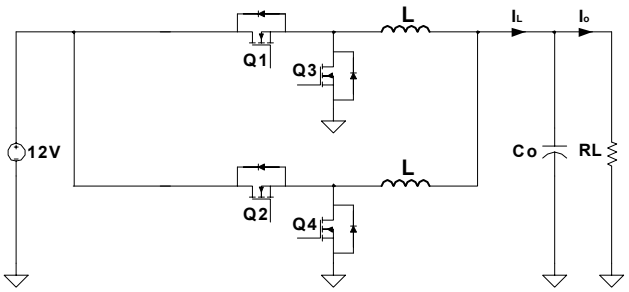
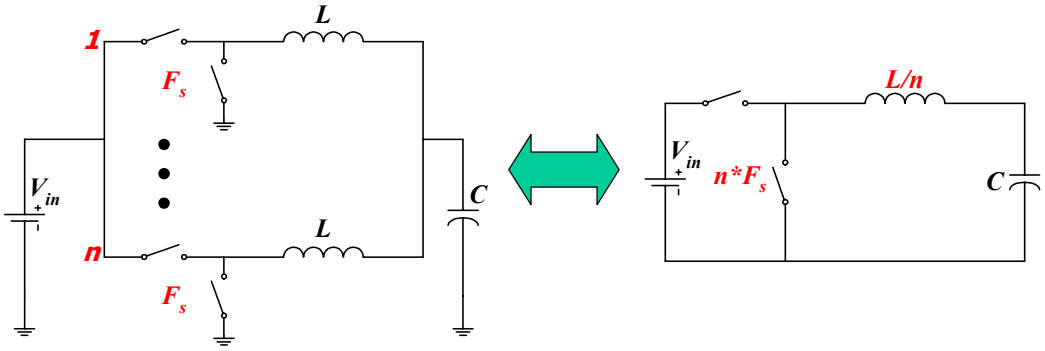
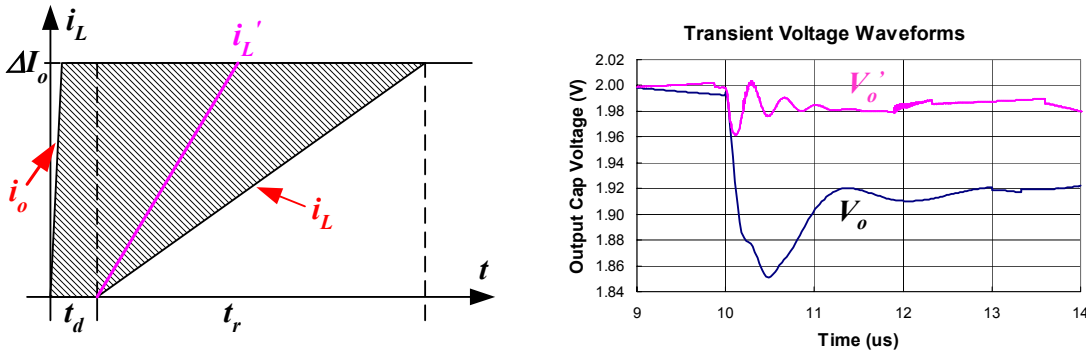


Fig. 2.2. Multi-phase interleaving synchronous rectifier buck converter.



(a) (b)

Fig. 2.3. An n-phase interleaving buck converter can be simplified as a single-buck converter (*L/n, n*Fs*) for small-signal analysis: (a) n-channel interleaving buck; and (b) equivalent single-buck converter.



(a) (b)

Fig. 2.4. Impact of inductor current slew rate on VRM output transient voltages: (a) two different inductor current slew rates; and (b) different corresponding transient voltage waveforms.

Intuitively, it seems that smaller inductance yields faster inductor current slew rate, but this is not always true.

During the transient, if the inductance is too large, it is possible for the duty cycle to become saturated. When the duty cycle is saturated, either the top switch or the bottom switch is always "on", so the equivalent circuit becomes that which is shown in Fig. 2.5. Under this circumstance, the feedback control is out of the picture, and the average i_o to i_L transfer function is an open-loop transfer function whose time constant is determined by the values of L and C. In this case, the inductor current slew rate can be improved by reducing the inductance at a fixed capacitance.

However, when the inductance is not too large, the duty cycle is not saturated; then the average i_o to i_L transfer function is a close-loop transfer function whose time constant is determined by the control bandwidth. In this case, reducing the inductance will not improve the inductor current slew rate.

A critical inductance causes the duty cycle to become nearly saturated during transient. The concept is explained via the three cases shown in Fig. 2.6, in which the control bandwidth ω_c is the same for each, while the inductances are different. There exists $L_1<L_2<L_3$.

The solid lines are the inductor current waveforms. The dashed lines are the average inductor current waveforms. The smaller inductance corresponds to the larger steady-state current ripple. The small inductance in case (a) corresponds to a small duty cycle increase ΔD during the transient response. The duty cycle is not saturated in this case. The average current slew rate is determined by the control bandwidth.

In case (b), the larger inductance results in larger ΔD. In this case, the duty cycle is at the boundary of saturation. The average current slew rate is also determined by the control bandwidth. Because the control bandwidths are the same for all three cases, the average current slew rates in cases (a) and (b) are the same. Although the switching inductor current waveforms are different in these two cases, the average inductor current waveforms (the dashed lines) are the same. The same transient voltage spikes are expected at the VRM output if the same output capacitance is used.

For case (c), the inductance is even larger. The compensator gives a larger error signal than in case (b). However, the duty cycle applied to the power stage is the same as that in case (b). In both cases, the duty cycle gets saturated during the transient responses. When the duty cycle is saturated, the current is determined by the inductance if the same output capacitors are used. Due to the larger inductance, case (c) has a lower current slew rate than that of case (b). The dot-dashed line in case (c) is the average current of cases (a) and (b). It has a higher slew rate than that of the dashed line, which is the average inductor current in case (c).

The critical inductance concept is also explained in Fig. 2.7. The curve in the figure is based on the average model simulation of step-down transient responses for a *12V*-input, *1.5V*-output buck VRM. For all the data points in the figure, the control bandwidths and the converter output capacitors are kept the same. The compensators for the different inductances are different in order to keep the same bandwidth. When the inductance is smaller than the critical inductance, the duty cycle does not saturate during transient responses. The transient responses are the same, and are determined by the control bandwidth. In this range, the inductance does not impact the transient response.

When the inductance is larger than the critical value, the duty cycle saturates during transient responses. The inductor current slew rate decreases as the inductance increases. In this range, the transient voltage spikes increase linearly as the inductances increase.

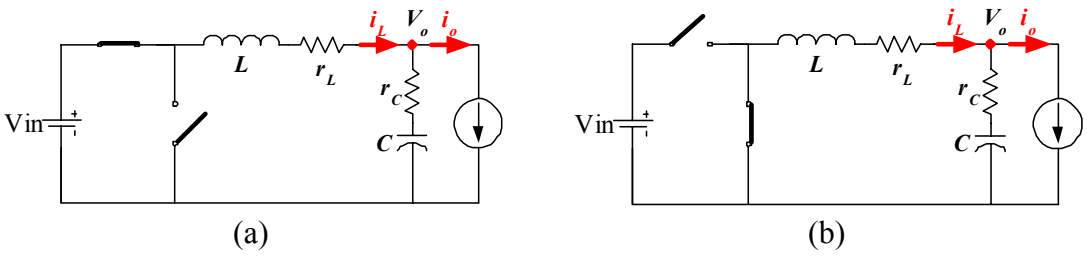
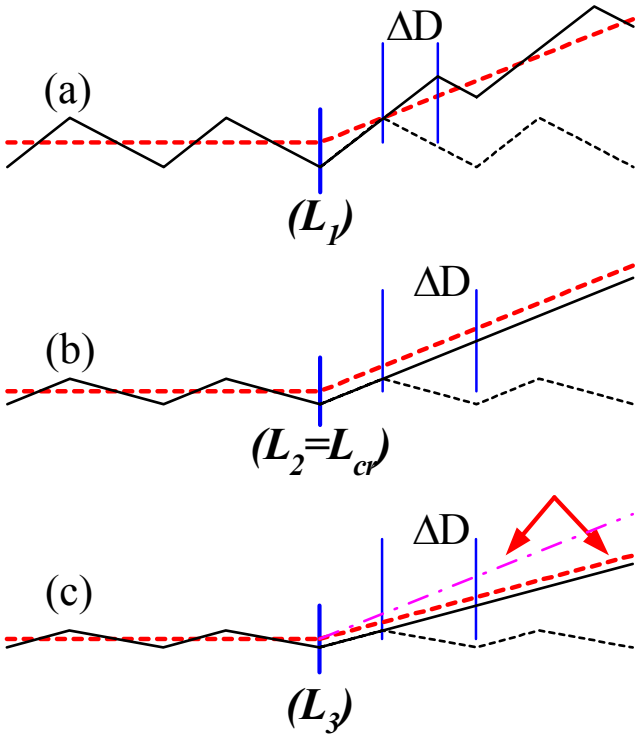


Fig. 2.5. Equivalent circuit when duty cycle is saturated:

(a) top switch is always "on"; (b) bottom switch is always "on."



(Constant ω_c, $L_1<L_2<L_3$)

Fig. 2.6. Impacts of inductance on inductor current slew rate: (a) & (b), same current slew rate, determined by ω_c; (c) lower current slew rate, determined by (V_{in}*$\Delta D/L$).

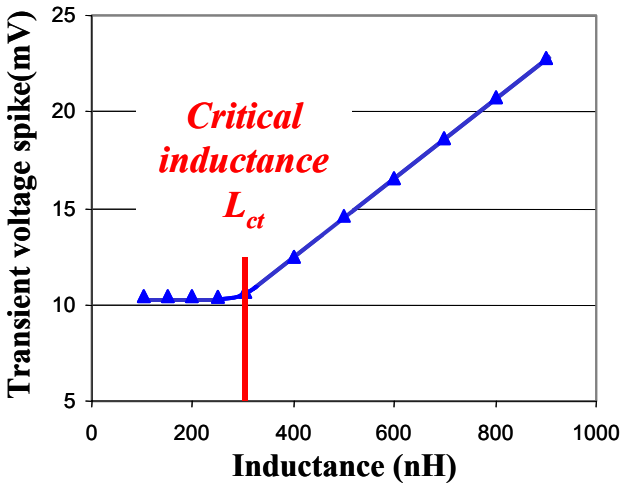


Fig. 2.7. Inductances smaller than L_{ct} give the same transient responses; transient voltage spikes increase for inductances larger than L_{ct}.

In order to identify the critical inductance, although the current slew rate is not constant within the rise time (as in Fig. 2.8), an approximation of the inductor current rise time is defined as follows:

$$t_r = \frac{T_c}{4} = \frac{\pi/2}{\omega_c}; \tag{2.1}$$

Within certain reasonable range of the control phase margin, the only factor that determines the inductor current rise time during transient responses is the feedback control bandwidth, as shown in (2.1). Formula (2.1) is true for different power stages. The inductor average current slew rate is approximately expressed as follows:

$$\left.\frac{di}{dt}\right|_{avg} = \frac{\Delta I_o}{t_r} = \frac{\Delta I_o \cdot \omega_c}{\pi/2}; \tag{2.2}$$

The inductor current slew rate can also be derived from the circuit operation. For the buck converter shown in Fig. 2.9, the steady-state duty cycle is D. The voltages of

both terminals of the inductor are $V_{in}\times D$. No net average voltage is applied to the inductor. The inductor current is constant in the average sense. During transient responses, the feedback control generates duty cycle increase ΔD. The duty cycle increase generates net voltage $V_{in}\times\Delta D$ for the inductor, which causes the inductor current to increase. The average inductor current slew rate can be easily derived as follows:

$$\left.\frac{di}{dt}\right|_{avg} = \frac{V_{in}\cdot\Delta D}{L}; \tag{2.3}$$

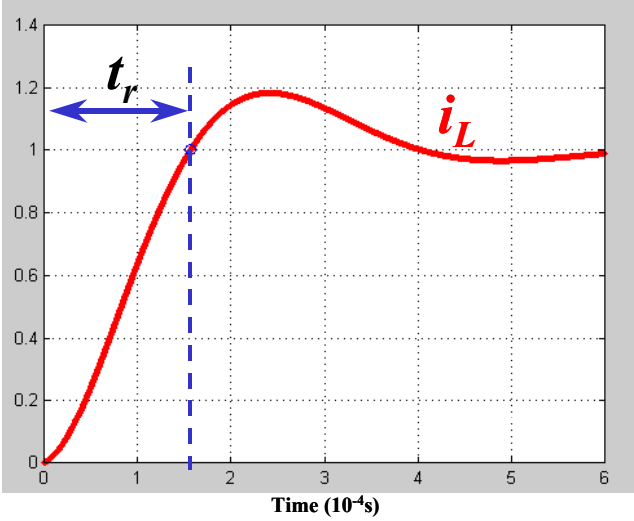


Fig. 2.8. Step response of open-loop current transfer function.

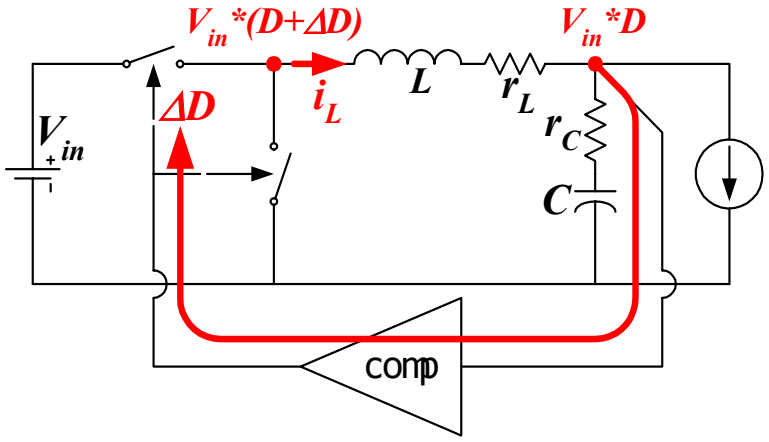


Fig. 2.9. Volt-seconds on inductor during a transient response.

Formulas (2.2) and (2.3) derive the inductor current slew rate from two different considerations: The former is valid as long as the duty cycle is not saturated, while the latter is always true. As long as the duty cycle is not saturated, the two formulas should be equal.

By equalizing Formulas (2.2) and (2.3), the transient duty cycle increase can be described as follows:

$$\Delta D = \frac{\Delta I_o \cdot \omega_c}{(\pi/2) \cdot V_{in}} \cdot L \; ; \tag{2.4}$$

Since the critical inductance makes the duty cycle nearly saturated, (2.4) can be rewritten as follows:

$$L_{ct} = \frac{(\pi/2) \cdot V_{in}}{\Delta I_o \cdot \omega_c} \cdot \Delta D_{\max} \; ; \tag{2.5}$$

where ΔD_{max} is the maximum duty cycle increase during the transient response.

2.2. Unequal Critical Inductances for Step Up and Step Down

Because ΔD_{max} may not be the same for step-up and step-down transient responses, the critical inductance for the two transient responses can be different. The step-up and step-down ΔD_{max} are defined as ΔD_{max1} and ΔD_{max2}, and accordingly, the step-up and step-down critical inductances are defined as L_{ct1} and L_{ct2}, respectively. Since $\Delta D_{max1}=1-D$, $\Delta D_{max2}=D$, it is easy to derive that

$$L_{ct2} = \frac{(\pi/2) \cdot V_{in}}{\Delta I_o \cdot \omega_c} \cdot D = \frac{(\pi/2) \cdot V_o}{\Delta I_o \cdot \omega_c} \tag{2.6}$$

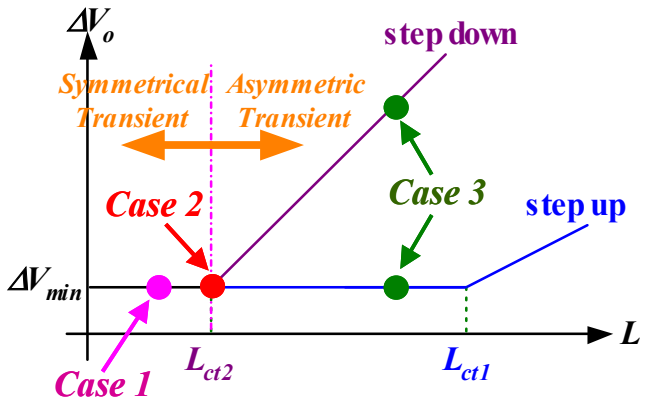
and

$$L_{ct1} = \frac{(\pi/2)\cdot V_{in}}{\Delta I_o \cdot \omega_c}\cdot(1-D) = \frac{(\pi/2)\cdot(V_{in}-V_o)}{\Delta I_o \cdot \omega_c}; \tag{2.7}$$

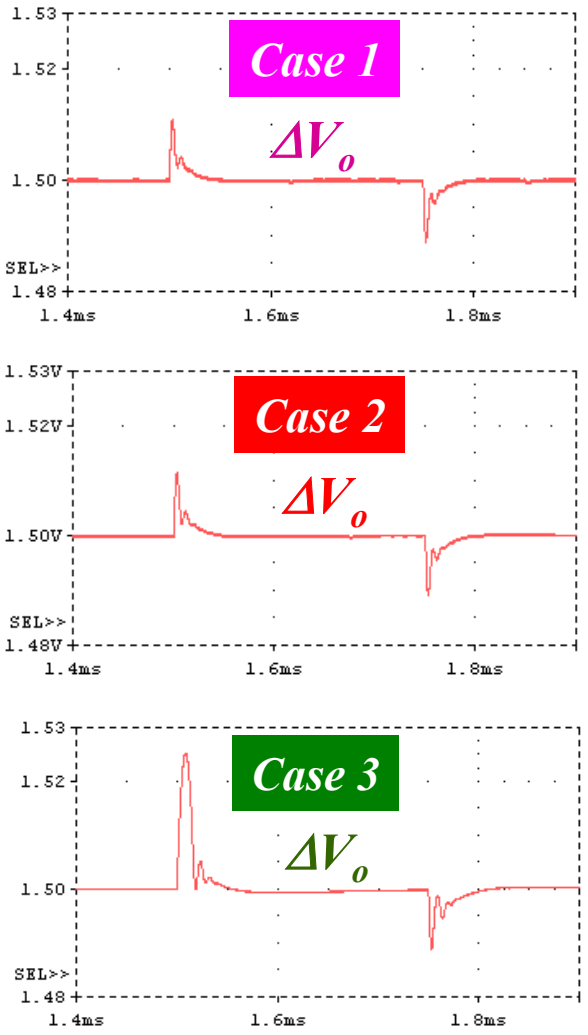
When the transient voltage spikes are determined by the control bandwidth ω_c, they are the same for both the step-up and step-down transient responses.

The step-up and step-down transient voltage curves are shown for comparison in Fig. 2.10. In a 12V-input buck VRM, for the 1~2V output voltage, the steady-state duty cycle D is less than 0.5; there is normally $\Delta D_{max1} > \Delta D_{max2}$, so $L_{ct1} > L_{ct2}$. It is observed that when $L < L_{ct2}$, the transient voltage spikes are determined by the control bandwidth ω_c; they are same for both the step-up and step-down transient responses. In another words, symmetrical transient response is obtained. When $L > L_{ct2}$, the step-up transient response has smaller voltage spike than the step-down transient response. Then the transient response is asymmetric.

Some switching model simulation examples for different cases are given in Fig. 2.10(a). In case 1, $L < L_{ct2}$; in case 2, $L = L_{ct2}$; in case 3, $L > L_{ct2}$. The results showing the output voltage transient responses for these three cases are shown in Fig. 2.10(b).



(a)



(b)

Fig. 2.10. Symmetrical and asymmetric transient response: (a) inductances smaller than L_{ct2} yield symmetrical transient responses; and (b) output voltage transient response.

In today's practice, adaptive voltage positioning (AVP) design is widely used.

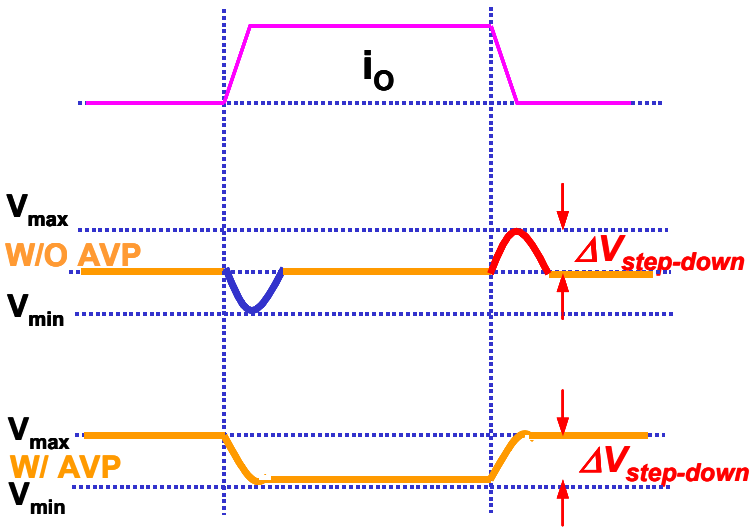
Fig. 2.11 explains AVP. The output voltage must stay within the regulation band. Without AVP, the sum of step-up and step-down voltage spikes must be less than V_{max}-V_{min}. In an AVP design, there is a steady state error. The output voltage stays at a lower level under heavy load conditions. This design reduces power at full load. When the load

changes, the voltage deviations for both step-up and step-down must be less than V_{max}-V_{min} individually. With the larger acceptable transient voltage deviation (as compared with the non-AVP design), fewer capacitors are required.

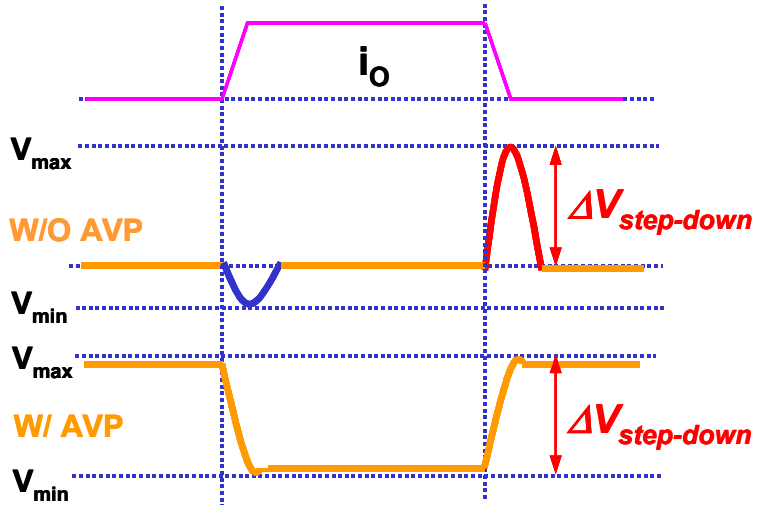
If the AVP design is applied, the larger voltage deviation must be less than V_{max}-V_{min}, which means the worse case of the step-up and step-down transient response dominates the transient response. From Fig. 2.10 it is identified that in the buck converter, the step-down load change always creates an equal or larger voltage deviation as compared with the step-up load change. Therefore, the transient voltage deviation is always determined by the step-down transient response.

When $L < L_{ct2}$, the transient response is symmetrical. The APV design in this case is shown in Fig. 2.11(a). When $L > L_{ct2}$, the transient response is asymmetric. The AVP design is shown in Fig. 2.11(b). Note that when $L > L_{ct2}$, the transient response is worse than when $L < L_{ct2}$. So for the sake of transient, there is no incentive to use a too-large inductance.

In a 12V buck VRM, the extreme steady-state duty cycle is determined by the input and output voltages, and there is no way to modify it. This extreme duty cycle is the fundamental reason why there are two very different critical inductance values. For instance, if the output voltage is *1.5V*, then the steady-state duty cycle is 0.125, and L_{ct2}=**7**L_{ct2}.



(a)



(b)

Fig. 2.11. Concept of adaptive voltage positioning (AVP): (a) when $L < L_{ct2}$, and (b) when $L > L_{ct2}$.

2.3. Penalties in Efficiency From the Extreme Duty Cycle

Since the output voltage is very low, the buck converter has a very small duty cycle. This extreme duty cycle impairs the efficiency [15].

A single-phase buck converter for analysis is specified as follows: V_{in}=*12V,* V_o=*1.5V,* I_{omax}=*12.5A,* F_s=*300KHz,* and *L=300nH*. The devices used are the Si4884DY for the top switch and the Si4874DY for the bottom switch. Fig. 2.12 shows the switch current waveforms.

According to the specified V_{in} and V_o, the steady-state duty cycle is

$$D = \frac{V_o}{V_{in}} = \frac{1.5}{12} = 0.125; \tag{2.7}$$

The bottom switch functions as a synchronous rectifier; therefore, the major loss is the conduction loss. The RMS current of the bottom switch is 12.3A.

Due to the very small duty cycle, to deliver the required energy to the output within a very short time interval, the top switch current waveform has to be very narrow and has a very large ripple. As a result, the top switch turn-off current is very large (20A) in order to provide the required average current (1.6A). This high turn-off current increases the switching loss so dramatically that the switching loss dominates the top switch loss.

Fig. 2.13 shows the device loss calculation result. From Fig. 2.13 it is identified that the major loss in the 12V buck VRM is the top switch switching loss and the bottom switch conduction loss.

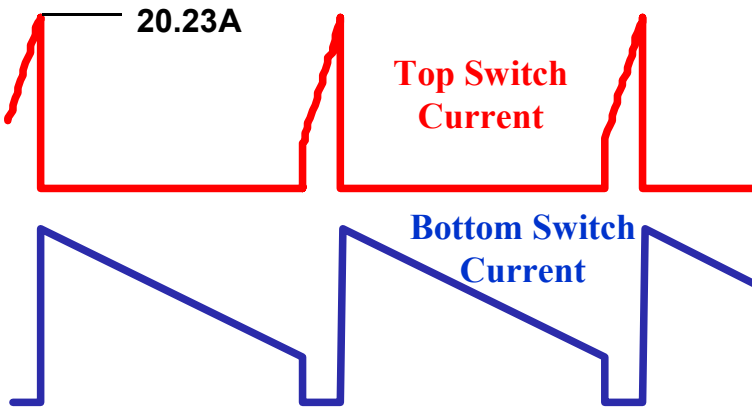


Fig. 2.12. Switch current waveforms of a 300nH 12V buck VRM @ full load.

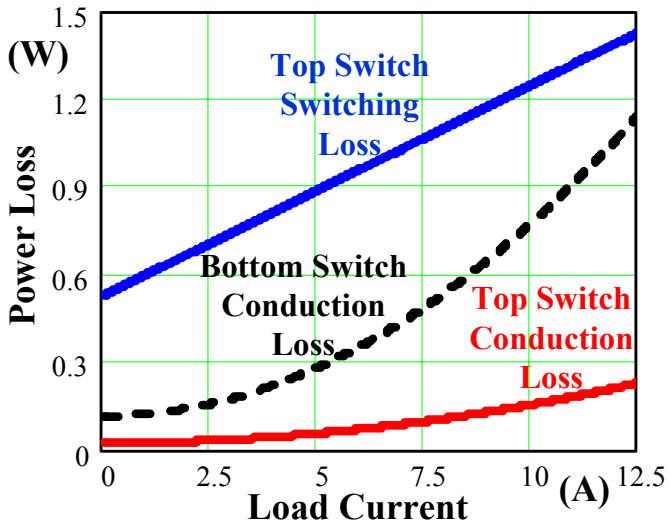


Fig. 2.13. 300nH device loss in 12V buck VRM.

2.4. Experimental Results of Four-Phase Interleaving Buck VRMs

A four-phase interleaving buck VRM prototype is built to test the performance, with the schematic shown in Fig. 2.14. The design specifications are: *12V* input, *1.5V* output, current load from *0~50A*, and *300 kHz/phase* switching frequency.

Devices optimizations are different for the top and bottom switches. Since switching loss dominates the top switch loss, devices featuring high switching speed are preferred. Therefore, devices with less gate charge are better candidates for top switches. The power device used for the top switches is the Si4884DY, which has 10.5mΩ on-resistance and 15.3nC gate charge. On the other hand, the fact that conduction loss dominates the bottom switch loss makes lower on-resistance devices better candidates for bottom switches. The power device used for the bottom switches is the Si4874DY, which has 7.5mΩ on-resistance and 35nC gate charge.

The choice of inductance considers both transient response and efficiency. Since it is the step-down transient response that dominates the transient voltage deviation, the choice of $L=L_{ct2}$ is the largest inductance that yields the best transient response. Assuming 100KHz bandwidth, the calculation based on Formula (2.6) yields the four-phase-equivalent critical inductance $L_{ct2}=75nH$. Since this is four-phase interleaving prototype, the real inductance of each phase is $4\times75nH=300nH$. The inductor is implemented using Philips EI-18 planar cores and PCB windings. The integrated magnetics technique is employed here. Fig. 2.15 shows the structure. Air gaps are put on the outer legs and there is no air gap on the center leg. In this way, two inductors are built in one EI core. The structure is also designed in a way such that the DC fluxes of the two inductors are added in the center leg. Because these two inductors belong to two 180°

interleaved phases, their AC fluxes get canceled in the center leg. This reduces the core loss.

The output capacitor is *6×1200μF* OSCON capacitors plus *18×22μF* ceramic capacitors.

Fig. 2.16 shows a photograph of the prototype.

Fig. 2.17 shows the top switch gate signal (upper trace) and the bottom switch gate signal (lower trace), respectively. As expected, the top switch duty cycle is very small. The measured efficiency of the prototype power stage is shown in Fig. 2.18. From the result, it is seen that the buck provides relatively low efficiency.

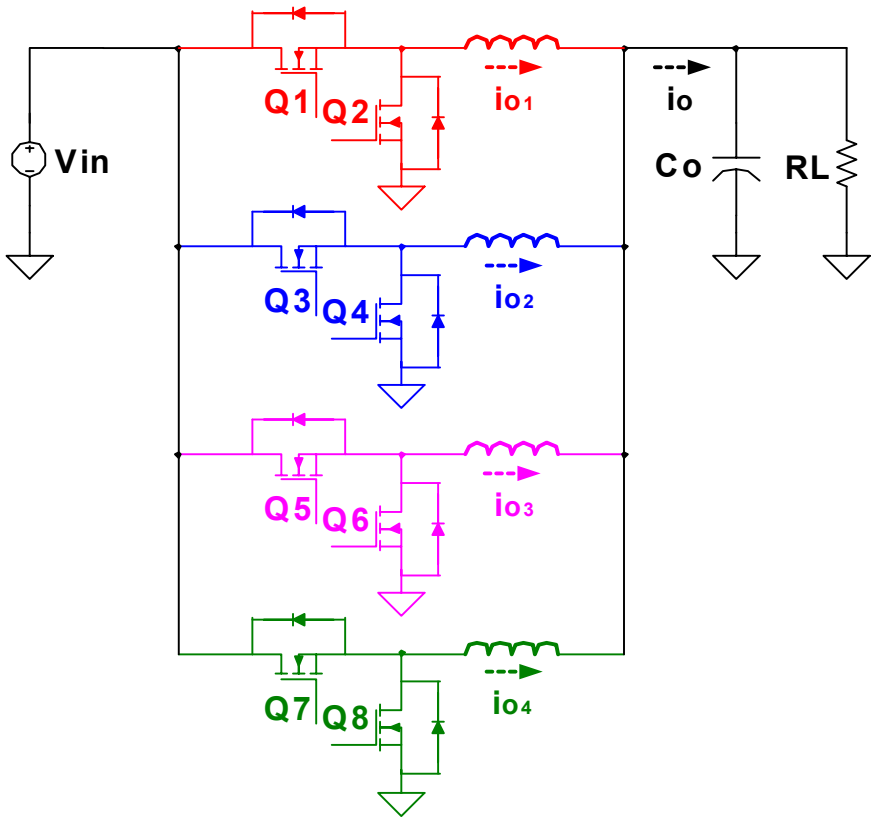


Fig. 2.14. Four-phase interleaving buck.

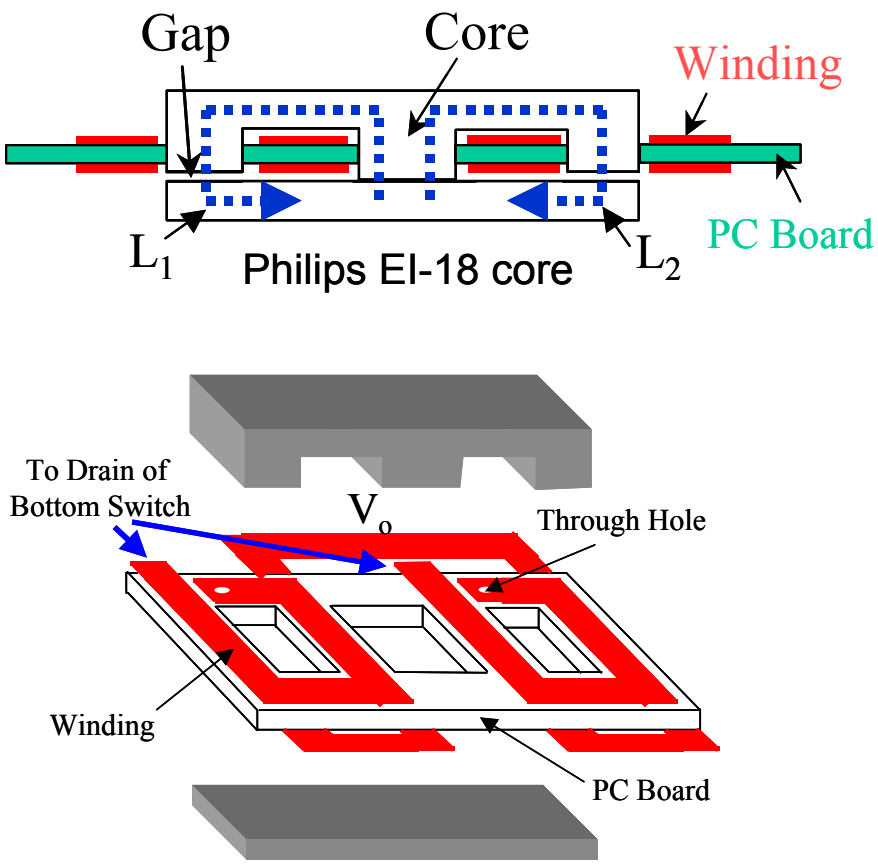


Fig. 2.15. Integrated magnetics implementation of the buck VRM.

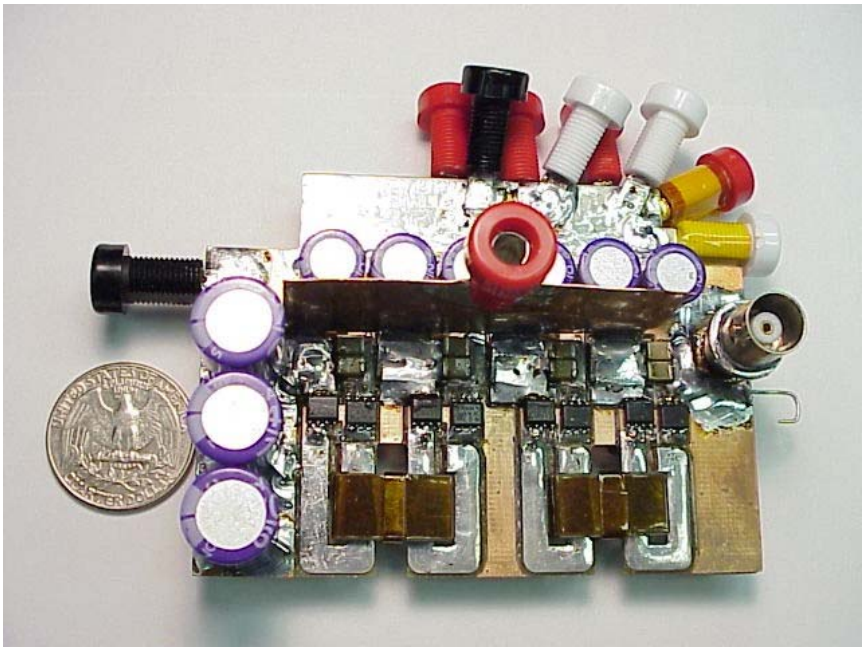


Fig. 2.16. Prototype picture of the four-phase interleaving buck VRM.

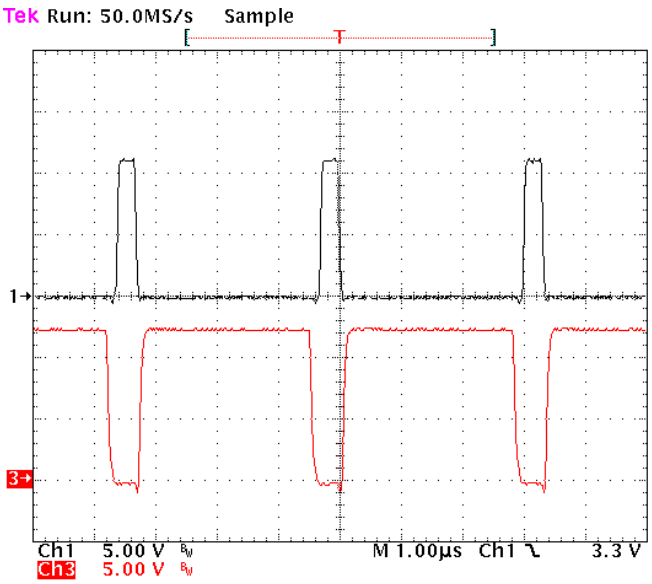


Fig. 2.17. Gate signals of the switches in the buck VRM.

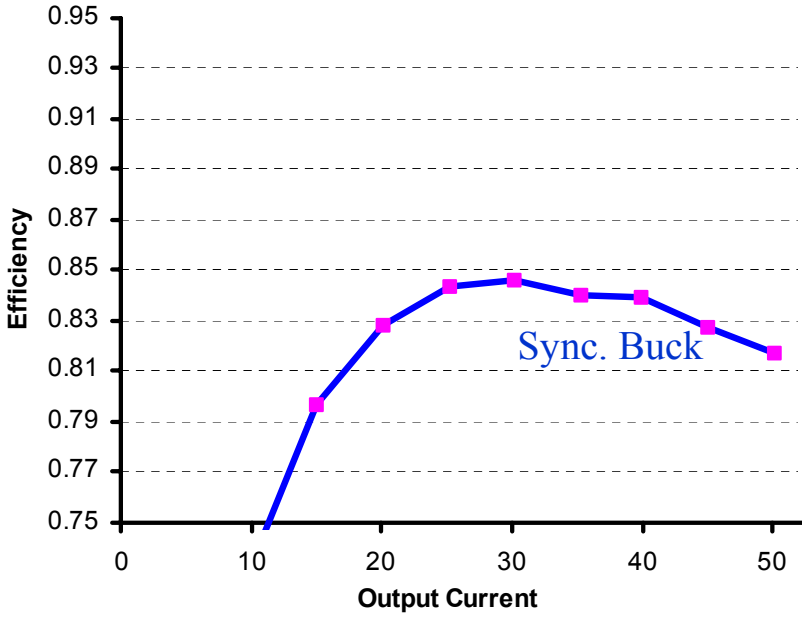


Fig. 2.18. Efficiency of the four-phase interleaving buck VRM.

2.5 Impact of Inductance on Efficiency

As discussed above, the largest inductance yielding the best transient response is L_{ct2}. However the choice of inductance is not only based on transient response, but also on efficiency. As a matter of fact, the inductance has an important impact on the efficiency.

Fig. 2.19 shows the change of the switch current waveforms when the inductance increases from 300nH to 500nH. A larger inductance yields a smaller current ripple, which reduces the top switch turn-off current and the bottom switch RMS current. 500nH inductance reduces the top switch turn-off current from 20.23A to 16.87A, and reduces the bottom switch RMS current from 12.3A to 11.9A. Device loss calculations for both 300nH and 500nH are plotted in Fig. 2.20. It is observed that the top switch switching loss and the bottom switch conduction loss are both reduced when a larger inductance is used. With these loss reductions, higher efficiency is expected.

A 500nH prototype is built to test the performance in comparison with the 300nH prototype. Everything remains the same except the inductance. Measured efficiency curves are plotted in Fig. 2.21. As expected, the 500nH prototype exhibits higher efficiency than the 300nH prototype.

From this analysis, it is seen that for the sake of the transient, a small inductance (as long as it is not smaller than L_{ct2}) is preferred; for the sake of efficiency, however, a large inductance is preferred. As a matter of fact, this trade-off between efficiency and transient response dominates the VRM design. Since the greatest challenge for VRMs comes from the very stringent transient response requirement, the optimal inductance is somewhere close to L_{ct2}.

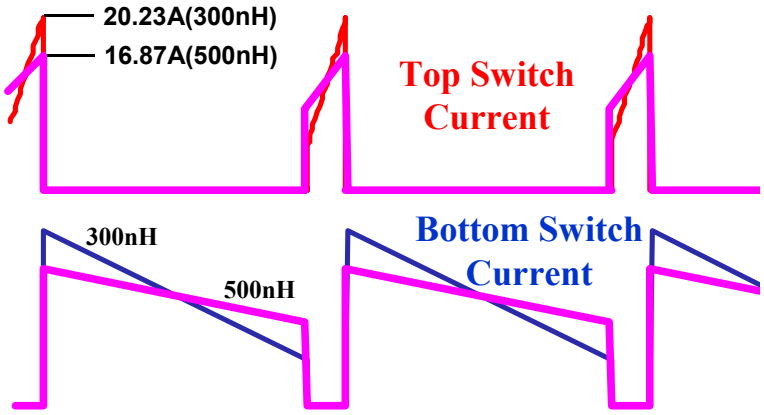


Fig. 2.19. Switch current waveforms comparison of 300nH and 500nH 12V buck VRM @ full load.

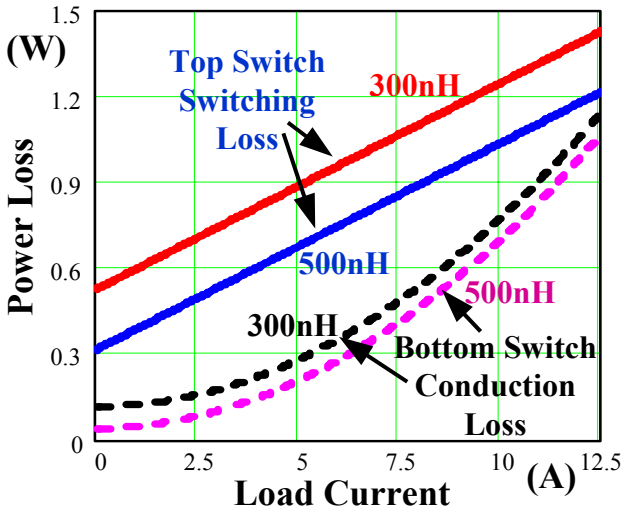


Fig. 2.20. Device loss comparison for different inductances in 12V buck VRM.

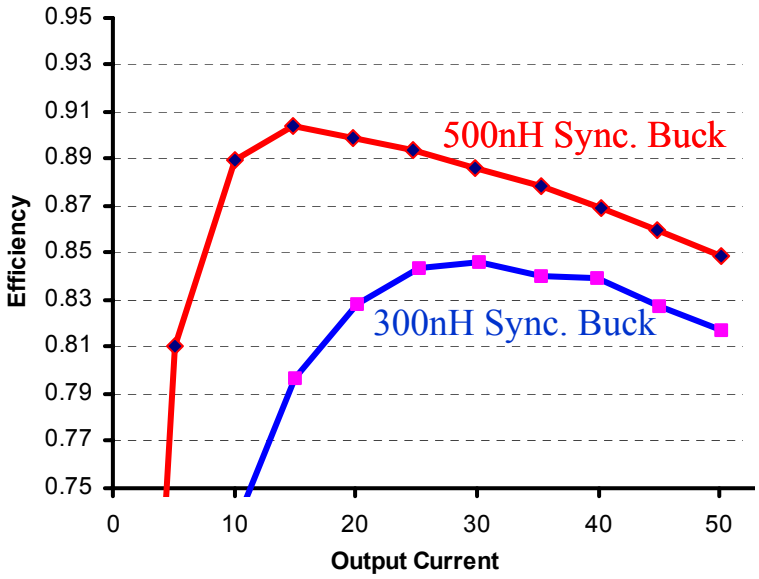


Fig. 2.21. Efficiency comparison of different inductances.

2.6. Poor Ripple Cancellation in the 12V Buck VRM

The 12V buck VRM has a very small duty cycle. This brings more issues in addition to the poor efficiency.

The multi-phase interleaving technique is a common industry practice to achieve current ripple cancellation. The effectiveness of the cancellation is a function of the duty cycle. For multi-phase interleaving cases, the ripple cancellation *vs.* duty cycle is shown in Fig. 2.22. The 12V buck VRM's steady-state duty cycle is around 0.1, which is located in the shaded region. Working in this region yields poor ripple cancellation.

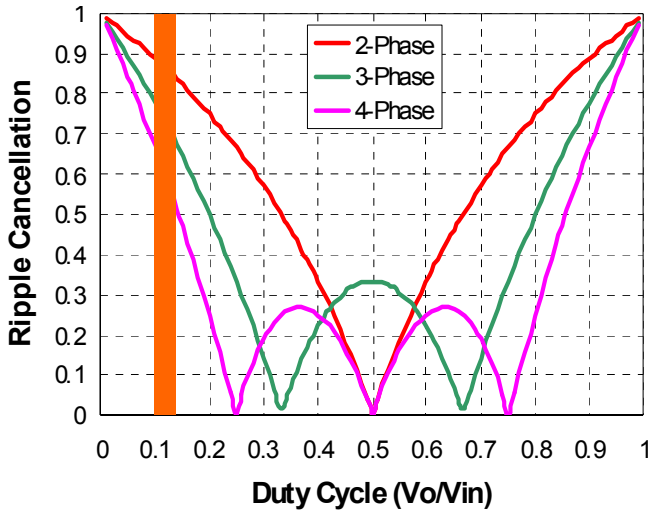


Fig. 2.22. Effectiveness of multi-phase interleaving ripple-cancellation.

2.7. Summary

In VRM design, the critical inductance is the largest inductance that yields the best transient response with given output capacitors and bandwidth.

Today's non-isolated high-input VRMs use multi-phase interleaving synchronous buck topology. Due to the high input voltage (12V) and the very low output voltage (≈1V), the duty cycle is very small (≈0.1). Therefore, in the buck converter, the step-up critical inductance is larger than the step-down critical inductance; the step-down transient response determines the transient voltage deviation when using AVP design.

The extreme duty cycle also impairs the VRM's efficiency. In addition, the extreme duty cycle weakens the ability of the interleaving to achieve effective current ripple cancellation. New solutions must be found to improve the performance.

Chapter 3.

High-Input-Voltage Non-Isolated VRM

— The Multi-Phase Interleaving Tapped-Inductor Buck VRM

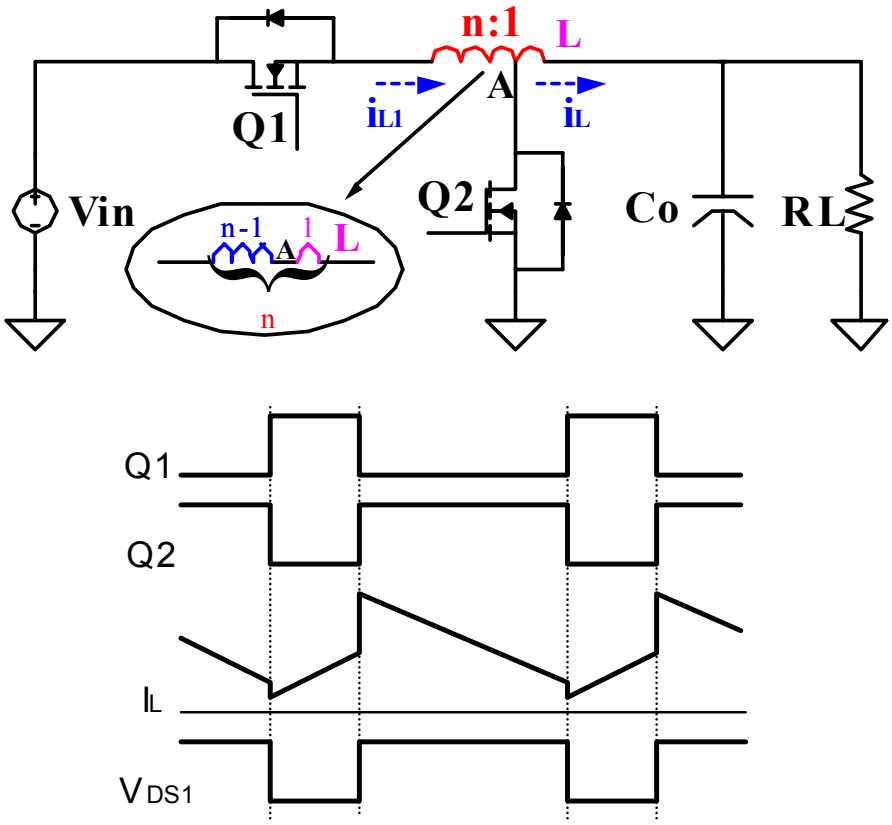
3.1. Tapped-Inductor Buck Converter

In the previous chapter, the extreme duty cycle was identified as the fundamental limitation of the 12V buck VRMs. Intuitively, the solution would be to extend the duty cycle.

For the buck topology, the duty cycle is simply $D = V_o / V_{in}$, so there is no way to modify it with given input and output voltages. A new topology, the so-called tapped-inductor buck [20], is able to extend the duty cycle and alleviate the problems in buck.

The tapped-inductor buck uses a tapped inductor instead of the simple inductor in the buck. The duty cycle then becomes a function of input voltage, output voltage and the turns ratio *n*. Fig. 3.1 shows this topology and its operation principle.

With properly designed turns ratio *n*, the duty cycle can be a more favorable value than that in the buck topology. Fig. 3.2 shows the duty cycle comparison between the buck and the tapped-inductor buck with different levels of *n*. The trend is that a larger *n* further extends the duty cycle. Thus there is an opportunity to improve the performance.



$$\frac{V_o}{V_{in}} = \frac{D}{n + (1-n)\cdot D}$$

Fig. 3.1. Tapped-inductor buck converter and its operation principles.

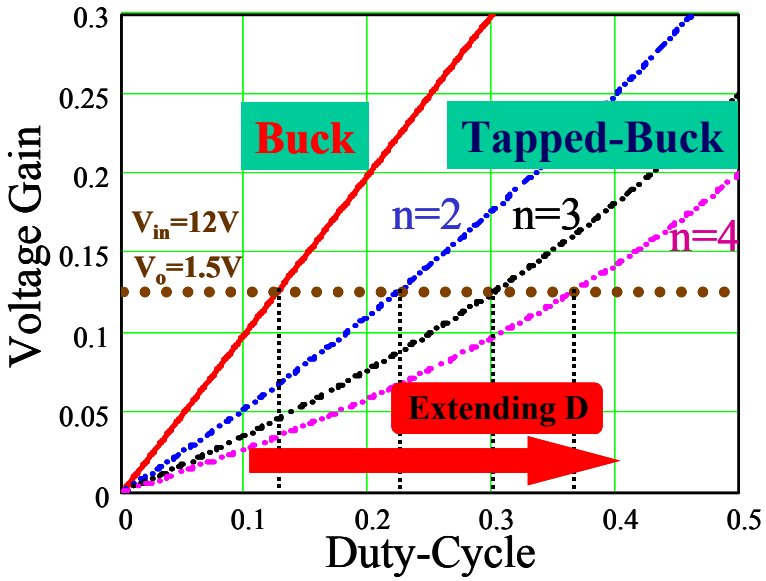


Fig. 3.2. Comparison of the duty cycles of buck and tapped-inductor buck.

3.2. Modeling of the Tapped-Inductor Buck Converter

To analyze the dynamic properties of the tapped-inductor buck converter, small-signal modeling is needed. Because of the tapped-inductor structure, the inductance of interest is selected as the one-turn "output" winding inductance, noted as L in Fig. 3.1. Then the n turn total inductance can be expressed as n^2L.

Choose the output inductor current i_L and the capacitor voltage V_o as the states for writing the state equations. Within one switching cycle, during $0 \sim DT_s$, the equivalent circuit is shown in Fig. 3.3(a). The state equations are

$$\begin{cases} \left(n^2 L\right) \cdot \dfrac{d\left(i_L / n\right)}{dt} = v_{in} - v_o \\ C_o \dfrac{dv_o}{dt} = \dfrac{1}{n} \cdot i_L - \dfrac{1}{R_L} v_o \end{cases}; \tag{3.1}$$

during $DT_s \sim T_s$, the equivalent circuit is shown in Fig. 3.3(b). The state equations are

$$\begin{cases} L \cdot \dfrac{di_L}{dt} = -v_o \\ C_o \dfrac{dv_o}{dt} = i_L - \dfrac{1}{R_L} v_o \end{cases} . \tag{3.2}$$

Do the cycle averaging to Equations (3.1) and (3.2), the average equations become

$$\begin{cases} L \cdot \dfrac{d\overline{i_L}}{dt} = \dfrac{\overline{d}}{n} \cdot \overline{v_{in}} + \dfrac{(n-1)\cdot \overline{d} - n}{n} \cdot \overline{v_o} \\ C_o \dfrac{d\overline{v_o}}{dt} = \dfrac{n + \overline{d} - n \cdot \overline{d}}{n} \cdot \overline{i_L} - \dfrac{1}{R_L} \overline{v_o} \end{cases} , \tag{3.3}$$

where variables with a bar on top stand for the cycle average values.

Define the corresponding perturbations

$\overline{i_L} = I_L + \hat{\overline{i_L}}$, $\overline{d} = D + \hat{\overline{d}}$, $\overline{v_{in}} = V_{in} + \hat{\overline{v_{in}}}$, and $\overline{v_o} = V_o + \hat{\overline{v_o}}$.

By imposing the condition of working around the steady-state point, the following equations are obtained:

$$\begin{cases} L \cdot \dfrac{d\hat{\overline{i_L}}}{dt} = \dfrac{D}{n} \cdot \hat{\overline{v_{in}}} + \dfrac{V_{in} + (n-1)\cdot V_o}{n} \cdot \hat{\overline{d}} - \dfrac{n + D - n \cdot D}{n} \cdot \hat{\overline{v_o}} \\ C_o \dfrac{d\hat{\overline{v_o}}}{dt} = \dfrac{n + D - n \cdot D}{n} \cdot \hat{\overline{i_L}} - \dfrac{n-1}{n} \cdot I_L \cdot \hat{\overline{d}} - \dfrac{1}{R_L} \hat{\overline{v_o}} \\ \hat{\overline{i_{in}}} = \dfrac{D}{n} \cdot \hat{\overline{i_L}} + \dfrac{I_L}{n} \cdot \hat{\overline{d}} \end{cases} . \tag{3.4}$$

From Equation (3.4), the equivalent circuit is obtained as shown in Fig. 3.4. Simplify the circuit; the final result is shown in Fig. 3.5, where

$$J(s) = \frac{n \cdot V_o}{R_L \cdot [D + n \cdot (1 - D)]^2},$$

$$L_e = \frac{n^2 \cdot L}{[D + n \cdot (1 - D)]^2},$$

$$\mu(D) = \frac{D + n \cdot (1 - D)}{D}, \text{ and}$$

$$e(s) = \frac{V_o \cdot [n + 2 \cdot D \cdot (1 - n)]}{D^2} \cdot \left\{ 1 + s \cdot \frac{L_e \cdot (1 - n) \cdot D}{R_L \cdot [n + 2 \cdot D \cdot (1 - n)]} \right\};$$

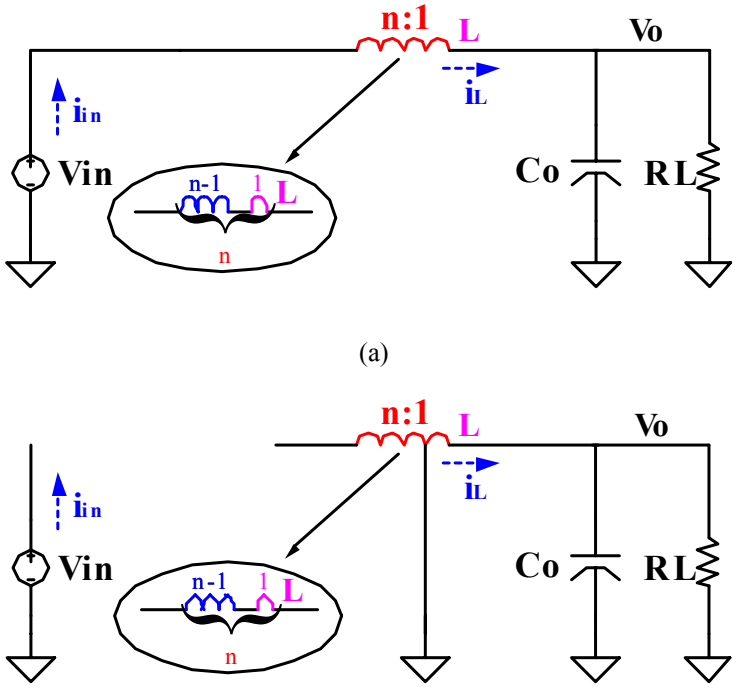


Fig. 3.3. Equivalent circuits of the tapped-inductor buck converter: (a) When Q1 is "on" and Q2 is "off", and (b) When Q2 is "on" and Q1 is "off"

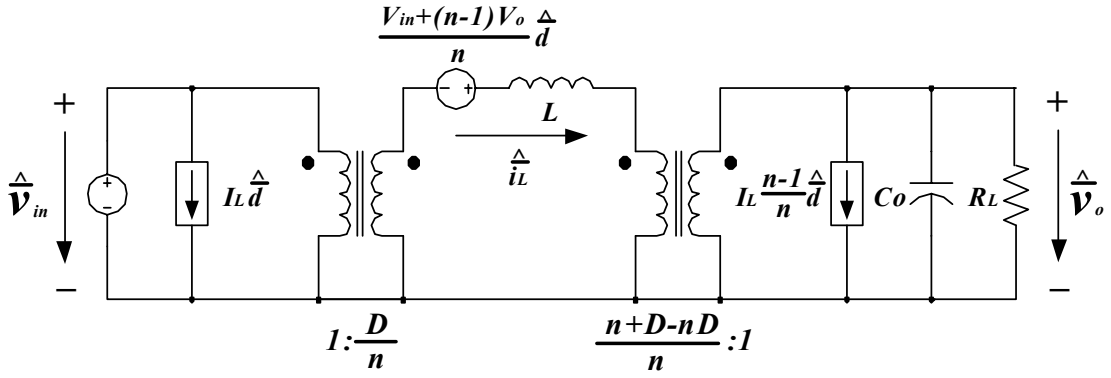


Fig. 3.4. Equivalent circuit of the small-signal model of the tapped-inductor buck converter.

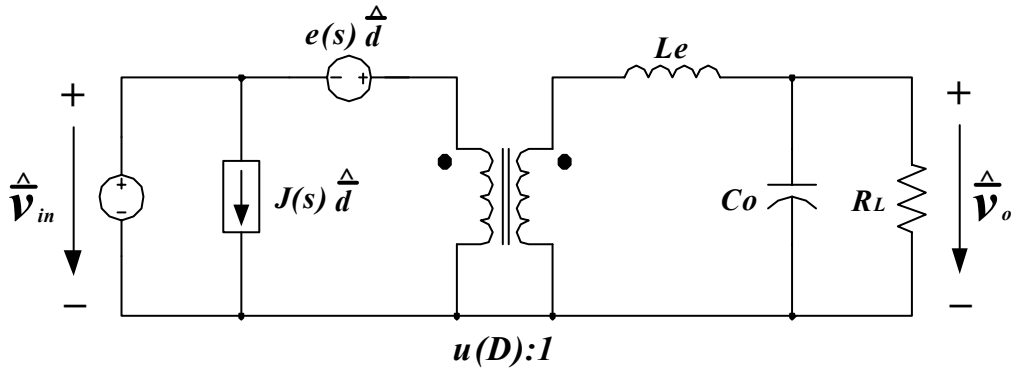


Fig. 3.5 Simplified equivalent circuit of the small-signal model of the tapped-inductor buck converter.

3.3. Critical Inductances of the Tapped-Inductor Buck Converter

It is understandable that the critical inductance concept still applies to the tapped-inductor buck converter. When the duty cycle is not saturated, the transient response is determined by the control bandwidth; when the duty cycle is saturated, the transient response is determined by L and C values. The inductance that causes the duty cycle to become nearly saturated is the critical inductance.

To derive the critical inductance of the tapped-inductor buck converter, the current slew rate is first studied. Assume the input voltage and the output voltage remain constant during the transient, then $\overline{v_{in}} = V_{in}$, and $\overline{v_o} = V_o$. By imposing the condition of working around the steady-state point for Equation (3.3), the following equation is obtained:

$$\frac{d\hat{\overline{i_L}}}{dt} = \frac{V_{in} + (n-1)V_o}{nL} \cdot \hat{d}. \tag{3.5}$$

Equation (3.5) is the control-determined output inductor current slew rate. According to Equation (2.2), when the duty cycle is not saturated, the output inductor current slew rate is

$$\frac{d\hat{\overline{i_L}}}{dt} = \frac{\Delta I_o \cdot \omega_c}{\pi/2}. \tag{3.6}$$

By equalizing Equation (3.5) and Equation (3.6), the transient duty cycle increase (when not saturated) is obtained, as follows:

$$\Delta D = \frac{n \cdot \Delta I_o \cdot \omega_c}{(\pi/2)\cdot\left[V_{in} + (n-1)V_o\right]} \cdot L. \tag{3.7}$$

Critical inductance is the value that makes the duty cycle nearly saturated during the transient response. Therefore the maximum duty cycle increase is

$$\Delta D_{\max} = \frac{n \cdot \Delta I_o \cdot \omega_c}{(\pi/2)\cdot\left[V_{in} + (n-1)V_o\right]} \cdot L_{ct}. \tag{3.8}$$

Rewriting Equation (3.8), the critical inductance is

$$L_{ct} = \frac{(\pi/2)\cdot\left[V_{in} + (n-1)V_o\right]}{n \cdot \Delta I_o \cdot \omega_c} \cdot \Delta D_{\max}. \tag{3.9}$$

Recall that in the buck converter, the critical inductance is expressed as

$$L_{ct} = \frac{(\pi/2)\cdot V_{in}}{\Delta I_o \cdot \omega_c} \cdot \Delta D_{\max}. \tag{3.10}$$

Since *n=1* makes the tapped-inductor buck become a buck, the same relationship between Equation (3.9) and Equation (3.10) is expected, and is shown to happen. Equation (3.9) degrades to Equation (3.10) when *n=1*.

As for the buck converter, there also exist two critical inductances for the tapped-inductor buck; one is for step-up and the other is for step-down transient response.

Following the definition for buck converter, L_{ct1} stands for step-up critical inductance and L_{ct2} stands for step-down critical inductance.

During the step-down transient response, the maximum duty cycle change is the steady-state value, which is

$$D_{\max 2} = D = \frac{n \cdot V_o}{V_{in} + (n-1) \cdot V_o} ;. \tag{3.11}$$

Substituting Equation (3.11) into Equation (3.9), the result is

$$L_{ct2} = \frac{(\pi/2) \cdot V_o}{\Delta I_o \cdot \omega_c} . \tag{3.12}$$

This is an interesting result. It reveals that in the tapped-inductor buck, the step-down critical inductance is NOT a function of the turns ratio *n*.

However, things are different for the step-up inductance. During the step-up transient response, the maximum duty cycle change is *1-D*, that is

$$D_{\max 1} = 1 - D = 1 - \frac{n \cdot V_o}{V_{in} + (n-1) \cdot V_o} = \frac{V_{in} - V_o}{V_{in} + (n-1) \cdot V_o} . \tag{3.13}$$

Substituting Equation (3.13) into Equation (3.9), the result is

$$L_{ct1} = \frac{(\pi/2) \cdot (V_{in} - V_o)}{n \cdot \Delta I_o \cdot \omega_c} , \tag{3.14}$$

which indicates that the step-up critical inductance IS a function of the turns ratio *n*.

From the trend shown by Equations (3.12) and (3.14), *n* modifies the critical inductances as illustrated in Fig. 3.6. The solid line stands for a case with a larger *n* than the case for which the dotted line stands. When *n* goes up, L_{ct2} remains constant and L_{ct1} goes down. To verify the change of the critical inductance as a result of the *n* change, some switching model simulations are done with different levels of *n* but the same

control bandwidth. Fig. 3.7(a) shows the simulated step-down transient voltage deviation for a buck converter. This L_{ct2} is about 300nH. Fig. 3.7(b) is the simulated step-down transient voltage deviation for an $n=2$ tapped-inductor buck converter. This L_{ct2} is also 300nH, just as expected. Figs. 3.8(a) and 3.8(b) show the simulated step-up transient voltage deviation for a buck converter and for an $n=2$ tapped-inductor buck converter, respectively. It is clear that when n increases from 1 to 2, L_{ct1} decreases as predicted. The L_{ct1} calculated based on Formula (3.14) is 1.05uH. This result matches the simulation result shown in Fig. 3.8(b).

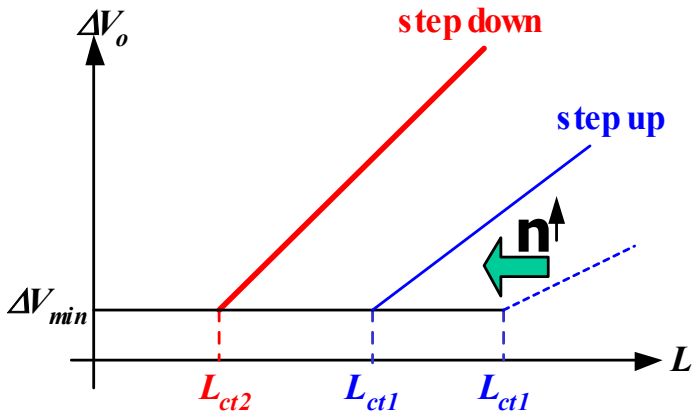
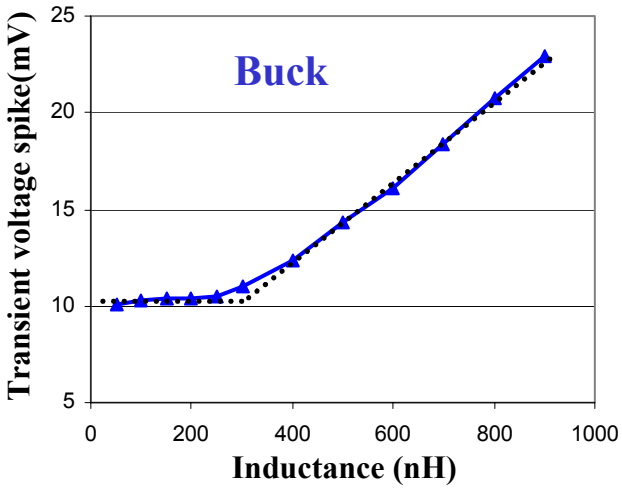
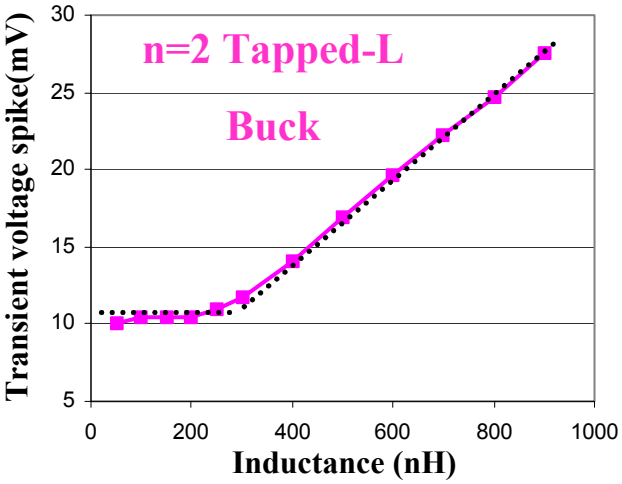


Fig. 3.6. Impact on the critical inductance from the turns ratio n.

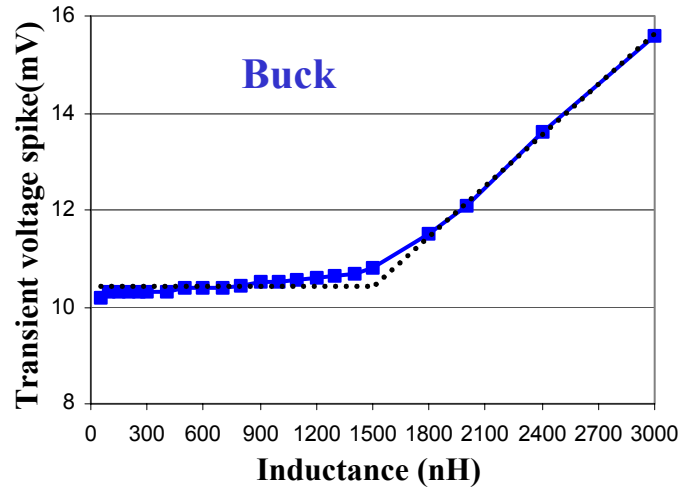


(a)

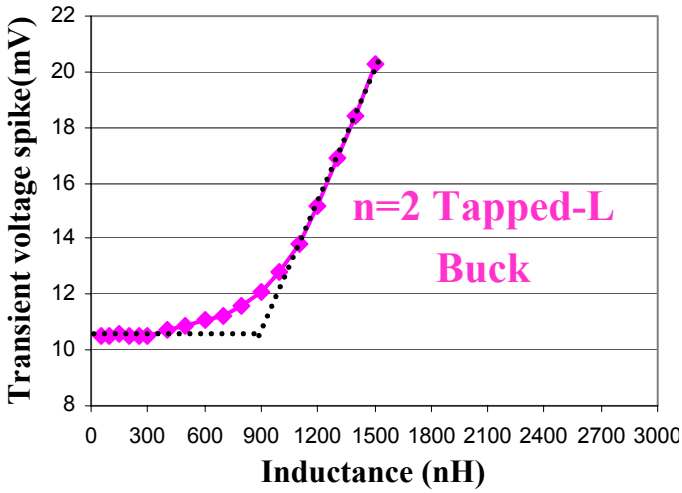


(b)

Fig. 3.7. Simulated step-down transient voltage deviation @ V_{in}=12V, V_o=1.5V, I_o=12.5A, ω_c=100KHz, L=300nH, and C_o=1800μF: (a) For buck converter and (b) For tapped-inductor converter.



(a)



(b)

Fig. 3.8. Simulated step-up transient voltage deviation @ V_{in}=12V, V_o=1.5V, I_o=12.5A, ω_c=100KHz, L=300nH, and C_o=1800μF: (a) For buck converter and (b) For tapped-inductor converter.

In the buck, due to the extreme duty cycle, there is always $L_{ct1} >> L_{ct2}$. For a tapped-inductor buck, with the same design specs, the L_{ct2} is same as the buck's. However, L_{ct1} is now not only dependent on specs, but also dependent on n. If n is not too large, $L_{ct1} \geq L_{ct2}$; if n is too large, there will be $L_{ct1} < L_{ct2}$. As shown in Fig. 3.9, when $L_{ct1} \geq L_{ct2}$, the step-up voltage spike is equal to or smaller than the step-down voltage spike; when $L_{ct1} < L_{ct2}$, the step-up voltage spike is larger than the step-down voltage spike. It

was discussed in Chapter 2 that when an AVP design is employed, the larger voltage spike determines the transient voltage deviation. Therefore, for different values of n, when $L_{ct1} \geq L_{ct2}$, the transient response is the same; when $L_{ct1} < L_{ct2}$, the transient response deteriorates.

The choice of n that yields the best transient response satisfies $L_{ct1} \geq L_{ct2}$, so

$$\frac{(\pi/2)\cdot(V_{in}-V_o)}{n\cdot\Delta I_o\cdot\omega_c} \geq \frac{(\pi/2)\cdot V_o}{\Delta I_o\cdot\omega_c}, \tag{3.15}$$

which is

$$n \leq \frac{V_{in}}{V_o} - 1. \tag{3.16}$$

A design example is shown in Fig. 3.10. In this design case, when $n \leq 7$, $L_{ct1} \geq L_{ct2}$, the choice of n within this range yields the best transient response.

From the preceding discussion, it is concluded that as long as $n \leq V_{in}/V_o - 1$, compared with the buck converter, the tapped-inductor buck converter maintains the same transient response. In the meantime, the duty cycle is extended. This supports the idea that there is an opportunity to improve the VRM performance through properly designing n.

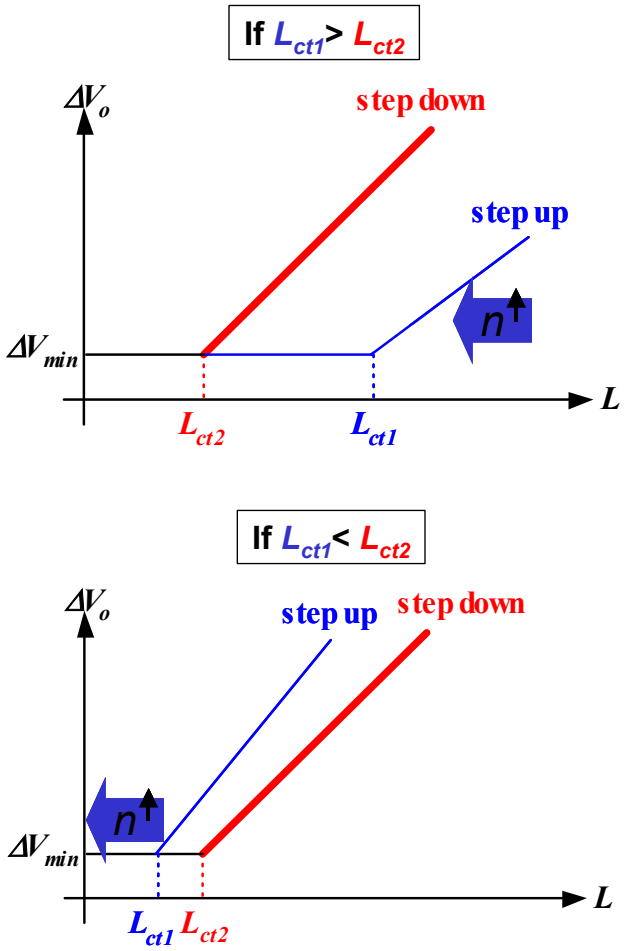


Fig. 3.9. Too-large n causes $L_{ct1} < L_{ct2}$.

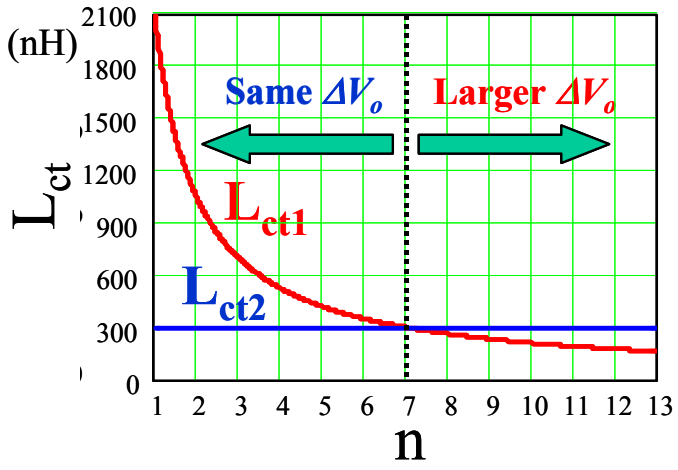


Fig. 3.10. An example showing how a too-large n impairs transient response
V_{in}=12V, V_o=1.5V, I_o=12.5A, and ω_c=100KHz.

3.4. Efficiency Improvement Gained From the Extended Duty Cycle

In a tapped-inductor buck, because the duty cycle is extended, the switch current waveforms are different from those of the buck. Fig. 3.11 shows a comparison of the switch current waveforms of a buck converter and an *n=2* tapped-inductor buck converter. With the extended duty cycle, the top switch turn-off current is dramatically reduced. This greatly reduces the top switch switching loss. The extended duty cycle also shapes the bottom switch current waveform, which changes the bottom switch conduction loss.

As discussed in the previous chapter, the dominant losses are the top switch switching loss and the bottom switch conduction loss. A loss-estimation for a specified design example is done with different levels of *n*, as shown in Fig. 3.12(a). The larger the *n*, the lower the top switch switching loss. In the meantime, the conduction loss is a "U" shape. When *n=2* or *3*, the conduction loss is at its lowest. The total device loss, including top switch switching loss, bottom switch conduction loss, and top switch conduction (although a small part of the total loss), is shown in Fig. 3.12(b). This result shows that the properly designed tapped-inductor buck is expected to have higher efficiency than the buck. As in the previous discussion, when $n \leq 7$ the transient response is same, but when $n > 7$ transient response is worse.

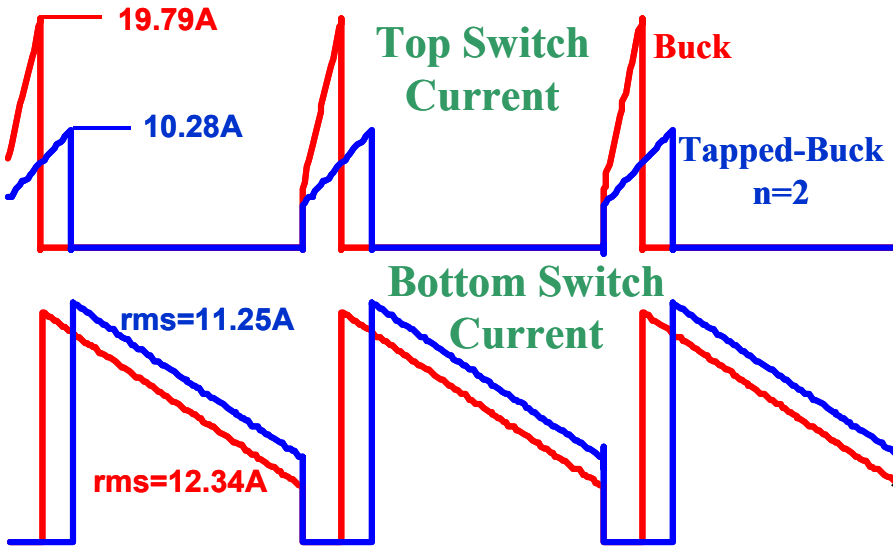
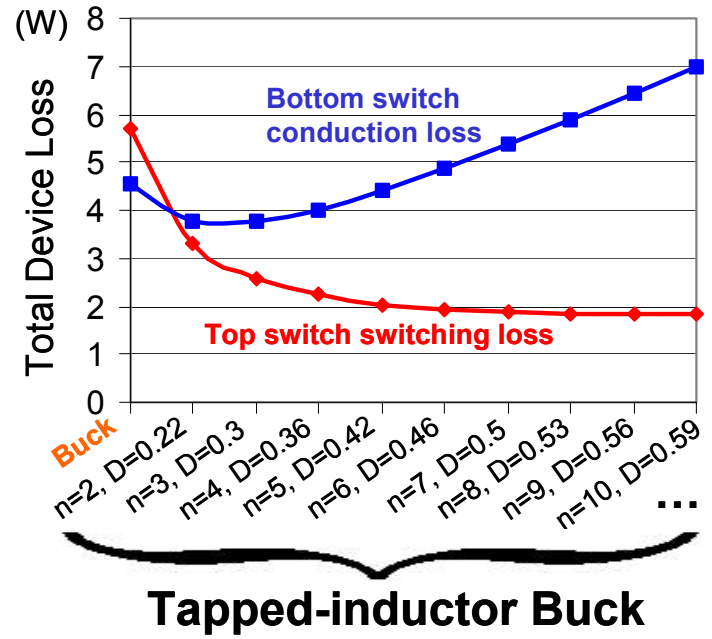
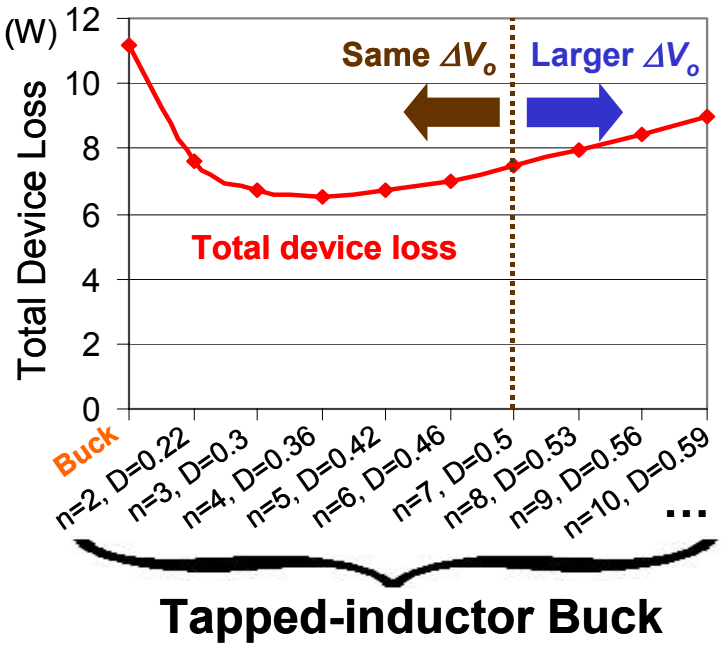


Fig. 3.11. Switch current comparison of buck and "*n=2*" tapped-inductor buck.



(a)



(b)

Fig. 3.12. Tapped-inductor buck major device loss as a function of n
V_{in}=12V, V_o=1.5V, I_o=12.5A, L=300nH;
Top device is Si4884DY(10.5mΩ, 15.3nC) and Bottom device is Si4874DY(7.5mΩ, 35nC):
(a) Top switch switching loss and bottom switch conduction loss, and (b) Total device loss.

3.5. Dynamic Issues in Tapped-Inductor Buck converter

The control-to-output transfer function is

$$G_{vd}(s) = e(s) \cdot \frac{1}{\mu(D)} \cdot \frac{1}{1 + \frac{s}{Q \cdot \omega_o} + \left(\frac{s}{\omega_o}\right)^2}, \tag{3.17}$$

where

$$\mu(D) = \frac{D + n \cdot (1 - D)}{D},$$

$$e(s) = \frac{V_o \cdot [n + 2 \cdot D \cdot (1 - n)]}{D^2} \cdot \left\{1 + s \cdot \frac{L_e \cdot (1 - n) \cdot D}{R_L \cdot [n + 2 \cdot D \cdot (1 - n)]}\right\},$$

$$L_e = \frac{n^2 \cdot L}{[D + n \cdot (1 - D)]^2},$$

$$\omega_o = \frac{1}{\sqrt{L_e \cdot C_o}}, \text{ and}$$

$$Q = R_L \cdot \sqrt{\frac{C_o}{L_e}}.$$

From the transfer function, the system poles are located at

$$s = -\frac{1}{2 \cdot R_L \cdot C_o} \pm i \cdot \sqrt{\frac{1}{L_e \cdot C_o} - \frac{1}{(2 \cdot R_L \cdot C_o)^2}}. \tag{3.18}$$

This is a moving double pole. It moves with the variation of the turns ratio n and load R_L. This brings some issues in the compensator design. The compensator has to be designed according to the worst case. However, things are more complicated than that. In addition to the moving double pole, there is a zero in the tapped-inductor buck. This zero is located at

$$z = -\frac{R_L}{L_e} \cdot \left(2D + \frac{n}{1-n} \right). \tag{3.19}$$

This is a moving zero, moving with both the variation of the turns ratio n and load R_L. Because the duty cycle can be express by V_{in} and V_o, Equation (3.19) is rewritten as

$$z = \frac{R_L}{L_e} \cdot \frac{n}{\frac{V_{in}}{V_o} + n - 1}. \tag{3.20}$$

In 12V VRM design, $V_{in} = 12V$. Then, the term $\frac{n}{\frac{V_{in}}{V_o} + n - 1}$, in Fig. 3.13, is plotted as a function of n and V_o. Current and future processors work at the shaded region, where for all the plotted cases, the value of $\frac{n}{\frac{V_{in}}{V_o} + n - 1}$ is positive. This means that the moving zero is located in the right half plane.

A right-half-plane (RHP) zero is already bad for stability. It shrinks the phase margin. When moving, it is even worse. Analysis of an example is done at $V_{in}=12V$, $V_o=1.5V$, and $I_o=12.5A/phase$. For $n=2$ to $n=7$, the locations of the RHP moving zero are plotted in Fig. 3.14. From this figure it is seen that this RHP zero could move to the frequency range of the intended control bandwidth (several tens of KHz). This introduces an obstacle for pushing the control bandwidth. Fig. 3.15(a) shows the control to output transfer function $G_{vd}(s)$ when $L=300nH$, and Fig. 3.15(b) shows $G_{vd}(s)$ when $L=800nH$. It is quite pronounced that the RHP zero introduces another -90° phase-delay in addition to the -180° phase-delay introduced by the double pole. This $G_{vd}(s)$ makes it difficult for a

compensator design to achieve high bandwidth. The larger the n, or the larger the L, the lower the bandwidth has to be.

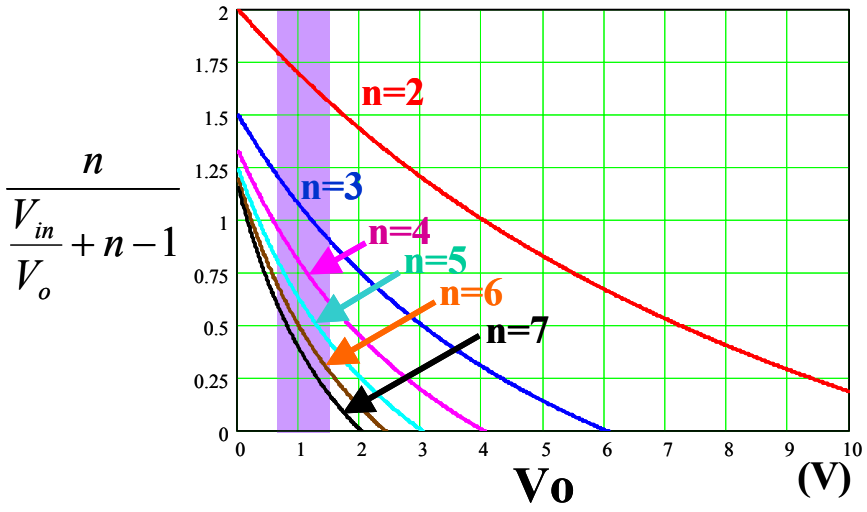


Fig. 3.13. Identifying the right-half-plane zero in the tapped-inductor buck.

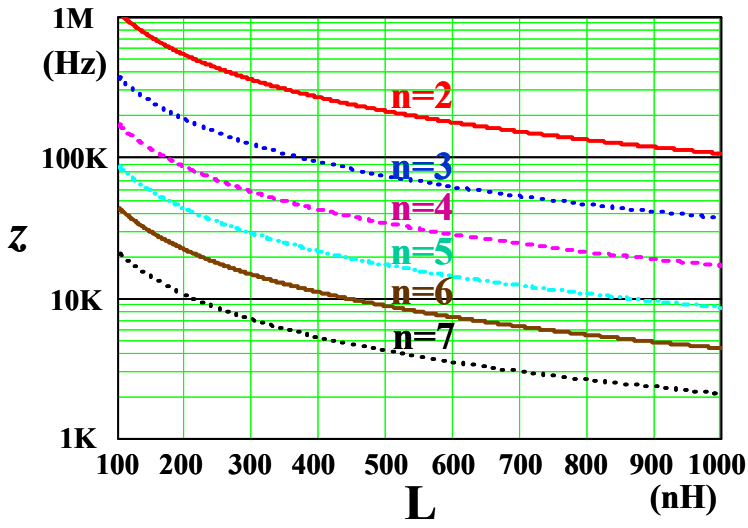
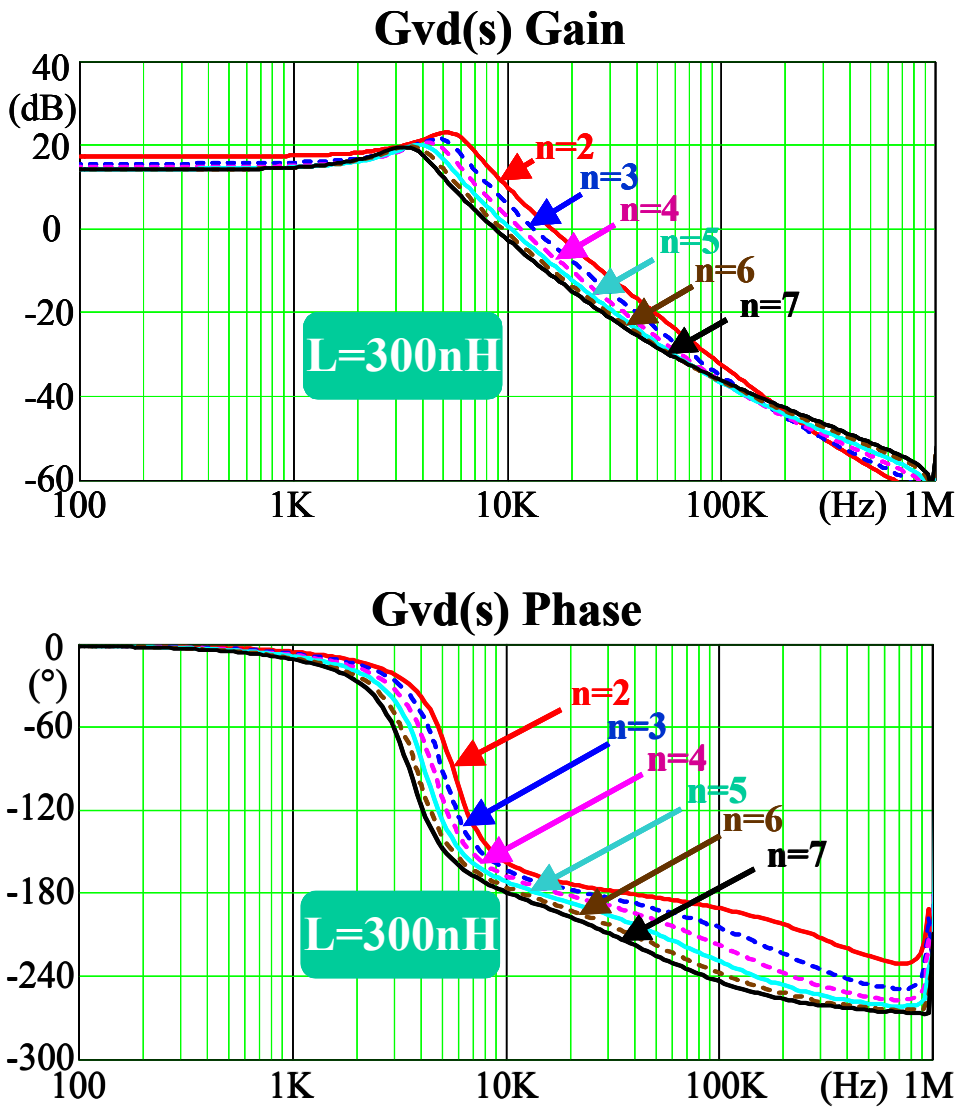
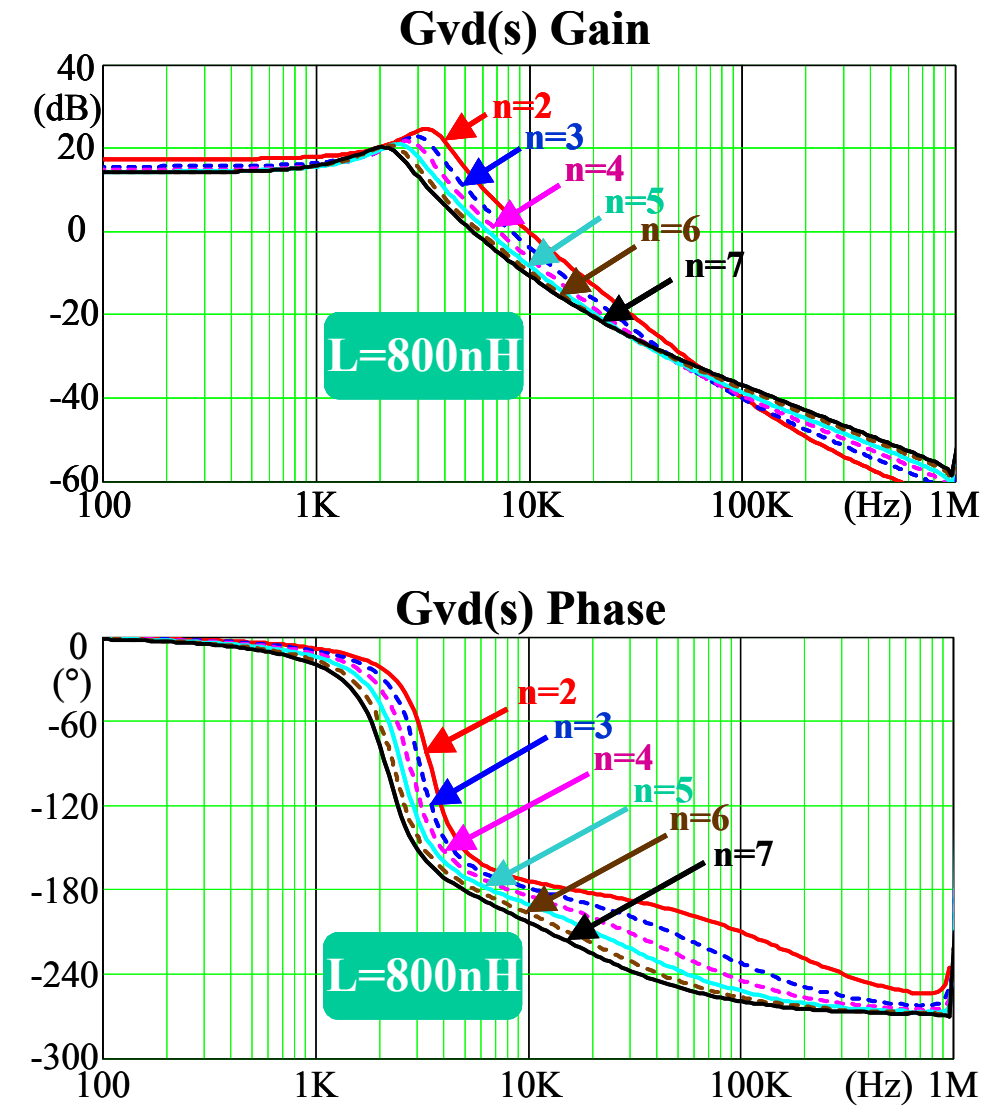


Fig. 3.14. The RHP zero in the tapped-inductor buck moves as a function of n and L.


Gvd(s) Gain
40
(dB)
20
0
-20
-40
-60
100
1K
10K
100K
(Hz)
1M
n=2
n=3
n=4
n=5
n=6
n=7
L=300nH
Gvd(s) Phase
0
(°)
-60
-120
-180
-240
-300
100
1K
10K
100K
(Hz)
1M
n=2
n=3
n=4
n=5
n=6
n=7
L=300nH

(a)



(b)

Fig. 3.15. The RHP zero presents some obstacles for wide bandwidth design:
(a) When *L=300nH* and (b) When *L=800nH*

3.6. Ripple Cancellation in the Multi-Phase Interleaving Tapped-Inductor Buck Converter

Interleaving can help achieve current ripple cancellation. Fig. 3.16 shows a four-phase interleaving configuration for the tapped-inductor buck converter. The four-phase output currents are $i_{o1} \sim i_{o4}$; the total output current is i_o. With interleaving, i_o can also achieve some ripple cancellation.

Figs. 3.17(a) through 3.17(c) show three design examples. In all three cases, four-phase interleaving is employed; $V_{in}=12V$, $V_o=1.5V$, and $I_o=50A$. The bottom four waveforms are $i_{o1} \sim i_{o4}$, and the top waveform is i_o. It is obvious that among the three examples, i_o has different AC components.

Since i_o's AC component goes through the output capacitor and causes loss on the ESR, the "ripple_ratio" is defined as the ratio of the i_o AC component RMS value and i_{o1} (or i_{o2}, or i_{o3}, or i_{o4}) AC component RMS value, expressed in Equation (3.21):

$$ripple\_ratio = \frac{rms\left(i_o\big|_{AC}\right)}{rms\left(i_{o1}\big|_{AC}\right)} \tag{3.21}$$

For the tapped-inductor buck, the ripple_ratio as a function of D is plotted in Fig. 3.18. Each curve in Fig. 3.18 corresponds to a different turns ratio from $n=2$ to $n=7$. As plotted, they are very close curves. This result indicates that the ripple cancellation is only a function of D, not a function of n. Compared with the buck, whose four-phase interleaving effectiveness is shown in Fig. 2.22, the tapped-inductor buck can achieve some ripple cancellation as well. But careful design is needed; otherwise the total output current ripple RMS value could be even larger than the one-phase current ripple RMS value.

For the above design example (V_{in}=12V, V_o=1.5V, and I_o=50A), the effectiveness of ripple cancellation is shown in Fig. 3.19.

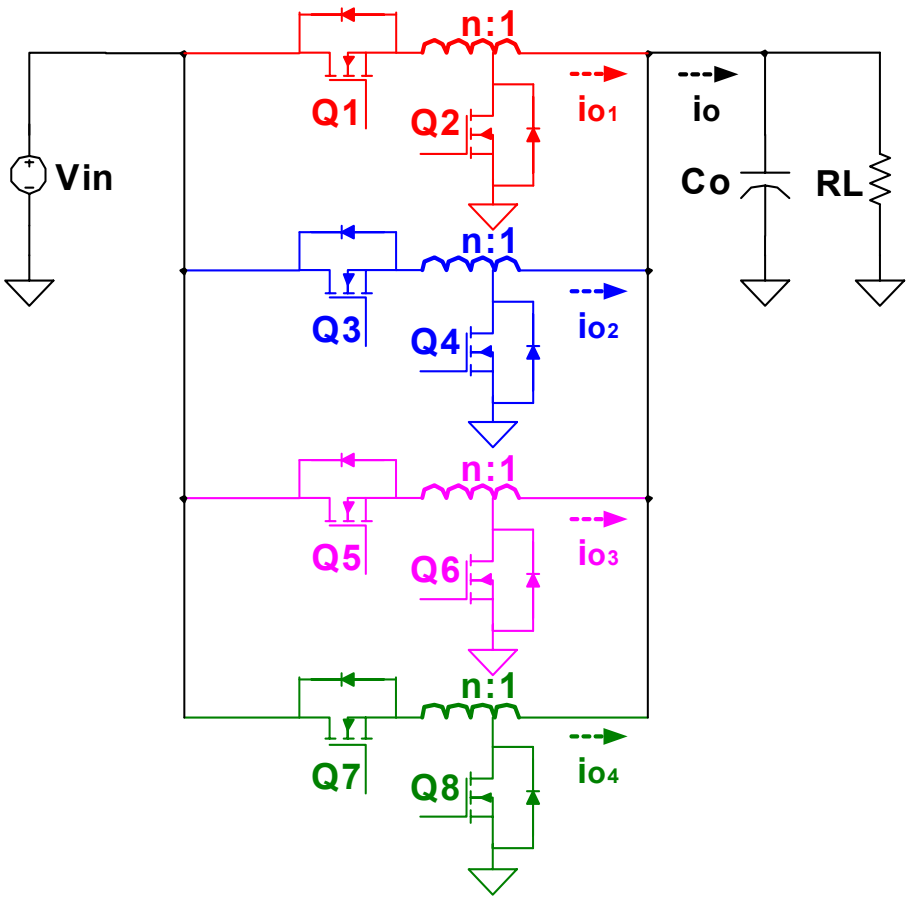
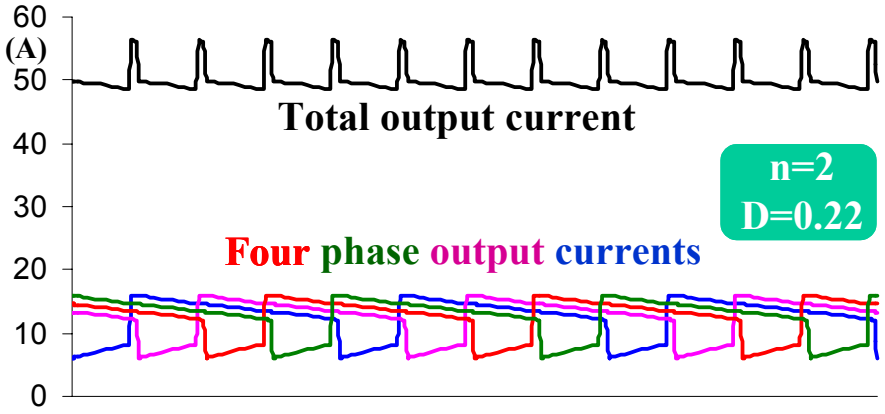
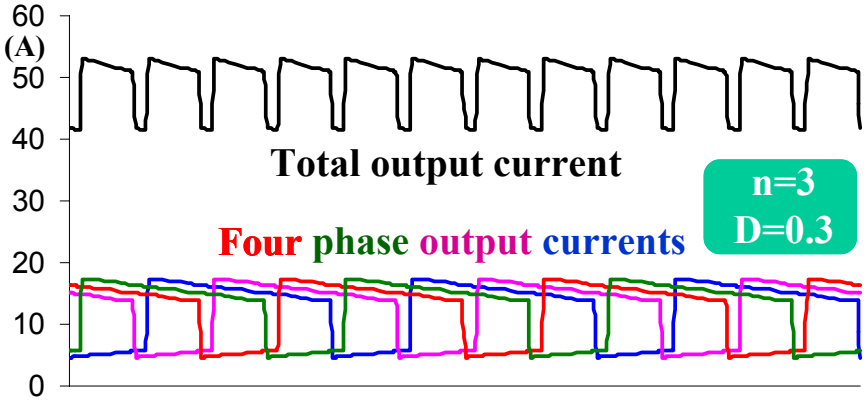


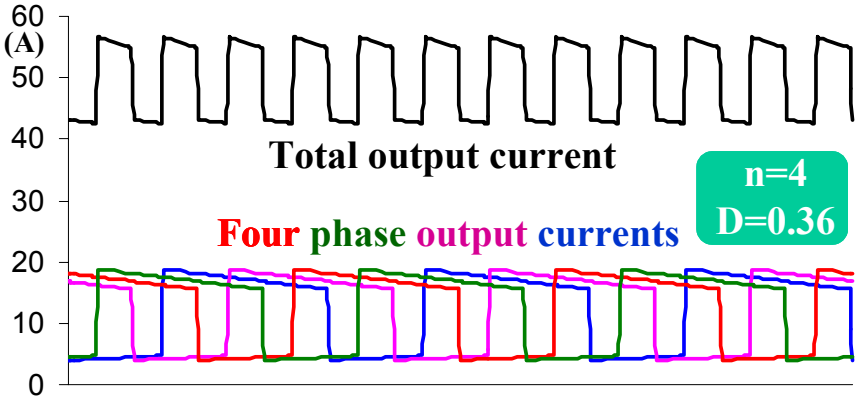
Fig. 3.16. Four-phase interleaving tapped-inductor buck converter.



(a)



(b)



(c)

Fig. 3.17. Examples of output ripple cancellation of the four-phase interleaving tapped-inductor buck when V_{in}=12V, V_o=1.5V, I_o=50A, and L=300nH/phase:
(a) *n=2; D=0.22, (b) n=3; D=0.3, and (c) n=4; D=0.36*

Fig. 3.18. Output ripple cancellation as a function of *n* and *D*.

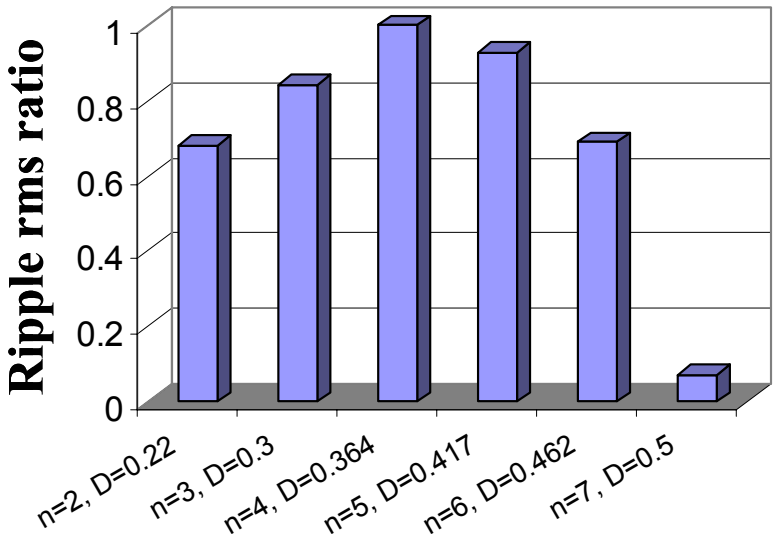
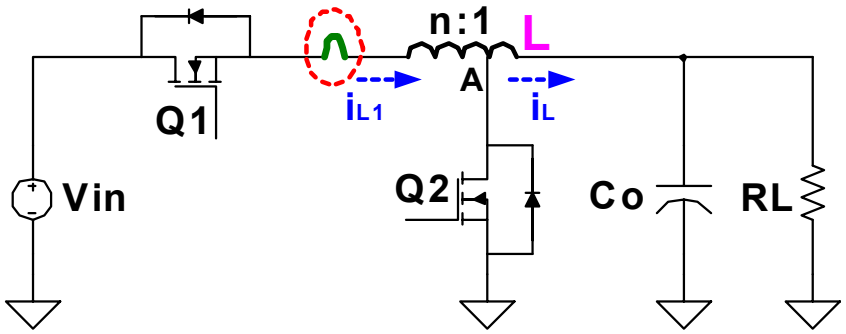


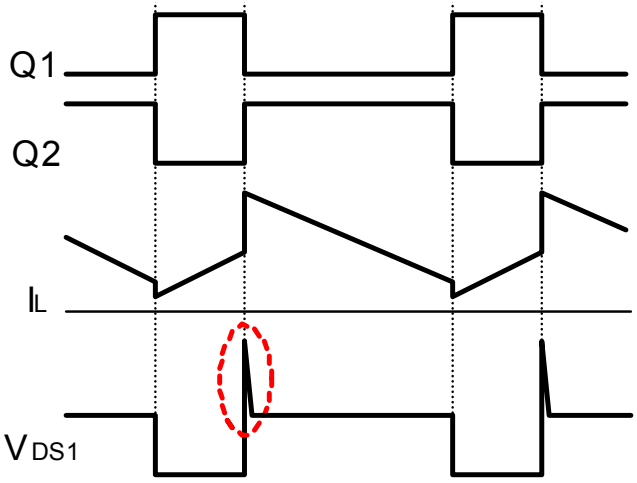
Fig. 3.19. Four-phase ripple cancellation for different designs when V_{in}=12V, V_o=1.5V, and I_o=50A.

3.7. Leakage Inductance Causes Issue in the Tapped-Inductor Buck Converter

In practice, the tapped-inductor structure always has some leakage inductance, shown by the circled area in Fig. 3.20(a). The energy stored in the leakage inductance causes a voltage spike when the top switch turns off, as shown in Fig. 3.20(b).



(a)



(b)

Fig. 3.20. Leakage inductance of the tapped-inductor structure causes a voltage spike across the top switch: (a) Leakage inductance always exists in the tapped-inductor structure and (b) Leakage inductance causes a voltage spike

3.8. Experimental Results of Four-Phase Interleaving Tapped-Inductor Buck VRM

Using as a benchmark the buck VRM built in Chapter 2, a four-phase interleaving tapped-inductor buck VRM prototype is built to test the performance, and is compared with the buck. The design specifications are the same as those for the benchmark buck: $V_{in}=12V$, $V_o=1.5V$, $I_o=50A$, and $f_s=300KHz/phase$. The turns ratio is $n=2$, which means this is a center-tapped structure.

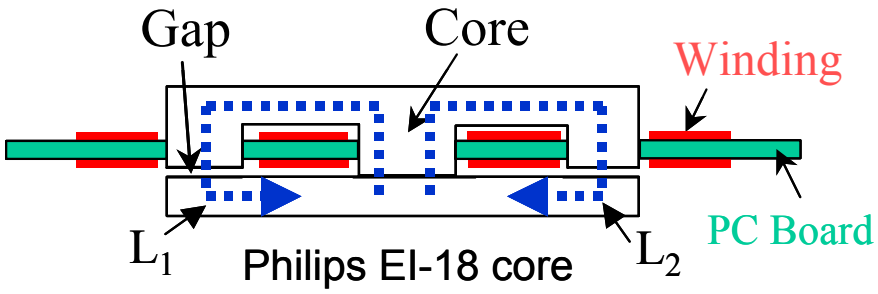
For the tapped-inductor buck, as discussed before, the dominant losses are the top switch switching loss and the bottom switch conduction loss. So the device optimization criteria are the same. Since switching loss dominates the top switch loss, devices with less gate charge, which are capable of switching fast, are preferred. The same devices as used in the buck VRM are used here: The top switches use the Si4884DY, which has a $10.5m\Omega$ on-resistance and a $15.3nC$ gate charge; on the other hand, the fact that conduction loss dominates the bottom switch loss makes lower on-resistance devices better candidates for bottom switches. The power devices used for bottom are the Si4874DY, which has a $7.5m\Omega$ on-resistance and a $35nC$ gate charge.

The choice of inductance considers both transient response and efficiency. L_{ct2} is only a function of V_o, I_o and ω_c, which here are all same as those of the buck. The L_{ct2} here is also the same as the L_{ct2} in the buck. In an $n=2$ tapped-inductor buck, it is still the step-down transient response that dominates the transient voltage deviation. Thus the choice of $L=L_{ct2}=300nH/phase$ is the largest inductance that yields the best transient response. The inductor is still implemented with Philips EI-18 planar cores and PCB

windings. The integrated magnetics technique is also employed here. Fig. 3.21 shows the structure. Air gaps are put on outer legs and there is no air gap on the center leg. In this way, two inductors are built in one EI core. The structure is also designed such that the DC fluxes of the two inductors are added in the center leg. Because these two inductors belong to two 180° interleaved phases, their AC fluxes get canceled in the center leg. This reduces the core loss.

The output capacitors are *6×1200uF* OSCON capacitors plus *18×22uF* ceramic capacitors.

A photograph of the prototype is in Fig. 3.22. Test waveforms are given in Fig. 3.23. The leakage inductance obviously causes a huge voltage spike on the top switch. Even when the 30V MOSFETs are used, the top switches do not survive at full load. The measured efficiency is plotted in Fig. 3.24. The tapped-inductor buck does improve the efficiency. But the level of full-load efficiency is not available due to device failure.



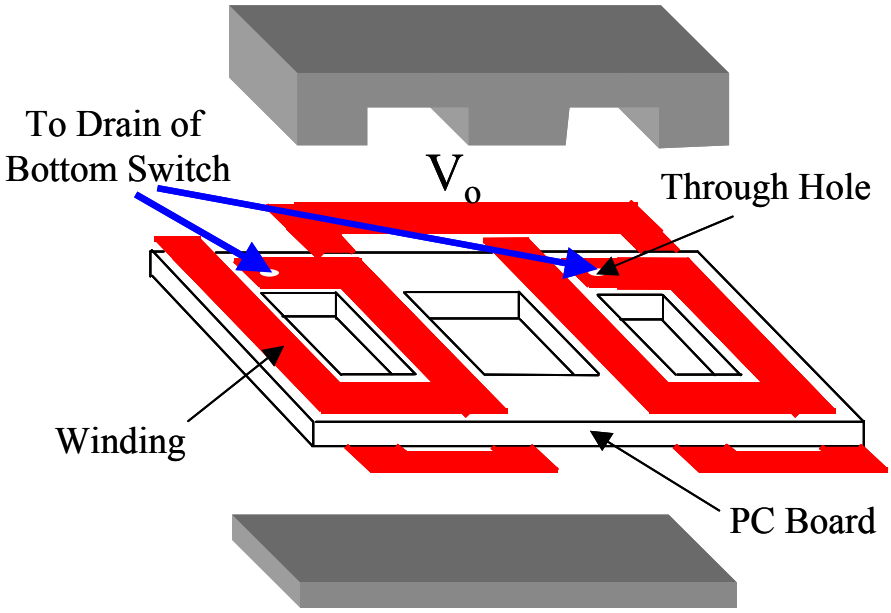


Fig. 3.21. Implementation of the magnetic structure.

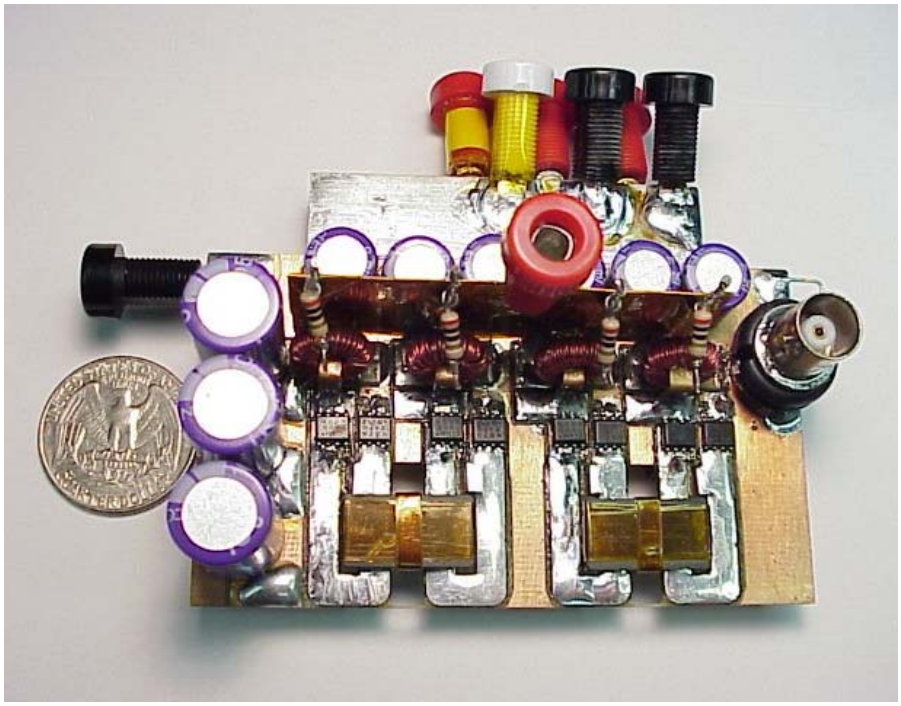


Fig. 3.22. Photograph of the four-phase interleaving tapped-inductor buck VRM prototype.

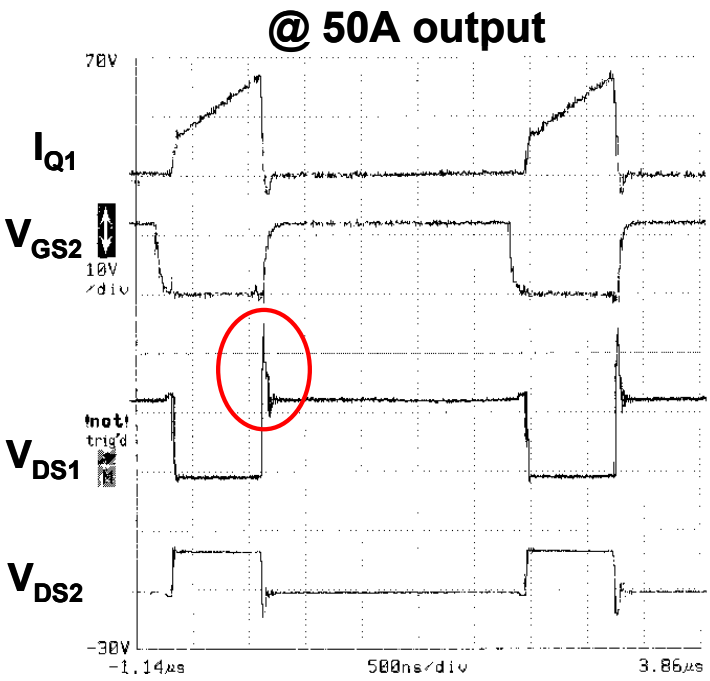


Fig. 3.23. Test waveforms of the tapped-inductor buck VRM.

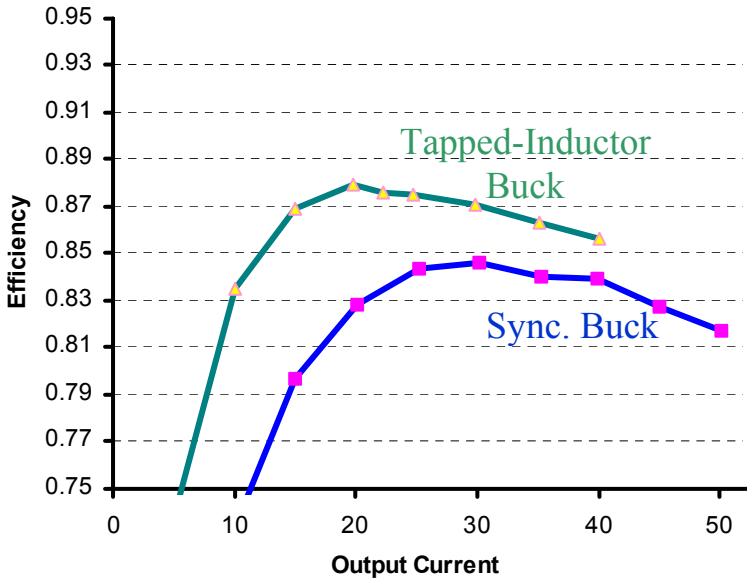


Fig. 3.24. Measured efficiency of the tapped-inductor buck VRM.

3.9. Summary

Compared with the buck, the tapped-inductor buck extends the duty cycle. Its larger turns ratio n yields a larger duty cycle.

In the tapped-inductor buck, L_{ct2} is the same as in the buck converter, but L_{ct1} decreases when n increases. When $L_{ct1} \geq L_{ct2}$, the transient response remains the same; when $L_{ct1} < L_{ct2}$, the transient response worsens.

With its extended duty cycle, the tapped-inductor buck can improve efficiency.

Interleaving can help cancel the output ripple. The effectiveness of the ripple cancellation is a function of the duty cycle, but is NOT a function of turns ratio n.

The tapped-inductor buck has a moving RHP zero. This zero impairs the stability of the system. When n or L becomes too large, the zero will move to such a low frequency that it prevents a wide control bandwidth from being achieved.

The leakage inductance introduces a detrimental voltage spike on the top switch.

Chapter 4.

High-Input-Voltage Non-Isolated VRM

— Multi-Phase Interleaving Active-Clamp Couple-Buck VRM

4.1. Active-Clamp Couple-Buck Converter

In the previous chapter, the tapped-inductor buck exhibited higher efficiency than the buck. It is an attractive candidate for 12V VRMs. But the leakage inductance causes a huge voltage spike on the top switch, thus removing this possibility of its use.

Solutions to this leakage problem could involve a snubber or a clamping circuit. One idea is to interleave two phases and let them help each other. To better explain this idea, an equivalent version of the tapped-inductor buck is introduced. Returning to the equivalent circuits shown in Fig. 3.3, it is easy to understand that the equivalent circuit shown in Fig. 4.1 has the same function as the original tapped-inductor buck. Based on this equivalent circuit, a clamping capacitor denoted as *Cc* is put across the two phases to clamp the voltage spike caused by the leakage inductance, as shown in Fig. 4.2. However, there is a serious problem in this configuration. The voltage across *Cc* is shown in Fig. 4.3. This voltage pulses, which means there is a huge circulating current flowing through the capacitor. This is unacceptable.

To obtain a constant voltage across *Cc*, one more modification is made to the configuration in Fig. 4.3. Another winding, which is coupled to the other phase, is put in anti-series with the original winding. The new configuration is shown in Fig. 4.4(a). L_{a3}

and L_{b3} are two additional windings. Since clamping capacitor *Cc* is put across node "A" and node "B," its voltage is

$$V_c = V_A - V_B = V_{in} + V_{La3} + V_{Lb1} - V_{Lb3} - V_{La1} - V_o . \tag{4.1}$$

Due to the good coupling, there are always

$$V_{La1} = V_{La3} \text{ and } V_{Lb1} = V_{Lb3} . \tag{4.2}$$

Therefore,

$$V_c = V_{in} - V_o . \tag{4.3}$$

This means that the clamping capacitor voltage is a constant determined by the input and output voltages.

The new circuit shown in Fig. 4.4(a) is called the active-clamp couple-buck [18][24][30]. Fig. 4.4(b) shows its operation waveform. The voltage gain is

$$\frac{V_o}{V_{in}} = \frac{D}{n + D} . \tag{4.4}$$

With properly designed turns ration *n*, the duty cycle can be a more favorable value than that of the buck. Fig. 4.5 shows the duty cycle comparison between the buck and the active-clamp couple-buck. A larger *n* further extends the duty cycle. Fig. 4.6 is an example showing the duty cycles of the buck, the *n=2* tapped-inductor buck and the *n=2* active-clamp couple-buck. In a design of a 12V-input, 1.5V-output, the buck is *D=0.125*, the tapped-inductor buck is *D=0.222*, and the active-clamp couple-buck is *D=0.286*. With the same turns ratio *n*, the active-clamp couple-buck can extend the duty cycle more than the tapped-inductor buck.

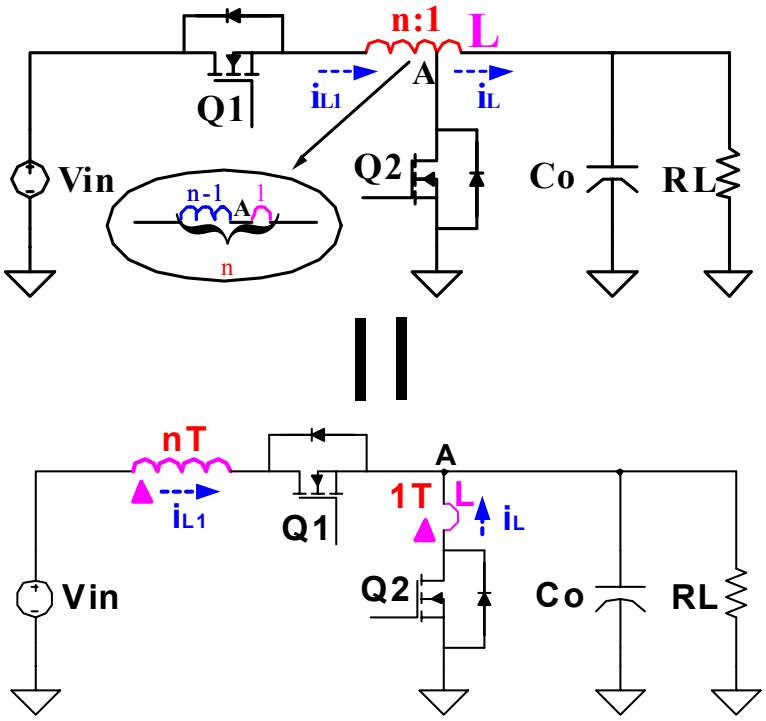


Fig. 4.1. An equivalent version of the original tapped-inductor buck.

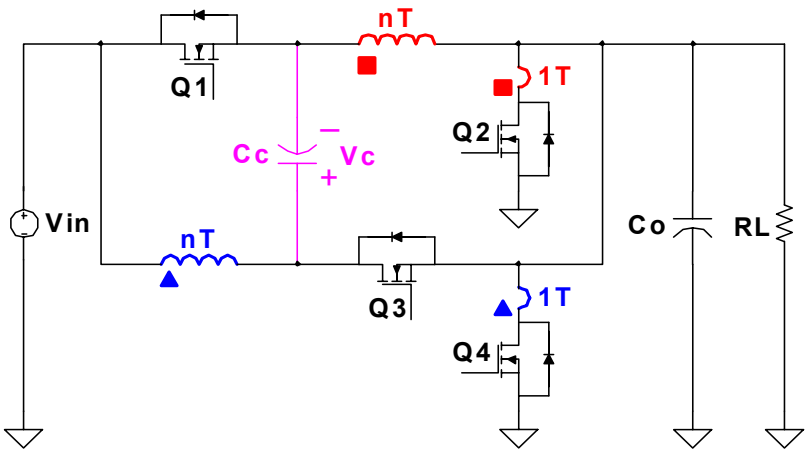


Fig. 4.2. A two-phase interleaving tapped-inductor buck with a clamping capacitor.

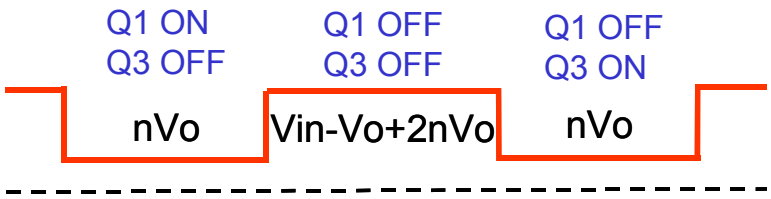
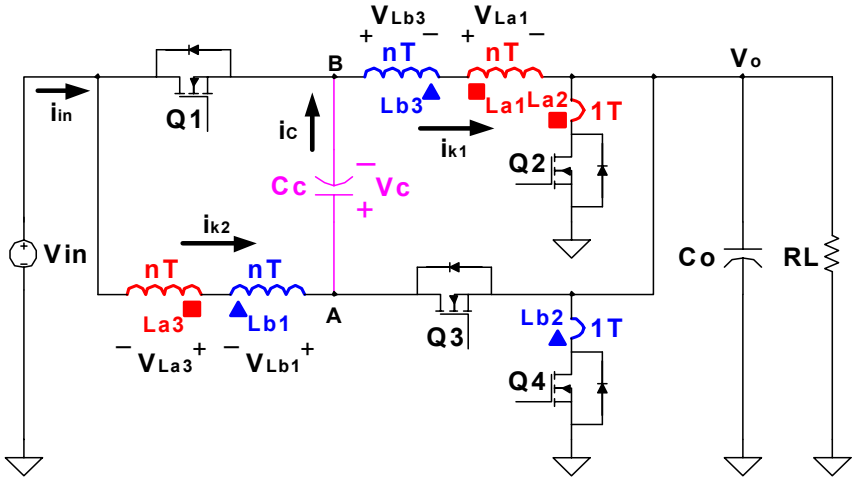
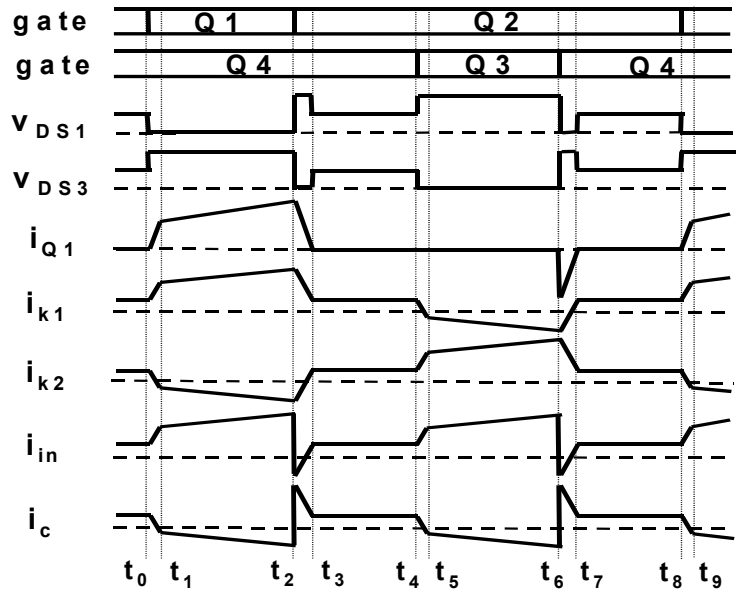


Fig. 4.3. Pulsating voltage across the clamping capacitor.



(a)



(b)

$$\frac{V_o}{V_{in}} = \frac{D}{n + D}$$

(c)

Fig. 4.4. Active-clamp couple-buck converter and its operation principles: (a) active-clamp couple-buck, (b) operation principles of the active-clamp couple-buck, and (c) voltage gain of the active-clamp couple-buck.

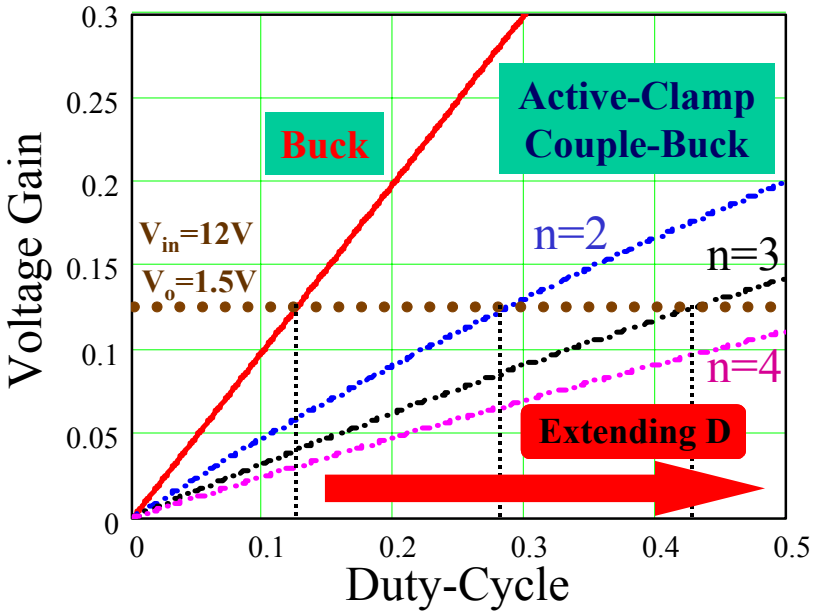


Fig. 4.5. Couple-buck extends the duty cycle.

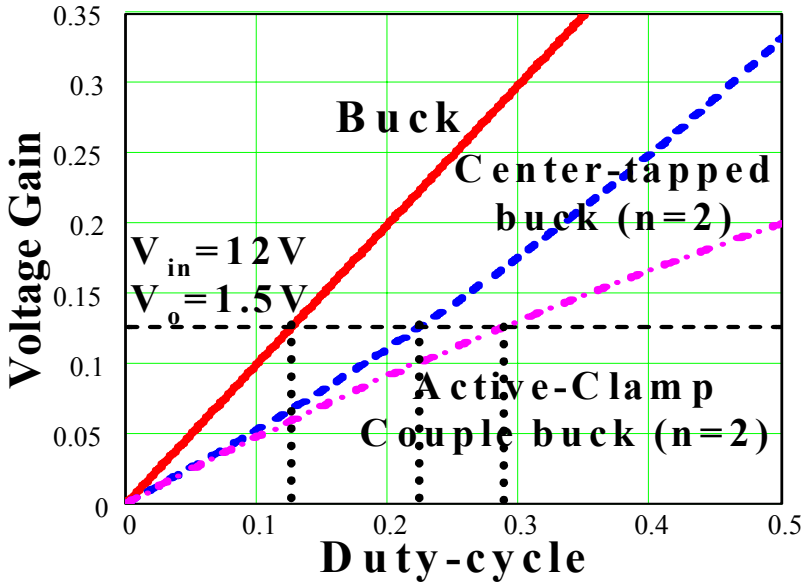


Fig. 4.6. Duty cycle comparison of buck, tapped-inductor buck and couple-buck.

4.2. Modeling of the Active-Clamp Couple-Buck Converter [19]

To study the dynamic performance of the active-clamp couple-buck, some modeling work is necessary. The equivalent circuit for modeling is shown in Fig. 4.7. L_1 and L_2 are the magnetizing inductors of the coupled windings; R_{L1} and R_{L2} are in series with the corresponding magnetizing inductors to represent the loss.

For simplicity, some reasonable assumptions are made in the modeling process: no leakage inductance; magnetizing inductances $L_1=L_2$; and $R_1=R_2$. Under the no-leakage-inductance assumption, only four time intervals exist — t_1~t_2, t_3~t_4, t_5~t_6, and t_7~t_8.

During t_1~t_2, the circuit behavior is shown in Fig. 4.8(a). The state equations are

$$\begin{cases} \dfrac{dv_{C1}}{dt} = \dfrac{1}{R_1C_1}v_{in} - \dfrac{1}{R_1C_1}v_{C1} - \dfrac{1}{R_1C_1}v_C \\ \dfrac{di_{L2}}{dt} = -\dfrac{1}{L}v_{in} + \dfrac{1}{L}v_C - \dfrac{R_L}{L}i_{L2} \\ \dfrac{di_{L1}}{dt} = -\dfrac{1}{L}v_{in} + \dfrac{n+1}{nL}v_C - \dfrac{R_L}{L}i_{L1} \\ \dfrac{dv_C}{dt} = \dfrac{R+R_1}{RR_1C}v_{in} - \dfrac{1}{R_1C}v_{C1} - \dfrac{R+R_1}{RR_1C}v_C - \dfrac{n+1}{nC}i_{L1} - \dfrac{1}{C}i_{L2} \end{cases} . \quad (4.5)$$

During t_3~t_4, the circuit behavior is shown in Fig. 4.8(b). The state equations are

$$\begin{cases} \dfrac{dv_{C1}}{dt} = \dfrac{1}{R_1C_1}v_{in} - \dfrac{1}{R_1C_1}v_{C1} - \dfrac{1}{R_1C_1}v_C \\ \dfrac{di_{L2}}{dt} = -\dfrac{1}{L}v_{in} + \dfrac{1}{L}v_C \\ \dfrac{di_{L1}}{dt} = -\dfrac{1}{L}v_{in} + \dfrac{1}{L}v_C \\ \dfrac{dv_C}{dt} = \dfrac{R+R_1}{RR_1C}v_{in} - \dfrac{1}{R_1C}v_{C1} - \dfrac{R+R_1}{RR_1C}v_C - \dfrac{n+1}{nC}i_{L1} - \dfrac{1}{C}i_{L2} \end{cases} . \quad (4.6)$$

During t_5~t_6, the circuit behavior is shown in Fig. 4.8(c). The state equations are

$$\begin{cases} \dfrac{dv_{C1}}{dt} = \dfrac{1}{R_1C_1}v_{in} - \dfrac{1}{R_1C_1}v_{C1} - \dfrac{1}{R_1C_1}v_C \\ \dfrac{di_{L2}}{dt} = -\dfrac{1}{L}v_{in} + \dfrac{n+1}{nL}v_C - \dfrac{R_L}{L}i_{L2} \\ \dfrac{di_{L1}}{dt} = -\dfrac{1}{L}v_{in} + \dfrac{1}{L}v_C - \dfrac{R_L}{L}i_{L1} \\ \dfrac{dv_C}{dt} = \dfrac{R+R_1}{RR_1C}v_{in} - \dfrac{1}{R_1C}v_{C1} - \dfrac{R+R_1}{RR_1C}v_C - \dfrac{1}{C}i_{L1} - \dfrac{n+1}{nC}i_{L2} \end{cases} . \quad (4.7)$$

Time interval t_7~t_8 is the same as t_3~t_4.

Assume the switching period is T_s, the duty cycle is defined as

$$D = \frac{t_2 - t_1}{T_s} \ ; \quad (4.8)$$

then

$$t_4 - t_3 = (\frac{1}{2} - D)T_s , \quad (4.9)$$

$$t_6 - t_5 = DT_s , \text{ and} \quad (4.10)$$

$$t_8 - t_7 = (\frac{1}{2} - D)T_s . \quad (4.11)$$

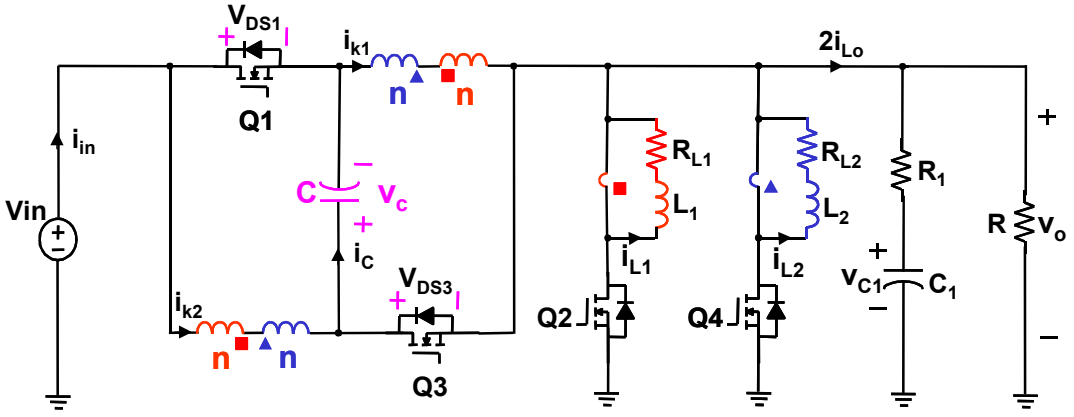
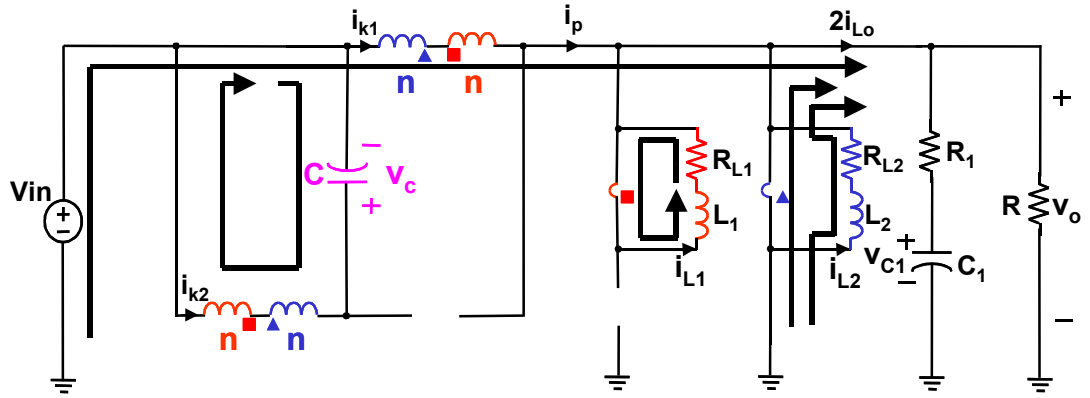
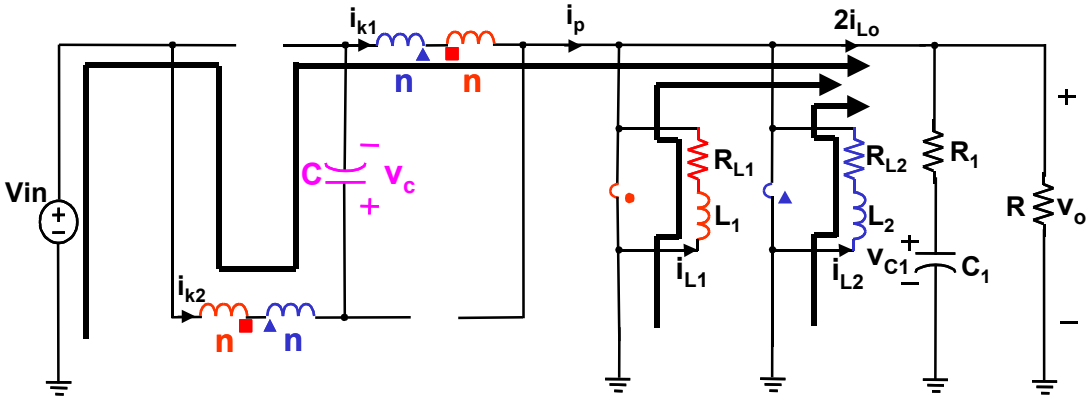


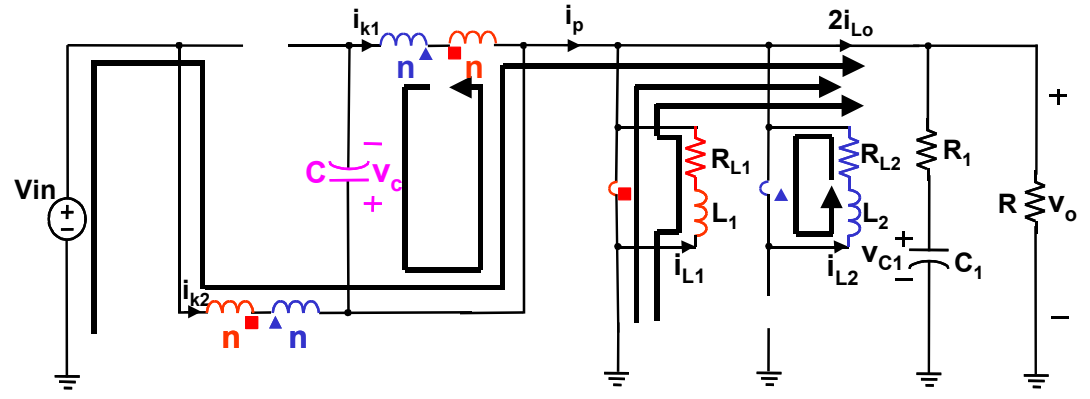
Fig. 4.7. Equivalent circuit for couple-buck modeling.



(a)



(b)



(b)

Fig. 4.8. Equivalent circuits within each interval: (a) t_1~t_2, (b) t_3~t_4 and (c) t_5~t_6.

Using the state space averaging technique, the DC and small-signal AC model can be derived as follows

DC model

$$\begin{cases} V_{C1} = \dfrac{D(D+n)R}{n^2 R_L/2 + (D+n)^2 R} \cdot V_{in} \\ V_C = \dfrac{n^2 R_L/2 + n(D+n)R}{n^2 R_L/2 + (D+n)^2 R} \cdot V_{in} \\ I_{L1} = I_{L2} = I_L = \dfrac{nD/2}{n^2 R_L/2 + (D+n)^2 R} V_{in} = \dfrac{n}{2(D+n)} \cdot \dfrac{V_o}{R} \end{cases} \tag{4.12}$$

and

Small Signal AC model

$$\begin{cases} \dfrac{d\hat{\overline{v_{C1}}}}{dt} = -\dfrac{1}{R_1 C_1} \cdot \hat{\overline{v_{C1}}} - \dfrac{1}{R_1 C_1} \cdot \hat{\overline{v_C}} \\ \dfrac{d\hat{\overline{i_{L2}}}}{dt} = \dfrac{D+n}{nL} \cdot \hat{\overline{v_C}} + \dfrac{V_C}{nL} \cdot \hat{\overline{d}} - \dfrac{R_L}{L} \cdot \hat{\overline{i_{L2}}} \\ \dfrac{d\hat{\overline{i_{L1}}}}{dt} = \dfrac{D+n}{nL} \cdot \hat{\overline{v_C}} + \dfrac{V_C}{nL} \cdot \hat{\overline{d}} - \dfrac{R_L}{L} \cdot \hat{\overline{i_{L1}}} \\ \dfrac{d\hat{\overline{v_C}}}{dt} = -\dfrac{1}{R_1 C} \cdot \hat{\overline{v_{C1}}} - \dfrac{R+R_1}{RR_1} \cdot \hat{\overline{v_C}} - \dfrac{D+n}{nC} \cdot \hat{\overline{i_{L1}}} \\ \qquad\qquad - \dfrac{D+n}{nC} \cdot \hat{\overline{i_{L2}}} - \dfrac{I_{L1}+I_{L2}}{nC} \cdot \hat{\overline{d}} \end{cases} \tag{4.13}$$

To verify the small-signal AC model, the control-to-output voltage transfer function $G_{vd}(s)$ is taken as an example for discussion. From the model, it is not difficult to derive that

$$G_{vd}(s)=\frac{v_{C1}(s)}{d(s)}=\frac{\left[\frac{2(D+n)}{n^2sC(R_L+sL)}\cdot\frac{n^2R_L/2+n(D+n)R}{n^2R_L/2+(D+n)^2R}+\frac{1}{sC}\cdot\frac{D}{n^2R_L/2+(D+n)^2R}\right]}{\left(1+\frac{R+R_1}{sRR_1C}\right)(1+sR_1C_1)+\frac{2(D+n)^2(1+sR_1C_1)}{n^2sC(R_L+sL)}-\frac{1}{sR_1C}}V_{in}, \quad (4.14)$$

in which $i_L=i_{L1}=i_{L2}$, $I_L=I_{L1}=I_{L2}$.

When $R_L=0$, with the assumptions $R>>R_1$, $C_1>>C$ (in practice, they are true), the simplified model is developed as

$$G_{vd}(s)=\frac{n}{(D+n)^2}\cdot\frac{\left(1+\frac{s}{z_1}\right)\left(1+\frac{s}{z_2}\right)}{\left(1+\frac{s}{\omega_0Q}+\left(\frac{s}{\omega_0}\right)^2\right)\left(1+\frac{s}{\omega_1}\right)}V_{in}, \quad (4.15)$$

where

$$z_1=-\frac{1}{R_1C_1};\ z_2=-\frac{2(D+n)^2R}{DnL},$$

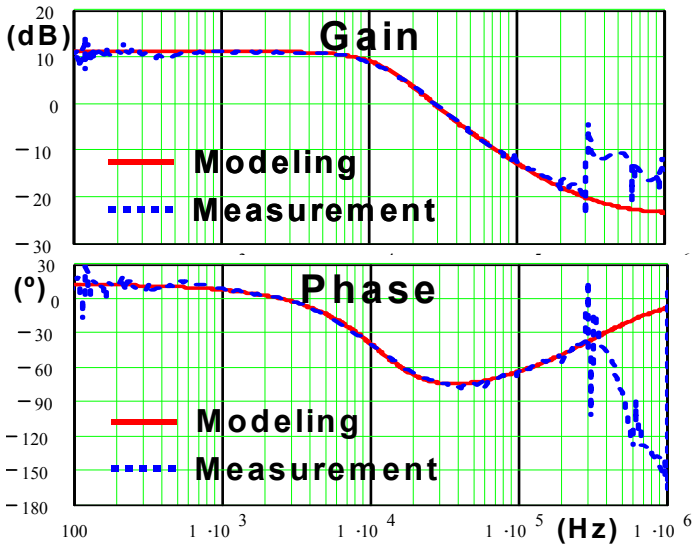
$$\omega_1=-\frac{1}{R_1C};\ \omega_0=\frac{D+n}{n}\sqrt{\frac{2}{LC_1}}, \text{ and}$$

$$Q=\frac{n}{D+n}\cdot\frac{1}{R_1}\cdot\sqrt{\frac{L}{2C_1}}.$$

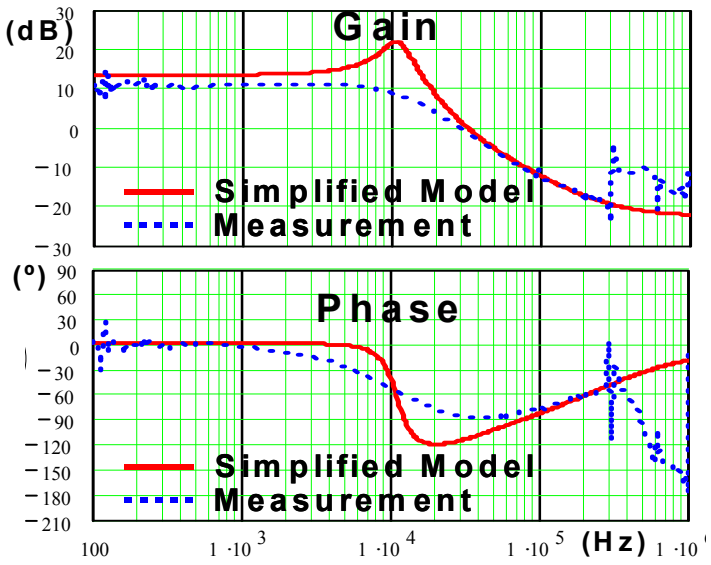
From the $G_{vd}(s)$ expression, there are three poles and two zeros. One pole comes from the clamping capacitor and the ESR of the output capacitor. In practice, this is a very high-frequency pole (in the order of tens of megahertz) so that it does not affect the

frequency range of interest. There is also a double pole. This double pole moves as a function of the output inductance, the output capacitance and the duty cycle, but not as a function of the load. Of the two zeros, one is the ESR zero introduced by the output capacitor, and the other is an interesting left-half-plane (LHP) moving zero. Normally moving is undesirable, but left-plane zeros are good for system design. In this case, this LHP moving zero is a function of duty cycle and load. When the load grows heavier, it moves to a lower frequency, which provides greater margins. Thus, the active-clamp couple-buck not only solves the voltage spike issue, but also is suitable for wide bandwidth design.

The measured $G_{vd}(s)$ is compared with the theoretical predication given in Fig. 4.9. The results match very closely.



(a)



(b)

Fig. 4.9. Modeled and measured $G_{vd}(s)$: (a) Accurate model vs. measurement and (b) Simplified model vs. measurement.

4.3. Critical Inductances of the Active-Clamp Couple-Buck Converter

In Formula (4.13), due to the symmetry of the circuit, it is reasonable to assume that

$$\frac{d\hat{\overline{i_L}}}{dt} = \frac{d\hat{\overline{i_{L1}}}}{dt} = \frac{d\hat{\overline{i_{L2}}}}{dt} \tag{4.16}$$

For simplicity, in the following analysis, $R_L = 0$ is also taken as an assumption. Therefore, the average current slew rate is

$$\frac{d\hat{\overline{i_L}}}{dt} = \frac{V_C}{nL} \cdot \hat{\overline{d}} . \tag{4.17}$$

From the DC model, it is already known that

$$V_C = \frac{n}{D+n} \cdot V_{in} . \tag{4.18}$$

So,

$$\frac{d\hat{\overline{i_L}}}{dt} = \frac{V_{in}}{(D+n)L} \cdot \hat{\overline{d}} . \tag{4.19}$$

The output current of the couple-buck is denoted in Fig. 4.7 as $2i_{Lo}$. Since the couple-buck is actually a two-phase interleaving configuration, i_{Lo} is the equivalent per-phase output current. Due to the coupled-inductor structure, it is easy to derive the following:

During t_1~t_2, according to the equivalent circuit shown in Fig. 4.8(a)

$$\overline{i_p} = \frac{1}{n} \cdot \overline{i_{L1}} + C \cdot \frac{d\overline{v_C}}{dt} . \tag{4.20}$$

During t_3~t_4, according to the equivalent circuit shown in Fig. 4.8(b)

$$\overline{i_p} = C \cdot \frac{d\overline{v_C}}{dt} . \tag{4.21}$$

During t_5~t_6, according to the equivalent circuit shown in Fig. 4.8(c)

$$\overline{i_p} = \frac{1}{n} \cdot \overline{i_{L2}} + C \cdot \frac{d\overline{v_C}}{dt} . \tag{4.22}$$

Time interval t_7~t_8, is the same as t_3~t_4.

State-space averaging of Equations (4.27) through (4.22) reveals that

$$\overline{i_p} = \frac{D}{n} \cdot \overline{i_{L1}} + \frac{D}{n} \cdot \overline{i_{L2}} + C \cdot \frac{d\overline{v_C}}{dt} = \frac{2D}{n} \cdot \overline{i_{L2}} + C \cdot \frac{d\overline{v_C}}{dt} . \tag{4.23}$$

Then

$$\overline{i_{Lo}} = \frac{1}{2}\cdot\left(\overline{i_{L1}} + \overline{i_{L2}} + \overline{i_p}\right) = \frac{D+n}{n}\cdot\overline{i_L} + \frac{1}{2}\cdot C\cdot\frac{d\overline{v_C}}{dt}. \tag{4.24}$$

Small perturbation to Equation (4.24), and assuming v_C is a constant, then

$$\overline{i_{Lo}} \approx \frac{D+n}{n}\cdot\overline{i_L}, \tag{4.25}$$

so

$$\frac{d\hat{\overline{i_{Lo}}}}{dt} = \frac{D+n}{n}\cdot\frac{d\hat{\overline{i_L}}}{dt}. \tag{4.26}$$

Substituting Equation (4.17) into Equation (4.26),

$$\frac{d\hat{\overline{i_{Lo}}}}{dt} = \frac{D+n}{n}\cdot\frac{d\hat{\overline{i_L}}}{dt} = \frac{V_{in}}{nL}\cdot\hat{\overline{d}}. \tag{4.27}$$

Equation (4.27) is the control-determined equivalent output average current slew rate. From the power stage point of view, according to Equation (2.2), when the duty cycle is not saturated, the output inductor current slew rate is

$$\frac{d\hat{\overline{i_{Lo}}}}{dt} = \frac{\Delta I_o\cdot\omega_c}{\pi/2} \tag{4.28}$$

By equalizing Equation (4.27) and Equation (4.28), the transient duty cycle increase (when not saturated) is obtained as follows:

$$\Delta D = \frac{n\cdot\Delta I_o\cdot\omega_c}{(\pi/2)\cdot V_{in}}\cdot L. \tag{4.29}$$

Critical inductance is the value that makes the duty cycle nearly saturated during the transient response. Therefore, from Equation (4.29), the maximum duty cycle increase is

$$\Delta D_{\max} = \frac{n \cdot \Delta I_o \cdot \omega_c}{(\pi/2) \cdot V_{in}} \cdot L_{ct} \tag{4.30}$$

Rewriting Equation (4.30), the critical inductance is

$$L_{ct} = \frac{(\pi/2) \cdot V_{in}}{n \cdot \Delta I_o \cdot \omega_c} \cdot \Delta D_{\max} . \tag{4.31}$$

Like the buck and the tapped-inductor buck, there are two critical inductances for the couple-buck; one is for step-up and the other is for step-down transient response. Following the previous definitions for the buck converter, L_{ct1} stands for step-up critical inductance and L_{ct2} stands for step-down critical inductance.

During the step-down transient response, the maximum duty cycle change is the steady-state value, which is

$$D_{\max 2} = D = \frac{n \cdot V_o}{V_{in} - V_o} . \tag{4.32}$$

Substituting Equation (4.32) into Equation (4.31), the result is that

$$L_{ct2} = \frac{(\pi/2) \cdot V_o}{\Delta I_o \cdot \omega_c} \cdot \frac{V_{in}}{V_{in} - V_o} . \tag{4.33}$$

Compared with the buck's and the tapped-inductor buck's level of the L_{ct2}, the couple-buck's L_{ct2} is modified by a factor $\frac{V_{in}}{V_{in} - V_o}$, which makes it slightly larger. It is still a function of the design specs, NOT a function of n.

To calculate the step-up inductance L_{ct1}, it is taken into consideration that the couple-buck does not allow the top switch to work at a duty cycle greater than *0.5*. So during the step-up transient response, the maximum duty cycle change is *0.5-D*, that is

$$D_{\max 1} = 0.5 - D = 0.5 - \frac{n \cdot V_o}{V_{in} - V_o} = \frac{0.5V_{in} - (n + 0.5)V_o}{V_{in} - V_o} . \tag{4.34}$$

Substituting Equation (4.34) into Equation (4.31), the result is

$$L_{ct1} = \frac{(\pi/2)\cdot V_o}{\Delta I_o \cdot \omega_c} \cdot \frac{0.5V_{in}^{\ 2} - (n+0.5)\cdot V_{in}\cdot V_o}{n\cdot\left(V_{in}\cdot V_o - V_o^{\ 2}\right)}. \tag{4.35}$$

From the trend shown by Equations (4.33) and (4.35), n modifies the critical inductances in the way illustrated in Fig. 4.10. Actually, it is very similar to the tapped-inductor buck. The solid line stands for a larger n case than the case the dotted line stands for. When n goes up, L_{ct2} remains constant and L_{ct1} goes down. Something different is that due to the "*0.5*" duty cycle limit, with similar steady-state duty cycle, the couple-buck has a smaller L_{ct1} than the tapped-inductor buck. Fig. 4.11 gives an example that shows the difference.

To verify the critical inductance in the couple-buck, some switching mode simulations are done with different levels of inductance L and the same control bandwidth ω_c. Fig. 4.12 shows the simulated transient voltage deviation for an $n=2$ couple-buck converter, with the listed design specs. Calculation based on Formula (4.33) predicts that $L_{ct2}=342nH$, and calculation based on Formula (4.35) predicts that $L_{ct1}=256nH$. In Fig. 4.12, it is seen that the simulation results match the prediction.

For comparison, simulation results of the buck converter and the $n=2$ tapped-inductor buck converter are also included in this discussion. All the simulations are done with the same control bandwidth ω_c. Fig. 4.13 shows the step-down transient response. It is seen that with the same design specs, all three converters have almost the same L_{ct2}. Fig. 4.14 shows the step-up transient response. This time things are significantly different. The buck has a much larger L_{ct1} than L_{ct2}; the tapped-inductor buck has a

smaller L_{ct1} than that of the buck converter; due to the "*0.5*" duty cycle limit, the couple-buck has an even smaller L_{ct1}.

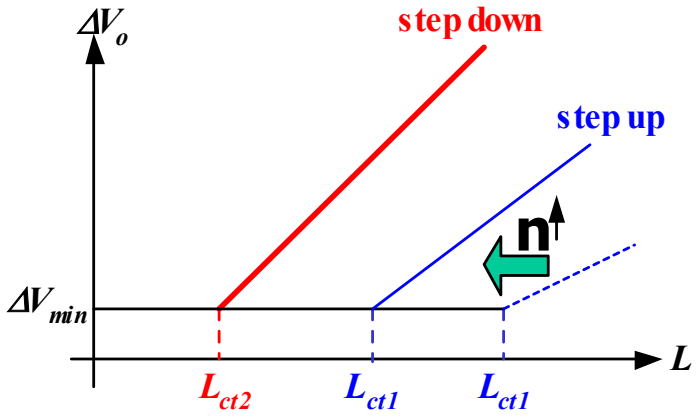


Fig. 4.10. Impact of turns ratio *n* on critical inductance.

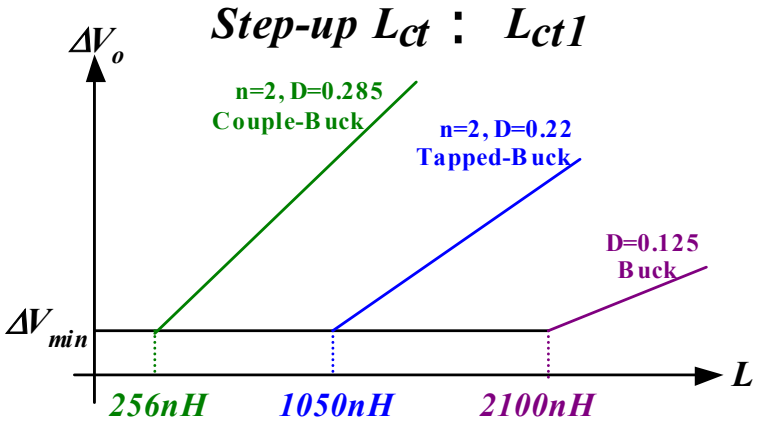
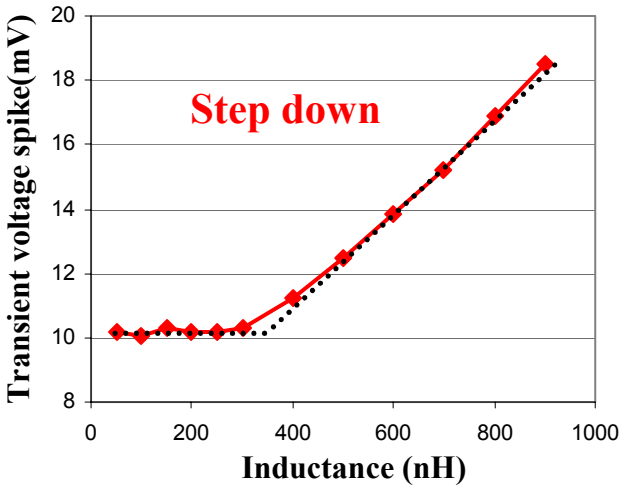
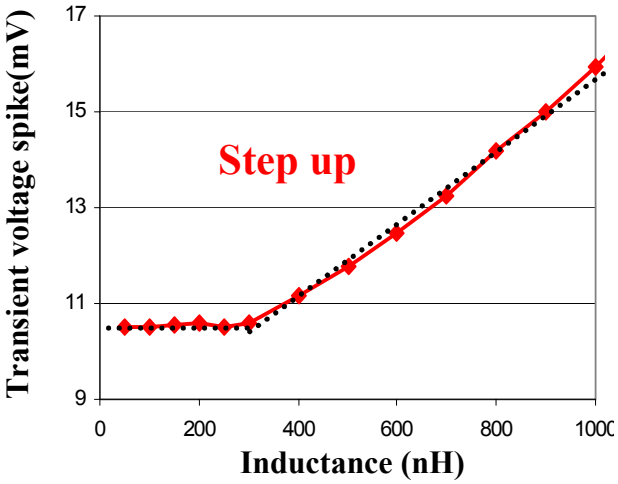


Fig. 4.11. Impact of "*0.5*"-duty-cycle-limit on L_{ct1} when V_{in}=12V, V_o=1.5V, I_o=12.5A/phase, ω_c=100KHz.



(a)



(b)

Fig. 4.12. Simulated transient voltage deviation of the couple-buck converter when V_{in}=12V, V_o=1.5V, I_o=12.5A/phase, ω_c=100KHz, L=300nH, C_o=1800μF/phase:
(a) For step down and (b) For step up.

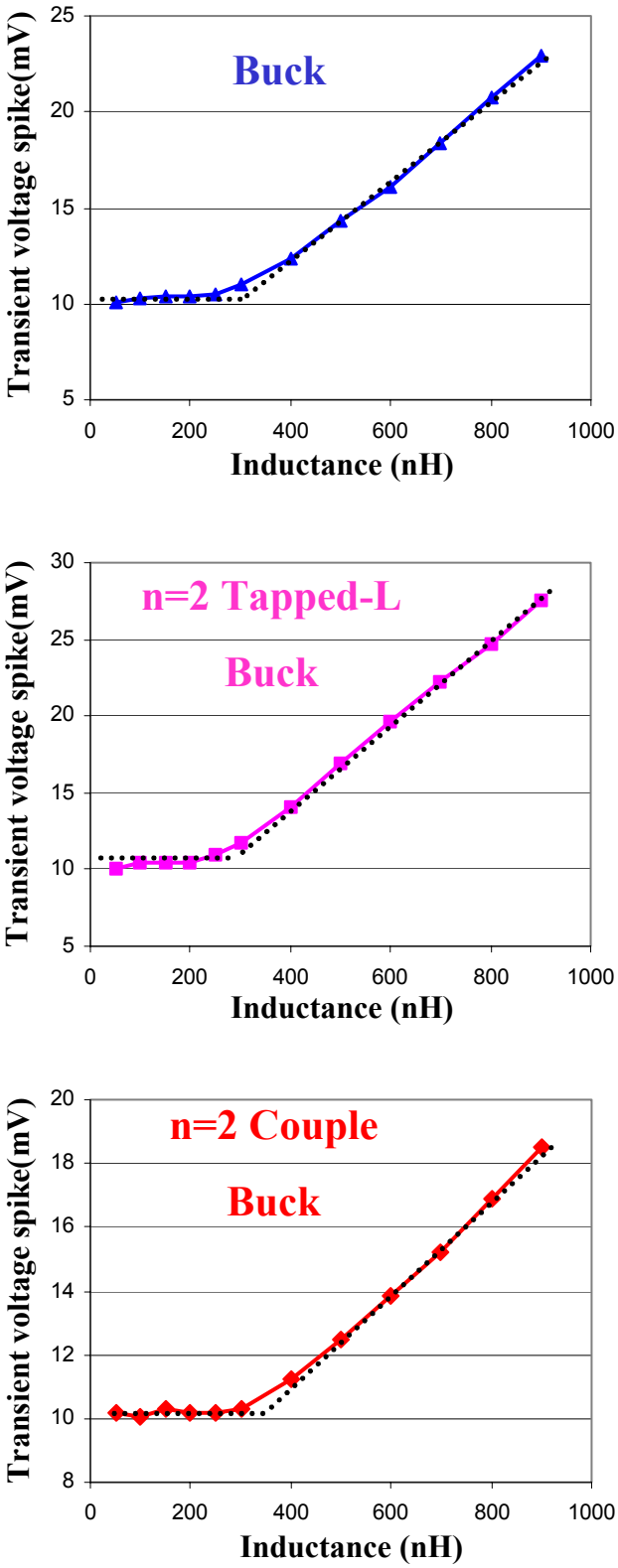


Fig. 4.13. Simulated step-down transient voltage deviation of three converters when V_{in}=12V, V_o=1.5V, I_o=12.5A/phase, ω_c=100KHz, L=300nH, and C_o=1800μF/phase.

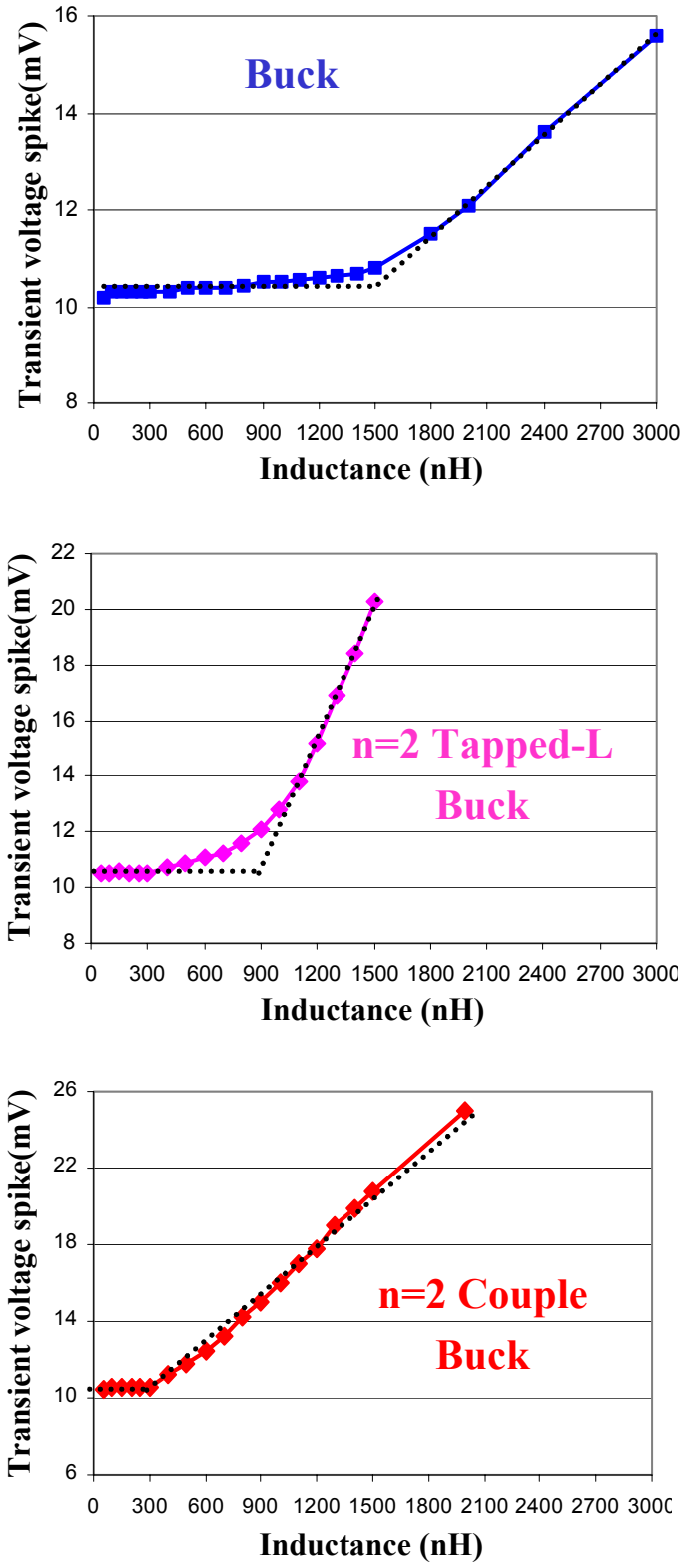


Fig. 4.14. Simulated step-up transient voltage deviation of three converters when V_{in}=12V, V_o=1.5V, I_o=12.5A/phase, ω_c=100KHz, L=300nH, and C_o=1800μF/phase.

There is an absolute condition that must be met in the couple-buck: The duty cycle cannot exceed 0.5. This condition is expressed as

$$\frac{nV_o}{V_{in}-V_o} \le 0.5, \tag{4.36}$$

rewritten as

$$n \le \frac{1}{2}\cdot\left(\frac{V_{in}}{V_o}-1\right). \tag{4.37}$$

This is the choice of n to make the couple-buck work.

As discussed in Chapter 3, when $L_{ct1} \ge L_{ct2}$ the transient response remains the same, but when $L_{ct1} < L_{ct2}$ the transient response becomes worse. The choice of n to get the best transient response satisfies $L_{ct1} \ge L_{ct2}$, so

$$\frac{(\pi/2)\cdot V_o}{\Delta I_o \cdot \omega_c}\cdot\frac{0.5{V_{in}}^2-(n+0.5)\cdot V_{in}\cdot V_o}{n\cdot\left(V_{in}\cdot V_o-{V_o}^2\right)} \ge \frac{(\pi/2)\cdot V_o}{\Delta I_o \cdot \omega_c}\cdot\frac{V_{in}}{V_{in}-V_o}, \tag{4.38}$$

which is

$$n \le \frac{1}{4}\left(\frac{V_{in}}{V_o}-1\right), \tag{4.39}$$

Since $\frac{1}{4}\cdot\left(\frac{V_{in}}{V_o}-1\right) < \frac{1}{2}\cdot\left(\frac{V_{in}}{V_o}-1\right)$, the choice of n based on Formula (4.39) automatically satisfies Formula (4.37). So when $n \le \frac{1}{4}\left(\frac{V_{in}}{V_o}-1\right)$, the best transient response is obtained.

In Fig. 4.15 is a design example. In this design case, when $n \le 2$, the transient response remains the same; when $n>2$, the transient response will be worse.

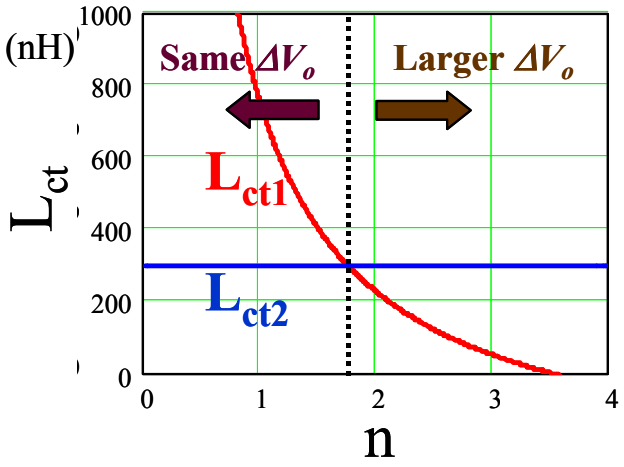


Fig. 4.15. Critical inductance from different choice of n when $V_{in}=12V$, $V_o=1.5V$, $I_o=12.5A/phase$, and $\omega_c=100KHz$.

4.4. Benefits Gained From the Extended Duty Cycle in Active-Clamp Couple-Buck

In a couple-buck converter, because the duty cycle is extended, the switch current waveforms are different from those in a buck converter. Fig. 4.15 shows the comparison of the buck, the $n=2$ tapped-inductor buck and $n=2$ couple buck converter switch current waveforms. With the most extended duty cycle, the couple buck has the most significantly reduced top switch turn-off current. This greatly reduces the top switch switching loss. The bottom switch current of the couple-buck has a different shape, which leads to a different RMS value. Among the three cases, the couple-buck has the largest bottom switch RMS current.

Different levels of n yield different amounts of device loss. As discussed in the previous chapters, the dominant losses are the top switch switching loss and the bottom switch conduction loss. Fig. 4.16 shows a design example. The loss estimation of each

valid design of n is shown in Fig. 4.16(a), and is compared with the buck converter. The result shows that the larger the n, the lower the top switch switching loss. However, when n grows, the bottom conduction loss increases. The total device loss estimation is shown in Fig. 4.16(b). A proper n does reduce the total loss. It is also identified that $n=2$ yields much better efficiency than $n=1$.

The choice of n is not only based on efficiency, but also on the consideration of transient response. In this design, when $n \le 2$, the transient response remains the same; when $n > 2$, the transient response will be worse.

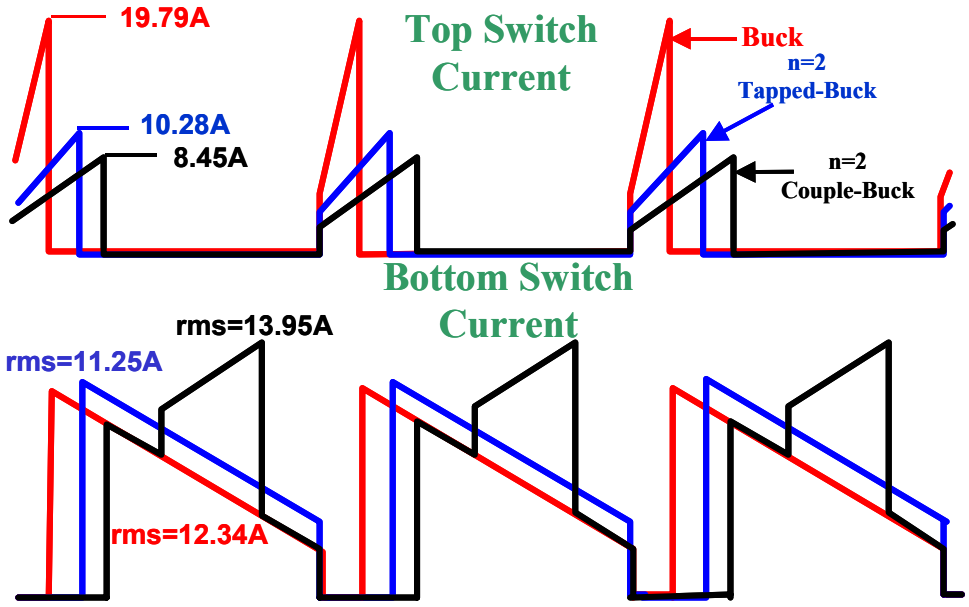
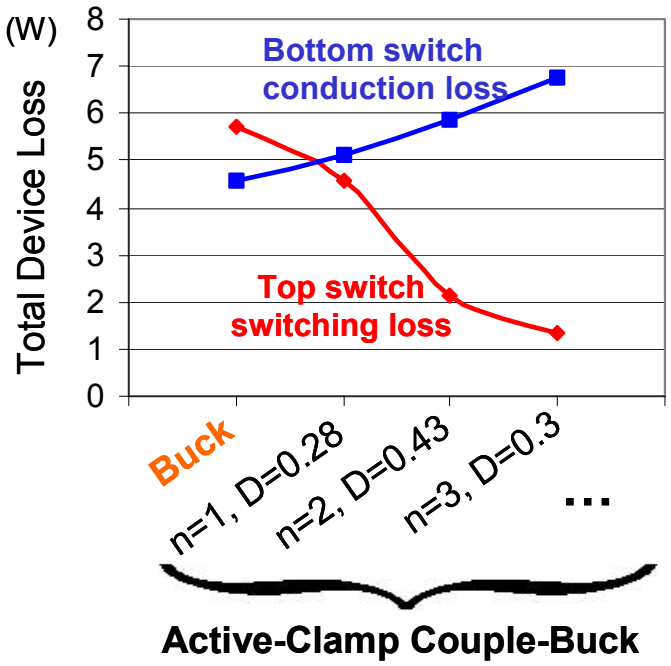
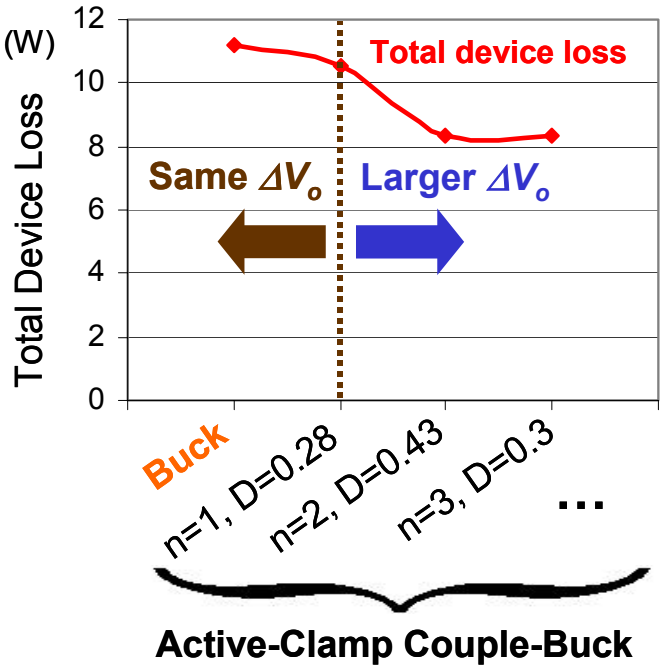


Fig. 4.15. Switch current waveforms comparison: buck, tapped-inductor buck and couple-buck.



(a)



(b)

Fig. 4.16. Active-clamp couple-buck major device loss as a function of *n* when V_{in}=12V, V_o=1.5V, I_o=12.5A, and L=300nH. *Top device: Si4884DY(10.5mΩ, 15.3nC) and bottom device: Si4874DY(7.5mΩ, 35nC:* (a) Top switch switching loss and bottom switch conduction loss and (b) Total device loss

4.5. Ripple Cancellation in the Multi-Phase Interleaving Active-Clamp Couple-Buck Converter

Interleaving helps achieve current ripple cancellation in the buck converter and the tapped-inductor buck converter. It also helps in the couple buck converter. When considering interleaving, there is something particular for the case of the couple-buck. A basic couple-buck, as shown in Fig. 4.4(a), has two phases. To interleave the couple buck, the total number of phases must be even. Fig. 4.17 shows a four-phase interleaving configuration. A basic cell of a couple-buck already has two interleaved phases. The output currents of these cells are defined as i_{o12} and i_{o34}, respectively; the total output current is i_o. With interleaving, i_o might achieve some ripple cancellation. To study the ripple cancellation in the couple-buck converter, the "ripple_ratio" is defined as the ratio of the i_o AC component RMS value and the i_{o12} *(or* i_{o34}*)* AC component RMS value, as expressed in Equation.4.40:

$$ripple\_ratio = \frac{rms\left(i_o\big|_{AC}\right)}{rms\left(i_{o12}\big|_{AC}\right)}. \tag{4.40}$$

Figs. 4.18(a) through 4.18(c) show three design examples. In all three cases, four-phase interleaving is used; $V_{in}=12V$, $V_o=1.5V$ and $I_o=50A$. The bottom two waveforms are i_{o12} and i_{o34}, and the top waveform is i_o. Among the three examples, i_o has different AC components. The current waveform could be a function of either the turns ratio n or the duty cycle *D*, or even both. Then, for designs with different *n* and different *D*, the effectiveness of the ripple cancellation could be very different.

For the couple buck, the ripple_ratio as a function of *D* is plotted in Fig. 4.19. Each curve in Fig. 4.19 corresponds to a different turns ratio from *n=1* to *n=3*. As

plotted, they are close curves. This result indicates that the ripple cancellation is approximately only a function of *D*, not a function of *n*. Compared with the buck whose four-phase interleaving effectiveness is shown in Fig. 2.22, the couple buck can achieve some ripple cancellation as well. But careful design is needed; otherwise the total output current ripple RMS value could be even larger than that of the one-phase current ripple rms value.

The design example (V_{in}=*12V,* V_o=*1.5V and* I_o=*50A*) is analyzed with four-phase interleaving and different levels of *n*. The effectiveness is shown in Fig. 4.20. From the result, it is seen that *n=2* cancels the ripple most effectively.

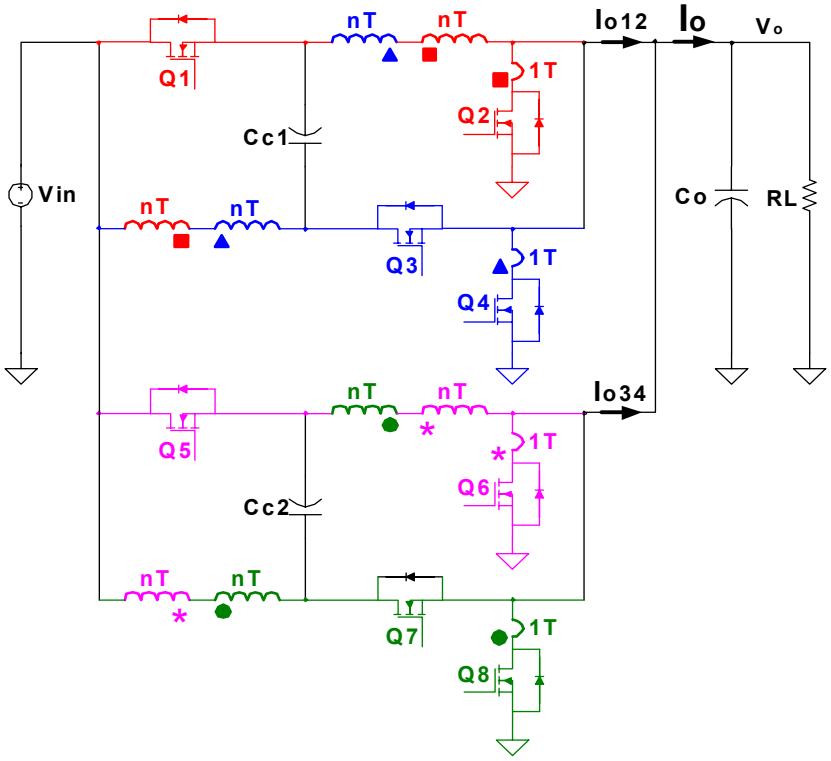
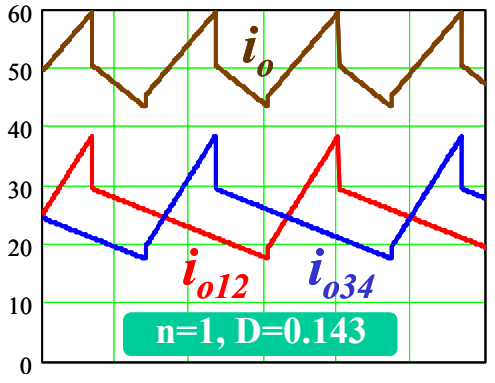
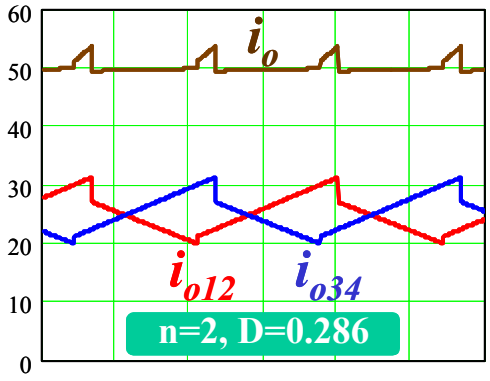


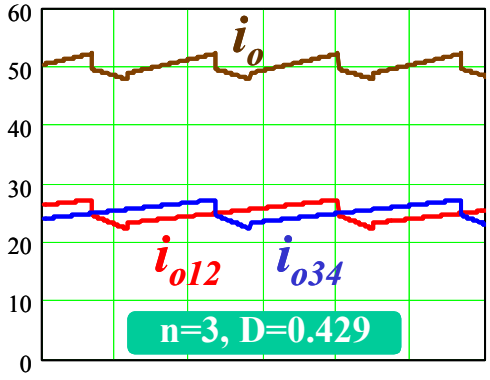
Fig. 4.17. Four-phase interleaving couple-buck converter.



(a)



(b)



(c)

Fig. 4.18. Examples of output ripple cancellation of the four-phase interleaving couple-buck when V_{in}=12V, V_o=1.5V, I_o=50A, L=300nH/phase: (a) n=1, D=0.143, (b) n=2, D=0.286 and (c) n=3, D=0.42.

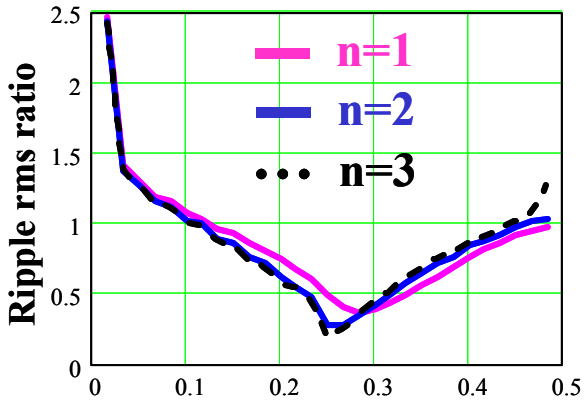


Fig. 4.19. Output ripple cancellation as a function of *n* and *D*.

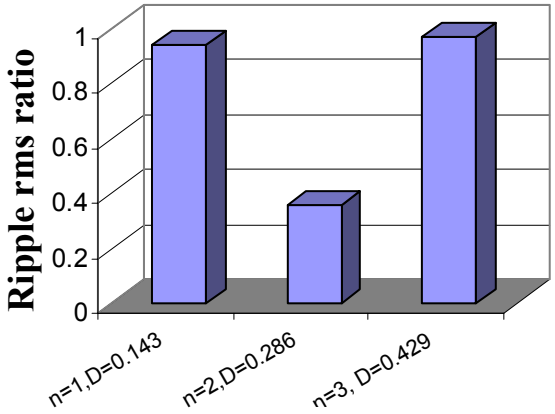


Fig. 4.20. Four-phase ripple cancellation for different designs when $V_{in}=12V$, $V_o=1.5V$, and $I_o=50A$.

4.6. Experimental Results of Four-Phase Interleaving Active-Clamp Couple-Buck VRM

Using as a benchmark the buck VRM built in Chapter 2, a four-phase interleaving active-clamp couple buck VRM prototype is built to test the performance and to be compared with the buck. The design specifications are the same as those for the benchmark: $V_{in}=12V$, $V_o=1.5V$, $I_o=50A$, and $f_s=300KHz/phase$. The turns ratio is $n=2$.

For the couple buck, as discussed before, the dominant losses are the top switch switching loss and the bottom switch conduction loss. So the device optimization criteria are the same. Since switching loss dominates the top switch loss, devices with less gate charge, which are capable of fast switching, are preferred. The same devices as used in the buck VRM are used here: The top switches are the Si4884DY, which has a 10.5mΩ on-resistance and a 15.3nC gate charge; on the other hand, the fact that conduction loss dominates the bottom switch loss makes lower on-resistance devices better candidates for bottom switches. The power devices here are the Si4874DY, which has a 7.5mΩ on-resistance and a 35nC gate charge.

The choice of inductance considers both transient response and efficiency. L_{ct2} is only a function of V_o, I_o and ω_c, which here are all same as those in the buck. The L_{ct2} here is also the same as the L_{ct2} in the buck. Because the transient response is symmetrical in an *n=2* couple-buck, the choice of $L=L_{ct2}=300nH/phase$ is the largest inductance that yields the best transient response. The inductor is still implemented with Philips EI-18 planar cores and PCB windings. The integrated magnetics technique is also employed here. Fig. 4.21 shows the structure. Air gaps are put on the outer legs and there is no air gap on the center leg. In this way, two inductors are built in one EI core. The structure is also designed such that the DC fluxes of the two inductors are added in the center leg. Because these two inductors belong to two 180° interleaved phases, their AC fluxes get canceled in the center leg. This reduces the core loss.

The output capacitors s are $6\times1200\mu F$ OSCON capacitors plus $18\times22\mu F$ ceramic capacitors.

The photograph of the prototype is given in Fig. 4.22. Test waveforms are shown in Fig. 4.23. The top switch drain-to-source voltage gets clamped. The test efficiency is plotted in Fig. 4.24. The couple buck improves the efficiency by more than 3% over the buck converter. Since the *n=2* couple buck has a symmetrical transient response in this design case, it is valid to say that L_{ct2} dominates the transient response. Because L_{ct2} in the couple buck is nearly the same as that in the buck converter, the same transient response is expected for both. Fig. 4.25 shows the transient response test waveforms. The same response is obtained.

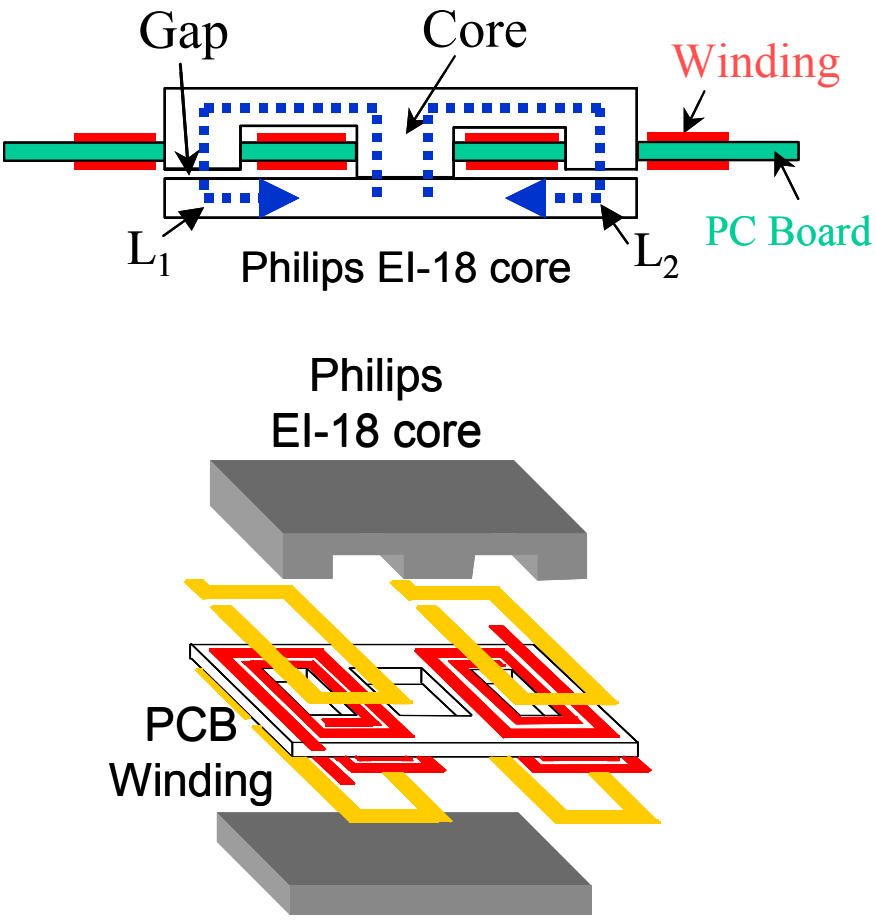


Fig. 4.21. Implementation of the magnetic structure.

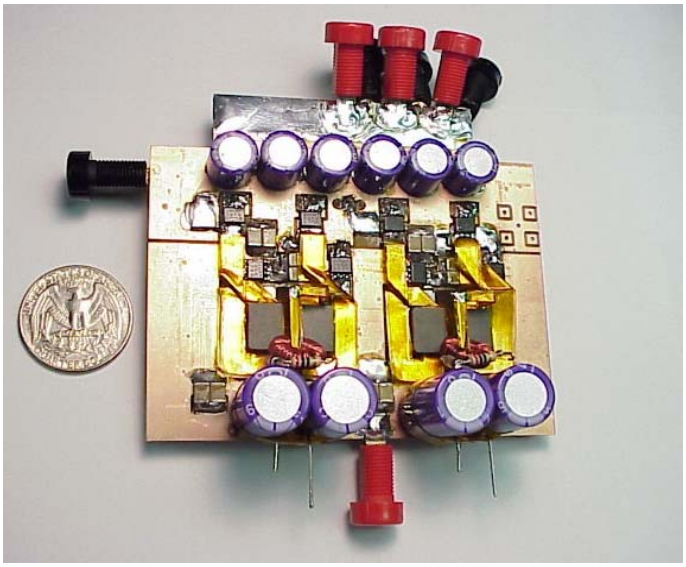


Fig. 4.22. Photograph of the four-phase interleaving active-clamp couple-buck VRM prototype.

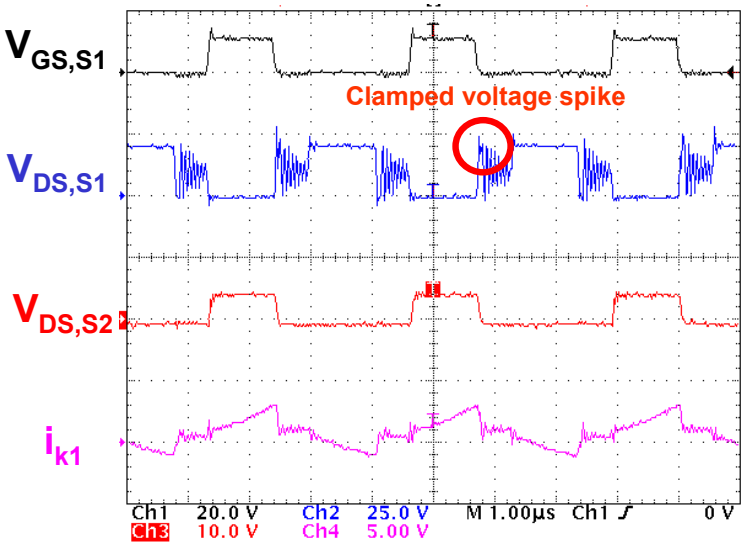


Fig. 4.23. Test waveforms of the active-clamp couple-buck VRM.

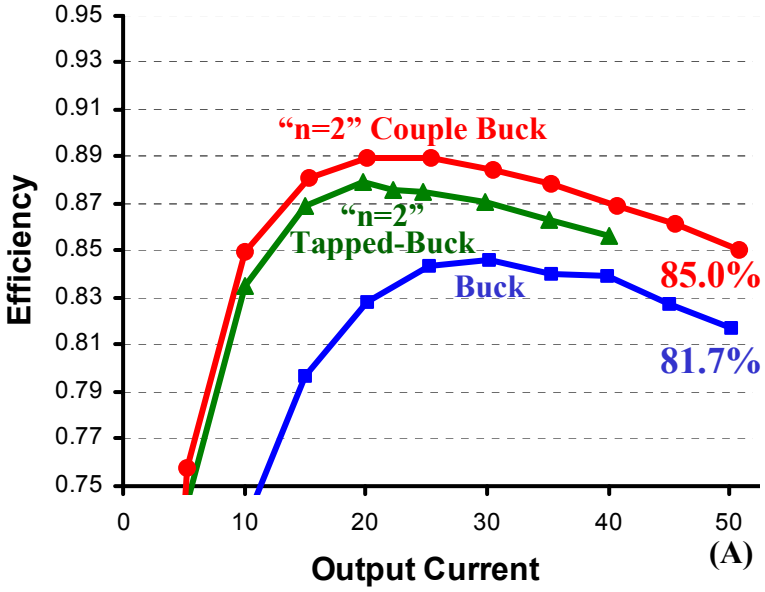
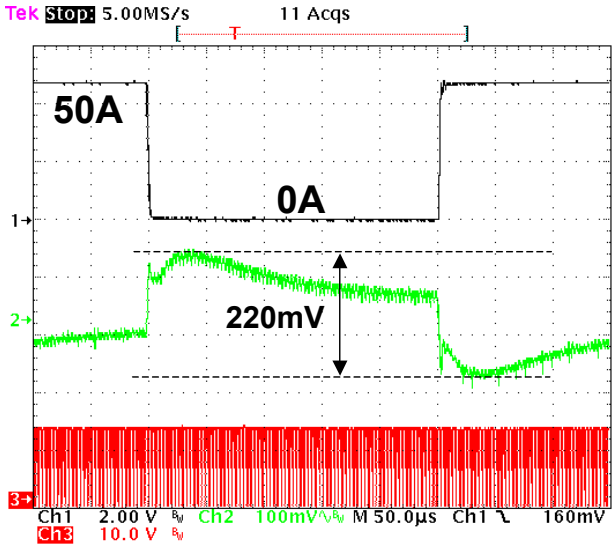


Fig. 4.24. Measured efficiency of the active-clamp couple-buck VRM.



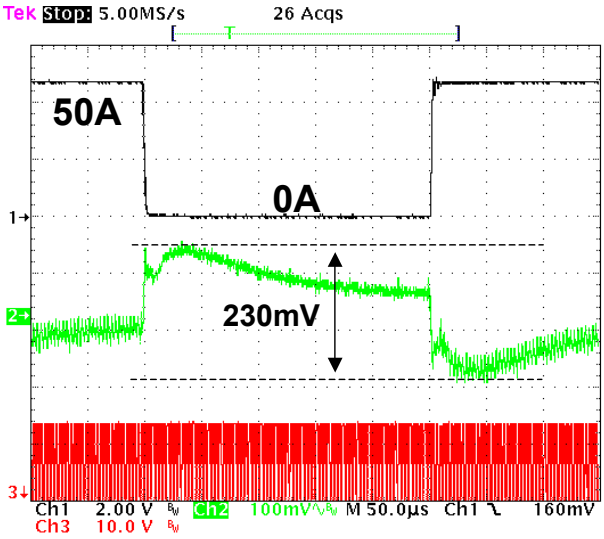


Fig. 4.25.Equal transient response of the buck and the active-clamp couple-Buck VRMs.

4.7. Summary

The active-clamp couple-buck converter clamps the voltage spike caused by the leakage inductor in the tapped-inductor buck converter and recovers the energy.

In an active-clamp couple-buck converter, L_{ct2} is fixed, but L_{ct1} decreases when n increases. When $L_{ct1} \geq L_{ct2}$, the transient response remains the same; when $L_{ct1} < L_{ct2}$, the transient response worsens.

With a properly designed turns ratio n, the duty cycle can be a more favorable value than that of the buck. Therefore, the efficiency can be improved.

Interleaving can help cancel the output ripple. The effectiveness of the ripple cancellation is a function of the duty cycle, but is NOT a function of turns ratio n.

The active-clamp couple-buck has good dynamic properties, which makes it appropriate for wide bandwidth design.

Chapter 5.

Conclusion

Since the early 80s, the computer industry has undergone rapid growth. Processors are becoming faster and more powerful. Power management issues in computing systems are becoming more complex and challenging. An evolution began when the high-performance Pentium processor was driven by a non-standard, less-than-5V power supply, instead of drawing its power from the 5V plane on the system board. A VRM is put close to the processor in order to provide the power as quickly as possible. In the past, VRMs basically drew power from the 5V output of the silver box. Nowadays, for the desktop and workstation applications, VRM input voltage has moved to the 12V output of the silver box. And for server applications, the 48V VRM is emerging as a standard practice.

Today's 12V VRMs use the multi-phase interleaving synchronous buck topology. Future microprocessors will run at very low voltage (below 1V), will consume up to 100A of current, and will have fast dynamics of about 400A/us. Due to the very low output voltage, the buck converter has a very small duty cycle, which may be even smaller than 0.1 in the future. This extreme duty cycle creates issues that complicate the design of an efficient converter with decent transient response.

In chapter 2, the multi-phase interleaving buck converter was analyzed to determine that the fundamental limitation is its extreme duty cycle. This extreme duty

cycle impairs its efficiency. Also, the extreme duty makes the output ripple cancellation ineffective.

The tapped-inductor buck converter was introduced in Chapter 3. This converter extends the duty cycle with the help of an additional design variable — turns ratio *n*. A properly designed *n* can extend the duty cycle; therefore, efficiency is improved. A properly designed *n* will not impair the transient response. But the tapped-inductor buck suffers a detrimental voltage spike caused by the leakage inductance. In addition, the tapped-inductor buck has a moving RHP zero, which makes it difficult to achieve wide-bandwidth design.

The active-clamp couple-buck was discussed in Chapter 4. It clamps the voltage spike caused by the leakage inductance and recovers the energy. By choosing turns ratio *n*, the duty cycle can be a more favorable value than that of the buck. Therefore, efficiency is improved. A properly designed *n* will not impair the transient response. The active-clamp couple-buck also has good dynamic properties, which makes it appropriate for wide-bandwidth design.

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