DM EMI Noise Analysis for Single Channel and Interleaved Boost PFC in Critical Conduction Mode

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Abstract

The critical conduction mode (CRM) power factor correction converters (PFC) are widely used in industry for low power offline switching mode power supplies. For the CRM PFC, the main advantage is to reduce turn-on loss of the main switch. However, the large inductor current ripple in CRM PFC creates huge DM EMI noise, which requires a big EMI filter. The switching frequency of the CRM PFC is variable in half line cycle which makes the EMI characteristics of the CRM PFC are not clear and have not been carefully investigated. The worst case of the EMI noise, which is the baseline to design the EMI filter, is difficult to be identified. In this paper, an approximate mathematical EMI noise model based on the investigation of the principle of the quasi-peak detection is proposed to predict the DM EMI noise of the CRM PFC. The developed prediction method is verified by measurement results and the predicted DM EMI noise is good to evaluate the EMI performance. Based on the noise prediction, the worst case analysis of the DM EMI noise in the CRM PFC is applied and the worst case can be found at some line and load condition, which will be a great help to the EMI filter design and meanwhile leave an opportunity for the optimization of the whole converter design.

What is more, the worst case analysis can be extended to 2-channel interleaved CRM PFC and some interesting characteristics can be observed. For example, the great EMI performance improvement through ripple current cancellation in traditional constant frequency PFC by using interleaving techniques will not directly apply to the CRM PFC due to its variable switching frequency. More research needs to be done to abstract some design criteria for the boost inductor and EMI filter in the interleaved CRM PFC.

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Chapter 1. INTRODUCTION

1.1. Background

The distributed power system (DPS) has been becoming an industry practice as a systematic solution for the offline switch mode power supplies (SMPS) used in information technology applications [1.1].

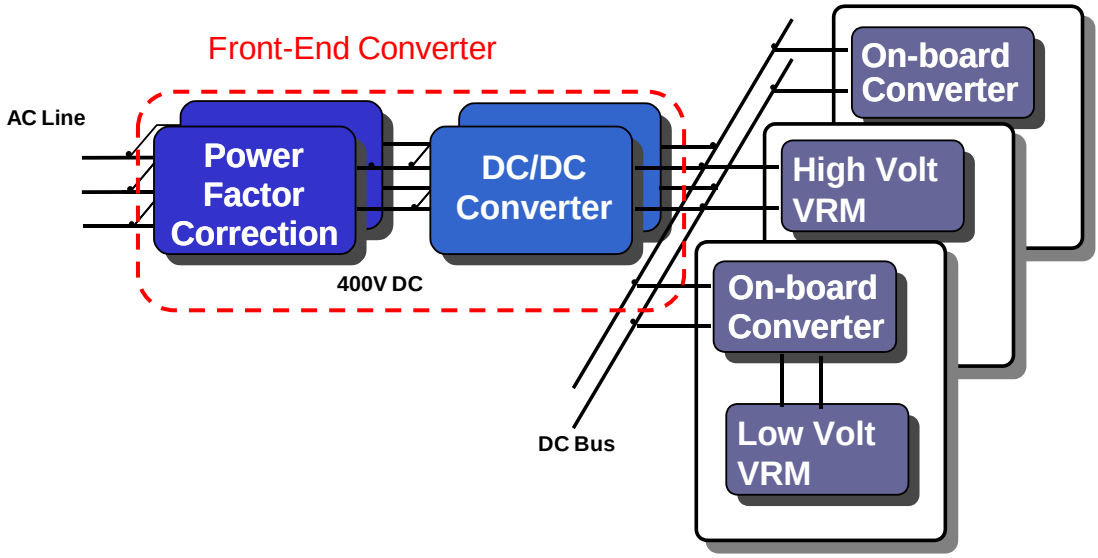

Figure 1.1: Distributed Power System

As shown in Figure 1.1, a typical DPS structure which is often found in laptops, desktops and servers applications could be divided into two parts, the frond-end converter and the voltage regulator module (VRM). For the front-end converter, the so called computer power supply, it generally adopts a two-stage approach, with the power factor correction (PFC) converter as the first stage and the DC-DC converter as the second stage.

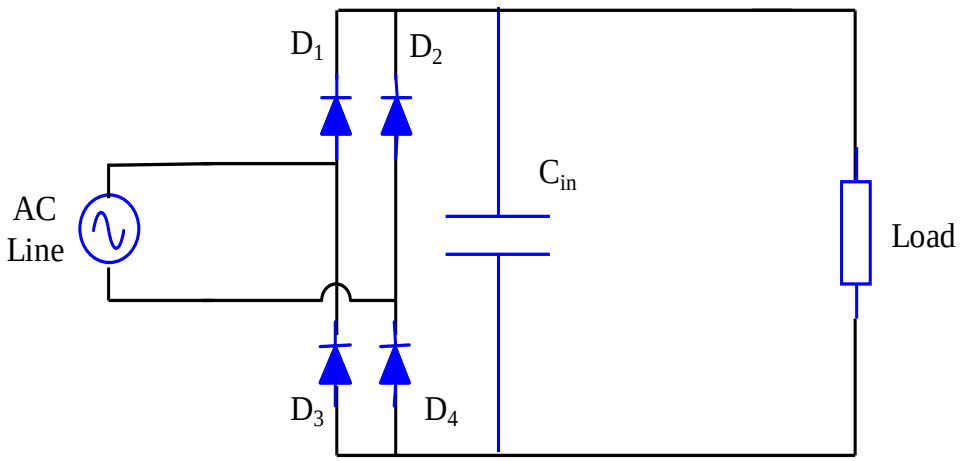

Figure 1.2: Full-wave Bridge Rectifier with Smoothing Capacitor

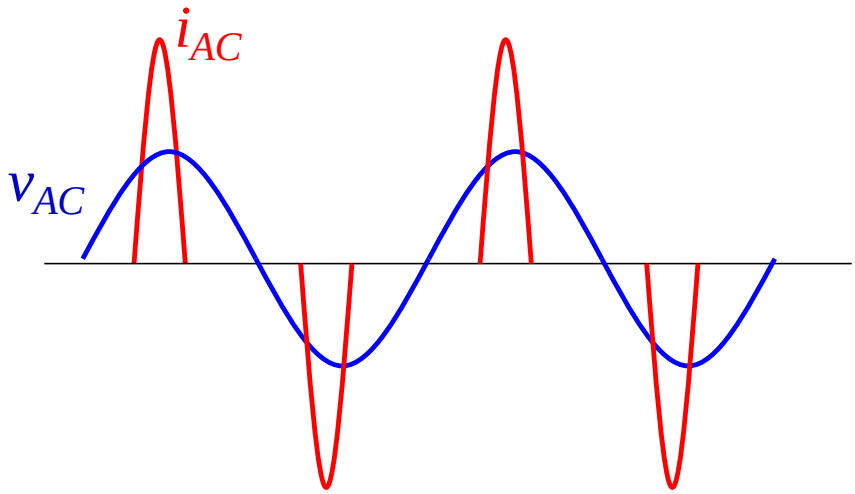

Figure 1.3: AC Input voltage and Distorted AC Input Current

A simple full-wave bridge rectifier is shown in Figure 1.2 and the AC input voltage and AC input current is shown in Figure 1.3. Due to the smoothing capacitor after the diode bridge, the AC input current is heavily distorted. As the power quality is always a major concern, there are stringent international standards which set limits to the input harmonic currents, such as IEC 1000-3-2 [1.2]. Therefore, the PFC converter is becoming a common practice and has been widely used in front-end converters to help the AC input current follow the sinusoidal AC input voltage, and thus meet the harmonic current limits.

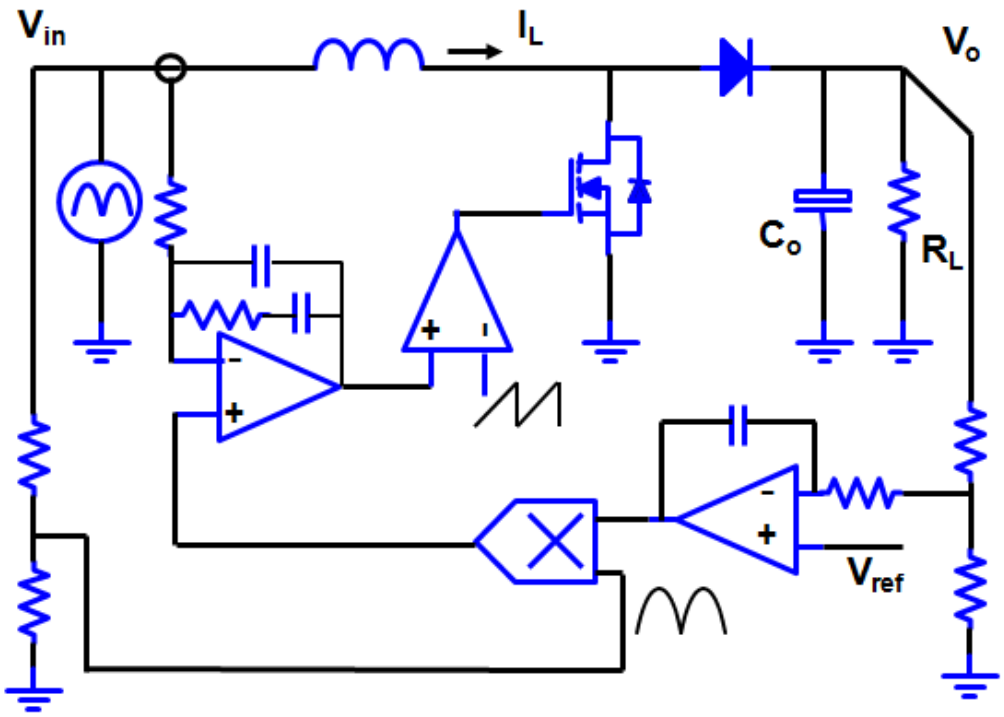

Figure 1.4: Average Current Control Scheme for Boost PFC in CCM

For PFC techniques, the boost converter is inborn a good topology since its input current is continuous. For the continuous conduction mode (CCM) boost PFC converter, average current-mode control is one of the most important control schemes. The diagram of the average current-mode control scheme for CCM boost PFC is shown in Figure 1.4 [1.3]. Through the current feedback loop, the average inductor current (i.e., AC input current) will be forced to follow the current reference, which is proportional to the sinusoidal AC input voltage. Thus the PFC function is achieved.

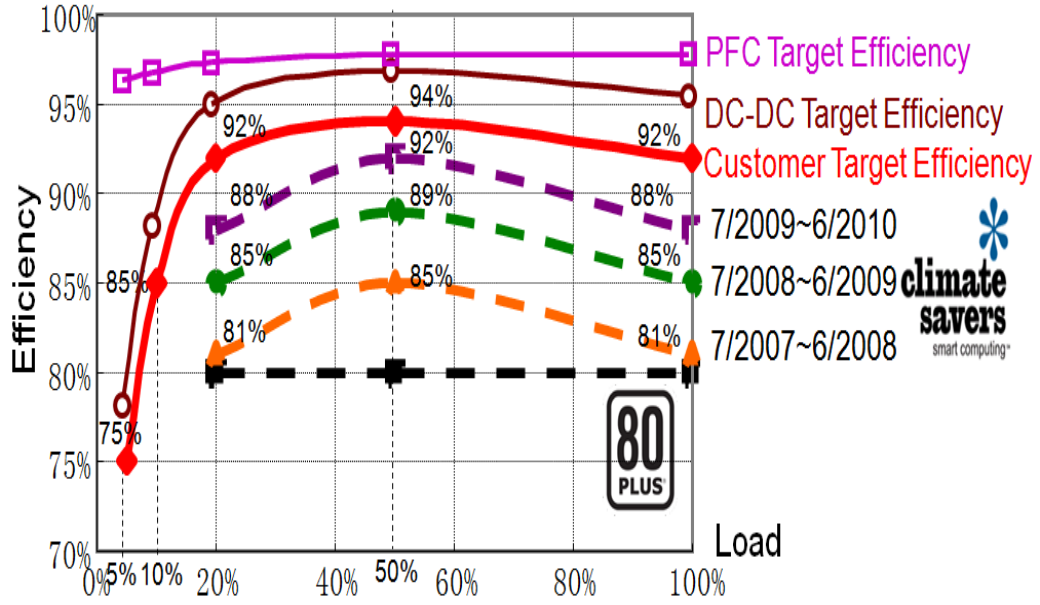

Figure 1.5: Efficiency Requirements for the Front-End Converter

The advantages of the CCM boost PFC converter with average current-mode control are obvious. Compared with CCM boost PFC with peak current control, it can achieve better power factor. Compared with CCM boost PFC with hysteresis control, it is constant frequency and can avoid too high switching frequency at the beginning and the end of each half line cycle. Moreover, compared with discontinuous conduction mode (DCM) boost PFC, it has smaller inductor current ripple and thus smaller conduction losses and smaller core losses. These advantages make the CCM boost PFC with average current-mode control the most popular circuit to achieve PFC function in industry.

However, with the fast increasing of the power consumption worldwide, the efficiency for the front-end converter is becoming more and more important. The dashed curves in Figure 1.5 show some of the efficiency requirements from organizations such as 80Plus and Climate Savers. The maroon and the pink solid curves in Figure 1.5 are DC-DC and PFC target efficiency, respectively, based on the red solid curve, which is the total target efficiency for the front end converter by some customer. It clearly demonstrates that the efficiency requirement for the PFC converter keeps increasing and is becoming the most dominant factor in PFC converter design.

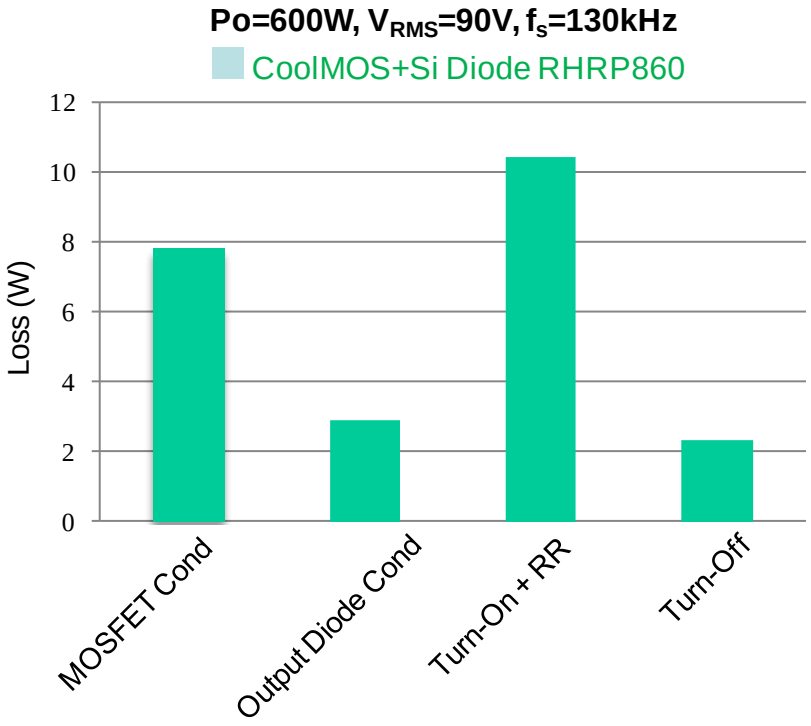

Figure 1.6: Loss Breakdown of Switching Devices in CCM Boost PFC

In regard to the efficiency, one disadvantage of CCM boost PFC is the large turn-on loss of the switch, which is mostly from the reverse recovery process of the output diode [1.4]. Figure 1.6 shows the loss breakdown of the switching devices in a 600Watts CCM boost PFC. From the figure we can see that the turn on loss is the most dominant one if silicon output diode is used.

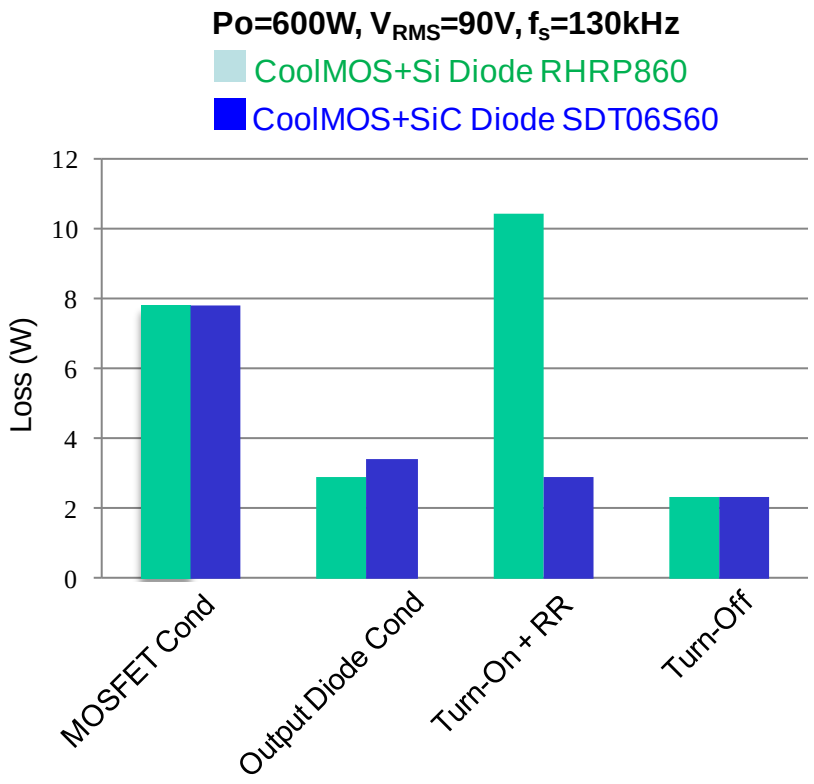

Figure 1.7: Loss Breakdown Comparison between PFCs w/o and w/ SiC Diode

To further boost the efficiency of the PFC converter, it would be advisable to reduce the turn-on loss of the switch. Using silicon carbide (SiC) diode to reduce the reverse recovery loss should be an obvious way. Figure 1.7 shows the loss comparison of the switching devices between CCM boost PFC with the silicon diode and that with the SiC diode. Although the conduction loss of the SiC diode increases a little bit, the reverse recovery related turn-on loss is dramatically decreased. Totally 7watts losses can be saved and efficiency can be boosted up by 1.2 percent.

The major concern for using the SiC diode is the cost. The retail price of the SiC diode SDT06S60 is much more, about 10 times more expensive than the retail price of the hyper-fast silicon diode RHRP860 from www.digitkey.com. For cost sensitive solutions, SiC diode would not be a very good choice.

1.2. Overview of Boost PFC in Critical Conduction Mode

To reduce the turn-on loss and further boost the efficiency of the PFC converter, the critical conduction mode (CRM) boos PFC converter is drawing more and more

attention recently [1.5][1.6]. It is actually operating in the boundary condition of the CCM and DCM [1.7], and thus also called boundary condition mode (BCM). There are two major control schemes for CRM boost PFC, current mode control [1.8] and voltage mode control [1.9], shown in Figure 1.8 and 1.9, respectively.

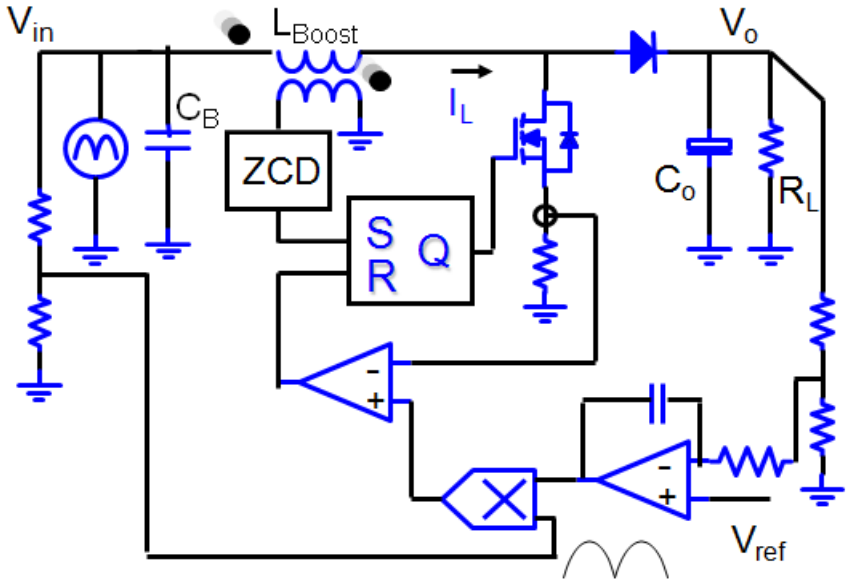

Figure 1.8: Current Mode Control Scheme for CRM Boost PFC

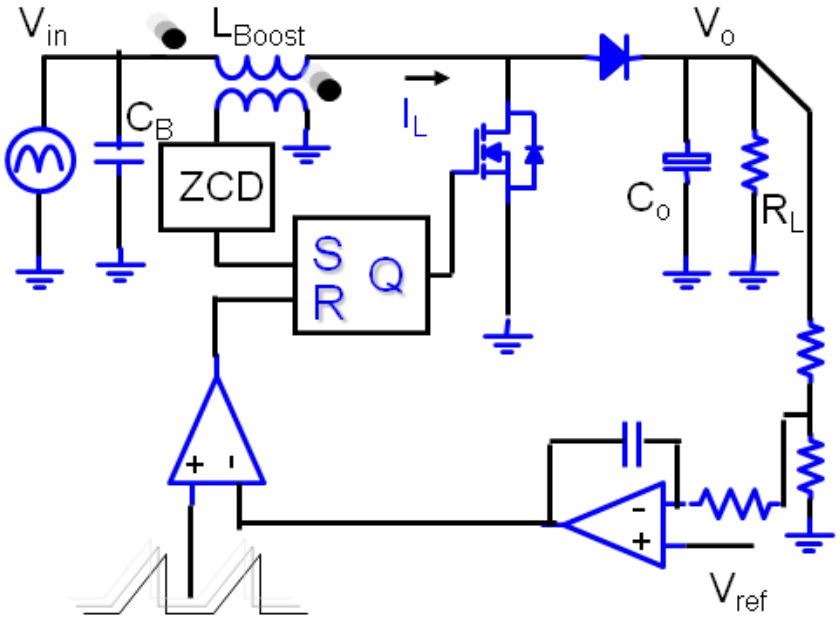

Figure 1.9: Voltage Mode Control Scheme for CRM Boost PFC

Comparing the two control schemes we can find that both control schemes use an auxiliary winding to detect when the inductor current reach zero to achieve zero

current turning-on. The difference is turning-off mechanism. For the voltage mode control, the on time of the switch is determined by the control voltage, the output of the voltage loop compensator, and a saw tooth waveform with fixed rising slope. After the switch is turned on, the saw tooth waveform will increase and when it is equal to the control voltage, the switch will be turned off and the saw tooth waveform will be reset to zero. Then the inductor current begins to decrease.

For the current mode control, the current reference of the peak inductor current is obtained by multiplying the sampled input voltage with the control voltage. When the inductor current is equal to the reference, the switch will be turned off.

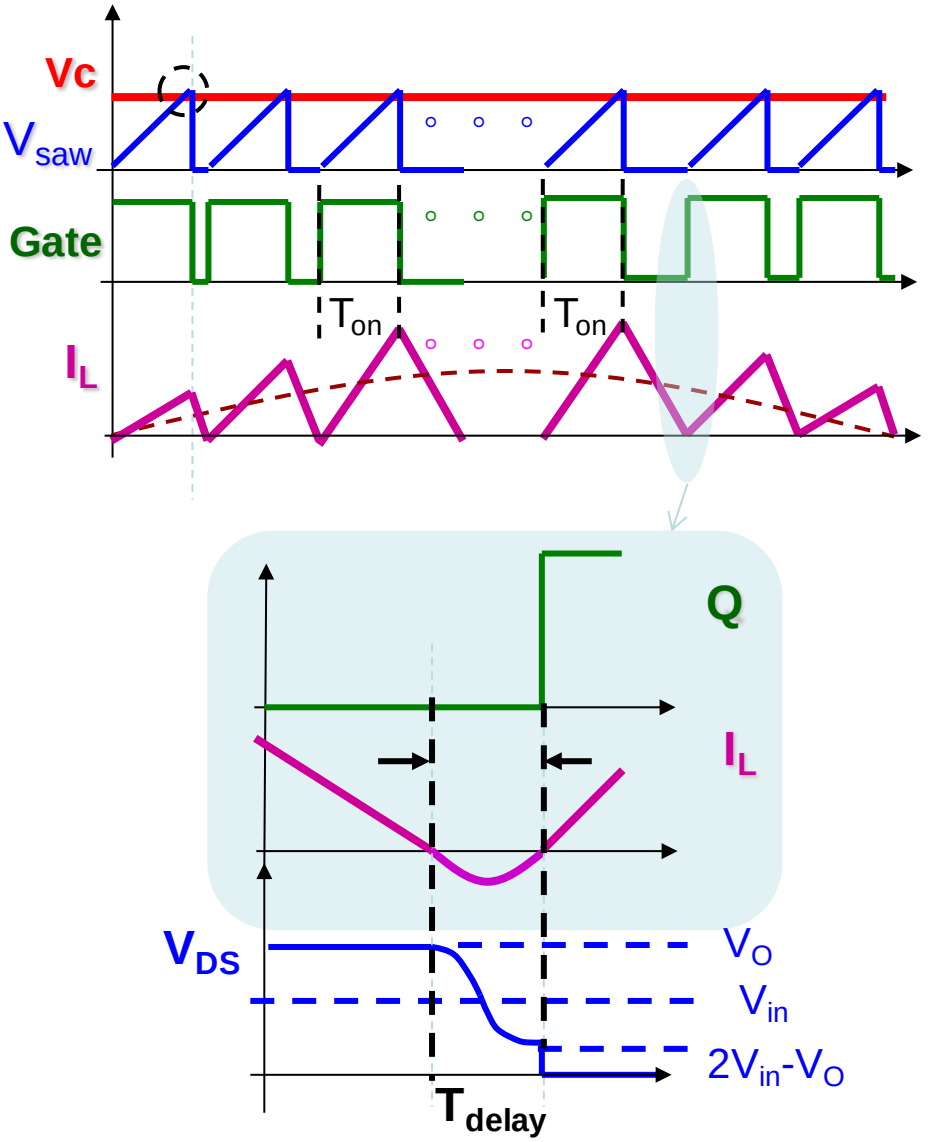

Figure 1.10: Waveforms Sketch for CRM Boost PFC with Voltage Mode Control and Zoom-in for Valley Switching

Compared with the voltage mode control, the current mode control needs extra circuits to sample the input voltage and the drain to source current of the switch and also the multiplier to obtain the current reference. Thus, the simplicity of the voltage mode control makes it more and more popular recently [1.10][1.11] Figure 1.10 shows the detailed waveforms in CRM boost PFC with voltage mode control.

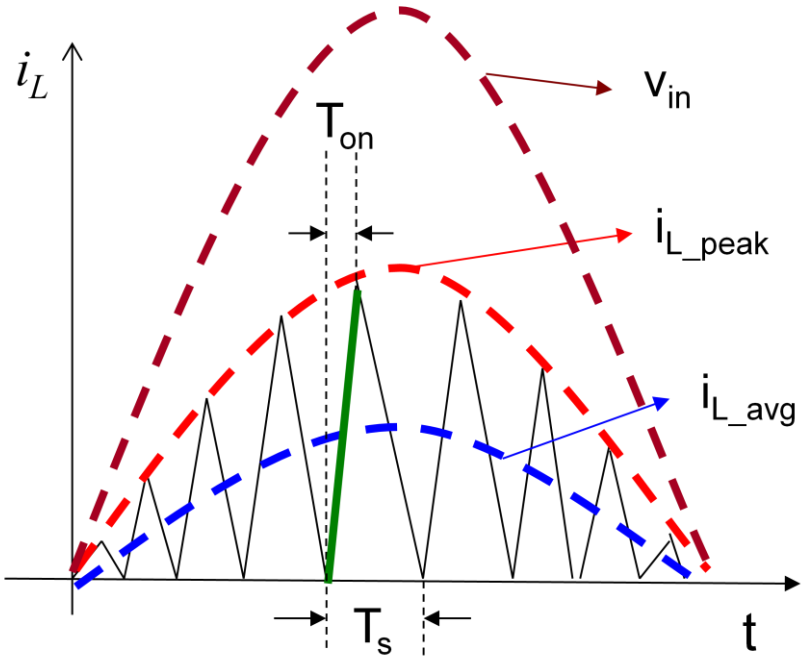

Figure 1.11: Inductor Current Waveform Sketch

Because of the low bandwidth of the voltage feedback loop in the PFC converter, the control voltage can be treated as a constant value in a half line cycle, which means the on time is constant for a half-line cycle. This would guarantee a unit power factor, theoretically, because, as shown in Figure 1.11,

$$i_{L\_avg}(t)=\frac{1}{2}i_{L\_peak}(t)=\frac{1}{2}T_{on}\frac{v_{in}(t)}{L_B}=\frac{1}{2}T_{on}\frac{\sqrt{2}V_{RMS}\left|\sin(\omega t)\right|}{L_B}\propto\sin(\omega t) \tag{1.1}$$

And it is also shown in Figure 1.10 that when the inductor current decreases to zero, actually the switch will not be turned on immediately but with a short delay, which allows the boost inductor to be resonant with the parasitic output capacitor of the switch and the parasitic capacitor of the output diode. This resonance will help to reduce the drain to source voltage of the switch and thus further reduce the turn-on loss. Actually, when the instantaneous input voltage is smaller than half of the output

voltage V_O, the V_{DS} can drop to zero and thus zero voltage switching (ZVS) can be achieved. When the instantaneous input voltage is larger than half of the output voltage Vo, valley switching could be achieved, with the minimum $V_{DS} = 2V_{in}(t) - V_O$.

1.3. CRM or CCM

The benefit of the CRM boost PFC over the CCM boost PFC is the ZCS to reduce the reverse recovery loss and the ZVS or valley switching to further reduce the turn-on loss. However, the current ripple in CRM boost PFC is much larger than that in CCM boost PFC, which means large conduction loss. Thus, the single channel CRM boost PFC is not suitable for high power applications. It is generally used below 300Watts in industry. For higher power applications, multi-channel CRM boost PFC needs to be adopted. In Figure 1.12, an efficiency comparison between a 2-channel interleaved CRM boost PFC with silicon diodes [1.12] and a 2-channel CCM boost PFC with SiC diode is made [1.13]. We can see the interleaved CRM boost PFC achieves the same good efficiency at full load as the interleaved CCM boost PFC.

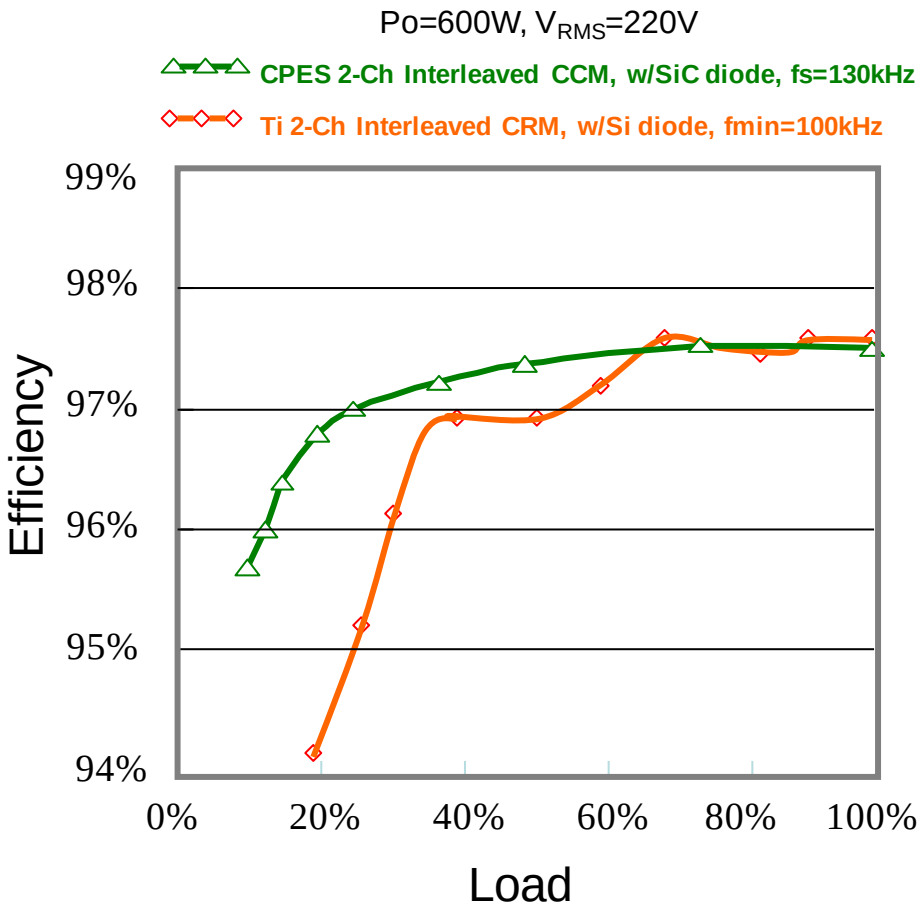

Figure 1.12: Efficiency Comparison between 2-Channel Interleaved PFC in CCM with SiC Diode and in CRM with Si Diode

However, at 20 percent load, the efficiency for 2-channel CRM boost PFC drops dramatically and is about 2.5 percentages below that for 2-channel CCM boost PFC. This is because for CRM boost PFC, the switching frequency is inverse-proportional to the load,

$$f_s(t) = \frac{V_{RMS}^2\left(V_o - \sqrt{2}V_{RMS}\sin(\omega t)\right)}{2L_B P_o V_o} \propto \frac{1}{P_o} \tag{1.2}$$

As load decrease, the switching frequency will increase, which will increase the switching loss and decrease the light load efficiency.

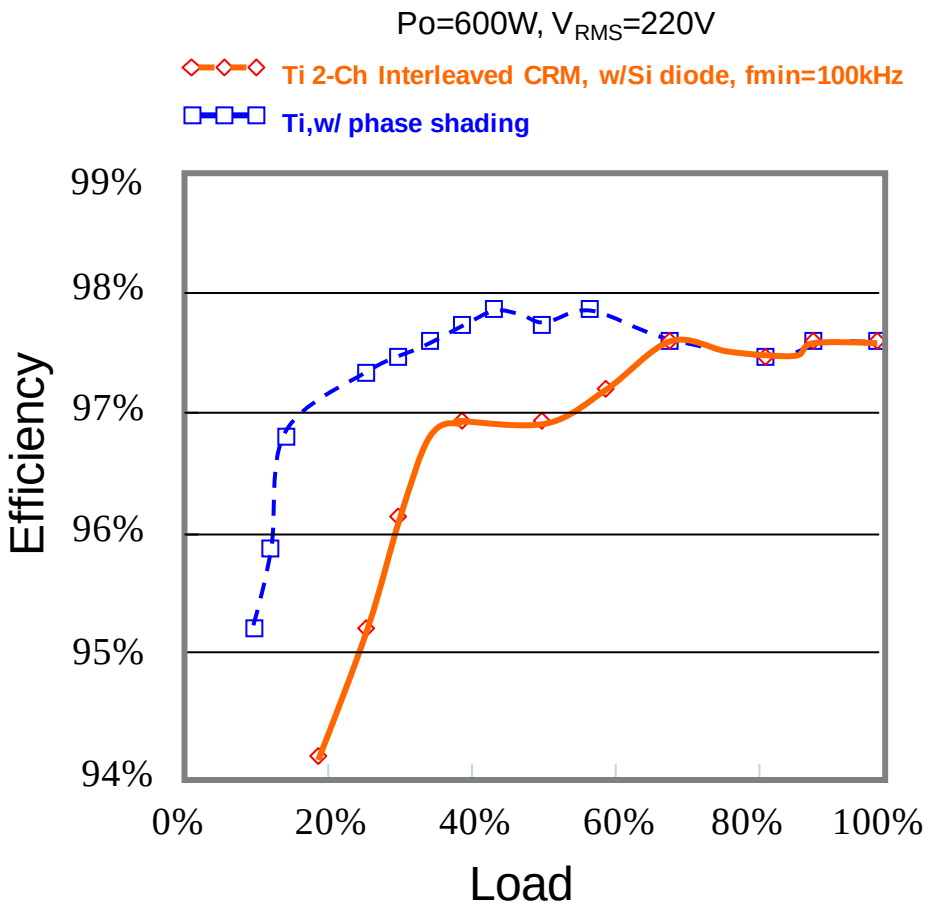

Figure 1.13: Efficiency Comparison between 2-Channel Interleaved PFC in CRM without and with phase shedding

To achieve better light load efficiency for CRM boost PFC, phase shedding technology could be used. Figure 1.13 shows the comparison between a 2-channel interleaved CRM boost PFC without and with phase shedding. We can see that by using phase shedding techniques, about 3 percentages efficiency boost can be achieved at 20 percent load.

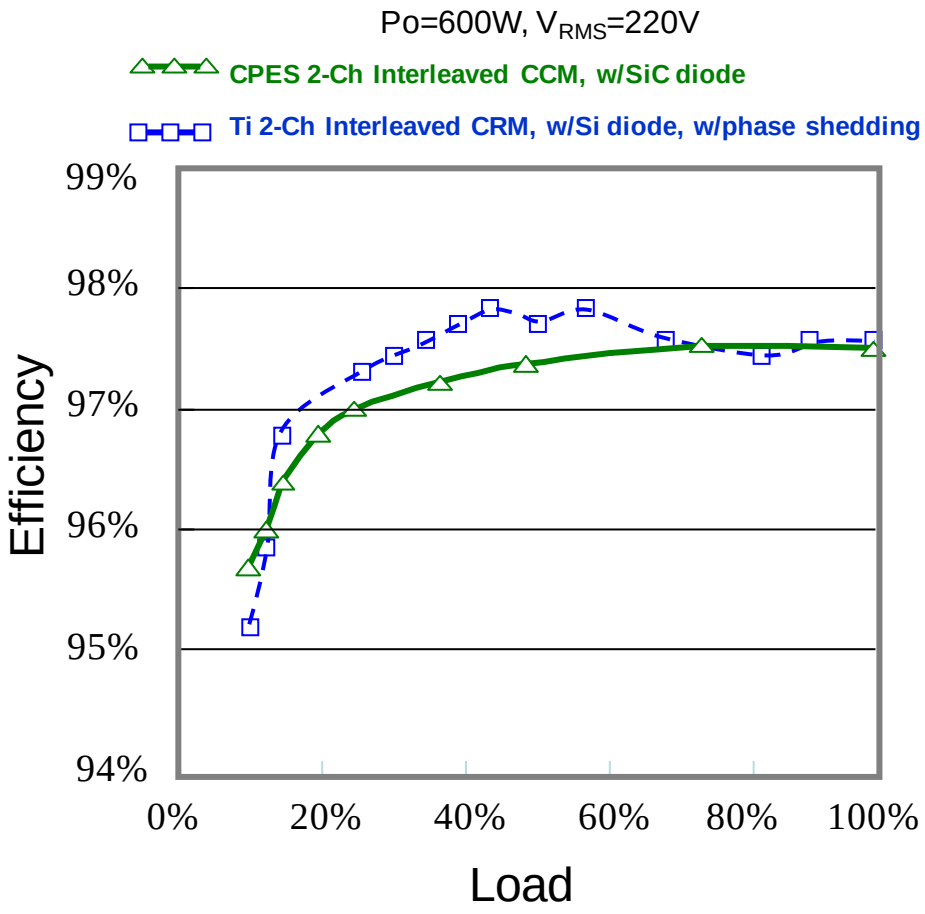

Figure 1.14: Efficiency Comparison between 2-Channel Interleaved CCM PFC with SiC Diode and CRM PFC with Si Diode and with Phase Shedding

From Figure 1.14, the 2-channel CRM boost PFC with phase shedding can achieve almost the same good or even better efficiency for overall load range as 2-channel interleaved CCM boost PFC. Thus, for mid-range power applications, 2-channel interleaved CRM boost PFC would be a cost-effective solution.

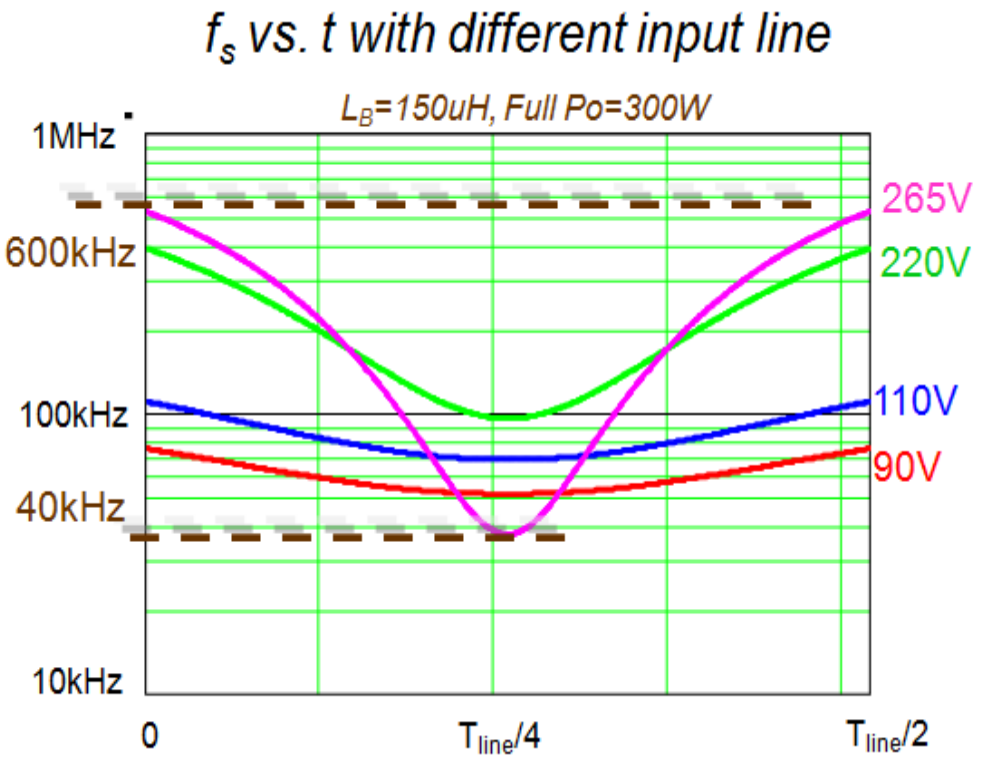

Figure 1.15: Switching Frequency Varies with Input Line

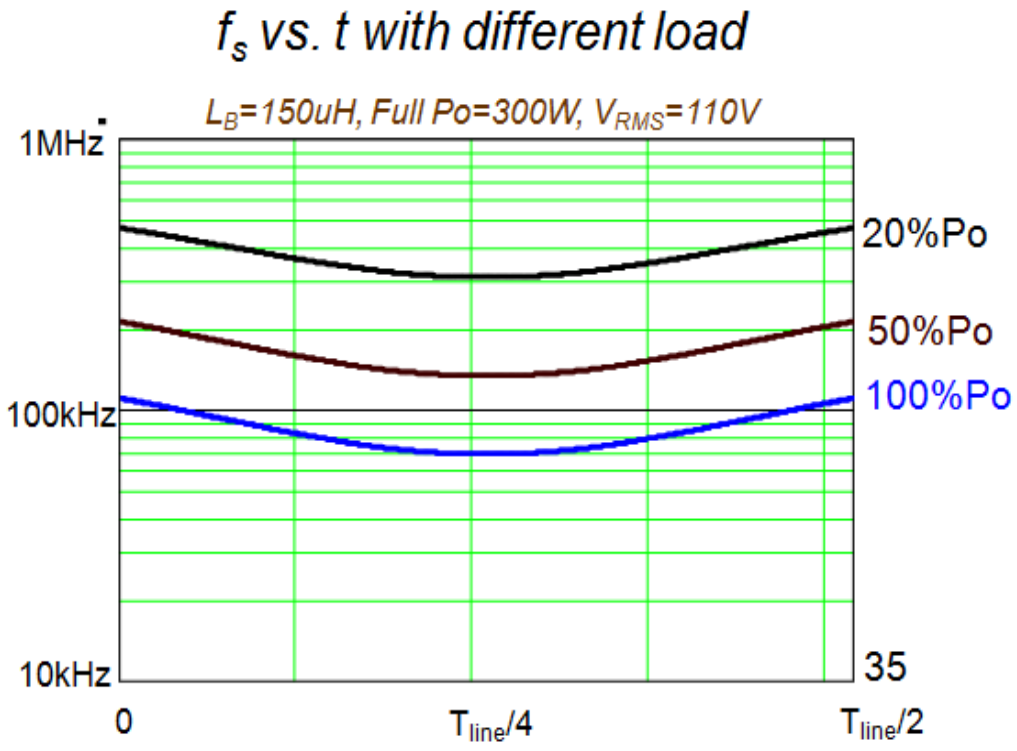

Figure 1.16: Switching Frequency Varies with Output Load

However, the major concern with the CRM boost PFC is the electromagnetic interference (EMI) noise due to the large ripple current. Different from the CCM

boost PFC which has the constant switching frequency, the switching frequency of the CRM boost PFC varies with both input line and load conditions, as shown in Figure 1.15 and Figure 1.16, respectively. At highest line V_{RMS}=265V, and full load, the switching frequency ranges from around 40 kHz to around 600kHz. Such wide range of switching frequency makes the EMI knowledge and experience we gain in CCM boost PFC could not be directly applied to CRM boost PFC.

1.4. Literature Survey

Because the PFC converters are widely used in SMPSs, there is a lot of research work being done in the area of EMI analysis for PFC converters [1.14][1.15][1.16][1.17].

However, all of these research papers are targeting on the EMI characteristics of the CCM boost PFC. The analyzing method adopted in these papers generally is the time domain waveform simulation plus the fast Fourier transformation. However, for waveforms with variable switching frequency, fast Fourier transformation would not apply. This makes that there is little research focusing on the EMI characteristics of the PFC converter with variable switching frequency.

In [1.18], ripple current of the CRM boost PFC is analyzed and DM EMI filters made for CRM boost PFC and CCM boost PFC are compared. However, harmonic current information of the ripple current is not enough to differentiate the EMI performance and thus cannot be directly used to design the DM EMI filter. Meanwhile, the DM EMI filter designed for the CRM boost PFC in this paper is based on one DM EMI noise measurement result at full load conditions, which is not sure yet to be the worst case.

In [1.19], the EMI performance of a DCM boost PFC with variable switching frequency control is evaluated based on circuit simulation and measurements. This paper focuses on the high frequency EMI noise reduction by proper packaging and PCB layout. More characteristics and EMI filter design criteria for PFC with variable

switching frequency still need to be identified.

EMI noise measurements, which are usually used in EMI noise analysis for CCM boost PFC, are definitely the most accurate and reliable tools to investigate the EMI performance. However, for CRM boost PFC, which is rather unclear in EMI characteristics, it would be quite a time-consuming process to do the investigation based on measurements.

In [1.20][1.21][1.22], different cancellation techniques are introduced to reduce the CM EMI noise. These techniques are based the CM current balance concept, which could be easily to apply to CRM boost PFC to attenuate the bare CM EMI noise. This will aggravate the concern for the DM EMI noise in CRM boost PFC, for which there is no easy way to cancel.

A possible way for ripple current cancellation is to use interleaving techniques. In [1.23], a novel interleaving technique is used to improve the EMI performance for the CCM boost PFC. The impact of the interleaving techniques on the EMI performance for the CRM boost PFC still needs to be clarified.

1.5. Objective and thesis organization

The main objective of this thesis is to characterize the DM EMI noise of the CRM boost PFC converter to benefit the EMI filter design because it has not been carefully investigated and thus is not clear yet. In order to fulfill this goal, several sub-objectives are achieved as listed below.

First, in Chapter 2, based on the investigation of the function of the EMI spectrum analyzer and especially of the different noise detection modes, a simplified block diagram for the function of the EMI spectrum analyzer is abstracted Procedures on how to analyze the DM EMI noise for the CRM boost PFC is discussed, which will make the noise prediction and worst case analysis in order.

Second, in Chapter 3, Fourier transformation is applied to the triangular ripple current waveform with variable frequency based on the quasi steady state approximation. Combined with the simplified EMI spectrum analyzer model, a complete approximate mathematical model is derived to predict the DM EMI noise for the CRM boost PFC. A general constant on-time PFC is designed and DM EMI noise measurements are carried out to verify the validity of the approximate mathematical model.

Third, in Chapter 4, based on the DM EMI noise prediction obtained from the approximate mathematical model for CRM boost PFC, worst case analysis is carried out and the worst DM EMI noise case for all the input line and load conditions can be found. Some criteria to ease the DM EMI filter design procedure of the CRM boost PFC are given. Based on the same principle, the DM EMI noise worst case analysis can also be done for the interleaved CRM boost PFC and the impact of interleaving techniques on the EMI performance could be understood.

Finally, in Chapter 5, limitation of the mathematical model is explained and plan for future work is proposed.

Chapter 2. PRE-REQUISITE TO EVALUATE DM EMI NOISE FOR BOOST PFC

2.1. EMI Noise Measurement and Standard

Electromagnetic compatibility (EMC) is becoming more and more important as the switching devices are widely used. In order to maintain a good electromagnetic environment, EMC standards are issued worldwide to limit the EMI. There is FCC part 15 in United States and CISPR 22 in Europe. All offline switching mode power supplies (SMPS) need to meet these standards before they can be marketed.

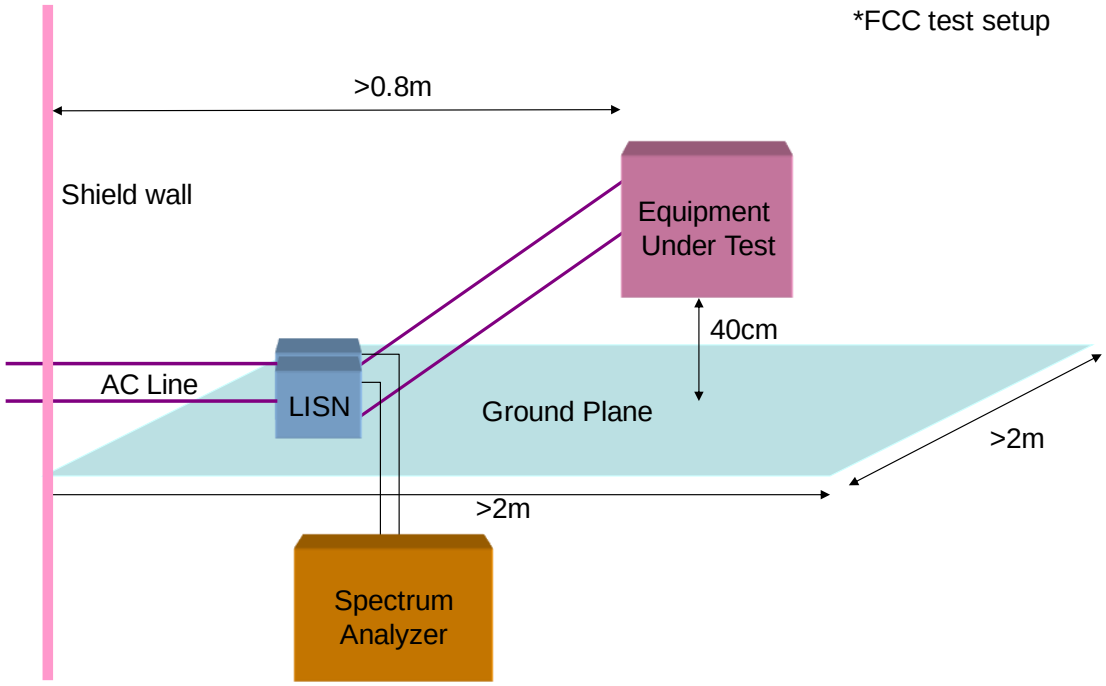

Figure 2.1: Measurement Setup for Conducted EMI Noise of Single Phase SMPS

Figure 2.1 shows the measurement setup for conducted EMI noise of the single phase SMPS. For measuring the conducted EMI noise, two Line Impedance Stabilization Networks (LISNs) are inserted between each AC line and the SMPS. The equivalent circuit for a LISN is shown in Figure. 2.2. The LISNs are used to stabilize the impedance of the input line and thus make sure that the measuring results are only related the equipment under test (EUT) without any influence from the impedance of different AC line.

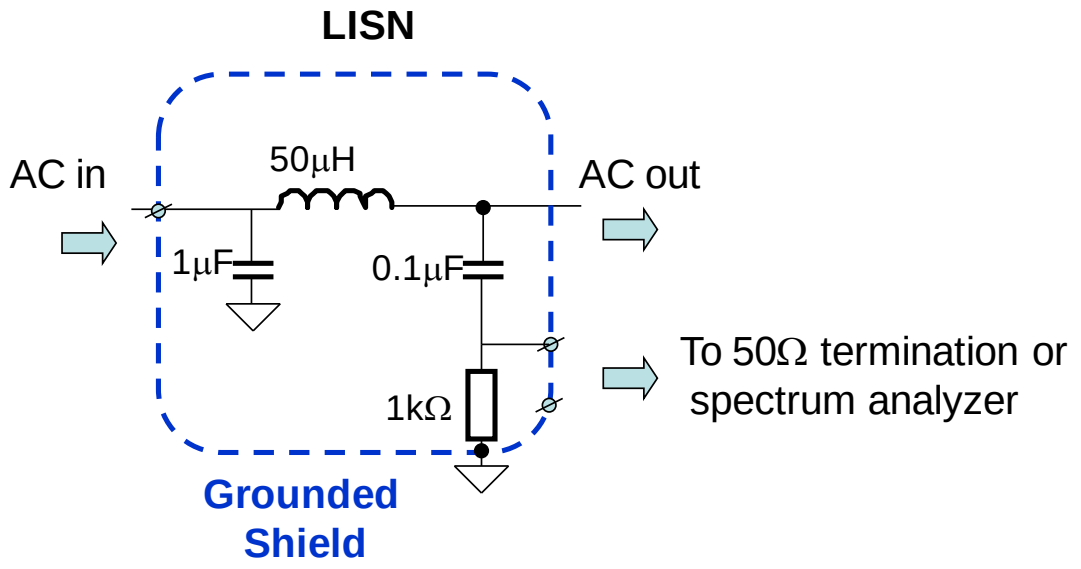

Figure 2.2: Equivalent Circuit of the LISN

Since each LISN will either be connected to a 50Ω termination or the spectrum analyzer whose input impedance is also 50Ω, the equivalent circuit for the measurement setup using the PFC converter as the EUT in Figure 2.1 can be obtained in Figure 2.3.

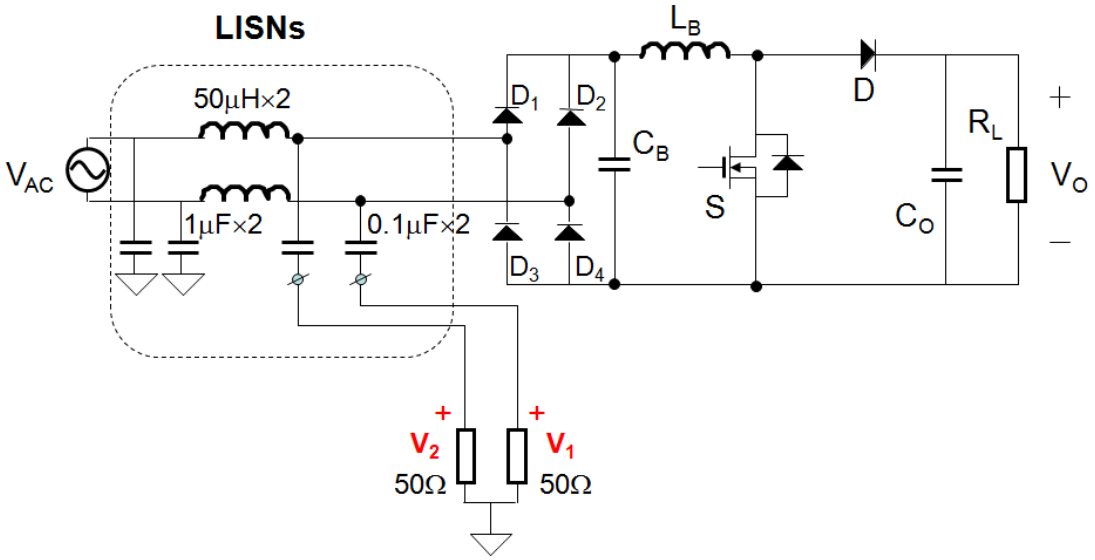

Figure 2.3: Equivalent circuit for Measurement Setup in Figure 2.1

The voltage drop on either 50Ω impedance can be seen as the total conducted noise voltage. For residential SMPSs such in laptops and desktops, the conducted EMI noise limit [2.1] is shown in Figure 2.4 and referred as the EMI noise standard in this thesis.

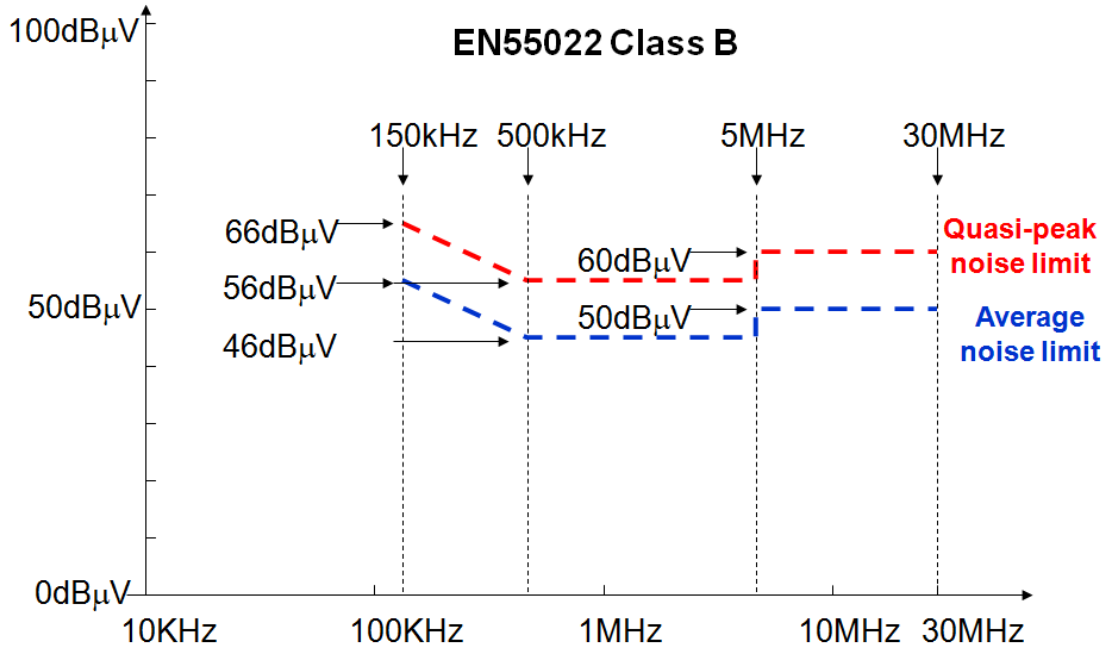

Figure 2.4: EMI Noise Standard

There are two types of noise limits, quasi-peak and average noise limits, which are corresponding to quasi-peak and average detector specified in [2.2]. Simply speaking, quasi-peak noise represents the repetitive peak noise energy and average noise represents the average noise energy. Both noise limits need to be satisfied.

2.2. Equivalent Differential Mode Loop

The total conducted noise includes two parts, differential mode (DM) conducted noise and common mode (CM) conducted noise. The propagation paths for both DM and CM noise are shown in Figure 2.5. The DM noise current, i_{DM} is defined as the current between AC line (hot) and AC line (neutral), shown as the pink dashed curve and the CM noise current, i_{CM} is defined as the current between AC lines and the ground, shown as the green solid curve. The C_{DG} is the parasitic capacitor from the heat sink of the switch to the ground, which is important in CM noise propagation path.

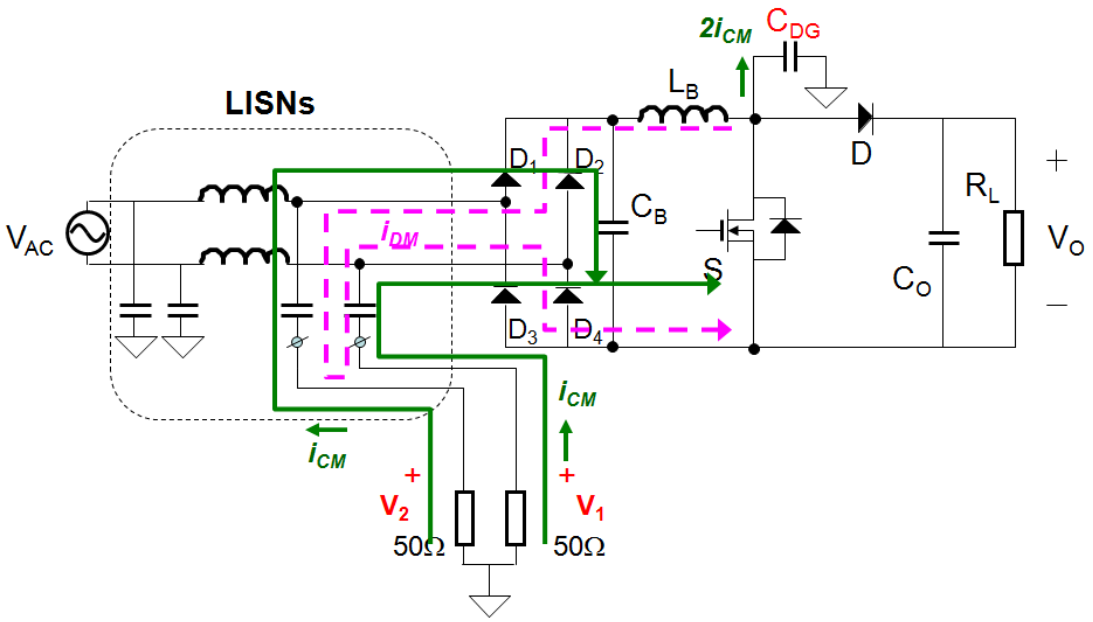

Figure 2.5: DM and CM Noise Current Propagation Paths

Thus, the DM noise voltage is,

$$\left|\mathbf{V_{DM}}\right| = \left|\frac{\mathbf{V_2 - V_1}}{\mathbf{2}}\right| = \left|\mathbf{50 i_{DM}}\right| \tag{2.1}$$

The CM noise voltage is,

$$\left|\mathbf{V_{CM}}\right| = \left|\frac{\mathbf{V_2 + V_1}}{\mathbf{2}}\right| = \left|\mathbf{50 i_{CM}}\right| \tag{2.2}$$

Due to the different propagation path for DM and CM EMI noise, they are generally analyzed separately. For the CRM boost PFC, because the most concern is the large DM EMI noise generated by the large inductor current ripple, thus only DM EMI noise is analyzed in this thesis. The simplified DM equivalent loop is shown in Figure. 2.6.

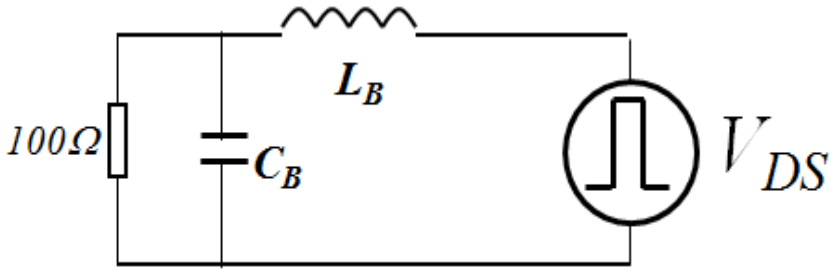

Figure 2.6: DM Equivalent Loop with Voltage Noise Source

Figure 2.6 is the traditional way [2.3] to model the DM loop with the drain to source voltage of the switch as the noise source. However, a more straightforward way would be to use the inductor ripple current, a combined action of the input AC voltage and V_{DS}, as the noise source. The equivalent loop is shown in Figure 2.7.

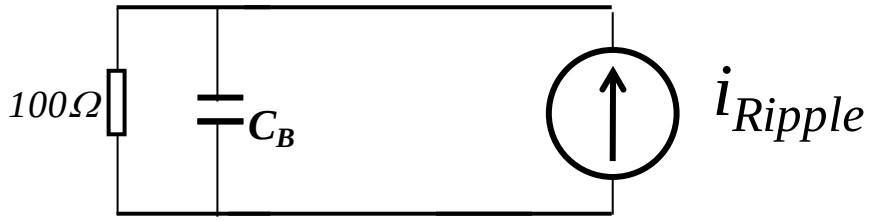

Figure 2.7: DM Equivalent Loop with Current Noise Source

Since the input capacitor C_B is playing the role of a low-pass filter and attenuating the noise current in Figure 2.7, it can be taken as part the DM EMI filter. Therefore for analyzing the bare noise to benefit the EMI filter design, C_B could be ignored here and put into the DM EMI filter. The final DM equivalent loop used in this thesis is in Figure 2.8 and,

$$\left|\mathbf{V_{DM}}\right| = \left|\mathbf{50i}_{Ripple}\right| \tag{2.3}$$

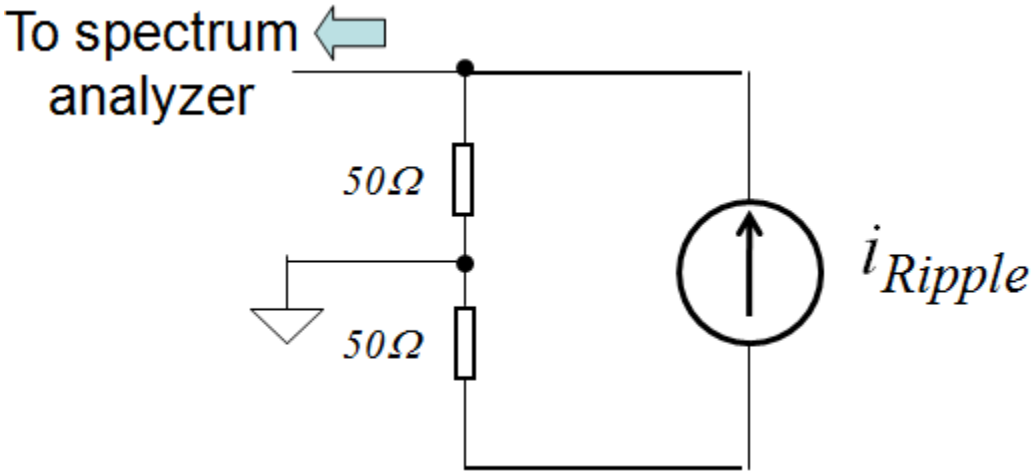

Figure 2.8: Final DM Equivalent Loop

2.3. Criterion to Evaluate the Size of the DM EMI Filter

The detailed design process for the EMI filter is not discussed in this thesis. However, in order to find the worst case of the DM EMI noise for the CRM boost

PFC, a criterion needs to be defined to evaluate the size of the DM EMI filter. According to [2.3], the corner frequency of the DM EMI filter would be a good criterion. Smaller DM corner frequency would mean larger DM EMI filter size and the smallest DM corner frequency would represent the worst case of the DM EMI noise.

In order to calculate the DM corner frequency, both the noise attenuation requirement and the DM EMI filter structure need to be known. In practice, both the one stage LC filter and two stage LCLC filter structures are adopted for DM EMI filter. For boost PFC operating in CRM or DCM which has a large inductor ripple current, generally the two stage LCLC filer structure will have a smaller size than one stage LC filter structure and this guideline is thoroughly discussed in [2.4] In this thesis, based on this guideline, we use two-stage DM EMI filter to continue our discussion.

Figure 2.9 shows the DM equivalent loop with the DM EMI filter. Please note that input capacitor is also part of the DM EMI filter and thus there are 5 passive components in the DM filter totally.

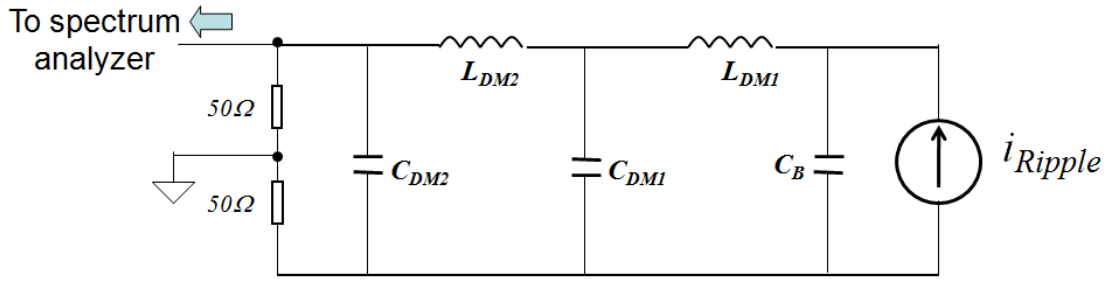

Figure 2.9: DM Equivalent Loop with DM EMI Filter

Define,

$$Insertion\ \ Gain = 20\log(|\mathbf{V}^{*}_{\mathbf{DM}}|) - 20\log(|\mathbf{V}_{\mathbf{DM}}|) \tag{2.4}$$

Where, V^{*}_{DM} is the DM noise voltage when the DM EMI filter is added.

Then the insertion gain is actually the attenuation in dB achieved by the DM EMI filter. Given $L_{DM1}=L_{DM2}=50uH$ and $C_B=C_{DM1}=C_{DM2}=0.22uF$, the insertion gain of the two stage DM EMI filter (including the input capacitor) can be drawn as in Figure 2.10.

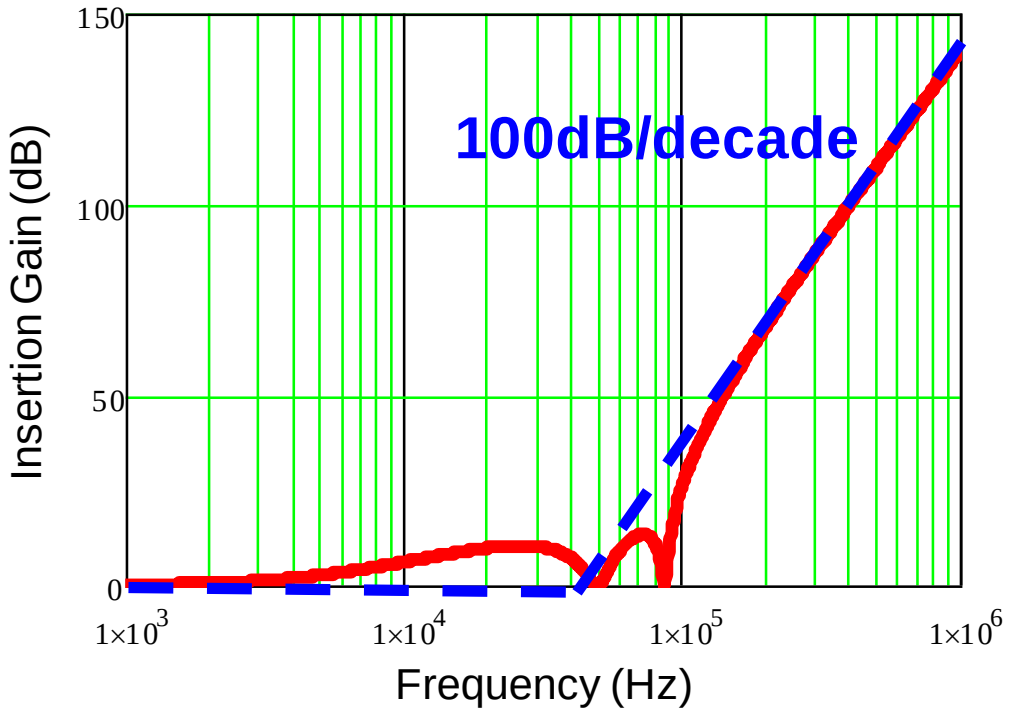

Figure 2.10: Insertion Gain for Given DM EMI Filter

This given DM EMI filter can achieve 100dB attenuation per decade when the frequency is above 100 kHz. This is generally true for a typical DM EMI filter design. Because the EMI standard starts to regulate the EMI noise from 150 kHz, we consider the two-stage DM EMI filter has 100 dB per-decade attenuation characteristics on DM EMI noise.

Thus for given attenuation requirement, the DM corner frequency can be calculated as,

$$f_{DM} = \frac{f_{Noise}}{10^{\frac{Att.}{100}}} \tag{2.5}$$

Where, Att. is the attenuation in dB and f_{Noise} is the noise frequency. This equation will be used in Chapter 4 to calculate the DM corner frequency.

Chapter 3. MATHEMATICAL PREDICTION OF QUASI-PEAK DM EMI NOISE FOR BOOST PFC WITH VARIABLE SWITCHING FREQUENCY

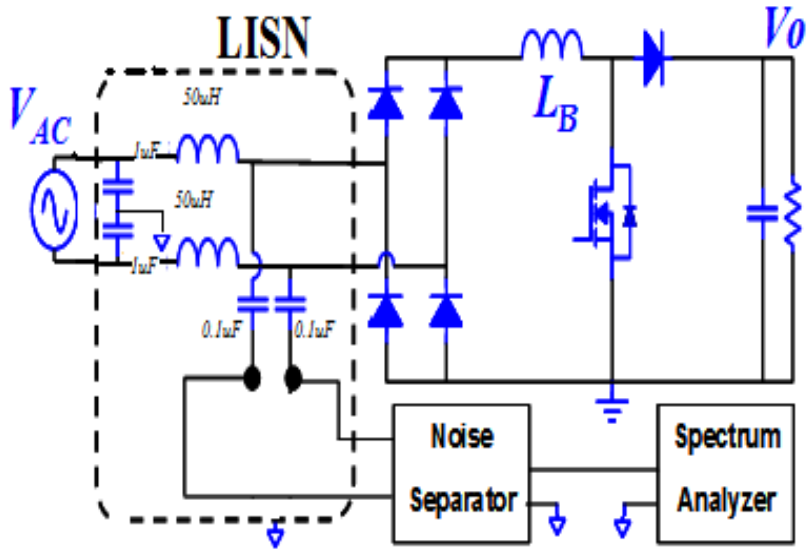

Figure 3.1: Circuit Diagram of the EMI Noise Measurement Set-up for Boost PFC

Based on the discussion in Chapter 2, the circuit diagram of the EMI noise measurement set-up for the boost PFC converter without EMI filter is redrawn in Figure 3.1.

The noise separator is used to separate the CM EMI noise and the DM EMI noise. Design of the noise separator is discussed in [3.1]. According to [3.1], the noise separator is capable of maintaining its input impedance from either input line to the ground to be 50Ω within the measured frequency range, i.e., from 150 kHz to 30 MHz. The two 1μF capacitors in the LISNs are considered as short circuit and the two 50μH inductors in the LISNs are considered as open circuit for the DM EMI noise. The ripple current of the boost inductor current is considered as the noise source, which is a current source. And thus the DM equivalent circuit of Figure 3.1 can be simplified as shown in Figure 3.2.

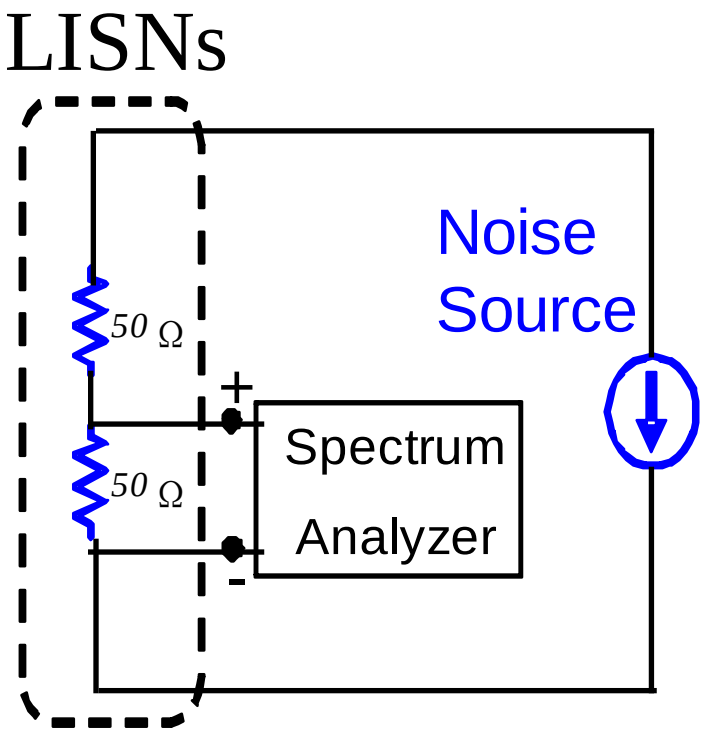

Figure 3.2: Simplified Equivalent Circuit for DM EMI Noise Measurement Set-up

Based on the simplified equivalent circuit in Figure 3.2, the input noise of the EMI spectrum analyzer is actually the voltage drop across the 50Ω resistance.

3.1. Principle of the Quasi-peak EMI Noise Measurement Procedure

There are two types of EMI noise limits as shown in Figure 2.4. Does that mean we should find the worst case for both quasi-peak DM EMI noise and average DM EMI noise for CRM boost PFC?

Figure 3.3 and Figure 3.4 are the quasi-peak DM EMI noise and average DM EMI noise measurements performed by the Agilent E7400A spectrum analyzer, respectively, for a CRM boost PFC at input line V_{RMS}=110V and load Po=150W, with 150uH boost inductor.

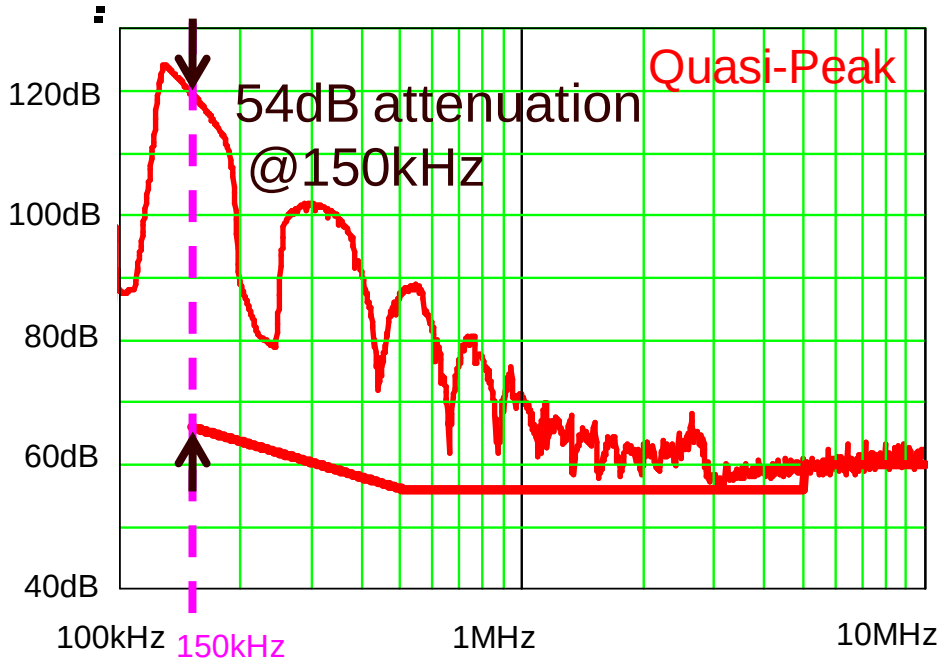

Figure 3.3: Quasi-peak DM EMI Noise Measurement Result for a CRM PFC

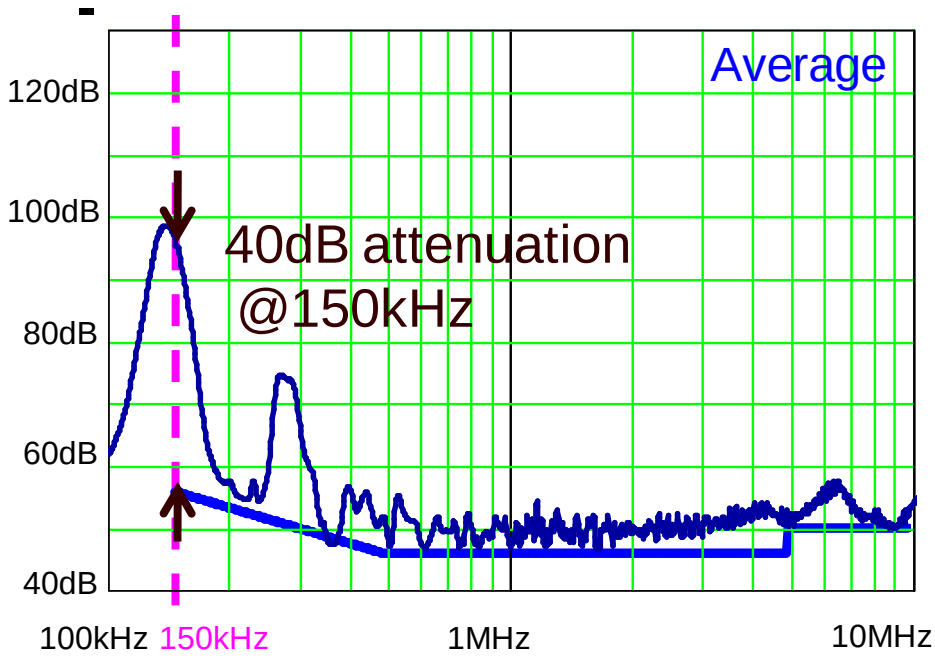

Figure 3.4: Average DM EMI Noise Measurement Result for a CRM PFC

The measured quasi-peak noise need 54dB attenuation at 150 kHz to meet the quasi-peak noise limit and the average noise need 40dB attenuation at 150 kHz to meet the average noise limit. By comparison, the quasi-peak noise needs 14dB more attenuation at 150 kHz than average noise, which means the quasi-peak DM EMI noise will determine the corner frequency of the DM EMI filter and the filter should

be designed based the quasi-peak DM EMI noise.

The average noise in CRM boost PFC is at quite low magnitude. For CRM boost PFC which is variable switching frequency, the noise energy is distributed in a wide frequency range, so that for certain frequency, the average noise is quite small. The same phenomena also appear in the frequency-modulated CCM boost PFC and the reasons are discussed in [3.2] and [3.3].

Since for boost PFC with variable switching frequency, the quasi-peak noise is dominant, the rest part of this thesis will focus on the quasi-peak DM EMI noise.

To carry out the quasi-peak noise prediction for CRM boost PFC, the function of the spectrum analyzer when measuring the quasi-peak noise need to be understood. Based on the investigation of the Agilent E7400A spectrum analyzer [3.4], a simplified diagram is shown in Figure 3.5 to illustrate the main procedure of measuring quasi-peak noise.

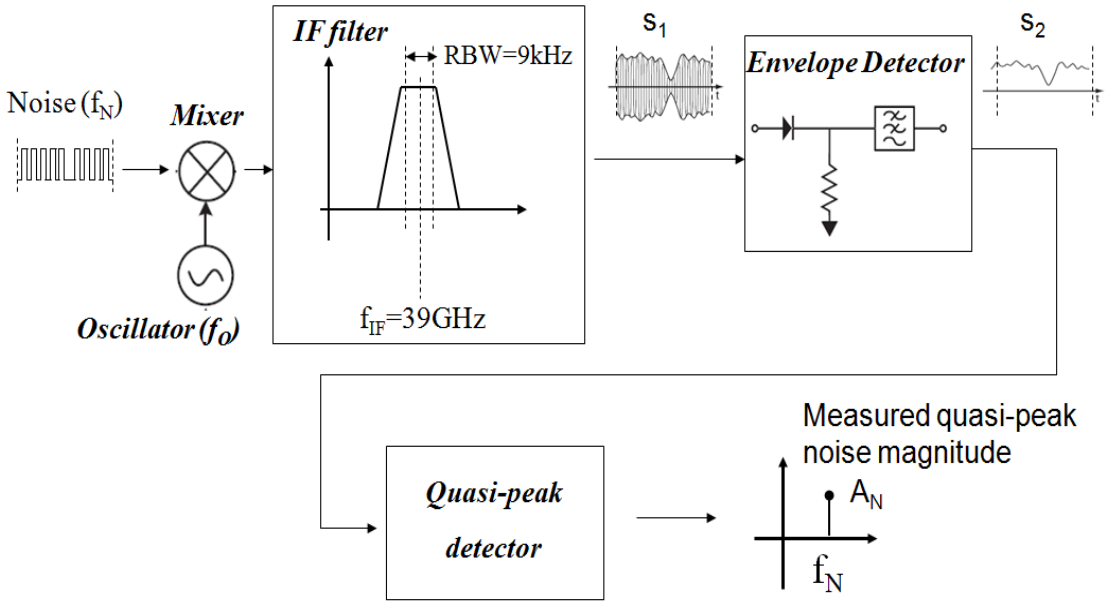

Figure 3.5: Simplified Quasi-peak Noise Measurement Procedure

Mixed with the oscillator signal of the tunable frequency fo, the noise component with frequency f_N will be translated to frequency fo-f_N and fo+f_N in frequency domain. If set fo = f_N + f_{IF}, then the noise signal with frequency fo-f_N will pass the intermediate frequency (IF) filter with 9kHz bandwidth.

Combined with the function of the oscillator and the mixer, the IF filter

equivalently can be seen as a band-pass filter with the tunable center frequency Then the diagram can be further simplified as in Figure 3.6, with the quasi-peak detector modeled in [3.5].

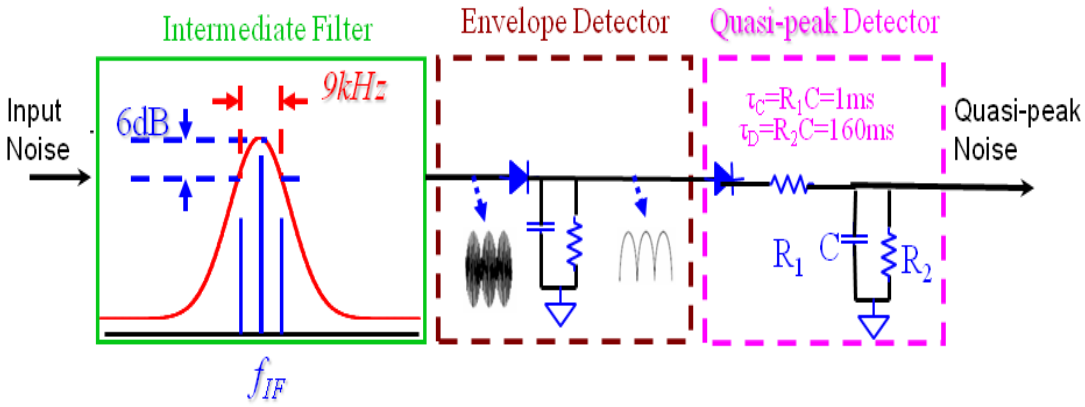

Figure 3.6: Simplified Block Diagram for EMI Spectrum Analyzer in Quasi-Peak Detection Mode

Combine Figure 3.2 and Figure 3.6, the complete equivalent circuit for quasi-peak DM EMI noise measurement is obtained. Now the question is how the measurement is proceeding. Based on the investigation and understanding of the quasi-peak detection process in Figure 3.5, an exemplar illustration of the measurement process is shown in Figure 3.7.

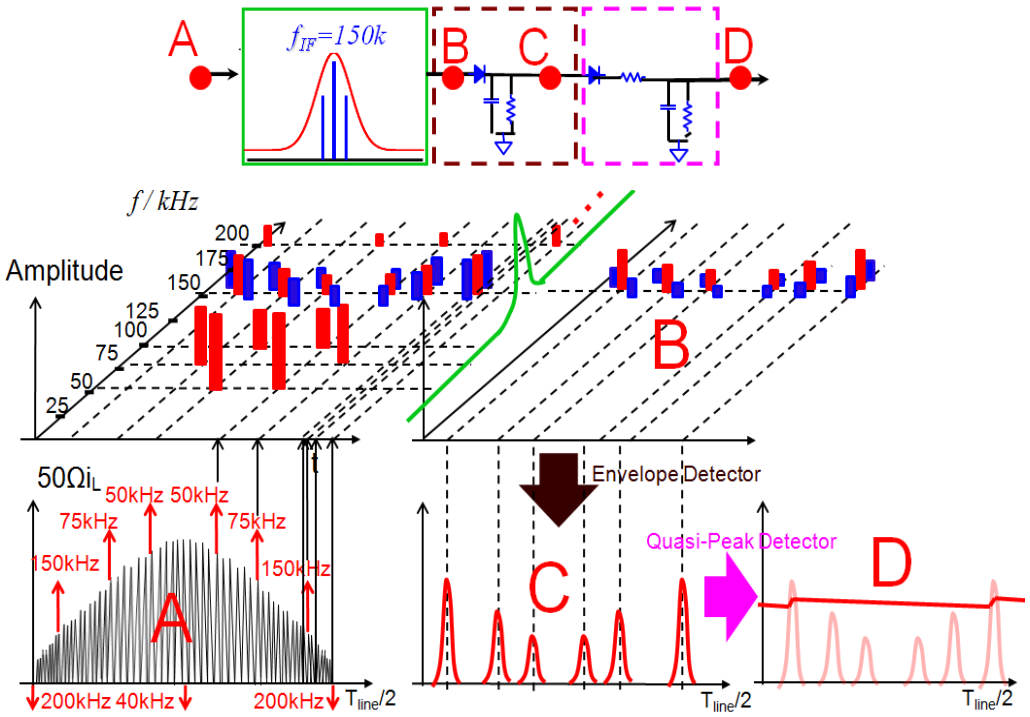

Figure 3.7: Illustration of the Principle of the Quasi-peak DM EMI Noise Measurement for Boost PFC with Variable Switching Frequency

Because the EMI standard starts to limit the EMI noise from 150 kHz, here the intermediate frequency for the intermediate filter is initially selected to be 150 kHz as an example.

At the top of Figure 3.7, the simplified block diagram for the EMI spectrum analyzer is shown to make the process easy to understand, with capital letter “A” standing for the input noise voltage, “B” for output of the intermediate filter and input of the envelope detector, “C” for output of the envelope detector and input of the quasi-peak detector and “D” for the measured quasi-peak noise at given intermediate frequency.

At “A”, triangular inductor ripple current with switching frequency range from 40 kHz to 200 kHz is used as an example. Because the switching frequency is very high, we assume the frequency of the triangular waveform is changing continuously. That means, there should exist triangular waveforms with frequency equals to 50 kHz, 75 kHz and 150 kHz, respectively.

To make the measuring process more clear, the time-domain ripple current waveforms is then transferred to time and frequency domain upward, with x axis as the time, y axis as the frequency, and z axis as the amplitude of the harmonic current.

As shown in Figure 3.7, at the beginning of a half line cycle, the triangular ripple current with frequency equal to 200kHz will cause harmonic currents at 200kHz, 400kHz, 600kHz and so on and so forth. A red bar is used in the time and frequency domain to represent the amplitude of the harmonic current. Here, only the 200kHz harmonic current is listed and for simplicity higher order harmonic currents are ignored.

With the time moving on, the frequency of the triangular waveform change. At a certain time, the triangular waveform with the frequency equal to 150kHz will appear and cause harmonic currents and 150kHz, 300kHz, 450kHz, and so on and so forth. Only the 150 kHz harmonic current is listed and others are ignored.

With the same principle, the 75kHz and 150kHz harmonic currents caused by the triangular ripple current with the frequency equal to 75kHz and the 50kHz, 100kHz,

150kHz and 200kHz harmonics currents caused by the triangular ripple current with the frequency equal to 50kHz are all listed on the time and frequency domain with the red bars.

Around the time when the triangular ripple current with the frequency equal to 150 kHz appears, there are two triangular ripple currents with the frequency equal to the (150±ζ) kHz before and after it. Here ζ kHz represents the very small frequency difference between two consecutive single-triangular waveforms. The two triangular ripple currents with the frequency equal to (150±ζ) kHz will cause harmonic currents and (150±ζ) kHz, (300±2ζ) kHz, (450±3ζ) kHz, and so on and so forth. Only the (150±ζ) kHz harmonic currents are listed with two blue bars and others are ignored.

With the same principle, the (150±2ζ) kHz harmonic currents caused by the triangular ripple current with the frequency equal to (75±ζ) kHz and the (150kHz±3ζ) kHz harmonics currents caused by the triangular ripple current with the frequency equal to (50±ζ) kHz are all listed on the time and frequency domain with the blue bars.

All the harmonic current components need to pass the intermediate filter before it can contribute to the final quasi-peak noise. Since the intermediate filter is a 9 kHz bandwidth filter with 6dB attenuation, and for this example intermediate frequency is equal to 150 kHz, only 150 kHz harmonic current and harmonic currents with close-by frequency can pass through the intermediate filter. All the other harmonic current components are filtered out.

Therefore, at “B”, all the 150 kHz harmonic currents pass the intermediate filter without any attenuation, shown as the red bars. And all the harmonic currents with frequency close to 150 kHz also pass the intermediate filter, but attenuated to some extent, shown as the blue bars.

Not all the harmonic component with frequency close to 150 kHz are listed or shown at “B”. For example, the (150±2ζ) kHz harmonic currents caused by the triangular ripple currents with the frequency equal to (150±2ζ) kHz are not. This is to make the figure compact and tidy. If all the harmonic currents with frequency close to

150 kHz are listed, then the red and blue bars at “B” will make a continuous curve. This continuous curve is the amplitude envelope of all the harmonic current components.

The function of the envelope detector is just to catch this amplitude envelope. As a peak detector, the envelope detector actually eliminates the frequency related information and only keeps the amplitude information. Then the harmonic current components in time and frequency domain at “B” can be mapped to the time domain at “C”.

This amplitude envelope will then be fed into the quasi-peak detector, a charging and discharging nonlinear network specified in [2.2]. Because the charging time constant is much smaller than the discharging time constant, it will be very quick for the voltage across the output capacitor of the quasi-peak detector to increase to a steady state value. After it is in steady state, the charge and discharge of the output capacitor in a half line cycle should reach a balance. Generally because the charging time is quite a small part of the half line cycle, the voltage ripple of the output capacitor is neglected and the steady state value thus could be predicted based on the charging balance and the quasi-peak noise for given intermediate frequency is then obtained.

During this measuring process, one of the characteristics of the PFC converter helps to reduce the complexity of the principle. That is, the minimum switching frequency for the PFC converter has to be always above 20 kHz to avoid generating any audible noise. This means that for two consecutive orders of harmonics currents, the frequency difference is at least 20 kHz and if one is falling in the bandwidth of the intermediate filter, another would never appear within the bandwidth. For example, the sixth order harmonic current of the 25 kHz triangular ripple current will have contribution to the noise at 150 kHz, but the fifth (125 kHz) or the seventh (175 kHz) order harmonic currents will be totally filtered out and have no impact on the noise at 150 kHz. This leads that, at each time point, only a single bar exists at “B” and makes the mapping from “B” to “C” mathematically possible.

Since the principle of the quasi-peak EMI noise measurement procedure is clear, the mathematical prediction of the quasi-peak DM EMI noise for boost PFC with variable switching frequency could be carried out step by step.

3.2. Model of the Input Noise Voltage

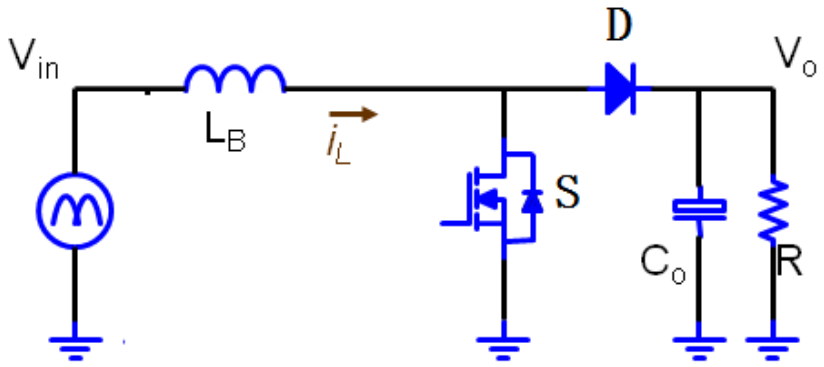

Figure 3.8: Power Stage of Boost PFC

The model of the input noise voltage is essentially the model of the inductor ripple current.

Figure 3.8 is the power stage for boost PFC with all the device, passive components and circuit variables labeled. Take boost PFC in CRM as an example. The sketched waveform for the inductor current is shown in Figure 3.9. For boost PFC with variable switching frequency, Fourier analysis cannot be directly applied to the whole inductor ripple current waveform to extract harmonic current components

However, the PFC circuit is running at high switching frequency and based on the **Quasi-Steady-State** assumption, within a very short time interval, the input voltage can be seen as a constant and the PFC can be seen as a DC-DC boost converter with that constant input voltage. Thus the inductor ripple current can be considered as periodical triangular waveform during that time interval. A zoom-in of the inductor ripple current at the time interval around time point t_0 is shown in Figure 3.10.

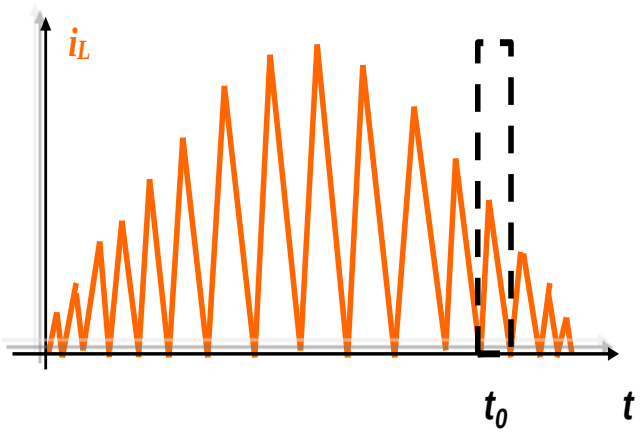

Figure 3.9: Inductor Current Sketch for Boost PFC with Variable Switching Frequency

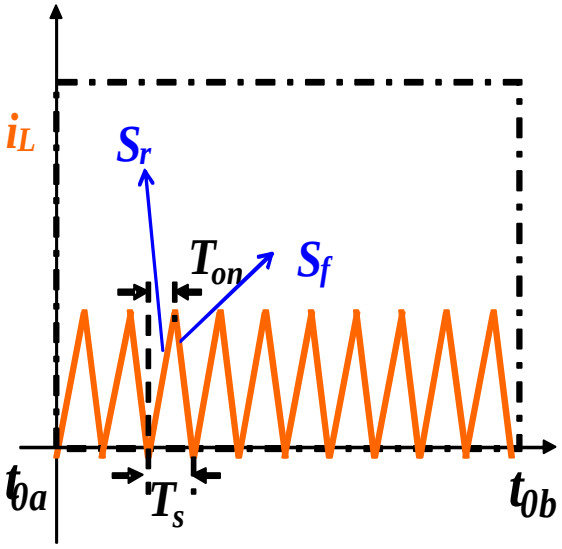

Figure 3.10: Zooming in around time point t_0 in Fig.3.6

For boost PFC converter, according to the voltage-second balance on the boost inductor, the equation below is always true.

$$T_{on}\frac{V_{in}(t_0)}{L_B}=(T_s(t_0)-T_{on})\frac{V_o-V_{in}(t_0)}{L_B} \tag{3.1}$$

Based on Fig. 3.10, the rising slope of the ripple current is,

$$S_r=\frac{V_{in}(t_0)}{L_B}=\left(1-\frac{T_{on}}{T_s(t_0)}\right)\frac{V_o}{L_B} \tag{3.2}$$

And the falling slope of the ripple current is,

$$S_f=\frac{V_o-V_{in}(t_0)}{L_B}=\frac{T_{on}}{T_s(t_0)}\frac{V_o}{L_B} \tag{3.3}$$

Then the ripple current in a switching cycle can be expressed as,

$$i_{rp}(\tau)=\begin{cases} S_r\cdot\tau-\frac{1}{2}S_r\cdot T_{on}=\frac{V_o}{L_B}\left(1-\frac{T_{on}}{T_s(t_0)}\right)\tau-\frac{1}{2}\frac{V_o}{L_B}\left(1-\frac{T_{on}}{T_s(t_0)}\right)T_{on} & 0\le\tau<T_{on} \\ \frac{1}{2}S_r\cdot T_{on}-S_f\cdot(\tau-T_{on})=-\frac{V_o}{L_B}\frac{T_{on}}{T_s(t_0)}\tau+\frac{1}{2}\frac{V_o}{L_B}\left(1+\frac{T_{on}}{T_s(t_0)}\right)T_{on} & T_{on}\le\tau<T_s(t_0) \end{cases} \quad (3.4)$$

Apply Fourier transformation to this periodical triangular waveform at the time interval around time point t_0 and the harmonic current amplitude can be derived as,

$$|i_k(f_s(t_0))|=\frac{1}{k^2}\frac{V_o}{L_B}\frac{1}{2\pi^2 f_s(t_0)}|e^{-jk2\pi f_s(t_0)T_{on}}-1| \quad (3.5)$$

Where,

$$f_s(t_0)=\frac{1}{T_s(t_0)} \quad (3.6)$$

And ***k*** is the order number of harmonic current and ***k***=1, 2, 3…, which are shown in Figure 3.11,

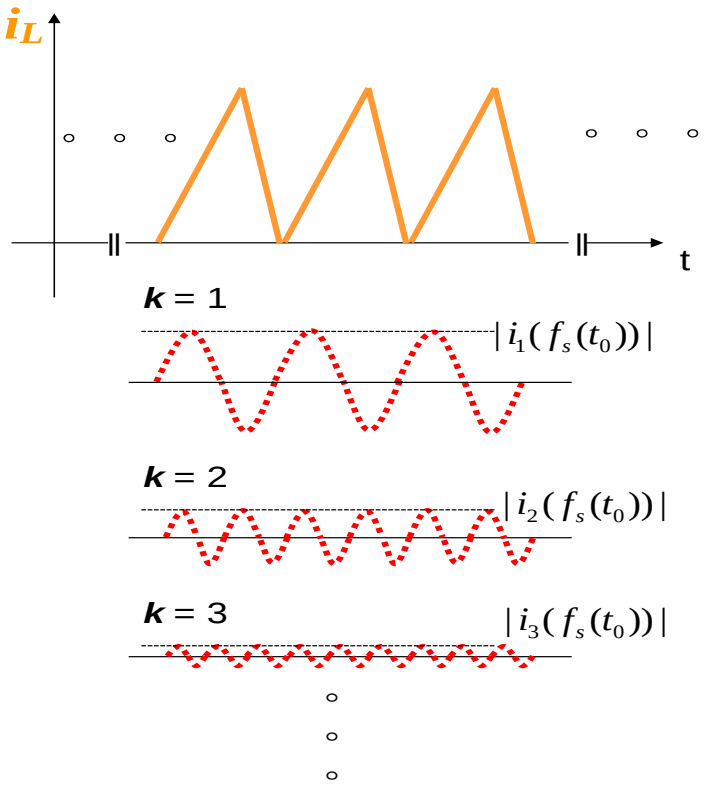

Figure 3.11 Harmonic Current Amplitude at Given Time Interval

Please note that phase information for each order harmonic current is not

interesting and thus not calculated and emphasized.

Equation 3.5 is applicable for the whole half line cycle, thus,

$$|i_k(f_s(t))| = \frac{1}{k^2}\frac{V_o}{L_B}\frac{1}{2\pi^2 f_s(t)}|e^{-jk2\pi f_s(t)T_{on}} - 1| \tag{3.7}$$

Where,

$$f_s(t) = \frac{1}{T_s(t)} \tag{3.8}$$

And ***k*** is the order number of harmonic current and ***k***=1, 2, 3…, which can be shown in Figure 3.12,

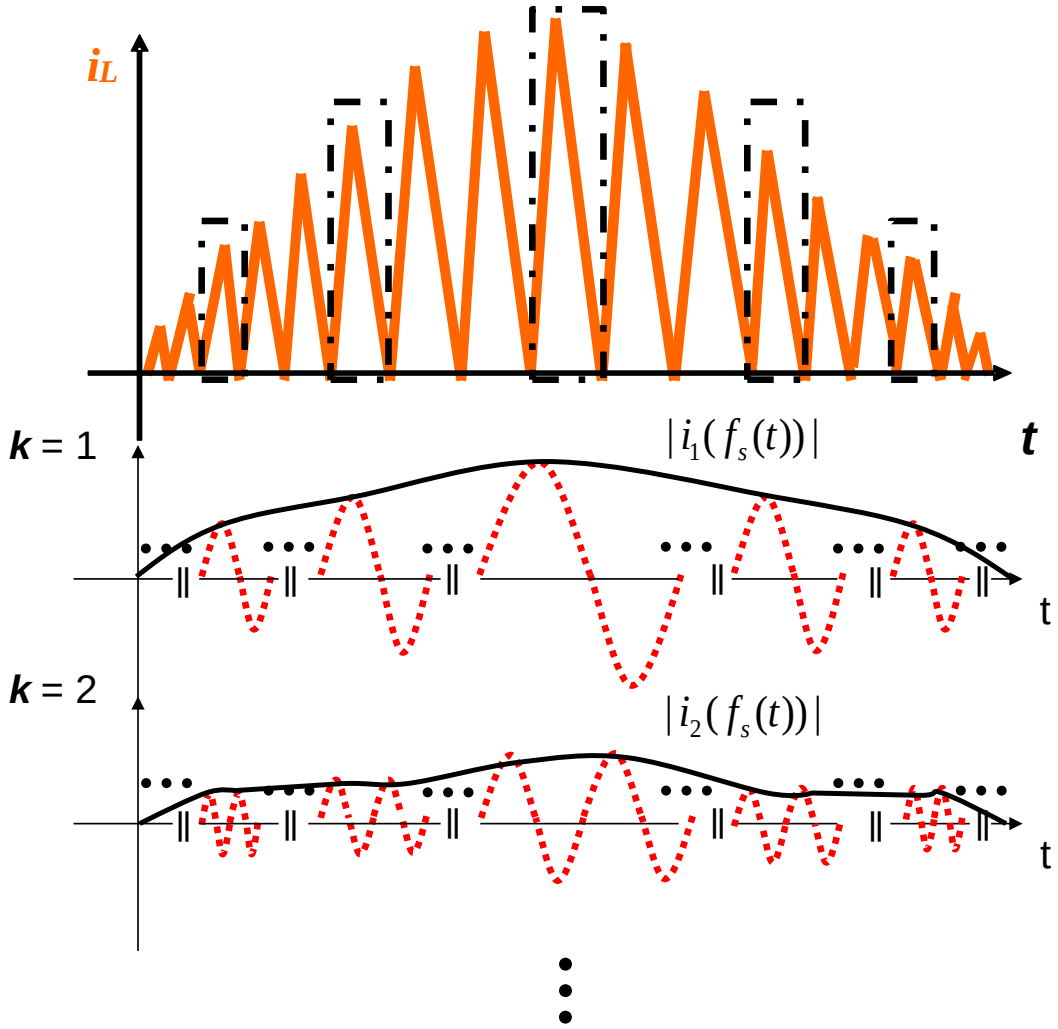

Figure 3.12: Harmonic Current Amplitude for Half Line Cycle

In some cases if the boost PFC with variable switching frequency operates in DCM,

with dead time T_{dead}, then Equation 3.7 could be re-derived as,

$$|i_k(f_s(t))| = \frac{1}{k^2}\frac{V_o}{L_B}\frac{1}{2\pi^2 f_s(t)}\left|\left(e^{-jk2\pi f_s(t)T_{on}}-1\right)-\frac{T_{on}}{\frac{1}{f_s(t)}-T_{dead}}\left(e^{-jk2\pi\left(1-f_s(t)T_{dead}\right)}-1\right)\right| \quad (3.9)$$

Where, T_{dead} can be either variable or constant over a half line cycle, determined by the specific control scheme.

Thus the harmonic current frequency and its related amplitude information have already been modeled and will be used in the following noise prediction.

3.3. Model of the Intermediate Frequency Filter

All the harmonic current components first need to pass through the intermediate frequency filter. What we most care about is the gain characteristics of the intermediate frequency filter. In the EMC standard [2.2], the gain characteristics has been specified, which is shown in Figure 3.13.

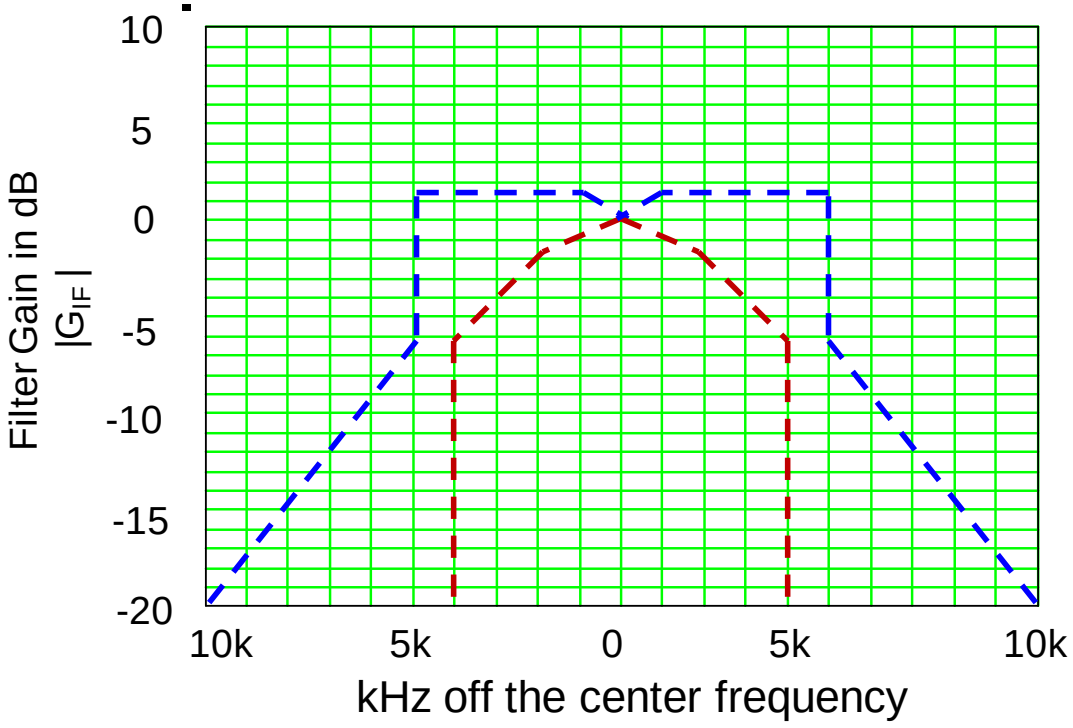

Figure 3.13: Gain Characteristics of IF Filter Specified by IEC CISPR 16-1-1

As shown in Figure 3.13, the x axis is the frequency difference between the frequency of the input noise voltage and the intermediate frequency. The y axis is the

corresponding attenuation to the input noise voltage that the intermediate frequency filter need to achieve for given frequency difference There are two dashed curves in Figure 3.13. The blue dashed curve is the upper attenuation limit and the maroon dashed curve is the lower attenuation limit. The gain characteristics of the intermediate frequency filter in the spectrum analyzer need to fall between these two attenuation limits. First, when the frequency of the input noise voltage is equal to the intermediate frequency, i.e., the frequency difference is zero, the attenuation should also be zero. This means no attenuation for the input noise voltage at the intermediate frequency, which is already shown in Figure 3.7. Second, for frequency difference between 4 kHz to 5 kHz, 6dB attenuation needs to be achieved. Therefore generally the intermediate frequency filter is characterized as 9 kHz bandwidth with 6dB attenuation.

The actual gain characteristics of the IF filter for different analog spectrum analyzer should be different and are not known. For the most direct way, either the upper lime or the lower limit can be used as the actual gain characteristics. However, it is hard to achieve such gain characteristics for IF filter. A classical type of filer with similar gain characteristics is the Gaussian filter. Is it possible to use Gaussian filter to describe the intermediate filter?

The equation for the gain characteristics of the Gaussian filter is,

$$|G(\Delta f)| = \frac{1}{\sqrt{2\pi}\cdot\sigma} e^{-\frac{(\Delta f)^2}{2\sigma^2}} \tag{3.10}$$

Based on the short discussion about the gain characteristics of the IF filter specified in the EMC standard, Equation 3.10 should satisfy the following two equations,

$$|G(\Delta f = 0)| = 0dB \tag{3.11}$$

and

$$|G(\Delta f = \pm 4.5kHz)| = -6dB \tag{3.12}$$

Because there is only one parameter σ in Equation 3.10, it is impossible for it to satisfy both Equation 3.11 and Equation 3.12. However, if we simply ignore the non-exponential part in Equation 3.10, then the Equation 3.11would be satisfied

naturally. Then based on the Equation 3.12, we can solve that,

$$\sigma = \frac{9k}{2\sqrt{2\ln 2}} \tag{3.13}$$

Thus, the equation of the gain characteristics of the IF filter can be expressed as,

$$|G_{IF}(f, f_{IF})| = e^{-\frac{(f-f_{IF})^2}{c^2}} \tag{3.14}$$

Where,

$$c = \sqrt{2}\sigma = \frac{9k}{2\sqrt{\ln 2}} \tag{3.15}$$

and f is the frequency of the input noise voltage and f_{IF} is the intermediate frequency.

Equation 3.14 can be seen as the expression for gain characteristics of a near Gaussian filter, which is also mentioned in [3.6].

The gain curve for Equation 3.14 is drawn in Figure 3.14 as the red solid curve and compared with the limit specified by the EMC standard. We can see the gain curve expressed with the modified gain equation fit in the limits very well. It will be good to filter the harmonic currents modeled in Section 3.2.

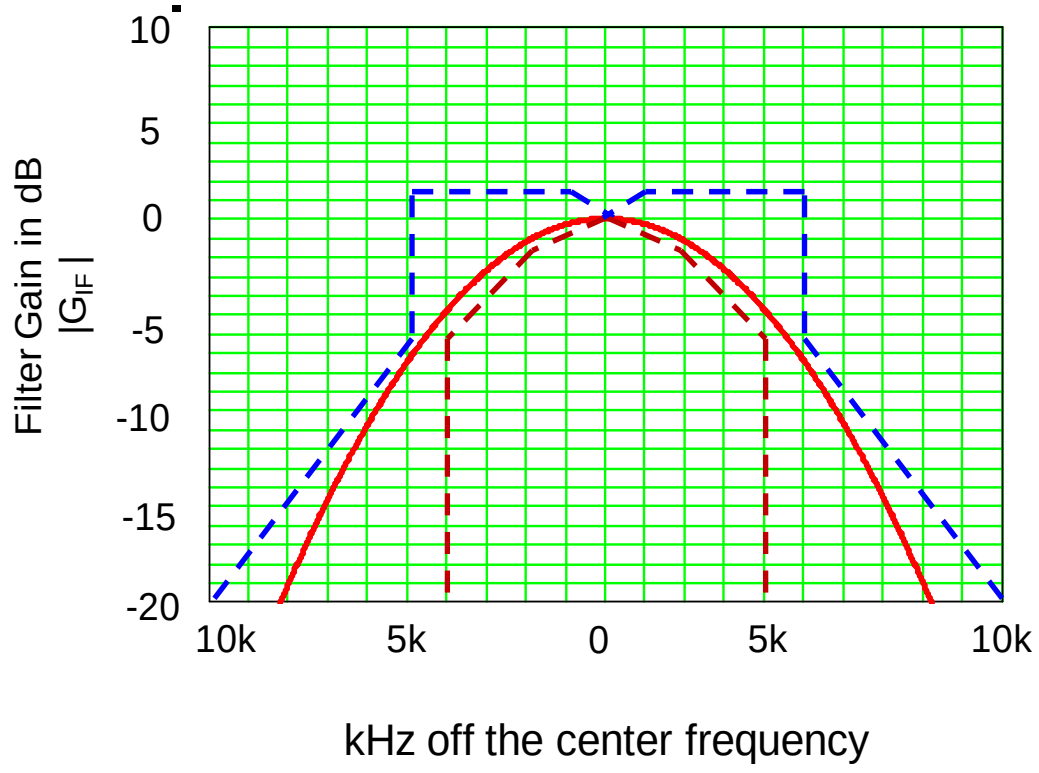

Figure 3.14: Comparison between Proposed Gain Characteristics and Limits by EMC Standard

3.4. Model of the Output of the Envelope Detector

For kth order input voltage noise, the equation of its amplitude over half-line cycle can be expressed as,

$$V_k(t) = 50\Omega \cdot |\, i_k(f_s(t))\,| \tag{3.16}$$

And after passing the IF filter, it will be selectively attenuated. These attenuated high frequency sinusoidal-shaped noise waveforms will continuously pass through the envelope detector. For the kth order noise voltage, the output of the envelope detector would be, shown in Figure 3.15,

$$V_k(t, f_{IF}) = 50\Omega \cdot |\, i_k(f_s(t))\,| \cdot |\, G_{IF}(kf_s(t), f_{IF})\,| \tag{3.17}$$

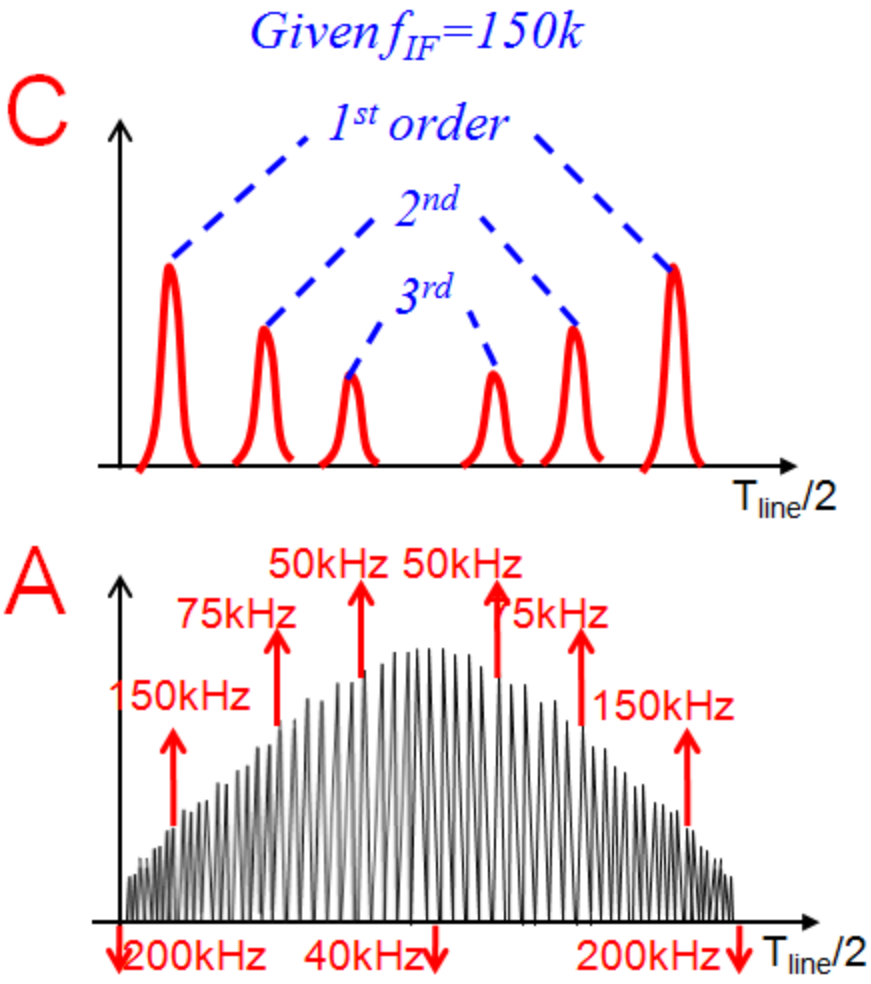

Figure 3.15: Output of the Envelop Detector for the Typical Example

All of these envelope plateaus at "C" are caused by difference order harmonic component and thus appear at different period of the half line cycle. The total output

of the envelop detector would be the sum of all the plateaus,

$$V_{Envelope}(t, f_{IF}) = \sum_{1}^{N} V_k(t, f_{IF}) \tag{3.18}$$

Where,

$$N = [\frac{f_{IF}}{\min f_s}] \tag{3.19}$$

3.5. Calculation of the Quasi-peak Noise for Given f_{IF}

Finally the envelope output described in Equation 3.18 is fed to Quasi-peak detector, which is a charging and discharging network with charging and discharging time constant specified in the standard: charging time constant τ_C=1ms and discharging time constant τ_D=160ms. Because the quasi-peak detector's charge constant is much smaller than the discharge constant, at the beginning the voltage across the output cap will be charged up and finally reach a steady state. This steady state is a charging balance and can be expressed by equation,

$$\int_0^{\Delta T} \left(\frac{V_{Envelope} - V_{Quasi}}{R_1} \right) dt = \frac{V_{Quasi}}{R_2} (\frac{T_{line}}{2} - \Delta T) \tag{3.20}$$

Where, $V_{Envelope}$ is known and V_{Quasi} is the unknown variable. ΔT is the total charging period, which is a function of V_{Quasi}.

The analog circuit for the quasi-peak detector in Figure 3.6 is a possible implementation. The diode is to prevent the output capacitor from discharging through the input side. Since there is a diode in the quasi-peak detection circuit, it is nonlinear and no analytical solution is solved for Equation 3.20.

Based on the charging balance on the output cap, for each given f_{IF}, a dichotomy algorithm is proposed in this thesis to solve Equation 3.20. And then the quasi peak noise value $V_{quasi}(f_{IF})$ can be calculated numerically using this dichotomy algorithm shown in Figure 3.16.

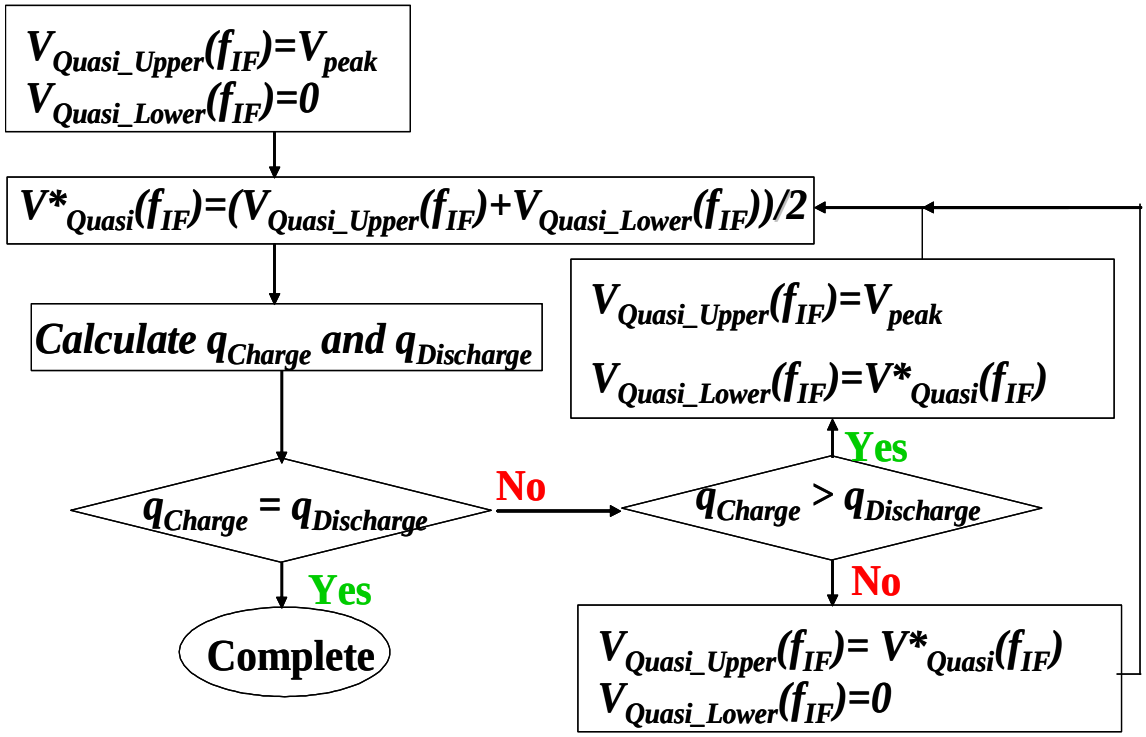

Figure 3.16: Numerical Algorithm Diagram to Calculate Quasi-peak Noise

Generally around 10 iterations, a numerical solution with 0.1% accuracy will be achieved and that is considered $q_{Charge}=q_{Discharge}$ and the algorithm completes. Finally we obtain the value of V_{quasi} for an intermediate frequency f_{IF}. The whole noise spectrum results can be obtained by sweeping f_{IF} from 150 kHz to 30MHz. However, when the noise frequency is up to several mega hertz, the circuit parasitic parameter such as the equivalent parallel capacitance of the boost inductor will come into playing an important role and weaken the accuracy of the prediction [2.3]. In this paper, only noise at low frequency range from 150 kHz to 1MHz, which determines the selection of the EMI filter inductance and capacitance [1.15], is considered, considering generally minimum switching frequency for PFC converters would be far below 1 MHz.

All above discussion since Section 3.2 only give us one data point, the quasi-peak DM EMI noise value for one given intermediate frequency. We can sweep f_{IF} from 100 kHz to 1 MHz and obtain the desired noise spectrum in the following section.

3.6. DM EMI noise prediction and verification based on the EMI noise measurement

To verify the validity of the prediction, measurements should be made to compare with the prediction.

Thus, a digitally controlled constant on time PFC is built in the CPES [3.7] to verify the approximate mathematical model. This constant-on time PFC is variable switching frequency. The control diagram is shown in Figure 3.17 and Figure 3.18. This constant on time PFC is able to run at CCM, CRM or DCM, with the typical waveform sketches in Figure 3.19, Figure 3.20 and Figure 3.21, respectively.

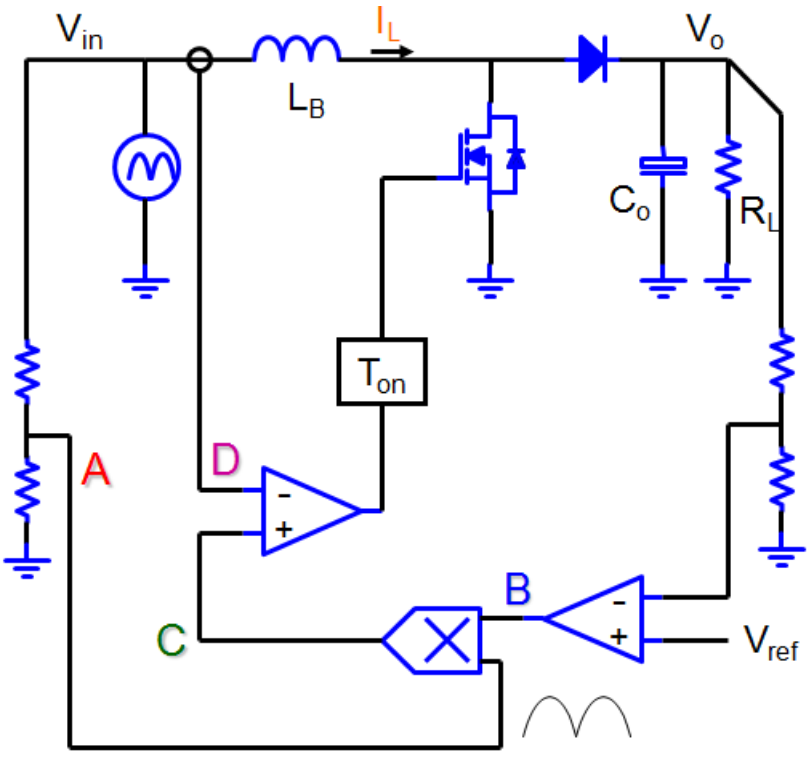

Figure 3.17: Control Scheme for Generalized Constant On-time PFC in CCM or CRM

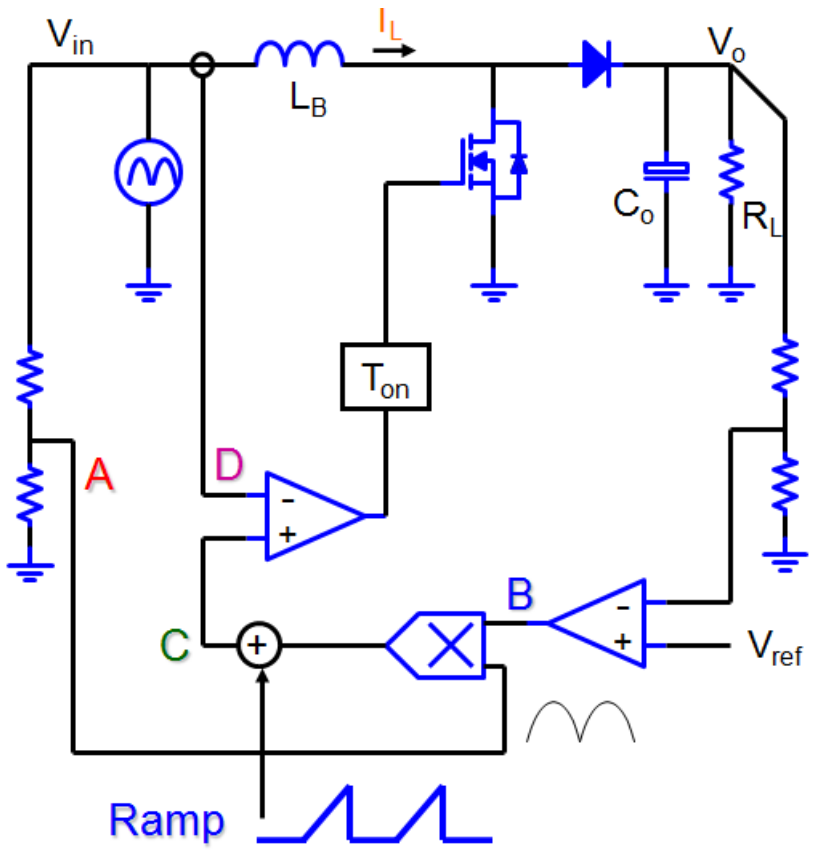

Figure 3.18: Control Scheme for Generalized Constant On-time PFC in DCM

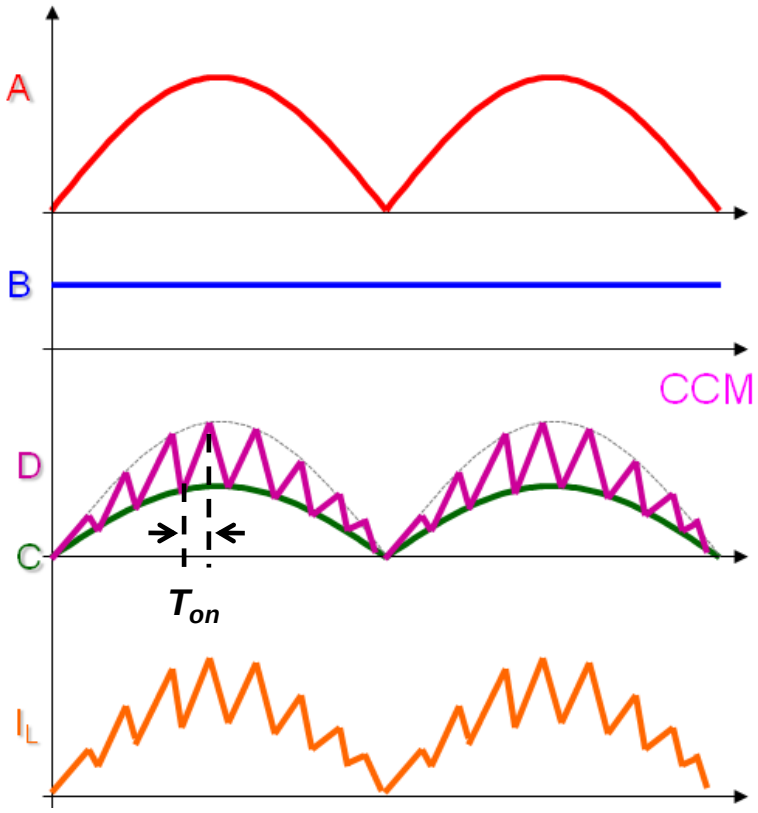

Figure 3.19 Typical Waveform Sketches for Constant On-time PFC in CCM

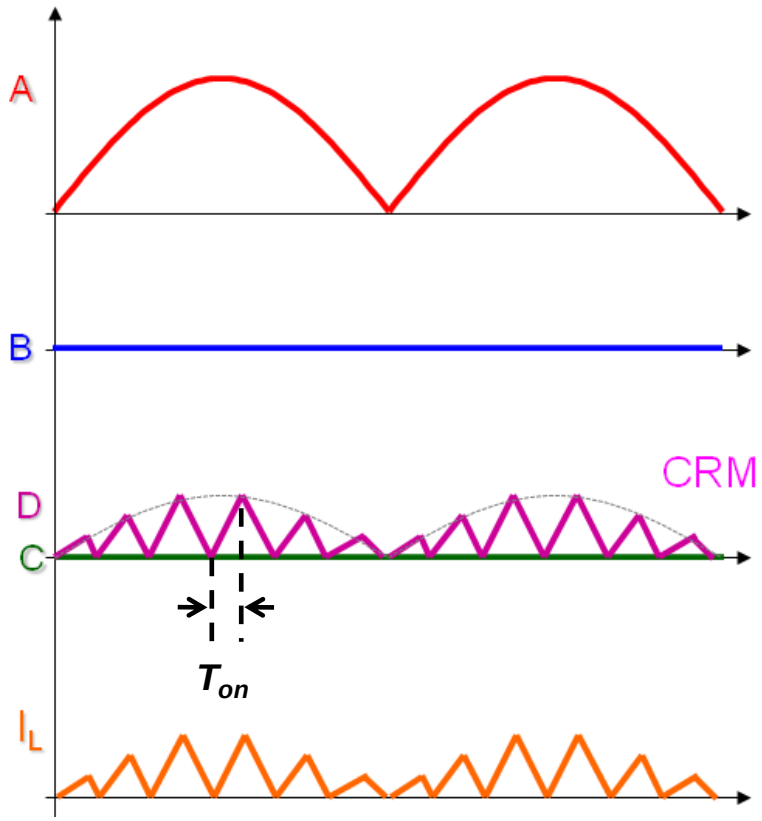

Figure 3.20: Typical Waveform Sketches for Constant On-time PFC in CRM

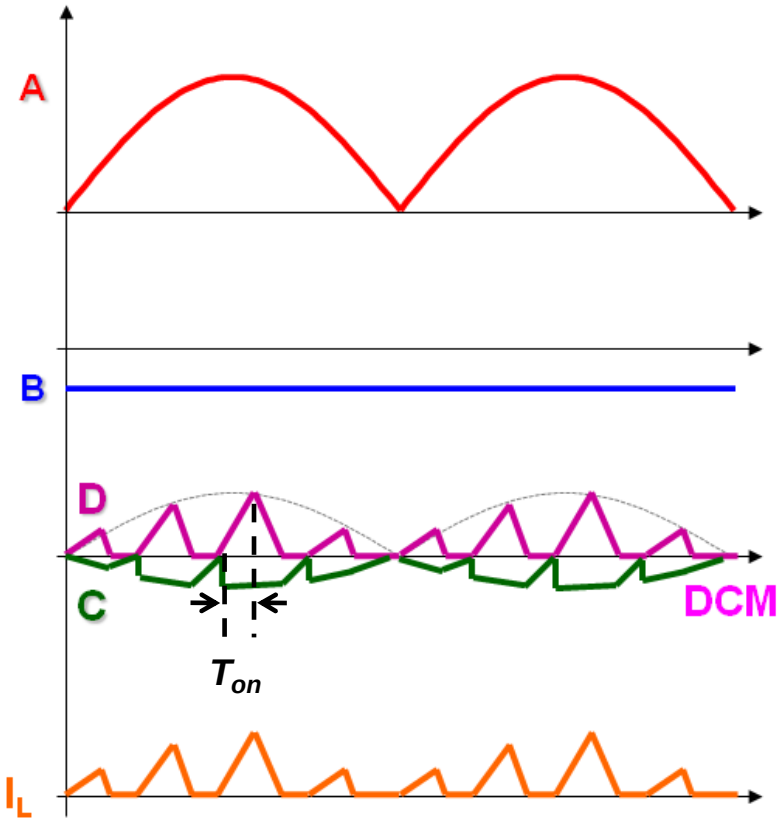

Figure 3.21: Typical Waveform Sketches for Constant On-time PFC in DCM

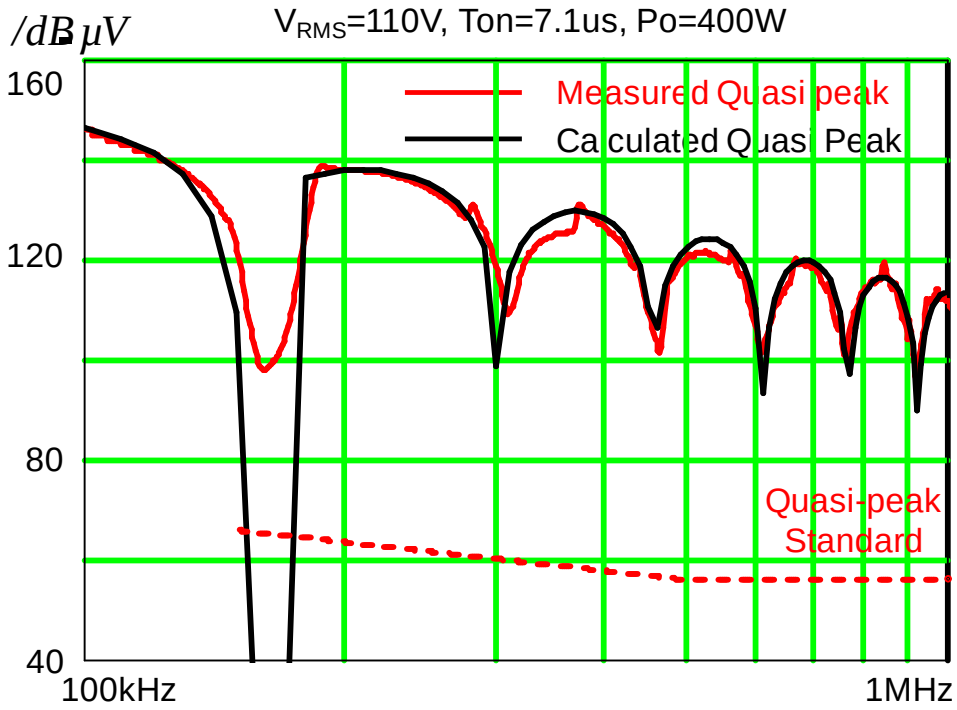

Figure 3.22: Quasi-peak DM Noise Comparison for Constant On-time PFC in CCM(CRM)

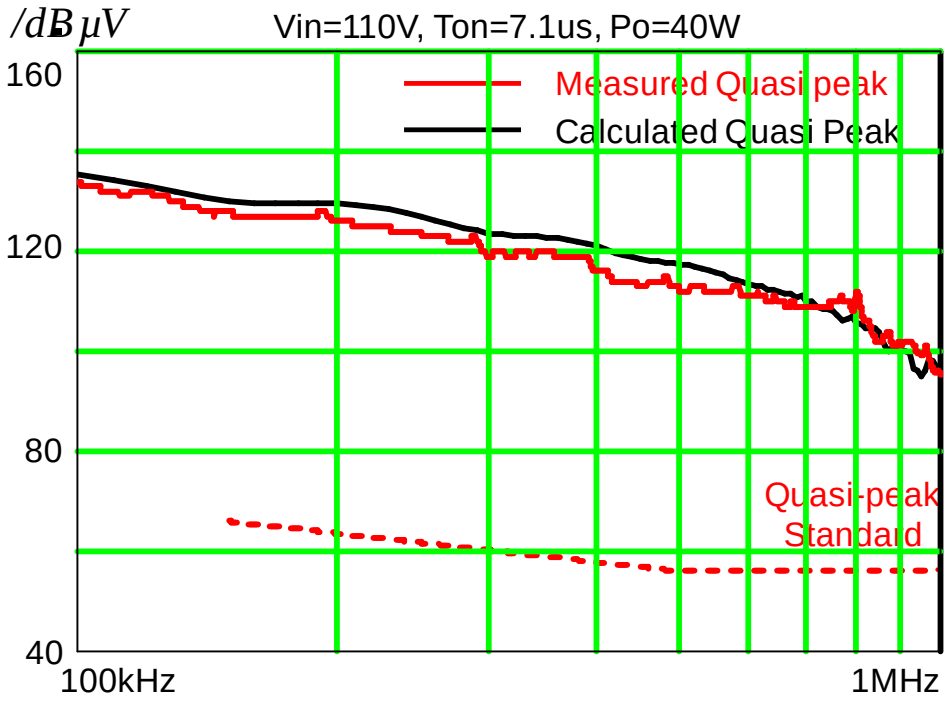

Figure 3.23: Quasi-peak DM Noise Comparison for Constant On-time PFC in DCM

Since the inductor current ripple in CCM and CRM are exactly the same, they would generate the same DM EMI noise. Figure 3,22 and Figure 3.23 show predicted DM EMI noise and measured DM EMI noise comparison for CCM(CRM) and DCM

cases, respectively, all with the same constant on time Ton=7.1us.

Based on the comparison we can see that the proposed mathematical model is good enough to predict the DM EMI noise and evaluate the EMI performance for boost PFC with variable switching frequency and it will be used in the DM EMI noise analysis for single channel and interleaved boost PFC in CRM, which is also variable switching frequency, in Chapter 4.

Chapter 4. DIFFERENTIAL MODE EMI NOISE WORST CASE ANALYSIS FOR BOOST PFC IN CRITICAL CONDUCTION MODE

The prediction of the EMI noise is not the final goal. The fundamental reason for the EMI noise prediction is to find the guidance that how to design the EMI filter and to reduce the whole converter size. In order to design an EMI filter to meet the EMC standard in all line and load conditions, the worst case for the EMI noise needs to be identified. In this chapter, the worst case analysis for the single channel and interleaved CRM boost PFC is carried out. All the noise used in this chapter is based on the prediction using the mathematical model proposed in Chapter 3.

Based on [2.3], corner frequency of the DM EMI filter would be a good index to evaluate the DM EMI noise. Larger corner frequency means smaller EMI filter size and thus better EMI noise and smaller corner frequency means larger EMI filter size and thus worse EMI noise. So the worst case of the DM EMI noise would be the noise which requires the DM EMI filter with the smallest DM corner frequency.

4.1. DM EMI Noise Worst Case Analysis for Single Boost PFC in CRM

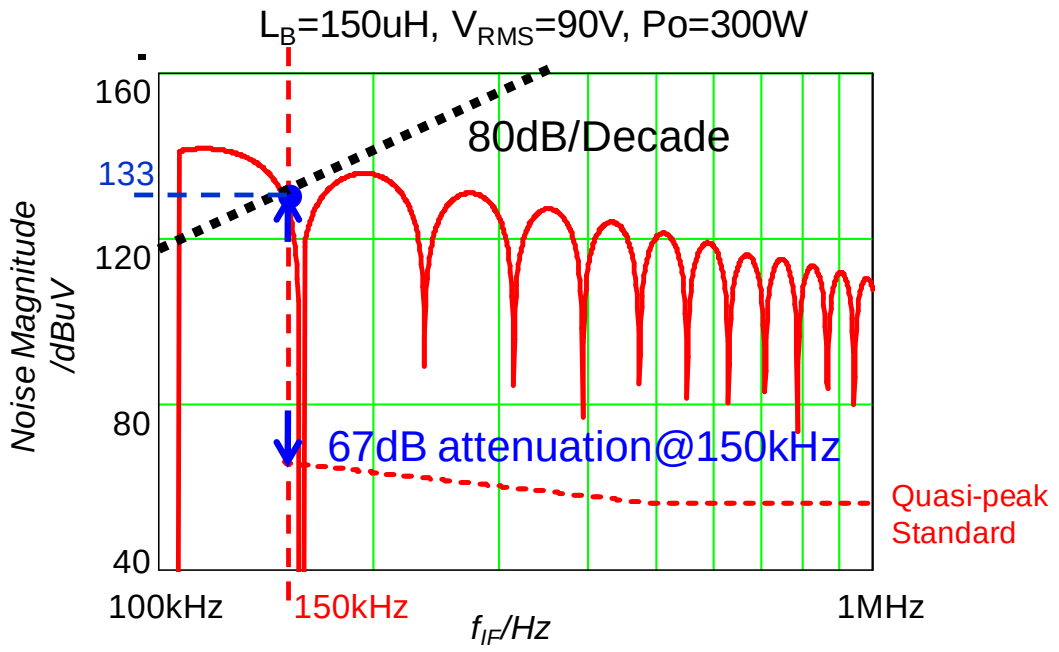

Figure 4.1: DM EMI Noise Prediction Example at Full Load with V_{RMS}=90V for CRM Boost PFC

As shown in Figure 4.1, for quasi-peak DM EMI noise at V_{RMS}=90V, Po=300W, the noise@150kHz is 133dBuV and needs 67dB attenuation to meet the quasi-peak EMI standard. Because the switching frequency range is from 53 kHz to 79 kHz, the noise at 150 kHz is dominated by the second order harmonic component. The black dotted line with 80dB/decade slope represents the slope of the insertion gain of the 2-stage EMI filter, 100dB/decade, plus the slope of the quasi-peak EMI standard from150 kHz to 500 kHz, -20dB/decade. It justifies that if the noise at 150 kHz will be attenuated below the EMI limit by the designed EMI filter, then noise all over the frequency spectrum will also meet the standard. It means for this case, the EMI filter could be designed based on the noise at 150 kHz.

Thus, the corner frequency of the two stage DM EMI filter can be calculate as,

$$f_C = \frac{150kHz}{10^{\frac{67dB}{100dB}}} = 32kHz \tag{4.1}$$

We obtain the first data point for the corner frequency of DM EMI filter.

The quasi-peak DM EMI noise at V_{RMS}=90V, Po=150W is predicted in Figure 4.2.

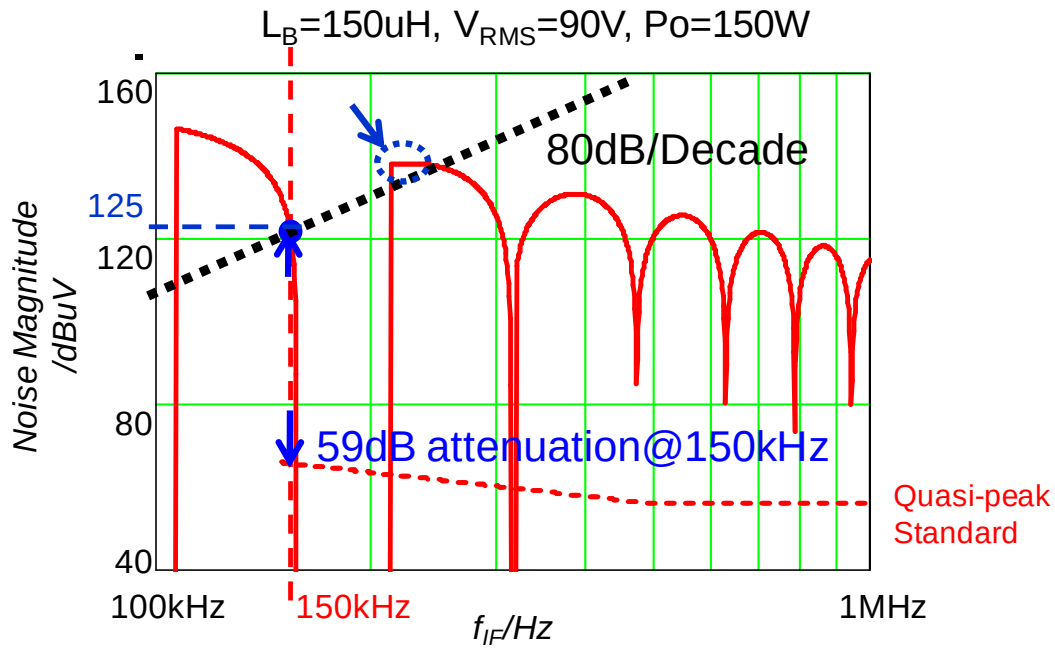

Figure 4.2: DM EMI Noise Prediction Example at Half Load with V_{RMS}=90V for CRM Boost PFC

Because the switching frequency range is from 106 kHz to 158 kHz, the noise at 150 kHz is dominated by the first order harmonic component this time. The noise@150kHz is 125dBuV and needs 59dB attenuation to meet the quasi-peak EMI standard. However, the EMI filter could not be designed based on the noise at 150 kHz this time. We can see that the black dotted line with 80dB/decade slope is below the noise dominated by the second order harmonic components encircled by the blue dotted circle. That means, if we design the DM EMI filter based on the noise at 150 kHz for this case, then at certain frequencies around 200 kHz, the EMI standard will not be satisfied. Thus, the EMI filter should be designed based on the right noise point, shown in Figure 4.3.

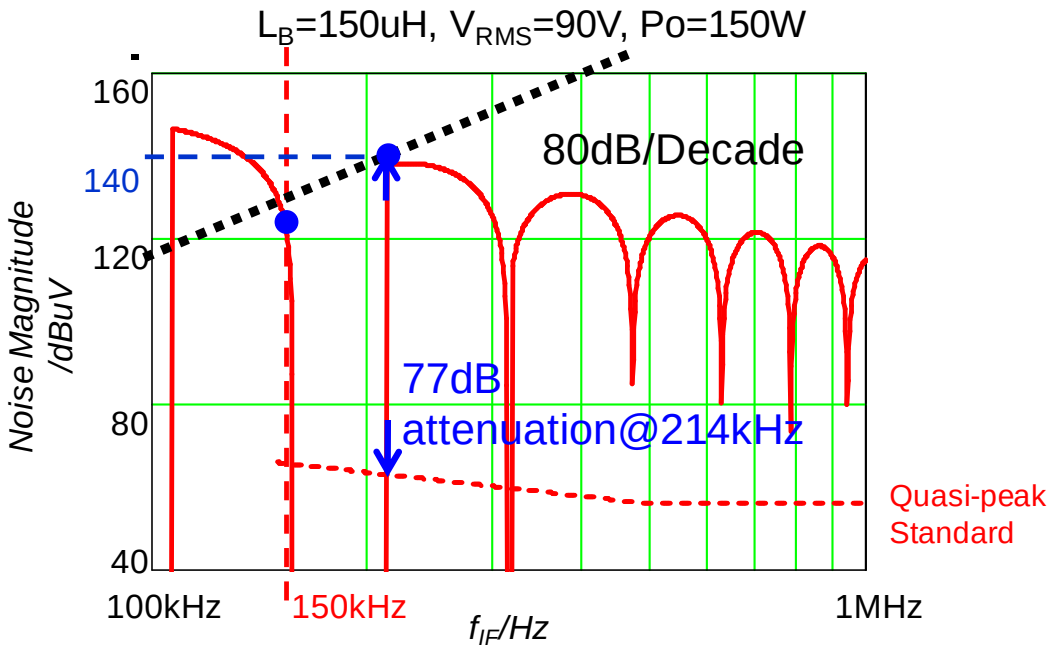

Figure 4.3: Choose Right Noise Point to Design EMI Filter

Thus, the corner frequency of the two stage DM EMI filter can be calculate as,

$$f_C = \frac{214kHz}{10^{\frac{77dB}{100dB}}} = 36kHz \tag{4.2}$$

We obtain another data point for the corner frequency of DM EMI filter.

These two data points can be drawn in Figure 4.4.

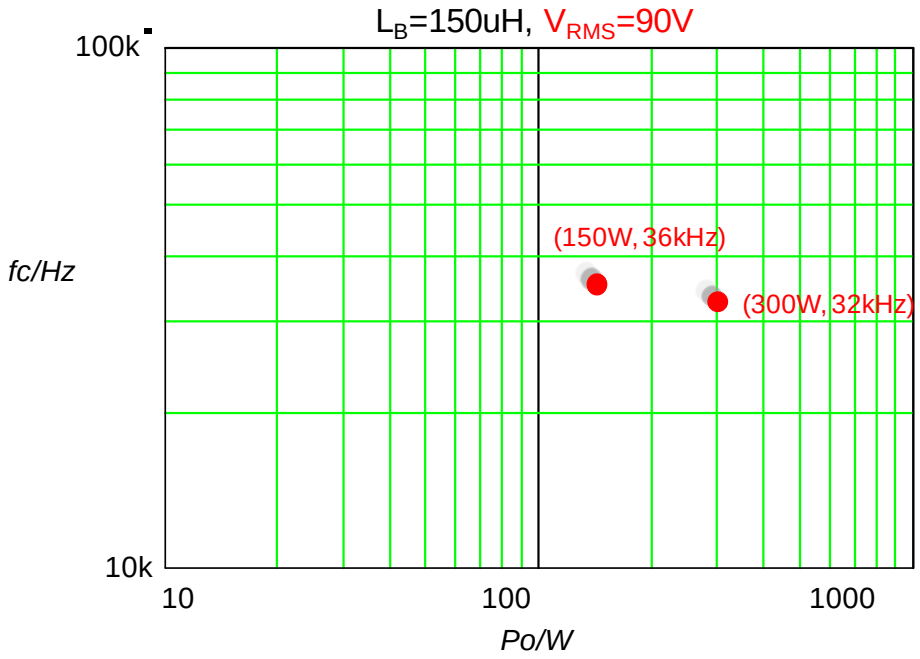

Figure 4.4: Data Points Collection for DM EMI Filter Corner Frequency

The corner frequency of DM EMI filter for 300Watts load is smaller than that for 150Watts, which means it has worse DM EMI noise. If we can draw the corner frequency vs. output power for the whole load range, we should be able to tell what is the worst EMI noise case.

Continue the corner frequency calculation process for the whole load range, we can draw Figure 4.5.

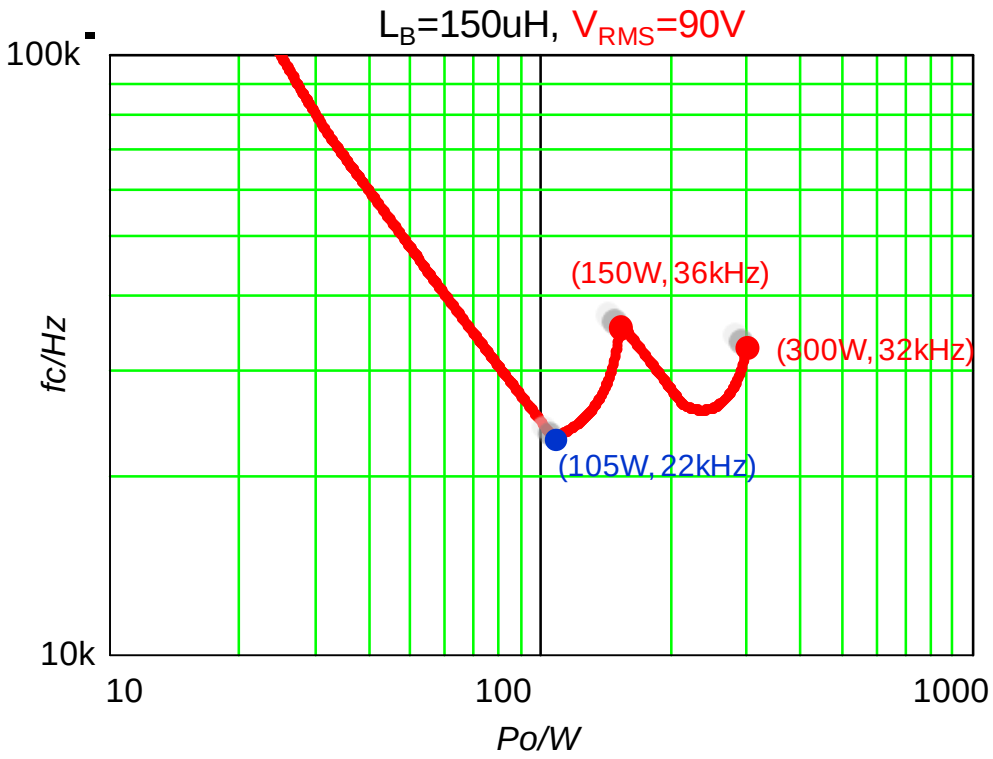

Figure 4.5: Corner Frequency vs. Output Power for V_{RMS}=90V

Thus the worst DM EMI noise case for V_{RMS}=90V is at 105W. The predicted DM EMI noise can be drawn in Figure 4.6.

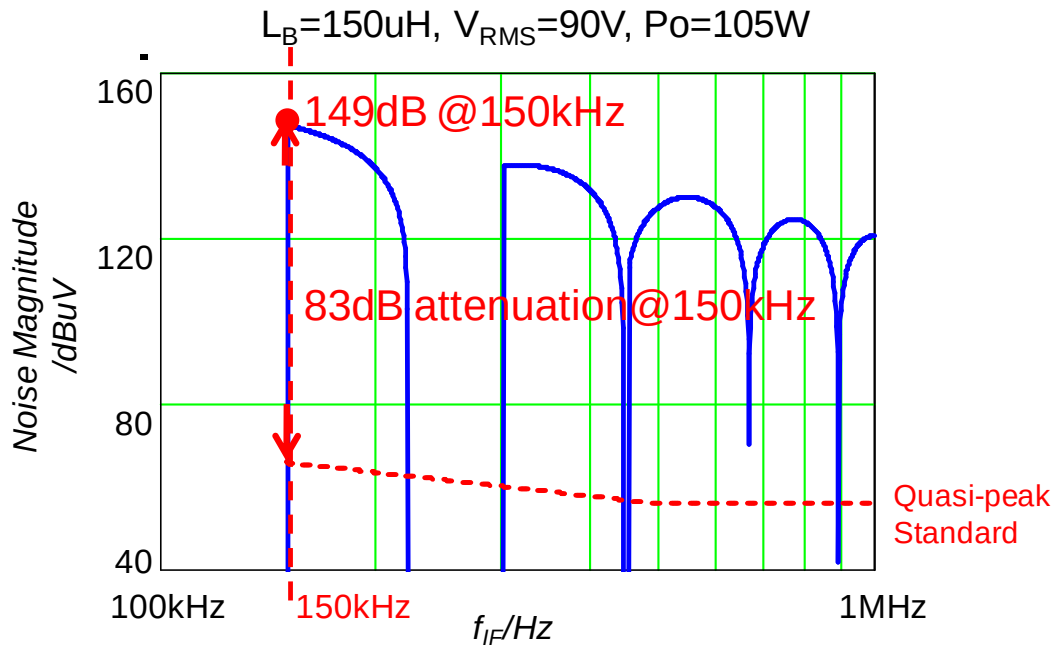

Figure 4.6 Worst DM EMI Noise Case for V_{RMS}=90V

We can see that the peak noise point is just at 150 kHz. And actually the switching frequency range for V_{RMS}=90V, P_O=105W is from 150 kHz to 222 kHz. Thus the first order harmonic component of the 150 kHz current ripple results in the high magnitude noise at 150 kHz, which dominates the EMI filter design.

This worst case is only the local worst case for the V_{RMS}=90V, not the global worst case until all the line conditions are considered. Based on the same principle, Figure 4.7-4.9 show the corner frequency vs. output power for V_{RMS}=110V, 220V, 265V, respectively.

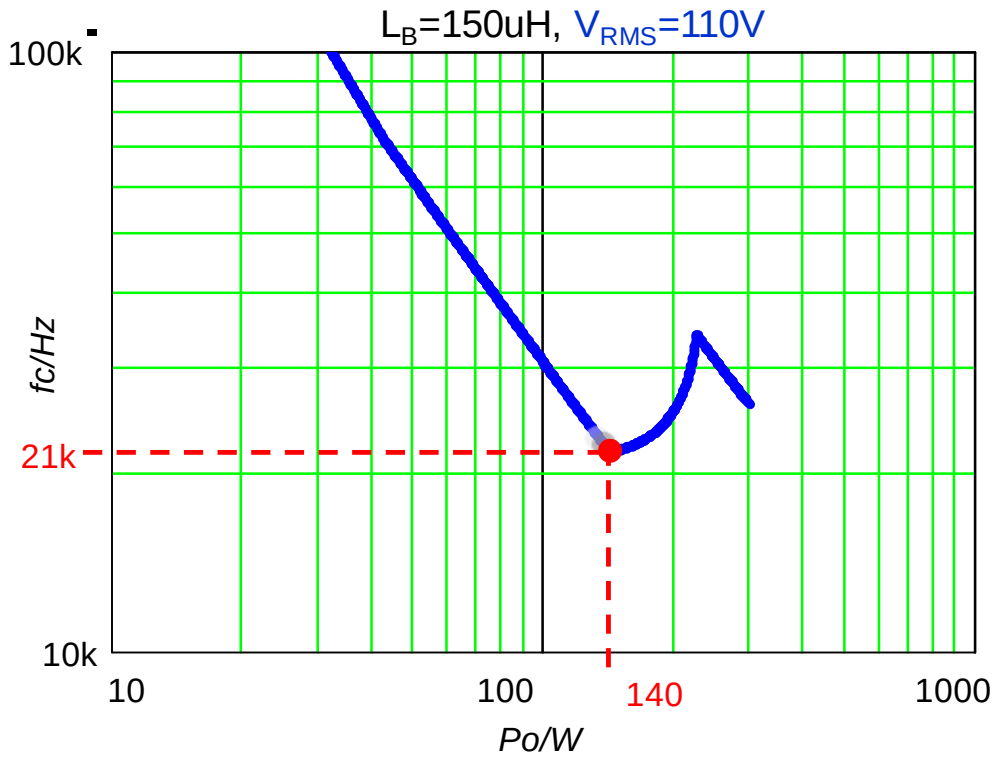

Figure 4.7: Corner Frequency vs. Output Power for V_{RMS}=110V

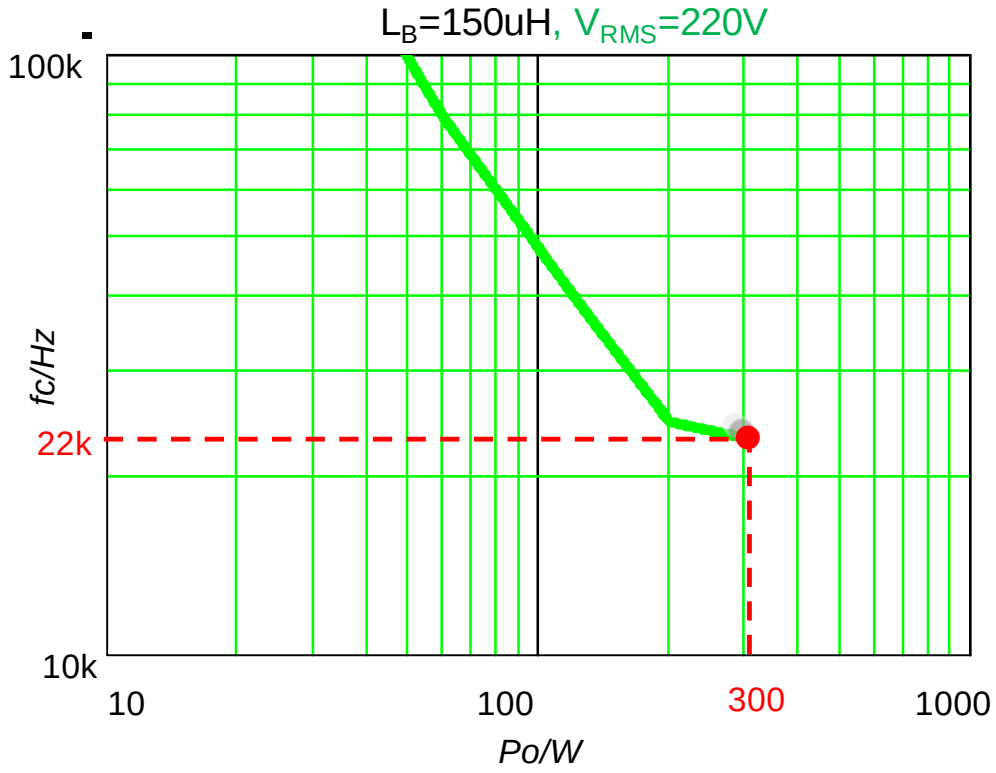

Figure 4.8: Corner Frequency vs. Output Power for V_{RMS}=220V

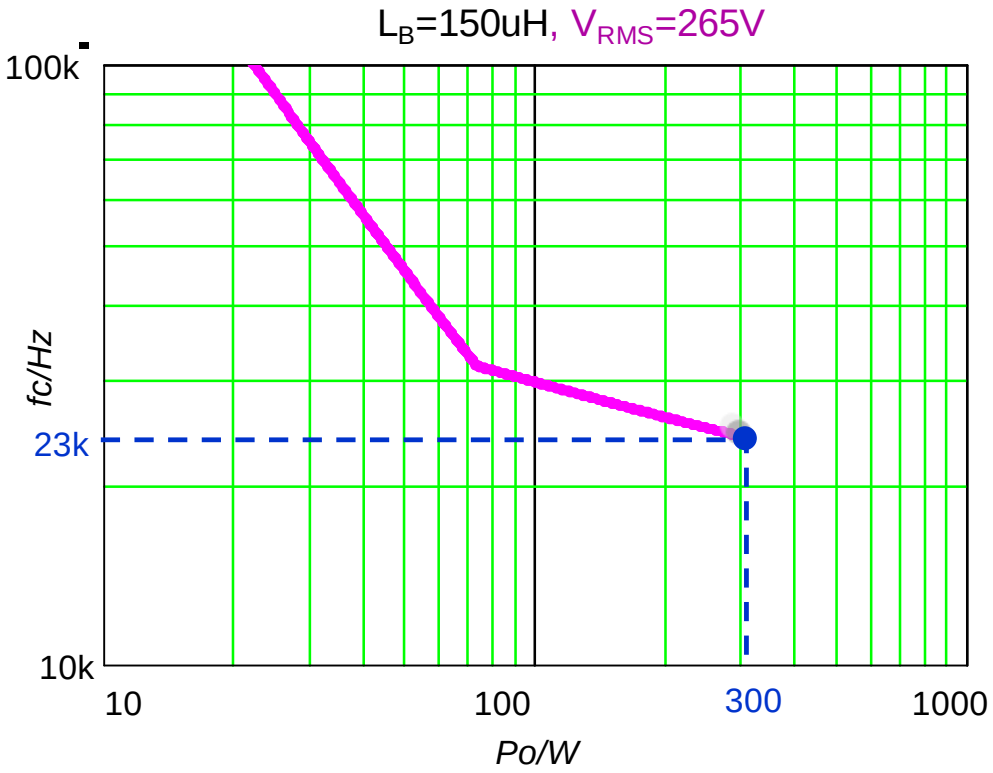

Figure 4.9: Corner Frequency vs. Output Power for V_{RMS}=265V

Put Figure 4.6-4.9 in one figure, we obtain Figure 4.10.

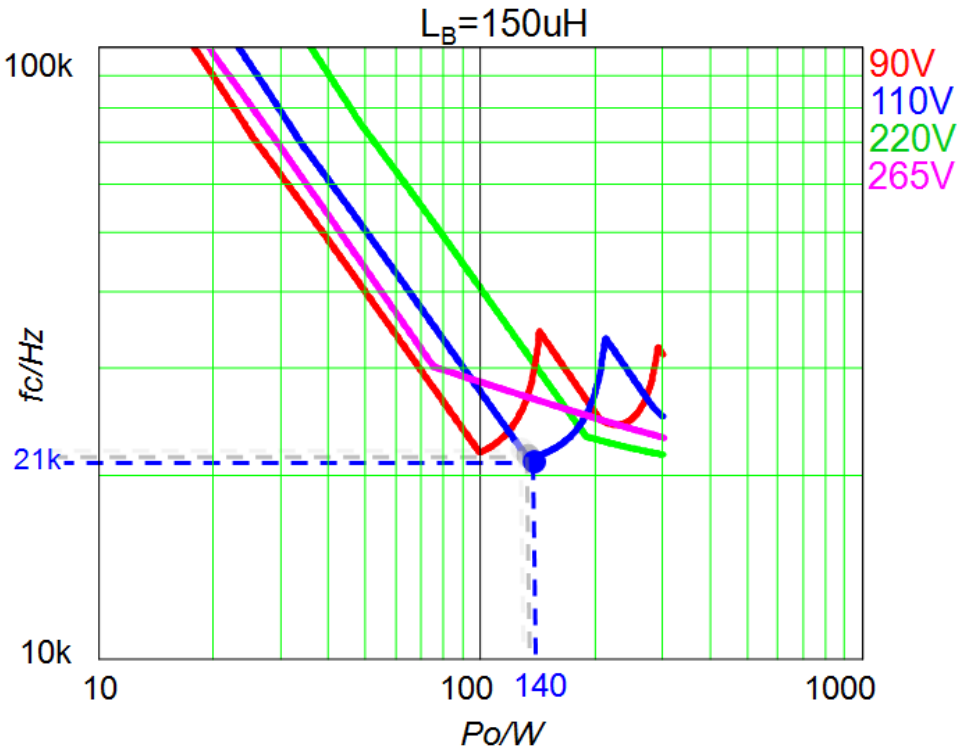

Figure 4.10: Corner Frequency vs. Output Power for All Input Line Conditions with L_B=150uH

Based on this figure, the worst case for all line and load conditions is easily

obtained, it is at low line (V_{RMS}=110V), partial load (Po=140W). Not as expected as in constant frequency CCM PFC, the lowest line (V_{RMS}=90V), full load (Po=300W) is not the worst case and it is even not a bad case. That is because this is variable frequency and you can hardly avoid noise at 150 kHz, which could be dominates by the first order harmonic component, the second order or even the third order.

4.2. DM EMI Filter Design Criteria for Single Boost PFC in CRM

In last section the DM EMI noise worst case is found for a given boost inductance. In practical design, boost inductance is selected based on the trade off the efficiency and the size of the boost inductor. So generally the boost inductance is the only design parameter for the CRM boost PFC.

One straightforward method to find the design criteria would be following the same process in section 4.1 and finding all the DM EMI noise worst case for different selection of the boost inductance.

For example, if L_B=200uH, the Corner Frequency vs. Output Power for All Input Line Conditions then is shown in Figure 4.11.

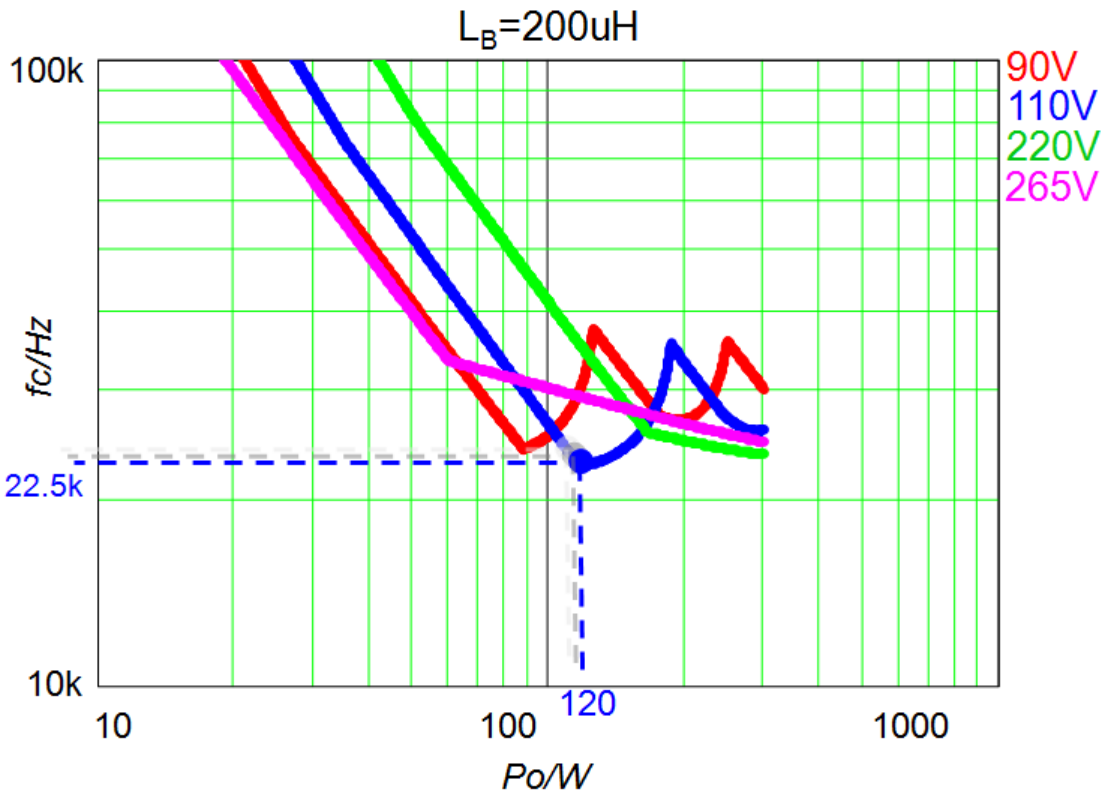

Figure 4.11: Corner Frequency vs. Output Power for All Input Line Conditions with L_B=200uH

So for different selection of boost inductance, we can go through this process again and again. Table 1 lists some of the results.

Table 1 Worst fc for different selection of boost inductance

Boost Inductance	Worst fc	V_{RMS}	Load
100uH	19.5 kHz	110V	240W
150uH	21 kHz	110V	140W
200uH	22.5 kHz	110V	120W
250uH	23.5 kHz	220V	300W
300uH	24 kHz	220V	300W

When LB is 300uH, the minimum switching frequency is 20 kHz, shown in Figure 4.12. When LB is larger than 300uH, the minimum switching frequency would be below 20 kHz, and then audible noise would be a concern. So 300uH is the largest selectable boost inductance.

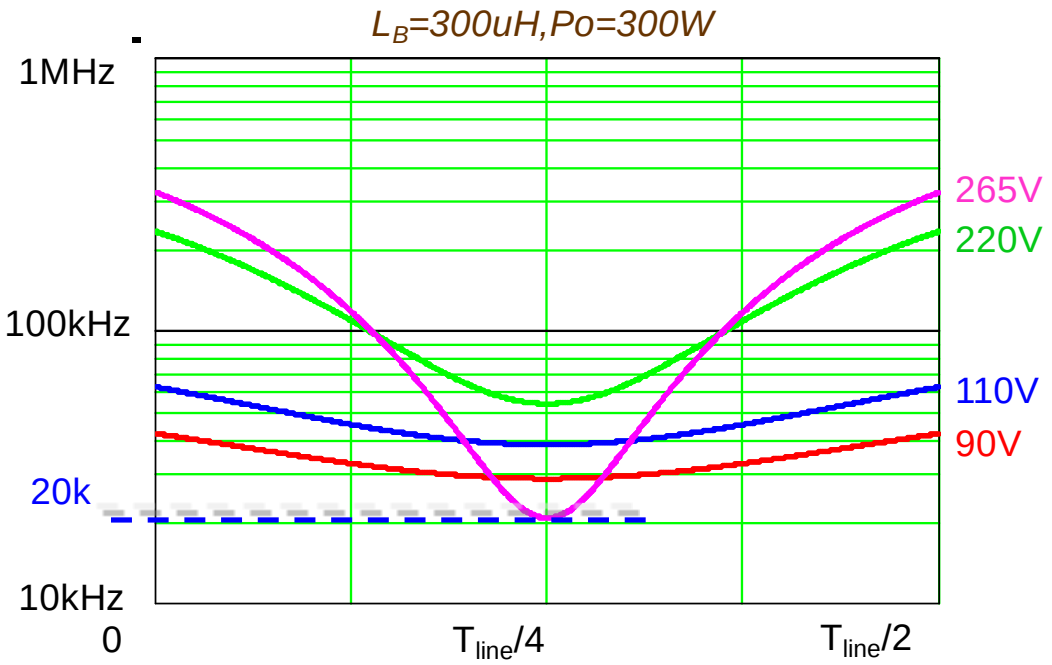

Figure 4.12 Switching Frequency over Half Line Cycle for Different Input Line Voltage

Based on Table 1, worst corner frequency vs. boost inductance could be obtained in Figure 4.13.

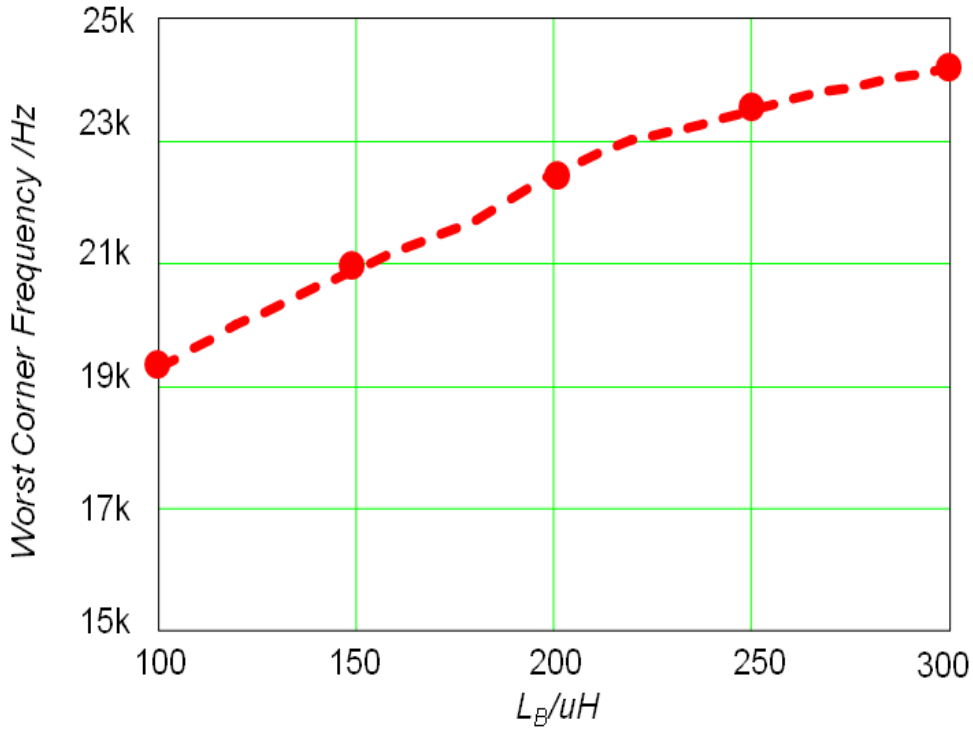

Figure 4.13: worst corner frequency vs. boost inductance

This curve could be used to design the DM EMI filter after selecting the boost inductance, which could help to avoid over-design of the EMI filter.

However, this is a little bit complex to get this curve to help design the EMI filter. Through the analysis, it is also found that the frequency range of the highest line (V_{RMS}=265V) is the largest, and generally includes 150 kHz at full load. That is to say, for the highest line, there is always a current ripple with frequency equal to 150 kHz, whose first order harmonic component will generate noise at 150 kHz. This is surely a bad case. Figure 4.7 and Figure 4.9 are redrawn together, shown in Figure 4.14.

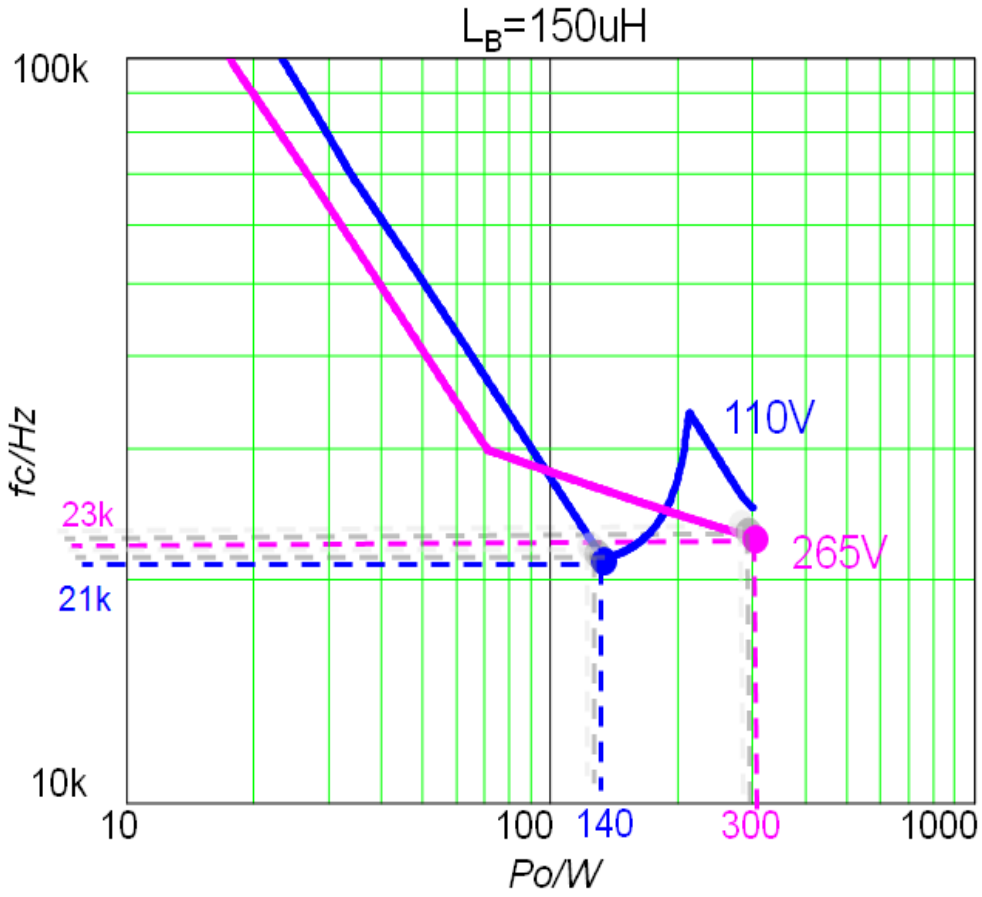

Figure 4.14: Corner Frequency Comparison between V_{RMS}=110V and V_{RMS}=265V

There is 2 kHz difference in corner frequency between worst case for V_{RMS}=265V and the global worst case and equivalently about 4dBuV different in noise at 150 kHz. So considering the highest line, full load as the worst EMI noise condition would be a simple way to design the EMI filter as long as some margins are considered.

4.3. DM EMI Noise Worst Case Analysis for Interleaved Boost PFC in CRM

Interleaving techniques are used in constant frequency CCM PFC to achieve ripple cancellation and improve EMI performance. Its influence on the CRM boost

PFC is also an interesting topic. The sketch diagram is shown in Figure 4.15.

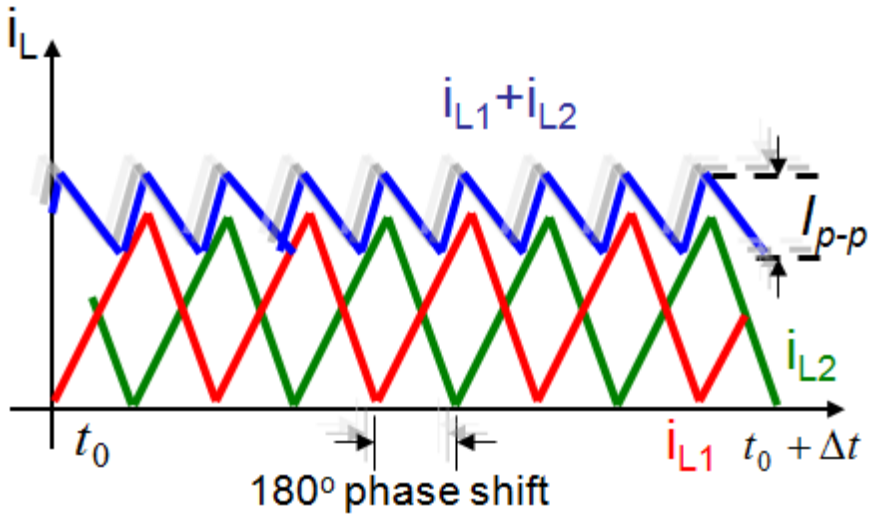

Figure 4.15: Total Inductor Ripple Current Sketch

Figure 4.16 and Figure 4.17 show the calculated ripple current reduction by using 2-channel interleaved CRM boost PFC.

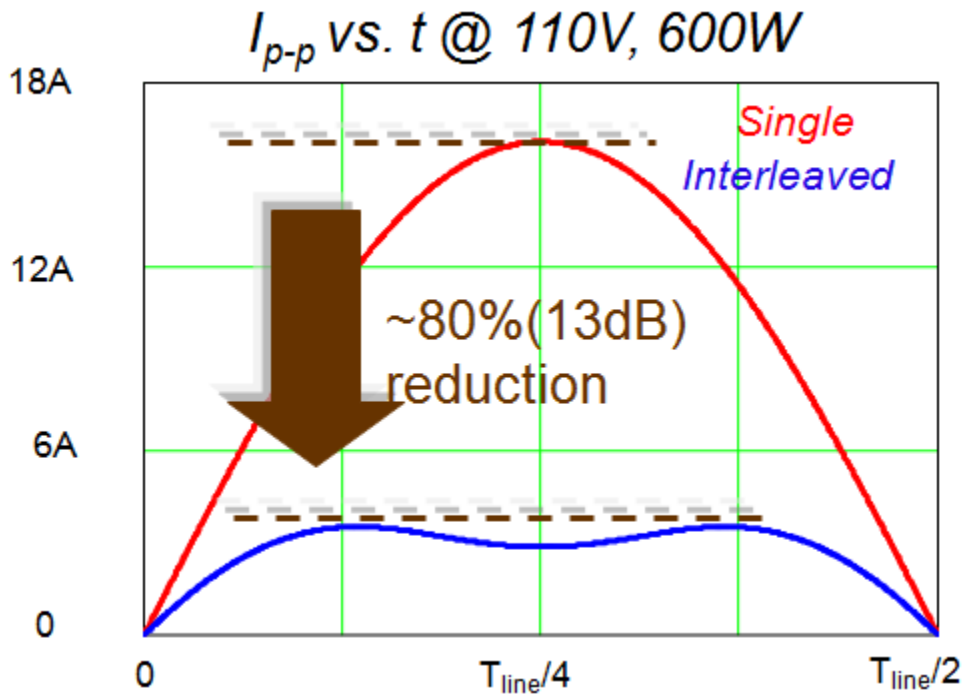

Figure 4.16: Ripple Current Reduction by Interleaving at Low Line

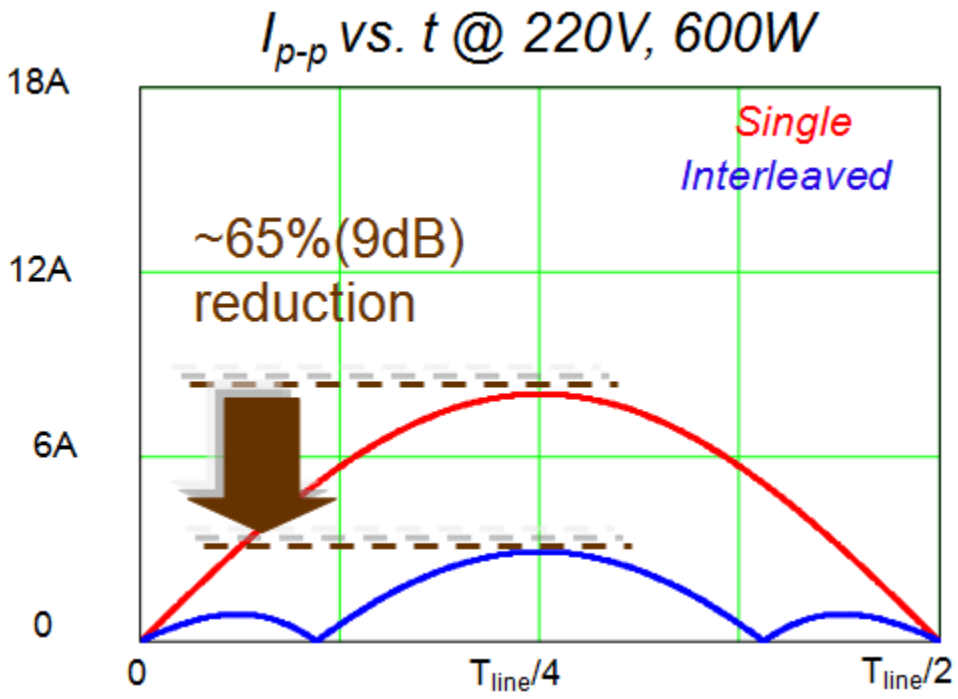

Figure 4.17: Ripple Current Reduction by Interleaving at High Line

We can see at least 9dB ripple current reduction can be achieved. Can the same EMI performance improvement be achieved?

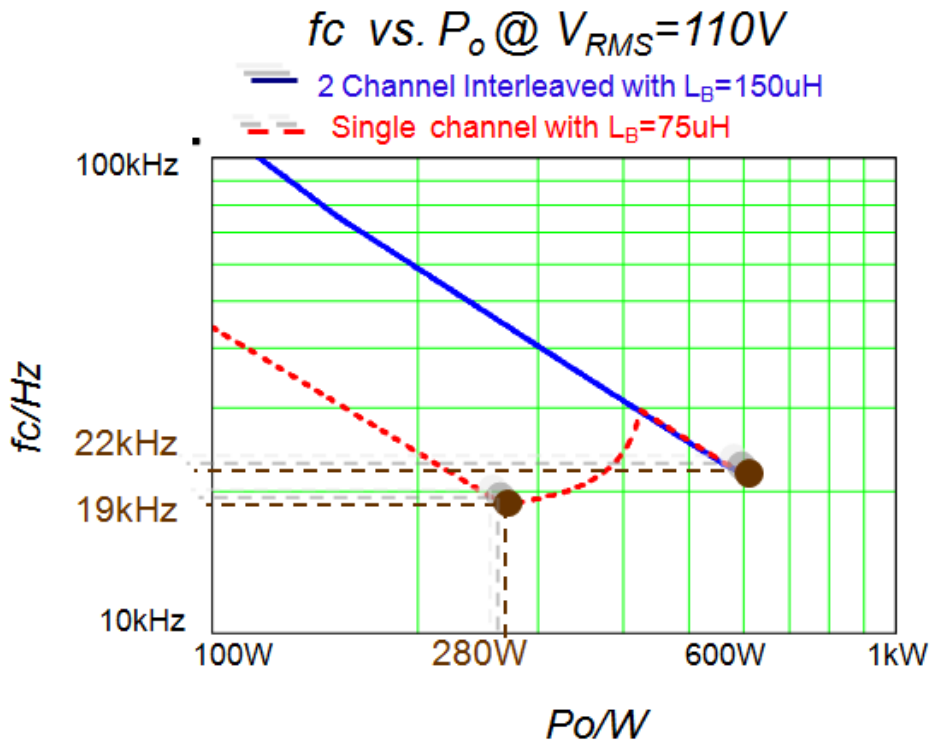

Figure 4.18: DM EMI Filter Corner Frequency Comparison

In Figure 4.18, the DM EMI noise worst cases in single channel CRM boost PFC and in 2-channel interleaved PFC are compared. We can see only 3 kHz improvement is achieved. If we compare the corresponding noises in Figure 4.19, we can see for 2-channel interleaved PFC with switching frequency from 71 kHz to 116 kHz, although the first order harmonic component is cancelled, the second order harmonic component of the 75 kHz ripple current appears at 150 kHz diminishes the improvement.

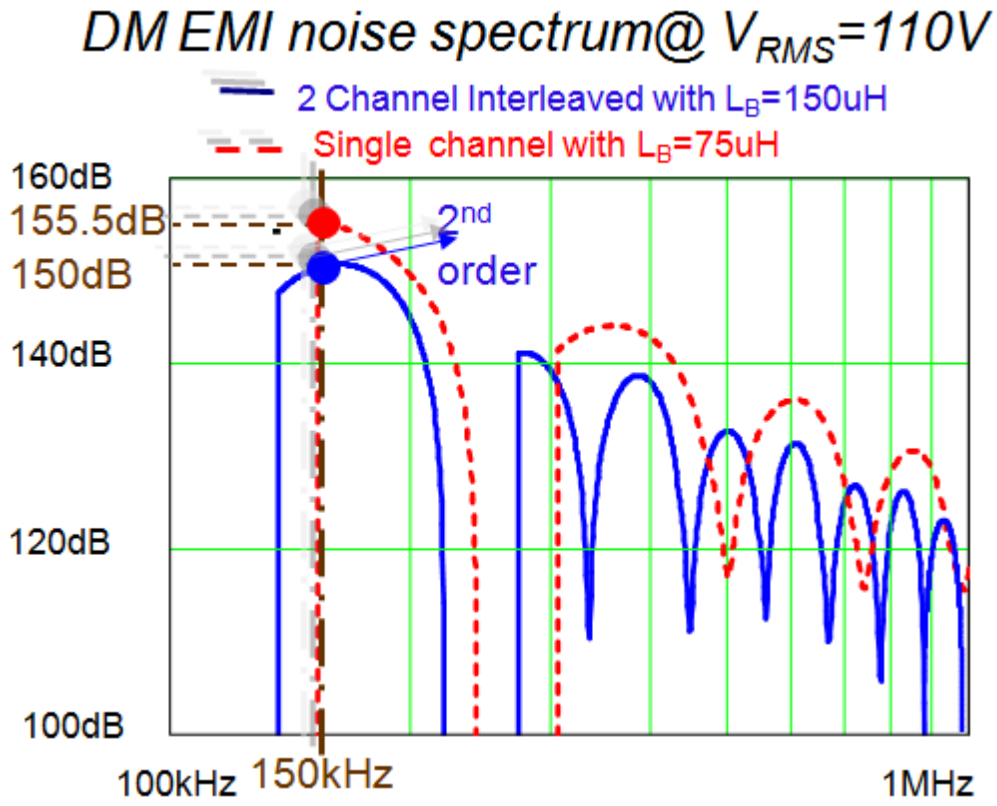

Figure 4.19: Worst Case of DM EMI Noise Comparison

One possible way to continue improving the EMI performance on the 2-channel interleaved boost PFC is to push the minimum switching frequency above 75 kHz. For 2 channel interleaved boost PFC, when L_B = 80 uH, the minimum switching frequency is 76 kHz, when V_{RMS}=265V. The corner frequency analysis with L_B = 80 uH is shown in Figure 4.20.

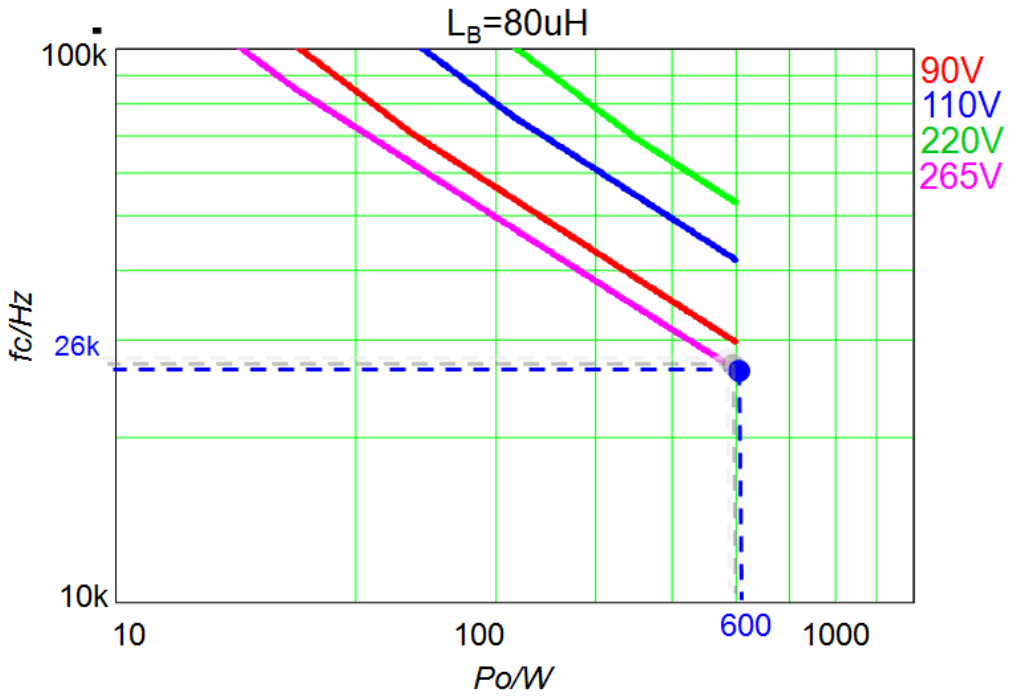

Figure 4.20: Corner Frequency vs. Output Power for All Input Line Conditions with L_B=80uH

We can see that the worst case happens at highest line V_{RMS}=265V, full load 600W, since for lower input line voltage, the minimum frequency is already far away above 75 kHz, which can be shown in Figure 4.21.

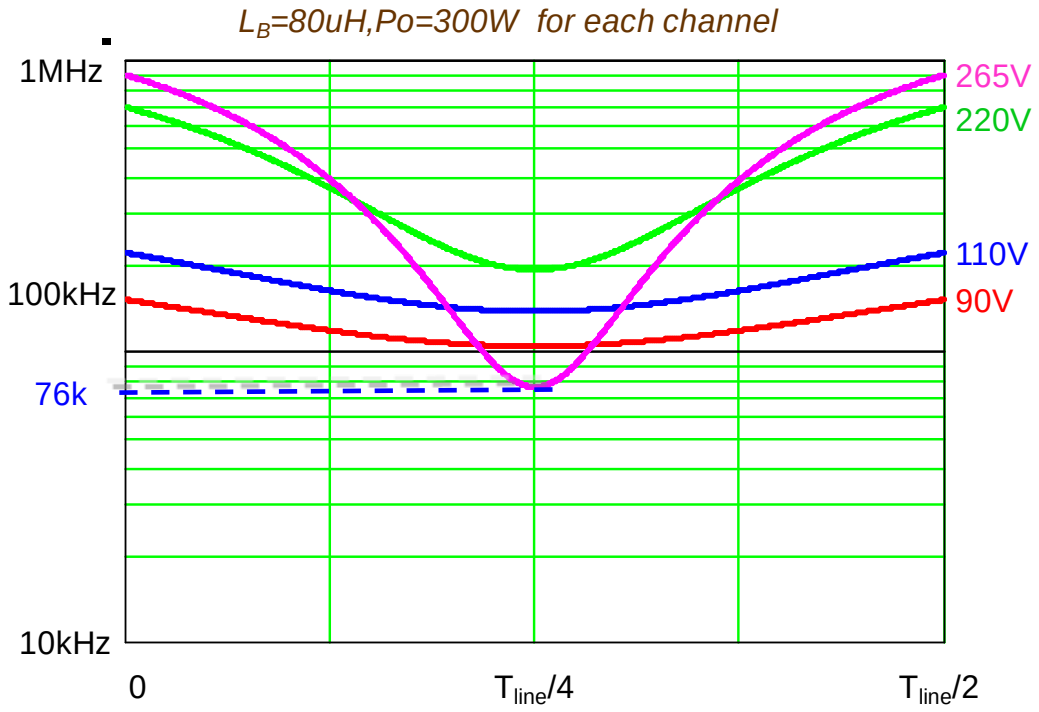

Figure 4.21: Switching Frequency Range of 2-Channel Interleaved CRM PFC for All Line Conditions

We can further reduce the boost inductance to benefit the EMI filter design, with

the penalty of higher switching loss. The DM EMI filter corner frequency for worst case DM EMI noise for different selection of boost inductance per channel is shown in Figure 4.22.

From Figure 4.22 we can see that, the DM corner frequency will increase when L_B decreases if the minimum switching frequency is above 75 kHz (or when L_B<80uH). When L_B is larger than 80uH, the minimum frequency is already below 75 kHz, then the EMI performance will be determined by the noise at 150 kHz caused by the second order harmonics of the 75 kHz current ripple.

The reason why from 80uH to around 110uH the DM corner frequency still decreases is that the magnitude of the noise at 150 kHz increases due to the duty cycle's impact where for the 75 kHz current ripple, different duty cycle may give different magnitude of second order harmonics.

From around 110uH to 1000uH, the increase of the DM corner frequency is caused by either the decreased magnitude of the noise at 150 kHz or dominant noise at a frequency higher than 150 kHz (which means there is a gap at 150 kHz between two consecutive orders of harmonics), since when L_B increases, the switching frequency decreases and thus the dominant noise is gradually transferred from 2^{nd} order harmonics of 75 kHz current ripple to 3nd order harmonics of 50 kHz current ripple and so on and so forth.

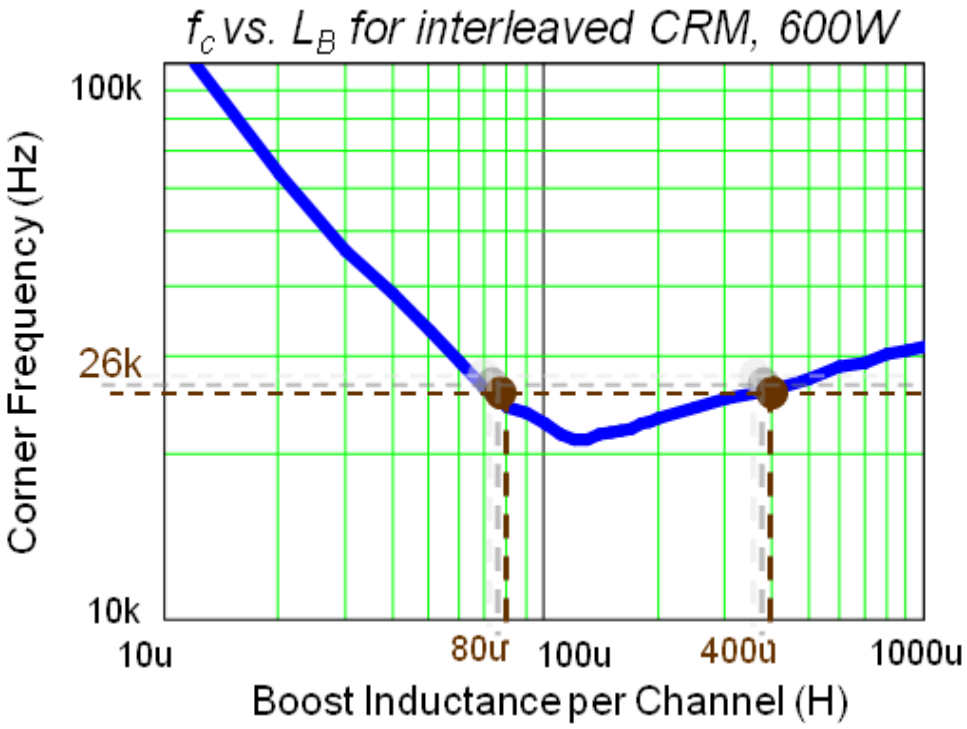

Figure 4.22: worst corner frequency vs. boost inductance per channel

Either L_B=80uH or L_B=400uH will lead to the same DM EMI filter design (fc=26 kHz in this example). The choice of L_B=80uH has smaller size of boost inductor but higher switching frequency, and the choice of L_B=400uH has larger size of boost inductor but lower switching frequency. Figure 4.22 can help to bring the DM EMI filter size into consideration when doing the efficiency and size trade off.

Chapter 5. SUMMARY AND FUTURE WORK

In this thesis, an approximate mathematical model is proposed to predict the quasi-peak DM EMI noise for the boost PFC with variable switching frequency. The measurement of the quasi-peak EMI noise is a very complex process and in order to be able to predict it, the measuring procedure is well investigated and the main functions of the spectrum analyzer are abstracted and simplified. For the noise source, the harmonic components of the inductor ripple current are analyzed based on the quasi steady state approximation, which makes the Fourier Transformation can be applied. This ignores the modulation effect on the inductor ripple current and definitely would cause some error. Error analysis would be one of the most important future works.

However, the comparison between the calculated noise and experimental results on the constant on-time PFC (variable switching frequency) shows the accuracy and the validity of this approximate model on evaluating the EMI performance. Then this method is used to analyze the single channel and interleaved CRM boost PFC, which also have constant on-time for given line and load condition, and some useful results are obtained.

One major limitation of this mathematical model is that it can only predict the EMI noise up to 1 MHz. Although this is good to design the inductance and capacitance for the EMI filters, the EMI performance from 1 MHz up to 30 MHz still need to be paid attention to. Thus the parasitic parameters need to be considered. So building simulation model based on the mathematical model to target the EMI noise at high frequency range would part of the future work, which will also help to deal with the CM EMI noise.

At last, the trend of the efficiency and total size of passive components for CRM boost PFC based on the analysis in this thesis should definitely be investigated in the future research, which is one of the original practical purposes of this research work.

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