Oscillator Phase Noise Reduction Using Nonlinear Design Techniques

by

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(ABSTRACT)

Phase noise from radio frequency (RF) oscillators is one of the major limiting factors affecting communication system performance. Phase noise directly effects short-term frequency stability, Bit-Error-Rate (BER), and phase-locked loop adjacent-channel interference.

RF oscillator circuits contain at least one active device, usually a transistor. The active device has noise properties which generally dominate the noise characteristic limits of an oscillator. Since all noise sources, except thermal noise, are generally proportional to average current flow through the active device, it is logical that reducing the current flow through the device will lead to lower noise levels. A theory based on the time-varying properties of oscillators proposes that narrowing the current pulse width in the active device will decrease the time that noise is present in the circuit and therefore, decrease phase noise even further.

The time-domain waveforms and phase noise of an active-biased 700MHz oscillator are analyzed, showing heavy saturation and high-harmonic content. Redesigns of the example oscillator in active-bias and four-resistor-bias configurations show improved phase noise and lower harmonic levels at the output. Five oscillator designs of each bias configuration, each having a different pulse width, are simulated. As predicted by the theory, the narrowest current pulse corresponds to the lowest phase noise of the simulated oscillators.

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Chapter 1

Introduction

An improved understanding of oscillator phase noise is needed for the improvement of oscillator performance. Such an understanding will help future electrical engineers cope with the expected dramatic rise in the amount of wireless communication traffic (Baberg, 2000; Kouznetsov & Meyer, 2000). As demands on the capacity of a system grow, more users will be required to fit in a given bandwidth. To accomplish this, the bandwidth of each user must be decreased. Oscillator phase noise, however, contributes to an increase of the bandwidth of each user, therefore limiting the number of users in a given frequency band (Robins, 1982).

Oscillators are a vital part of any radio-frequency (RF) hardware. They are necessary for frequency synthesis, operation of phase-locked loops, and mixing, and typically several oscillators exist in any given receiver or transmitter. Phase noise of each oscillator in a system is additive and has negative effects on frequency stability, bit-error rate (BER) and adjacent channel signals (Robins, 1982; Siweris, 1985).

The roots of phase noise lie in the noise sources of the transistor (or other active device) used in the oscillator. Shot noise, burst noise, partition noise, thermal noise and $1/f$ noise are the major transistor noise sources. All of these noise sources, except thermal noise, exist only when current is flowing in the device and can be controlled to some extent by controlling the current duty cycle. The basic process creating oscillations is by feedback using a resonant circuit with period current pulses charging the tuned circuit. Between charging pulses, the transistor conducts zero current and is considered 'off.' Phase noise is produced depending on the shape of the current pulse when the transistor is 'on.' If the current is a relatively narrow pulse, existing for very short time, there will be less phase noise produced than with a wider and longer pulse. From the engineer's perspective, the narrow pulse provides less contribution to creating time shifts in the energy storage when lined up with the output waveform peak. Making the designer's job easier is that only pulse width need be considered in design because the feedback process automatically synchronizes the current pulse with the output waveform peak. The pulse width can be designed into an oscillator using nonlinear design techniques, thus gaining control over transistor noise sources affecting phase noise.

Using nonlinear design methods based on the circuit principles in the text Communication Circuits: Analysis and Design by Kenneth K. Clarke and Donald T. Hess (1971), it is possible to control the current pulse width in the oscillator transistor. Pulse-width control is accomplished by varying the drive voltage of an active device. Other benefits of designs based on the principles of

Clarke and Hess include the ability to set harmonic levels, output power, and oscillation frequency with reasonable precision..

To examine the relationship between phase noise and current pulse width, Hewlett-Packard Advanced Design System (ADS) software was used to simulate several 700MHz Colpitts oscillators. An example active-biased oscillator producing 20mW at 700MHz was used as a comparison for the oscillators. The example oscillator is shown to have decent phase noise but exhibited extremely high harmonic content and transistor saturation, both usually considered to be undesirable traits of an oscillator (Rohde, 1983). Both active and four-resistor bias oscillators were designed, each producing 20mW without saturation and with less harmonic content. The four-resistor bias configuration was introduced so that phase-noise measurements of two different oscillator configurations could be compared. Phase-noise measurements were simulated in the range spanning 100Hz to 100kHz above the carrier frequency.

To observe the effect of current pulse width on phase noise, five oscillators of each configuration, all producing 5mW, were designed with differing pulse widths. The power level of 5mW was selected to focus the study on the pulse width of the collector current and not dealing with saturation and other undesired performance effects. The results showed a definite correlation between current pulse width and phase-noise level.

1.1 Literature Review

Until recently, oscillator phase noise reduction has been primarily based on ideas proposed by D. B. Leeson in 1966 (Driscoll, 1973; Prigent et al. 1999). Leeson's model of oscillator phase noise was based on viewing an oscillator as a time-invariant system. Properties of the oscillator such as signal power, resonator Q, and noise figure, which do not vary with time, are used to obtain optimal phase noise performance. In this light, well-known oscillator noise models presented by Randall Rhea (1990), W. P. Robins (1982), and Ulrich Rohde (1983) are all very similar. This is not to say that Leeson derived models are not useable; they just have seen their time in the spotlight. Circuit designers must take care when attempting phase noise optimization by these methods. For example, attempts at increasing Q have, also, unknowingly, increased noise figure, thus completely counteracting the beneficial effects of improved Q (Hajimiri & Lee, 1998).

Two papers: "A General Theory of Phase Noise in Oscillators" (Hajimiri & Lee, 1998), and "Oscillator Phase Noise: A Tutorial" (Lee & Hajimiri, 2000), offer a view of oscillator noise different than that of previous works. Hajimiri and Lee develop a phase noise model based on the time-varying properties of oscillators. Specifically, the transient characteristics of the device current flow. Hajimiri & Lee developed a noise model that accounts for noise sources from this current flow by studying the actual waveforms of the active device in an oscillator. Unlike Leeson's approach, Hajimiri & Lee made no assumptions concerning the effects of device $1/f$ noise and resonator bandwidth on the phase noise characteristics of an oscillator.

Evidence from references on oscillator phase noise demonstrate that noise sources located in the transistor or other active device were the culprits responsible for phase noise. Some excellent sources on general device noise sources are found in the original solid-state electronics texts by Manasse et al. (1967), Thornton et al. (1966) and Spangenburg (1957).

For a detailed look at transistor noise, references concerned solely with semiconductor noise were consulted The text Noise in Electronic Devices and Systems by M.L. Buckingham (1983), detailed noise sources associated with pn junctions and transistors. Another, more recent text

Electronic Noise and Fluctuations in Solids by Sh. Kogan (1996), complemented Buckingham's work. Kogan's semiconductor noise descriptions were intricately detailed, beginning at the atomic level and using a physical orientation. In addition to having an extensive explanation of burst noise, Kogan claims to have compiled the most comprehensive theory of $1/f$ noise. Sources reviewed to quantify Buckingham's and Kogan's work included "$1/f$ noise sources" by Hooge (1994) and other papers specializing in $1/f$ noise by Kirtania et al. (1996), Van Der Ziel et al. (1986), and Vempati et al. (1996).

Nonlinear design principles from Clarke and Hess (1971) were used in the design process. The work of Davis (1996), based on the previous work of Clarke and Hess, summarized oscillator circuits with appropriate nonlinear design techniques.

Chapter 2

Background

2.1 Oscillator Fundamentals

One of the most uncomplicated ways to view an oscillator is as an amplifier with a high-Q filter as a feedback network. This is commonly referred to as the feedback oscillator model and is shown in Fig 2.1.

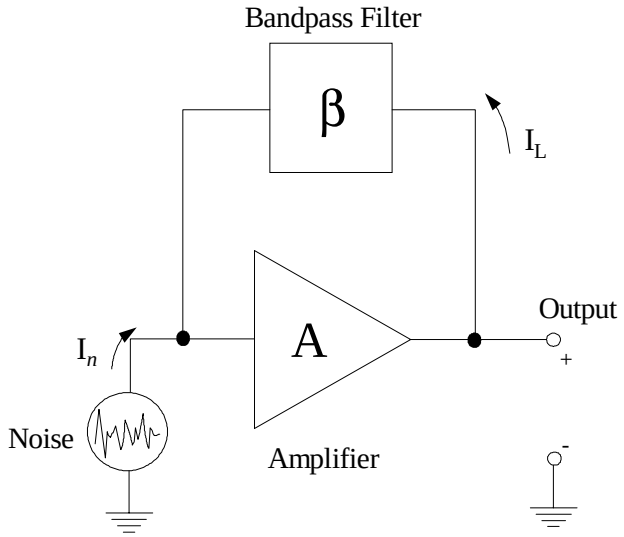

Figure 2.1. Feedback oscillator model (Rohde, 1983).

Broadband noise is present everywhere in the circuit. The amplifier boosts the signal level of the noise at all frequencies. This amplified noise then travels through the feedback loop back to the input of the amplifier. The feedback loop consists of a filter that allows the signal of the desired frequency to pass. This frequency passes through the amplifier and filter repeatedly. A sinusoidal signal, centered around the frequency of the filter, begins to emerge from the noise as the signal travels around the loop many times. The amplitude of this signal cannot grow infinitely since the bias circuit or the characteristics of the device used as the amplifier will limit the final amplitude.

Although the passband of the filter in the feedback loop is centered at the desired oscillation frequency, it does not have a bandwidth narrow enough to reject other frequencies. To select a single frequency component at the output of the oscillator, a Q-enhancement occurs as a result of the feedback process. The frequency is set by the resonance of the feedback circuit. A simple expression for loop current in Fig. 2.1, showing Q-enhancement, is

$$I_L = \frac{A}{1 - A\beta} I_n = \frac{\frac{A}{1-A}}{1 - j\left[\frac{QA}{1-A}\right]\left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega}\right)} I_n \tag{1}$$

where I_n represents broadband noise components, A is the amplifier transmittance at resonance, β is the filter characteristic, and Q is the quality factor of the filter. To observe this filter enhancement effect in the frequency domain, β is replaced with the frequency characteristic of a single-resonator, shunt bandpass filter. At the resonant frequency, ω_o, the imaginary term in the denominator equals zero leaving only $I_L = AI_n/(1 - A)$, with A approaching unity. When ω is not equal to ω_o the imaginary term in the denominator becomes significant, highly attenuating the loop current and providing a significant out-of-phase cancellation. The phase shift and amplitude reduction off resonance reject off frequency components and provide the enhancement needed for the desired signal output frequency.

2.2 Design

The active device in an oscillator operates in a nonlinear mode. This nonlinear operation means, for example, that if the input level is doubled the output will not necessarily be doubled and may in fact only increase a small percentage. The nonlinear characteristics of a bipolar-junction transistor (BJT) and how they pertain to oscillators will be examined here. The techniques used are easily applicable to characteristics of tubes and semiconductor devices other than BJTs. Oscillator design used in this work was performed using a three-terminal model for the device and related components, coupled with basic nonlinear techniques from Clarke and Hess (1971). As previously mentioned, this design method allows the engineer to set oscillation frequency, output power, and harmonic levels.

2.2.1 Nonlinear Sources

The characteristic relating current and voltage of active devices used in oscillator circuits is nonlinear. It is the nonlinearity which controls oscillation amplitude as well as produces harmonic content in the output signal, while the resonant circuit and resultant phase shift sets the oscillator frequency at resonance. Fig. 2.2 shows the nonlinear, exponential relationship between voltage and current at the base-emitter junction of a BJT. The waveform with amplitude V_1 is considered the input, or drive voltage across the junction. When a sinusoidal voltage of a great enough amplitude is applied across the base-emitter junction the resulting current is a periodic series of pulses whose amplitude depends on the nonlinear characteristic of the device. In a BJT, current flows when the drive voltage is above approximately 0.7V.

The existence of short current $pulses$ leads to a relatively strong harmonic content. If the current output were a perfect sinusoid then its Fourier transform would yield a single impulse in

the frequency domain, therefore having no harmonic content. Taking the Fourier transform of a pulse or series of pulses in the time domain yields a number of frequency components. These frequency components are called harmonics and are an inevitable trait of circuits using nonlinear devices. The peak current approaches $2I_{DC}$ for extremely short pulses. It follows that if the drive level V_1 is increased, the harmonics will also increase as the current pulse width becomes shorter and the peak current amplitude becomes greater. This harmonic trade-off is an important consideration in reducing noise content by using shorter pulses.

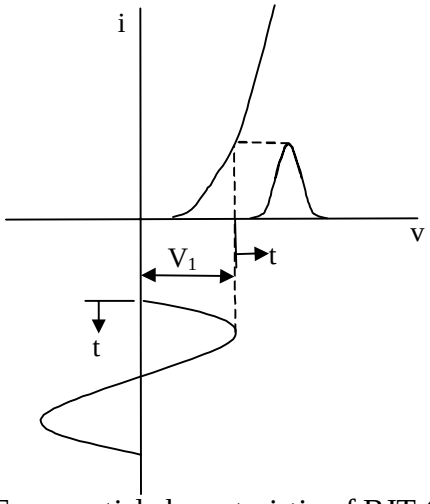

Figure 2.2. Exponential characteristic of BJT (Davis, 1996).

To derive the harmonic content mathematically, it is necessary to start with the nonlinear equation of the device. The current in a forward biased pn junction of a diode or transistor is typically approximated by (Clarke & Hess, 1971)

$$i = I_s e^{qv/kT}, \tag{2}$$

where I_s is the device saturation current, v is the voltage applied across the junction, k is Boltzman's constant, q is the charge of an electron, and T is the temperature of the device junction. The voltage v consists of a DC component as well as a sinusoidal, $v = V_{dc} + V_1\cos(\omega t)$, Eq. (2) becomes

$$i = I_s e^{\frac{qV_{dc}}{kT}} e^{\frac{qV_1}{kT}\cos(\omega t)}. \tag{3}$$

For $T = 300°K$, kT/q is approximately 26mV. The drive level, x, is defined as the normalized drive level of V_1 compared to 26mV or $(V_1/26\text{mV})$. For example, if V_1 were 260mV, x would be equal to 10. Since, $e^{x\cos(\omega t)}$ is a periodic function it can be expanded into a Fourier series. Once in a Fourier series the output current i will be a series of terms for each harmonic frequency. For inclusion into Eq. (3), the sinusoidally driven exponential may be expanded in a Fourier series of the form

$$e^{x\cos(\omega t)} = \sum_n a_n(x)\cos(n\omega t). \tag{4}$$

The Fourier integral for the DC coefficient, a_o, is

$$a_o = \frac{1}{2\pi}\int_0^{2\pi} e^{x\cos(\omega t)}\, d(\omega t) = I_o(x), \tag{5}$$

which is the zero-order modified Bessel function, $I_o(x)$. Coefficients for the remainder of the series are found from

$$a_n(x)\Big|_{n>0} = \frac{1}{\pi}\int_0^{2\pi} e^{x\cos(\omega t)} \cos n(\omega t)\, d(\omega t) = 2I_n(x), \tag{6}$$

where $a_n(x)\Big|_{n>0}$ is precisely twice an n^{th}order modified Bessel function, $2I_n(x)$. Having the coefficients in the form of modified Bessel functions greatly simplifies the analysis. If the results from Eq. (4), (5), and (6) are substituted into Eq. (3), i becomes

$$i = I_s e^{\frac{qV_{dc}}{kT}}\left[I_0(x) + \sum_n 2I_n(x)\cos n\omega t\right]. \tag{7}$$

Finally, Eq. (7) can be rearranged so that the harmonics are relative to the DC current.

$$i = \underbrace{I_s e^{\frac{qV_{dc}}{kT}} I_0(x)}_{I_{DC}}\left[1 + \sum_n \frac{2I_n(x)}{I_0(x)}\cos n\omega t\right] \tag{8}$$

Fig. 2.3 shows Eq. (8) in graphical form. The significance of Fig 2.3 is that the designer is able to predict the harmonic content for a given DC current and drive level. For example, for a BJT oscillator biased at 1mA with $V_1 = 260\text{mV}\,(x = 10)$, the peak amplitude of the first harmonic will be 1.89mA, a second harmonic of 1.6mA, and so forth. It should be noted that there is a fundamental limit of twice the DC current which all harmonics approach asymptotically. As a general design rule, for any substantial drive level $(x \geq 10)$, the fundamental current peak will be roughly twice the DC current flowing in the device.

2.2.2 Three-Terminal Model

Three-terminal models provide a simple way of representing the active device and resonator components of an oscillator. The resultant oscillator equations based on simple approximations for such a three-terminal model are generally found to be excellent approximations in well designed oscillators. To derive the three-terminal model of an oscillator circuit, the AC equivalent circuit of the oscillator must be determined. Next, each resonator reactance in parallel with any bias resistance is placed across the appropriate terminals of the device. Fig 2.4 and Table 1 show the three-terminal model for a Colpitts oscillator and the appropriate resistor relationships. When reduced to a three-terminal model, the common-base, common-emitter, and common-collector configurations of the same oscillator all have the same topology.

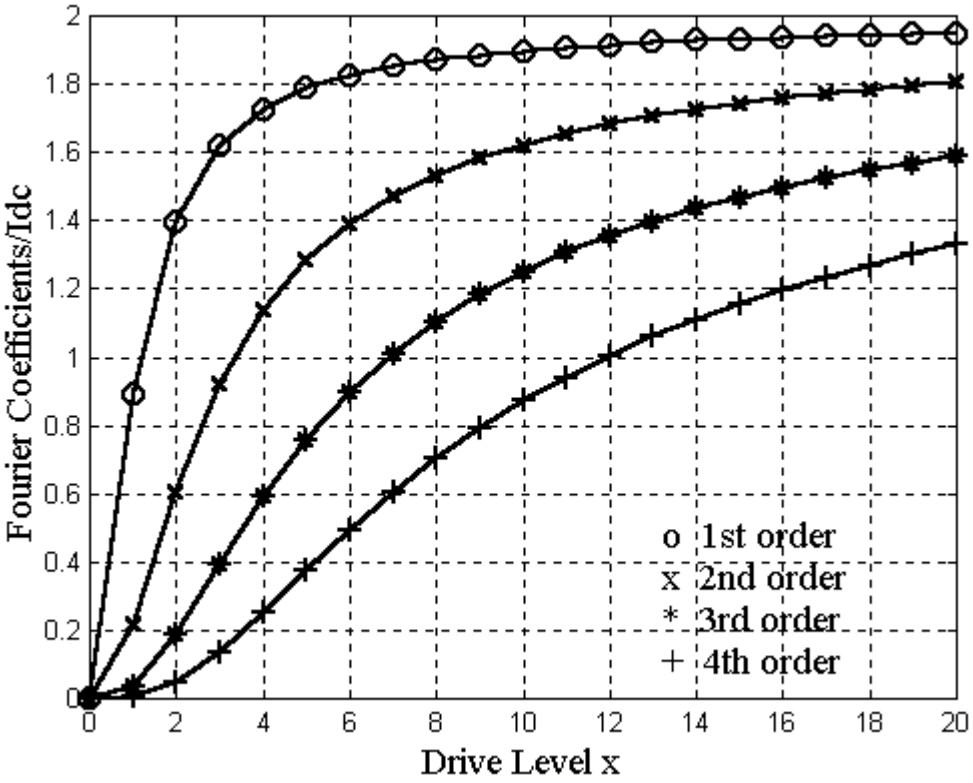

Figure 2.3. Fourier coefficients for BJT characteristic.

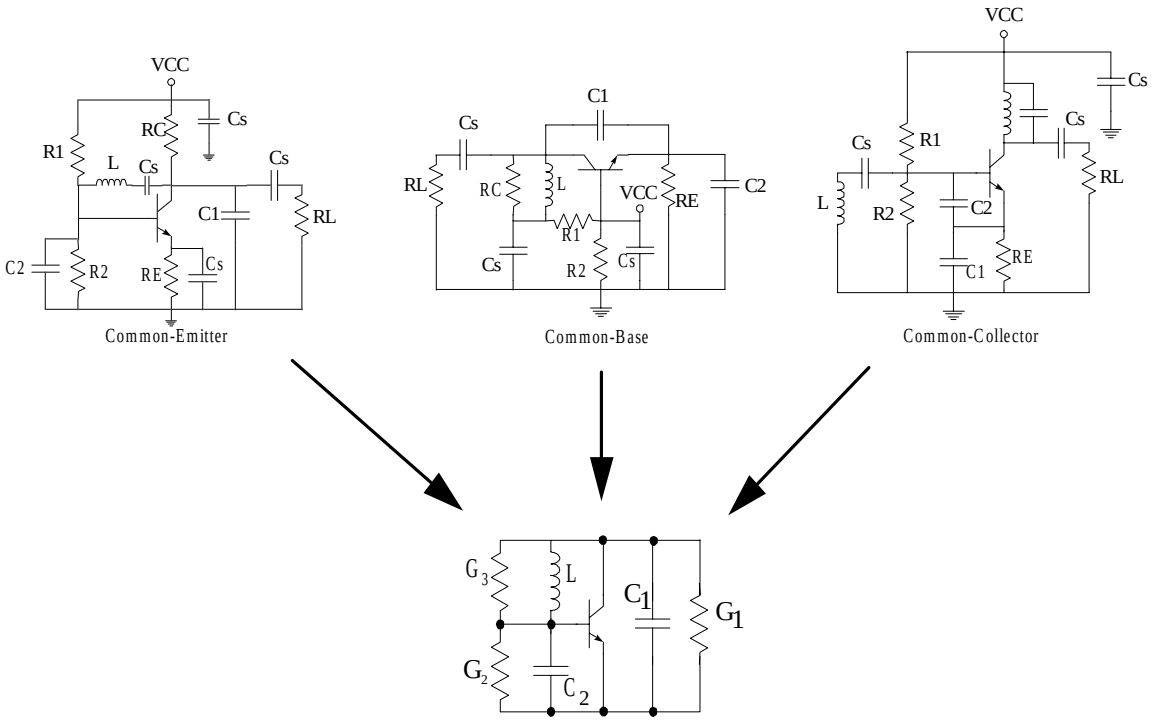

Figure 2.4. Common-base, common-collector, and common-emitter Colpitts configurations reduce to same three-terminal model.

In the common-collector configuration, the output is often taken from the collector terminal, simply acting as a buffer for the oscillator connection at the base-emitter terminals. This is the only Colpitts arrangement in which the load is not part of the three-terminal model or the oscillator equation; though care must be taken to ensure that the collector output voltage does not significantly feedback through the base-collector junction capacitance. As an alternative, the output of the common collector could also be taken across R_E.

Table 1. Conductances for Colpitts three-terminal model.

Oscillator Configuration	G1	G2	G3
Common-Emitter	$\frac{1}{R_L \| R_C}$	$\frac{1}{R_1 \| R_2}$	0
Common-Base	0	$\frac{1}{R_E}$	$\frac{1}{R_L \| R_C}$
Common-Collector	$\frac{1}{R_E}$	0	$\frac{1}{R_1 \| R_2}$

2.2.3 Oscillator Design

Basic oscillator design specifications often require a given output power into a specified load at the design frequency. The drive level and bias current set the fundamental output current and the oscillation frequency is set by the resonator components. An oscillator equation is derived taking into account the effects of the bias circuit and the resonator reactances on the output level of the oscillator. Design steps for an oscillator are explained below, along with a specific BJT Colpitts example:

Step 1: Choose an oscillator topology (i.e., Colpitts, Hartley, Pierce, etc.) and derive the appropriate three-terminal model and oscillator equations.

Step 2: Select a transistor best suited for the desired frequency of operation. Transistor selection should consider noise, frequency, and power requirements. Based on the particular device, the design may account for parasitics of the device affecting resonator components as well as nonlinear performance specifications.

Step 3: Select a normalized drive level x for desired harmonic content. The drive level should consider the trade-off between harmonic content, oscillator stability, and noise. Oscillator stability refers to the oscillator circuit's ability to sustain proper operation. A small drive level ($x = 2$) is desirable for low harmonic content, however such a choice may make the oscillation unreliable, particularly as a function of temperature and other circuit parameters.

Step 4: Determine the resonator and bias-circuit components to satisfy the oscillator equations of step 1.

Example Step 1:

A common-collector BJT Colpitts oscillator has been chosen to demonstrate the design process. An output of 5mW into 500Ω at a frequency of 10MHz using a 12V supply was specified. Fig. 2.5 shows the general schematic for this oscillator.

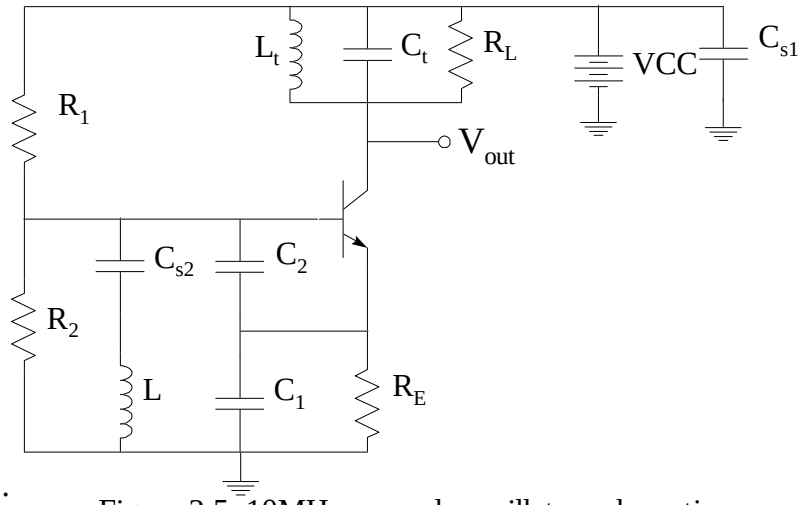

Figure 2.5. 10MHz example oscillator schematic.

Resistors R_1, R_2, and R_E provide the bias and R_L represents the load. Capacitor C_{s1} provides a bypass of the power supply at the oscillation frequency. Capacitor C_{s2} isolates the inductor L so the base bias will not be shorted to ground through L. The resonator that provides the feedback and sets the resonant frequency consists of C_1, C_2, and L. Components L_t and C_t provide the resonant tuning for the desired output frequency and harmonic content reduction, having little effect on the basic oscillator operation in the base-emitter circuit. In fact, the output tuning may even be used to select a harmonic of the fundamental frequency of oscillation for output applications.

The transistor is modeled by the α-model equivalent circuit from Fig. 2.6 for ease of analysis. An AC model of the general Colpitts configuration including the α-model, shown in Fig 2.7, is laid out in a manner to simplify the development of the oscillator equations.

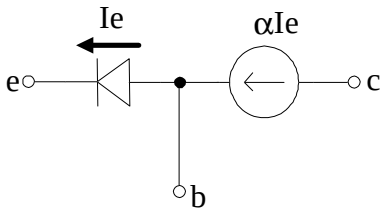

Figure 2.6. α model of BJT (Davis, 1996).

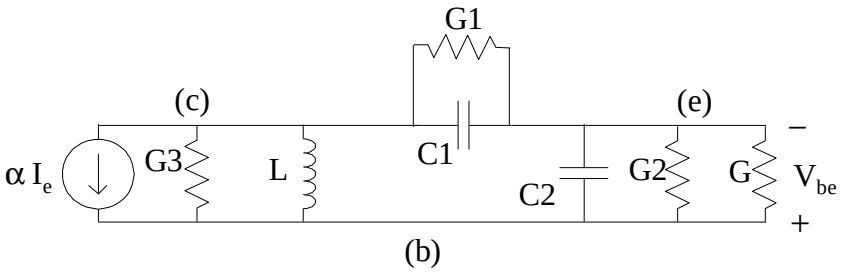

Figure 2.7. BJT Colpitts model (Davis, 1996).

In Fig 2.7, the active device is represented by the current source and the input conductance at the emitter, G. Conductances G_1, G_2, and G_3 represent the bias and/or load conductances connected in parallel with the resonator components C_1, C_2, and L, respectively. Conductance G is the large-signal AC or fundamental frequency conductance of the transistor, given by the fundamental-frequency current amplitude divided by the fundamental-frequency drive voltage magnitude or I_{1peak}/V_{1peak}. Using high-Q reactive voltage division and related impedance transformations, the current source will see a total conductance G_{total}. The current source is connected from collector to base, suggesting each voltage division be computed with respect to the voltage from the collector to base. Conductances G and G_2 are transformed to the current source through the voltage divider V_{eb}/V_{cb}, while the conductance G_1 is transformed by the voltage divider V_{ce}/V_{cb}. The conductance G_3 is already in parallel with the current source so it remains unchanged. The voltage ratios may be written as

$$\frac{V_{eb}}{V_{cb}} = \frac{C_1}{C_1 + C_2} = \frac{1}{n} \quad \text{and} \quad \frac{V_{ce}}{V_{cb}} = \frac{C_2}{C_1 + C_2} = \frac{n-1}{n}, \tag{9}$$

where the factor n represents the ratio of the collector-base voltage to the emitter-base voltage at the design frequency. The transformed conductances are proportional to $(1/n^2)$ and $[(1-n)/n]^2$, giving a total conductance seen by the current source at resonance as

$$G_{total} = G_3 + \frac{G + G_2}{n^2} + \left[\frac{n-1}{n}\right]^2 G_1. \tag{10}$$

In order to sustain oscillation the loop gain must be unity, implying both unity amplitude and zero phase shift. In this case, the equation for the closed loop gain at resonance is

$$V_{be} = \alpha G \frac{1}{nG_{total}} V_{be.} \tag{11}$$

Combining Eq. (10) with Eq. (11) gives

$$\alpha G = nG_{total} = n\left[G_3 + \frac{G + G_2}{n^2} + \left(\frac{n-1}{n}\right)^2 G_1\right]. \tag{12}$$

Collecting the nonlinear conductance terms together gives the final amplitude oscillator equation as

$$\frac{\alpha n - 1}{n^2} G = G_3 + \frac{G_2}{n^2} + \left(\frac{n-1}{n}\right)^2 G_{1.} \tag{13}$$

The series combination of the reactive elements L, C_1, and C_2 set the resonant frequency of the oscillator and insure that the loop phase shift is an integer multiple of 2π. The resonant frequency at which there is no phase shift in the oscillator is given by

$$L\frac{C_1 C_2}{C_1 + C_2} = \frac{1}{\omega^2}. \tag{14}$$

From Eq. (8) the relation between the capacitors C_1 and C_2 is

$$C_1 = \frac{C_2}{n-1}. \tag{15}$$

Equations (13), (14), and (15) are the necessary equations needed to design a BJT Colpitts oscillator (Davis, 1996). The resonant frequency, ω_o, and voltage ratio, n, are related to C_1, C_2, and L. The output level I_1 is generally selected to meet the output power requirements, thus setting the drive level V_1 and voltage ratio n in combination with the conductances G_1, G_2, and $G_{3.}$

The three-terminal model for the example oscillator of Fig. 2.5 is shown in Fig 2.8. The conductance G_1 models the resistor R_E connected across C_1. Resistor R_1 in parallel with R_2 provide the classic base bias resistance and the resultant model conductance G_3. There is no physical resistor across $C_{2,}$ therefore G_2 is set to zero.

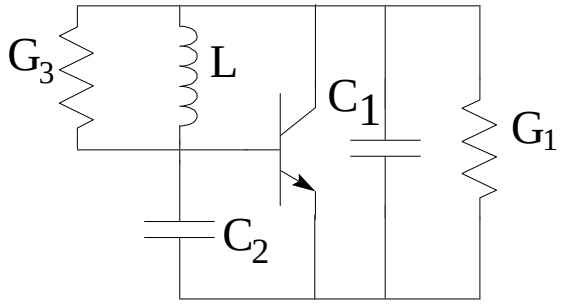

Figure 2.8. Three-terminal model of 10MHz oscillator example.

Example Step 2:

A 2N2369 transistor was chosen to meet the needs of frequency performance as well as ease of design at 10MHz. The typical value for α is approximately equal to 0.98 for the 2N2369. Other values may be used for α, but the actual value generally has little effect on the analysis.

Example Step 3:

The normalized drive level was chosen as $x = 10$ to allow adequate drive level to sustain oscillation and yet not produce excessive harmonic content. For an x of 10 the relative harmonic values of peak current from Fig. 2.3 are

$$I_1 = 1.897\, I_{DC}$$
$$I_2 = 1.621\, I_{DC}$$
$$I_3 = 1.249\, I_{DC}$$
$$I_4 = 0.871\, I_{DC}.$$

The fundamental current I_1 is specified by the output power needed for the designated load. For an output power, P_{out}, of 5mW to be delivered to a 500Ω termination, the required AC voltage peak is 2.24V. The corresponding fundamental current I_1 is related to the voltage through Ohm's law as

$$I_1 = V/R_L = 2.24/500 = 4.5\text{mA}.$$

Therefore, for $I_1 = 4.5$mA, I_{DC} must be set to 2.4mA for the desired drive level.

Example Step 4:

To avoid saturation in the transistor, it is important to select an emitter resistor to maintain a sufficiently small emitter signal voltage. For the design example this may be on the same order as the collector resistor for a common collector configuration. For the four-resistor bias configuration, the DC emitter voltage should also be set to provide a reasonable offset to variations in the base-emitter bias voltage. The bias resistor R_{E} was chosen to be 250Ω, for a $G_3 = 4$mS, though somewhat marginal in the need to avoid bias voltage variations. The parallel combination of bias resistors R_1 and R_2 was chosen to be twice R_{E}, or 500Ω, making $G_1 = 2$mS. This small choice gives a stiff bias circuit to minimize effects of variations in the transistor current gain, β. If a more stable bias is needed, then Clarke and Hess (1971) recommend using an R_{B} approximately equal to $\mathrm{R_E}$.

The values of R_1 and R_2 needed to supply the 2.4mA bias current are found. Using the common equation for four resistor bias (Hambley, 1994),

$$V_B = I_E(R_E + \frac{R_B}{\beta + 1}) + V_{BE}, \tag{16}$$

the base bias voltage V_B is found to be 1.26V. With a 12V supply and the criteria that $R_B = 500\Omega$, R_1 and R_2 are found to be 5.31 $k\Omega$ and 558Ω, respectively.

The drive voltage for $x = 10$ is 260mV. Therefore,

$$G = \frac{I_1}{V_1} = \frac{4.5\text{mA}}{260\text{mV}} = 17.3\text{mS}.$$

Eq. (13) can be rearranged into the quadratic equation

$$0 = n^2(G_3 + G_1) + n(-\alpha G - 2G_1) + G + G_1.$$

Solving for n gives the values $n = 2.96$ and $n = 1.20$. As a rule of thumb, the larger value of n is used for the solution. For the smaller value of n (typically about unity), C_2 becomes negligible in the circuit and invalidates the analysis as well as lowering the circuit Q. In this design, $n = 2.96$ was selected.

To solve for the resonator components, L, C_1, and C_2, one of the values must be selected to meet the quality factor requirements. Capacitor C_2 was chosen to be 5nF to provide a small reactance compared to the associated R of 250Ω, though a bit extreme in practical terms. The corresponding capacitor C_1 was found to be 2.55nF from Eq. (15). The effect of capacitor C_{s2} on the series reactance of L must be taken into consideration when computing L from Eq. (14). Capacitor C_{s2} was chosen to be 1nF, making L = 403nH.

The parallel tank circuit tuning the output resistance was derived from the equation for a parallel resonant circuit

$$Q = \frac{R}{\omega L} = \omega RC \text{ (Davis, 1996).}$$

A Q of 10 at 10MHz was chosen making L_t =796nH and C_t =318pF. Finally, C_{s1} was chosen to be 47nF to provide a reasonable AC short at 10MHz.

Example Results:

The final schematic shown in Fig 2.9 was simulated using ADS. The output voltage, collector current, and drive voltage are shown in Fig. 2.10. For a first pass design, the results were found to be close to specifications. With a bit of adjustment, the circuit may perform exactly as specified. A comparison of the design goals to the achieved results is shown in Table 2.

Table 2. 10MHz example oscillator simulation results.

Parameter	Design Goal	Measured
Vout	2.24 V	2.41 V
Pout	5 mW	5.8 mW
Drive, x	10	10.87
Frequency	10 MHz	10 MHz

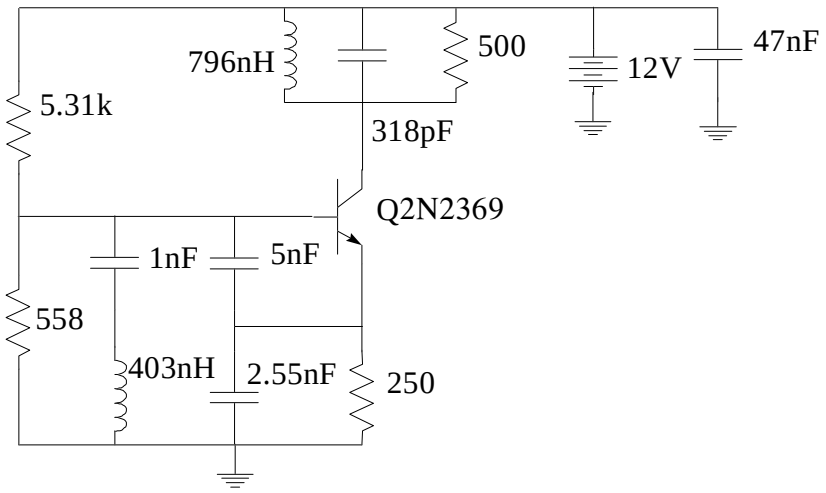

Figure 2.9. Final schematic of 10MHz oscillator example.

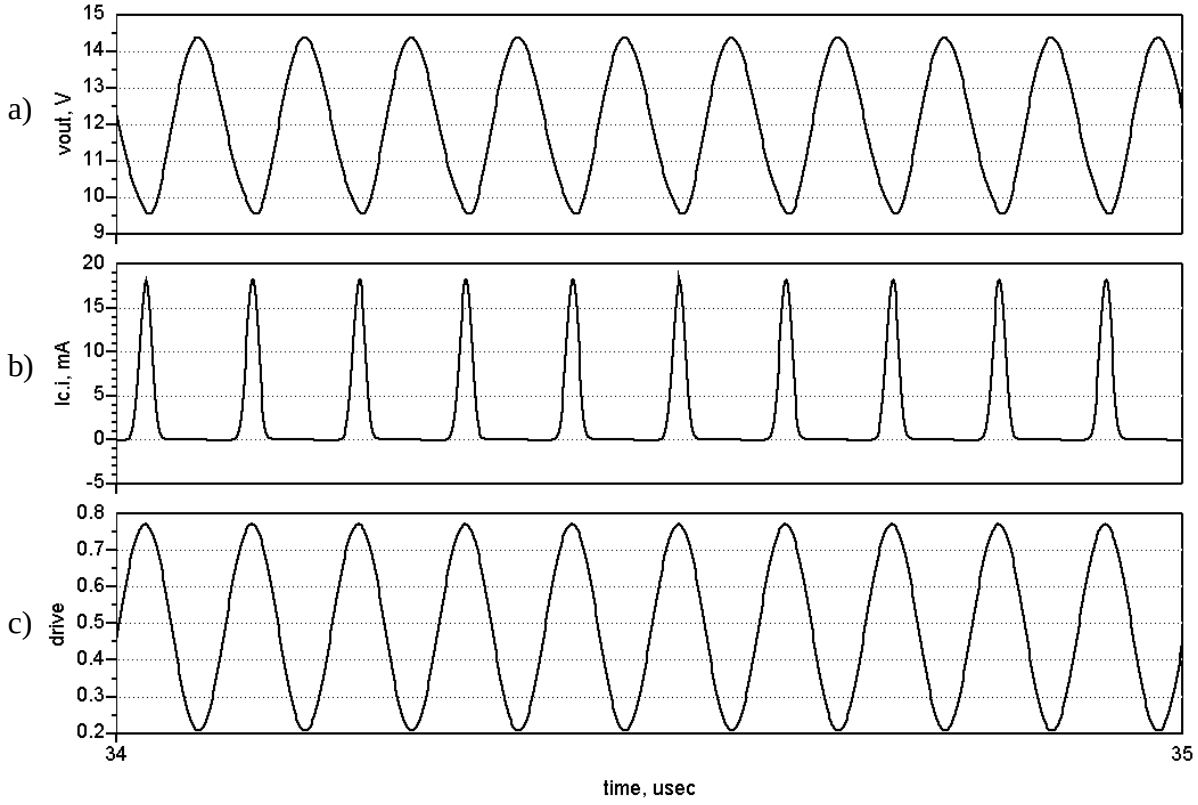

Figure 2.10. 10MHz example oscillator waveforms showing: a) collector output voltage; b) collector current; c) base-emitter drive voltage.

2.3 NOISE

Although all components of a circuit create noise, the major source of noise in an oscillator is the active device. The noise sources in any oscillator circuit ultimately combine to form amplitude modulation (AM) noise and phase modulation (PM) noise. The AM noise component is usually ignored because the gain limiting effects of the circuit control the output amplitude, allowing little variation due to noise. The PM noise is of great concern because it typically is an order of magnitude greater than the AM noise contribution and directly effects the frequency stability of the oscillator (Siweris, 1985) and related noise sidebands. Before accounting for noise effects in oscillator design, it is beneficial to understand how the noise arises in a transistor.

The designer has limited control over the noise sources in a transistor, only being able to control the device selection and bias point. For example, the bulk resistance of a transistor, upon which thermal noise depends, is an unchangeable, intrinsic property of the device. However, using knowledge about how noise affects oscillator waveforms, the designer is able to substantially improve phase-noise performance by the selection of bias point and signal level.

2.3.1 Sources of Noise

There are several primary noise sources in any electronic circuit: broadband sources due to thermal and shot noise effects as well as the low-frequency noise characteristics of $1/f$ noise. For example, current flow is not a continuous process, but is made up of the diffusive flow of many discrete carriers. The motions of these carriers are, on the atomic level, random, but they have been classified into general motions which can explain the noise phenomenon. The main mechanisms for noise in a semiconductor device include both thermal fluctuations in minority carrier flow and bulk and depletion area generation-recombination events (Buckingham,1983). The effects of these processes are categorized as thermal noise, shot noise, partition noise, burst noise and $1/f$ noise. Although thermal and shot noise are the two fundamental sources of noise for an RF oscillator, the others do exist and have important ramifications for near-sideband phase noise.

At any temperature above absolute zero, thermal agitation causes electrons in any conductor or semiconductor to be moving at random. Although, over a period of time, these perturbations average to zero, at any one instant of time the electrons may be concentrated in some areas more than others. These concentrations produce a potential referred to as thermal noise. Thermal noise is expressed as either a current or voltage associated with a resistance. The average thermal noise voltage squared is expressed as

$$\overline{v_n^2} = 4kTR\Delta f, \tag{17}$$

where k is Boltzman's constant, T is device temperature in $°K$, R is the resistance, and Δf is the associated bandwidth (Manasse et al. 1967). The basis for this noise arises from the degrees of freedom in a thermally agitated material with typical noise power per degree of freedom given by kTB. In a semiconductor, R is simply the resistance of the bulk material. Choosing a device with the least possible bulk resistance in combination with a low temperature will minimize the thermal noise created. The thermal noise expressed in Eq. (17) is spectrally flat at radio frequencies, far below the infrared spectral peak. While Eq. (17) is valid for RF design, thermal

noise power actually begins to increase in the high GHz range peaking somewhere in the infrared frequencies.

Shot noise is the noise generated by the movement of individual electrons within the current flow. One may conceptualize shot noise by thinking of the noise heard when rain is falling on a tin roof. It is a continuous roar made from the combination of many individual drops striking the roof surface. Shot noise is dependent on the average current providing this flow of charge and is described by the equation

$$\overline{i_n^2} = 2qI\Delta f, \tag{18}$$

where q is the charge of an electron, I is the DC current, and Δf is the associated bandwidth (Spangenburg, 1957). It can be seen that, like thermal noise, shot noise is spectrally flat as well. It is interesting to note that with a simple substitution into Eq. (18), the average noise current becomes

$$\overline{i_n^2} = \frac{2kT\Delta f}{\frac{kT}{qI}} \text{ or equivalently } \overline{v_n^2} = 2kT\left(\frac{kT}{qI}\right)\Delta f, \tag{19}$$

where kT/qI is the small signal resistance of the device and v_n is the Thevenin equivalent of the i_n. This shows that shot noise is, in effect, similar to thermal noise from an equation perspective.

In transistors, each current path will have its own associated shot noise. For example, a BJT will have shot noise for each of the emitter, base, and collector currents (Thornton, 1966). An additional source of noise resulting from shot noise is called partition noise. Partition noise occurs at current junctions and is caused by each electron having to make a decision to go one way or another. A statistical fluctuation in the collector and base currents equating to noise occurs (Krauss et al.,1980). In a BJT, the majority of electrons flow from the emitter into the collector. A fraction of the emitter current must also flow to the base. The splitting of the emitter current into the base and collector current components provides this basic partition noise contribution.

The final noise source, $1/f$ noise, also called flicker noise, is not a broadband phenomena like thermal and shot noise (Thornton, 1966). The nonlinear performance of oscillators transforms this low frequency $1/f$ noise by up-conversion into the near-sideboards of the fundamental oscillation signal (Hajimiri, 1998). The spectrum of $1/f$ noise varies inversely with frequency and therefore is only noticeable at low frequencies and near sidebands of an oscillator spectrum. The low frequency performance is shown in Fig 2.11. The upper frequency at which the $1/f$ noise sinks into the noise floor caused by thermal and shot noise in the device is called the $1/f$ corner frequency. This corner frequency is typically between 100Hz and 1MHz and the low frequency limit of $1/f$ noise has been followed to 10^{-7}Hz. A strict description of the low frequency limit is not available, but is not typically needed in the analysis. The exact sources of $1/f$ noise are not yet completely understood (Kogan, 1996), however it is basically agreed by most researchers that it is a result of carrier recombination in isolated traps caused by imperfections in the semiconductor crystal (Hooge, 1994; Kirtania et al., 1996; Kogan, 1996; Van Der Ziel et al., 1986). Although $1/f$ noise is current dependent, measurements must be performed on a device to know the exact $1/f$ characteristic (Kirtania et al. 1996). It is assumed in this thesis that the average current dependency of this noise is similar to that of shot noise.

A contributor to $1/f$ noise in a device is called Random Telegraph Noise (RTN), also known as burst noise. RTN is the observed phenomenon whereby device current switches between several discreet values at random times. RTN is closely linked with $1/f$ noise in that it has spectral components which contribute to low frequency noise (Kogan, 1996). A simple plot showing the RTN noise characteristic is shown in Fig 2.12.

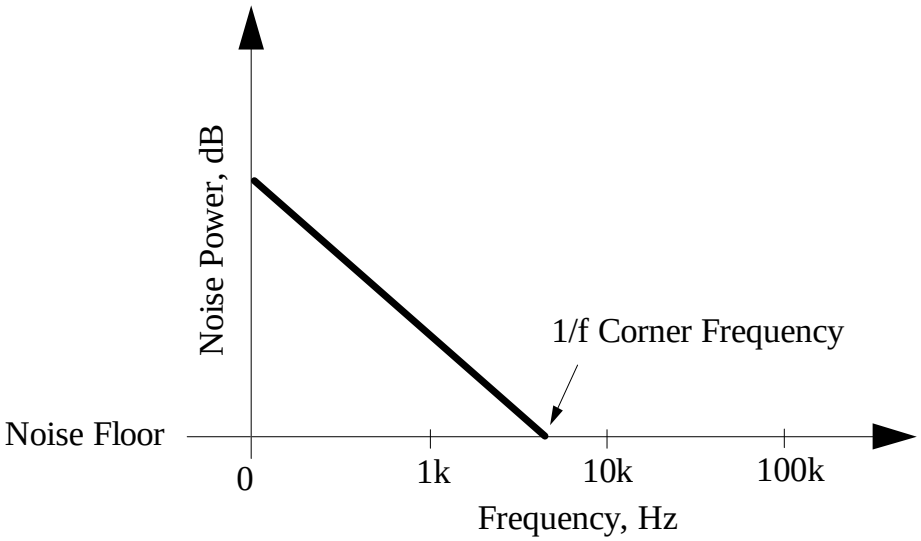

Figure 2.11. Possible $1/f$ characteristic of a transistor.

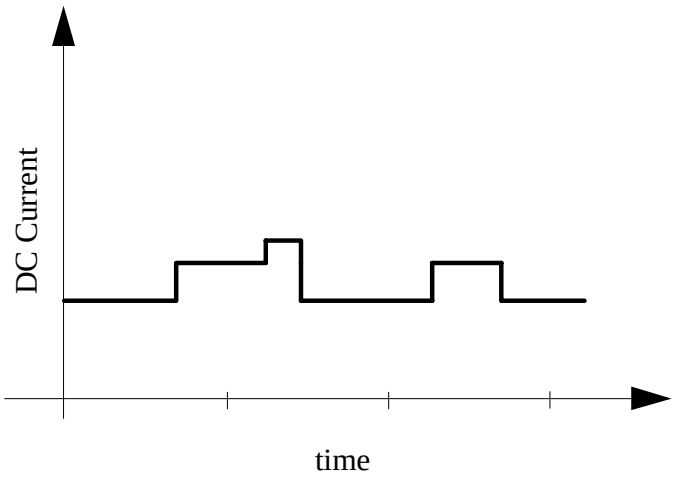

Figure 2.12. General RTN characteristic.

2.3.2 Oscillator noise models

There are, at present, two separate but closely related models of phase noise of oscillator output. The first is a collection of ideas put together by Leeson (1966). It will be referred to here as Leeson's model. Noise prediction using Leeson's model is based on the time-invariant properties of the oscillator such as resonator Q, feedback gain, output power, and noise figure. The second, an improvement on Leeson's model, was proposed by Lee and Hajimiri (1998, 2000). Lee and

Hajimiri's model is based on the time-varying properties of the oscillator current waveform and the resultant implications on phase noise production.

The phase noise output of an oscillator is measured as power relative to the power output at the center frequency. It is referred to in units of decibels below the carrier per hertz (dBc/Hz). The general phase noise output spectrum of an oscillator consists of three distinct sections located in the sidebands of the carrier frequency. Fig. 1 shows a single sideband (SSB) view of the oscillator phase noise for simplicity. Immediately surrounding the carrier frequency there exists a region of noise which decays as $1/f^3$. At some frequency offset called the $1/f^3 - 1/f^2$ corner frequency, the noise spectrum changes to a $1/f^2$dependence. The $1/f^2$ region continues on to the phase-noise floor of the circuit. The noise floor of the circuit is a result of thermal and shot noise sources. The noise floor exists across all frequencies, even in the $1/f^2$ and $1/f^3$ regions. The relative powers associated with each section depend on each section's corner frequency and the noise floor level.

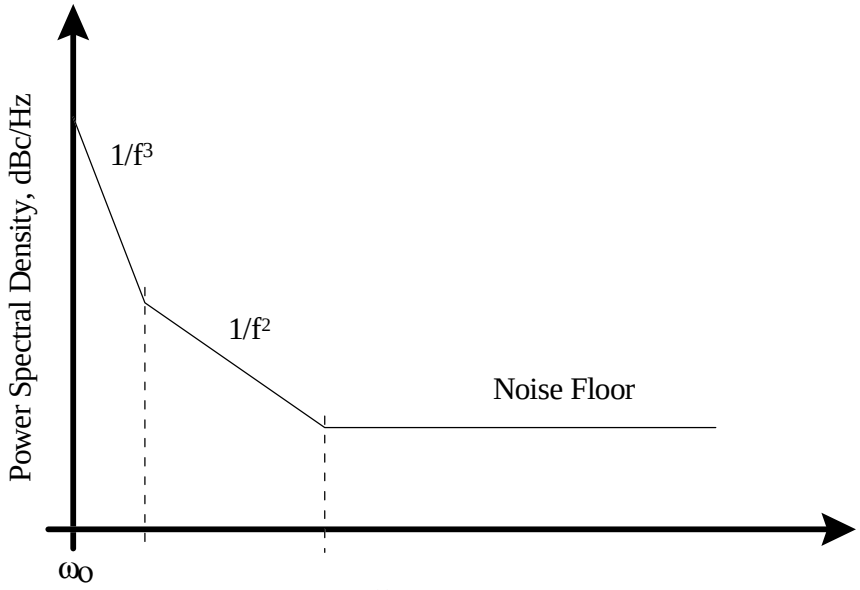

Figure 2.13. SSB oscillator phase noise output spectrum.

The $1/f^2$ region is unavoidable as it is a result of the characteristics of the oscillator resonator. Any LC resonator will have a voltage dependence which varies as $1/f$ from the center frequency. Since power is proportional to voltage squared, the resulting power spectrum is therefore $1/f^2$. The $1/f^3$region comes from upconverted $1/f$ noise of the device. The $1/f^3$dependency appears when $1/f$ is multiplied by the $1/f^2$characteristic of the resonator resulting in $1/f^3$.

The phase-noise models summarized below are both taken from Hajimiri and Lee (Hajimiri, 1998; Lee ,2000). Leeson's phase-noise model is

$$L\{\Delta\omega\} = 10\log\left\{\frac{2FkT}{P_{sig}}\left[1+\left(\frac{\omega_o}{2Q\Delta\omega}\right)^2\right]\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\}, \tag{20}$$

where $L\{\Delta\omega\}$ is SSB noise spectral density in units of dBc/Hz. The symbol k is Boltzman's constant, T is temperature in Kelvin, P_{sig} is the oscillator signal power, ω_o is the oscillation

frequency, and $\Delta\omega$ is the offset from ω_o. The quality factor Q is the loaded Q of the oscillator resonator, F is the noise figure of the oscillator, and $\Delta\omega_{1/f^3}$ is the corner frequency between the $1/f^3$ and $1/f^2$ regions. In Leeson's model $\Delta\omega_{1/f^3}$ is equal to the $1/f$ noise corner frequency of the device. In practice, $\Delta\omega_{1/f^3}$ is rarely equal to the $1/f$ noise corner of the device (Lee, 2000). An existing problem is that the noise figure of an oscillator is extremely difficult to predict (Robins, 1982). The factor F remains a correction factor which can only be determined by measurement of the phase noise spectrum of the oscillator. Since F and $\Delta\omega_{1/f^3}$ must almost always be measured from the oscillator spectrum, the predictive power of Eq. (20) is quite limited. From Eq. (20) it can be seen that the corner frequency at which the $1/f^2$sinks into the noise floor is exactly equal to the resonator half bandwidth, $\omega_o/2Q$. This also is not completely justifiable. In summary, according to Leeson's model, the only way to improve $L\{\Delta\omega\}$ is to increase the output power or increase the loaded Q of the resonator. It is important to note here that oscillator must be designed so that the transistor does not saturate. Saturation lowers the Q of the entire oscillator circuit, thus increasing phase noise (Rhea, 1990).

Lee and Hajimiri approached oscillator noise by first looking at how a noise impulse would affect a periodic signal. Fig. 2.14 shows how such an impulse injected onto a periodic waveform may cause phase disturbances.

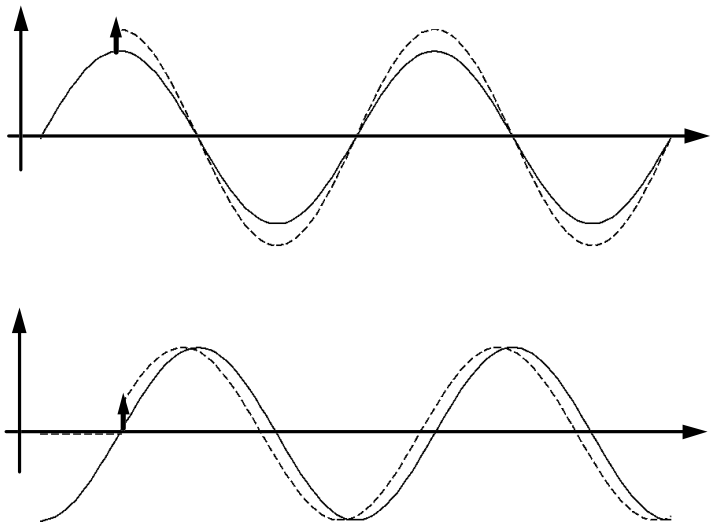

Figure 2.14. Impulse effects on a sinusoid (Hajimiri, 1998)

If an impulse is injected at the peak of the signal it will cause maximum amplitude modulation and no phase modulation. If an impulse is injected at the zero crossing of the signal there will be no amplitude modulation and maximum phase modulation. Injected between the zero crossing and the peak, there will be components of both phase and amplitude modulation. Remember, as suggested earlier amplitude variations are generally ignored because they are limited by the gain control mechanism of the oscillator. Therefore, according to this theory, to obtain the minimal phase noise, any noise impulses should coincide in time with the peaks of the output voltage signal.

Hajimiri and Lee (1998) introduced an impulse sensitivity function (ISF), $\Gamma(x)$, for each oscillator. Simply put, an ISF is a dimensionless function periodic in 2π, greatest where an impulse will potentially cause the most phase modulation and smallest where an impulse would

cause the most amplitude modulation. Fig. 2.15 shows the ISF for a sample LC oscillator.

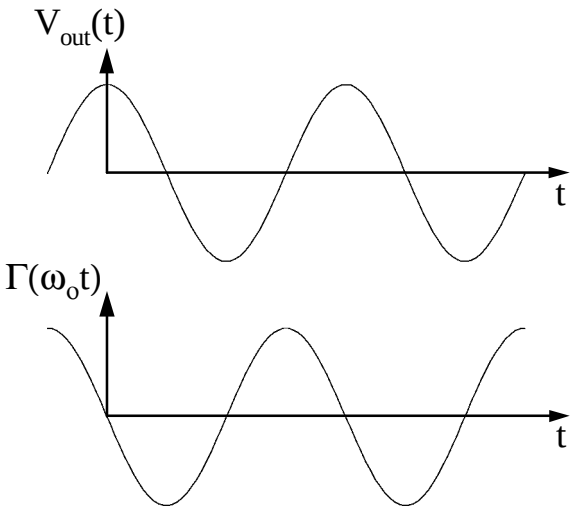

Figure 2.15. ISF of an LC oscillator (Hajimiri, 1998).

Since the ISF is periodic, it can be expressed as a Fourier series in the form of

$$\Gamma(\omega_o\tau) = \frac{c_o}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_o\tau + \theta_n). \tag{21}$$

Hajimiri and Lee explain that the noise at each frequency is converted to the noise sidebands depending on the Fourier coefficients. The device $1/f$ noise is upconverted to become $1/f^3$noise around the carrier, ω_o, and is related to c_0. Device noise close to ω_o is also present and depends on c_1. The $1/f^2$ region comes from downconverted white noise at harmonic frequencies. Noise downconverted from $2\omega_o$ depends on c_2. Noise from $3\omega_o$ depends on c_3 etc...

As compared to Leeson's equation, the equations for the various sections of the SSB phase noise spectrum using Hajimiri and Lee's method are:

The $1/f^3$portion,

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot Log\left(\frac{c_o^2}{q_{max}^2} \cdot \frac{i_n^2/\Delta f}{8\Delta\omega^2} \cdot \frac{\omega_{1/f}}{\Delta\omega}\right), \tag{22}$$

and the $1/f^2$portion,

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot Log\left(\frac{\Gamma_{rms}^2}{q_{max}^2} \cdot \frac{i_n^2/\Delta f}{4\Delta\omega^2}\right), \tag{23}$$

The coefficient c_o is the 0th-order component of the ISF, i_n is the noise current magnitude, Δf is the noise bandwidth, $\omega_{1/f}$ is the $1/f$ noise corner frequency of the device, $\Delta\omega$ is the offset from the carrier frequency, q_{max} is the maximum charge on the capacitors in the resonator, and Γ_{rms} is the rms value of the ISF.

The implication of Lee and Hajimiri's theory is that the designer does have some control over how noise is injected into the circuit. From Section 2.2.1, it was demonstrated that the drive

voltage produces an output current consisting of a series of pulses. During the time between pulses, the current will be negligible or zero. Therefore, aside from thermal noise, the noise sources which depend on current such as shot, partition, and $1/f$, exist only during the current pulses. Fig. 2.16 shows the output voltage and how noise shows up relative to current for a Colpitts oscillator. The natural operation of the oscillator will cause the current pulses to be centered on the negative peaks of the resonator tank voltage. If the current pulse, and consequently the noise pulse, is wide, it will have components which contribute a substantial amount of PM noise. If the drive level is increased the current/noise pulse will become narrower and therefore have less PM noise contribution than the wider pulse.

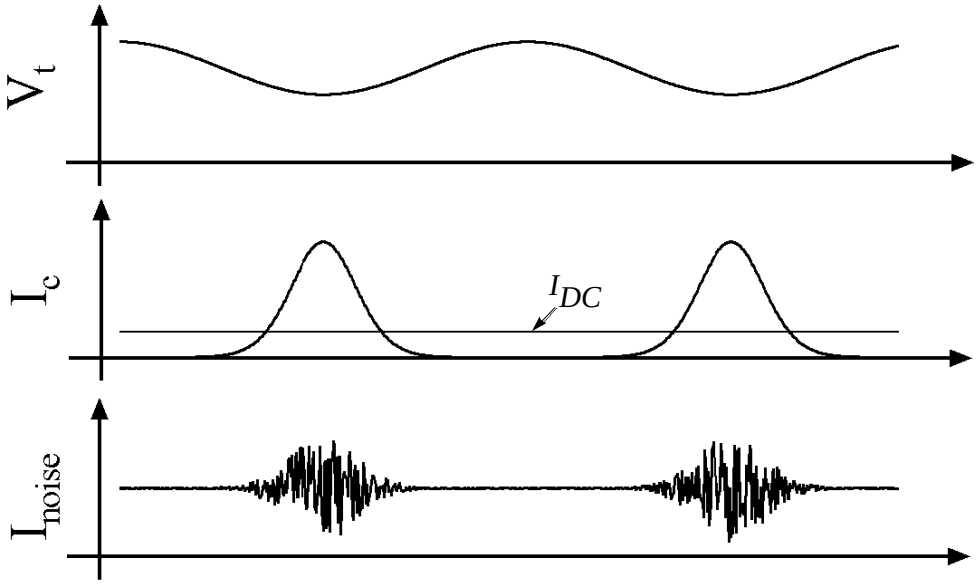

Figure 2.16. Oscillator circuit waveforms demonstrating noise current flow relative to the output voltage peaks. The majority of noise current exists only during collector current pulses.

The following chapter will connect this noise concept and the nonlinear design process in an example specifically designed to demonstrate the design options available to an engineer to lower oscillator phase noise.

Chapter 3

Verification

A common-collector configuration is again used to demonstrate the basic design and performance trade-offs of oscillators. The oscillator circuit to be considered is an example of an active-biased, 700MHz oscillator exhibiting saturation and excessive harmonics. Saturation and high harmonic content are often considered to be undesirable traits of an oscillator (Rhea, 1990). The non-ideal operation of the example oscillator served as a reference to show how nonlinear design techniques may be employed for redesigning the oscillator for improved performance. Two alternative designs were created to improve phase-noise performance and decrease harmonics, while delivering the same power as the example. One of the designs was configured using an active bias; the other was configured as a passive, four-resistor bias.

These design concepts were extended to demonstrate Lee and Hajimiri's phase-noise theory. The oscillators produced the same power, but with differing current pulse widths for phase-noise comparison. Five active bias oscillators and five passive bias oscillators were designed. Each oscillator produced 5mW with drive levels of $x = 6$, 8, 10, 12, and 20. The single-sideband phase-noise characteristics of all designs were simulated from 100Hz to 100kHz above the oscillator center frequency (700MHz) using ADS software.

At 700MHz, the design requires additional factors to be considered. Operation at such a high frequency introduces parasitic effects not typically observed at low frequencies. The design principles presented in Chapter 2 still hold at high frequencies, but the engineer must realize that additional reactances associated with the pn junctions of the transistor and the transistor packaging exist. Fig. 3.1 shows the packaging parasitics associated with the NE68819. All oscillators simulated here use the NE68819 bipolar transistor (BJT), which was developed for use in oscillators and low-noise amplifiers in the GHz range (NEC, 1995).

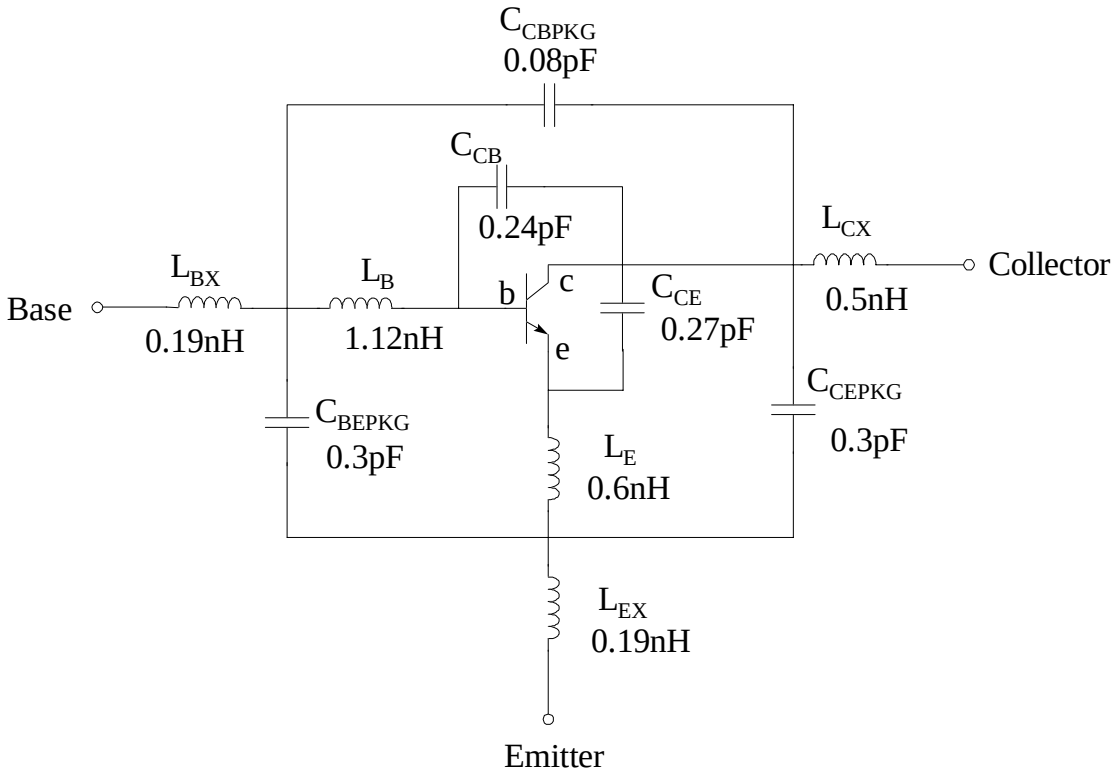

Figure 3.1. Packaging parasitics of NE68819 (CEL, 1998)

For all of the oscillator designs below, the resonator capacitor C_2 was connected between the base and emitter terminals in Fig 3.1. The combination of reactances from L_{BX}, L_B, C_{CBEPKG}, L_E, L_{EX}, and the transistor base-emitter capacitance were accounted for when solving Eq. (15) for capacitor C_2. Additionally, the transistor packaging capacitance C_{CBPKG}, along with the collector-base junction capacitance were included in the reactance of the oscillator inductor L through the Miller effect (Hambley, 1994).

Using the circuit in Fig. 3.1 for the NE68819 in simulation allowed measurement of the actual drive level and current in the intrinsic transistor itself. Measurements of drive voltage and collector current were performed at the terminals labeled b, c, and e. Had these measurements been taken at the package leads 'base', 'collector, and 'emitter', the results would not have been accurate due to the packaging reactances, though results would have demonstrated similar trends.

3.1 How ADS Simulates Phase Noise

ADS simulates phase noise using two methods: analysis of the oscillator's frequency sensitivity to noise, and small-signal mixing of noise. The mixing analysis tends to be accurate for large offset frequencies and the sensitivity analysis tends to be accurate for close-in phase noise. Phase noise simulation at frequencies relatively close to the carrier were required, therefore, the frequency sensitivity to noise method was employed.

The frequency sensitivity to noise is found from the large-signal harmonic balance solution of the oscillator by accounting for the effects of all sources injecting noise into the circuit. Phase

noise is computed from the total spectral density of frequency fluctuations summed over every noise source (Hewlett-Packard, 1999).

3.2 Basic Oscillator Simulations

3.2.1 700MHz Example Oscillator

The oscillator considered is shown in Fig. 3.2. It is a typical, active-bias, Colpitts oscillator circuit, similar to those circuits presented by Rhea (1990). The active bias circuit is created by the two pnp transistors labeled Q2 and Q3. A 25Ω load is coupled to the collector of the oscillator transistor Q1 through a 470pF coupling capacitor. The 9pF and 8.8nH parallel circuit allows the fundamental-frequency loading effects of the 22Ω resistor to be multiplied to about 400Ω at the emitter terminal.

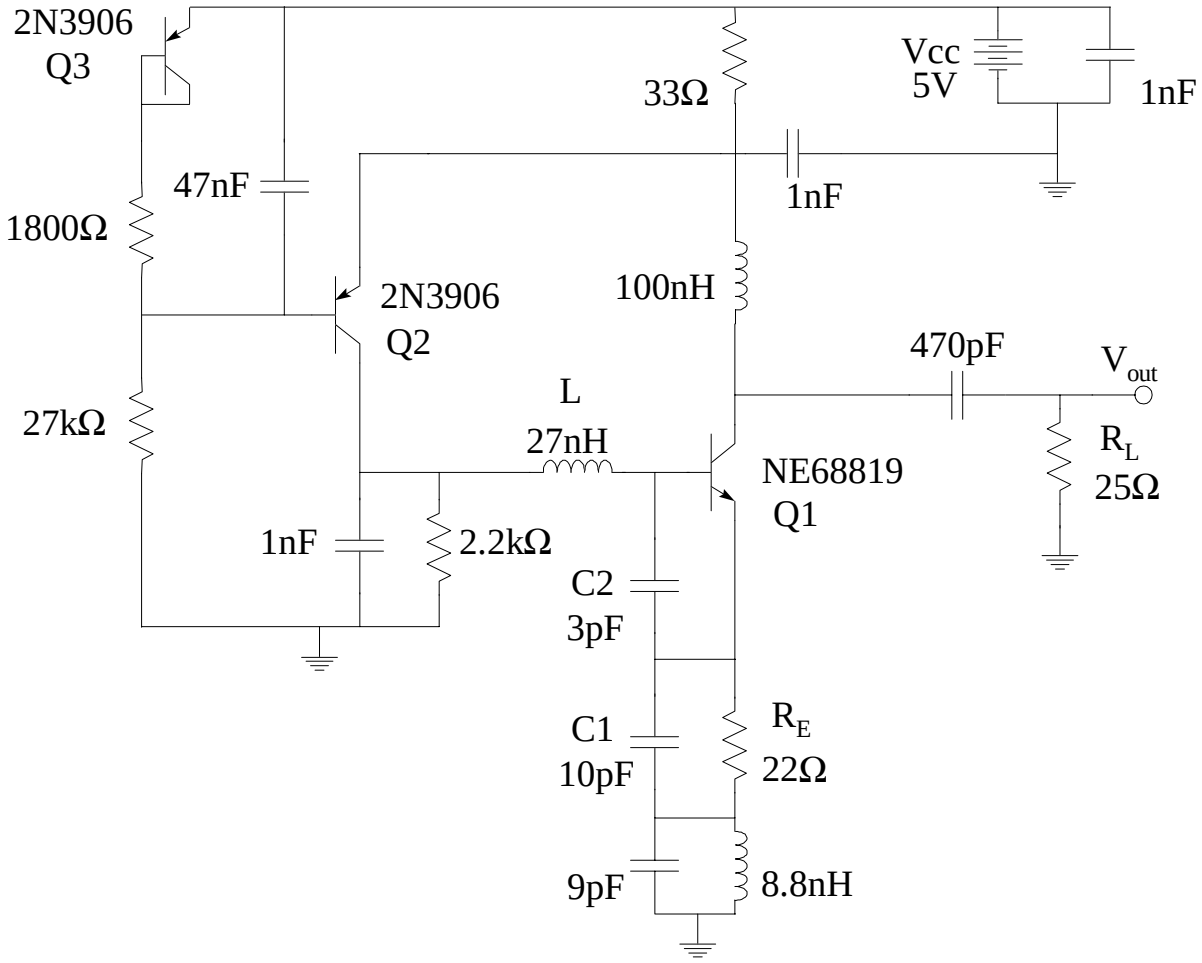

Figure 3.2. 700MHz 20mW example oscillator schematic

Upon visual inspection of the waveform in Fig. 3.3c, it can be seen that the output voltage, V_{out}, is periodic, but highly non-sinusoidal because of high harmonic content. Voltage V_{out} shows approximately a 1 volt peak into the 25Ω load resistor, corresponding to an output power of

20mW. Fig 3.3a shows the collector current envelope from startup through 300ns. The collector current takes approximately 250ns to settle to a steady-state peak of 40mA. The graphic in Fig 3.3b is a view of NE68819 collector current for three cycles of oscillation. It is interesting that the shape of each pulse resembles a 'V' shape. As each pulse reaches 40mA, the NE68819 saturates, and the current flow is redirected to the base. As the transistor comes out of saturation, current flow resumes for the remainder of the pulse.

In a BJT transistor, saturation occurs while the emitter voltage is equal to the collector voltage. In Fig. 3.4 the NE68819 is in a state of saturation while $V_{\mathrm{e}} = V_{\mathrm{c}}$. The duration of saturation corresponds to the time, in Fig 3.3b, during which the collector current approaches zero half way through the pulse and the emitter is charging the base circuit.

Normal operation of a BJT requires that the base-collector junction remains reverse-biased at all times. In Fig. 3.4 V_{b} rises above V_{c}, forward biasing the base-collector junction for saturation. The drive voltage V_1, the difference between the base and emitter voltages, is shown in Fig. 3.3c. Voltage V_1 is approximately 4.9V peak-to-peak, corresponding to $x = 94$. This is an $extremely$ high drive level. If $x = 94$ is used in Eq. (8), the first, second, third, and fourth harmonics will all be $2I_{DC}$.

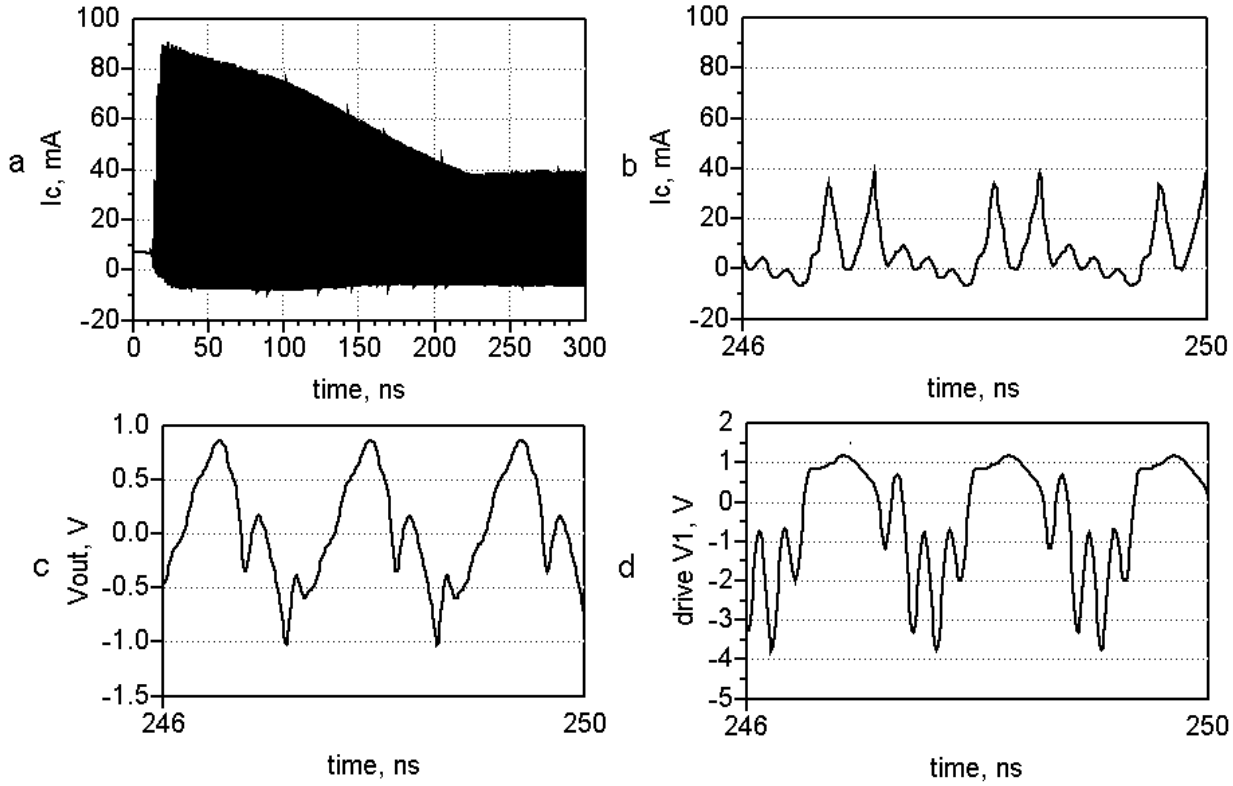

Figure 3.3. 700MHz 20mW example oscillator waveforms showing: a) collector current from start-up to 300ns; b) steady-state collector current for three oscillation cycles; c) output voltage across 25Ω load resistor; d) drive voltage.

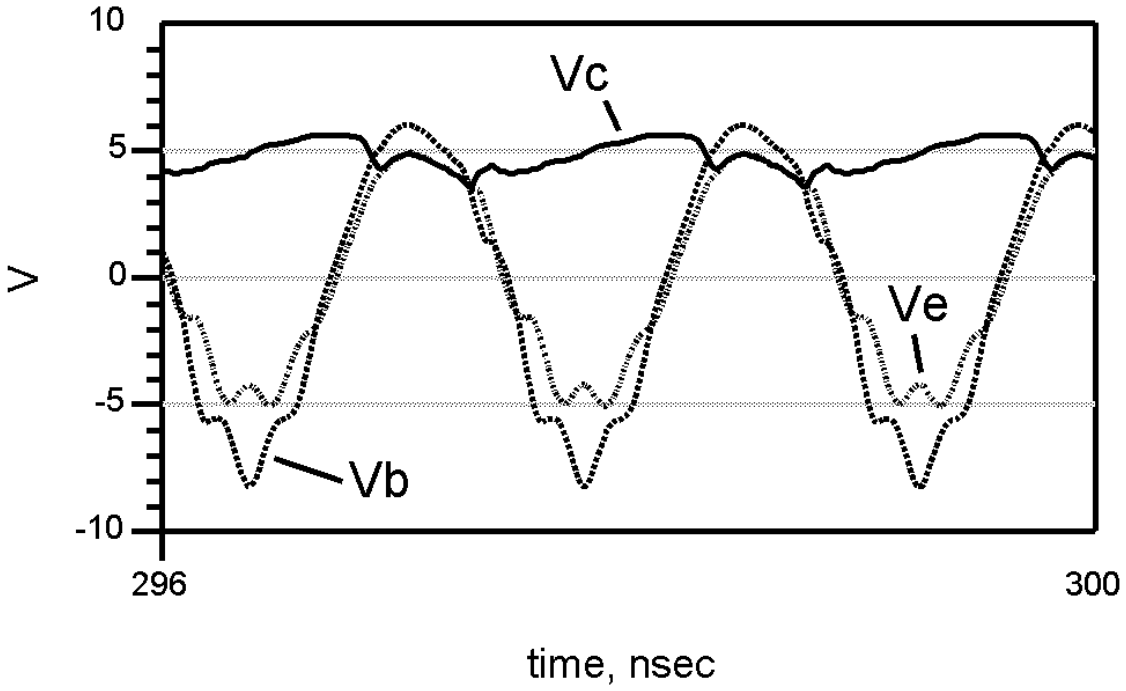

Figure 3.4. NE68819 collector, base, and emitter voltages of the 700MHz example show that the transistor saturates while Ve = Vc. The collector-base junction is reverse biased while Vb > Vc.

3.2.2 Redesign with Active Bias

The active-bias redesign circuit is almost exactly the same as the example in Fig 3.2. However, several modifications were made: resistor R_e was inserted to limit the start-up current pulse, bypass capacitors were reduced to 100pF to reduce charging time constants in the bias, and C_t and L_t were inserted for tuning. Table 3 lists the component values used for the 20mW active-bias oscillator redesign.

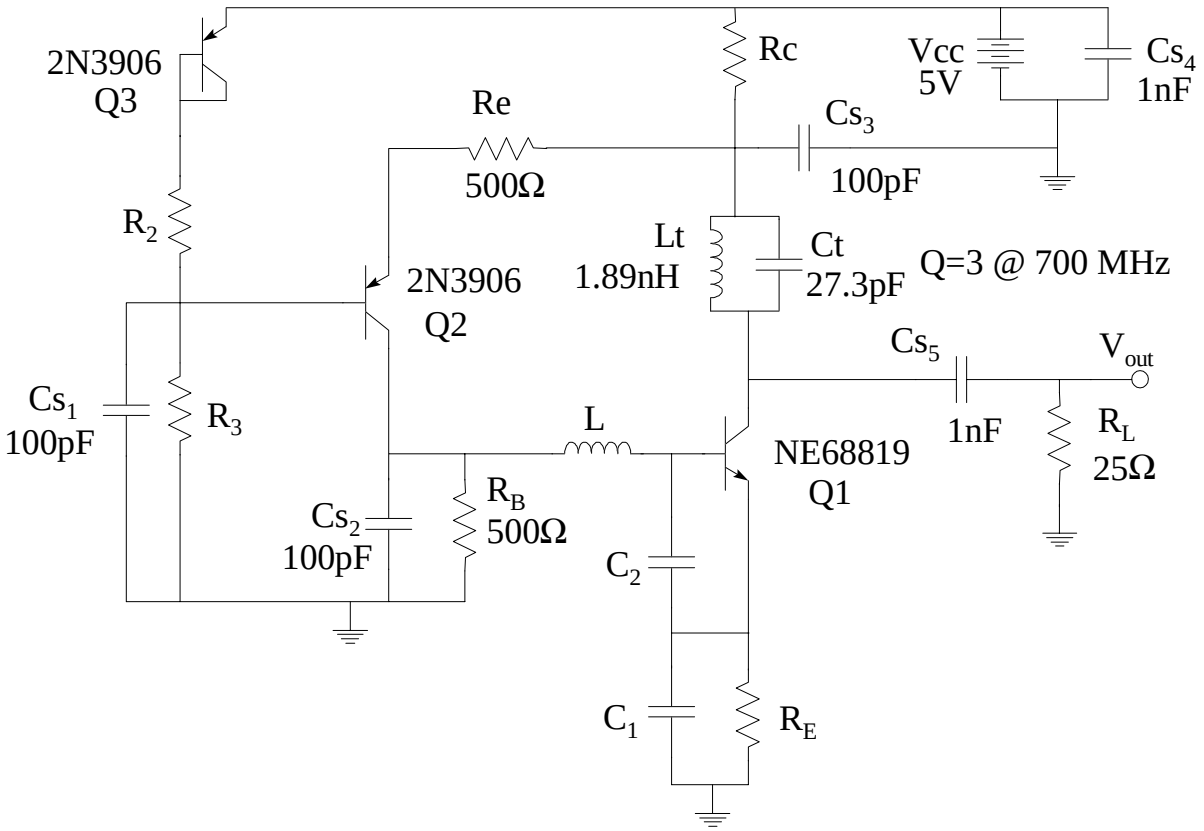

Figure 3.5. Active bias oscillator schematic.

Table 3. Component values and DC current of 20mW active bias redesign.

P_{out}, mW	x	L, nH	C_1, pF	C_2, pF	R_2, Ω	R_3, Ω	R_E, Ω	I_{DC}, mA
20	44	2.4	50.0	50.0	551	592	55	12.4

Fig. 3.7 and Fig. 3.8 show the waveforms of the 20mW active bias redesign. Fig. 3.7a shows an improved settling time over the example in Fig. 3.4a. The current pulses in Fig. 3.7b are not affected by saturation as in the example. The ripples seen following each current pulse in Fig. 3.7b are caused by resonating currents in the transistor packaging parasitic reactances. The ripple is a trait of all oscillators simulated here. The packaging parasitics of the transistor resonate at higher frequencies and cause the ripple. Voltage V_{out} in Fig. 3.7c is much more sinusoidal than the example V_{out} and has a low harmonic content. Addition of the tuned circuit and the use of a much lower drive level contributed to the lower harmonic levels.

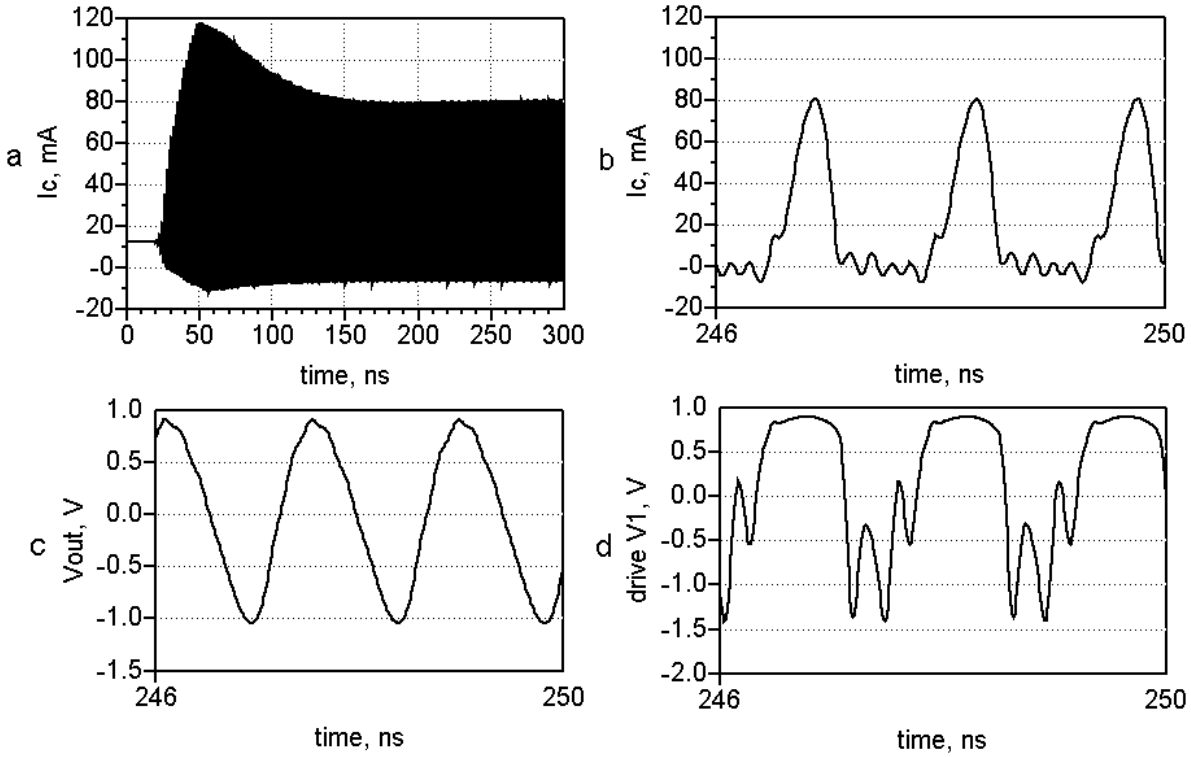

Figure 3.6. Active-bias 20mW oscillator waveforms showing: a) collector current from start-up to 300ns; b) steady-state collector current for three oscillation cycles; c) output voltage across 25Ω load resistor; d) drive voltage.

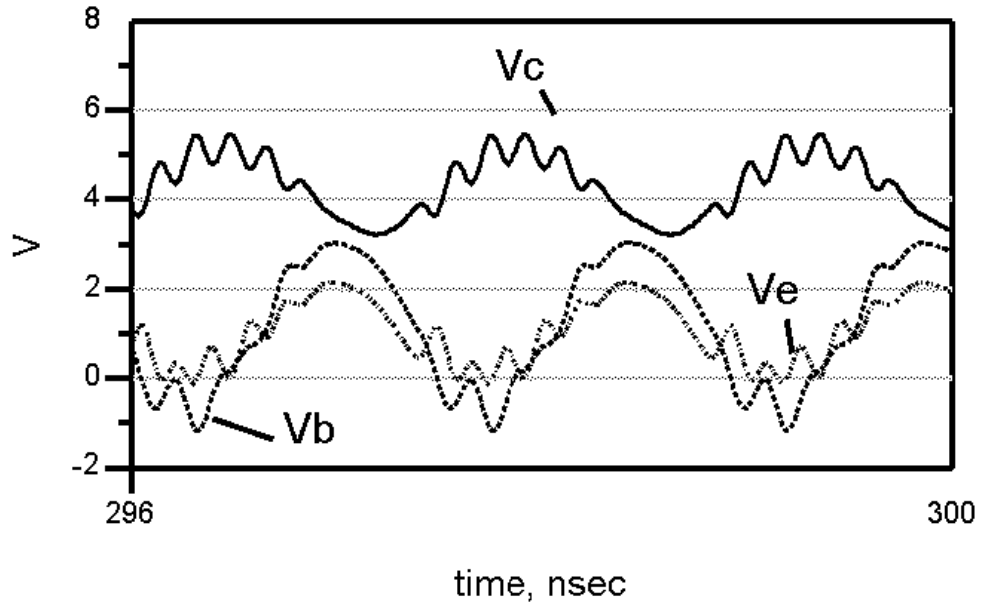

Figure 3.7. NE68819 collector, base, and emitter voltages for the 20mW active bias redesign show that the transistor does not exhibit saturation.

3.2.3 Redesign with Four-Resistor Bias

The goal of introducing the four-resistor bias, shown in Fig. 3.9, was to compare phase noise performance with the active bias circuit. The 20mW oscillator was designed to compare with the 700MHz example. A stable bias was chosen to avoid any bias shift. A general guideline was to keep V_E, the DC emitter voltage, on the order of V_{BE} of the NE68819. Additionally, to eliminate the effects of β on bias current, R_B ($R_2 \parallel R_3$) was made approximately equal to R_E. Eq. (16) solve for the bias. Resistor R_1 was left at 33Ω, though not required for this design. As with the active-bias redesign, the collector was tuned to a Q of 3 at 700MHz by inductor L_t and capacitor C_t. Capacitors labeled C_s are selected to provide short circuits at 700MHz. Table 4 shows all component values for the four-resistor bias redesign.

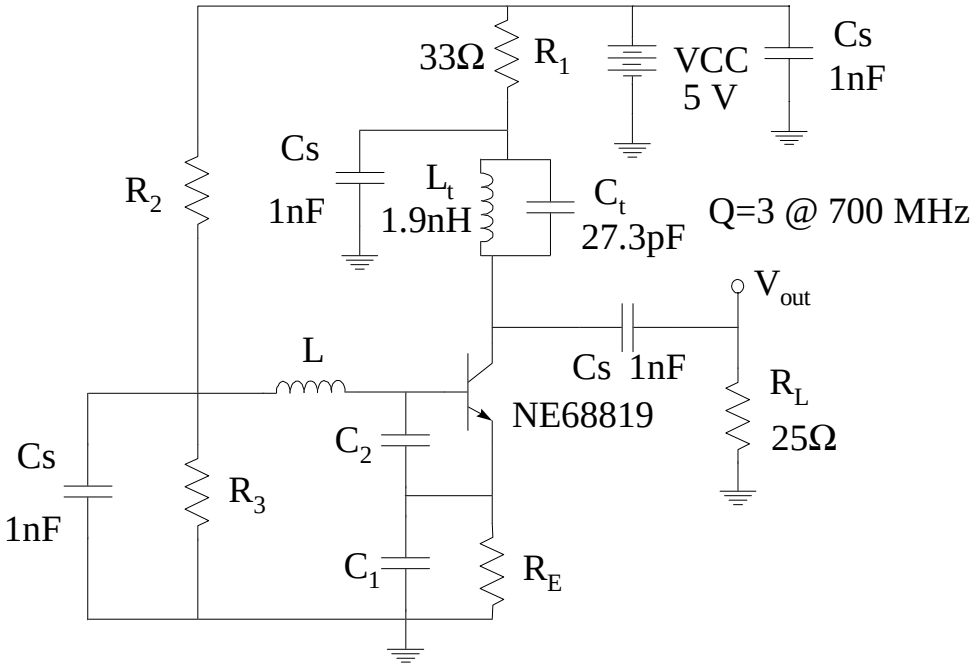

Figure 3.8. Four-resistor bias oscillator schematic.

Table 4. Component values and DC current of 20mW four-resistor bias redesign.

P_{out}, mW	x	L, nH	C_1, pF	C_2, pF	R_2, Ω	R_3, Ω	R_E, Ω	I_{DC}, mA
20	44	2.2	40.0	45.0	120	36	50	7.2

Figs. 3.10 and 3.11 show the waveforms of the 20mW four-resistor bias redesign. Fig. 3.10a shows that there is almost no settling time with the four-resistor bias. The current pulses in Fig. 3.10b are not affected by saturation as in the example. Three cycles of the collector, emitter, and base voltages are shown in Fig. 3.11. This oscillator exhibits no saturation and does not reverse bias the collector-base junction of the transistor. Voltage V_{out} in Fig. 3.10c is much more sinusoidal than the example V_{out} and has a low harmonic content. Addition of the tuned circuit and a much lower drive level contributed to the lower harmonic levels.

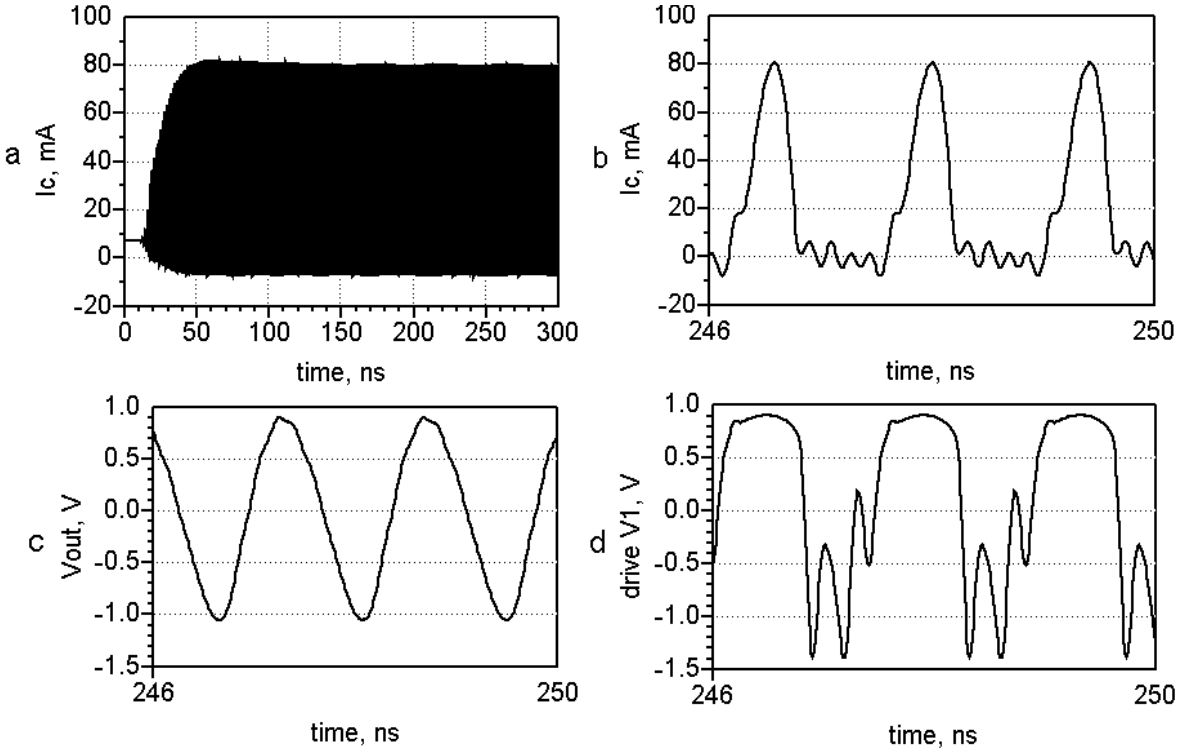

Figure 3.9. Four-resistor bias 20mW oscillator waveforms showing: a) collector current from start-up through 300ns; b) steady-state collector current for three oscillation cycles; c) output voltage across 25Ω load resistor; d) drive voltage.

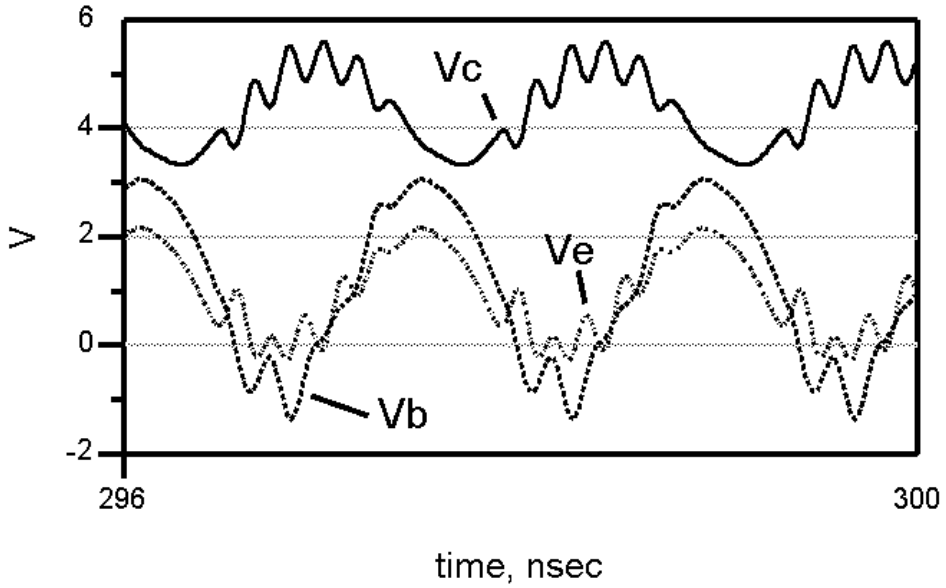

Figure 3.10. NE68819 collector, base, and emitter voltages for the 20mW four-resistor bias redesign show that the transistor does not exhibit saturation.

3.2.4 Redesign Noise Comparison

Fig. 3.11 shows a phase noise comparison between the example oscillator, the 20mW active-bias and 20mW four-resistor bias redesigns. The general schematics for the active bias and four-resistor bias redesign circuits are shown in Figs. 3.5 and 3.8 respectively. The circuit component values for each oscillator are found in Tables 3 and 4. Phase noise was improved by approximately 3dB by the redesigned oscillators. Recall that each redesigned oscillator does not exhibit transistor saturation and has very low harmonic content.

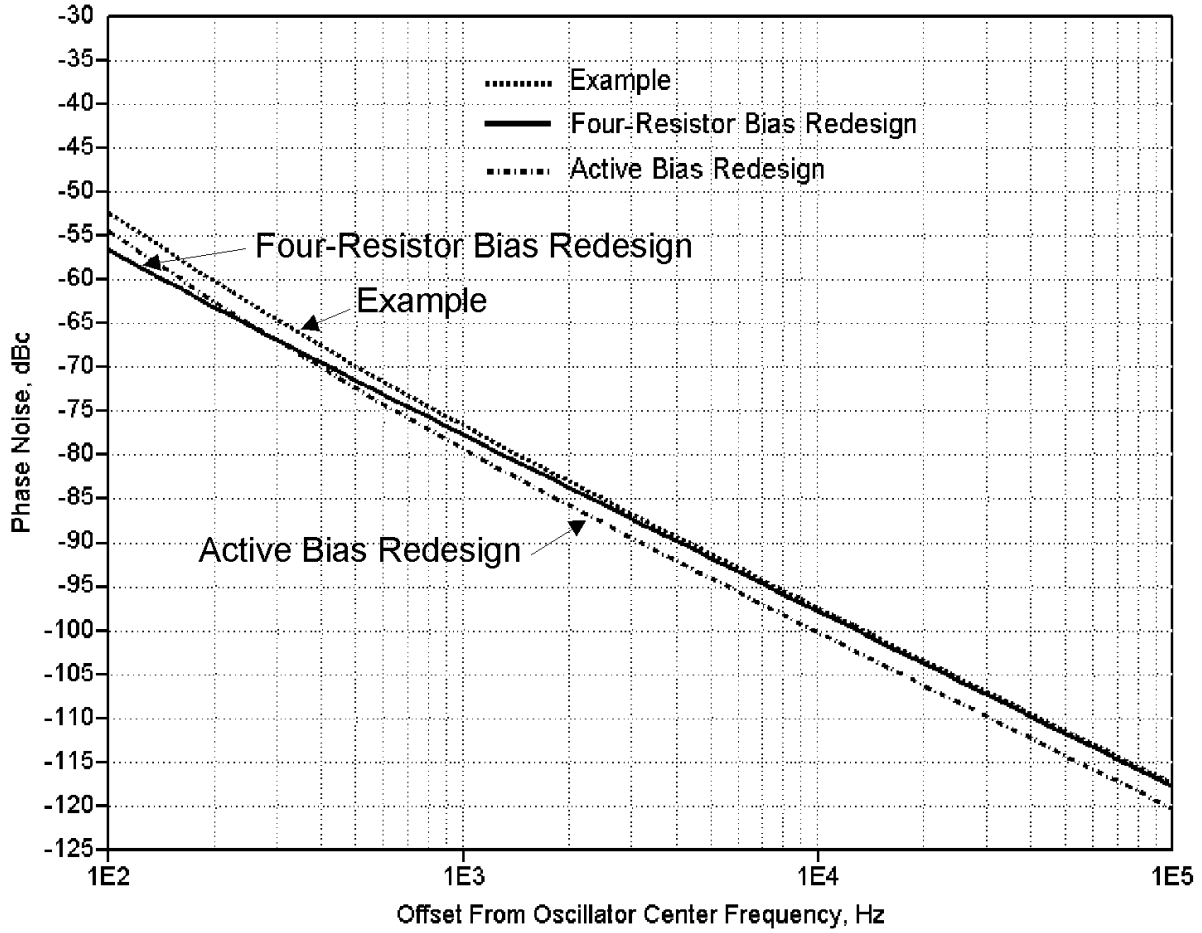

Figure. 3.11. Phase noise of 700MHz example, 20mW active bias redesign, and 20mW four-resistor bias redesign.

3.3 Phase Noise - Pulse Width Comparison

The circuits of Fig. 3.5 and 3.8 were used in simulation to demonstrate the phase noise - pulse width relationship. The designs presented are the same as the 20mW redesigns except that the output power requirement was decreased to 5mW. Phase noise for each oscillator is compared

for each bias configuration. Tables 5 and 6 show the component values and DC current for each set of oscillators designed.

Simulated phase noise of the 5mW active bias oscillators is shown in Fig. 3.12. As x increases the pulse width decreases and phase noise is thus reduced. The relationship between x and current pulse width is shown in Fig. 3.13 for the active bias oscillators. Since all oscillators are producing 5mW, the area under each pulse is approximately equal.

Table 5. Component values and DC current of 5mW active-bias oscillators.

P_{out}, mW	x	L, nH	C_1, pF	C_2, pF	R_2, Ω	R_3, Ω	R_E, Ω	I_{DC}, mA
5.0	6	5.0	5.3	42.0	563	604	43	14.3
5.0	8	5.5	5.9	40.2	563	604	56	12.3
5.0	10	6.3	5.8	35.4	563	604	63	11.4
5.0	12	6.1	7.3	35.4	563	604	74	10.3
5.0	20	5.2	11.2	35.4	563	604	108	7.88

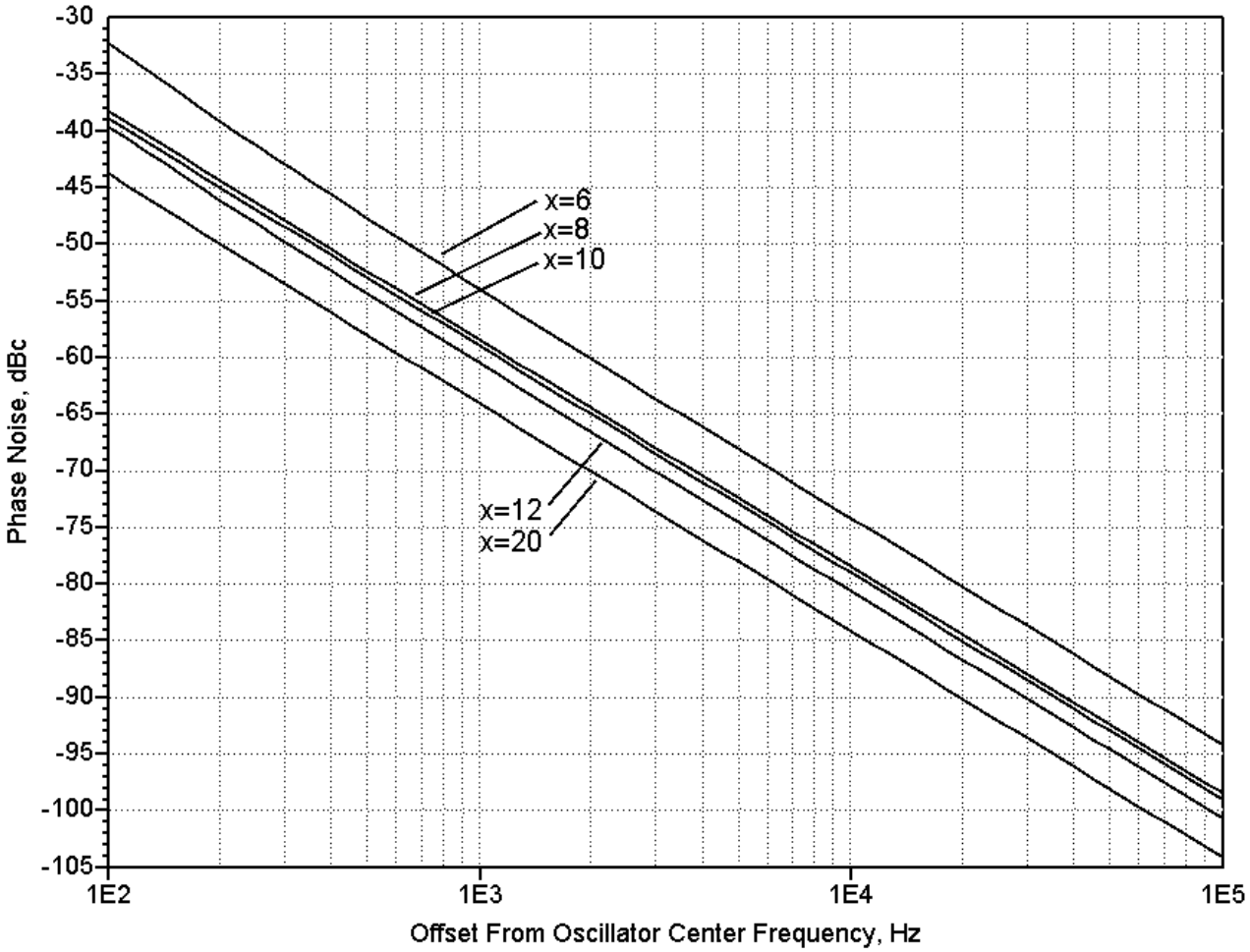

Figure 3.12. Phase noise comparison of 5mW active bias oscillators.

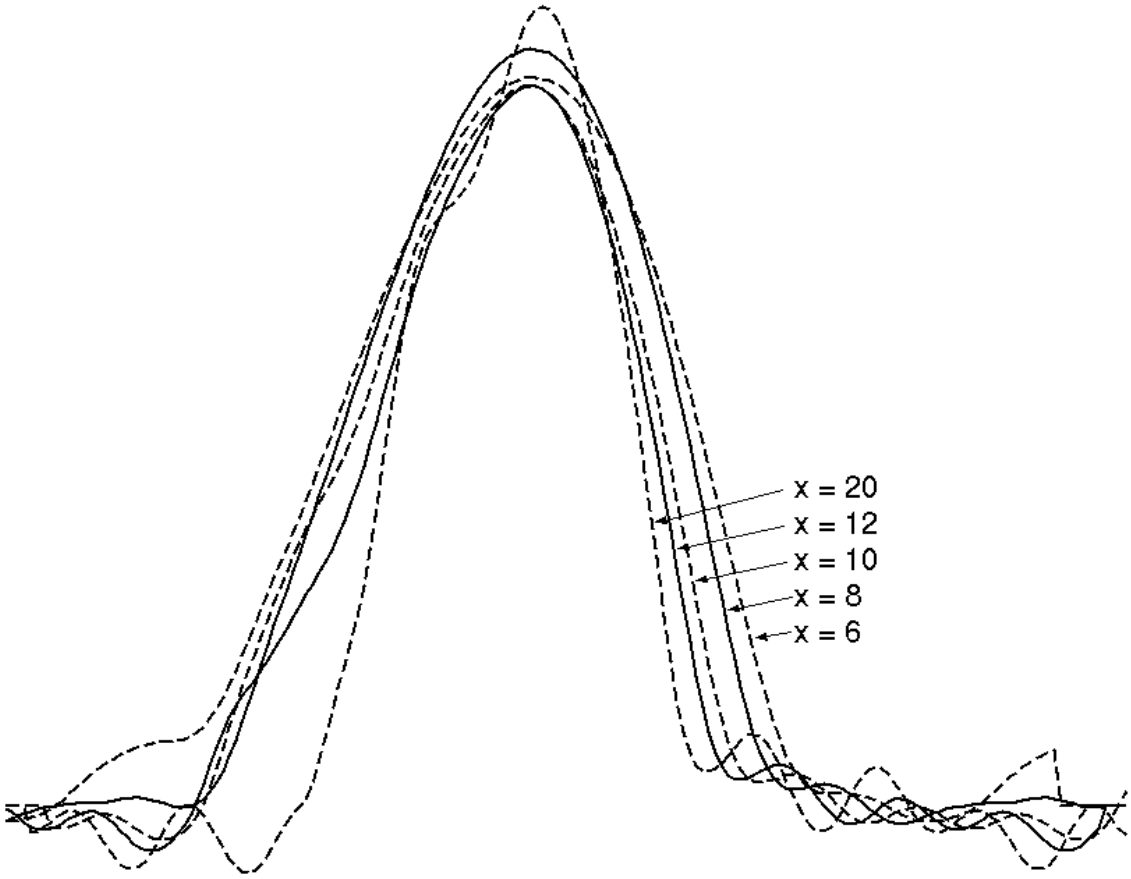

Figure 3.13. Collector current pulse-width comparison of 5mW active bias oscillators.

Table 6. Component values and DC Current of 5mW four-resistor bias oscillators.

P_{out}, mW	x	L, nH	C_1, pF	C_2, pF	R_2, Ω	R_3, Ω	R_E, Ω	I_{DC}, mA
5.0	6	6.1	3.7	45.0	222	130	75	13.5
5.0	8	5.5	5.8	45.0	222	110	75	11.2
5.0	10	5.2	7.5	45.0	222	106	75	10.6
5.0	12	4.5	10.3	45.0	222	98	75	9.6
5.0	20	3.2	20.5	45.0	222	75	75	6.2

As with the Active-Bias oscillators, the pulse width and DC current decrease. These decreases are accompanied by a corresponding decrease in the phase noise. The phase noise results of the four-resistor 5mW designs are shown in Fig. 3.14, and current pulse widths of each oscillator are compared in Fig 3.15. The lowest drive level, $x = 6$, had the highest phase noise as well as the widest current pulse.

Fig 3.16 shows the Phase noise of all ten 5mW oscillators. The dashed lines are phase noise of the active bias oscillators and the solid lines represent the four-resistor bias oscillators. For each bias topology, the highest phase noise level was for $x = 6$, while the lowest noise corresponded to $x = 20$. Beginning at the top two curves, each successively lower phase noise

corresponds to the next higher value of x. For equal pulse widths and drive level, the four-resistor bias phase noise performance is slightly better than the active biased oscillators.

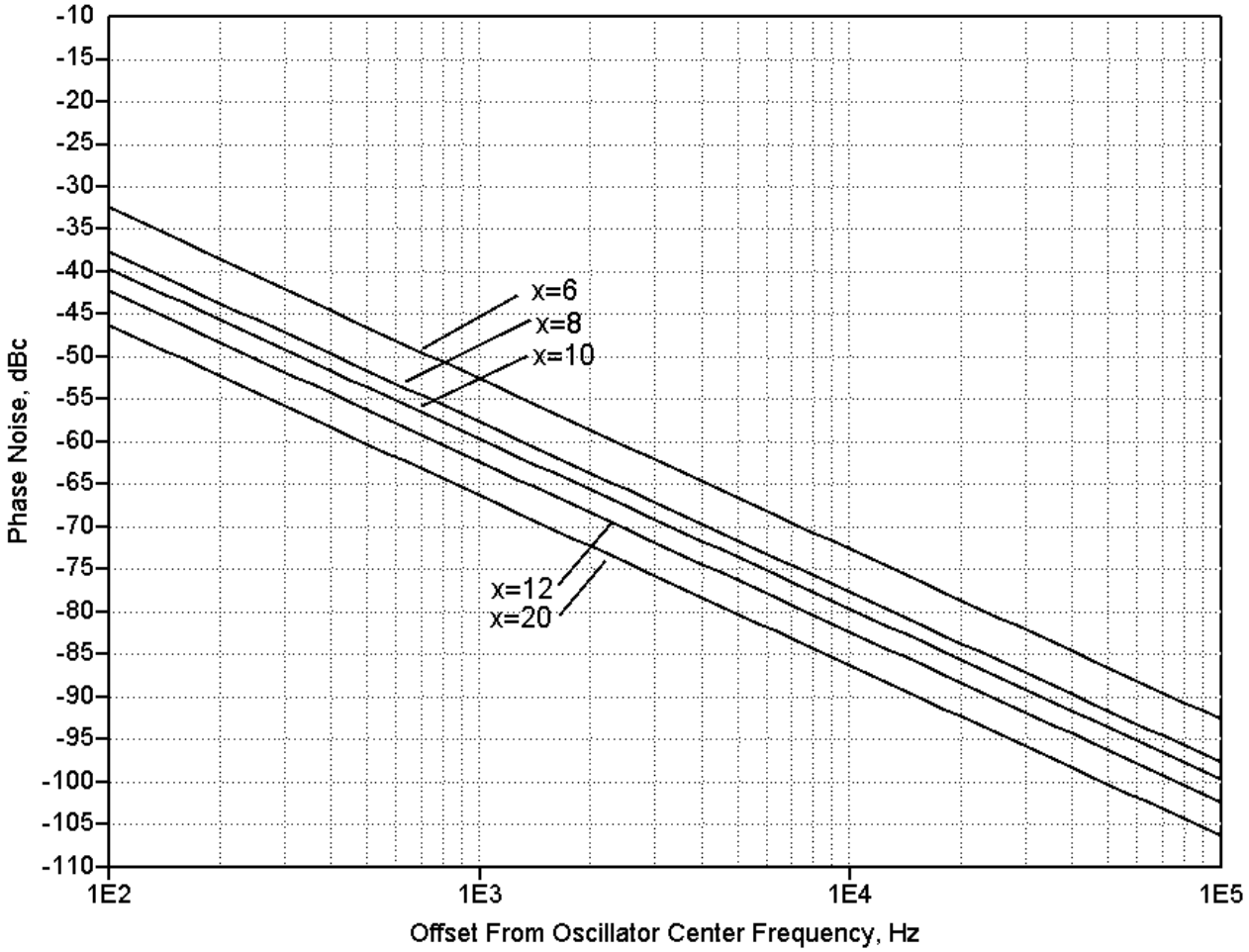

Figure 3.14. Phase noise comparison of 5mW four-resistor bias oscillators.

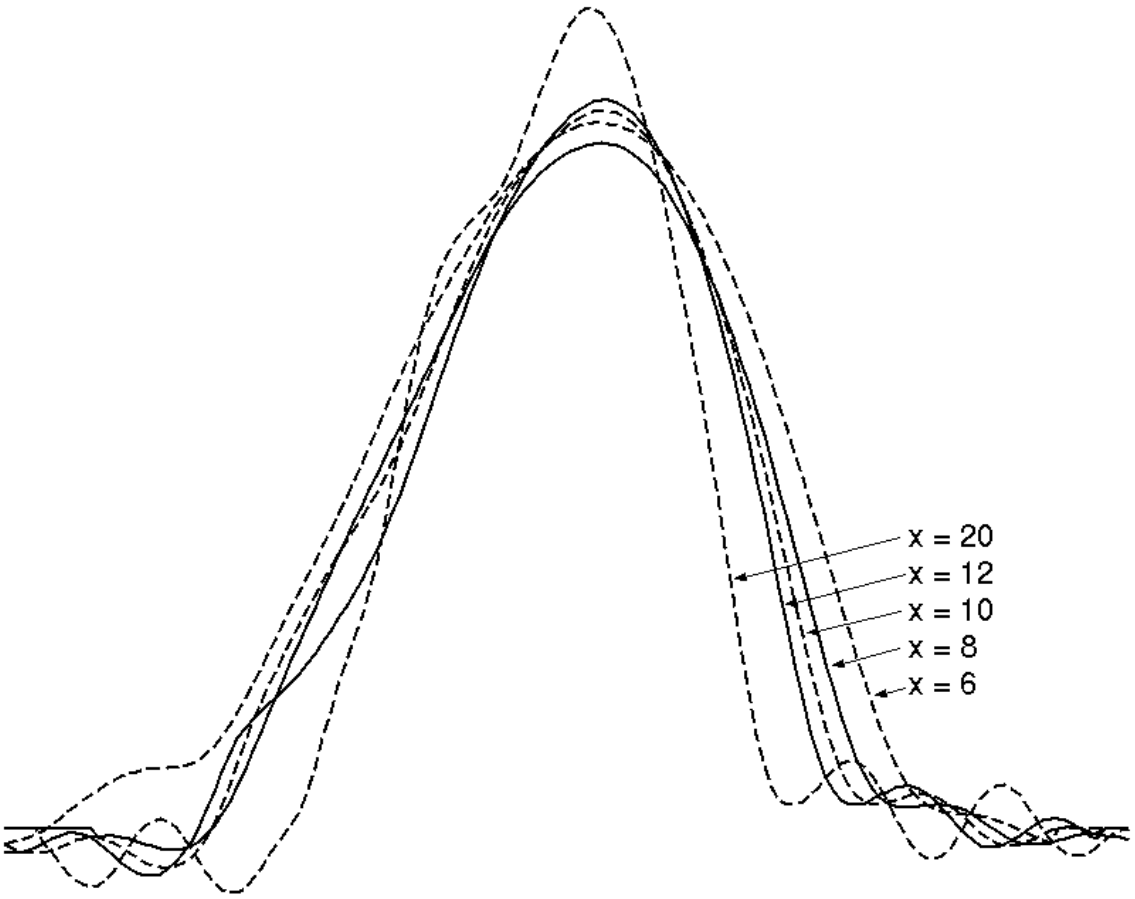

Figure 3.15. Collector current pulse-width comparison of 5mW four-resistor bias oscillators.

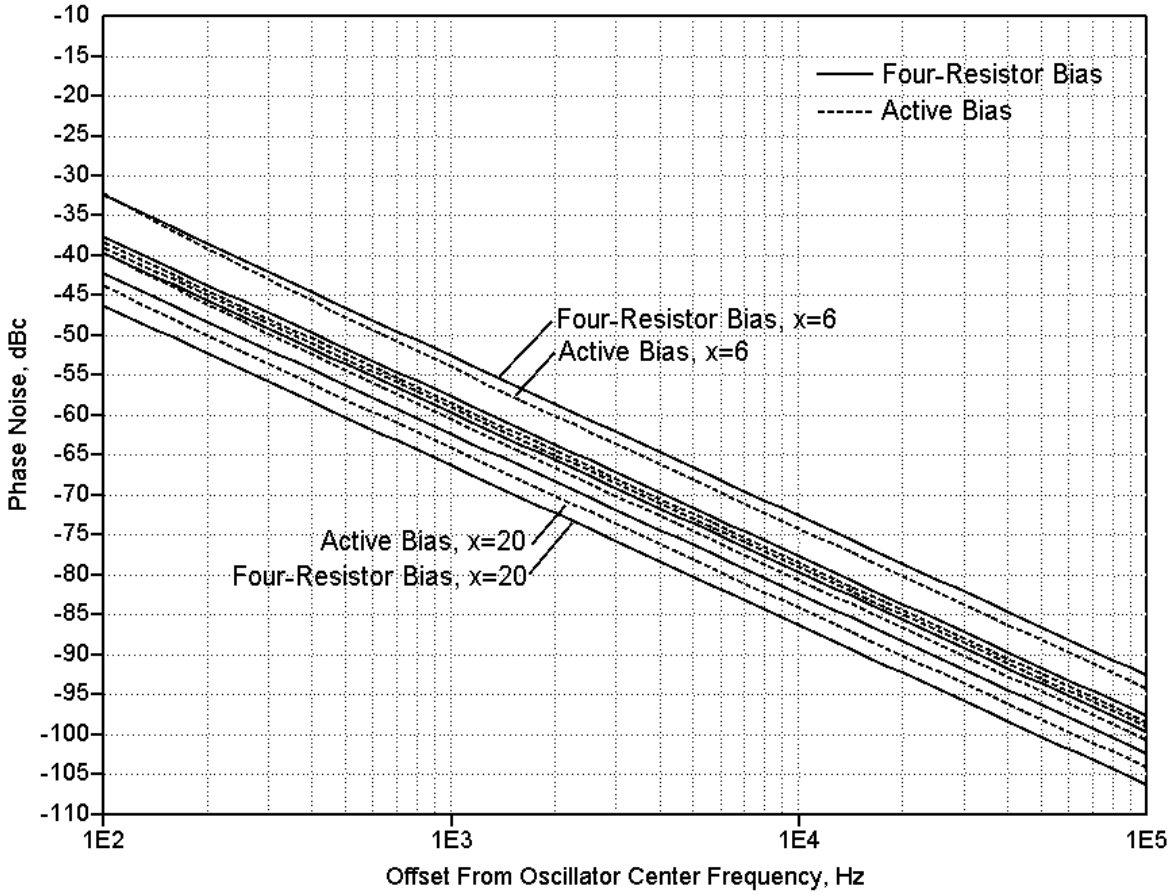

Figure 3.16. Phase noise comparison of all 5mW active and four-resistor bias oscillators

Chapter 4

Conclusions and Recommendations for Future Work

A relationship between drive level, current pulse width and phase noise output clearly exists for the simulated oscillators. The results support Lee and Hajimiri's theory (1998, 2000) which states that narrowing the current pulse width will decrease phase noise output. The results also support the shot noise equation by the observed fact that the lower average current corresponds to lower noise. The higher the DC current in the device, the higher the shot noise. From Section 2.3.2 it is known that shot noise contributes to the noise mixed into the sidebands of the oscillator signal. Therefore the designer should strive to keep the DC current as low as possible, to within the limits of the thermal noise contributions.

It is still important to follow the general suggestions for phase noise reduction from Leeson's model, combining a high quality factor for the resonator circuit with an operation point chosen to avoid device saturation. It is interesting that the 700MHz oscillator has such a 'decent' phase noise performance, being that it operates in saturation. Perhaps the current pulse width is a much larger factor influencing the phase noise characteristics than saturation. In addition, since the current drawn by the base during saturation is not substantial, the loading effect on the quality factor may not be as critical a factor as the pulse width. Further studies are necessary to determine what circumstances cause the current pulse width to dominate other noise controls.

There are several areas for potential research. The biasing of a transistor for lowest noise figure is often considered a worthwhile goal for oscillators. All of the oscillators designed here were biased without regard to manufacturers' recommendations for lowest noise figure, but for output power requirements. Such bias variations should be considered for comparison of noise performance in oscillators. The effects of particular bias topologies should be investigated further.

The values of the circuit resistive loading due to biasing and other circuits effects may be important considerations. Rohde (1983) claims a 40dB device flicker noise improvement simply by adding a resistor in series with emitter terminal of between 10Ω and 30Ω. Further consideration should be given to the performance effects of such a resistor and the actual noise contribution mechanism.

The effects of different capacitance ratios in the design have not been pursued in depth. Hajimiri (1998) indicates measurements of oscillators having different ratios show an optimal

capacitance ratio of four. However, it is unclear weather the pulse widths were kept the same for each the oscillators studied.

Effects of device materials and technological advances have allowed device noise characteristics of SiGe to become competitive with existing Si and GaAs (Niu, 1999; Vempati, 1996). An investigation comparing oscillator phase noise performance from devices made of various materials would be useful.

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Vita

David Steinbach was born on March 20, 1978 in Toronto, Ontario. In 1984 his family moved to Bainbridge, New York. David earned his Bachelor of Science from Virginia Tech in December 1999 and began working as a graduate research assistant for CWT in January 2000. He has completed several internships with the Motorola and Amphenol Corporations. His main interests within electrical engineering include discrete analog RF circuit design, AC induction motors, and alternate, renewable energy sources.