Four-Output Isolated Power Supply for the Application of IGBT Gate Drive

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Abstract

This thesis focuses on the design issues of the multiple-output boost full-bridge converter, which is constructed by cascading the boost regulator with the inductor-less full-bridge converter. The design of the boost regulator has been proposed briefly with component selection and compensator design. After that, the inductor-less full-bridge converter is analyzed extensively. In the first place, the operation principle of the inductor-less full-bridge converter is introduced. Later, the effect of parasitic resistance and inductance is analyzed in an L-R series circuit model as step-response, which relates the drop of output voltage to the load current. Then, the effects of the dc blocking capacitor for the unbalanced load condition and unbalanced duty cycle are tackled. The theoretical results are compared with the experimental results and the simulation results to verify the relationship between the output voltage drop and load current. The overall efficiency of the converter is tested under various conditions.

The design of the planar transformer is critical to limit the profile of the converter and the leakage phenomenon. A planar transformer fit for the inductor-less full-bridge converter is designed and analyzed in 3D FEA software. An N-port transformer model is proposed to implement the inductance matrix into the leakage inductance matrix for circuit analysis. Based on this N-port model several measurements to extract the parameters in this model are proposed, where only impedance analyzer is needed. Finally, the effects of trace layout and encapsulation on breakdown voltage in PCB are summarized from experimental results.

To my parents

You raise me up to more than I can be.

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Chapter 1 Introduction

1.1 Thesis background

Three-phase bridge power modules are widely used in electric/hybrid vehicle, uninterrupted power supply (UPS) for telecommunication systems, and other electric systems [1-4], as in Figure 1.1. The emerging market of electric/hybrid vehicle desires for more integrated and higher power density power solution of motor drive system [1-2].

Figure 1.1 Applications of 3-Phase Bridge PM in EV and UPS

As illustrated in Figure 1.2, the driving system for a 3-phase Power Module (PM) is composed of a PWM controller, isolated power supplies, and a gate-drive circuit. The PWM controller senses the output feedback signal and controls the PM by sending a signal to control the operation of the gate-drive switches in the PWM manor. The isolated power supplies provide isolated voltage sources for the IGBT gate-drive circuit. During operation, the emitter voltages of the three high-side IGBTs are floating during operation, while the low-side IGBTs hold the same emitter voltage. Therefore, at least four isolated voltage sources are needed. The gate-drive circuit includes six totem-pole switches and over-current protection circuits.

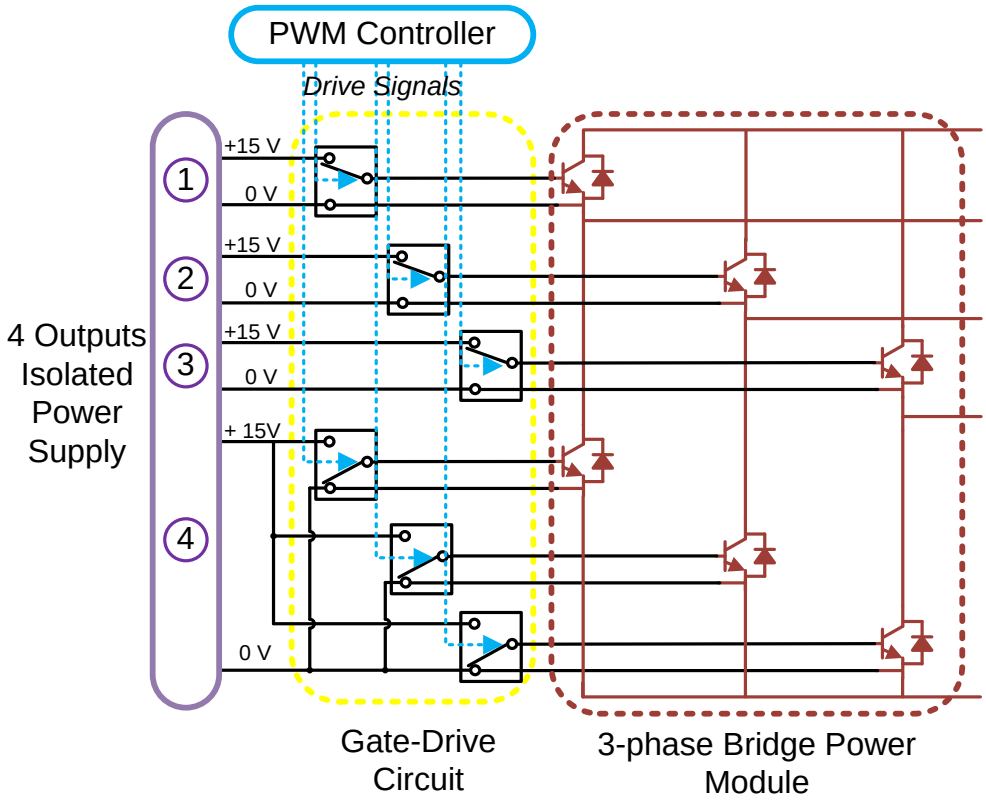

Figure 1.2 Diagram of driving system for 3-Phase bridge IGBT PM

On a typical gate-drive interface module, which is usually composed of isolated power supplies and a gate-drive circuit, most of the board area is occupied by four discrete power supplies for the gate-drive circuit. In one commercialized product, as in Figure 1-3, the four discrete power supplies takes 58% of the whole board area. In order to improve the power density of the whole power system, an integrated solution for these four isolated power supplies is necessary. In this thesis, a high power-density and low profile integrated converter is analyzed, designed and tested systematically. These four discrete isolated converters with a total size at 10 cm $\times$3.5 cm $\times$3 cm, are successfully integrated into one converter at 3.6 cm $\times$2.2 cm$\times$0.5 cm.

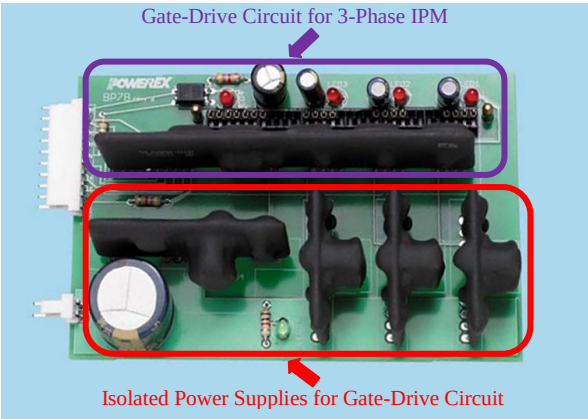

Figure 1.3 Gate drive interface module for 3-Phase PM (in reference to[7])

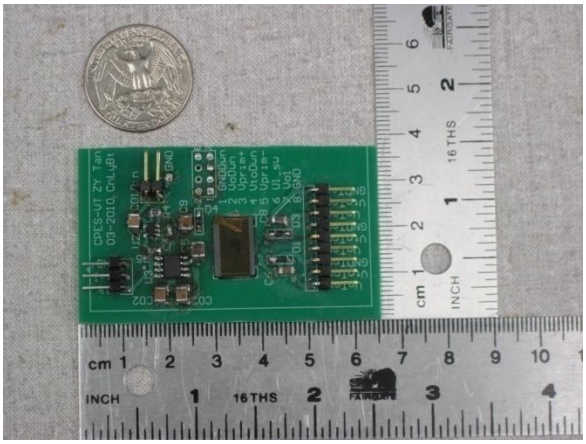

Figure 1.4 Four-output power supply for IGBT gate-drive application

1.2 Multi-output isolated DC-DC converter

Flyback topology is generally employed in a multi-output isolated DC-DC converter, and has been analyzed extensively in [5-6]. However, several drawbacks of the flyback converter limit its performance in the application of the IGBT gate-drive power supply.

1. Large core size compared to other topology.

In the flyback converter, the transformer has another role: converter inductor. Therefore, a more proper name should be coupled-inductor rather than transformer. During operation, the coupled

inductor needs to store energy. Therefore, a larger magnetic core with air gap is needed to prevent saturation. Otherwise, a larger core loss will be observed.

2. Large cross-regulation effect.

Because of the cross-regulation effect, the uncontrolled output voltage will be shifted by all variations in output loads as reported in [5]. Even an average voltage or weighted voltage control scheme on each output will not reduce this error, but redistribute them into each output. It should be mentioned that the asymmetry between the high-side output and the low-side output, as in Figure 1.2, makes this situation even worse.

3. High output voltage at no-load condition.

The flyback converter suffers from a high output voltage at no load or very light load condition. As is shown in the Appendix, at no-load condition, there is a chance this output voltage will rise up to more than 20 V, which will destroy the driving IGBT device.

4. Infeasibility of output extension.

If another non-isolated output is needed, e.g., one 15V output to power the PWM controller, the coupled-inductor needs to be redesigned to add another winding.

5. Isolation feedback needed.

The output is isolated from the input stage and, therefore, makes the feedback circuit complicated and increases the footprint of the converter.

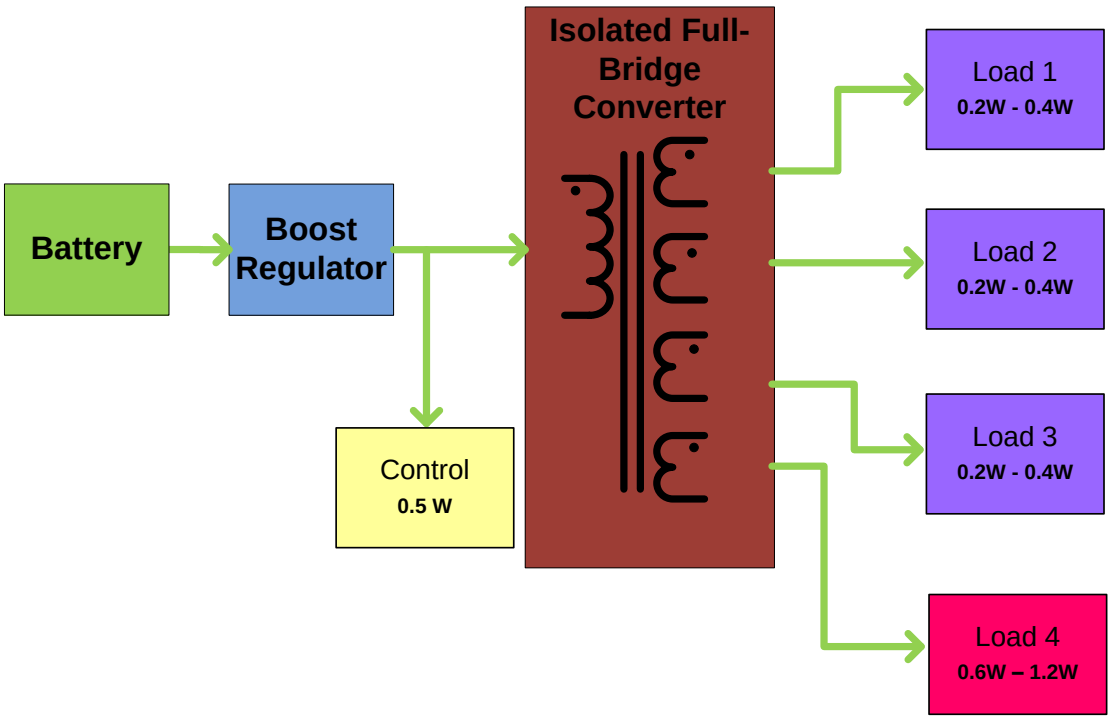

Figure 1.5 Schematic diagram for boost full-bridge cascaded converter

This thesis focuses on a two-stage converter system to provide multiple outputs for the IGBT driver. The schematic diagram is illustrated in Figure 1.5. The first-stage boost regulator will lift the input voltage into non-isolated however regulated output, then an unregulated full-bridge converter, works under 50% duty cycle to pass the regulated output through the voltage barriers as isolated outputs. Compared to the flyback converter, the merit of the topology proposed in this thesis is that it solves these five problems.

1.3. Thesis organization

Chapter 2 discusses the design issues of the boost full-bridge converter. The design of the boost regulator and the inductor-less full-bridge converter are proposed. An in-depth analysis of the inductor-less full-bridge converter is presented from the aspect of meeting the design specification of regulated outputs. The effects of parasitic resistance and inductance and dc

blocking capacitor are well presented and solved. A real converter is built and tested to verify the theory.

In chapter 3, the design of a planar transformer is discussed in three aspects. First, a 3D FEA software simulation is built based on a PCB winding layout. Second, an N-port transformer model is proposed to implement these simulation results into a circuit analysis. Based on this N-port model the test to extract the parameters in this model are proposed and compared with the simulation results. Third, the effects of the trace layout and encapsulation on the breakdown voltage in the PCB are discussed and tested.

Finally, chapter 4 summarizes the thesis, and proposes future works.

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Chapter 2 Boost Full-Bridge Converter Design

2.1 Design Specification

The specification of this design for a typical EV application is listed in Table 2.1. The schematic diagram is shown in Figure 1-5. There are 5 outputs in the system, three for a high-side IGBT gate driver, one for all low-side IGBT gate drivers, and one non-isolated output for the PWM controller. To leave enough margin, the power consumption of load 1 to 3 ranges from 0.15 W to 0.45 W; while for load 3 it ranges from 0.5 W to 1.5 W.

Table 2.1 Design Specification for Multi-output Converter

Battery Input Voltage	12 to 18 V
Isolated Output Voltage for Gate Driver	15 V ±3%
Non-isolated Controller Voltage	15 V ±2%
Power Consumption of Gate Driver for High-side IGBTs	0.2 to 0.4 W
Power Consumption of Gate Driver for Low-side IGBTs	0.6 to 1.2 W
Power Consumption of Controller	0.5 W
Isolation Voltage	6 kV
Height	5 mm
Volume	2 cm^3

2.2 Boost Full-Bridge Topology

The boost full-bridge converter has been analyzed extensively in [1-3]. Most of them focused on the issue of soft switching in high-power application. However, none of them attempted to revise this topology for low-power application with minimum components. In, this thesis, a simplified

boost full-bridge converter is proposed as in Figure 2.1. The merit of this topology is to use the minimum components needed for low-power application. The boost topology is employed to boost the input voltage into a regulated output voltage, i.e., V_L. The inductor-less H-bridge inverter has been proposed in [4] for application in EV motor drive, however not for low-power converter application. In Figure 2.1, the second stage is one inductor-less full-bridge converter working with fixed duty cycle. Compared to traditional full-bridge converter, only one output winding and one barrier diode are employed for each output to shrink its size. During normal operation, when switches S1 and S4 are on, the full-bridge charges three high-side IGBT output capacitor, i.e., C1, C2, and C3, while D4 blocks the negative voltage from the forth winding, C4 discharges by low-side IGBT gate drive loads.

Because the battery input voltage is ranging from 12 V to 18 V, the nature of the boost converter requires a higher output voltage. In this design, this output voltage (V_L) is fixed at 19.8 V. The turn number of the transformer is designed as 5:4, which transforms this line voltage into 15V outputs through the output barriers. The switching frequencies of these two stages are designed as 1 MHz and 600 kHz separately.

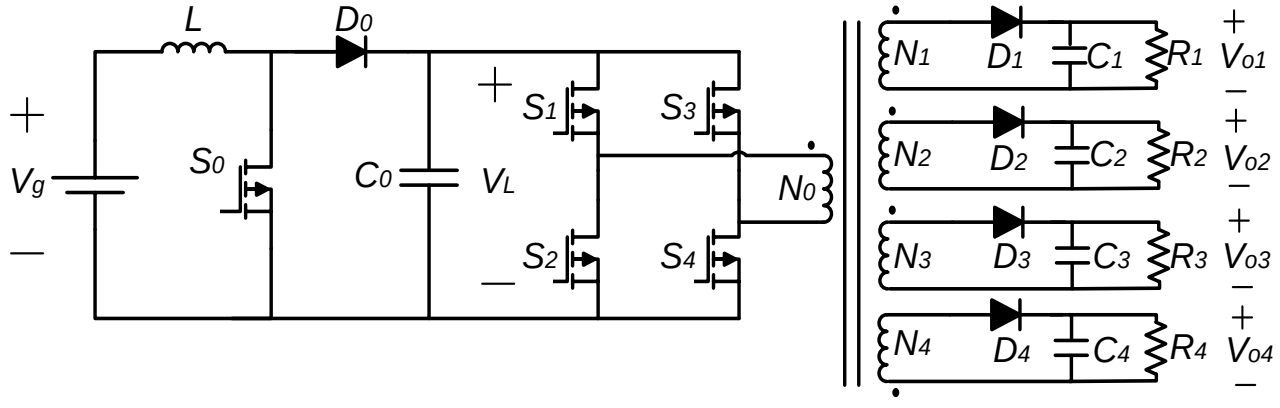


Figure 2.1 Topology of boost full-bridge converter

2.3 Boost Converter Design

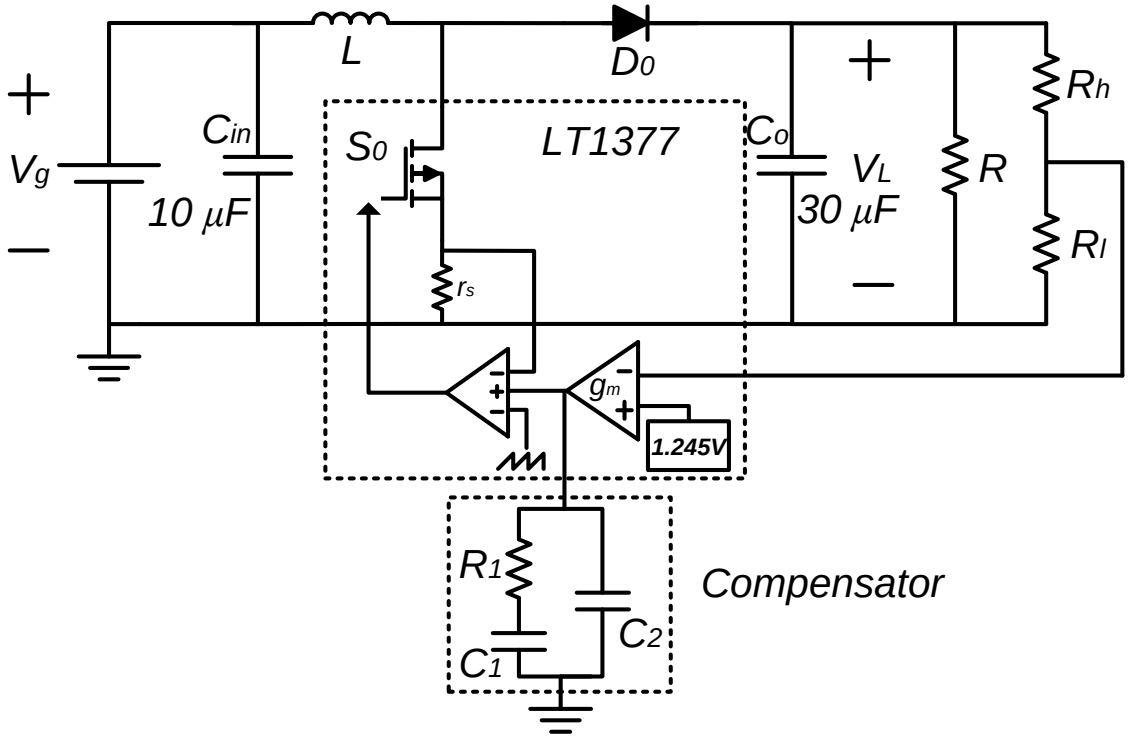


Figure 2.2 Schematic diagram of boost converter using LT1377 switch/controller

The schematic diagram of a boost converter using LT1377 is shown in Figure 2.2. The controller integrated inside this IC employs the peak current mode control (PCC) scheme, which is analyzed widely in [5-9]. Following the application note [11], the components are selected as in Table 2.3, and the compensator is designed as in Table 2.2. The power dissipation on load R is ranging from 1.5 W to 3 W.

Table 2.2 Parameters for compensator and feedback voltage divider

Designator	Rh	Rl	R1	C1	C2
Value	100 kΩ	6.71 kΩ	2 kΩ	390 pF	100 nF

Table 2.3 Bill of material for boost converter

Designator	Description	Part No. (Vendor)
S_0	1 MHz 1.5 A 35 V Switching Regulator	LT1377 (Linear)
L	4.7 μH 1A 185 mΩ Inductor	B82468 (Epcos)
D_0	40 V 400 mA Schottky Diode	ZHCS400 (Zetex)
C_o	3× 10 μF 50V Y5V Ceramic Cap	C3225Y5V1H106Z (TDK)
C_{in}	10 μF 50V Y5V Ceramic Cap	C3225Y5V1H106Z (TDK)

2.3.1 Simulation Results of Boost Converter

The schematic diagram of the boost converter designed in the previous section is implemented in Simplis model as Figure 2.3. The peak current mode control scheme and the voltage feedback loop are modeled under the data from [1].

The simulation results for the boost converter under 12 V input, at various loads are shown as in Figure 2.4. Because of the low power application, the boost stage works under discontinuous current mode. During this operation mode, the inductor current will reach zero before the start of each cycle. Whenever this current reached zero, the diode turned off and the switch voltage jumped from the output voltage to the input voltage, which caused a ringing between the inductor and the switch output capacitor as Figure 2.4. Due to the DCM operation, there will be no reverse recovery effect from the diode during the switch turning on instance, which usually causes a voltage spike on the switch potentially causing it to break down.

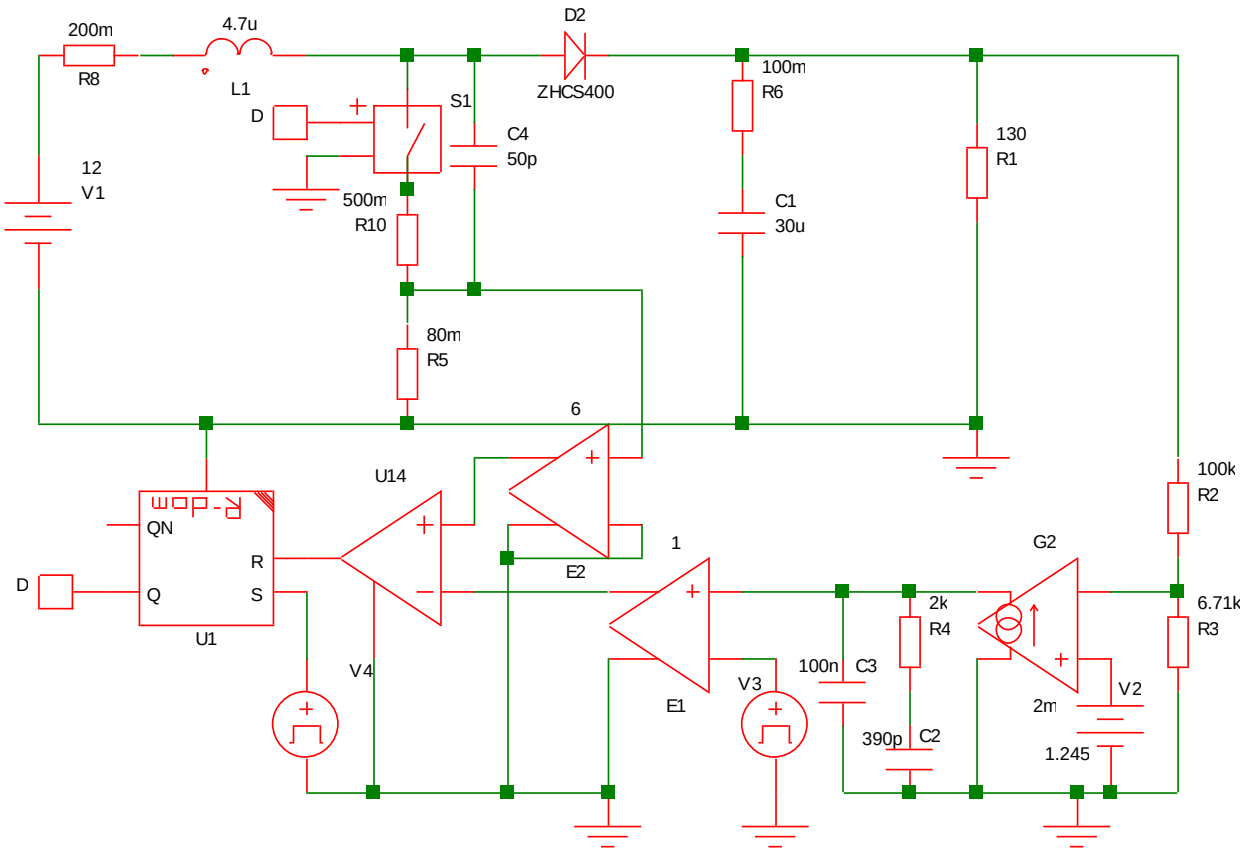


Figure 2.3 Simulation schematic diagram of boost converter under PCC in Simplis

The power loss on device is also analyzed under simulation. These results are listed in Table 2.4. The simulation results show the efficiency is 92% at light-load condition and 94% for heavy-load condition. The major power dissipations are on the switch and the diode. It should be noticed that the power loss for the control devices are not counted in this simulation and it will degrade the overall efficiency in a real system.

Table 2.4 Power loss and efficiency under different load conditions

	Light load (1 W)	Heavy load (3 W)
Loss on S0 (Rdson)	58.9 mW	84.1 mW
Loss on D0	18.6 mW	70.6 mW
Loss on L (ESR)	5.0 mW	26.0 mW
Loss on Co (ESR)	1.2 mW	5.1 mW
Total loss	87.0 mW	185.8 mW
Efficiency	92 %	94 %

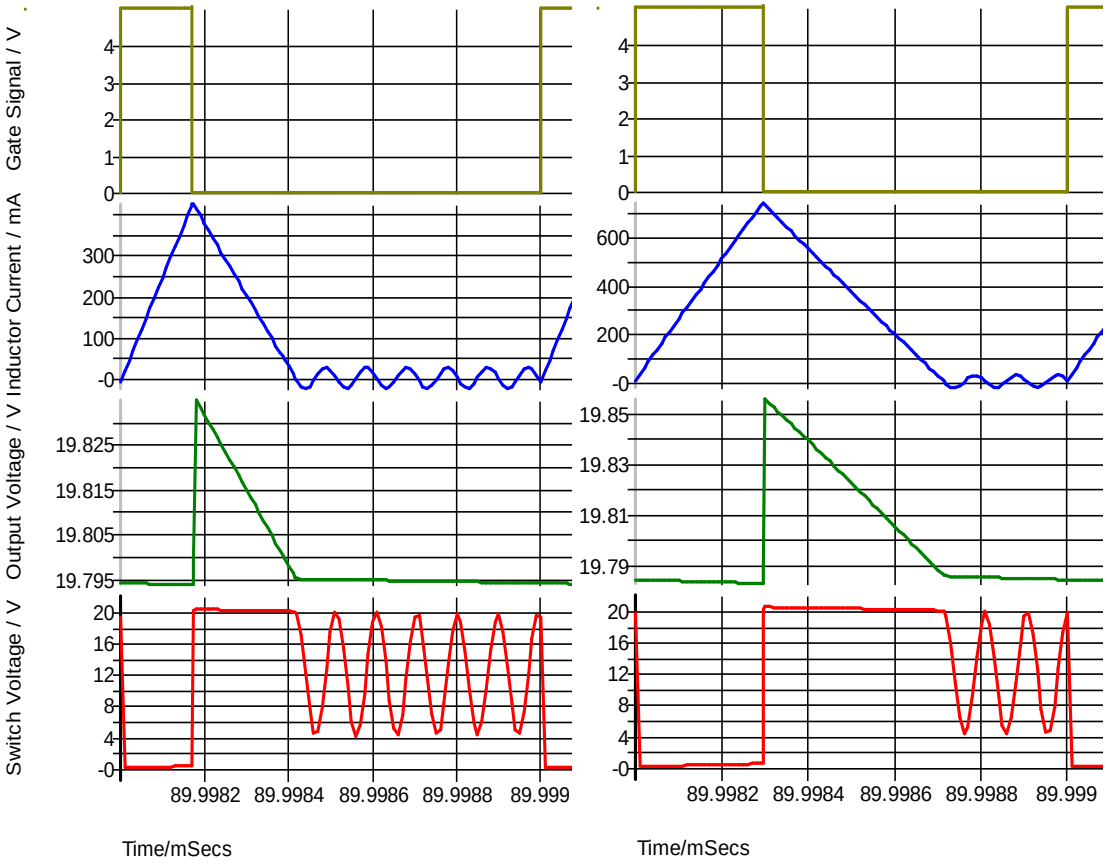


Figure 2.4 Simulation results of boost converter

(Left-side waveforms for 1W load, right-side waveforms for 2.85 W load)

2.4 Inductor-less Full-Bridge Converter

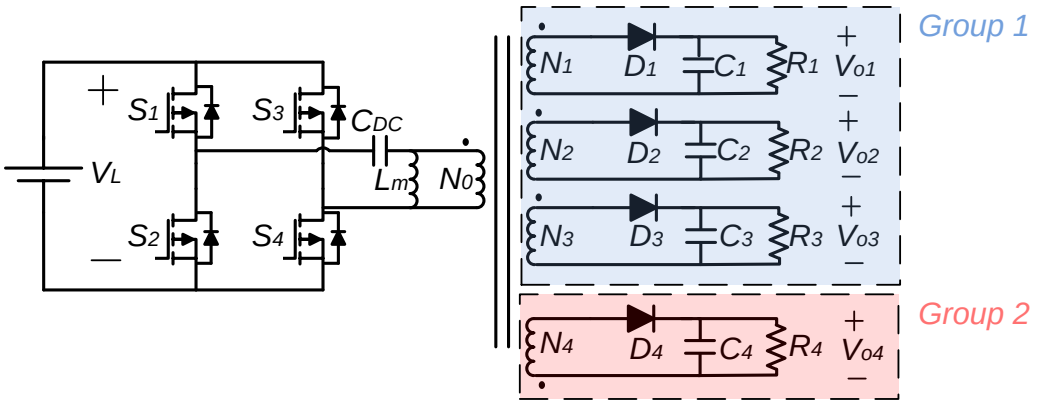


Figure 2.5 Schematic diagram of inductor-less full-bridge converter

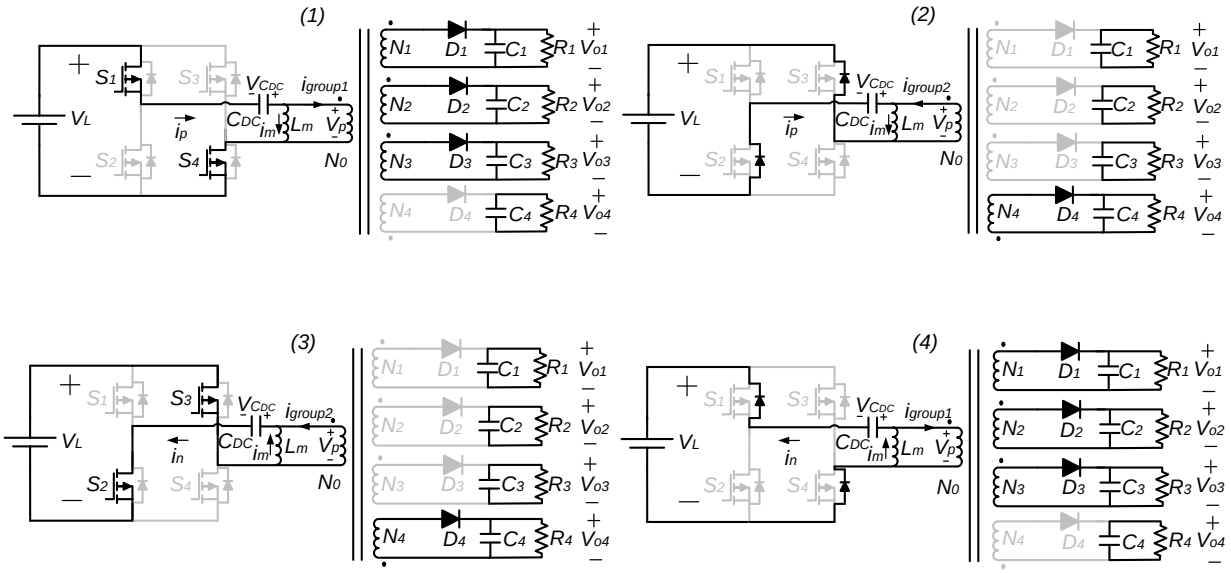


Figure 2.6 Operation Principle of inductor-less full-bridge converter during 4 intervals

The schematic diagram of the inductor-less full-bridge converter is proposed in Figure 2.5. Since a regulated line voltage is supplied from the first-stage boost converter, the second stage is designed as an open-loop converter, with a fixed 50% duty cycle. This structure eliminates the circuit to feedback the isolated output voltage; while provides four isolated regulated output to

power IGBT gate driver. The detailed operation principle is illustrated in Figure 2.6. The voltage on the capacitor C_{DC} could be considered as constant over the whole period, since its function is to block the DC voltage across the transformer to prevent DC saturation of the transformer.

During interval 1, S1 and S4 are on, and S2 and S4 are off. The primary side voltage of the transformer is positive. So the voltage on winding N1, N2, and N3 is positive; and diode D1, D2, and D3 are forwarding the winding voltages to charge output capacitors. At the same time, the diode D4 is off to block the negative voltage on winding N4. The load R4 is powered by discharging C4.

After S1 and S4 turn off and before S2 and S4 turn on, the converter operates in interval 2. During this dead-time interval, the current in the magnetic inductor of the transformer will force the body diodes of S2 and S3 to turn on. Therefore, the transformer primary voltage is flipped into a negative voltage. The diodes D1, D2, and D3 will block the flipped negative voltage from winding N1, N2, and N3; while diode D4 forwards the positive voltage of winding N4 to its output capacitor.

After the body diodes of S2 and S3 are forced to turn on in interval 2, the voltage across switch S2 and S3 drops to the diode forward voltage. Therefore, S2 and S3 could turn on in a Zero Voltage Switching manor, which could save the system from a high switching loss. After the S2 and S3 is turned on, the converter reaches interval 3. The output status is the same as interval 2.

Similar to interval 2, after switches S2 and S3 turn off, the body diodes of S1 and S4 are forced to turn on; and the statuses of the output windings are flipped by the inverted transformer primary voltage. This dead-time interval also enables the switching operation of S1 and S4 in interval 1 in ZVS.

Under ideal conditions, i.e., no transformer leakage inductance, no winding resistance, and no switch on-state resistance, the output voltages are defined as,

$$V_{o(i)} = \frac{N_i}{N_0} V_L - V_f \qquad (2\text{-}1)$$

From equation (2-1), it is noticeable that the output voltage will be regulated, since the turn ratio and input voltage are fixed, while the change on the diode forward voltage is negligible. However, these parasitics are impossible to avoid in a real system. Their effects on output voltage level will be analyzed in the following section.

2.4.1 Effect of Parasitic Resistance and Inductance on the Output Voltage Error

Under normal application, the load could be divided into two groups, loads 1 to 3 and load 4. As indicated in Figure 2.6, each group operates at 50% duty cycle, while the dead-time intervals, i.e., interval 2 and interval 3, is negligible. Therefore, they are decoupled from the effect of parasitic resistance and inductance.

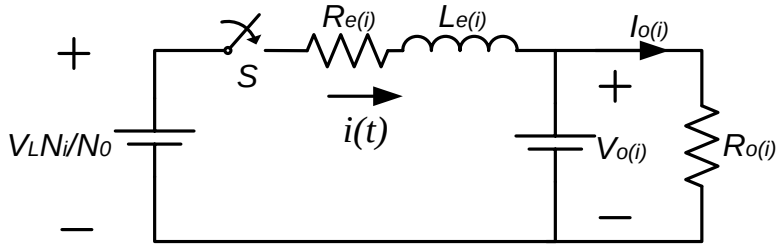


Figure 2.7 L-R series model to analyze the output voltage error from various loads

In the practical application, the power for load 1 to 3 is the same and the power for load 4 is three times of the power of other loads. Assuming the instant current on each branch from winding 1 to 3 is proportional to its output current, during interval 1 and 4, these three branches are

decoupled, and could be analyzed in the L-R series model as in Figure 2.7. It should be noticed that the resistance shared by these three loads should be tripled under identical load current.

The effects of parasitic parameters might initial a voltage error in this open-loop converter. This effect could be analyzed in an L-R series model under step change as in Figure 2.7 for each output branch. In this model, the primary side voltage has been pushed into the secondary side. The voltage on the dc blocking capacitor is assumed to be 0. The equivalent resistor *Re* is defined as the sum of switch on-state resistance, winding resistance, and diode forward resistance in reference at the secondary side as in equation (2-2) for group 1 and in equation (2-3) for group2. In these two equations, $R_{ds(on)\text{-}high}$ is the on-state resistance of high-side switch, as S1 and S3 in Figure 2.6; $R_{ds(on)\text{-}low}$ is the on-state resistance of low-side switch, as S2 and S4 in Figure 2.6; R_D represents the on-state resistance of output diode; $R_{TX(i)}$ characterizes the resistance of i-th winding in planar transformer. The equivalent inductor *Le* is determined by the winding leakage inductance of the transformer as in equations (2-4) and (2-5), where the mutual leakage inductance ℓ_{ij} is defined in future section 3.3.1.

$$R_{e(i)} = \frac{N_1 I_{o1} + N_2 I_{o2} + N_3 I_{o3}}{N_i I_{o(i)}} \frac{N_i^2}{N_0^2} \times (R_{ds(on)-high} + R_{ds(on)-low} + R_{TX\,0}) + R_{TX\,(i)} + R_D \quad (i \in group1) \tag{2-2}$$

$$R_{e4} = \frac{N_4^2}{N_0^2}(R_{ds(on)-high} + R_{ds(on)-low} + R_{TX\,0}) + R_{TX\,4} + R_D \tag{2-3}$$

$$L_{e(i)} = \frac{N_1 I_{o1} \ell_{1i} + N_2 I_{o2} \ell_{2i} + N_3 I_{o3} \ell_{3i}}{N_i I_{o(i)}} \quad (i \in group1) \tag{2-4}$$

$$L_{e4} = \ell_{44} \tag{2-5}$$

The output capacitor has been replaced by a constant voltage source to simplify the analysis. During normal operation, switch S turns on for 50% duty cycle to charge the output capacitor and shut down for the other 50% of the duty cycle to charge the other windings. As the step-response in L-R series model, the circuit current will increase exponentially to the steady state value as in equation (2-6), where the time constant and drop voltage is defined in equation (2-7.) Under steady state, the output current is equal to the average value of current $i(t)$, as in equation (2-8), since the net charge is balanced on the output capacitor.

$$i(t) = \frac{V_{d(i)}}{R_{e(i)}}(1 - e^{-t/\tau(i)}) \tag{2-6}$$

In which,

$$\tau(i) = \frac{L_{e(i)}}{R_{e(i)}}, V_{d(i)} = V_L \frac{N_i}{N_0} - V_{o(i)} \tag{2-7}$$

Under steady state, the net charge in output capacitor is zero, which validates equation (2-8)

$$\frac{\int_0^{T/2} i(t)dt}{T} = \frac{V_{o(i)}}{R_{o(i)}} = I_{o(i)} \tag{2-8}$$

$$V_{d(i)} = I_{o(i)} R_{e(i)} \frac{1}{\frac{1}{2} + \frac{\tau(i)}{T}(e^{-T/2\tau(i)} - 1)} \tag{2-9}$$

Under conditions the time constant τ is much smaller than the half switch period. The equation (2-9) could be simplified into the following equation (2-10)

$$V_{d(i)} = I_{o(i)} R_{e(i)} \frac{1}{\frac{1}{2} - \frac{\tau(i)}{T}} \qquad (\tau(i) \ll T) \qquad (2\text{-}10)$$

The equation (2-9) shows the relationship between the load current and the voltage drop on the winding from the L-R series model. Considering that the input voltage is regulated, the variation of this voltage drop from different load conditions will cause an voltage error to output. Figure 2.8 shows the the output voltage error vs *Le* and *Re* between light load condition and full load condition.

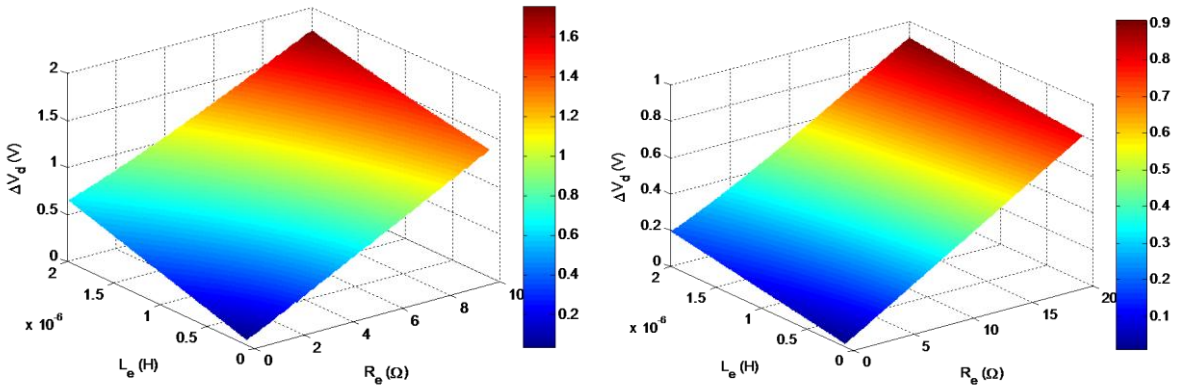


Figure 2.8 Voltage error vs Le and Re between full-load and light-load conditions

(Left-side plot is for winding 4, and right-side plot is for winding 1 to 3. *f* =600 kHz)

The Figure 2.8 shows that the output voltage error on winding 4 will be much more severe than the other windings under same leakage inductance condition. This is because the load variation is much larger on winding 4. To keep the voltage error within specification, the leakage inductance should be no more than 1 μH and equivalent resistance should be no more than 6 Ω; while leakage inductance should be less than 2 μH and equivalent resistance should be less than 15 Ω for winding 1to 3. In practical design, the leakage inductance for winding 4 and equivalent resistance for winding 1 to 3 are the most critical design issues.

Table 2.5 Predicted voltage error for each output

(ΔI_{o1}= ΔI_{o2}=ΔI_{o3}=0.02 A, ΔI_{o4}=0.067 A)

	N1	N2	N3	N4
Re (Ω)	9.4	9.4	9.4	3.7
Le (nH)	349	244	251	125
ΔVo (V)	0.72	0.62	0.63	0.58
ΔVo/Vo	4.8%	4.1%	4.1%	3.9%

Based on simulation results of leakage inductance in section 3.3.1, the effective resistance and inductance are calculated and listed in Table 2.5. Assuming the current in each group is the same, the voltage errors are predicted from equation (2-10) in Table 2.5 over the entire operational range.

2.4.2 Effect of DC Blocking Capacitor on Output Voltage Error

In section 2.3.1 the effect of parasitic resistance and inductance on output voltage error are analyzed in details. Within that model, the high-side loads and low side load are isolated by the operation principle. However, in reality, these two groups are still coupled through the dc blocking capacitor, i.e., C_{DC} in Figure 2.6, in two aspects as shown in Figures 2.9 and 2.10.

As illustrated in Figure 2.9, the unbalanced loads between group 1 and group 2 will cause a DC voltage drop across the DC capacitor, which will cause the peak values of the primary side voltage to be different in two groups. The result of this DC voltage is that the output voltages in group 1 will increase by $V_{C_{DC}} \frac{N_i}{N_0}$, while the output voltage in group 2 will decrease by the same amount. The primary-side resistance, i.e., *Rp*, is the sum of switch on-state resistance and primary-side winding resistance as in equations (2-11).

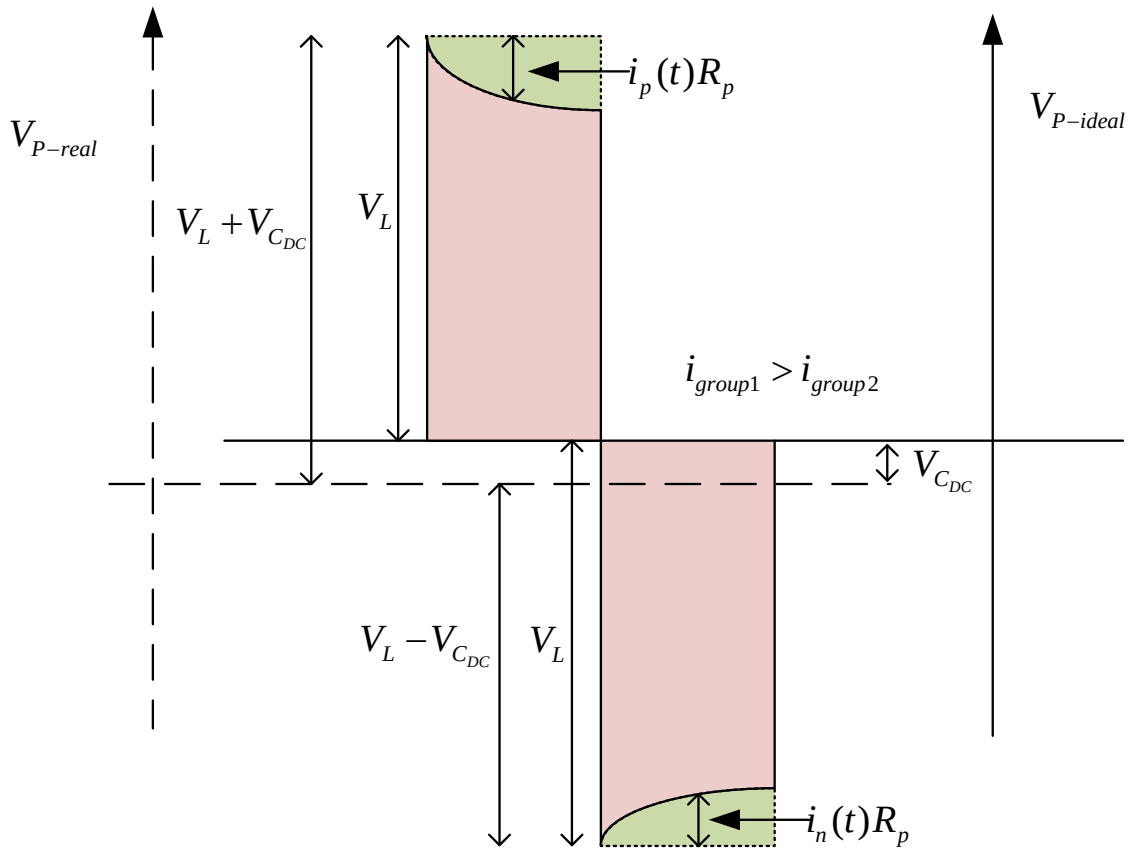


Figure 2.9 Output voltage shifting caused by unbalanced loads between group 1 and group 2

In reference to Figure 2.6, equations (2-12) and (2-13) describe that the input currents of transformer under positive and negative voltage are composed with two parts: magnetizing current, i.e., im, and primary-side current of ideal transformer, i.e., $igroup1$or $igroup2$.

$$R_p = R_{ds(on)-high} + R_{ds(on)-low} + R_{TX0} \qquad (2\text{-}11)$$

$$i_p = i_m + i_{group1} \qquad (2\text{-}12)$$

$$i_n = i_m + i_{group2} \qquad (2\text{-}13)$$

The average value of primary-side current during each interval equates to the output currents powered during that interval, as in equations (2-14) and (2-15).

$$\int_0^{T/2} \frac{i_{group1}(t)}{T} dt = \frac{N_1}{N_0} I_{o1} + \frac{N_2}{N_0} I_{o2} + \frac{N_3}{N_0} I_{o3} \quad (2\text{-}14)$$

$$\int_{T/2}^{T} \frac{i_{group2}(t)}{T} dt = \frac{N_4}{N_0} I_{o4} \quad (2\text{-}15)$$

Since the dc blocking capacitor filters out the dc bias on transformer, the magnetic current holds equations (2-16).

$$\int_0^{T/2} i_m(t) dt = \int_{T/2}^{T} i_m(t) dt \quad (2\text{-}16)$$

In reference to Figure 2.9, the voltage across dc blocking capacitor is defined as equation (2-17).

$$V_{C_{DC}} = \frac{\int_0^{T/2} i_p(t) R_p dt - \int_{T/2}^{T} i_n(t) R_p dt}{T} \quad (2\text{-}17)$$

Based on equations (2-12)-(2-17), the voltage across dc blocking capacitor is solved as in equation (2-18).

$$V_{C_{DC}} = \frac{1}{N_0^2} (N_1^2 I_{o1} + N_2^2 I_{o2} + N_3^2 I_{o3} - N_4^2 I_{o4}) R_e \quad (2\text{-}18)$$

From the equation (2-18), the change of output voltage caused by this effects is described in equations (2-19) and (2-20) for group 1 and group 2 separately.

$$\Delta V_{o4}^1 = -\frac{1}{N_0^2} (N_1^2 I_{o1} + N_2^2 I_{o2} + N_3^2 I_{o3} - N_4^2 I_{o4}) R_p \quad (2\text{-}20)$$

$$\Delta V_{o(i)}^{1} = \frac{1}{N_0^2}(N_1^2 I_{o1} + N_2^2 I_{o2} + N_3^2 I_{o3} - N_4^2 I_{o4})R_p \quad (i \in group1) \tag{2-19}$$

As indicated in equations (2-19) and (2-20), this effect will lift up the output voltage in high load group by lowering down the output voltage in light load group. Intuitively, at high load condition, the output voltage is tempting to drop. Therefore, this effect helps the converter to alleviate from the voltage drop in unbalanced high-load condition. However, for balanced-load condition, this mechanism will have no effect on correcting the output voltage, since the dc blocking voltage will be zero as indicated in equation (2-18).

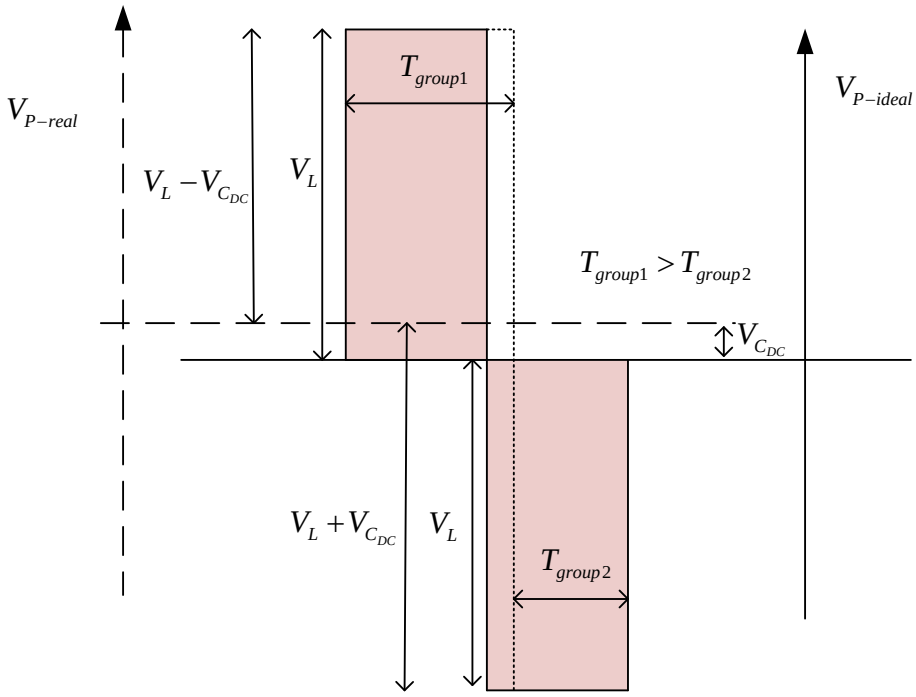


Figure 2.10 Output voltage shifting caused by unbalanced duty cycle

Besides unbalanced loads between two groups, unbalanced duty cycle will also introduce the voltage shifting effect between outputs, illustrated in Figure 2.10. This effect can be described in equations (2-22) and (2-23), where ΔD is defined as in equation (2.21).

$$\Delta D = \frac{T_{group1} - T_{group2}}{T_{group1} + T_{group2}} \tag{2-21}$$

$$\Delta V_{o(i)}^2 = -\frac{N_i}{N_0}\Delta D V_L \quad (i \in group1) \tag{2-22}$$

$$\Delta V_{o4}^2 = \frac{N_4}{N_0}\Delta D V_L \tag{2-23}$$

Finally, based on the analysis in section 2.4.1 and 2.4.2, the output voltage could be solved as in equation (2-24).

$$V_{oi} = V_L \frac{N_i}{N_0} - V_{d(i)} + \Delta V_{o(i)}^1 + \Delta V_{o(i)}^2 \tag{2-24}$$

After substitute equation (2-9), (2-19), (2-20), (2-22), and (2-23) into equation (2-24), the output voltages for group 1 and group 2 are presented in equation (2-25) and (2-26) separately.

$$\begin{aligned} V_{oi} = {} & V_L \frac{N_i}{N_0}(1-\Delta D) \\ & - \frac{I_{o(i)} R_{e(i)}}{\frac{1}{2} + \frac{\tau}{T}(e^{-T/2\tau(i)} - 1)} \quad (i \in group1) \\ & + \frac{1}{N_0^2}(N_1^2 I_{o1} + N_2^2 I_{o2} \\ & + N_3^2 I_{o3} - N_4^2 I_{o4}) R_p \end{aligned} \tag{2-25}$$

$$V_{O4} = V_L \frac{N_4}{N_0}(1+\Delta D) - \frac{I_{o4}R_{e(4)}}{\frac{1}{2}+\frac{\tau}{T}(e^{-T/2\tau_4}-1)} + \frac{1}{N_0^2}(N_4^2 I_{o4} - N_1^2 I_{o1} - N_2^2 I_{o2} - N_3^2 I_{o3})R_p \quad (2\text{-}26)$$

The last term in equation (2-25) and (2-26) indicates that there is cross-regulation effect among the outputs, which is caused by unbalanced loads as discussed before. The key to minimize this effect is to either balance the loads between two groups or reduce the primary-side resistance. From equations (2-25) and (2-26), the output error are calculated and listed in Table 2.6, where only one output load is changed at one time. As indicated from Table 2.6, whenever one output load decreases, all output voltage will increase. On the other way, whenever one output load increases, all output voltage will decrease. Therefore, when all output loads are at heaviest, all output voltages are highest; when all output loads are at lightest, all output voltages are lowest.

Table 2.6 Predicted cross-regulation effects for full-bridge converter

($I_{o1\text{-}normal} = I_{o2\text{-}normal} = I_{o3\text{-}normal}$=0.02 A, $I_{o4\text{-}normal}$ =0.067A)

I_o (A)	I_{o1}		I_{o2}		I_{o3}		I_{o4}	
ΔV_o (mV)	0.01	0.03	0.01	0.03	0.01	0.03	0.033	0.1
V_{o1}-$V_{o1\text{-}normal}$	44 mV	-44 mV	33 mV	-33 mV	31 mV	-31 mV	98 mV	-98 mV
V_{o2}-$V_{o2\text{-}normal}$	33 mV	-33 mV	42 mV	-42 mV	31 mV	-31 mV	98 mV	-98 mV
V_{o3}-$V_{o3\text{-}normal}$	31 mV	-31 mV	31 mV	-31 mV	44 mV	-44 mV	98 mV	-98 mV
V_{o4}-$V_{o4\text{-}normal}$	29 mV	-29 mV	29 mV	-29 mV	29mV	-29 mV	190 mV	-190 mV

2.4.3 Components for Inductor-less Full-bridge Converter

The block diagram of an inductor-less full-bridge converter is drawn in Figure 2.11. The structure of 555 timer plus IXDN404 is employed to perform the full-bridge switching. The IC IXDN404 is one double low-side driver for non-isolated driving applications as in Figure 2.12. However, its nature of two totem poles enables it to perform the 2-phase bridge switching action. This design saved the system by a large footprint from a traditional full-bridge converter, which usually requires a bootstrap driver to drive the high-side MOSFET, as S1 and S3 in Figure 2.11. A typical boot-strap chip with peripheral components will occupy a footprint on the PCB about 0.6 cm^2.

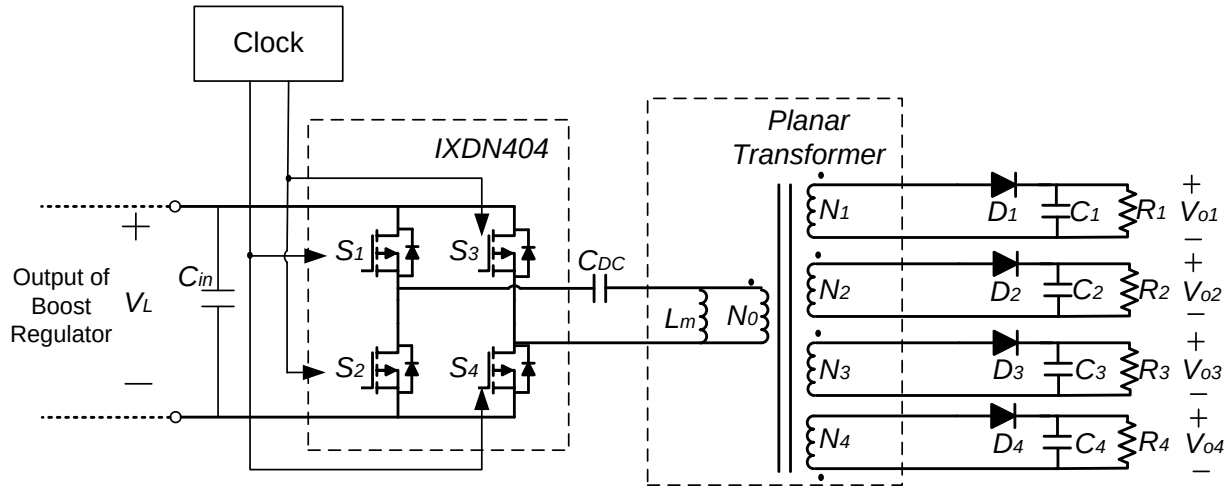


Figure 2.11 Schematic diagram of inductor-less full-bridge converter in function blocks

Inside the IXDN 404, it integrates a anti-cross conduction circuit, as in Figure 2.12. This circuit provides a dead time to full-bridge operation, i.e., interval 2 and 4 in Figure 2.6. This will improve the overall efficiency by reducing the switching loss. The detailed design on the planar transformer for this converter will be carefully discussed in Chapter 3.

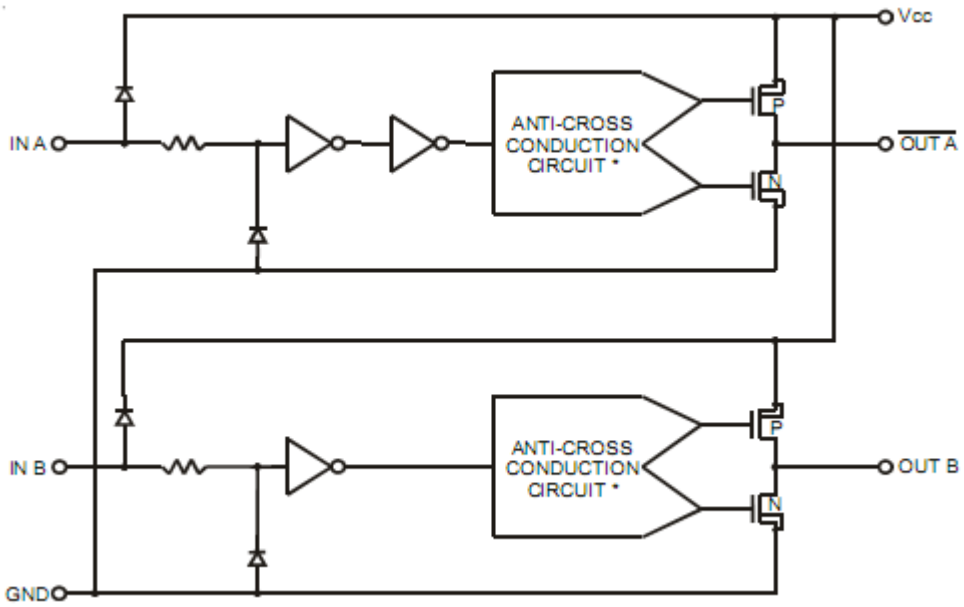


Figure 2.12 Functional Diagram of IXDN 404

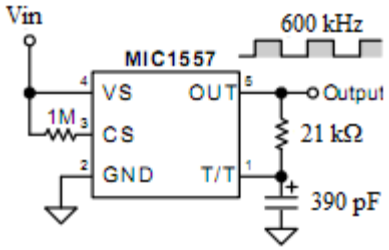


Figure 2.13 Configuration of MIC 1557 oscillator

Unfortunately, there is no internal clock inside IXDN404. An oscillator as proposed in Figure 2.13 is necessary to provide a 50% duty cycle signal at 600 kHz to drive the full-bridge switches. Another drawback of IXDN404 is its high on-state resistance as reported in [12]. Because of the difference between high-side and low-side MOSFET types, there are two on-state resistance curves to describe the resistance from various supply voltage and temperature in Figures 2.14 and 2.15. Assuming IXDN404 operates at 19.8 V supply voltage and 75 ℃, the $R_{ds(on)\text{-}high}$ for high-side P-MOS is 2.28 Ω, and $R_{ds(on)\text{-}low}$ for the low-side N-MOS is 1.82 Ω. Therefore, an effective resistance on the secondary side by only considering the switch resistance could be solved out as 2.62 Ω.

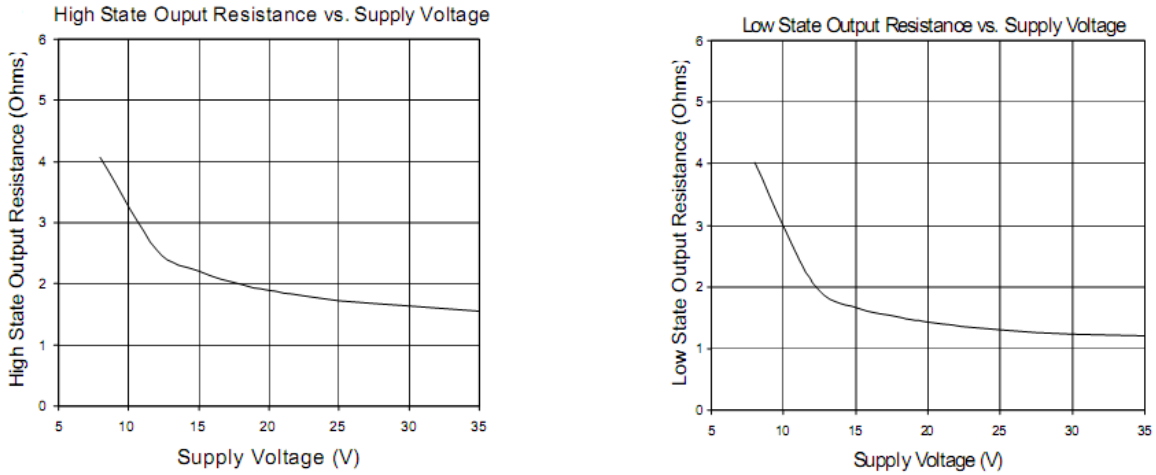


Figure 2.14 IXDN404 MOSFET R_{dson} vs Supply Voltage for different sides

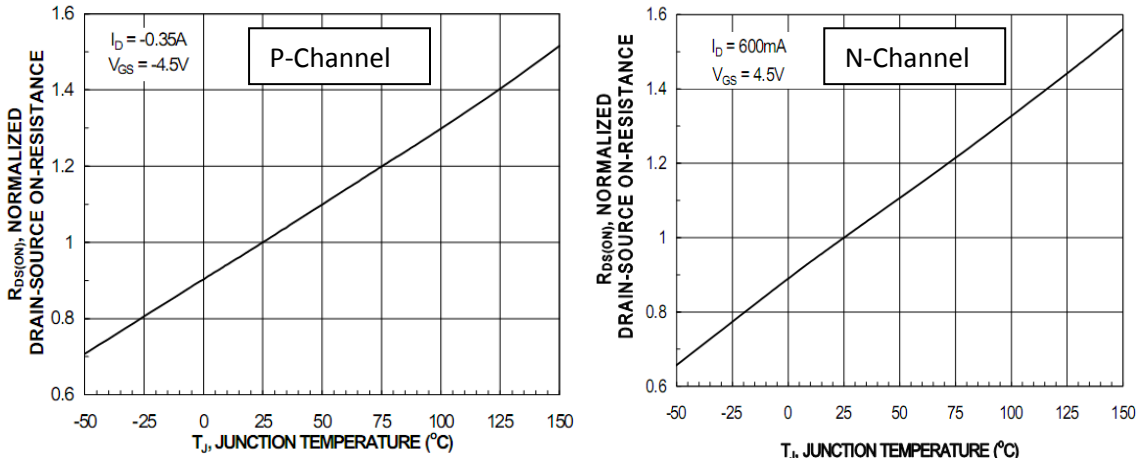


Figure 2.15 Typical MOSFET R_{dson} vs Supply Voltage for different channel types (from [13])

All components for this full-bridge converter are listed in the Table 2.7.

Table 2.7 Bill of material for full-bridge converter

Designator	Description	Part No. (Vendor)
S_1, S_2, S_3, S_4	Dual low side MOSFET driver, 4 A, V_{CCMAX} 35 V	IXDN 404 (IXYS)
D_1, D_2, D_3, D_4	60 V 500 mA Schottky Diode	STPS0560Z (ST)

C_1, C_2, C_3	3.3 μF 50V Y5R Ceramic cap	C3225X7R1H335M (TDK)
C_{DC}	100 μF 10V X5R Ceramic cap	LMK325BJ107MM-T (Taiyo Yuden)
C_4, C_{in}	10 μF 50V Y5V Ceramic cap	C3225Y5V1H106Z (TDK)
Clock	5 MHz, V_{CCMAX} 18 V, Timer	MIC1557 (Micrel)
R_T	21 kΩ, 0603, Timing resistor	ERJ-3EKF2102V (ECG)
C_T	390 pF, 50 V, Timing capacitor	C1608C0G1H391J (TDK)

2.4.4 Simulation of Inductor-less Full-Bridge Converter

The designed inductor-less full-bridge converter with parasitic parameters is implemented in simplis model as Figure 2.16, whose simulation conditions are listed in Table 2.8. The model of the planar transformer is followed by the proposed model in section 3.3.1. At the same time, the parameters of the planar transformer are values from the 3-D FEA simulation results in section 3.3.2.

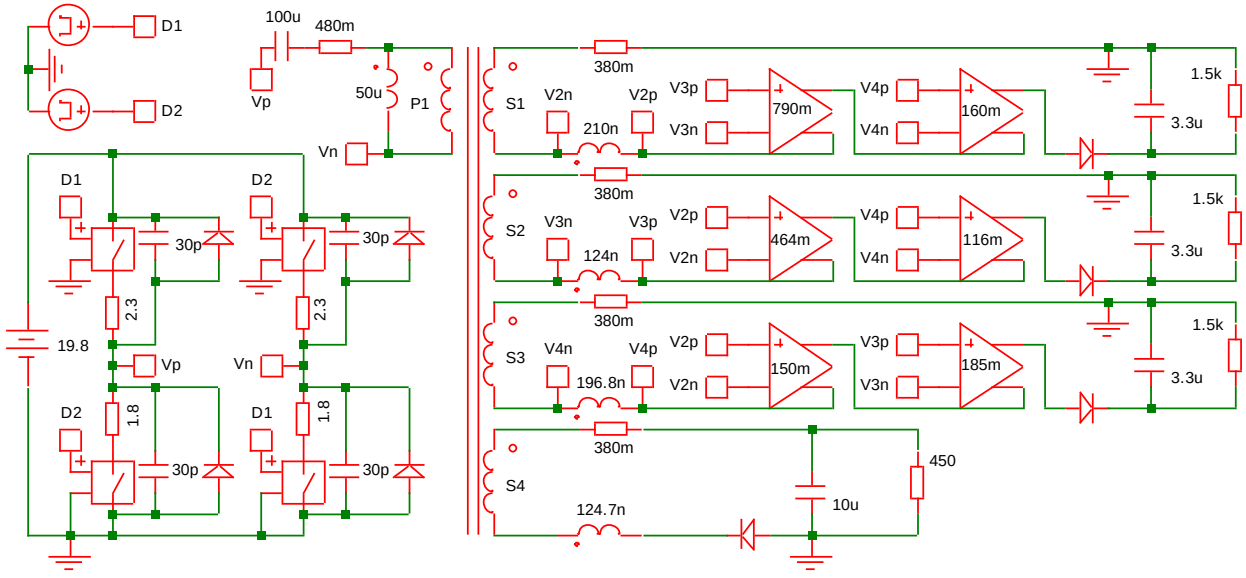
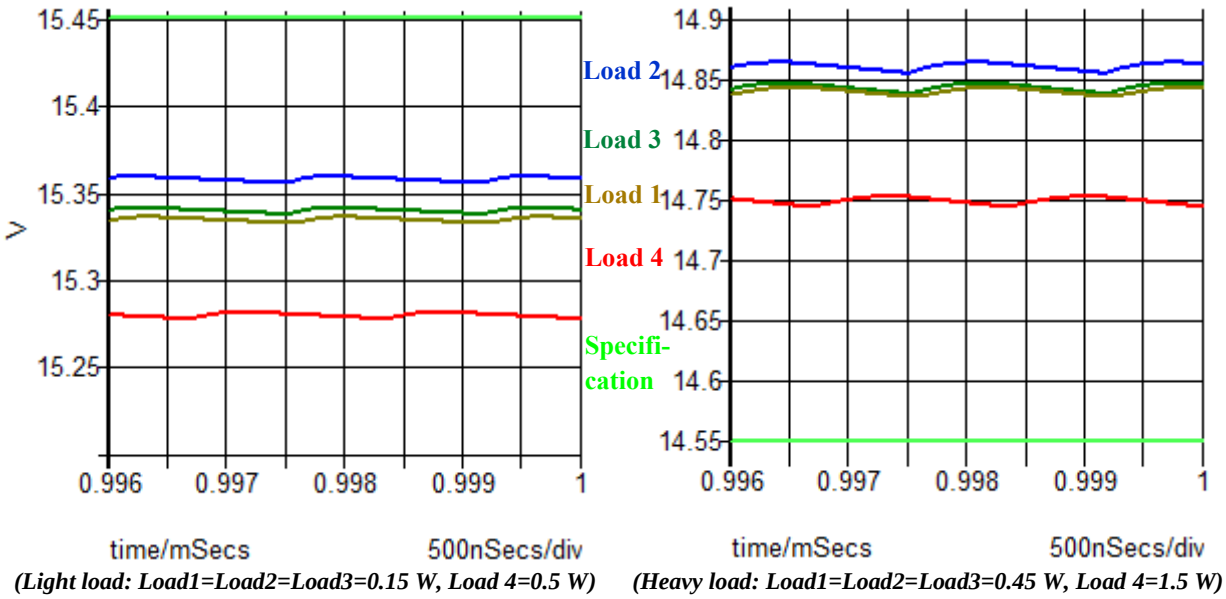


Figure 2.16 Simulation schematic diagram of full-bridge with cross-regulation in Simplis

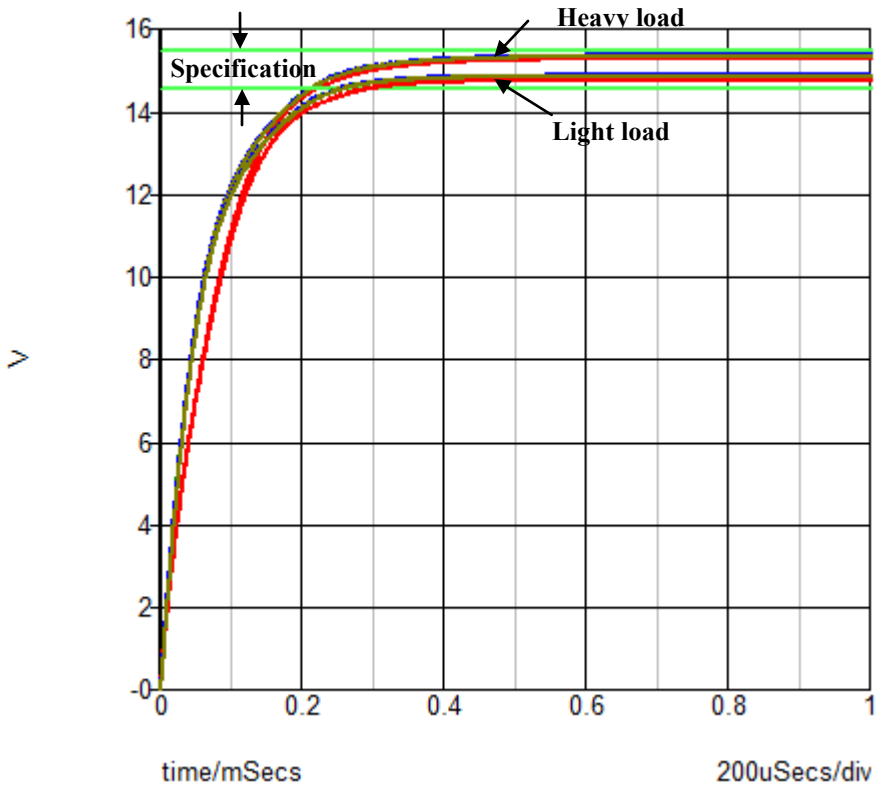
Table 2.8 Simulation conditions for inductor-less full-bridge converter

Switching frequency	600 kHz		
Duty cycle for D1 and D2	49.5%		
Phase angle between D1 and D2	180 °		
Full-bridge switch capacitance	30 pF		
$R_{ds(on)\text{-}high}$	2.3 Ω		
$R_{ds(on)\text{-}low}$	1.8 Ω		
Primary winding resistance	0.48 Ω		
Secondary winding resistance	0.38 Ω		
Turn ratios	5:4:4:4:4		
DC blocking capacitor	100 μF		
Leakage inductance	References to table 3.3		
Load resistor for N1, N2, and N3	Heavy load	Light load	Normal load
	500 Ω	1.5 kΩ	750 Ω
Load resistor for N4	Heavy load	Light load	Normal load
	150 Ω	450 Ω	225 Ω



(Light load: Load1=Load2=Load3=0.15 W, Load 4=0.5 W) *(Heavy load: Load1=Load2=Load3=0.45 W, Load 4=1.5 W)*

Figure 2.17 Simulation results of output voltages under different loads



(Light load: Load1=Load2=Load3=0.15 W, Load 4=0.5 W; Heavy load: Load1=Load2=Load3=0.45 W, Load 4=1.5 W)

Figure 2.18 Start-up transient waveforms of output voltages under different loads

The simulation results of each port under different loads are shown in Figure 2.17 and 2.18. As from equation (2-16), the wire voltage drop is proportional to the output current. Therefore the worst cases for this system is either all outputs at full load or all outputs at light load. The situations have been simulated in both cases. The simulation results show that the output voltage are effectively confined within specification. The highest output voltage would be observed on load 4 under light load condition at 15.33 V, while the lowest output voltage would be seen on load 1 under full load condition at 14.71 V. This error range is within the specification requirement. This simulation results will be compared with real system measurement in section 2.4. It is noticeable during simulation that the transformer magnetizing inductance value and clock frequency also have an effect on the output voltage. When a larger magnetizing inductance

is acheived, for example under high temperature, it is temping to drop the output. At the same time, a larger switching frequency in a full-bridge converter will result in a larger voltage drop on leakage inductance, which will lower down the output value. However this effect could be ignored with a precise clock.

The cross-regulation effects are analyzed trough the simulation. The results are listed in Table 2.9. From comparison between Tables 2.6 and 2.9, it is noticeable that all the polarity in two methods are identical. Therefore, the conclusion that the worst cases for output voltage are at heaviest loads and at lightest load is verified trough simulation. However, there is a relative error around 50% between the modeling and simulation. This is because the modeling is not exactly accurate, which assumes the instant current in each winding of group 1 is proportional with its output current to simplify the coupled case into decoupled L-R series model. To better model the cross-regulation effect within group 1, a more complicate model is needed, which will be one of the future works of this thesis.

Table 2.9 Simulation results of cross-regulation effects for full-bridge converter

($I_{o1\text{-}normal} = I_{o2\text{-}normal} = I_{o3\text{-}normal}$=0.02 A, $I_{o4\text{-}normal}$ =0.067A)

I_o (A)	I_{o1}		I_{o2}		I_{o3}		I_{o4}	
ΔV_o (mV)	0.01 A	0.03 A	0.01 A	0.03 A	0.01 A	0.03 A	0.033 A	0.1 A
V_{o1}-$V_{o1\text{-}normal}$	76 mV	-63 mV	52 mV	-46 mV	51 mV	-43 mV	76 mV	-71 mV
V_{o2}-$V_{o2\text{-}normal}$	52 mV	-43 mV	83 mV	-63 mV	52 mV	-42 mV	75 mV	-71 mV
V_{o3}-$V_{o3\text{-}normal}$	48 mV	-39 mV	50 mV	-43 mV	93 mV	-66 mV	76 mV	-70 mV
V_{o4}-$V_{o4\text{-}normal}$	21 mV	-21 mV	21 mV	-21 mV	21 mV	-21 mV	170 mV	-170 mV

2.5 Experiment Results of Boost Full-Bridge Converter

In this section, a converter is built for the experimental measurement. The switching waveforms and line output ripple in first stage boost converter are recorded in Figure 2.19, which is tested under normal load (2 W) and 12 V input. Two spike voltages could be seen on the line voltage ripple, which is caused by the switching of the second stage converter. The proof on that this spike is caused by the switching of second stage is the time interval between spikes is the same as the switching interval in the second stage converter. The output voltage across the outputs of two totem poles is plotted in Figures 2.20 and 2.21, scaled from whole period to detailed plot in commute-time. The switching time of the totem pole could be read from the Figures 2.21 and 2.22 as around 6 to 7 ns. The voltage ripples of group 1 and group 2 are shown in Figure 2.23 with the transformer primary side voltage waveform as reference.

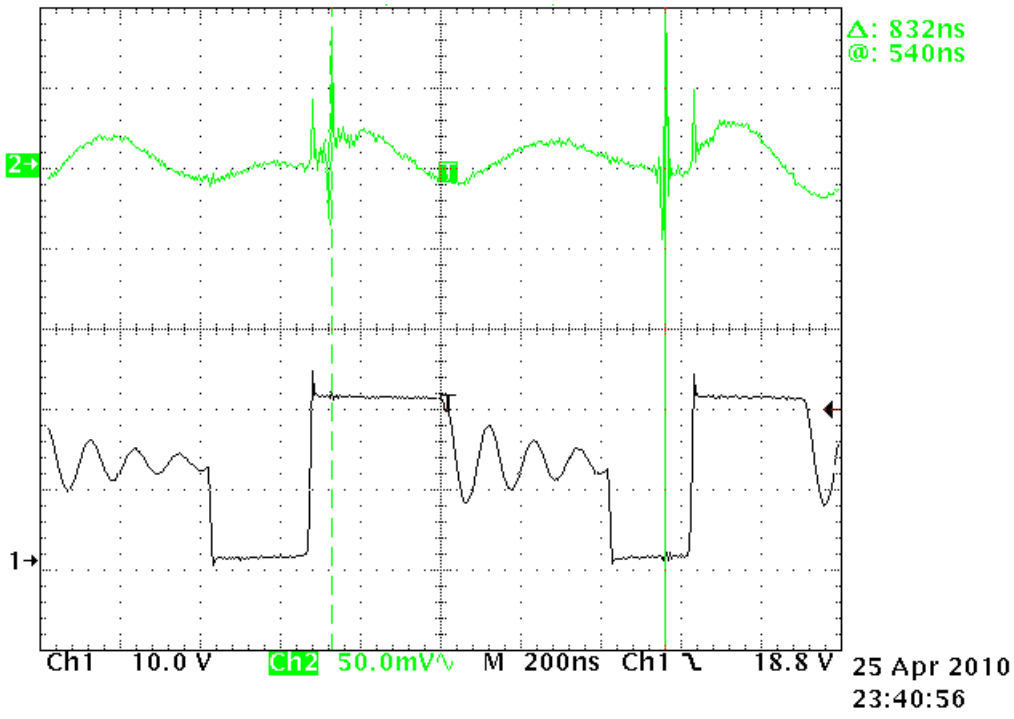


Figure 2.19 Waveforms of switch voltage and V_L (AC) of boost converter under normal load (2 W) and 12 V input voltage

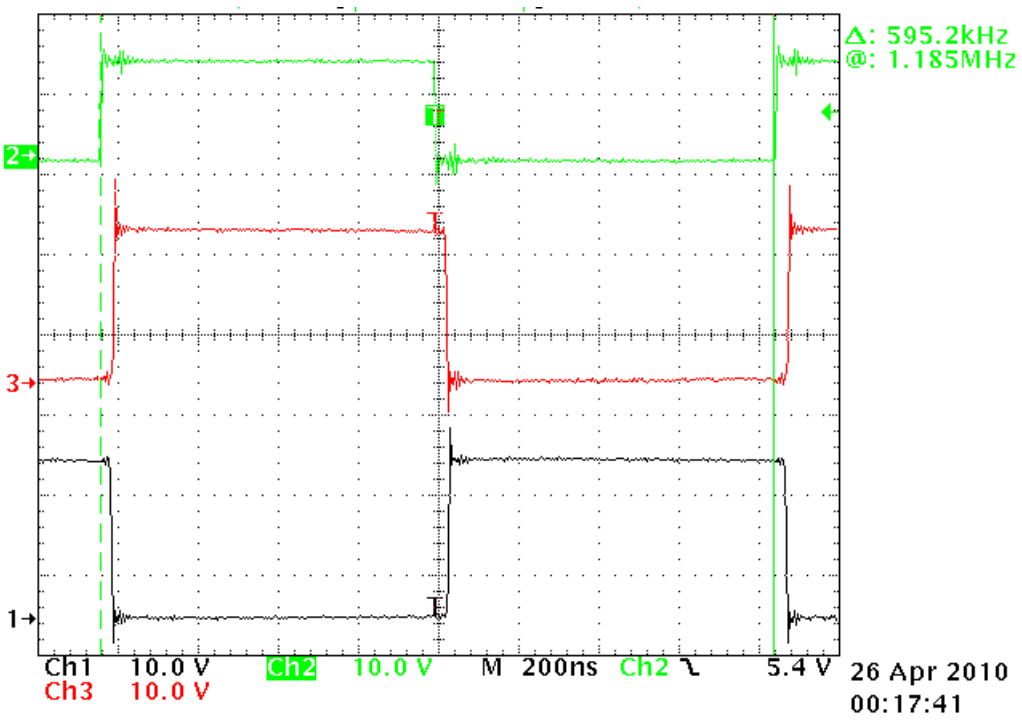


Figure 2.20 Waveforms of clock signal and output voltages of totem poles in full-bridge converter under normal load at 12 V input voltage

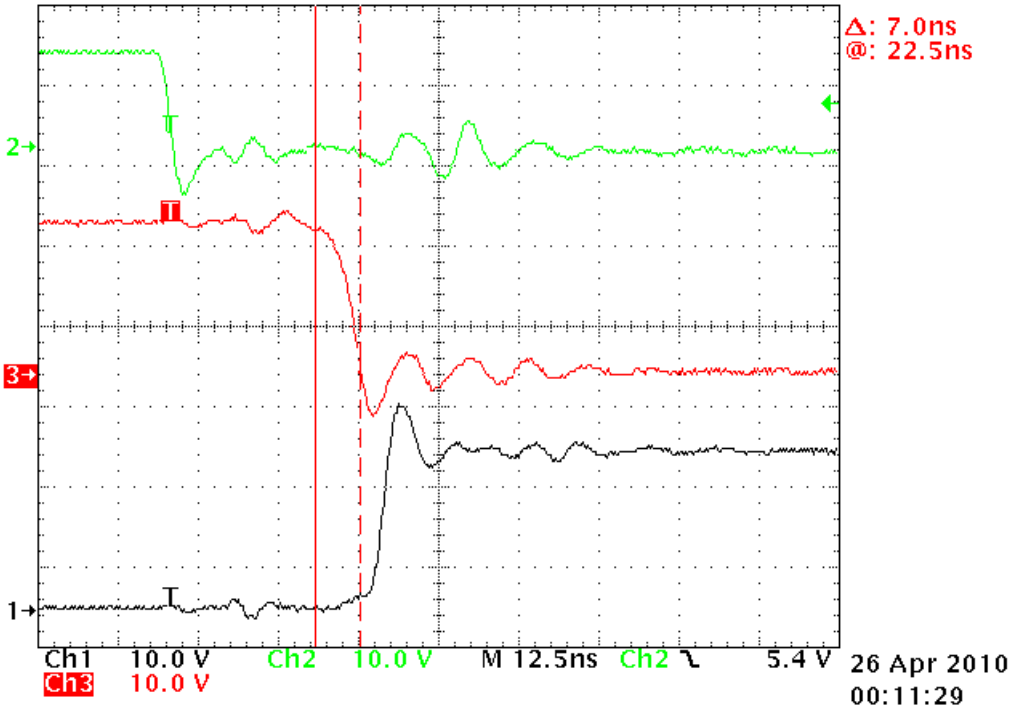


Figure 2.21 Waveforms of clock signal and output voltages of totem poles in full-bridge converter under normal load at 12 V input voltage (in detailed view when clock signal flips to 0)

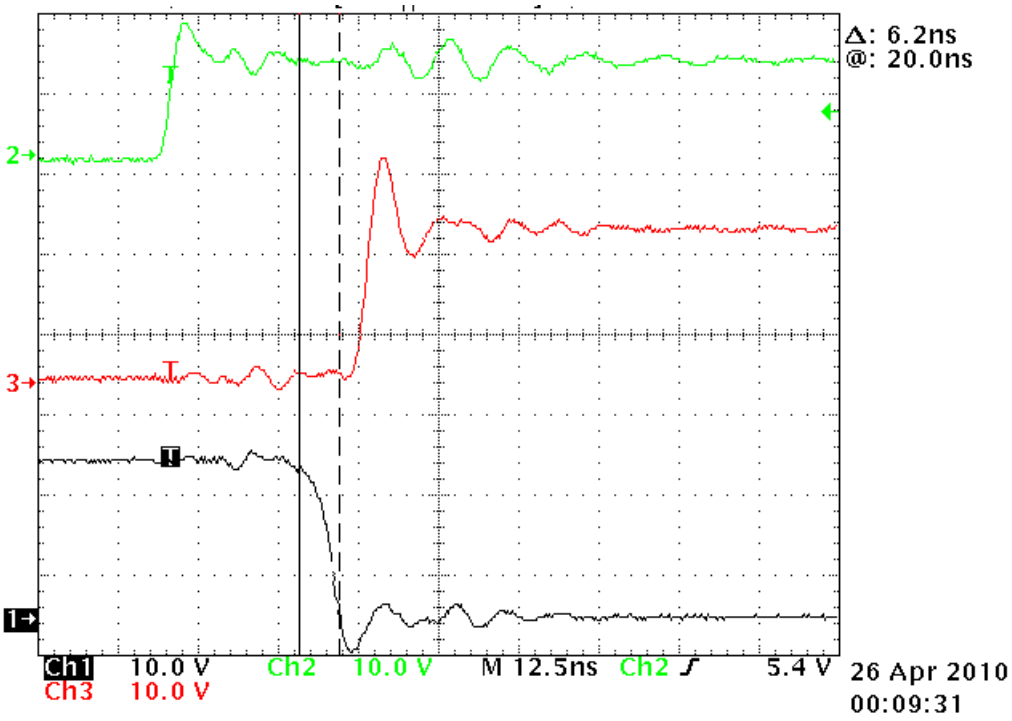


Figure 2.22 Waveforms of clock signal and output voltages of totem poles in full-bridge converter under normal load at 12 V input voltage (in detailed view when clock signal flips to 1)

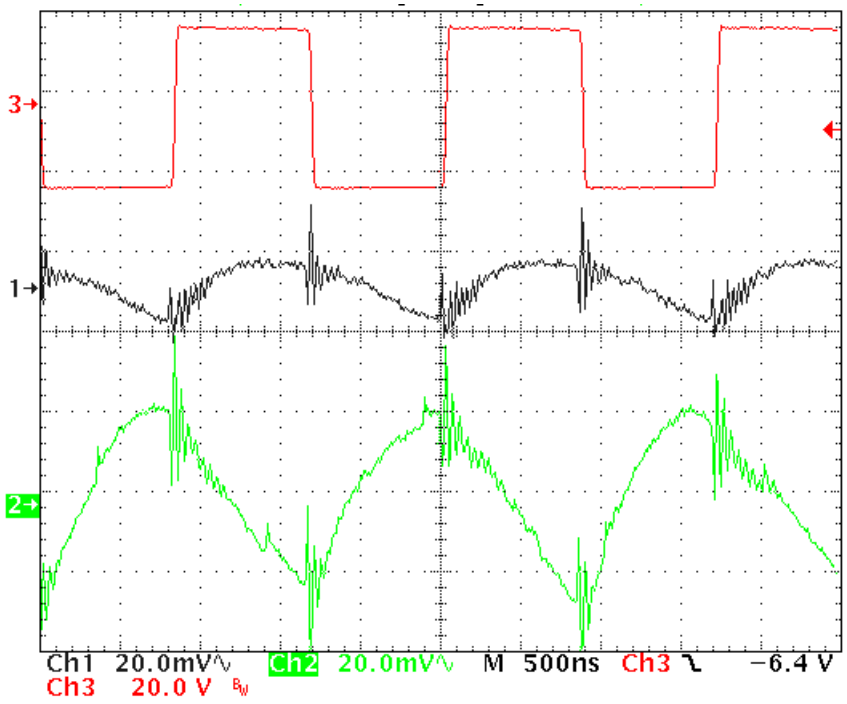


Figure 2.23 Waveforms of transformer primary side voltage and output ripples for load 1 and load 4

Table 2.10 Test results for different input voltage at light load condition

V_{in} (V)	V_{load1} (V)	V_{load2} (V)	V_{load3} (V)	V_{load4} (V)	f_{clock} (kHz)	V_L (V)	V_{Cdc} (V)
12	15.26	15.24	15.22	15.36	592.4	19.78	0.134
14	15.30	15.28	15.26	15.36	599.5	19.80	0.100
16	15.33	15.31	15.30	15.36	602.4	19.81	0.068
18	15.36	15.35	15.33	15.36	605.3	19.82	0.036

Table 2.11 Test results for different input voltage at heavy load condition

V_{in} (V)	V_{load1} (V)	V_{load2} (V)	V_{load3} (V)	V_{load4} (V)	f_{clock} (kHz)	V_L (V)	V_{Cdc} (V)
12	14.60	14.58	14.56	14.64	591.0	19.77	0.134
14	14.63	14.62	14.60	14.63	595.2	19.79	0.100
16	14.68	14.66	14.64	14.64	599.5	19.80	0.068
18	14.73	14.70	14.69	14.65	603.9	19.82	0.036

The experimental results of the converter under different loads and input voltages are listed in Tables 2.10 and 2.11. The worst conditions are at light load under the highest input voltage or heavy load under the lowest input voltage. It is noticeable, even the load current is balanced, there is dc voltage blocked by dc blocking cap. This is caused by the effect of unbalanced duty cycle. From the datasheet of the clock chip [14], the change of input voltage will shift the duty cycle at 0.5% /V. From equation (2-22), a dc voltage across the dc blocking capacitor is solved at 0.12 V, which fits the simulation results in Tables 2.10 and 2.11. The experimental results show the final converter could be properly working from 12 V to 18 V input range, under loads changing from 1.45 W to 2.85 W. However, the lowest voltage on load 2 and load 3 under light load condition dropped out from specification by 0.06 V. This can be improved by limiting the

equivalent resistance in section 2.3.1, or just by replacing their output diode with forward voltage decreased by 0.04 V. But in all other aspects, this converter meets with the specification requirements.

Table 2.12 Comparison on voltage errors from modeling, simulation, and experiment

(ΔI_{o1}= ΔI_{o2}=ΔI_{o3}=0.02 A, *ΔI_{o4}*=0.067 A*)*

	ΔVo (V)			
	N1	N2	N3	N4
Experimental results	0.66	0.66	0.66	0.72
Simulation	0.52	0.52	0.52	0.58
L-R series model	0.72	0.62	0.63	0.58

In Table 2.12, the voltage errors from modeling, simulation, and experiment are compared. The predicted values from L-R series model are close to both simulated and experimental results. This accordance further verifies the equations (2-10).

Table 2.13 Experimental results of efficiency in boost full-bridge converter vs P_{LOAD} and V_{IN}

Load Power	Input Voltage	Efficiency
Load1=0.15 W Load2=0.15 W Load3=0.15 W Load4=0.5 W	12V	49.0%
	15 V	49.4%
	18V	49.6%
Load1=0.45 W Load2=0.45 W Load3=0.45 W Load4=1.5 W	12V	67.0%
	15	69.0%
	18V	70.6%

The efficiency of the system under different operation conditions is measured in various experiments and listed in Table 2.13. The breakdown of the loss in the system is plotted in Figure 2.25. In this analysis, the core loss and conduction loss are obtained from calculation; the loss on boost stage, clock, and output diodes are measured from experiment; the loss of full-bridge switch is estimated from the sum of measured switching loss under no-load condition and calculated conduction loss.

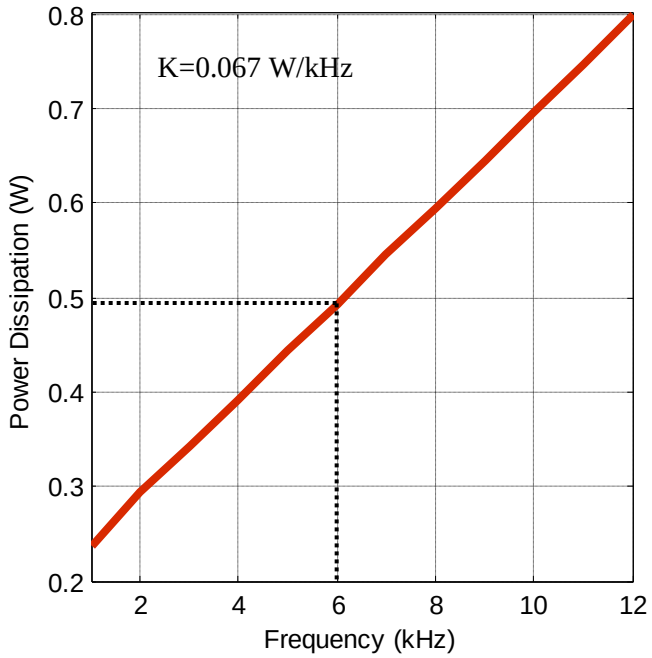


Figure 2.24 Power dissipation vs switching frequency under no-load (IXDN404)

As indicated in Figure 2.25, the major loss is caused by the full-bridge switch. The relationship of the full-bridge switch loss and switching frequency under no-load condition are measured and plotted in Figure 2.23. At the designed switching frequency, i.e., 600 kHz, the loss on the full-bridge switch is around 0.5 W. Under load condition, this loss would be even more severe, since the on-resistance of the switch is around 4.1 Ω. Therefore, high loss is the major drawback of using this dual low-side driver to perform full-bridge switching. Compared to the board area

saved by using this structure, there is a tradeoff between size and efficiency. At the same time, the efficiency on the previous boost stage has been tested at around 85% under 0.95 W load and 90% under 2.85 W load. Except for these factors, the losses from other parts are negligible.

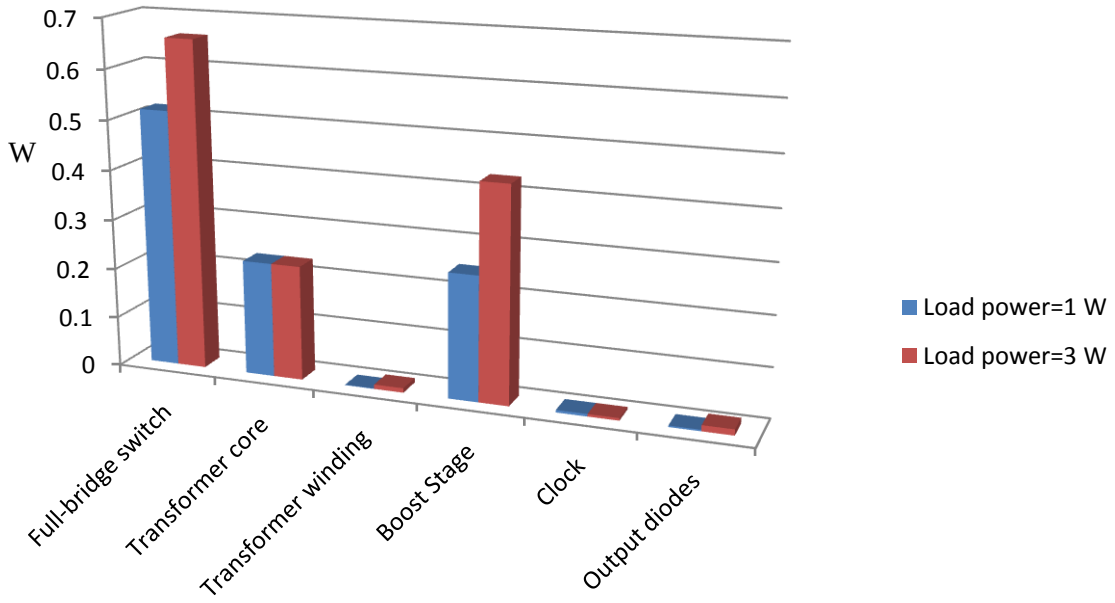


Figure 2.25 Breakdown of power loss under different loads (V_{IN}=15 V)

2.6 Summary

In this chapter, the operating principle of a boost full-bridge converter is briefly presented. After that, the design issues on each stage are carefully presented. The boost stage is designed to operate under peak current mode control. The components are selected, and the feedback circuit is carefully designed. Simulation results of the boost stage converter show the design operates in stable status. The operation principle of the second stage inductor-less full-bridge converter is presented in detail. The effects of parasitic resistance and inductance on output voltage error are analyzed in a numerical model, where the calculated results are shown. Then, two effects on dc blocking voltage are discussed. The simulation results of the full-bridge converter shows the

output voltage is effectively confined within the specification windows. Finally, a converter is built and tested. The test results show the real converter operates properly under 12 V to 18 V input voltage and 1.5 W to 2.85 W load condition. The only exception is that the lowest voltage on load 2 and load 3 under light load condition are out of the specification requirement by 0.06V. Several methods to fix this problem are proposed. The efficiency of the system is tested under various conditions by different loads and input voltages. The breakdown of power loss is listed, and the major loss of switching chip IXDN404 is analyzed.

2.7 Reference

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[11] Application note: LT1377 - 500kHz and 1MHz High Efficiency 1.5A Switching Regulators , Linear Technology.

[12] Datasheet: IXDN404/IXDI404/IXDF404 4 Ampere Dual Low-Side Ultrafast MOSET Drivers, IXYS.

[13] Datasheet: FDY4000CZ Complementary N & P-Channel PowerTrench MOSFET, Fairchild Semiconductor.

[14] Datasheet: MIC1555/1557 IttyBitty RC Timer / Oscillator, Micrel.

Chapter 3 Planar Transformer Design

Since the specification of the converter requires the total volume to be no more than 2 cm^3 and the profile to be less than 5 mm, the size of transformer is extremely important. To construct a higher power density and low-profile converter, the planar transformer design is a must under this situation. The structure of a typical planar transformer is illustrated in the Figure 3.1. The windings layouts on the PCB have been sandwiched by the magnetic core. A clip or tape should be used to clamp the core to minimize the air gap between each side.

Figure 3.1 The structure of a typical planar transformer (in reference to [1])

In this section, the detailed design of a low-height planar to meet the benchmark converter specifications is shown. The 3D FEA simulation result of the transformer is also presented. Furthermore, a real transformer is build and measured. A comparison between the simulation results and the measurement is made. After these, a model to analyze the cross-regulation effect from the transformer design is tackled. Based on this model, the simulation results for an

inductor-less full-bridge converter are shown. Finally, the issue on voltage isolation in PCB is analyzed in detail and methods to improve the breakdown voltage are proposed.

3.1 Transformer Design

The core selection is the key to the design, on consideration of size, leakage, and loss. There are several available core types for planar transformer application as shown in Figure 3.2. To minimize the leakage effect of the transformer, the EIQ core set is selected, which is composed with one half EQ core and one half I core. The first merit of this core is that almost the whole winding area is buried inside the core rather than extruded outside the core. The second merit of this core type is its large winding area, which is a key to ensure the minimum turn number on PCB in this miniature structure.

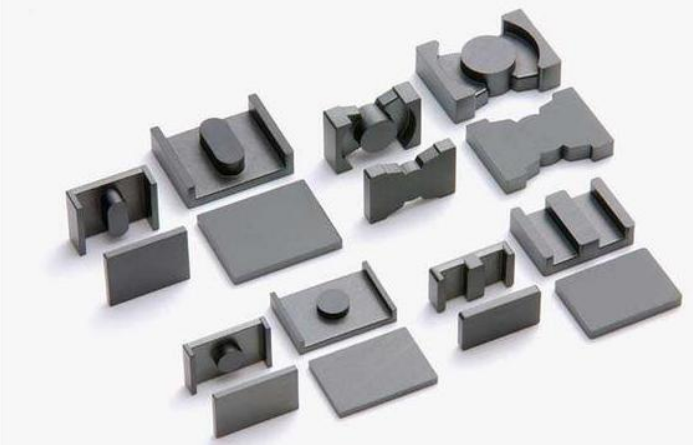

Figure 3.2 Magnetic cores for planar transformer (in reference to [2])

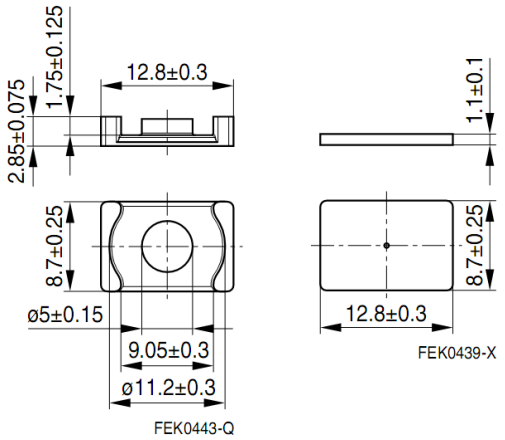

Figure 3.3 Dimensions of EIQ 13 core set (Unit: mm)

Table 3.1 Summary of planar transformer for full-bridge converter

Core	EIQ 13
Core material	R (Magnetics Inc.)
Frequency	600 kHz
Height	4.95 mm
Footprint	111.4 mm2
Primary inductance	47.5 μH
Turns	5:4:4:4:4
Trace width/ clearance	5 mil/ 5mil
PCB layer number	6
PCB thickness	64 mil
Bmax	0.0829 T
Primary winding resistance	0.48 Ω
Secondary winding resistance	0.38 Ω
Core Loss	243.6 mW
Copper Loss (DC approximation)	9.3 mW
Total Loss	252.9 mW

After times of retrospective try-out design, the final design employs the EIQ 13 core set, as shown in Figure 3.3. The design details are shown in the Table 3.1. One major approach to reduce the magnetic components size is to increase the switching frequency. Therefore, in this design the switching frequency is pushed into 600 kHz, which is the optimal point from the view

of core loss. Both the width and clearance of the PCB winding trace is designed as 5 mil, which is the minimal value the PCB manufacturer can make in acceptable costs. A six layer PCB is used to minimize the leakage inductance. Its layout is illustrated in Figure 3.4 for each layer, where colored lines represent trace on each layer and yellow outlines is the rout area to fit the core. The clearance from the edge of the trace to the rout area outline is designed as 20 mil. As in Figure 3.5, five windings are arranged on each layer, while the connection wires are routed in the bottom layer. The stack-up sequence is optimized to balance the leakage inductance of high-side loads and minimize the leakage inductance of the low-side load. To arrange each winding on each layer can also improve the voltage isolation of the planar transformer, considering the core material between each layer is FR-4, which can survive extremely high dielectric strength.

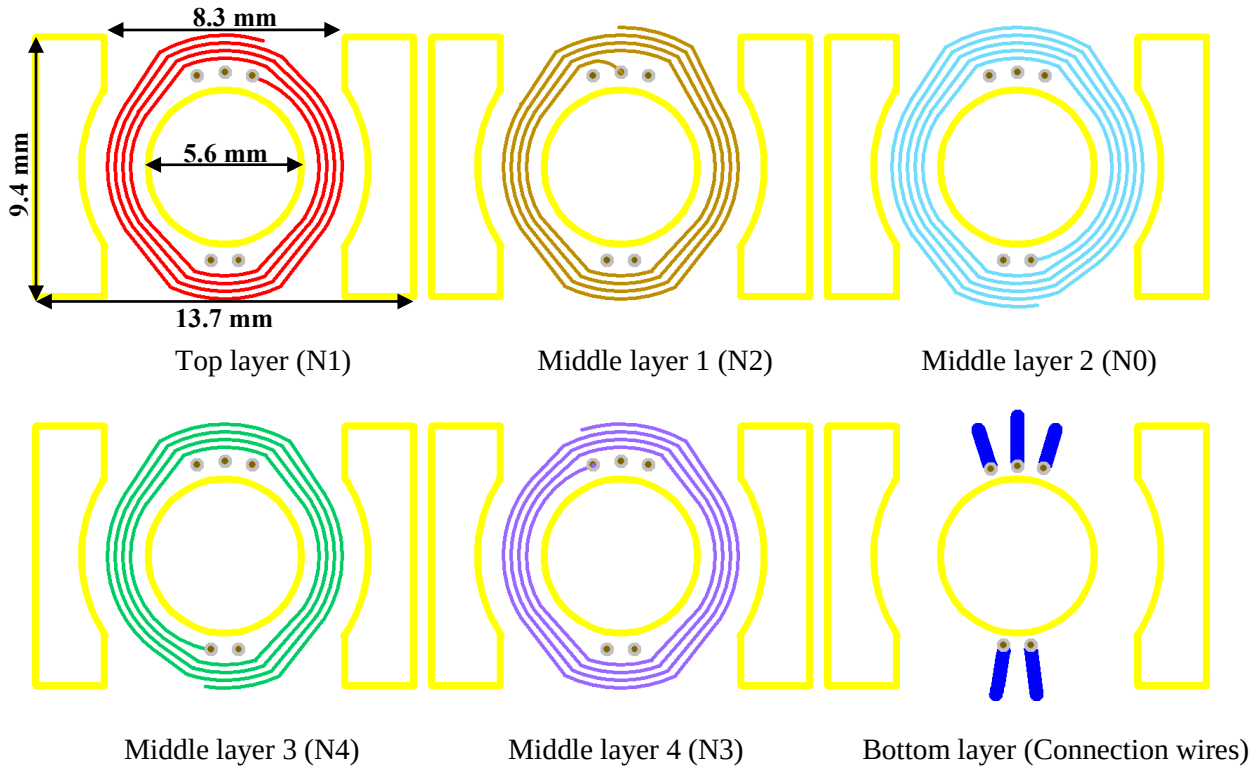

Figure 3.4 PCB layout of planar transformer

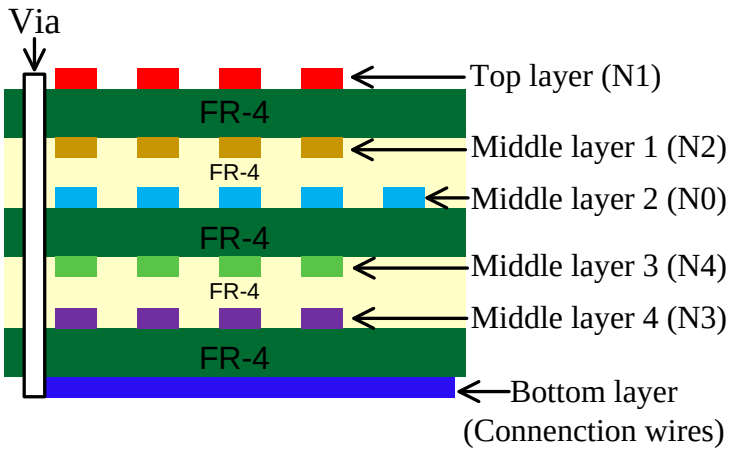

Figure 3.5 PCB stack-up diagram

3.2 Planar Transformer Layout and FEA Simulation

The planar transformer layout is imported into Ansoft Maxwell 3D FEA software for magnetic analysis. To import the layout in Protel into Maxwell, the layout should be saved in standard autocad format; then, imported into Maxwell in 2D model. After the 2D model for each layer in PCB layout is imported in Maxwell, a 3D model can been built by elongating the 2D model with proper thickness and arranging at proper height as Figure 3.5. Finally, the model is built as Figure 3.6, where the dimensions are according to this design. The extruded connection wires are included in the simulation model to improve the accuracy of the simulation, since the leakage inductance is critical in this design. It is worth mentioning that in the Maxwell simulation software these extruded extensions are needed to assign excitation from the boundary surfaces. The relative permeability of the transformer material is selected to be 1080, which is calibrated by the test measurement.

Table 3.2.A Simulation result of inductance matrix for planar transformer

***L* (μH)**	N_0	N_1	N_2	N_3	N_4
N_0	51.165	40.844	40.876	40.831	40.868
N_1	40.844	32.815	32.728	32.626	32.65
N_2	40.876	32.728	32.78	32.643	32.669
N_3	40.831	32.626	32.643	32.781	32.71
N_4	40.868	32.65	32.669	32.71	32.768

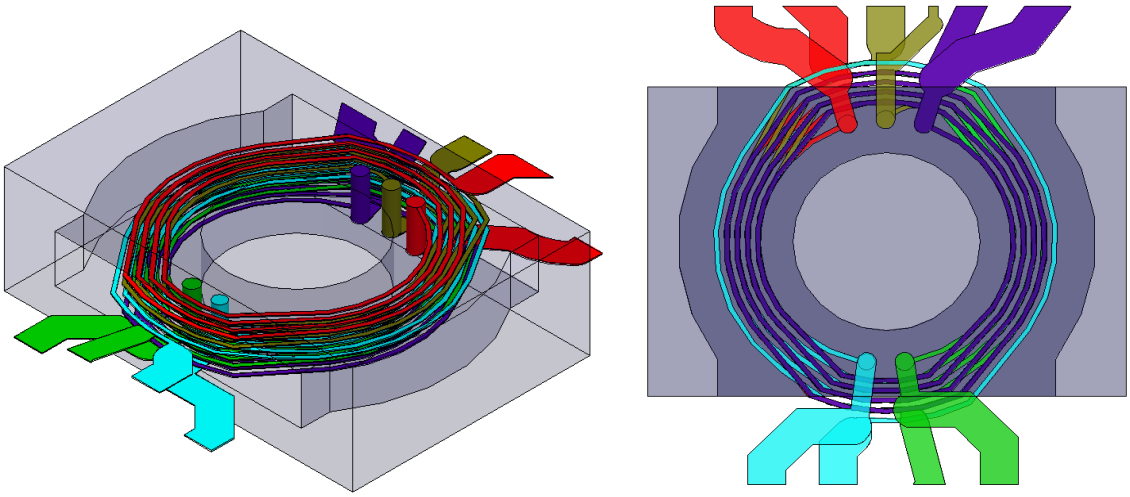

Figure 3.6 3-D model of planar transformer in Maxwell

Table 3.2.B Simulation result of coupling coefficient for planar transformer

K	N_0	N_1	N_2	N_3	N_4
N_0	1	0.99681	0.99809	0.99699	0.99809
N_1	0.99681	1	0.99788	0.99475	0.99568
N_2	0.99809	0.99788	1	0.9958	0.99681
N_3	0.99699	0.99475	0.9958	1	0.99802
N_4	0.99809	0.99568	0.99681	0.99802	1

The simulation results are listed in Table 3.2.A and 3.2.B. The simulation result of coupling coefficient proves the coupling between each winding is extremely firm, more than 99.47%.

Therefore, a minimized effect from leakage effect can be expected. The reason for such a firm coupling is the 6-layer PCB design employed. The clearance between each layer is as small as 12 mil (0.3 mm), and even the distance between the top layer and the bottom layer is only 1.5 mm. The only drawback of such a planar transformer is the limitation on the current provided. However, for this low-power application this does not affect the performance of the system.

3.3 Transformer Model in Circuit Analysis

Nowadays, one major objective of power electronics is to increase the power density. For multiple-output converters, one of the critical issues to achieve this goal is to integrate the magnetic components, where multiple-winding transformers are widely used. But the drawback of the multiple-winding transformer is the intrinsic cross-regulation effect, which has a close relationship with the leakage phenomenon of the transformer. This effect will degenerate the performance of the converters, which has been extensively analyzed in [3-5].

Paper [6-17] had proposed several models of a multiple-winding transformer to analyze the relationship between the leakage phenomenon and the cross-regulation effect. However, most of them involve complicated mathematical calculations or experimental measurement. Therefore, they are helpless in the practical design to limit the cross-regulation effect.

This thesis presents a new model for a multiple-winding transformer to tackle the effect of leakage phenomenon on converter operation in a designer friendly form. Based on the basic mutual inductance equations, the N-port model is derived. Further, a linear model is derived based on a tightly coupling assumption, i.e., coupling coefficients between winding pairs are more than 0.9. Finally, a four winding transformer is build and measured under the proposed

transformer model. Comparison in experiment measurement, N-port model, and simplified model are made.

3.3.1 Derivation of N-port cross-regulation Transformer Model

Intrinsically, the multiple-winding transformer is one implementation of mutual inductance. Therefore, the terminal voltage and current are described in the equation

$$\begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_n \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} & \cdots & L_{1n} \\ L_{12} & L_{22} & \cdots & L_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ L_{1n} & L_{2n} & \cdots & L_{nn} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_n \end{bmatrix} \qquad (3\text{-}1)$$

This mutual inductance matrix *L*, in an n winding transformer, can be decomposed into three parts: 1. the first row, 2. the first column in the rest, and 3. the rest n-1 ×n-1 matrix. In such a way, the equation (3-1) can be decomposed into two equations (3-2) and (3-3).

$$v_1 = \sum_{j=1}^{n} L_{1j} \frac{di_j}{dt} = L_{11} \frac{di_1}{dt} + \sum_{j=2}^{n} L_{1j} \frac{di_j}{dt} \qquad (3\text{-}2)$$

$$\begin{bmatrix} v_2 \\ \vdots \\ v_n \end{bmatrix} = \begin{bmatrix} L_{12} \\ \vdots \\ L_{1n} \end{bmatrix} \frac{di_1}{dt} + \begin{bmatrix} L_{22} & \cdots & L_{2n} \\ \vdots & \ddots & \vdots \\ L_{2n} & \cdots & L_{nn} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_2 \\ \vdots \\ i_n \end{bmatrix} \qquad (3\text{-}3)$$

Equation (2) can be rewritten in to the following equation

$$\frac{di_1}{dt} = \frac{v_1}{L_{11}} - \frac{1}{L_{11}} \sum_{j=2}^{n} L_{1j} \frac{di_j}{dt} \qquad (3\text{-}4)$$

Substitute (3-4) into (3-3), the N-port model can be solved out in equation (3-5). A schematic diagram for 4-winding transformer in this N-port cross-regulation model is shown in Fig. 1. In this model, the input side has a parallel inductor, which equates to the self-inductance of the primary winding. The secondary side output voltages are the sums of the primary-side voltage times effective turn ratio, the voltage drop on leakage inductance ℓ_{ii}, and all sensed voltages of cross-regulation inductance ℓ_{ik},which is named as mutual-leakage inductance through this thesis, from other secondary windings. If the winding resistance is not negligible, corresponding winding resistors should be placed in serial of each winding into this model.

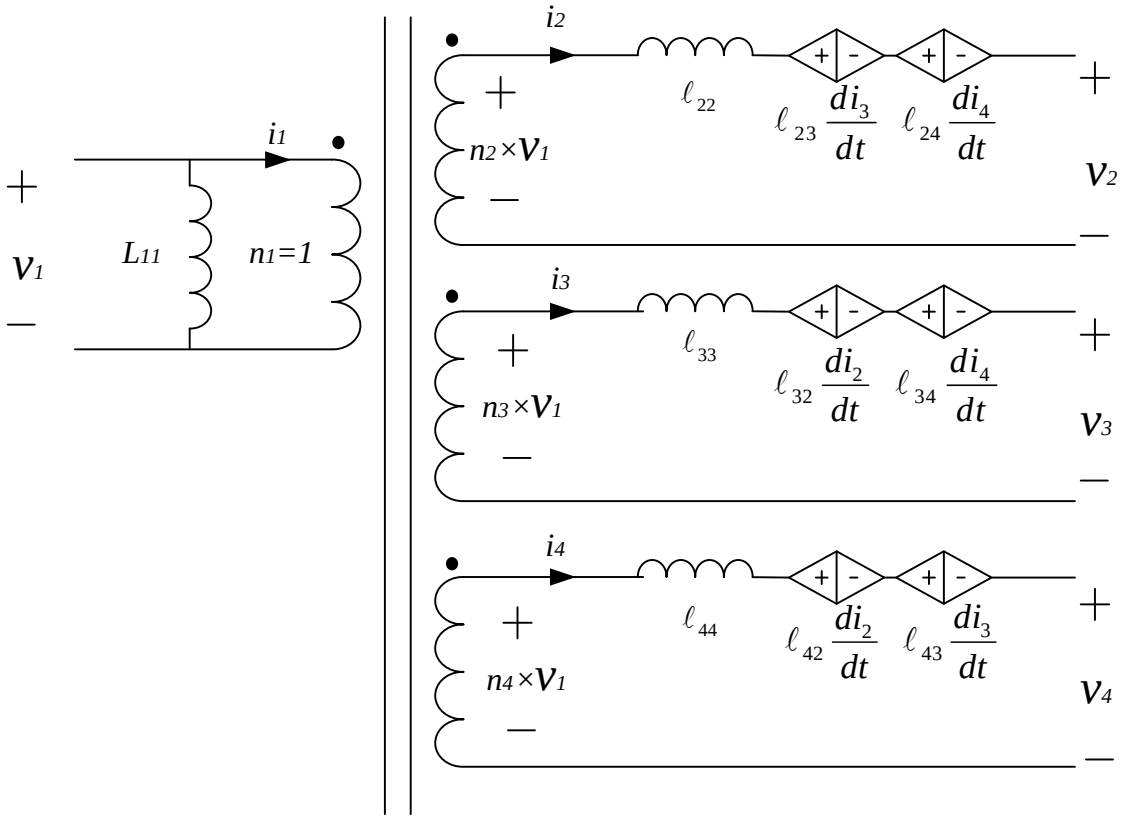

Figure 3.7 N-port model for 4-winding transformer

$$\begin{bmatrix} v_2 \\ \vdots \\ v_n \end{bmatrix} = v_1 \begin{bmatrix} L_{12}/L_{11} \\ \vdots \\ L_{1n}/L_{11} \end{bmatrix} + \ell \frac{d}{dt} \begin{bmatrix} i_2 \\ \vdots \\ i_n \end{bmatrix} \qquad (3\text{-}5)$$

In which, the turn number n and leakage inductance matrix ℓ is

$$n_1 = 1, \qquad n_i = L_{1i}/L_{11} \ (i = 2, \cdots, n) \qquad (3\text{-}6)$$

$$\ell_{jk} = L_{jk} - \frac{L_{1j} L_{1k}}{L_{11}} \qquad (3\text{-}7)$$

The coupling coefficient k_{ij}, between winding i and j, is between 0 and 1, and can be calculated directly from the transformer geometry. If the leakage coefficient d_{ij} is defined as equation (3-8), it is also limited to the range from 0 to 1.

$$d_{ij} = 1 - k_{ij} \qquad (3\text{-}8)$$

In a tightly coupling case, the leakage coefficient is close to zero. After the differential approximations, equations (3-6) could be linearized into equation (3-8) in the terms of winding self-inductance and leakage coefficients.

$$n_j = \sqrt{\frac{L_{jj}}{L_{11}}}(1 - d_{1j}), \ \ell_{jk} = \sqrt{L_{jj} L_{kk}}(d_{1j} + d_{1k} - d_{jk}) \quad (3\text{-}9)$$

This linear model shows that effective turn ratio will decrease as the leakage inductance increases; the cross-regulation inductance can be decreased by increasing leakage between the secondary winding pairs or increasing the coupling between the primary winding and secondary

winding. At the same time, this linear model links the geometry layout of windings with the circuit leakage inductance linearly, which is a key for the optimization of transformer geometry to minimize the effect of leakage in circuit performance.

From the linear model, it is clearly indicated that the effective turn ratio will decrease as the leakage inductance increase; the cross-regulation inductance could be decreased by increase leakage between secondary winding pairs or increase the coupling between the primary winding and secondary winding. This would be a general design guideline for applications where cross-regulation is critical to converter operation.

3.3.2 Calculation of Leakage Inductance Matrix from Its 3-D FEA Simulation Results

Based on the model proposed in section 3.3.1 and the 3D-FEA simulation results of planar transformer in section 3.2, the leakage inductance matrix has been solved in the Table 3.3.

Table 3.3 Leakage inductance matrix from 3-D FEA simulation

$\ell\ (nH)$	N_1	N_2	N_3	N_4
N_1	210.0	97.5	31.4	25.9
N_2	97.5	124.0	22.9	19.3
N_3	31.4	22. 9	196.8	96. 3
N_4	25.9	19.3	96.3	124.7

The result of the leakage inductance matrix, as in Table 3.3, shows a planar transformer with a maximum leakage inductance at 210 nH. Refer to the conclusion in section 2.3.2, the leakage effect of the planar transformer for this design on the output voltage error is expected to be negligible. At the same time, this simulation result is compared with the real set-up measurement in the next section, which shows that this simulation result is a good fit with reality with acceptable error at 10s of nH.

3.4 Extraction of Transformer Parameters

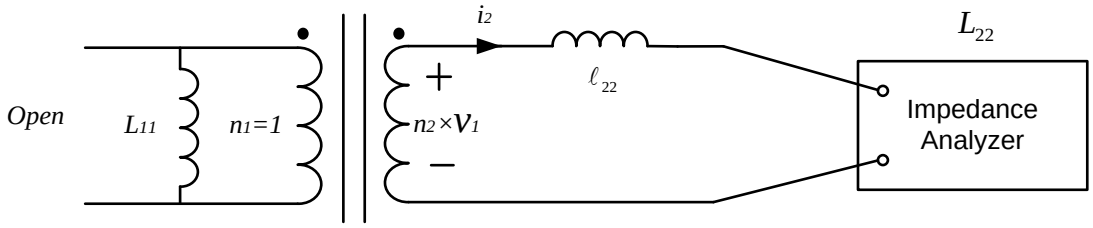

Figure 3.8 Test setup for self-inductance measurement

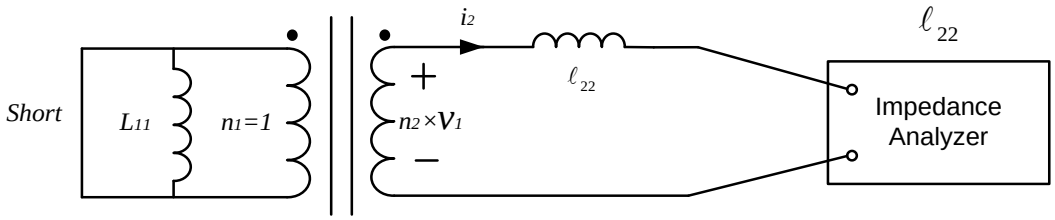

Figure 3.9 Test setup for self-leakage inductance measurement

Based on the N-port model as in Figure 3.7, the parameter can be extracted under several tests as in the Figure 3.8 to 3.10. First, as in Figure 3.8, the self-inductance of each winding can be measured by an impedance analyzer with all other winding open. Secondly, as in Figure 3.9, the self-leakage inductance on the secondary winding is measured by an impedance analyzer with the primary side winding shorted. Finally, the mutual inductance is measured indirectly by the subtraction of two measurement results. As in Figure 3.10 A and B, the primary side winding is shorted; and the two windings, whose mutual inductance is going to be measured, are connected serially in two different directions. The impedance of the two windings connected with the same current direction is $\ell_{22}+\ell_{33}+2\ell_{23}$; while the impedance of the two windings connected with the reverse current direction is $\ell_{22}+\ell_{33}-2\ell_{23}$. The mutual inductance ℓ_{23} can be calculated from the test results in test A and test B as in equation (3-11).

$$\ell_{23} = \frac{L_{TestA} - L_{TestB}}{4} \qquad (3\text{-}11)$$

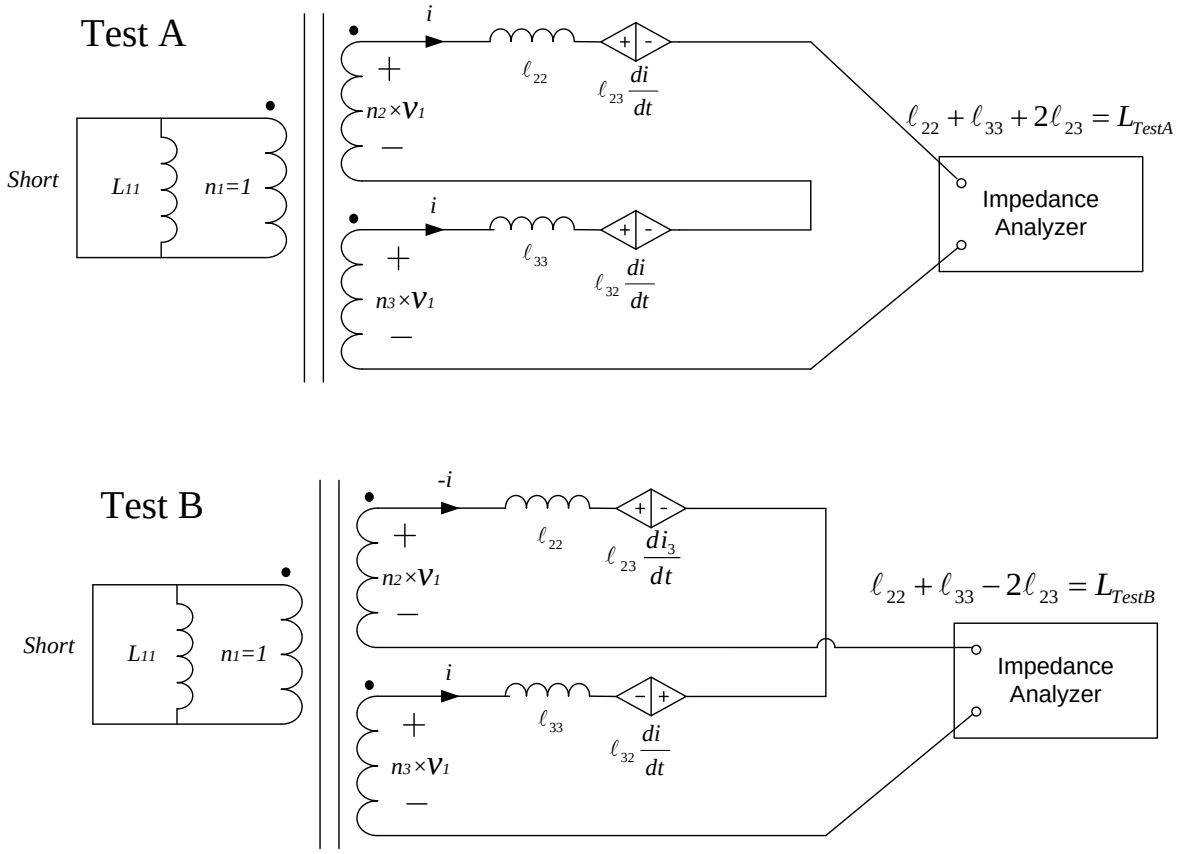

Figure 3.10 Test setup for mutual-leakage inductance measurement

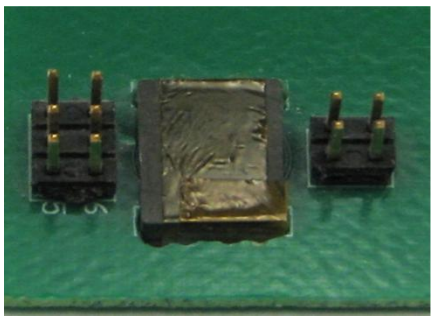

Figure 3.11 Planar transformer built for parameter extraction

In this section, a planar transformer has been built for the test measurement. The self-inductance values are measured, as illustrated in Figure 3.8, and listed in Table 3.4.

Table 3.4 Measured self-inductance values

Parameter	L_{00}	L_{11}	L_{22}	L_{33}	L_{44}
Value (μH)	51.07	32.82	32.79	32.81	32.78

As proposed in Figures 3.9 and 3.10, the cross-regulation inductances are measured and compared with predicted values from simulation in Table 3.5. From the results of the measured cross-regulation inductances and the predicted values listed in Table 3.5, it can be concluded that the model predictions are very close to experimental measurement results.

Table 3.5 Comparison of measured cross-regulation inductances and predicted values

Parameter	ℓ_{11}	ℓ_{22}	ℓ_{33}	ℓ_{44}	ℓ_{12}	ℓ_{13}	ℓ_{23}
Measured value (nH)	230	173	226	126	126.5	34.8	38.3
Predicted value from simulation	210.0	124.0	196.8	124.7	97.5	31.4	22.9
Relative error	8.7%	28.3%	12.9%	1.0%	22.9%	9.7%	40.2%

3.5 Effect of Trace Layout and Encapsulation on Breakdown Voltage in PCB

On the Printed Circuit Board, the solder mask is a polymer material, which provides a protective and isolative coating for copper traces to prevent short circuit, as in [18, 26, 27, 31, and 32]. The physical and electrical property of the polymer material used as a solder mask on the PCB is widely analyzed in papers [19-32]. However, the analysis concerning the breakdown voltage of the PCB is scare, since the polymer for the solder mask is usually considered as highly resistive material rather than isolation material. This thesis begins with analysis and testing of the

breakdown voltage of the PCB. Thereafter, one type of silicon elastomer is employed as isolation material covering the solder mask to prevent break down at voltage as high as 6 kV, and the test results and comparison are shown.

3.5.1 PCB Test Pattern

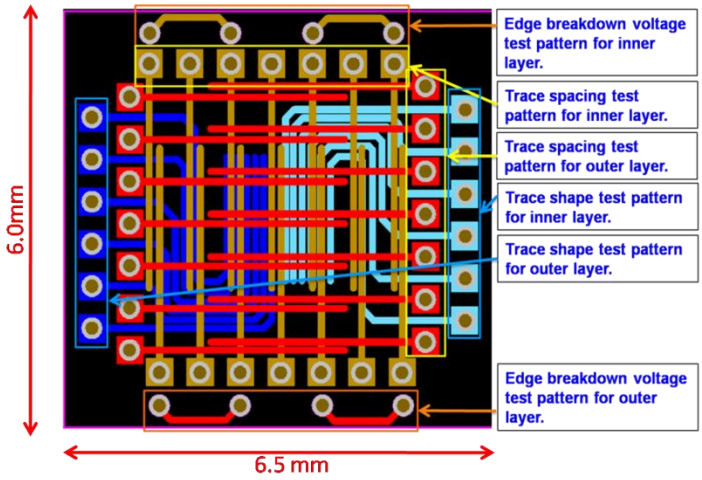

Figure 3.12 Test pattern layout for the breakdown voltage test

A PCB trace test pattern is designed to test the impacts of the trace clearance, edge clearance, and the winding shape on the breakdown voltage of the PCB traces, as illustrated in Figure 3.12. The trace clearances to be tested are 178 μm (7 mil), 255 μm (10 mil), 305 μm (12 mil), 381 μm (15 mil), 508 μm (20 mil). The edge clearances to be tested are 255 μm (10 mil), and 381 μm (15 mil). The winding shape to be tested is a 45-degree angle with the trace clearance varied as previous. The PCB board tested is one 4 layer PCB manufactured from Sierra Proto Express.

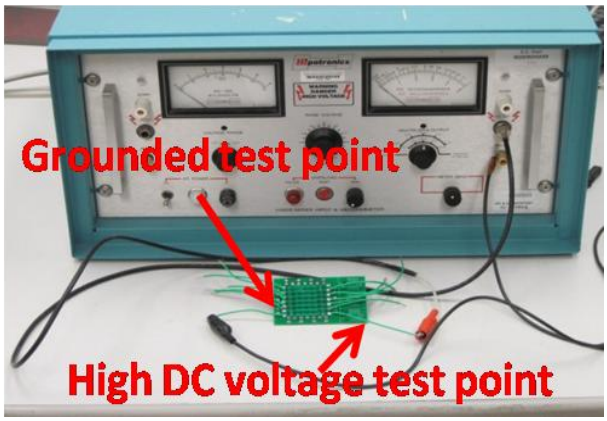

Figure 3.13 Test setup of breakdown voltage between PCB trace

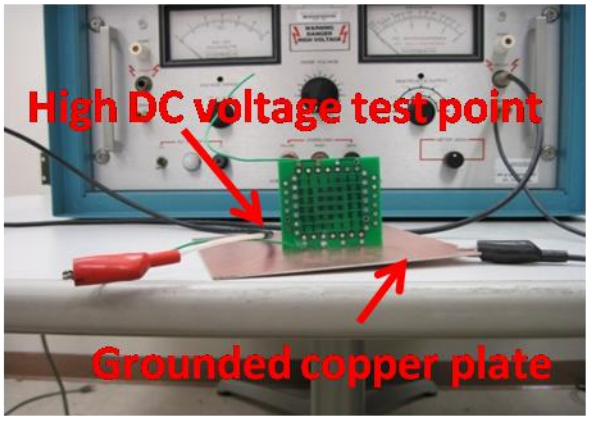

Figure 3.14 Test setup of breakdown voltage for edge trace

3.5.2 Test of Breakdown Voltage for the PCB

The test of breakdown voltage for the PCB is measured with a Hipotronics H300B Series HiPot at room temperature, i.e., 27 ℃. The voltage applied between traces is increased to the breakdown voltage or 6 kV, which is the maximum DC voltage that can be applied on this device. The test setups are illustrated in Figure 3.13 and 3.14. The results of the breakdown voltage for various clearances and patterns are listed in Table 3.6 and Table 3.7.

Table 3.6 The breakdown votages between PCB traces

Clearance (μm/mil)	Trace Breakdown voltage (kV)			
	Straight traces on outer layer	Straight traces on inner layer	Meandering traces on outer layer	Meandering traces on inner layer
178 / 7	4.1	>6	4.2	>6
255 / 10	4.2	>6	4.3	>6
305 / 12	4.0	>6	4.1	>6
381 / 15	4.3	>6	4.2	>6
508 / 20	4.2	>6	4.3	>6

Table 3.7 The breakdown voltage of edge trace

Clearance (μm / mil)	Edge breakdown voltage (kV)	
	Outer layer	Inner layer
255 / 10	2.1	>6
381 / 15	2.0	>6

In the edge-trace breakdown voltage test, one DC voltage is applied across the edge trace and the copper plate, which the test PCB is standing on. Silicon elastomer is used to cover the vias and soldered joints, as shown in Figure 3.16.

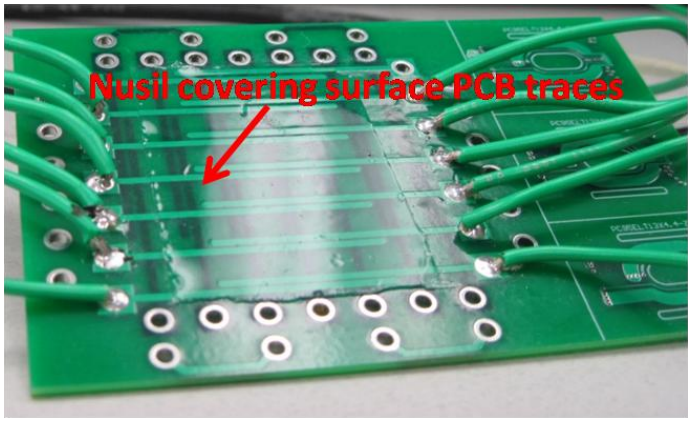

Figure 3.15 The PCB with silicon elastomer covered on surface

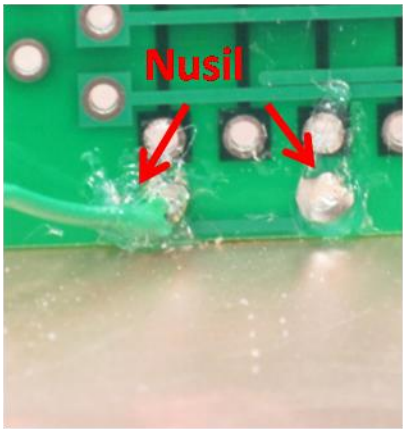

Figure 3.16 The PCB with silicon elastomer covered on the via and solder joint

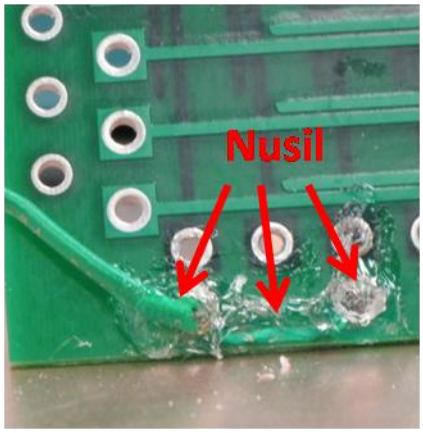

Figure 3.17 The PCB with silicon elastomer covered on the solder joint, edge via and trace

Table 3.8 The breakdown voltage between PCB traces (covered with silicon elastomer)

Clearance (μm / mil)	Trace breakdown voltage (kV)	
	Straight traces on outer layer (Covered with R-2188)	Meandering traces on outer layer (Covered with R-2188)
178 / 7	>6	>6
255 / 10	>6	>6
305 / 12	>6	>6
381 / 15	>6	>6
508 / 20	>6	>6

Table 3.9 The breakdown voltage of edge trace (covered with silicon elastomer on traces)

Clearance (μm / mil)	Edge breakdown voltage (kV)
	Outer layer (Covered with R-2188)
255 / 10	>6
381 / 15	>6

From the test results shown in Table 3.6, and Table 3.7, the surface traces pairs on the surface layer broke down at about 4 kV. As illustrated from Figure 3.16 and Figure 3.17, the outer layer traces are covered with R-2188 by NuSil Technology LLC, which is one type of silicon elastomer with high dielectric strength. The comparative experimental results after covering with silicon elastomer are shown in Table 3.8, and 3.9. The new test results show that if R-2188 is properly applied over the PCB traces, all surface trace breakdown voltage would be improved to more than 6 kV.

3.6 Summary

In this chapter, the detailed planar transformer design is proposed. After that, a 3-D FEA model has been built in Maxwell. The inductance matrix and coupling coefficient have been solved from the 3-D FEA simulation.

At the same time, an N-port model is presented, where the cross-regulation effects of a multiple-winding transformer are modeled by cross-regulation inductances on output windings, which link the output voltage with the change rate of current in other windings. To simplify the calculation, a linear model is proposed to calculate the cross-regulation inductances from leakage coefficients under tightly coupling.

Based on this N-port model, the scheme to extract every parameter is proposed. Later, a planar transformer is built for parameter extraction measurement. Comparison in experiment measurement, N-port model from 3-D simulation results shows consistency between experiment and model prediction.

Finally, the impacts of the trace clearance, edge clearance, and the winding shape on the breakdown voltage of the PCB traces in different layers are tested. Based on these test results, a noticeable increase of trace clearance on surface layer by 13 mil does not improve the breakdown voltage significantly. To improve the breakdown voltage without increasing the clearance to a larger scale, R-2188 by NuSil Technology LLC, is used as dielectric material to cover the weak area on the PCB surface. The further test results show that the breakdown voltage of PCB is improved from 4 kV to more than 6 kV by covering the surface with R-2188.

3.7 Reference

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Chapter 4 Conclusion and Future Works

4.1 Conclusion

In this thesis, an inductor-less full-bridge converter is firstly proposed with small footprint construction. One isolated multiple-output gate drive power supply is achieved by a structure cascading boost regulator with an unregulated full-bridge converter. The operation principle of the inductor-less full-bridge converter is introduced, and several effects on output voltage error are analyzed. The real converter built proves the previous analysis and meets with specification s.

Based on a proposed N-port transformer model, parameter extraction measurement and simulation method are proposed. The real system measurement fits the simulation very well, which proves the consistency from the model to the method of parameter extraction. To improve the isolation voltage between each output, an encapsulation method is proposed and tested. Covering silicon elastomer on the surfacing layout would help the design achieve an isolation voltage of more than 6 kV.

Compared with the flyback converter, this boost full-bridge converter has the following merits:

1. Smaller core size

In Full-bridge converter, the transformer does not need to store energy to perform the role as inductor, which makes a possible smaller magnetic core size possible.

2. Less severe cross-regulation effects

The full-bridge converter does not suffer from the cross-regulation effect as severe as the flyback converter. Moreover, the four loads can be divided into two groups to interleave during each 50% duty cycle. Therefore, a heavier load on output 4 can be isolated from the other three outputs in the sense of cross-regulation. This further reduces the effect of cross-regulation.

3. Clamped output voltage

At no-load condition, the output of the full-bridge converter will not rise to the dangerous region to destroy the IGBT device.

4. Easy for output extension

The non-isolated power supply for the PWM controller can be placed between the boost regulator and the full-bridge converter, as in Figure 1-5. If its desired voltage is lower from the boost regulator, a Linear Regulator (LR) could be employed to reduce the line voltage.

5. No need of isolation feedback

Only the first stage is regulated, while the isolated full-bridge stage is unregulated. Therefore, there is no complicated feedback circuit needed to feedback the isolated output.

4.2 Future Works

To improve the efficiency of the system and limit the errors of output voltage, the full-bridge switch, i.e., IXDN404, should be replaced with another IC with less switching loss and drain-to-source resistance. However, it is almost true that this better performance chip has a larger

footprint. Therefore, the overall size of the converter will increase. A trade of between size and efficiency should be made.

In section 3.3.1, the concept of the decoupling coefficient is raised. A linear model to calculate leakage inductance from this coefficient is derived under a firm coupling assumption. In fact, there is a linear relationship between two winding distance and decoupling coefficient. Therefore, there is a linear model connecting the geometry layout to the leakage inductance by a bridge as the decoupling coefficient. This linear model might lead us to a scheme on the optimization of limiting leakage inductance design from winding geometry layout. For application with emphasis on limiting cross-regulation effect, this possible optimization method could save design engineers from time-consuming trial and error method in magnetic design.

Appendix: Benchmark Comparison

In this chapter, a flyback converter as benchmark is designed at the beginning. Afterward, this design has been characterized into a simulation model in Simplis. The simulation results are compared with the ones from boost full-bridge converter designed in previous chapter. From the comparison, the pros and cons of boost full-bridge converter will be discussed extensively as the conclusion. Finally, future works are proposed.

A.1 Benchmark Converter Design

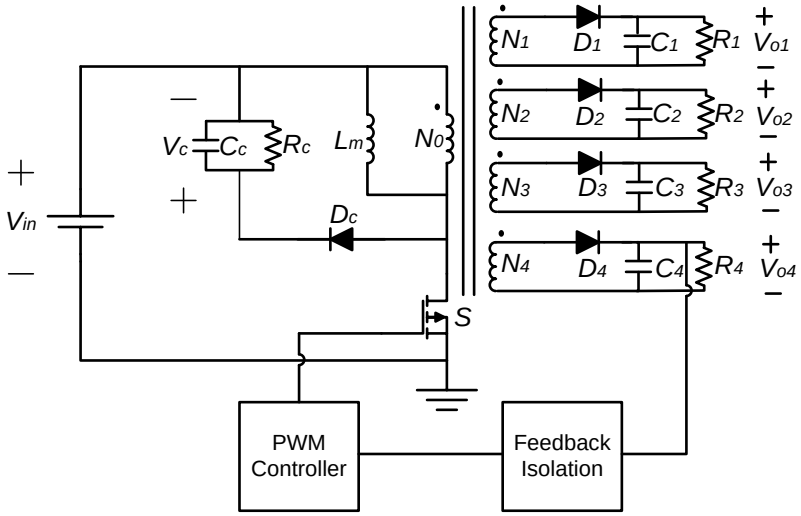


Figure A.1 Schematic diagram of flyback converter with feedback isolation

A schematic diagram of flyback converter is shown in the Figure A.1. The voltage on load 4 is sensed and compared with 15 V to control the output voltage. The major components of this converter are five-winding coupled inductor, feedback isolation circuit, PWM controller, primary side power switch, and snubbed circuit. In this section, those major components are selected and

listed in Table A.1. From the footprints of these major components, the overall footprint of this flyback converter is estimated.

Table A.1 Bill of materials of major components in flyback converter

Designator	Description	Footprint (cm^2)	Part No. (Vendor)
Feedback Isolation	7500 V_{ISO}, 500 kHz, Optocoupler	0.9	MCT2-M (Fairchild)
PWM Controller	100V, Current Mode PWM Controller	0.1	LM5030 (National Semi)
S (Primary Switch)	60 V, 1.7 A, 0.18 Ω, N-Channel MOSFET	0.1	FDN5630 (Fairchild)
Planar inductor	EIQ 13	1.2	EIQ 13 (Magnet Inc)

The total footprint of the major components in the flyback can be solved from Table A.1 as 2.3 cm^2. Assuming the same filling factor as the boost converter, as in Table A.2, the overall footprint of the flyback converter is estimated as 9.6 cm^2. The major reason of a larger size is that the requirement on 6 kV isolation voltage needs a large optocoupler to isolate the output from the primary side, which is not necessary in boost full-bridge topology.

Table A.2 Footprints of major components in boost full-bridge converter

	LT1377	MIC1557	IXDN404	EIQ13	Components	Total
Footprint (cm^2)	0.3	0.1	0.3	1.2	1.9	7.9

The planar coupled-inductor is designed in Table A.3. The same core is employed for a fair comparison. The air gap is included in the new design to protect the magnetic core from saturation.

Table A.3 Summary of planar inductor for flyback converter

Core	EIQ 13
Core material	R (Magnetics Inc.)
Frequency	600 kHz
Height	4.95 mm
Footprint	111.4 mm2
Primary inductance	10 μH
Air gap length	24.6 μm
Turns	5:5:5:5:5
Trace width/ clearance	5 mil/ 5mil
PCB thickness	64 mil
Bmax	0.210 T
Primary winding resistance	0.48 Ω
Secondary winding resistance	0.48 Ω
Core Loss	1.21 W
Copper Loss (DC approximation)	0.07 W
Total Loss	1.36 W

The core loss is huge because of the large B_{max}, which is caused by a small turn number confined by the limited winding area in the core and the minimal trace width and clearance. The relationship confines the maximum magnetic flux density, i.e., B_{max}, in the equation (A-1). In which the flux Φ could be solved in (A-2).

$$B_{max} = \Phi / A_C \qquad \text{(A-1)}$$

$$\Phi = \frac{L \cdot I_{max}}{n} \qquad \text{(A-2)}$$

In equation (1) and (2), A_C is the core cross-section area, which is 9.8 mm^2 from the datasheet of EIQ 13 core set; I_{max} is the maximum current in the inductor, which is 1.03 A from the simulation results under 2.85 W total output and 15 V input voltage. In an actual design, a magnetic core with a much larger size should be employed to increase the winding turns.

A.2 Simulation of Benchmark Converter

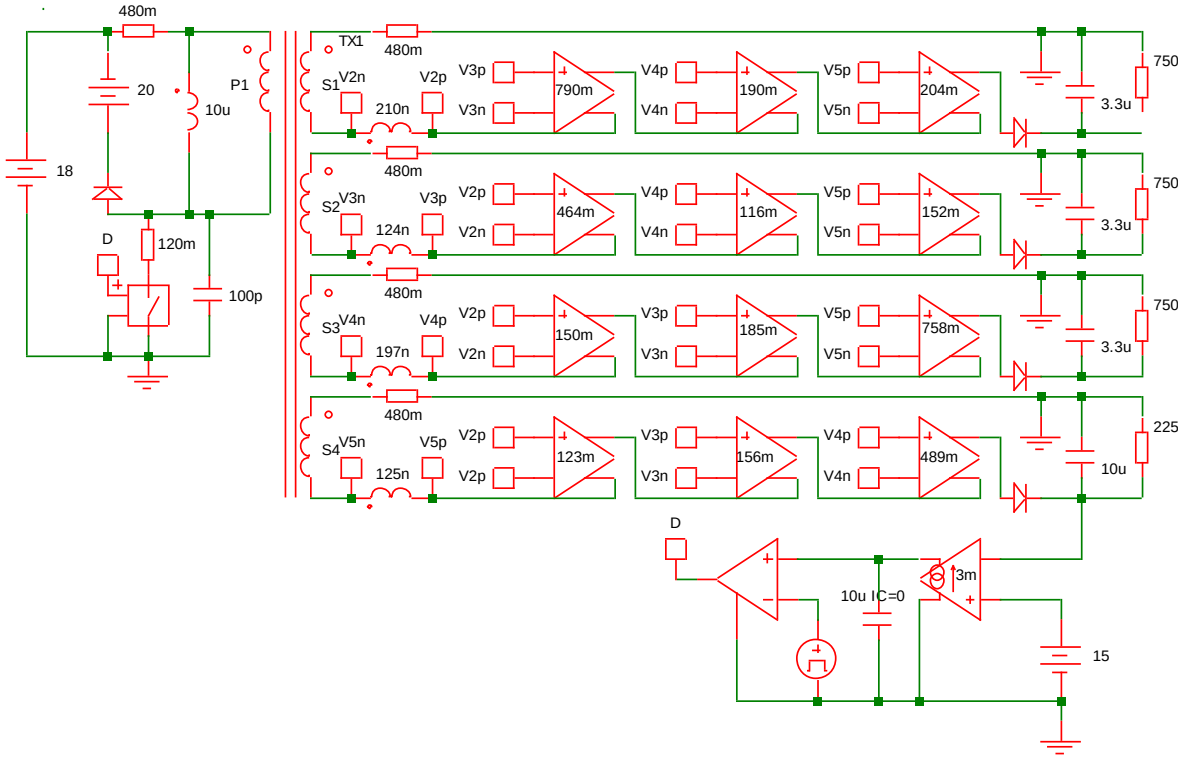
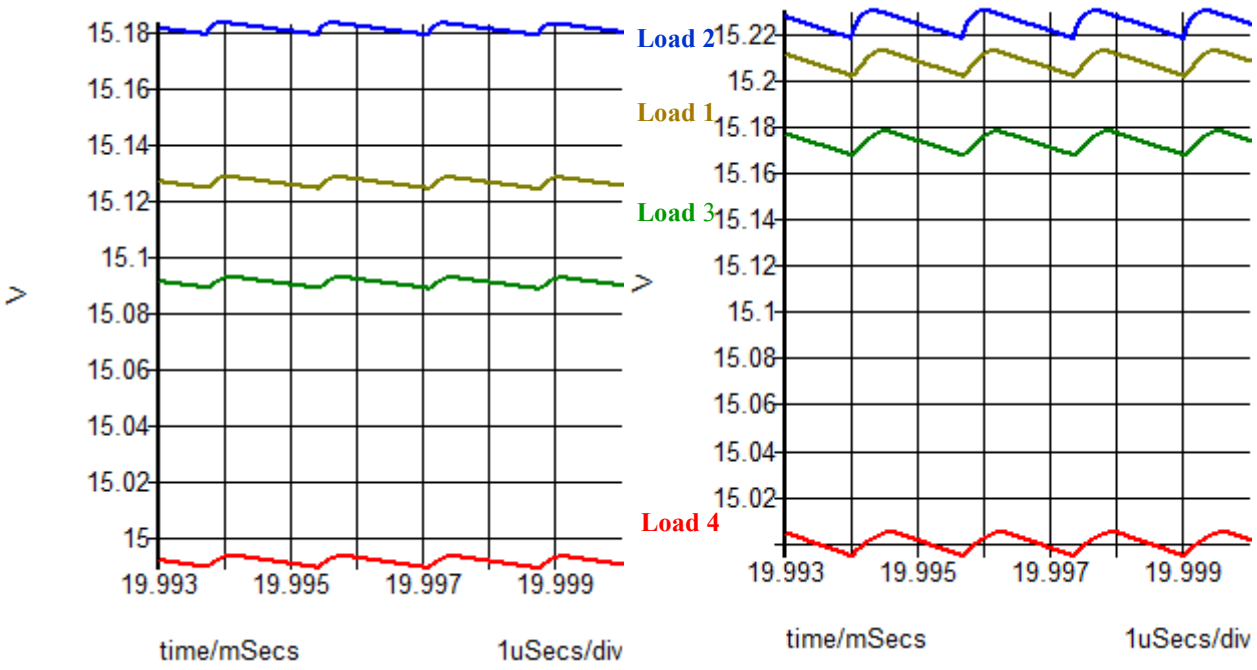
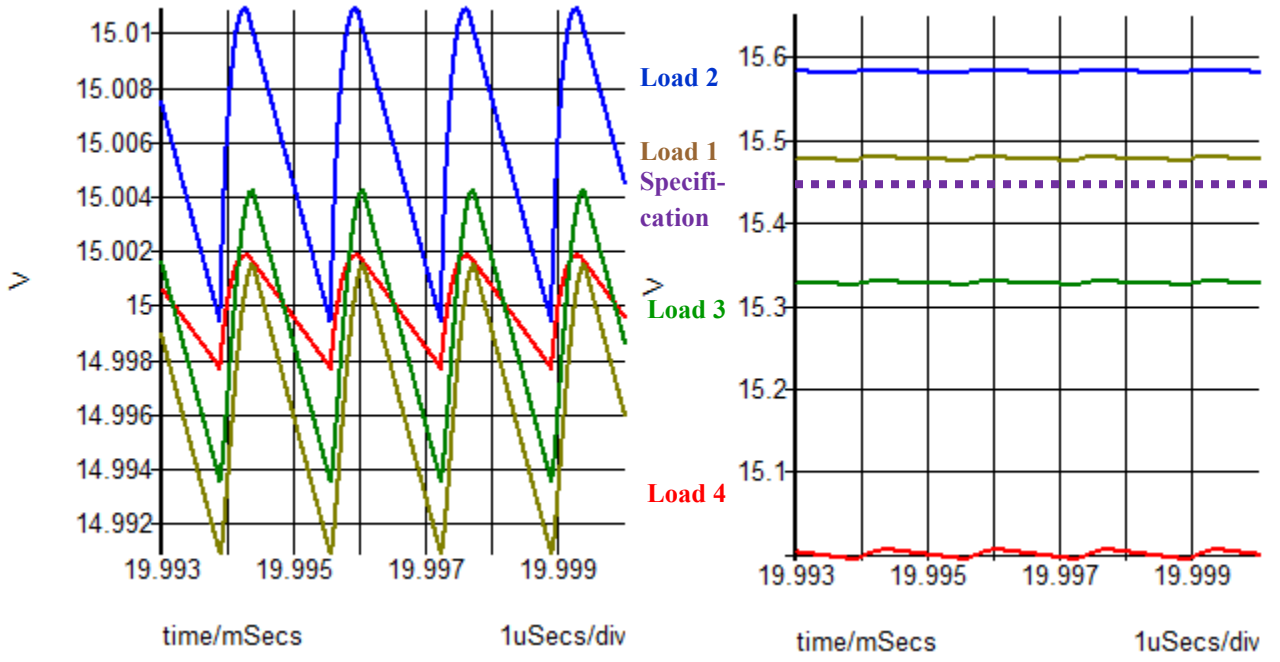


Figure A.2 Schematic diagram of flyback converter with cross-regulation effect in Simplis

The flyback converter has been simulated as in Figure A.2, where the cross-regulation effect is included and its parameters are from Maxwell simulation results and N-port model as discussed in Chapter 3. The simulation results are plotted in Figure A.3.



(Load1=Load2=Load3= 0.15 W, Load4=0.5 W) (Load1=Load2=Load3= 0.45 W, Load4=1.5 W)



(Load1=Load2=Load3= 0.45 W, Load4=0.5 W) (Load1=Load2=Load3= 0.15 W, Load4=1.5 W)

Figure A.3 Simulation results of flyback converter under various loads

In reference to Figure A.3, the worst case happens when load 4 is 1.5 W while 0.15 W for all other loads. Under this condition, the maximum voltage will be seen on port 2 at 15.58 V, which is out of the specification requirement by 54%. This scenario is caused by the cross-regulation effect from port 4, which is operating at maximum output current. It is noticeable, when the winding cross-regulation inductance is changed to smaller value, this output voltage error will drop. However, this is difficult to minimize in real transformer design. Moreover, when replaced with a larger core with larger winding numbers, this cross-regulation effect is inevitable to increase by large, since these will result in larger leakage inductance. Therefore, it will be agonizing to improve the flyback converter.

Table A.4 Loss of flyback converter under various conditions

Load Power (W)	Input Voltage (V)	Loss in Simulation, Except Core Loss (W)	I_{max} (A)	B_{max} (T)	Core Loss (W)	Total Loss (W)	Efficiency
0.95	12	0.050	0.58	0.12	0.50	0.550	67.8%
	15	0.040	0.57	0.12	0.50	0.540	66.0%
	18	0.054	0.58	0.12	0.50	0.554	61.7%
2.85	12	0.33	1.00	0.21	1.2	1.53	65.1%
	15	0.30	1.01	0.21	1.2	1.50	65.5%
	18	0.15	1.03	0.21	1.2	1.45	66.3%

Under the no-load condition, simulation results show the output voltage for all output will be 20.3 V, which is the same to clamp voltage plus the diode forward voltage. This could be explained from Figure A.1. When the switch turns off, the leakage current forces the clamp diode to turn on and the secondary side voltage equates to the primary side voltage, which is the sum of the clamp voltage and the diode forward voltage.

The loss is analyzed and listed in Table A.4. The total converter loss breaks down into two parts device loss and core loss. In that, the device loss is calculated by the simulation, while the core loss is estimated by the peak current. The results show the converter will work at around a 65% efficiency.

A.3 Comparison between Flyback and Boost Full-Bridge Converters

To compare the flyback with boost full-bridge converter fairly, in the comparison the full-bridge switches are replaced with the same switch used in flyback converter, whose on resistance is $0.12\ \Omega$. The comparison on efficiency and output voltage error, under normal input voltage, i.e., 15 V, is listed in Table A.5. The loss is estimated from the sum of simulation loss and core loss. The worst output voltage error is the largest one of output voltage error in four outputs under all possible load combinations through simulation. In Table A.6, the cross-regulation effects in flyback are compared with boost full-bridge converter, where the two worst outputs are listed for each topology. It is obvious that the cross-regulation effect in flyback converter is more severe than in boost full-bridge converter.

Table A.5 Comparison of flyback and boost full-bridge converter

	Flyback Converter	Boost Full-Bridge Converter
Efficiency (at 0.95 W load)	66.0%	70.4%
Efficiency (at 2.85 W load)	65.5%	84.3%
Worst Output Voltage Error (V)	0.58	0.12
Output Voltage Percentage Error	3.9%	0.8%

Table A.6 Comparison on cross-regulation effects between flyback and boost full-bridge converter

I_o (A)	*Flyback*				*Boost full-bridge*			
	I_{o2}		I_{o4}		I_{o3}		I_{o4}	
ΔV_o (mV)	0.01 A	0.03 A	0.033 A	0.1 A	0.01 A	0.03 A	0.033 A	0.1A
V_{o1}-$V_{o1\text{-}normal}$	22 mV	-17 mV	-145 mV	127 mV	12 mV	-9 mV	0.5 mV	-7 mV
V_{o2}-$V_{o2\text{-}normal}$	160 mV	-75 mV	-152 mV	132 mV	11 mV	-9 mV	0.4 mV	-7 mV
V_{o3}-$V_{o3\text{-}normal}$	8 mV	-5 mV	-117 mV	100 mV	37 mV	-29 mV	0.3 mV	-7 mV
V_{o4}-$V_{o4\text{-}normal}$	0	0	0	0	1 mV	-0.5 mV	90 mV	-82 mV

1. The core size in flyback converter should be larger than the one in full-bridge converter, otherwise a much larger core loss will be seen. This is discussed extensively in section 1.

2. The flyback converter suffers from cross-regulation effect much more severe than boost full-bridge converter. In flyback converter, the output voltages fly out of specification by 54 %, under worst case. This is majorly caused by cross-regulation effect between load 4 and load 1, 2, and 3. However, this effect will not been seen in the boost full-bridge converter, where group 1 and group 2 do not charge at the same time. The major concern to attenuate this voltage error in flyback converter is to limit the leakage phenomenon in inductor, which is extremely hard to improve by a large factor. In order to decrease the voltage error in boost full-bridge converter, to decrease the drain-to-source voltage of full-bridge switch is much easier, considering the high-side at 2.28 Ω and low-side at 1.82 Ω.

3. The isolation feedback in flyback converter, i.e., the optocoupler, makes its size larger than boost full-bridge converter by 21%, as discussed in section 1. Smaller optocoupler will have a smaller isolation voltage, failing the system from the specification on 6 kV isolation voltage.

4. Under no-load condition, the output voltage will equates to clamp voltage, which might be dangerous to IGBT device. While the tested value for full-bridge converter is around 16 V.