

Analysis and Design of Phase Lock Loop Based Islanding Detection

Methods

Daniel Joseph Martin

Thesis submitted to the faculty of the Virginia Polytechnic Institute and
State University in partial fulfillment of the requirements for the degree of

Master of Science

In

Electrical Engineering

Jih-Sheng Lai

Kathleen Meehan

Wensong Yu

May 4, 2011

Blacksburg, VA

Keywords: Anti-islanding, distributed power generation, anti-islanding,
smart grid

Copyright 2011, Daniel Joseph Martin

Analysis and Design of Phase Lock Loop Based Islanding Detection

Methods

Daniel Joseph Martin

ABSTRACT

As distributed generation penetrates the electric power grid at higher power levels, grid interface issues with distributed generation must be addressed. The current power system consists of central power generators, while the future power system will include many more distributed resources. The centralized power generation system is controlled by utility operators, but many distributed resources will not be controlled by utility operators. Distributed generation must use smart control techniques for high reliability and ideal grid interface.

This thesis discusses the grid interface issue of anti-islanding. An electric island occurs when a circuit breaker in the electric power system trips. The distributed resource should disconnect from the electric grid for safety reasons. This thesis will give an overview of the possible methods. Each

method will be analyzed using the ability to detect under the non-detection zone and the economic feasibility of the method.

This thesis proposes two addition cases for analysis that exist in the electric power system: the effect of multiple methods in parallel in the non-detection zone and the possibility of a false trip caused by a load step. Multiple methods in parallel are possible because the islanding detection method is patentable, so each grid interface inverter company is likely to implement a different islanding detection method. The load step represents a load change when a load is switched on.

Acknowledgements

I would like to express my most sincere gratitude and appreciation to my advisor, Dr. Jason Lai, for his support and guidance for this work while at Virginia Tech. His valuable expertise, advices, and encouragements have been extremely useful in the completion of these studies.

I would like to thank Dr. Kathleen Meehan, Dr. Wensong Yu for serving as members of my committee, and for their interests, suggestions and kind supports for this work.

I would also like to thank the Future Energy Electronics Center (FEEC) colleagues, Mr. Chien- Liang Chen, Mr. Thomas LaBella, Mr. Chris Hutchens, Mr. Gary Kerr, Mr. Sung-Yeul Park, Mr. Rae- Young Kim, Ms. Junhong Zhang, Mr. Hidekazu Miwa, Mr. Young Hoon Cho, Mr. Pengwei Sun, Mr. Hao Qian, Mr. Brett Whitaker, Mr. Baifeng Chen, Mr. Zakariya Dalala, Mr. Ahmed Koran, Mr. Zidong Liu, , Mr. Ben York, Mr. Alex Kim, Mr. Hsin Wang, Mr. Cong Zheng, Mr. Bin Gu, Mr. Ms. Hongmei Wan, Ms. Zheng Zhao, and Mr. Zaka Ullah Zahid. My study and research were enjoyable and valuable experiences with their helpful discussions, great supports and friendship. My gratitude needs to go to the visiting scholars, Mr. Kuan-Hung Wu, Mr. Yen-Shin Lai, Mr. Yuang-Shung Lee, Mr. Yu-Bin Wang, Mr. Huang-Jen Chiu, Mr. Chuang Liu, Mr. Hong-Po Ma, and Mr.

Sano Kenichiro for their kindly suggestions and help on my research. I also want to give thanks to Department of Energy and Virginia Tech for the financial and technical supports of the projects.

Table of Contents

1	Introduction	1
2	Phase Lock Loop	7
3	Passive Method.....	11
4	Anti-Islanding Standard Test Method	14
5	Active Frequency Jump Method	17
6	Harmonic Injection Method	21
7	Enphase Method	24
8	Multiple Methods In Parallel.....	28
8.1	Frequency Jump and Harmonic Injection in Parallel at Different Power Levels	29
8.2	Frequency Jump and Harmonic Injection in Parallel at Equal Power Levels	33
8.3	Enphase Method in Parallel with Passive Method.....	36
9	Load Step.....	38
10	Power Line Communications	43
11	SCADA.....	46
12	Conclusion.....	47
13	Future Work.....	48
14	References	50

List of Figures

Fig. 1 DC/DC converter with DC/AC inverter cascaded	2
Fig. 2 DC/AC inverter	2
Fig. 3 AC/DC rectifier with DC/DC converter and a DC/AC inverter cascaded	2
Fig. 4 Example power system with circuit breakers and DGs	4
Fig. 5 Prototype circuits used for the experiments	6
Fig. 7 Simplified Phase Lock Loop	9
Fig. 8 Phase Lock Loop Bode Plot	10
Fig. 9 LCL filter and sensor locations	11
Fig. 10 IEEE 1547 voltage and frequency requirements	12
Fig. 12. Passive method in the non-detection zone	13
Fig. 13 IEEE 1547 Islanding detection test	14
Fig. 14 Anti-Islanding test turn on with $L=25.13\text{m}$, $C=280\text{u}$, $R=360$ with $9/6$ ohm resistor.....	15
Fig. 15 Anti-Islanding Test Turn on with $L=25.13\text{m}$, $C=280\text{u}$, $R=360$	16
Fig. 16 Anti-Islanding Test Turn on with $L=25.13\text{m}$, $C=281\text{u}$, $R=360$	17
Fig. 17 Frequency jump method diagram.....	17
Fig. 18 Grid current and output voltage before island forms	18
Fig. 19 Before and after islanding condition	19

Fig. 20	Before islanding condition	20
Fig. 21	After islanding condition.....	20
Fig. 22	Harmonic injection phase lock loop.....	21
Fig. 23	Harmonic injection simulation	22
Fig. 24	Harmonic injection before and after islanding condition.....	23
Fig. 25	Before islanding condition	23
Fig. 26	After islanding condition.....	24
Fig. 28	Enphase method before islanding condition	25
Fig. 29	Enphase method after islanding condition	26
Fig. 30	Enphase different islanding point with frequency measurement	28
Fig. 31	Parallel inverters with different islanding detection methods.....	29
Fig. 32	Frequency jump and harmonic injection method at different power levels	30
Fig. 35	Two methods in parallel after islanding	32
Fig. 36	Two methods in parallel at equal power	34
Fig. 38	Two methods in parallel before islanding	35
Fig. 39	Two methods in parallel after islanding	36
Fig. 41	Enphase and passive method in parallel.....	38
Fig. 42	Load step test setup	39
Fig. 43	Zoom in load step result	40

Fig. 44 Load step results	40
Fig. 45 Phase Lock Loop Load Step Simulation	41
Fig. 46 Phase Lock Loop High Power Load Step Simulation.....	42
Fig. 47 Test setup of the load step test.....	43
Fig. 48 Current phase change at load step	43
Fig. 49 Transmission line Bode plot.....	45
Fig. 50 Power line communications before 1 km and after 1 km transmission line	46

1 Introduction

Distributed generation for renewable energy sources is penetrating the electric power system due to the rising cost of traditional energy sources and the environmentally friendly features of renewable energy. Over 60 countries around the world have set targets for renewable energy supply [1]. The types of renewable energy include solar, wind, hydrogen, biomass, geothermal, hydropower, and biodiesel. Many of these renewable energy sources are designed to supply energy into the electric power system.

For renewable energy, the interface between the energy source and the electric grid is power electronics. If the sources are DC sources, the power electronics may be a configuration of a DC/DC converter and a DC/AC inverter (Fig. 1) or a single DC/AC inverter (Fig. 2). If the source is an AC source, the power electronics can be a combination of an AC/DC rectifier, a DC/DC converter, and a DC/AC inverter (Fig. 3).

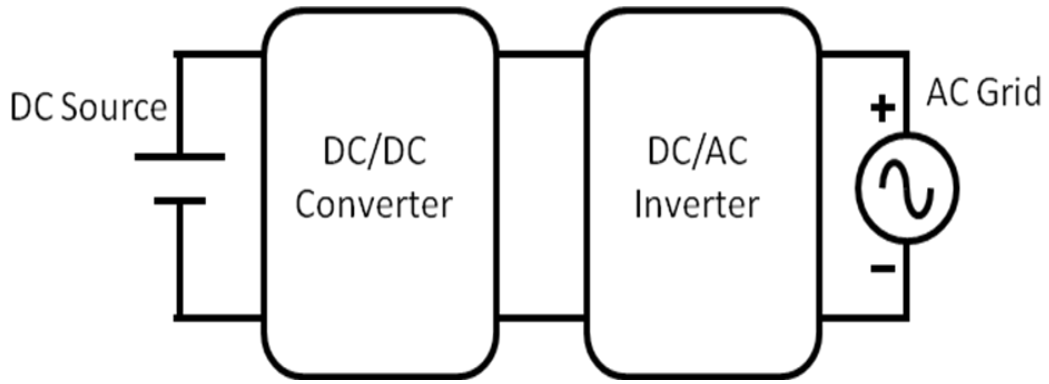


Fig. 1 DC/DC converter with DC/AC inverter cascaded

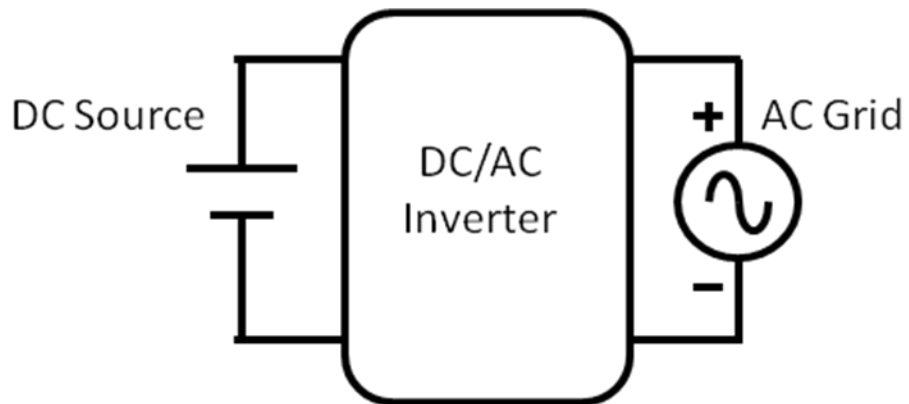


Fig. 2 DC/AC inverter

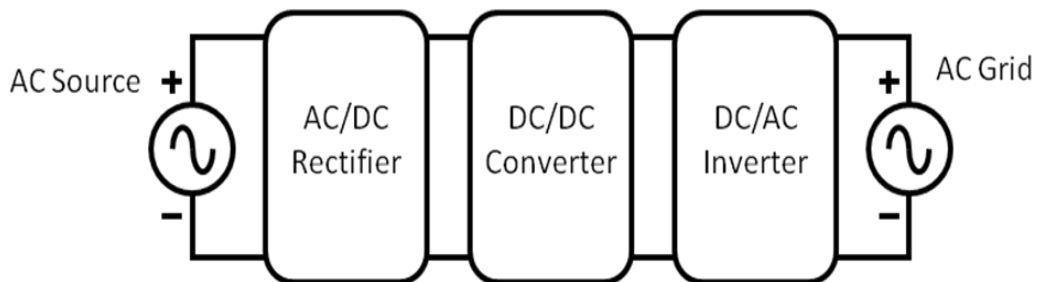


Fig. 3 AC/DC rectifier with DC/DC converter and a DC/AC inverter cascaded

Each power electronics interface should provide quality power to the electric grid for the loads. This means the harmonics should be low, the inverter should be turned off if the voltage or frequency goes out of range, and the inverter should be able to detect when the centralized generator is no longer connected; this case is called unintentional islanding. An island may occur for many reasons; such as, a disconnection for servicing, human error, an act of nature, or one of the circuit breakers in the power system trips as shown in Fig. 4 with distributed generation (DG). Under the island condition, the distributed resource (DR) is required to disconnect within 2 seconds according to IEEE 1547[2]-[3]. A distributed resource should disconnect from the electric grid for many reasons: to prevent the electric power grid from reconnecting with the distributed resource out of phase causing a large spike in voltage damaging the loads, a line worker could get hurt, and the utility is liable for power lines even when distributed resources use them to transmit power. In the future, the distributed resource may switch operation to a properly controlled island mode or microgrid operation when an island is detected [4]-[9].

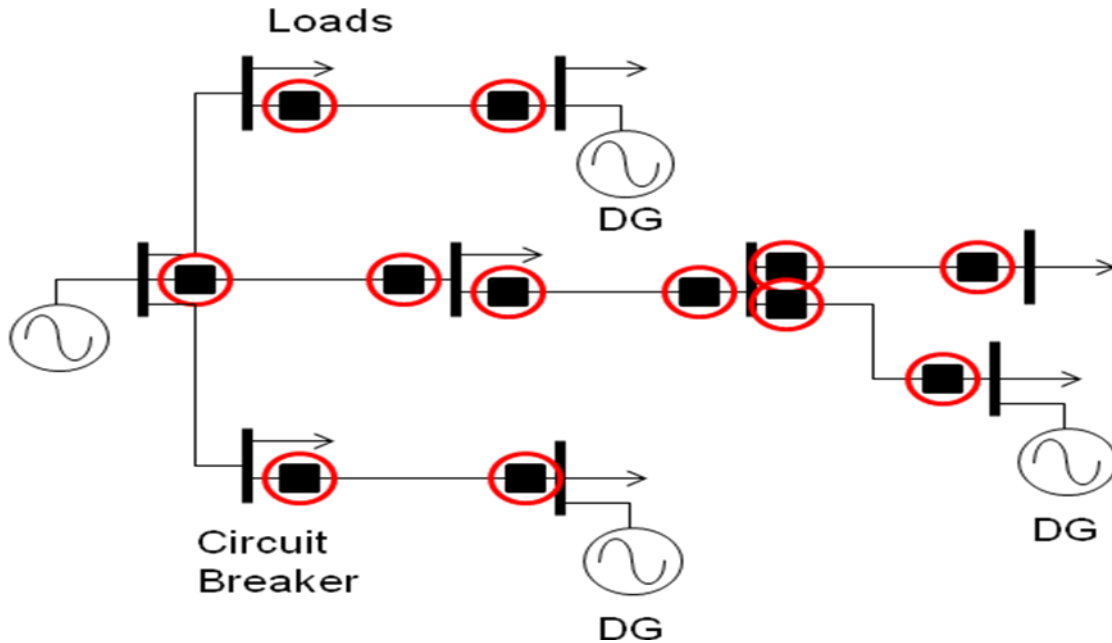


Fig. 4 Example power system with circuit breakers and DGs

As the distributed generation penetration gets higher, many problems have been identified on how to effectively transition from the centrally controlled electric power system (EPS) to a distributed system with many electric sources controlled separately. The problem this paper discusses is the scenario where the EPS is lost and an electric power island is formed.

There are many methods in literature to detect an island [10]-[32]. Change in frequency, change in voltage, change of impedance, harmonic injection, reactive power injection, phase shift, frequency jump, voltage shift, power line carrier communication, and supervisory control and data acquisition are a short list of possible methods. Passive methods detect a

change in the output to detect the connection of the grid. Active methods inject a disturbance to detect the connection of the grid. Hybrid methods are a combination of both. SCADA methods use communication to detect the loss of the grid.

Each method has its strengths and weaknesses. Typically methods are evaluated by three considerations: the non-detection zone, cost, and power quality [33]-[35]. This paper proposes two additional considerations: the anti-islanding method should not cause false trips caused by turning on or off local loads and the method should be able to detect even with multiple methods in parallel within the non-detection zone. Any method could possibly have issues with false trips and not detecting an island when there are multiple methods in parallel. This thesis suggests these conditions be considered in the islanding detection design.

Three methods are simulated and tested on a prototype power conditioner with a DC-DC converter [36] connected to an inverter [37] shown in Fig. 5. The $120 V_{\text{rms}}$ outlet is used as the grid.

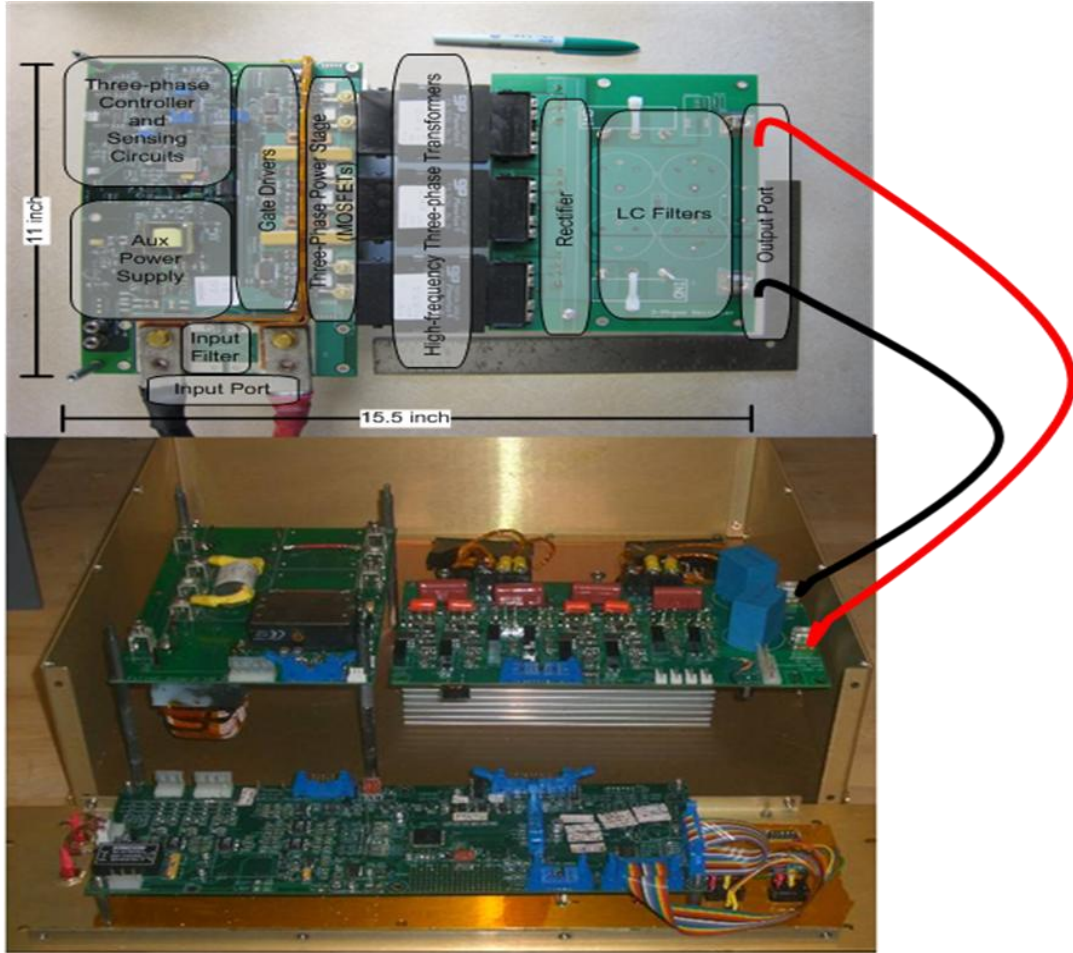


Fig. 5 Prototype circuits used for the experiments

One method is executed on a commercial unit. The method is simulated and tested using the information available on the patent [32]. The first case that can cause a method to be undetectable is the non-detection zone. Under this condition, the load within the island matches the power generated which means the current from the EPS goes to zero. This condition is found to be probable in [38]-[39]. The next condition is the parallel inverter case within the nondetection zone where multiple methods are used in the same island.

This is possible since there are many different DRs in the market that have patented their anti-islanding method. Lastly, the anti-islanding method should not cause a false trip when there is a load step from local loads. When local loads turn on and off, there is a change in voltage at the point of common coupling. Also, there will be a phase shift in the current due to the inductance and capacitance of the load turning on or off, and the control loops of the distributed resource will have a step response. These factors should not cause an undesired turn off of the distributed resources.

2 Phase Lock Loop

Each islanding detection method in this thesis uses the phase lock loop as the foundation for detecting [40]-[45]. Each active method perturbs the phase lock loop in order to detect an island. While the perturbation is non-ideal, it is necessary to detect the island. The phase lock loop is used to synchronize an oscillating waveform with a measured waveform. The measured waveform is from the point of common coupling of the inverter. The oscillating waveform is generated by the phase lock loop. The phase lock loop is comprised of a voltage controlled oscillator, an integrator, and a phase detector. A simplified phase lock loop structure is shown in Fig. 6. For the simplified phase lock loop to operate, the grid measurement must have a magnitude of one. The matrix equation shown in (1) is used to get the

magnitude of the grid voltage and multiply sin and cosine values for the phase lock loop to force the phase difference between the measured and oscillating waveforms. The signal at V_e is equivalent to the measured waveform (V_{grid}) multiplied by the phase lock loop output (V_f) shown in (2). Where θ_1 is the angle of V_{grid} and θ_2 is the angle of V_f . The purpose of the loop is to make the measured waveform equivalent to the reference waveform or θ_1 equal to θ_2 .

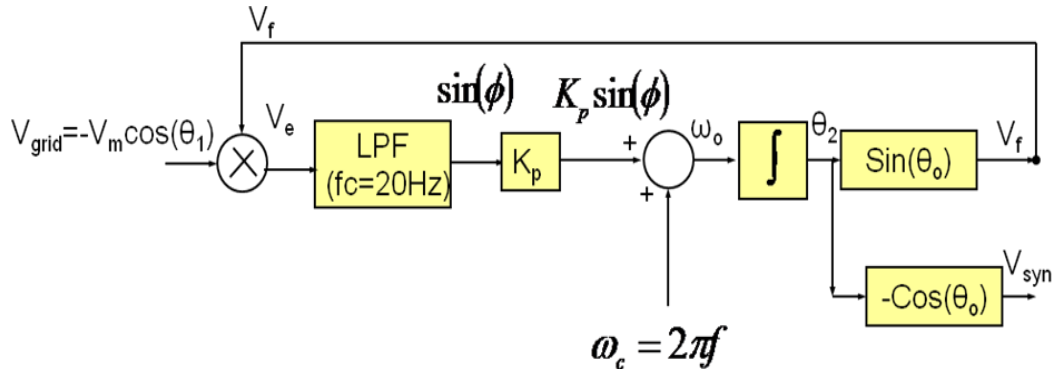


Fig. 6 Phase Lock Loop

$$\begin{bmatrix} -\cos \theta_2 & \sin \theta_2 \\ -\sin \theta_2 & \cos \theta_2 \end{bmatrix} \begin{bmatrix} V_{grid} = -V_m \cos \theta_1 \\ \frac{\omega_1 - s}{\omega_1 + s} V_{grid} = V_m \sin \theta_1 \end{bmatrix} \approx \begin{bmatrix} V_d = V_m \\ V_q = 2V_m \sin \theta_1 \cos \theta_2 \end{bmatrix} \text{ as } \theta_1 = \theta_2 \quad (1)$$

$$V_e = V_q / V_d = 2 \cos \theta_1 \sin \theta_2 = \sin(\theta_1 + \theta_2) + \sin(\theta_1 - \theta_2) \quad (2)$$

If $\theta_2 = \theta_1 + \phi$, then (2) can be rewritten as (3).

$$V_e = \sin(\theta_1 + \phi) + \sin(\theta_1) \quad \theta_1 = 2\pi 60 \quad (3)$$

The low pass filter (LPF) needs to be designed to significantly attenuate the 120 hertz signal so only $\sin(\phi)$ is left which at small values of ϕ is equivalent to just ϕ . After the low pass filter, the 120 hertz term will be filtered. The ϕ term, which is the difference between the two θ terms, will have a gain (K_p) and added to the expected angular frequency (ω_c). The gain of K_p is chosen for the maximum bandwidth and a sufficient step response. The integral of the new angular frequency (ω_o) is equal to (4). The integral constant is not necessary for this application.

$$\int \omega_o dt = \omega_o t = \theta_o \quad (4)$$

A simplified control loop of the phase lock loop is shown in Fig. 7. Sisotool in MATLAB is used to design the filter and compensator of the phase lock loop. The open loop Bode plot of the phase lock loop with the designed filter and compensator is given in Fig. 8. The cross over frequency is 27.8 hertz.

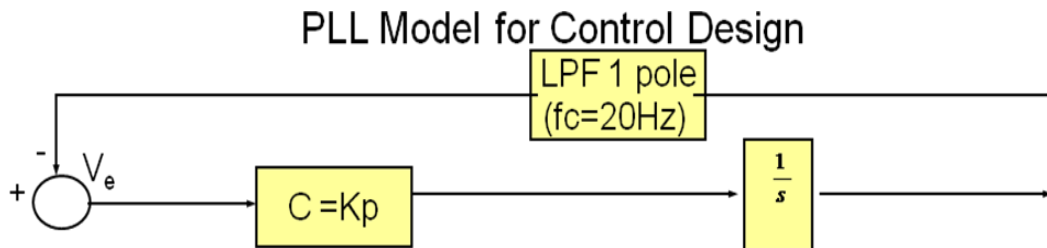


Fig. 7 Simplified Phase Lock Loop

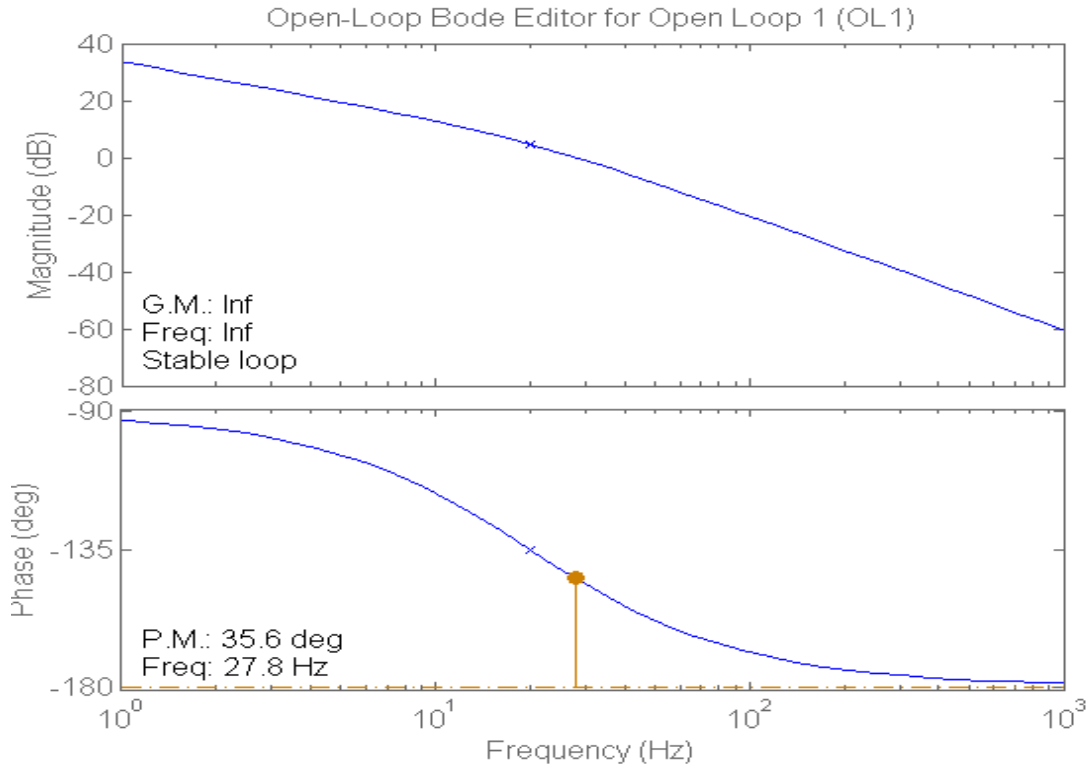


Fig. 8 Phase Lock Loop Bode Plot

The phase lock loop is important to meet the requirement to synchronize with the grid voltage and it allows smooth transitions between frequency, phase, and magnitude transients. The fact that the phase lock loop does not set the frequency, phase, or magnitude but follows the measured waveform is necessary for electric grid connection.

The inverter measures the grid voltage for the phase lock loop before an output filter inductor (L_g) in the LCL output filter as shown in Fig. 9. The grid line inductance is represented as L_s . The grid will naturally have noise due to electromagnetic interference, but an additional noise component will

be added because there is a difference between the actual grid voltage and the sensed grid voltage due to the output inductor filter. The experiments throughout this thesis will have noise in the grid current.

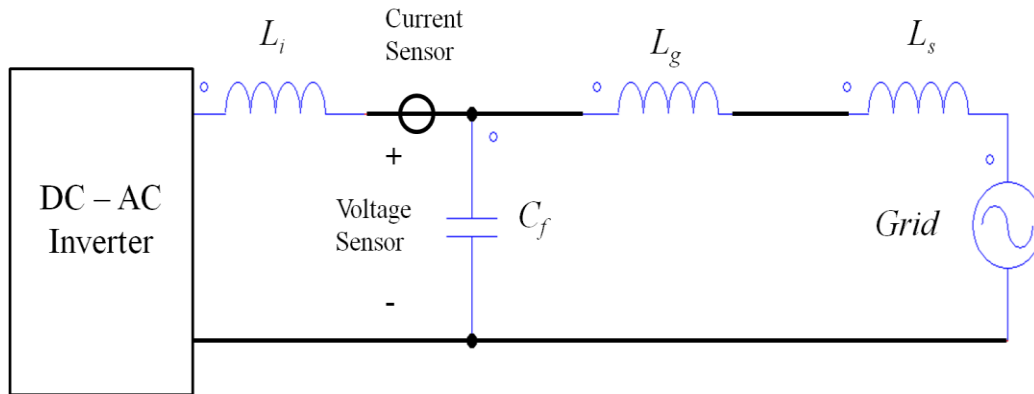


Fig. 9 LCL filter and sensor locations

3 Passive Method

The passive method uses the over/under voltage and over/under frequency requirements of the IEEE 1547 (Fig. 10) as the way to detect the island. The operating voltage range of the inverter is between 88% and 110% of the nominal voltage at the point of common coupling. The operating frequency range is 59.3 to 60.5 hertz. It is expected that in the future a low voltage ride through requirement will be added so the distributed generation will stay on to during a fault condition. Voltage ride through is used to prevent a blackout. The conditions outside the voltage and frequency range must disconnect within the clearing times shown. The reason for this requirement is that a low voltage condition could cause the

current draw on the loads to increase. A high current could damage the load.

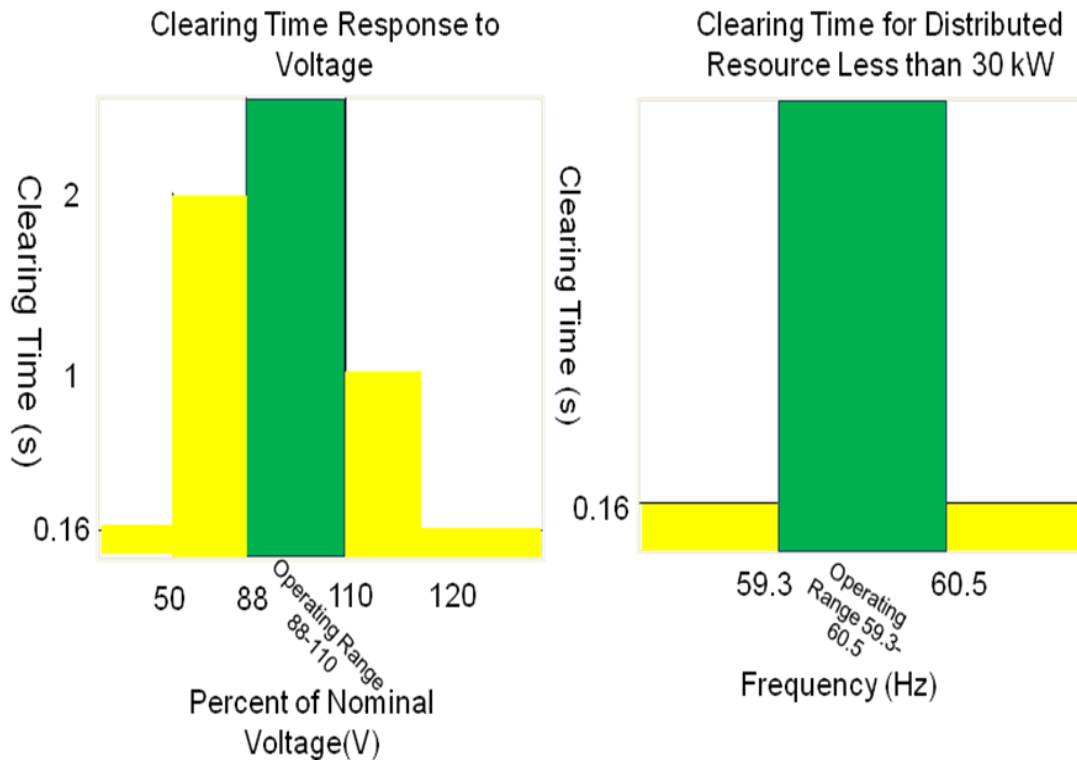


Fig. 10 IEEE 1547 voltage and frequency requirements

The non detection zone of this islanding detection method is tested. The non detection zone is the condition where the current from the grid to the local loads goes is small and the generation from the distributed generators match the local loads. The test setup is shown in Fig. 11. The current, I_{grid} , will go to zero which means the real power from the inverter is equal to the real power of the resistive load.

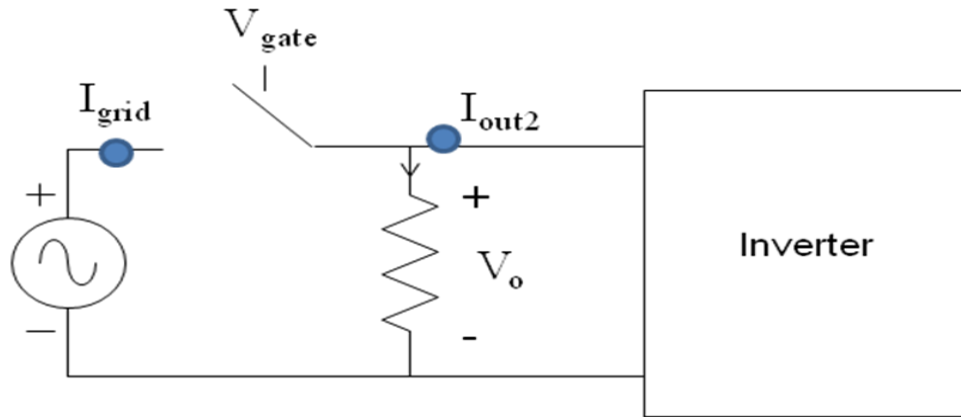


Fig. 11 Test setup for islanding tests

This method is tested in the non-detection zone in Fig. 12. Notice that the voltage, current, and frequency do not noticeably change when the island is formed.

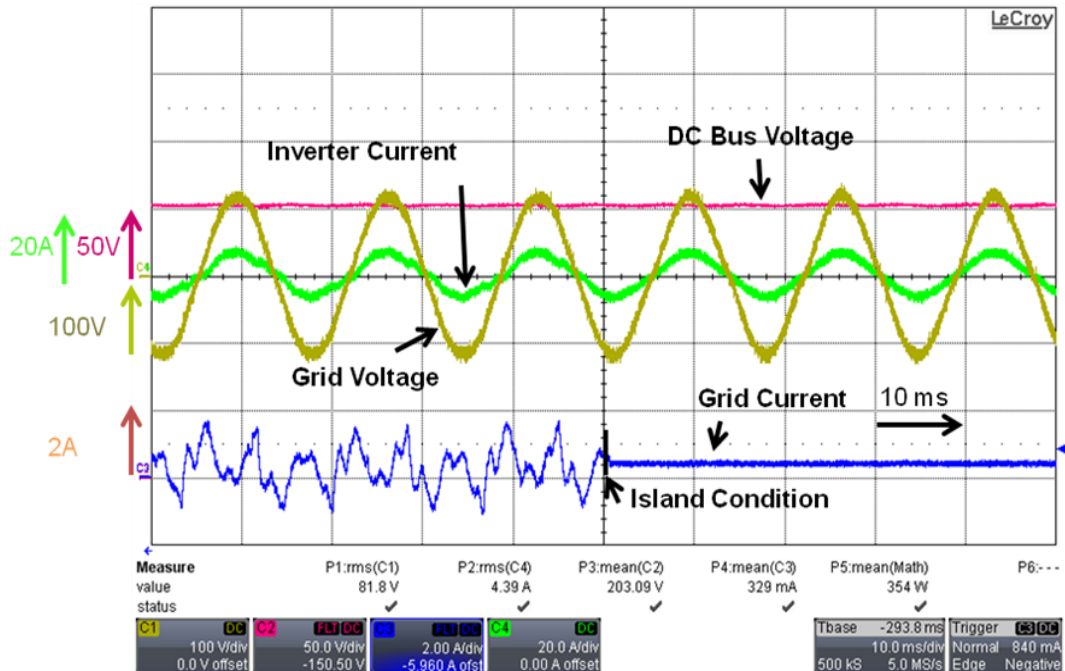


Fig. 12. Passive method in the non-detection zone

This method cannot be used because it will not meet the islanding detection requirements of the IEEE 1547 standard.

4 Anti-Islanding Standard Test Method

The test setup of the islanding detection test used to verify the islanding detection method for IEEE 1547 standard compliance is shown in Fig. 13. The purpose of this test is to have the current from the grid go to zero. Both the real power current and the reactive power current must go to zero. The resistor is chosen to match the real power from the inverter. The inductor and capacitor is chosen so that the inductive or capacitive output filter of the inverter will combine with the additional inductor and capacitor to resonate at a 60 hertz frequency (5).

$$f = \frac{1}{2\pi\sqrt{LC}} = 60\text{Hz} \quad (5)$$

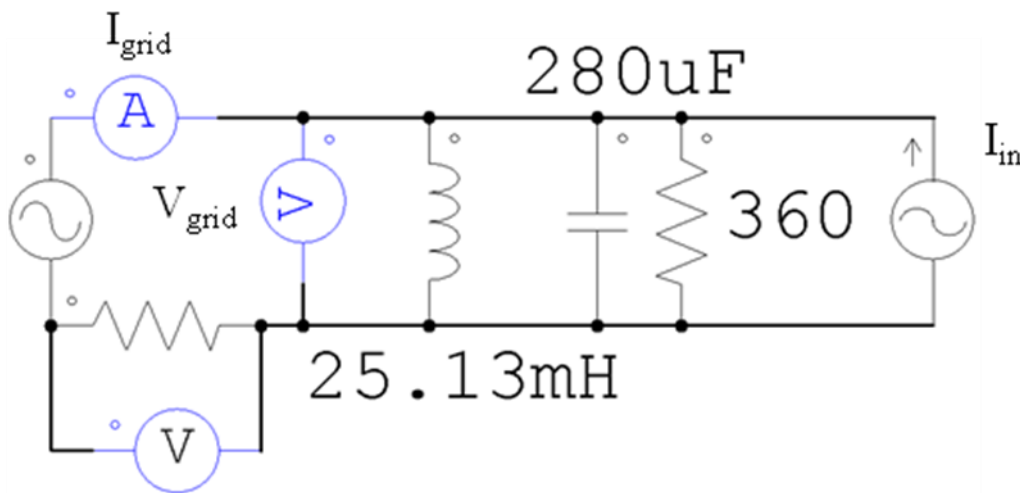


Fig. 13 IEEE 1547 Islanding detection test

Since the uncharged capacitor and inductor act as shorts before the grid is connected, the current will spike at turn on. This is shown in Fig. 14. Precautions should be made to prevent an excessive spike at turn on such as adding an addition resistor as shown in Fig. 13.

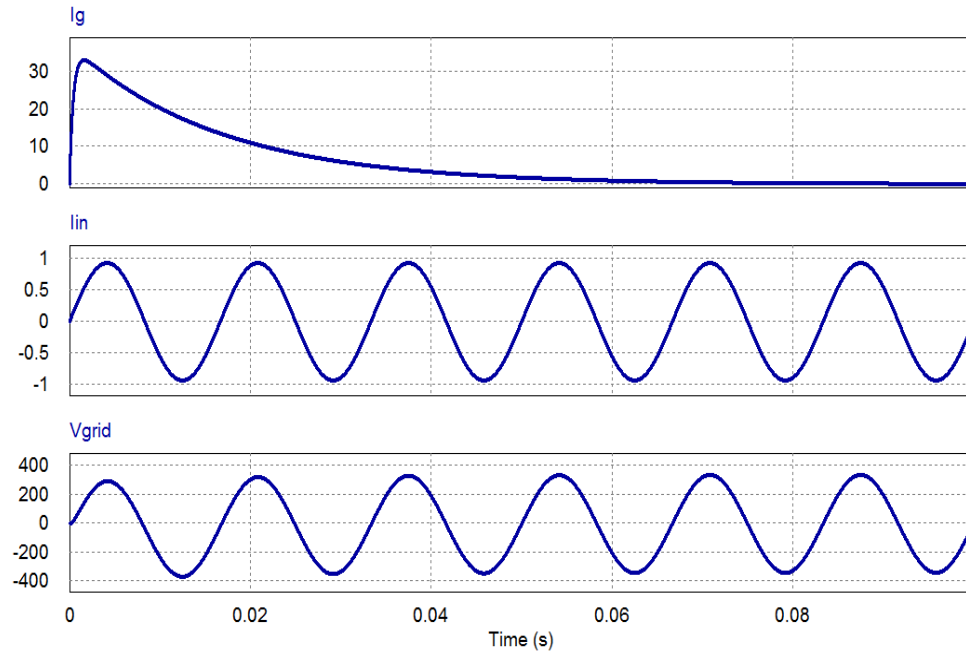


Fig. 14 Anti-Islanding test turn on with $L=25.13\text{m}$, $C=280\mu$, $R=360$ with $9/6$ ohm resistor

The test setup uses capacitors and inductors which will have a variation between the actual value in the experiment and the nominal value. Due to this difference there will be an effect on the actual resonant frequency of the test. A comparison is done where the capacitance is varied by 1 microfarad in Fig. 15 to Fig. 16. When the capacitance is increased by 1 microfarad, the

reactive current is increased 50 times. To properly set the capacitance, a variable capacitor should be used while measuring the grid current.

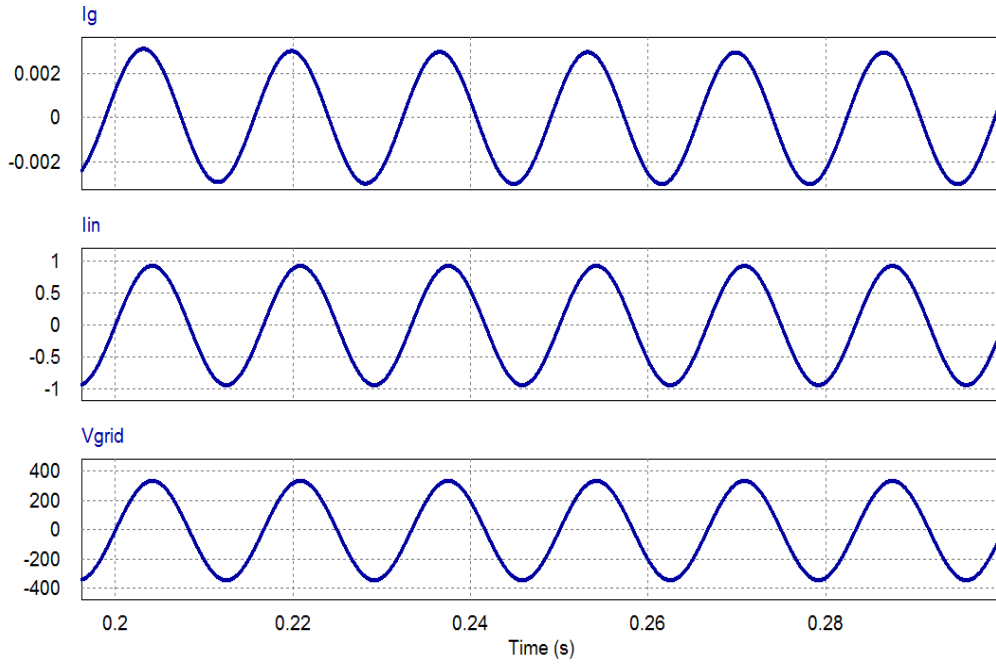


Fig. 15 Anti-Islanding Test Turn on with $L=25.13\text{m}$, $C=280\mu$, $R=360$

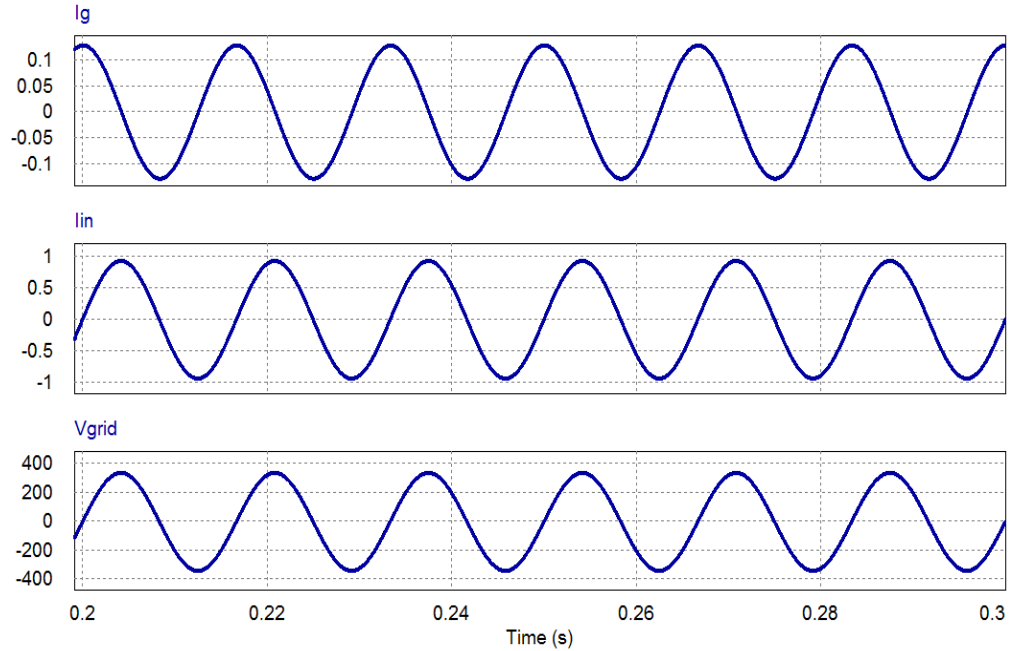


Fig. 16 Anti-Islanding Test Turn on with $L=25.13\text{m}$, $C=281\mu$, $R=360$

5 Active Frequency Jump Method

The frequency jump method adds an additional frequency to the phase lock loop (Fig. 17). The additional frequency used in this paper is 10 Hz.

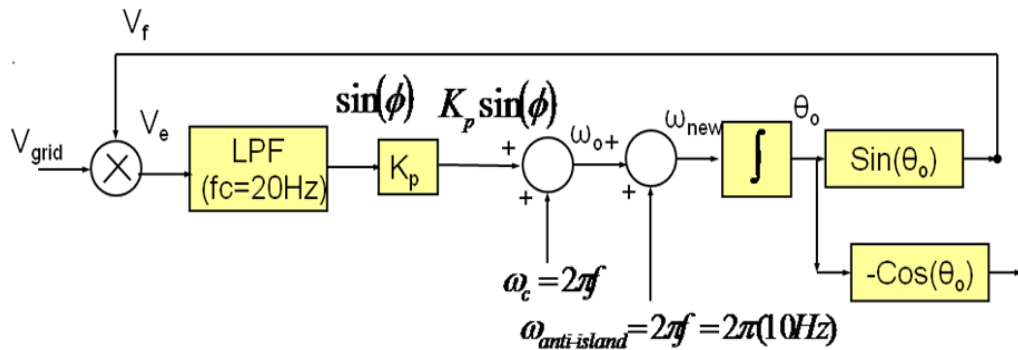


Fig. 17 Frequency jump method diagram

This method is simulated in PSim to verify detection ability. Fig. 18

shows the output voltage and grid current before and after an island is formed. The grid current is much smaller than the inverter current so the simulation is in the non-detection zone.

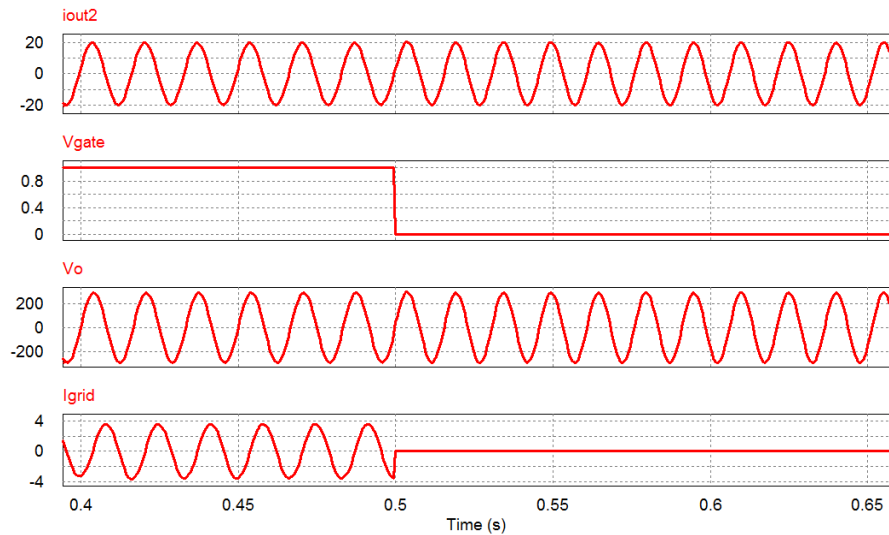


Fig. 18 Grid current and output voltage before island forms

After the island forms (Fig. 21), the frequency jumps to 67 Hz. Over time the frequency will go up to 70 Hz. This method is detectable in the non-detection zone.

The experimental results in Figs. 19-21 match the simulation results.

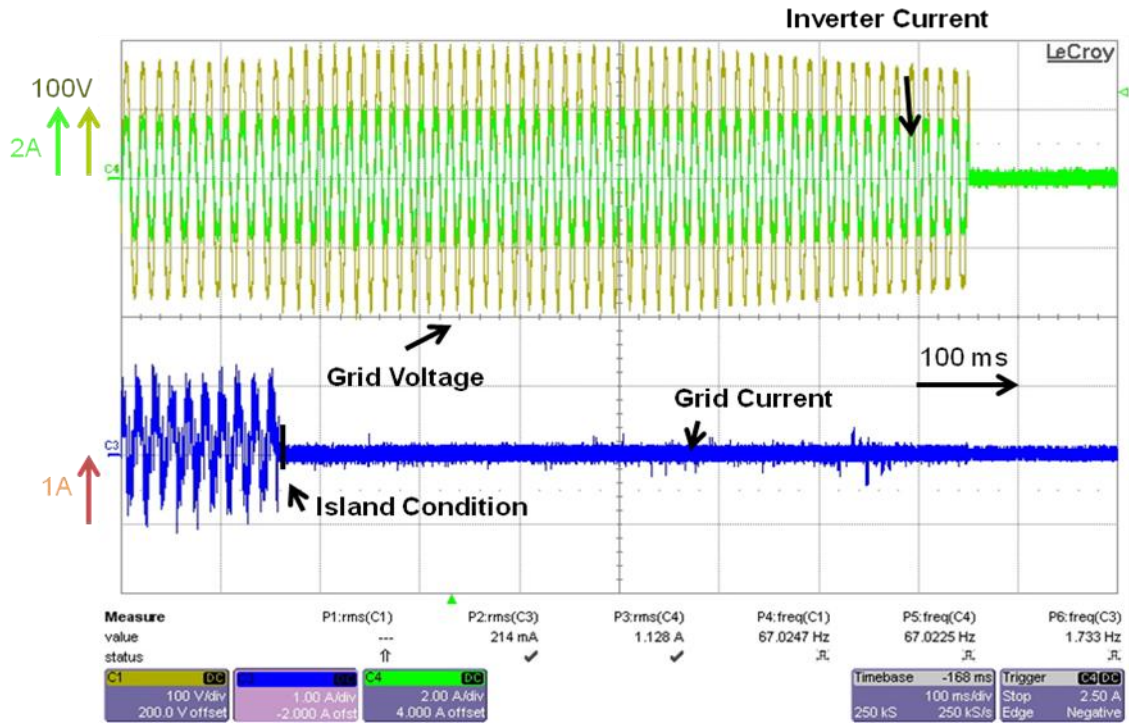


Fig. 19 Before and after islanding condition

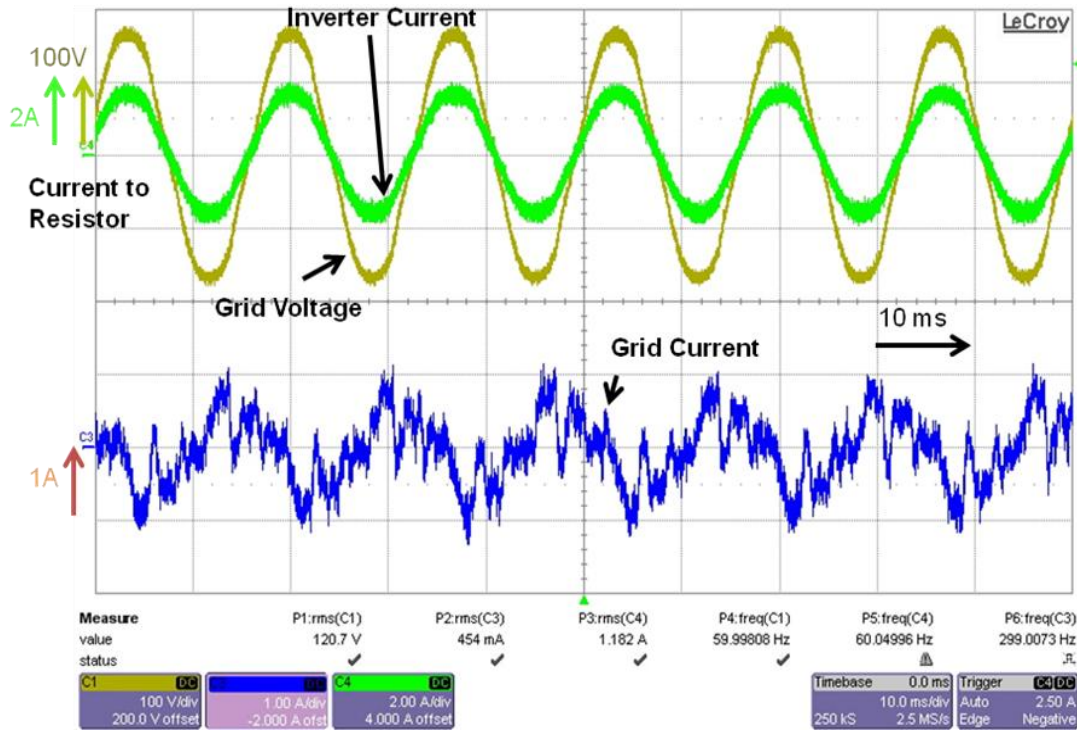


Fig. 20 Before islanding condition

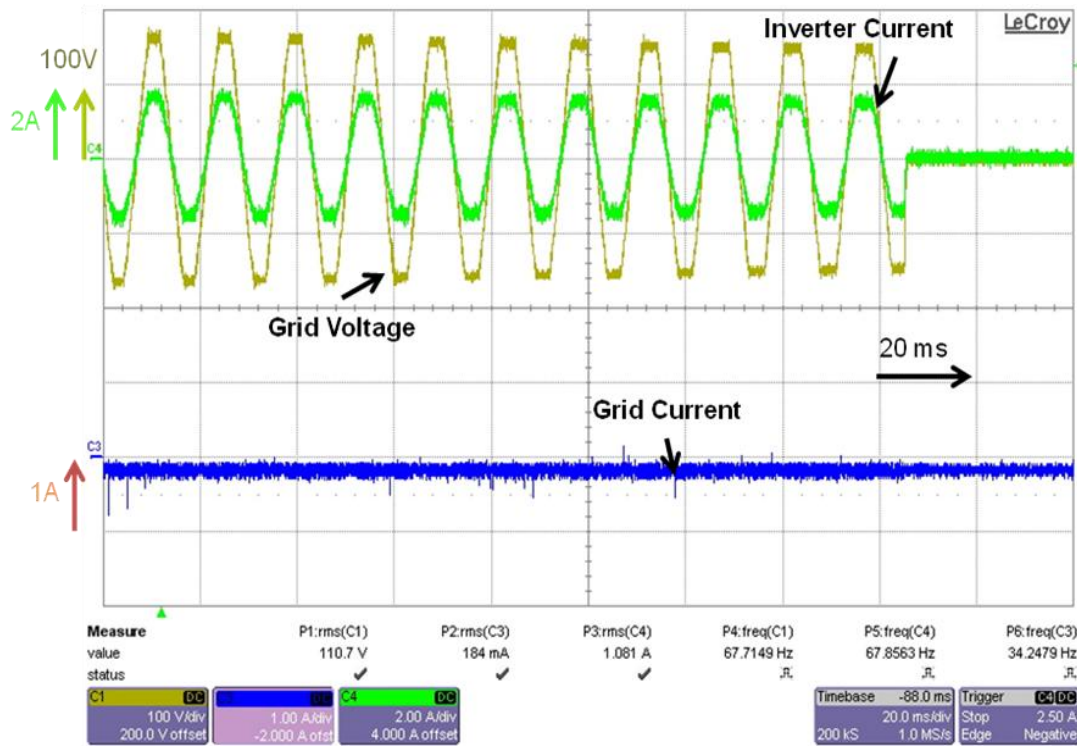


Fig. 21 After islanding condition

6 Harmonic Injection Method

The harmonic injection method perturbs the phase lock loop with a sine wave in addition to the original theta value [31]. The new phase lock loop output (V_f) is now (6) when V_{grid} 's magnitude is unity.

$$V_f = \sin \theta_o + K \sin \theta_o \tag{6}$$

If K is small, the cosine term will go to 1 and the sine term will go to K making this method similar to a second harmonic injection. The new phase lock loop is shown in Fig. 22.

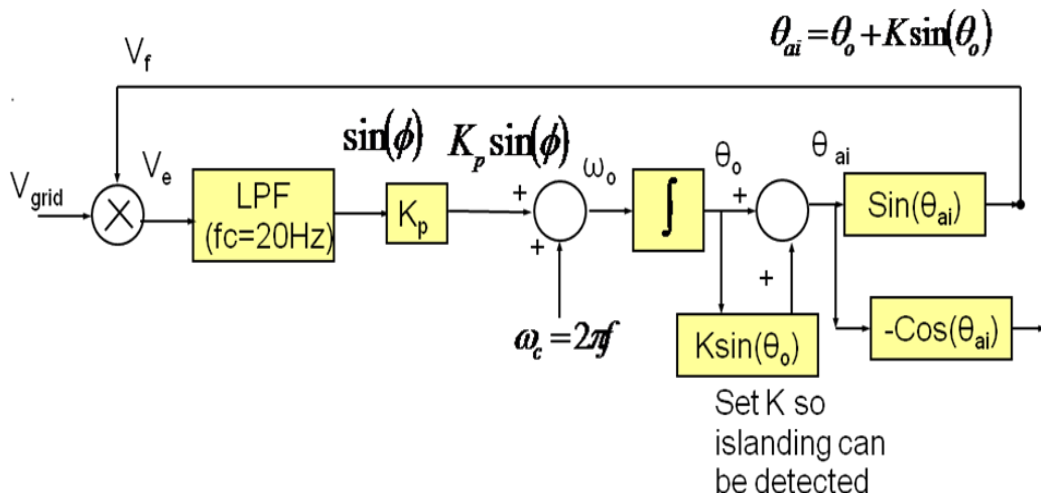


Fig. 22 Harmonic injection phase lock loop

The simulation result is shown in Fig. 23. The inverter current continuously injects a harmonic which is poor power quality. The grid current is a 120 hertz sine wave because the load current must follow Ohm's

law. When the inverter current and the grid current are added together, the load current is sixty hertz following Ohm's law and the grid voltage.

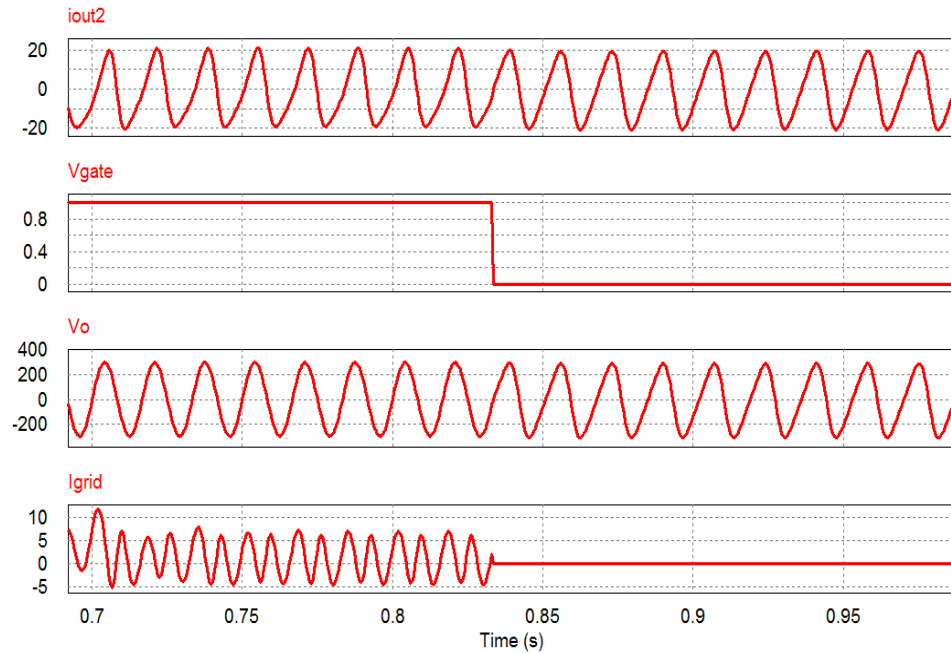


Fig. 23 Harmonic injection simulation

The experimental results verify the harmonic is noticeable in the output voltage for the single inverter case (Figs. 24-26). The inverter anti-islanding disconnect time can be adjusted for anytime less than 2 seconds. In this case, the inverter stays connected longer than the plot shows.

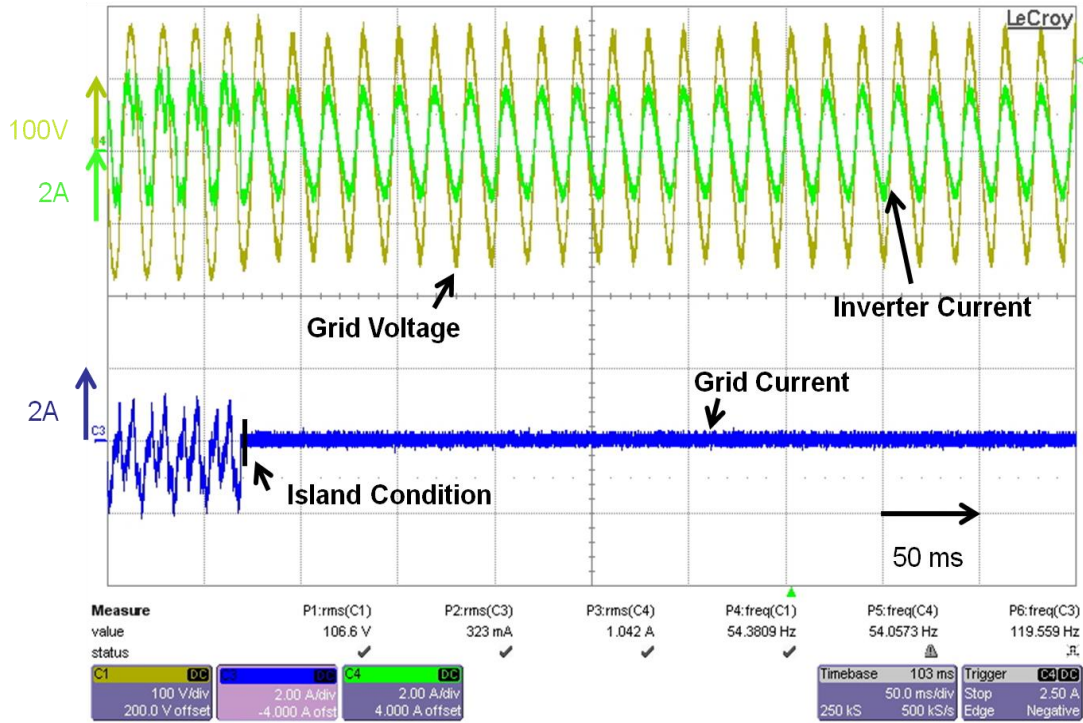


Fig. 24 Harmonic injection before and after islanding condition

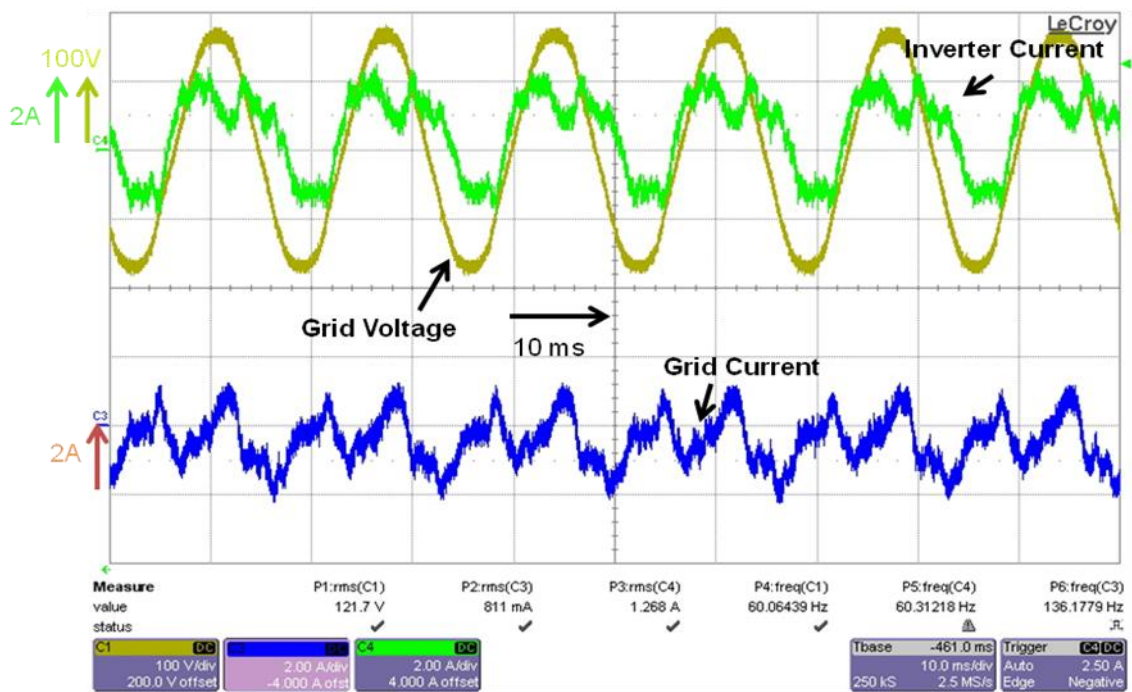


Fig. 25 Before islanding condition

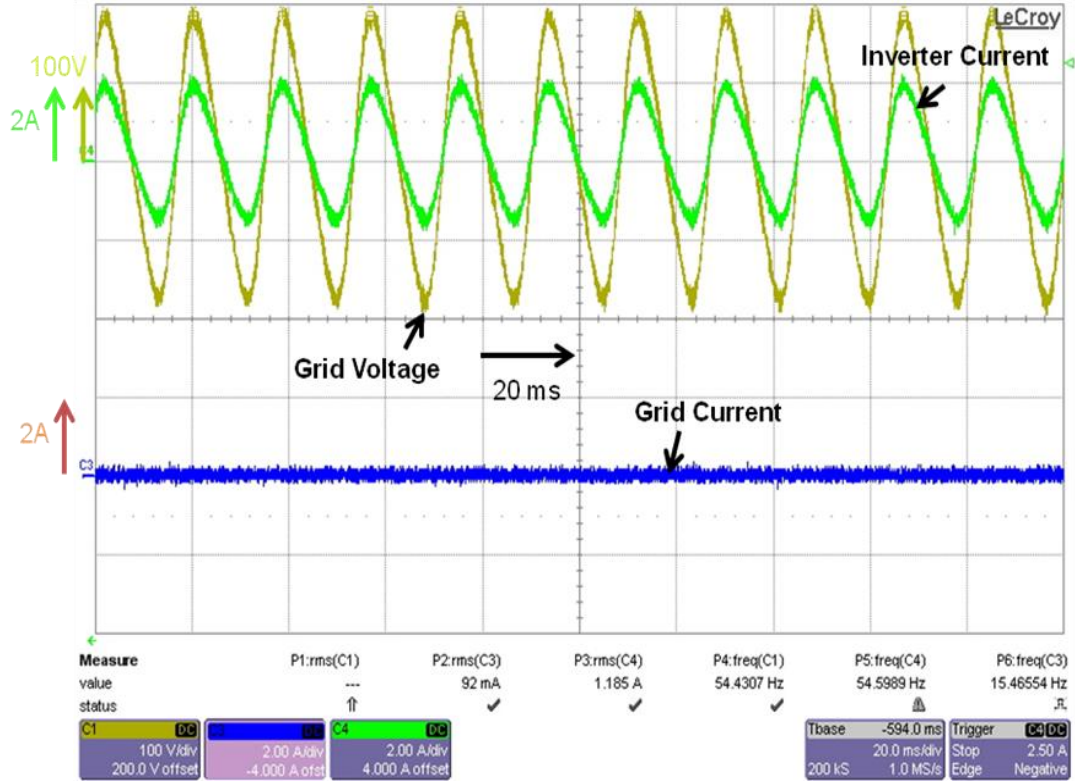


Fig. 26 After islanding condition

7 Enphase Method

A commercial inverter anti-islanding method is studied using its patent [32]. The Enphase micro-inverter uses a phase shift islanding detection method. The Enphase will phase shift every 0.5 seconds for a full cycle (Fig. 27). Instead of relying on a voltage change to detect an island, this method uses the fact that the phase lock loop error will be different when there is an island compared to when there is not an island. The signal at $\sin(\phi)$ is considered the error signal since it should be equal to 0 if the measured signal and the phase lock loop output are the same.

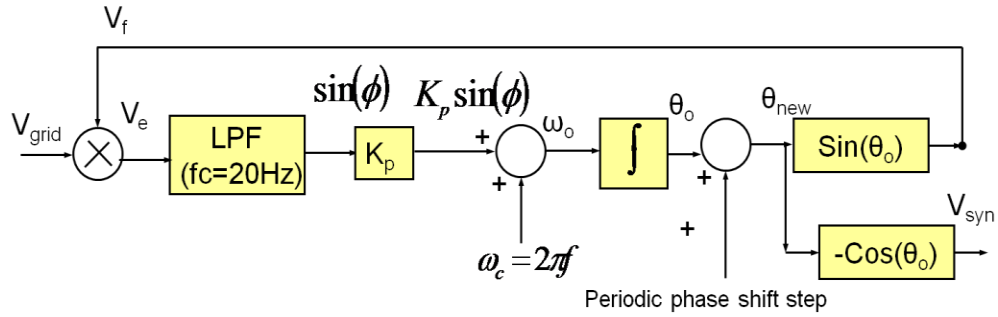


Fig. 27 Enphase method phase lock loop

The Enphase method is simulated for the grid connected case (Fig. 28). The Enphase error will increase an equal amount once the phase shift starts as it decreases after the phase shift is over. Notice that the $K_p \Delta \omega$ error is in the range of 0.02.

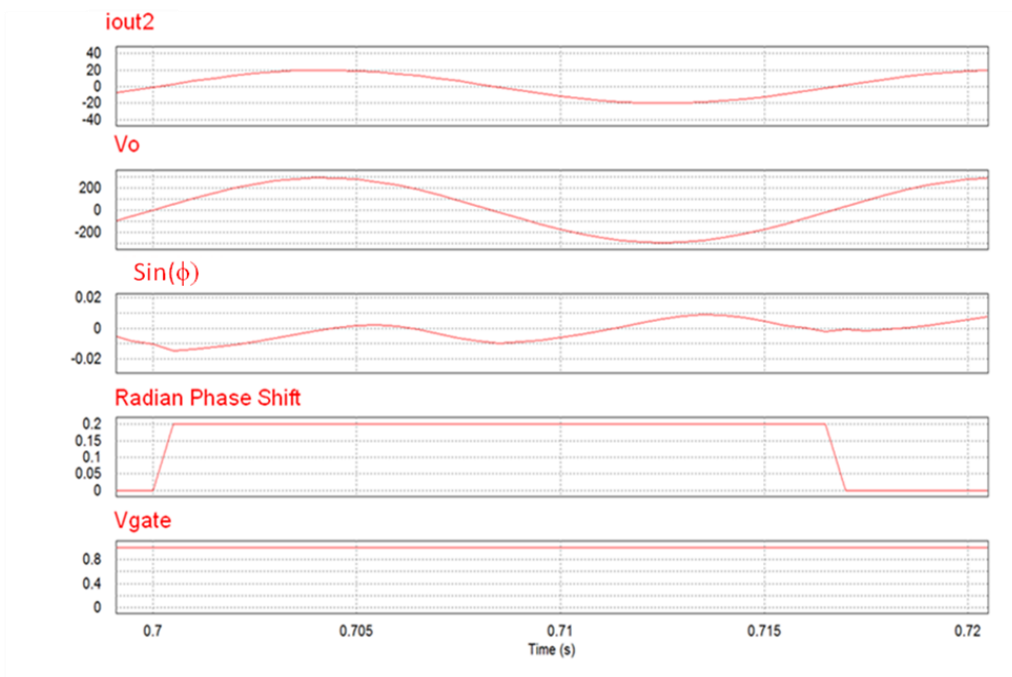


Fig. 28 Enphase method before islanding condition

After the islanding condition (Fig. 29), the error signal will decrease but will not increase above the steady state value. Which means the average value will not be 0 taken from the steady state offset value. The change the error makes is about 1 which is a very small value considering the gain K_p is 300.

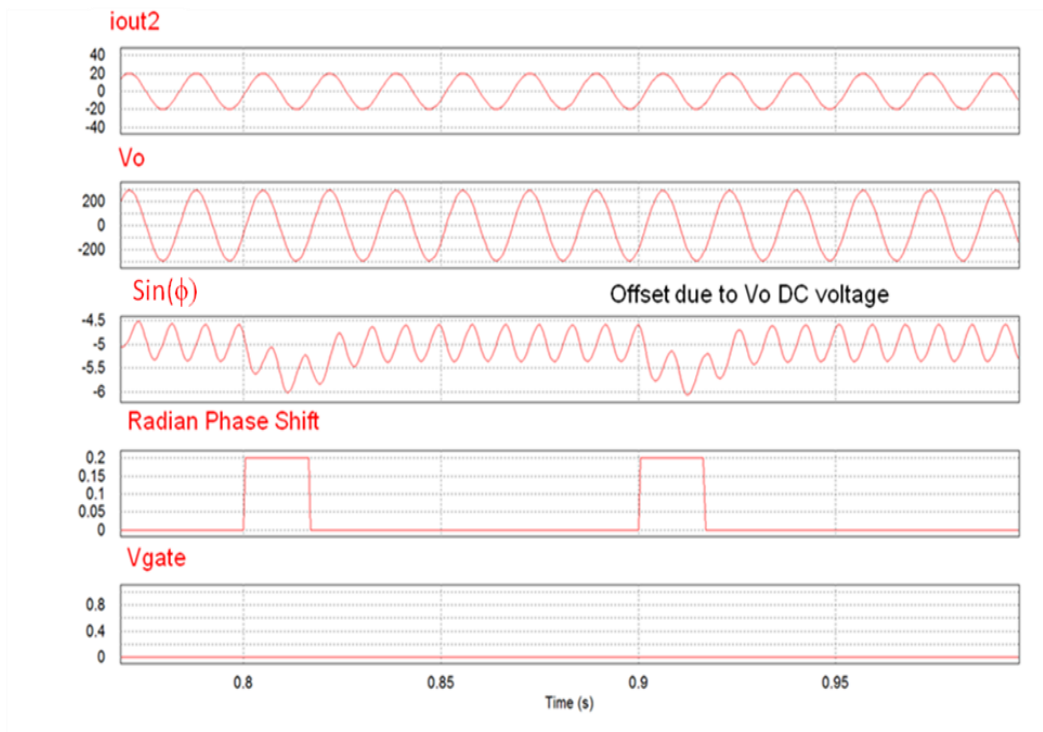


Fig. 29 Enphase method after islanding condition

Enphase will turn off at the zero crossing following the islanding condition. This is verified by repeating the experiment many times in the single inverter case Fig. 30. Switching at different times in the waveform still causes the inverter to detect at the next zero crossing. The islanding detection presented in the patent suggests that the islanding condition will

only be detected after the phase shift injection. Tests show this is not the case. It is noticed in Fig. 30 there is a phase shift after the island is formed causing the frequency between peaks to be 57.8Hz. Which means the Enphase method also detects a phase shift and switches off at the next zero crossing.

The phase shift is caused by the output capacitor of the Enphase. The Enphase is controlled after the capacitor to provide a power factor of 1 at the output; but, the capacitive reactive power is noticeable in the EPS current when the power output matches the local load. These tests were conducted with an 80W load and the supply current is adjusted so the power out is equal to 80W.

Another problem is that the EPS could come back within 2 seconds but the Enphase unit has already disconnected. If the inverter stayed connected for up to 2 seconds, the inverter could provide ride through support to the EPS. DRs that are more sensitive in disconnecting can cause problems to the EPS. This is a way this method could be improved.

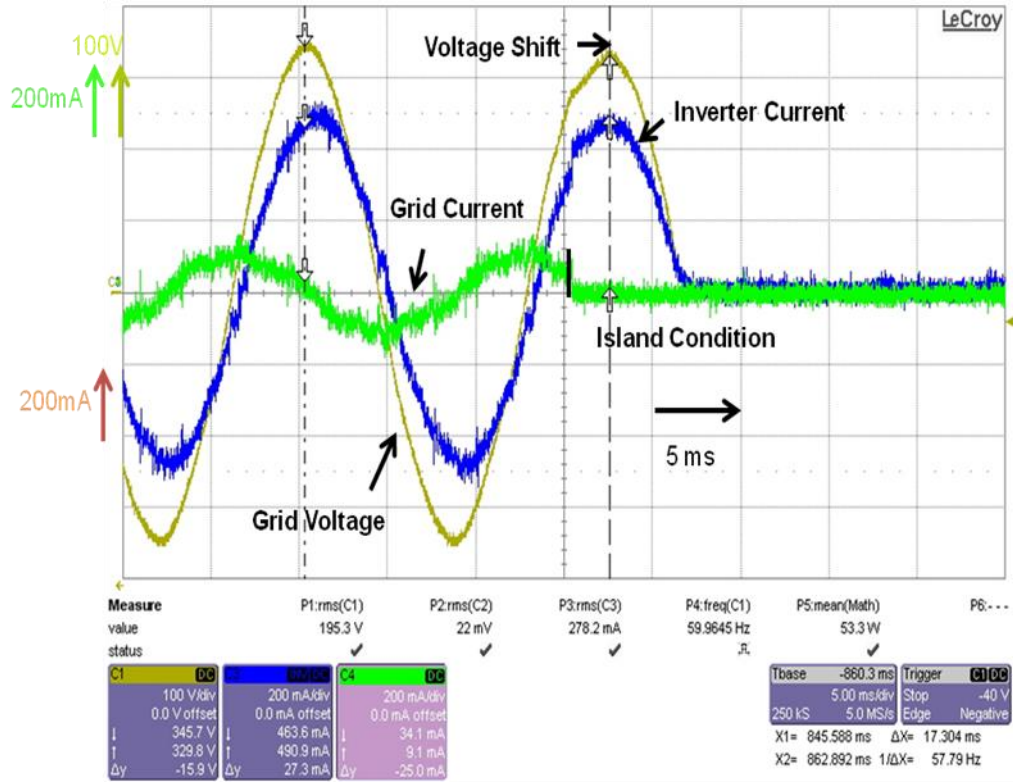


Fig. 30 Enphase different islanding point with frequency measurement

8 Multiple Methods In Parallel

As more DRs are used, it is likely multiple methods will be in parallel in an island so it is necessary to study how multiple methods operate in parallel [46]-[48]. It is possible to patent the islanding detection method which means each company is likely to use a different method for islanding detection. Two different methods are tested in parallel at the same power level and different power levels. The frequency jump method and harmonic injection method are simulated and tested in parallel using the configuration shown in Fig. 31.

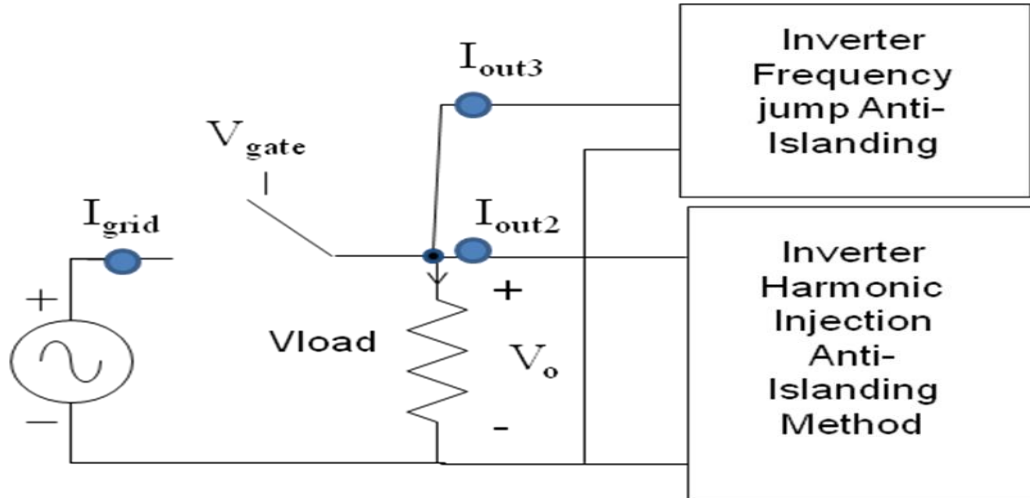


Fig. 31 Parallel inverters with different islanding detection methods

8.1 Frequency Jump and Harmonic Injection in Parallel at Different Power Levels

This case considers the scenario where the frequency jump method is at a much lower power level than the harmonic injection method. The frequency jump method has an 11 amp peak while the harmonic injection method has a 34 amp peak (Fig. 32). In this case, the frequency stays close to 60 Hz. The frequency jump method does not affect the output voltage enough to detect an island. Under this condition, first the harmonic injection method will disconnect then the frequency jump method can detect. The effect of the inverter current on the output voltage during the island condition can be related by (7), where Z is the impedance of the local load. In the case where there are multiple units in parallel in the non-detection zone, the current from each inverter will be lower to get the same voltage as the single inverter test that is currently considered in the IEEE 1547 standard.

Islanding detection methods measure the effect on the voltage from a perturbation from the current. When the current is less, the effect on the voltage will be less in the non-detection zone with multiple units in parallel.

$$V = IZ \tag{7}$$

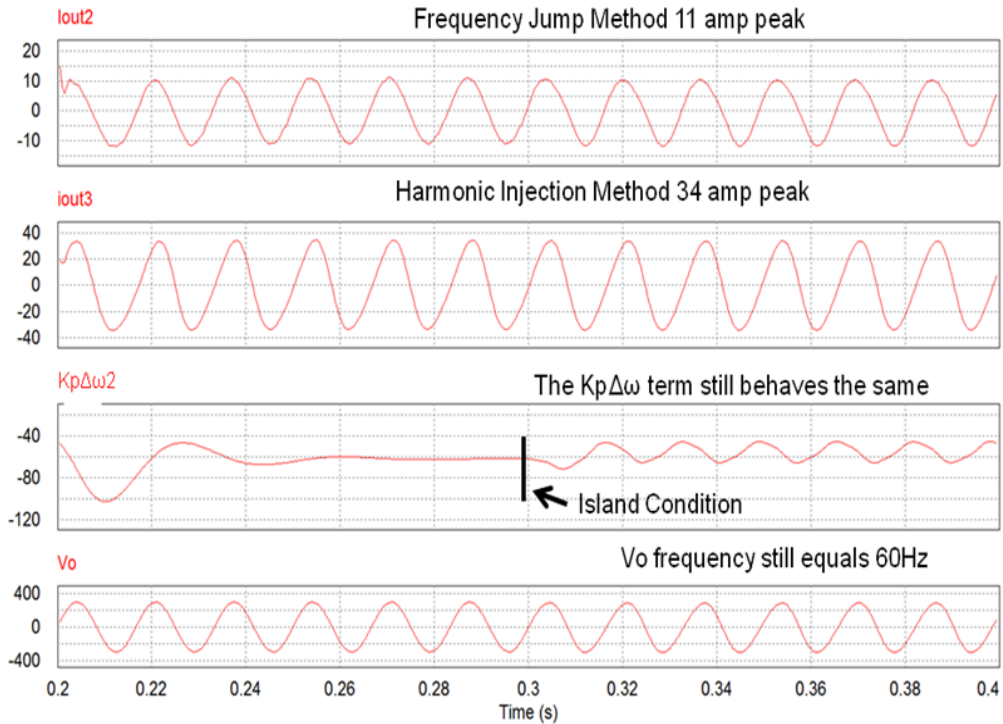


Fig. 32 Frequency jump and harmonic injection method at different power levels

Figs. 33-35 show the experimental results for multiple methods in parallel. Notice that the frequency increases to only 63.5 hertz when the single frequency jump inverter caused the frequency to jump to 67.8 hertz. The frequency jump is 3.5 hertz as opposed to 7.8 hertz. The jump is

approximately half which is expected since the current of the frequency jump method is half.

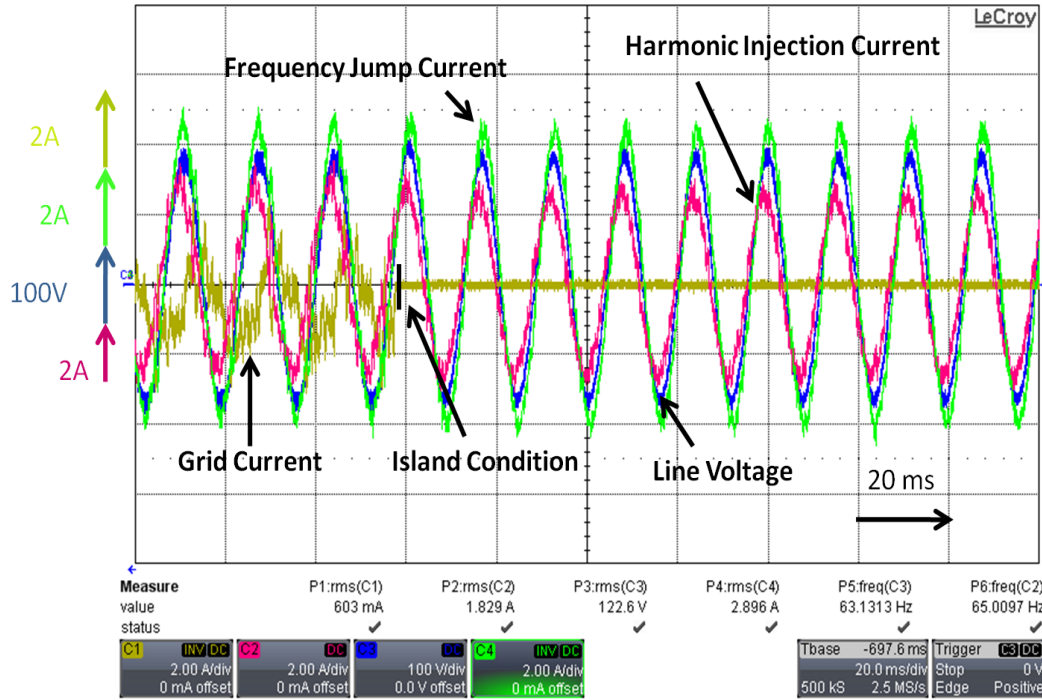


Fig. 33 Two methods in parallel at different power levels

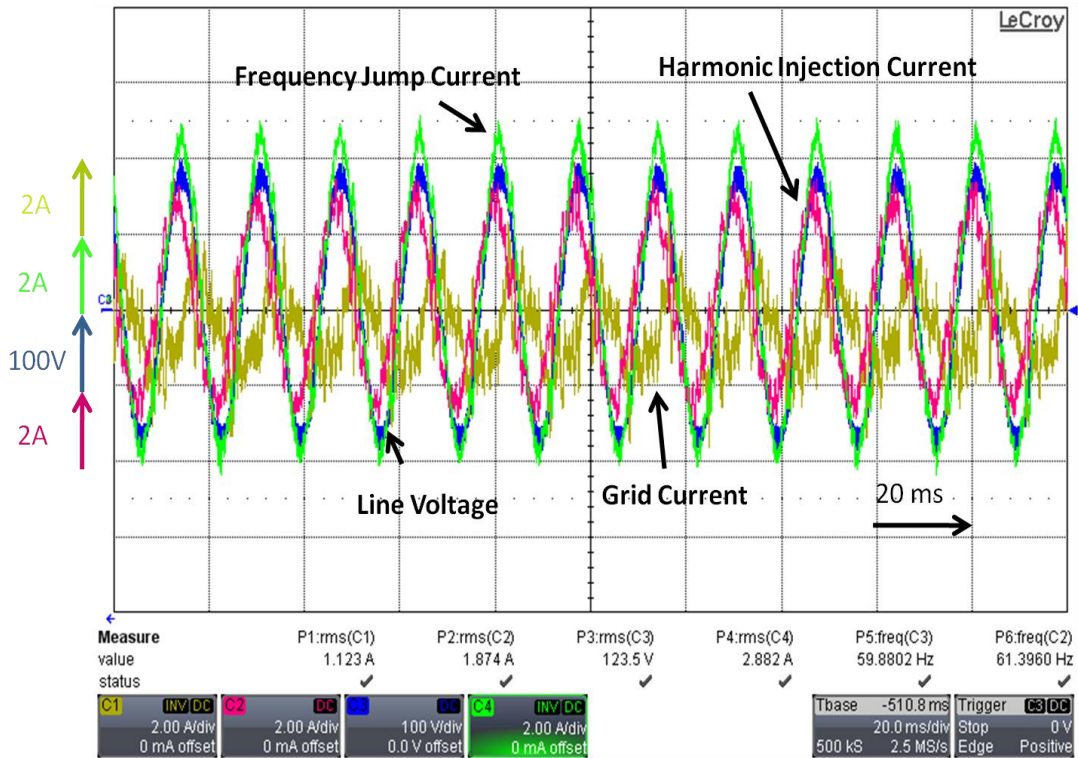


Fig. 34 Two methods in parallel before islanding

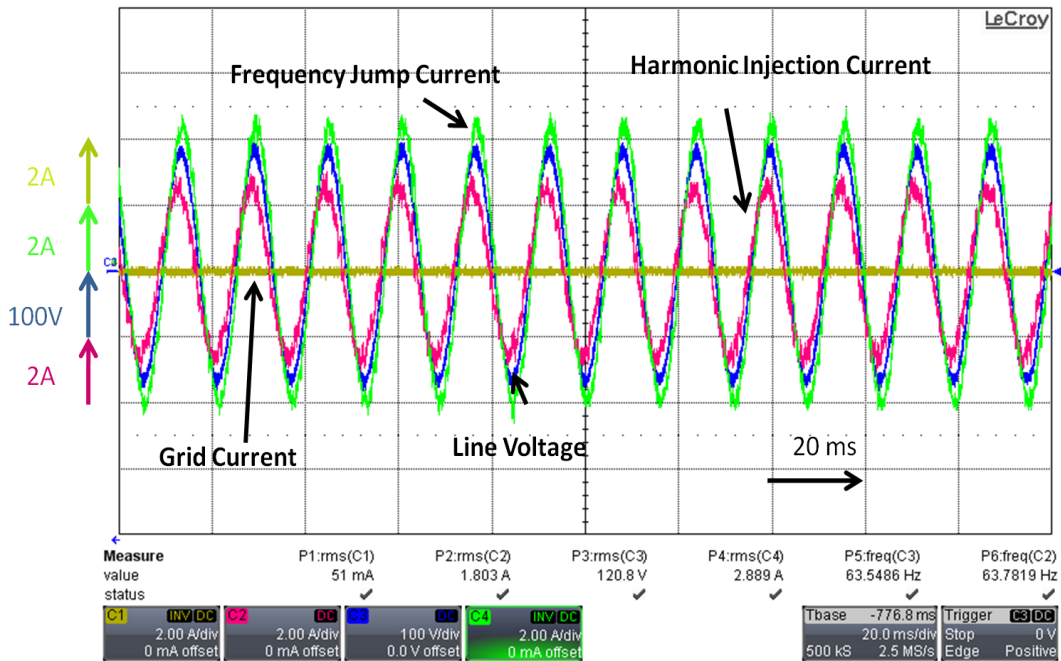


Fig. 35 Two methods in parallel after islanding

8.2 Frequency Jump and Harmonic Injection in Parallel at Equal Power Levels

When the two methods are in parallel at equal power levels, the voltage output will also have a less noticeable variation when the island condition occurs (Fig. 36-39). When both inverters output equal power levels, one islanding method is no longer dominant. This means each method should have a low enough threshold to disconnect in this condition. Notice the output voltage in the islanding condition jumps to 64.2 hertz. This is a frequency jump of 4.2 hertz which is about half of the 7.8 hertz of the single inverter test. Each method should be sensitive enough to detect under this likely electric grid condition but should not be sensitive enough to cause a false detection.

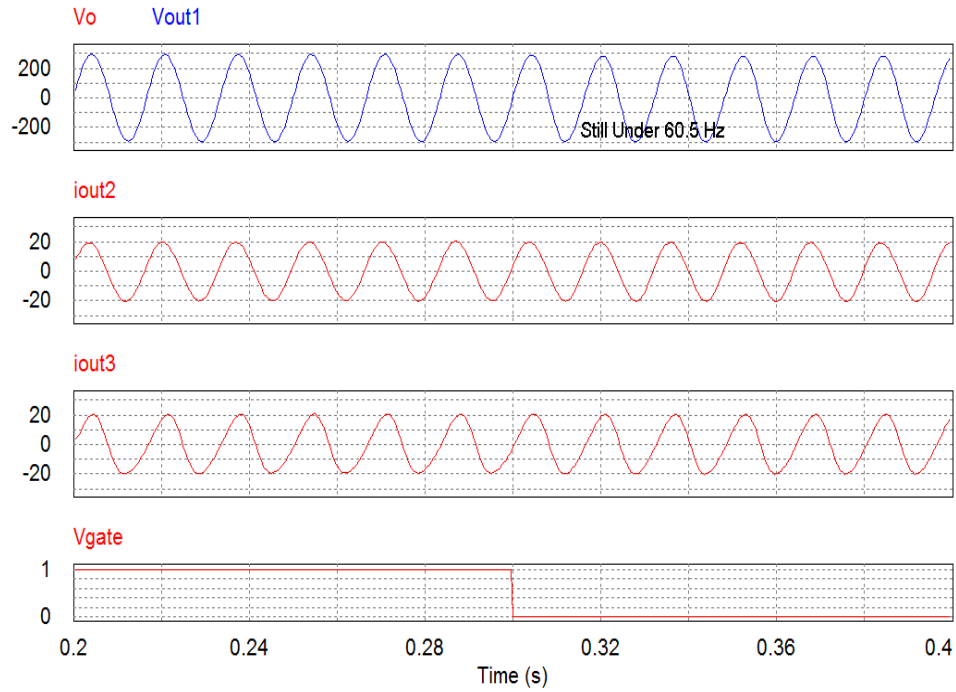


Fig. 36 Two methods in parallel at equal power

The experimental results in Figs. 37-39 show before and after an island is formed in the case with multiple methods in parallel. The frequency only increases to 63.6 hertz in this case. The islanding method is more difficult to detect when there are multiple methods in parallel.

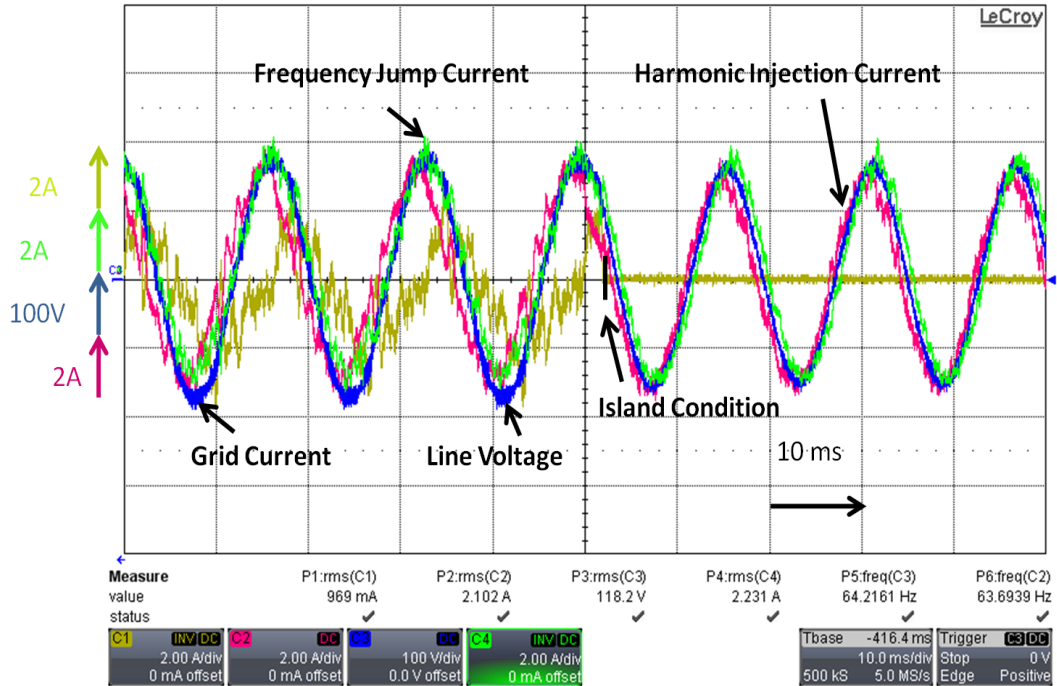


Fig. 37 Two methods in parallel at equal power

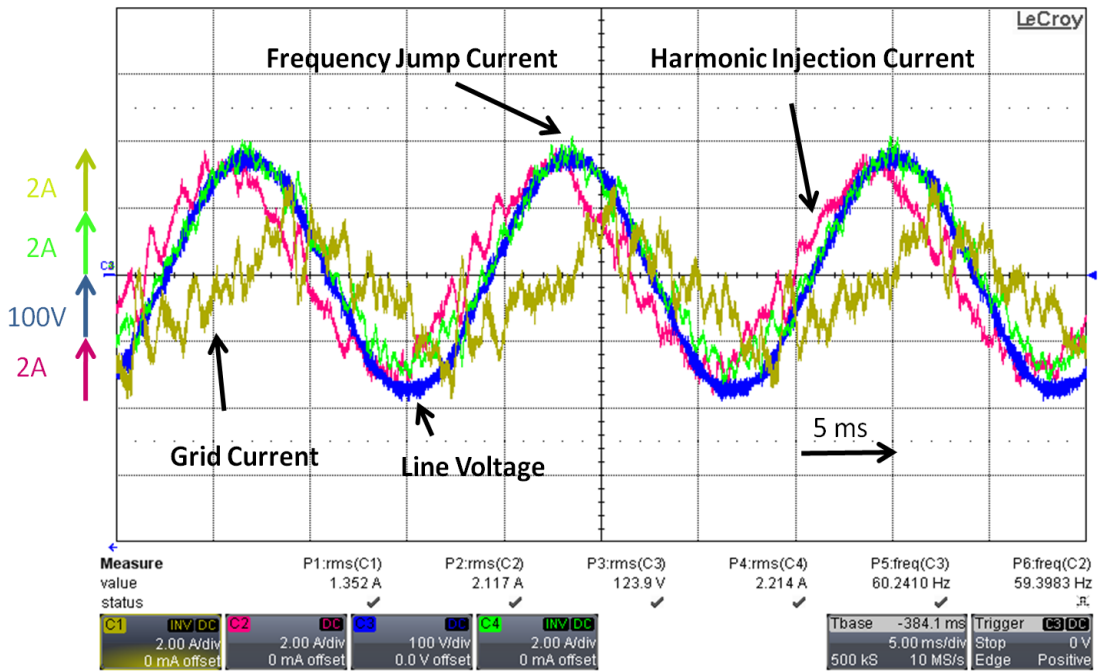


Fig. 38 Two methods in parallel before islanding

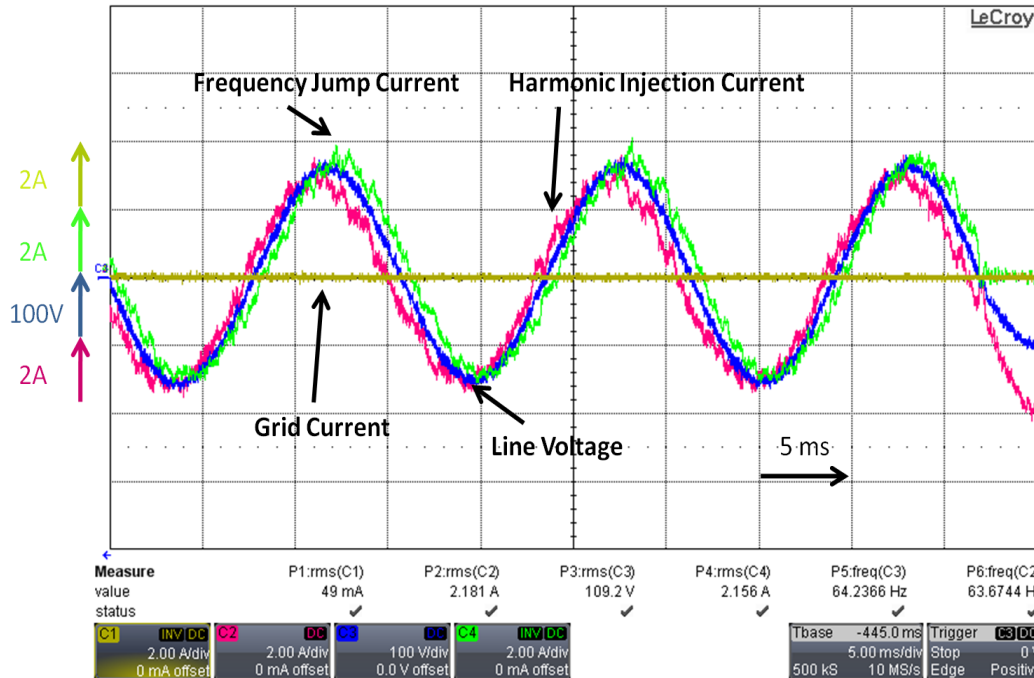


Fig. 39 Two methods in parallel after islanding

8.3 Enphase Method in Parallel with Passive Method

The Enphase method is simulated in parallel with the passive method (Fig. 40). Notice the KpDeltaW signal or error signal was oscillating until 0.49. From above, this method requires accuracy to about 0.02. Using the error signal to detect an island, allows the power quality to be higher and the voltage is hardly affected. This method must require extremely accurate measurements.

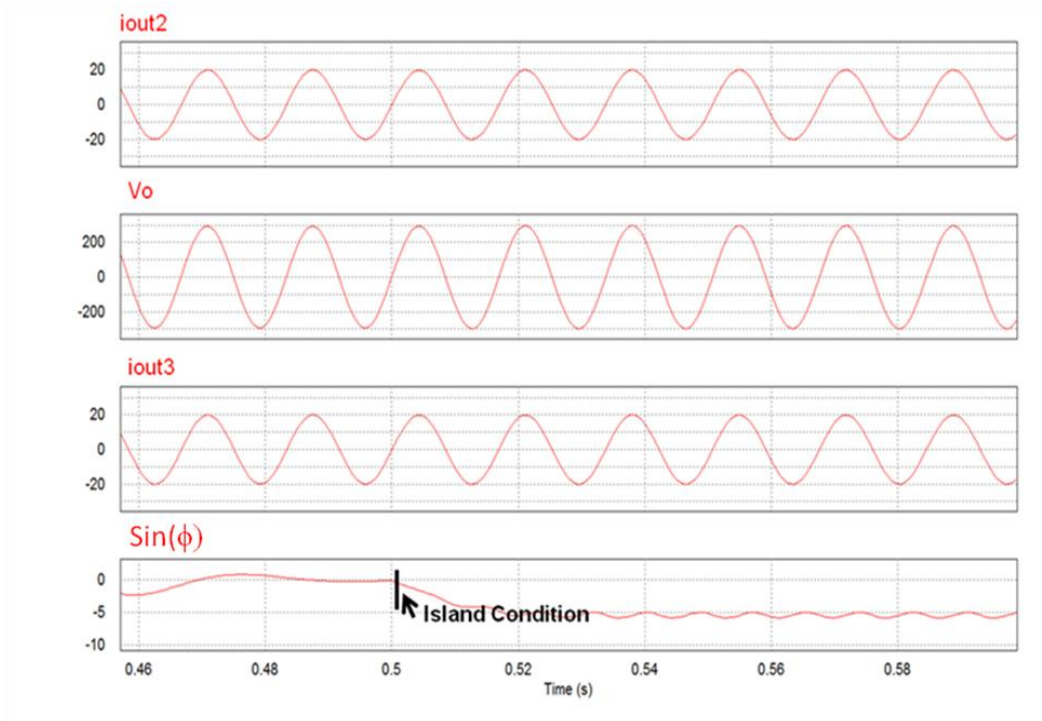


Fig. 40 Enphase in parallel with passive method

The Enphase will stay connected longer in the parallel condition (Fig. 41). The parallel condition is much more difficult to detect and represents a likely grid condition.

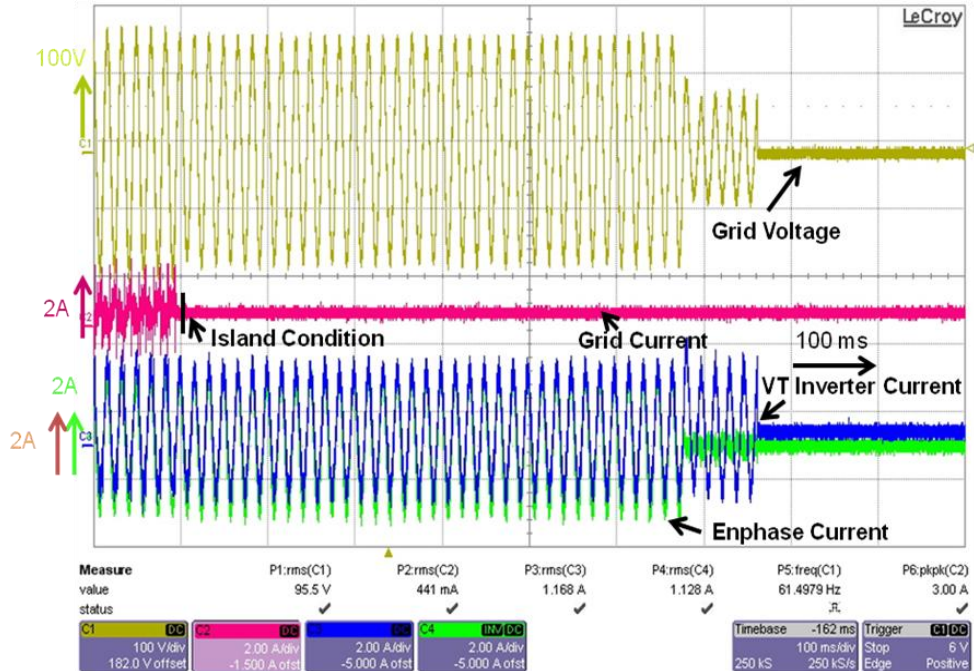


Fig. 41 Enphase and passive method in parallel

9 Load Step

The load step is setup where the Enphase output is in parallel with a 300 Ω (160 W) load and the EPS. The EPS connection comes from a 208 V_{rms} outlet connected to a 208 V_{rms} to 240 V_{rms} transformer. There is a switch connected to a 6 Ω (9.6 kW) resistor (Fig. 42). The loads have the 240 V_{rms} waveform across them. The load step represents an increase in the grid current while the inverter output current stays the same.

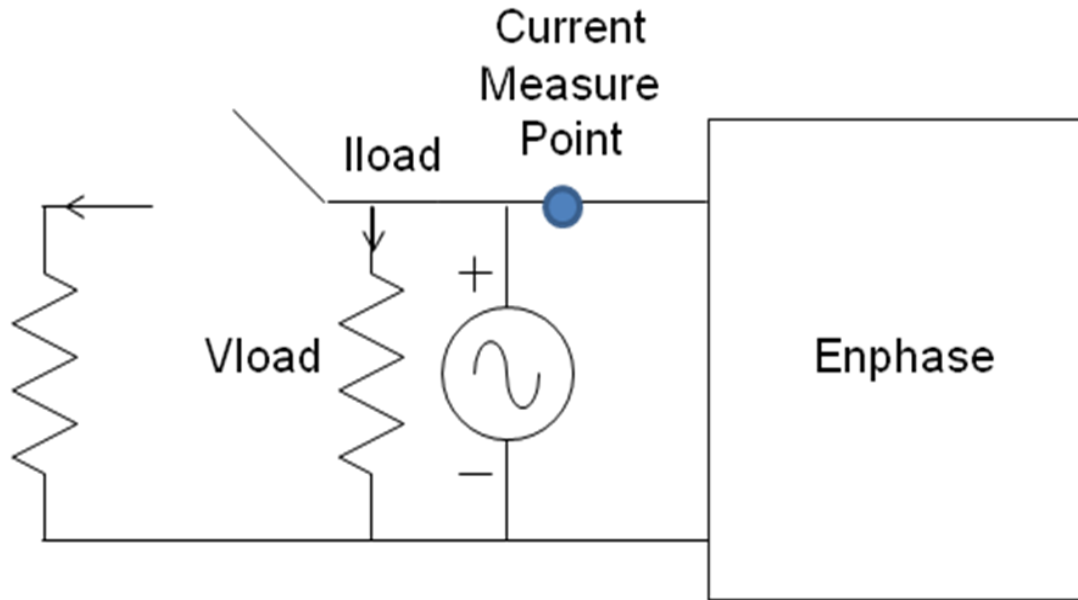


Fig. 42 Load step test setup

The load step will cause more current to come from the EPS which will cause the voltage drop across the line impedance to be higher. This causes the voltage at the inverter to drop. The voltage drops from the nominal voltage to 91%-93% of nominal voltage. This is above the 88% lower rating of the voltage which means the inverter should stay on according to the IEEE 1547 standard. This test was repeated a few times and the result shown in Figs. 43-44 only happens if the switch occurs near the zero crossing. Since this has the potential of shutting off when the loads actually need more power demonstrates this could cause a significant problem. If the voltage continues to drop, circuit breakers on the electric grid may need to disconnect causing a blackout in the grid.

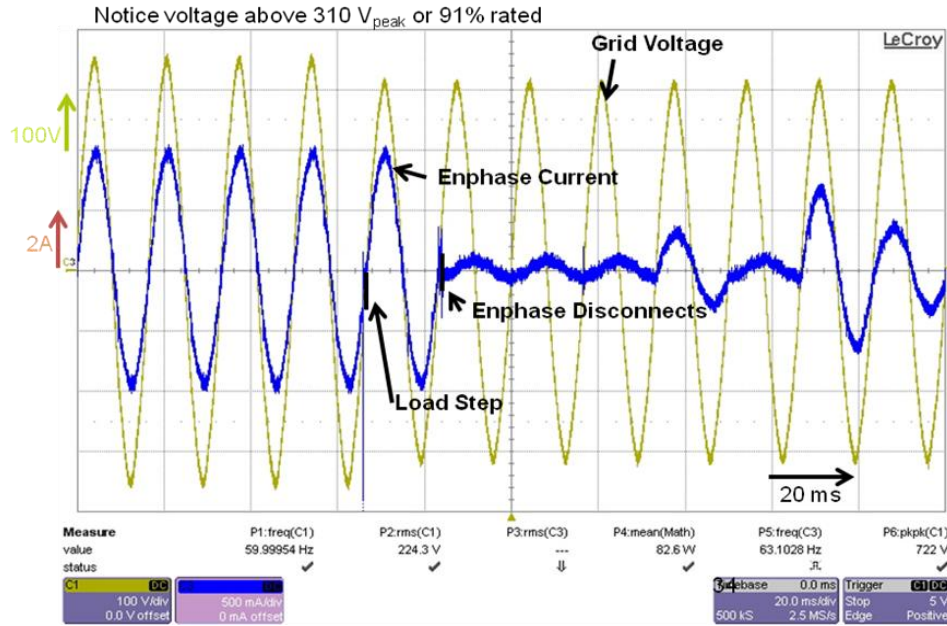


Fig. 43 Zoom in load step result

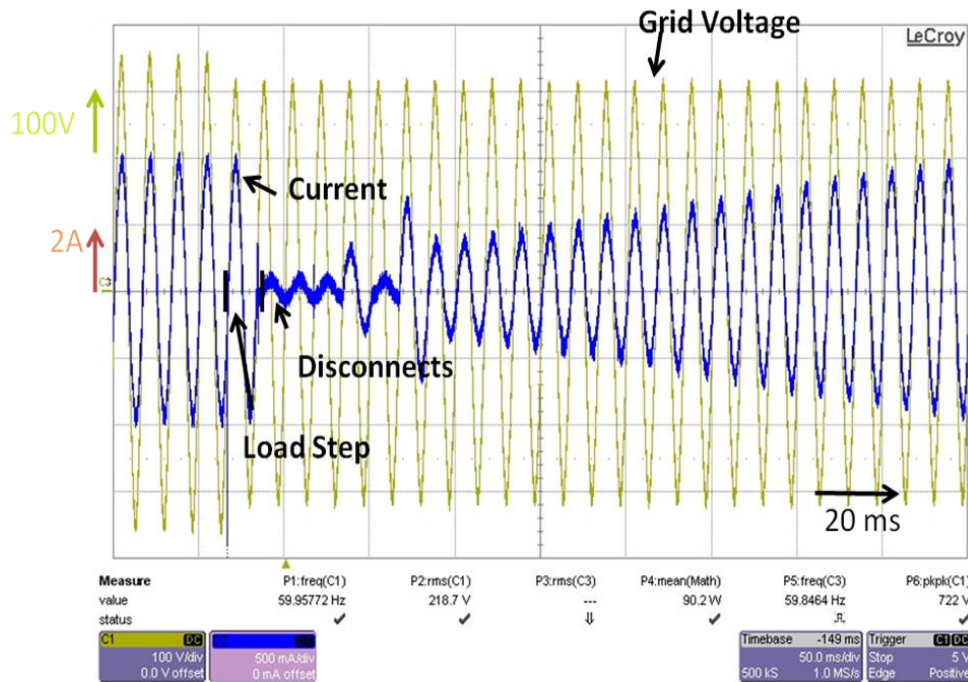


Fig. 44 Load step results

The load step effects the frequency measurement in the phase lock loop.

Fig. 45 shows a 14 ohm resistor has a load step where an additional 29 ohm

resistor goes in parallel with it. The frequency changes less than 0.1 rad/s. Fig. 46 shows a 14 ohm load that goes in parallel with a 7 ohm load. This load step has a large change in the phase lock loop frequency. This shows that if the phase lock loop frequency is used to measure frequency for an anti-islanding method, the frequency measurement has the possibility of going out of range even though there is not an island.

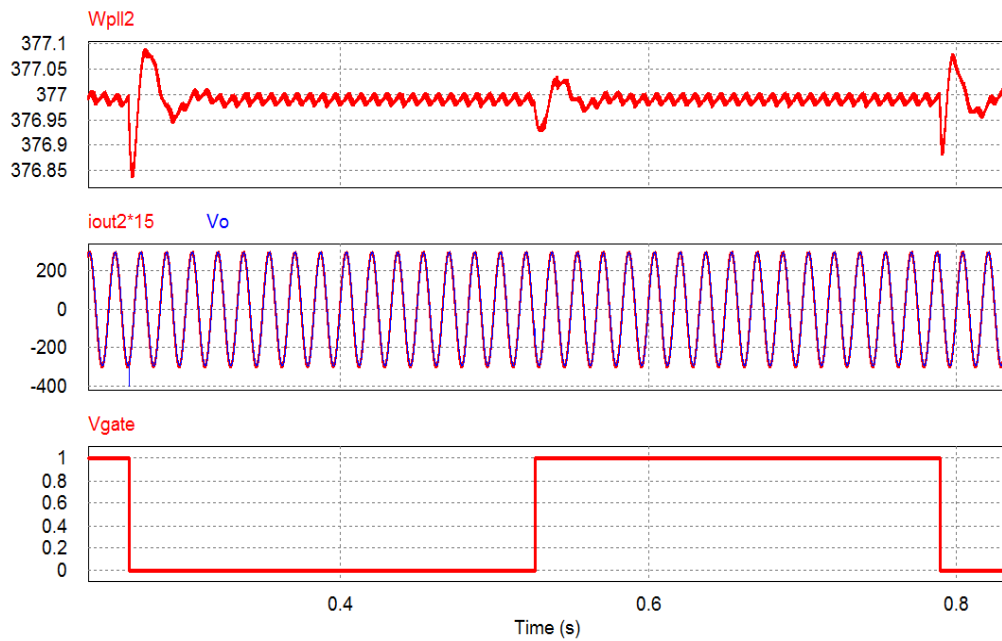


Fig. 45 Phase Lock Loop Load Step Simulation

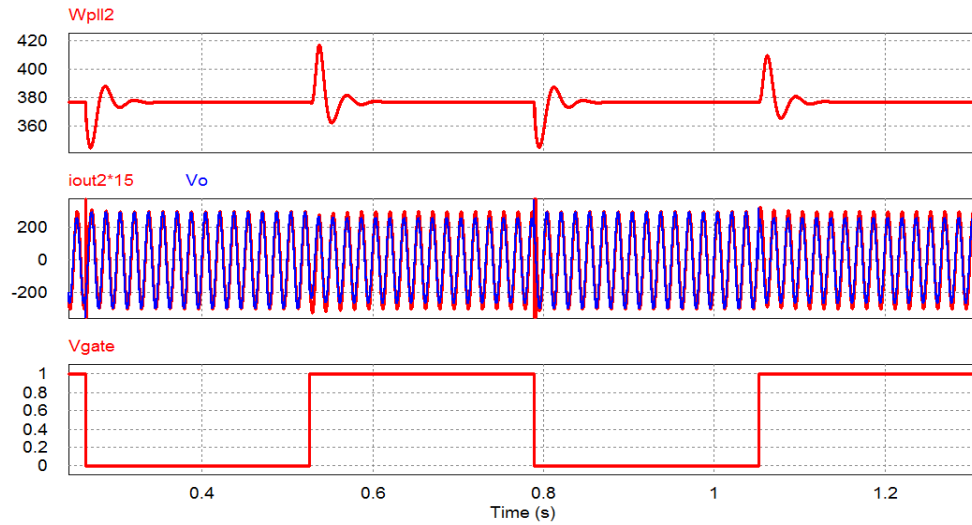


Fig. 46 Phase Lock Loop High Power Load Step Simulation

A load step will cause a phase shift and magnitude jump in the grid current. The load step is from 150 ohm to 15 ohm in parallel with a 500uF capacitor (Fig. 47). The voltage source is a 208rms volt source and the current source is a 15 amp source. The results shown in Fig. 48 illustrate the transient response. This condition is likely to occur on the power grid and should be considered in the design in islanding detection methods.

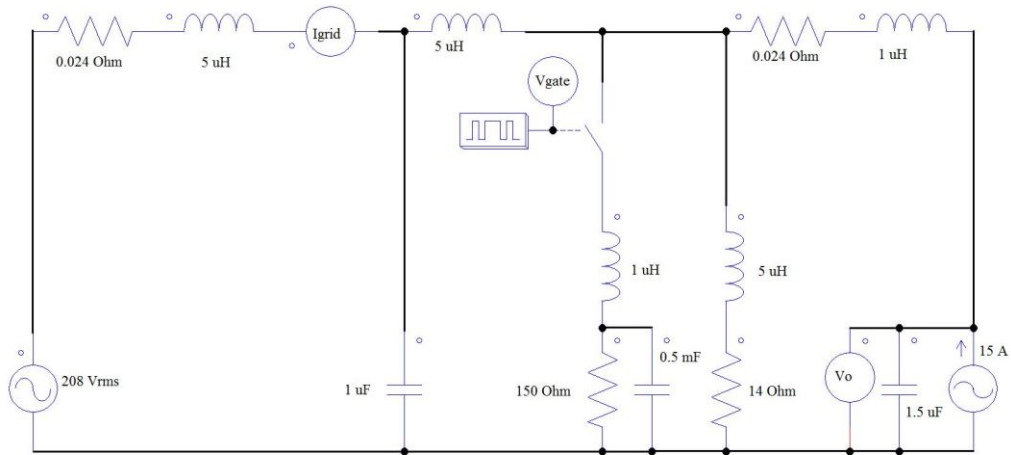


Fig. 47 Test setup of the load step test

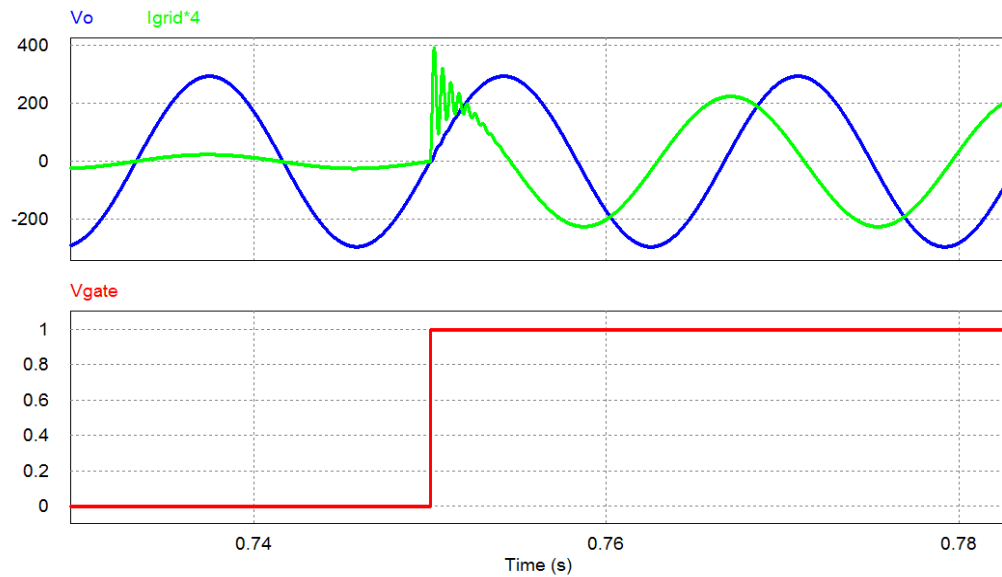


Fig. 48 Current phase change at load step

10 Power Line Communications

Power line communications are often discussed for islanding detection [49]. The problem with this method is that power lines act like an inductor

and capacitor to filter the communication signal. The transfer function of the filter is shown in (8) where R_l is the load resistance.

$$T = \frac{R_l}{CLR_l s^2 + Ls + R_l} \quad (8)$$

The capacitance and inductance of the line is usually characterized to be 1 mH/km and 8 nF/km but can vary by temperature, wire size, distance between sending and receiving lines, and other variables. This transfer function does not take into account the many step up and step down transformers in the EPS. The Bode plot of 1 km and 10 km lines are shown in Fig. 49. This does not include transformer inductances which are likely to attenuate any power line communication signals even more.

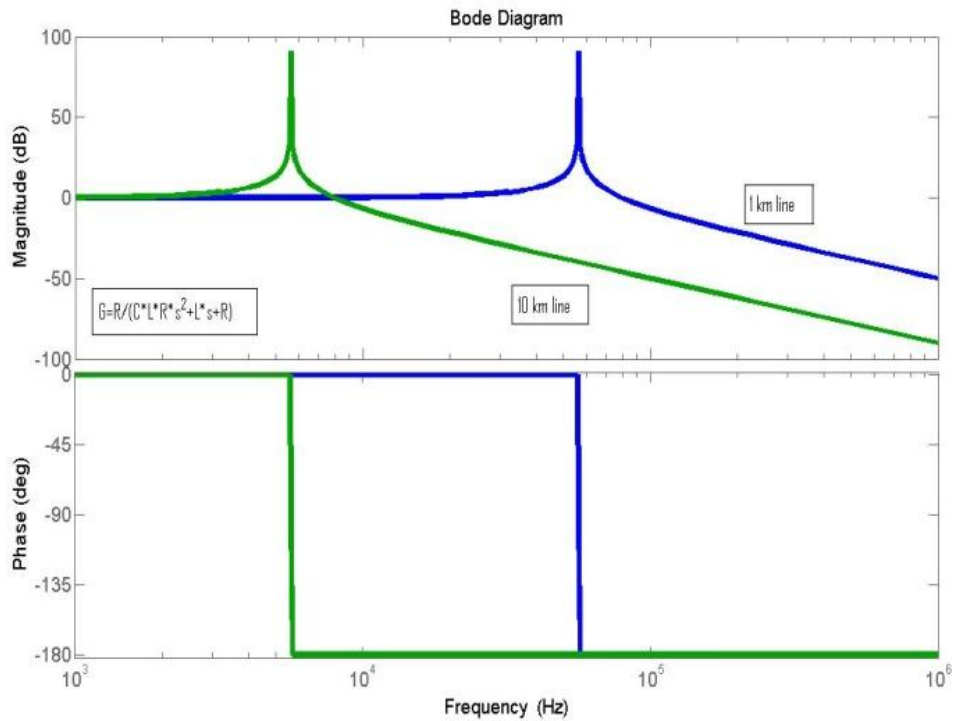


Fig. 49 Transmission line Bode plot

The transmission line is simulated at 56 kbits/sec to show that the communication signal will be attenuated significantly; as shown in Fig. 50, where V_{out} is the signal down the line. Repeaters may be used to extend the distance of the communication signal, but these are likely to be expensive.

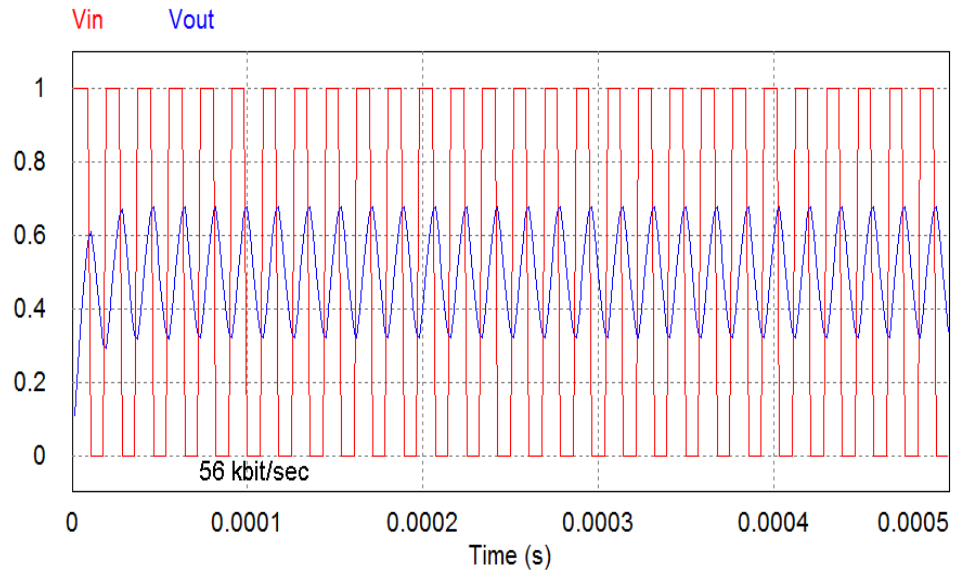


Fig. 50 Power line communications before 1 km and after 1 km transmission line

11 SCADA

The future power system will include more monitoring and communication to provide better reliability and monitor DRs. The communication requires proper security and a large investment to deploy. The communications are still likely to fail sometimes. The islanding detection methods discussed in this paper will still be necessary in the condition where communication is lost between the DR and the EPS operator.

12 Conclusion

Multiple islanding detection methods and conditions were presented. The passive method will not detect under the non-detection zone. While the active methods detected in the non-detection zone, the harmonic injection method provided poor power quality to the grid. Each method must affect the voltage. When the current decreases, the effect on the voltage is much less. It is expected that in the multiple methods in parallel case, that when one method has a very small output current compared to other methods it will not detect. This condition requires the inverter to be sensitive. The Enphase method detected an island and turned off when at the next zero crossing. This provides good power quality, but can trip unnecessarily. Proving this by switching a large load connected to the grid showed that Enphase is extremely sensitive to output transients.

The improvements that can be made are that the methods can require a 1-2 second island ride through in case the EPS comes back quickly. Currently, if the inverter is disconnected, it must wait a fixed delay of 5 minutes or a user adjustable delay to reconnect. A balance must be found between making the islanding method too sensitive that it will trip unnecessarily or not sensitive enough that it will not detect an island in the parallel inverter case. The multiple methods in parallel test is currently not considered even

though it is highly likely in the EPS since each inverter company owns different intellectual property for the islanding detection methods. The load step case is also not considered and is highly likely since it represents a load turning on or off. The load can be any load such as an industrial load, commercial load, or a residential load. There is some speculation that power lines may filter the load step transient but distributed generation is likely to be used near the load for lower losses. The power line communication method is not a good alternative since power lines are likely to filter the communication signal. The power line communications method requires a very low transmission frequency so that the signal is not filtered by the transmissions lines over long distances. There is a lot of noise on power lines at low frequencies which makes reading the communication signal difficult at lower frequencies. Also, the lower the transmission frequency, the less information that can be sent making power line communications an uneconomical alternative. If the SCADA method is used, inverter based methods are required in the loss of communications case.

13 Future Work

The future work includes adding more methods in parallel to test the case when the current out of each method is small. If there are 5 methods in parallel, each method can send a fifth of the required current out making one

single method difficult to affect the voltage. The future work involves testing multiple methods in parallel where each source provides a smaller current. With more methods in parallel, one method should not become dominant and trip first. When the inverter providing the most power trips, the other inverter with the other method will trip from an under voltage condition.

The operating principle of each method is that the grid is a voltage source controlled by the utility. It is possible that if there is a large impedance of the grid causing the grid to act as a current source, the islanding method may detect an island unintentionally. The future work would be studying anti-islanding detection methods under various grid impedances to verify a possibility of a false trip.

There is some concern that multiple methods in parallel will cause an unstable condition. The future work will study the stability of multiple methods in parallel using eigenvalue analysis.

14 References

[1] “*Renewables 2007 Global Status Report*,” Paris:REN21 Secretariat and Washington, DC: Worldwatch Institute, REN21. 2008.

[2] *IEEE Standard for Interconnecting Distributed Resources with Electric Power System*, IEEE standard 1547, 2003

[3] L. Kumpulainen, K. Kauhaniemi, P. Verho, and O. Vähämäki, “New Requirements for System Protection Caused by Distributed Generation,” *18th International Conference on Electricity Distribution*, Turin, Jun. 2005.

[4] C.L. Chen, Y. Wang, J.S. Lai, Y.S. Lee, and D. Martin, "Design of Parallel Inverters for Smooth Mode Transfer Microgrid Applications," *IEEE Trans. on Power Electronics*, vol. 25, pp. 6-15, Jan. 2010.

[5] I. Balaguer, Q. Lei, S. Yang, U. Supatti, and F. Z. Peng, “Control for Grid-Connected and Intentional Islanding Operations of Distributed Power Generation,” *IEEE Trans. on Industrial Electronics*, vol. 58, pp. 147-157, Jan. 2011.

[6] X. Yu, A. Khambadkone, H. Wang, and S. T. Terence, “Control of Parallel-Connected Power Converters for Low-Voltage Microgrid-Part I: A

Hybrid Control Architecture,” *IEEE Trans. on Power Electronics*, vol. 25, pp. 2962-2970, Dec. 2010.

[7] G. Xu, V. Vittal, A. Mcklin, and J. E. Thalmann, “Controlled Islanding Demonstrations on the WECC System,” *IEEE Trans. on Power Systems*, vol. 26, pp. 334-243, Feb. 2011.

[8] S. S. Ahmed, N. C. Sarker, A. B. Khairuddin, M. Ghani, and H. Ahmad, “A Scheme for Controlled Islanding to Prevent Subsequent Blackout,” *IEEE Trans. on Power Systems*, vol. 18, pp. 136-143, Feb. 2003.

[9] R. Walling, and N. Miller, “Distributed Generation Islanding – Implications on Power System Dynamic Performance” *Power Engineering Society Summer Meeting*, Chicago, IL, Sep. 2005, pp. 92-96.

[10] M. Francesco, M. Liserre, and A. Aquila, “Overview of Anti-Islanding Algorithms for PV Systems. Part II: Active Methods,” *Power Electronics and Motion Control Conference*, 2006, pp. 1884-1889.

[11] V. Menon, “A New Islanding Detection Technique for Distributed Generation,” Master’s Thesis, Montana State University, 2006.

[12] Z. Ye, R. R. Walling, R. Garces, R. Zhou, L. Li, and T. Wang, “Study and Development of Anti-Islanding Control for Grid-Connected Inverters,” NREL/SR-560-36243, May 2004.

[13] L. Lopes and Y. Zhang, "Islanding Detection Assessment of Multi-Inverter Systems with Active Frequency Drifting Methods," *IEEE Trans. on Power Delivery*, vol. 23, pp. 480-486, Jan. 2008.

[14] D. Persson, "Islanding Detection in Power Electronic Converter Based Distributed Generation," *Industrial Electrical Engineering and Automation*, 2007.

[15] E. Estébanez, V. Moreno, A. Pigazo, and M. Liserre, "An Overview of Anti-Islanding Detection Algorithms in Photovoltaic Systems in Case of Multiple Current-Controlled Inverters," *35th Annual Conference of IEEE Industrial Electronics*, Feb. 2010, pp. 4555-4560.

[16] R. Bhandari, S. Gonzalez, and M. Ropp, "Investigation of Two Anti-Islanding Methods in the Multi-Inverter Case," *Power and Energy Society General Meeting- Conversion and Delivery of Electrical Energy in the 21st Century*, Pittsburgh, PA, Aug. 2008, pp. 1-7.

[17] C. Jeraputra, and P. N. Enjeti, "Development of a Robust Anti-Islanding Algorithm for Utility Interconnection of Distributed Fuel Cell Powered Generation," *IEEE Trans. on Power Electronics*, vol. 19, pp. 1163-1170, Sep. 2004.

[18] P. Mahat, Z. Chen, and B. Bak-Jensen, "Review of Islanding Detection Methods for Distributed Generation," *Third International*

Conference on Electric Utility Deregulation and Restructuring and Power Technologies, Nanjing, May 2008, pp. 2743-2748.

[19] H. Vahedi, R. Noroozian, A. Jalilvand, and G. B. Gharehpetian, "A New Method for Islanding Detection of Inverter-Based Distributed Generation Using DC-Link Voltage Control," *IEEE Trans. on Power Delivery*, vol. 26, pp. 1176-1186, Apr. 2011.

[20] T. Funabashi, K. Koyanagi, and R. Yokoyama, "A Review of Islanding Detection Methods for Distributed Resources," *IEEE Bologna Power Tech Conference*, Bologna, Italy, pp. 1-6, Jun. 2003.

[21] T. Thacker, "Control of Power Conversion Systems for the Intentional Islanding of Distributed Generation Units," Master's thesis, Virginia Polytechnic Institute and State University, 2005.

[22] C. Jeraputra, "Investigation of Anti-Islanding Schemes for Utility Interconnection of Distributed Fuel Cell Powered Generations," Ph.D. dissertation, Texas A&M, 2004.

[23] W. El-Khattam, A. Yazdani, T. Sidhu, and R. Seethapathy, "Investigation of the Local Passive Anti-Islanding Scheme in a Distribution System Embedding a PMSG-Based Wind Farm," *IEEE Trans. on Power Delivery*, vol. 26, pp. 42-52, Jan. 2011.

[24] S. Lee, and J. Park, “New Islanding Detection Method for Inverter-Based Distributed Generation Considering Its Switching Frequency,” *IEEE Trans. on Industry Applications*, vol. 46, pp. 2089-2098, Sep. 2010.

[25] S. Huang, and F. Pai, “A New Approach to Islanding Detection of Dispersed Generators with Self-Commutated Static Power Converters,” *IEEE Trans. on Power Delivery*, vol. 15, pp. 500-507, Apr. 2000.

[26] H. H. Zeineldin, and J. L. Kirtley, “A Simple Technique for Islanding Detection With Negligible Nondetection Zone,” *IEEE Trans. on Power Delivery*, vol. 24, pp. 779-786, Apr. 2009.

[27] Y. Jung, J. Choi, B. Yu, and G. Yu, “Optimal Design of Active Anti-islanding Method Using Digital PLL for Grid-connected Inverters,” *Power Electronics Specialists Conference*, 2006, pp. 1-6.

[28] W. Bower, and M. Ropp, “Evaluation of Islanding Detection Methods for Photovoltaic Utility-Interactive Power Systems,” *IEA Photovoltaic Power Systems Programme*, T5-09, Mar. 2002.

[29] L. Lopes, and H. Sun, “Performance Assessment of Active Frequency Drifting Islanding Detection Methods,” *IEEE Trans. on Energy Conversion*, vol. 21, pp. 171-180, Mar. 2006.

[30] H. Xiang, Y. Yan, and H. Jiang, "A Two-Stage PV Grid-Connected Inverter with Optimized Anti-Islanding Protection Method," *International Conference on Sustainable Power Generation and Supply*, 2009, pp. 1-4.

[31] M. Ciobotaru, V. Agelidis, and R. Teodorescu, "Accurate and Less-Disturbing Active Anti-Islanding Method Based on PLL for Grid-Connected Converters," *IEEE Trans. on Power Electronics*, vol. 25, pp. 1576-1583, Jun. 2010.

[32] F. Martin, M. Hassan-Ali, and T. Bolfan, "Method and Apparatus for Anti-Islanding of Distributed Power Generation Systems," US Patent no. 0021877, Jan. 2009.

[33] J. Vieira, W. Freitas, W. Xu, and A. Morelato, "An Investigation on the Nondetection Zones of Synchronous Distributed Generation Anti-Islanding Protection," *IEEE Trans. on Power Delivery*, vol. 23, pp. 593-600, Apr. 2008.

[34] M. E. Ropp, M. Begovic, A. Rohatgi, G. A. Kern, R. H. Bonn, and S. Gonzalez, "Determining the Relative Effectiveness of Islanding Detection Methods Using Phase Criteria and Nondetection Zones," *IEEE Trans. on Energy Conversion*, vol. 15, pp. 290-296, Sep. 2000.

[35] Z. Ye, A. Kolwalkar, Y. Zhang, P. Du, and R. Walling, "Evaluation of Anti-Islanding Schemes Based on Nondetection Zone Concept," *IEEE Trans. on Power Electronics*, vol. 19, pp. 1171-1176, Sep. 2004.

[36] J.-S. Lai, S. R. Moon, R.-Y. Kim, F.-Y. Lin, Y.-H. Liu and M.-H. Lin, "A Versatile Three-Phase DC-DC Converter Circuit for Fuel Cell Applications," *Journal of the Chinese Institute of Engineers*, Nov. 2007, pp. 1145-1152.

[37] J.-S. Lai, S.-Y. Park, S. R. Moon, C.-L. Chen, "A High-Efficiency 5-kW Soft-Switched Power Conditioning System for Low-Voltage Solid Oxide Fuel Cells," *Power Conversion Conference*, Nagoya, Japan, Apr. 2007, pp. 463 - 470.

[38] S. Ranade, D. Sagi, R. Mulpuri, R. Surabhi, and J. Mitra, "Likelihood of Islanding in Distribution Feeders with Photovoltaic Generation," *Power Engineering Society General Meeting*, Tampa, FL, Jul. 2007, pp. 1-6.

[39] R. Bründlinger and B. Bletterie, "Unintentional Islanding in Distribution Grids with a High Penetration of Inverter-Based DG: Probability for Islanding and Protection Methods," *IEEE Power Tech*, St. Petersburg, Russia, pp. 1-7, May 2008.

[40] D. Dong, D. Boroyevich, P. Mattavelli, and I. Cvetkovic, "A High-Performance Single-Phase Phase-Locked-Loop with Fast Line-Voltage

Amplitude Tracking,” *Applied Power Electronics Conference and Exposition*, Fort Worth, TX, 2011, pp. 1622-1628.

[41] C. Chen, “Design, Implementation, and Analysis for an Improved Multiple Inverter Microgrid System,” Ph. D. dissertation, Dept. Elect. and Comp. Eng., Virginia Tech., Blacksburg, VA, 2011.

[42] D. Dong, “Modeling and Control Design of a Bidirectional PWM Converter for Single-phase Energy Systems,” M. S. thesis, Dept. Elect. and Comp. Eng., Virginia Tech., Blacksburg, VA, 2009.

[43] R. Teodorescu, and F. Blaabjerg, “Flexible Control of Small Wind Turbines with Grid Failure Detection Operating in Stand-Alone and Grid-Connected Mode,” *IEEE Trans. on Power Electron.*, vol. 19, pp. 2293-2298, Nov. 2007.

[44] J. Sangmin, B. Youngsang, C. Sewan, and K. Hyosung, “A Low Cost Utility Interactive Inverter for Residential Fuel Cell Generation,” *IEEE Trans. on Power Electron.*, vol. 22, pp. 2293-2298, Nov. 2007.

[45] T. Haimin, J. L. Duarte, and M. A. M. Hendrix, “Line-Interactive UPS Using a Fuel Cell as the Primary Source,” *IEEE Trans. on Ind. Electron.*, vol. 55, pp. 3012-3021, Aug. 2008.

[46] X. Wang, W. Freitas, V. Dinavahi, and W. Xu, “Investigation of Positive Feedback Anti-Islanding Control for Multiple Inverter-Based

Distributed Generators,” *IEEE Trans. on Power Systems*, vol. 24, pp. 785-795, May 2009.

[47] G. Kim, H. Seo, S. Jang, S. Park, S. Kim, N. Kim, M. Park, and I. Yu, “Performance Analysis of the Anti-islanding Function of a PV-AF System under Multiple PV System Connections,” *International Conference on Electrical Machines and Systems*, Tokyo, Japan, 2009, pp. 1-5.

[48] E. J. Estébanez, V. M. Moreno, A. Pigazo, M. Liserre, and A. D. Aquila, “Performance Evaluation of Active Islanding-Detection Algorithms in Distributed-Generation Photovoltaic Systems: Two Inverters Case,” *IEEE Trans. on Industrial Electronics*, vol. 58, pp. 1185-1193, Apr. 2011.

[49] M. E. Ropp, K. Aaker, J. Haigh, and N. Sabbah, “Using Power Line Carrier Communications to Prevent Islanding [of PV Power Systems],” *Photovoltaic Specialists Conference*, Anchorage, AK, 2000, pp. 1675-1678.