Modeling and Characterization of Power Electronic Converters with an Integrated Transmission-Line Filter

Andrew C. Baisden

Thesis submitted to the Faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

MASTERS OF SCIENCE

in

Electrical Engineering

APPROVED:

Dushan Boroyevich, Chairman

Jacobus Daniel van Wyk

Hardus Odendaal

May 2, 2006

Blacksburg, Virginia

Keywords: Electro-magnetic Interference (EMI), High frequency modeling, Transmission line filter, Common Mode (CM), Differential Mode (DM), Power Factor Correction (PFC) Boost

Copyright 2006, Andrew Carson Baisden

Modeling and Characterization of Power Electronic Converters with an Integrated Transmission-Line Filter

by

Andrew C. Baisden

Dushan Boroyevich, Chairman

Electrical Engineering

ABSTRACT

In this work, a modeling approach is delineated and described in detail; predominantly done in the time domain from low frequency, DC, to high frequencies, 100 MHz. Commercially available computer aided design tools will be used to determine the propagation path in a given structure. Next, an integrated transmission-line filter – fabricated using planar processing technologies – is modeled to accurately predict the EMI characteristics of the system. A method was derived to model the filter's performance in the time-domain while accurately depicting the highly frequency dependant transmission-line properties. A system model of a power factor correction (PFC) boost converter was completed by using active device models for diodes, MOSFETs, and the gate driver. In addition, equivalent circuits were used to characterize high frequency impedances of the passive components.

A PFC boost converter was built and used to validate the model. The PFC operated at a peak output power of 1 kW, switching at 400 kHz, with a universal input ranging from 90-270 V_{RMS} with unity power factor. The time-domain and EMI frequency spectrum waveforms are experimentally measured and agree very well with the simulated values; within 5 dB for EMI.

The transmission-line filter was also manufactured for model verification, and it is tested for the first time with an operating converter: a PFC at 50 W output and 50 V_{DC} input. The small signal characteristics match the model very well. In addition, impedance interactions between the filter, the converter, and the EMI measurement set-up are discussed, evaluated, measured, and improved to minimize undesired resonances and increase low-frequency EMI attenuation. Experimentally measured attenuation provided by the filter in the range from 100 kHz to 100 MHz was 20-50 dBμV. The simulation also shows a similar attenuation, with the exception of one key resonance not seen in the simulation.

ACKNOWLEDGEMENTS

I would like to extend my greatest thanks to my advisor Dr. Dushan Boroyevich. He has continually guided and pushed me to excel past any barrier through his perpetual questioning. His support, knowledge, confidence, and mentorship are unprecedented and I strive to incessantly learn from him day in and day out. His creative approach has kept my interest and drive at its peak throughout my pursuit for my masters degree. I would also like to thank the rest of my committee members, Dr. Daniel Jacobus van Wyk for his endless knowledge of the subject matter and ability to always find something to improve upon. He helped guide me from day one as if I was his own student and always provided his time for my infinite questions. Dr. van Wyk's curiosity and problem solving capabilities are among the best and I am honored to have had the privileged to learn and experience them. Dr. Hardus Odendaal's graduate EMI class furthered my understanding and expanded my capabilities to struggle through this phenomenon. He has been very kind and generous with his time and efforts to assist me during this task.

I would also like to thank all of the staff at CPES for their assistance for the ever so important day to day matters. Bob Martin and Dan Huff kept the labs in working order and provided insight to many problems along the way. Marianne Hawthorne, Michelle Czamanske, Trish Rose, Teresa Shaw, and Elizabeth Tranter for their administrative ingenious to get me from one day to the next.

None of this could have been possible without the network within CPES; working at CPES has provided the knowledge and experience of nearly a hundred people at my fingertips. I want to express my thanks to all of the CPES students who have helped me along the way, especially, Bryan Charboneau, Tim Thacker, Daniel Ghizoni, Jerry Francis, Qian Liu, Bing Lu, Anish Prasai, Arman Roshan, and David Reusch for their suggestions and friendship whether it be related to this work or not. I would also like to thank Vassilis Siomos, Rory Cantu, Brandon Hoeft, Chad Hudson, and my beautiful girlfriend Kristie Wolfe for their support and friendship throughout our lives.

My family has provided me the strength to continue on through their love and support. I want to thank my mother, Theresa Baisden, and father, John Baisden for an endless amount of love, support, and belief in their youngest son. I would also like to extend thanks to my brothers,

Jeff and Steve, my sister, Jennifer, and all their families. Finally, I would like to send a thank you to all my extended family, especially my grandmother who has shown how to live my life as a model citizen. I will forever love her and try to model my life after her and spread her love.

This work was supported primarily by the Engineering Research Center Program of the National Science Foundation under NSF Award Number EEC-9731677. Any opinions, findings and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect those of the National Science Foundation. This work was conducted with the use of Simplorer and Maxwell, donated in kind by the Ansoft Corporation of the CPES Industrial Consortium.

To my Grandmother

Bernice Endres

And

Godson

Hunter Karl Baisden

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. INTRODUCTION

1.1. BACKGROUND

Existing trends within power electronics focus on driving the switching frequency higher and enhancing thermal management. As a result, the power density of the converters increases. These trends are the motivation behind the research of planar technologies for power electronic converters. Modules implemented using planar technologies have the advantages of improved power densities, standardized production processes, and enhanced performances [1]. However, modules with higher switching frequencies and closer proximities of the power stage components are more vulnerable to electro-magnetic interference (EMI). Electro-magnetic noise, or EMI, that propagates through a system can potentially harm the components or deteriorate the systems operation [2]. The integrity of the system – including the supply, conversion, and load – is highly dependant on the EMI generated and propagating through the system. As seen in Fig. 1.1 any noise produced from the converter can reduce the quality of both the input and output lines.

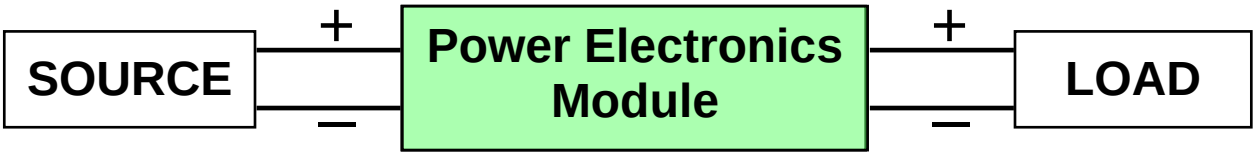


Fig. 1.1: Typical matching of the characteristics of a source to the load using a power electronics switching module.

The noise susceptibility of the load will determine if the system will function as designed. When EMI is propagated back into the system with other power conversions and loads, they too can be damaged or malfunction due to the noise. With the growing number of electronic loads and power supplies using active switching devices at increased switching frequencies degradation of the utility system is of concern. This is the reason many standards have been set for EMI noise generated [3]. The standards help protect the utility grid and the components connected to it from any disturbances produced by EMI. Standards range in severity depending on application and location. An example of an EMI noise frequency spectrum and a common standard is shown in Fig. 1.2. The solid (red) line is the International Special Committee on Radio Interference, (CISPR, from its French title, Comite International Special des Perturbations

Radioelectriques) Publication 22 standard for residential applications under their testing guidelines [4, 5]. The (black) noise plot is an example of the total EMI noise generated by a typical power supply used in a household. The noise is measured in decibels with a base unit of a μV (dBμV), over a frequency spectrum usually specified from 150 kHz to 30 MHz (conducted noise region).

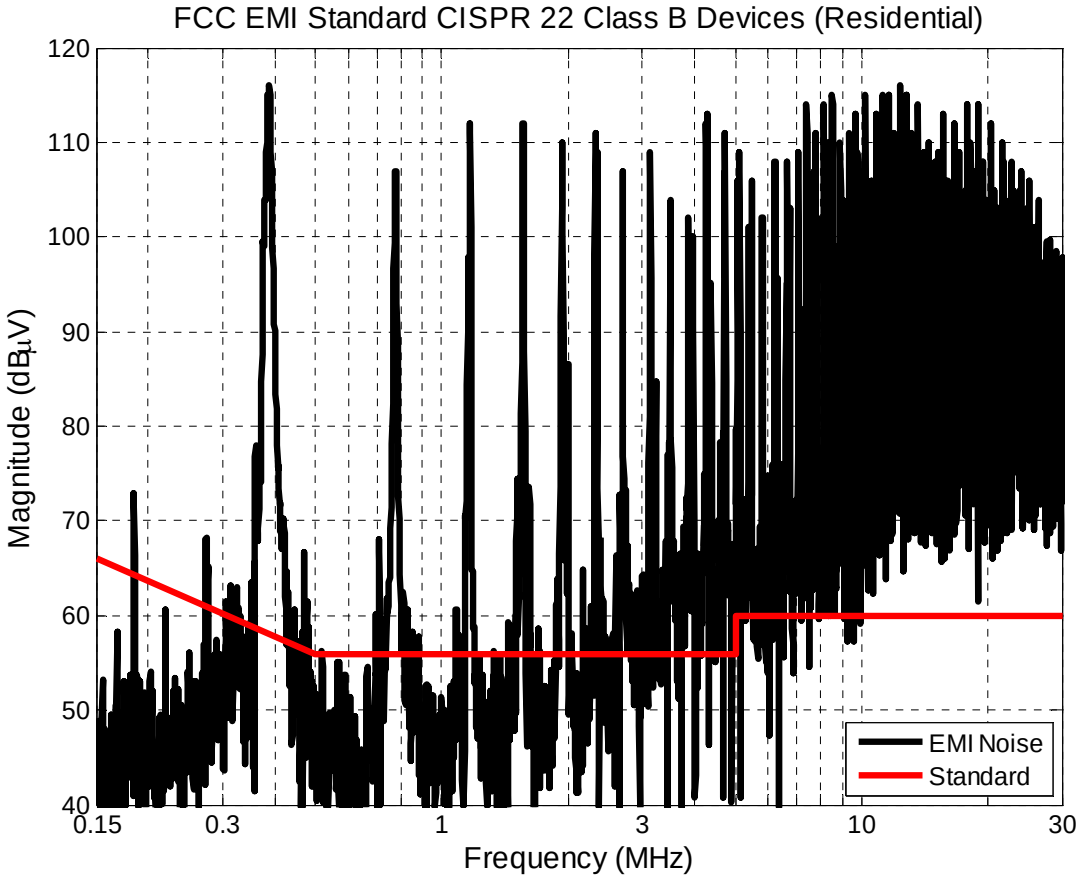


Fig. 1.2: CISPR 22 EMI Standard for Class 2 devices (residential).

There are many techniques to reduce the EMI emissions of a converter; some methods include, for example, numerous variations of passive and active filters [5-9], shielding and grounding [2, 5, 10], noise balancing or canceling [8, 11-13], converter's controls [8, 14, 15], and packaging design [8, 16-19]. EMI still posses many challenges to a power electronic engineers albeit there are many known ways of reducing the noise in the system [5]. The later the engineer attempts to reduce the noise the more costly the task becomes. If the filtering or containment of the noise is achieved earlier in the design stage more techniques are available to the engineer. Layout, device selection, or filtering are only a few of the options that can reduce

the noise and can easily be changed earlier in the design process. If the EMI is still a problem in the production phase of the product the only option an engineer has is to increase the size of the EMI filter with the consequence of increased cost, longer design cycle time, and decreased power density. A quantitative graph of this is given in Fig. 1.3.

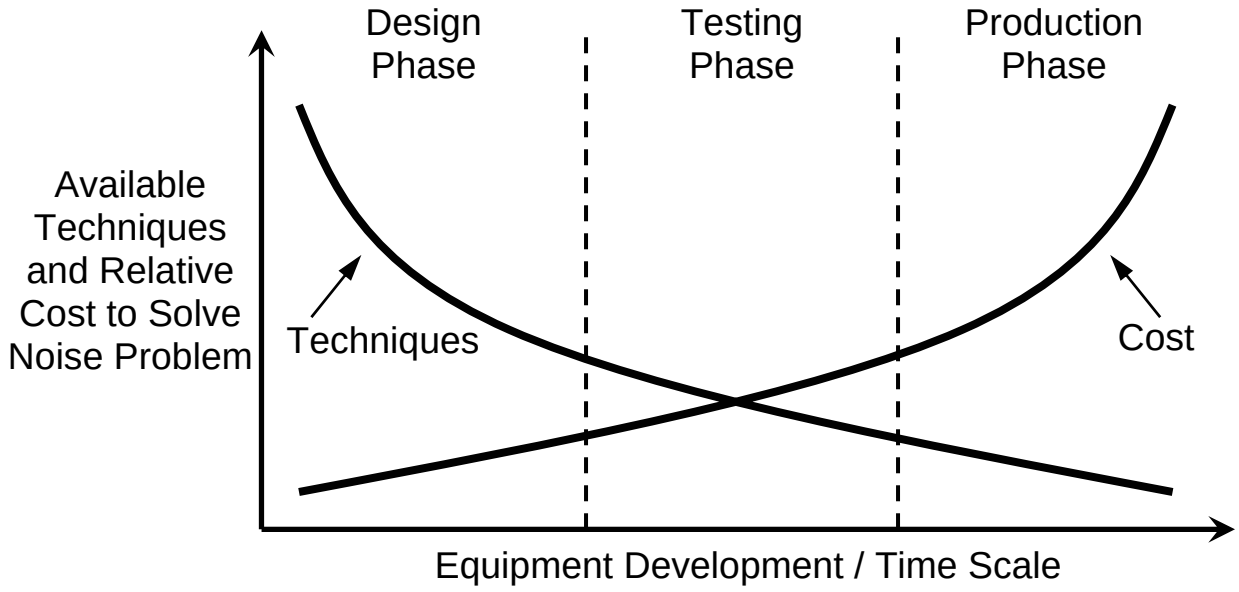


Fig. 1.3: Trade-off of available EMI reduction techniques and cost versus time [2].

The total EMI produced in a system can be categorized into conducted and radiated EMI. Conducted EMI is typically regulated between 150 kHz and 30 MHz as seen in Fig. 1.2. Radiated EMI typically is for the frequency above the conducted region; it will not be considered since it is at frequencies higher than the focus of this study. Emissions or susceptibility define the two directions EMI noise can take. Emissions are regulated through the standards mentioned where the susceptibility a device has to outside noise is self-regulating. If the unit in question is susceptible to EMI then it will not function properly and likewise not produce income. With this in mind conducted emissions of EMI will be studied in this work. A picture to represent some EMI phenomena is shown in Fig. 1.4. The dashed line represents the conducted EMI propagating from and to all sources, conversions, and loads. Furthermore, the radiated EMI is emitted by every piece of equipment, and can cause susceptibility issues as well. In the end, everything affects each other in some form or another and all components must be able to work in all conditions without emitting too much noise.

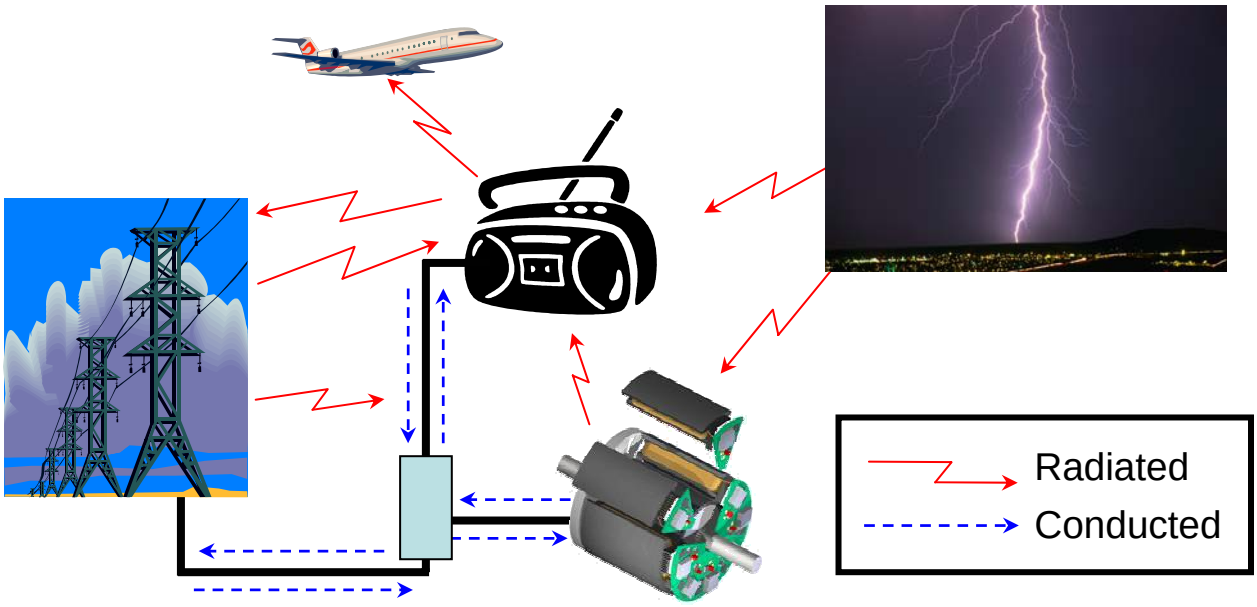


Fig. 1.4: Conducted and Radiated EMI example, showing emissions and susceptibility from potential sources and loads.

Conducted emissions can be further categorized into common-mode (CM) and differential-mode (DM) EMI. CM EMI is noise that is conducted through a common path: often a heatsink. The common path is coupled to the system via parasitic impedances such as the capacitance between a device and the heatsink as seen in Fig. 1.5a. The current through that capacitance (which contributes to the overall CM current) is found by $i_c = C\frac{dv_c}{dt}$. Similarly, the DM noise conducted throughout the system circulates through the power paths via coupled impedances such as self and mutual inductances as shown in Fig. 1.5b. Considering the closer proximities and higher switching frequencies both the coupling impedances and rate of change of the voltage and current increase respectively, therefore increasing the CM and DM noise.

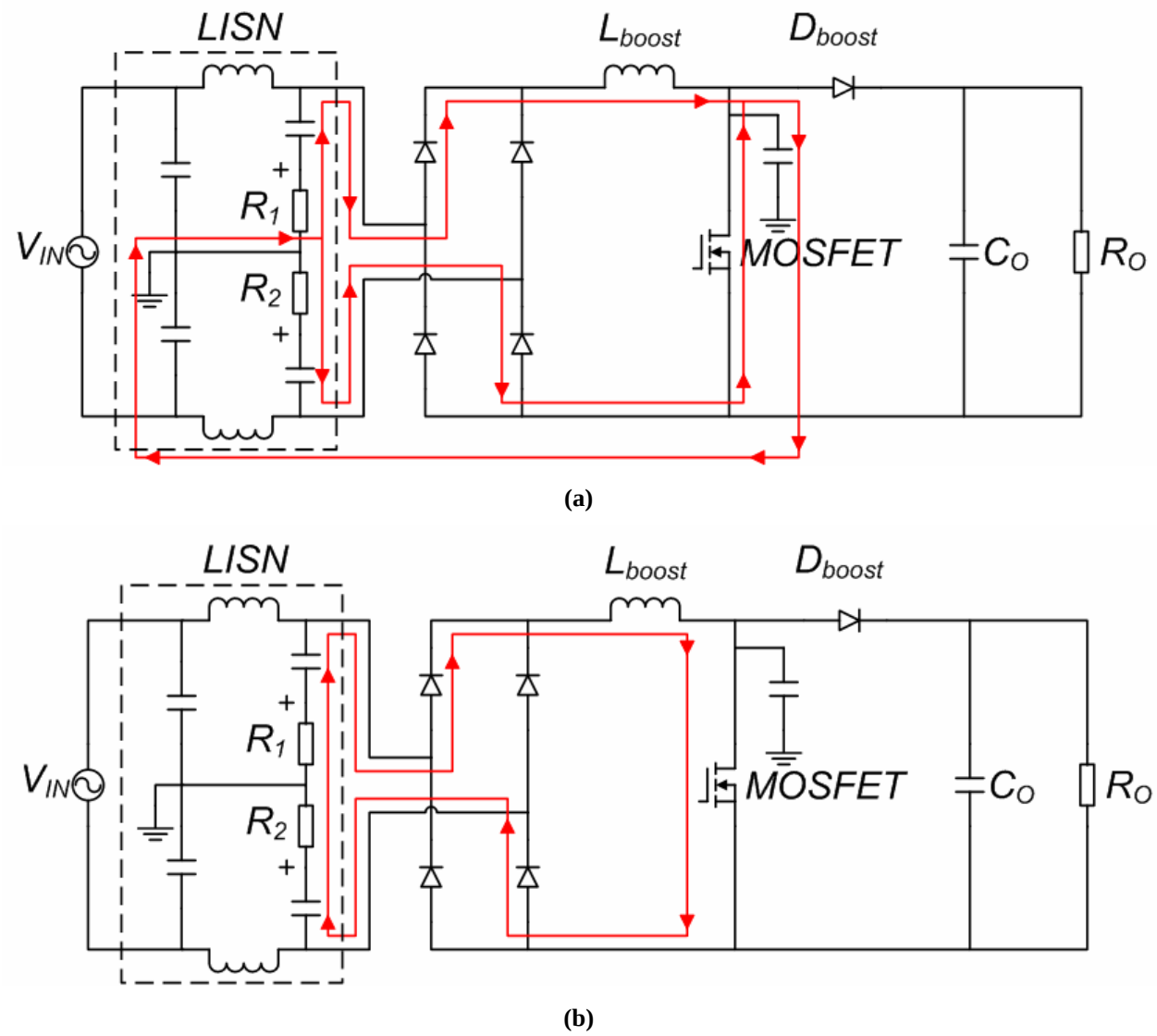


Fig. 1.5: A path for (a) CM and (b) DM noise in a power factor correction (PFC) boost converter.

In order to measure EMI that provides reproducible results and to be in compliance with the standards a line impedance stabilization network (LISN) is used. Also shown in Fig. 1.5 the LISN is composed of passive components and designed to filter out any outside noise in the system and only measure noise emitted and propagated related to the device under test (DUT). A LISN provides a nearly pure resistive component – 100 Ω and 25 Ω for DM and CM, respectively – at the input of the DUT over the frequencies in question for conducted EMI. Likewise at frequencies below the conducted range the LISN passes the power. The voltage is measured across the two resistors R_1 and R_2, where the CM and DM EMI are calculated using equations 1-1 and 1-2, respectively.

$$V_{CM} = \frac{V_{R_1} + V_{R_2}}{2} \tag{1-1}$$

$$V_{DM} = \frac{V_{R_1} - V_{R_2}}{2} \tag{1-2}$$

Voltages V_{R_1} and V_{R_2} are the total noise voltages measured across the LISN resistors, R_1 and R_2 respectively, as shown in Fig. 1.5.

A front-end converter is a particular type of converter in which it is essential to have superior EMI characteristics [9]. Fig. 1.6 is a distributed system driven from an AC supply (utility grid) that has many DC loads. The front-end converter is comprised of the first two converters, the power factor correction (PFC) circuit and the pre-regulator.

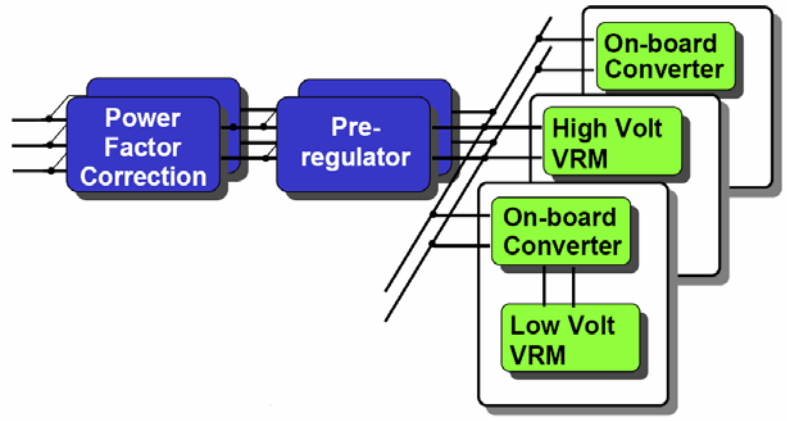


Fig. 1.6: An example of a distributed power system. The (darker) blue block signifies the front end converters, and the (lighter) green blocks are the loads.

The first aspect of the front-end converter is the PFC circuit. Typically the PFC is of a boost type and regulates its output at about 400V with unity power factor at the input [20, 21]. This is needed in many electronic loads at the front-end to maintain the integrity of the system with sinusoidal currents in phase with the voltage. Although the PFC circuit regulates its output voltage at 400V it is not a very precise voltage due to fundamental energy conservations and the primary operation of the converter to provide unity power factor. A second converter, that takes the 400V output from the PFC circuit, provides a very precise and robust output voltage for the DC bus: this converter is the pre-regulator. The front-end converter is the primary link between the loads and supply. This link can be the path for conducted EMI to corrupt the integrity of the system as well as impair the performance of the loads. Although any converter needs to have

adequate EMI characteristics, due to the mentioned importance of the front-end conversions EMI performance, a PFC converter will be used to look at in more detail.

Passive filtering is the most common type of filtering of EMI attenuation. In order to attenuate switching frequencies the cut-off frequency of the EMI filter must be low enough. With the inherent functionality of passive components the higher frequency characteristics become less ideal due to the parasitics and the EMI can no longer be attenuated; in fact, it can produce other resonances in the EMI. This causes the need for a second filter stage to attenuate at frequencies higher than the bandwidth of the first; typically above 1 MHz.

In order for an accurate design of the filter some form of modeling must be available. It is the focus of this work to build upon previous models and extract a new and potentially easier to use model for design purposes.

1.2. PREVIOUS WORK

Modeling of a converter's parasitic impedances has been done in a variety of ways and is constantly improving [22-27]. It is not the objective of this work to create a new approach for modeling the converter's EMI characteristics, but rather determine the key components that affect the EMI and study the characteristics of a converter with a filter, specifically a transmission-line filter.

A variety of integrated low-pass filters are proposed in [28]. A study of 16 designs were completed all using planar processing technologies. The work showed that complex structures containing ferrite or magnetic low σ material are not required to realize a desired attenuation. In fact the least complex structure exhibited the highest attenuation, despite its relatively small high frequency resistance. With this information an integrated transmission-line EMI filter for usage in integrated power electronics has been proposed in [29] and experimental results presented in [30].

Previous modeling methods using distributed transmission line theory focuses on the modeling of the transmission-line filter in the frequency domain only. Initial models were developed in [31, 32] using multi-conductor generalized transmission line theory [33]. This approach provides the impedance of each conductor within the filter. The impedance is defined not only by the self resistance and inductance but coupling with the other conductors in the system. In addition to the resistive and magnetic coupling, the capacitive coupling is also

accounted for. Although this method produces good results there are some downfalls to it. For example, this method does not take into account the proximity effects between the conductors; rather only the skin effect within each conductor. Inductance is only calculated at a given frequency and is not considered to change as a function of frequency. This causes the models accuracy to decrease at higher frequencies. Finally, the solution is very complicated and often unable to converge due to the complexity of the system. With this in mind the multi-conductor generalized transmission line models were later improved in [34] with the use of a common ground and solved using even-odd decomposition. This also took into account the proximity effect and all impedances as a function of frequency; while improving the ability to solve the model.

1.3. OBJECTIVES

This work investigates the EMI produced by a power electronic converter, specifically a PFC converter. The goal of the work is to model the entire system from source to load in the time domain using commercial simulation tools. The model must be adequately accurate at high frequencies to properly model the EMI phenomenon. A transmission-line filter that behaves like an LC low pass filter, first introduced in [28] and modified in [31, 32], will be used to attenuate EMI. The filter uses transmission line theory to attenuate the CM and DM EMI at higher frequencies propagating through the converter. Attenuation of the filter will be shown in conjunction with the PFC converter where an accurate model is made and verified for discrete components on a printed circuit board (PCB). The modeling procedure can then also be expanded from the PCB to use with an active integrated power electronic module (IPEM) proposed in [1].

The filter and IPEM are both processed using comparable planar technologies and modeled in Ansoft's Maxwell [35] finite element method (FEM) software. The Maxwell Q3D, a package within Maxwell, model provides parasitic impedances of the active stage in the converter. Maxwell Q3D solves the parameters by the partial element equivalent circuits (PEEC) method. PEEC uses Maxwell's equations in their integral form and calculates the inductances and capacitances analytically based on the geometry [24, 25]. Furthermore, Maxwell Q3D does not take the relative permeability, μ_r, into account. This provides an accurate method for the parameters at lower frequencies; however, at higher frequencies the accuracy decreases. Since

FEM is extremely time consuming and requires vast amounts of computing resources for the extremely complex structure of the PCB and IPEM the PEEC method is chosen. Fortunately, the materials in the power stage allow for adequate results at the frequencies being studied where the transmission-line filter, however, does not and needs to be modeled using FEM.

Similarly, Maxwell Q2D solves the transmission line characteristics of the filter model. Maxwell Q2D is capable of accurate results at very high frequencies; it solves the parameters using the field equations and FEM. In addition, Maxwell Q2D takes into account more material properties, such as the relative permeability, μ_r, which has a large role in the skin depth and proximity effects of materials. The simple linear structure of the proposed filter allows for simple modeling in 2-dimensions.

These parasitic impedances offer an accurate model of the system that is useful in many facets of the design process. Given the increasing switching frequency trend that causes high dv/dt and di/dt slew rates in power converters it is important to have a precise impedance model. Characteristics such as the electrical stresses on the devices, thermal issues from losses in the system, and EMI are predicted with high accuracy [18]. This provides the means for an enhanced design process that allows for optimization of the system through methods such as parametric or sensitivity studies. Specifically, the conducted EMI noise is produced as a result of the switching in the active stage of the module and propagates throughout the converter [5, 36]. With the parasitics modeled the propagation of the EMI noise is characterized accurately.

The transmission-line filter's parameters drastically change as a function of frequency which makes it difficult to model with the converter in the time domain. The filter's impedances are achieved through Maxwell Q2D at various frequencies and then manipulated to simplify the filtering into a constant resistive-inductive-capacitive (RLC) filter model. This new model takes into account the filtering characteristics at all frequencies with use in the time domain. Therefore, the converter can be implemented using a circuit simulator to determine the effects with and without the filter.

In this work, the effects of the parasitic impedances of the power stage are modeled for both discrete and integrated versions and the effects of a transmission-line filter are studied. In Chapter 2, the modeling process of the system is delineated. It is created and performed using all commercial computer simulation software packages: a field simulator, electrical circuit simulator, and mathematical analysis software. The results and experimental validation of the

modeling and system simulations for the discrete power stage are provided in Chapter 3. The simulations present a detailed breakdown of the effects of the EMI filter in the system. Confirming the simulations provide the means to utilize the modeling method for other applications. Finally, Chapter 4 summarizes the modeling and experimental data and discusses some future topics to be studied based on the findings.

2. MODELING APPROACH

Providing the correct dimensions, material parameters, and boundary conditions Maxwell Field Solver can extract the structural impedances of the power stage, whether it is a PCB interface or an integrated module, as well as transmission line parameters of a filter. These parameters can then be implemented in a circuit simulator for system level performances.

2.1. POWER STAGE PARAMETERS

Many methods for extracting parasitic impedances of a geometric structure have previously been reported, including impedance measurement, time domain reflectometry, and computer aided design [37-39]. Maxwell Q3D allows for a detailed 3-dimentional (3D) composition of the geometry (as seen in Fig. 2.4 and Fig. 2.8). Providing the correct dimensions, material parameters (σ and ε_r), and boundary conditions (defining conductors and current paths) Maxwell Q3D can extract the structural impedances of the geometry.

Maxwell Q3D provides a lumped impedance model of the parasitic self and mutual inductances, capacitances, and resistances of the given system. Inductances and resistances are calculated between the terminals of the system: which define the current paths. The capacitances are then calculated between each conductor, including capacitances to a common ground. This model can then be implemented in Simplorer [40], a commercial circuit simulator tool, to analyze transient and frequency domain responses, EMI characteristics, and parametric studies of the system.

Provided correct modeling of the geometry an equivalent circuit is produced to accurately depict the parasitics. Maxwell provides some flexibility with the topology of the equivalent circuit it will produce. Fig. 2.1a gives an overview of Maxwell's equivalent circuit. In this illustration, each current path has the resistances and inductances divided in two equal components (depicted as 'Half'); the capacitances (depicted as 'Parallel') are then connected to each current path in between the two 'Half' components. This example of the equivalent circuit is using two 'Half' components; Maxwell allows the user to choose the "number of modules" – denoted as '*M*' – which defines the number of 'Half' components (2 or greater). Therefore the number of 'Parallel' components is then defined as $M-1$. As this number increases the system behaves more like a distributed model at the cost of complexity.

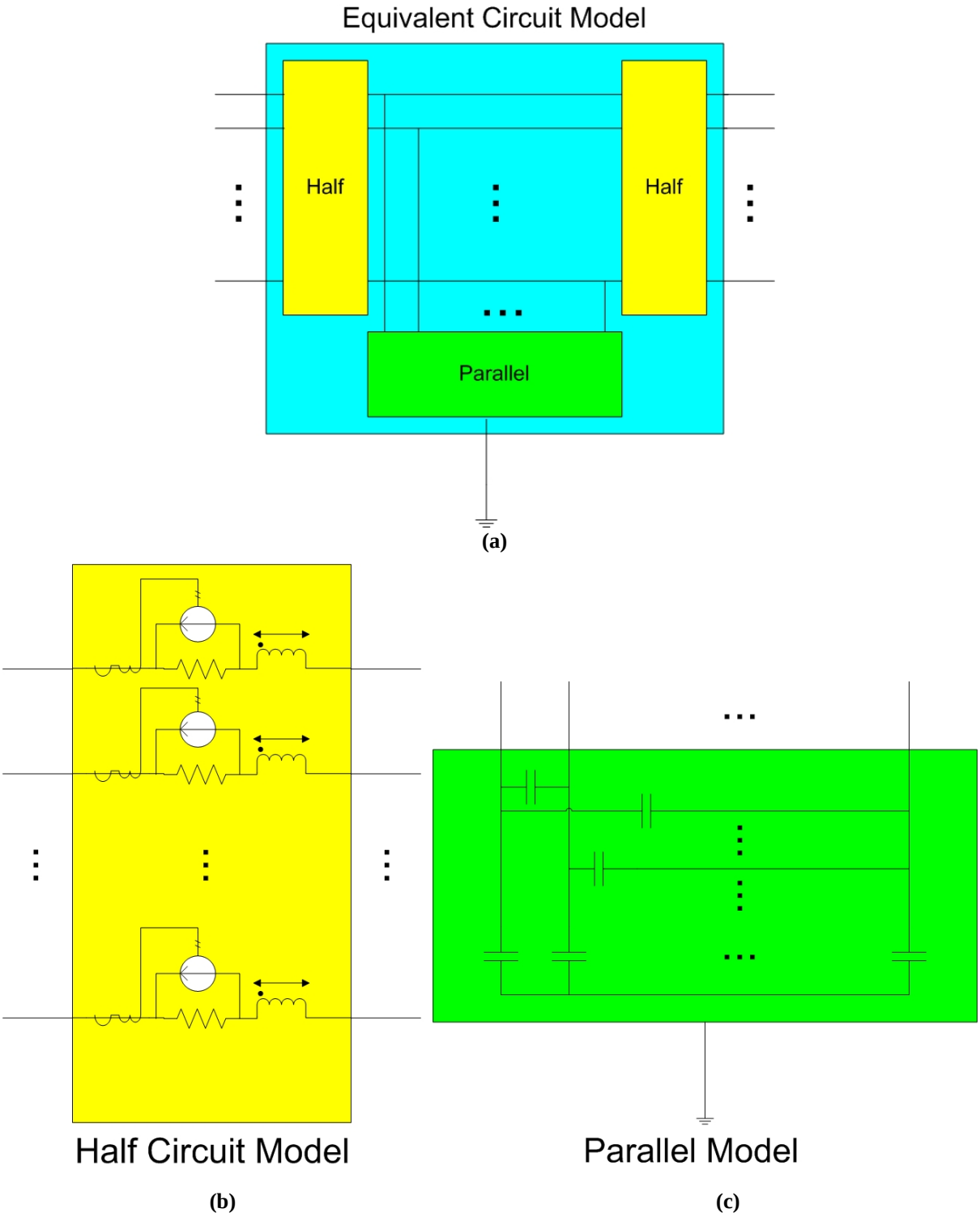
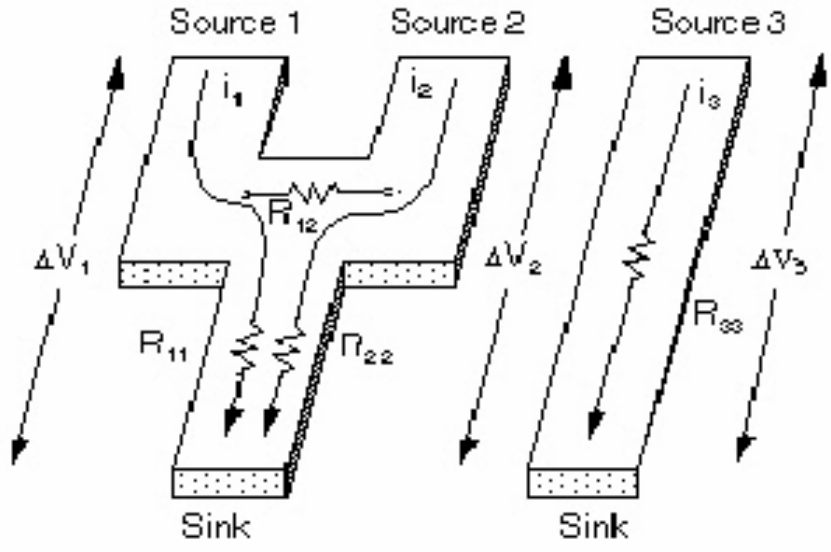


Fig. 2.1: Maxwell Q3D equivalent circuit schematic.

Each ‘Half’ module contains the resistance and self inductance of each current path defined in the system. Furthermore, the mutual inductance to every other current path is also defined in the ‘Half’ modules. In addition to the mutual inductances, a compensation for the resistances

within each conductor, or net, is included. The resistance compensation done in Maxwell Q3D can be for AC or DC currents. The DC currents in one conductor with multiple sources cause the need for an accurate current sharing. Similarly, for AC currents induced currents from one trace to another will affect the self resistance and in turn the mutual resistances. Maxwell accomplishes this compensation by sensing the current through each resistor and using a fraction of that current to adjust every other current path in the net. This modeling approach is shown in Fig. 2.1b and Fig. 2.2.



$$\Delta V_1 = i_1 R_{11} + i_2 R_{12} + i_3 R_{13}$$
$$\Delta V_2 = i_2 R_{22} + i_1 R_{12} + i_3 R_{13}$$
$$\Delta V_3 = i_3 R_{33} + i_1 R_{13} + i_2 R_{23}$$

Fig. 2.2: Maxwell Q3D diagram to show mutual resistance theory [35].

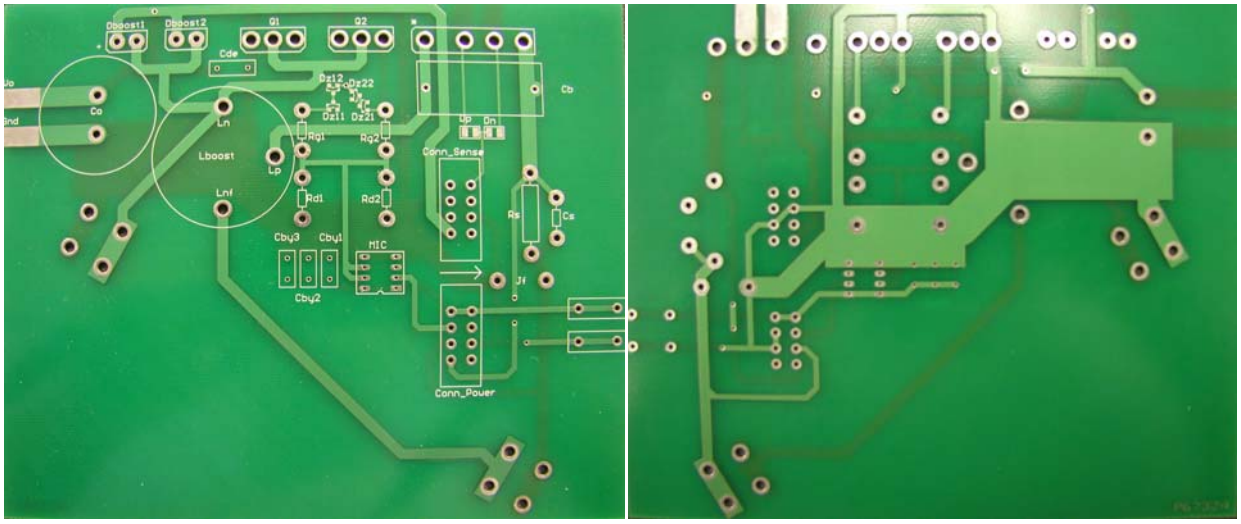
Finally, to complete the equivalent circuit model the capacitances are implemented. A capacitance between each current path is calculated as well as a capacitance from each path to a defined common ground. The capacitance module is shown in Fig. 2.1c.

2.1.1. PCB

Initially, a discrete version of the PFC converter will be modeled. The discrete converter uses a PCB board for its interconnections. In order to accurately model the electrical and magnetic coupling in the converter the parasitic parameters of the PCB will be modeled using Maxwell Q3D.

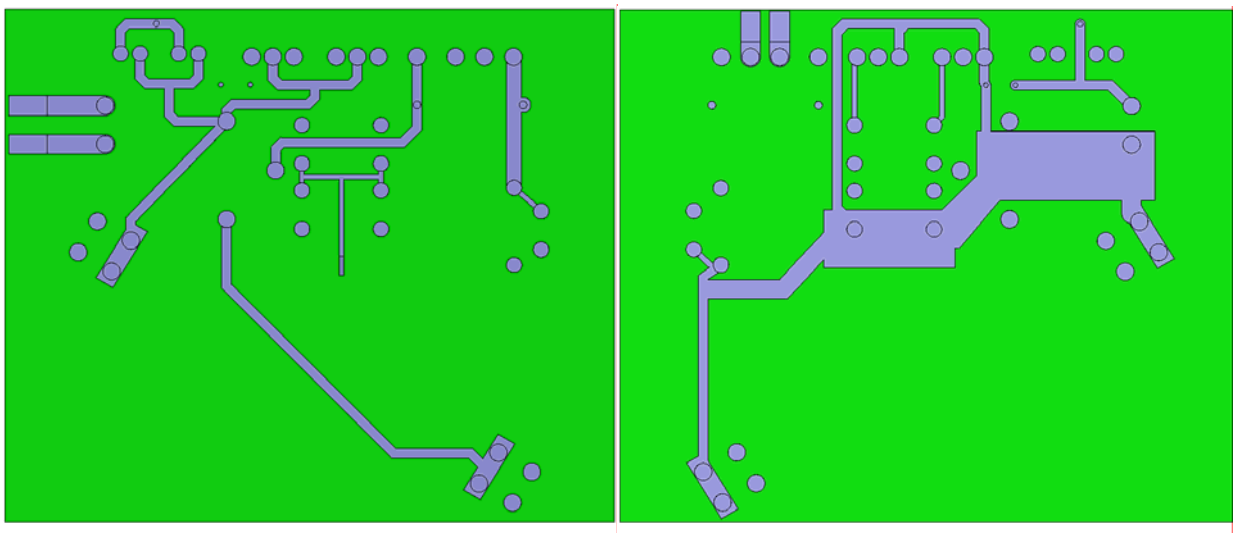
The PCB was designed with a few basic features. It is known [18] that the majority of common mode current is due to the capacitances from the active devices to a heatsink. Therefore, to simplify the modeling a simple common ground is implemented: one heatsink. It will be used to extract heat from all the devices: diode bridge, 2 MOSFETs, and 2 diodes. In

addition to the need for a simple common ground it is mandatory to implement the transmission-line filter without excessive interconnect impedances. The filter can easily be placed before the diode bridge using the inputs to the converter. However, a more difficult task is to implement the filter in between the diode bridge and the boost inductor. This was accomplished with the use of auxiliary traces to connect the filter. The rest of the PCB design was based on the proper operation of the converter. The PCB is pictured in Fig. 2.3, with the Maxwell model in Fig. 2.4.



(a) Top side of PCB **(b) Bottom side of PCB**

Fig. 2.3: PCB used for discrete boost PFC converter.



(a) Top side of PCB **(b) Bottom side of PCB**

Fig. 2.4: Maxwell Q3D geometry of the PCB power stage of the boost PFC converter.

With a proper design and correct modeling in Maxwell Q3D the impedances of the traces can be extracted. Due to the large number of interconnects and complexity of the power stage board, approximations must be made. When considering simplicity and simulation time, the number of current paths, *N*, defines the complexity of the system. When the number of current paths increases the Maxwell simulation will take longer, but the majority of the increased simulation time will be in the time domain simulations of the lumped parameters. As discussed in Section 2.1 each current path has two resistors and inductors (when *M*=2), producing $2 \cdot M \cdot N$ components. Mutual inductances and capacitances produce $M \cdot \left(\sum_{k=1}^{N-1} k \right)$ and $(M-1) \cdot \sum_{k=1}^{N} k$ components, respectively, between every current path. Furthermore, there is a compensation for resistances in the same conductor. As stated earlier, if there are more than 2 current paths in the same conductor an ammeter is added to sense the current through each path, which is used to compensate the resistances within that net. This characteristic is not as straight forward to generically show the complexity of the system since it depends on how many different nets and how many paths are in each net. In the PCB model there are 10 different nets with 1, 1, 1, 1, 2, 3, 4, 4, 4, 9 current paths for the different nets. This gives $2 \cdot (2+6+12+12+12+72) = 232$ resistance compensation components, respectively, in addition to the 26 ammeters needed, for a total of 258 components for this resistance operation.

For example, a model with M number of 'Half' modules, N current paths the number of circuit components, x, used to model the geometry is given by equation 2-1 (not including the resistance compensations).

$$\begin{aligned} x &= 2 \cdot M \cdot N + M \cdot \left(\sum_{k=1}^{N-1} k \right) + (M-1) \cdot \sum_{k=1}^{N} k \\ &= 2 \cdot M \cdot N + M \cdot \left(\frac{1}{2} N(N-1) \right) + (M-1) \cdot \frac{1}{2} N(N+1) \\ &= \left(2 \cdot M - \frac{1}{2} \right) \cdot N + \left(M - \frac{1}{2} \right) \cdot N^2 \end{aligned} \tag{2-1}$$

From equation 2-1 the plot in Fig. 2.5 illustrates how quickly the solution can become very complex and increases simulation time respectively.

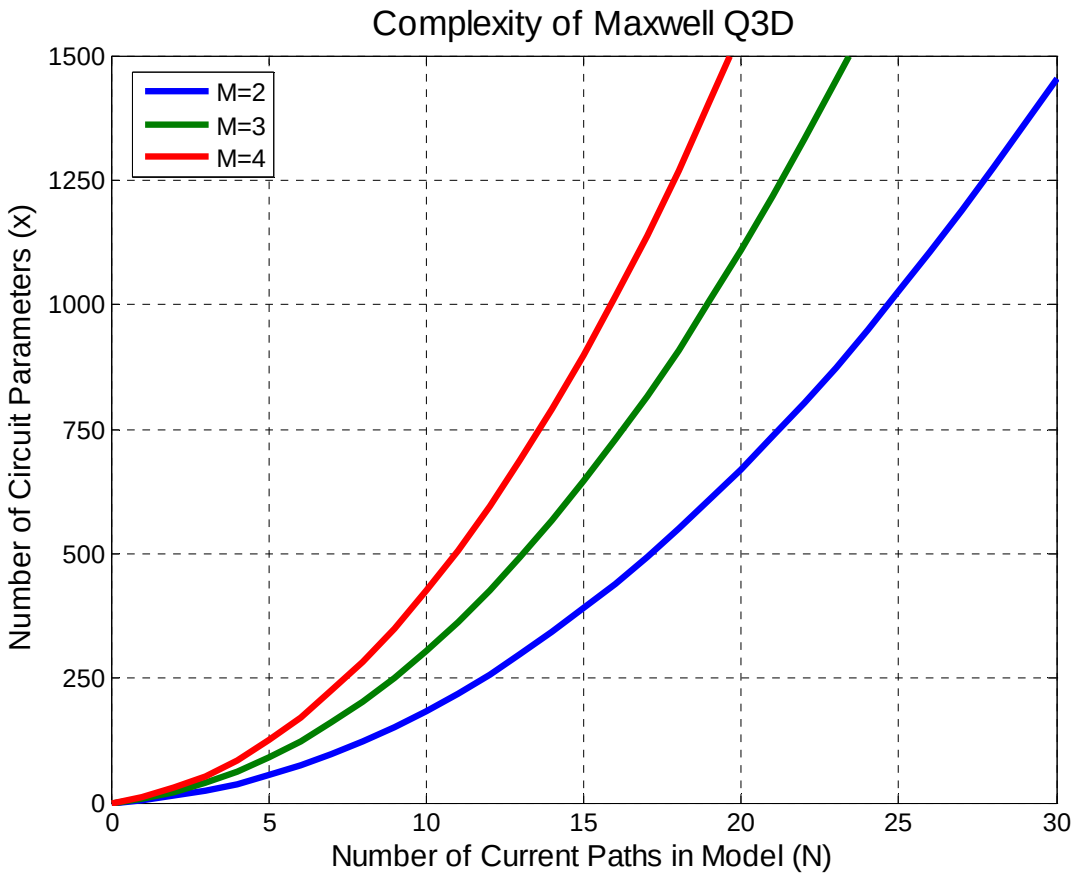


Fig. 2.5: Complexity of a Maxwell Q3D model.

Any approximation or simplification of the model must be in such a way as to not affect the characteristics of the PCB and its impact on the circuit. For simplicity reasons it is chosen to have M=2. One of the most dominant ways to reduce the complexity is to decrease the number of current paths defined by the system. The following paths/traces (numbers shown in parentheses are the number of paths removed) were simplified from the original model:

(2) Gate resistors to MOSFETs removed (incorporated in MOSFET models)

(3) Gate/static resistors lumped together as one terminal (where the gating signal is applied)

(1) Ground of gate signal located to a nearby ground

(1) Ground of static resistors lumped together as one terminal

(1) Decoupling capacitor's negative pin located to a nearby terminal

(2) Output capacitor to output/load terminals removed

(2) Sense resistor/capacitor on same terminals

(2) Capacitor, Cb, to DC side of diode bridge together as one terminal

(2) AC Input to Diode bridge removed

This simplification alone reduces the number of current paths from 30 to 14; therefore, reducing the number of components from 1455+258=1713 to 343+71=414 (value from equation 2-1 + components form resistance compensation). Another further simplification is to remove the components that have insignificant values. The following reduction (numbers shown in parentheses are the number of components removed) was also done:

(106) Mutual inductance values less than 10% of the self value

(16) Resistance compensation values less than 10% of the self value

(54) Mutual inductance values between 10-30% of the self value

(14) Resistance compensation values between 10-30% of the self value

(72) Capacitances less than a 10^{-15} F (fF)

Removal of the smaller valued components further reduces the number of components from 414 to 111+41=152 components. Note that all resistances and inductances remained in the model. The overall reduction of components is from 1713 to 152. This simplifies the number of components in the model to less than 9% of the original version; a more than an order of magnitude in the model simplification.

A simplified schematic of the final model is given in Fig. 2.6. The figure does not include any mutual resistive, inductive or capacitive values.

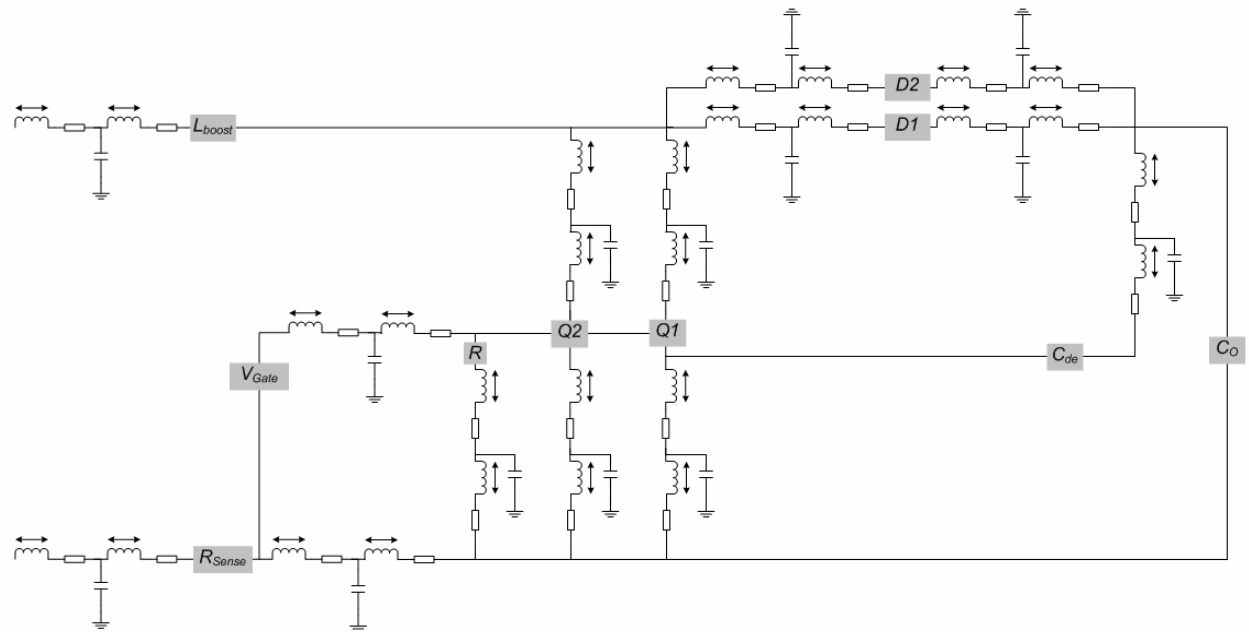
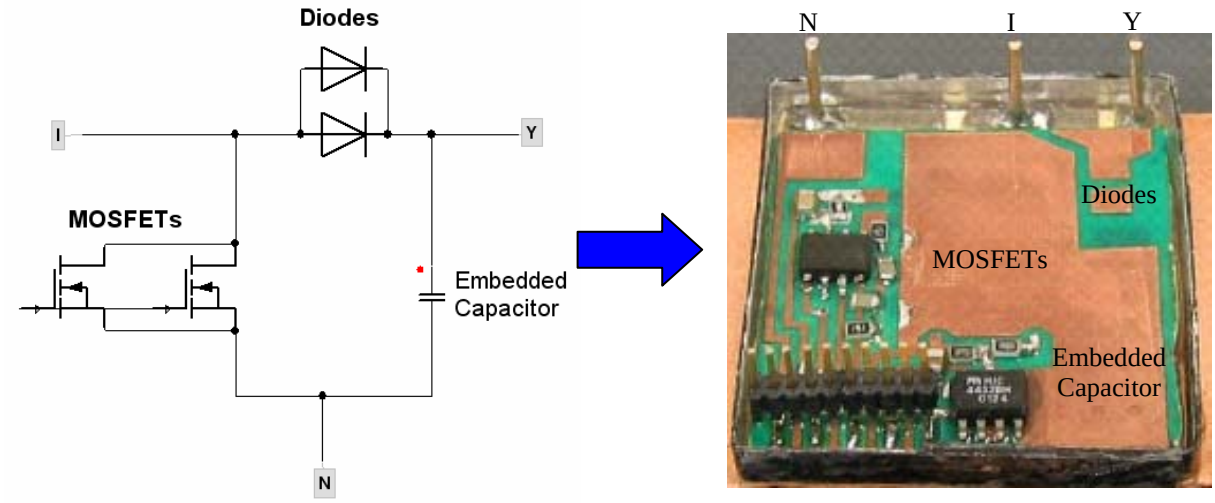


Fig. 2.6: Simplified schematic of PCB parasitic model.

2.1.2. IPEM

Given the validity of the Maxwell Q3D model – that will be determined in Chapter 3 – a model for the active IPEM stage can be extracted as well. The IPEM contains two MOSFETs, two diodes, and an embedded capacitor as illustrated in Fig. 2.7a. All the active components are then interconnected using planar technologies into a single module [1]; an IPEM can be seen in Fig. 2.7b, with the Maxwell model in Fig. 2.8.



(a) Ideal schematic of active IPEM **(b) Active IPEM stage for boost PFC**

Fig. 2.7: Layout of the active IPEM of a boost converter.

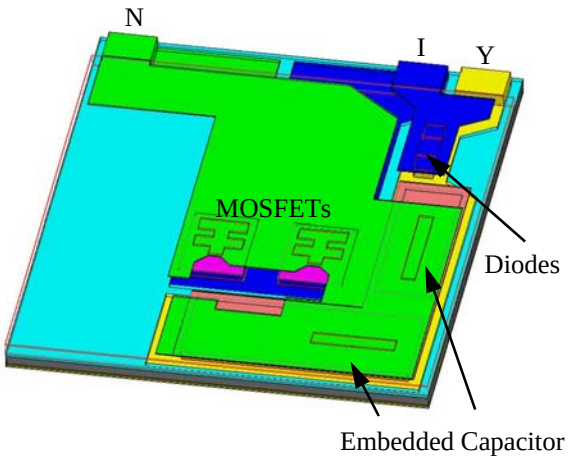


Fig. 2.8: Maxwell Q3D geometry of the active IPEM for the boost PFC converter.

TABLE 2.1 shows the geometric and electrical properties of the IPEM modeled on the double bonded copper (DBC) substrate.

TABLE 2.1: COMPONENTS USED IN IPEM MODULE

Part	Part Number (quantity) / Thickness (mil)	Description
CoolMOS™	SPW20N60C3 (2)/10 mil	600 V / 20A
SiC Diode	SDP06S60 (2)/15.75 mil	600 V / 6 A
Copper	3	Top metallization layer
Polyimide	5	Top surrounding layer
Al_2O_3	25	Middle surrounding layer
Polyimide	5	Bottom surrounding layer
Copper	10	Top DBC layer
Al_2O_3	25	Middle DBC layer
Copper	10	Bottom DBC layer (GND)

The IPEM module defines the parasitic impedances involved in the schematic of Fig. 2.7. Similar to the PCB, between each connection a resistance and inductance is found, including the mutual inductance between each current path. Likewise, the capacitance is also found between each conductor in the circuit. Fig. 2.9 displays a schematic model of the active IPEM module. As with Fig. 2.6, this figure does not show the mutual inductance between each inductor or the mutual capacitance between each conductor; only the capacitances to ground—bottom DBC copper—are shown. However, all parameters are accounted for in the simulations.

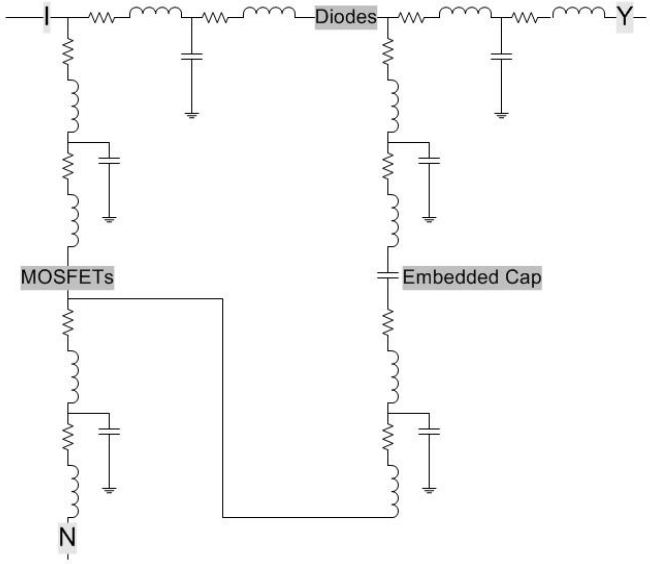


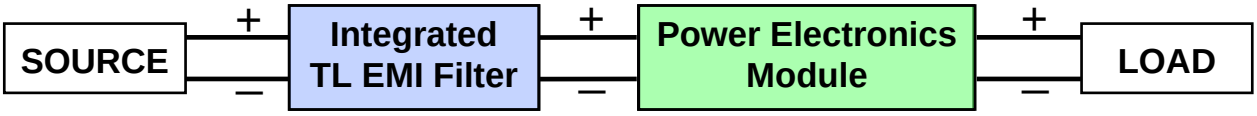
Fig. 2.9: Simplified model of the parasitic impedances in the IPEM.

Similar approximations that were done with the PCB model were also done with the IPEM model. However, it is not as crucial since there are considerably less current paths (6) and nets (3) involved with the IPEM.

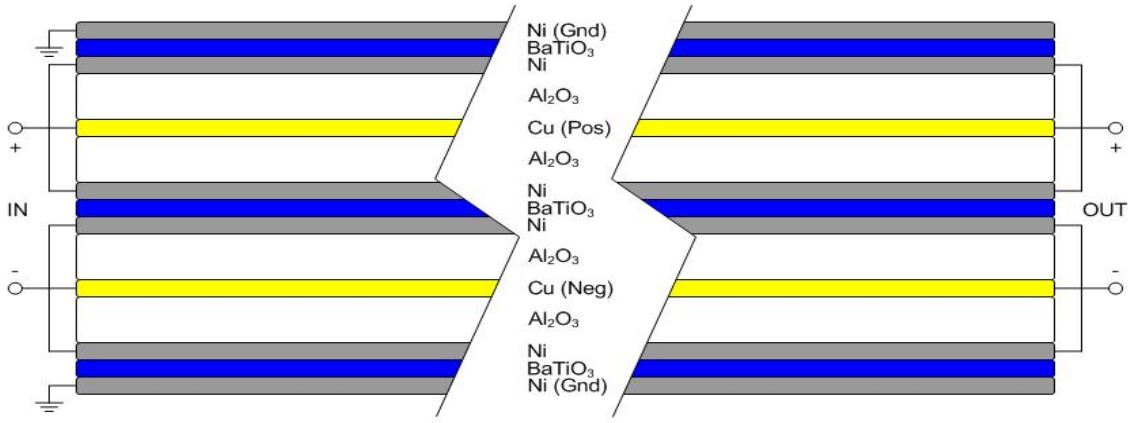
2.2. FILTER MODEL

2.2.1. Introduction to Transmission-Line EMI Filters

Provided the parasitic impedances of the system are modeled and the EMI characteristics are accurately determined the effects of a filter in the system is now desired. The implementation of the filter in a power electronic converter is shown in Fig. 2.10a. Furthermore, the longitudinal illustration of the RF filter is given in Fig. 2.10b; the operation of the filter is discussed in [32]. The filter is manufactured with the properties in TABLE 2.2. A detailed description of the fabrication process for planar processing techniques, specifically for the transmission line filter, is given in Appendix A – Filter Fabrication.



(a) System view depicting location of transmission-line (TL) filter in converter



(b) Longitudinal cross-section view of filter

Fig. 2.10: Integrated transmission-line EMI filter.

TABLE 2.2: PARAMETERS OF PROTOTYPE TRANSMISSION-LINE FILTER

Length	100 mm
Width	10 mm
Copper bus thickness	254 μm
Nickel thickness	17 μm
$BaTiO_3$ thickness (DM/CM)	150/300 μm
Al_2O_3 thickness	635 μm
ε_r of $BaTiO_3$	14,000
μ_r of Nickel (estimated)	100

Let it be noted that the relative permeability of nickel can vary greatly, $50 \leq \mu_{r,Ni} \leq 600$. The permeability depends on many parameters such as the method of plating or purity of materials used in the process. With this known, the exact value cannot be determined simply, so a standard value of $\mu_r = 100$ is chosen for all nickel materials in the filter.

Due to skin and proximity effects the circuit parameters vary as a function of frequency. Although Maxwell Q2D can determine the impedances as a function of frequency, implementing these parameters in a time domain simulation is not trivial. Therefore, before the filter can be used in a transient system level simulation, an intermediate step must be performed.

In Simplorer, a small signal frequency sweep can be commutated to determine the attenuation as a function of frequency. With the use of lookup tables that vary the impedances as a function of frequency an accurate frequency response of the filter is determined. This alone still does not facilitate the performance of the filter with the variable parameters in the time domain; however, the frequency response can be used as a guide to create a constant parameter filter model. Matlab, by Mathworks, [41] is used to manipulate the frequency response curve to fit a transfer function to the data. Within Matlab, a simple program was produced to create a constant RLC filter that attenuates the CM and DM noise according to the frequency responses produced from the small signal analysis in Simplorer. Transfer gain, input and output impedances are used to synthesize an impedance network with constant parameter that depicts the same filter that had impedances vary as a function of frequency. The Matlab program consequently produces a Simplorer netlist ready to be implemented. Finally, the filter is ready to be used in time domain simulations to determine the converters performance with and without the filter. The whole modeling process is illustrated in Fig. 2.11.

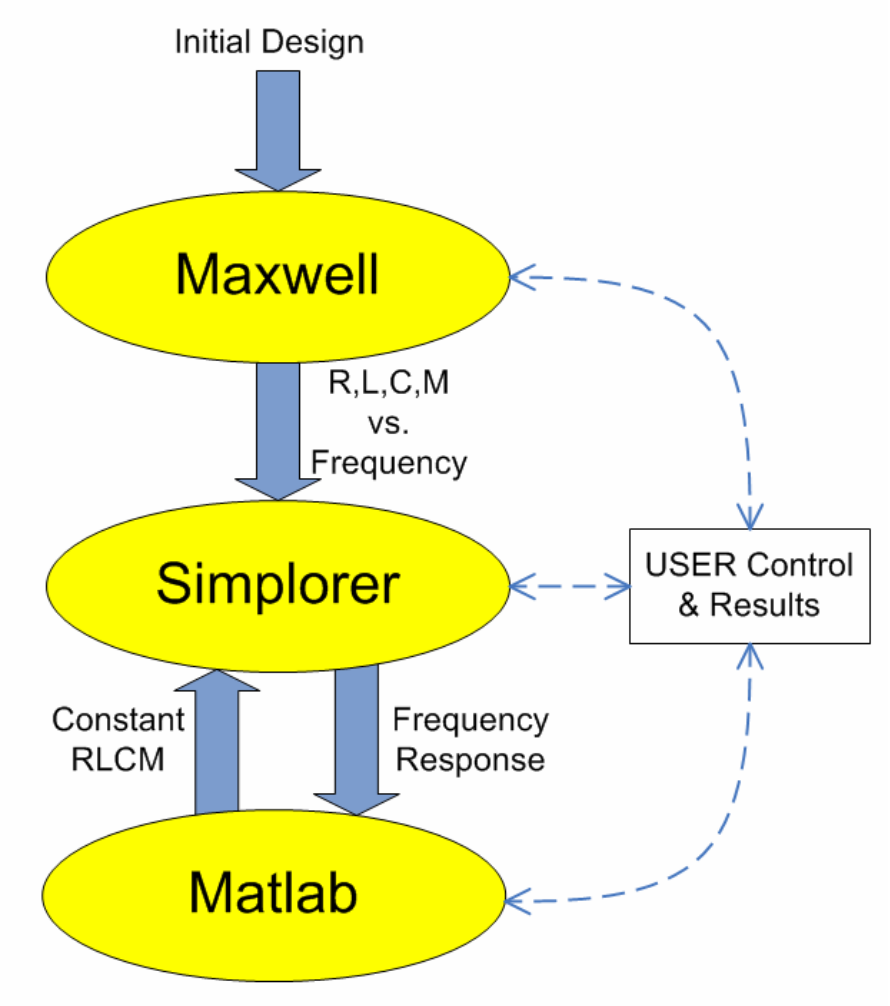


Fig. 2.11: Modeling process flowchart.

2.2.2. Field Solver

Maxwell Q2D is used to model the filter due to its simple geometry and the need for increased accuracy at higher frequencies. With the filter parameters in TABLE 2.2 the material properties are used in the same manner that they were for the 3D parameter extraction of the IPEM. After inputting the geometry (seen in Fig. 2.12 and Fig. 2.13), material properties (σ, ε_r, and μ_r), and boundary conditions (conductors and current paths) the resistance, self and mutual inductance, and capacitances are solved for. As stated earlier, using Maxwell Q2D allows the capability to accurately model the parameters versus frequency. Specifically, the inductances and resistances drastically change as a function of frequency. Once the electrical parameters are calculated at various frequencies the filter model is subsequently exported to Simplorer.

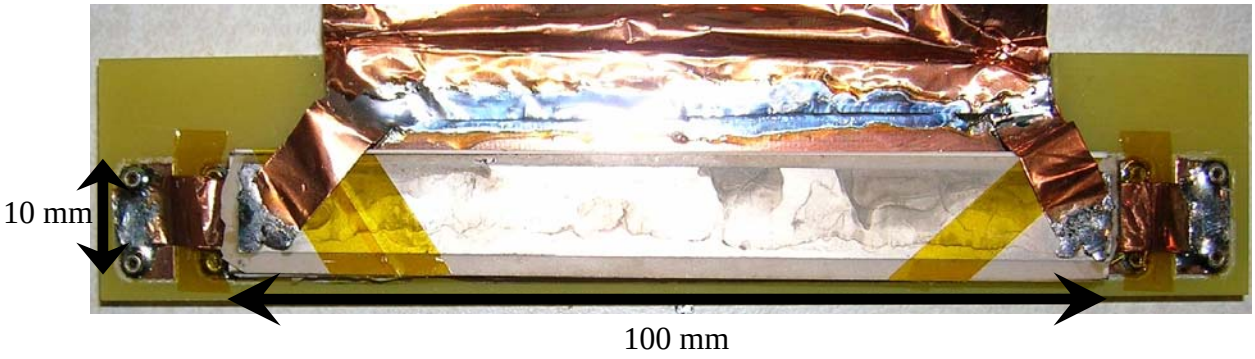


Fig. 2.12: Top view of transmission-Line EMI Filter.

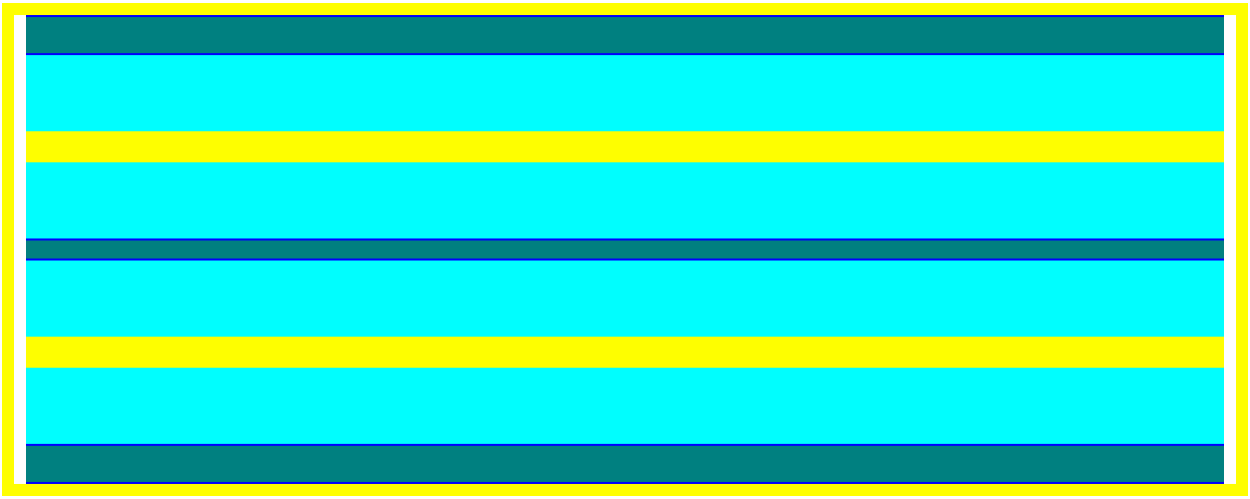
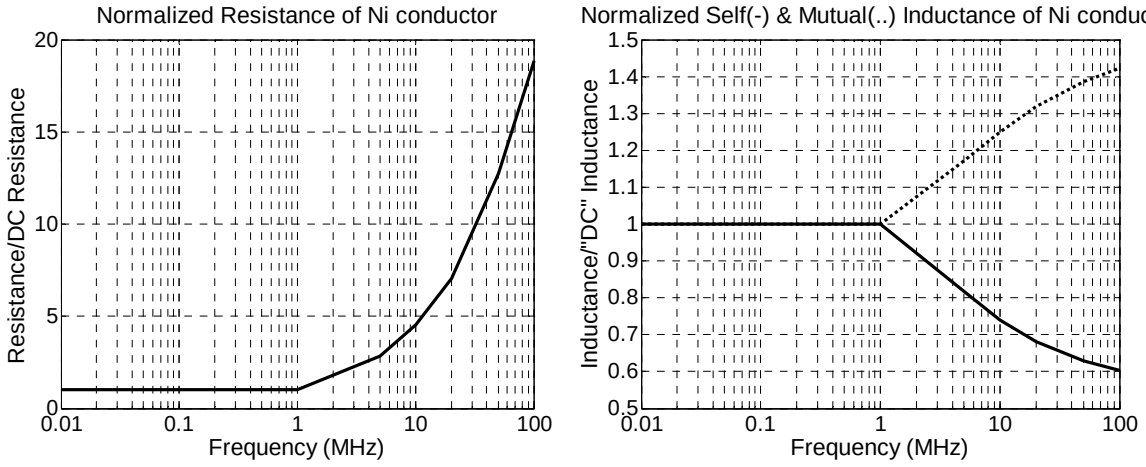


Fig. 2.13: Maxwell Q2D model of Transmission-Line EMI filter (Cross-section view).

2.2.3. Circuit Simulator

In order for an accurate attenuation model of the transmission-line EMI filter the electrical parameters resistance (R), self-inductance (L), and mutual-inductance (M), are calculated as a function of frequency. Fig. 2.14 plots the normalized impedance values as a function of frequency. The plots show that the impedances vary as much as an order of magnitude over the desired frequency range, thus confirming the need to account for these variations. Additionally, the impedances in Fig. 2.14 are for the top nickel conductor in the middle (DM) section of the filter.



(a) Resistance **(b) Inductance**

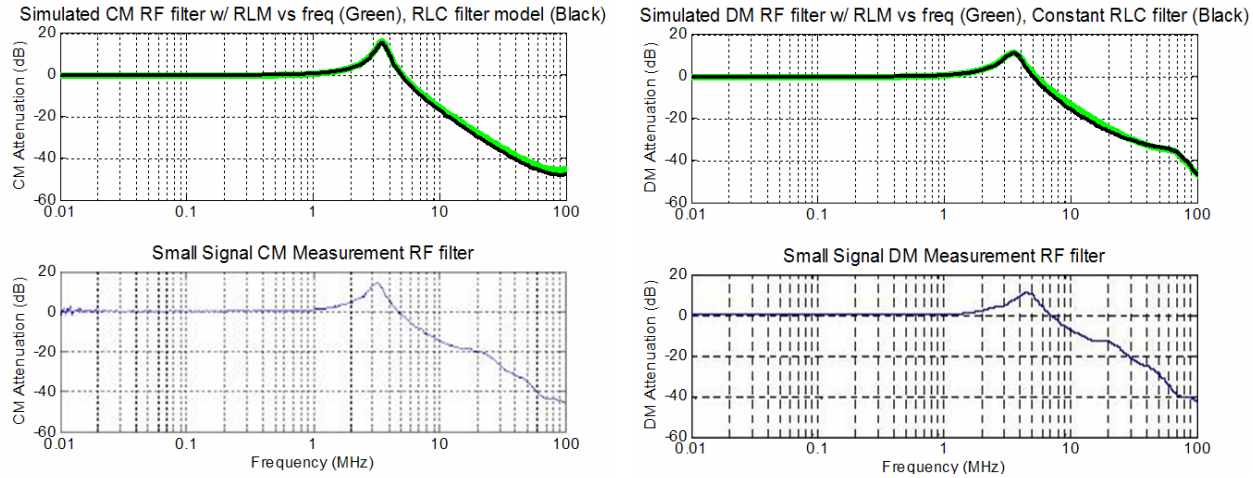
Fig. 2.14: Normalized impedance vs. frequency for top Ni conductor in the DM RF-EMI filter.

The impact of resistance of the Ni conductors is vital to the attenuation. As resistance increases the attenuation increases linearly. The mutual inductance is extremely important to the filters performance as well, even though it does not change as drastically as the resistance. As the mutual inductance increases the attenuation decreases. If the mutual inductance does not change with frequency and is maintained at its nominal, low frequency, value the attenuation at 100 MHz is increased by nearly an order of magnitude. Furthermore, the self inductance at 100 MHz changes to 60% of its nominal value. Self inductance does not effect the attenuation as much as the resistance or mutual inductance, however, the attenuation decreases as the function of the square root of the self-inductance increase. Therefore, it is critical that the parameters, R, L, and M, are modeled as they change with frequency. Additionally, the capacitances do not change as a function of frequency. Predominantly, the reason for the increase in the resistance of the Ni layer is due to the skin effect, which is enhanced with the increase of μ_r. The changes in the inductance values, however, are not as straightforward. Self inductance is composed of an internal and external component; when the spacing of two conductors is close the internal inductance dominates. The internal component is a function of the conductor's current distribution; the skin and proximity effects will increase the current densities at the periphery of the conductor, therefore causing a larger path or loop and likewise decreasing the self inductance [42]. As for the mutual inductance, when the skin and proximity effects dominate the crowding of the fields are on the edge of the conductor and therefore a greater coupling is achieved at these interfaces.

Given all the impedances at various frequencies, a table of each resistance and inductance versus frequency is created. These tables can then be used as lookup tables for the filter model's impedances. When a small signal frequency sweep is performed on the model the attenuation, input and output impedances of the filter as a function of frequency is then accurately captured.

2.2.4. Time Domain Approximation

After implementing the impedances varying as a function of frequency in Simplorer a resistive-inductive-capacitive (RLC) filter whose values are constant versus frequency is created in Matlab. The RLC filter is fit to the small signal response to the CM and DM filter operations. The top plots in Fig. 2.15 demonstrate the comparison of the constant RLC filter's attenuation with the transmission-line EMI filter's attenuation (using lookup tables). The lighter (green) curves are the data points from Simplorer with the parameters varying with frequency. The black curve is the response of the equivalent circuit that has constant impedances versus frequency. Furthermore, in [31, 32] the attenuation of the filter was verified using small-signal measurements as seen in the lower plots of Fig. 2.15. The PCB, IPEM and filter are now accurately modeled and implemented into the converter at the system level.



(a) CM attenuation **(b) DM attenuation**

Fig. 2.15: RF-Filter attenuation model simulation and measurement.

2.3. FINAL SIMULATIONS

Following the modeling of the PCB, active IPEM and transmission-line filter, simulations can be initiated to study the effects the filter has on the converter. The schematic in Fig. 2.16 is used for the simulations. The input voltage source is 120 V_{RMS} at 60 Hz. The PFC boost

converter operates at 1 kW with an output of about 400 V at a switching frequency of 400 kHz. Additionally, control for the circuit is based on classical PFC control theory [21], with the detailed control schematic given in Fig. 2.17. The circuit nominally operates with the waveforms provided in Fig. 2.18.

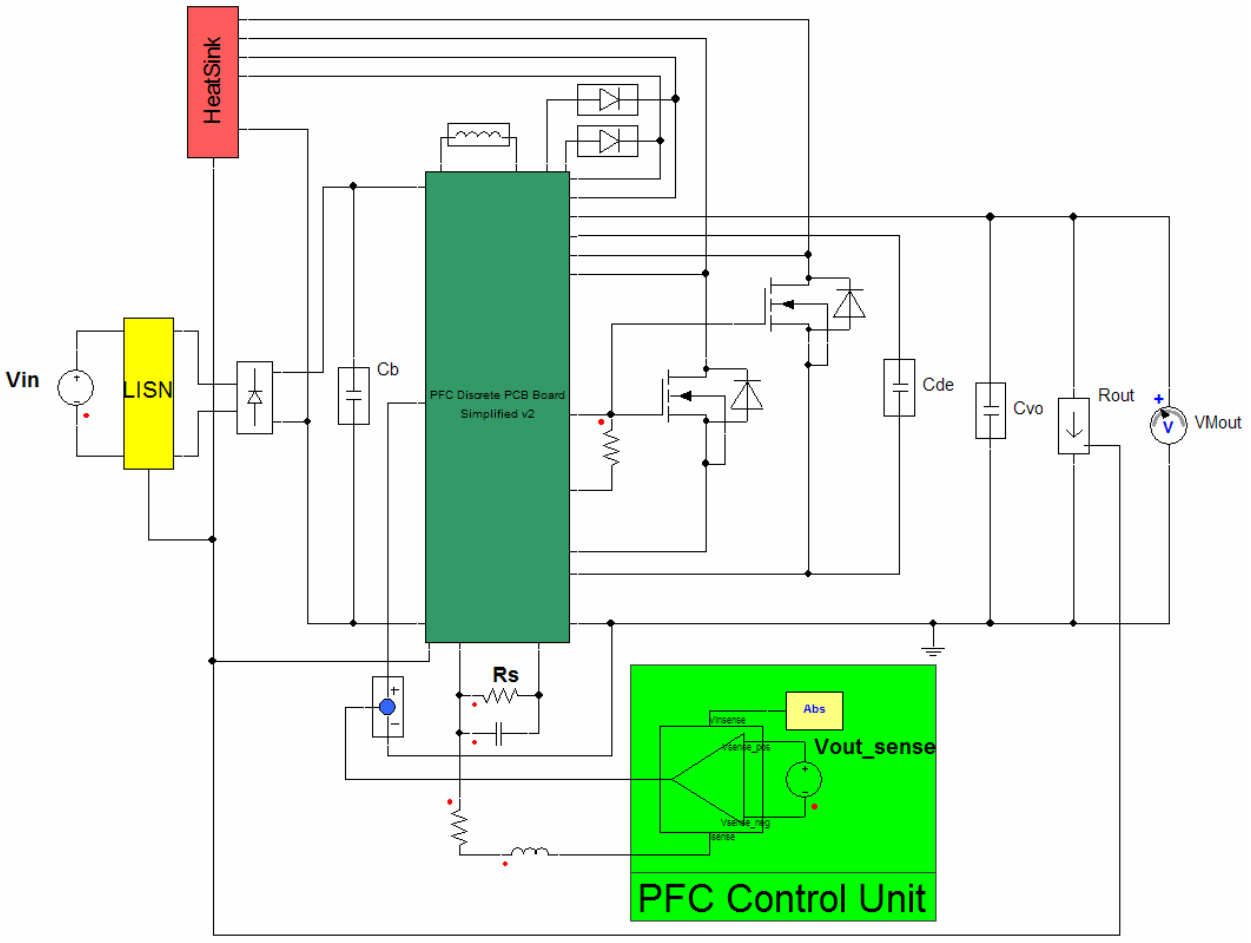


Fig. 2.16: System schematic of the PFC boost converter with PCB and all components modeled.

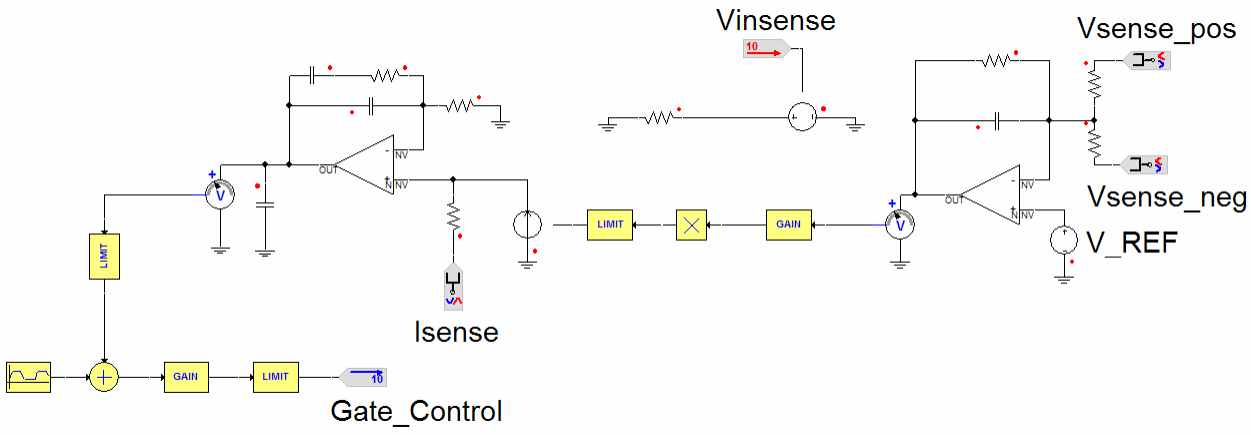


Fig. 2.17: Control Circuit for PFC Boost shown in Fig. 2.16.

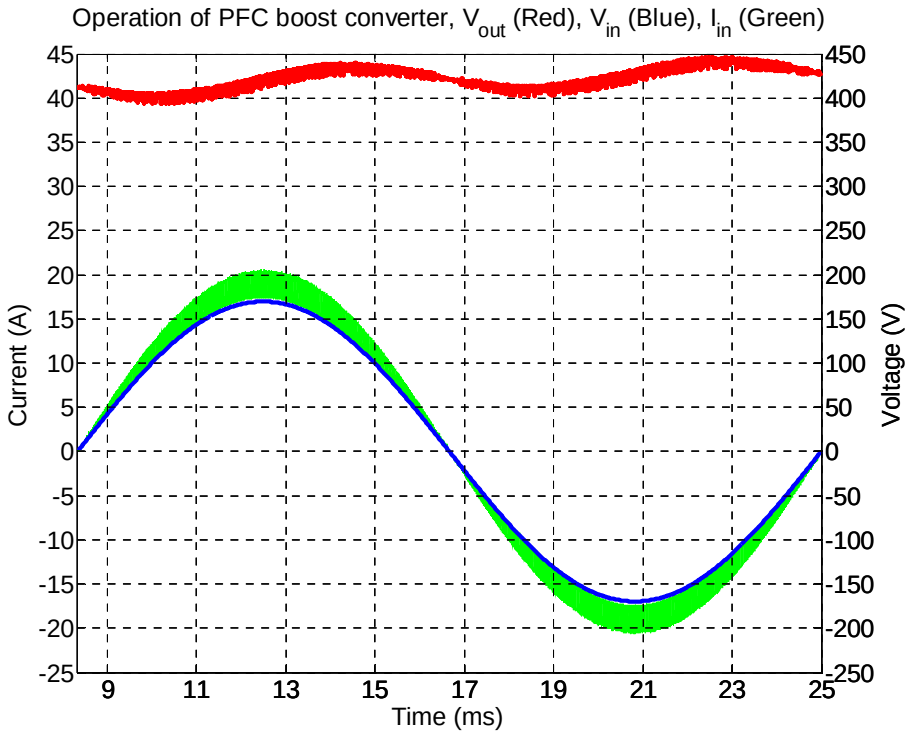


Fig. 2.18: Standard operation of the PFC boost converter with PCB and RF-EMI filter modeled.

In addition to the PCB modeling with the use of Maxwell Q3D, other parameters such as the capacitors, boost inductor, MOSFETs, silicon carbide (SiC) diodes, diode bridge, and the gate driver need to be accurately modeled as well. The converter is to be modeled up to 100 MHz with the attempt to be very accurate up to the 30 MHz EMI range as well as have the ability to visualize what is occurring after the EMI frequency range. This will provide the means to determine if it is necessary to shift the corner frequency lower if superior attenuation occurs above 30 MHz, and it will also allow the ability to shift various resonances or noise outside the 30 MHz range. Therefore, each component needs to be accurate up to this frequency. The passive component's impedances are measured using the Agilent 4294A impedance analyzer – accurate from 40 Hz to 110 MHz – and then an equivalent circuit is used to match the measurement. The active devices were modeled to match the datasheet values and figures.

The boost inductor is a critical path in the influence of DM noise [36]. The inductor's measured impedance (lighter green) and simulated impedance (black) are shown to nearly fully overlap in Fig. 2.19. Furthermore, the schematic model for the inductor is given in Fig. 2.20. The first two stages (on the left) of the boost inductor are used for modeling up to 30 MHz, similarly the last two stages (on the right) are for modeling at higher frequencies, up to 100 MHz and may be excluded if further simplification is desired.

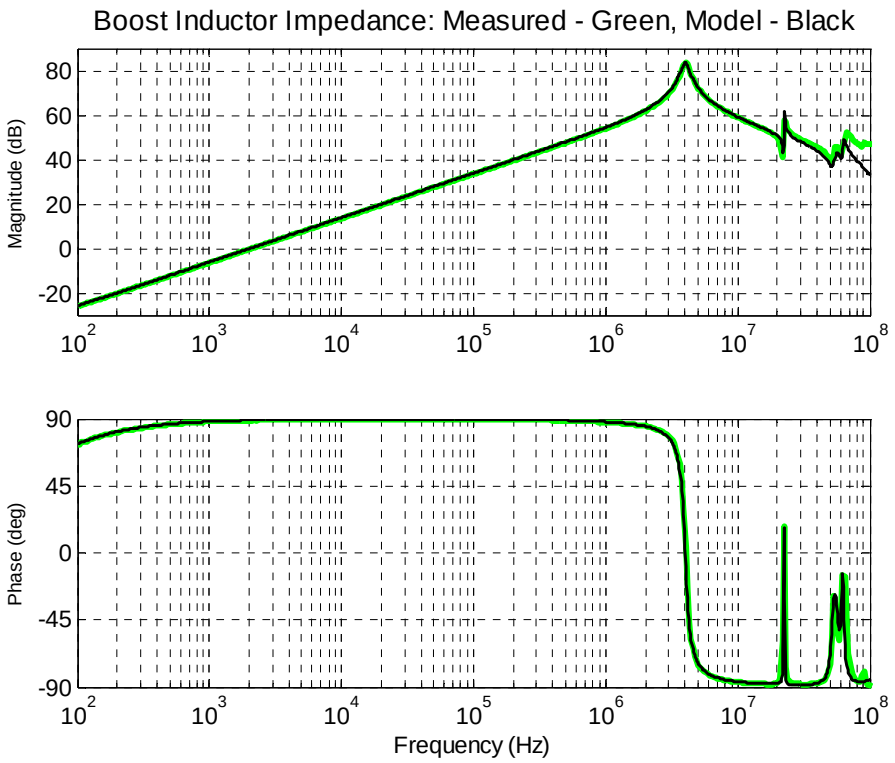


Fig. 2.19: Measured and simulated impedance of the boost inductor.

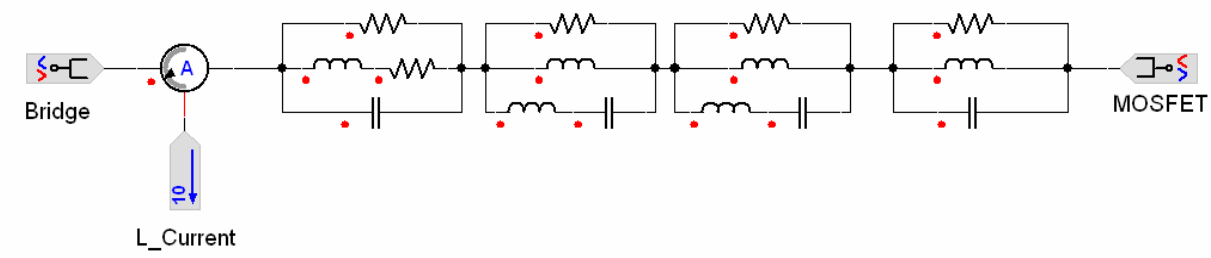
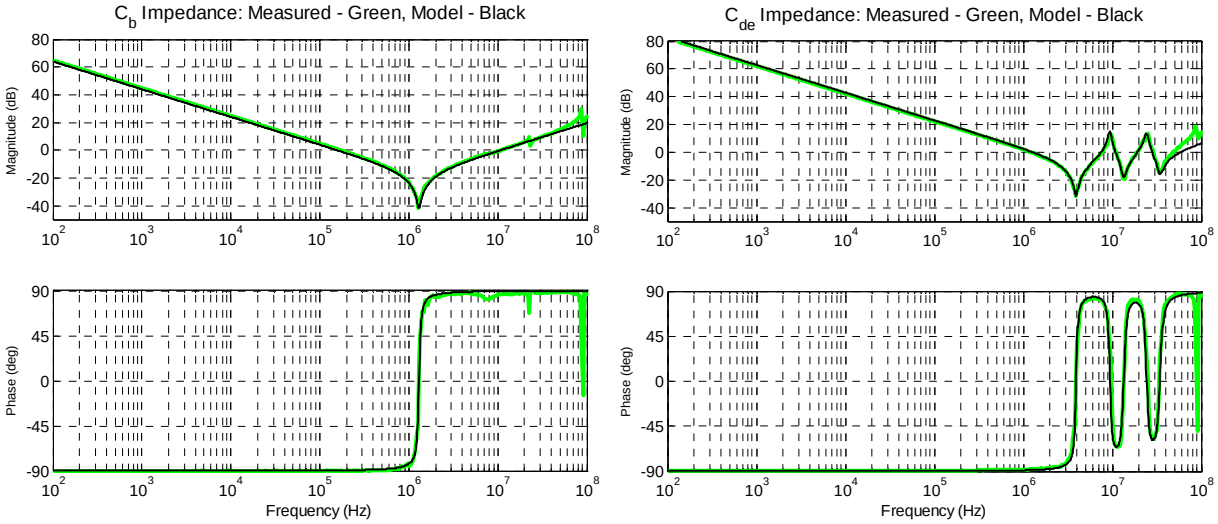


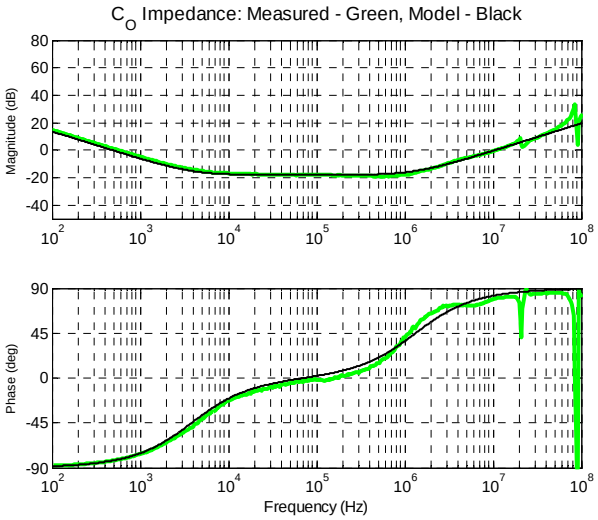
Fig. 2.20: Schematic of boost inductor.

Each capacitor was done in the same manner as the inductor. The capacitance was measured using the impedance analyzer and then modeled with an equivalent series resistance and inductance (ESR and ESL, respectively). The measured and simulated impedances of the capacitors are given in Fig. 2.21. Capacitors C_b and C_o are composed of one capacitor, while capacitor C_{de} is a combination of three capacitors to minimize the high frequency effects. Impedances of capacitor C_b is shown in Fig. 2.21a, C_{de} in Fig. 2.21b, and C_o is given in Fig. 2.21c. Additionally, the schematics of the capacitors are given in Fig. 2.22, respectively.



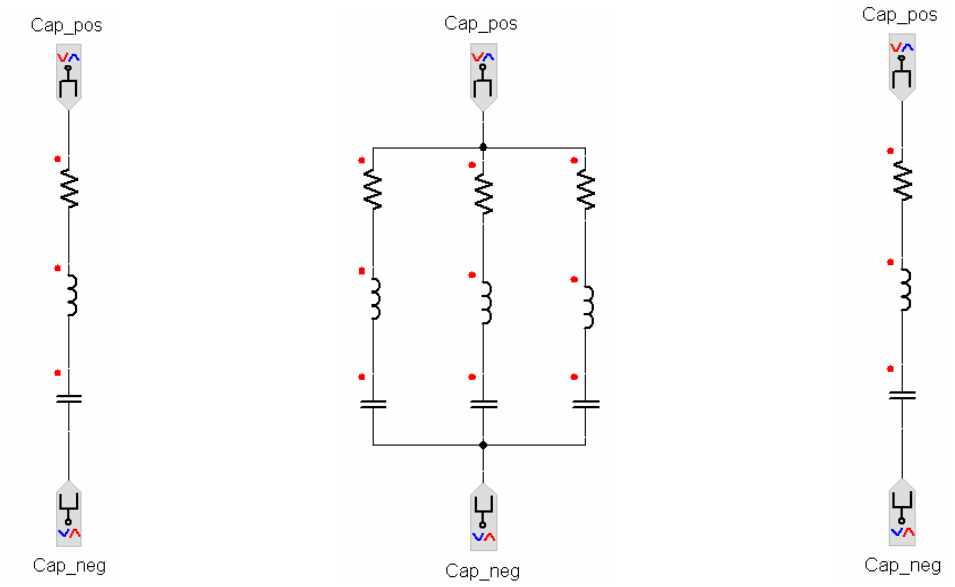
(a) Capacitor C_b

(b) Capacitor C_{de}



(c) Capacitor C_o

Fig. 2.21: Measured and simulated impedances of the capacitors in the system.



(a) Capacitor C_b **(b) Capacitor C_{de}** **(c) Capacitor C_o**

Fig. 2.22: Schematic of capacitors in the system.

The last set of capacitors needed is the capacitance from each active device to the heatsink (or the common ground). These values were again measured with the impedance analyzer and put in the system as ideal capacitors. The capacitance for the diode bridge to ground was 15 pF, while the capacitances from each diode were 30 pF and 31 pF and each MOSFET 58 pF and 61 pF. The accuracy of the measurement is hard to determine at this low of frequency. Even a small capacitance in the measurement equipment could affect the results. This capacitance is directly proportional to the magnitude of the CM noise. The system's common ground is defined as the heatsink within Maxwell. All capacitances are then connected to this same ground as well as the LISN ground.

The passive components in the system are the key elements in the propagation path of noises within the system. With the propagation paths modeled accurately the noise sources needs to be modeled as well. The noise sources are the active components such as the MOSFETs and diodes. The SDP06S60 SiC diodes have a device model provided by the vendor [43]. There are no models, however, provided for the SPW20N60C3 MOSFETs so a model was created using Simplorer's system level MOSFET. Simplorer's MOSFET model takes into account the non-linear capacitances, resistances (including gate resistance), inductances, voltage vs. current plots defining the linear and saturation regions, device limits, and the anti-parallel body diode as shown in Fig. 2.23. All parameters are created to match the device's datasheet [44].

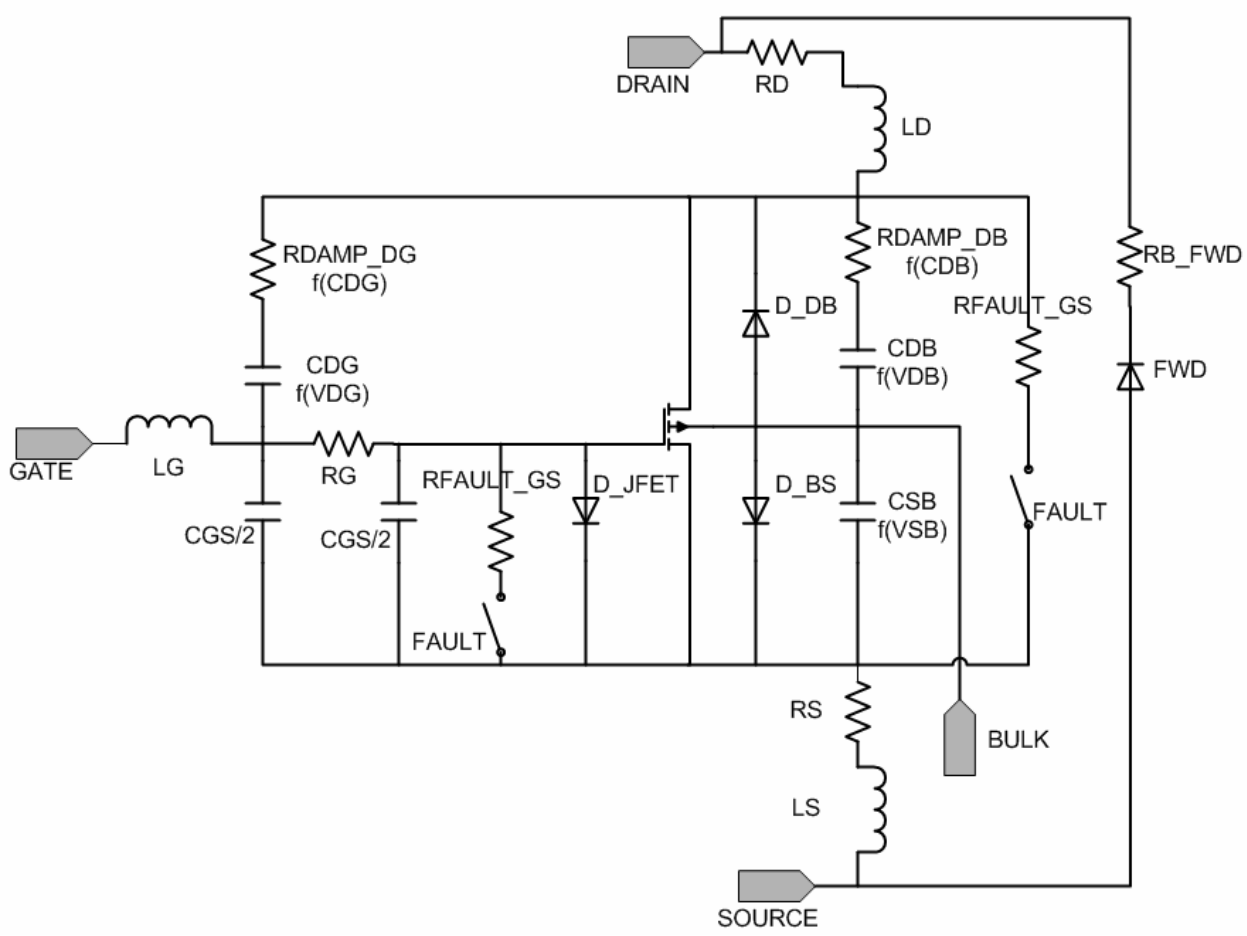


Fig. 2.23: Simplorer's system level MOSFET model.

The forward characteristics that will help define the turn-on and turn-off characteristics are not shown specifically in Fig. 2.23. The linear and saturation regions are defined by equation (2-2). V_{GS} is the gate to source voltage the model senses, all other parameters A, M, N, and K_0, are user defined, and V_{PO} is the threshold voltage for the switch. V_{sat} is the point where the switch becomes saturated and conducts a constant current of I_{sat}. Before the switch goes into saturation, the linear state will be defined by $I_{D,linear}$. A, M, N, K_0 are all user defined to best fit the switch characteristics; this was done by an iterative process in Matlab to best match the datasheets characteristics. The comparison for the output characteristics are provided in Fig. 2.24.

$$V_{sat} = A \cdot \left(V_{GS} - V_{PO}\right)^{M}$$
$$I_{sat} = \frac{K_0}{2} \cdot \left(V_{GS} - V_{PO}\right)^{N} \tag{2-2}$$
$$I_{D,linear} = I_{sat} \cdot \left(2 - \frac{V_{DS}}{V_{sat}}\right) \cdot \left(\frac{V_{DS}}{V_{sat}}\right)$$

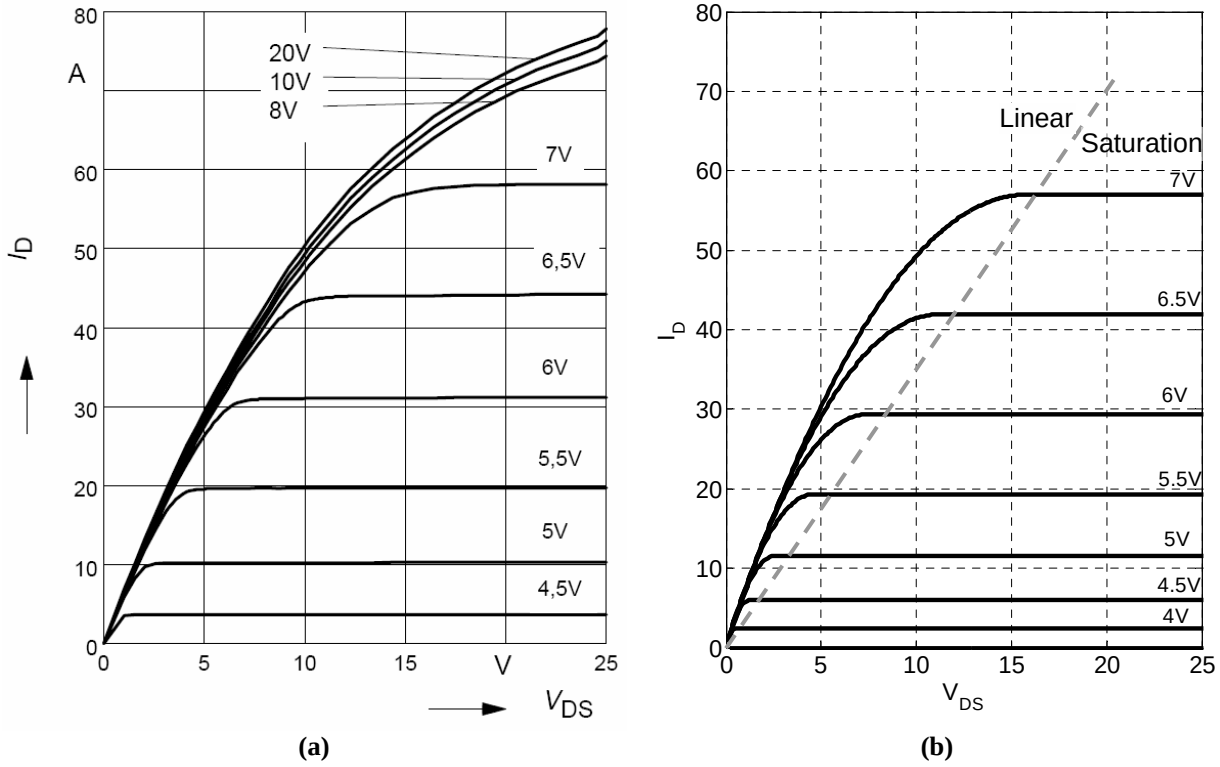


Fig. 2.24: Output characteristics of SPW20N60C3 MOSFET (a) Datasheet, (b) Simplorer's model.

Another critical factor in modeling the MOSFET's turn-on and turn-off characteristics, as well as the parasitic propagation paths, are the device impedances. The lead/terminal impedances are entered as lumped parameters of inductance and resistance (the gate resistor is embedded into this model as well). The output and input capacitors, however, are very non-linear and require a different model. The capacitances are defined by equation (2-3). These can be determined from the datasheet as well in a similar iterative manner using Matlab. The values C_0, Δ, V_{diff}, and α are user defined while V_{jnct}, is the voltage across the capacitor that the model senses. C_0 is the initial value of the capacitance with 0 V potential across it, while Δ and α define the non-linear characteristics. The capacitance comparisons are provided in Fig. 2.25.

$$C = C_0 \cdot \left(\Delta + \frac{1-\Delta}{\left(1+\frac{V_{jnct}}{V_{diff}}\right)^{\alpha}} \right) \tag{2-3}$$

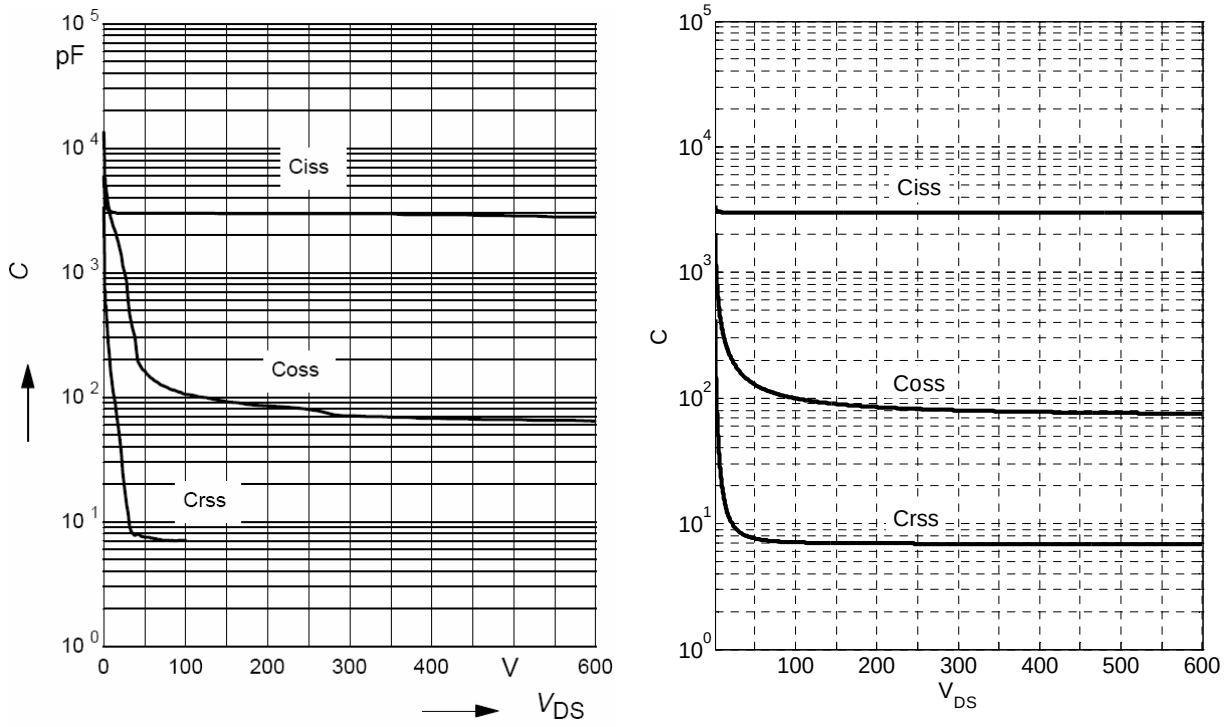


Fig. 2.25: Capacitances' of SPW20N60C3 MOSFET (a) Datasheet, (b) Simplorer's model.

The final steps for the MOSFET model are the damping resistances or ESR's of the capacitors and the breakthrough models. The damping resistors are simple calculated by a proportional damping factor that relates to the inductance and capacitance of each leg. As for the breakthrough model, the maximum limits are taken from the datasheet and inputted; although this is not critical for the EMI noise, it will provide the user with information when the simulation attempts to force the MOSFET to operate outside its nominal range. Additionally, the diode bridge model is created in a similar manner as the MOSFETs. However, the model is greatly simplified; only the forward characteristics and junction capacitances are modeled. Any of these Simplorer models can be simplified and reduced by the user to include only the components desired.

The final component in Fig. 2.16 is the gate driver. Driving the active devices is vital in determining the transient characteristics at turn-on and turn-off of the switches. Output current of the gate driver is critical in the device's rise and fall times, which will in turn affect the voltage overshoot and a high frequency noise source. The gate signal is a voltage source with a peak output current of 1 A. In order to account for this non-linearity, the schematic in Fig. 2.26 is used. The gate driver is implemented with a voltage source that will switch to a current source once the load requires more than the set current limit. When the voltage across the current source attempts to surpass a set limit (the defined gate driver limit), the circuit will switch back to a voltage source. An example of the operation is given in Fig. 2.27, where two switching periods are shown.

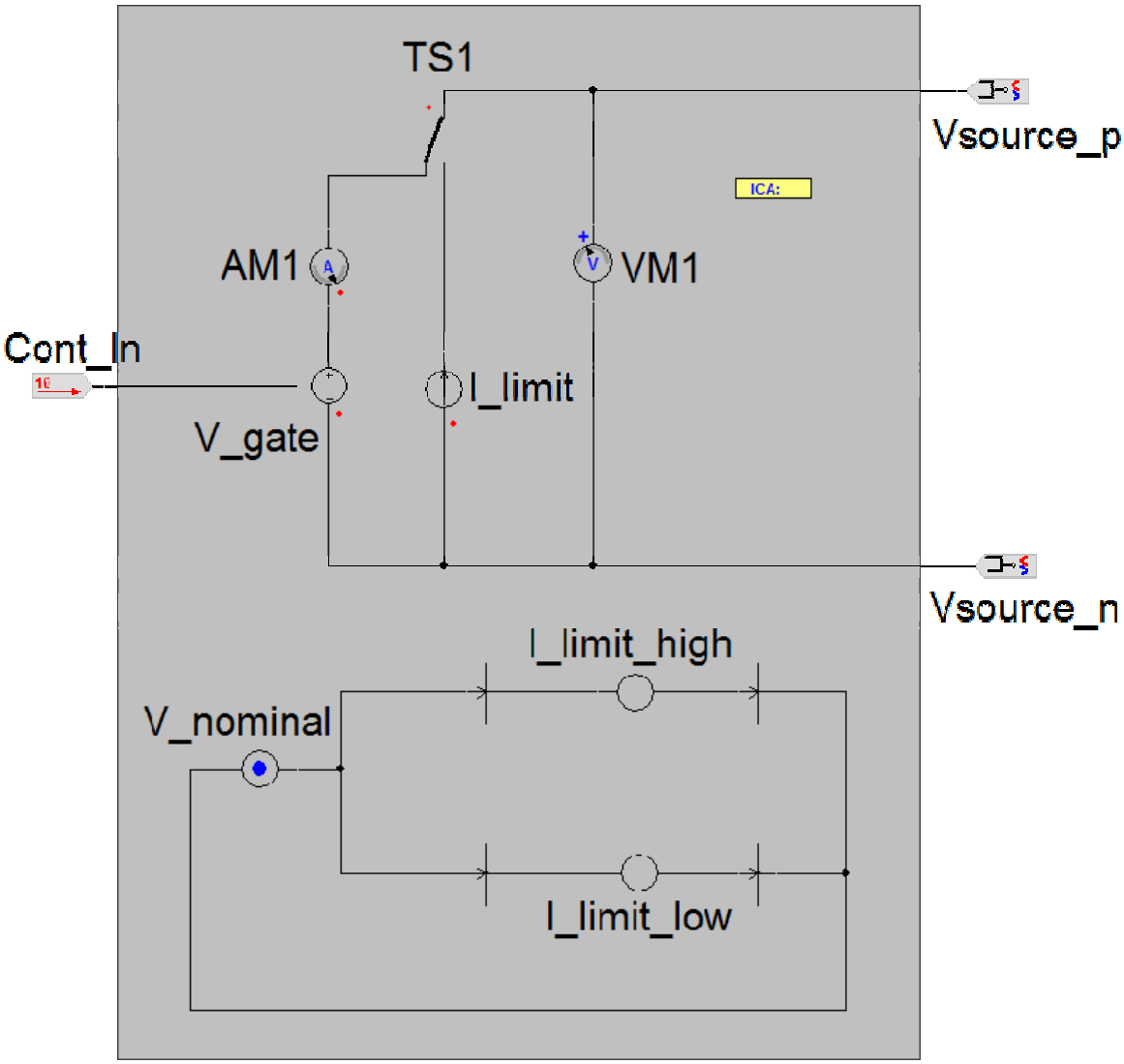


Fig. 2.26: Gate driver model.

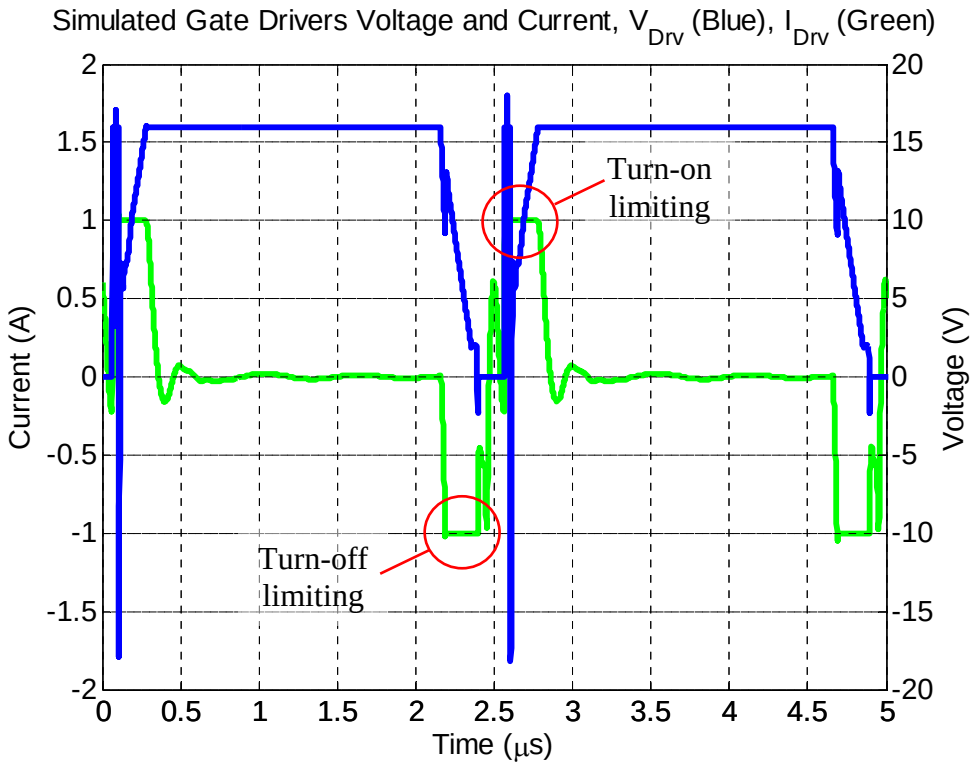


Fig. 2.27: Two switching cycles of gate driver voltage and current.

The converter is now modeled accurately from DC up to about 100 MHz, which will be determined in Chapter 3. Therefore, the converter can be simulated with and without the filter to determine the effects of the filter on the EMI noise propagating through the system. The EMI noise in simulation is computed by a fast Fourier transform (FFT) on the time-domain voltages across the LISN resistors as discussed in Chapter 1. In order to accurately perform an FFT on the transient response of the noise a constant step size is needed. A sampling rate of 500 MHz is used which easily validates the frequencies in question according to the Nyquist criterion.

Let it be noted that the equivalent circuit models do not necessarily represent a physical meaning in the hardware. For example, the inductor equivalent circuit is not intended to validate the physical existence of all passive components. Furthermore, the equivalent circuit used to model the filters performance is not a physical representation, but rather to characterize its performance.

3. EXPERIMENTAL VALIDATION

The ability to accurately predict EMI noise generation and propagation is very important in designing the power stage of the converter in addition to the EMI filter needed to meet the standards. With earlier knowledge of the EMI noise the system has the ability to be optimized according to its application. However, in order for the modeling methods to be of any use to a power electronics engineer the validity must be shown. In this chapter experimental results will be given and discussed to demonstrate the accuracy of the models.

3.1. SWITCHING OF ACTIVE DEVICES

The PFC converter used for the experimental verification is shown in Fig. 3.1. All the components shown here are the same as the modeled components in Fig. 2.16. As can be seen all the active devices are on the same heatsink which is also electrically grounded to the ground plane through a wire. The input power is on the right side of the picture with the output connection on the left. Furthermore, the transmission-line filter is shown connected to the circuit on the small board at the input. The experimental setup is such that the input can be used with or without the filter. In order to minimize the difference of various interconnect impedances of the filter, when the filter is not used in the circuit a simple copper bus bar is placed at the input. This bus bar is the same bus bar structure that the filter uses: two copper strips 10mm wide and 25 mils thick with a piece of Al_2O_3 used as isolation. With this approach the filter can easily be added or removed from the circuit by simply plugging it in to the small stage at the input. Furthermore, when the filter is removed and the simple copper bus bar structure is plugged in at the input, the bulk of the power will always be flowing through the copper bus bars. Hence the only difference between the circuit with the filter and without the filter, are the transmission line components of the integrated filter; that is, the three $BaTiO_3$ and Ni layers (2 CM and 1 DM) as seen in Fig. 2.10b. The two configurations are displayed in Fig. 3.2.

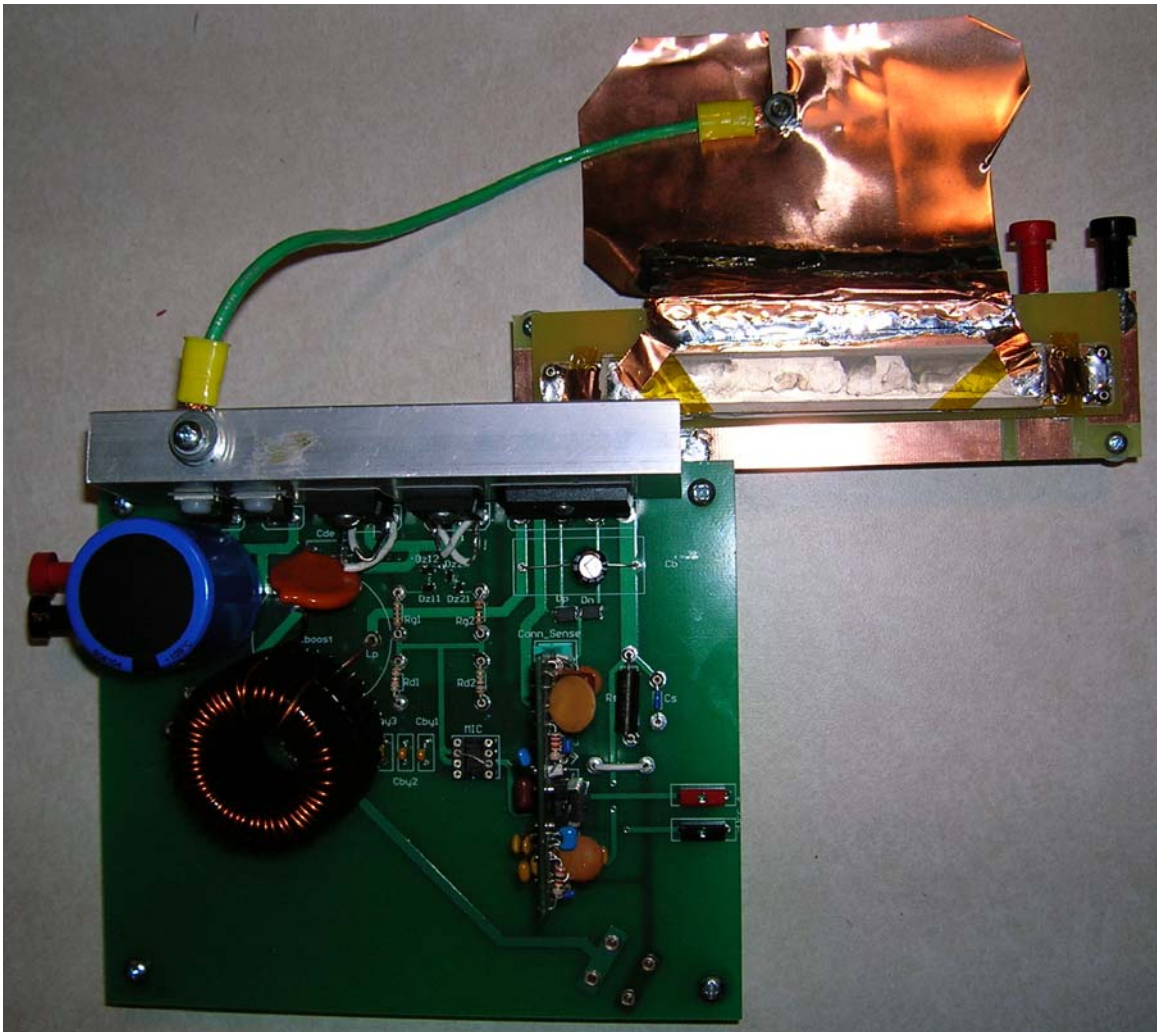
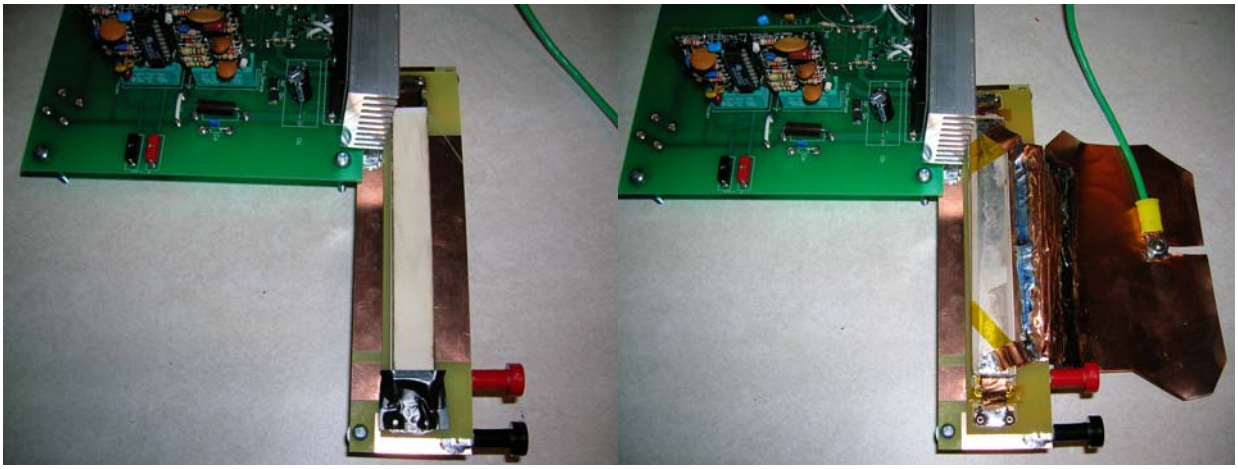


Fig. 3.1: PFC circuit with the transmission line filter at the input.



(a) Input without filter **(b) Input with filter**

Fig. 3.2: Bus bar input of PFC converter (a) with and (b) without the filter.

The operation of the PFC converter was first verified and found to perform correctly; that is it accepted a universal input with an output voltage of 390 V_{DC} and unity power factor up to 1 kW output power. Next, various voltage and current measurements were taken. Some key measurements entail rise time, fall time, overshoot, and ringing [45]. Measurements were taken at the peak of the input voltage – where the overshoot and ringing were at a maximum. Voltages for each active device were compared to the simulations and were found to have good agreement. As an example, Fig. 3.3 shows the comparison for three switching periods for one of the MOSFETs at full power of 1 kW, 120 V_{RMS} 60 Hz input voltage.

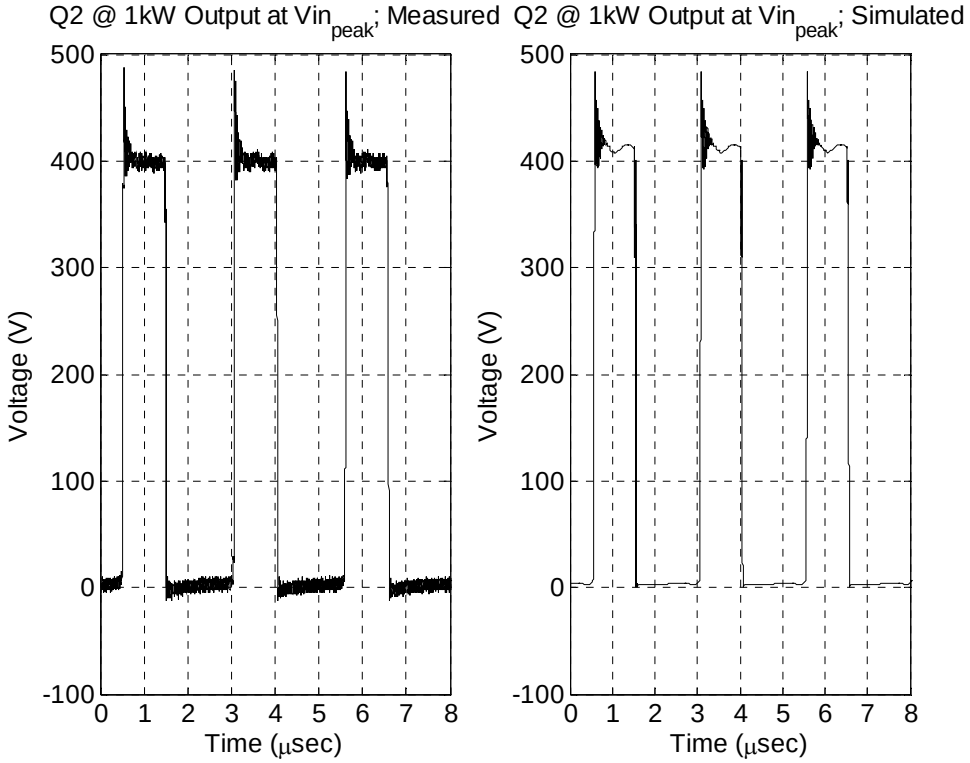


Fig. 3.3: Voltage across MOSFET, V_{DS}, for three switching periods when input voltage was at its peak.

A zoomed in view of a turn-off transition from Fig. 3.3 is shown in Fig. 3.4. It can be seen that the voltage overshoot in the measured and simulated results are in good agreement with each other. The rise time of the voltage is also very close as well. The ringing is not exactly accurate, however, up to the desired frequency range of 100 MHz the measurement is still within good comparison. A lower frequency ringing also occurs in the off state of the switch and can be seen in Fig. 3.3. Again both the measurement and simulated results compare well. A smaller difference is that the measurement results settle at a voltage slightly lower than the simulated

data. This is due to the simulated controller precisely controlling the voltage to 400V output while the actually controller has an output voltage of 390V. Finally, TABLE 3.1 summarizes three key results for the simulated and measured data.

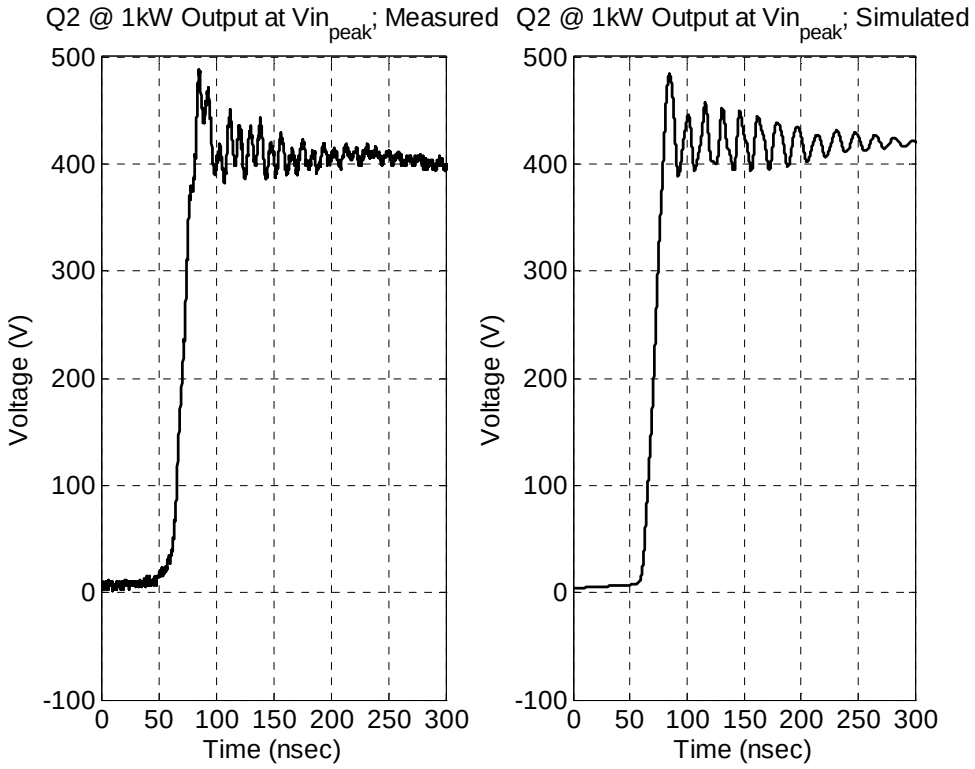


Fig. 3.4: Detailed view of measured versus simulated data at MOSFET turn-off.

TABLE 3.1: MEASURED VERSUS SIMULATED COMPARISON OF KEY NOISE SOURCE VALUES.

	Measured	Simulated
Rise Time	16 ns	17ns
Fall Time	33ns	35ns
Overshoot	83V	83V

3.2. EMI NOISE

Time domain results are necessary for nominal operation of the converter, device limits and troubleshooting. However, in addition to the time domain the frequency domain is also used for characterization of the system. One frequency domain measurement that is important to power electronic engineers is the EMI noise spectrum. In order to meet various noise standards the frequency spectrum measured across the LISN must be below a certain value depending upon the

application, see Fig. 1.2. A LISN is used in both the simulations and experiments to acquire the EMI noise. The measurement of the noise spectrum is acquired using Agilent's E7402A EMC Analyzer with a resolution bandwidth (RBW) of 9 kHz. The measured voltages from each LISN resistor is are sent through a noise separator that will either reject the DM or the CM noise. Therefore two measurements will be taken one for CM noise and again for DM noise. Time domain simulated results across the LISN resistors are used with equations 1-1 and 1-2 to determine the total noise propagating through the system for both CM and DM, respectively. These results are to perform a fast Fourier transform (FFT) to view the frequency spectrum of the noise. The simulation step time was chosen to be 2ns to provide for a good resolution of data points for the desired frequency range.

The converter was also operated at full power of 1 kW with 120 V_{RMS} 60 Hz input voltage to measure the EMI. It was found that the simulated noise in the frequency domain is also in good agreement with the experimental results; Fig. 3.5 shows the simulated (black plot) and experimental EMI spectrums within the standard's limits (150 kHz-30 MHz). There are, however, some discrepancies. First, the fundamental peak differs by 10 kHz. This is because the actual switching frequency enforced by the PFC control is 390 kHz, where the simulation used exactly 400 kHz. Another noticeable difference is the sidebands of each resonant peak and the lowest level the noise reaches, or floor. This is due to the FFT calculation versus the measured data. The FFT does not incorporate the 9 kHz RBW that the standards require, so the peaks are shown to be much narrower and more defined. Similarly, the floor of the measured results is around 40 dBμV where the simulated floor is less than 20 dBμV. Without any power, however, the EMC analyzer still produces about 40 dBμV so this is simply background noise.

Using this information a designer can acquire important aspects of the converter when designing it. Some examples are that the noise in the system is predominantly due to the CM noise; therefore attention should be focused on this aspect of the converter to produce optimal results. Furthermore, the peaks of the resonances agree quite well so an EMI filter can be devised prior to fabrication of the converter for a more optimal layout and design.

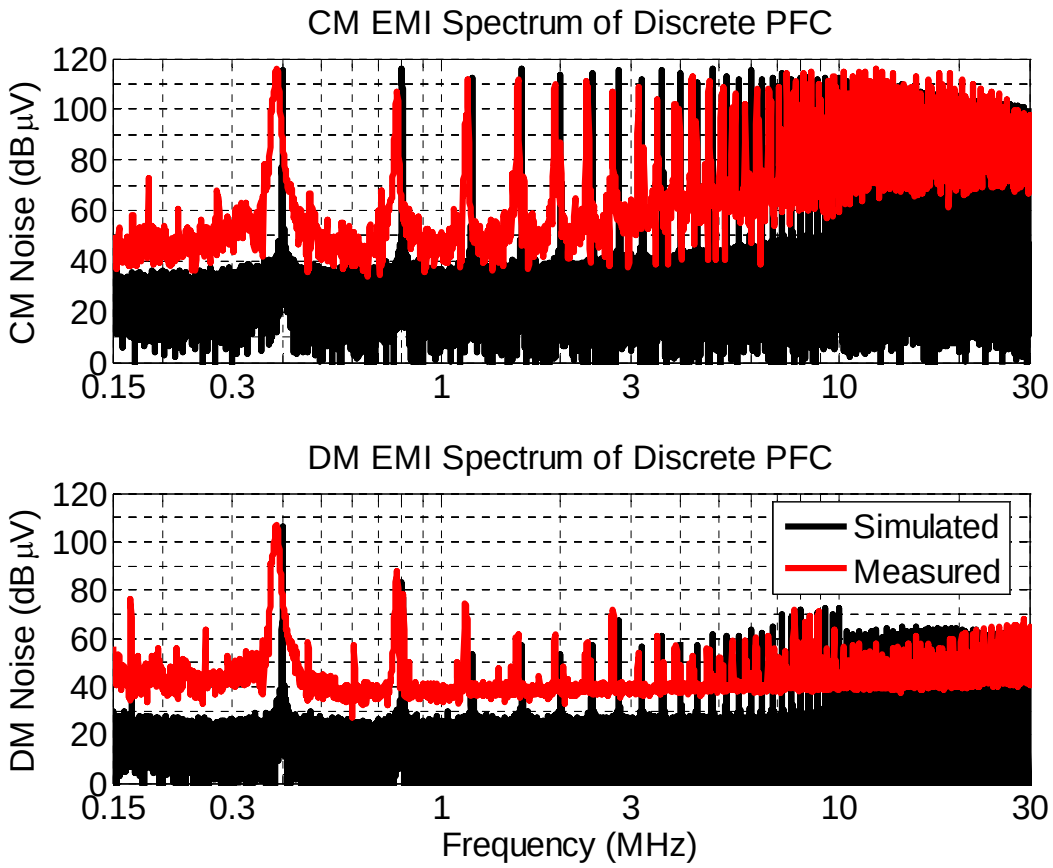


Fig. 3.5: Simulated and experimental EMI noise spectrums.

3.3. TRANSMISSION LINE FILTER

3.3.1. Small Signal

Implementation of the transmission line filter with a converter is studied to determine the effects the filter has on the performance of the converter and the resulting noise attenuation. Simply connecting the filter to the converter does not ensure proper operation, needless to say optimal operation. Various issues need to be considered when cascading filters or converters [46, 47]. One critical element is the impedance interactions between the filter and corresponding converter. The output impedance of the filter and input impedance of the converter are the system impedances in question for the interactions. Due to the uncertainties of the transmission line filter's characteristics, the nominal operating conditions will initially be 50 V_{DC} input voltage and 50 W output. Definitions for the system impedances are given in Fig. 3.6; with the

main interactions between the LISN, $Z_{O,\,LISN}$, and the filter, Z_{IF}, and between the filter, Z_{OF}, and converter, Z_{IC}.

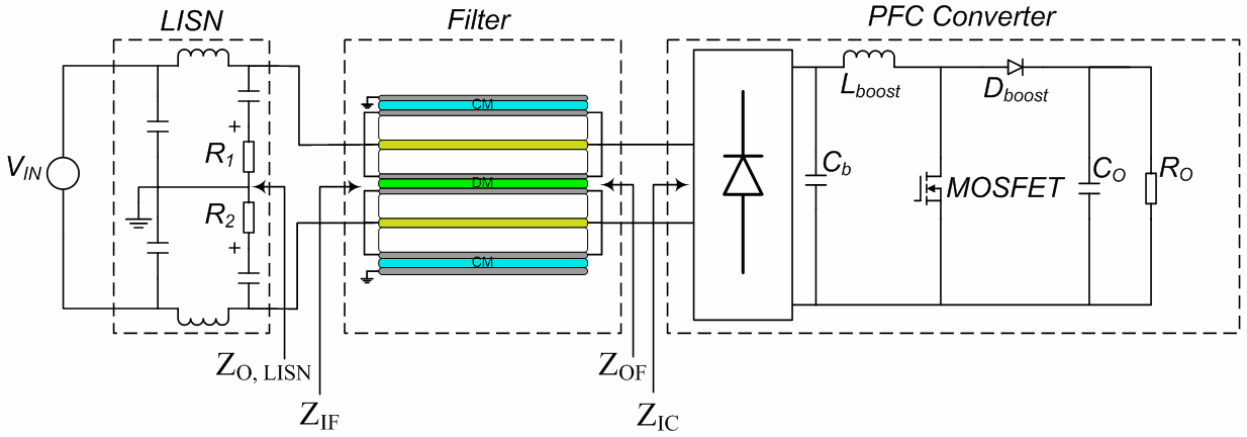


Fig. 3.6: System impedance definitions.

The interconnection impedances at this operating condition are given in Fig. 3.7. In order for there to be no interactions the input impedance of the converter is desired to be much greater than the output impedance of the filter. It is clear from Fig. 3.7 that the impedances cross at about 500 kHz. This caused a large ringing in the circuit at this frequency during operation. Since the switching frequency is 400 kHz, an additional ringing at 500 kHz will not allow the converter to operate with the designed parameters. The decrease in the converter's input impedance as frequency increases is caused by the capacitor on the DC side of the diode bridge, C_b. This problem was remedied by simply changing that capacitor with a higher capacitance model and also a higher ESR. This increase in capacitance and loss will prevent the magnitude of the input impedance from dropping as much. The system impedances after the capacitor change are shown in Fig. 3.8. There is nearly a 30 dB separation between the input and output impedances of the converter and filter, respectively, at 500 kHz now. However, this did not fully fix the problem, rather moved it. There is now a resonance interaction at 25 MHz. Although this will not affect the nominal performance of the converter it will cause noise issues at that specific frequency, which will be seen later. This does, however, show the importance of having knowledge of the impedance interactions in the design process of the converter and filter.

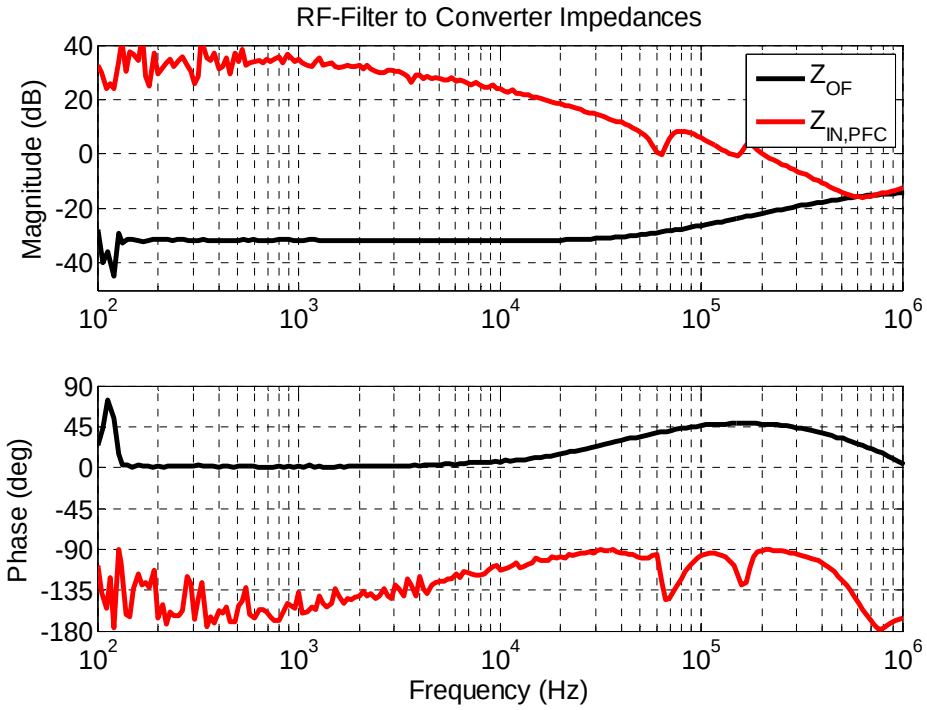


Fig. 3.7: Impedances at the input of the converter (operating at 50 V_{DC} and 50 W output); clearly an interaction at 500 kHz between the output of the filter and input of the converter.

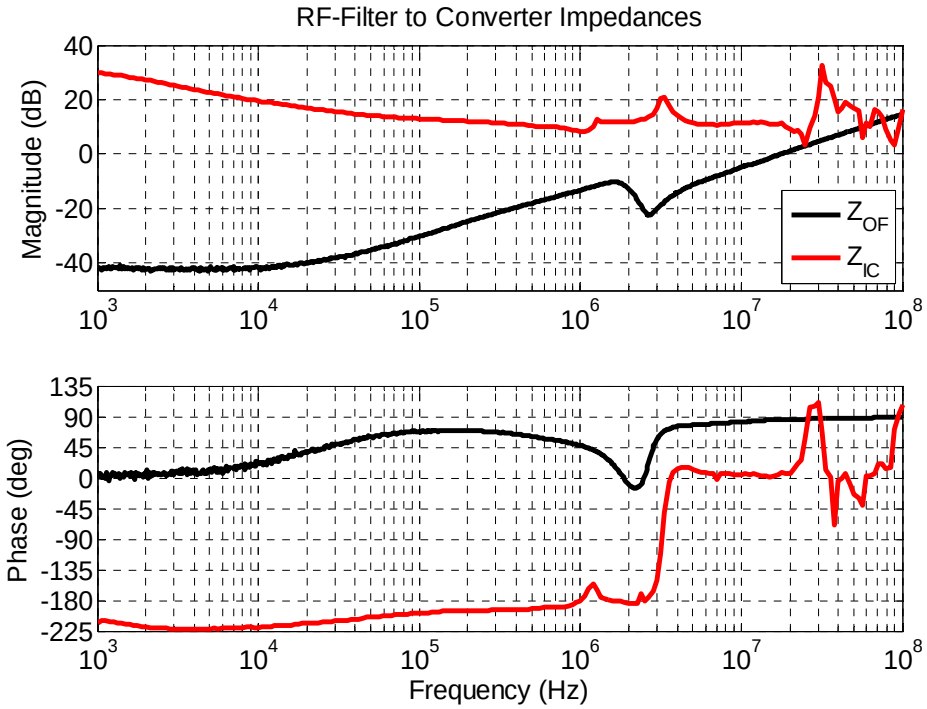


Fig. 3.8: Impedances at the input of the converter (operating at 50 V_{DC} and 50 W output) with a new capacitor, C_b, to move impedance interaction to higher frequencies (25 MHz).

In order to further predict the attenuation caused by the filter the transfer gain is often looked at to determine the corner frequency. The CM and DM transfer gain plots are given in Fig. 3.9. Referring to Fig. 2.10 the CM gain is measured and defined as having the + and – terminals shorted together and referenced to ground, likewise the DM gain is the + terminal referenced to – terminal. The measurements were taken using Agilent's 4395A Network/Spectrum/Impedance Analyzer. One drawback of this measuring technique is that the reference side for the measurements is shorted together. That is, for example, the – terminal's path is shorted when measuring DM transfer gain. This, theoretically, could show the attenuation to be half as much as it is actually attenuating. Another factor in the measurement is the connecting apparatus. For these measurements, the same fixture that was used to attach the filter to the converter was used. This will give the effective transfer gain of the filter that will be seen during the converter's operation. However, this will cause for some undesired results. As seen in Fig. 3.9, the high frequency characteristics have a nearly constant or resistive gain of about -30 dB. Previous publications [32] have shown that a similar filter is capable of having the gain decrease further at higher frequencies, the results here are directly caused from the interconnect impedances of the fixture that holds the filter. The resistance connecting the filter at its input and output are the dominant factor at these higher frequencies in this case. Similarly, the small resonance at 3 MHz in the CM mode measurement is directly related to the ground impedance from the filter to the measurement point. As seen in Fig. 3.2b, a small sheet of copper was used to make this connection. Different connection methods were used and the resonance shown in Fig. 3.9 at 3 MHz is the smallest with the declared ground connection. Although these results are not as ideal as desired, that is, a -40 dB/decade decrease at higher frequencies, it does show the importance of designing not only the filter structure but also the interconnections of the filter to the system. It is clear that the -3 dB cutoff frequency in the transfer gain plot is just above 1 MHz with a resonance at 800 kHz and 900 kHz for DM and CM, respectively. This implies that the filter will start to attenuate noise around these frequencies when implemented into the converter.

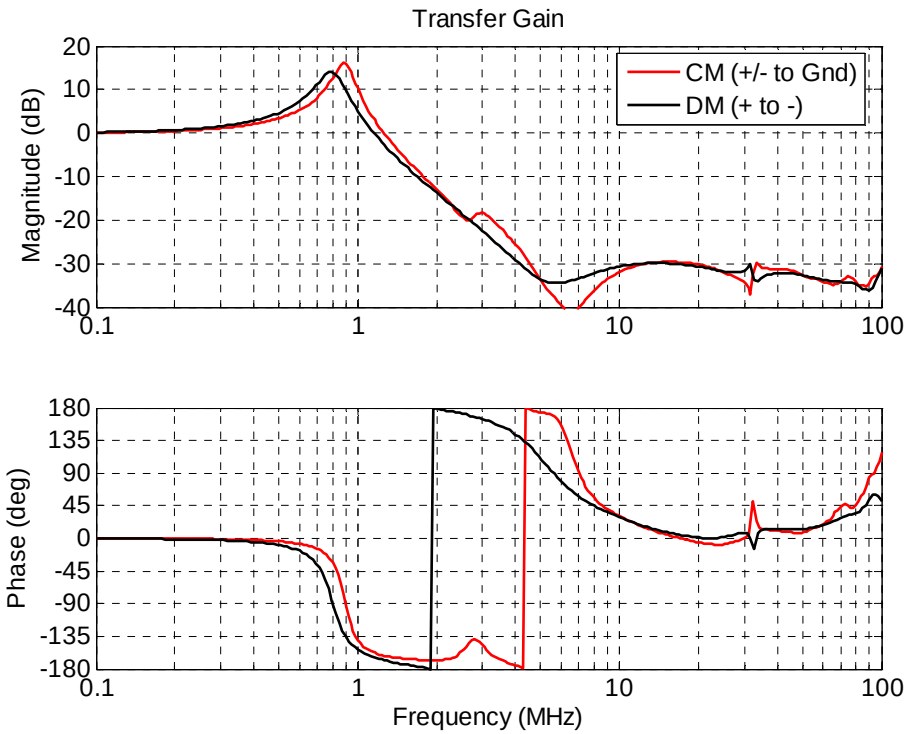


Fig. 3.9: Transfer gain of transmission line filter; CM (+ and – terminals shorted together referenced to ground) and DM (+ terminal referenced to – terminal).

Looking at the transfer function does not, however, take into account any of the characteristics of the load, converter, or source. To further investigate the attenuation of the filter, the impedance plots of the LISN and filter are evaluated. The interaction of the output impedance of the LISN and input impedance of the filter is another determination of the attenuation caused by the filter. When the input impedance of the filter is equal to the output impedance of the LISN, the filter will be consuming 50% of the power. The CM impedances are shown in Fig. 3.10; the point where they cross is approximately 30 kHz. This does not take into account how the converter interacts with the filter, however. As will be seen with the DM case, when the converter is incorporated as the load of the filter, the impedance will change and likewise the attenuation.

The DM impedances, as seen in Fig. 3.11, cross at approximately 15 kHz. At frequencies higher than this point the attenuation is characterized by the magnitude difference between the output of the LISN and input of the filter, which ranges anywhere from 20 to more than 60 dB up to 100 MHz. The filter in Fig. 3.11 has a voltage bias of 40 V_{DC} and the output is unloaded. The bias voltage is critical to the relative permittivity of the ceramic [48]. With only 40 V across the filter, the permittivity does not decrease too much, however a small resonance occurs at 200 kHz.

At 50 V bias this resonance is more pronounced. Care needs to be taken when increasing the voltage across the filter, for it will decrease the permittivity and likewise the attenuation. Although the voltage bias will give some characteristics of the nominal operation of the filter, the termination of the filter is critical. The output of the filter will affect the input impedance, which can be seen in Fig. 3.12. This is the same filter except loaded with the converter running at its nominal operation of 50 V_{DC} input and 50 W output. A few critical differences are seen in the input impedance of the filter from Fig. 3.12 compared to Fig. 3.11. The low frequency, or DC, value is capacitive without the converter, however, when the converter is loading the filter the DC value is the operation of the converter, that is $20 \cdot \log\left(\frac{50V}{1.3A}\right) = 31dB$, which will dominate the low frequency impedance. The intermediate impedances, from 10 kHz to ~100 kHz, the filter's input impedance is the dominate factor, which is what causes the attenuation at these frequencies. At higher frequencies, the converter's input impedance seen from Fig. 3.8 dominates the input impedance of the filter. Observing the distance between the LISN's output impedance and the filter's input impedance when loaded with the converter it is clear that attenuation will decrease. This again shows that it is important to know the whole system's performance when designing a converter and/or a filter.

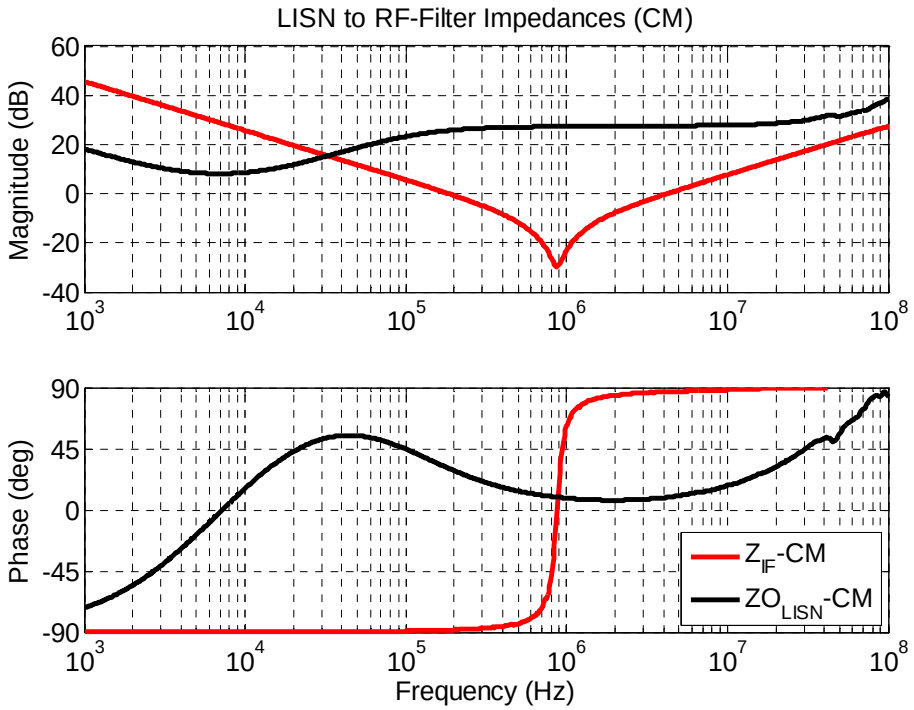


Fig. 3.10: Input CM impedance of transmission-line filter unloaded and output CM impedance of LISN.

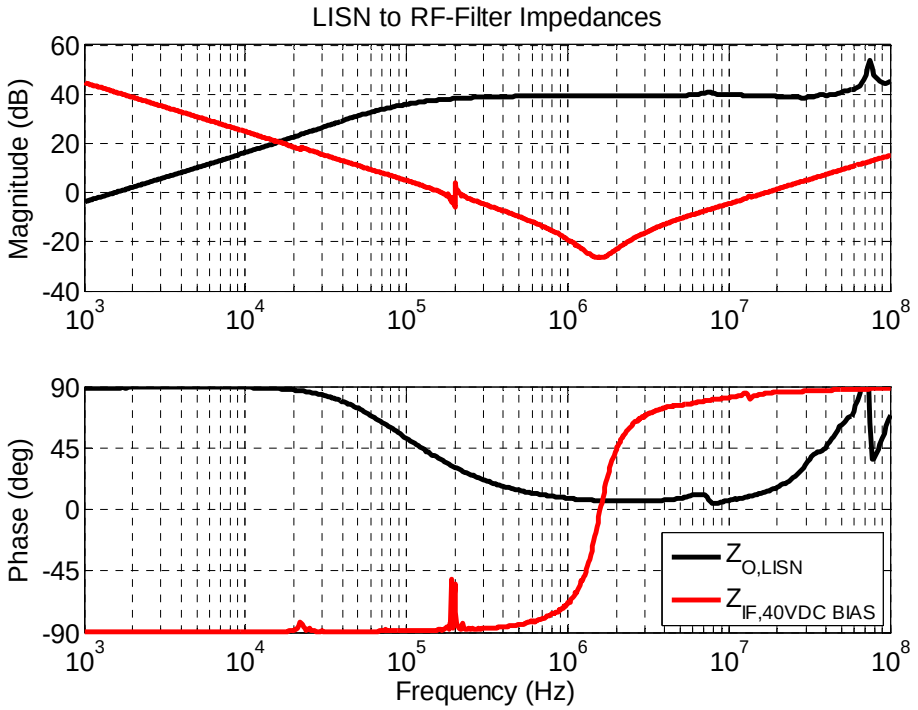


Fig. 3.11: Input DM impedance of transmission-line filter with 40 V_{DC} bias across terminals unloaded and output impedance of LISN.

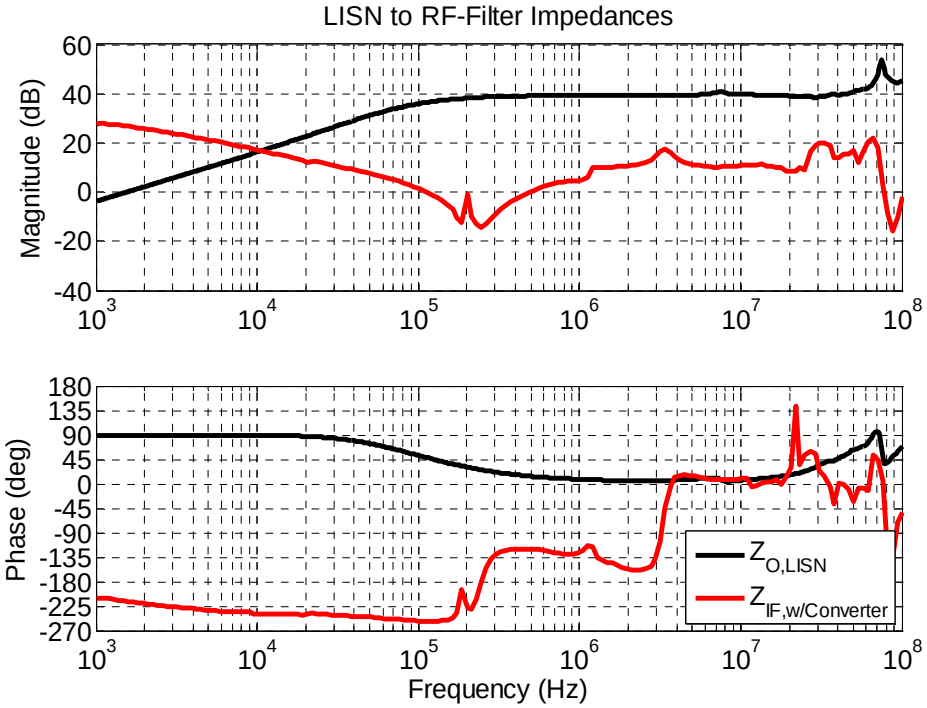
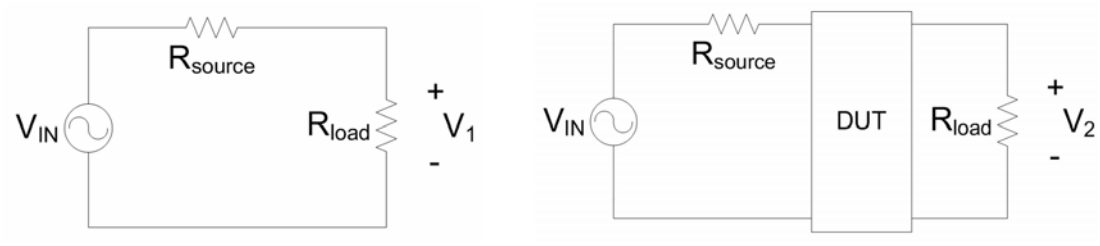


Fig. 3.12: Input DM impedance of transmission-line filter loaded with converter in nominal operation and output DM impedance of LISN.

Finally, the insertion gain (IG) is another method to determine the performance of the filter. Insertion gain measures the gain a DUT has in a circuit compared to without it there. This is also measured with a fixture that has a 50 Ω source impedance and a 50 Ω load impedance, see example in Fig. 3.13. The definition of insertion gain is $IG = \frac{V_2}{V_1}$, where V_2 is the voltage of the load with the DUT and V_1 is the voltage of the load without the DUT. Insertion gain provides a more realistic depiction of the filters attenuation in the circuit compared to the transfer gain. The transmission line filter's DM insertion gain is given in Fig. 3.14.



(a) **(b)**

Fig. 3.13: Test setup and definition for insertion gain; $IG = \frac{V_2}{V_1}$.

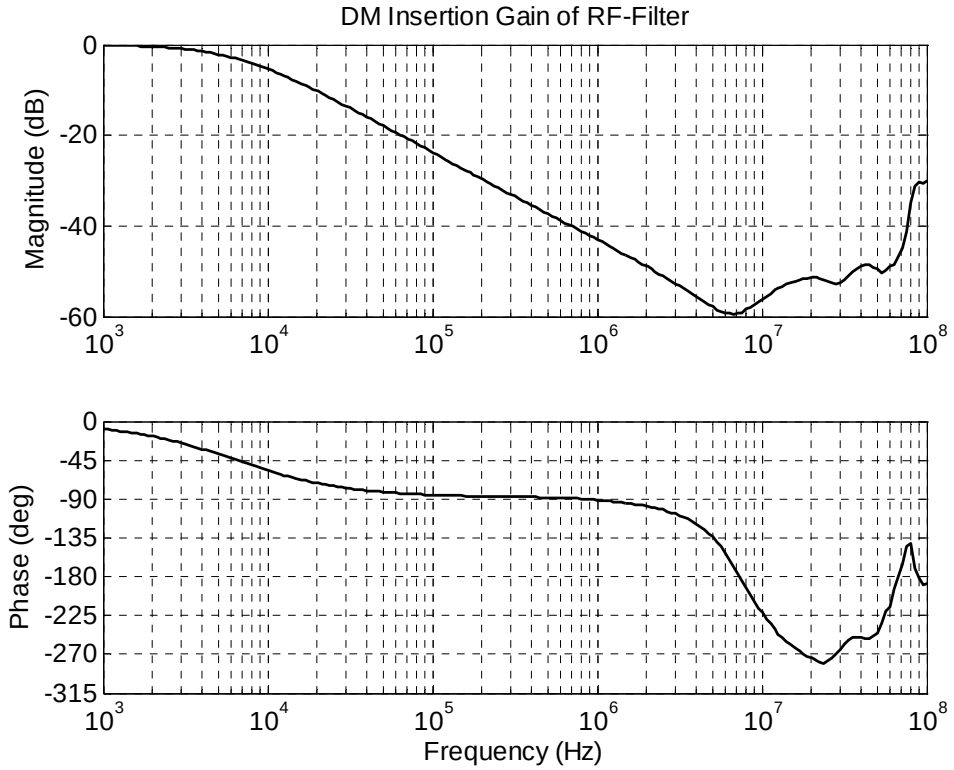


Fig. 3.14: DM insertion gain of transmission-line filter with a 50 Ω source and load impedance.

It is clearly seen that the -6 dB point is about 15 kHz which the same point that was seen in Fig. 3.11 when comparing the LISN's output impedance and the filter's input impedance. Although this method provides a better portrayal of the filter's performance, the ideal characteristics of a 50 Ω source and load impedance will not be met in the actual implementation of the filter to the LISN or the converter. Which, in turn, causes the need for the detailed impedance plots to be investigated as well.

3.3.2. Converter Operation

The methods provided in the previous section are all useful to predict the filter's noise attenuation from a converter. Through measuring transfer gain, insertion gain, or impedance interaction the filter does not need to be implemented with the converter and the test can be done as small signal test without any appreciable power. This offers a simple way to predict the filter's performance. However, the true test for the filters performance is to measure the EMI spectrum under controlled conditions with and without the filter. First, the simulated model is compared to the measured model at the decreased power level of 50 V_{DC} input and 50 W output. The results of the simulated converter (black plot) are given in Fig. 3.15 superimposed on top of the measured (red plot) EMI spectrum. The measurements are in close agreement with the simulated measurements; there are, however, some discrepancies. The main difference is at the 25 MHz resonance where the simulated is about 10 dBμV less than the measured results. The same floor and RBW conditions hold for these results as well.

The performance of the filter is shown in Fig. 3.16. It is clear that the filter already has an attenuation of 30 dBμV in the CM noise spectrum at the switching frequency of 400 kHz. This shows similar agreement to the corner frequencies seen in Fig. 3.10 and Fig. 3.12. One aspect to note is that the CM filter impedance cannot be measured during nominal system operations, since the definition of the CM impedance is defined by shorting the two power terminals together. The overall attenuation ranges from 15-55 dBμV throughout the CM EMI spectrum and up to 30 dBμV in the DM EMI spectrum. One potential reason the DM noise does not attenuate to the same degree of the CM noise could be due to the magnitude difference of the two. That is, the CM EMI spectrum reaches 115 dBμV in the frequencies of interest where the DM EMI spectrum reaches as high as 100 dBμV and nominally only about 85 dBμV. The magnitude of the filtered signal is consistently lower in the DM signal even though the

attenuation was not as great. This is caused because the CM EMI noise dominates in this system.

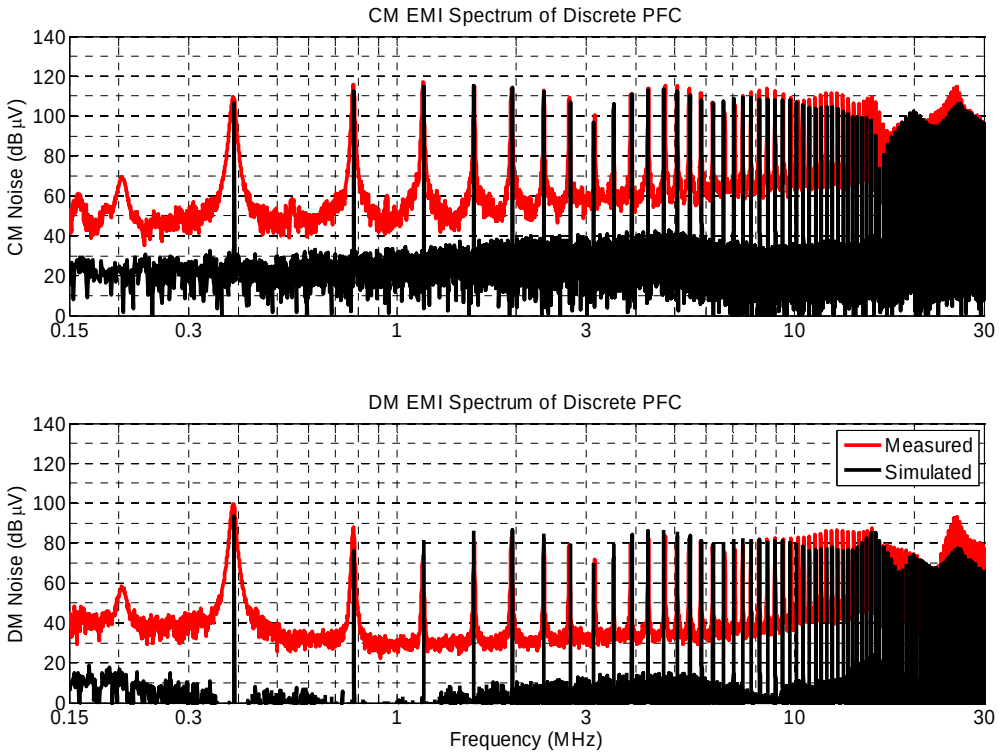


Fig. 3.15: Simulated versus measured EMI spectrum with 50 V_{DC} input operating at 50 W output.

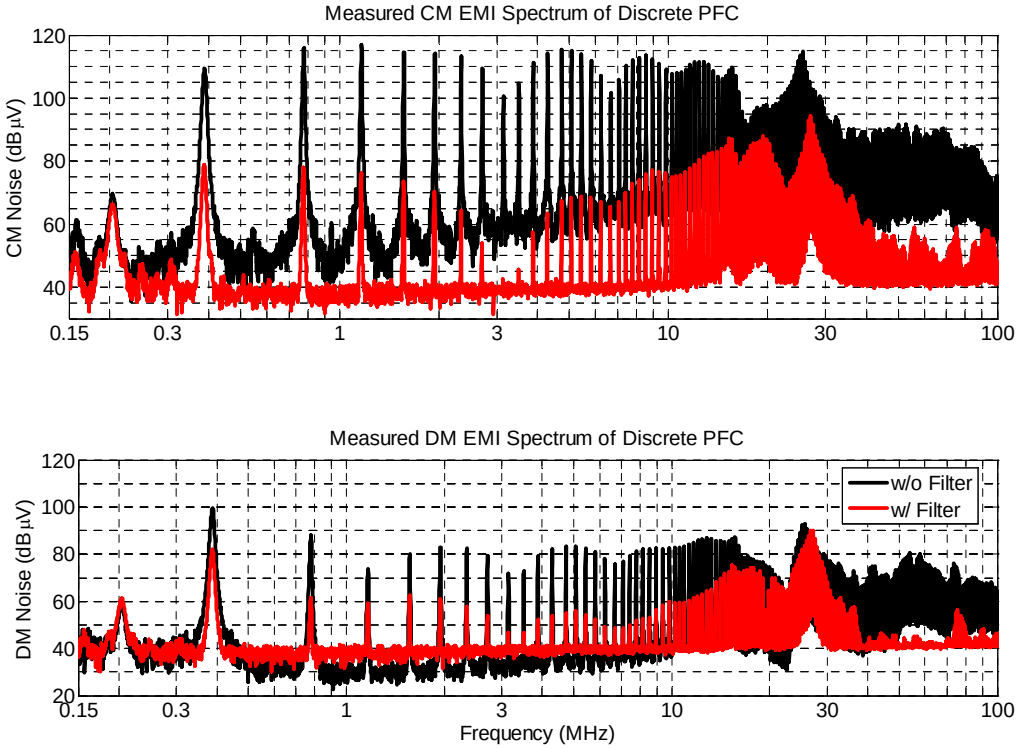


Fig. 3.16: Measured EMI spectrum; filtered versus unfiltered operating with 50 V_{DC} input and 50 W output.

Another way to view the attenuation of the filter is to look at the total noise produced by the converter with and without the filter. An example of this can be seen in Fig. 3.17. The total EMI attenuation ranges from 20-50 dBμV throughout the frequencies of interest. These results agree with the impedance measurements in the previous section, showing that the corner frequency for the attenuation is much lower than the original thought with this style of transmission-line filter. The attenuation begins well below the 1 MHz cutoff frequency the transfer gain alluded to. This shows that the filter, originally thought to be used as a high frequency second stage filter, could be optimized further to drastically decreasing the size of the primary EMI filter. In extreme cases, the transmission line filter could even serve as the sole filtering method for EMI.

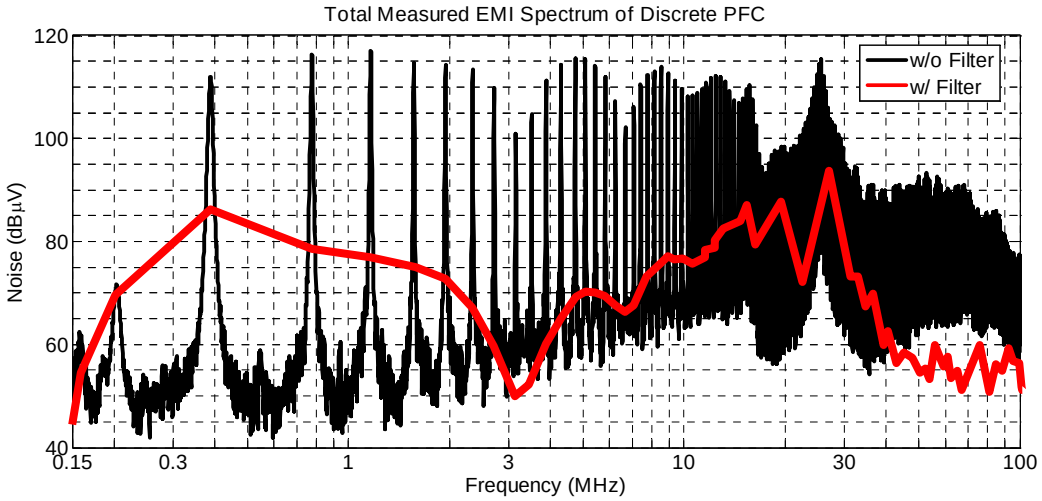


Fig. 3.17: Total EMI noise with filter versus without filter operating at 50 V_{DC} input and 50 W output.

As can be seen in the EMI noise spectrums of Fig. 3.16 and Fig. 3.17, the noise after 30-40 MHz is nearly zero. It appears that the noise drops off drastically and is only limited by the floor of the measurement. This could be important in the design process for it would give great benefit to decrease the corner frequency even a little to further improve the attenuation in the EMI frequency range.

Finally, the validity of the filter model should be shown through EMI measurement results. The converter with the filter model was simulated under the test conditions to compare to the experimental data; the spectrums are shown in Fig. 3.18. There is more discrepancy in this EMI spectrum than any other one. Below 10 MHz the filter model is very accurate; however, between 10 and 30 MHz the model is missing some of the resonating phenomenon. After 30 MHz the model shows a large attenuation. This cannot accurately be compared to the measured results.

The measurement shows the EMI is below 40 dBμV, which is floor of the EMI measurement equipment. How far below the floor the filter is actually capable of attenuating, is not clear, but the model does show a continual attenuation up to 100 MHz.

The lack of accuracy between 10-30 MHz is that the simulation was not able to account for the impedance interaction between the converter and filter at these frequencies. This could be for a few reasons: one main reason is that the resonance between the filter and converter was caused by a measurement technique that was not accounted for. At frequencies of this magnitude a very little difference in the model and measurement could cause for the slightest difference in impedances and therefore cause, or not cause, a critical resonance, such as the one between the filter and the converter at 25 MHz. Another factor is that when the operating condition of 50 V_{DC} input and 50 W output was used the EMI spectrum without the filter, as seen in Fig. 3.15 was not as accurate as the model using 120 V_{AC} 60 Hz input and 1 kW output as seen in Fig. 3.5. When the filter was added, these differences could have been magnified and easier to depict.

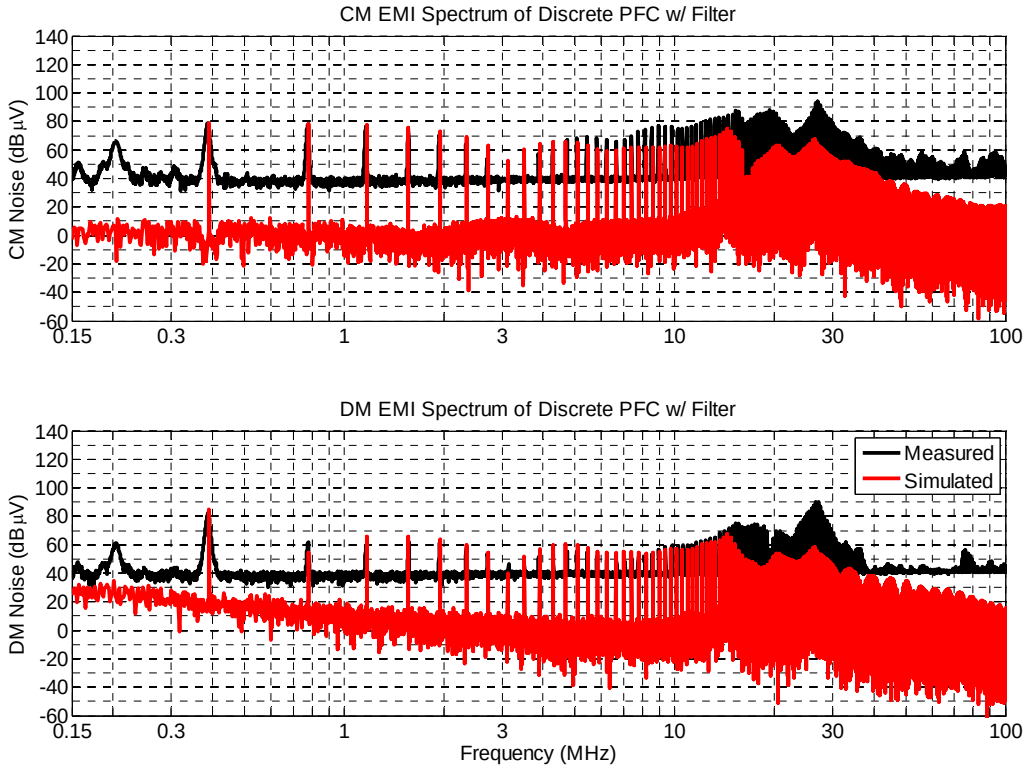


Fig. 3.18: Simulated versus measured CM and DM EMI spectrum with filter operating at 50 V_{DC} input and 50 W output.

A final view of the simulated model is shown in Fig. 3.19. This plot shows the simulated model at 50 V_{DC} input and 50 W output with and without the filter. Again it is clear that the filter is attenuating 30 and 20 dB at the fundamental switching frequency for CM and DM, respectively.

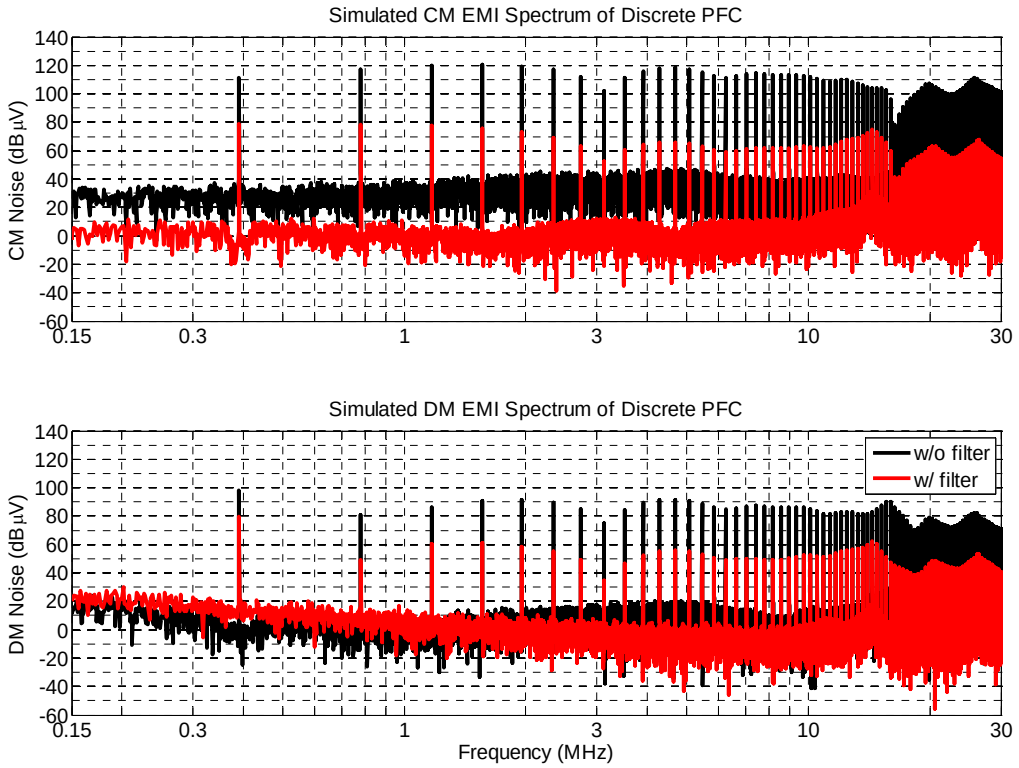


Fig. 3.19: Simulated CM and DM EMI spectrum with filter operating at 50 V_{DC} input and 50 W output.

4. CONCLUSION

4.1. SUMMARY

The growing number of electronic loads and devices require the use of power electronics to match the load power characteristics to that of the source. This demand has brought upon the need to strictly regulate the EMI emissions from power electronic equipment. It is strongly desired to contain the emissions early in the design stage to increase the available techniques while decreasing the cost and potentially the power density of the equipment. Proper modeling of the system's EMI and filter's attenuation is required to optimize the design.

In order to characterize the system's EMI accurately the noise source and noise propagation path need to be modeled. The noise source was modeled using device based behavioral models either provided by the manufacturer or through characterization from datasheet values. Additionally, the gate driving circuit was also expressed to depict the non-linear current limiting effects that are critical for switching transients. These two features – switching device and gate drive model – provide for an accurate noise source model. The propagation path was modeled using Maxwell Q3D and impedance measurements. The power interconnections can be modeled using Maxwell Q3D to determine critical impedances; likewise, the passive components are measured with an impedance analyzer and modeled with the appropriate parasitics. Using these two approaches for the generation and propagation of the noise, the frequency spectrum of the EMI as well as the time domain transients are in good agreement with each other.

Given a proper model of the EMI in a system, a filtering model is needed to characterize the overall attenuation. Classical filters can be modeled with similar approaches to the power stage; however, advanced filtering techniques such as the transmission-line filter require a unique model due to its inherent functionality. The transmission-line filter's parameters change drastically as frequency varies and, therefore, require an extra step to model. Using Maxwell Extractor in conjunction with Simplorer and Matlab a simplified model was created that depicts the input and output impedances as well as the transfer characteristics. This provides the means to use the models to predict the EMI and its associated attenuation due to the filtering. Other complications are also involved with the implementation of the filter that further shows the need

for accurate modeling techniques to solve problems earlier in the converter's design. Overall, the modeling approaches agreed very well with the experimental validation.

4.2. FUTURE RESEARCH

4.2.1. Improving Attenuation

Given that an accurate attenuation characterization is obtained, an optimization can be done to the system. The attenuation seen with the transmission-line filter was not optimized but rather used as an example in the modeling approach. The models allow the possibilities to perform parametric studies without the cumbersome tasks of fabricating many filters and using a trial and error approach. However, the stated method can be time consuming due to the long system time constants and high frequency modeling. It was also shown that the impedance interactions of the filter in the system are critical to the performance of the filter. Additional modeling and studies could be done to match (or mismatch) the impedances of the filter and system to maximize the attenuation. Similarly, it is clear that the attenuation after 30 MHz is superior and is only limited by the noise floor. Further optimization can be carried out to shift the high attenuation region to a lower frequency range, as well as, shift major resonances beyond the upper limit of 30 MHz.

4.2.2. System Integration of Filter

The bus bar structure of the filter may be cumbersome in some system designs. An eventual goal could be to integrate the filter with other power electronics, specifically with an IPEM. This brings up questions of different geometries for the filter. One option to reduce the size is to eliminate the Al_2O_3. It has previously been shown that the Al_2O_3 does not have a significant effect on the attenuation. Another possibility, that has been previously discussed, is to fabricate the filter around an IPEM or even as a layer within the IPEM. This has the advantage to contain the noise at the source and add only a couple extra fabrication processes without drastically affecting the volume of the IPEM. This could cause for a smaller filter at the front end and drastically increase the overall power density. In order to make this a reality the performance of the filter will need to be characterized in different locations of the converter or system, and to optimize the location to maximize the functionality of the filter. However, this causes the need for a 3D filter structure. The modeling used for the filter in this work was done using a 2D field solver. This limits the geometry to be studied. In reality, a filter with 3D geometries that can

potentially enhance the attenuation cannot be modeled with this approach. At the higher frequencies coupling between the filter can occur with 3D structures. This requires the need for a 3D field solver, which increases the solving complexity and computation time. Accurate approximations are necessary in order to model a 3D structure in a timely, accurate manner.

APPENDIX A – FILTER FABRICATION

TRANSMISSION-LINE FILTER SECTION

A 120x60 mm high permittivity ceramic substrate is used, in this case Y5V $BaTiO_3$. The first step in the fabrication process is a physical vapor deposition, or physical sputtering, of the metal onto the substrate. The sputtering process will deposit a thin (on the order of nanometers) layer of a metal onto a substrate. Since Cu or Ni will not adhere to the ceramic well, a titanium (Ti) buffer layer is used between the ceramic material and the Ni. Before the sputtering is begun the substrate must be cleaned for best adhesion of the Ti. The substrate is rinsed with acetone followed by isopropyl alcohol in turn followed by de-ionized (DI) water rinse. Acetone is used to remove any organics on the substrate; the alcohol is then applied immediately after the acetone, before the acetone evaporates to prevent any organics drying to the substrate. Likewise the DI water rinses off the substrate of all solutions. The ceramic is then dried with nitrogen gas before inserting the substrate into the sputtering chamber.

A vacuum is pulled in the chamber with the substrate in there to a pressure less than 2 μTorr. This is done to remove impurities from the chamber. The sputtering process works at about 5 mTorr in an argon gas plasma. First, before the sputtering is begun but after the chamber is under an adequate vacuum, a purge of the argon gas line and chamber is done for 30 minutes. This will help remove any further impurities or pockets of air in the line. Next, with a vacuum pulled, the sputtering of Ti is done for 2 - 15 minute periods, followed by 2 - 15 minute periods of Ni deposition. The sample is cooled down for an hour after the sputtering is completed while the chamber remains under a vacuum. The substrate is then flipped over and the same sputtering process is repeated on the second side of the substrate [49].

Normally, that is, when etching Cu, the etching step is done after a thicker electroplated layer is added. However, due to the difficulty of etching Ni, a mask is first placed on the sputter Ni layer and the electroplated Ni will only plate on the desired areas. The first step in preparing the sample to be etched, is to mask off all the area that Ni is desired to remain. A photoresist mask is carefully applied to a whole side of the substrate with a spatula. Then by using the spin coater a thin uniform layer across the whole surface is achieved. The spin coater settings were roughly 600-700 RPM for 15 seconds followed by 1600-1700 RPM for 60 seconds. Now, the uniform

photoresist needs to be baked on the hot plate for 35 min. In order to keep the hotplate clean a layer of kapton tape is placed and the substrate is elevated off the kapton by 4 thin pieces of scrap ceramic at each corner. This is important to prevent the ceramic from sticking to the kapton tape on the hotplate. After baking the photoresist and letting it completely cool, the second side is repeated in the same manner. It is especially important to elevate the ceramic from the hotplate (by less than a mm) to prevent the first side's photoresist from sticking. Both sides of the ceramic are now completely coated with a thin uniform layer of photoresist.

A mask is created using AutoCAD and is used when exposing the photoresist. The mask is printed on a clear transparency, when the sample is in-between the mask for both sides it will block UV light were desired. The mask allowed three strips of Ni to remain with a few mm in-between each 10 mm wide trace to cut with the laser. The mask is given in Fig. A.1.

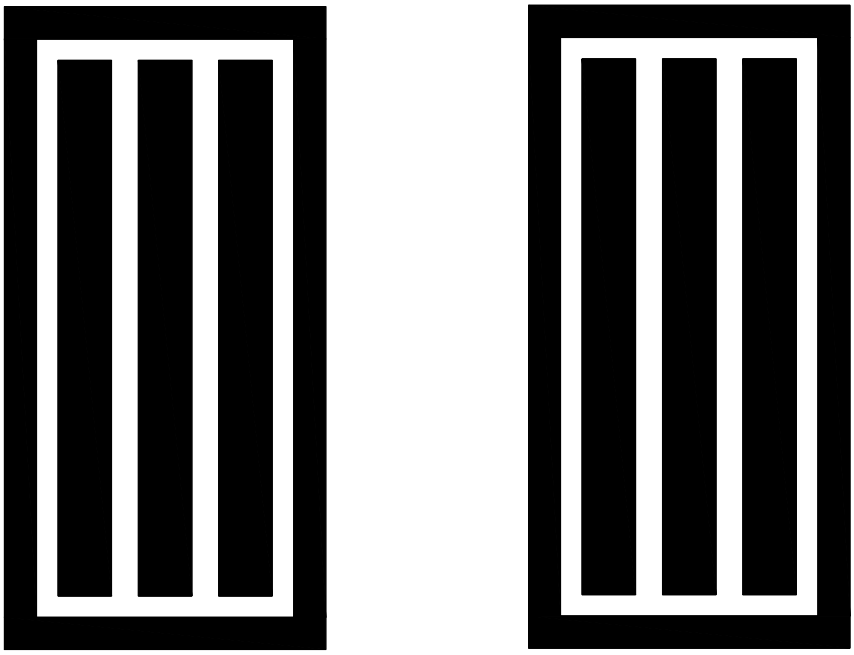


Fig. A.1: Mask to provide three 10 mm wide strips of Ni on each side of the $BaTiO_3$.

When the photoresist layer is exposed to UV light it will not respond to the photoresist developer. The developer removes any un-exposed photoresist material; therefore, the photoresist mask will remain where the Ni traces are desired.

The next step is to electroplate Ni onto the sputtered substrate. Electroplating will plate the metal from an anode to cathode through an ionic solution when excited by an external current. This is needed to provide a thicker metallization layer than the thin sputtered layer. The anode in this case will be a piece of solid nickel and will plate to the sputtered layer, the cathode. With

the nickel solution and the anodes ready for sputtering, a frame is used to hold the anode and provide a conducting path for current to flow. The frame is a piece of FR4 board with Cu on one side. The board's total size is about 10 mm larger than the substrate on each side; a section is cut out in the middle of the board to provide an opening about 2 mm smaller than the substrate size. This allows the substrate edges to be in contact to the copper on the FR4 board while keeping most of the sample exposed to the solution. The FR4 board is then connected to the cathode terminal and will allow current to pass from the nickel anode through the solution to the substrate's side connected to the FR4 copper. In order to plate both sides of the substrate a frame was made to contact both sides of the sputtered ceramic and two nickel anodes were used on each side of the substrate. A picture of the frame used is shown in Fig. A.2.

(a) **(b)**

Fig. A.2: FR4 Frame to hold cathode (sputtered ceramic) in the electroplating process; (a) inside of frame with Cu contact, (b) closed frame.

Now that the electroplating apparatus is set up the values for the process need to be determined. A plating current density is determined from Fig. A.3; a tradeoff of the metallization stresses, hardness, and speed are related to the deposition rate. In general, the higher the deposition rate the greater the stress and the lower the rate the harder the deposit. A

rate of 20 A/ft^2 has been found to be a good compromise between the tradeoffs. The actual current to be applied is found by the set of equations below:

$$A_{Total} = 40mm \cdot 100mm \cdot 2$$
$$= 8000mm^2$$
$$= 0.086\,ft^2$$

$$I = 20\,A/ft^2 \cdot 0.155\,ft^2$$
$$= 1.72A$$

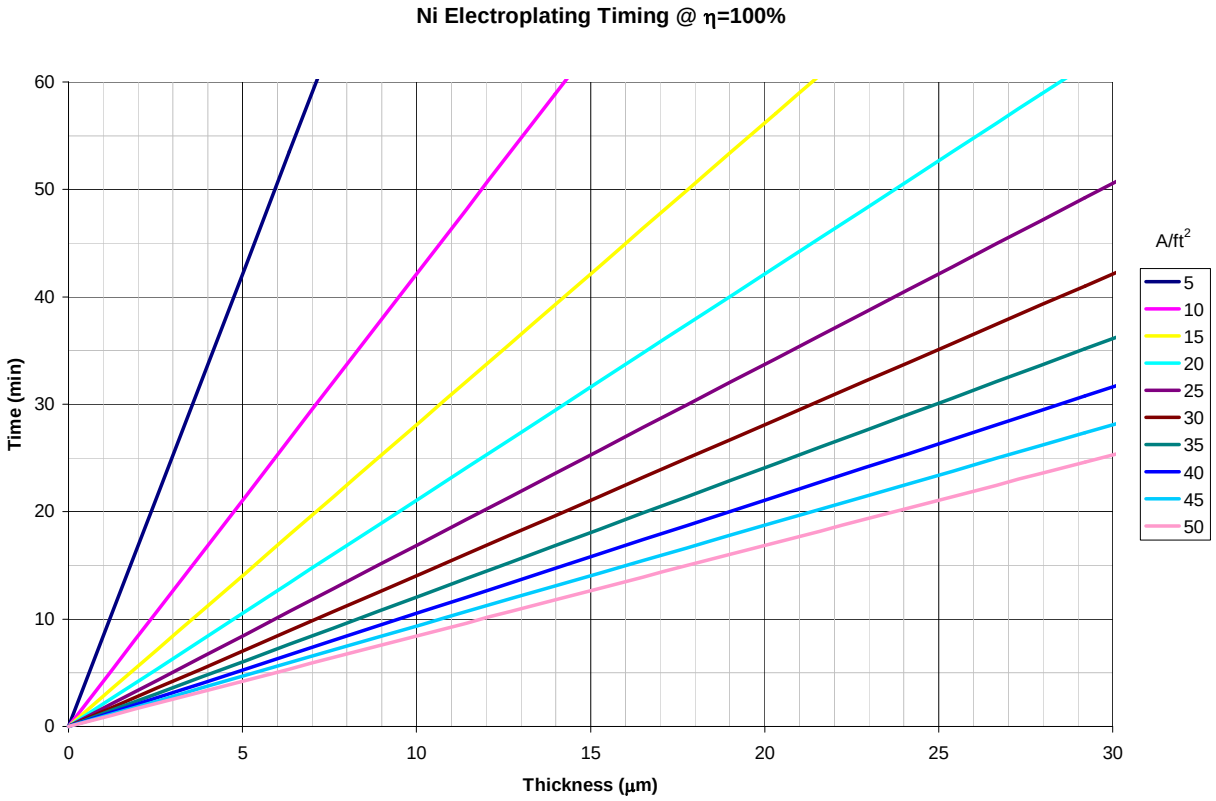


Fig. A.3: Nickel Electroplating times for various thickness and current densities.

At the chosen plating rate, the time to plate 15-20 μm is about 35 min at 1.72A. When plating nickel, the solution – that is purchases as a 'ready to use' solution – should be heated up to 120 ºF (usually takes about 4 hours with Technic baths). As a general rule, a more uniform plating occurs when the anodes smaller than the cathode by 1.5-2x in a similar shape to the cathode. After plating for the desired time etch the sputtered Ni away with a diluted solution of HNO_3, (about 5:1 H_20:HNO_3) at 50 ºC. This solution will slowly dissolve the photoresist too, which is another reason to perform the Ni mask early.

The remaining metal on the substrate is the thin Ti layer that was initially sputtered. To remove the Ti a micro-etch solution that should be diluted to 20 parts H_20 to 1 part Ti etchant is used at room temperature. Use care when using the Ti etchant due to its toxic nature. Removing

a sputtered layer will take between 15-20 minutes. Follow the etching process with a DI water rinse again.

This completes the process for making the metallization (Ni) traces. Finally, the strips that were produced from the etching are cut apart using a laser cutter. The laser will cut the ceramic material in-between the metallizations and each strip is one filter. Additional steps can be taken for aesthetics and protection from environmental elements. These include, but are not limited to, solder masking the substrate and electroless Ni plating. These steps are unnecessary for the functionality of the transmission line structure; however the electroless Ni plating process is outlined below for completeness.

BUS BAR SECTION

The Cu bus bar was simply produced from DBC substrates. The same size substrate was used, 60 mm x 120 mm. The same process for applying the photoresist mask was done to produce strips 10 mm wide and 100 mm long on one side and remove all the Cu on the other side. The Cu etching process is now ready to be completed. The Cu etching solution is ferric chloride and first needs to be heated for effective etching. To etch the Cu, place the substrate into the etching machine with the heated solution. Then close the top and start the timer. Etching in 10 minute increments was done to monitor the process and not expose the substrate to the solution any longer than needed; this avoids any undesired etching or undercutting of the traces. Finally, rinse the sample to remove any excess ferric chloride. Then the laser cutter is used to cut the strips into multiple pieces, where each strip served as a bus bar and the Al_2O_3 spacing layer.

FILTER ASSEMBLY

The filter assembly is simply done by stacking the transmission-line filter sections together with the Al_2O_3 and Cu bus bar in between each. Small Cu straps were used to electrically connect the appropriate terminations and the soldered down to the stage.

NICKEL ELECTROLESS PLATING

CHEMICAL COMPOSITION INSTRUCTIONS FOR ELECTROLESS PLATING

ACID CLEAN (700mL)

1) 500mL DI H_2O
2) 20-30% (140-210mL) PC-455 *(180mL)*
3) Top off to 700mL if under

MICROETCH (700mL)

1) 500mL DI H_2O
2) 1-2% (7-14mL) Sulfuric Acid, H_2SO_4 *(10mL)*
3) Cool to 21-30°C *(25℃)*
4) Stir slowly and carefully while adding 42-84g of AD-485 *(65g)*
5) Top off to 700mL if under

INITIATOR (700mL)

1) 400mL DI H_2O
2) Stir slowly and carefully while adding 3% (21mL) Hydrochloric Acid HCl
3) Stir slowly and carefully while adding 2% (14mL) Initiator 852
4) Top off to 700mL if under

NICKEL PLATING (750mL)

1) 500mL DI H_2O
2) 6% (45mL) Ni-8600A
3) 20% (150mL) Ni-8600B
4) Top off to 750mL if under
5) Pre-heat solution to 85°C
6) PH should be 4.7-4.9, adjust as needed (see below)

PH ADJUSTMENT

1) Mix 1:3 ratio of Ammonium Hydroxide, NH_4OH, with DI H_2O in order to increase the PH
2) Mix 1:4 ration of Sulfuric Acid, H_2SO_4, with DI H_2O in order to decrease the PH
3) Add either 1) or 2) in small amounts checking PH frequently until 4.7-4.9

NOTES:

Clean all beakers thoroughly before all usage

Italic characters are median values

Percentages are for total batch size

ELECTROLESS PLATING PROCESS

1) Beaker 1, Acid Clean

    5 minutes @ 45°C

    DI H_2O wash for 2-5 min

2) Beaker 2, Microetch (Skip this step for sputtered substrates)

    No more than 2 minutes *(1 min 45 sec)* @ 21-27°C *(25℃)*

    DI H_2O wash for 2-5 min

3) Beaker 3, Initiator

    2 minutes @ Room Temp

    DI H_2O wash for 2 min

4) Beaker 4, Nickel Plating

    15 minutes @ 85°C for 0.12-0.2 mils (plating longer than 30-45 min caused “bubbles” to form in the plated metal)

    DI H_2O wash for 1-3 min

REFERENCES

[1] F. C. Lee, J. D. v. Wyk, D. Boroyevich, G.-Q. Lu, Z. Liang, and P. Barbosa, "Technology trends towards a system-in-a-module in power electronics," in *IEEE Circuits and Systems Magazine*, vol. 2, 2002, pp. 4-22.

[2] H. W. Ott, *Noise Reduction Techniques In Electronic Systems*, 2 ed. New York, NY: John Wiley & Sons, 1988.

[3] R. Redl, "Power Electronics and Electromagnetic Compatibility," in *IEEE 27th Annual Power Electronics Specialists Conference (PESC)*, vol. 1. Baveno, Italy, 1996, pp. 15-21.

[4] International Special Committee on Radio Interference, "Information technology equipment – Radio disturbance characteristics – Limits and methods of measurement," CISPR 22, Ed., 5 ed: International Electrotechinical Commission, 2005.

[5] V. P. Kodali, *Engineering Electromagnetic Compatibility: Principles, Measurements, Technologies, and Computer Models*, 2 ed: Wiley-IEEE Press, 2001.

[6] C. R. Paul and K. B. Hardin, "Diagnosis and Reduction of Conducted Noise Emissions," *IEEE Transaction on Electromagnetic Compatibility*, vol. 30, pp. 553-560, 1988.

[7] M. C. Caponet, F. Profumo, and A. Tenconi, "EMI Filters Design for Power Electronics," in *IEEE 33rd Annual Power Electronics Specialists Conference (PESC)*, vol. 4. Cairns, Qld., Australia, 2002, pp. 2027-2032.

[8] Q. Zhaoming, W. Xin, L. Zhengyu, and M. H. Pong, "Status of electromagnetic compatibility research in power electronics," in *The 3rd International Power Electronics and Motion Control Conference Proceedings (PIEMC)*, vol. 1. Beiging, China, 2000, pp. 46-57.

[9] V. Vlatkovic, D. Boroyevic, and F. C. Lee, "Input Filter Design for Power Factor Correction Circuits," *IEEE Transaction on Power Electronics*, vol. 11, pp. 199-205, 1996.

[10] L. Ferraris and C.-Y. Wu, "EMI Shielding-Common Problems and Containment Strategies," in *IEEE International Symposium on Electromagnetic Compatibility Proceeding (EMC)*. Beijing, China, 1997, pp. 86-89.

[11] W. Xin, F. N. K. Poon, C. M. Lee, M. H. Poon, and Z. Qian, "A Study of Common Mode Noise in Switching Power Supply from a Current Balancing Viewpoint," in *International Conference on Power Electronics and Drive Systems*, vol. 2. Hong Kong, 1999, pp. 621-625.

[12] T. Broom and I. W. Hofsajer, "Some Origins and Mitigation of Conducted Common Mode EMI in Switching Converters," in *Africon Conference in Africa*, vol. 2. George, South Africa, 2002, pp. 779-784.

[13] D. Cochrane, D. Y. Chen, and D. Boroyevich, "Passive Cancellation of Common-Mode Noise in Power Electronic Circuits," *IEEE Transactions on Power Electronics*, vol. 18, pp. 756-763, 2003.

[14] D. H. Liu, J. G. Jiang, and Z. M. Zhao, "A Systematic Approach to Analyze EMI in Control Circuit of Power Electronic Equipment," in *16th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, vol. 1. Anaheim, CA, 2001, pp. 208-212.

[15] L. Rossetto, S. Buso, and G. Spiazzi, "Conducted EMI Issues in a Boost PFC Design," in *12th International Telecommunications Energy Conference (INTELEC)*. San Francisco, CA, 1998, pp. 188-195.

[16] W. Zhang, M. T. Zhang, F. C. Lee, J. Roudet, and E. Clavel, "Conducted EMI Analysis of a Boost PFC Circuit," in *12th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, vol. 1. Atlanta, GA, 1997, pp. 223-229.

[17] K. N. Sakthivel, S. K. Das, and R. Ganesan, "Significance of critical components placement to control EMI in power supplies: A case study," presented at Proceedings of the International Conference on Electromagnetic Interference and Compatibility, 1999.

[18] J. Z. Chen, Y. F. Pang, D. Boroyevich, E. P. Scott, and K. A. Thole, "Electrical and thermal layout design considerations for integrated power electronic modules," in *IEEE 37th IAS Annual Meeting Conference Record of the Industry Applications Conference*, vol. 1. Pittsburgh, PA, 2002, pp. 242-246.

[19] J.-L. Schanen, L. Jourdan, and J. Roudat, "Layout optimization to reduce EMI of a switched mode power supply," in *IEEE 33rd Annual Power Electronics Specialists Conference, (PESC)*, vol. 4. Cairns, Qld., Australia, 2002, pp. 2021-2026.

[20] R. B. Ridley, "Average small-signal analysis of the boost power factor correction circuit," in *VPEC Seminar Proceedings*. Blacksburg, VA, 1989, pp. 108-120.

[21] L. H. Dixon, Jr., "High Power Factor Preregulator for Off-Line Power Supplies," Texas Instruments, Dallas, Texas 2001.

[22] M. Kchikack, Y. S. Yuan, Z. M. Qian, and M. H. Poon, "Modeling and Simulation for Conducted Common-Mode Current in Switching Circuits," in *IEEE International Symposium on Electromagnetic Compatibility Proceeding (EMC)*, vol. 1. Montreal, Que., Canada, 2001, pp. 681-685.

[23] M. N. Gitau, "Modeling Conducted EMI Noise Generation and Propagation in Boost Converters," in *Proceedings of the IEEE International Symposium on Industrial Electronics (ISIE)*, vol. 2. Cholula, Puebla, Mexico, 2000, pp. 353-358.

[24] B. Gutsmann, P. Mourick, and D. Silber, "Extract inductive parasitic extraction for analysis of IGBT parallel switching including DCB-backside eddy currents," in *IEEE*

31st Annual Power Electronics Specialist Conference (PESC), vol. 3, 2000, pp. 1291-1295.

[25] E. Ruehli and A. C. Cangellaris, "Progress in the methodologies for the electrical modeling of interconnects and electronic packages," *Proceedings of the IEEE*, vol. 89, pp. 740-771, 2001.

[26] J. A. Ferreira and S. J. Marais, "A new approach to model component parasitics," in *Conference Record of the 13th Annual IEEE Industry Applications Conference (IAS)*, vol. 2. Orlando, FL, 1995, pp. 1031-1037.

[27] S. Yan, J. Liu, and W. Shi, "Improving boundary element methods for parasitic extraction," presented at Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC) Kitakyushu, Japan, 2003.

[28] J. D. van Wyk, Jr., W. A. Cronje, J. D. van Wyk, P. J. Wolmarans, and C. K. Campbell, "Integrated power filters utilizing skin-and proximity effect based low-pass interconnects," in *IEEE/VDE 2nd International Conference Integrated Power Systems*, 2002, pp. 73-82.

[29] P. J. Wolmarans, J. D. van Wyk, J. D. van Wyk, Jr., and C. K. Campbell, "Technology for integrated RF-EMI transmission line filters for integrated power electronic modules," in *IEEE 37th IAS Annual Meeting Conference Record of the Industry Applications Conference*, vol. 3. Pittsburgh, PA, 2002, pp. 1774-1780.

[30] J. D. van Wyk, Jr., P. J. Wolmarans, J. D. van Wyk, and W. A. Cronje, "Integrated RF-EMI transmission line filters for integrated power electronics modules," in *Proceedings of CPES Seminar*, vol. 1. Blacksburg, VA, 2002, pp. 439-444.

[31] L. Zhao and J. D. van Wyk, "Electromagnetic modeling of an integrated RF EMI Filter," in *IEEE 38th IAS Annual Meeting Conference Record of the Industry Applications Conference*, vol. 3. Salt Lake City, UT, 2003, pp. 1601-1607.

[32] L. Zhao, R. Chen, and J. D. van Wyk, "An integrated common mode and differential mode transmission line RF-EMI filter," in *IEEE 35th Annual Power Electronics Specialists Conference (PESC)*, vol. 6. Aachen, Germany, 2004, pp. 4522-4526.

[33] L. Zhao, J. T. Strydom, and J. D. van Wyk, "The Modeling of Planar Multi-cell Integrated Reactive Components Based on Multi-conductor Generalized Transmission Structure Theory," in *IEEE 37th IAS Annual Meeting Conference Record of the Industry Applications Conference*, vol. 3. Pittsburgh, PA, 2002, pp. 1787-1794.

[34] R. Chen, "Integrated EMI filters for switch mode power supplies," in *Electrical and Computer Engineering*, vol. Ph.D. Blacksburg, VA: Virginia Polytechnic Institute and State University, 2004.

[35] "Maxwell 3D Field Solver," 10.0 ed. Pittsburgh, PA: Ansoft Corporation, 2005.

[36] L. Yang, "Modeling and characterization of a PFC converter in the medium and high frequency ranges for predicting the conducted EMI," in *Electrical and Computer Engineering*, vol. Masters. Blacksburg, VA: Virginia Polytechnic Institute and State University, 2003.

[37] M. Trivedi and K. Shenai, "Parasitic extraction methodology for insulated gate bipolar transistors," *IEEE Transactions on Power Electronics*, vol. 15, pp. 779-804, 2000.

[38] H. Zhu, A. R. Hefner, Jr., and J.-S. Lai, "Characterization of power electronics system interconnect parasitics using time domain reflectometry," *IEEE Transactions on Power Electronics*, vol. 14, pp. 622-628, 199.

[39] E. McShane and K. Shanai, "RF de-embedding technique for extracting power MOSFET package parasitics," in *International Workshop on Integrated Power Packaging (IWIPP)*, 2000, pp. 55-59.

[40] "Simplorer," 7 ed. Pittsburgh, PA: Ansoft Corporation, 2005.

[41] "MATLAB/Simulink," 14 ed. Natick, MA: MathWorks, 2005.

[42] J. A. Ferreira, *Electromagnetic Modeling of Power Electronic Converters*. Boston: Kluwer, 1989.

[43] "SDP06S60 Datasheet," Infineon Technologies, 2001.

[44] "SPW20N60C3 Datasheet," Infineon Technologies, 2003.

[45] Q. Liu, "Modular Approach for Characterizing and Modeling Conducted EMI Emissions in Power Converters," in *Electrical and Computer Engineering*, vol. Ph.D. Blacksburg, Virginia: Virginia Polytechnic Institute and State University, 2005, pp. 188.

[46] R. D. Middlebrook, "Design Techniques for Preventing Input-Filter Oscillations in Switched-Mode Regulators," presented at Fifth National Solid State Power Conversion Conference, 1978.

[47] R. D. Middlebrook, "Input Filter Considerations in Design and Application of Switching Regulators," presented at IEEE Industry Applications Society, 1976.

[48] Y. Liang, C. Rengang, and J. D. van Wyk, "Large Signal Dielectric Characterization for Integrated Electromagnetic Power Passives," presented at 20th Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2005.

[49] D. M. Mattox, *Handbook of Physical Vapor Deposition (PVD) Processing*. Westwood, NJ: Noyes, 1998.

VITA

The author, Andrew Carson Baisden was born on August 20, 1979. He grew up in Naperville, IL where he earned two Bachelors of Science degrees: one from the Illinois Institute of Technology in Electrical Engineering in 2003 and another from Benedictine University in Mathematics and Engineering Sciences in 2003. He has worked for Argonne National Laboratories in the summers of 2000, 2001, and 2002. Since August 2003 he has been at Virginia Tech working towards a Masters of Science and a Doctoral degree in the area of Power Electronics with the Center for Power Electronic Systems. His research interests include electromagnetic interference, modeling and design of EMI and power electronics, and integration of power electronic converters.