Extending the Flexibility of an RFIC Transceiver Through Modifications to the External Circuit

by

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(ABSTRACT)

The recent trend in the RF and microwave industry has been a move towards increasing the number of components realized on one radio frequency integrated circuit (RFIC) (or microwave integrated circuit (MIC)). This trend has resulted in complex RFICs which often require reactive as well as other circuit components to be supplied in the form of an external circuit. Because the manufacturer's suggested circuit is often developed with a specific application in mind, the same circuit may not satisfy the demands of another application. Provided the necessary functionality and connections are possible, the external circuit may be altered such that the requirements of the other application can be met, thus extending the flexibility of the RFIC.

The work presented here is focused on investigating modifications to RF Microdevices' suggested external circuit for the RF29X5 family of low cost, half duplex, FM/AM/ASK/FSK RFIC transceivers originally intended for operation in the 433, 868, or 902-928 MHz industrial, scientific, and measurement (ISM) bands. Examinations of the operating principles of the transceiver components were performed which facilitated the identification of suitable modifications. Among the modifications identified were implementation of a phase locked detector, various methods for extending the FSK data rate limitations of the transmitter, improving the phase noise of the VCO, and the implementation of a fractional-N synthesizer using the RF2905 internal phase-locked loop (PLL) components and external inexpensive logic circuits. In addition to these modifications to the external circuit, the investigation of the oscillators of the RF2905 resulted in a potentially improved implementation of the VCO by modifying the internal active circuitry as well.

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1. Introduction

1.1 Motivations

Usually, a manufacturer of an RFIC will design it for a specific application or group of applications. The requirements of these applications (operating frequency range, output power, etc.) tend to shape the specification of the device and the external circuit in which the RFIC is implemented. For simple RFICs, such as I-Q modulators or down converters, there are very few other ways of implementing the external circuit outside of varying the bandwidth and center frequency of the matching provided to the IC. In the case of the more complicated RFICs, there exists the potential for a variety of implementations and applications outside the manufacturer's original conception. This is exactly the situation of the RF29X5 transceiver family produced by RF Microdevices. The connections available between the internal components of the RFIC and the external circuit on each of the RF29X5 transceivers allow most of the on-chip component inputs and outputs to be directly available to the external circuit. This arrangement provides wide flexibility in the implementation of the transceivers since the topology of the external circuit can be varied to meet the needs of the application.

The aim of the work presented has been to explore the aspect of finding alternative ways of implementing the external circuit for the RF2905 and related transceiver family. In some instances, these alternate implementations are intended to overcome limitations of the original manufacturer's implementation. In others, they create entirely new possibilities for using the chip. These RFIC transceivers were originally intended to be incorporated into consumer devices as inexpensive, half-duplex transceiver radios. They are capable of transmitting up to 2 Mb/s using a frequency shift keying (FSK) modulation format at output powers ranging from –10 dBm to +10 dBm. Though the devices are specified to operate over the range 300-1000 MHz, the manufacturer's specifications are focused on operation within Industrial, Scientific, and Measurement (ISM) bands (433, 868, 902-928 MHz) which do not require a license to operate. For the designer who can sacrifice cost for increased functionality or who may want to use the transceiver at

different frequencies, there is a limited amount of information available concerning the operation of the transceiver outside its intended application.

The focus of the work undertaken was to analyze and measure the performance of the components present within the RF2905 and identify, where possible, alternative external circuit implementations that may provide some advantage over the typical recommended circuits. As an inevitable result of this process, potential improvements to the internal circuits of the transceiver were also identified.

1.2 Literature Review

The development of new circuits and applications for an existing RFIC is an interesting and often challenging task. Very often the manufacturer has already spent a great deal of time developing the external circuit for the product in order to ensure its performance is superior to competitors' products. Since the work presented here is specifically focused on finding new applications and implementations, the manufacturer's suggested external circuit is simply a starting point. In order to proceed from this starting point, each of the components and the systems composed of those components must be well understood.

The fundamental principles of the phase-locked loop (PLL) at the heart of the system must be grasped for any significant understanding of the system. Because the phase-locked frequency source provides the carrier for both the transmitter and the receiver local oscillator, it is an essential part of the overall transceiver design. Authors such as Blanchard, Gardner, and Egan [1-3] have excellent books providing both introductions and more detailed analyses and applications of phase-locked loops. There also exists a wealth of application notes provided by Motorola and National Semiconductor on the design of PLLs and their various applications from the company web pages (www.mot.com and www.national.com).

One such application, the PLL frequency synthesizer, has a wealth of information devoted to it in the form of traditional references, applications notes, and technical society papers. This application bears a special importance to the present work because of the successful investigation for modifying the external circuit of the RF2905 to incorporate

fractional-N frequency synthesis. Frequency synthesizers have become a common component in portable wireless devices. The advantages of fractional-N frequency synthesis [4] have prompted the development of new integrated circuits which realize these kinds of synthesizers. Several very well known references exist for frequency synthesizers by authors such as Rohde[5], Manassewitsch[6], and Crawford[7]. An interesting technical paper by Nakagawa and Tsukahara[8] provides a concise description of the non-standard form fractional-N synthesis to be implemented with the RF2905. A large number of other papers regarding the various aspects of the standard fractional-N synthesis have appeared recently, most of which are concerned with the phase noise of the fractional N synthesizer.[9-11]

The phase noise aspect of both oscillators and frequency synthesizers has attracted a fair amount of attention. Originally, phase noise was only a major concern in radar and space applications where the received power of an information-bearing signal is extremely low. With the increased number of wireless devices sharing common spectrum, phase noise begins to present a concern in other applications as well as tending to reduce receiver sensitivity in environments with strong adjacent channel interferers. A good reference on the subject of phase noise is W.P. Robins' book [12] which unfortunately is out of print. Many of the previously mentioned references on synthesizers also include a chapter or section devoted to the subject of phase noise. Additionally, Hewlett Packard also provides application notes [13][14] which clearly explain both the principles of phase noise and the techniques for minimizing it. Phase noise in oscillators, is also treated in these application notes as well as in many technical papers and articles in the trade literature.

The oscillators in the PLL act as the primary sources of phase noise, though there are other sources that should not be overlooked. Research into improving synthesizer phase noise ultimately rests on the analysis of the oscillators themselves. Numerous descriptions of oscillators and their basic operating principles appear in almost every introductory text on RF circuits; however, very few actually delve into the actual nonlinear behavior of the oscillator required to predict the output drive level of the oscillator. Since the phase noise model of the oscillator known as Leeson's equation [16]

requires this value, a more advanced reference by Clarke and Hess [17] which deals with the nonlinear aspects of oscillators and other circuits proves indispensable for these situations.

1.3 Thesis Organization

The focus of this thesis is on the development of a fractional-N synthesizer using the RF2905, and to a lesser extent, the oscillators of the RF2905. Some additional background material is included to provide a treatment of the entire transceiver. This thesis starts with an initial overview of the basic transceiver, which includes the manufacturer's intended applications and the potential for other applications. The possibility for implementing a phase-locked discriminator instead a quadrature detector for FM detection is discussed. Limitations of the transmitter are discussed along with limitations on the transmitter modulation. Several methods are proposed for extending these limitations to fit the designer's needs. The operation of the oscillators, which plays the key role in controlling the performance of the RF2905, is then discussed in detail. This discussion ultimately results in a proposed improvement to a current voltage controlled oscillator (VCO) implemented on the chip and a relatively new way of looking at noise in oscillators. In addition to other contributors, the impact of the reference oscillator and VCO noise on the overall phase noise of the RF2905 PLL is discussed. The culmination of the discussion is the introduction and implementation of a simple method for making the RF2905 PLL into a fractional-N frequency synthesizer. Along with other possibilities, the potential for implementing a frequency hopped spread spectrum (FHSS) transceiver is presented before concluding.

2. Transceiver Overview

2.0 Chapter Overview

This chapter is intended to provide the reader with an overview of the architecture of the RF2905 transceiver, its functional capabilities, and applications. The RF2905 is a member of a family of products produced by RF Microdevices as a set of inexpensive transceivers for European and North American Industrial, Scientific, and Measurement (ISM) band applications. These radio frequency integrated circuits (RFICs) are intended to be operated in the 433 MHz or 868 MHz European ISM bands or the 902-928 North American ISM band. The RF2905 RFIC transceiver is the specific focus of this work, however, many of the points made throughout apply to the other members of the RF29X5 family(RF2905, RF2925, RF2915, and RF2945).

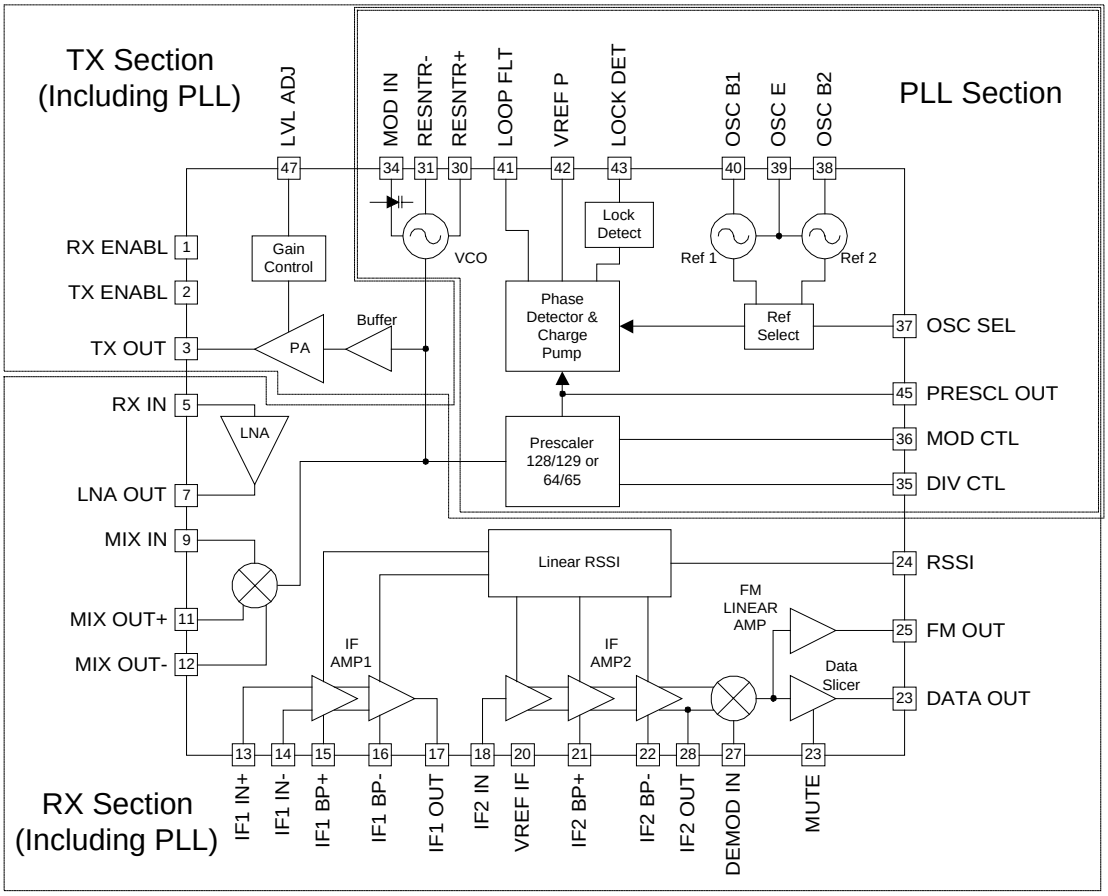


Figure 2.1. RF2905 functional block diagram from RF2905 data sheet.

2.1 Integrated Circuit Architecture and Capabilities

The RF2905 RFIC block diagram is presented in Fig. 2.1. Dividing lines have been added to the block diagram in order to highlight the three major systems that compose the RF2905 transceiver, namely the phase-locked loop (PLL) frequency source, the transmitter, and the receiver. As indicated by Fig. 2.1, the PLL frequency source is the common block shared by both the receiver and the transmitter. Both the receiver and transmitter have independent power connections as well as a power down pin to reduce power consumption when the chip is in an idle state. These sections will now be broken out further into the components realized on the chip.

2.1.1. PLL Frequency Source

The components realized within the IC are the dual-modulus, dual-divisor prescaler, the phase detector with charge pump(providing a tristate output), and the active circuitry for a pair of crystal controlled reference oscillators and a saturating balanced pair voltage controlled oscillator (VCO). Each reference oscillator requires two capacitors and a quartz crystal to be fully functional, while the VCO requires a voltage adjustable resonant network to be fully realized. The only other building block required is the loop filter which connects the output of the charge pump to the control voltage input of the VCO. The internal interconnections of the on-chip devices are depicted in Fig. 2.1. Upon connecting the loop filter and other external components, a complete PLL frequency source is ready for use.

2.1.2. Transmitter Section

The transmitter section is composed of the PLL frequency source, the power amplifier, and the modulation input to the VCO. The transmitter is capable of either amplitude modulation (AM) or frequency modulation(FM) for analog signals whose digital signal equivalents are amplitude-shift keying(ASK) and frequency-shift keying(FSK). The AM/ ASK modulation format is achieved by applying the modulating signal to the LVL ADJ which controls the output signal amplitude. To perform FM/ FSK modulation, an internal pair of varactor diodes are provided via the MOD IN pin which are connected to the resonator input pins.

2.1.3. Receiver Section

The receiver section follows the standard superheterodyne radio receiver structure optimized for FM signal reception while still retaining some provision for AM signal detection. All of the active receiver components are realized internally leaving only the reactive components, preselector, and IF band pass filters to be realized externally. Because the preselector filter could be placed before or after the low noise amplifier (LNA), the input and output connections of the LNA are done externally. The impedance matching and biasing for the LNA are also provided externally via inductors. This is also the case for the first mixer which has one external input and a balanced output used for external connection. The other input to the mixer is internally connected to the VCO of the PLL frequency source which acts as the local oscillator (LO) for the receiver. The balanced output of the mixer is intended to be connected to the first IF band-pass filter, in turn connecting to the first limiting IF amplifier strip. The output of this stage is meant to connect to another IF band-pass filter which then connects to the second IF amplifier strip. The detector is intended to be a quadrature detector which is composed of both on chip and off chip components. The on chip portion of the detector is a mixer with one input connected internally to the output of the second stage of IF amplifiers, and the output connected internally to an RC low pass filter with cut off frequency of 1.6 MHz. This filter then connects to a “data slicer” (or preconfigured comparator) and a linear amplifier, the outputs of each are provided externally.

Demodulation in the receiver is achieved by one of two methods depending on the original format of the transmitted signal. For FM signals, the quadrature detector demodulates the limited FM signal and the low pass filtered analog signal is available from the FM OUT pin or a digital form of the output can be obtained from the DATA OUT pin. Since the amplitude modulation is actually a power modulation, the received signal strength indicator (RSSI) output is used as the detector for amplitude modulated signals.

2.2 Intended Applications

The RF29X5 family are intended for very low cost, relatively short range applications such as keyless entry, remote meter reading, security systems applications, and simple, wireless data radios. Excluding the latter application, these applications basically require a very simple radio operating only part of the time with a burst mode transmission format. Several of these applications involve battery operation for which several power down controls are provided to lengthen battery life. Additionally, due to the structure of the transceiver, only half-duplex operation is possible.

2.3 Other Potential Applications and Implementations

Because of the shared wireless channel, this family of transceivers is envisioned as providing an inexpensive wireless wire between two devices. Because the data directly modulates the VCO of the PLL, a long sequence of digital ones or zeros may potentially be tracked out by the PLL of the transmitting transceiver. While the precise nature of the tracking mechanism is left as the focus of Sec. 4.2.2, and simple methods for overcoming this low frequency limitation have been proposed in Sec. 4.3, making the wireless wire application still viable. It is also foreseeable that the transceiver could be used as a remote control with a feedback to the user on the device or system under control. This opens up the possibility for a telemetry system as well.

With the functionality already present in the transceiver, the potential for implementing it with a fractional-N frequency synthesis frequency source is explored in detail in Ch. 7. This potential opens up the possibility to implement the RF29X5 transceivers as frequency hopped spread spectrum (FHSS) transceivers, and creates the opportunity to use an external power amplifier to increase the range over which the radio can transmit. The fractional-N technique can be used to channelize the ISM band into more channels and provide a greater flexibility in end product frequency selection. Other alternate implementations that have been considered include modifications to the FM detector to increase the capture range of the receiver, creating an multilevel FSK system, and a potential improvement to the VCO currently implemented.

3. Receiver

3.0 Chapter Overview

The receiver of the RF29X5 family employs the standard superheterodyne architecture which dominates radio architecture today. Since there is little that can be done to the external circuit besides changing the frequency modulation (FM) detector circuit, this chapter primarily focuses on the basic operating principles of the receiver and its components. After briefly reviewing the structure of the receiver, the effect of the limiting mechanism on the noise performance of the intermediate frequency (IF) amplifiers is examined. The focus then moves down the receiver structure to the operating theory of the quadrature detector, and finishes with the potential modification of the receiver structure to implement a phase-locked loop as an FM detector.

3.1 FM/FSK Receiver Structure with Quadrature Detector

The manufacturer's suggested implementation of the RF2905 receiver is illustrated in Fig. 3.1. The LNA and mixer use external components to provide impedance matching, allowing the designer to use filters with other than 50 Ω impedances and also to use the bandwidth of the impedance match as part of the IF or image filtering. Although there is no provision for an automatic gain control (AGC), the received signal strength indicator (RSSI) output does allow the designer to build in a squelch circuit of sorts that disables

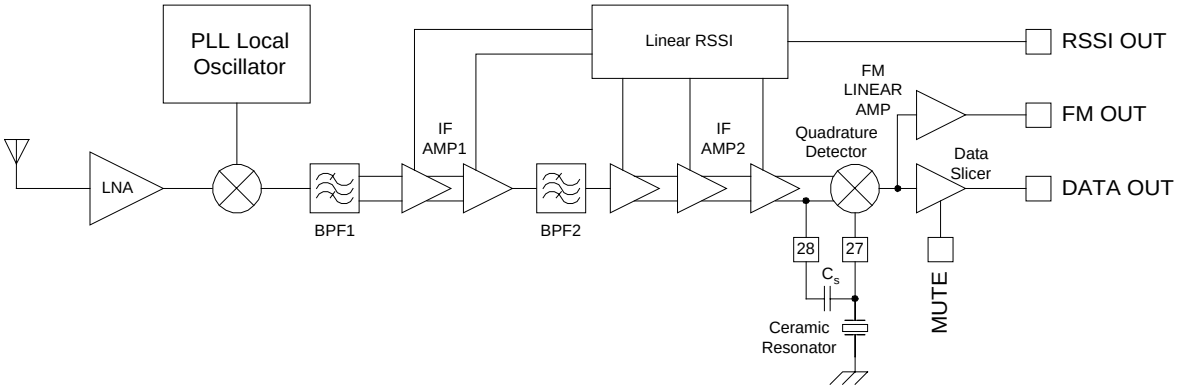


Figure 3.1. Manufacturer's suggested implementation of RF2905 receiver.

the demodulation output when the receiver signal power is below a certain threshold. The RSSI acts as the detector for on-off keyed (OOK) or AM signals as well.

3.1.1. The Limiting Mechanism of the RF2905 IF Chain

Limiting in FM receivers using a quadrature detector is practically essential to ensure reliable FM demodulation. Unlike more complicated I-Q phase modulated schemes which require both amplitude and phase linearity in the receiver, the FM receiver detects the instantaneous frequency of the carrier. Variations in the amplitude of the carrier degrade this ability to some degree which is why most practical FM receivers possess a limiter for the purpose of removing most of the AM variations imposed on the FM signals. The RF2905 IF amplifiers are designed so that they can perform this function without saturating the transistors that make up the amplifiers. Due to the nonlinear characteristic of the differential pair amplifiers making up the IF amplifiers, very small signals (less than 78 mV_{pk}) are amplified almost linearly while larger signals are amplified less. For large signals (approximately 260 mV_{pk} and greater), the amplifier actually ceases to amplify the signal and produces a constant output voltage signal whose peaks begin to become flattened. Because the output of the amplifiers are filtered, the harmonics produced by the flattening of the received signal do not interfere with the demodulation process. The effect limiting has on the spectrum of the signal applied to the detector is not intuitively obvious, especially for those more familiar with systems employing I-Q modulation.

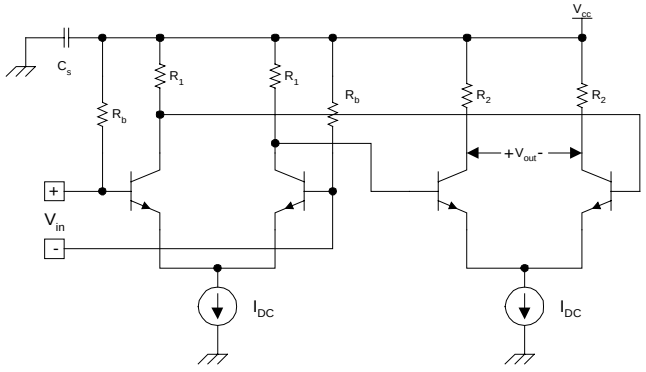
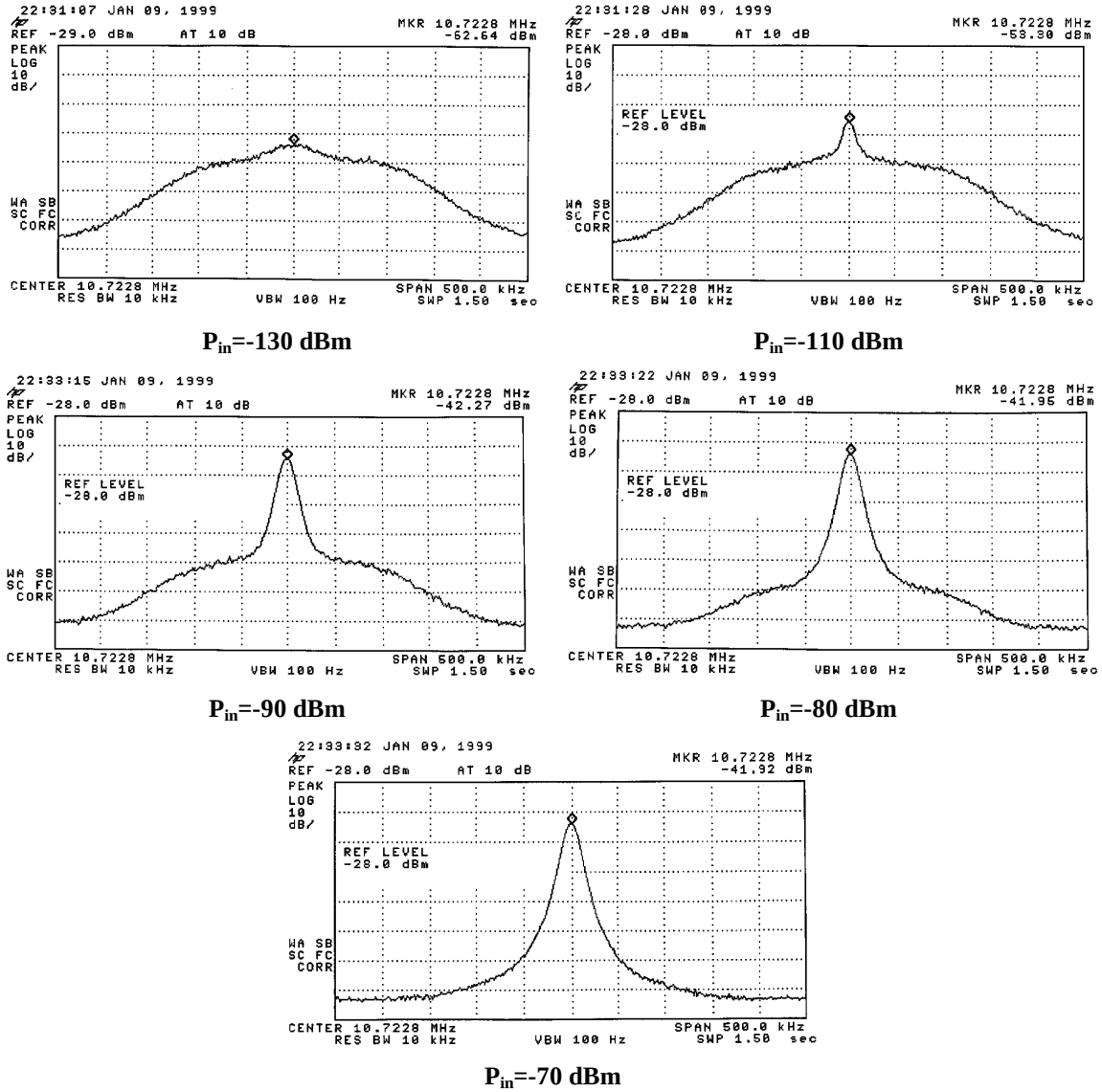


Figure 3.2. Representation of one possible IF amplifier circuit typology.

To illustrate the effect of limiting on the IF spectrum, measurements of the final IF amplifier output spectrum under several different received power conditions are presented in Fig. 3.3 in order of increasing signal power. The apparent effect of the increasing signal power is first to increase the power in the carrier until a drive level is reached that causes the thermal noise to decrease while the carrier power stays constant. This behavior is at first somewhat counter-intuitive due to the general familiarity with AM systems where additive thermal noise never decreases but instead the power of the modulated carrier is increased. Initially, both the signal and the noise are weak enough



P_{in}=-130 dBm **P_{in}=-110 dBm**

P_{in}=-90 dBm **P_{in}=-80 dBm**

P_{in}=-70 dBm

Figure 3.3 IF amplifier limiting effect on noise floor, measured at the IF output for various input carrier levels, vertical scale 10 dB / div with a maximum of –28 dBm, horizontal scale 50 kHz / div.

to allow the IF amplifiers to operate linearly. As the carrier power level increases, the IF amplifiers begin limiting. Since the output power of the IF amplifiers is fixed, the harder the carrier signal drives the IF amplifiers, the greater the portion of the output power present in the carrier signal at the output. Eventually a limit is reached where all of the IF amplifier output power resides in the carrier signal.

3.1.2 Quadrature Detector

The FM detector scheme intended for use in the RF2905 is a quadrature detector. As shown by the block diagram in Fig. 3.4, the detector is composed of a mixer, a passive phase shift network and a low pass filter. On a very conceptual level, the signals V_1 and V_2 are essentially the same signal except V_2 possesses a phase shift with respect to to V_1 (it is assumed that the phase shift network has no influence on their relative amplitudes.).

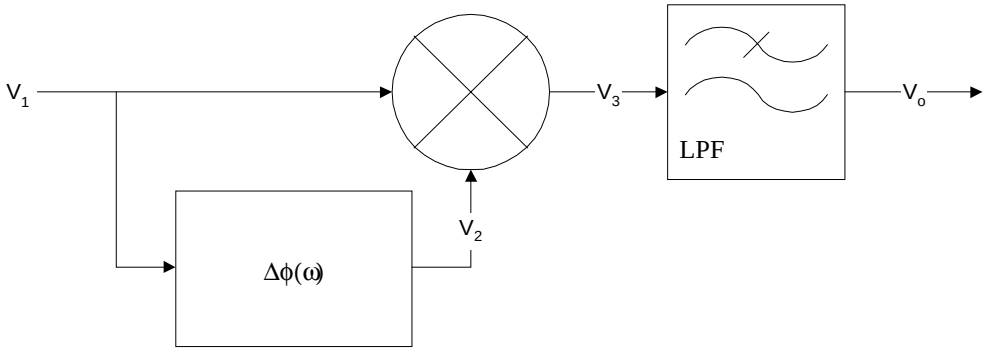


Figure 3.4. Diagram of quadrature detector composed of mixer, low pass filter, and phasing circuit.

The signal V_1 can be expressed as a sinusoidal carrier whose instantaneous frequency is some function of time, consistent with the expected frequency modulation it is assumed to possess. Similarly, V_2 can also be expressed in the same manner by including the phase change as a function of frequency incurred by passing through the phase shift network. Proceeding in this manner, the two signals at the input ports of the mixer are,

$$V_1 = A_1 \cos\omega(t)t \tag{3.1}$$

$$V_2 = A_2 \cos\left(\omega(t)t + \phi(\omega)\right) \tag{3.2}$$

and their product can be expressed using simple trigonometric identities as given by

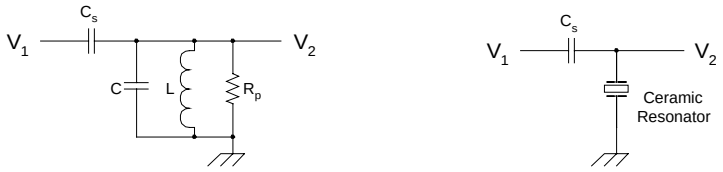
$$V_1 V_2 = \frac{A_1 A_2}{2}\left[\cos\left(2\omega(t)t + \phi(\omega)\right) + \cos\phi(\omega)\right] \tag{3.3}$$

Assuming the cut off frequency of the low pass filter is chosen such that the higher frequency component is removed and that the product of A_1 and A_2 is constant, the resulting detector output voltage is given approximately by,

$$V_o = C\cos\phi(\omega) \tag{3.4}$$

The expression clearly indicates the output signal is directly dependent upon the phase shift contributed by the phase shift network. Because the phase shift is directly related to the instantaneous frequency of V_1 the exact relationship between the instantaneous frequency of V_1 and the phase shift of the network must be examined.

The typical implementations of the phase shift network are depicted in Fig. 3.5. For the sake of argument, the input impedance of the mixer shall be assumed high enough



(a) (b)

Figure 3.5. Typical phase shift network implementations.

such that it will not affect the properties of the phase shift network, and that the mixing process operates on the voltages appearing at the input ports of the mixer. Because the structure depicted in Fig. 3.5b can be treated in a similar manner as that of Fig. 3.5a, the analysis will first focus on the circuit typology of Fig. 3.5a. The series combination of voltage source V_1 and the capacitor C_s can be converted using a Norton equivalent source composed of parallel current source of value $j\omega C_s V_1$ and parallel capacitor of value C_s as depicted in Fig. 3.6.

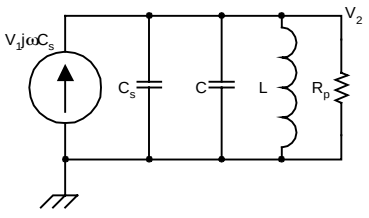


Figure 3.6. Norton equivalent representation of Fig. 3.5a.

The value of V_2 is now given by the simple equation,

$$V_2 = I \times Z(j\omega) = j\omega C_s V_1 \times Z(j\omega) \tag{3.5}$$

where Z(jω) is given by,

$$Z(j\omega) = \frac{R_p}{1 + jQ\left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega}\right)} \tag{3.6}$$

and Q and ω_o are related to the network parameters by,

$$Q = \frac{R_p}{\omega_o L} = R_p \omega_o (C + C_s) \qquad \text{and} \qquad \omega_o^2 = \frac{1}{L(C + C_s)} \tag{3.7a \& b}$$

Using voltage phasors to find the phase shift contributed by the network to V_2 with respect to V_1 and then substituting the result into the output voltage versus frequency characteristic results in

$$\phi(\omega) = \tfrac{\pi}{2} - \tan^{-1} Q\left(\tfrac{\omega}{\omega_o} - \tfrac{\omega_o}{\omega}\right) \tag{3.8}$$

and

$$V_o = C\cos\left[\tfrac{\pi}{2} - \tan^{-1} Q\left(\tfrac{\omega}{\omega_o} - \tfrac{\omega_o}{\omega}\right)\right] = C\sin\left[\tan^{-1} Q\left(\tfrac{\omega}{\omega_o} - \tfrac{\omega_o}{\omega}\right)\right] \tag{3.9}$$

It is interesting to note that upon passing through capacitor C_s , the input signal is already shifted in phase by +90°. Thus, to swing the output of the quadrature detector to plus-or-minus full scale, the resonant network has only to provide an additional ±90° of phase shift.

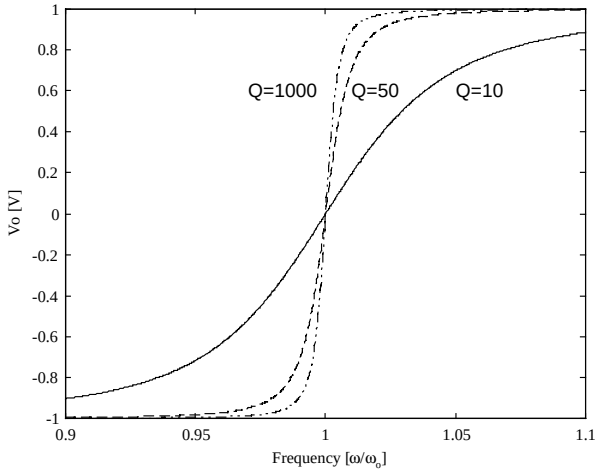


Figure 3.7. Quadrature detector output voltage vs. frequency characteristic for different parallel phase shift network Q values.

The frequency-to-voltage characteristic curve, normalized to ω_o of the phase shift network, has been plotted for several values of phase shift network Q in Fig. 3.7. The plot indicates that the Q of the parallel phase shift network can be viewed as controlling the conversion gain of the instantaneous frequency-to-voltage conversion process in the linear range where the demodulation voltage is directly dependent upon the instantaneous phase difference between the two signals. Because the difference between the instantaneous frequency and ω_o is small, the slope of the characteristic can be approximated as $2Q(\Delta\omega/\omega_o)$ where $\Delta\omega$ is the difference between the instantaneous frequency and the resonant frequency of the network. In the case of linear FM, the frequency-to-voltage characteristic should possess a linear slope and the peak frequency deviation of the signal should not extend beyond the linear range of the characteristic. For FSK systems, the requirements on linearity are relaxed since making a decision between high and low logic levels is the primary concern. In this case, the optimum slope is steep enough to cause the output voltage to limit slightly with the maximum frequency shift of the data. Beyond this optimum slope, the detector output signal-to-noise ratio is degraded since the noise components are amplified while the desired signal is limited. For this reason, excessively high phase shift network Q values should be avoided.

Commercial Frequency Discriminators

The use of a parallel tuned phase shift network will most likely require at least three to five parts and some manual adjustment of the resonant frequency such that it will coincide with the IF center frequency. Several manufacturers produce components which are termed frequency discriminators, but these components are nothing more than ceramic resonators. These resonators behave much like a quartz crystal resonator except the Q of the ceramic resonator is substantially lower than that of a quartz crystal. To illustrate the similarity between the two, the ceramic resonator used on the evaluation board of the RF2905 was measured using an HP vector impedance meter. The resonator model near its fundamental resonance is illustrated in Fig. 3.8. The values of this model based on vector impedance measurements were L = 160 µH, C = 1.45 pF, C_o = 15 pF and R_s = 28 Ω.

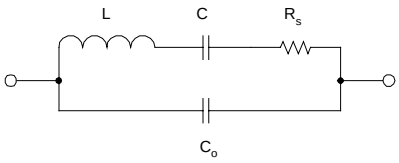
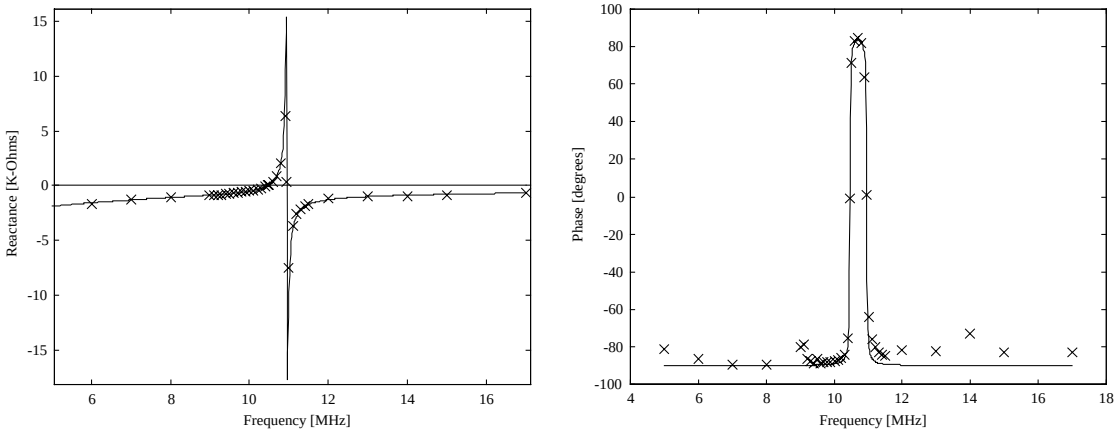


Figure 3.8. Model of quartz crystal near fundamental resonance.

As a means of comparison, the model parameters for a 10.000 MHz quartz crystal measured under the same conditions were L = 9.7 mH, C = 26.11 fF, Co = 8 pF, and Rs = 7.5 Ω, indicating the substantially higher Q of the quartz crystal resonator. The resulting match between the crystal model and the measured ceramic resonator is illustrated in Fig. 3.9 where each "x" corresponds to a measured data point and the solid line corresponds to the values predicted by the model.



a. b.

Figure 3.9. Reactance (a) and phase shift (b) characteristics of the ceramic discriminator.

The effect of the series capacitor will be simply to move the parallel resonant frequency to the left, toward the series resonance frequency and provide a parallel tuned circuit equivalent. Unlike the parallel resonant phase shift network, the ceramic resonator's phase shift returns to -90° near its series resonant frequency limiting the maximum frequency deviation that can be demodulated. One might think of using the phase shift provided by the series resonance; however, the loading due to the low series resistance associated with the series resonance of the resonator will prevent the input of the mixer from limiting. Without the limiting mechanism present, any AM modulation components of the received signal will potentially affect the demodulated signal adversely. A similar phenomenon occurs in between the pass band and stop bands of the

IF filters where the attenuation is not great enough to completely attenuate the signal but is great enough to prevent the signal from limiting at the input of the demodulator. In this case, the output voltage is reduced despite the fact that there is enough frequency deviation to cause the phase shift to range between 0° or 180°.

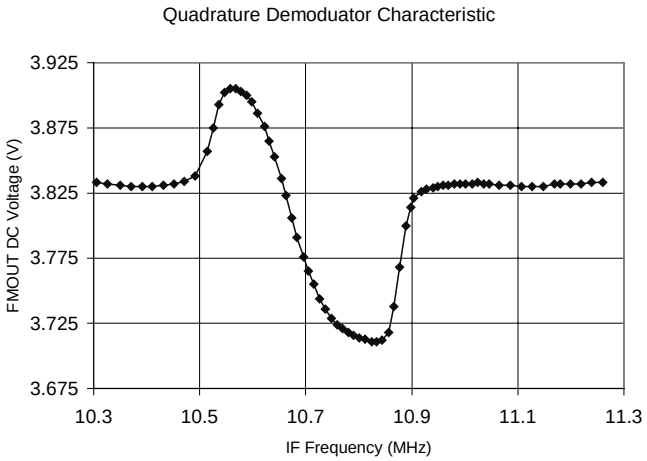


Figure 3.10. Voltage vs. Frequency characteristic of quadrature detector.

An output voltage versus frequency characteristic was measured with the IF filters and discriminator in place on the manufacturer's evaluation board, and it appears in Fig. 3.10. For frequencies that lie outside the pass-band of the IF filters, the attenuation afforded by the filters no longer causes the input to the quadrature detector to limit. Without limiting, the detector output voltage increasingly depends on both the FM deviations of the carrier and the amplitude of the signal at the detector input which gives rise to the nonlinear "S" shape of the voltage-to-frequency characteristic of the detector. For reliable FM demodulation, operation is intended to take place only over the linear range of the detector characteristic.

3.2 Receiver Modifications

Because there is little room for modification within the receiver structure of the RF2905, only two modifications will be mentioned here. The first is the addition of a squelch circuit which uses the RSSI output to determine when a received signal is too weak to demodulate reliably. This is easily accomplished using a CMOS comparator (LM339 or comparable) in a hysteresis circuit. Once the received signal strength rises

above a certain threshold, the comparator disables the MUTE control on the receiver which allows data to appear at the DATA OUT pin until the RSSI falls below an acceptable level, and the comparator then enables the MUTE control.

The second modification involves replacing the quadrature detector with a phase-locked loop to be used as a phase-locked discriminator (PLD). The incorporation of a PLD into the RF2905 receiver is presented here on a conceptual level as one particular modification that designers may wish to consider. Gardner has pointed out the advantage of using a phase locked discriminator as opposed to an ideal FM detector [2] whose output voltage is linearly proportional to the instantaneous frequency of the input signal. Over its linear range of operation, the quadrature detector approximates the ideal FM detector. Similarly, a phase locked loop's error voltage is dependent upon the instantaneous frequency difference between the reference (which in this case is the received signal) and the VCO signal. The phase locked loop not only tracks frequency, but phase as well, which gives it a distinct advantage over the idealized FM detector in the form of an "extended capture range"[2]. The extended capture range means simply that a linear relationship exists between the detector output signal-to-noise ratio and the input carrier-to-noise ratio for the PLD over a greater amplitude range than for the ideal FM detector.

There are several ways the manufacturer's typical circuit can be augmented to obtain a PLD type detector. An external phase locked loop integrated circuit such as the 74HC4046 which contains an internal phase detector and VCO can be connected to the output of the second IF amplifier. This solution is an expensive one compared to using the mixer originally intended to be the quadrature detector as the phase detector of the PLD. Using the quadrature detector to detect phase, an external oscillator or multivibrator circuit or the on-board PLL (which supplies the local oscillator) could be used as the VCO section of the PLD at a much lower cost. The on-board PLL implementation requires a fixed offset oscillator to be built and applied to the second mixer. This structure, depicted in Fig. 3.11, has an advantages in that a cheap TTL clock oscillator might be used for the fixed oscillator rather than designing an external oscillator to act as the VCO. To some extent, the additional circuitry required to pull the

reference oscillator and the potential implications for the on-board PLL bandwidth, may ultimately make this method less advantageous than using an external low frequency VCO.

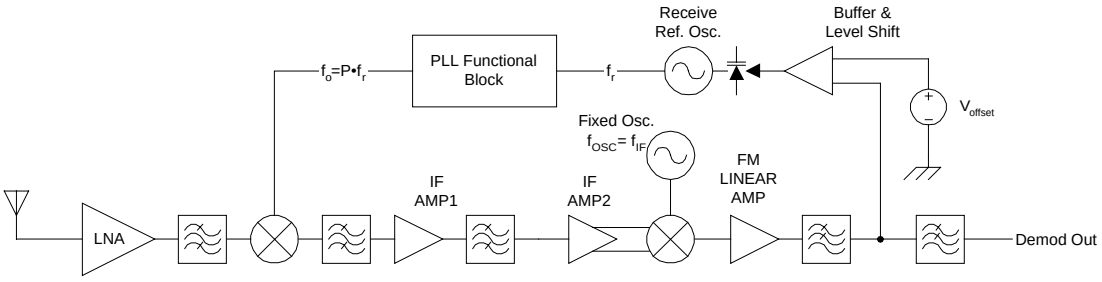


Figure 3.11. Illustration of a potential RF2905 PLD setup.

Several important considerations must be accounted for in order to determine the practicality of the PLD structure of Fig. 3.11. The optimum loop filter for the discriminator application must be identified. The value of the gain and offset voltage required from the buffer to drive the reference oscillator pulling scheme must be found. The PLL loop bandwidth must be greater than that of the PLD loop bandwidth in order to prevent a new delay mechanism from being introduced into the phase-locked loop. Unfortunately, the PLD bandwidth must be on the order of the maximum modulation bandwidth, which creates a conflicting requirement for the on-board PLL bandwidth if the internal varactor diodes are to be used. Also, some provision must be made to prevent the on-board PLL output frequency moving out of the locking range when no receive signal is present, and potentially the same or an additional circuit must sweep the PLL if it does not lock when a signal is present. Finally, the fixed oscillator must still be supplied and the output level set such that it drives the second mixer at the appropriate level.

4. Transmitter

4.0 Chapter Overview

This chapter is devoted to various aspects of the transmitter. The structure of the transmitter is reviewed followed by a brief look at the influence the power amplifier (PA) exerts on the remainder of the transmitter circuitry. Then the limitations imposed on the operation of the transmitter by the on board phase-locked loop (PLL) frequency source are considered before concluding with a presentation of simple methods to overcome these limitations.

4.1 Transmitter Concepts

The transmitter is composed of the power amplifier(PA) and PLL frequency source which are internally connected together. A block diagram of the transmitter implemented on the manufacturer's evaluation board appears in Fig. 4.1. The transmitter is capable of generating either frequency or amplitude modulated signals and potentially both at the same time. Frequency Modulation (FM) is achieved through a pair of internal varactor diodes which pull the instantaneous frequency of the Voltage Controlled Oscillator (VCO) of the PLL frequency source in proportion to their reverse bias voltage. These varactor diodes are connected to the external circuit via the MOD IN pin of the RF2905. Amplitude modulation (AM) is performed by applying the modulation signal to the LVL ADJ pin, which alters the bias point of the PA such that the fundamental output power level is a direct function of the voltage applied to the LVL ADJ pin. If the peak voltage of the output were linearly dependent on the LVL ADJ pin, a vertical log scale plot of

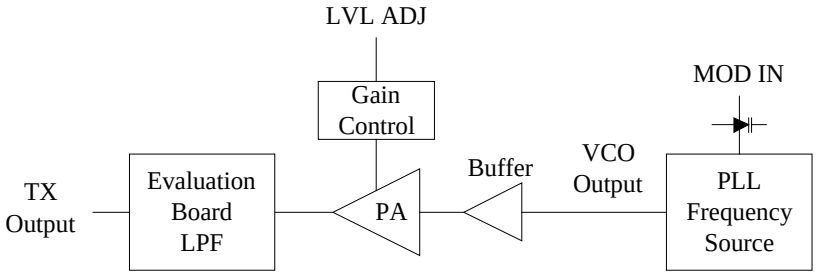


Figure 4.1. Block diagram of transmitter.

fundamental output power versus the logarithm of the LVL ADJ voltage should have a linear relationship with a slope of 2. Measurements of the fundamental, second, and third harmonics versus LVL ADJ voltage in Fig. 4.2 show that the relationship is in fact nonlinear. Another interesting property of the PA is the change that occurs in the second

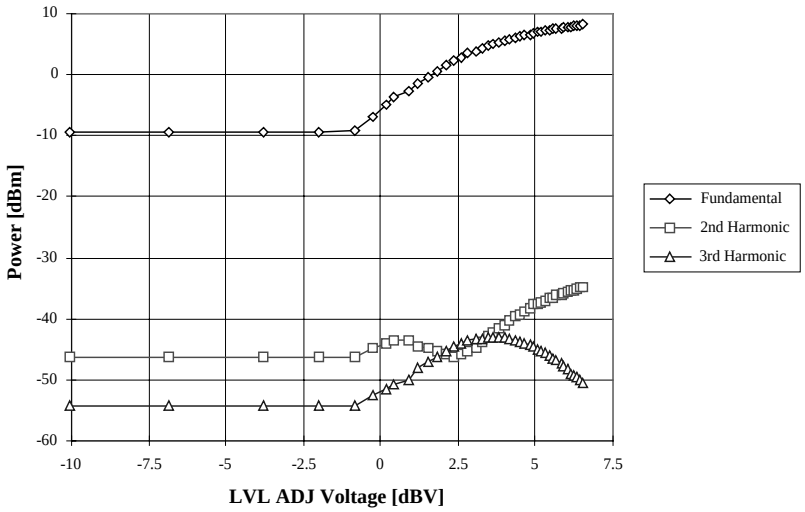


Figure 4.2. Harmonic content of the output signal vs. LVL ADJ voltage

and third harmonic output power levels as the LVL ADJ voltage is increased. Under purely linear conditions, the harmonics produced by the oscillator should increase with the LVL ADJ voltage in the same manner. The trend for the second and third harmonics to seemingly vary differently from each other and the fundamental suggests one or more nonlinear mechanisms at play. First of all, the balanced nature of the VCO suggests that the second harmonic should not be present if the VCO is connected to the PA in a balanced fashion. The presence of the second harmonic raises the question of whether it generated due to a single-ended connection between the PA and the VCO or it is the result of nonlinearity in the PA. Referring to Fig. 4.2, for LVL ADJ voltage greater than approximately 1.5 V, the second harmonic power level increases in the same fashion as the fundamental. This trend indicates that the dominant source of the second harmonic is originating in the VCO due to a single-ended connection. Additionally, as the power level is increased, it is possible the loading presented by the buffer amplifier affects the balance of the balanced oscillator itself due to asymmetric loading. Further support for this is indicated by Fig. 4.3 where the open loop frequency of the VCO is shown to be a function of the applied LVL ADJ voltage. This is representative of an effect known as

"load pulling" in oscillators where a change in the output load impedance of the oscillator results in a shift in the frequency of oscillation [18]. This creates a minor concern that simultaneous modulation of the amplitude and the frequency or sudden shifts in the LVL ADJ voltage many result in an undesired distortion of the frequency modulation.

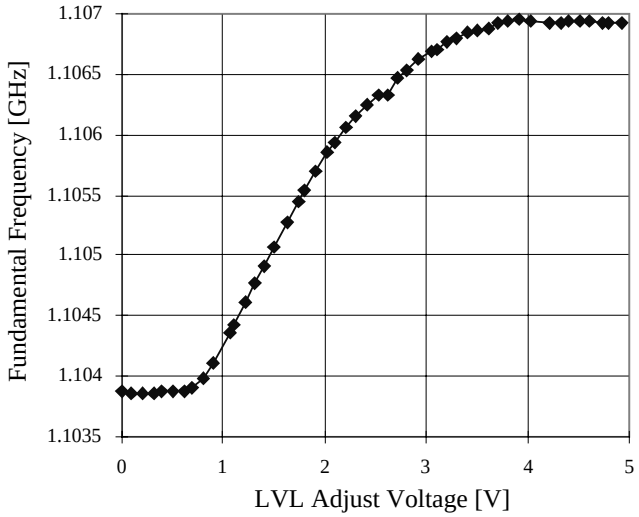


Figure 4.3. Open loop VCO frequency vs. LVL ADJ voltage.

There is still evidence that a nonlinearity is also at play in the PA in the form of the behavior of the third harmonic measured after the filter which increases steadily, and then falls rapidly as the fundamental output power increases beyond +5 dBm. The trend for the falling third harmonic may be another result of the load pulling effect on the oscillator, which is supported by simulation. Further support for the presence of the nonlinearity is provided by the change in the slope of the third harmonic output power at approximately the same fundamental output power that the second harmonic begins a decline. Thus, it can be said that there is a nonlinearity present in the PA, though the nature of the nonlinearity is difficult to determine.

The issues addressed here indicate that the AM function of the chip should be restricted to ASK where the nonlinearity of the control range will not significantly affect the transmitted signal. The perturbation of the VCO frequency of oscillation illustrated in Fig. 4.3 suggests a sudden change in the LVL ADJ pin voltage will cause the PLL to undergo a transient step response due to the potential pulling of the oscillator frequency.

For this reason, it is doubtful that a dual AM/FM modulation scheme would be practical due to the effects discussed here.

4.2 PLL Frequency Source

The PLL frequency source generates the output frequency of the transmitter with the frequency stability associated with the quartz-crystal reference. It is the phase-locking mechanism employed in the source which allows the VCO to be synchronized with the lower frequency quartz crystal reference oscillator. Because the modulation is applied to the VCO, the instantaneous output frequency changes with the modulation. Over the long term, the frequency remains stable about the nominal value that would occur in the absence of modulation. A detailed description of a basic PLL and components is provided in Appendix A to which the reader unfamiliar with phase-locked loops is directed. In this section, only a brief overview of the PLL frequency source will be provided.

The PLL is a special form of control loop, where the control variables are the phase and frequency of the VCO. In control terminology, the VCO is the plant to be controlled by the reference oscillator phase and frequency command input. The uniqueness of the PLL is that the physical output of the VCO and the reference oscillator are sinusoidal voltage waveforms whose phase and frequency are compared in the phase detector, which is an inherently nonlinear device. The nonlinearity of the phase detector is the mechanism by which the phase difference between the sinusoidal voltage waveform input is made proportional to the output voltage of the phase detector. For the classic sinusoidal phase detector, which is a simple multiplier, the low-pass filtered output voltage is a sinusoidal function of the phase difference. Since the sine function is approximately equal to its argument for values of the argument much less than one radian, this represents the linear range of operation for the phase detector. Thus, over this interval, the PLL can be analyzed as a linear control system. Outside this range, the behavior of the phase detector is no longer linearly related to the phase difference and other techniques must be used to analyze its behavior. Other phase detectors commonly in use offer an increased phase difference range over which the output voltage is linearly

related to the input phase difference. As will be shown, even these phase detectors have a region of operation over which the operation is nonlinear. The nonlinear operation is most pronounced when the PLL is in the process of acquisition, where the initially unsynchronized VCO and reference oscillator become synchronized via the nonlinear mechanism of the phase detector.

4.2.1. Acquisition Behavior

Acquisition is the nonlinear process by which the initially unsynchronized reference oscillator and VCO become synchronized. Acquisition may be caused by a transient step of significant size to cause the VCO become unsynchronized with respect to the reference oscillator. It also takes place after the initial power-on transient since the VCO and reference oscillator will begin their oscillations at different frequencies, making it the job of the PLL to synchronize the VCO to the reference oscillator. Whatever the reason for the loop to be out of lock, acquisition will cause the VCO output frequency to perform a nonlinear sweep across the VCO tuning range until the loop finally locks. If the transmitter were enabled while this behavior occurs, the transmitted signal would interfere with other devices using the band as well as create the potential for the receiver to misinterpret the acquisition behavior as an incoming data sequence. The RF2905 includes provisions for a lock-detection circuit which may be used to control the transmitter output. Since the transceiver has separate reference oscillators for transmit and receive, the acquisition phenomenon can affect the receiver as well. In this case, the receiver MUTE control should be set such that the data output is disabled while the PLL is acquiring lock. For some applications, it may be necessary to reduce the acquisition time as much as possible. An approximation for the PLL acquisition time is required to determine the PLL parameters which must be changed to minimize the acquisition time. The operation of the phase detector and filter are the key to developing this expression.

The phase detector in the RF2905 is a phase-frequency detector with a tristate charge pump output. This type of phase detector provides several advantages over a classic phase detector in both increased linear range of operation and acquisition performance. This increase is primarily due to the relationship between the input phase error and the

average output current of the phase detector as illustrated in Fig. 4.4. Of primary concern here, the acquisition performance enhancement results from the behavior of the output to

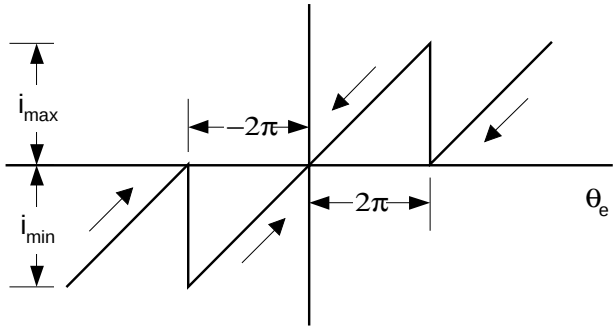


Figure 4.4. Phase-Frequency detector average output current vs. phase error characteristic.

be biased either positively or negatively depending on whether the reference oscillator frequency is greater or less than the VCO frequency (when the magnitude of the phase error is greater than 2π). The relationship illustrated in Fig. 4.4 is not always clear and can also be shown by opening the PLL and observing the steady state output of the phase detector given a frequency difference between the reference oscillator and the VCO. Limiting the input voltages to create 50 % duty cycle square waves with leading edge detection, the time domain inputs and output of the phase detector are presented in Fig. 4.5. It is important to note that the initial phase error between the input signals has

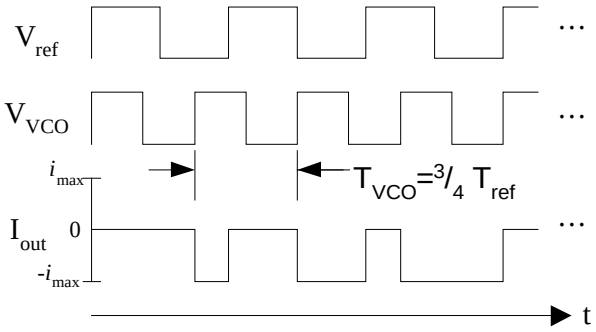


Figure 4.5. Time domain phase detector output with frequency difference between input signals.

been set to zero. From Fig. 4.5, it can be observed that the repetition frequency of the output is f_{ref} - f_{VCO}, and since f_{ref} is less than f_{VCO} the output is always switching between the high impedance state ($I_{out} = 0$) and the current sink state ($I_{out} = -i_{max}$). This behavior causes the long-term average of the output of the phase-frequency detector to be

approximately one-half the value of $-i_{max}$[1]. The additional DC offset decreases the acquisition time since the loop filter integrates the DC offset until the frequency difference between the reference oscillator and the VCO is within the range of linear operation. Integrating the DC offset component, the time required for an initial frequency difference Ω_o at the phase detector to be reduced to the PLL bandwidth ($2\zeta\omega_n$) is given by

$$t_{acq} = \frac{\tau_1}{\pi K_d K_o}\left(|\Omega_0| - 2\zeta\omega_n\right) \tag{4.1}$$

where K_o denotes the VCO tuning sensitivity, τ_1 denotes the pole of the first order PLL loop filter, ζ is the dampening ratio and ω_n is the natural frequency of the second order PLL closed loop system. This equation does not account for the other dynamics which are the significant contributors to the acquisition process in a PLL using a sinusoidal phase detector and that it only applies to loops using the loop filter transfer function comprised of an integrator and lead correction network. The other dynamic effects investigated by Viterbi involve the use of a graphical solution technique referred to as the phase plane approach [19] and may provide a minor correction to (4.1) for the phase-frequency detector.

4.2.2. Influence of PLL Dynamics on FSK Modulation

There are two aspects of the PLL transient response that have direct implications on successful FSK data transmission. The first is ensuring that the peak frequency deviation of the data is small enough to prevent the phase detector from exceeding its linear range of operation. This requirement is usually equivalent to ensuring that the peak frequency deviation at the phase detector is less than the PLL bandwidth. The maximum peak frequency deviation of the VCO is 200 kHz according to the RF2905 data sheet. The maximum deviation occurring at the phase detector would then be 200 kHz divided by the smallest value of the prescaler division ratio which is 64. The resulting value of 3125 Hz represents the smallest value the PLL bandwidth should be without limiting the peak amplitude of the modulation while using a prescaler division ratio of 64. The manufacturer's evaluation board intended for operation in the 902-928 MHz industrial,

[1] The phase detector gain is defined as $K_d = i_{max} / 2\pi$

scientific, and measurement (ISM) band uses a prescaler value of 128 which makes the lower limit on the PLL bandwidth 1563 Hz.

The second aspect of the PLL dynamics affecting FSK modulation is related to the tracking behavior of the PLL. The RF2905 modulates the instantaneous frequency of the VCO with the signal applied to the MOD IN pin. If the modulation signal is composed of mostly low frequency components compared to the bandwidth of the PLL, the loop begins tracking-out the modulation. Under linear operation, the initial correction

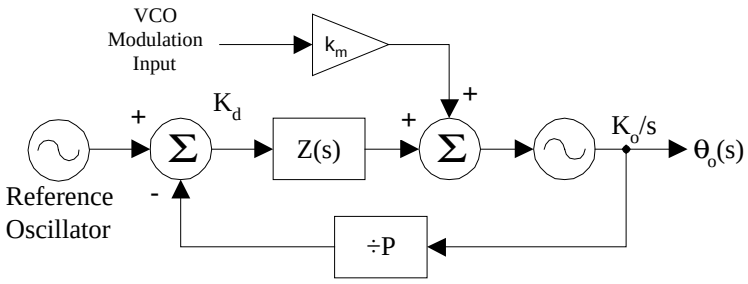


Figure 4.6. PLL with direct modulation of the VCO.

afforded by the loop is dominated an exponential function of the product of the dampening ratio ζ, the natural frequency ω_n, and the time following the step. If the period for which the MOD IN pin is held fixed is small as compared to $\zeta\,\omega_n$, the distortion caused by the tracking mechanism of the loop is small. As the period approaches $\zeta\,\omega_n$, the step response of the loop becomes more pronounced. Eventually, the period of the step becomes so long that the data is corrected out by the loop entirely, except for a rising edge aspect (resulting from the delay between the time the modulation changes the instantaneous frequency of the VCO and the time required for the loop to track). Since the bandwidth of the PLL is $2\zeta\,\omega_n$, the input level must change at a rate much greater than twice the bandwidth of the PLL. This result helps explain why the manufacturer suggests minimum data rates on the order of five to ten times the PLL bandwidth for satisfactory performance.

4.3 Extending the Data Limitations

Due to the correcting nature of the PLL described above in Sec. 4.2.2, there is a lower limit on the modulation frequency that can be applied to the VCO modulation input. In

applications where the RF29X5 transceivers are meant to provide a “wireless wire” connection between two serial data systems, the sustained data rates increase the probability that long runs of either high or low level data bits will cause the modulation frequency to drop below the lower limit created by the PLL bandwidth. In order to overcome this limitation, several methods of modifying the transmitter and receiver structure have been devised and will be discussed.

4.3.1 Manchester Encoding

Manchester encoding is the manufacturer’s suggested method for alleviating the problems associated with very low frequency data. Manchester encoding replaces a single high or low level bit with two pulses; the width of each is one half the original pulse width. The magnitude of the two pulses is the same, but the voltage levels are complementary such that one pulse is positive and the other is negative. It is the order of the two pulses that distinguishes the difference between a logic high or low having been transmitted. The effect of Manchester encoding is to double the frequency of the modulation; thus it almost removes the possibility that the loop will have sufficient time to react to the modulation. Additionally, to successfully decode the data, the encoder and decoder must be synchronized. This method is also relatively expensive if implemented with commercially available Manchester encoder/decoder chips. If implemented using a microcontroller, most of the controller’s instruction cycles are spent converting data into Manchester encoding which becomes increasingly inefficient as the frequency of the data increases.

4.3.2 Digital Data Modulation

An economical alternative to Manchester encoding is to digitally modulate the data with a locally generated 50 % duty cycle square wave as illustrated in Fig. 4.7. The data and the square wave are applied to an AND gate (74HC08 or equivalent) or NAND gate (74HC00 or equivalent) and the output is then applied to the modulation input. Selecting a local square wave frequency higher than the bandwidth of the PLL prevents the loop from tracking out the modulation. After demodulation by the quadrature detector of the receiver, the output of the DATA OUT pin is applied to the input of a retriggerable,

monostable multivibrator (74HC122, or 74HC123). This logic circuit uses an external RC network to generate TTL/CMOS compatible pulses whose width is a function of the

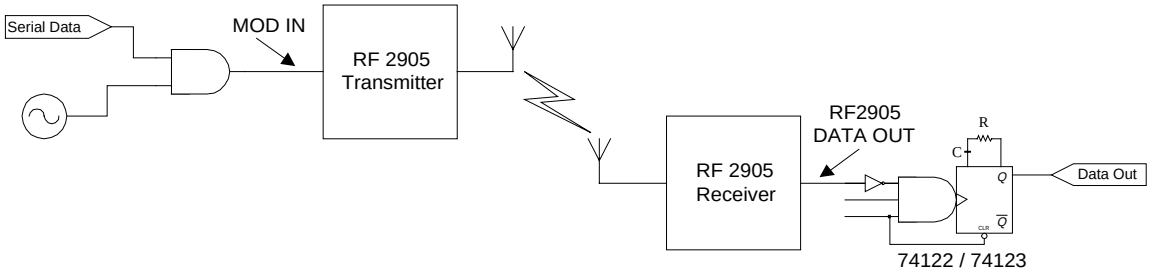


Figure 4.7. Illustration of digital data modulation.

time constant of the RC network, when a rising edge at one of the inputs of the monostable multivibrator occurs. The multivibrator can be "retriggered" by another rising edge occurring before the initial output pulse has ended. If the multivibrator is retriggered once, the output pulse width is twice that which would otherwise occur. Thus, setting the RC time constant such that the pulse width at the receiver is slightly more than period of the transmitter's local square wave causes the 50% duty cycle square wave to be removed from the DATA OUT signal. For example, assuming a logic level high were applied to the transmitter AND gate indefinitely, the DATA OUT signal would consist of only the 50 % duty cycle square wave. Since the RC network time constant is slightly larger than the period of the square wave, the multivibrator continuously retriggers holding the output logic level high. This scheme allows data rates between DC and the transmitter clock frequency to be transmitted without being affected by the PLL tracking mechanism. Besides the economic advantage, this method does not require any synchronization with the transmitter clock as is the case with Manchester coding(which is required to determine the order of the two Manchester pulses). Also because the 74HC123 has two parts in a package, it allows the designer to implement time-out circuits which would power down the receiver, or transmitter, depending in battery applications.

4.3.3 Reference Oscillator Pulling

For low frequency data, rather than circumventing the PLL transient behavior, pulling the frequency of the reference oscillator may prove a better solution. By introducing a

varactor diode into the reference oscillator reactive network, the reference oscillator frequency is made voltage variable over a very small range. Provided the PLL bandwidth is set wide enough, it will track the modulation causing the output to shift an amount corresponding to the prescaler division ratio multiplied by the frequency shift of the reference oscillator. There is an upper frequency limit associated with this method because the loop responds less and less to modulations that exceed the loop bandwidth as frequency increases. Some care must be exercised in applying this method because it is possible to add enough capacitance to cause oscillations to cease, additional noise may be added, or the long-term stability may suffer. Additionally, the difference in frequency between the nominal value of the reference oscillator and its maximum value when pulled must not exceed the PLL bandwidth in order to prevent the loop from losing lock. For the reader interested in a greater detailed description, this method is treated in more detail in Sec. 5.5.

4.3.4 Dual Modulation: Linear Technique

Linear dual modulation is a means by which the modulation characteristics of the loop might be made wideband. Because pulling the reference oscillator is inherently a low frequency modulation method, and directly modulating the VCO is a high frequency modulation method, combining the two methods into a single method potentially allows a wideband modulation format. The modulation signal is applied to the loop through the normal direct VCO modulation scheme and also a reference oscillator pull scheme simultaneously (see Fig. 4.8). The dependence of the FM deviation on the modulation signal v_m is given by

$$\Delta\omega_o = \frac{v_m A_2 k_r F(s) K_o K_d P + v_m A_1 k_v P s}{F(s) K_o K_d + P s} \tag{4.2}$$

where k_r is the reference oscillator pulling sensitivity, k_v is the VCO FM modulation sensitivity, F(s) is the PLL filter transfer function, K_o is the VCO tuning sensitivity, K_d is the phase detector gain, and P is prescaler division ratio. Assuming linear modulation, Eq. 4.2 reduces to simply v_m if A_2 / A_1 is equal to $k_v / (P \bullet k_r)$. Thus, in order to obtain truly wideband modulation, the phase shift versus frequency for the amplifiers must be exactly matched as well as the gains precisely set. An additional concern is that pulling

the reference oscillator with the low frequency spectral content of the data, the long term frequency stability of the PLL transmitter will suffer because it will vary with the running average of the data (as indicated in Sec. 4.3.3).

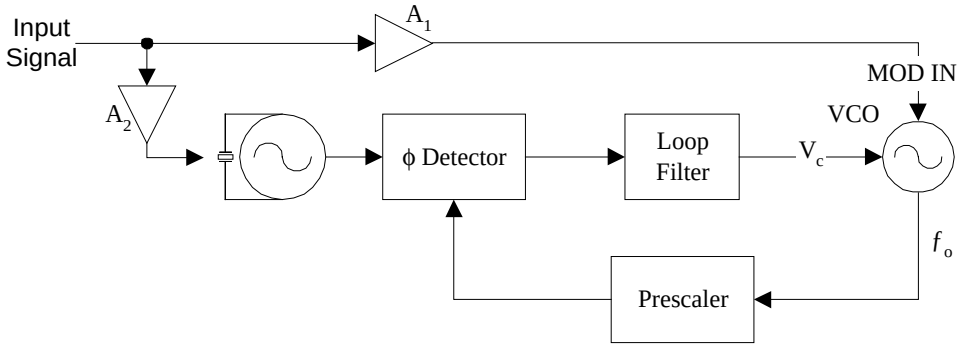


Figure 4.8. Analog dual modulation technique.

4.3.5 Dual Modulation: Digital Technique

Data is constantly checked to determine if a period of consecutive high or low logic levels has occurred that would cause the PLL to begin the acquisition process. For a sufficiently long string of consecutive highs or lows, the data is applied to a reference oscillator pull scheme, otherwise it is applied to the modulation input pin on the VCO of the RF2905. One possible implementation of this scheme is illustrated in Fig. 4.9. The data is buffered into a series shift register while at the same time applied to the clock input of a CMOS counter. The local clock controls the number of bits counted by the

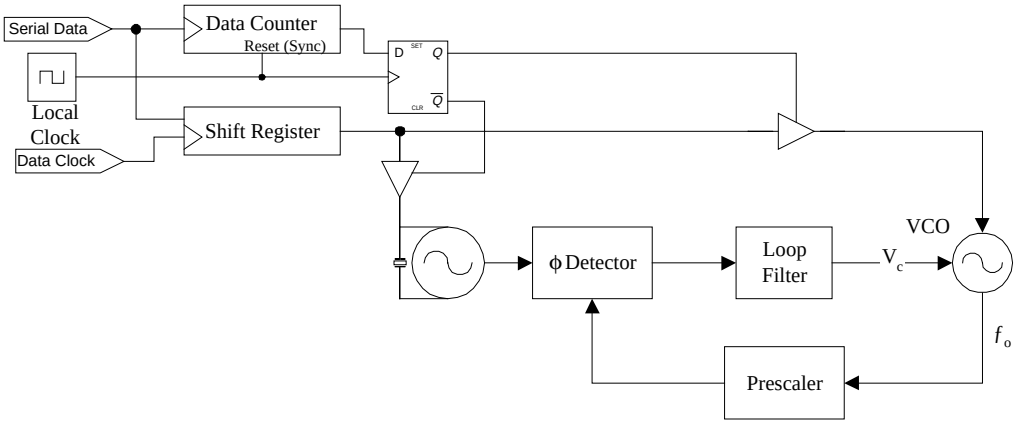


Figure 4.9. Digital wideband modulation conceptualization.

data counter . After a predetermined interval, the value of the data counter is checked. If the value is below the minimum number of transitions required, the data within the shift

register is applied to the reference oscillator pull scheme by shifting it out of the shift register. Variations on this scheme for the sake of economy or higher scale integration may be warranted. As an added feature of this technique, the value of the data clock can be appended to the end of the data to act as a check sum for error checking to improve the reliability of the link. This extra feature is not included in Fig. 4.9. Instead of operating on a bit by bit basis as with the linear technique, the digital technique works on a discrete set of data bits inherently introducing a delay element in the transmission.

4.3.6 Multilevel FSK

In transitioning from direct modulation of either the VCO or reference oscillator to a multilevel FSK modulation, the designer makes the trade off between required RF bandwidth and signal to noise ratio. Rather than using one frequency to represent each of the two possible data bit levels, several frequencies are used to represent multiple bits of data. This implies that the modulation rate is no longer equal to the serial data rate, but instead, equal to the serial data rate divided by the result of the logarithm "base two" of the number of frequencies used. This extends the upper limit on the data rate that can be used and also implies that the RF bandwidth required to transmit a particular serial data rate is reduced as compared to direct modulation. This bandwidth reduction can be shown using Carson's rule which approximates the RF bandwidth occupied by an FM signal as

$$B = 2(\Delta f + f_m) \tag{4.3}$$

The modulation frequency, f_m, in Eq. 4.3 is given by

$$f_m = \frac{R}{\log_2(M)} \tag{4.4}$$

where M represents the number of discrete frequencies used to transmit the data and R represents the original data rate. Denoting the difference between the highest and lowest frequencies in the multilevel FSK scheme as Δf, the occupied bandwidth of the multilevel FSK scheme differs from direct binary FSK using the same peak deviation by

$$\Delta B = 2R\left(1 - \frac{1}{\log_2(M)}\right) \tag{4.5}$$

This result implies the designer could use a slightly smaller IF bandwidth to decrease the noise bandwidth of the receiver, though how much less depends directly upon R. It can be shown that for ever increasing values of M, the required IF bandwidth approaches $2\Delta f$. This implies that the main advantages in reducing the RF bandwidth are mostly in the form of opening up space in the ISM band for more channels for simultaneous use.

As mentioned before, the increase in the number of frequencies used to transmit comes at the price of a higher signal-to-noise ratio (SNR) to achieve the same symbol error rate. Due to the capture effect, there is not a direct correspondence between the carrier to noise ratio presented to the quadrature detector and the SNR appearing at the output of the quadrature detector. Taking this into account, a maximum increase in the bit error can be formulated by holding the ratio of E_b / N_0 constant (where E_b is the energy per bit calculated as the carrier power in watts multiplied by the bit period, $C \bullet T_b$, and N_0 is the thermal noise density kT) and comparing the effect of changing the number of the frequencies used for the noncoherent FSK modulation. In general, M-ary noncoherent-FSK reception can achieve an upper bound [20] of

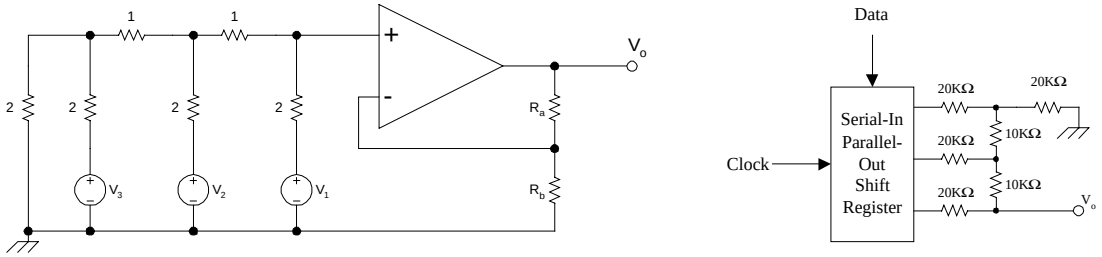
$$P_e \leq \frac{M-1}{2} e^{-\left(\frac{E_b}{2N_0}\right)} \tag{4.6}$$

for a given value of E_b / N_0. Thus, the penalty in error rate due to increasing the number of frequencies used for modulation from 2 to M is

$$P_e \leq \frac{M-2}{2} e^{-\left(\frac{E_b}{2N_0}\right)} \tag{4.7}$$

Although the probability of error increases linearly with the number of frequencies used in the modulation process, the exponential relationship between the bit energy noise density ratio and the probability of error suggests that the required carrier to noise ratio of the receiver will not be drastically affected. The probability of error above is the symbol error, which is the error made when the wrong frequency is chosen as the one that was transmitted. This can be related to the bit error probability on average, but it depends greatly on the assignment of bits to frequencies that are spectrally adjacent to each other.

Implementing multilevel FSK economically is the key to the method. Without an economical implementation, the method is not practical and the advantages are purely hypothetical. In order to realize a multilevel FSK scheme, a digital to analog conversion must take place. A commercially available digital to analog (D/A) converter could be used; though it would significantly raise the cost of the radio. Another way of creating a D/A converter is by using a resistive ladder circuit and an OP AMP. The OP AMP becomes unnecessary provided resistor values greater than 5 kΩ are used and the same peak deviation value can be tolerated. The schematic diagram of the D/A circuit with the OP AMP, normalized resistor values, and implemented with a shift register and typical resistor values appear in Fig. 4.10. Any resolution D/A converter can be realized in this fashion with the frequency limits being controlled by the speed of the logic family in question. The trade off in performance is the accuracy of the D/A process. An integrated D/A converter is able to keep all the resistor values matched in their proper ratios within very tight tolerances whereas the discrete version may suffer from component tolerances. To some degree this is alleviated by using single in-line package (SIP) resistor networks which usually achieve a closer match between components and reduce layout area. Since a shift register or buffer of some sort is required to buffer the serial data before applying it to the modulator, the outputs could be used instead of an OP AMP, provided the



a. **b.**

Figure 4.10 D/A converter circuit typologies for multilevel FSK implementations.

modulation input being driven by the D/A is a voltage mode input. Depending on the D/A, temperature compensation may be provided in the form of a closed loop control which is not present in the circuit of Fig. 4.10. Additionally, some gating may be required to change the level of the modulator only when the register is full and not while it is loading. To provide some error checking, the value of the shift register may be

transmitted when it is only half full such that half the data is from the previous time and one half is new creating a simple redundancy check to be performed at the receiver. Another simple means of error checking is inserting an 74HC280 parity generator/checker bit. Since the RF29X5 units cannot transmit and receive simultaneously, and the 74HC280 serves as both a generator and tester, a single parity chip in each transceiver could be used for both transmit and receive at a cost in volume below 50 cents each. It would also provide the advantage of separating the frequencies used as well. Because only frequencies corresponding to the even values or odd values of the D/A would be used.

In order to recover the modulated signal, the receiver must be modified with an analog-to-digital (A/D) converter and potentially an additional amplifier. These modifications may offset the cost saved in the transmitter modifications because A/D converters are more complex than D/A converters, making it cost prohibitive to make one out of discrete components. Using A/D converters also raises concerns over sampling frequency and symbol synchronization. To some degree, the higher cost associated with this technique can be justified since the complexity and capabilities are enhanced as compared to the standard direct data modulation formats.

5. Oscillators of the RF2905

5.0 Chapter Overview

The most critical components of the transceiver system are the oscillators of the RF2905. The reference oscillator and the voltage controlled oscillator (VCO) control the output spectrum of the PLL both inside and outside the PLL bandwidth. An understanding of these oscillators is necessary to successfully implement many of the solutions to the PLL bandwidth distortion problems without adversely affecting the performance of the transmitter. Starting with an analysis of the reference oscillator, modifications necessary to use the same analysis approach for the VCO will be discussed. Integrated into this discussion is the introduction and design of a non-saturating version of the VCO oscillator and the relationship between the non-saturating version and the present VCO. Following this discussion, methods and considerations for tuning the reference oscillator and VCO topologies previosly presented. Since one of the primary considerations in oscillator tuning and VCO applications is the effect on the noise present in the oscillator, the noise behavior of the oscillator is discussed. This discussion first focuses on the Leeson model [16] commonly used in practice and the problems with its inherently linear approach to oscillator noise. The discussion then moves on to present a revised model developed by applying nonlinear analysis techniques.

5.1 Analysis of the Reference Oscillator

The reference oscillator of the RF2905 is a grounded collector Colpitts oscillator intended to employ a quartz crystal as the inductive component of its resonant network. The Colpitts oscillator AC equivalent circuit can be represented by the generalized, three-node circuit depicted in Fig. 5.1. The designation as to which node is at ground potential has been omitted intentionally because the node voltage and current relations hold irrespective of which node is grounded. Approaching the oscillator in this manner, a single equation can be developed which is applicable to all three basic typologies of the reference oscillator (common-base, common-emitter, common-collector). Additionally,

these same equations can be applied to the Hartley oscillator typologies as long as the appropriate substitutions are made involving the capacitors and inductors.

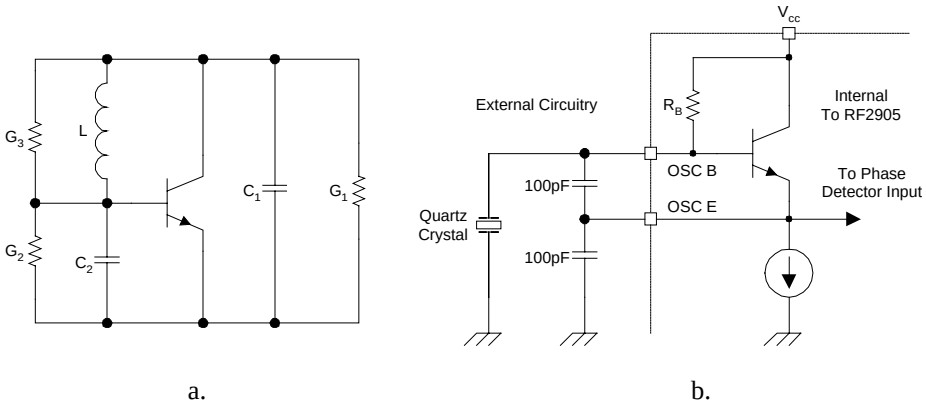


Figure 5.1. General three node Colpitts oscillator circuit(a) and RF2905 reference oscillator(b).

The circuit elements of the reference oscillator AC equivalent circuit must first be matched to their equivalent representations in Fig. 5.1. Starting with the reactive components, the two external 100 pF capacitors of the reference oscillator correspond to C_1 and C_2 of the general circuit while the parallel mode quartz crystal corresponds to the inductor L. The series combination of the two capacitors is equal to the total capacitance required for parallel resonance to occur at the specified frequency for the quartz crystal. The characterization of the conductances provides more of challenge since there are no external resistors used in the reference oscillator circuit. Referring to the data sheet for a moment, the manufacturer suggests that the emitter is directly connected to a current source. Since this current source is most likely a current mirror, the presence of conductance G_2 seems very unlikely. In order to determine the remaining conductances, measurements of the physical circuit must be made.

Because the RF2905 has the capability of selecting between two reference oscillators, a more complicated bias control system than simply a resistor connected from the power supply to the base and a current mirror connected to the emitter is implied. Measurements of the bias voltage on the pin shared by the two emitters and current source show that the emitter voltage is roughly constant at 3.83 V independent of which oscillator is selected. The bias voltage on each of the pins connected to a transistor base is 4.54 V and 3.5 V when the device is selected and deselected respectively. This

indicates that there is an internal circuit connected to the two bases for the purpose of controlling the bias voltage. Using a digital multimeter (DMM), the resistance between the base of the transistor and the power supply connection was measured to be 83 kΩ. In

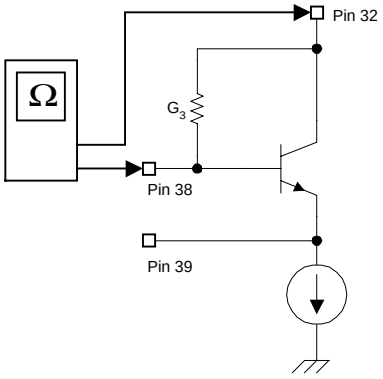


Figure 5.2. Measurement of the bias resistor of the RF2905.

order to ensure that the value measured represented a bias resistor and not the forward conductance of the base-collector junction, the polarity of the meter was reversed and the measurement taken again (Fig. 5.2). The DMM was then used to measure the resistance between from the base of the transistor to ground which turned out to be larger than the maximum resistance the meter could measure indicating the possibility that the bases

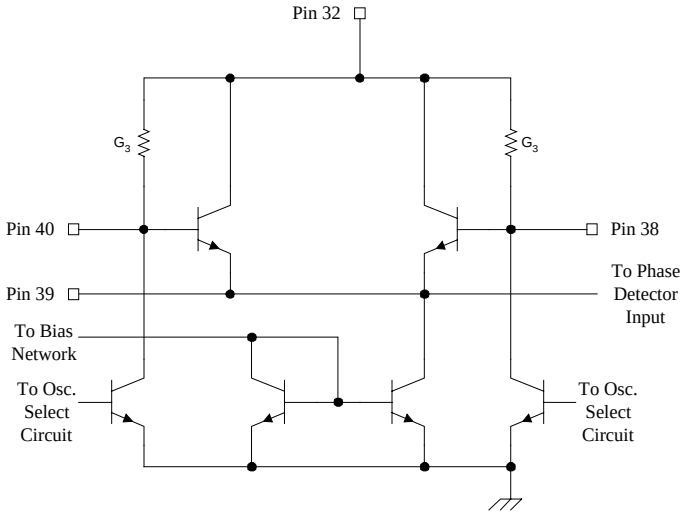


Figure 5.3. Most likely reference oscillator bias interconnections.

were connected to another transistor's collector as in the case of the current source. The working model of the internal circuit is presented in Fig. 5.3. This diagram can be used

as a basis for determining the values of the remaining two conductances. It can safely be assumed that for the selected transistor oscillator, the conductance connected across the base-emitter junction is approximately zero, while the conductance connected across the base-collector junction is approximately 12 μS $(83\ k\Omega)^{-1}$. The remaining conductance, G_1, is the result of the loading on the oscillator by the phase detector input. Since the input to the phase detector is most likely a voltage driven logic gate, it is reasonable to assume the input impedance is on the order of 500 Ω.

With the modeling of the linear components completed, the modeling of the transistor itself must now be discussed. The transistor provides both the gain and amplitude limiting mechanism required to create a stable sinusoidal oscillator. The nonlinear characteristic of the transistor stabilizes the output amplitude by causing the oscillator signal amplitude to be proportional to the DC current of the transistor. Since the DC current is maintained constant by the current mirror bias, the output amplitude remains constant as well. The nonlinearity of the transistor can be characterized using the Ebers-Moll model for a bipolar transistor, illustrated in Fig. 5.4 [21], along with some simplifying assumptions. Under non-saturating conditions, the diode generating the I_{CN} current is always reverse biased and generates only a leakage current. The circuit of Fig. 5.3 suggests that it is very unlikely for saturation to occur allowing the base-collector diode an associated dependent current source between the base and emitter to omitted. This simplification reduces the Ebers-Moll model to a single diode and a linear dependent current source. Before proceeding, it should be noted that the Ebers-Moll model does not account for the nonlinear junction capacitance that exists as part of the base-emitter and base-collector junctions. These nonlinear capacitances will be neglected since the base-collector capacitance is minimized due to non-saturating conditions while the base-emitter capacitance will be assumed to be a small fraction of the value of the circuit capacitance in parallel with the junction (in this case 100 pF).

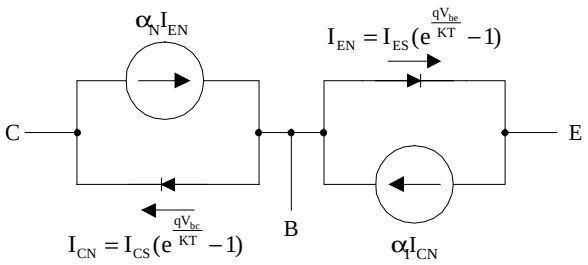


Figure 5.4. Ebers-Moll model of an NPN transistor.

Because the current source is linearly dependent on the emitter current, the only nonlinearity in the oscillator is the diode. The relationship between the base-emitter junction voltage and the emitter current is given by

$$I_e = I_{ES}\left(e^{\frac{qV_{be}}{kT}} - 1\right) \tag{5.1}$$

where I_{ES} can be assumed to be on the order of $2 \bullet 10^{-16}$ A and $^{kT}/_{q}$ can be assumed to be approximately 26 mV for a room temperature junction. For values of V_{be} increasingly greater than 26 mV, Eq. 5.1 is approximated by neglecting the term in unity. Because Eq. 5.1 is a nonlinear equation, the relation between V_{be} and I_e must be analyzed in the time domain using Fourier series techniques. Letting V_{be} to be given by,

$$V_{be} = V_{DC} + V_1 \cos\omega t \tag{5.2}$$

permits I_e to be formulated as a Fourier series with a 0^{th} order term corresponding to the DC emitter current under excitation, and a sum of harmonics of the fundamental frequency ω. The resulting Fourier series for the exponential nonlinear characteristic is given by,

$$I_e(t) = I_{dc}\left[1 + \sum_{n=1}^{\infty} \frac{2I_n(x)}{I_0(x)} \cos(n\omega t)\right] \tag{5.3}$$

where x is V_1 / V_{th}, and $I_0(x)$ and $I_n(x)$ represent the 0^{th} and n^{th} orders of the modified Bessel functions of argument x [17]. With the aid of Eq. 5.3, it is now possible to calculate the input conductance of the transistor as well as the amplitude of the emitter and collector current components at DC and all of the harmonics of the sinusoidal excitation. The input conductance of the transistor at the fundamental frequency of excitation is calculated by dividing the fundamental component of the current by the fundamental component of the excitation voltage. The diode in the Ebers-Moll model

can now be replaced by this nonlinear conductance which is only valid under the same DC current and applied fundamental component drive level. In performing this substitution, the Ebers-Moll model has been converted to an equivalent large signal alpha model of the transistor.

Substituting the large signal alpha model for the fundamental frequency components into the general three-node circuit and rearranging its appearance slightly, the resulting equivalent circuit of the oscillator is depicted in Fig. 5.5. Due to the high Q nature of the oscillator circuit, the reactances of capacitors at the fundamental frequency of oscillation should be greater than the resistances in parallel with them. The ratio between V_{be} and the voltage developed across G_3 is primarily controlled by the reactances of the

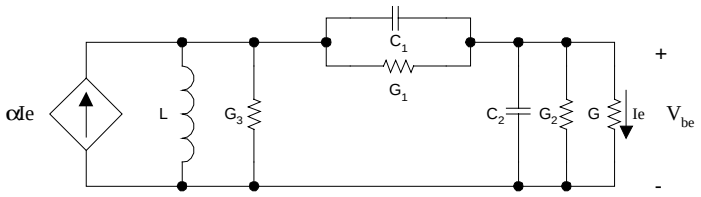


Figure 5.5. Equivalent circuit of the Colpitts oscillator.

capacitors. The tapped capacitor arrangement of Fig. 5.5 can be replaced with an ideal transformer with turns ratio n and a single capacitor across the primary side (Fig. 5.6a). The value of the turns ratio and shunt capacitance are given by,

$$n = \frac{C_1 + C_2}{C_1} \qquad C_T = \frac{C_1 C_2}{C_1 + C_2} \qquad (5.4\ a\ \&\ b)$$

The base-emitter nonlinear conductance, G_2, and G_1 can be moved to the other side of the transformer by changing the value of their respective impedances such that the power dissipated in each of the conductances remains the same as before. (Fig. 5.6b) After performing this last step, the loaded Q of the oscillator's resonator which is necessary for calculating the noise performance of the oscillator is easily calculated.

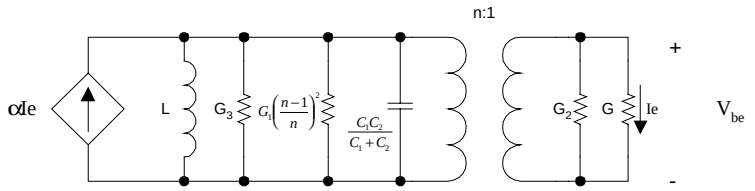


Figure 5.6a. Equivalent circuit using ideal transformer.

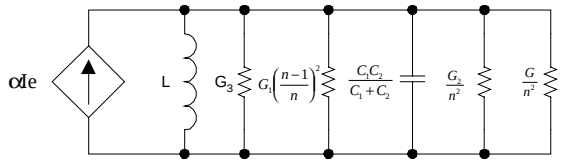


Figure 5.6b. Equivalent parallel resonant circuit.

For stable oscillation to take place, the linear circuit must be configured properly to ensure that the large signal loop gain is unity. Under stable oscillation, the fundamental components of V_{be} and I_e are fixed and define the nonlinear conductance G (I_e / V_{be}). The emitter current can be expressed in terms of the base-emitter voltage and nonlinear conductance as G • V_{be}. The collector current is then simply the result of the emitter current multiplied by the alpha current factor given by α • G • V_{be}. All of the conductances in Fig. 5.6b can be combined into a single conductance, G_T. The voltage across G_3 is then the value of the collector fundamental current divided by the total conductance. This voltage corresponds to the voltage present on the primary side of the transformer in Fig. 5.6a. The voltage across the primary side of the transformer divided by the turns ratio, n, is equal to the voltage across the secondary side. The voltage on the secondary side of the transformer, given by α • G • V_{be} / [G_T • n], must be equal to the original value of V_{be} to ensure unity loop gain. By substituting the expressions for the conductances that G_T is composed of, and gathering all of the terms in G on one side of the equation, the oscillator loop gain requirement is expressed as,

$$G\frac{\alpha\, n-1}{n^2} = G_3 + \frac{G_2}{n^2} + G_1\left(\frac{n-1}{n}\right)^2 \qquad (5.5)$$

By relating the oscillator circuit parameters (G_1, G_2, G_3, and n) to the operating point of the device (G), Eq. 5.5 permits the determination of the oscillator fundamental

component of V_{be} provided the DC bias point of the device can be obtained. Since the reference oscillator may potentially share its power supply connection, measuring the DC current at this pin would not guarantee an accurate representation of the bias current. Instead, measurements of the DC voltage drop across the 83 kΩ bias resistor were made to indicate that a 4.5 μA current is present in the resistor. Assuming the β factor of the transistor is on the order of 100, the value of I_{dc} is approximately 450 μA. Assuming a phase detector conductance (G_1) of 2 mS, voltage division ratio (n) of 2, and bias resistor conductance (G_3) of 12 μS, the right-hand side of Eq. 5.5 reduces to 512 μS. The value of α corresponding to a β factor of 100 is 0.990. Solving for the value of the large signal conductance of the transistor base-emitter junction, G is determined to be 2.13 mS. Through iteration, the value of the drive level normalized to $^{kT}/_{q}$ that results in a close match for this value of G is 15.7. This value of x corresponds to a base-emitter fundamental voltage component of 408 mV.

Subsequent measurements using an oscilloscope with fast Fourier transform capabilities have indicated that the fundamental component of the base-emitter voltage is 530 mV. Taking into consideration that the value of the phase detector input conductance was not measured but assumed to be 500 Ω, the agreement between the value of the fundamental component predicted by the analysis and that determined by measurement is reasonable. Comparing the fundamental components of the emitter current, an even better correspondence between predicted (0.968 mA) and measured (0.975 mA) is obtained. It should also be noted that the influence of the oscilloscope probe on the oscillator operation has not been accounted for and remains as an additional contribution to the difference between the analysis prediction and the measured value of the fundamental component. Thus, under the circumstances, the nonlinear analysis approach has reasonably predicted the fundamental component of the oscillator emitter current as well as the fundamental component of the base-emitter voltage.

5.2 Nonlinear Characteristic of the Balanced Pair

To investigate the operation of the VCO, the nonlinear characteristic of the balanced pair must be determined. Like the exponential nonlinear characteristic relationship

between the base-emitter voltage and the emitter current of the reference oscillator transistor, the nonlinear characteristic of the differential pair is the means by which the amplitude stability of the oscillator is maintained. Determining the nonlinear characteristic equation for the differential pair seems at first glance, a daunting task; however, by taking advantage of the balanced nature of the differential pair, finding the expression for the collector currents as a function of the applied base emitter voltages becomes a rather simple task. First, it is assumed that the bias network connected to the bases of the differential pair transistors provide a fixed DC voltage, V_{DC}. Two single-ended single tone sinusoidal voltages 180° out of phase with each other are also present across the base emitter junction of the transistors as illustrated in Fig. 5.7. The combination of the DC and sinusoidal voltages excite the DC (I_{DC}) and sinusoidal (*i*)

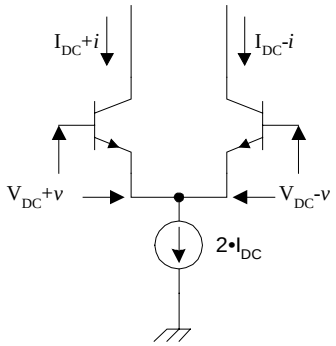


Figure 5.7. Differential pair schematic.

currents present in the collectors. The total current through collector of each of the two transistors can be expressed in the time domain using the Ebers-Moll model equation as,

$$I_C = I_{ES}\alpha\left(e^{\frac{q(V_b - V_e)}{KT}} - 1\right) \tag{5.6}$$

Where I_{ES} is the saturation current of the emitter and α is the alpha factor of the transistor. These currents can also be expressed in terms of DC and AC components as discussed previously, and here named I_{DC} and *i* respectively. For the transistors Q_1 and Q_2 the collectors currents are,

$$I_1 = I_{DC} + i = I_{ES}\alpha\left(e^{\frac{q(V_{b_1} - V_{e_1})}{KT}} - 1\right) \tag{5.7a}$$

$$I_2 = \mathrm{I}_{DC} - i = \mathrm{I}_{ES}\alpha\left(e^{\frac{q(\mathrm{V}_{b_2}-\mathrm{V}_{e_2})}{\mathrm{KT}}} - 1\right) \tag{5.7b}$$

where for most practical circumstances, the exponential term is much greater than unity. By combining the expressions for the base voltages and the expressions for the collector currents, (neglecting the term in unity) the AC component of the collector current can be solved for in terms of the DC component. This is done by first solving the collector current equations for I_{DC} and subsequently for *i*. This results in the expressions,

$$i = \frac{\mathrm{I}_{ES}\alpha}{2}\left(e^{\frac{q(\mathrm{V}_{cc}-\mathrm{V}_e)}{\mathrm{KT}}}\right)\left(e^{\frac{q(v)}{\mathrm{KT}}} - e^{\frac{q(-v)}{\mathrm{KT}}}\right) \tag{5.8a}$$

$$\mathrm{I}_{DC} = \frac{\mathrm{I}_{ES}\alpha}{2}\left(e^{\frac{q(\mathrm{V}_{cc}-\mathrm{V}_e)}{\mathrm{KT}}}\right)\left(e^{\frac{q(v)}{\mathrm{KT}}} + e^{\frac{q(-v)}{\mathrm{KT}}}\right) \tag{5.8b}$$

Now expressing *i* in terms of I_{DC} and some exponential terms, the equation relating the AC component of the base voltage to the AC component of the collector current can be determined as,

$$i = \mathrm{I}_{DC}\frac{\left(e^{\frac{q(v)}{\mathrm{KT}}} - e^{\frac{q(v)}{\mathrm{KT}}}\right)}{\left(e^{\frac{q(v)}{\mathrm{KT}}} + e^{\frac{q(-v)}{\mathrm{KT}}}\right)} \tag{5.9}$$

which is the exponential form of the hyperbolic tangent as expressed as,

$$i = \mathrm{I}_{DC}\tanh\left(\frac{q\,v}{\mathrm{KT}}\right) \tag{5.10}$$

A plot of the hyperbolic tangent function appears in Fig. 5.8. From the plot, it can be observed that an approximately linear region exists for $|x|<1$. Between one and two the

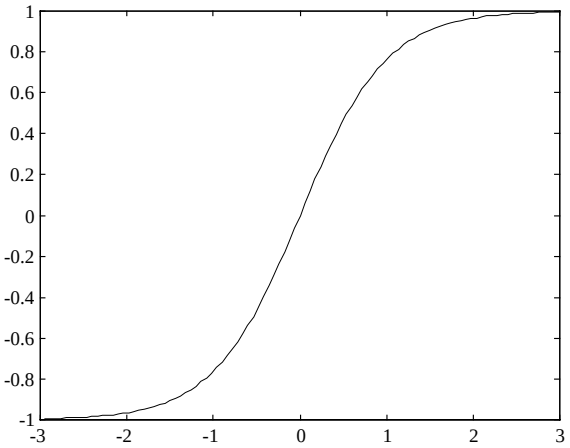


Figure 5.8. Plot of the hyperbolic tangent function.

nonlinearity becomes noticeable, and for values of the argument greater than two, the hyperbolic tangent function in essence saturates, converging to a value of plus or minus one. Because the value of $^{q}/_{KT}$ is approximately 26 mV for a room temperature junction, a voltage source driving the base-emitter junction with only 78 mV (x = 3) will generate an essentially square-wave output which would consist mainly of the fundamental frequency and the odd order frequency harmonics. It is important to note that this limiting process is not due to the actual transistor saturation which involves the nonlinearity introduced by forward biasing the base collector junction. In the above expressions, this effect has not been accounted for and is not the cause for the limiting behavior described above.

Because the characteristic is indeed nonlinear, the Fourier transform cannot be applied directly to the device in this situation.

$$I(j\omega) \neq H(j\omega) \cdot V(j\omega) \tag{5.11}$$

The nonlinearity has the direct implication that Fourier analysis can be applied in an indirect manner to obtain a solution. Defining the AC component of the base-emitter voltage of Q_1 to be a single frequency sinusoid given by

$$v = \mathrm{V}_1 \cos \omega_1 t \tag{5.12}$$

in the time domain, the time domain output current waveform can be calculated using the previously derived nonlinear voltage-to-current characteristic of the differential pair. The Fourier transform of the collector current waveform then provides the needed information

regarding fundamental (first order) current amplitude along with the amplitudes of the harmonic components (higher orders). Using numerical techniques, a plot of the first through fifth order harmonic collector current amplitudes versus base-emitter voltage normalized to 26 mV (the normalized drive level denoted x) appears in Fig. 5.9. The plot indicates that the original prediction concerning the absence of even order harmonic terms in the collector current was correct. It also shows that due to the limiting effect of the hyperbolic tangent nonlinear characteristic, as drive level increases the collector current harmonic components approach a fixed value implying that the input impedance of the differential pair is in fact increasing with applied drive level. This basically provides a limiting effect on the output level, such that variations in the normalized drive level above a drive level of 5 to 10 will not significantly alter the magnitude of the fundamental output current component.

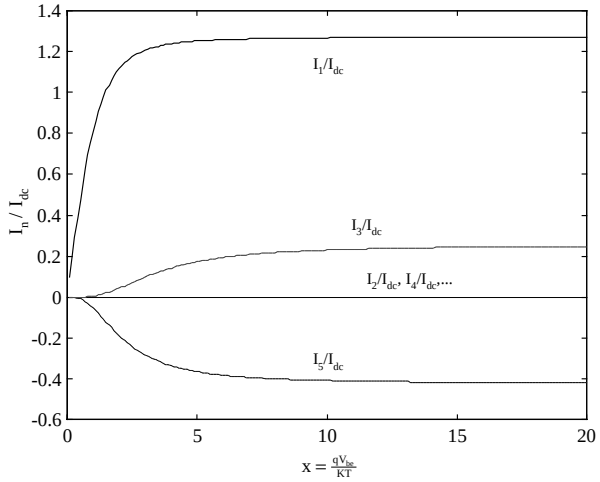


Figure 5.9. First five orders of collector current components vs. drive level[17].

For the purpose of oscillator design, it is useful to develop a model of the differential pair that treats it as an equivalent single transistor. Doing this allows the design equation developed for the Colpitts reference oscillator to be used for the differential pair oscillator as well. This modeling procedure involves finding an expression for the input conductance of the differential port formed by the two transistor bases, and the current amplification factor which relates the voltage applied to differential input port to the collector current of one of the two transistors. Drawing upon the analysis of the reference oscillator, the two transistors can be modeled with the alpha model once again. The

nonlinear conductance of the alpha model will now be designated G_a to differentiate it from the nonlinear conductance in the beta model which will be introduced shortly. Assuming the two transistors are matched, the differential voltage (V_{diff}) applied across the two bases of the transistors is divided equally across the G_α conductances. The AC fundamental collector current is then given by $\alpha\, G_\alpha\, V_{diff} / 2$. The structure to which this result corresponds is still not in a form suitable for use in the Colpitts generic circuit. To obtain a suitable model structure, the Ebers-Moll based models (alpha models) must be replaced with hybrid pi models (beta models). The collector current already calculated in terms of the alpha model parameters can be rewritten in terms of the beta model

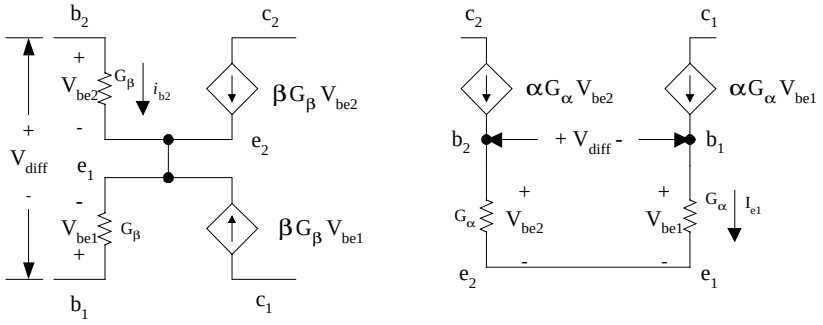


Figure 5.10. Equivalent representations of the differential pair.

parameters by equating the alpha model conductance to $G_\beta\,(\beta + 1)$, which causes the alpha model collector current to be $\alpha\, G_\beta\,(\beta + 1)\, V_{diff} / 2$ which is equivalent to $G_\beta\, \beta\, V_{diff} / 2$. The equivalent modeling of the differential pair with alpha models and beta models is illustrated in Fig. 5.10. Using beta models to model the differential pair makes the arrangement resemble two matched, interconnected alpha models with current gains whose value is beta instead of alpha. It is also important to note that the single ended input conductance is G_β, not G_α which a factor of $(\beta + 1)$ greater than G_β. The difference between the two values is a direct indication that compared to a single transistor, the input impedance of the differential pair is significantly higher. Another interesting implication of Fig. 5.10 is that only the collector of one transistor and the base of the opposite transistor are required to create a fully functional Colpitts oscillator provided both transistors are biased properly.

5.3 Non-Saturating Balanced Oscillator

The basic circuit typologies of the nonsaturating balanced pair oscillator is illustrated in Fig. 5.11. The topology actually resembles two oscillators operating 180° out of phase with each other. The oscillator can be designed using a modified approach to the three-terminal model of the oscillator circuit discussed in Sec. 5.1. Using the discussion of the nonlinear characteristic of the differential pair as a starting point, a quick design example of the nonsaturating balanced pair oscillator will be used to illustrate the manner in which the analysis of the reference oscillator can be applied to the balanced pair oscillator. Then, the simulation results of the design example will be reviewed. The criterion for the design has been set arbitrarily and is presented in Table 5.1. These criterion represent parameters that could be measured in the laboratory without compromising the accuracy of the measurements.

Base-Emitter Fundamental Voltage†	130 mV
Load Resistance†	1 kΩ
Output Fundamental Voltage†	1 V_{pk}
Approximate Frequency	10 MHz
Transistors	2N2222

† Denotes Single Ended Quantity

Table 5.1. Balanced oscillator design parameters.

Using Fig. 5.9 by normalizing the single-ended base-emitter fundamental drive voltage of 130 mV by $^{kT}/_{q}$ (~26 mV), the approximate value of the resulting output current is 1.23 • I_{DC}. The required collector current value is determined by dividing the output peak voltage by the load resistance. In this case, a collector current value of 800 μA results. Using the alpha factor of the 2N2222 transistor, the DC emitter current and in turn the DC current source values are determined from the value of the collector current. Because the alpha of the 2N2222 transistor is 0.998, the emitter current was set equal to the collector current in the simulations, causing the value of the DC current source to be 1.6 mA (2 • I_{DC}).

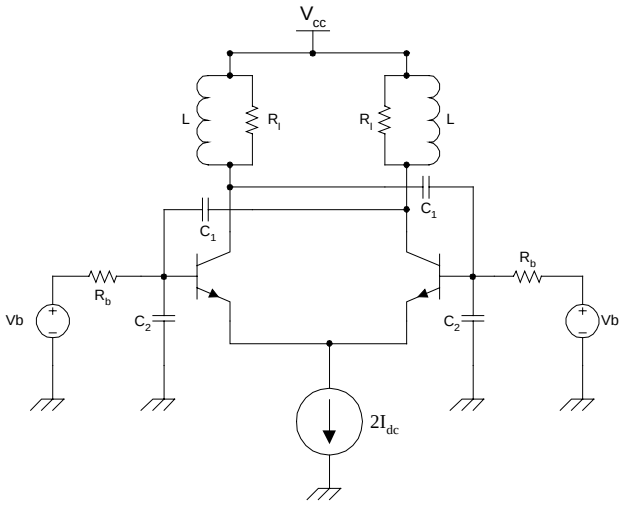


Figure 5.11. Non-saturating balanced pair oscillator circuit.

Assuming the reactances of the capacitors forming the feedback network are less than any resistance in parallel with them, the voltage division across the feedback network is dominated by the capacitor reactances. The choice of the voltage division ratio of the feedback network must reflect the balanced nature of the oscillator which causes the emitters of the two transistors to be at a virtual AC ground. For this reason, the feed back network must be chosen such that the single-ended output fundamental voltage divided by the voltage transformation ratio, n, will be 0.13 V. The required value of n is 7.6923 (1 ÷ 0.13). Having obtained n, the loop gain equation the Colpitts oscillator (Eq. 5.5) is modified for the differential pair to determine the value of the bias resistors connected to the bases that will ensure oscillation. Returning to the beta model representation of the differential pair in Fig. 5.10, balanced operation with non-zero V_{diff} requires $-v_{be1}$ to equal v_{be2} where both have magnitudes equal to one-half that of V_{diff}. The result is what appears to be two alpha models interconnected at their bases. Combining the models of Fig. 5.10 with the circuit topology of Fig 5.11 results in the oscillator equivalent circuit illustrated in Fig. 5.12. The arrangement of Fig. 5.12 is identical to a pair of Colpitts oscillators, with the controlled-current source of one driving the linear feedback network

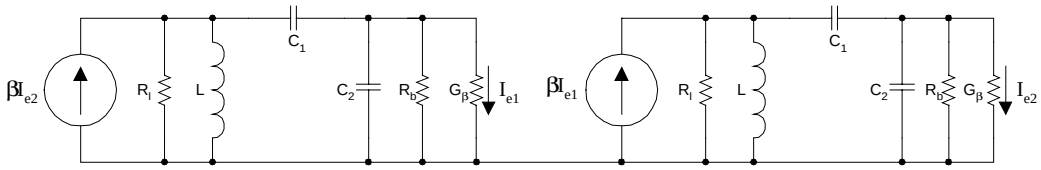


Figure 5.12 Beta model equivalent circuit of balanced oscillator.

connected across the base-emitter junction of the other. Thus, provided the balance is not significantly disturbed, the operation is akin to a pair of Colpitts oscillators operating 180° out of phase with each other as predicted . With this in mind, Eq. 5.5 can be modified to apply the differential pair oscillator by exchanging β for α. The nonlinear input conductance must also be changed from G_α to G_β to reflect the original use of the beta model. The resulting form of the loop gain equation is

$$G_\beta \frac{\beta\, n\text{-}1}{n^2} = G_3 + \frac{G_2}{n^2} + G_1\left(\frac{n-1}{n}\right)^2 \tag{5.13}$$

Because β is usually large (on the order of 100) and n should always be greater than one, the unity term on the left hand side of the equation makes little change to the overall result. In the circuit topology of Fig. 5.12, the term G_1 is zero consequently, simplifying the process of determining the required bias conductances. The remaining values for the bias resistors, R_b, along with the final values of the capacitors and inductors to achieve the 10 MHz oscillation frequency were determined and entered into a PSPICE simulation. The value of the voltage source biasing the base was chosen to be 2.6 V to ensure saturation would not occur. These voltage sources are intended to represent the Thevenin equivalents of the actual bias scheme.

The simulation initial conditions were adjusted such that the DC bias conditions were well established for the transistors at the start of the simulation. Transient simulations were run for a total of 60 µs with both step and print sizes set to 0.5 ns. The final 30 µs of the resulting time domain voltage waveforms were post processed using the FFT option of Microsim™ PSPICE. The resulting spectrum was then plotted using a logarithmic vertical axis and a linear frequency axis. A plot of the differential voltage between the collectors of the transistors appears in Fig. 5.13a while a plot of one of the transistor's collector current appears in Fig. 5.13b. The fundamental component of the

differential voltage across the two 1 kΩ loads was 1.834 V, indicating that across each one it was 917 mV which is very close to the original desired value of 1 V. The deviation from the desired value is not altogether unexpected since the original calculations did not account for the presence of the additional harmonic components of the base-emitter drive voltage, or the nonlinear base-emitter junction capacitances. The presence of even harmonic currents in Fig. 5.13b should not be surprising since the current depicted is a single-ended signal which highlights the effect of imbalances on the output spectrum of the differential pair.

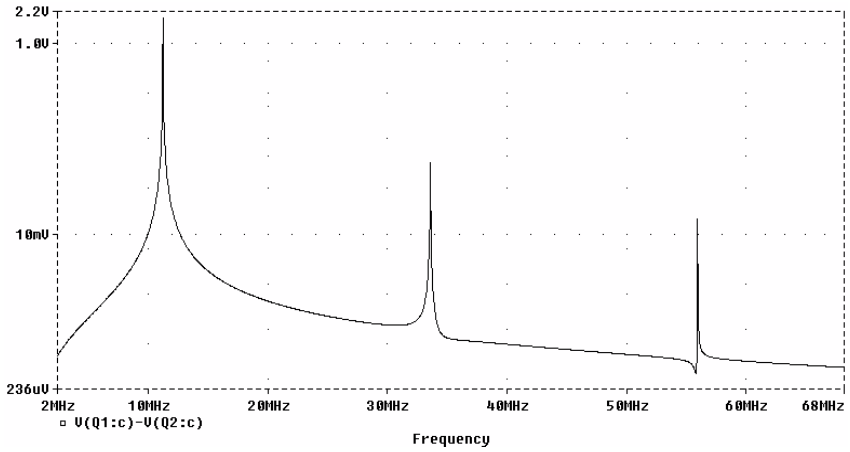


Figure 5.13a. Differential voltage between collectors of non-saturating balanced pair oscillator.

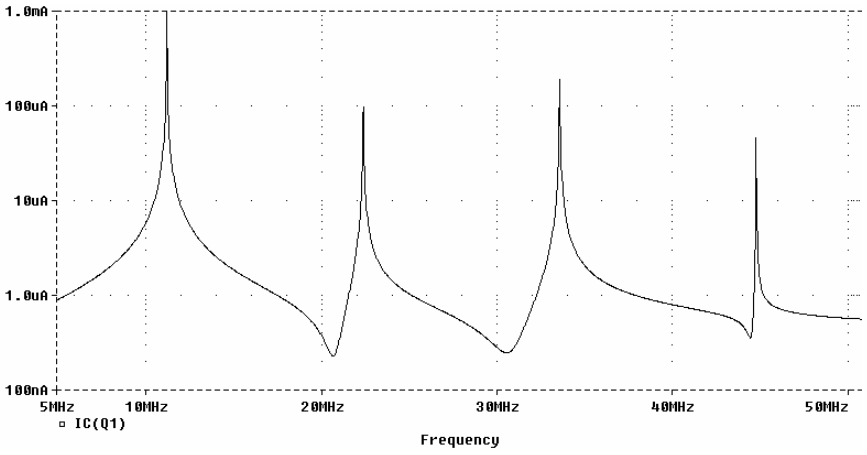


Figure 5.13b. Collector current of one transistor of non-saturating balanced pair oscillator.

5.4 Saturating Balanced Pair Oscillator

The most common realization of the saturating balanced pair oscillator is depicted in Fig. 5.14. In some respects, its structure resembles that of a multivibrator, while in other respects it resembles the non-saturating balanced pair oscillator. Upon comparison, the saturating balanced pair oscillator is equivalent to the non-saturating balanced-pair oscillator where the capacitors corresponding to C_1 in the Colpitts feedback configuration have been assigned the value infinity and the capacitors corresponding to C_2 are assigned the value zero. This causes the value of the voltage transformation ratio to be one, and the load and bias conductances to be combined into a single load resistance designated R_l. The one important distinction between the two oscillators is the saturation mechanism.

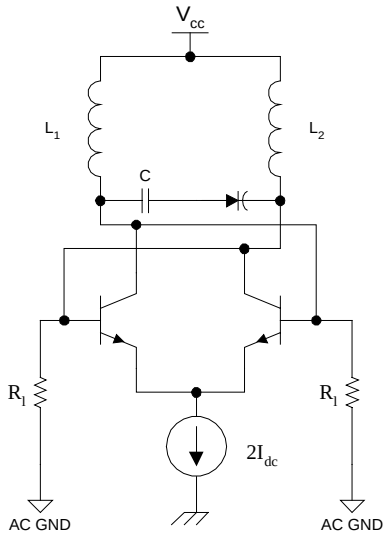


Figure 5.14. Typical implementation of the saturating balanced pair oscillator.

In the case of the non-saturating balanced-pair oscillator, base-collector junctions were reverse biased for all excursions of the oscillator signal. The construction of the saturating balanced-pair oscillator is such that the base-collector junction is periodically forward and reverse biased causing rectification to occur in the base-collector junction. Returning to the Ebers-Moll model, the saturation properties of the transistor can be accounted for by introducing another diode with cathode connected to the base and anode connected to the collector. The additional diode can then be modeled as an equivalent conductance, G_{bc}. In doing this for the topology of Fig. 5.14, the balanced nature of the circuit causes the conductance to act in parallel with the lumped load conductance R_l.

The load conductance G_l can be combined with G_{bc} to form a total loading conductance G_{res} shown in the oscillator's AC equivalent circuit (Fig. 5.15).

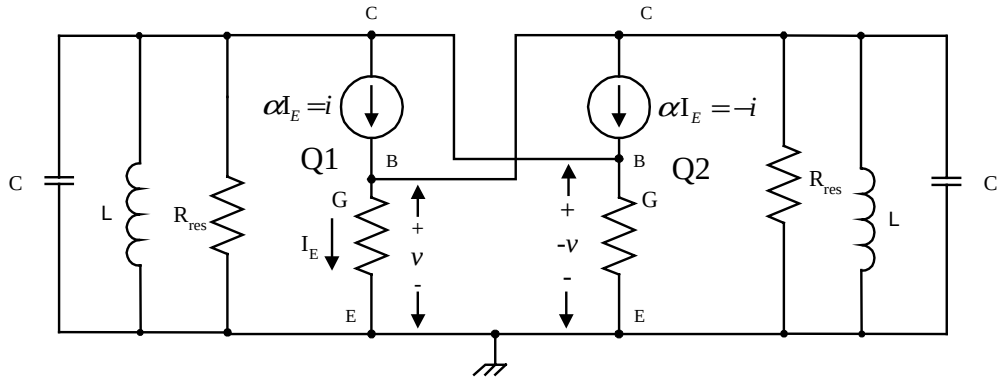


Figure 5.15. AC equivalent circuit of saturating balanced pair oscillator.

Provided the load conductance is small compared to G_{bc}, the conductance presented to the oscillator is essentially G_{bc} and oscillation is sustained. As the value of the load conductance increases and becomes comparable to G_{bc}, the amplitude stability suffers while the oscillation signal amplitude begins to diminish until finally the loop gain falls below one and oscillation ceases. To obtain some idea of the nature of the effect the loading conductance has on the oscillator, Eq. 5.13 can be rewritten for the saturating oscillator by substituting unity for the value of n and taking G_1 to be zero, resulting in the form,

$$G_3 = G_{res} = G_\beta(\beta - 1) = 4G_{bc} + G_L \tag{5.14}$$

Using equivalent expressions for G_β and β, Eq. 5.14 can be rewritten as,

$$R_{res} = \frac{v_1}{i_1\,(2 - 1/\alpha)} \tag{5.15}$$

Further analytical determination of the bias point of the oscillator is prohibitively difficult and has not been pursued. In order to progress farther, G_{bc} must be expressed as a function of twice the single-ended fundamental drive voltage. The values of the collector current fundamental current versus the drive level for the balanced pair operating linearly must be used expressing G_β as a function of the single-ended fundamental drive voltage. The final step would involve substituting the circuit parameters into Eq. 5.14 along with the two nonlinear conductance functions and iteratively stepping through values of drive

level until the equation is satisfied. This process bears a strong resemblance to the method of harmonic balance, only in this case there is only one harmonic in use.

Measurements of the effects of additional loading on the oscillator's output amplitude have been made using the VCO of the RF2905. The original varactor diode and fixed capacitor of the VCO illustrated in Fig. 5.14 were replaced by two identical varactors whose Q values were approximately $^1/_4$ that of the original varactor diode. An external source was used to provide the control voltage input to the VCO, after breaking the connection to the PLL loop filter. Measurements of the output power versus control voltage were made and appear in Fig. 5.16. As the reverse bias voltage on the varactor diodes was reduced, the output power stayed relatively constant until over a very short range of control voltage the output power fell off rapidly. The loading on the circuit

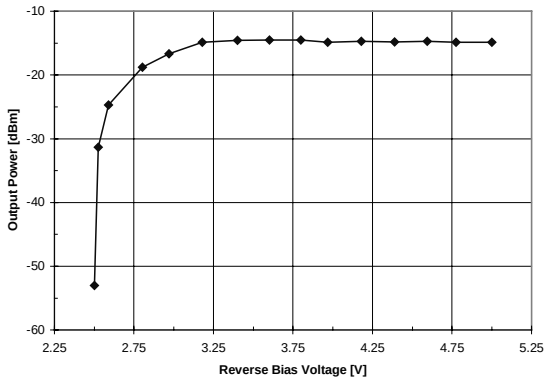


Figure 5.16. Plot of RF2905 output power vs. varactor reverse bias voltage.

increases as the reverse bias voltage is decreased because the depletion regions within the two varactor diodes shorten, leaving more undepleted semiconductor material to act as a series resistance. Thus, returning to Fig. 5.15, it becomes clear that initially the losses in the resonator circuit are low enough that the saturation conductance is dominant. As the reverse bias voltage decreases, the losses in the external resonant tank circuit begin to become dominant until finally, there is enough loss to lower the loop gain of the oscillator below unity.

The saturation mechanism makes the design of the oscillator much easier than the linear version. With no tapped capacitor network to be determined or careful biasing to prevent the transistors from saturating, the design of the saturated oscillator is reduced to

picking the values of the tuning elements and a DC bias. Since the output level is controlled by the saturation mechanism, the changes in the loading presented to the oscillator by the transmitter output stages (See Sec. 4.1) should not significantly affect the amplitude of the oscillator signal. It would be undesirable to have the output level of the oscillator decreasing as the bias on the power amplifier was increasing. The advantages afforded by saturation do come at the price of increased oscillator noise. This arises because the limiting mechanism associated with saturation causes the Q of the resonator to be lowered, widening the noise bandwidth of the oscillator. Additionally, because the bases are directly connected to the collectors and the resonator, the loading presented by the external circuitry also has an effect on the Q of the resonator. Noise is one area where the non-saturating balanced pair oscillator has a definite advantage over the saturating version since the tapped capacitor networks transform the loading impedances into higher values, thus decreasing the loading directly on the resonator and providing a better phase noise performance.

5.5 Tuning Methods for the Oscillators of the RF2905

Both oscillators bear striking similarities in the mechanisms employed to tune their respective frequencies of oscillation. The balanced pair oscillator can be thought of as a pair of coupled Colpitts oscillators operating 180° out of phase with each other which helps explain the similarity between the methods for selecting and varying the frequency of oscillation used for two oscillators. Differences both in Q and frequency arise between the two oscillators due to the difference between the quartz crystal resonator of the Colpitts reference oscillator and the lumped element LC resonator of the VCO. Quartz crystal resonators are typically limited to frequencies at or below 100 MHz and have a Q in the range of 10,000 to 150,000. While the LC tank configurations of the VCO can range up to a few gigahertz, the Q of these networks are usually on the order of only 50 to 100.

For frequencies near the fundamental mode of resonance, the crystal resonator of the reference oscillator is modeled by the equivalent circuit of Fig. 5.17. Due to the presence

of the shunt capacitance which arises as a result of the crystal holder's parasitic capacitance, the crystal possesses both a series and parallel resonance (anti-resonance).

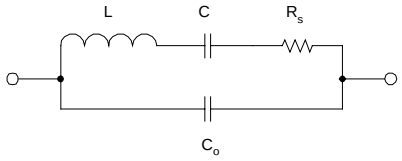


Figure 5.17. Equivalent Circuit of quartz crystal near fundamental resonance.

The anti-resonant frequency of the crystal can be related to the series resonant frequency of the crystal by[22][23],

$$\omega_a = \omega_s \sqrt{1 + \frac{C}{C_o}} \tag{5.16}$$

where ω_a is the anti-resonant frequency and ω_s is the series resonant frequency given by $(LC)^{-½}$. The parallel mode crystal of the RF2905 reference oscillator requires a particular external load capacitance in parallel with the crystal to be resonant at its specified frequency. This load capacitance is realized by the series combination of the feedback network capacitors in the oscillator. The two frequencies, ω_a and ω_s, define what is termed the pulling range of the crystal. The series resonance represents the lowest frequency at which resonance will occur, since no additional external loading capacitance is required to achieve a condition of resonance. The anti-resonant frequency is the highest frequency at which a resonance condition will take place since all of the inductive reactance of the crystal is equal to the external capacitve reactance. The frequency of oscillation may be adjusted by adding a capacitive reactance in parallel or series with the crystal. Adding the capacitive reactance in series will have a greater effect on the frequency than adding the reactance in parallel because the reactances add in series configurations and the susceptances add in parallel configurations. Care must be taken to avoid pulling the crystal too close to its series resonance where the series resistance (and resultant losses) dominate.

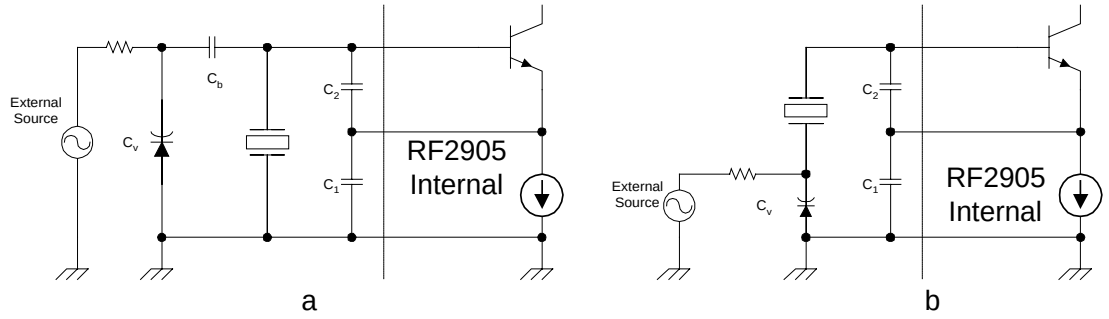


Figure 5.18. (a) Parallel and (b) series mode oscillator pull setups.

The additional variable value of capacitive reactance is realized by adding a reverse biased varactor diode in the appropriate arrangement as illustrated in Fig. 5.18 a and b respectively. Some care must be exercised in selecting the placement of the bias resistor and DC blocking capacitor used in the parallel pull method to ensure that the Q of the crystal resonator is not degraded by the AC loading of the bias resistor. A good explanation of the proper values of bias resistor and bias arrangement for using varactor diodes in tuning circuits is given in Rohde's book on Microwave synthesizers. Using the arrangements illustrated in Fig. 5.18, the frequency versus voltage characteristics for the two methods were measured and are plotted in Fig. 5.19 a and b respectively.

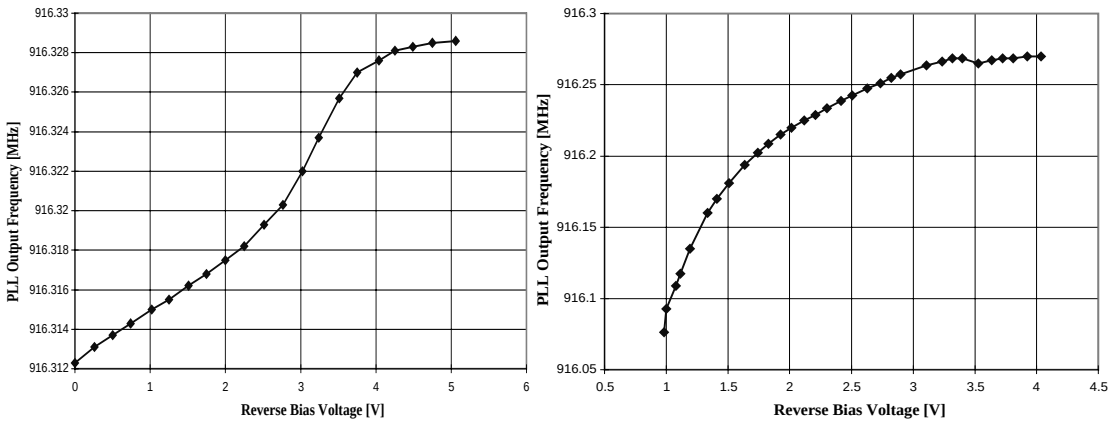


Figure 5.19. Measured performance of (a) parallel and (b) series reference oscillator pull.

Returning to the case of the saturating balanced pair oscillator, the typical resonator of the RF2905 is composed of two inductors, a fixed capacitor, and a varactor diode. Due to the balanced nature of the oscillator, the voltage across the resonator can be split into two AC voltages to be denoted $+v$ and $-v$, with a virtual ground within the resonator circuit

dividing the reactances into two equal quantities as depicted in Fig. 5.15. Assuming the components of the original resonator circuit are ideal, the value of each of the inductors in Fig. 5.15 will be the arithmetic mean of the values of the two inductors in the physical circuit. Similarly, the series combination of the varactor diode capacitance and the fixed capacitor is equal to C_{eq}, then the virtual ground would exist exactly in the middle of this equivalent capacitance, making the value of each capacitor in Fig. 5.15 equal to $2C_{eq}$. Thus, the frequency of oscillation is calculated as

$$f_0 = \frac{1}{2\pi\sqrt{\frac{1}{2}\left(L_1 + L_2\right)\left(\frac{2C_1C_2}{C_1+C_2}\right)}} \tag{5.17}$$

Parasitic inductances and stray capacitances will ultimately cause the resonant frequency of the resonator to deviate from this value (Eq. 5.17) to some degree. The nonlinear base-emitter and base-collector junction capacitances will affect the tuning of the saturating balanced-pair oscillator as well. The value of these capacitances is directly related to the DC bias and AC peak voltage applied to the junctions. If these capacitances were included in the equivalent circuit of Fig. 5.15, one set of base-emitter and base collector junction capacitances would be in parallel with the capacitors of value $2C_{eq}$. Provided the value $2C_{eq}$ is significantly larger than these junction capacitances, the effect on the output frequency is minimized. As discussed briefly in Ch. 4, the output frequency can be pulled significantly by changes in the loading presented to the oscillator. Although it may be desirable to increase the tuning capacitance in a given application, the internal varactors must change the total value of capacitance by the same proportion to achieve the same FM deviation originally specified.

It is widely believed that using balanced varactor diodes may have an advantage over a single varactor diode in noise performance. The basis for this perception is that the noise is due to a single noise source connected to the common connection of the diodes, and blatantly ignores the independent noise contributions due to the losses in the individual diodes themselves. An additional problem with the balanced varactor arrangement is that it requires the two varactors to be nearly identical in device characteristics and runs the risk of increasing the noise if they are not. The increase is primarily due to the fact that in general the tuning sensitivity of the VCO is increased by a

factor of two over that of using a single varactor. One potential advantage it does provide is for the situation where the peak voltage present in the resonator is sufficient to forward bias the varactor for a portion of a cycle. The balanced varactor arrangement will balance the resulting distortion of the output voltage such that the second harmonic that would result will not be present in the differential output voltage.

Using two nearly identical discrete varactor diodes, the standard resonator circuit was used as the basis to test the noise improvement provided by balanced varactors over a single varactror. With a very small PLL bandwidth (< 1 kHz), the single sideband phase noise density of the RF2905 VCO was measured with the two varactors in place instead of a single varactor and a fixed capacitor. One of the diodes was then replaced with a fixed capacitor whose value was equal to the capacitance of the varactor at 1 V reverse bias. The single-sideband phase noise measurement for the balanced varactor setup was stored on the spectrum analyzer and then overlaid on the measurement of the single varactor configuration. The resulting spectrum analyzer display appears in Fig. 5.20. Interestingly, the dual varactor configuration performed approximately 3 dB worse than the single varactor configuration. This result is not altogether unexpected as the Q of each of the varactors is much less than that of the fixed capacitor. As will be shown in Ch. 6, the intrinsic phase noise of the VCO dominates the performance of the PLL at frequencies offset from the output signal that lie outside the PLL bandwidth. Thus, the noise contribution from the control line (which the balanced nature of the varactors removes) is small compared to the phase noise contribution from the loss mechanism associated with the varactor. Since the noise generated by the varactors is dominant, the loss mechanisms within the resonator double in the balanced varactor arrangement causing the phase noise outside the PLL bandwidth to double as well.

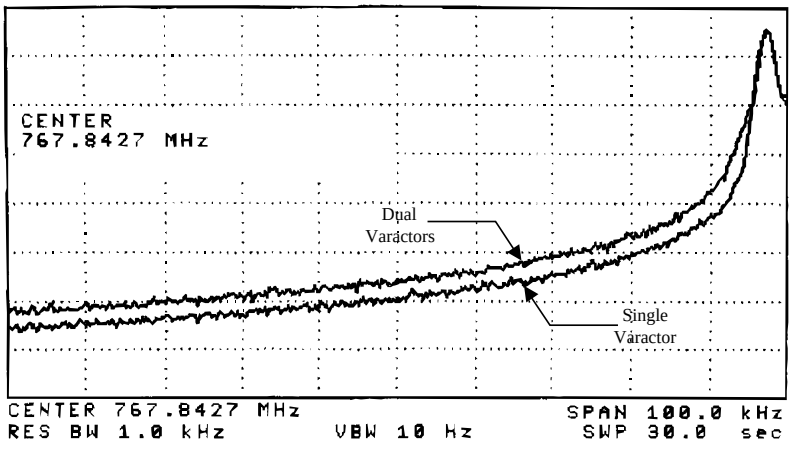


Figure 5.20. Sideband oscillator noise spectrum using balanced tuning varactors vs. single varactor.

Finally, using Eq. 5.17 as a guide, other resonant network components such as microstrip, or printed inductors can be used with the saturating balanced pair oscillator. The low Q associated with printed inductors may be unacceptable for some applications. Some experiments were conducted with the aim of examining the frequency limits of the oscillator. It was found that though the oscillator would operate at higher frequencies, the output power was significantly lower and the gain control performance was no longer monotonic. Due to the cost associated with a higher frequency PLL IC chip and the limitations on the gain control mechanism, use of the RF2905 structure at frequencies higher than 1 GHz is probably not practical.

5.6 Noise In Oscillators

Noise is present within all oscillators, primarily due to the internal noise generation mechanisms associated with the transistor. The noise mechanisms associated with the transistor can be accounted for by introducing noise voltage and current sources at either the input or output of the transistor two port [13]. The location of the noise sources, representative of an ABCD parameter approach to characterizing the transistor noise figure within the oscillator circuit, are illustrated in Fig. 5.21. At first glance, one might assume the noise current source does not contribute to the emitter current because the emitter current is modeled as depending solely upon the base-emitter voltage. The noise current does affect the base-emitter noise voltage by driving the value of the conductance G_T reflected through the transformer.

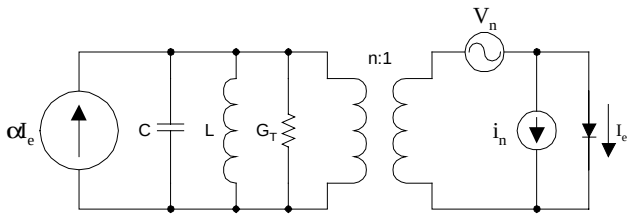


Figure 5.21. Illustration of oscillator with transistor noise sources present.

A widely used model for predicting the effects of noise in oscillators is the Leeson Model [16] which consists of an amplifier with noise figure, F, and a filter connected in a positive feedback circuit. This arrangement is illustrated in Fig. 5.22. The additive noise present at the output of the oscillator can be expressed in terms of amplitude and phase modulation components. Because the amplitude modulation components can be removed using a limiter, Leeson's model focuses on the phase modulation component, $S_{\Delta\theta}(j\omega_m)$, which comprises one-half of the additive noise power present at the offset frequency ω_m. The filter transfer function, $L(j\omega_m)$, is the low pass equivalent of the bandpass transfer function of the oscillator resonator. This substitution is made because the most common

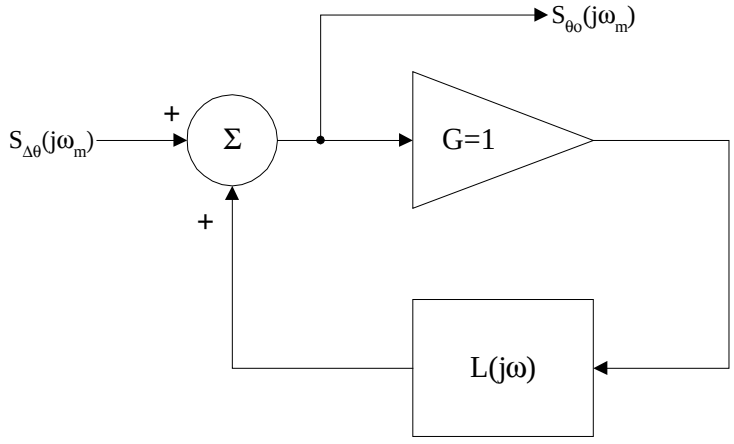


Figure 5.22. Illustration of Leeson's oscillator model.

method of describing the noise of the oscillator is by expressing the single sideband power relative to the total signal power at a frequency offset from the carrier [6]. The low pass equivalent transfer function is expressed as,

$$L(j\omega) = \frac{1}{1 + j2Q_{loaded}\frac{\omega_m}{\omega_o}} \tag{5.18}$$

while the input phase noise power spectral density, $S_{\Delta\theta}(j\omega)$, is assumed to be given by [14],

$$S_{\Delta\theta}(j\omega) = \frac{FkT}{2(P_s)_{av}}\left(1+\frac{\omega_c}{\omega_m}\right) \tag{5.19}$$

where k is Boltzmann's constant ($1.38 \bullet 10^{-23}$ J/K), and T is the noise temperature (in Kelvin units). Leeson's original model did not include the term accounting for the transistor f^{-1} noise (ω_c / ω_m) in Eq 5.19, but only the term corresponding to flat thermal noise. The amplifier of Fig. 5.22 is assumed to provide sufficient gain to ensure that the loop gain at resonance is unity. Using Eq. 5.18 to express the magnitude-squared, closed-loop transfer function of the oscillator loop, the expression for the single sideband noise density normalized to the total signal power as a function of offset frequency is given by,

$$S_{\theta o}(j\omega) = \frac{S_{\Delta\theta}(j\omega)}{\left|1-L(j\omega)\right|^2} = \frac{FkT}{2(P_s)_{av}}\left(1+\frac{\omega_c}{\omega_m}\right)\left(\frac{\omega_o^2}{4Q_{loaded}^2\omega_m^2}\right) \tag{5.20}$$

provided the frequency offset is sufficiently small ($\omega_m < 2Q_{loaded} / \omega_o$). Other authors have made modifications to Eq 5.20 in order to relate the unloaded resonator Q to the value of the loaded resonator Q [5][14][15]. Although the transistor is operating as a nonlinear device in order to provide the amplitude stability required for sinusoidal oscillation, the transistor is modeled as a linear gain element in the Leeson model. The assumption that the transistor behaves linearly to the noise, while it operates in a nonlinear fashion would appear to undermine the validity of the model. In order to shed some light on this contradiction, the noise present in the oscillator must be analyzed using a nonlinear approach in order to determine the overall effect of the nonlinear behavior of the transistor on the oscillator noise.

Returning to Eq. 5.2, the nonlinear expression for the emitter current is rewritten to include a random variable term representing the noise voltage (ΔV) present across the base emitter junction. The resulting emitter current with noise is given by,

$$I_e = I_{ES}\left(e^{\frac{qV_{DC}}{kT}}\right)\left(e^{\frac{qV_1\cos\omega t}{kT}}\right)\left(e^{\frac{q\Delta V}{kT}}\right) \tag{5.21}$$

Using Eq. 5.3, the first three terms of Eq. 5.21 can be replaced with a Fourier series representation. Since ΔV can be assumed small compared to $^{kT}/_{q}$ (26 mV), it is possible to approximate the exponential function of the noise voltage by the first two terms of a Taylor series. Performing these substitutions, the resulting expression for the emitter current with noise is given by,

$$I_e(t) = I_{dc}\left[1 + \sum_{n=1}^{\infty} \frac{2I_n(x)}{I_0(x)} \cos(n\omega t)\right]\left(1 + \frac{\Delta V}{V_{th}}\right) \tag{5.22}$$

where V_{th} represents $^{kT}/_{q}$ and $x = V_1 / V_{th}$. After expanding the expression, three basic components will be present; one corresponds to the original oscillator solution in the absence of noise, another is a small signal amplification of the noise, and the third is a large signal modulation of the low-frequency noise. In effect, this expression suggests the nonlinearity modulates the oscillator fundamental signal and its harmonics with the noise present across the base emitter junction. The power spectral density (PSD) of ΔV, denoted $S_{\Delta V}$, is translated in frequency by the modulation process since ΔV is not correlated with the harmonics of the oscillator. Because this frequency translation results from a nonlinear process, the PSD of the noise voltage across the base-emitter junction must be split into two functions, one which is linearly amplified by the small signal transconductance and one which is modulated by the large signal transconductance. This split is illustrated in Fig. 5.21, where the oscillator has been redrawn conceptually, to illustrate the effect of the oscillator circuit components on the noise. The noise current source and voltage sources have been lumped into a single voltage source to simplify the diagram.

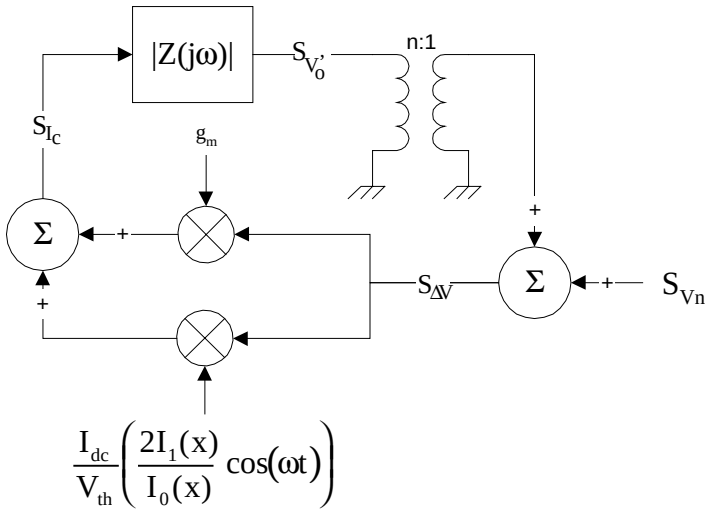


Figure 5.23. Block diagram of noise in nonlinear oscillator circuit.

The block |Z(jω)| represents the parallel resonant network of Fig. 5.6b which is assumed to be a high-Q, bandpass resonant network with center frequency equal to ω_o. The effect of the nonlinear behavior of the transistor is represented conceptually by the blocks between the PSDs, $S_{\Delta V}$ and S_{Ic}. Due to the bandpass nature of the resonant network, the $S_{Vo'}$ will consist of the filtered components of S_{Ic} in the vicinity of ω_o. The components of I_c in the vicinity of ω_o are generated by components of $S_{\Delta V}$ near ω_o amplified by the small signal transconductance, g_m, and components of $S_{\Delta V}$ near DC and $2\omega_o$ modulated by the oscillator fundamental frequency term (see Fig. 5.24). Since $S_{Vo'}$ is concentrated in the vicinity of ω_o, the DC and $2\omega_o$ components of $S_{\Delta V}$ are contributed by

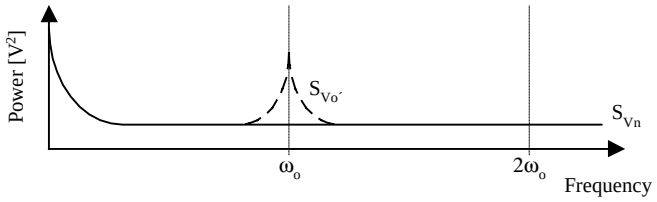


Figure 5.24. Illustration of noise voltage PSD's vs. frequency.

S_{Vn} only. Thus, any given spectral component of S_{Ic} near ω_o is the sum of the modulated DC and $2\omega_o$ components of S_{Vn} plus the component of $S_{\Delta V}$ near ω_o, which can be expressed as,

$$S_{I_c}(j\omega) = \left(\frac{\alpha I_{dc}}{V_{th}}\right)^2 \left(S_{\Delta V}(j\omega) + \left(\frac{I_1(x)}{I_0(x)}\right)^2 \left(S_{V_n}(j(\omega-\omega_0)) + S_{V_n}(j(\omega+\omega_0)) \right) \right) \quad (5.23)$$

The higher order harmonic terms of the oscillator signal modulated by noise are neglected since their contribution is small compared to the fundamental's contribution. It is reasonable to assume the DC and $2\omega_o$ components of S_{Vn} are uncorrelated with the components of $S_{\Delta V}$ that are within the bandwidth of the resonator. This assumption allows the mixer can be removed, and the terms resulting from the modulation process can be represented by a new noise current source adding noise to the collector current. Since the resulting transfer function is linear, this noise source can be moved to the input by dividing its PSD by the small signal transconductance squared. This step simplifies the analysis in that it allows a single expression for the closed loop transfer function to be used for both the modulated and linearly amplified noise components.

The oscillator loop becomes a simple linear positive feedback loop whose open loop transfer function in terms of offset frequency is given by,

$$G(j\omega_m) = \frac{g_m}{nG_T\left(1 + 2jQ\frac{\omega_m}{\omega_o}\right)} \quad (5.24)$$

where G_T is the total conductance presented to the resonant network, g_m is the small signal transconductance given by $\alpha\ I_{dc} / V_{th}$, and Q represents the loaded Q of the network at frequency offset ω_o. The magnitude-squared closed loop transfer function in terms of offset frequency is given by,

$$|H(j\omega_m)|^2 = \left|\frac{V_o(j\omega_m)}{V_n(j\omega_m)}\right| = \frac{1}{\left(\frac{G_T}{g_m}\right)^2 \left(\left(1 - \frac{g_m}{nG_T}\right)^2 + 4\left(Q\frac{\omega_m}{\omega_o}\right)^2 \right)} \quad (5.25)$$

where it is important to note that the term g_m / nG_T is the small signal open loop gain at resonance. Under the linear assumption of the Leeson model, this term would be equal to unity, and the closed loop transfer function would be equal to the low pass equivalent transfer function L(jω) of Leeson's model. Because the linear assumption is invalid due to the nonlinear operation of the transistor, the magnitude-squared response of the closed

loop transfer function, $H(j\omega_m)$, becomes flat for sufficiently small offset frequencies. The total noise PSD, $S_{Vn'}$, applied to the input of this closed-loop transfer functions is given by.

$$S_{V_n'}(j\omega_m) = FkT\left(1+\left(\frac{\omega_c}{\omega_m}\right)\left(\frac{I_1(x)}{I_0(x)}\right)^2\right) \tag{5.26}$$

The output noise PSD, given by the product of (5.25) and (5.26), at offset frequencies below the corner frequency, f_c, increases as $1/f$ and not $1/f^3$ as the modified Leeson model (Eq. 5.20) would suggest.[5][14] This result may be indicative of the nonlinear amplitude limiting which causes the large signal loop gain to be unity. As was the case with the limiting IF amplifiers, the phase modulation component of the noise may not be affected in the same manner as the amplitude modulation components. In order to investigate this result further, it may be necessary to express the additive noise spectral density S_{Vn} in terms of potentially correlated amplitude and phase modulation noise components. This extension of the analysis goes beyond the intended scope of this section and is left as the subject of further study.

6. Phase Noise in Phase-Locked Loops

6.0 Chapter Overview

Phase noise is a concern for all signal sources, and the RF2905 is no exception. For frequency and phase modulated systems, phase noise generated by the local oscillator and thermal sources can reduce receiver sensitivity. Additive thermal noise combines with the phase noise modulated onto the down-converted signal and presents an increased level of noise to the demodulator. The extent to which this additive noise is a concern depends upon the sensitivity requirements of the receiver. For FM transceivers like the RF29X5 family, the FM deviation can be made very large making phase noise less of a concern. There is a disadvantage to using a wider deviation than necessary because it ultimately reduces the number of possible channels available within the Industrial Scientific and Measurement (ISM) band due to the increase in the occupied RF bandwidth. In order to achieve a fine channelization within the limited ISM band, a smaller deviation would be required, raising concerns over the effects of phase noise. The following section will provide some insight into the various contributors to the overall local oscillator (LO) phase noise and their magnitudes.

6.1 Introduction to Phase Noise

The signal generated by any frequency source can be described in terms of amplitude and frequency stability. The short term instabilities which influence the demodulation process are typically described in the frequency domain as opposed to the long term variations described in the time domain. In the frequency domain, short term instabilities create noise sidebands about the carrier frequency that can be related to random amplitude and phase modulations of the carrier. This noise is expressed by

$$V_o(t) = V_c(t)\cos\left(2\pi f_c t + \phi_n(t)\right) \tag{6.1}$$

where $V_c(t)$ and $\phi_n(t)$ represent the effect of the noise on the amplitude and phase respectively of a perfect single tone sinusoidal carrier. Provided the amplitude effect is removed by either nonsaturating limiting or is negligible due to good oscillator design

practices, the frequency spectrum would consist of the carrier and symmetric phase noise sidebands on either side of it.

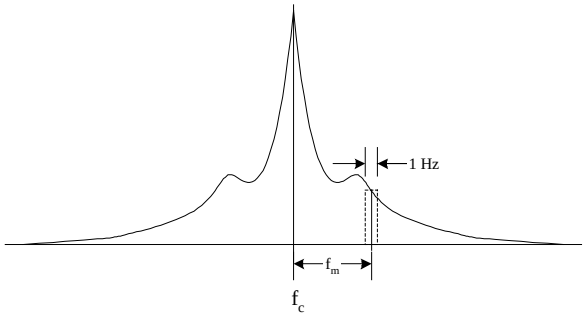


Figure 6.1. Illustration of carrier with phase noise.

Though the phase noise density is not flat over the entire frequency spectrum as depicted in Fig. 6.1, the noise in any given 1 Hz bandwidth at an frequency offset f_m from the carrier can be related to a random sinusoidal phase modulation at frequency f_m and peak phase deviation of $\Delta\theta$ [12]. By first expressing the modulation in the form

$$V_o(t) = \sqrt{2C}\cos(\omega_c t + \Delta\theta \sin \omega_m t) \tag{6.2a}$$

$$= \sqrt{2C}\left(\cos(\omega_c t)\cos(\Delta\theta \sin \omega_m t) - \sin(\omega_c t)\sin(\Delta\theta \sin \omega_m t)\right) \tag{6.2b}$$

$\Delta\theta$ can be assumed small compared to one radian allowing the cosine of the modulation term to be replaced by unity and the sine of the modulation term to be replaced simply by the modulation term. This simplification results in the desired carrier and two sidebands as given by

$$V_o(t) = \sqrt{2C}\left[\cos(\omega_c t) - \tfrac{\Delta\theta}{2}\left(\cos(\omega_c - \omega_m)t - \cos(\omega_c + \omega_m)t\right)\right] \tag{6.3}$$

Replacing the peak phase deviation with an RMS deviation (assuming that $\Delta\theta = \theta_{RMS}\sqrt{2}$), the power in one sideband divided by the power residing in the carrier is given by

$$P_{SSB} = \frac{\theta_{RMS}^2}{2} \tag{6.4}$$

This equation has particular significance to the analysis of the phase noise of a phase-locked loop (PLL). Since the VCO is a frequency modulated oscillator, the phase modulation model which describes phase noise is directly applicable. Also, because of the high SNR levels within a PLL synthesizer, the influence of noise is so small that the

linear approximation of its behavior is appropriate. This linearity allows the PLL to be treated as a time invariant filter allowing for the use of superposition in the analysis of the PLL phase noise. Since each component is a contributor in some degree to the phase noise of the loop, all of the components can be modeled as ideal with an additive noise source corresponding to the noise generated by each device. Using superposition of noise power, the effect noise sources at each point in the loop have on the output oscillator phase is easily determined.

In order to proceed, several assumptions must be stated. The loop filter type will have an impact on the transfer functions used to propagate each of the noise sources to the VCO. The type of loop filter employed will be assumed to be a second order loop filter with one pole beyond the loop bandwidth for spurious signal rejection. Also, it is assumed that the each of the noise sources are independent of all the others. Thus, the RMS phase noise will be the square root of the sum of the variances of each of the noise sources filtered by their respective transfer functions.

6.2 Reference Oscillator

Because of the position of the reference oscillator within the loop, the phase noise imparted to the loop is directly proportional to the oscillator phase noise. Using Fig. 6.2 as a reference, the transfer function for the noise propagated through the loop from the

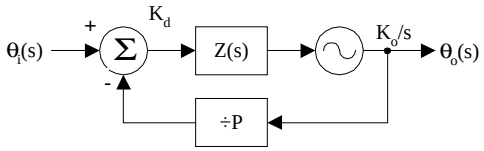


Figure 6.2. Reference oscillator as a noise source.

reference oscillator can be calculated. The transfer function is the same as that derived for transient analysis, and is given by,

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{K_o K_d Z(s)}{s\left(1+\frac{K_o K_d Z(s)}{sP}\right)} \tag{6.5a}$$

and in terms of the second order loop filter components is

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{K_o K_d\left(RC_2 s+1\right)}{s^2\left(C_1+C_2\right)\left(\frac{RC_1C_2}{C_1+C_2}s+1\right)+\frac{K_o K_d}{P}\left(RC_2 s+1\right)} \tag{6.5b}$$

Using Eqs. 6.2-4, the measured single-sideband phase noise of the reference oscillator can be related to its corresponding phase noise density (expressed as radians/Hz). The contribution to the PLL output phase noise from the reference oscillator is then determined by multiplying the RMS phase noise density (which is a function of offset frequency f_m) by the magnitude of Eq. 6.5b where $j2\pi f_m$ is substituted for the Laplacian variable s.

6.3 VCO

The phase noise source associated with the inherent phase noise of the VCO is introduced after the VCO transfer function block as illustrated in Fig. 6.3.

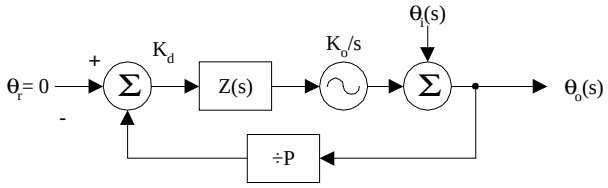


Figure 6.3. VCO phase noise effect on output.

The transfer function for the additive noise on the VCO control line to the output phase deviation is given in a general form by

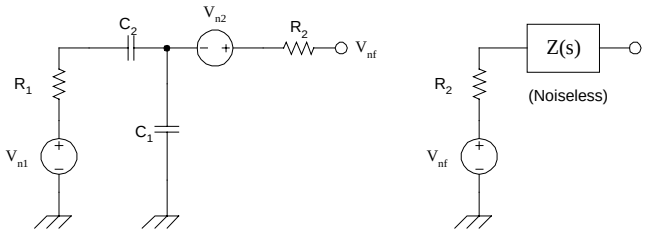
$$\frac{\theta_o}{\theta_i} = \frac{1}{1+\frac{K_o K_d Z(s)}{sP}} \tag{6.6a}$$

specifically for the second order loop filter, as

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{s^2\left(C_1+C_2\right)\left(\frac{RC_1C_2}{C_1+C_2}s+1\right)}{s^2\left(C_1+C_2\right)\left(\frac{RC_1C_2}{C_1+C_2}s+1\right)+\frac{K_o K_d}{P}\left(RC_2 s+1\right)} \tag{6.6b}$$

6.4 Loop Filter

Although often ignored by most designers, the loop filter resistors can also be a source of noise generation within the loop. The thermal noise power generated within the loop filter resistors can be described using noise voltage sources as depicted in Fig. 6.4.



a. **b.**

Figure 6.4. Noise sources within the loop filter.

Neglecting the minor effect of $1/f$ noise in resistors, the thermal noise power is typically flat over the entire frequency spectrum. The RMS value of the voltage source corresponding to the noise generated in R_1 is given by

$$V_{n1}(s) = \sqrt{4KTBR_1} \tag{6.7}$$

The value for the voltage corresponding to R_2 is calculated in a similar manner. The filter output voltage applied to the VCO is the result of the contributions of both of these noise voltages shaped by the RC network. An additional capacitance not shown in Fig. 6.4 is the capacitance of the varactor diode which is connected between the output of the loop filter and ground. The presence of this capacitance adds another RC pole usually higher than the second order loop filter poles which is often neglected. After some algebraic manipulation, the equation relating the resistor noise voltage sources, V_{n1} and V_{n2}, to the control line noise voltage, V_{nf}, is given by

$$V_{nf}(s) = \sqrt{\frac{\left|V_{n_1}\right|^2}{\left|\frac{(C_1+C_2)}{C_2}\left(\frac{R_1C_1C_2}{C_1+C_2}s+1\right)\right|^2} + \left|V_{n_2}\right|^2} \tag{6.8}$$

This equation shows that only the integrator pole in the VCO and the high frequency pole of the filter are responsible for reducing the noise generated in the resistor R_1 which corresponds to the resistor value denoted earlier as R. In the case of the second resistor, R_2, the noise voltage contribution from R_2 combines directly with the noise voltage perturbations applied to the VCO as evidenced by Fig. 6.4b. This implies that unnecessarily large values of R_2 should be avoided in order to keep the phase noise to contribution to a minimum. On the other hand, the value of R_2 must be made sufficiently

high to present an approximate open circuit to the VCO resonant tank circuit and filter output.

The transfer function of the output phase versus the control voltage must be determined in order to relate the noise generated in the loop filter to the output phase

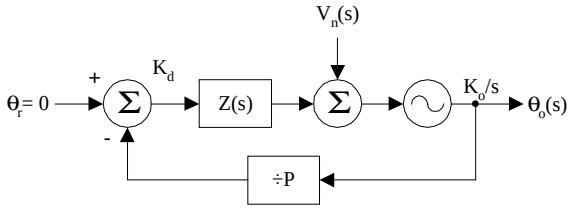


Figure 6.5. Addition of loop filter noise.

noise. With the aid of Fig. 6.5, this relationship is determined generally as

$$\frac{\theta_o(s)}{V_n(s)} = \frac{K_o}{s + \frac{K_o K_d}{P} Z(s)} \tag{6.9a}$$

and specifically for the second order filter as

$$\frac{\theta_o(s)}{V_n(s)} = \frac{K_o s(C_1 + C_2)\left(s\frac{RC_1C_2}{C_1+C_2} + 1\right)}{s^2(C_1 + C_2)\left(s\frac{RC_1C_2}{C_1+C_2} + 1\right) + \frac{K_o K_d}{P}(RC_2 s + 1)} \tag{6.9b}$$

6.5 Other Sources

Both the prescaler and phase detector devices have internal noise mechanisms associated with them as well. Because of their position in the PLL structure, as depicted in Fig. 6.6, these noise sources can be lumped into the overall noise associated with the reference oscillator. At relatively close offset frequencies this is not a bad estimate since

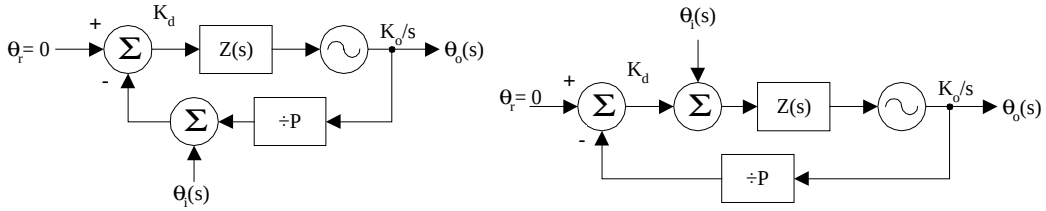


Figure 6.6. Prescaler and phase detector noise sources.

the phase noise of the reference oscillator should dominate over these two other sources. Additionally, measurements of the phase noise contributed by discrete dividers has been shown to be on the same order or less than that of a typical crystal oscillator.

6.6 Overall PLL Phase Noise

The previous sections have provided some indication of the contributions of each of the noise sources to the PLL output phase noise. The present focus will be on identifying the dominant contributors to the PLL phase noise versus frequency. Focusing on Eq. 6.6b, as $s \rightarrow \infty$, the transfer function quickly approaches unity; however, as $s \rightarrow 0$, the transfer function becomes

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{s^2(C_1 + C_2)}{s^2(C_1 + C_2) + \frac{K_o K_d}{P}(RC_2 s + 1)} \tag{6.10}$$

which bears a striking resemblance to a second order high pass filter transfer function with cut-off frequency given by

$$\omega_c = \sqrt{\frac{K_o K_d}{P(C_1 + C_2)}} = \omega_n \tag{6.11}$$

which is also the natural frequency of the loop. Using similar reasoning, (6.5b) reduces to

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{K_o K_d}{s^2(C_1 + C_2) + \frac{K_o K_d}{P}} \tag{6.12}$$

which is the equation for a second order low pass filter with cutoff frequency equal to ω_n. The reference oscillator transfer function differs slightly from that of the VCO as it does not approach the behavior of a second order filter until $s < (RC_2)^{-1}$ whereas the VCO only requires $s < [R(C_1 \| C_2)]^{-1}$. Additionally, letting s go to zero, the transfer function of the reference oscillator phase noise approaches the value P, implying the phase noise appearing at the VCO for very close frequency offsets is approximately P times the reference oscillator phase noise. Because very low phase noise sources are used as reference oscillators (e.g. crystal controlled oscillators), sacrifices in resonator Q of the VCO may be made for tuning range. The ratio of the VCO to the reference oscillator phase noise should be greater than the prescaler value expressed in decibels ($20 \cdot \log_{10}(P)$) to minimize its contribution over this range.

To illustrate these effects, the parameters of the RF2905 PLL with a 9 kHz bandwidth used for the fractional-N synthesis method of the next chapter were used to plot the magnitude of the noise transfer functions under consideration. The phase detector and

VCO gains were 6.366 μA/rad and 126 Mrad/s/V respectively with a prescaler division ratio of 128. The loop filter capactiors were 1000 pF and 0.01 μF for C_1 and C_2 while the resistor values were 10 kΩ and 4.2 kΩ for R_1 and R_2 respectively. The transfer functions

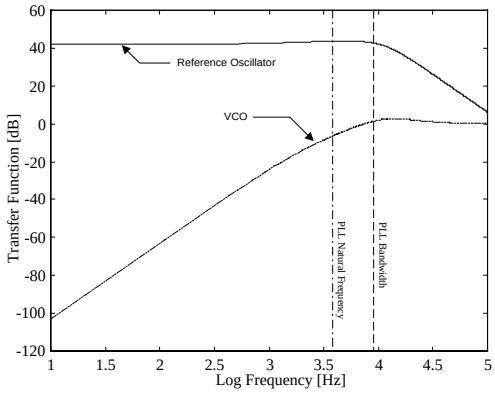


Figure 6.7. Transfer functions for VCO and reference oscillator phase noise.

for the reference oscillator RMS phase noise and VCO RMS phase noise contributions appear in Fig. 6.7. From Fig. 6.7, it is clear that the influence of the additional zeros in the VCO transfer function have the effect of shifting the cutoff frequency to the PLL bandwidth, which intuitively makes sense since the PLL bandwidth

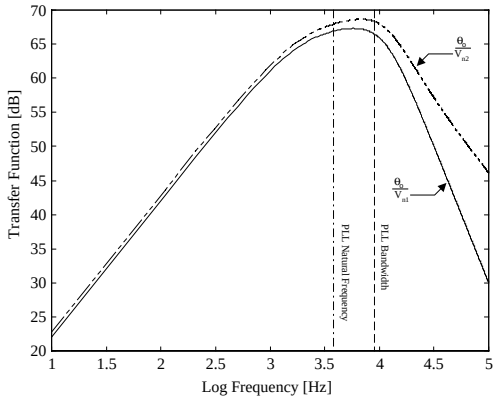


Figure 6.8. Noise contributions of loop filter resistors.

is supposed to be the limit on the loop ability to track perturbations. The transfer functions for the noise generated by the loop filter resistors appear in Fig. 6.8. At first glance, the resistor noise plot would appear to suggest that the contribution from the filter resistors is the dominant one. Because the RMS thermal noise voltage contributed by the resistors is extremely small, the only region where the resistors significantly contribute to the PLL output noise is near the PLL bandwidth. This contribution often results in a

small peaking of the single-sideband noise of the PLL as depicted in Fig. 6.9. The peaking illustrated was the result of changing the 4.2 kΩ varactor bias resistor (R_2) with a

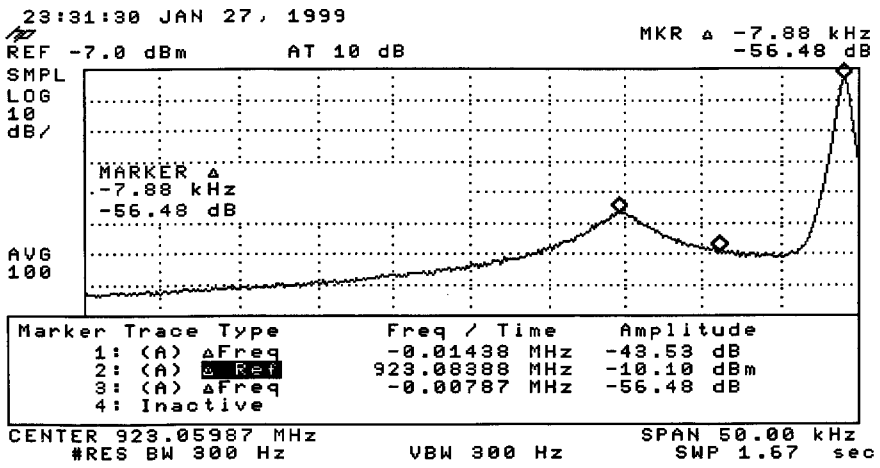


Figure 6.9. Illustration of phase noise peaking due to high loop filter resistor value.

100 kΩ resistor. The flat region between the noise peak (left) and the oscillator signal (right) represents the internal PLL noise. Because this measurement was taken with a resolution bandwidth of 300 Hz the actual noise density is -80.7 dBc/Hz (-56 dB - 10•$\log_{10}$(300)). The flat region arises due to the reference oscillator phase noise density decreasing below the mostly thermal noise contributors in the loop whose phase noise density functions are relatively flat.

In the chapter to follow, external influences on the phase noise performance of the VCO will be introduced that many individuals typically disregard, along with measured noise performance. Additionally, the transfer functions developed in this chapter for random noise variations will be found useful for small signal modulations and an understanding of the mechanisms responsible for the generation of the fractional-N base-frequency spurs.

7. Modifying the RF2905 PLL for Fractional-N Frequency Synthesis

7.0 Chapter Overview

The standard implementation of the RF2905 phase-locked loop (PLL) uses the dual modulus prescaler in its fixed division mode. With a single reference oscillator, the value of the prescaler is selected to be either P or P+1 (64/128 or 65/129) implying that only two channels over the entire band can be used. This limitation has the potential of becoming a problem if another radio system happens to use the same channels in the future. Through the technique of fractional-N frequency synthesis, the PLL output frequency can be made a non-integer multiple of the reference frequency. The value of the fractional portion of this non-integer division ratio can be programmed on the fly and the numerator and denominator can be altered to some extent to control the resolution of channelization.

There are several disadvantages to using fractional-N systems namely an increase in spurious signal generation and a potential for increased phase noise, not to mention the increased complexity of the overall system. There is also an increased emphasis on the performance of the loop filter outside the bandwidth of the PLL to ensure sufficient spurious signal rejection. Fractional-N synthesis may also introduce further complications resulting from FCC regulations (Part 15.209 [25]) for the ISM bands which require harmonic and spurious signals to be at least 50 dB below the carrier.

The RF2915 and RF2945 are versions of the RF2905 specifically designed to interface to a commercial PLL frequency synthesis integrated circuit (IC). Though recently fractional-N synthesizer chips have become available, most manufacturers have been supplying ICs which implement a frequency synthesizer using a high speed prescaler and several lower speed counters in a single chip. The method implemented in these ICs was augmented slightly to result in a new simple method of achieving a fractional-N frequency synthesis that will work with the RF2905 and RF2925 with a minimum of additional components. In the following sections, the techniques of swallow-counter

frequency synthesis as employed in commercial PLL ICs and two forms of fractional-N synthesis will be presented along with their advantages and disadvantages.

7.1 Standard Frequency Synthesis with a Swallow Counter

Before discussing fractional-N synthesis, the related technique of PLL frequency synthesis utilizing a swallow counter will be discussed as a way to introduce the concepts involved. This method of frequency synthesis provides the advantage of using a single high speed, dual modulus prescaler(with division ratio selectable to be either P or P+1), followed by a slower CMOS or TTL counter whose output connects to the phase detector. The structure of the frequency synthesizer is depicted in Fig. 7.1. The dual modulus prescaler of the RF2905 is basically two counters in parallel whose division ratio varies by one (for example ÷2/÷3) followed by a single fixed length counter (÷64). The swallow enable control allows the higher value counter (÷3) to reach its full count once and advance the fixed counter from a 0 to 1. Once this occurs the lower value counter (÷2) is used to clock the fixed divider until the fixed counter reaches its full count (63). The process repeats until the swallow enable is set to logic low. The net effect of activating the swallow enable control is to increase the prescaler divide ratio from its base value P, to P+1 by "swallowing" one VCO pulse.

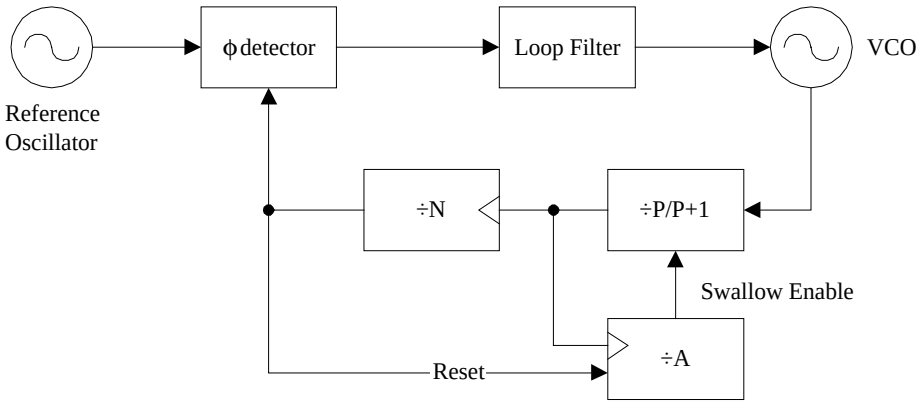


Figure 7.1. Block diagram of PLL swallow counter frequency synthesizer.

An additional counter clocked by the prescaler output (here referred to as the A counter) is added to the PLL structure to provide the required enable control signal for the swallow counter. The low speed counter connecting the output of the prescaler to the

phase detector (here referred to as the N counter) must be programmed to any value greater than A. Otherwise, the prescaler division ratio will always be P+1. Initially, the prescaler's division ratio is P+1 as both counters begin counting down from their initial values. When the A counter reaches zero, it is disabled and the prescaler division ratio changes to P. The N counter continues to count down. Once the N counter reaches zero, both counters are reloaded with their initial values, and the process is repeated.

The operation of the swallow counter frequency synthesizer can be compared to a weighted averaging process. The average frequency appearing at the output of the N counter is the sum of A prescaler output cycles, counted with a division ratio of P+1, and N-A cycles, counted with a division ratio of P, averaged over one reference cycle. In this case, the average reduces to a simple sum; however, the fractional-N synthesis methods average the divider output frequency over more than one reference cycle making the concept of the frequency average an important one. Performing the sum indicated previously, the resulting relationship between the reference oscillator frequency and the VCO frequency is given by,

$$f_o = f_{ref} \bullet (N \bullet P + A) \tag{7.1}$$

The equation above shows that selecting the values of A and N involves a potentially hidden consideration. Since the maximum value of the A counter should be at least equal to the number of channels required, the N counter must be at least one plus this number. The reference frequency required for a small frequency step size using this method must be very low raising problems associated with PLL lock time and reference spur suppression. Additionally, many of the commercially available PLL IC's use a higher frequency oscillator connected to a frequency divider as the reference source applied to the phase detector. In effect, this scheme still utilizes a low frequency reference, but it also provides some minor advantages in terms of phase noise performance.

7.2 Standard Fractional-N Synthesis

Standard fractional-N frequency synthesis extends the technique described above to generate output frequencies at non-integer multiples of the reference oscillator frequency. The traditional architecture of the fractional-N PLL synthesizer is illustrated in Fig. 7.2.

The structure of the loop is similar to the frequency synthesis using a swallow counter method previously discussed with a few significant changes. The value of the prescaler division ratio, P, is externally programmable to provide the coarse tuning of the frequency synthesizer (integer steps of the reference oscillator frequency). The division ratio of the loop is also programmable in non-integer steps of the reference oscillator frequency by programming the accumulator block.

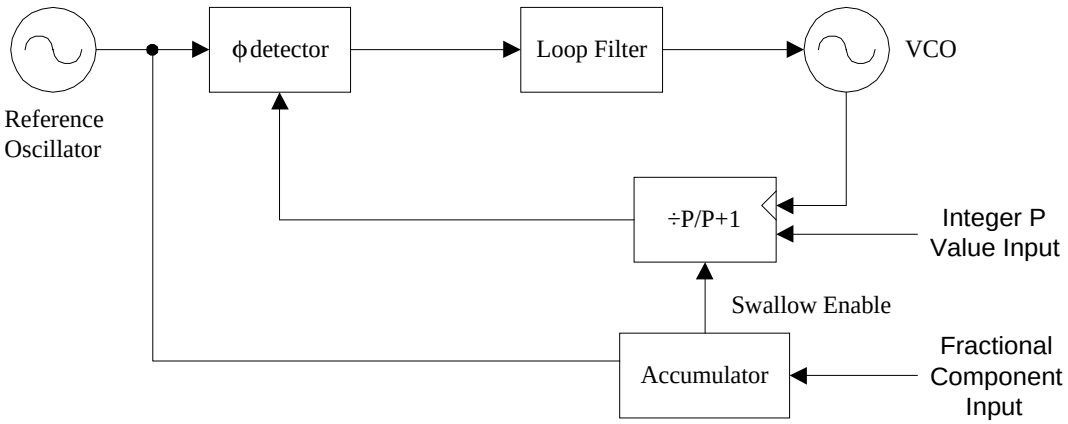


Figure 7.2. Standard fractional-N frequency synthesizer without phase compensation.

To understand how the fractional tuning is achieved, the operation of the accumulator must be described in detail. The accumulator consists of a multi-stage, fixed-length, binary adder and two registers as illustrated in Fig. 7.3. One register is programmed with a binary number related to the fractional portion of the relationship between the reference

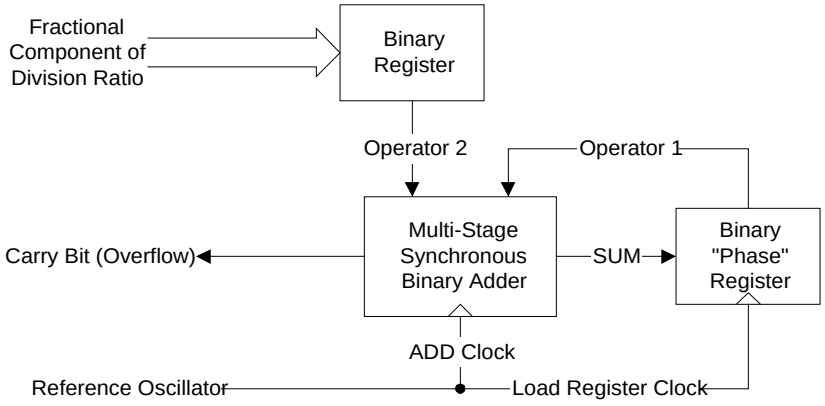


Figure 7.3. Conceptual drawing of accumulator block.

frequency and the output frequency. The binary number contained in the register is added to the contents of other binary "phase" register. The result of the binary addition is then stored in the binary phase register. The circuit arrangement essentially creates a counter whose count increment is programmable instead of fixed at unity. The carry output (also termed the "overflow" output) of the adder controls when the division ratio is changed from P to P+1. Since the accumulator advances every reference cycle, the prescaler division ratio is only P+1 for one reference cycle. If the value contained in the binary register (operator 2) is denoted A, and the minimum sum that causes the adder to overflow is N, then a carry will occur every N/A reference oscillator cycles. For example, if A were 1 and N were 10, it would take exactly ten reference cycles for the accumulator to generate a carry. After N reference oscillator cycles A pulses of the VCO will have been divided by P+1 and N-A pulses will have been divided by P. Thus, the VCO frequency maintains an integer relationship with the reference oscillator frequency divided by N, which for lack of a better name shall be termed the base frequency. The relationship between the VCO frequency and the base frequency is then the same as that given in Eq. 7.1, with the exception that the reference frequency must be replaced by the base frequency. The expression can then be rewritten to describe the relationship between the reference frequency and the VCO frequency as,

$$f_o = (f_{ref} \div N) \bullet (N \bullet P + A) \tag{7.2}$$

As a result of the integer relationship between the base frequency and the VCO frequency, spurious signals appear at offsets that are integer multiples of the base frequency from the VCO frequency. Further discussion of the FM mechanism responsible for generating these spurs and methods for reducing their amplitude is left to a later section. At the moment, it is important to recognize that the advantage the standard fractional-N method is the use of a higher reference frequency. The higher reference causes the reference spurs associated with the charge pump current spikes to be higher in frequency, easing the requirements on the filtering required to reduce their effect. Additionally, the higher reference frequency implies a faster acquisition than could be afforded with a very low frequency reference. Finally, the lower overall division

ratio means a lower reference oscillator phase noise contribution will be present on the VCO signal.

7.3 Simple Fractional -N Synthesis

Simple fractional-N synthesis is a related way of achieving the same advantages of the standard fractional-N synthesis, but using a simpler, easily scaled circuit. Originally published in a short paper in the IEEE MTT [8], this method appears to have received little attention since. The architecture of the synthesizer is closely related to the frequency synthesizer utilizing a swallow counter except that the prescaler is directly connected to the input of the phase detector. The A and N counter still perform the function of controlling the division ratio of the prescaler and the N counter still acts as the reset mechanism for the A counter. The block diagram of the simple fractional-N synthesis method appears in Fig. 7.4.

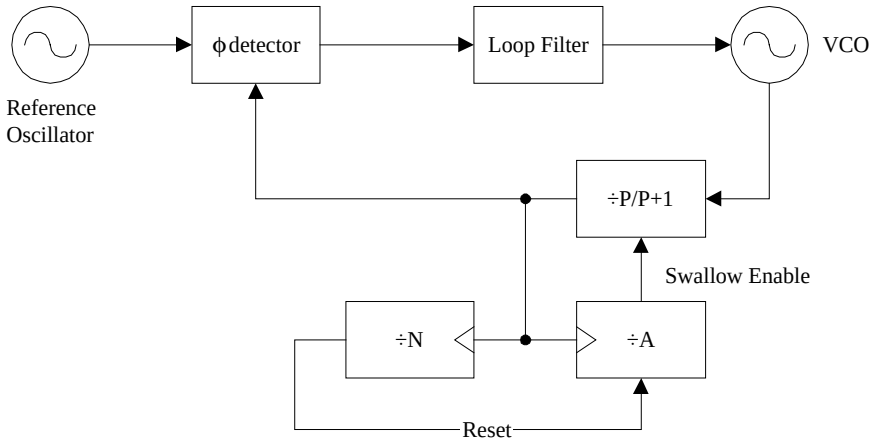


Figure 7.4. Block diagram of the simple fractional-N synthesis method.

Similar in appearance and operation to the swallow counter frequency synthesis technique, the relationship between the A counter, N counter, reference frequency, and the VCO output frequency is more reminiscent of the standard fractional-N technique. Returning to the case of the swallow counter synthesis, the total period of the process of dividing by P and P+1 was required to take only one cycle of the reference oscillator. With the simple fractional-N method, the process repeats every N reference oscillator cycles which was the case with the standard method of fractional-N synthesis. Adjusting

the equation for the swallow counter synthesis method to reflect the increased number of reference oscillator periods, the equation for the simple method becomes,

$$f_o = f_{ref} \bullet (P + A / N) \tag{7.3}$$

which is identical to Eq. 7.2 for the standard fractional-N method. The true advantage of simple fractional-N is the simplicity of the circuit which can be realized with economical TTL / CMOS counters. This method is especially useful for the RF2905 which possesses all the necessary components for fractional-N except for the additional counter. Since external PLL IC's are typically greater than the cost of the transceiver itself, the simple fractional-N method provides the functionality of a programmable synthesizer without the associated cost. Additionally, most PLL IC's contain additional registers which can only be serially programmed, adding a complication not present in the simple fractional-N method. One disadvantage of the simple method is the potential for increased spurious signal amplitude which is left as the focus in a later discussion.

7.3.1 Simple Fractional-N CMOS/TTL Implementation

The external circuit connected to the RF2905 evaluation board for the purpose of demonstrating the simple fractional-N concept is illustrated in Fig. 7.5. TTL discrete logic circuits were used in the laboratory due to their immediate availability and the lack of constraints on power consumption. In practice, low power CMOS equivalent components would replace these circuits, but the functionality of the circuit would not change significantly. Because the TTL 74LS163 counters are a count up only type counter, the counters are loaded with the complement of the value they would normally count, correcting for the direction of the count. Also, because there is a built in delay of one count required to load the counters, the actual value of the N counter is one plus the value programmed, or effectively (N+1).

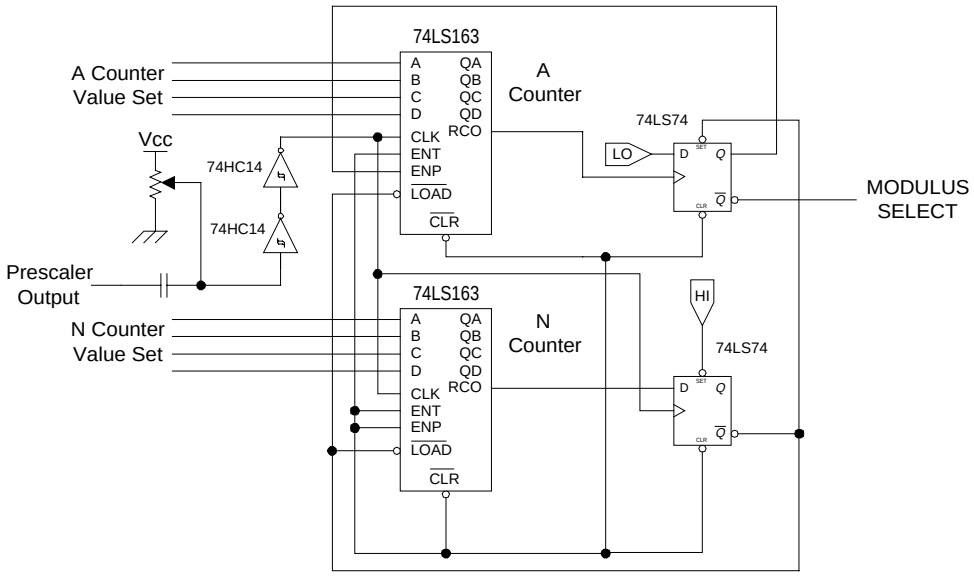


Figure 7.5. Schematic of TTL realization of Fractional-N counters.

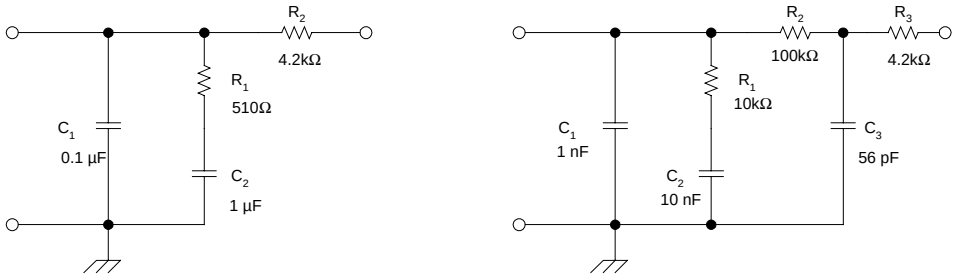
Interfacing to the prescaler proved to be a cumbersome task. The current sourcing capability of the prescaler output port is limited to such an extent that AC coupling into a high impedance was required to preserve the peak-to-peak voltage swing of the output. After AC coupling, the output was DC offset with a potentiometer and connected to the input of a 74HC14 HCMOS schmidt trigger inverter whose output connected to another inverter. The addition of the 74HC14 gates provided the necessary buffering to clock the counters and the flip flop. The TTL counter circuits were located on an additional circuit board which fastened to the RF2905 evaluation board using standoffs. The output labeled MODULUS SELECT was connected to the modulus control pin of the RF2905 via a twisted pair of wires with one wire carrying the control signal and the other wire connected to ground. Although not immediately apparent, the wire inductance introduced by the twisted pair caused the voltage transitions at the modulus control pin to overshoot and ring occasionally resulting in damage to the control input. To remedy this problem, two 1N4148 small signal diodes were added to the evaluation board connecting the power supply and ground to the modulus section pin in a reverse biased manner. When the voltage began to overshoot the level of the power supply or undershoot the board ground potential, one of the diodes would become forward biased and effectively clamp the voltage to within 0.7 V of either the power supply or ground.

Two PLL loop filters were used for the measurements of the implementation. The first was a third order PLL with a bandwidth of 460 Hz, while the second was a fourth order PLL with a bandwidth of approximately 9 kHz. The relevant parameters of the two PLLs are summarized in Table 7.1. Both PLLs employed a second order loop filter used

Parameter	460 Hz Bandwidth	9 kHz Bandwidth
Ko	126 Mrad/s/V	126 Mrad/s/V
Kd	6.336 μA/rad	6.336 μA/rad
P/P+1	128/129	128/129
ω_n	2.38 krad/s	23.78 krad/s
ζ	0.606	1.19

Table 7.1: Experiment PLL parameters.

consisting of a shunt capacitor in parallel with a series resistor capacitor combination as illustrated in Fig. 7.6[1]. The components used for the PLL with a bandwidth of 460 Hz were C_1 = 0.1 μF, C_2 = 1 μF, and R_1 = 510 Ω, while for the 9 kHz bandwidth PLL were C_1 = 1 nF, C_2 = 10 nF, and R_1 = 10 kΩ. The 9 kHz PLL possessed an additional low pass, L network consisting of a 100 kΩ resistor and a 56 pF capacitor immediately following the loop filter. The control voltage was coupled to the VCO varactor (~3 pF) and fixed capacitor (~5 pF) tuning network via a 4.2 kΩ resistor for both PLLs. The primary motivation for using two PLL bandwidths was to first achieve satisfactory



a. **b.**

Figure 7.6. Illustration of loop filters for (a) 460 Hz PLL bandwidth and (b) 9 kHz PLL bandwidth.

[1] In practice, the second order loop filter acts as a first order filter in the theoretical analysis with the second pole primarily offering a rejection of spurious frequencies.

operation using the very narrow bandwidth of 460 Hz that would indicate the concept was sound. Then, adjustments in the bandwidth and the evaluation board circuit could be made to achieve a higher PLL bandwidth while still maintaining the same level of performance.

7.3.2 Measured Performance

Using an HP 8594E spectrum analyzer, the output spectra of the simple fractional-N implementation circuit was plotted. The spectra for the 460 Hz and 9 kHz PLL bandwidths appear in Fig 7.7 and Fig. 7.8 respectively. For both of these plots, the

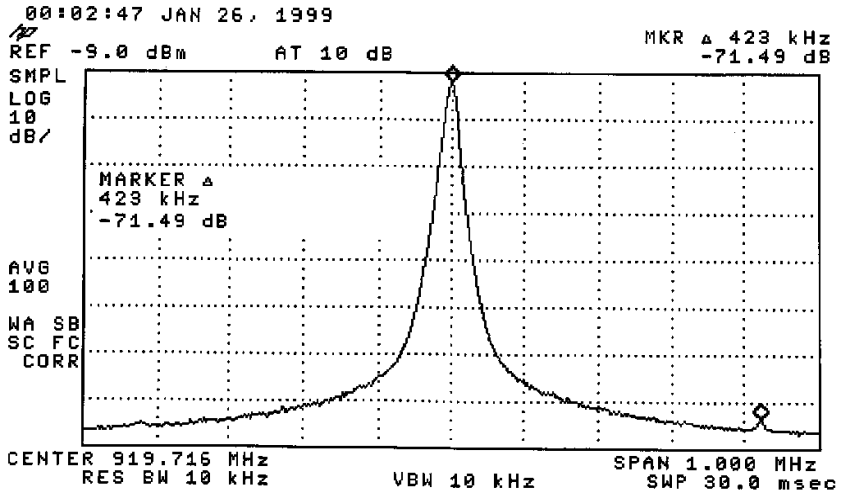


Figure 7.7. Output spectrum of implementation circuit with PLL bandwidth of 460 Hz.

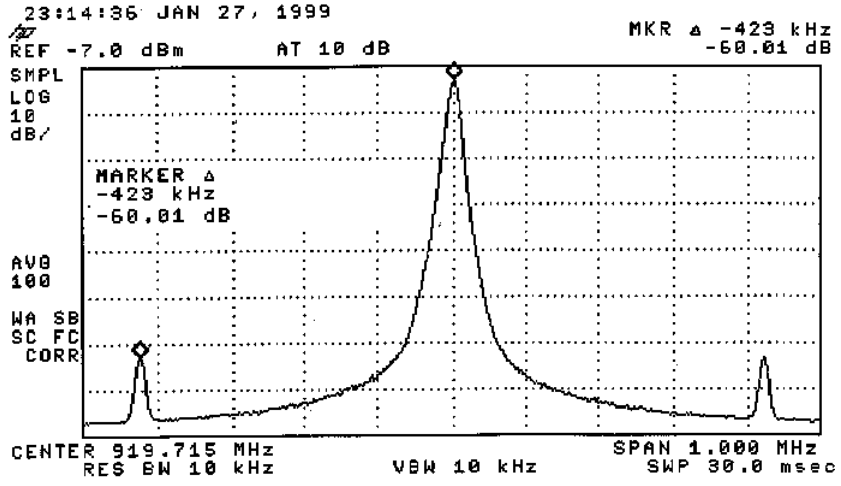


Figure 7.8. Output spectrum of implementation circuit with PLL bandwidth of 9 kHz.

A counter value is 8, the effective N counter value is 17, and the reference oscillator frequency (f_{ref}) is 7.16 MHz. Because each plot is only a 1 MHz span about the carrier, only the base frequency of 423 kHz (f_{ref} / (N+1)) spurs are shown. The small asymmetry in the amplitude of the base frequency spurs indicates the presence of either a low-level amplitude modulation or a second FM modulation on the output signal.

For reasons to be discussed shortly, the amplitude levels of the base frequency spurs are primarily dependent on the ratio of the A and N counter values. Measurements were made of the base frequency spur amplitudes for each value of A in the range of 1 to 15, while holding the effective value of N equal to 17. The measurements of the 9 kHz PLL bandwidth case are presented in Fig. 7.9. The difference between the maximum and minimum base frequency spur amplitudes is almost 10 dB. The same measurements of the system employing a PLL bandwidth equal to 460 Hz exhibit only a fraction of a decibel difference between the maximum and minimum amplitude of the base frequency spurs.

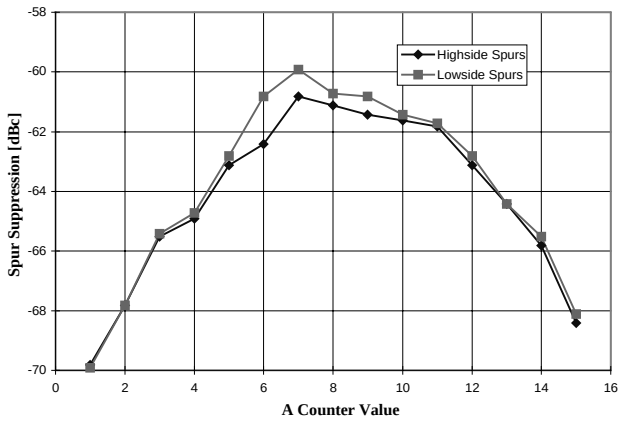


Figure 7.9. Graph of base frequency spur amplitude relative to the carrier vs. A counter value.

The phase noise sideband of the 9 kHz bandwidth PLL was examined to determine the effect of the value of the A counter on the single sideband phase noise. The measurements were performed using the spectrum analyzer set to a 12.5 kHz offset from the carrier, with a 25 kHz span. The video and resolution bandwidths were set to 300 Hz, and video averaging of 100 samples was used. The value of the A counter was set to 1, 8, and 15 and compared each time to the phase noise sideband of the PLL acting without the fractional-N modulus control signal connected (resulting in a fixed prescaler value). In

each case, there was no measurable change in the phase noise single sideband (SSB) level of –84.3 dBc / Hz at 7.5 kHz offset.

7.4 Spurious Signal Considerations

There are two primary sources of spurs generated by the fractional-N synthess technique. One set of spurs results from the operation of the charge-pump which causes a frequency modulation of the VCO at the frequency of the reference oscillator. The second is an FM mechanism operating at the base frequency of the synthesizer. These two distinct sets of spurs appear in the spectrum illustrated in Fig. 7.10. The narrowly spaced, low amplitude spurs correspond to the base frequency spurs, while the larger amplitude, farther offset spurs correspond to spurs at the reference oscillator frequency. To remain locked, the phase detector must make minor corrections to the loop filter voltage due to leakage and the effects of the phase detector "dead spot" near 0° phase error. These minor corrections to the loop filter voltage occur at the reference oscillator frequency which causes the VCO to be modulated in an FM manner.

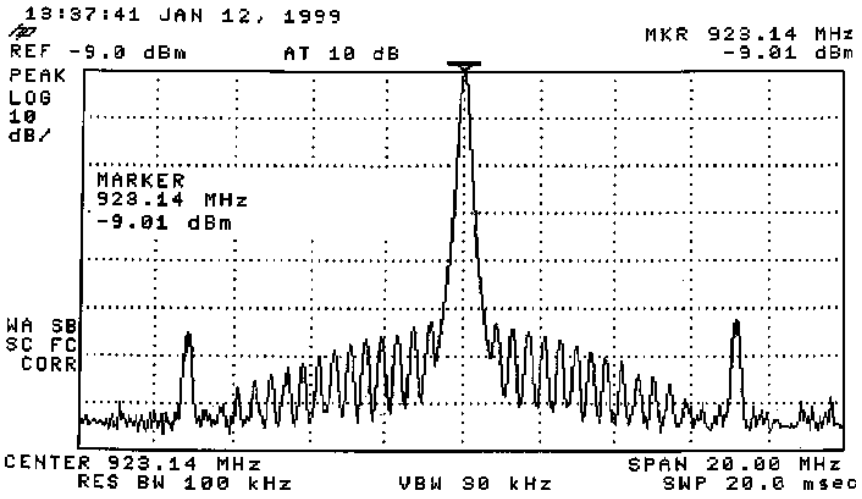


Figure 7.10. Illustration of two types of spurs resulting from fractional-N synthesis[2].

The base frequency spurs are associated with a different FM mechanism that results from the periodic change in the prescaler value at the base frequency. To a first order, the long-term, average VCO frequency can be assumed to be constant at a non-integer

[2] Base frequency spur amplitudes are artificially elevated for the purposes of illustration and do not represent the actual amplitudes under normal operating conditions (Fig. 7.6 & Fig. 7.7).

multiple of the reference oscillator frequency. The non-integer relationship between the reference oscillator and the VCO causes an incremental phase error to accumulate with each reference oscillator cycle. Each prescaler output pulse with the division ratio equal to P increases the phase error by $2\pi A/(N \bullet P+A)$ while a prescaler division ratio of P+1 decreases the phase error by $2\pi(A-N)/(N \bullet P+A)$. The width of the phase detector current pulses are directly proportional (K_d) to the magnitude of the phase error. It is the variation in the width of these pulses, that when integrated by the loop filter, gives rise to a small ramping waveform superimposed on the DC value of the VCO control voltage. Although there is a minor difference in the appearance of the triangular waves of the standard fractional-N and the simple fractional-N methods, as will be discussed shortly, the basic repetition frequency of the two triangular waveforms is equal to the base frequency of the synthesizer. It is the triangular wave that modulates the frequency of the VCO causing the base frequency spurs to appear in the output spectrum. Provided the phase error magnitude never exceeds 2π, which is the linear range of operation for the phase-frequency detector, the PLL does not slip a cycle and undergo the acquisition process. This condition clearly holds for N<P.

The difference between the triangular phase-error waveforms of the two fractional-N methods arises from the manner in which the P+1 prescaler division ratio is used during the total base frequency period of N / f_r . To achieve the same division ratio, both methods must divide the output frequency by P+1 a total of A times. The simple fractional-N approach uses the P+1 division ratio for A consecutive prescaler pulses, while the standard fractional-N approach distributes the division by P+1 over the entire base frequency period. The process of successively dividing by P+1 causes the incremental phase error of the simple fractional-N method to accumulate over a longer period and reach a larger peak value than the standard method. For the case of N = 8 and A = 3, the phase error ramping waveforms of the simple and standard fractional-N synthesis methods are illustrated in Fig. 7.11 and Fig. 7.12 respectively. It is important to note that these illustrations are both in the same scale suggesting that the standard method does have an inherent advantage in terms of spurious signal performance. The spurious performance of the two methods converges at the extremes of the fractional-N division

ratios since in each case either the P or P+1 division ratio is used only once over the base frequency cycle.

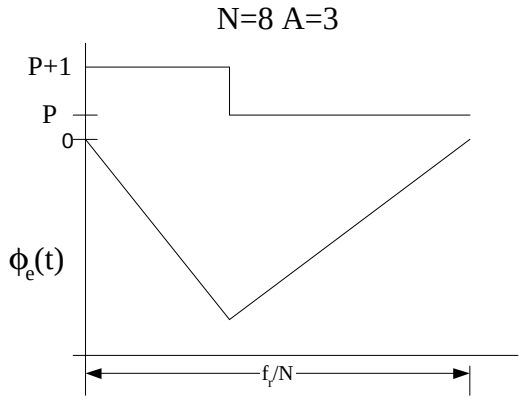


Figure 7.11. Illustration of phase error and prescaler value for simple fractional-N technique.

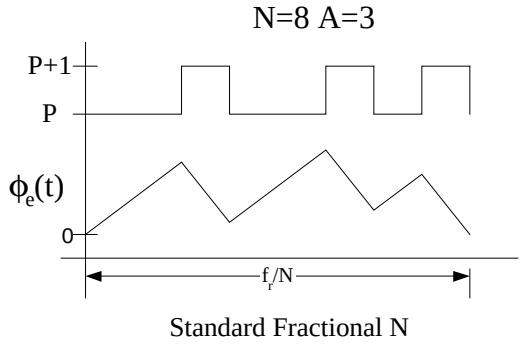


Figure 7.12. Illustration of phase error and prescaler value for standard fractional-N technique.

Returning to the measured behavior of the 9 kHz PLL bandwidth presented in Sec. 7.3.2, the maximum amplitude of the base frequency spurs occurs when the value of A is approximately one-half that of N. This trend is related to the incremental increase in the phase-error which is maximized for the case where A = ½ N. Additionally, the incremental increase is phase error is minimized for either of the extreme values of A (1 or 15 in this case) which agrees with the observable trend in the data for the 9 kHz case.

There is also evidence that suggests a source independent of the ramping phase error mechanism may be contributing to the base frequency spurs. The asymmetry in the spectrum analyzer plots of the fractional-N synthesizer performance seems to indicate the presence of a second signal at the base frequency that is either frequency modulating the

VCO or amplitude modulating the output signal. Amplitude measurements of the base frequency spurs generated by the 460 Hz PLL bandwidth setup have shown that the difference between the maximum and minimum spur amplitudes were a fraction of a decibel. The very low power residing in the base frequency spurs (-85 dBm) suggests that the contribution of a second source is dominating over the ramping phase error mechanism. Though the exact nature has yet to be determined, the second source could be attributed to limits on power supply filtering in addition to internal coupling within the RF2905.

Obtaining satisfactory spurious signal suppression from the implementation of the simple fractional-N synthesizer involved significant changes to the power supply filtering provided on the RF2905 evaluation board. The filtering provided on the RF2905 evaluation board is an L network of resistor and capacitors in a low pass configuration. Each of these individual filters is then connected to a common power supply connection. Because the logic circuits are clocked by the prescaler, all of the logic circuits transition at approximately the same time. The TTL logic circuits all require their maximum current when an output transition occurs (the same is the case for CMOS logic circuits). Small perturbations of the power supply voltage could result due to the cyclical increasing and decreasing logic current consumption at the base frequency. Since the reverse bias voltage of the VCO varactor diodes is developed directly from the power supply connection to the VCO, these perturbations would ultimately cause the VCO output frequency to be modulated at the base frequency.

Instead of the tree structured power supply filtering realized on the evaluation board, a ladder structure would improve the filtering of the power supply to especially sensitive sections of the synthesizer (e.g. the VCO resonator connections). Another way to reduce the spurious signals generated by the power supply is to reduce the VCO gain constant, since it directly controls the modulation index for all the sources of spurious signals. Reducing the VCO gain constant also provides the added benefit of improving the phase noise performance of the simple fractional-N PLL as well. Care must be taken in undertaking this change, since the stability of the PLL is directly dependent upon the VCO gain constant.

Depending on the application, it may prove necessary to reduce the amplitude of the base frequency spurs more than is possible through the simple methods mentioned above. A common method for removing the base frequency spurs in standard fractional-N synthesizers is by adding an external signal derived from the value of the accumulator to the output of the phase detector. This scheme is illustrated in Fig. 7.13. The value of the phase register is inverted and applied to a digital to analog converter (D/A) and added to the phase detector signal. The same arrangement could be applied to the simple fractional-N circuit using the output of the A and N counter to generate the correction voltage. In this case, the compensation might not be equal to the original phase ramp creating the possibility that compensation might in fact increase the base frequency spurs. One author has proposed an analog phase accumulator to achieve a closer matching compensation signal [26]. The phase noise of the synthesizer might be increased by the introduction of the external correction signal whether due to additional noise coupled into the signal, or smaller errors in synchronization and signal amplitude.

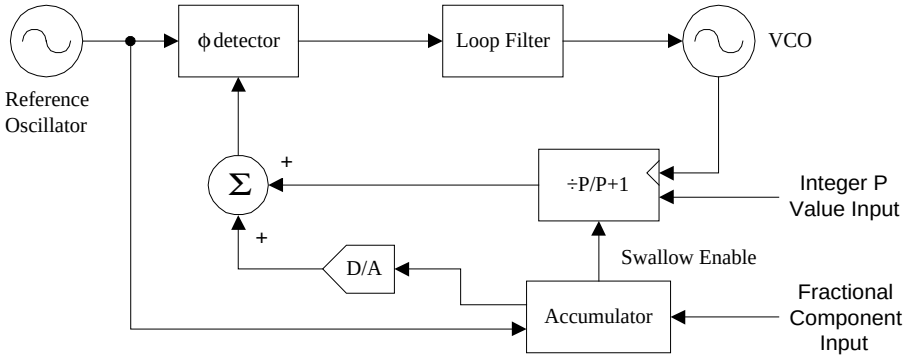


Figure 7.13. Fractional-N with spurious signal compensation.

Other techniques for reducing the base frequency spurs involve introducing a sample and hold circuit between the loop filter and the VCO or in the D/A of the compensation. Some advantages may be obtained through this method; however, since it is likely that a periodic gating signal will be used with the same-and-hold circuit introducing a spur at the gating frequency. Recently, a sigma-delta modulation scheme in the compensation has received some attention due to several advantages in both spurious signal reduction and phase noise shaping [9-11]. As a final thought, one way of reducing the base

frequency spurs would be to modulate the reference oscillator frequency with signal derived from the swallow enable signal. In standard a PLL, a step change of sufficiently short duration in the reference oscillator frequency results in ramping phase error at the phase detector. By providing the necessary scaling to the swallow enable signal of the simple fractional-N method, a suitable signal for modulating the reference oscillator might be obtained. The modulation of the reference oscillator frequency with this signal might cause the simple fractional-N PLL to generate a phase error ramp which is the complement of the fractional-N accumulating phase error.

7.5 Phase Noise Considerations

Phase noise refers to the noise sidebands that surround the output signal of the synthesizer. Discussed in greater detail in Ch. 6, the phase noise present at the output of a PLL frequency source is dominated by the contributions from the VCO and reference oscillator. For frequency offsets less than the bandwidth of the PLL, the output signal phase noise is approximately equal to the reference oscillator phase noise multiplied by the division ratio of the loop. As compared to frequency synthesis with a swallow counter, the phase noise performance of the simple fractional-N technique will be $20 \bullet \log_{10} N$ dB lower. With a prescaler value of 128 and a PLL bandwidth of 9 kHz, the SSB phase noise density of the RF2905 simple fractional-N synthesizer was measured to be -84.3 dBc / Hz at 7.5 kHz offset. Compared to a commercially produced frequency synthesizer IC (MC1415191), the SSB phase noise density of the RF2905 fractional-N circuit appears to be higher. In the case of the frequency synthesizer IC, the phase noise is lower due to a frequency divider located between the reference oscillator and the phase detector. The dividers typically possess division ratios high enough to cause the phase noise to be reduced to the inherent jitter of the divider. The ultimate limit on the output of the divider is -174 dBm / Hz (thermal noise) which is approached by the TTL dividers implemented in these frequency synthesizer integrated circuits. The phase noise density at the input of the RF2905 simple fractional-N circuit is –126 dBc / Hz at 7.5 kHz offset. To improve the performance of the RF2905 simple fractional-N synthesizer, an additional divider could be incorporated either one chip by the manufacturer or off chip by the designer. Realization of the off chip divider simply requires adding a standard

TTL counter and AC coupling the output signal of the divider to the OSC E pin of the RF2905 reference oscillator section. The simple fractional-N for the RF2905 still possesses the advantage of operating the phase detector at a higher frequency.

Although the phase noise of the RF2905 fractional-N synthesizer circuit should not be affected by changes in the value of the ratio of A to N, additional SSB phase noise measurements were made to verify this. The value of A was set to 1, 8, and 15 while maintaining the effective value of N equal to 17, and measurements of the SSB phase noise were made as described in Sec. 7.3.2. These measurements were compared to a measurement of the SSB phase noise made with the modulus control held low to provide a fixed prescaler value. All three cases exhibited nearly identical phase noise performance with at most a fraction of a decibel difference at offset frequencies ranging between 1 kHz s to 25 kHz. This result confirms the initial hypothesis that the phase noise of the simple fractional-N synthesizer is not dependent on the ratio of A to N.

Finally, the impact of power supply filtering on the fractional-N synthesizer phase noise performance was investigated as well. As suggested in Sec. 7.4, the switching noise associated with the TTL logic may modulate the VCO if sufficient power supply filtering is not provided. This switching noise is relatively wideband since the signals produced by the fractional-N logic circuitry operate at the reference frequency and below. Measurements of the SSB phase noise density at frequency offsets up to 50 kHz were made for two different power supply filter networks. The filter networks used were both single pole RC low pass filter networks using a resistor value of 10 Ω. The first set of power supply filter networks employed 0.1 µF capacitors only, while the second set employed 10 µF capacitors. The cutoff frequency of the networks using 10 µF capacitors is approximately 1.5 kHz while the cutoff frequency of the networks using 0.1 µF capacitors is approximately 15 kHz. The SSB phase noise density measurements illustrated in Fig. 7.14 indicate for the case of the 15 kHz cutoff frequency, the noise contributed by the power supply is the dominant contributor to the phase noise. Because the 1.5 kHz cutoff frequency is near the 460 Hz PLL bandwidth used for these measurements, the effect is not as dramatic in the illustration.

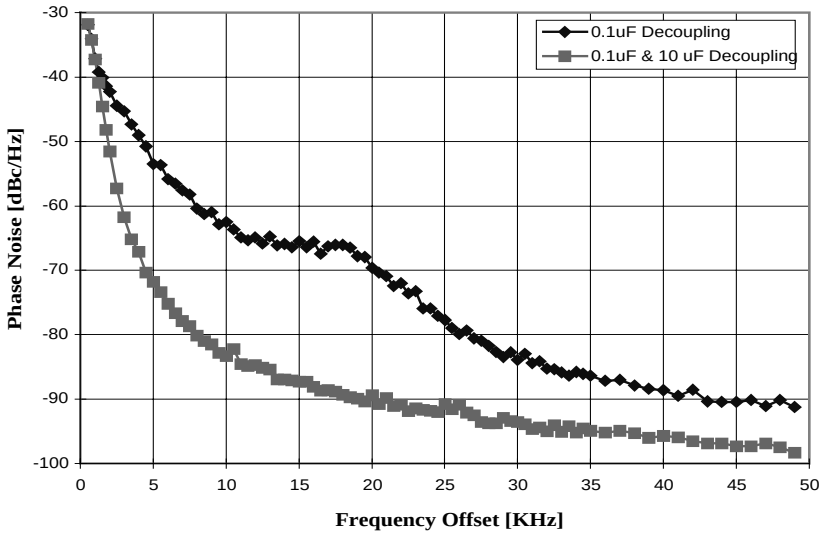


Figure 7.14. Effect of power supply filtering on output SSB phase noise.

Several aspects of the phase noise performance of the RF2905 fractional-N synthesizer circuit have been discussed. Methods for further improving the phase noise performance of the fractional-N synthesizer have been proposed, and the impact of insufficient power supply filtering was presented. Although the additional digital circuitry required for fractional-N synthesis can introduce an additional source of phase noise, good system design and sufficient filtering can reduce the contributions of this undesired noise source to a minimum.

8. Fractional-N System Considerations

8.0 Chapter Overview

Incorporating fractional-N frequency synthesis into the RF2905 transceiver circuit opens up new possibilities and considerations for the implementation of the transceiver. Without fractional-N synthesis, the typical implementation of the RF2905 makes use of only four channels of the 902-928 MHz North American industrial, scientific, and measurement (ISM) band. With fractional-N synthesis, the ISM band may be divided into enough channels allowing implementing the RF2905 transceiver to be a frequency-hopped spread spectrum (FHSS) system using FM/FSK modulation. Although fractional-N synthesis provides a greater flexibility in selecting the operating frequency, it also introduces new spurious signals (termed "base frequency" spurs) that may impact the quality of the received signal. Fractional-N synthesis also complicates the selection of phase-locked loop (PLL) filter topology and PLL bandwidth in order to comply with Federal Communications Commission (FCC) guidelines for spurious signal suppression and frequency hopping rate. This chapter will focus on the tradeoffs and considerations of implementing a transceiver using the fractional-N technique and the practicality of creating a FHSS transceiver using the RF2905.

8.1 Channelization

The minimum frequency step of the synthesizer is given by maximum occupied RF signal bandwidth. The signal bandwidth may be determined from Carson's rule using the maximum bit rate and deviation. The basic PLL of the RF2905 design is capable of generating only two frequencies corresponding to the integer values of the RF2905 dual modulus prescaler (P and P+1) multiplied by the reference oscillator frequency (f_r). Using the fractional-N technique, additional frequencies that lie between f_r • (P+1) and f_r • P can be generated. These frequencies are selected by loading counters referred to as the A and N counters with the appropriate values as developed in Ch. 7. The A counter may be programmed with any value between 1 and N-1, while the N counter can be

loaded with any value up to its maximum count. The output frequency generated by the fractional-N synthesizer is given by,

$$f_o = f_r\left(P + \tfrac{A}{N}\right) \tag{8.1}$$

Since each possible value of the A counter corresponds to a different frequency, the fractional-N synthesizer can generate a total of N-1 channels. Unfortunately, the fractional-N method has base frequency spurs that appear at multiples of f_r / N offsets from the synthesizer output frequency due to an undesirable frequency modulation produced by the fractional-N method. Using the two frequencies that correspond to f_r • (P+1) and f_r • P eliminates most of the spurious problems, but provides only two channels. By proper design, the spurious responses of the fractional-N method can be made sufficiently small for acceptable use.

The RF2905 provides two reference oscillators to allow one to be used when the transmitter is active and one to be used when the receiver is active. Provided the same value of N is used by both the transmitting unit and the receiving unit, the IF frequency for a low side injected arrangement will be given by,

$$\pm f_{IF} = (f_r)_{TX}\left(P + \frac{A_{TX}}{N}\right) - (f_r)_{RX}\left(P + \frac{A_{RX}}{N}\right) \tag{8.2}$$

where $(f_r)_{TX}$ and $(f_r)_{RX}$ are the reference oscillator frequencies for the transmitter and receiver respectively and A_{TX} and A_{RX} are the values programmed into the A counter of the transmitter and receiver respectively. Eq. 8.2 suggests that in order to use the same IF frequency typically implemented with the manufacturer's evaluation board (10.7 MHz) either the difference between the transmitter and receiver reference oscillator frequencies must be changed to account for different values of A_{TX} and A_{RX}.

8.2 FM/FSK Demodulation

Because both the transmitter and receiver must utilize the fractional-N technique to successfully communicate, the base frequency spurs produced by the fractional-N technique will influence demodulation. The fractional-N frequency synthesizer output signal has frequency modulation spurious signals at the base frequency. The incoming IF signal will have similar spurious modulation at the base frequency. This base frequency

FM is present at a low level on the intermediate frequency (IF) signal and is amplified with the desired signal by the IF amplifiers. Because the spurs are an FM phenomenon, the limiting behavior of the IF has little effect on them before they are presented to the quadrature detector. The IF filters provide the necessary mechanism to reduce these spurs, provided the spurs lie outside the IF bandwidth. One might assume that for systems employing higher IF bandwidths that these spurs are not attenuated. It must be noted that for a system with higher bandwidth IF, the occupied RF bandwidth of the signal is larger and the value of N is small increasing the offset of the base frequency spurs and causing their amplitude to decrease proportionally.

The low level FM modulation on the IF carrier is demodulated by the quadrature detector to result in a low level sinusoidal output. As long as the FM deviation afforded by the modulation varactors of the transmitter is greater than the deviation associated with the PLL base-frequency FM feedthrough, the base frequency spurs do not impact the performance of schemes using the data output of the RF2905. A multilevel FSK system will be more sensitive to this additional interference since the detector output voltage thresholds separating one received symbol from another are closer together. To achieve an acceptable level of spurious performance, the sampling timing of a receive analog to digital (A/D) converter may be set to occur at the same period of the demodulated base frequency sinusoid. By periodically sampling the output signal at integer multiples of the base frequency period, the effect of the variation on the demodulated signal will be minimized without the need for additional filtering.

8.3 Frequency Hopped Spread Spectrum

The considerations and tradeoffs discussed until now can be applied to transceivers using the fractional-N synthesis technique to provide more channels for transmission as well as frequency hopped spread spectrum (FHSS) transmissions. The former application does not have any acquisition time requirements, allowing a great deal of flexibility in choosing PLL bandwidths to provide the level of the base frequency spurs required for FCC compliance. For the FHSS systems, there are limitations on the smallest PLL bandwidth usable due to the maximum dwell time at any one frequency as specified by

the FCC. Additionally, the frequency hopping pattern must be random in nature. This randomness implies that the fractional-N synthesizer may be required to hop from one end of its operating range to the other in less than the dwell time, possibly requiring an even wider PLL bandwidth to meet the requirement.

In order to be compliant with FCC Part 15.249 guidelines, a frequency hopping communication device must be able to hop pseudo-randomly among 25 channels of width[2] 250 KHz to 500 KHz, or 50 channels of width less than 250 KHz, and not remain on any one frequency longer than 400 ms. Within the context of the fractional-N presented previously for the RF2905, the latter case requires the N counter to have its full count minimum value equal to 49. Because of the relatively large value of N, the 64/65 division ratio of the prescaler is desirable to force the base frequency spurs to be farther from the output frequency. To occupy the ISM 902-928 MHz band, this requires a minimum transmit reference oscillator frequency of 14.0938 MHz. Using a reference oscillator very near this frequency will result in base frequency spurs at 290 KHz offset from the transmit frequency. The FCC Part 15.209 requires that all spurious signals be suppressed to a level of -50 dBc or lower relative to the carrier power in order to be in compliance. This level should be achievable without additional costly phase compensation since the 9 KHz PLL bandwidth presented in Ch. 7 achieved better than this level of performance. Additionally, the 9 KHz PLL bandwidth implementation should possess a short enough lock time to satisfy the FCC dwell time requirements. Thus, it is possible to build a fractional-N synthesizer using the RF29X5 transceivers and inexpensive logic circuits meeting the FCC requirements to transmit at power levels up to +30 dBm.

[2] Where the channel width is defined to be the 20 dB bandwidth of the channel and the transmitted signal is not allowed to possess a bandwidth greater than the channel bandwidth

9. Conclusion

9.1 Summary

The work presented in this thesis has focused on extending the flexibility of the RF2905 transceiver RFIC via different implementations of the external circuit. As an introduction to the RF2905 and the RF29X5 family, the operation and implementation of each of the three main sections of the transceiver, namely the phase-locked loop (PLL) frequency source, transmitter, and receiver have been reviewed. The potential modification of the receiver to include a phase-locked discriminator (PLD) was discussed to a limited degree. As presented, the primary advantage of the PLD is the extended capture range over the idealized FM detector. This advantage comes at the cost of a rather complicated circuit structure which ultimately may not be practical due to the amount of supporting circuitry to realize a functional detector.

The PLL operation was found to place limits on the transmitter operation. The nonlinear effects of the transmitter power amplifier on amplitude linearity ultimately ruled out the possibility of simultaneous AM/FM transmission. Methods for overcoming the data rate limitation of the RF2905 were discussed. Simple economical methods for overcoming the low frequency limitation on the data rate have been proposed as well as a scheme for implementing a multilevel FSK(frequency shift keying). The impact of implementing the multilevel FSK scheme on both the symbol error probability and external circuit of the transceiver was discussed. An approximate expression for the acquisition time of the PLL utilizing a phase-frequency detector was also developed.

The key functional blocks of the RF2905 PLL were found to be the oscillators. The oscillators were analyzed and proposed improvements for operation presented. A general three terminal model of the oscillator incorporating the nonlinear limiting mechanism of the active device (single BJT and the differential pair) was used. Methods for varying the frequency of the oscillators and their respective tuning mechanisms were also discussed. The commonly used model for analyzing noise in such oscillators has been introduced and its validity examined. The noise contributions from the reference oscillator, VCO,

and other PLL components to the noise at the output of the PLL were evaluated and the combined effect on the output spectrum determined.

The manufacturer's suggested method of implementing a frequency synthesizer (frequency synthesis with a swallow counter) with the RF2905 has been discussed and compared to a simple method for realizing a fractional-N PLL synthesizer using the internal components of the RF2905. The operation of the simple fractional-N synthesizer was likened to the standard approach used by Hewlett Packard (HP) and several integrated circuit manufacturers now supplying fractional-N integrated circuits. The effect of both fractional-N synthesis approaches on spurious signals and phase noise appearing in the output spectrum were compared. Finally, implementation considerations and tradeoffs of the simple fractional-N synthesis approach into the RF2905 transceiver design were addressed, leading to at least one possible set of design parameters for an economical fractional-N transceiver that complies with FCC Part 15 regulations.

9.2 Conclusions

Using the results of this research, an array of end product transceiver radios could be constructed with new features. The simplest implementation might resemble the manufactured evaluation board circuit with only a few modifications to enhance performance. At the opposite extreme, the radio might employ a fractional-N synthesizer to realize a frequency-hopped spread -spectrum (FHSS) transceiver using a multilevel FSK modulation format. Thus, the work presented has opened new possibilities for implementation which might have otherwise been overlooked, or been considered prohibitively difficult or complex to be worth pursuing. Most importantly, an inexpensive simple fractional-N frequency synthesis method was developed which may be applied to the RF2905 as well as several other devices as an alternative to swallow-counter frequency synthesis. Finally, the explanations concerning the operation of the RF2905 components provide the manufacturer with information to better acquaint customers with the RF29X5 family of RFICs and their true capabilities.

9.3 Recommendations

The phase noise of the RF2905 VCO could be improved by allowing the VCO transistors to be linearly biased. This bias arrangement could be provided by simply connecting the bases of the transistors to two additional pins. These pins could be connected to the opposite collectors by the designer for applications where the phase noise performance is not critical; however, they could also be connected to a tapped capacitor arrangement as in the case of the linearly biased balanced pair oscillator. In providing this type of arrangement, the capabilities of the transceiver are increased without a significant change to the structure.

The additional flexibility of the fractional-N method raises the question of whether the additional counters required to realize the method should be incorporated into either an accompanying IC or into a more flexible version of the RF2905. Compensation for the fractional-N phase ramp may be incorporated to reduce the spurious signals present at the output of the loop. The fractional-N synthesis especially attractive for IC implementation, providing all the necessary components to realize the synthesizer except the loop filter.

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APPENDIX A. Introduction to the Phase-Locked Loop

A.0 Introduction to PLL

Within the context of the RF2905, the phase locked loop (PLL) acts as the local oscillator for the receiver and a combination of frequency source and modulator for the transmitter. The PLL itself is a special form of control system whose control variables are the phase and frequency of the VCO and reference oscillator outputs. The basic structure of the PLL is diagrammed in Fig. A.1.

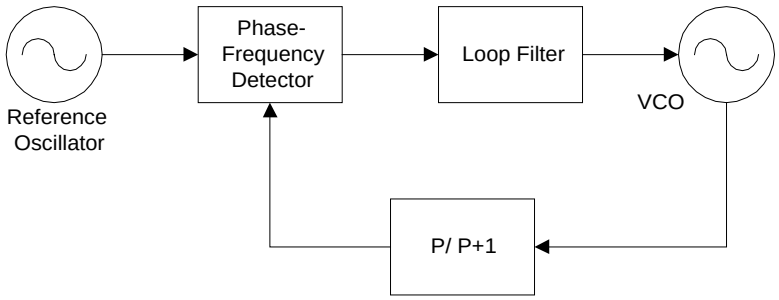

Figure A.1. PLL block diagram.

The phase detector is a nonlinear device which acts upon the time domain signals of the reference oscillator and the prescaler output to produce a DC signal whose value is proportional to the phase, and consequently, the frequency difference of the two input signals. In addition to the DC voltage, frequency components representing the interaction between the two input signals as well as harmonics of both are present and must be removed by the loop filter. The choices of the loop filter frequency response and gain distribution throughout the loop will inevitably determine the dynamics of the loop. It is often said that *ideally* only the DC term is passed through the filter, however, this focuses on the steady state performance of the loop and leads to misinterpretation of the loop filter's role. If the loop filter only allowed the DC term to be passed, then the loop would have no dynamic response at all. More than merely a means of rejecting unwanted harmonics, the loop filter plays a role along with the overall gain of the loop to control the rise and fall times that directly relate to the PLL's frequency response. The resulting low frequency output of the loop filter is applied to the VCO whose nominal frequency of oscillation is offset by the influence of the control voltage. The output of the VCO is fed

back to the prescaler which acts as a limiter and frequency divider. The prescaler's output is connected internally to the phase detector closing the loop.

Having developed an initial qualitative understanding of the PLL's operation, a description of the modeling of each of the functional blocks will be provided. These models in conjunction with the loop filter transfer function will be used to develop the open and closed loop transfer functions. Having obtained these transfer functions, the relevant aspects of the PLL operation including stability and acquisition will be discussed and suitable criterion for acceptable operation will be presented.

A.1 Overview of PLL Components

A.1.1 Phase Detector

The primary role of the phase detector within the PLL is to act as the point of negative feedback where the phase of the prescaler output signal is subtracted from the phase of the reference oscillator signal. For the reasons previously mentioned, a proportionality constant is also assigned to the phase detector. This proportionality constant represents the relationship between a steady state phase error between the two signals at the input of the phase detector and the DC component of the output of the phase detector and varies depending upon the type of detector in use. The classic phase detector as discussed partially in Sect. 3.2 , is the sinusoidal phase detector which is a balanced mixer. For most applications below 1 GHz, this type of phase detector has been replaced by the phase detector employed in the RF2905 PLL section, commonly referred to as the phase-frequency detector. One possible realization of this type of phase detector is depicted below (Fig. A.2a), with a diagram depicting the time domain input voltage waveforms and the ideal time domain output current waveform (Fig. A.2b). The fundamental operation of this type of phase detector can be described as measuring the time period between the rising edges of the input signals. From Fig. A.2b, it is clear that when the reference leads the other input, the output is a positive current source while the opposite condition results in the phase detector sinking current for the time duration between the

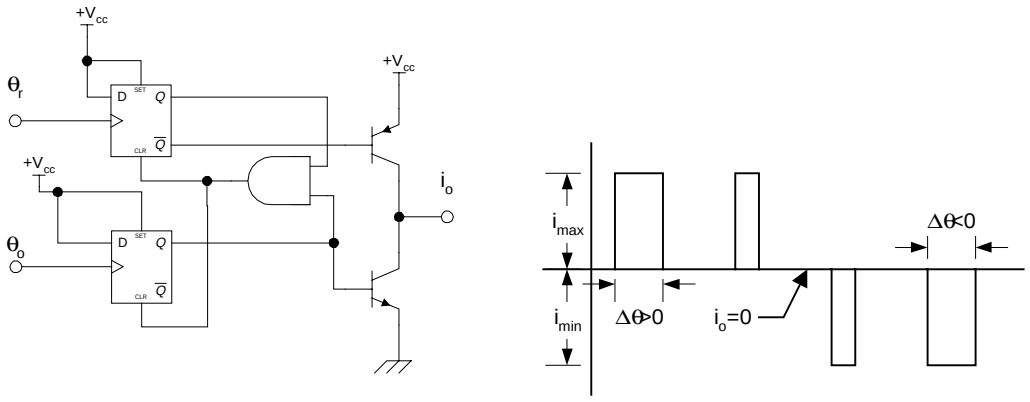

Figure A.2. (a) Phase-Frequency detector block diagram and (b) output waveform.

rising edge of the other input and the reference input. The operation can also be described in terms of a finite state diagram which can be found in both Rohde's book on microwave frequency synthesizers [5] and the Motorola MC14046 data sheet.

Using Fig. A.2b, the value of the proportionality constant commonly referred to as the phase detector gain can be determined. When the two input signals have a zero phase error, the average output current is zero. As the phase difference increases linearly so does the DC component of the output until, the two signals are 2 π radians out of phase. This causes the output current source to be on all the time, implying that the DC component is equal to the peak value of the current source. An analogous situation exists for a negative phase difference where the DC component of the output current is negative. Thus, the proportionality constant can be determined as the peak value of the output current source divided by the 2π radian phase difference. In the case of the RF2905, the peak output value is 40 μA which will result in a phase detector gain of 6.336 μA/rad (40 μA / 2π). Using these values, the DC component of the output current versus the phase difference between the two signals at the input has been plotted in Fig A.3.

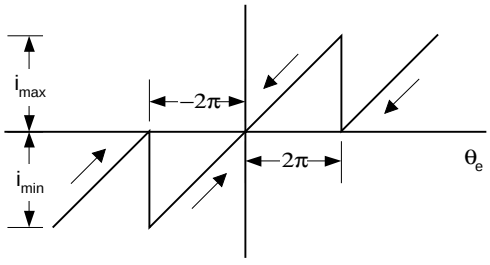

Figure A.3. Phase-Frequency detector characteristic vs. phase error.

A subtle effect that phase-frequency detectors suffer from is a “dead spot” in the phase detector characteristic within the vicinity of the phase error equal to zero. This dead spot results from the increasingly narrow pulses required from the phase-frequency detector for compensation. As the phase error becomes increasingly small, the resulting pulses decrease in width, until finally, the frequency limit of the charge pump and/or the timing jitter of the logic circuits is reached causing the output to lose its dependence on the phase error present at the input. There are various schemes for compensating for this effect [5].

A.1.2 Voltage Controlled Oscillator (VCO)

The VCO plays the role of the plant in the PLL control system. The only input variable to the VCO is the control voltage while the two output variables are the phase and instantaneous frequency of the VCO output sinusoid. The linear relationship between the phase and instantaneous frequency can be expressed as either an integration process in the time domain or as a division by the Laplacian operator s. The instantaneous frequency is also directly proportional to the control voltage. The constant of proportionality is the tuning sensitivity of the VCO. The value of the tuning sensitivity is determined by the particular components as well as the typology of the resonant network realized as part of the VCO. Typical realizations of the RF2905 VCO have tuning sensitivities between 10 MHz/V and 90 MHz/V. Combining this proportionality constant with the previously stated relation, the transfer function of the output phase resulting from a given input control voltage is found to be

$$\frac{\theta_o(s)}{V_c(s)} = \frac{2\pi K_o}{s}$$ Where Ko is the VCO tunning sensitivity

A.1.3 Digital Counters

The prescaler of the RF2905 operates in a manner similar to a synchronous counter where the division ratio is related to the number of flip flops in the counter and all of the flip flops change state simultaneously. For a division ratio of N, the output frequency is in fact equal to the input frequency divided by N. The previously stated relationship between the phase and frequency requires that the output phase is equal to the input phase

divided by N. The prescaler of the RF2905 is a type commonly known as a dual-modulus-dual-divide prescaler which implies several things. First, the dual divide implies that either the last stage or second to last stage can be selected such that the division ratio is either 128 or 64 respectively. The dual-modulus description implies that the prescaler contains a "swallow counter" making the division ratio also selectable between 128 and 129 for the last stage enabled and 64 or 65 for the second to last stage enabled. It does this by initially removing one pulse (termed "swallowing a pulse") and counting the next 64 or 128 depending on which is division ratio is selected. In this way, the counter's output becomes periodic on 65 or 129. Because the division ratio of the prescaler is on the order of seven to eight stages, there may be some form of internal delay compensation in order to trigger the swallow counter for the appropriate pulse.

A.1.4 Loop filter

As described in the introduction, the loop filter performs controls the dynamic behavior of the PLL. It also serves the purpose of suppressing higher frequency modulations of the VCO. Variations in loop filter design focus primarily around whether an active or passive filter is in use. Active filters have the potential to introduce additional low frequency noise into the loop as well as potential undesirable dynamic behavior. On the other hand, active filters can also reduce noise by allowing the designer to implement a lower gain VCO and using a wide voltage swing in the active filter. They are also easier from the standpoint of introducing modulation signals or voltage offsets without introducing additional noise or loading effects.

A.1.5 Reference Oscillator

The reference oscillator is the primary frequency and phase reference of the loop. Usually, a high Q oscillator such as a quartz crystal oscillator is used for this component. The reference oscillator as depicted in Fig. A.1 may also incorporate a TTL or CMOS divider as discussed in Sect. A.1.3 in order to reduce the noise present on the oscillator output signal. Many manufacturer's of PLL integrated circuits include counters of this type; however, it should be noted that the noise on the oscillator signal can only be reduced to the noise floor of the counter through division which is close to the thermal

noise limit. Dividing the frequency down any further is impractical as it provides no gains in noise performance and lowers the frequency at which the loop operates.

A.2 PLL Stability and Transient Response

The stability criterion and transient response of the PLL control system are inherently interrelated since my of the concepts used to discuss the stability of the system refer to the nature of the transient response. For example, the use of phase margin[3] , dampening factor, and natural frequency[4] would be rather esoteric without understanding their relationship to the transient response. It is their relationship to the transient step response that provides the widespread understanding and acceptance of these quantities.

A.2.1 PLL Stability

The PLL is considered to be stable if a frequency difference between the VCO and the reference oscillator of sufficiently small magnitude is removed through the normal action of the PLL. To some extent, the stability of the loop also describes its ability to remain in lock despite possible disturbances caused by external sources. Because the PLL is a negative feedback system, the standard approaches involving open loop gain and phase margin can be used to determine the criterion necessary to insure stability.

Although the phase detector introduces a nonlinearity into the control structure of the loop, a linear approximation of its behavior can be used to determine its stability. This approximation assumes that the difference in the phases is such that the phase detector is operating on the linear portion of its slope which for the phase-frequency is from -2π to $+2\pi$. When the phase difference extends beyond these limits, it shall be shown that the frequency difference between the reference oscillator and the prescaler output is so large that the required amount of correction will take more than one period of the reference oscillator to build up. Due to this build up action, the loop will reach a state where the frequency difference is small enough to make the phase difference magnitude less than 2π. At this point, before locking the loop will be operating in its linear mode where the

[3] Phase Margin is defined as the difference between -180° and the phase of the open loop transfer function of a negative feedback closed loop system.

output of the phase detector is linearly proportional to the phase difference between its inputs. Thus, because the loop will lock while in its linear mode of operation, the PLL stability criterion can be based upon a linear model of the PLL control system.

Proceeding in this manner, the open loop transfer function of the linear system is expressed as

$$G(s) = \frac{K_o K_d Z(s)}{s N} \tag{A.1}$$

where Z(s) is the impedance transfer function of the filter, K_o is in terms of rad/s/V, and K_d is in terms of A/rad. Because the output of the phase detector is a current source and the input of the VCO is a voltage source, the resulting transfer function required is an impedance transfer function. The most commonly used loop filter transfer function is the third order filter depicted in Fig. 5.4 with its corresponding impedance function.

$$Z(s) = \frac{(RC_2 s + 1)}{s(C_1 + C_2)(R\frac{C_1 C_2}{C_1 + C_2} s + 1)}$$

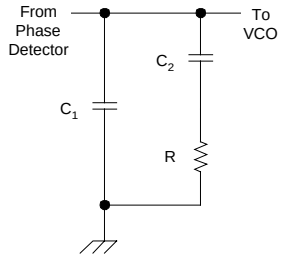

Figure A.4. Third order loop filter and impedance transfer function.

The combination of the phase-frequency detector and the third order filter gives the system several advantages. Because the open loop system possesses two poles at s = 0, the steady state phase error resulting from a frequency step will be zero which will require minimal amounts of correction from the phase detector to maintain. The additional pole in the filter will act as a low pass filter for higher frequency signals provided that the time constant τ_3 is set sufficiently greater than the 0 dB point of the open loop transfer function (termed the PLL locking bandwidth) so as not to affect the phase margin. Finally, because the output of the phase detector is a charge pump, an OP AMP is not required to realize the integrator functionality, and as a consequence problems associated with

[4] Dampening factor and natural frequency are the parameters used to express the poles of a second order closed loop control system in the form $s^2+2\zeta\omega_n+\omega_n^2$ [1]

frequency response (slew rate), offset voltages, and bias currents of the OP AMP do not complicate the design of the loop filter. In addition to this, the absence of the OP AMP removes the additional source of VCO control voltage corruption due to power supply noise.

If the zero of the filter function is not placed sufficiently lower than the 0 dB point of the open loop transfer function, the phase margin of the system will be zero, and the loop will not be stable. The radian frequency at which the open loop system would cross 0 dB in the absence of the loop filter zero is

$$\omega = \sqrt{\left(\frac{K_o K_d}{\tau_1 N}\right)} \qquad \text{(A.2)}$$

where τ_1 is equal to (C_1+C_2). Choosing the value of the zero frequency $(1/\tau_2 = (R \bullet C_2)^{-1})$ such that it is less than the result of the above expression and that $1/\tau_3$ (where $\tau_3 = \frac{RC_1C_2}{C_1+C_2}$) is significantly greater than the above expression, the loop stability criterion will be satisfied. Provided these conditions are satisfied, the PLL locking bandwidth will be $K_d \bullet K_o \bullet \tau_2/[N \bullet \tau_1]$. In some cases, additional filtering after the loop filter is required to reduce the level of reference frequency spurs present in the output. A low pass or notch filter can be added to the output provided that the cut off frequency of the low pass filter is greater than the PLL locking bandwidth and somewhere near the $1/\tau_3$ pole of the loop filter.

Having chosen the values of the time constants of the loop filter, the phase margin can be determined using the expression for the open loop phase shift transfer function and evaluating it at the locking bandwidth frequency. The performance of the loop will be that of a second order control system because the additional poles in the transfer function (if present) are located above the locking bandwidth and consequently below the -3dB point of the closed loop transfer function. Thus, for the frequency synthesizer application of the RF2905, the best trade off between response time and overshoot would be a phase margin of approximately 45° which corresponds roughly to a dampening factor, ζ, of 0.707.

A.2.2 Transient Response

To consider the transient response of the loop it must be assumed that the loop is initially in a locked state and that the transient signal applied to the loop is such that it will not cause the loop to become completely unsynchronized and undergo the acquisition process. An underlying principle in the transient analysis is that the linear approximation to the PLL's behavior is applicable which is in fact an implication of the previous statement. Upon substituting the impedance transfer function into the open loop transfer function of the PLL, it becomes clear that the system actually possesses two poles at the origin thus making it a Type II control system. This is significant because Type II linear control systems have no steady state errors to step inputs and ramp inputs. Since the transfer function is in terms of phase, this implies that upon reaching lock, the loop will have zero frequency and phase error. Additionally, the PLL can be closely modeled by a second order Type II linear control system provided, the additional pole associated with the τ_3 time constant is significantly higher than the locking bandwidth. This restriction makes the second order correction factor unnecessary and simplifies the analysis of the transient response.

The transient responses of the second order Type II PLL due to the phase step, frequency step, and frequency ramp have been calculated in several classic PLL references [1-3] as well in several control systems references. Only the important results of the frequency step will be reviewed here due to its relation to Sect. 4.2.2. Closing the loop, the phase transfer function of the linear PLL can be written,

$$H(s) = \frac{\omega_n^2 + j2\zeta\omega_n\omega}{\omega_n^2 - \omega^2 + j2\zeta\omega_n\omega} \tag{A.3}$$

where the relations between the dampening and natural frequency to the loop parameters of K_o, K_d, N, τ_1, and τ_2 are summarized as

$$\omega_n^2 = \frac{K_o K_d}{N\tau_1} \tag{A.4a}$$

$$2\zeta\omega_n = \frac{K_o K_d}{N}\frac{\tau_2}{\tau_1} \tag{A.4b}$$

The phase error transfer function is simply [1-H(s)], which makes calculating the phase error resulting from a frequency step a rather simple task. Writing the frequency step, in the context of the reference oscillator phase, the phase error becomes

$$\Phi_e(s) = \frac{\Delta\omega}{s^2}\left[1 - H(s)\right] = \frac{\Delta\omega}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{A.5}$$

When the Laplace transform form is transformed back into the time domain, the phase error is given by

$\zeta > 1$,
$$\Phi_e(t) = \frac{\Delta\omega}{\omega_n\sqrt{\zeta^2 - 1}} e^{-\zeta\omega_n t} \sinh\left(\omega_n t\sqrt{\zeta^2 - 1}\right) \tag{A.6a}$$

$\zeta = 1$,
$$\Phi_e(t) = \frac{\Delta\omega}{\omega_n} e^{-\zeta\omega_n t}\omega_n t \tag{A.6b}$$

$\zeta < 1$,
$$\Phi_e(t) = \frac{\Delta\omega}{\omega_n\sqrt{1 - \zeta^2}} e^{-\zeta\omega_n t} \sin\left(\omega_n t\sqrt{1 - \zeta^2}\right) \tag{A.6c}$$

depending on the value of the dampening factor ζ. The resulting frequency error can be obtained by simply s multiplied by Eq. A.5 which as it turns out has the same form as the equation resulting for the phase step transient. Taking advantage of this relationship, the inverse transformed frequency error in the time domain is expressed as

$\zeta > 1$,
$$f_e(t) = \Delta\omega e^{-\zeta\omega_n t}\left(\cosh\left(\omega_n t\sqrt{\zeta^2 - 1}\right) - \frac{\zeta}{\sqrt{\zeta^2 - 1}}\sinh\left(\omega_n t\sqrt{\zeta^2 - 1}\right)\right) \tag{A.7a}$$

$\zeta = 1$,
$$f_e(t) = \Delta\omega e^{-\zeta\omega_n t}\left(1 - \omega_n t\right) \tag{A.7b}$$

$\zeta < 1$,
$$f_e(t) = \Delta\omega e^{-\zeta\omega_n t}\left(\cos\left(\omega_n t\sqrt{1 - \zeta^2}\right) - \frac{\zeta}{\sqrt{1 - \zeta^2}}\sin\left(\omega_n t\sqrt{1 - \zeta^2}\right)\right) \tag{A.7c}$$

once again depending on the value of the dampening factor ζ. Since all of these are equations of constantly decreasing functions, the conclusion can be drawn that they represent stable systems all of which eventually reach synchronism. Additional constraints on the overshoot and settling time tend to restrict acceptable values of ζ and ω_n. This constitutes a brief overview of the transient step response.

Vita

The author, Scott D. Marshall was born in Barberton, Ohio, a town outside of Cleveland, Ohio. He received a Bachelor of Science in Electrical Engineering and Applied Physics from Case Western Reserve University in 1997. Following graduation, he worked at the University of Rochester Laboratory for Laser Energetics where his primary responsibilities were maintenance of the facility precision timing system. In the fall of 1997, he enrolled in the Master degree program at Virginia Polytechnic and State University and completed his degree in May of 1999. He has been a graduate research assistant at the Center for Wireless Telecommunications where his primary research interests have been RF and microwave circuits. During the completion of his graduate degree, he did an internship with Motorola Semiconductors Product Sector working within the Land Mobile Power Products Group.