Device Selection Criteria

---- Based on Loss Modeling and Figure of Merit

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(ABSTRACT)

With the increasing speed of the microprocessor and its rapidly increasing demand for power, determining how to power the microprocessors for our computers becomes an important issue. So far, industry has been struggling to operate the VR/VRM at higher and higher switching frequencies while maintaining acceptable power conversion efficiency. As a consequence, the power switches used in the VR/VRM must be able to work efficiently at a higher switching frequency and with a higher current density.

To evaluate the performance of the MOSFET for this low-output-voltage, high-current and high-switching-frequency application, a prevalent criterion, the Figure-of-Merit (FOM), is being widely adopted for determining the top switch of the buck converter in the VR/VRM. By comparing the FOMs of different devices, the device with the lowest FOM value should have the best performance and lead to the lowest loss for this device in the circuit. Qgd*Rdson is a widely accepted and widely used FOM for power devices. Due to the lack of accuracy of the power loss model, this FOM is no longer suitable for VRM applications. Furthermore, the question of how to use this FOM to select the right device for different application is another important issue.

This work presents an investigation of a new Figure-of-Merit based on a more accurate loss model, which includes the factor of Qgs2, the gate-driving voltage and the packaging parasitics. Furthermore, a simple method is proposed to select the right device and gate-driving voltage for different circuit conditions. A new simple and accurate closeform model for device loss with packing parasitics is derived. This model can provide more

physical information for each of the device parameters. The loss influence of the different packaging method is analyzed and discussed at the end of the work.

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TO MY PARENTS

Jianping Ying and Jingzhi Chen

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Chapter 1 Introduction

1.1. Background

With the increasing speed of the microprocessor and its demand for far more power, the method for powering the microprocessors for our computers becomes an important issue. The requirements of the Voltage Regulator (VR/VRM) for the future generation of microprocessors can be summarized as [1]:

1) Low output voltage (1.0-1.8V),
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So far, people within the industry have been struggling to operate the VR/VRM at a higher and higher switching frequency while maintaining acceptable power conversion efficiency. As a consequence, the power switches used in the VR/VRM must be able to work efficiently at a higher switching frequency and with higher current density.

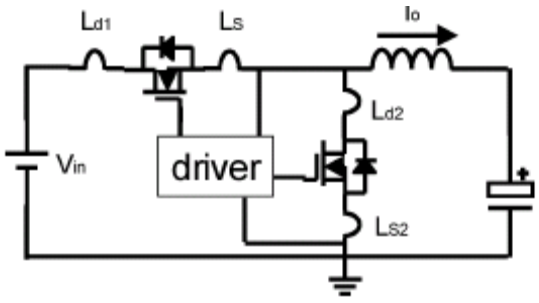


Figure 1-1 Buck DC/DC converter

To evaluate the performance of a MOSFET for this low output voltage, high output current and high switching frequency application, the prevalent criterion is the Figure-of-Merit (FOM), which has been widely adopted for the top switch of the buck converter in VRs/VRMs, which is shown in Figure 1-1.

By comparing different FOMs of different devices, the device with lowest FOM value should to have the best performance and lead to the lowest loss for this device in the circuit. Unfortunately, the most widely accepted FOM, which uses the product of the gate charge and the on-resistance (QgdRdson), is derived using the most simplistic loss model. This simple model doesn't consider several critical factors, such as the switching loss that occurs due to the current rising or falling period, the gate driving loss, and the packaging parasitic inductances, which are all very important for the low-voltage device.

The widely accepted FOM stemming from this over-simplified loss mode cannot accurately provide the operation performance of the top switch in a real buck converter, especially at a high switching frequency. The FOM should be modified with a more accurate loss model that can closely model the switching behavior of the top switch as well as its loss during operation. The bottom switch should have a different FOM to evaluate the device performance because its switching mechanism is very different from that of the top switch.

With this intention, this thesis focuses on how to find a more pragmatic FOM and to develop a method for selecting the optimal device for both the top and bottom switches for use during different circuit operation conditions.

1.2. Thesis Outline

In Chapter 2, the previously proposed and widely accepted FOMs are reviewed, and the major drawbacks of these FOMs are discussed.

In Chapter 3, an accurate analytical loss model is discussed, which includes the non-linear junction capacitor and the packaging parasitic inductor. The result of this model is quite accurate compared with the simulation result from a physics-based model.

In Chapter 4, the accurate analytical model is further simplified by ignoring the packaging parasitic inductor for the first-step analysis. The minimum loss equation of the top switch is derived. The importance of the Qgs2 factor is discovered based on that equation, and is compared with the previous FOM.

In Chapter 5, the importance of the gate-driving voltage is discussed, and the driving loss term is added to the minimum loss equation. A new Figure-of-Merit is proposed for the top switch based on the minimum loss equation. Compared with the previous widely accepted FOM, this FOM provides a more accurate indication of the device's minimum loss. A new method of selecting the optimal device and gate-driving voltage of the top switch is proposed based on the Normalized Power Loss equation.

In Chapter 6, the importance of the packaging parasitic inductor is discussed, and a new, simple closed-form analytical loss model is derived that can provide more physical information for each of the device parameters. The performances of different commercial packaging methods are compared, and the device selection method introduced in Chapter 5 is shown to still be valid with the packaging's parasitic inductor.

In Chapter 7, the bottom switch minimum loss is discussed, and a Figure-of-Merit for the bottom switch is proposed. The method of selecting the device for the top switch can also be used to select the bottom switch.

Chapter 2 Review of Device Figure-of-Merit

2.1. Review of Device Figure-of-Merit

There have been several device and material Figure-of-Merits (FOMs) published since the 1960s. Some of these focus on evaluating the semiconductor material performance, and some of them focus more on evaluating the device's processing technology.

In 1965, Johnson proposed the material Figure-of-Merit

$$JFOM = \frac{E_c v_s}{2\pi} \tag{2.1}$$

where E_c is the critical electric field and v_s is the carrier saturation drift velocity[2]. The JFOM defined the transistor cut-off frequency and the maximum allowable voltage. This FOM is used to evaluate the devices in signal amplification applications.

In 1983, J. Baliga derived a new material Figure-of-Merit,

$$BFOM = \varepsilon \mu E_C^3 \tag{2.2}$$

where ε is the dielectric constant of the material, μ is the majority carrier mobility, and E_C is the critical breakdown field of the semiconductor[3]. This FOM is good for evaluating materials when the device is operating at a relatively low frequency and the device loss is dominated by its conduction loss.

In 1989, J. Baliga again proposed a device FOM in an attempt to take the switching loss into account for high switching frequency applications. This FOM is

$$BHFFOM = \frac{1}{R_{on,sp} C_{in,sp}} \tag{2.3}$$

where $R_{on,sp}$ is the specific on-resistance and $C_{in,sp}$ is the specific input capacitance[4]. In the paper in which the BHFFOM is introduced, the author claims that in the case of a high operating frequency, it is necessary to include the switching losses and assume that the switching losses are due to the charging and discharging of the input capacitance of the MOSFET. This is why the total power loss is then given by

$$P = I_{rms}^2 \cdot R_{on} + C_{in} \cdot V_G^2 \cdot f \,. \tag{2.4}$$

Both the on-resistance and the input capacitance are related to the area of the device by their "specific" values. By using the substitution of (2.4), we can get

$$P = I_{rms}^2 \cdot \frac{R_{on,sp}}{A} + C_{in,sp} \cdot A \cdot V_G^2 \cdot f \tag{2.5}$$

where $R_{on,sp}$ and $C_{in,sp}$ are the specific on-resistance and capacitance, respectively. After applying the BHFFOM definition in (2.3), this loss equation becomes

$$P = I_{rms}^2 \cdot \frac{R_{on,sp}}{A} + \frac{A \cdot V_G^2 \cdot f}{R_{on,sp} \cdot BHFFOM} \,. \tag{2.6}$$

As the area of the device is increased, the first term decreases and the second term increases. Consequently, the total power loss exhibits a minimum value at an area at which

$$\frac{dP}{dA} = 0 \,. \tag{2.7}$$

This results in a minimum power loss of

$$P_{L,m} = 2 I_{rms} \cdot V_G \cdot \sqrt{\frac{f}{BHFFOM}} \tag{2.8}$$

at a device area given by

$$A_m = \frac{I_{rms} \cdot R_{on,sp}}{V_G} \cdot \sqrt{\frac{BHFFOM}{f}} \,. \tag{2.9}$$

In [4], the author claims that in order to improve the efficiency of the high-frequency power system, it is desirable to maximize the value of BHFFOM.

This BHFFOM is not that popular or widely used today for selecting devices. There are two major reasons behind this.

The first reason is that $C_{in,sp}$ is not directly related to the device switching loss but instead the gate driving loss. From power loss equation (2.4) we can see that the BHFFOM is trying to minimize the sum of the conduction loss and the gate-driving loss.

The second reason for its lack of popularity is that this BHFFOM can only be used for actual device technology comparison once $R_{on,sp}$ and $C_{in,sp}$ are known. Generally speaking, the device user can't find this kind of information directly from a device datasheet. Even if this information is given, the device user still can't select the right device by calculating this BHFFOM directly for different operating frequencies, different input and output voltages, etc. This is because this FOM only evaluates the device technology of one company but not one single device itself.

For these reasons, designers prefer to use another FOM that is the product of gate-to-drain charge (Q_{gd}) and on-resistance (R_{dson}).

$$FOM = Q_{gd} \cdot R_{dson} \tag{2.10}$$

The original date and proposer of this figure-of-merit is no longer traceable and this definition of the FOM was widely used to evaluate device performance in both high- and low-voltage MOSFETs until 2004. A. Huang provided a mathematic derivation of this figure-of-merit in [5].

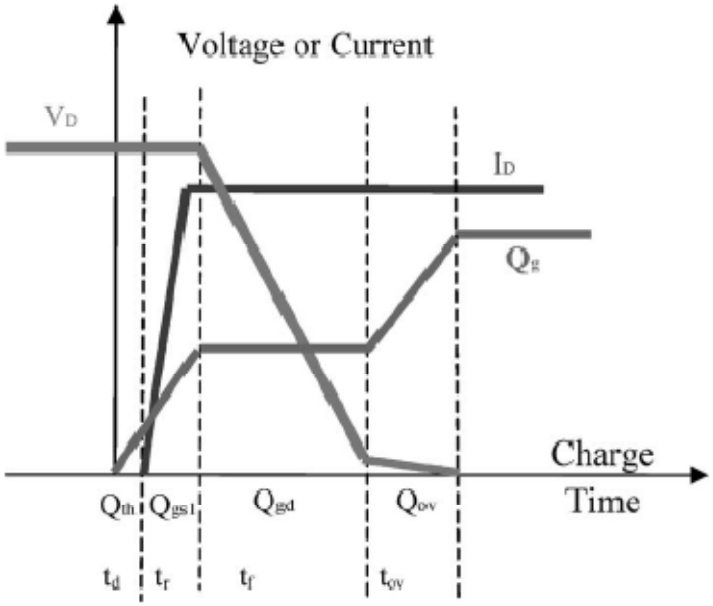


Figure 2-1 A typical switching waveform of a power MOSFET

A typical switching waveform of a power MOSFET is drawn in Figure 2.1. There are two periods, the current rising period (t_r) and the voltage falling period (t_f), that contribute to the switching loss when both the drain-to-source voltage and current are varying.

Hence the total power loss of the power device can be calculated by

$$P_{loss} = I_{rms}^2 R_{on} + V_D I_D (t_r + t_f) f \tag{2.11}$$

where the first term stands for the conduction loss and the second term stands for the switching loss, f is the switching frequency, V_D is the converter bus voltage, and I_D is the switch turn-on and turn-off current.

The drain-to-source current rising time t_r is approximately

$$t_r = \frac{Q_{gs2}}{i_{g,av}} \tag{2.12}$$

where Q_{gs2} is the gate charge of the input capacitance, which results in the rise of the drain-to-source current to I_D, and $i_{g,av}$ is the average gate current.

The time it takes the drain-to-source to fall from V_D to zero t_f can be approximated by

$$t_f = \frac{Q_{gd}}{i_{g,avg}} \tag{2.13}$$

where Q_{gd} is the gate charge of the drain-to-gate capacitor. As Q_{gd} is discharged by i_g, the drain voltage decreases to zero. This charge is also widely known as the Miller charge.

In this paper, the author assumes that during the switching period, the charging and discharging of the gate-to-drain charge Q_{gd} dominates the switching loss, which basically means $t_r << t_f$. This assumption is particularly true for high-voltage devices (>600V).

Under this assumption, and applying the same concept of the device area as done previously, the total power loss of the device can be simplified from (2.11) to

$$\begin{aligned} P_{loss} &\approx I_{rms}^2 R_{on} + V_D I_D t_f f \\ &= \frac{I_{rms}^2 R_{on,sp}}{A} + \frac{V_D I_D f Q_{gd,sp} A}{i_{g,av}} \end{aligned} \tag{2.14}$$

where $R_{on,sp}$ and $Q_{gd,sp}$ are the specific on-resistance and specific gate-to-drain charge, respectively.

Similarly, as the area of the device is increased, the first term decreases and the second term increases. Consequently, the total power loss exhibits a minimum value at an area at which

$$\frac{dP}{dA} = 0. \tag{2.15}$$

Therefore

$$P_{loss,\min} = 2 I_{rms} \sqrt{\frac{V_D I_D f}{i_{g,av}}} \sqrt{R_{on,sp} Q_{gd,sp}} \tag{2.16}$$

when the chip area is

$$A_{opt} = \frac{I_{rms}}{\sqrt{\frac{V_D I_D f}{i_{g,av}}}} \sqrt{\frac{R_{on,sp}}{Q_{gd,sp}}} \quad (2.17)$$

.

A. Huang claims that the first term of (2.16) is related to circuit operating conditions and the last term is related to the device. That's why the author proposes a new figure-of-merit:

$$HDFOM = \sqrt{R_{on,sp} Q_{gd,sp}} = \sqrt{R_{on} Q_{gd}} \quad (2.18)$$

.

This FOM looks similar to the one used previously ($Q_{gd} \cdot R_{dson}$) because the square root function is monotonic in the first quadrant. This paper gives theoretical support and a mathematic explanation of the figure-of-merit that is currently used to select devices.

2.2. Issues with current Figure-of-Merit

It is very obvious that the FOM ($Q_{gd} \cdot R_{dosn}$) is derived as a part of the device minimum loss. Hence minimizing this value means minimizing the device total loss, which is assumed to be dominated by the conduction loss and the switching loss due to the charging and discharging of the gate-to-drain charge Q_{gd}. If this assumption is especially true for high-voltage-rated devices as the author mentioned in his paper, this FOM is originally derived for high-voltage devices, but is widely used in low-voltage devices. So what's the difference between the low-voltage and high-voltage devices and their application? Does the loss related to charging and discharging of the gate-to-drain charge Q_{gd} still dominate the total switching loss? Does the figure-of-merit ($Q_{gd} \cdot R_{dosn}$) still work for low-voltage-rated devices, or there is a more suitable FOM for low-voltage devices?

Figure 2-2 shows a typical turn-off waveform of a high-voltage-rated device used in a PFC application. In this waveform, there are two periods that contribute to the power loss of the device because the drain-to-source voltage and current overlap. The first period corresponding to the drain-to-source voltage rising is called the voltage rising period (*Tr*). During this period, the gate current discharges the junction capacitor inside the power MOSFET and forms a depletion layer to block the drain-to-source voltage. The total charge is called the Miller charge or Q_{gd} . The second period corresponding to the drain-to-source current falling is called the current falling period (*Tf*). During this period, the gate current discharges the gate oxide capacitor in order to remove the charge stored in the inversion layer, and therefore this also removes the current steps following in the channel. The total charge is Q_{gs2} .

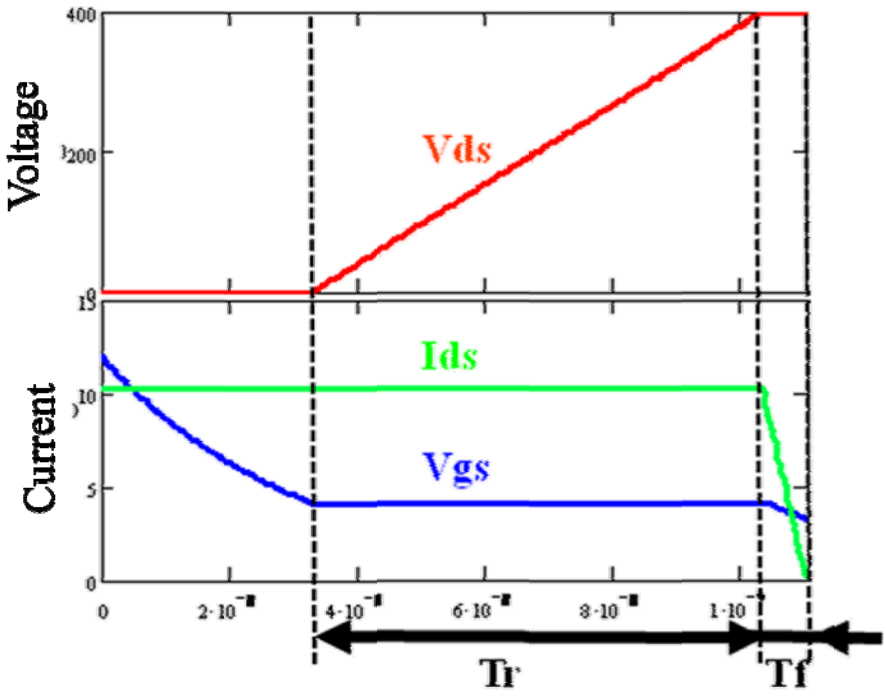


Figure 2-2 Typical turn-off waveform of a high voltage rating device

Comparing a low-voltage-rated device to a high-voltage-rated device, it becomes clear that the high voltage related device needs to spend a longer time to remove a larger amount of charge to block the higher voltage. By comparing Figure 2-2 with Figure 2-3,

which is a typical turn off waveform of a low-voltage-rated device used in a VRM application, we can see that the high-voltage device's voltage rising period occupies almost 91% of the total switching period, while for the low-voltage device the rising period only occupies 69% of the total switching period.

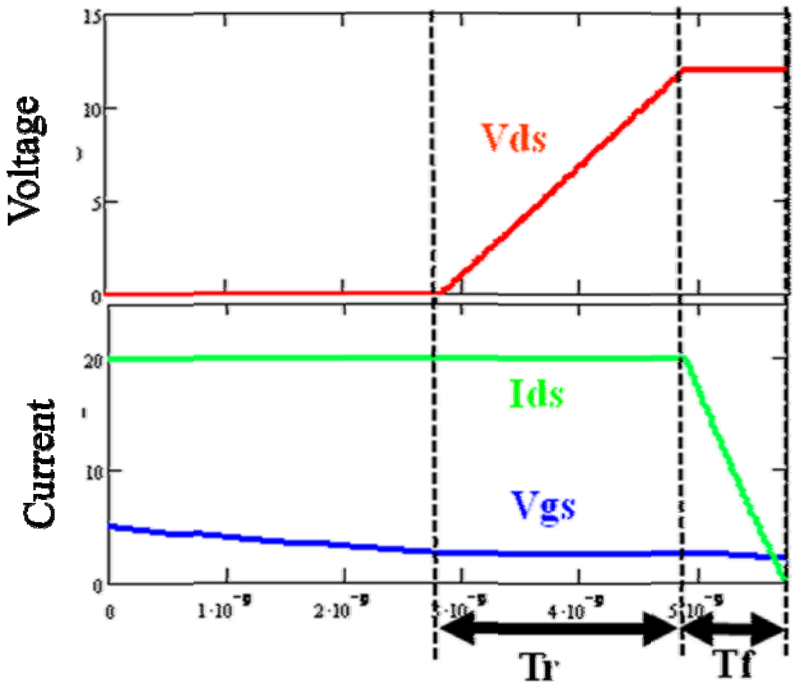
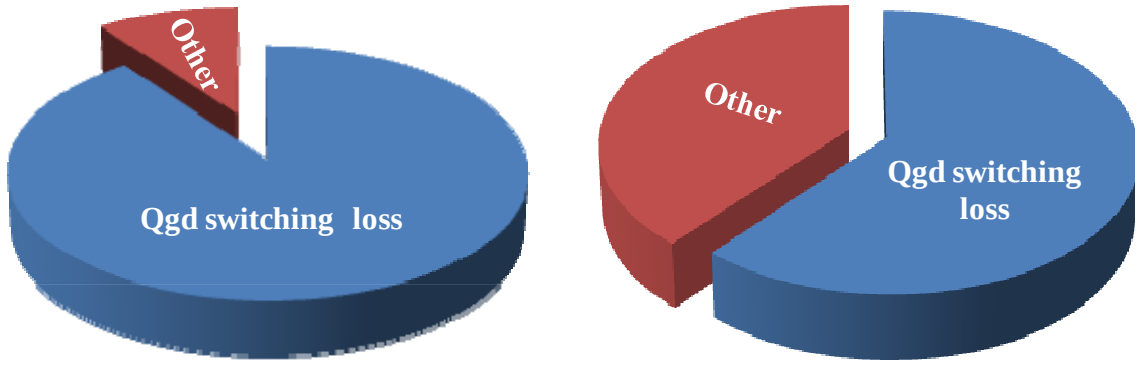


Figure 2-3 Typical turn off waveform of a low voltage rating device

As shown in Figure 2-4, the loss that occurs due to the charging and discharging of the gate-to-drain charge Q_{gd} dominates the total switching loss in a high-voltage application. The loss associated with Q_{gd} in low-voltage applications only occupies about half of the total switching loss.



High-voltage application **Low-voltage application**

Figure 2-4 Switching loss breakdown and comparison

2.3. Summary

From this analysis, we can conclude that the figure-of-merit ($Q_{gd} \cdot R_{dosn}$) is not quite suitable for selecting the device in low-voltage applications. This is because the loss due to charging and discharging of the gate-to-drain charge Q_{gd} in low-voltage devices not the dominant part of the total switching loss, as it is for high-voltage applications. The "other" losses are a large enough portion of the total switching loss that they need to be considered. We need to have a better loss model to model the device total loss, especially the switching loss.

Chapter 3 Accurate Device Analytical Model

3.1. Catalog of device model

There are many device loss models that have been proposed and published in the past years. Generally these can be catalogued into three types of models.

The first type of loss model is the physics-based model, such as the Medici and ISE-TCAD device models. [6] This kind of model is based on physical parameters of the device, such as cell geometry, doping concentration and so on. Figure 3-1 shows an ISE-TCAD cell structure model of the HAT2168 provided by Renesas and the simulation schematic used in the ISE-TCAD for a buck converter. This model is entered into device simulation software to do the finite element analysis (FEA), and the voltage and current waveforms are used to calculate the results. The final result from simulation of this physics-based model is very accurate when compared with the experimental results. However, this model needs proprietary information, and usually the device companies are not willing to release this information. The second drawback is that this kind of simulation is very time–consuming, and it normally takes one to two days for a high-end server to simulate only two switching cycles of a simple buck converter.

The second common loss model is the behavior model, such as the Saber and PSpice models. This kind of model uses key parameters such as the junction capacitance and the on-resistance to predict the device behavior though simulation. Because there are no proprietary issues and this model makes a good trade-off between accuracy and simulation time, this method is widely used in loss analysis, and almost every device

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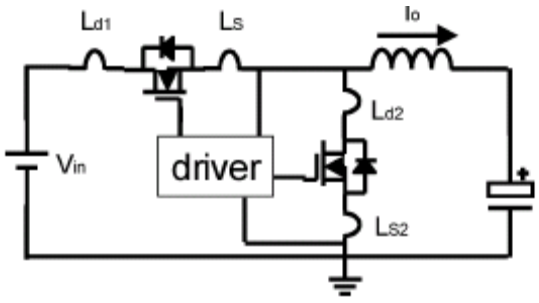

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Chapter 2 Review of Device Figure-of-Merit

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Both the on-resistance and the input capacitance are related to the area of the device by their "specific" values. By using the substitution of (2.4), we can get

$$P = I_{rms}^2 \cdot \frac{R_{on,sp}}{A} + C_{in,sp} \cdot A \cdot V_G^2 \cdot f \tag{2.5}$$

where $R_{on,sp}$ and $C_{in,sp}$ are the specific on-resistance and capacitance, respectively. After applying the BHFFOM definition in (2.3), this loss equation becomes

$$P = I_{rms}^2 \cdot \frac{R_{on,sp}}{A} + \frac{A \cdot V_G^2 \cdot f}{R_{on,sp} \cdot BHFFOM} \,. \tag{2.6}$$

As the area of the device is increased, the first term decreases and the second term increases. Consequently, the total power loss exhibits a minimum value at an area at which

$$\frac{dP}{dA} = 0 \,. \tag{2.7}$$

This results in a minimum power loss of

$$P_{L,m} = 2 I_{rms} \cdot V_G \cdot \sqrt{\frac{f}{BHFFOM}} \tag{2.8}$$

at a device area given by

$$A_m = \frac{I_{rms} \cdot R_{on,sp}}{V_G} \cdot \sqrt{\frac{BHFFOM}{f}} \,. \tag{2.9}$$

In [4], the author claims that in order to improve the efficiency of the high-frequency power system, it is desirable to maximize the value of BHFFOM.

This BHFFOM is not that popular or widely used today for selecting devices. There are two major reasons behind this.

The first reason is that $C_{in,sp}$ is not directly related to the device switching loss but instead the gate driving loss. From power loss equation (2.4) we can see that the BHFFOM is trying to minimize the sum of the conduction loss and the gate-driving loss.

The second reason for its lack of popularity is that this BHFFOM can only be used for actual device technology comparison once $R_{on,sp}$ and $C_{in,sp}$ are known. Generally speaking, the device user can't find this kind of information directly from a device datasheet. Even if this information is given, the device user still can't select the right device by calculating this BHFFOM directly for different operating frequencies, different input and output voltages, etc. This is because this FOM only evaluates the device technology of one company but not one single device itself.

For these reasons, designers prefer to use another FOM that is the product of gate-to-drain charge (Q_{gd}) and on-resistance (R_{dson}).

$$FOM = Q_{gd} \cdot R_{dson} \tag{2.10}$$

The original date and proposer of this figure-of-merit is no longer traceable and this definition of the FOM was widely used to evaluate device performance in both high- and low-voltage MOSFETs until 2004. A. Huang provided a mathematic derivation of this figure-of-merit in [5].

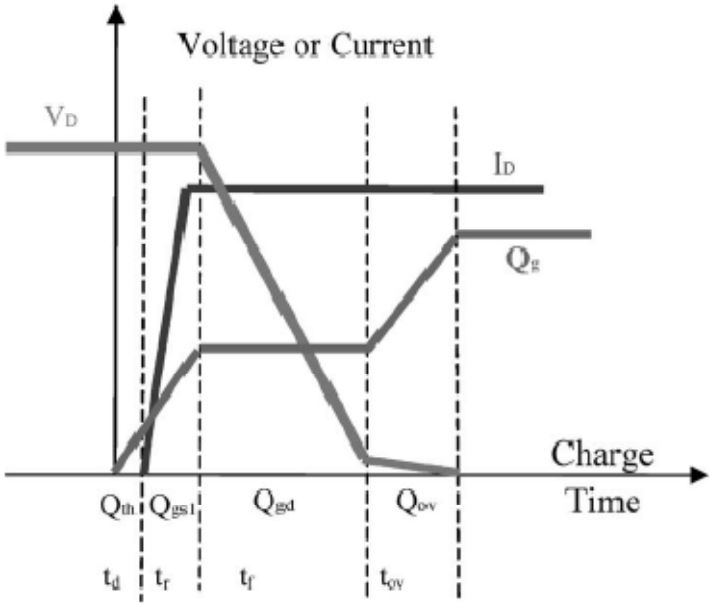


Figure 2-1 A typical switching waveform of a power MOSFET

A typical switching waveform of a power MOSFET is drawn in Figure 2.1. There are two periods, the current rising period (t_r) and the voltage falling period (t_f), that contribute to the switching loss when both the drain-to-source voltage and current are varying.

Hence the total power loss of the power device can be calculated by

$$P_{loss} = I_{rms}^2 R_{on} + V_D I_D (t_r + t_f) f \tag{2.11}$$

where the first term stands for the conduction loss and the second term stands for the switching loss, f is the switching frequency, V_D is the converter bus voltage, and I_D is the switch turn-on and turn-off current.

The drain-to-source current rising time t_r is approximately

$$t_r = \frac{Q_{gs2}}{i_{g,av}} \tag{2.12}$$

where Q_{gs2} is the gate charge of the input capacitance, which results in the rise of the drain-to-source current to I_D, and $i_{g,av}$ is the average gate current.

The time it takes the drain-to-source to fall from V_D to zero t_f can be approximated by

$$t_f = \frac{Q_{gd}}{i_{g,avg}} \tag{2.13}$$

where Q_{gd} is the gate charge of the drain-to-gate capacitor. As Q_{gd} is discharged by i_g, the drain voltage decreases to zero. This charge is also widely known as the Miller charge.

In this paper, the author assumes that during the switching period, the charging and discharging of the gate-to-drain charge Q_{gd} dominates the switching loss, which basically means $t_r << t_f$. This assumption is particularly true for high-voltage devices (>600V).

Under this assumption, and applying the same concept of the device area as done previously, the total power loss of the device can be simplified from (2.11) to

$$\begin{aligned} P_{loss} &\approx I_{rms}^2 R_{on} + V_D I_D t_f f \\ &= \frac{I_{rms}^2 R_{on,sp}}{A} + \frac{V_D I_D f Q_{gd,sp} A}{i_{g,av}} \end{aligned} \tag{2.14}$$

where $R_{on,sp}$ and $Q_{gd,sp}$ are the specific on-resistance and specific gate-to-drain charge, respectively.

Similarly, as the area of the device is increased, the first term decreases and the second term increases. Consequently, the total power loss exhibits a minimum value at an area at which

$$\frac{dP}{dA} = 0. \tag{2.15}$$

Therefore

$$P_{loss,\min} = 2 I_{rms} \sqrt{\frac{V_D I_D f}{i_{g,av}}} \sqrt{R_{on,sp} Q_{gd,sp}} \tag{2.16}$$

when the chip area is

$$A_{opt} = \frac{I_{rms}}{\sqrt{\frac{V_D I_D f}{i_{g,av}}}} \sqrt{\frac{R_{on,sp}}{Q_{gd,sp}}} \quad (2.17)$$

.

A. Huang claims that the first term of (2.16) is related to circuit operating conditions and the last term is related to the device. That's why the author proposes a new figure-of-merit:

$$HDFOM = \sqrt{R_{on,sp} Q_{gd,sp}} = \sqrt{R_{on} Q_{gd}} \quad (2.18)$$

.

This FOM looks similar to the one used previously ($Q_{gd} \cdot R_{dson}$) because the square root function is monotonic in the first quadrant. This paper gives theoretical support and a mathematic explanation of the figure-of-merit that is currently used to select devices.

2.2. Issues with current Figure-of-Merit

It is very obvious that the FOM ($Q_{gd} \cdot R_{dosn}$) is derived as a part of the device minimum loss. Hence minimizing this value means minimizing the device total loss, which is assumed to be dominated by the conduction loss and the switching loss due to the charging and discharging of the gate-to-drain charge Q_{gd}. If this assumption is especially true for high-voltage-rated devices as the author mentioned in his paper, this FOM is originally derived for high-voltage devices, but is widely used in low-voltage devices. So what's the difference between the low-voltage and high-voltage devices and their application? Does the loss related to charging and discharging of the gate-to-drain charge Q_{gd} still dominate the total switching loss? Does the figure-of-merit ($Q_{gd} \cdot R_{dosn}$) still work for low-voltage-rated devices, or there is a more suitable FOM for low-voltage devices?

Figure 2-2 shows a typical turn-off waveform of a high-voltage-rated device used in a PFC application. In this waveform, there are two periods that contribute to the power loss of the device because the drain-to-source voltage and current overlap. The first period corresponding to the drain-to-source voltage rising is called the voltage rising period (*Tr*). During this period, the gate current discharges the junction capacitor inside the power MOSFET and forms a depletion layer to block the drain-to-source voltage. The total charge is called the Miller charge or Q_{gd} . The second period corresponding to the drain-to-source current falling is called the current falling period (*Tf*). During this period, the gate current discharges the gate oxide capacitor in order to remove the charge stored in the inversion layer, and therefore this also removes the current steps following in the channel. The total charge is Q_{gs2} .

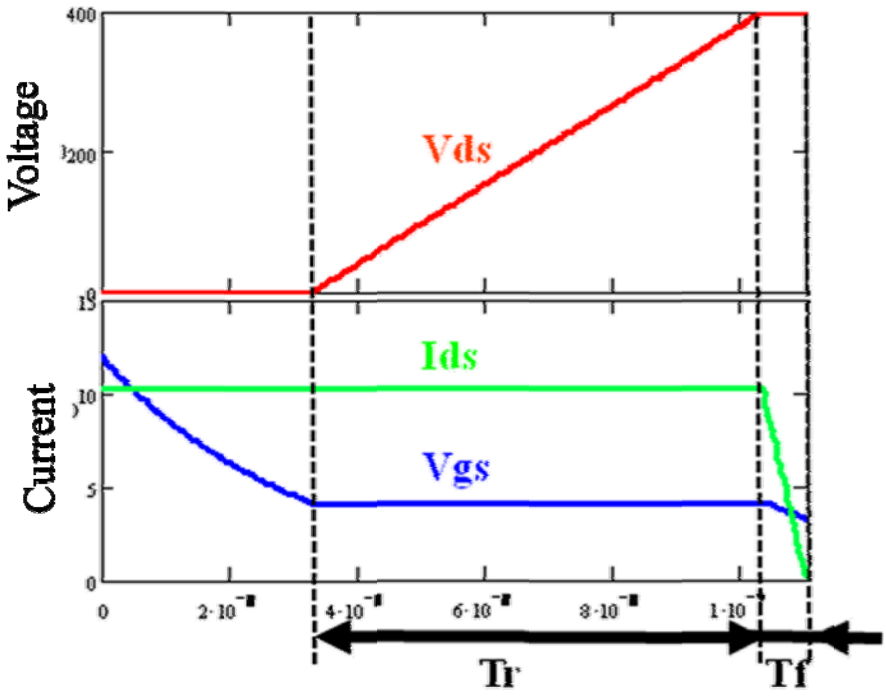


Figure 2-2 Typical turn-off waveform of a high voltage rating device

Comparing a low-voltage-rated device to a high-voltage-rated device, it becomes clear that the high voltage related device needs to spend a longer time to remove a larger amount of charge to block the higher voltage. By comparing Figure 2-2 with Figure 2-3,

which is a typical turn off waveform of a low-voltage-rated device used in a VRM application, we can see that the high-voltage device's voltage rising period occupies almost 91% of the total switching period, while for the low-voltage device the rising period only occupies 69% of the total switching period.

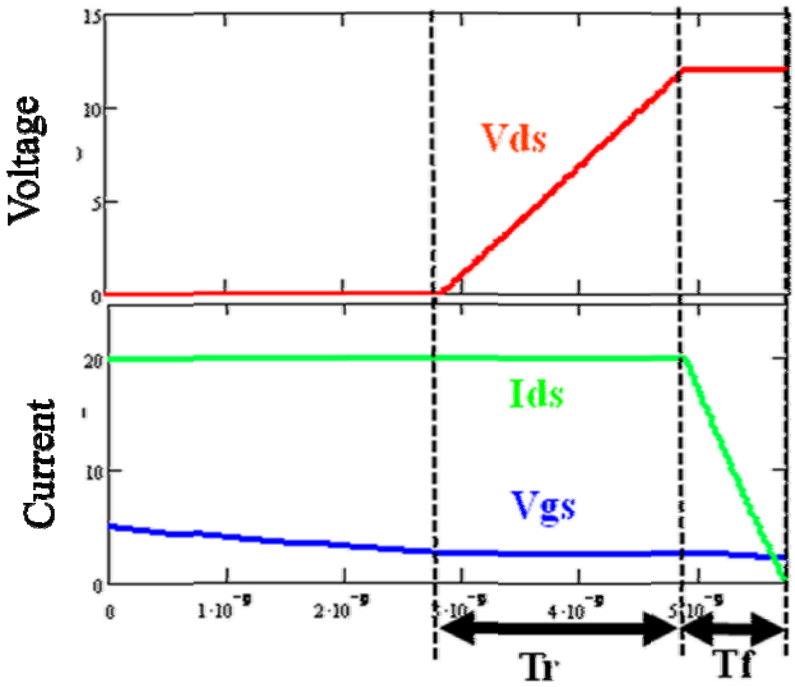
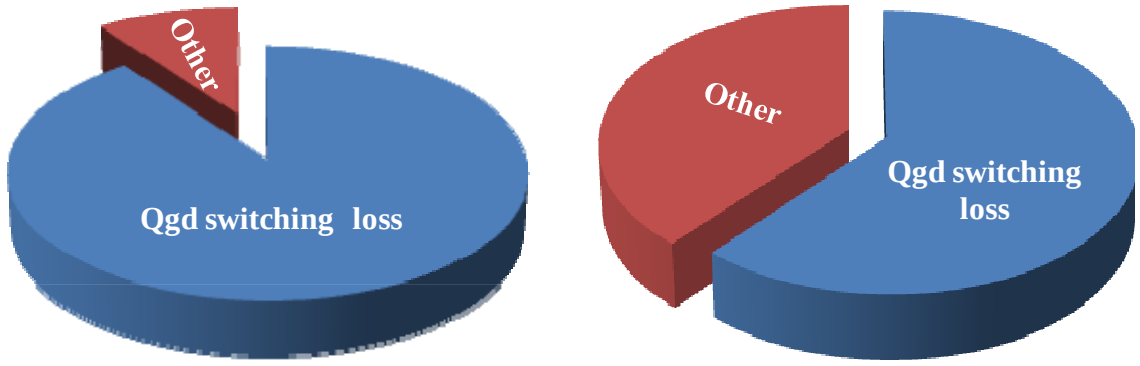


Figure 2-3 Typical turn off waveform of a low voltage rating device

As shown in Figure 2-4, the loss that occurs due to the charging and discharging of the gate-to-drain charge Q_{gd} dominates the total switching loss in a high-voltage application. The loss associated with Q_{gd} in low-voltage applications only occupies about half of the total switching loss.



High-voltage application **Low-voltage application**

Figure 2-4 Switching loss breakdown and comparison

2.3. Summary

From this analysis, we can conclude that the figure-of-merit ($Q_{gd} \cdot R_{dosn}$) is not quite suitable for selecting the device in low-voltage applications. This is because the loss due to charging and discharging of the gate-to-drain charge Q_{gd} in low-voltage devices not the dominant part of the total switching loss, as it is for high-voltage applications. The "other" losses are a large enough portion of the total switching loss that they need to be considered. We need to have a better loss model to model the device total loss, especially the switching loss.

Chapter 3 Accurate Device Analytical Model

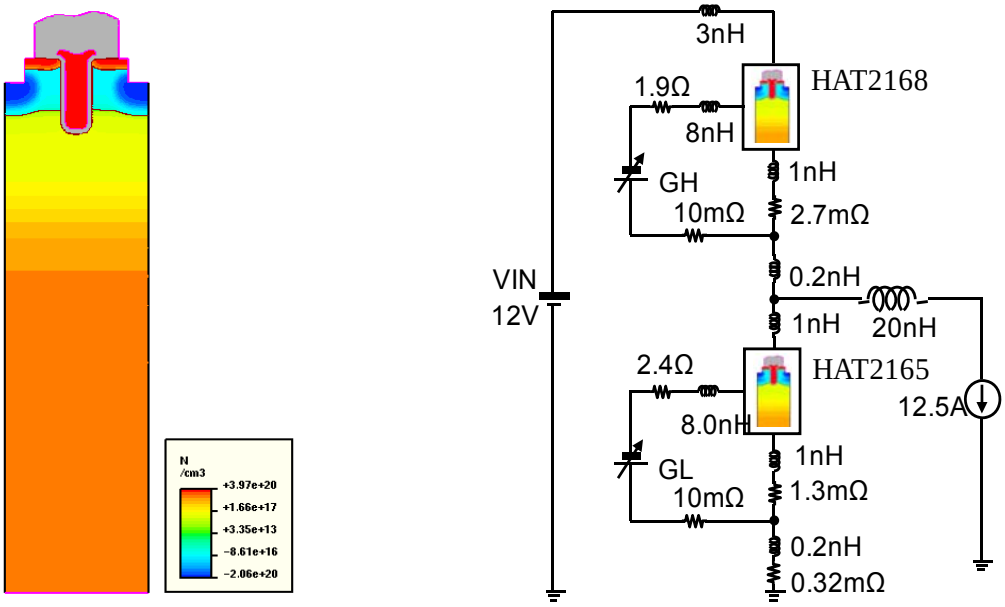
3.1. Catalog of device model

There are many device loss models that have been proposed and published in the past years. Generally these can be catalogued into three types of models.

The first type of loss model is the physics-based model, such as the Medici and ISE-TCAD device models. [6] This kind of model is based on physical parameters of the device, such as cell geometry, doping concentration and so on. Figure 3-1 shows an ISE-TCAD cell structure model of the HAT2168 provided by Renesas and the simulation schematic used in the ISE-TCAD for a buck converter. This model is entered into device simulation software to do the finite element analysis (FEA), and the voltage and current waveforms are used to calculate the results. The final result from simulation of this physics-based model is very accurate when compared with the experimental results. However, this model needs proprietary information, and usually the device companies are not willing to release this information. The second drawback is that this kind of simulation is very time–consuming, and it normally takes one to two days for a high-end server to simulate only two switching cycles of a simple buck converter.

The second common loss model is the behavior model, such as the Saber and PSpice models. This kind of model uses key parameters such as the junction capacitance and the on-resistance to predict the device behavior though simulation. Because there are no proprietary issues and this model makes a good trade-off between accuracy and simulation time, this method is widely used in loss analysis, and almost every device

company will provide this behavior model. However, this model is still not suitable for a figure-of-merit because it is still a simulation-based model.



ISE-TCAD cell model of HAT2168 Simulation schematic in ISE-TCAD

Figure 3-1 Cell model and simulation schematic in ISE-TCAD

The third common loss model is the analytical model, which is also called the mathematical model. This model uses a mathematical way to derive the loss equation based on some key parameters and some equivalent circuits. Compared to the physics-based model and behavior model, this model is much faster and more clearly shows the relationship between the device loss and key parameters. Therefore this method is more meaningful as a starting point for coming up with a new FOM. The major challenge is how to determine a trade-off between simplicity and accuracy.

3.2. One accurate loss model

In 2006, CPES ex-graduate student Yuancheng Ren published an advanced and accurate analytical loss model in the IEEE transaction paper “Analytical Loss Model of Power

MOSFET"[7]./ In this paper, the author includes the influence of several key parameters which were not considered before.

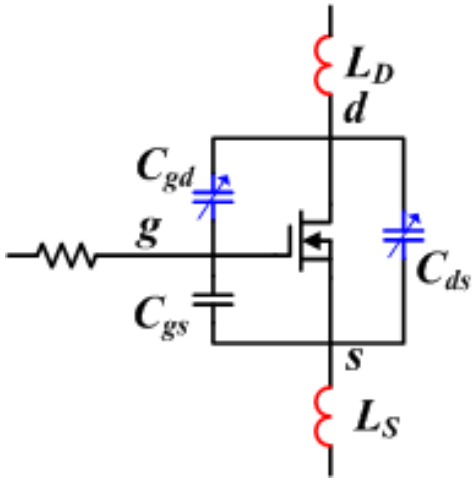


Figure 3-2 Equivalent circuit of a power MOSFET

Figure 3-2 shows the equivalent circuit of a power MOSFET where C_{gd}, C_{gs} and C_{ds} are three parasitic capacitors, and L_d and L_s are the package parasitic inductors.

The first key set of parameters is for the non-linear junction capacitors of a MOSFET. As explained in [8], C_{gs} is the capacitor related to gate oxide thickness, which is almost constant, and C_{gd} and C_{ds} are the junction capacitors, which are quite non-linear in terms of drain-to-source voltage (V_{ds}). Because the drain-to-source voltage is always varying during the switching period, it is very important to model this non-linear behavior. A curve fitting method is used to match the accurate capacitance value.

Usually the device datasheet would give some typical input capacitance (C_{iss}), output capacitance (C_{oss}) and reverse transfer capacitance (C_{rss}) values at a certain drain-to-source voltage (V_{ds}). For example, we have these three capacitances at V_{ds} at 16V and 1V. Because C_{gs} is almost constant in terms of drain-to-source voltage, it can be derived by directly subtracting two capacitances.

$$C_{gs} = C_{iss\_16V} - C_{rss\_16V} \tag{3.1}$$

We can also calculate the drain-to-source capacitance at 16V and 1V.

$$C_{ds}(16V) = C_{oss\_16V} - C_{rss\_16V} \tag{3.2}$$

$$C_{ds}(1V) = C_{oss\_1V} - C_{rss\_1V} \tag{3.3}$$

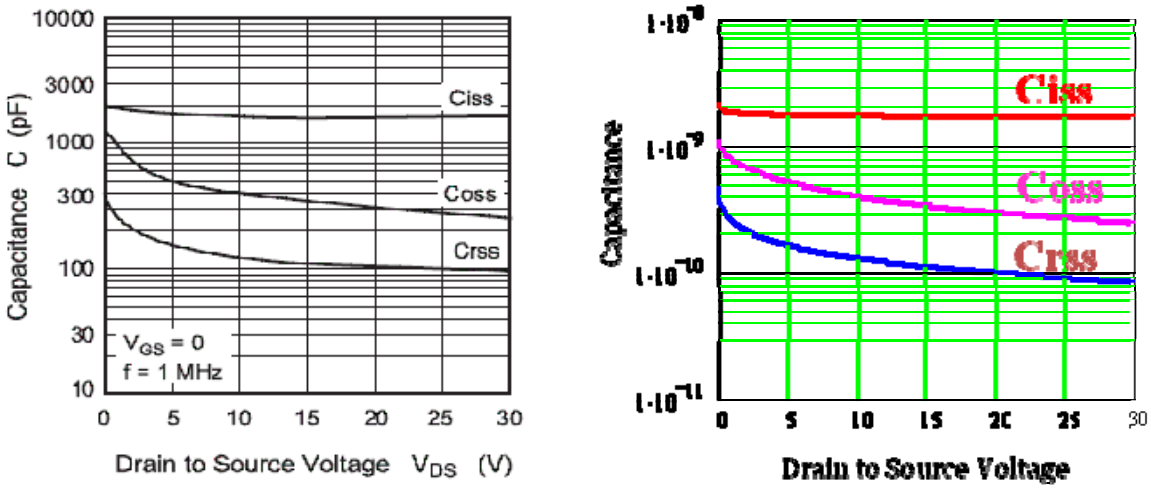
The general drain-to-source capacitance can be expressed as

$$C_{ds}(V_{ds}) = \frac{C_{j1}}{\sqrt{1+\frac{V_{ds}}{\Phi 1}}}. \tag{3.4}$$

Substituting (3.2) and (3.3) into (3.4) in turn, two equations are obtained. Based on these equations, two coefficients can be solved. The same method can also be applied to the gate-to-drain capacitor, which can be generally expressed as

$$C_{gd}(V_{ds}) = \frac{1}{\frac{1}{C_{gd\_0V}} + \frac{V_{ds}^{x}}{C_{j2}}}. \tag{3.5}$$

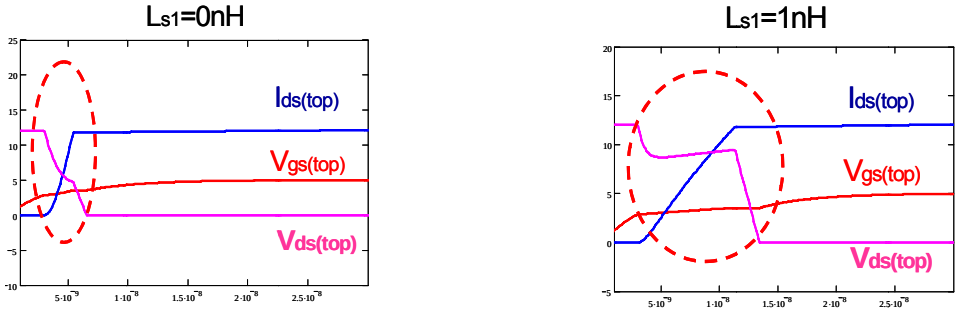
Figure 3-3 shows a comparison between the curve fitting results and the typical capacitance curve from the device datasheet [9]. The two curves match very well.



Curves from HAT2168 datasheet　　Curves derived by curve fitting

Figure 3-3 Comparison between curve fitting results and datasheet

The second key set of parameters is for the two packaging parasitic inductors shown in Figure 3-2. One is known as the common source inductor (Ls), which is defined as the inductor shared by the power stage and the driver loop. This common source inductor will dramatically increase the current rising and falling speed during the switching processing, and significantly impacts the switching loss. Figure 3-4 shows the switching waveform with and without the common source inductor.



Without Ls　　With Ls

Figure 3-4 Switching waveforms with and without Ls

The operation of a MOSFET can be separated into three different modes, depending on the voltages at the terminals. Figure 3-5 shows a typical current-voltage curve of a power MOSFET.

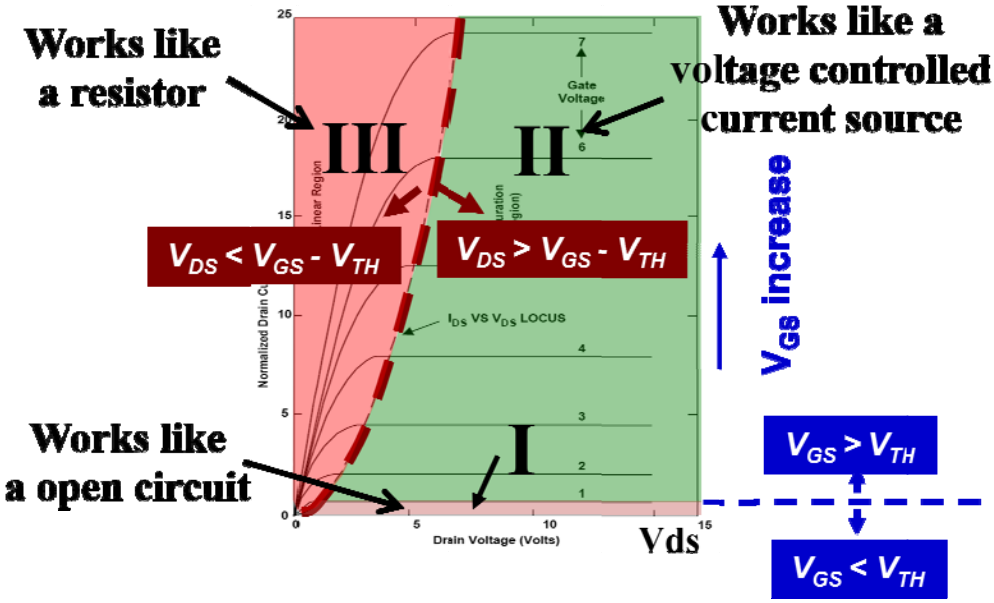


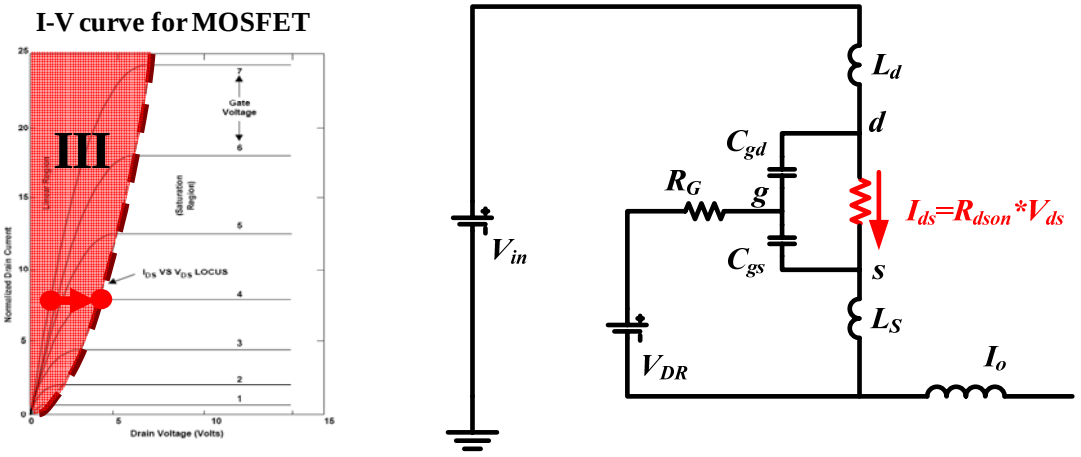
Figure 3-5 A typical MOSFET current-voltage curve

We can see that during the turn-off switching processing, the MOSFET will go though the linear region (Region III), where the MOSFET works like a resistor; the saturation region (Region II), where it works like a voltage controlled current source; and the cut-off region (Region I), where it works like a open circuit. Thus it is necessary to use a piece-wise linear model to model the MOSFET working in different regions.

For example, according to the operation in different regions, the MOSFET turn-off period can be further divided into four periods, described below.

The delay period

During this period, after removing the driving voltage from the gate, the gate-to-source voltage starts to fall and discharge the two device parasitic capacitances C_{gs} and C_{gd}. The drain-to-source current is clamped by the load current. This period ends when the gate-to-source voltage is reduced to the plateau voltage. From the I-V curve of MOSFET we can see that during the delay period, the operating point is moving within the linear region, and the MOSFET is equivalent to a resistor, as shown in Figure 3-6.



MOSFET I-V curve MOSFET equivalent circuit

Figure 3-6 MOSFET I-V curve and equivalent circuit for the delay period

Using the equivalent circuit shown in Figure 3-6 we can derive

$$v_{gs}(t) = V_{DR} \cdot e^{\frac{-t}{R_G (C_{gs}+C_{gd})}}, \tag{3.6}$$

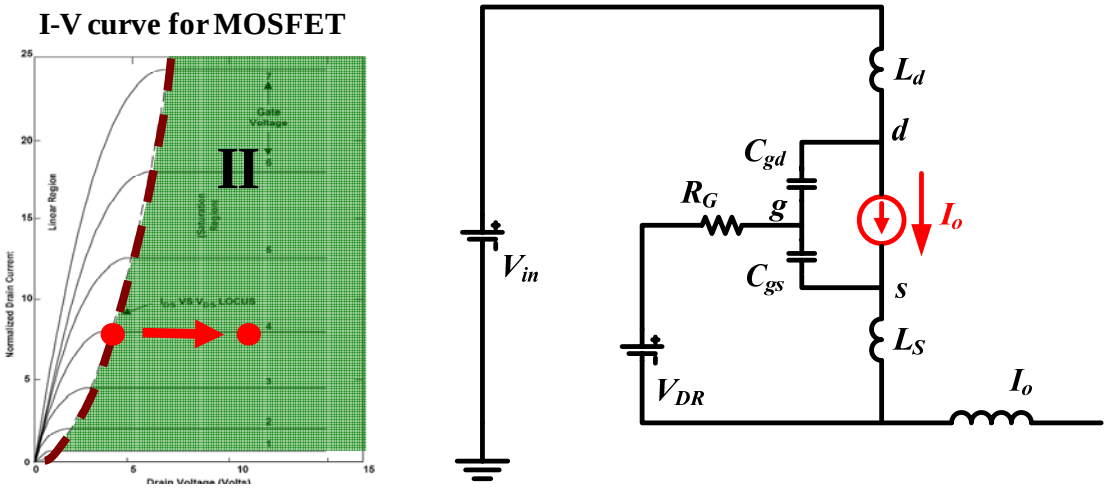
$$v_{ds}(t) = i_{ds}(t) \cdot R_{dson}, \text{ and} \tag{3.7}$$

$$i_{ds}(t) = I_o. \tag{3.8}$$

By integrating the drain-to-source voltage and current over the period time, we can obtain the loss during the delay period, and this loss is basically a part of the conduction loss.

The drain-to-source voltage rising period

During this period, the MOSFET operating point moves into the saturation region, in which it acts like a voltage-controlled current source. The equivalent circuit is shown in Figure 3.7.



MOSFET I-V curve MOSFET equivalent circuit

Figure 3-7 MOSFET I-V curve and equivalent circuit for the voltage rising period

The drain-to-source current and gate-to-source voltage have the following relationship

$$i_{ds} = g_{fs}(v_{gs} - V_{th}) \tag{3.9}$$

where g_{fs} is the transconductance of the MOSFET and V_{th} is the threshold voltage.

Because the drain-to-source current is still clamped by the load current, the gate-to-source voltage will remain constant at a value called the plateau voltage.

$$v_{gs}(t) = V_{plt} = \frac{I_o}{g_{fs}} + V_{th} \tag{3.10}$$

The gate current will charge the gate-to-drain parasitic capacitor to raise the drain voltage linearly as

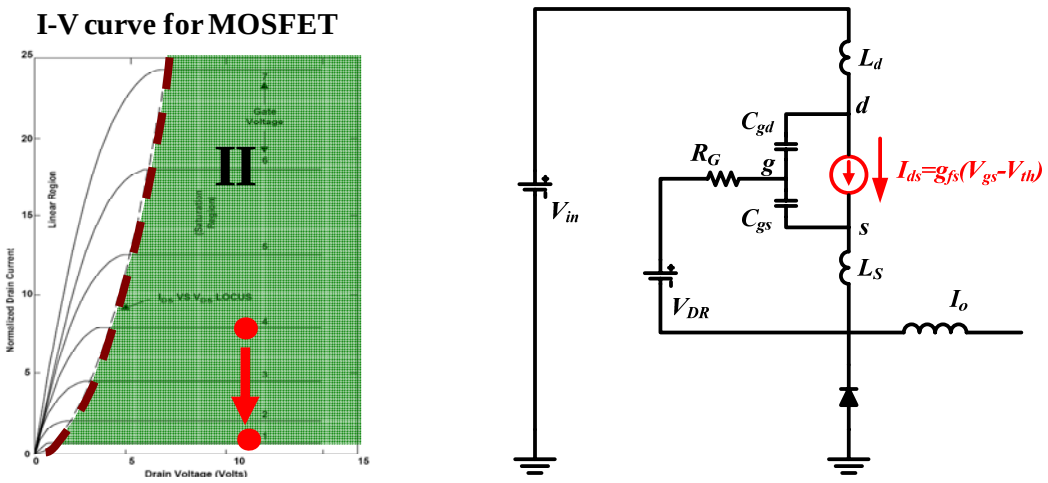
$$v_{ds}(t) = \frac{g_{fs}V_{th} + I_o}{(1 + g_{fs}R_G)C_{gd}}t \tag{3.11}$$

This effect is known as the Miller effect, and the gate-to-drain capacitor is called the Miller capacitor.

This period ends when the drain-to-source voltage equals the input voltage. The integral of the drain-to-source voltage and current over this period time will give the loss during the voltage rising period.

The current falling period

Following the voltage rising period is the current falling period. Because the drain-to-source voltage rose to the input voltage, the bottom switch's anti-parallel body diode will start to conduct current, and the top switch drain-to-source current is not correctly clamped by the load. Like the previous period, the MOSFET still works in the saturation region and can still be treated as a voltage-controlled current source, as shown in Figure 3-8.



MOSFET I-V curve MOSFET equivalent circuit

Figure 3-8 MOSFET I-V curve and equivalent circuit for the current falling period

Hence along with the drain-to-source current falling, the gate-to-source voltage will drop as well in order to stay a voltage-controlled voltage source.

The equivalent circuit of the MOSFET for this period is shown in Figure 3.8, and based on this equivalent circuit, a time-domain solution can be solved by using the Laplace transform. Two possible solutions exist depending on the different time constants.

Defining $\tau_m = g_{fs}(L_d + L_s)$ $\tau_{G'} = C_{gd}R_G$ $\tau_{G''} = (C_{gd} + C_{gs})R_G L_S$,

the sinusoidal solutions occur when $\tau_{G''}^2 < 4\tau_{G'}\tau_m$.

$$v_{gs}(t) = (\frac{I_o}{g_{fs}} + V_{th})e^{\frac{-t}{\tau_a}}[\cos(\omega_a t) + \frac{1}{\omega_a \tau_a}\sin(\omega_a t)] \tag{3.12}$$

$$i_{ds}(t) = (g_{fs}V_{th} + I_o)e^{\frac{-t}{\tau_a}}[\cos(\omega_a t) + \frac{1}{\omega_a \tau_a}\sin(\omega_a t)] - g_{fs}V_{th} \tag{3.13}$$

$$v_{ds}(t) = V_{in} + (g_{fs}V_{th} + I_o)\omega_a(L_s + L_d)e^{\frac{-t}{\tau_a}}[1 + (\frac{1}{\omega_a \tau_a})^2]\sin(\omega_a t) \tag{3.14}$$

where $\tau_a = \frac{2\tau_m \tau_{G'}}{\tau_{G''}}$ and $\omega_a = \sqrt{\frac{1}{\tau_m \tau_{G'}} - (\frac{\tau_{G''}}{2\tau_m \tau_{G'}})^2}$.

The exponential solutions occur when $\tau_{G''}^2 > 4\tau_{G'}\tau_m$.

$$v_{gs}(t) = (\frac{I_o}{g_{fs}} + V_{th}) \frac{e^{\frac{-t}{\tau_b}} \tau_b - e^{\frac{-t}{\tau_c}} \tau_c}{\tau_b - \tau_c} \tag{3.15}$$

$$i_{ds}(t) = (I_o + g_{fs} V_{th}) \frac{e^{\frac{-t}{\tau_b}} \tau_b - e^{\frac{-t}{\tau_c}} \tau_c}{\tau_b - \tau_c} - g_{fs} V_{th} \tag{3.16}$$

$$v_{ds}(t) = V_{in} + (g_{fs} V_{th} + I_o)(L_d + L_s) \frac{e^{\frac{-t}{\tau_b}} - e^{\frac{-t}{\tau_c}}}{\tau_b - \tau_c} \tag{3.17}$$

where $\tau_b = \frac{2(\tau_m \tau_{G'})^2}{\tau_{G''} - \sqrt{\tau_{G''}^2 - 4\tau_m \tau_{G'}}}$ and $\tau_c = \frac{2(\tau_m \tau_{G'})^2}{\tau_{G''} + \sqrt{\tau_{G''}^2 - 4\tau_m \tau_{G'}}}$.

This period ends when the drain-to-source current falls to zero. The integral of the drain-to-source voltage and current over this period time will give the loss during the current falling period.

After the current falls to zero, the gate-to-source voltage will continue dropping from the threshold to zero. However, during this period, the device is already turned off and there is no current following though the channel of the device. This is why there is no loss produced during this period.

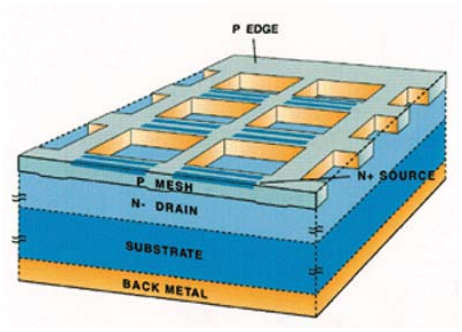
3.3. Summary

Yuancheng Ren's analytical loss model includes non-linear junction capacitors, packaging parasitic inductors, and the piece-wise linearity method to provide an accurate switching loss calculation of the top switch, which is the most difficult part of the loss modeling. However, although this model is accurate, it is an open-form solution and needs some iteration and judgment in the calculation which can only be done by Mathcad software. In summary, this analytical model provides a very good starting point and needs to be further simplified.

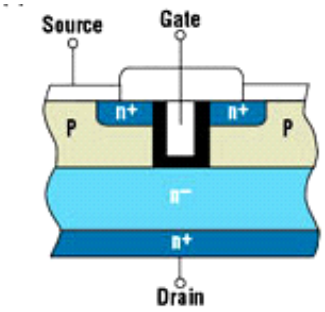
Chapter 4 Importance of the Qgs2 Factor

4.1. Basic assumption of power device

According to [8], a power MOSFET die is composed of several thousands of elementary cells. Figure 4-1 shows a power MOSFET cell structure and the cross-section of a Trench elementary cell.



Power MOSFET cell structure



Cross-section of a Trench elementary cell

Figure 4-1 Power MOSFET cell structure

Based on the cell structure assumption, we can conclude that for a given MOSFET a large number of elementary cells are paralleled inside. Paralleling more elementary cells would achieve a smaller Rdson value but a larger gate charge. Basically, the given MOSFET has the following relationship:

$$R_{dson} = \frac{R_{dson,sp}}{N_{cell}} \tag{4.1}$$

and

$$Q_g = Q_{g,sp} \cdot N_{cell} \quad Q_{gd} = Q_{gd,sp} \cdot N_{cell} \quad Q_{gs2} = Q_{gs2,sp} \cdot N_{cell} \tag{4.2}$$

where $Q_{g,sp}$, $Q_{gd,sp}$, $Q_{gs2,sp}$ and $R_{dson,sp}$ are the specific value of one elementary cell and N_{cell} is the cell number related to a given device.

4.2. Simplified loss-model-based ideal package

Although Yuancheng Ren's model is a very accurate analytical loss model, its mathematical calculation requires a lot of iteration work and some boundary conditions. This can only be performed by using a mathematic software program such as Mathcad. The analytical model, although very accurate, is still too complex to define a figure-of-merit, and a simplified model must be found. To simplify the model, we first neglect the packaging parasitic inductors and assume an ideal package.

From the previous analysis, we can observe that there are only two periods involving loss during the device turn-off period; one is the voltage rising period and one is the current falling period.

For the voltage rising period, the parasitic inductor doesn't have too much of an impact on the loss. This is because, as shown in Figure 3-7, the current is clamped at the load current during that period, and the parasitic inductor won't able to produce any voltage significant enough to influence either the power stage loop or the gate driving loop. Therefore the drain-to-source voltage would rise according to the same equation as (3.11). For convenience this equation is rewritten here.

$$v_{ds}(t) = \frac{g_{fs}V_{th} + I_o}{(1 + g_{fs}R_G)C_{gd}}t \tag{4.3}$$

Because $g_{fs}R_G >> 1$ is always true for a power MOSFET,

$$v_{ds}(t) \approx \frac{g_{fs}V_{th} + I_o}{g_{fs}R_G C_{gd}}t \tag{4.4}$$

.

The drain-to-source current is clamped at load current

$$i_{ds}(t) = I_o \tag{4.5}$$

.

This period ends when the drain-to-source voltage rises to the input voltage. This means the period length equals

$$Tr = \frac{g_{fs} R_G C_{gd}}{g_{fs} V_{th} + I_o} \quad (4.6)$$

The switching loss during this period can be calculated as

$$P_{off\_Tr} = \int_0^{Tr} v_{ds}(t) i_{ds}(t) dt = \frac{V_{in} I_o}{2} \frac{V_{in} C_{gd} g_{fs} R_g}{g_{fs} V_{th} + I_o} f_s \quad (4.7)$$

Because $V_{th} + \frac{I_o}{g_{fs}} = V_{plt}$, which comes from Equation (3.10), and $V_{in} C_{gd} \approx Q_{gd}$ which is derived by the definition of Miller charge, Equation (3.22) becomes

$$P_{off\_Tr} = \frac{V_{in} I_o}{2} \frac{Q_{gd} R_g}{V_{plt}} f_s \quad (4.8)$$

With the ideal package assumption, during the current falling period, the drain-to-source current equation will reduce to

$$i_{ds}(t) = (I_o + V_{th} \cdot g_{fs}) e^{\frac{-t}{R_g (C_{gs} + C_{gd})}} - V_{th} \cdot g_{fs} \quad (4.9)$$

because $\tau_b << \tau_c$ in Equation (3.16).

The drain-to-source voltage stays at the input voltage, which is

$$v_{ds}(t) = V_{in} \quad (4.10)$$

Expanding the exponential term by using Taylor series and neglecting the high order terms, Equation (3.24) becomes

$$i_{ds}(t) = I_o - (I_o + V_{th} \cdot g_{fs}) \frac{t}{R_g (C_{gs} + C_{gd})} \quad (4.11)$$

and this period ends when the drain-to-source current falls to zero. Thus the period length can be calculated by

$$T_f = I_o \cdot \frac{R_g (C_{gs} + C_{gd})}{I_o + V_{th} \cdot g_{fs}} \quad (4.12)$$

The integral of the drain-to-source voltage and current over the period length will give the loss during the voltage-rising period.

$$P_{off\_Tf} = \int_0^{T_f} V_{ds}(t) I_{ds}(t) f_s dt = \frac{V_{in} I_o}{2} \frac{I_o (C_{gd} + C_{gs}) R_g}{g_{fs} V_{th} + I_o} f_s \quad (4.13)$$

Because $V_{th}+\frac{I_o}{g_{fs}}=V_{plt}$, which comes from Equation (2.10), and $\frac{I_o}{g_{fs}}(C_{gs}+C_{gd})=Q_{gs2}$, which is the definition of the *Qgs2*, Equation (3.28) becomes

$$P_{off\_Tf}=\frac{V_{in}I_o}{2}\frac{Q_{gs2}R_g}{V_{plt}}f_s \quad . \tag{4.14}$$

The same simplification method can also be applied to calculate the turn-on loss, and will give very similar results. Table 4-1 gives a summary of the simplified loss equations within each period of turn-on and turn-off loss.

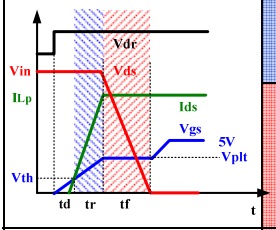
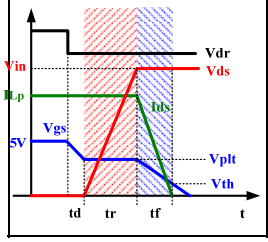
		Loss equations for ideal package
Turn on 	**Current Rising Period**	$\frac{V_{in}\cdot I_o}{2}\cdot\frac{Q_{gs2}\cdot R_g}{V_{plt}}$
	Voltage Falling Period	$\frac{V_{in}\cdot I_o}{2}\cdot\frac{Q_{gd}\cdot R_g}{V_{plt}}$
Turn off 	**Voltage Rising Period**	$\frac{V_{in}\cdot I_o}{2}\cdot\frac{Q_{gd}\cdot R_g}{V_{plt}}$
	Current Falling Period	$\frac{V_{in}\cdot I_o}{2}\cdot\frac{Q_{gs2}\cdot R_g}{V_{plt}}$

Table 4-1 Summary of simplified loss equations

The conduction loss of the top switch can be calculated as:

$$P_{cond}=I_o^2\cdot\frac{R_{dson,sp}}{N}\cdot\frac{V_o}{V_{in}} . \tag{4.15}$$

So the total loss of the top switch finally becomes:

$$P_{top}=\frac{V_{in}\cdot I_o}{2}\cdot(Q_{gd}+Q_{gs2})\cdot R_g\cdot(\frac{1}{V_{plt}}+\frac{1}{V_{DR}-V_{plt}})\cdot f_s+I_o^2\cdot R_{dson}\cdot\frac{V_o}{V_{in}} \tag{4.16}$$

which is essentially the sum of the turn-on loss, turn-off loss, and conduction loss.

4.3. Minimum loss and the importance of the Qgs2 factor

Applying the relationship of (4.1) and (4.2) into the top-switch total loss of Equation (4.16), it becomes:

$$P_{top}(N) = \frac{V_{in} \cdot I_o}{2} \cdot (Q_{gd,sp} + Q_{gs2,sp}) \cdot N \cdot R_g \cdot (\frac{1}{V_{plt}} + \frac{1}{V_{DR} - V_{plt}}) \cdot f_s + I_o^2 \cdot \frac{R_{dson,sp}}{N} \cdot \frac{V_o}{V_{in}} \qquad (4.17)$$

which means the total top-switch loss is a function of the number of cells in the device. When the number of cells in a device increases, the first two terms increase, which means the switching-related loss increases and the last term decreases, which in turn means the conduction loss decreases. Consequently the total top-switch loss exhibits a minimum loss point when

$$\frac{dP_{top}(N)}{dN} = 0. \qquad (4.18)$$

The point at which this occurs can be calculated as:

$$N_{opt} = \sqrt{\frac{I_o^2 \cdot \frac{V_o}{V_{in}} \cdot R_{dson,sp}}{\frac{V_{in} \cdot I_o}{2} \cdot R_g \cdot (\frac{1}{V_{plt}} + \frac{1}{V_{DR} - V_{plt}}) \cdot f_s \cdot (Q_{gd,sp} + Q_{gs2,sp})}}; \qquad (4.19)$$

when the minimum top switch loss will be achieved, which equals:

$$P_{top\_\min} = \sqrt{2 \cdot I_o^3 \cdot V_o \cdot R_g \cdot f_s} \cdot \sqrt{\frac{V_{DR}}{V_{plt} \cdot (V_{DR} - V_{plt})}} \cdot \sqrt{(Q_{gd,sp} + Q_{gs2,sp}) \cdot R_{dson,sp}} \qquad (4.20)$$

where N_{opt} is the optimized cell number associated with the minimum loss value.

When we substitute the optimized cell number of Equation (4.19) back into the first term of Equation (4.17), which is the switching loss, and the second term, which is the

conduction loss, we can derive the optimized device cell point at which the switching loss equals the conduction loss.

$$P_{sw} = P_{cond} = \frac{1}{2} P_{top\_\min} \tag{4.21}$$

This result is very obvious from a mathematical point of view. This is because all switching loss is proportional to the device's cell number, and all conduction loss is inversely proportional to the device's cell number. So the total device loss can be simplified as

$$P_{top}(N) = K_{sw} \cdot N + \frac{K_{cond}}{N} \tag{4.22}$$

where Ksw and Kcond are the coefficient-related switching loss and conduction loss. Calculating derivative $\frac{dP_{top}(N)}{dN} = 0$ would give:

$$N_{opt} = \sqrt{\frac{K_{cond}}{K_{sw}}} \text{ and} \tag{4.23}$$

$$P_{top} = 2\sqrt{K_{sw} K_{cond}} . \tag{4.24}$$

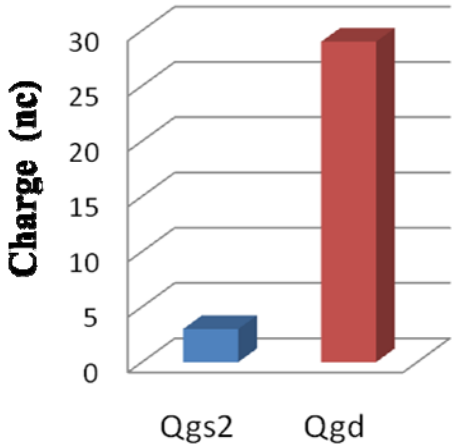
From Equation (4.20) we can observe that the total top-switch minimum loss is proportional to the square root of the product of charges *Qgd* and *Qgs2* and on-resistance *Rdson*. Comparing this with Equation (2.16), the most significant difference is that this second result includes the charge of *Qgs2*. So we must examine this question: how important is *Qgs2* in low-voltage devices and low-voltage applications?

As explained in Chapter 2, *Qgs2* is the total charge stored or removed from the inversion layer in order to conduct or cut off the channel current. This would indicate that in order to conduct a high current, which is usually what is done in a low-voltage application, the low-voltage-rated device needs to store a large amount of charge (*Qgs2*) in the inversion layer. Equation (4.21) shows this relationship.

$$Q_{gs2} = C_{iss} \frac{I_o}{g_{fs}} \tag{4.25}$$

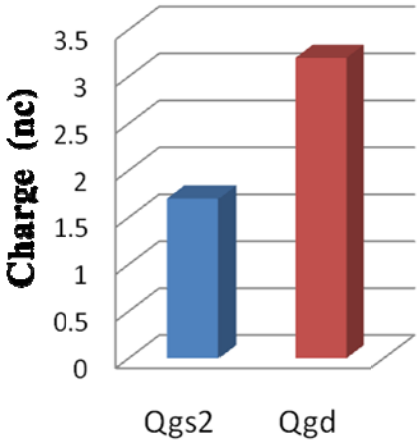
Compared with a high-voltage-rated device in which *Qgd* is much larger than *Qgs2*, in a low-voltage-rated device, *Qgs2* and *Qgd* value are very similar. Figure 4-2 shows the *Qgs2* and *Qgd* comparison between a high-voltage device and a low-voltage-rated device.

High voltage device



IRFP460A (600V) with 400V and 10.3A

Low voltage device

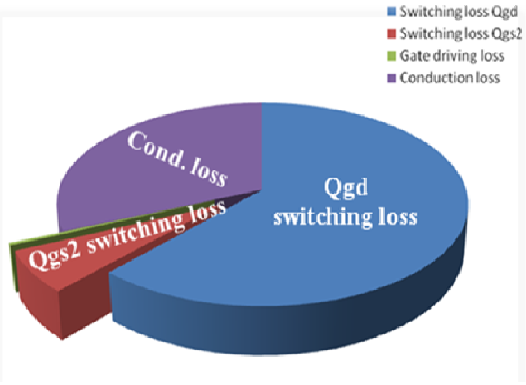


HAT2168 (30V) with 12V and 20A

Figure 4-2 Qgs2 V.S. Qgd for a low and high voltage device

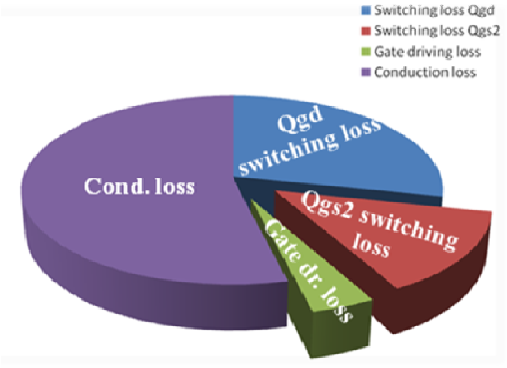
In terms of power loss, the Qgs2-related loss is also very important in low-voltage-rated devices and their applications. Figure 4-3 shows the loss breakdown for a 600V device, IRFP460A from International Rectifier, for a boost converter with 400V output and 10.3A peak current in a PFC application; and a 30V device, HAT2168 from Renesas, for a buck converter with a 12V input and a 20A peak current in a VRM application.

High-voltage device



IRFP460A (600V) with 400V and 10.3A

Low-voltage device



HAT2168 (30V) with 12V and 20A

Figure 4-3 Loss breakdown for a high and low voltage device

From Equation (4.19), we can see that the optimal number of cells in a device for different circuit conditions will be very different because the factor of *Qgs2* is considered. As explained previously, the number of cells in the device will be optimal when the switching loss equals the conduction loss. Because of the included the factor of *Qgs2*, the switching loss will increase tremendously. As Figure 4-5 shows, if we normalize the device HAT2168 cell number to be one, we can calculate the switching loss under different cell numbers (12V Vin, 1.2V Vo and 20A per phase) by sweeping the device cell number. The resulting loss curves show that including *Qgs2* will greatly increase the switching loss.

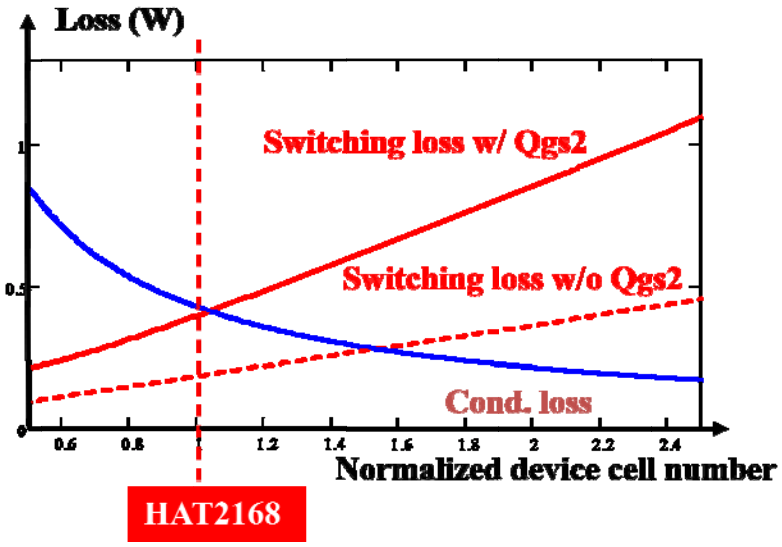


Figure 4-4 Qgs2 is an important factor to the switching loss

Because of the increasing of switching loss, the optimized cell number will be quite different from the previous instance, as shown in Figure 4-4.

4.4. Summary

By simplifying the accurate loss model based on the ideal packing method, we can observe that besides the *Qgd* factor, *Qgs2* is another important factor, especially in low-voltage applications. In a low-voltage device, the *Qgs2* factor is almost as important as

the *Qgd* factor, and without *Qgs2*, both the device minimum loss and the device optimized cell number will be misinterpreted.

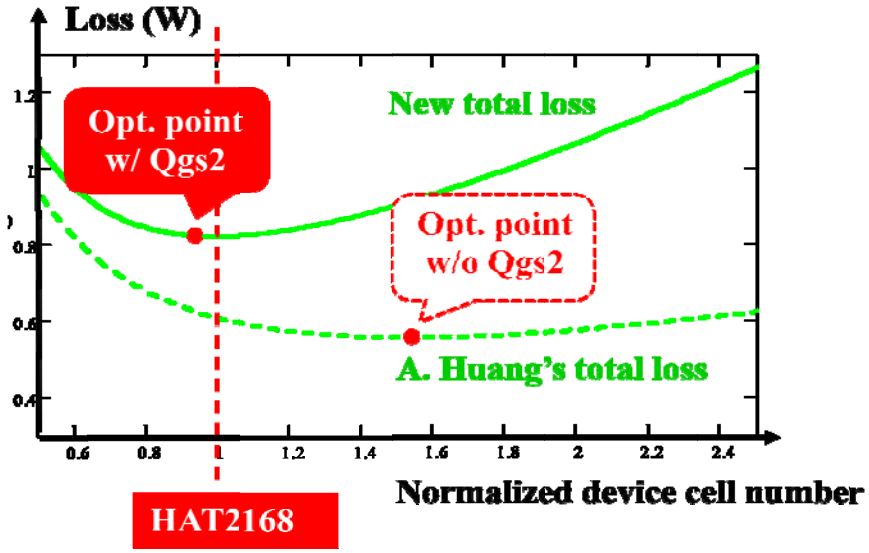


Figure 4-5 Qgs2 is an important factor to device selection

Chapter 5 Importance of the Gate Driving Voltage and a New Figure-of-Merit

5.1. Relationship between Pcond, Pdr and Vdr

Chapter 4 shows that the charge *Qgs2* is an important factor which should be considered in a low-voltage application. In addition to the factor of *Qgs2*, the gate driving voltage is another critical factor which will influence turn-on loss, conduction loss and gate driving loss.

Figure 5.1 shows a typical gate-charging waveform from a MOSFET datasheet. It is shown that the total gate charge *Qg* is a function of the gate driving voltage and the gate charge will increase by increasing the gate driving voltage.

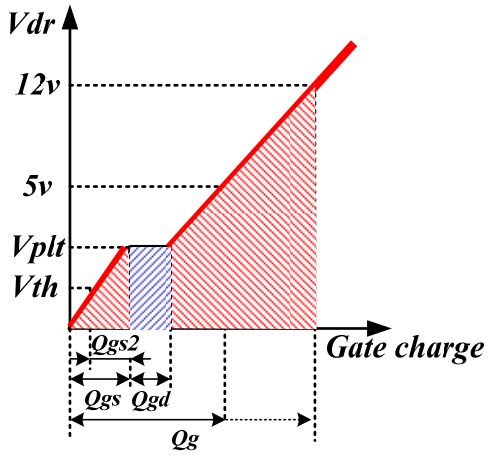


Figure 5-1 A typical gate charging waveform

From the charging waveform, we can observe that there are three charging periods. These are: charging before the plateau, charging during the plateau, and charging after the plateau. In terms of the equivalent circuit, theoretically the gate current charges the input capacitor (*Cgs*||*Cgd*) both in before and after the plateau period, as shown in Figure 5.2.

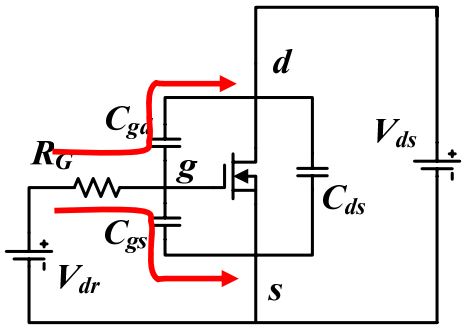


Figure 5-2 Equivalent gate charging circuit before and after plateau

Usually for a Trench MOSFET, the gate-to-source (*Cgs*) capacitor is much larger than the gate-to-drain (*Cgd*) capacitor. The gate-to-source capacitor is quite constant in terms of the Vds voltage. In essence, the gate-charging slope before and after the plateau is almost the same as the red curve in Figure 5.1. Then *Qg* can be broken into a function of *Qgs2* and *Qgd* in terms of the driving voltage.

$$Q_g(V_{DR}) = Q_{gs2} \cdot \frac{V_{DR}}{V_{plt} - V_{th}} + Q_{gd} \tag{5.1}$$

The gate driving loss equals:

$$P_{DR}(V_{DR}) = Q_g(V_{DR}) \cdot V_{DR} \cdot f_s = Q_{gs2} \cdot V_{DR}^2 \cdot \frac{f_s}{V_{plt} - V_{th}} + Q_{gd} \cdot V_{DR} \cdot f_s . \tag{5.2}$$

From (5.2) we can observe that the gate driving loss has a quadratic coefficient for the *Qgs2* term, which means that for a high driving voltage the gate driving loss will be tremendously increased if the *Qgs2* is large. In the other words, *Qgs2* is much more important than Qgd in the case of a high gate driving voltage.

Figure 5-3 shows another important factor, the on resistance, which is also a function of the gate driving voltage. It is very obvious from the curve that a high driving voltage could greatly reduce the on-resistance value and essentially reduce the conduction loss.
From [8] we know that when a MOSFET works in the linear region, which is marked in Figure 5-4, the drain-to-source current (*Ids*) and drain-to-source voltage (*Vds*) have the following relationship:

$$I_D = \mu_e \frac{w_g}{L_g} C_{ox}(V_{GS} - V_{th})V_{DS} = K(V_{GS} - V_{th})V_{DS} \tag{5.3}$$

where K is often referred as *"the device transconductance parameter"*.

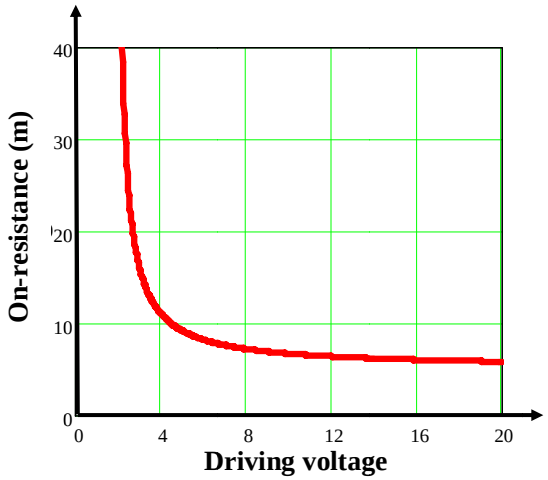


Figure 5-3 On-resistance vs. gate driving voltage

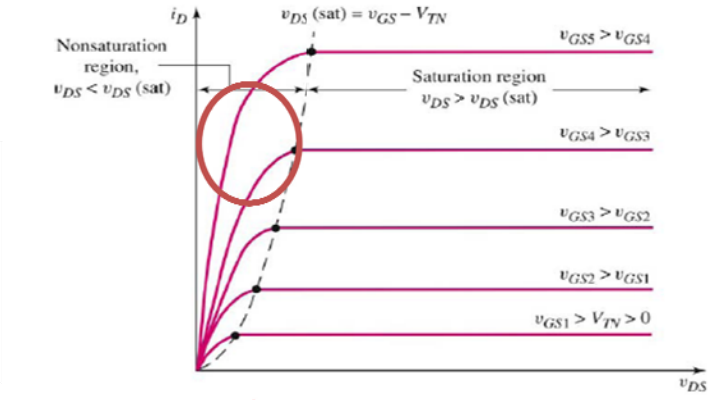


Figure 5-4 Linear region of MOSFET

From Equation (5.3) we can determine that the channel resistance equals

$$R_{ch}(V_{DR}) = \frac{L_g}{w_g \mu_e C_{ox}} \cdot \frac{1}{(V_{GS} - V_{th})} = \frac{1}{k(V_{GS} - V_{th})} \tag{5.4}$$

which is a function of the gate driving voltage.

Therefore the total on-resistance can be derived as

$$R_{dson}(V_{DR}) = R_{ch}(V_{DR}) + R_{Sub} + R_{Epi} = \frac{1}{k(V_{GS} - V_{th})} + C \tag{5.5}$$

where *Rsub* and *Repi* are the resistance of the sub-layer and epi-layer, which both can be treated as constant in terms of the gate driving voltage.

Usually the device datasheet will provide two data points for the Rdson value under different driving voltages. Using these two values, we can solve for the two coefficients *K* and *C*.

Using a high driving voltage will increase the gate driving loss and decrease the conduction loss because both the gate charge (*Qg*) and the on-resistance (*Rdson*) are functions of the gate driving voltage. As follows, there is always an optimum gate driving voltage which is a tradeoff between the gate driving loss and the conduction loss. Figure 5-5 shows a loss breakdown comparison between a 5V gate drive and a 12V gate drive for a Renesas device RJK0305DPB running in a buck converter from 12V down to 1.2V, with 20A per phase and at a 600kHz frequency. From the loss breakdown, we can see that the gate driver loss needs to be included in the total loss model to find the optimized gate drive voltage.

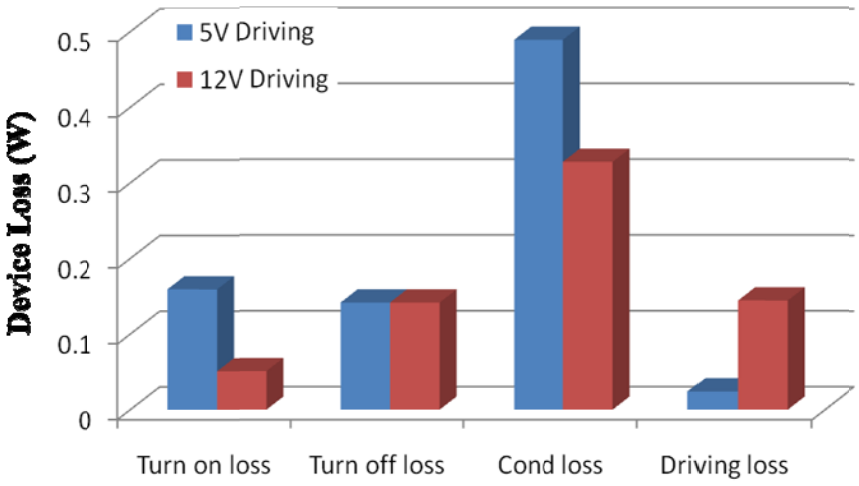


Figure 5-5 Loss breakdown for 5V and 12V driving

5.2. Loss model with the factor of gate driving voltage

By including the gate driver loss into the total loss equation shown in Equation 4.16, it becomes:

$$P_{top} = \frac{V_{in} \cdot I_o}{2} \cdot (Q_{gd} + Q_{gs2}) \cdot R_g \cdot (\frac{1}{V_{plt}} + \frac{1}{V_{DR} - V_{plt}}) \cdot f_s + Q_g \cdot V_{DR} \cdot f_s + I_o^2 \cdot R_{dson} \cdot \frac{V_o}{V_{in}} \quad (5.6)$$

where the last term represents the gate driving loss.

Using the same argument as the previous chapter that the MOSFET is built by paralleling a large amount of identical cells inside, we can directly apply Equations (4.1) and (4.2) and the knowledge that the total loss is a function of device cell number (N).

$$P_{top}(N) = \frac{V_{in} \cdot I_o}{2} \cdot \frac{(Q_{gd,sp} + Q_{gs2,sp}) \cdot N \cdot R_g}{V_{DR} - V_{plt}} \cdot f_s + \frac{V_{in} \cdot I_o}{2} \cdot \frac{(Q_{gd,sp} + Q_{gs2,sp}) \cdot N \cdot R_g}{V_{plt}} \cdot f_s$$
$$+ V_{DR} \cdot f_s \cdot Q_{g,sp} \cdot N + I_o^2 \cdot \frac{R_{dson,sp}}{N} \cdot \frac{V_o}{V_{in}} \quad (5.7)$$

The same is true when the device cell number increases. Here the first three terms increase, which means the switching-related loss increases and the last term decreases, which means the conduction loss decreases. Consequently the total top-switch loss exhibits a minimum loss point when

$$\frac{dP_{top}(N)}{dN} = 0 \quad (5.8)$$

which is when

$$N_{opt} = \sqrt{\frac{2 \cdot I_o^2 \cdot V_o}{V_{in}^2 \cdot I_o \cdot R_g \cdot f_s} \cdot \frac{V_{plt} \cdot (V_{DR} - V_{plt})}{V_{DR}} \cdot \frac{R_{dson,sp}}{(Q_{gd,sp} + Q_{gs2,sp} + \frac{2 \cdot V_{plt} \cdot (V_{DR} - V_{plt})}{V_{in} \cdot I_o \cdot R_g} \cdot Q_{g,sp})}} \quad (5.9)$$

And the minimum total top switch loss equals

$$P_{top\_\min} = \sqrt{2 \cdot I_o^3 \cdot V_o \cdot R_g \cdot f_s} \cdot \sqrt{\frac{V_{DR}}{V_{plt} \cdot (V_{DR} - V_{plt})}} \cdot \sqrt{(Q_{gd,sp} + Q_{gs2,sp} + \frac{2 \cdot V_{plt} \cdot (V_{DR} - V_{plt})}{V_{in} \cdot I_o \cdot R_g} \cdot Q_{g,sp}) \cdot R_{dson,sp}} \quad (5.10)$$

To analyze the influence of the gate driving voltage (*Vdr*), it is very important to understand that both the gate charge (*Qg*) and the on-resistance (*Rdson*) are functions of the gate driving voltage (*Vdr*) shown in Equations (5.1) and (5.4).

By substituting Equation (5.1) and (5.4) into (5.9) and (5.10), the minimum loss becomes:

$$P_{top\_\min} = \sqrt{2 \cdot I_o^3 \cdot V_o \cdot R_g \cdot f_s} \cdot \sqrt{\frac{V_{DR}}{V_{plt} \cdot (V_{DR} - V_{plt})}} \sqrt{(Q_{gd,sp} + K_{gs2} \cdot Q_{gs2,sp}) \cdot R_{dson,sp}} \quad (5.11)$$

when

$$N_{opt} = \sqrt{\frac{2 \cdot I_o^2 \cdot V_o}{V_{in}^2 \cdot I_o \cdot R_g \cdot f_s} \cdot \frac{V_{plt} \cdot (V_{DR} - V_{plt})}{V_{DR}} \cdot \frac{R_{dson,sp}}{(Q_{gd,sp} + K_{gs2} Q_{gs2,sp})}} \quad (5.12)$$

where Kgs2 represents the influence from the gate driving loss and is a function of the gate driving voltage.

$$K_{gs2}(V_{DR}) = 1 + \frac{V_{DR}}{V_{plt} - V_{th}} \frac{2V_{plt}(V_{DR} - V_{plt})}{V_{in} \cdot I_o \cdot R_g} \quad (5.13)$$

Figure 5-6 shows an example of *Kgs2* in term of the gate driving voltage (*Vdr*) for a Renesas RJK0305DPB device.

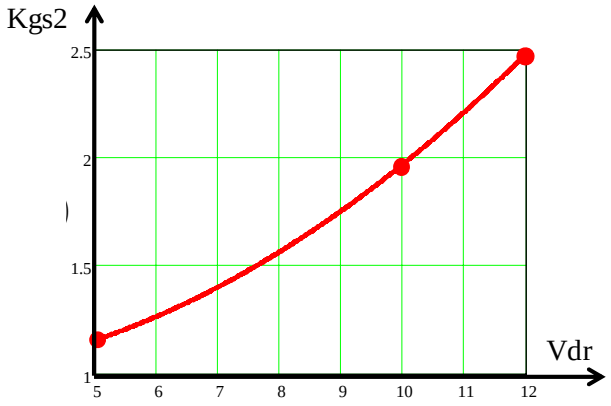
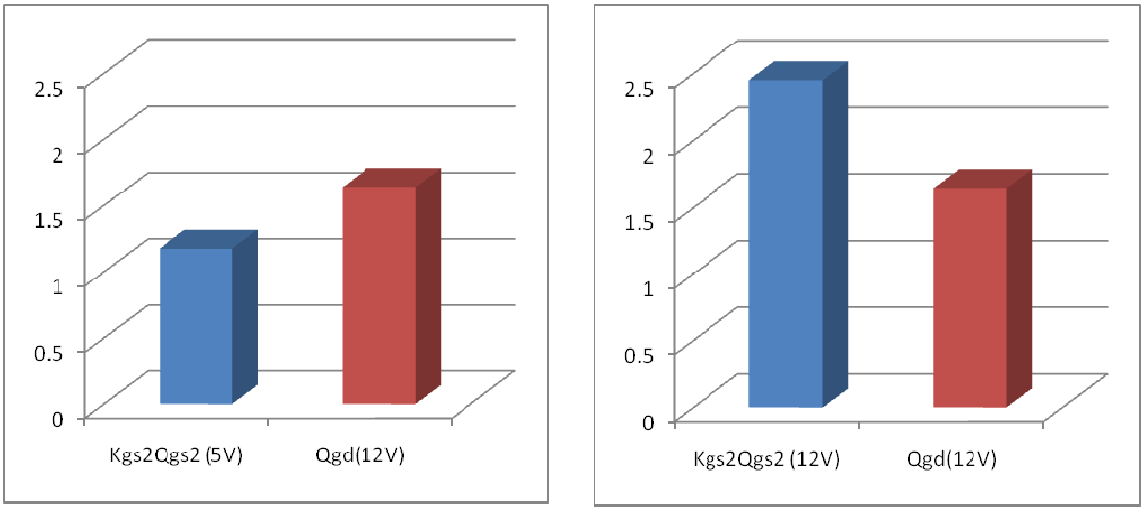


Figure 5-6 Kgs2 is a function of gate driving voltage

From the curve we can observe that *Kgs2* is quite non-linear in terms of the gate driving voltage, which reflects the quadratic effect of Qgs2 in the gate driving loss shown in Equation (5.2).

As shown in Figure 5-6, for a high driving voltage, the coefficient of *Qgs2* could be as high as 2.5, which makes *Kgs2Qgs2* a much more important term than the Qgd term. Figure 5-7 gives a comparison of the *Kgs2Qgs2* and *Qgd* of the Renesas RJK0305DPB under different driving voltages.



5V driving Kgs2=1.2 12V driving Kgs2=2.5

Figure 5-7 Comparison of Kgs2Qgs2 term and Qgd term under different driving voltage

From Equation (5.11) we can observe that the minimum device loss is related to threefactors. The first factor is the circuit parameters, such as input voltage (*Vin*), output voltage (*Vo*), load current (*Io*), and switching frequency (*fs*). The second factor is the gate driving voltage (*Vdr*). The third factor is the device parameters, such as the gate charges (*Qg*, *Qgs2*, *Qgd*) and on-resistance (*Rdson*).

5.3. New device figure-of-merit

The third part of Equation (5.11) is related to the device parameters, which means, under the same circuit conditions, a MOSFET with a minimum $(Q_{gd,sp} + K_{gs2} \cdot Q_{gs2,sp}) \cdot R_{dson,sp}$ value will achieve a minimum total top-switch loss.

Under the assumption discussed in Section 4.1, one series of devices should have the same product of the gate charge (*Qgd or Qgs2*) and on resistance (*Rdson*).

$$Q_{gd,sp} \cdot R_{dson,sp} = Q_{gd} \cdot R_{dson} \tag{5.14}$$

$$Q_{gs2,sp} \cdot R_{dson,sp} = Q_{gs2} \cdot R_{dson} \tag{5.15}$$

In addition, one series of devices from a manufacturer will have the same $(Q_{gd} + K_{gs2} \cdot Q_{gs2}) \cdot R_{dson}$ value, and this can be used to evaluate the device performance under the same circuit condition. A new device figure-of-merit is proposed as:

$$FOM = (Q_{gd} + K_{gs2} \cdot Q_{gs2}) \cdot R_{dson} \tag{5.16}$$

This figure-of-merit is based on a loss model which includes the factor of *Qgs2* and the gate driving loss. This is why this figure-of-merit should be a better indicator of the device minimum loss.

Device	Qgs2 (20A)	Qgd (12V)	Rdson (@5V 75º)	Qgd*Rdson	(Kgs2*Qgs2+Qgd)Rdson
Infineon OptiMOS3 (BSC090N03)	0.9nC	1.5nC	12.9m	19.61	30.83
Renesas D9 Trench (RJK0305DPB)	1nC	1.6nC	12.2m	20.01	31.96
Renesas D8 Trench (HAT2168)	1.1nC	2.7nC	10.7m	28.36	39.91
Vishay WFET (Si4390DY)	1.4nC	1.8nC	12.8m	23.55	41.09
IR Trench (IRF7823PBF)	1.8nC	2.9nC	11.3m	35.36	51.68
Infineon OptiMOS2 (BSC097N03)	1.2nC	2.6nC	13.6m	32.32	52.09
Vishay TrenchFET (SI4860DY)	1.7nC	2.6nC	13.4m	34.84	57.62

Table 5-1 List of commercial devices and their FOM values

Table 5-1 shows a list of several commercial device series from different companies. We can find the *Qgs2, Qgd* values at 12V and 20A per phase from the devices' datasheets. In

order to compare the figure-of-merit value with the minimum loss that each device is able to achieve, Yuancheng Ren's loss model can be used to calculate the minimum loss because it makes it easy to sweep the cell number in his model. By sweeping the cell number, the minimum loss of each series of devices at 12V input, 1.2V output, 20A per phase and 600kHz can be calculated as Figure 5-8 shows.

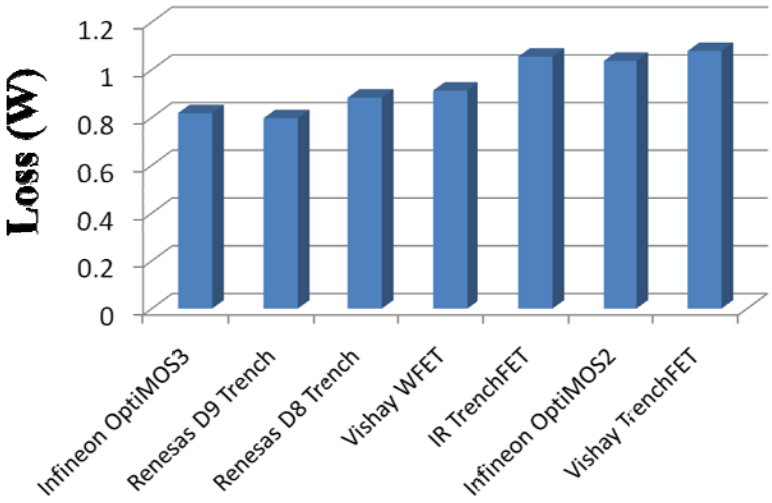


Figure 5-8 Minimum loss of different series of devices

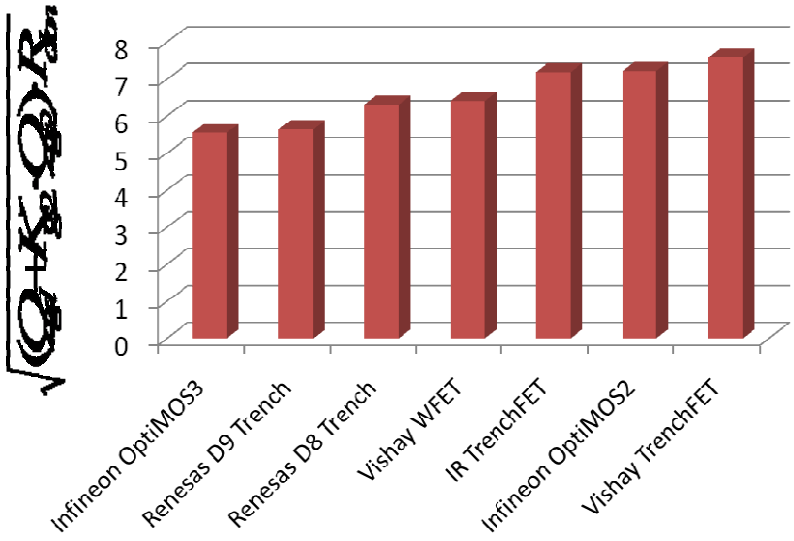


Figure 5-9 New FOM value of different series of devices

By comparing the minimum loss with new and previous figure-of-merit values shown in Figure 5-9 and Figure 5-10, we can see that the envelope of the new figure-of-merit is closer to the minimum loss of each device series.

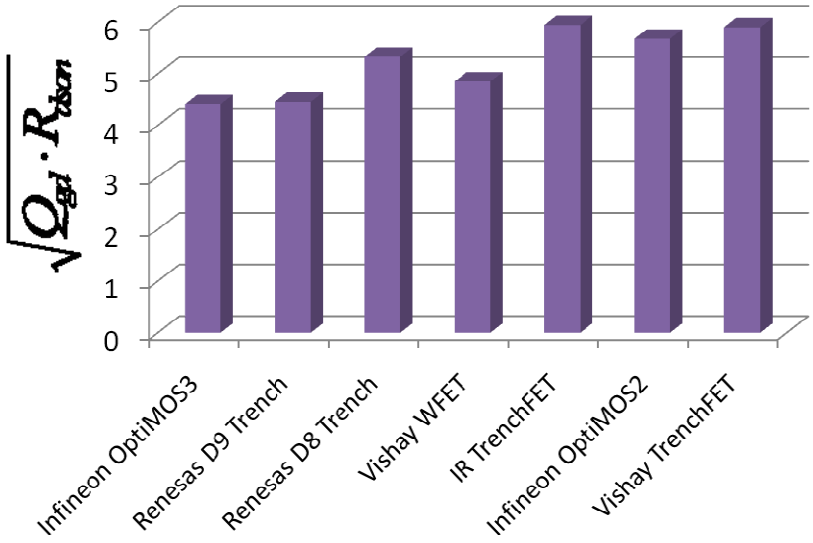


Figure 5-10 Previous FOM value of different series of devices

If we go one step further to find the reason behind this data, we can find out that the percentage of the *Qgs2* term is the cause of this discrepancy. Figure 5-11 shows the comparison of *Qgs2* percentage of each device series. From this figure we can see both a low and a high percentage will cause a mismatch with the previous figure-of-merit with minimum achievable loss. This is why the *Qgs2* term is an important term which should be included in the figure-of-merit, and also explains why the new figure-of-merit has a better indication of device minimum loss.

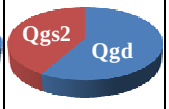
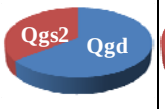
Infineon OptiMOS3	Renesas D9 Trench	Renesas D8 Trench	Vishay WFET	IR TrenchFET	Infineon OptiMOS2	Vishay TrenchFET
						
40.7%	41.8%	**32.8%**	**47.2%**	**35.6%**	42.3%	44%

Figure 5-11 Percentage of Qgs2 term for each device series

Infineon mentioned one Figure-of-Merit to compare MOSFET in one of their application notes which uses the product of the switching charge and on-resistance value[10].

Although it is not clearly mentioned and derived, I assume this FOM is proposed for the top switch device because the switching charge is defined as the charge which applies for a Vgs between the threshold voltage and the first rise after the plateau voltage (the end of the plateau). And the switching charge is basically the same as the sum of the *Qgs2* and *Qgd* charge.

Comparing with the FOM proposed by Infineon, the new proposed FOM has its benefit, especially in the high voltage gate driving case, because it includes the influence from gate driving loss. Figure 5-12 to Figure 5-15 shows a comparison between the FOM (*Qsw*Rdson*) proposed by Infineon and new proposed FOM at a 5V driving voltage with the device minimum loss for different device series. And from the comparison we can figure out that because the gate driving loss influence is small in the 5V driving case, both of the FOMs are able to well indicate the trend of the device minimum loss.

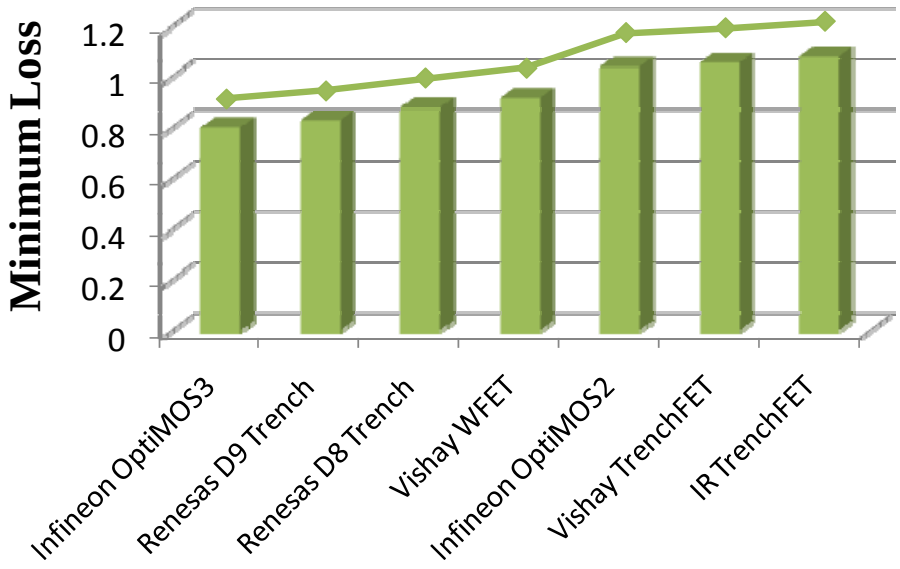


Figure 5-12 Minimum loss of different series of devices @5V

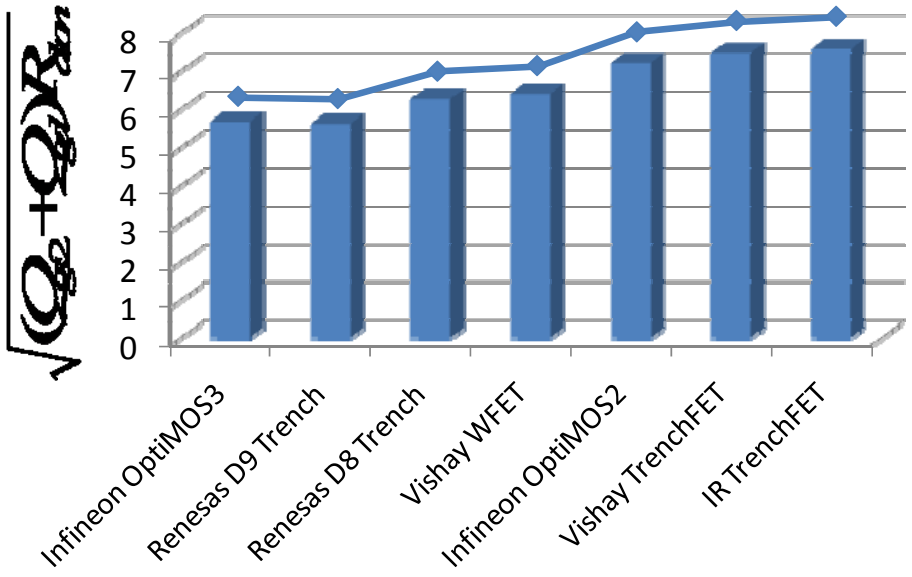


Figure 5-13 FOM (Qsw*Rdson) value of different series of devices @5V

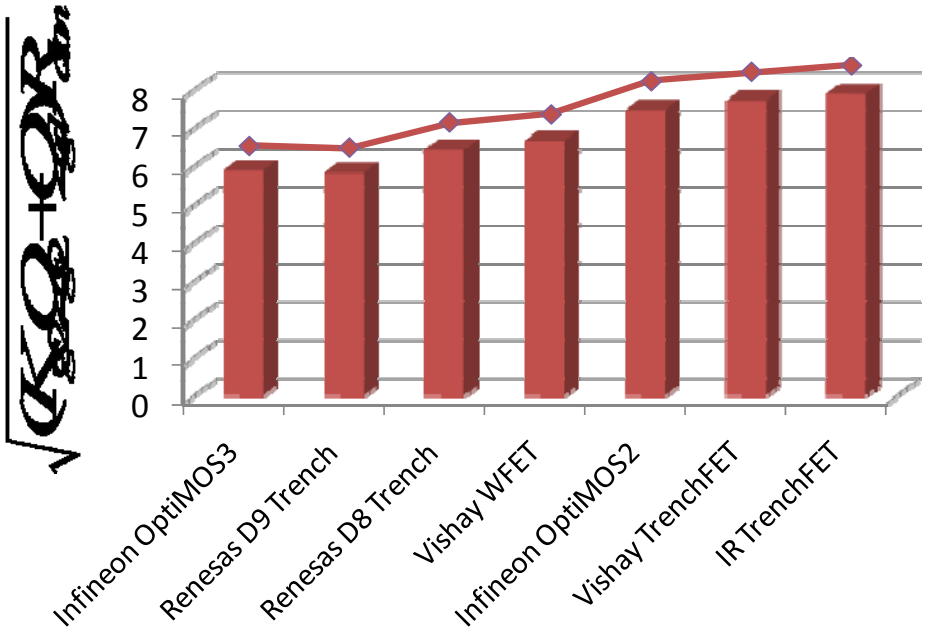


Figure 5-14 New FOM value of different series of devices @5V

Figure 5-15 to Figure 5-17 shows the same comparison at 8V driving voltage. Because the driving loss influence in the 8V driving case is bigger than the 5V driving case, we can observe that the FOM (Qsw*Rdson) proposed by Infineon shows some difference with the device minimum loss.

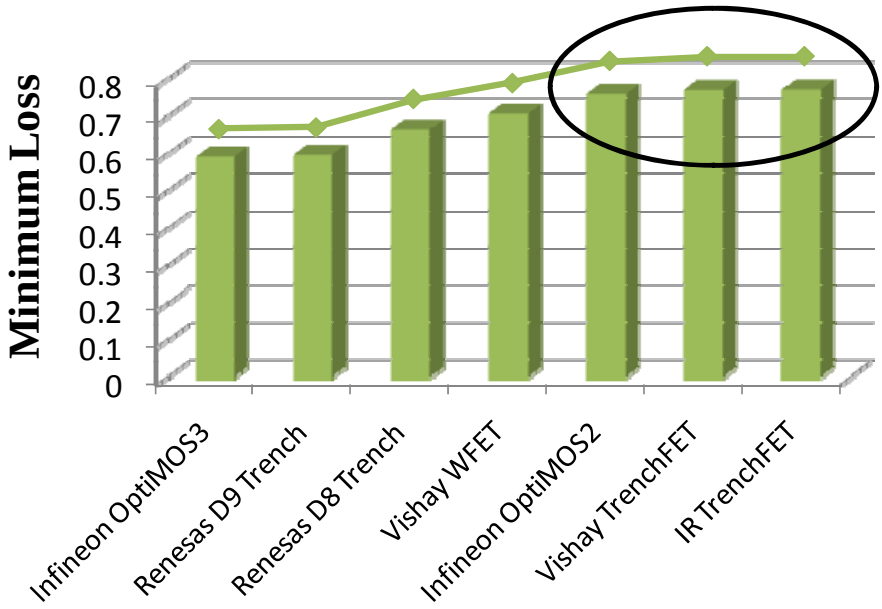


Figure 5-15 Minimum loss of different series of devices @8V

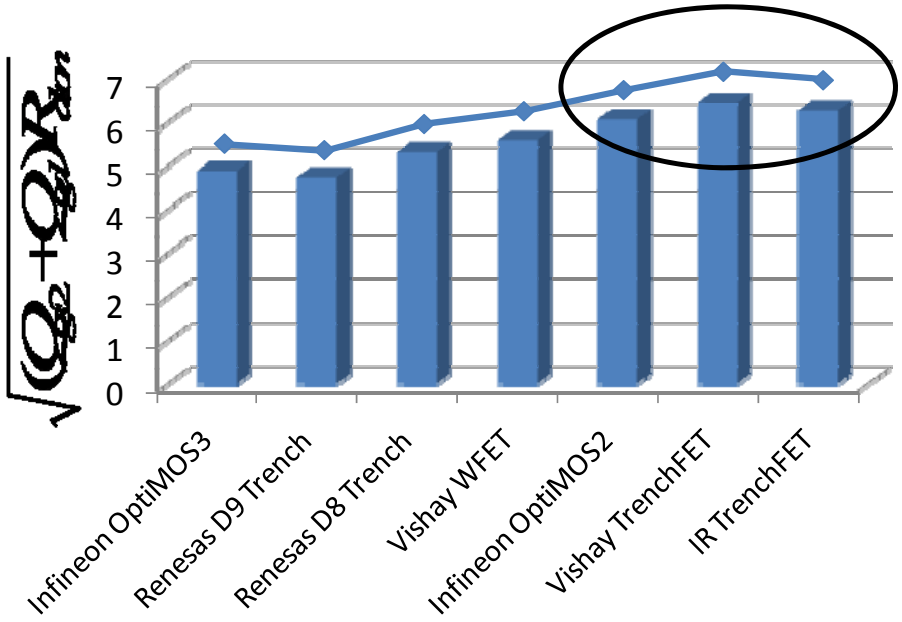


Figure 5-16 FOM (Qsw*Rdson) value of different series of devices @8V

Figure 5-18 to Figure 5-20 shows the same comparison at 12V driving voltage. We can observe that the FOM (*Qsw*Rdson*) proposed by Infineon shows large difference with the device minimum loss in the 12V driving case because of the big gate driving loss influence.

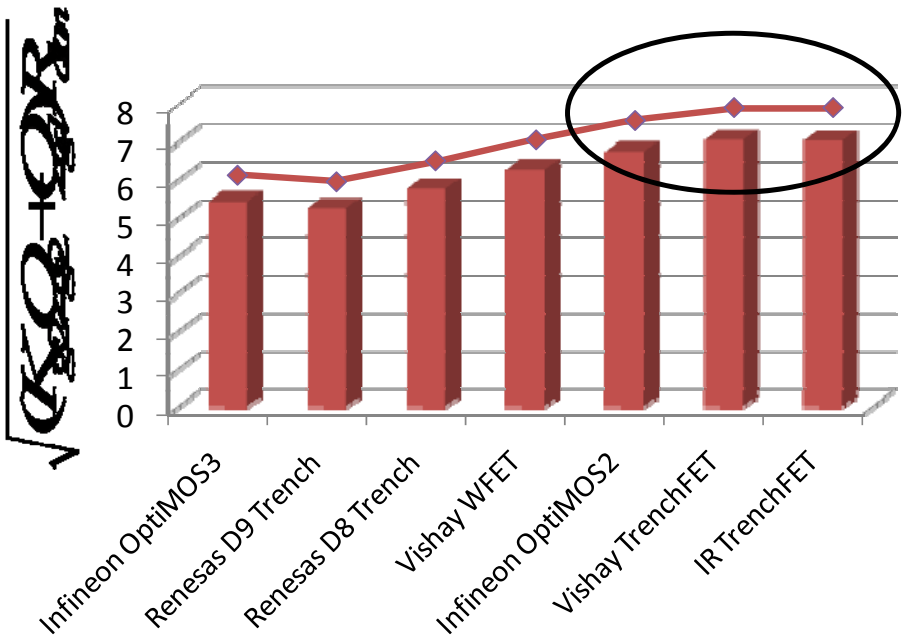


Figure 5-17 New FOM value of different series of devices @8V

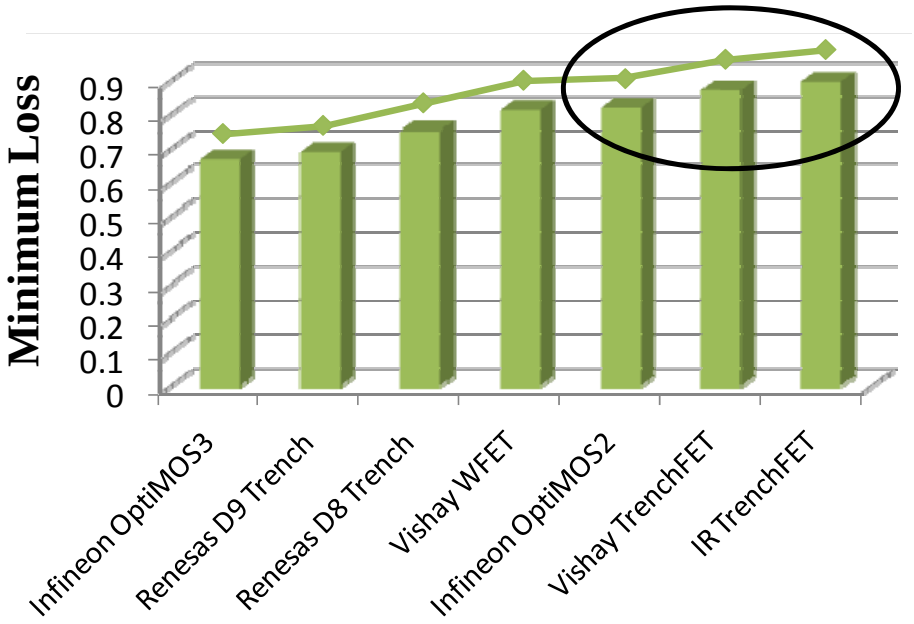


Figure 5-18 Minimum loss of different series of devices @12V

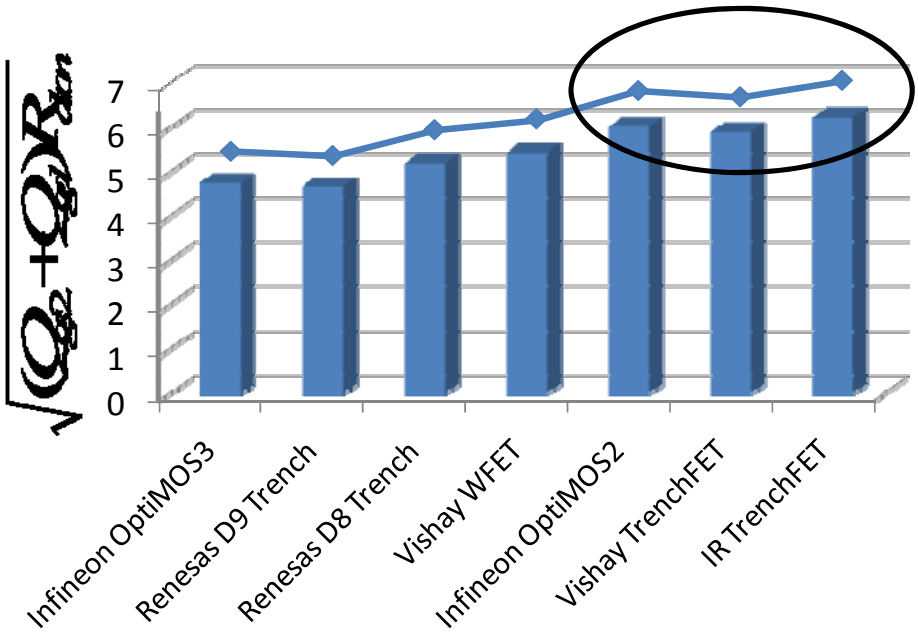


Figure 5-19 FOM (Qsw*Rdson) value of different series of devices @12V

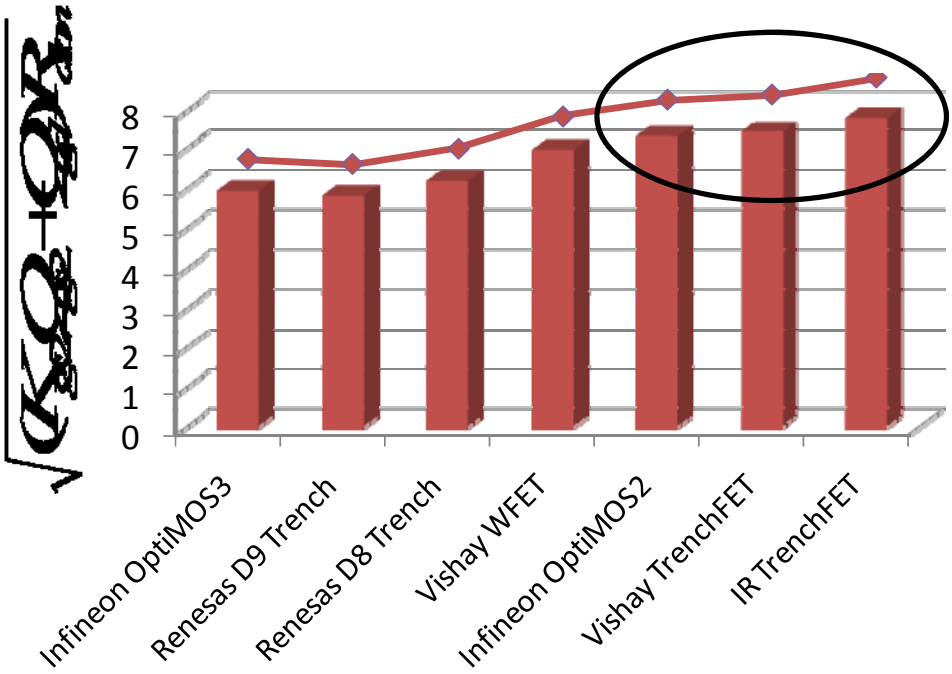


Figure 5-20 New FOM value of different series of devices @12V

5.4. New Normalized Power Loss

As we discussed above, the driving voltage is another important parameter that requires a tradeoff between the conduction loss and gate driving loss. Different devices at different driving voltages will have different performances, so for the circuit designer, it is important to select the driving voltage together with the device to achieve total minimum loss. When we take a look at the minimum loss equation (5.11), only the second term is related to the driving voltage; so combining the second term with the third term is like a normalized minimum power loss, and this can be used to select the driving voltage and device at the same time.

The proposed normalized power loss equation:

$$NPL(V_{DR}) = \frac{V_{DR}}{V_{plt} \cdot (V_{DR} - V_{plt})} (Q_{gd} + K_{gs2}(V_{DR}) \cdot Q_{gs2}) \cdot R_{dson}(V_{DR}) \qquad (5.17)$$

where the normalized power loss is a function of the gate driving voltage, and *Kgs2* is the same definition given in (5.12).

Because one series of devices should have the same product of gate charge (*Qgd or Qgs2*) and on resistance (*Rdson*), it should also have the same normalized power loss. Therefore we can map one series of device into a parabolic curve by using *Rdson* as the x axis and using $\frac{V_{DR} \cdot (Q_{gd} + K_{gs2} \cdot Q_{gs2})}{V_{plt} \cdot (V_{DR} - V_{plt})}$ as the y axis. Figure 5-21 shows an example of the Renesas D9 trench MOSFET device series. There are four devices with different gate charges and on-resistance values, but they are all located in the same parabolic curve. Either a different device series with a different gate charge (*Qgd, Qgs2*) and a different on-resistance (*Rdson*) or a different driving voltage (*Vdr*) will cause a different normalized power loss value, which would generate a different parabolic curve. The combination of the device and driving voltage with the smaller normalized power loss value could achieve the minimum device loss.

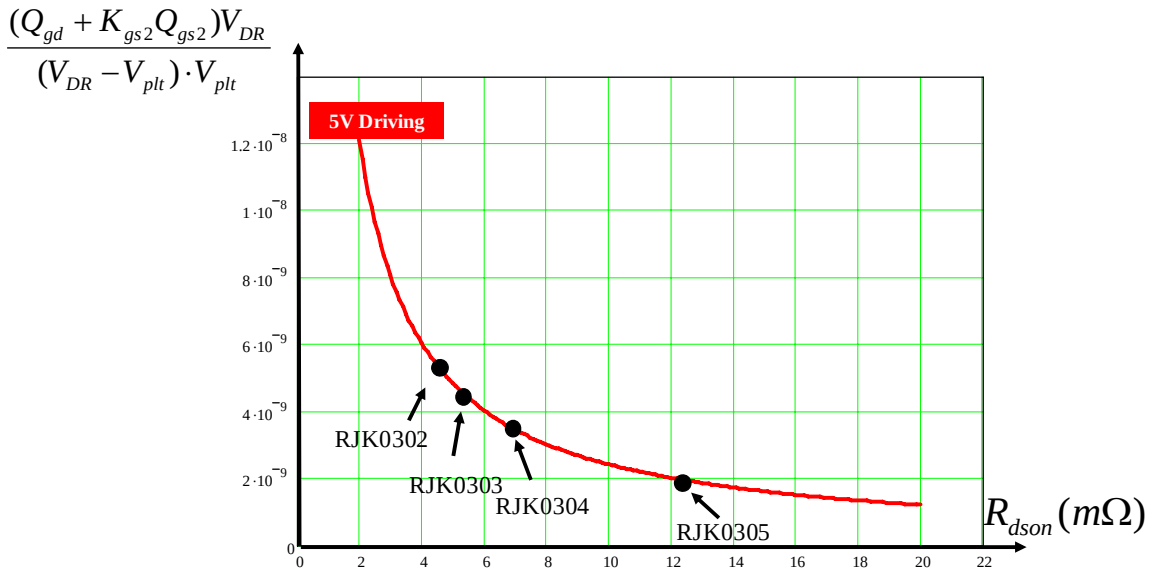


Figure 5-21 Map Renesas D9 Trench MOSFET series into one parabolic curve

From Equation (5.12) we know that, in one series of devices, only the device with the optimized cell number (*Nopt*) can achieve the minimum loss. Under different circuit conditions, such as a different load current or a different switching frequency, the optimized cell number would be charged.

However, to a circuit designer, the optimized cell number value is not so obvious and it cannot be used directly. So alternatively we can use the ratio between $\frac{V_{DR}\cdot(Q_{gd}+K_{gs2}\cdot Q_{gs2})}{V_{plt}\cdot(V_{DR}-V_{plt})}$ and *Rdson* to determine which device has the optimized number, because

$$\frac{\frac{(Q_{gd}+K_{gs2}\cdot Q_{gs2})\cdot V_{DR}}{V_{plt}\cdot(V_{DR}-V_{plt})}}{R_{dson}}=\frac{\frac{(Q_{gd,sp}+K_{gs2}\cdot Q_{gs2,sp})\cdot V_{DR}}{V_{plt}\cdot(V_{DR}-V_{plt})}\cdot N_{opt}^{2}}{R_{dson,sp}}, \tag{5.18}$$

which means the ratio is one-to-one related to the optimized cell number.

Substituting Equation (5.12) into (5.18), we obtain:

$$\frac{\dfrac{(Q_{gd}+K_{gs2}\cdot Q_{gs2})\cdot V_{DR}}{V_{plt}\cdot(V_{DR}-V_{plt})}}{R_{dson}} = \frac{\dfrac{(Q_{gd,sp}+K_{gs2}\cdot Q_{gs2,sp})\cdot V_{DR}}{V_{plt}\cdot(V_{DR}-V_{plt})}\cdot N_{opt}}{\dfrac{R_{dson,sp}}{N_{opt}}} = \frac{2\cdot I_o\cdot V_o}{V_{in}^2\cdot R_g\cdot f_s} \qquad (5.19)$$

which means the device with the optimized cell number should satisfy this ratio, which is related to only some of the circuit parameters.

With this ratio, we can draw a second straight line on Figure 5-21; this second line is shown in Figure 5-22. The optimized device is located at the intersecting point because it should satisfy the ratio in Equation (5.19). Different circuit conditions such as a different switching frequency would give a different straight line to yield a different optimized cell number.

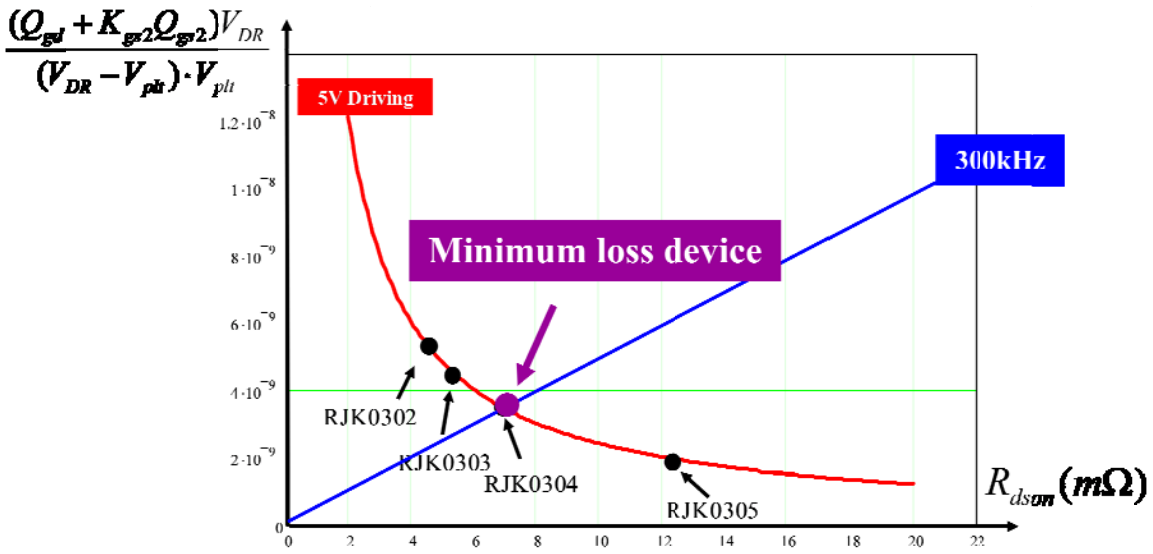


Figure 5-22 A straight line satisfies the optimized cell number

For example, for a VR application of 12V down to 1.2V and 20A per phase, the Renesas D9 Trench MOSFET series includes three devices optimized for the top switch under different switching frequencies. As Figure 5-23 shows, by using the method just introduced, it is very easy to find the optimized switching frequency for each device.

Among the three devices, the RJK0303DPB has the biggest die size. It is optimized at a 200kHz switching frequency because conduction loss is important. Usually for laptop applications, the light-load efficiency is very important. Therefore the state–of-the-art design is around 200kHz switching frequency and uses two phases to handle around a 40A load current. The loss breakdown in Figure 5-24 shows that the RJK0303DPB can indeed give a minimum loss at 200kHz when corrected with the other two devices.

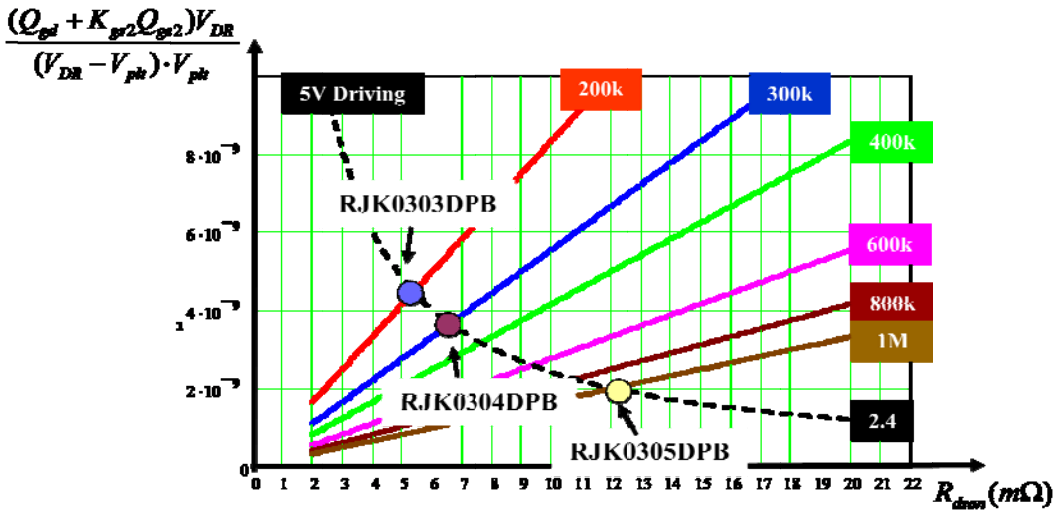


Figure 5-23 Renesas D9 Trench MOSFET series optimized at different switching frequencies

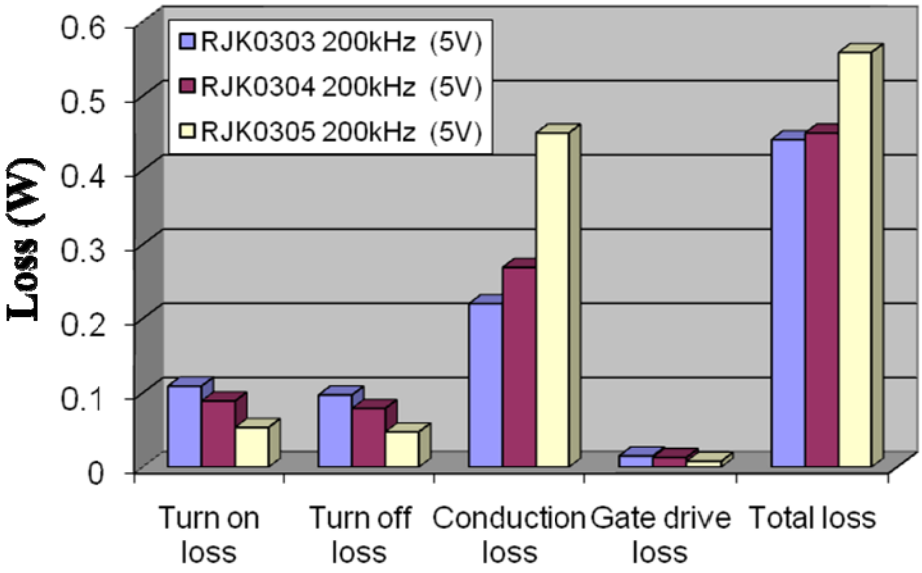


Figure 5-24 Loss breakdown for Renesas D9 devices for laptop application

This method can also be used to select devices from among different series of devices. For example, Figure 5-25 shows two curves, representing the Renesas current-generation D9 MOSFET series and the last-generation D8 MOSFET series. We can see both the device HAT2167 and RJK0304DPB are optimized at 300kHz, which is usually used in desktop applications. However, because RJK0304DPB (D9 generation) uses better device manufacturing technology, which reduces the *Qgs2*, *Qgd*, and *Rdson* values and generates a smaller normalized power loss, it will achieve better performance than the HAT2167 (D8 generation), as Figure 5-26 shows.

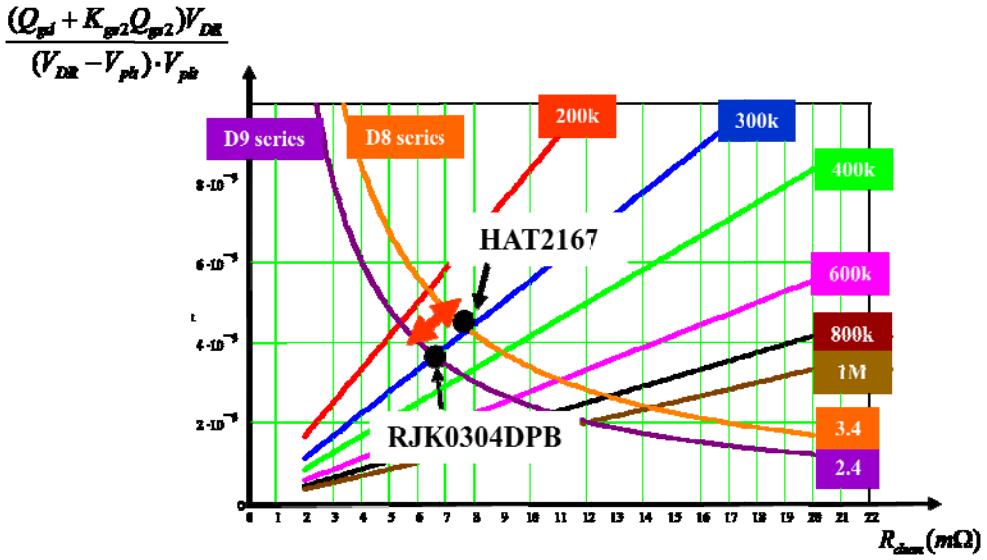


Figure 5-25 Renesas D9 MOSFET series vs. D8 MOSFET series

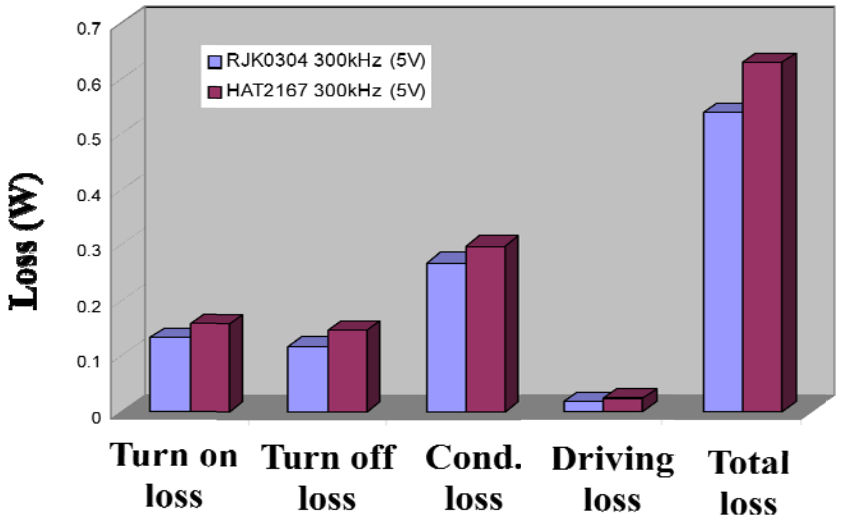


Figure 5-26 Loss breakdown of RJK0304DPB vs. HAT2168 at 300kHz

This method not only suitable for selecting among different series of devices, it can also be applied to selecting the optimized driving voltage at the same time. Figure 5-27 shows the use of two different driving voltages to drive the Renesas D9 series devices. From the curves we can see that by increasing the driving voltage from 5V to 7V, the same D9 device series could achieve an even smaller normalized power loss value. From the loss breakdown in Figure 5-28, we can see that a 7V driving voltage could achieve a 16.7% loss savings.

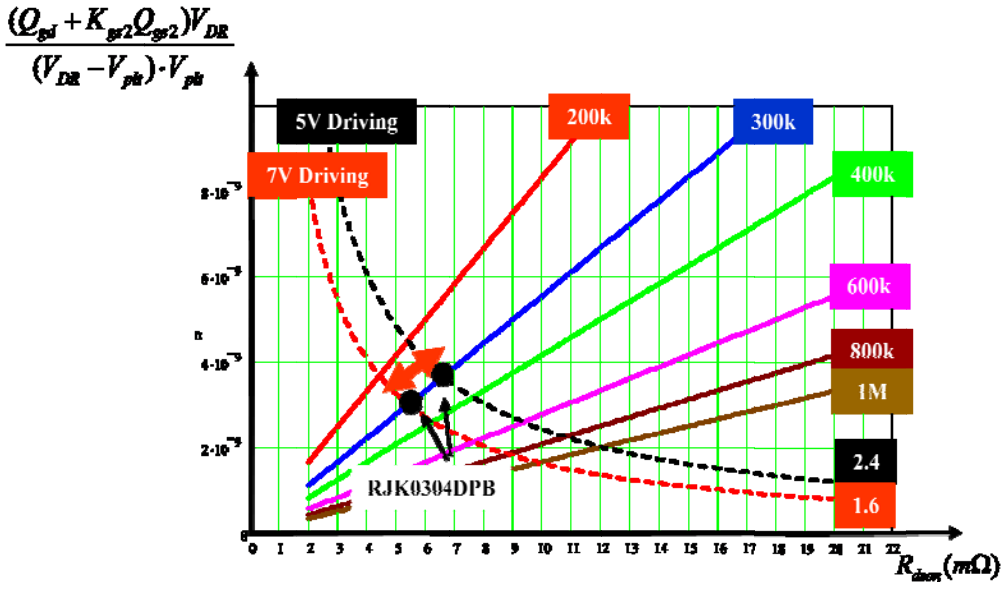


Figure 5-27 5V driving vs. 7V driving for Renesas D9 devices

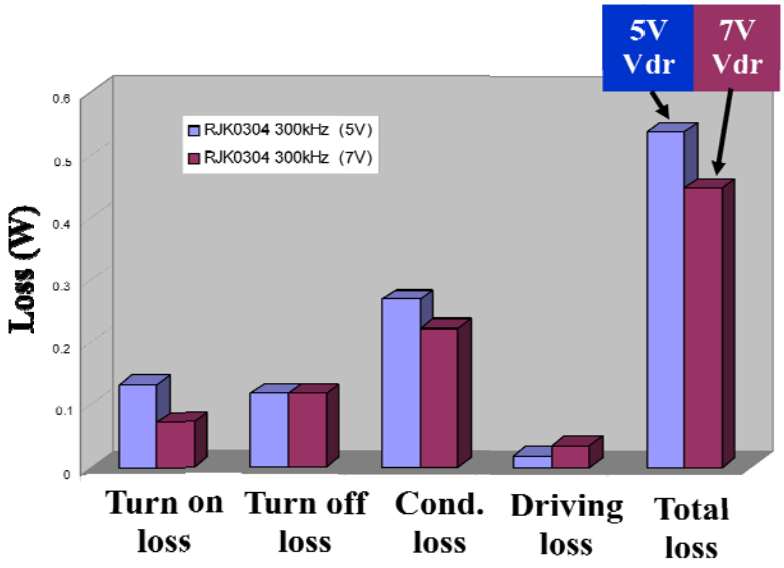


Figure 5-28 Breakdown of RJK0304DPB at 5V driving and 7V driving

One paper from TI also shows that a full load efficiency (5V to 1.8V 20A) gain of up to 1.7% can be realized when the MOSFET gates are driven at 9V as opposed to 5V [11]. The paper only provide a specific case to show the benefit of rising gate driving voltage but didn't provide a method to choose the optimized gate driving voltage for different circuit condition. But with the method proposed in Chapter 5.4, it is very easy to draw different Normalized Power Loss curves for different gate driving voltage case. And the one with the lowest calculated Normalized Power Loss value could give the minimum power loss.

5.5. Summary

The new proposed figure-of-merit includes the factor of the *Qgs2* and the factor of the gate driving voltage. The new FOM has a better indication of the device minimum loss than the previously accepted FOMs. A new simple method is proposed to select the device and driving voltage which to achieve the minimum loss.

Chapter 6 Importance of the Packaging Parasitics

6.1. MOSFET packaging parasitic inductor and its importance

To operate, the MOSFET must be connected to the external circuit using a certain packaging method. Different packaging methods use different ways to connect the MOSFET die to pins; for example, wire bonding, solid copper strap and so on. These packaging methods will introduce the packaging parasitic inductors which are shown in the MOSFET equivalent circuit in Figure 6-1.

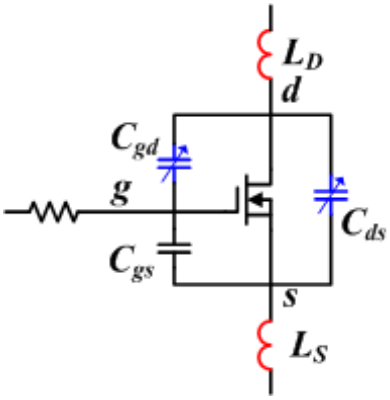


Figure 6-1 MOSFET equivalent circuit with packaging parasitcs

As shown in Figure 6-1, there are two very important packaging parasitic inductors; the common-source inductor (*Ls*) and the drain inductor (*Ld*). The common-source inductor (*Ls*) is defined as the inductor shared by the driving loop and main power loop. The drain inductor is defined as the drain-side loop inductor, which is also related to the layout. Both of these have an important effect on the total power loss which is discussed in paper [12][13].

Figure 6-2 shows the MOSFET equivalent circuit during the current rising period of the turn on. In that period, the main power-loop current (*Ids*) increases and generates a positive voltage on the common-source parasitic inductor (V_{LS}), as the figure shows.

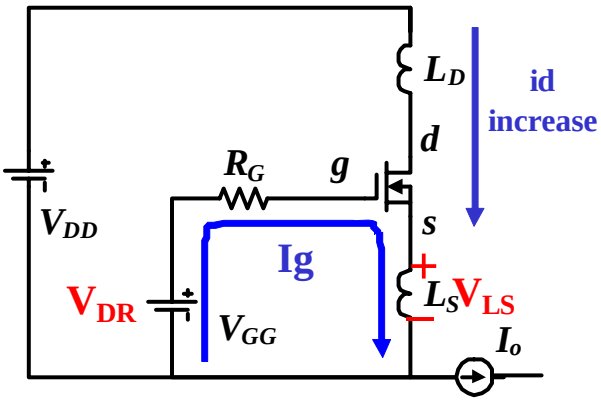
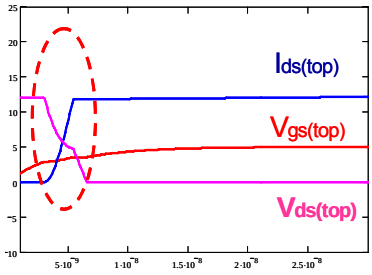


Figure 6-2 Impact of Ls during MOSFET turn-on

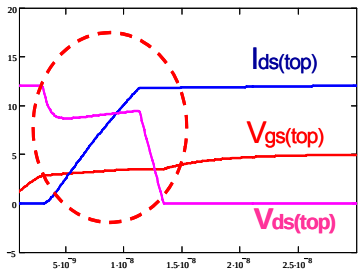
Because the voltage generated by the common-source parasitic inductor (V_{LS}) has a contradictory polarity with the driving voltage (V_{DR}), the driving current used to charge the input capacitor (*Ciss*) can be calculated as

$$I_g = \frac{V_{DR} - V_{Ls}}{R_G}. \tag{6.1}$$

From Equation (6.1) we can see that including the common-source parasitic inductor will reduce the gate driving speed, leading to a longer overlapping time of the voltage and current, which results in a higher switching loss.



Without Ls



With Ls

Figure 6-3 Impact of Ls during MOSFET turn-off

Figure 6-3 shows a comparison of the turn-on switching waveforms of a buck converter with and without the common-source parasitic inductor (*Ls*) under the same circuit operating conditions. From these waveforms we can observe that the current-rising time period will increase tremendously when the *Ls* parameter is considered.

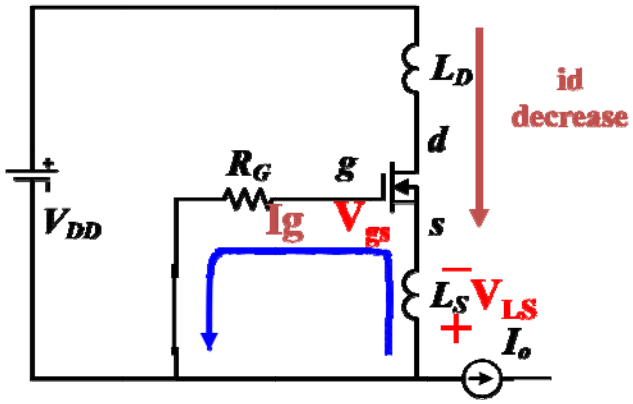


Figure 6-4 MOSFET equivalent circuit during current-falling of turn-off

The same analysis follows for the current-falling period during the turn-off of the top-switch; the equivalent circuit is shown in Figure 6-4. The voltage generated by the common-source parasitic inductor (V_{LS}) has a contradictory polarity with the drain-to-source voltage (*Vgs*), which is used to discharge the input capacitor (*Ciss*). Therefore, the driving current can be calculated as

$$I_g = \frac{V_{gs} - V_{Ls}}{R_G}. \tag{6.2}$$

Due to the effect of the common-source parasitic inductor (V_{LS}), the gate driving speed reduces, the overlapping time between voltage and current increases, and so the switching loss increases.

From the above analysis, we can see that the common-source parasitic inductor (*Ls*) will always have a negative effect by delaying the driving speed and thus increasing the switching loss. Figure 6-5 shows the switching loss analysis performed by sweeping the common-source parasitic inductor (*Ls*) of a Renesas RJK0305DPB MOSFET under 12V input, 1.2V output, 20A per phase and 1MHz 5V driving conditions.

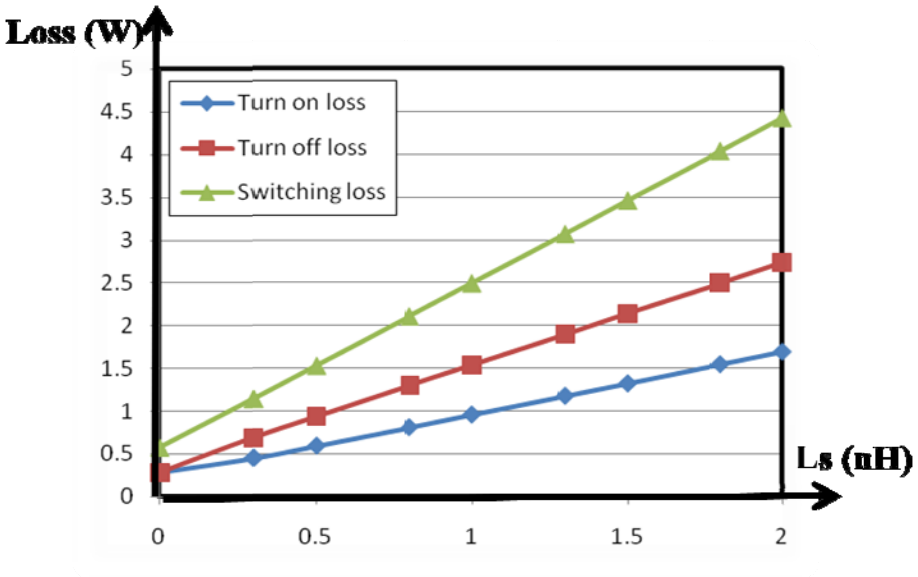


Figure 6-5 Switching loss analysis vs. the common-source parasitic inductor (Ls)

We observe that both turn-on and turn-off loss will increase by increasing the common-source parasitic inductance (*Ls*). The total switching loss is tremendously impacted by the common-source parasitic inductance (*Ls*).

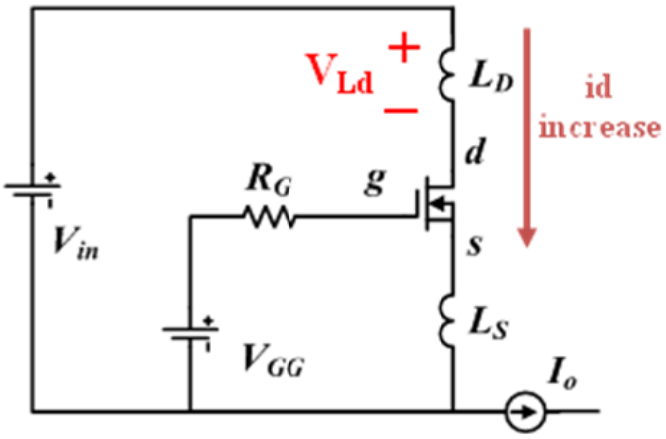


Figure 6-6 Impact of Ld during MOSFET turn on

The drain-side loop inductor (*Ld*) is not as critical as the common-source parasitic inductance (*Ls*), but it will play an important role if Ld is increased beyond a certain

value. Shown in Figure 6-6 is the equivalent circuit during the current-rising period of the turn-on of the top switch. When the channel current is increased, it will generate a positive voltage on the inductor Ld (V_{LD}). Because of this voltage, the voltage stress across the MOSFET drain and source (*Vds*) is reduced. The drain-to-source voltage is one contributory factor in the switching loss.

$$V_{ds} = V_{in} - V_{Ld} \tag{6.3}$$

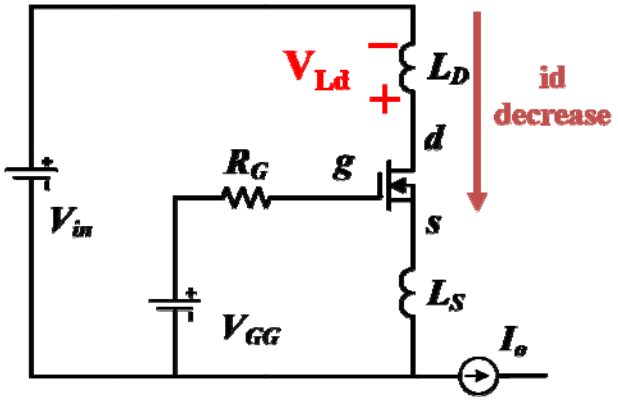


Figure 6-7 Impact of Ld during MOSFET turn-off

The equivalent circuit for the turn-off of the top switch is shown in Figure 6-7. When the channel current is decreased, it will generate a negative voltage on the inductor Ld (V_{LD}), which increases the voltage stress across the MOSFET drain and source (*Vds*).

$$V_{ds} = V_{in} + V_{Ld} \tag{6.4}$$

From the analysis we can see that the drain-side parasitic inductor (*Ld*) would decrease the turn-on loss but would increase the turn-off loss. Figure 6-8 gives an example of the switching loss breakdown of a Renesas RJK0305DPB MOSFET versus different drain-side parasitic inductors (*Ld*). The loss is calculated under a 12V input, 1.2V output, 20A per phase and 1MHz 5V driving condition.

From the curves shown in Figure 6-8, we can observe that increasing the drain-side parasitic inductor (*Ld*) will not significantly influence the total switching loss in some

ranges because the gain from the turn-on loss and the loss from the turn-off loss will cancel each other out.

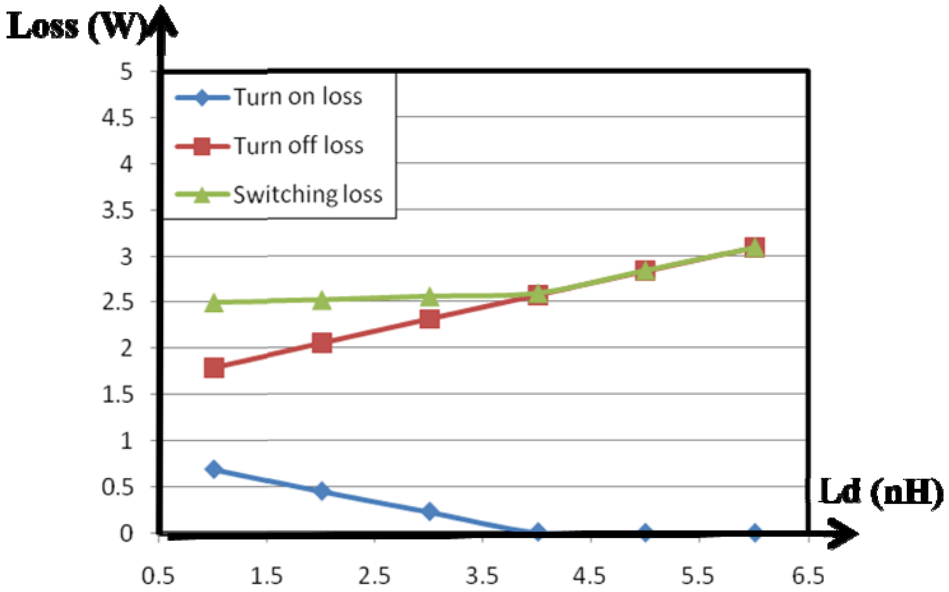


Figure 6-8 Switching loss breakdown vs. the drain side parasitic inductor (Ld)

6.2. Adding packaging parasitic inductor to loss model

From the previous analysis, we can see that the packaging parasitic inductor has a huge impact on the switching loss, especially the common-source parasitic inductor (*Ls*). Threrefore it is very important to include the packaging parasitic inductor parameter into our loss model.

The most difficult aspect of adding the packaging parasitic indutors into the loss model is the fact that that the common-source parasitic inductor (*Ls*) is shared by two loops, the gate driving loop and the main power flowing loop, as Figure 6-9 shows.

$$V_{Ls} = L_S\left(\frac{di_{gs}}{dt} + \frac{di_{ds}}{dt}\right) \tag{6.5}$$

To decouple the voltage drop from the two loops, it is assumed that the slew rate of the MOSFET channel current is much larger than its gate current.

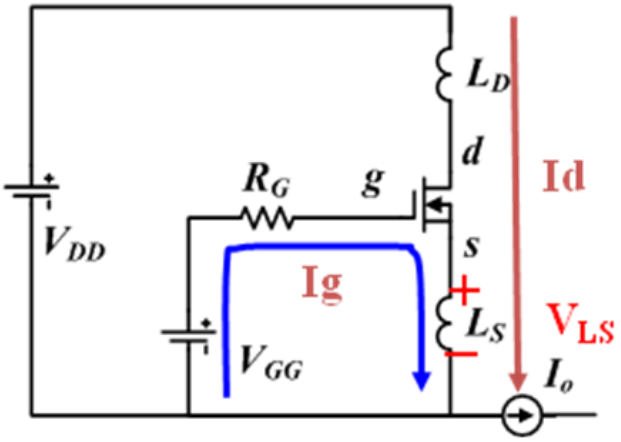


Figure 6-9 Ls is shared by two loops

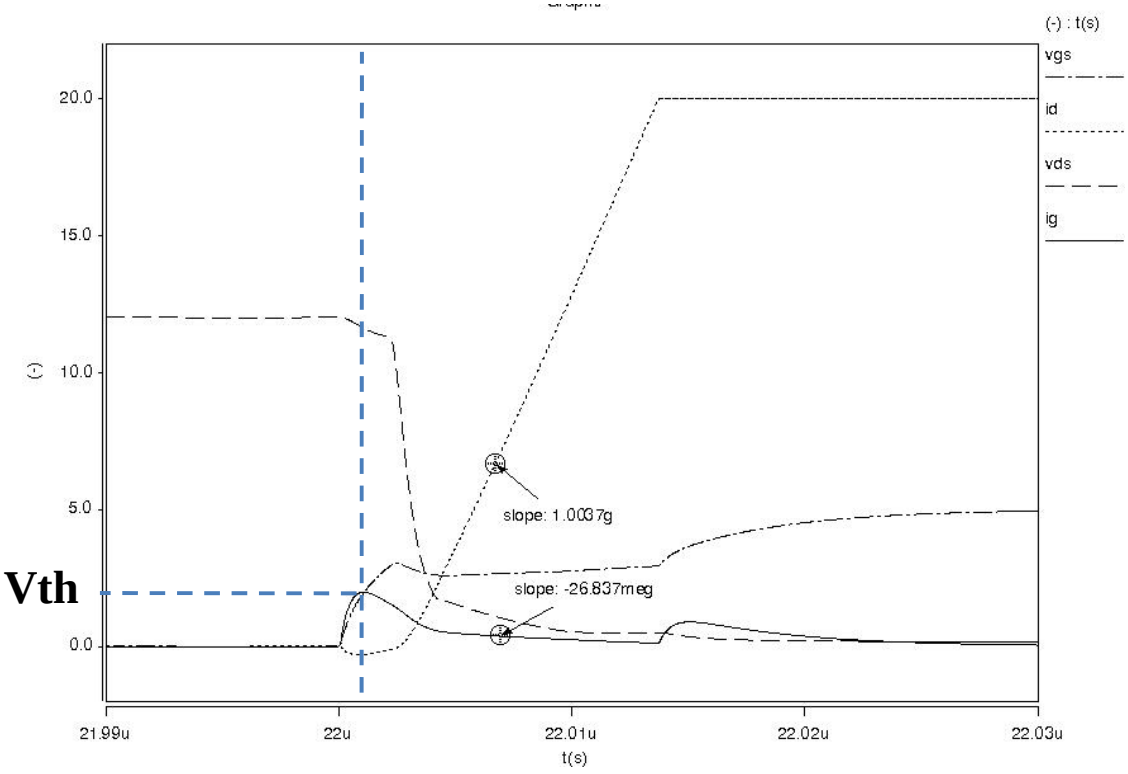


Figure 6-10 Drain to source current V.S. Gate to source current

Figure 6-10 shows a simulation result of the Renesas HAT2168 MOSFET turn on waveform under a step gate driving voltage (5V). From the result we can see that, before

the gate-to-source voltage (*Vgs*) reaches the threshould voltage (*Vth*), the gate current will charge the MOSFET input capacitor (Ciss) via a RLC resonant network.

So we can get the following second order differential equation:

$$L_s C_{iss} \frac{d^2 u_{ciss}}{dt^2} + R_g C_{iss} \frac{du_{ciss}}{dt} + u_{ciss} = V_{DR} \tag{6.6}$$

Because $R_g > 2\sqrt{\frac{L_s}{C_{iss}}}$, differential equation (6.6) has a general solution:

$$u_{ch}(t) = A_1 e^{s_1 t} + A_2 e^{s_2 t} \tag{6.7}$$

where $s_1 = \frac{-R_g}{2L_s} + \sqrt{(\frac{R_g}{2L_s})^2 - \frac{1}{L_s C_{iss}}}$ and $s_2 = \frac{-R_g}{2L_s} - \sqrt{(\frac{R_g}{2L_s})^2 - \frac{1}{L_s C_{iss}}}$

and a particular solution

$$u_{cp} = V_{DR} \tag{6.8}$$

So the voltage on the input capacitor (*Ciss*) can be written as:

$$u_{ciss}(t) = A_1 e^{s_1 t} + A_2 e^{s_2 t} + V_{DR} \tag{6.9}$$

And the current on the common source inductor (I_{LS}) can be calculated as:

$$i_{Ls}(t) = C_{iss} \frac{du_{ciss}}{dt} = C_{iss}(A_1 S_1 e^{s_1 t} + A_2 S_2 e^{s_2 t}) \tag{6.10}$$

Applying two boundary condition $u_{ciss}(0-) = u_{ciss}(0+) = 0$ and $i_{Ls}(0-) = i_{Ls}(0+) = 0$ can solve out the coefficient A_1 and A_2.

For a Renesas HAT2168 MOSFET driven by a 5V step driving voltage, shown in Figure 6-10, the gate-to-source voltage (Vgs) and gate-to-source current (Igs) can be calculated as:

$$V_{gs}(t) = -7.311e^{-4.803 \cdot 10^8 t} + 2.311e^{-1.52 \cdot 10^9 t} + 5 \tag{6.11}$$

$$I_{gs}(t) = 4.811e^{-4.803 \cdot 10^8 t} - 4.811e^{-1.52 \cdot 10^9 t} \tag{6.12}$$

Their waveform is shown in Figure 6-11.

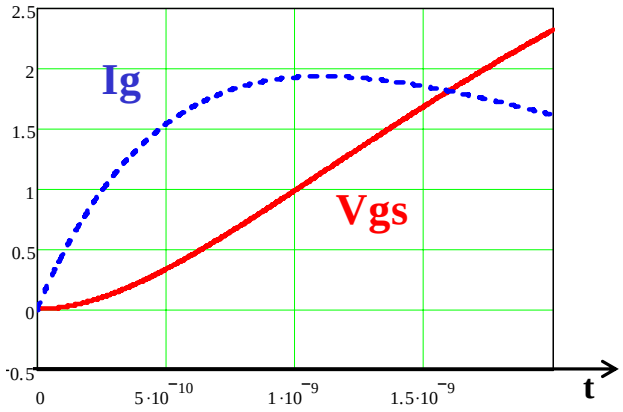


Figure 6-11 Gate voltage and current waveform for Renesas HAT2168

From the equation we can solve that when the gate-to-source voltage (*Vgs*) reaches the threshould voltage (*Vth*), the gate current is around:

$$I_{g\_th} = 1.8A \tag{6.13}$$

After the gate-to-source voltage (*Vgs*) reaches the threshould voltage (*Vth*), the MOSFET channel starts to conduct current.

During the turn on, if the parasitic inductance (*Ls and Ld*) is not too big or the input voltage (*Vin*) is not too low which could satisfy the equation

$$\frac{I_{g\_th}}{C_{iss}} \cdot g_{fs} < \frac{V_{in}}{L_s + L_d} \tag{6.14}$$

which is usually satisfied. This equally means $V_{ds} > V_{gs} - V_{th}$. Thus the MOSFET works in the saturation region like a voltage controlled current source. During the turn off MOSFET will always work in the saturation region within the transition period.

Use turn on as an example. In order to keep the gate current increasing at certain slew rate, from the circuit, we need to satisfy the following relationship:

$$V_{DR} - I_g \cdot R_G - V_{gs} \geq L_s \frac{di_{ds}}{dt} \tag{6.15}$$

And Vgs varys from threshould voltage (*Vth*) to plateau (*Vplt*) as current increases. Therefore the drain to source current (*Ids*) and the gate to source voltage (*Vgs*) has the following relationship

$$\frac{di_{ds}}{dt} = g_{fs} \frac{dv_{gs}}{dt} = g_{fs} \frac{I_g}{C_{iss}} \tag{6.16}$$

When we substitute (6.16) into (6.14), we can derive an inequation:

$$I_g \leq \frac{V_{DR} - V_{th}}{(\frac{L_s \cdot g_{fs}}{C_{iss}}) + R_g} \tag{6.17}$$

This equation means only when the gate current (*Ig*) smaller than right hand side equation, it will continue increasing. Today's power MOSFETs all have a very large trans-conductance (g_{fs}). From calculation we can get that, unless the gate current is smaller than 0.2A which is obviously not possible from previous analysis, the gate current will not increase after the MOSFET reaching the threshould voltage.

As calculated in equation (6.13), during the current rising period of the MOSFET turn on, the gate current (*Ig*) mostly would have a negative slew rate, as shown in Figure 6-10. Because the peak gate current point which happens at the gate-to-source voltage (*Vgs*) reaches the threshould voltage (*Vth*) is much more smaller than the load current. So the gate current slew rate is much smaller than the channel current slew rate.

Figure 6-12 shows a comparison of the Renesas HAT2168 MOSFET's channel and the gate current slew rate during the current-rising period that corresponds to the turn-on of the device.

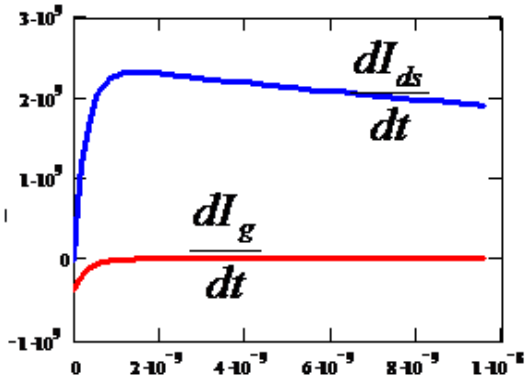


Figure 6-12 The comparison between channel and gate current slew rate

With the assumption $\frac{dI_{ds}}{dt} >> \frac{dI_g}{dt}$, Equation (6.5) can be simplified to

$$V_{Ls} \approx L_S \frac{di_{ds}}{dt} \tag{6.18}$$

Then we can use the turn-off loss as an example to explain the following derivation. The equivalent circuit during the current-falling period of the device turn-off is shown in Figure 6-13.

We can directly calculate the gate discharging current (*Ig*) as:

$$i_g = -\frac{V_{gs} + V_{Ls}}{R_g} = -\frac{V_{gs} + L_s \frac{dI_{ds}'}{dt}}{R_g}, \tag{6.19}$$

The MOSFET gate-to-source voltage can be reorganized as

$$\Delta V_{gs} = \frac{1}{C_{gs}} \int i_g dt = -\frac{1}{C_{gs}} \int \frac{V_{gs} + L_s \frac{dI_{ds}'}{dt}}{R_g} dt . \tag{6.20}$$

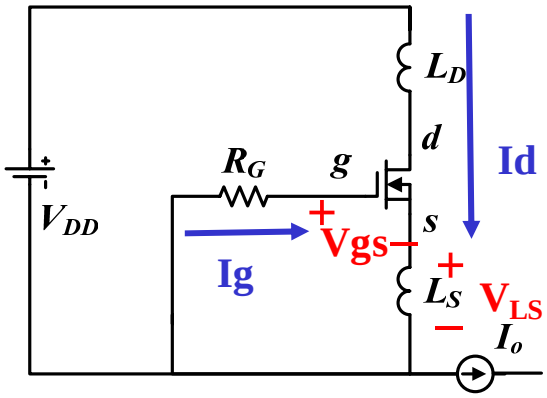


Figure 6-13 Equivalent circuit during the current-falling period of turn-off

Taking a derivative of the gate-to-source voltage, equation (6.20) becomes

$$\frac{dV_{gs}}{dt} = -\frac{1}{C_{iss} \cdot R_g}(V_{gs} + L_s \frac{dI_{ds}'}{dt}) \tag{6.21}$$

Because $I_{ds}' = g_{fs}(V_{gs} - V_{th})$, and Vth is a constant value in terms of time. Hence Equation (6.21) equals

$$\frac{dV_{gs}}{dt} = -\frac{1}{C_{iss} \cdot R_g}(V_{gs} + L_s \cdot g_{fs} \frac{dV_{gs}}{dt}) \tag{6.22}$$

Which can be rearranged to

$$\frac{dV_{gs}}{dt} + \frac{V_{gs}}{R_g \cdot C_{iss} + L_s \cdot g_{fs}} = 0. \tag{6.23}$$

This equation has the general solution

$$V_{gs}(t) = A \cdot e^{-\frac{t}{\tau'}} \tag{6.24}$$

Where

$$\tau' = R_g C_{iss} + L_s \cdot g_{fs}. \tag{6.25}$$

Applying the boundary condition that when t=0, $V_{gs}(0) = V_{th} + \frac{I_o}{g_{sf}}$, equation (6.23) can be solved to :

$$V_{gs}(t) = (V_{th} + \frac{I_o}{g_{fs}}) \cdot e^{-\frac{t}{\tau'}}, \tag{6.26}$$

So the current can be derived as:

$$I_{ds}'(t) = g_{sf} \cdot [(V_{th} + \frac{I_o}{g_{fs}}) \cdot e^{-\frac{t}{\tau'}} - V_{th}]. \tag{6.27}$$

Using the Taylor series to expand the exponantial terms, and neglecting the high-order terms, equation (6.27) becomes:

$$I_{ds}'(t) = I_o - (I_o + V_{th} \cdot g_{fs}) \cdot \frac{t}{\tau'} \tag{6.28}$$

Where

$$\tau' = R_g C_{iss} + L_s \cdot g_{fs}. \tag{6.29}$$

Equation (4.11), which is the current-falling equation for the ideal packaging case, is repeated here as Equation (6.30) for comparison.

$$I_{ds}(t) = I_o - (I_o + V_{th} \cdot g_{fs}) \frac{t}{\tau} \tag{6.30}$$

Where

$$\tau = R_g C_{iss}. \tag{6.31}$$

Comparing Equation (6.30), which is for ideal packaging, to Equation (6.28), which is considered the packaging parasitics, we see they have a similar form, and the only difference is the time constant.

The time constant $\tau' = R_g \cdot C_{iss} + L_s \cdot g_{fs}$ (with packaging parasitics) is always bigger than the the time constant $\tau = R_g C_{iss}$ (without packaging parasitics). This result shows that,

with packaging parasitics, the MOSFET channel current-falling speed will be greatly reduced.

For the modern MOSFET design, the device transconductance (*gfs*) typically is designed to be very large; around 50 for the top switch. Even at 1nH the common-source parasitic inductance (*Ls*) could make the term $L_s \cdot g_{fs}$ much larger than the term $R_g \cdot C_{iss}$. For most of the current packaging methods, the common-source parasitic inductance (*Ls*) is much higher than 1nH.

After we get the equation for the channel current, it is very easy to calculate the equation for the drain-to-source voltage. As mentioned above, the drain-side parasitic inductor (*Ld*) would generate a voltage that adds to the input voltage during the turn–off, which in turn increases the turn-off loss.

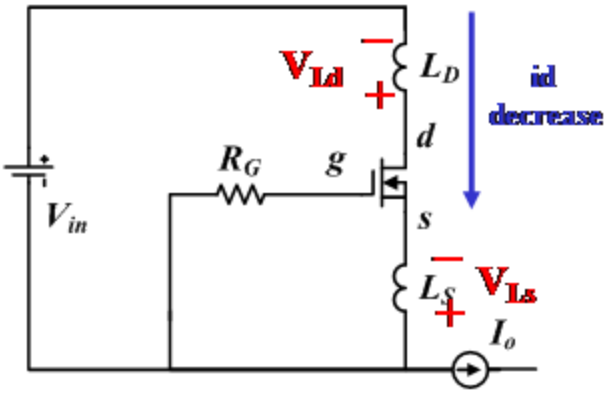


Figure 6-14 MOSFET drain-to-source voltage during the turn-off

Shown in Figure 6-14, the MOSFET drain-to-source voltage during the turn-off period can be calculated as:

$$V_{ds}(t) = V_{in} - (L_s + L_d)\frac{dI_{ds}'(t)}{dt} \tag{6.32}$$

where *Ids'(t)* is the same as in Equation (6.29).

The current falling time period can be calculated as

$$t_f = \frac{I_o \cdot \tau_G{}'}{I_o + V_{th} \cdot g_{fs}}. \tag{6.33}$$

Finally we can get the power loss during the current-falling period of the turn-off period by calculating the integral of the channel current (6.28) and the drain-to-source voltage (6.32) over time period (6.33).

$$P_{off\_Tf} = \int_0^{Tf} v_{ds}(t) \cdot i_{ds}{}'(t) \cdot f_s = \frac{V_{in} \cdot I_o \cdot R_g}{2 \cdot V_{plt}} \cdot (Q_{gs2} + \frac{L_s \cdot g_{fs}}{R_g \cdot C_{iss}} Q_{gs2}) \cdot f_s + \frac{(L_s + L_d) I_o^2}{2} \cdot f_s \tag{6.34}$$

Equation (6.34) can be further simplified, because $Q_{gs2} = C_{iss} \cdot \frac{I_o}{g_{fs}}$, as discussed previously. Therefore,

$$\frac{L_s \cdot g_{fs}}{R_g \cdot C_{iss}} Q_{gs2} = \frac{L_s \cdot I_o}{R_g} \tag{6.35}$$

and the loss eqution (6.33) becomes

$$P_{off\_Tf} = \frac{V_{in} \cdot I_o \cdot R_g}{2 \cdot V_{plt}} \cdot Q_{gs2} \cdot f_s + \frac{V_{in} \cdot I_o}{2} \cdot \frac{L_s \cdot I_o}{V_{plt}} \cdot f_s + \frac{(L_s + L_d) I_o^2}{2} \cdot f_s. \tag{6.36}$$

Equation (4.14), which is based on ideal packaging, is repeated here as (6.36) for the sake of comparison.

$$P_{off\_Tf} = \frac{V_{in} I_o}{2} \frac{Q_{gs2} R_g}{V_{plt}} f_s \tag{6.37}$$

Comparing the loss equation (6.37), which is based on ideal packaging, with the loss equation (6.36), which includes the packaging parasitics, we can see that the packaging parasitics (*Ls* and *Ld*) add two additional terms, $\frac{V_{in} \cdot I_o}{2} \cdot \frac{L_s \cdot I_o}{V_{plt}} \cdot f_s$ and $\frac{(L_s + L_d) I_o^2}{2} \cdot f_s$, which are not related to the device die size at all.

Using the same method, we can get the loss equation for the current-rising period of the turn-on of the device.

$$P_{on\_Tr} = \frac{V_{in} \cdot I_o \cdot R_g}{2 \cdot (V_{DR} - V_{plt})} \cdot Q_{gs2} \cdot f_s + \frac{V_{in} \cdot I_o}{2} \cdot \frac{L_s \cdot I_o}{V_{DR} - V_{plt}} \cdot f_s - \frac{(L_s + L_d) I_o^2}{2} \cdot f_s \qquad (6.38)$$

Previous analysis neglects the current ripple information of both turn on and turn off. To consider the current ripple, we can use the valley current (*Iv)* and peak current (*Ip*) instead of the load current (*Io*) for turn on and turn off in equation (6.36) and (6.38).

Table 6-1 give a complete comparison of loss between ideal packaging and loss of packaging with considering parasitic inductance.

		Switching loss with Parasitic Inductance (Ld and Ls)	Switching loss of ideal Package
Turn on	Current Rising Period	$\frac{V_{in} \cdot I_o \cdot R_g}{2 \cdot (V_{DR} - V_{plt})} \cdot Q_{gs2} \cdot f_s + \frac{V_{in} \cdot I_o}{2} \cdot \frac{L_s \cdot I_o}{V_{DR} - V_{plt}} \cdot f_s - \frac{(L_s + L_d) I_o^2}{2} \cdot f_s$	$\frac{V_{in} \cdot I_o \cdot R_g}{2 \cdot (V_{DR} - V_{plt})} \cdot Q_{gs2} \cdot f_s$
	Voltage Falling Period	$\frac{V_{in} \cdot I_o \cdot R_g}{2 \cdot (V_{DR} - V_{plt})} \cdot Q_{gd} \cdot f_s$	$\frac{V_{in} \cdot I_o \cdot R_g}{2 \cdot (V_{DR} - V_{plt})} \cdot Q_{gd} \cdot f_s$
Turn off	Voltage Rising Period	$\frac{V_{in} \cdot I_o \cdot R_g}{2 \cdot V_{plt}} \cdot Q_{gd} \cdot f_s$	$\frac{V_{in} \cdot I_o \cdot R_g}{2 \cdot V_{plt}} \cdot Q_{gd} \cdot f_s$
	Current Falling Period	$\frac{V_{in} \cdot I_o \cdot R_g}{2 \cdot V_{plt}} \cdot Q_{gs2} \cdot f_s + \frac{V_{in} \cdot I_o}{2} \cdot \frac{L_s \cdot I_o}{V_{plt}} \cdot f_s + \frac{(L_s + L_d) I_o^2}{2} \cdot f_s$	$\frac{V_{in} \cdot I_o \cdot R_g}{2 \cdot V_{plt}} \cdot Q_{gs2} \cdot f_s$

Table 6-1 Comparison loss model with and without packaging parasitics

Finally, the turn-on loss equals

$$P_{on} = \frac{V_{in} \cdot I_o}{2} \cdot \frac{(Q_{gd} + Q_{gs2}) \cdot R_g}{V_{DR} - V_{plt}} \cdot f_s + \frac{V_{in} \cdot I_o}{2} \cdot \frac{L_s \cdot I_o}{V_{DR} - V_{plt}} \cdot f_s - \frac{(L_s + L_d) I_o^2}{2} \cdot f_s, \qquad (6.39)$$

the turn off loss equals

$$P_{off} = \frac{V_{in} \cdot I_o}{2} \cdot \frac{(Q_{gd} + Q_{gs2}) \cdot R_g}{V_{plt}} \cdot f_s + \frac{V_{in} \cdot I_o}{2} \cdot \frac{L_s \cdot I_o}{V_{plt}} \cdot f_s + \frac{(L_s + L_d) I_o^2}{2} \cdot f_s, \quad (6.40)$$

the conduction loss equals

$$P_{cond} = I_o^2 \cdot R_{dson} \cdot \frac{V_o}{V_{in}}, \quad (6.41)$$

And the gate driving loss equals

$$P_{dr} = V_{DR} \cdot f_s \cdot Q_g. \quad (6.42)$$

Figure 6-15 shows a comparison between the loss calculated by this model and the loss simulated by ISE-TCAD based on a physics-based model provided by Renesas. The comparison is made under the following conditions; 12V input, 1.2V ouput, 12.5A/phase, 1MHz and 5V driving.

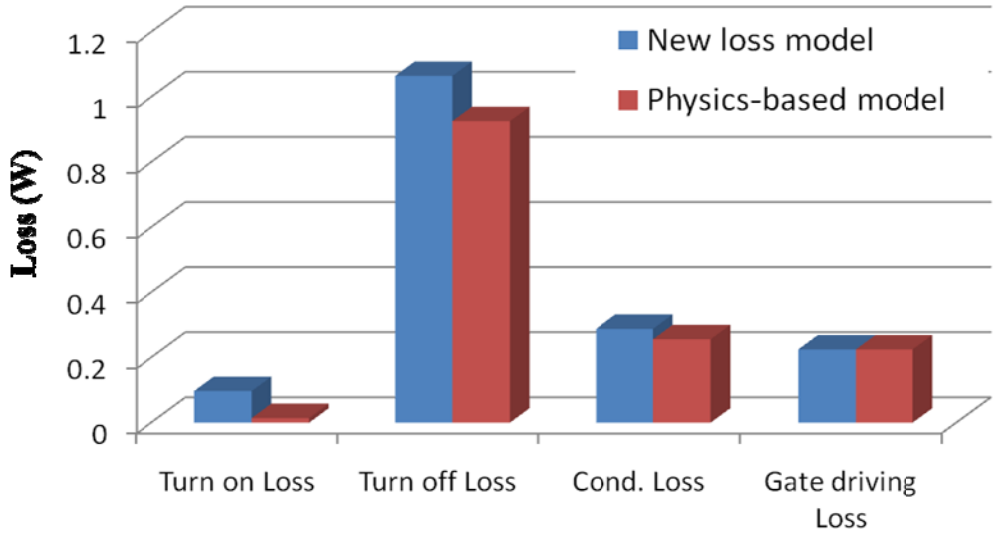


Figure 6-15 Loss comparison between new loss model and physics-based loss model

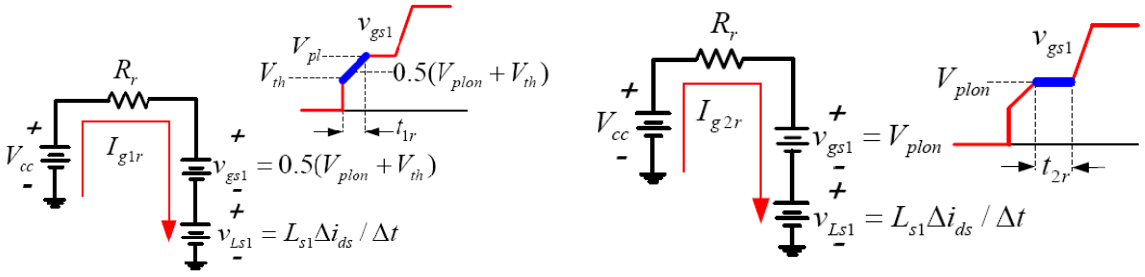
From the comparison results, we can see that the new loss model is quite accurate when compared with the physics-based model. Furthermore, comparing with previous loss model [7], this model is a closed-form analytical loss model which can separate the loss influence from the device die and the packaging parasitics and can give a concrete meaning of each parameter. This will be discussed in the later part of this chapter.

Another paper is published recently talking about a simple loss model with packaging parasitics[14]. In the paper, the author treated the MOSFET voltage and current waveform as a piece-wise linear curve and also included the delay effect coming from the common source inductance. But there is two major difference make the new proposed loss model much more simple and accurate.

The first one is the way to calculate the gate charge current. The author uses two different Vgs values to calculate the gate charging current for the current rising period and the voltage falling period (Turn on for example) as Figure 6-16 and equation (6.43)(6.44) shown.

$$I_{g1r} = \frac{V_{cc} - 0.5(V_{plon} + V_{th}) - L_{s1}\dfrac{\Delta i_{ds}}{\Delta t}}{R_r} \tag{6.43}$$

$$I_{g2r} = \frac{V_{cc} - V_{plon} - L_{s1}\dfrac{\Delta i_{ds}}{\Delta t}}{R_r} \tag{6.44}$$



Current rising period Voltage falling period

Figure 6-16 Gate charging current difference

While the new porposed loss model only use one vaule.

$$I_g = I_{g1r} = I_{g2r} = \frac{V_{cc} - V_{plon} - L_{s1}\dfrac{\Delta i_{ds}}{\Delta t}}{R_r} \tag{6.45}$$

Vplon and *0.5(Vplon+Vth)* only have *0.1V* different in today's MOSFET application because the transconductance is usually designed very large. With the help of similar gate

charging current for the current rising period and the voltage falling period, the total switching charge (*Qgs2+Qgd*) can be combined and calculated together as equation (6.46) shown.

$$t_{1r} + t_{2r} = \frac{Q_{gs2} + Q_{gd}}{I_g} \tag{6.46}$$

While in the paper [14] the author need to seprate it into two parts as equation (6.47)(6.48) shown.

$$t_{1r} = \frac{C_{gs1}\Delta V_{gsr} + C_{gd1}(\Delta V_{gsr} + L_{loop}\frac{\Delta i_{ds}}{\Delta t})}{I_{g1r}} \tag{6.47}$$

$$t_{2r} = \frac{C_{gd1}(V_{in} - L_{loop}\frac{\Delta i_{ds}}{\Delta t})}{I_{g2r}} \tag{6.48}$$

Where $C_{gs1}\Delta V_{gsr} + C_{gd1}\Delta V_{gsr} = Q_{gs2}$ and $C_{gd1}V_{in} = Q_{gd}$.

Because MOSFET junction capacitor is quite non-linear function of the drain-to-source voltage, it is better and more accurate to use the total gate charge to calculate the transition time.

The second difference comes from the way to linearize the voltage and current waveform. In the paper [14], the author assumes that during the swtiching transition period both of the MOSFET drain-to-source voltage (*Vds*) and current (*Ids*) are changing linearly, shown in Figure 6-17, which is obviously not ture from MOSFET operating point of view.

Because $V_{ds} = V_{in} - (L_s + L_d)\frac{dI_{ds}}{dt}$, The MOSFET drain-to-source voltage (*Vds*) and current (*Ids*) can not changing linearly at the same time.

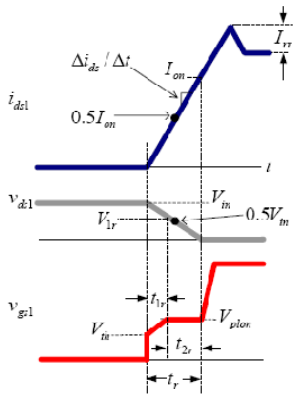


Figure 6-17 Different way to linearize the voltage and current waveform

For some extreme cases, either the parasitic inductance (*Ls and Ld*) is too big or the input voltage (*Vin*) is too low which can not satisfy equation (6.18), the MOSFET will go to the linear region directly. In this case the drain-to-source current (*Ids*) slew rate is much slower than the gate-to-source voltage (*Vgs*). So we can assume that *Vgs* already reached the driving voltage (V_{DR}) before Ids starts to increase. Then the on-resistance (*Rdson*) value at V_{DR} can be used to calculate the loss. And the channel current slew rate is determined by

$$\frac{di_{ds}}{dt} = \frac{V_{in}}{L_s + L_d} \tag{6.49}$$

And the power loss can be calculated as

$$P = f_s \cdot \int_t V_{ds}(t) \cdot I_{ds}(t) dt = f_s \cdot \int_t V_{ds}(t) \cdot I_{ds}(t) dt = \frac{1}{3} I_o^3 f_s R_{dson} \frac{L_d + L_s}{V_{in}} \tag{6.50}$$

In this case, because MOSFET goes to linear region directly, MOSFET turn on processing is more like a ZCS and the power loss during this period is more like a conduction loss. Although a large Ld could save some turn on loss, but it will pay more turn off loss due to a higher drain-to-source voltage stress.

6.3. Optimized device selection method is still valid

By adding the equations (6.39) to (6.42) together, the total top-switch loss will become:

$$P_{top} = \frac{V_{in} \cdot I_o}{2} \cdot \frac{(Q_{gd} + Q_{gs2}) \cdot R_g}{V_{DR} - V_{plt}} \cdot f_s + \frac{V_{in} \cdot I_o}{2} \cdot \frac{(Q_{gd} + Q_{gs2}) \cdot R_g}{V_{plt}} \cdot f_s + V_{DR} \cdot f_s \cdot Q_g + I_o^2 \cdot R_{dson} \cdot \frac{V_o}{V_{in}}$$
$$+ \frac{V_{in} \cdot I_o}{2} \cdot \frac{L_s \cdot I_o}{V_{DR} - V_{plt}} \cdot f_s + \frac{V_{in} \cdot I_o}{2} \cdot \frac{L_s \cdot I_o}{V_{plt}} \cdot f_s \tag{6.51}$$

From Equation (6.51) we can observe the first four terms are exactly the same as they are in the loss equation of the ideal packaging case (5.16), and the last two terms are the additional terms related to packaging parasitcs.

Using the same assumption that the MOSFET is built by paralleling a large number of identical cells, and all the gate charges (*Qg, Qgs2 and Qgd*) are proportional to number of cells in the device, the on-resistance (*Rdson*) is inversely proportional to the number of cells in the device.

We can substitute $Q_g = Q_{g,sp} \cdot N_{cell}$ $Q_{gd} = Q_{gd,sp}$ $Q_{gs2} = Q_{gs2,sp}$ and $R_{dson} = \frac{R_{dson,sp}}{N_{cell}}$ into Equation (6.51), and take a derivative, $\frac{dP_{top}(N)}{dN} = 0$.

The minimum loss equals

$$P_{top\_\min} = \sqrt{2 \cdot I_o^3 \cdot V_o \cdot R_g \cdot f_s} \cdot \sqrt{\frac{V_{DR}}{V_{plt} \cdot (V_{DR} - V_{plt})}} \cdot \sqrt{(Q_{gd,sp} + Q_{gs2,sp} + \frac{2 \cdot V_{plt} \cdot (V_{DR} - V_{plt})}{V_{in} \cdot I_o \cdot R_g} \cdot Q_{g,sp}) \cdot R_{dson,sp}}$$
$$+ \frac{V_{in} \cdot I_o}{2} \cdot \frac{L_s \cdot I_o}{V_{DR} - V_{plt}} \cdot f_s + \frac{V_{in} \cdot I_o}{2} \cdot \frac{L_s \cdot I_o}{V_{plt}} \cdot f_s \tag{6.52}$$

when

$$N_{opt} = \sqrt{\frac{2 \cdot I_o^2 \cdot V_o}{V_{in}^2 \cdot I_o \cdot R_g \cdot f_s} \cdot \frac{V_{plt} \cdot (V_{DR} - V_{plt})}{V_{DR}} \cdot \frac{R_{dson,sp}}{(Q_{gd,sp} + Q_{gs2,sp} + \frac{2 \cdot V_{plt} \cdot (V_{DR} - V_{plt})}{V_{in} \cdot I_o \cdot R_g} \cdot Q_{g,sp})}} . \tag{6.53}$$

From Equation (6.52) we can see that the minimum loss with packaging parasitic inductors is consistent with the minimum loss without packaging parasitic inductors shown in Equation (5.10), plus two additional terms related to packaging parasitic inductors.

We can also compare the optimized cell number with the packaging parasitic inductors case (Equation 6.53) and see that it is exactly the same as the case without packaging parasitic inductors (Equation 5.9).

This basically means that because the loss due to packaging parasitic inductors is not related to either the gate charge (*Qg, Qgs, Qgd*) or the on-resistance (*Rdson*); adding a packaging parasitic inductor won't change the optimized die size selection; and all previous analysis and method of selecting the right device is still valid.

6.4. Loss impact analysis of different packaging methods

As mentioned above, different packaging methods use different ways to connect the MOSFET die to the pins, resulting in different packaging parasitic inductances. For example, Renesas has three major packaging methods, SO-8, LFPAK and Dr.MOS, for its 30V MOSFET product line, as listed in Table 6-2.

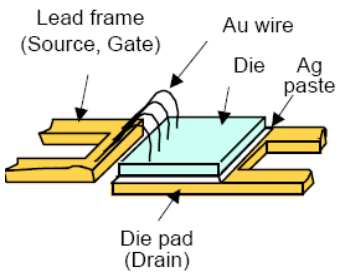
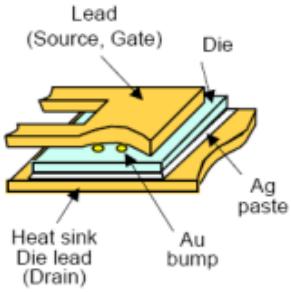
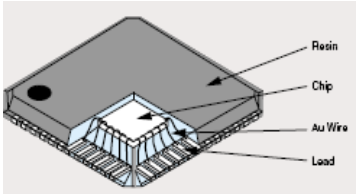
SO8	LFPAK	Dr.MOS
		
Ls=1.5nH Ld=3nH	**Ls=1nH Ld=3nH**	**Ls=0.1nH Ld=2.5nH**

Table 6-2 Parasitic inductance of commercial packaging methods

In order to make a fair comparison of the loss performance between different packaging methods, it is reasonable to use the same device die during the analysis. Thus the following analysis is all based on a Renesas RJK0305DPB die with different packaging methods.

- *Renesas RJK0305DPB die + SO8 packaging*

The standard SO-8 packaging has been the standard package of devices for POL power supplies for several years due to its small size, standard footprint, low cost and reasonable performance. As shown in Table 6-2, the SO-8 package uses wire-bonds to connect the device die to the pin, which causes a large common-source parasitic inductance (*Ls*).

Figure 6-18 shows a detailed loss breakdown of the device using a Renesas RJK0305DPB die plus SO8 packaging based on 12V input, 1.2V output, 20A per phase, 600kHz and 12V driving.

From the loss breakdown, we can clearly see that because the SO-8 package has a large Ls inductance, the Ls-related loss is the dominant part of the total loss. If we consider that the Ls and Ld-related loss is the packaging-related loss; and the Qgs2 and Qgd-related loss, conduction loss, and gate driving loss are all part of the silicon-die-related loss; in this case, the packaging-related loss is far more impotant than the silicon-die-related loss. As shown in Figure 6-19, the packing-related loss occupies 61% of the total loss while the silicon-die-related loss only occupies 39%.

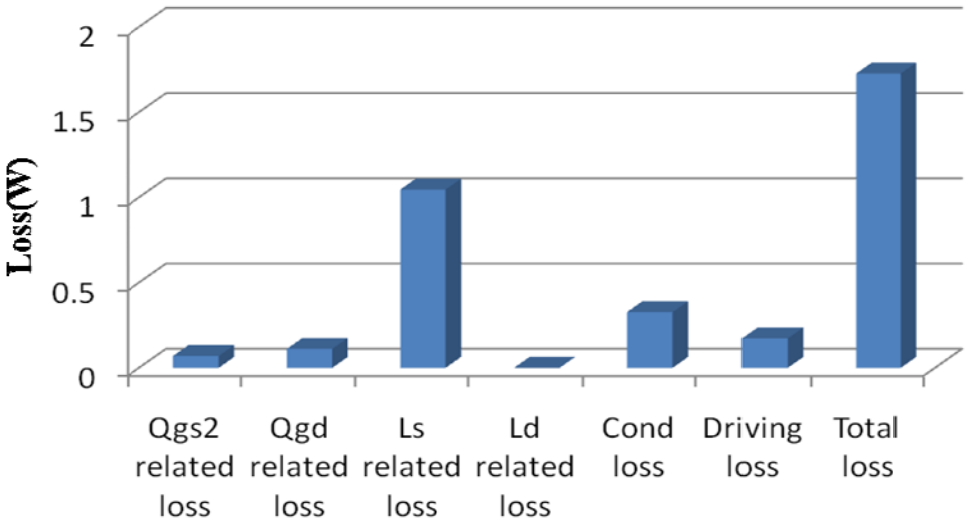


Figure 6-18 Loss break down for SO8 packaging

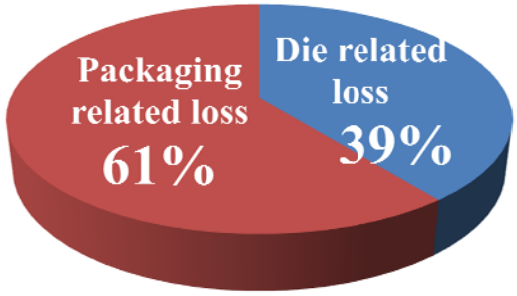


Figure 6-19 Packaging-related loss vs. die-related loss of SO8 packaging

- *Renesas RJK0305DPB die + LFPAK packaging*

The LFPAK is introduced to improve the performance. The LFPAK is a wire-bondless structure because it uses a conducting electrode plate connected directly to the silicon. Therefore the parasitic inductance is greatly reduced to almost half that of the SO-8 package.

Figure 6-20 shows a detailed loss breakdown of the device using a Renesas RJK0305DPB die plus the LFPAK package based on 12V input, 1.2V output, 20A per phase, 600kHz and 12V driving.

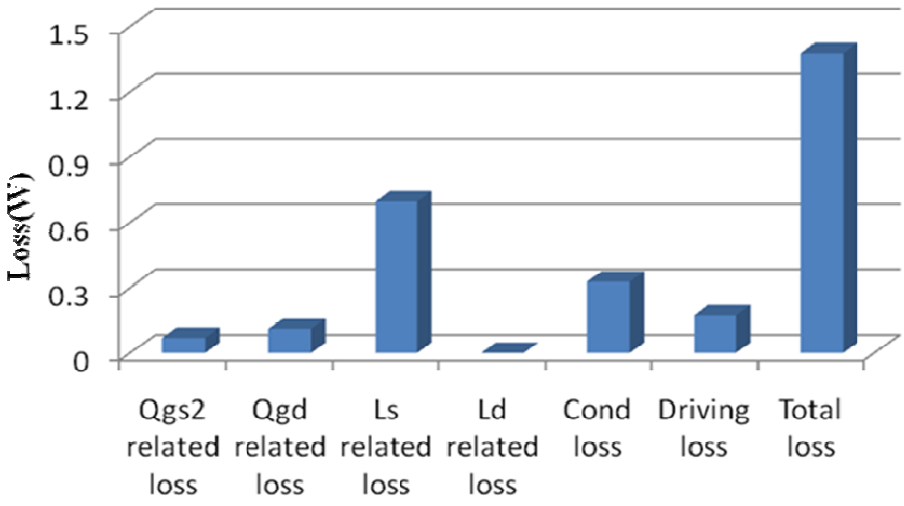


Figure 6-20 Loss breakdown for LFPAK packaging

From the loss breakdown, we can see that by changing to the LFPAK from the SO-8 package, the LS related loss can be greatly reduced because of the smaller parasitic inductance, Ls. But the Ls related loss is still a dominant part of the total loss. The silicon-die-related loss and the packaging-related loss are almost half and half, as shown in Figure 6-21.

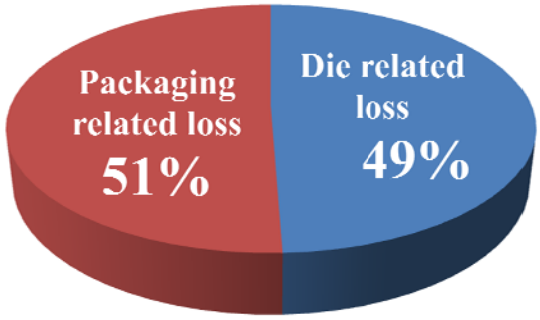


Figure 6-21 Packaging related loss V.S. die related loss of LFPAK packaging

- *Renesas RJK0305DPB die + Dr.MOS packaging*

The Dr.MOS packaging method can further improve the performance by integrating the MOSFET and the driver. By integrating these components together, it is possible to make

the driver very close to the MOSFET and minimize the gate driving loop. Therefore the common-source parasitic inductance (*Ls*) can be greatly reduced to 0.1nH.

Figure 6-22 shows a detailed loss breakdown of the device using a Renesas RJK0305DPB die plus the Dr.MOS package based on 12V input, 1.2V output, 20A per phase, 600kHz and 12V driving.

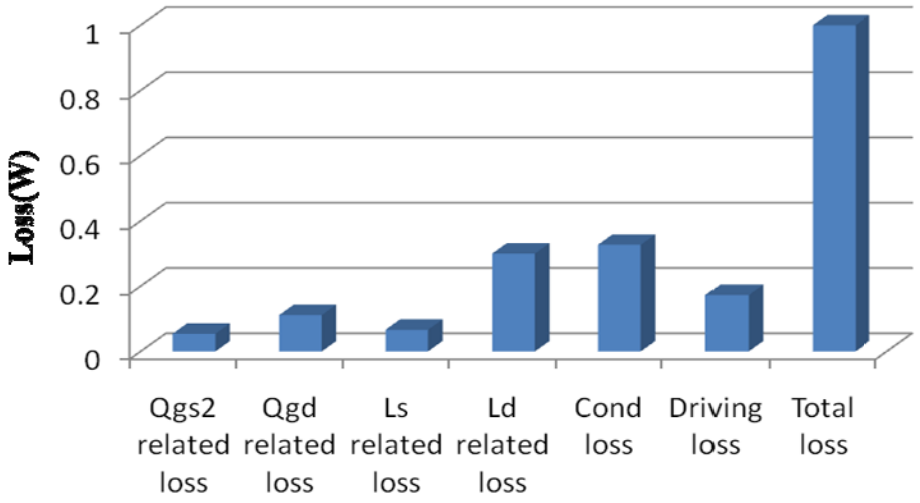


Figure 6-22 Loss breakdown for Dr.MOS packaging

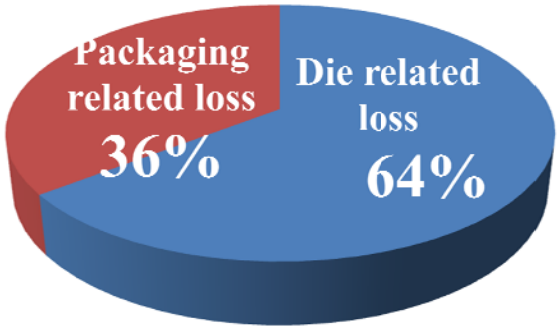


Figure 6-23 Packaging-related loss vs. die-related loss of Dr.MOS packaging

From the loss breakdown shown in Figure 6-22, we can see that because the inductance Ls in the Dr.MOS is reduced to a relatively low level, the Ls-related loss is no longer a dominant part of the total loss. Figure 6-23 shows that in this case the silicon-die-related loss is more important than the packaging-related loss.

6.5. Summary

The device packaging parasitics play an important role in the total device loss. Sometimes they are an even more important factor than the device die itself. A new simple and accurate closed-form loss model is derived, which can provide more physical meaning for each of the device parameters. The loss coming from the packaging parasitic is shown to be independent of the loss coming from the device die itself. All previous analysis about device selection is still valid even with the packaging parasitics.

Chapter 7 The Bottom-switch FOM

7.1. Bottom-switch power loss

For the bottom switch in the buck converter shown in Figure1-1, its total power loss is very different than the top switch because of the different switching strategy. Before turning on and turning off the bottom switch, in order to prevent a short-though almost all commercial driver circuits will leave a certain period of dead time when both the top and bottom switch are off, as shown in Figure 7-1. During the dead time, the inductor current is freewheeling though the bottom-switch anti-parallel diode, and the drain-to-source voltage is clamped at almost zero voltage. Thus both the bottom switch turn-on and turn-off actions are zero-voltage-switching actions.

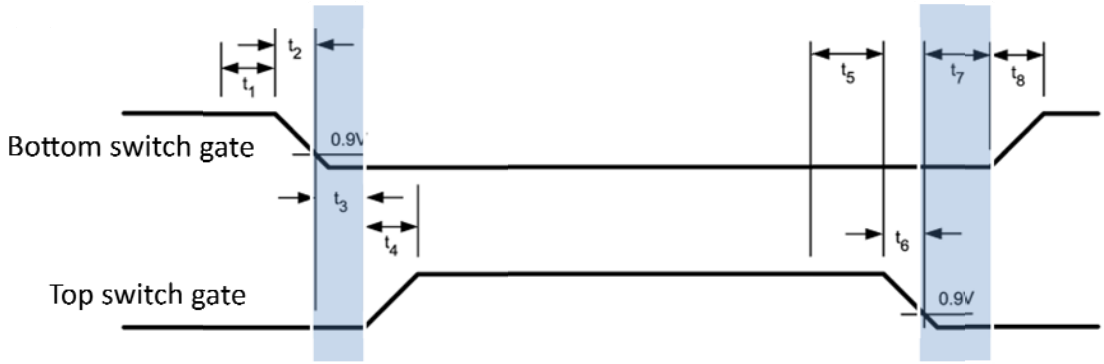


Figure 7-1 Dead time between top and bottom switch

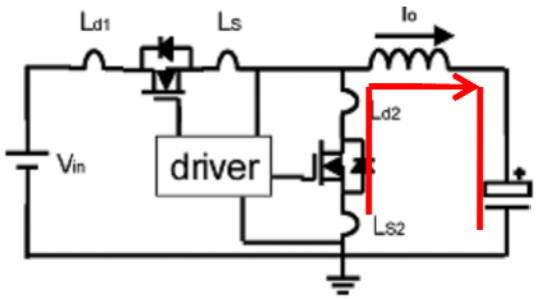


Figure 7-2 Inductor current freewheeling though anti-parallel diode

Because the bottom switch doesn't have switching loss, the previous FOM is obviously no longer suitable. Following the same method used with the top switch, we can derive the FOM for the bottom switch through its minimum loss equation.

For the bottom switch, the total device power loss includes the conduction loss, the gate drive loss, the output capacitor loss, the body diode conduction loss, and the reverse recovery loss, as shown in Equation (7.1).

$$P_{loss\_bot} = I_o^2 \cdot R_{dson}(1-\frac{V_o}{V_{in}}) + Q_g \cdot V_{DR} \cdot f_s + \frac{1}{2} Q_{oss} \cdot V_{in} \cdot f_s + Q_{RR} \cdot V_{in} \cdot f_s + V_{DF} \cdot I_o \cdot t_{dead} \cdot f_s \quad (7.1)$$

From Equation (7.1) we observe that the first three terms, which are the conduction loss, the gate drive loss and the output capacitor loss, are related to the device. The last two terms, which are the body diode conduction loss and the reverse recovery loss, are more closely related to the circuit design, driver selection and PCB layout.

Following the same assumption made in Section 4.1, the Qg, Qoss and Rdson have the following relationship with device cell number (N)

$$Q_g = Q_{g,sp} \cdot N_{cell} \quad Q_{oss} = Q_{oss,sp} \cdot N_{cell} \quad R_{dson} = \frac{R_{dson,sp}}{N_{cell}} . \quad (7.2)$$

When you substitute Equation (7.2) into Equation (7.1) and calculate the derivative $\frac{dP_{loss\_bot}}{dN} = 0$, the optimized cell number can be calculated as:

$$N_{opt} = \sqrt{\frac{I_o^2 \cdot (1-\frac{V_o}{V_{in}}) \cdot R_{dson,sp}}{f_s \cdot (Q_{g,sp} \cdot V_{DR} + Q_{oss,sp} \cdot \frac{V_{in}}{2})}} \quad (7.3)$$

and the total device minimum loss can be derived as:

$$P_{bot\_\min} = 2\sqrt{I_o^2 \cdot (1-\frac{V_o}{V_{in}}) \cdot f_s} \cdot \sqrt{(Q_{g,sp} \cdot V_{DR} + Q_{oss,sp} \cdot \frac{V_{in}}{2}) \cdot R_{dson,sp}} + P_{RR} + P_{BD} . \quad (7.4)$$

From the minimum loss equation we can see that the $(Q_g \cdot V_{DR} + Q_{oss} \cdot \frac{V_{in}}{2}) \cdot R_{dson}$ term is the most suitable term to be a figure-of-merit (FOM) for the bottom switch.

7.2. Bottom-switch device selection method

Following the same method used in the top-switch device selection method, we can also generate one parabolic curve for a series of devices by using Rdson as the x-axis and $(Q_g \cdot V_{DR} + Q_{oss} \cdot \frac{V_{in}}{2})$ as the y-axis.

Rearranging Equation (7.3) would give the optimized device cell number as determined by a ratio:

$$\frac{(Q_g \cdot V_{DR} + Q_{oss} \cdot \frac{V_{in}}{2})}{R_{dson}} = \frac{I_o^2}{f_s} \cdot (1 - \frac{V_o}{V_{in}}) \tag{7.5}$$

which would generate a straight line that is totally determined by external circuit conditions.

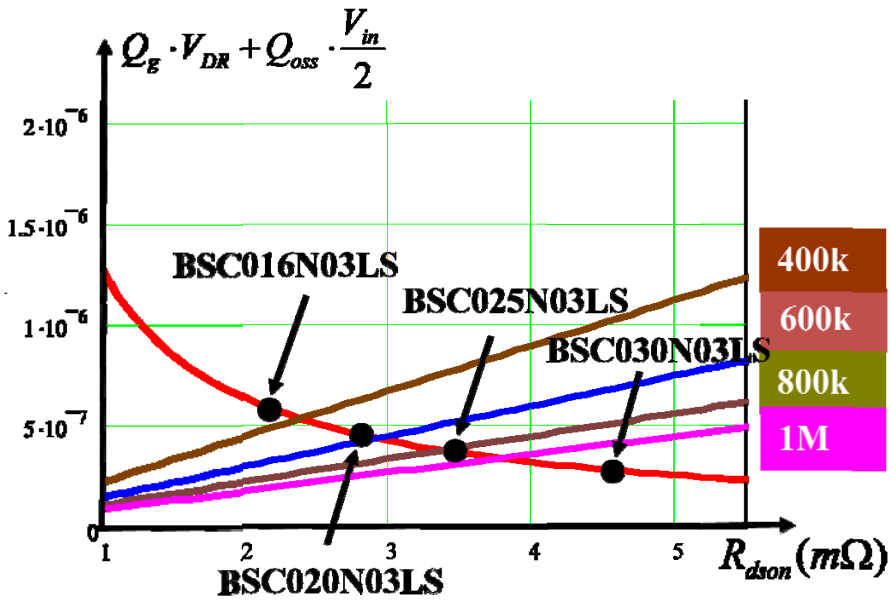


Figure 7-3 Bottom switch device selection method

Different circuit conditions will result in a different ratio and a different straight line, crossing at the parabolic curve at different points which means we need a different optimized die size.

Figure 7-3 shows an example of a buck converter running from 12V down to 1.2V for a VRM application. People in the industry usually use two bottom switches paralleled to handle a 20A per-phase current. From the results we can observe that for the Infineon OptiMOS3 30V MOSFET series, there are several devices optimized at different switching frequencies.

7.3. Summary

The bottom switch has a different figure-of-merit (FOM) from the top switch because the bottom switch doesn't have switching loss. Following the same method to select the device for the top switch, we can select the suitable bottom switch by intersecting a parabolic curve and a straight line.

Chapter 8 Summary

With the increasing speed of the microprocessor and its demand for far more power, determining how to power the microprocessor of our computers becomes an important issue. So far, the power electronics industry keeps struggling to maintain an acceptable power conversion efficiency while operating the VR/VRM at higher and higher switching frequencies. As a consequence, the power switches used in the VR/VRM must be able to work efficiently at a higher switching frequency and with higher current density.

To evaluate the performance of the MOSFET for these low-output-voltage, high-current and high-switching-frequency applications, the prevalent criterion is the figure-of-merit (FOM), which is being widely adopted for the top switch of the buck converter in VRs and VRMs. When comparing the FOMs of different devices, the device with the lowest FOM value is supposed to have the best performance, and therefore be the device that leads to the lowest loss in the circuit. Qgd*Rdson is a widely accepted and widely used FOM for power devices. However, due to the lack of accuracy of the power loss model, this FOM is no longer suitable for VRM applications. Furthermore, using this FOM to select the right device for different applications is another important issue.
The Qgd*Rdson FOM is also not suitable for evaluating the device performance in a low-voltage application because the loss due to charging and discharging of the gate-to-drain charge Q_{gd} is no longer the dominant part of the total switching loss.

Besides the Qgd factor, the Qgs2 is another important factor, especially in low-voltage applications. In a low-voltage device, the Qgs2 factor is almost as important as the Qgd factor, and without the Qgs2 both the derived device minimum loss and the derived optimmum device cell number will be miscalculated.

A new Figure-of-Merit for the top switch, which includes the factor of the Qgs2 and the factor of the gate driving voltage, has been proposed. It is a better indication of the device minimum loss than the previous accepted FOM. Additionally, a new, simple method is proposed for selecting the device and driving voltage which can achieve the minimum loss.

The device packaging parasitics plays an important role in the device loss. Sometimes they can be even more important than the device die itself. A new simple and accurate closed-form loss model is derived that can provide more physical meaning for each of the device parameters. Loss coming from the packaging parasitic is independent from the loss coming from the device die itself. All previous analysis about device selection is still valid even with the packaging parasitics.

Finally a new figure-of-merit for the bottom switch and the method for selecting the bottom switch device is discussed.

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