

# **Modeling and Control of Single Switch Bridgeless SEPIC PFC Converter**

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## Abstract

Due to increasing concerns on the power quality, power factor correction (PFC) has become an important issue in light-emitting diode (LED) lighting applications. A boost converter is one of the most well-known PFC topologies, due to its simple circuitry, simple control scheme and small number of passive components. Even though a boost converter is recognized as a typical PFC converter, its output voltage must be higher than its input voltage. This feature is disadvantageous because the device requires an additional buck-stage for LED lighting systems.

As an alternative to the boost converter, a single-ended primary-inductor converter (SEPIC) allows output voltage to be lower or higher than the input voltage. Thus, the SEPIC converter is gaining popularity as a LED driver because it does not require additional power conversion stage. However, designing a controller to meet stability requirements and international standards is quite challenging for SEPIC converters. Additionally, if the digital controller is adopted for its built-in communication features, creating a digitally controlled SEPIC converter would be even more challenging.

This thesis focuses on the state-space averaging modeling of the SEPIC PFC converter and the design of controllers based on both analog and digital controls with precise modeling. The proposed SEPIC converter incorporates RC damping circuits to avoid the instability, and

thus the entire SEPIC converter becomes a 5<sup>th</sup> order system. Such a high-order system model was derived mathematically and verified with circuit simulator modeling. After verification of the circuit model, the controller was designed with analog transfer functions and converted to and the discrete domain for digital controller implementation. A 150-W single-switch bridgeless SEPIC PFC converter prototype was built accordingly to verify the design. In addition to the current loop controller design for stability, a feed-forward compensator for is introduced and derived for better waveform quality. Simulation results and experiment results are also presented to verify the complete controller with feed-forward compensation. The Texas Instruments (TI) digital signal processor (DSP) TMS320F28335 was adopted for digital controller implementation. For comparison purpose, the TI UC3854 controller was implemented to verify the analog controller design results.

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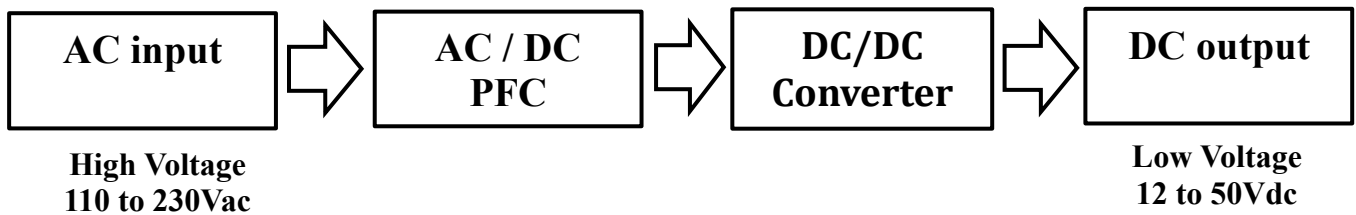
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## 1 INTRODUCTION

LED lighting is gaining popularity in lighting applications, due to the growing trend of eco-friendly design. As a result, the power quality of LED lighting has become an important subject in power electronics. Figure 1.1 shows a block diagram of a conventional LED lighting system. A high ac voltage passes through ac/dc PFC stage [1, 2], which rectifies the ac to dc, and the PFC control produces high-quality power for the LED lighting system. The output from the ac/dc PFC stage is the input of the dc/dc converter, and the output of dc/dc converter generates a low-input voltage for the LED lighting module, which generally requires an input voltage ranging from 12V to 50V. As shown in Figure 1.1, the PFC stage is necessary and important to supply high-quality power for LED lighting applications [1-5].



*Figure 1.1 Block diagram of LED system*

Power factor is expressed as follows: [6-8]

$$PF = \cos \theta \quad (\text{Eq. 1.1})$$

where:

( $\theta$ : phase difference between input current and input voltage)

The PFC stage also plays an essential role in eliminating input power loss. Input power loss may emanate from input current harmonics. A PFC places the input current in phase with input voltage sine waveforms. When PF is 1.0, the input current is perfectly in phase with the input

voltage, with low current distortion. This situation generates low power loss; thus, the system can be highly efficient.

The second reason why many studies [4, 6, 9] are currently focused on PFC is to meet international standard requirements such as EC-62000-3-2. This standard is divided into 4 classes according to application type as shown in Table 1.1 [10]. This thesis focuses on the Class C standard, which applies for all lighting equipment.

*Table 1.1 Class classification of EC-62000-3-2 standard*

<b>Class</b>	<b>Applications</b>
Class A	Balanced three-phase equipment Single-phase equipment not in other classes:
Class B	Portable power tools
Class C	All lighting equipment
Class D	Single phase, below 600W

## **1.1 LITERATURE REVIEWS**

Several of the most popular topologies for PFC converters are the followings: fly-back converter [4, 11], buck-boost converter [3], boost converter [8, 12-15], SEPIC converter [2, 5, 16-22] and Cuk converter [22, 23]. In this chapter, the boost PFC converter and the SEPIC PFC converter [17-19, 23] are briefly introduced to compare their advantages and disadvantages. In addition, the bridgeless SEPIC topology [22, 24] is introduced to discuss its advantages over-converters with rectifying diodes [17].

### 1.1.1 Boost PFC Converter

The boost converter is the most popular PFC device because of its simple power circuitry and simple control scheme arising from its single-switch and ground-referenced switch design [12-14, 25, 26]. Furthermore, low input current distortion could be the reason why the boost converter is so popular for PFC applications. However, the boost converter is limited by the fact that its input voltage must be smaller than its output voltage. This disadvantage requires an additional dc/dc stage for LED applications. Figure 1.2 shows the circuit diagram of the boost converter.

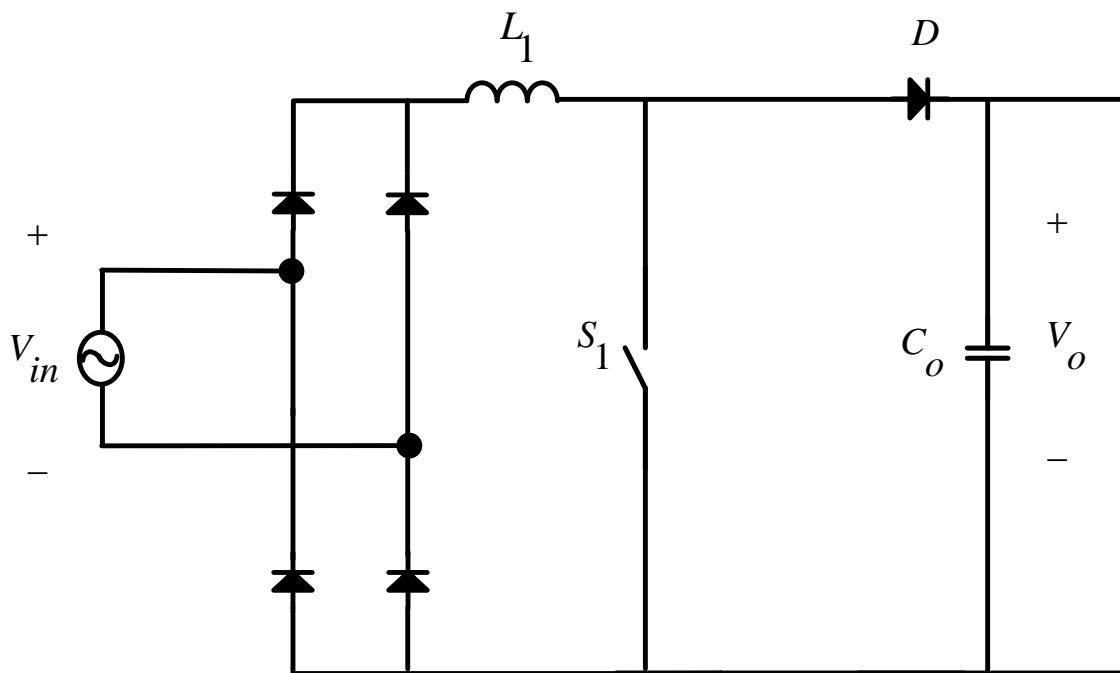


Figure 1.2 Boost PFC converter

### 1.1.2 SEPIC PFC Converter

A SEPIC converter is a less popular topology for PFC converter design because the control can be complex, due to its 2 pairs of un-damped complex poles, compared with other PFC converters, such as the boost converter [12-14, 26], fly-back converter [4, 27]. The advantage of the SEPIC converter is that its output voltage is not necessarily limited by its input voltage range. This property means that the output voltage can be higher or lower than input voltage. Moreover, this property means that the SEPIC PFC converter does not require an additional dc/dc stage for LED applications. Additionally, the SEPIC converter can reduce the input current ripple by incorporating 2 properly wound inductors [16, 18, 22]. This characteristic means that the power loss due to the current ripple can be reduced. Figure 1.3 shows the circuit diagram of the SEPIC converter.

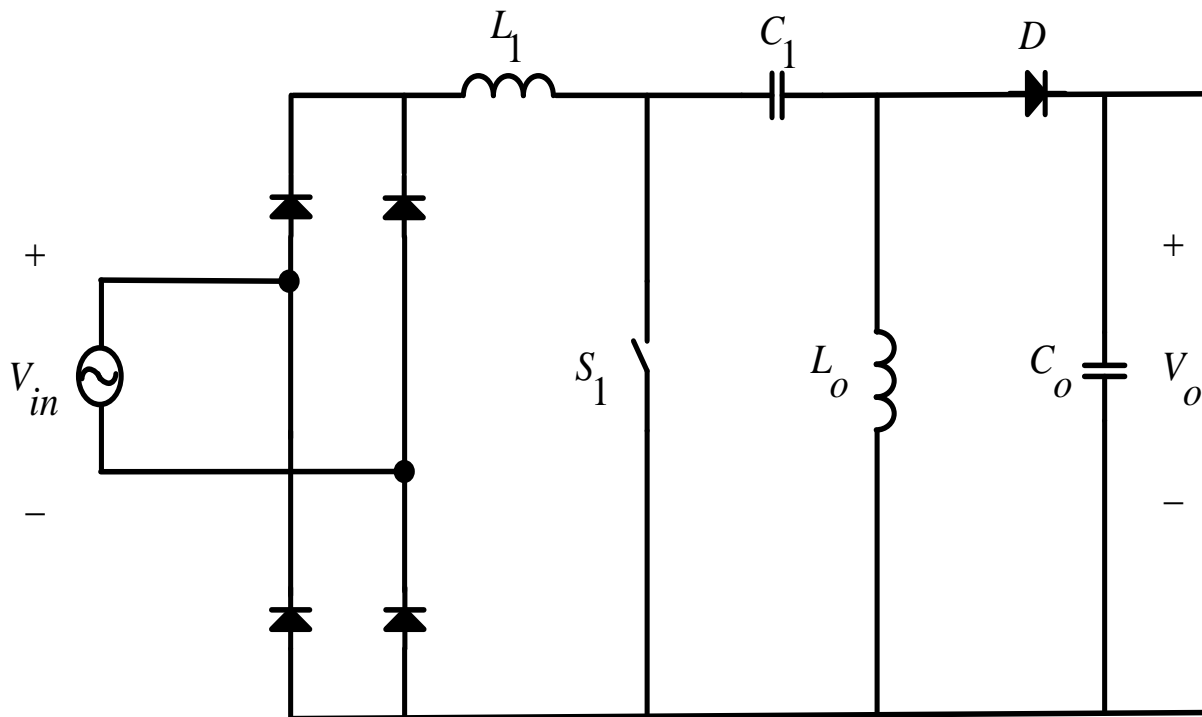


Figure 1.3 SEPIC PFC Converter



### 1.1.3 Bridgeless PFC Converters

Bridgeless PFC topologies are currently gaining increasing interests [22, 24, 28]. Generally, bridgeless PFC converters suffer from the difficulty of implementation and control, but a bridgeless topology can reduce conduction losses from rectifying bridges; thus, overall system efficiency can be increased. In addition, a bridgeless topology has the advantage of total harmonic distortion (THD) decreasing from input diode reduction. The bridgeless converter circuit shown in Figure 1.4 is typically popular for bridgeless topologies [22], in which the converter operates separately over positive and negative cycles. This circuit is simple and easy to implement, there are fewer limitations to choosing the main passive components. This circuit can be modified into a single-switch bridgeless converter, which has low conduction loss and requires fewer components.

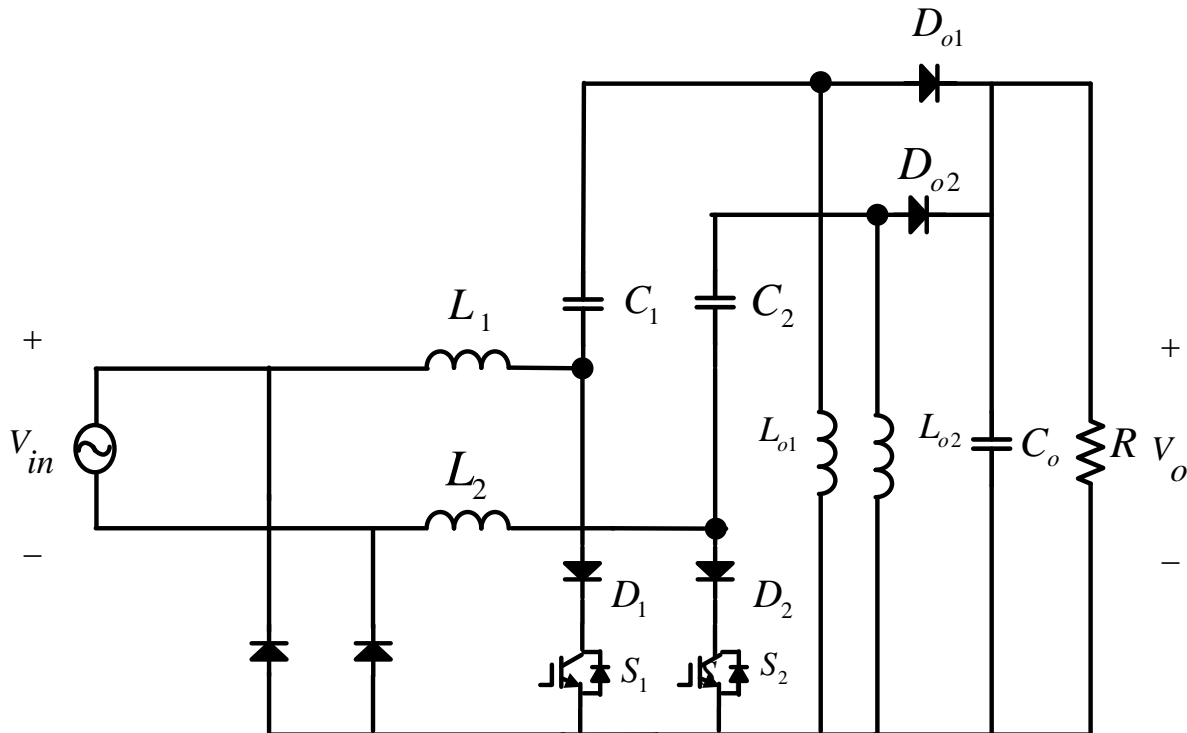
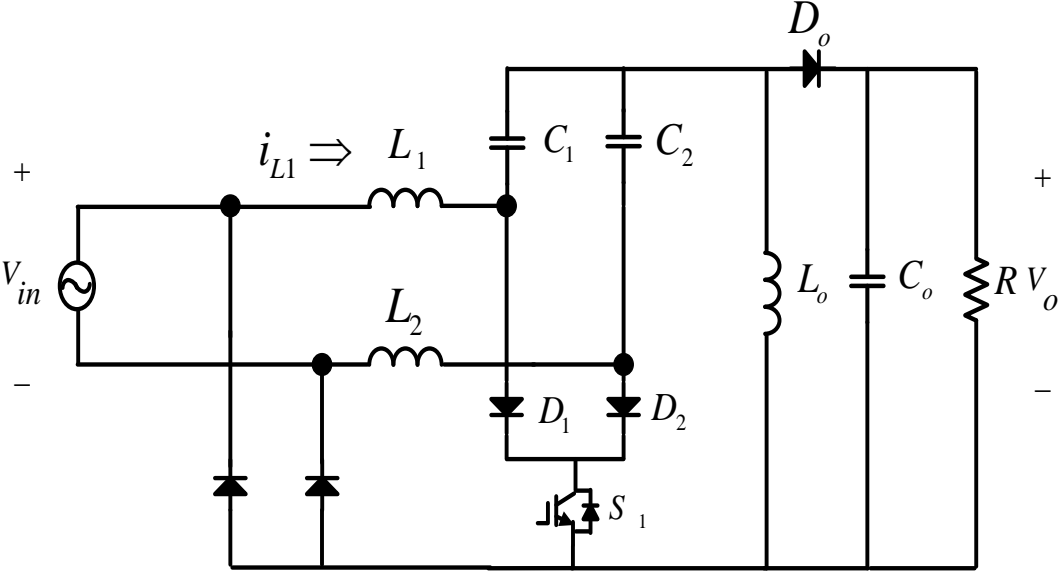


Figure 1.4 Bridgeless SEPIC Converter with separate operation

Figure 1.4 and 1.5 show bridgeless SEPIC converter circuit diagrams. Figure 1.4 shows a bridgeless SEPIC converter that has 2 switches. This circuit requires MOSFET Q1 and Q2 and a series of high-voltage ultra-fast diodes [22, 24]. Thus, the switching and conduction losses are increased. Figure 1.5 shows a single-switch SEPIC converter, which reduces switching and conduction losses but may result in high circulating current losses due to the undesired capacitive coupling loop. The details will be described in Chapter 2.

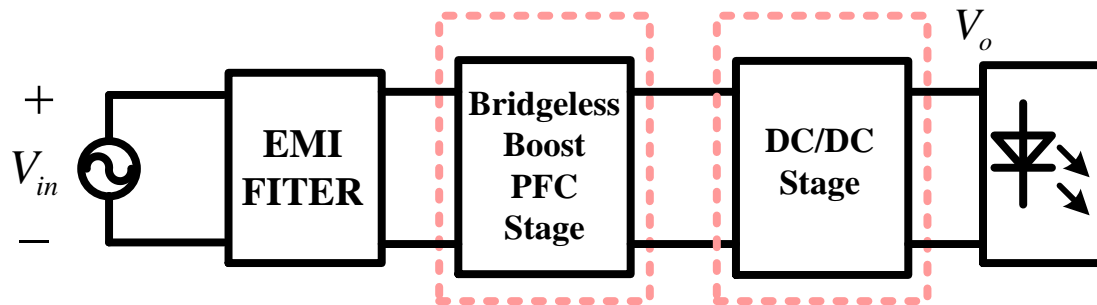


*Figure 1.5 Single Switch Bridgeless SEPIC PFC Converter*

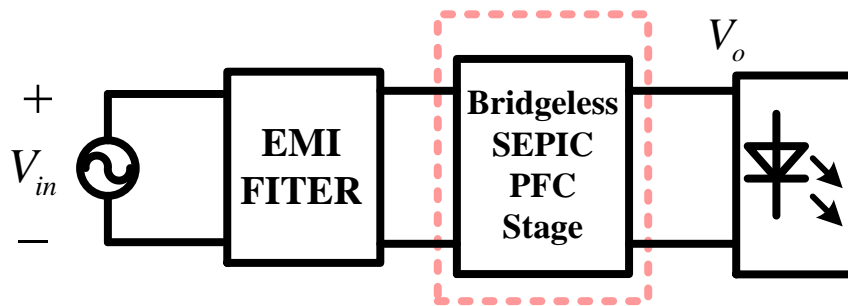
#### ***1.1.4 Comparison and Summary***

As mentioned in section 1.1.1, 1.1.2 and 1.1.3, each topology has advantages and disadvantages regarding to the output voltage limitation, the difficulty of controller implementations. Furthermore, for LED lighting applications, the input of the LED module must be lower than the ac input voltage. Usually, this voltage ranges from 12V to 50V. Therefore, if a boost converter--the most famous and simplest topology-- is adopted, then a second stage is needed to supply proper input power for LED applications, as shown in Figure 1.6. SEPIC with single stage can also be implemented, as shown in Figure 1.7. Considering the above-mentioned advantages and disadvantages, a SEPIC PFC converter can be a good choice if the controller is designed with accurate modeling.

A 150-W single-switch bridgeless SEPIC PFC converter operating in continuous conduction mode (CCM) was adopted in this study. Figure 1.5 shows the circuit diagram of the bridgeless SEPIC PFC converter.



*Figure 1.6 Conventional 2 stage LED driver with boost PFC converter*



*Figure 1.7 Single stage LED driver with SEPIC PFC converter*

## **1.2 REVIEW OF ANALOG AND DIGITAL CONTROL**

This chapter briefly introduces the advantages and disadvantages of analog control and digital control [12, 28-33]. In general, digital control is recognized as being flexible and adaptable to changes in system environment and specifications [12, 27-30, 34]. Thus, digital controller parameters can be modified easily to address variations in device parameters. Moreover, a digital controller has the ability to implement adaptive control. On the other hand, in analog control, manifold small components must be replaced to change control parameters. However, the time delay caused by the computation of a control algorithm with DSP should be considered in digital controller implementation [30, 33]. In addition, the fewer components are required in digital controller implementation, this causes the cost saving. However, this reduction of the cost may not always apply for low-power applications. Many low-cost digital ICs are currently on the market. The selection of low-cost digital control ICs should be considered to take advantage of digital control in low-power applications.

## **1.3 GOAL OF THESIS**

This thesis is concerned with the modeling and controller design of a 150 W single-switch bridgeless SEPIC PFC converter. Verification through implementation is performed. Although, the SEPIC PFC converter has many advantages, it is not currently receiving much attention because of the associated difficulty of implementation and complexity of control caused by the complex structure of the circuit. In this thesis, the controller design procedure is described; it is based on precise modeling and a proper design of the damping circuit because the controller design of a SEPIC converter is known to be difficult. Analog and digital controller design will be presented. The digital controller design of a bridgeless SEPIC PFC converter is particularly significant because most of the literature discusses the use of a boost converter as a

PFC converter topology. Furthermore, 5<sup>th</sup>-order system modeling, which includes a damping circuit, is performed and expressed both symbolically and numerically. The simulation and experimental results are presented to verify the controller design and to compare with the EC 62000-3-2 Class C standard to determine whether the design meets the international standard.

#### **1.4 THESIS OUTLINE**

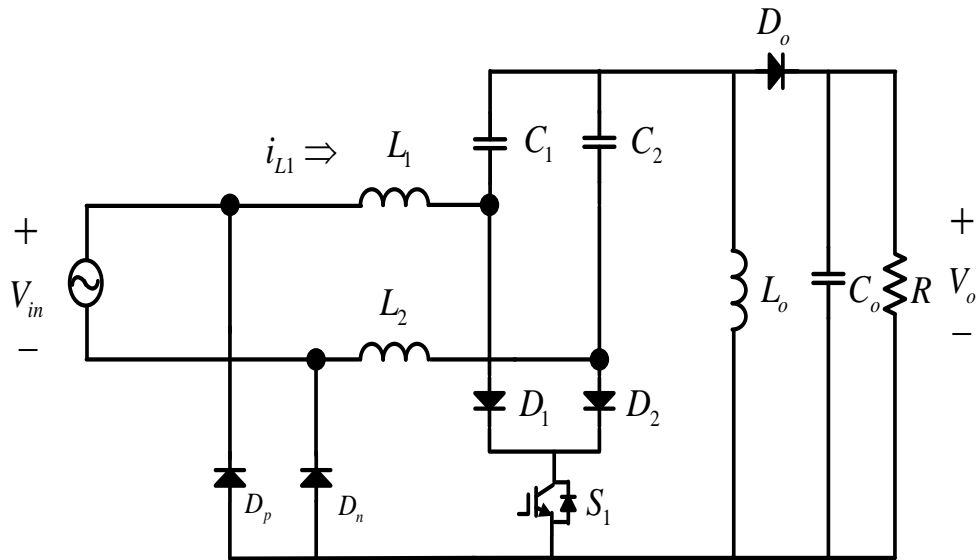
This thesis focuses on the modeling and controller design of a bridgeless SEPIC PFC converter. An analog and a digital controller are implemented. Chapter 1 presents the introduction of this thesis and literature reviews. Chapter 2 introduces the modeling procedure and the verification of the derived model. Chapter 3 discusses the analog controller design and verifies the simulation and experimental results. Chapter 4 focuses on the digital controller design and its verification by simulation results and experiment. Finally, chapter 5 concludes the thesis and offers ideas for future work.

## 2 MODELING THE SINGLE SWITCH BRIDGELESS SEPIC CONVERTER

### 2.1 INTRODUCTION

To design a robust controller, a precise modeling is necessary. The conventional SEPIC converter has a complex model of the 4<sup>th</sup> order, which is derived from the four passive components in the power-stage. This complex high-order system increases the difficulty of obtaining a precise model.

As the SEPIC converter works in CCM, two operation modes (the on-time of switch  $S_1$  and the off-time of switch  $S_1$ ) need to be analyzed to obtain the system transfer functions. The obtained transfer functions are an essential part of the design of the feedback controllers. In this chapter, a modeling method will be briefly introduced. Then, the process of system modeling will be shown. Finally, the obtained model will be verified using the design software.



*Figure 2.1 A diagram of the bridgeless SEPIC PFC converter.*

### 2.1.1 Power Stage Specification

The power stage specifications of the bridgeless SEPIC PFC converter, as shown in Figure 2.1, is designed with following power stage specification:

- Input voltage ( $V_{in}$ ):  $95V_{RMS} \sim 135V_{RMS}$  at 60 Hz
- Output voltage ( $V_o$ ): 50 V
- Output power ( $P_o$ ): 150 W
- Switching frequency ( $F_s$ ): 100 kHz
- Meet the EC 61000-3-2 Class C standard for lighting equipment
- Power Factor (PF) : > 0.95

### 2.1.2 Components Selections

The main components were selected according to the following rationale [7].

- Energy transfer capacitor C1:  $0.47\mu F$ 
  - ➔ The 2 inductors current ripple steering effect depends on the C1 capacitance
- Output capacitor Co:  $3mF$ 
  - ➔ The magnitude of the regulated output voltage ripple is decided by the C2 capacitance.
- Input inductor L1 & output inductor L2:  $600\mu H$ 
  - ➔ The size of the inductor current ripple is decided by the L1 inductance.



## 2.2 MODELING BRIDGELESS SEPIC PFC CONVERTER

### 2.2.1 *Bridgeless SEPIC Converter Model*

Figure 2.1 shows a diagram of the single-switch bridgeless SEPIC PFC converter that will be verified in this thesis. As shown in the diagram, there is only one active switch that makes the topology simple, but the two inductors and two capacitors make the modeling complicated. Figure 2.2-(a) and (b) depict the operations for each cycle of the switch on-time and the switch off-time in the positive half cycle. During the positive half cycle, L1 is working and L2 is left uncontrolled. Although the desired sensing current is the only current through L1, the actual sensing current is the sum of currents flowing into L1 and L2. The current flowing in L2 creates an undesired ripple of the sensed current during positive half line cycle. Inductances of L1 and L2 should be selected with consideration of these ripples. Another distinction of this topology is the undesired circulating current from the capacitive coupling loop, shown in Figure 2.2 (a) and (b) by the green line. The circulating current causes power loss but does not significantly affect the total efficiency, so, in this these it will not be considered.

Although the two features mentioned above affect the system performance, the effects are not significantly impact the model of the system. Thus, the analysis of the small-signal linear model is performed while assuming a quasi-static condition [23], and the input and output voltage are considered to be constant voltages because the switching frequency is much higher than the line frequency.

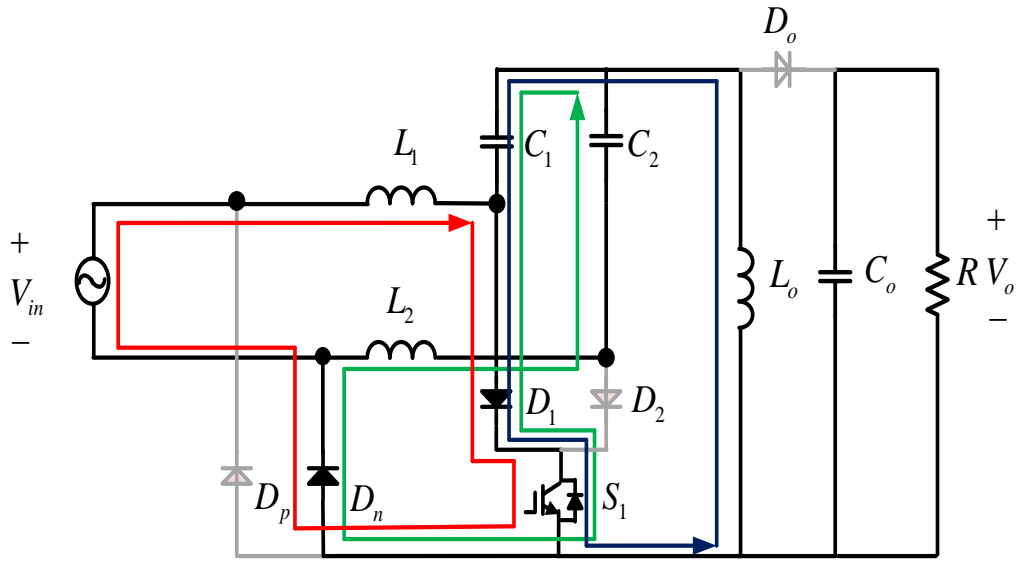


Figure 2.2 (a) Diagram of the bridgeless SEPIC PFC converter (switch-on).

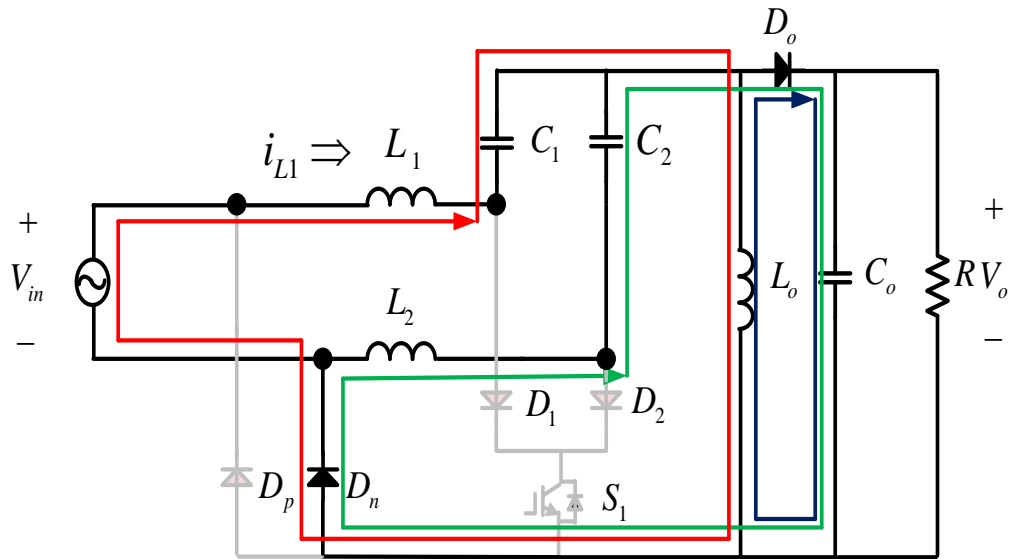


Figure 2.2 (b) Diagram of the bridgeless SEPIC PFC converter (switch-off).

## 2.2.2 Operation Mode Analysis

### ❖ Switch-On stage

Figure 2.3 shows the on-time diagram for switch S1, for which switch S1 is on, and diode D1 is off. The input side inductor L1 is charged from the input voltage in this stage, the charged C1 transfers energy into the output side inductor Lo, and Lo is charging in this stage. In addition, the load current comes from the charged output capacitor Co. Based on the inductor volt-second balance and the capacitor charge balance, (Eq. 2.1-2.4) are obtained.

- The voltage across L1 is the same as input voltage,  $V_{in}$ .

$$L_1 \frac{di_{L1}}{dt} = V_{in} \quad (\text{Eq. 2.1})$$

- The voltage across Lo is the same as the voltage across capacitor, C1.

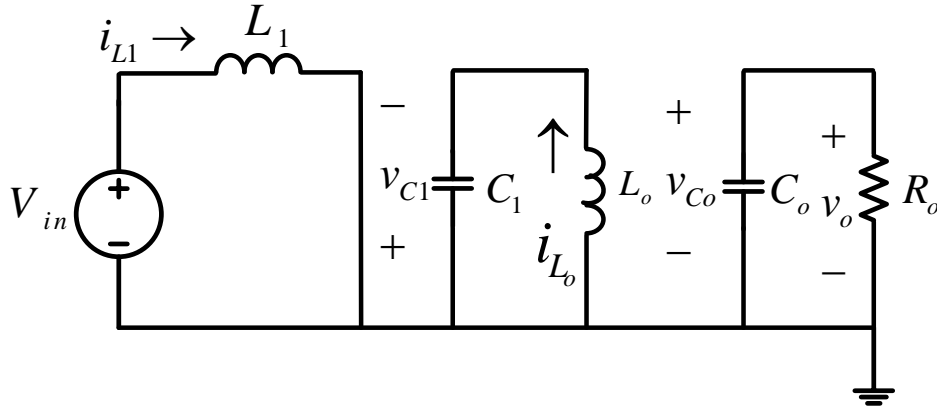
$$L_o \frac{di_{Lo}}{dt} = v_{C1} (\approx V_{in}) \quad (\text{Eq. 2.2})$$

- The current through C1 is the same as the current through inductor L2.

$$C_1 \frac{dv_{C1}}{dt} = -i_{Lo} \quad (\text{Eq. 2.3})$$

- The current through C2 is the same as the load current.

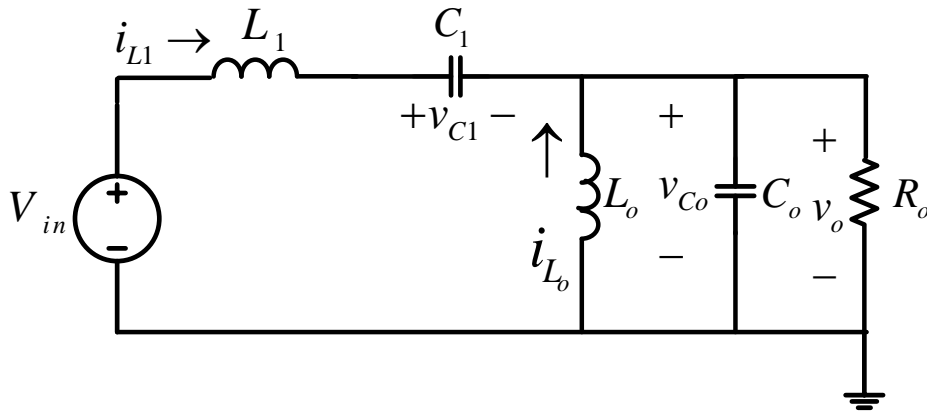
$$C_o \frac{dv_{Co}}{dt} = -\frac{v_o}{R} = -\frac{v_{Co}}{R} \quad (\text{Eq. 2.4})$$



**Figure 2.3 Operation of the SEPIC Converter Switch On-Stage.**

❖ **Switch-Off stage**

Figure 2.4 shows the off-state diagram for switch S1, in which switch S1 is off and the diode D1 is on. Inductor L1 charges the capacitor C1 and provides the load current. The Inductor L2 is connected to the load: it charges the output capacitor C<sub>o</sub> and provides the load current. (Eq. 2.5 – 2.8) are obtained according to the volt-sec balance and the capacitor charge balance.



**Figure 2.4 Operation of the SEPIC Converter Switch Off-Stage.**

- The voltage across L1 is the same as the input voltage,  $V_{in}$ .

$$L_1 \frac{di_{L1}}{dt} = v_{in} - v_{C1} - v_{Co} \quad (\text{Eq. 2.5})$$

- The voltage across L<sub>o</sub> is the same as the voltage across capacitor C1.

$$L_o \frac{di_{Lo}}{dt} = -v_{Co} \quad (\text{Eq. 2.6})$$

- The current through C1 is same as the current through inductor L2.

$$C_1 \frac{dv_{C1}}{dt} = i_{L1} \quad (\text{Eq. 2.7})$$

- The current through C<sub>o</sub> is the sum of currents through two inductors and the current of the load substrate.

$$C_o \frac{dv_{Co}}{dt} = i_{L1} + i_{Lo} - \frac{v_{Co}}{R} \quad (\text{Eq. 2.8})$$

### 2.2.3 State-Space Averaging Model

There are different kinds of averaging modeling methods for a given power stage: the state-space averaging method, the PWM switch modeling method and the circuit average method. In this thesis, the state-space method [35], which describes an averaging model of the system during 1 switching cycle, is adapted to analyze the SEPIC converters [21]. Given that the SEPIC converter is operating in CCM, there are 2 time intervals during 1 switching cycle, T, for which: switch S1 has an on-time, (d)T and an, off-time, (1-d)T, where d is the duty cycle.

The state-space equations over 1 cycle can be expressed according to (Eq. 2.9 - 2.10):

$$\frac{dx}{dt} = Ax + Bu = (A_1d + A_2d')x + (B_1d + B_2d')u \quad (\text{Eq. 2.9})$$

$$y = Ru \quad (\text{Eq. 2.10})$$

where,

$$x = \begin{bmatrix} i_{L1} \\ i_{Lo} \\ v_{C1} \\ v_{Co} \end{bmatrix}, \quad u = [v_g], \quad \dot{x} = \begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{Lo}}{dt} \\ \frac{dv_{C1}}{dt} \\ \frac{dv_{Co}}{dt} \end{bmatrix}$$

After differentiating (Eq. 2.9), the result is as following:

$$\frac{d\hat{x}(t)}{dt} = A\hat{x}(t) + \{(A_1 - A_2)X + (B_1 - B_2)V_g\}\hat{d}(t) \quad (\text{Eq. 2.11})$$

After applying Laplace transforms on (Eq. 2.11), and re-organizing the results to obtain the transfer functions, the result is:

$$\frac{x(s)}{d(s)} = (sI - A)^{-1} \{ (A_1 - A_2)X + (B_1 - B_2)V_g \} \quad (\text{Eq. 2.12})$$

From (Eq. 2.12), the control-to-output voltage transfer function,  $G_{vd}(s)$ , and the control-to-inductor current,  $G_{id}(s)$  can be obtained.

According to (Eq. 2.1 - 2.4) for an interval of time  $d$ , the state vectors for the switch on-time are:

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{RC_o} \end{bmatrix} \quad B_1 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_o} \\ 0 \\ 0 \end{bmatrix} \quad (\text{Eq. 2.13})$$

According to (Eq. 2.5 – 2.8) for an interval of time  $d'$  ( $=1-d$ ), the state vectors of the switch off-time are as follows:

$$A_2 = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & -\frac{1}{L_1} \\ 0 & 0 & 0 & -\frac{1}{L_o} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{1}{C_2} & \frac{1}{C_o} & 0 & -\frac{1}{RC_o} \end{bmatrix} \quad B_2 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (\text{Eq. 2.14})$$

One of the benefits of the state-space method is the ease of obtaining transfer functions using generic software. Thus, MATLAB will be used as the design-software in this thesis.

### 2.2.4 Frequency Response Analysis

According to the design specification parameters mentioned in chapter 2.1.1, the state vectors for both switching intervals (Eq.2.13 - 2.14) and a quasi-state assumption, following the numerical expression of the control-to-inductor current transfer function is obtained assuming a 120V input [21, 35].

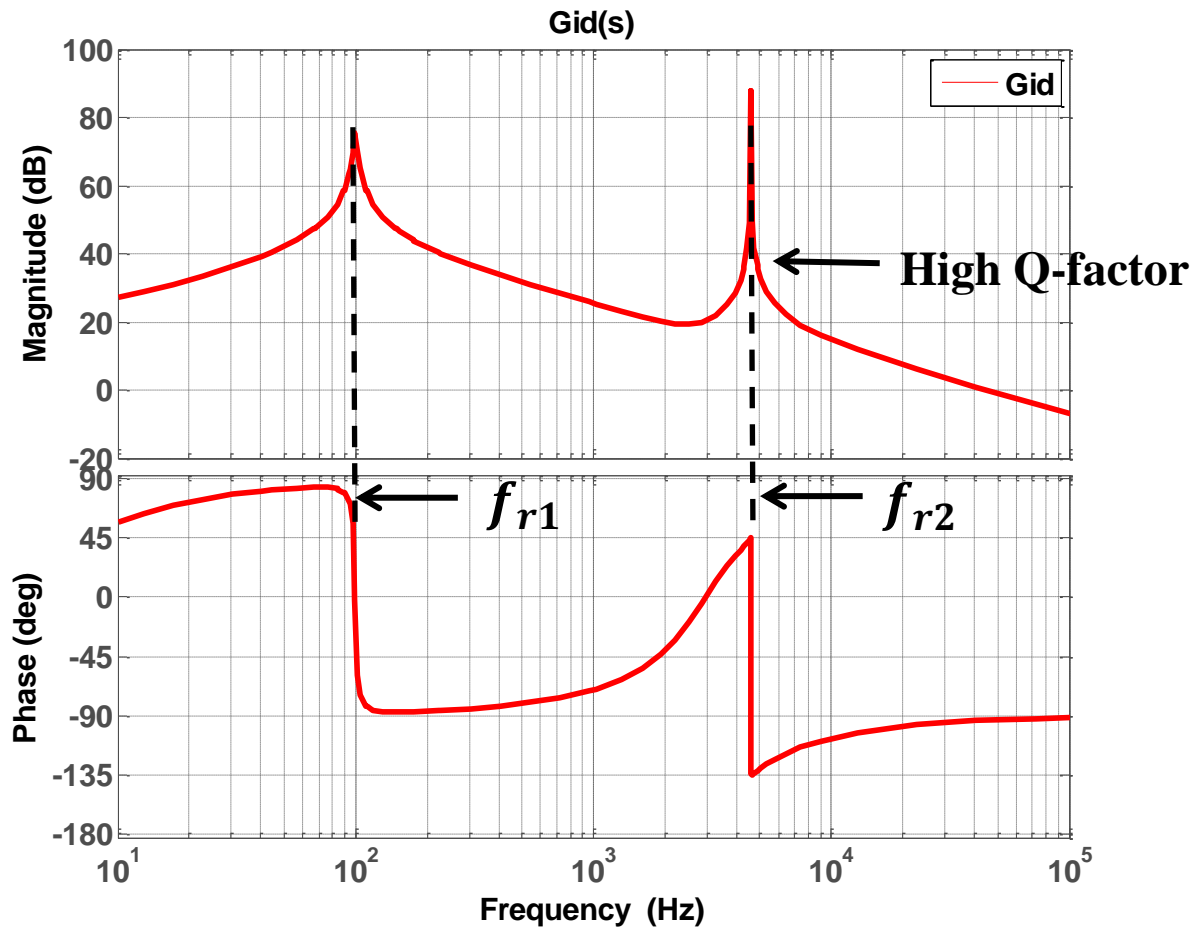
$$G_{id}(s) = \frac{(2.83 * 10^5)s^3 + (5.07 * 10^9)s^2 + (9.81 * 10^{13})s + (3.92 * 10^{15})}{s^4 + 20s^3 + (8.31 * 10^8)s^2 + (1.66 * 10^{10})s + (3.26 * 10^{14})} \quad (\text{Eq. 2.15})$$

Figure 2.5 shows the frequency response of the derived control-to-inductor model. As shown in Figure 2.5, there are 2 resonance locations, and one of them has high Q-factor. In addition, from the state-matrix and the transfer function with the characterized parameters, the locations of 2 resonance points are determined as shown in Table 2.2. Those locations are related to the main passive components and the duty cycle that presents the relation between the input voltage and the output voltage.

*Table 2.1 Locations of resonance.*

	<b>Resonance point 1</b>	<b>Resonance point 2</b>
<b>Frequency</b>	$f_{r1} = \frac{1}{2\pi} \sqrt{\frac{(1-D)}{L_o C_o}}$	$f_{r2} = \frac{1}{2\pi} \sqrt{\frac{(1-D)}{L_1 C_1}}$





*Figure 2.5 Frequency Response with 120V input voltage*

### 2.2.5 Issue of SEPIC PFC Converter

A stabilized system is not easy to achieve with a second resonance point due to the significant high Q-factor of it. The un-damped resonance causes oscillations in the input current with the same frequency of the second resonance point. The oscillating current makes the system unstable. This current is observed either in a closed loop Bode diagram, simulation results or experimental results. To overcome this issue, implementing a damping circuit seems to be better solution than designing a controller that lacks a damping circuit to prevent resonance with high Q.

## 2.3 MODELING THE MODIFIED BRIDGELESS SEPIC

### 2.3.1 The Modified Bridgeless SEPIC Converter Model

As mentioned in Chapter 2.2.5, the system has the high possibility of instability. The method can reduce high Q effect needs to be considered to make a stable system. Then, the system can address in uncertain interrupt. In addition, the damping circuit will make controller designs much easier than with high Q-factor. In this thesis, the R-C damping circuit parallel with the energy transfer capacitor  $C_1$  is adopted to reduce the Q-factor and to prevent from oscillation current issues [23, 36]. The modified bridgeless SEPIC converter diagram is shown in Figure 2.6 with the introduced R-C damping circuit.

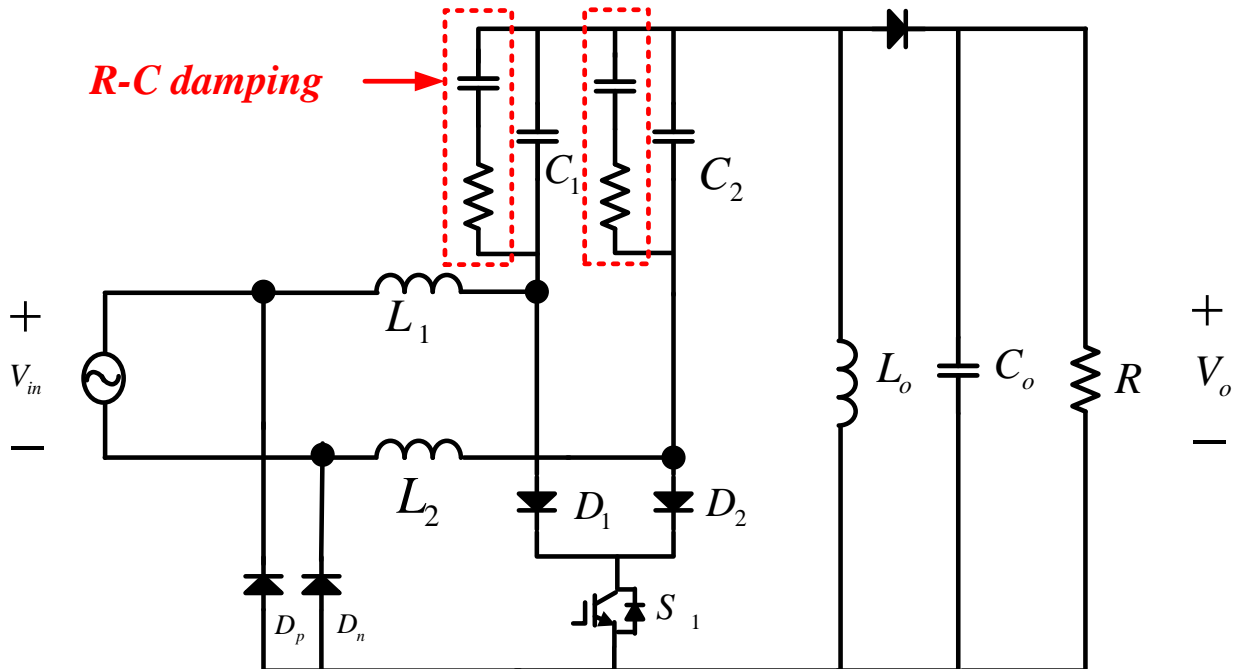
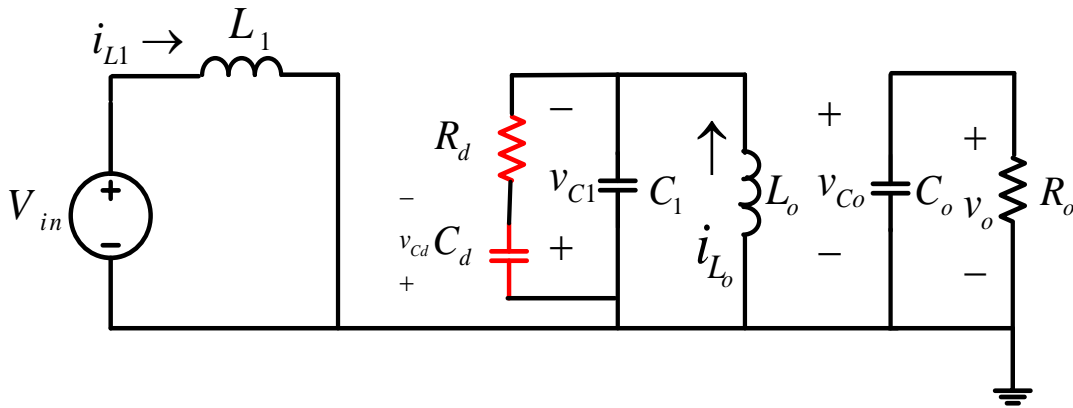


Figure 2.6 Diagram of the modified Bridgeless SEPIC PFC converter.

### 2.3.2 Operation Mode Analysis

#### ❖ Switch-On stage

Figure 2.7 shows the on-time diagram for switch S1, for which switch S1 is on and the diode D1 is off. This circuit includes a Rd-Cd damping circuit to decrease the risk of instability. The basic operations of L1, C1, Lo and Co are same as conventional SEPIC operations which are described in chapter 2.2. Only the difference is the added Rd-Cd damping circuit parallel with the energy transfer capacitor C1. The current pass through C1 is divided into Lo and Rd-Cd circuit as well. In this modified SEPIC converter, the state vector needs to consider the damping capacitor Cd.



**Figure 2.7 Operation of the modified SEPIC Converter Switch On-Stage.**

- The voltage across L1 is the same as the input voltage,  $V_{in}$ .

$$L_1 \frac{di_{L1}}{dt} = V_{in} \quad (\text{Eq. 2.16})$$

- The voltage across Lo is the same as the voltage across capacitor C1.

$$L_2 \frac{di_{L2}}{dt} = v_{C1} (\approx V_{in}) \quad (\text{Eq. 2.17})$$

- The current through C1 is the sum of currents through inductor Lo and damping resistor Rd.

$$C_1 \frac{dv_{C1}}{dt} = -i_{L_o} - \frac{v_{C1} - v_{Cd}}{R_d} \quad (\text{Eq. 2.18})$$

- The current through the damping capacitor Cd is the same as the current through damping resistor Rd, and the voltage across Rd is the difference between voltages across C1 and Cd.

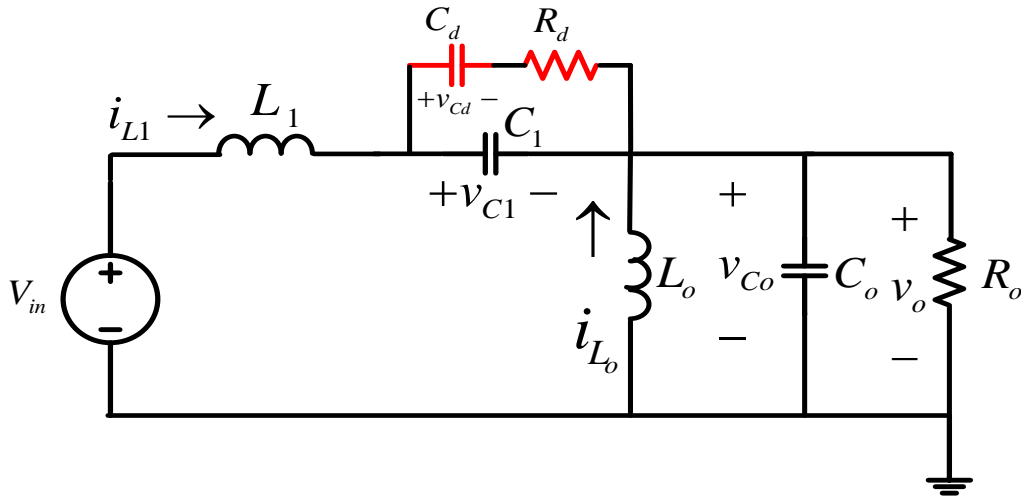
$$C_d \frac{dv_{Cd}}{dt} = \frac{v_{C1} - v_{Cd}}{R_d} \quad (\text{Eq. 2.19})$$

- The current through Co is the same as the load current.

$$C_2 \frac{dv_{C2}}{dt} = -\frac{v_o}{R} = -\frac{v_{C2}}{R} \quad (\text{Eq. 2.20})$$

❖ *Switch-Off stage*

Figure 2.8 shows a switch S1 off-state diagram with the Rd-Cd damping circuit. The switch S1 off-state operation is also similar to conventional SEPIC operations. Only the difference is that the added damping circuit should be analyzed with other passive components, so the state vector could have an element of Cd.



**Figure 2.8 Operation of the modified SEPIC Converter Switch Off-Stage.**

- The voltage across L1 is the difference between the input voltage and the output voltage.

$$L_1 \frac{di_{L1}}{dt} = V_{in} - v_{C1} - v_{Co} \quad (\text{Eq. 2.21})$$

- The voltage across Lo is the same as the output voltage.

$$L_o \frac{di_{Lo}}{dt} = -v_{Co} \quad (\text{Eq. 2.22})$$

- The current through L1 divides into the current through the damping circuit and the C1 capacitor. So, the current through C1 is the difference between the current through C1 and L1.

$$C_1 \frac{dv_{C1}}{dt} = i_{L1} - \frac{v_{C1} - v_{Cd}}{R_d} \quad (\text{Eq. 2.23})$$

- The current through the damping capacitor Cd is the same as the current through the damping resistor Rd. The voltage across Rd is the voltage difference between the voltages across C1 and Cd.

$$C_d \frac{dv_{Cd}}{dt} = \frac{v_{C1} - v_{Cd}}{R_d} \quad (\text{Eq. 2.24})$$

- The current through Co is the sum of currents through two inductors and the current of the load substrate.

$$C_o \frac{dv_{Co}}{dt} = i_{L1} + i_{Lo} - \frac{v_{Co}}{R} \quad (\text{Eq. 2.25})$$

### 2.3.3 State-Space Averaging Model

The state-space method [35] is used to analyze the given modified SEPIC converter. The procedures to obtain state vectors are the same as that of chapter 2.2.3. In this chapter, the procedures will be omitted and the final state vectors are shown for the modified SEPIC converter.

❖ State vectors of for the switch on-time are:

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C_1} & -\frac{1}{R_d C_1} & \frac{1}{R_d C_1} & 0 \\ 0 & 0 & \frac{1}{R_d C_d} & -\frac{1}{R_d C_d} & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{RC_o} \end{bmatrix} \quad B_1 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_o} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (\text{Eq. 2.26})$$

❖ State vectors of the switch off-time are as follows:

$$A_2 = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & 0 & -\frac{1}{L_1} \\ 0 & 0 & 0 & 0 & -\frac{1}{L_o} \\ \frac{1}{C_1} & 0 & -\frac{1}{R_d C_1} & \frac{1}{R_d C_1} & 0 \\ 0 & 0 & \frac{1}{R_d C_d} & -\frac{1}{R_d C_d} & 0 \\ \frac{1}{C_o} & \frac{1}{C_o} & 0 & 0 & -\frac{1}{RC_o} \end{bmatrix} \quad B_2 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (\text{Eq. 2.27})$$

where,

$$x = \begin{bmatrix} i_{L1} \\ i_{L_o} \\ v_{C1} \\ v_{Cd} \\ v_{Co} \end{bmatrix}, \quad u = [v_g], \quad \dot{x} = \begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L_o}}{dt} \\ \frac{dv_{C1}}{dt} \\ \frac{dv_{Cd}}{dt} \\ \frac{dv_{Co}}{dt} \end{bmatrix}$$

### 2.3.4 Frequency Response Analysis

❖ Control-to-inductor model,  $G_{id}(s)$

Based on state matrices, (Eq. 2.26 – 2.27) and (Eq. 2.12), the symbolic expression of the control-to-inductor model transfer function is obtained as follows:

$$G_{id}(s) = \frac{N_1 s^4 + N_2 s^3 + N_3 s^2 + N_4 s + N_5}{D_1 s^5 + D_2 s^4 + D_3 s^3 + D_4 s^2 + D_5 s + D_6} \quad (\text{Eq. 2.28})$$

All numerators are defined with symbolic parameters as follows:

$$\begin{aligned} N_1 &= C_1 C_o C_d R R_d V_{in} \\ N_2 &= C_o L_o R V_{in} (C_1 R + C_d R + C_1 C_d R_d + C_1 C_d D R_d + C_d D R_d) \\ N_3 &= L_o R V_{in} \{(1 + D)(C_1 + C_d) + C_o D\} + C_d D R_d V_{in} (L_o + C_o R^2 D) \\ N_4 &= D V_{in} \{L_o + R D (C_o R + C_d R_d)\} \\ N_5 &= 2 R V_{in} D^2 D' \end{aligned}$$

All the denominators are defined with symbolic parameters as follows:

$$\begin{aligned} D_1 &= C_1 C_o C_d L_1 L_o R^2 R_d D' \\ D_2 &= (L_1 L_o R D')(C_1 C_o R + C_o C_d R + C_1 C_d R_d) \\ D_3 &= L_1 L_o R D'(C_1 + C_d) + (C_d R^2 R_d)(C_1 L_1 + C_1 L_o + C_o L_o)(1 - D^3 - 3 D D') \\ D_4 &= R^2 (L_1 + L_o)(C_1 + C_d)(1 - 3 D D') + L_o R (C_o R + C_d R_d)(1 - 3 D + 3 D^2 - D^3) \\ D_5 &= C_d R_d R^2 (D^4 - 4 D^3 + 6 D^2 + 4 D + 1) + L_o R (-D^3 + 3 D^2 - 3 D + 1) \\ D_6 &= R^2 (D^4 - 4 D^3 + 6 D^2 - 4 D + 1) \end{aligned}$$



The parameter selection of damping circuit is done by a trial-and-error using simulations to make an accordance with C1. The choice of  $R_d$  is not considerably relative to the power loss because it is only less than  $1/4W$  in this power stage. The other parameters except  $R_d$ - $C_d$  circuit parameters are same as specified parameters as mentioned in chapter 2.1.1 and  $R_d$ - $C_d$  parameters are chosen to make a proper damping. Following the numerical expression of the control-to-inductor current transfer function with the damping circuit is obtained with  $R_d$ - $C_d$  selections of  $R_d = 60\Omega$ ,  $C_d = 1\mu F$

As expressed in (Eq. 2.29), the numerical expression of modified SEPIC converter became a 5th order system.

$$G_{id\_damp}(s) = \frac{(2.83 * 10^5)s^4 + (1.98 * 10^{10})s^3 + (2.76 * 10^{14})s^2 + (3.48 * 10^{18})s + (1.40 * 10^{20})}{s^5 + (5.22 * 10^4)s^4 + (8.32 * 10^8)s^3 + (2.95 * 10^{13})s^2 + (9.15 * 10^{14})s + (1.16 * 10^{19})} \quad (\text{Eq. 2.29})$$

where,

$$L_1 = 600\mu H, L_o = 600\mu H, C_1 = 0.47\mu F, C_o = 1mF$$

$$V_{in\_rms} = 120V, V_o = 50V, F_s = 100kHz$$

❖ Control-to-output model,  $G_{vd}(s)$

Based on state matrices, (Eq. 2.26 - 2.27) and (Eq. 2.12), the symbolic expression of control-to-output model transfer function is obtained as follows:

$$G_{vd}(s) = \frac{N_1s^4 + N_2s^3 + N_3s^2 + N_4s + N_5}{D_1s^5 + D_2s^4 + D_3s^3 + D_4s^2 + D_5s + D_6} \quad (\text{Eq. 2.30})$$

All numerators are defined with symbolic parameters as follows:

$$\begin{aligned} N_1 &= C_1C_dL_oR_dV_{in} \\ N_2 &= DL_1L_oV_{in}(C_1 + C_d) - C_1C_dRR_dV_{in}(L_1 + L_o)(1 + 2D + D^2) \\ N_3 &= RV_{in}(C_1 + C_d)(L_1 + L_o)(-1 - D^2 + 2D) \\ N_4 &= C_dR_dRV_{in}(D^3 - 3D^2 + 3D - 1) \\ N_5 &= RV_{in}(D^3 - 3D^2 + 3D - 1) \end{aligned}$$

All the denominators are defined with symbolic parameters as follows:

$$\begin{aligned} D_1 &= C_1C_oL_1L_oR(-D^2 + 2D - 1) \\ D_2 &= -L_1L_o(C_1C_oR + C_dC_oR + C_1C_dR_d)(D^2 - 2D + 1) \\ D_3 &= C_dRR_d(C_1L_1 + C_1L_o + C_oL_o)(-D^4 + 4D^3 - 6D^2 + 4D - 1) - L_1L_o(C_1 + C_d)(D - 1)^2 \\ D_4 &= \\ & (C_1L_1R + C_1L_oR + C_oL_oR + C_dL_1R + C_dL_oR + C_dL_oR_d)(-D^4 + 4D^3 - 6D^2 + 4D - 1) \\ D_5 &= L_o(-D^4 + 4D^3 - 6D^2 + 4D - 1) + C_dR_dR(D^5 - 5D^4 + 10D^3 - 10D^2 + 5D - 1) \\ D_6 &= R(D^5 - 5D^4 + 10D^3 - 10D^2 + 5D - 1) \end{aligned}$$

Following the numerical expression of control-to-output transfer function with the added damping circuit is obtained with the Rd-Cd selections of  $R_d = 60\Omega$ ,  $C_d = 1\mu F$ .

As expressed in (Eq. 2.31), the numerical expression of modified SEPIC converter became a 5th order system.

$$G_{vd\_damp}(s) = \frac{(-1417)s^4 + (5.73 \cdot 10^7)s^3 + (6.84 \cdot 10^{12})s^2 + (7.60 \cdot 10^{16})s + (2.69 \cdot 10^{21})}{s^5 + (5.22 \cdot 10^4)s^4 + (8.32 \cdot 10^8)s^3 + (2.95 \cdot 10^{13})s^2 + (9.04 \cdot 10^{14})s + (1.12 \cdot 10^{19})}$$

(Eq. 2.31)

where,

$$L_1 = 600\mu H, L_o = 600\mu H, C_1 = 0.47\mu F, C_o = 1mF$$

$$V_{in\_rms} = 120V, V_o = 50V, F_s = 100kHz$$

### 2.3.5 Comparison of Frequency Response Results

Figure 2.9 shows a small-signal response of control-to-inductor model. It presents the damping effect on the system. Figure 2.10 shows a small-signal response of control-to-output model. As shown in Figure 2.9 and Figure 2.10, there is a significantly reduced resonant Q-factor due to the damping circuit. It could make a different magnitude of resonance depend on selections of  $R_d$ - $C_d$  parameters by simulation. With considering a crossover frequency and a resonant magnitude, the  $R_d$ - $C_d$  parameters are decided. Concerning of a power loss on the damping circuit could be ignored because it is only under  $\frac{1}{4}$  W.

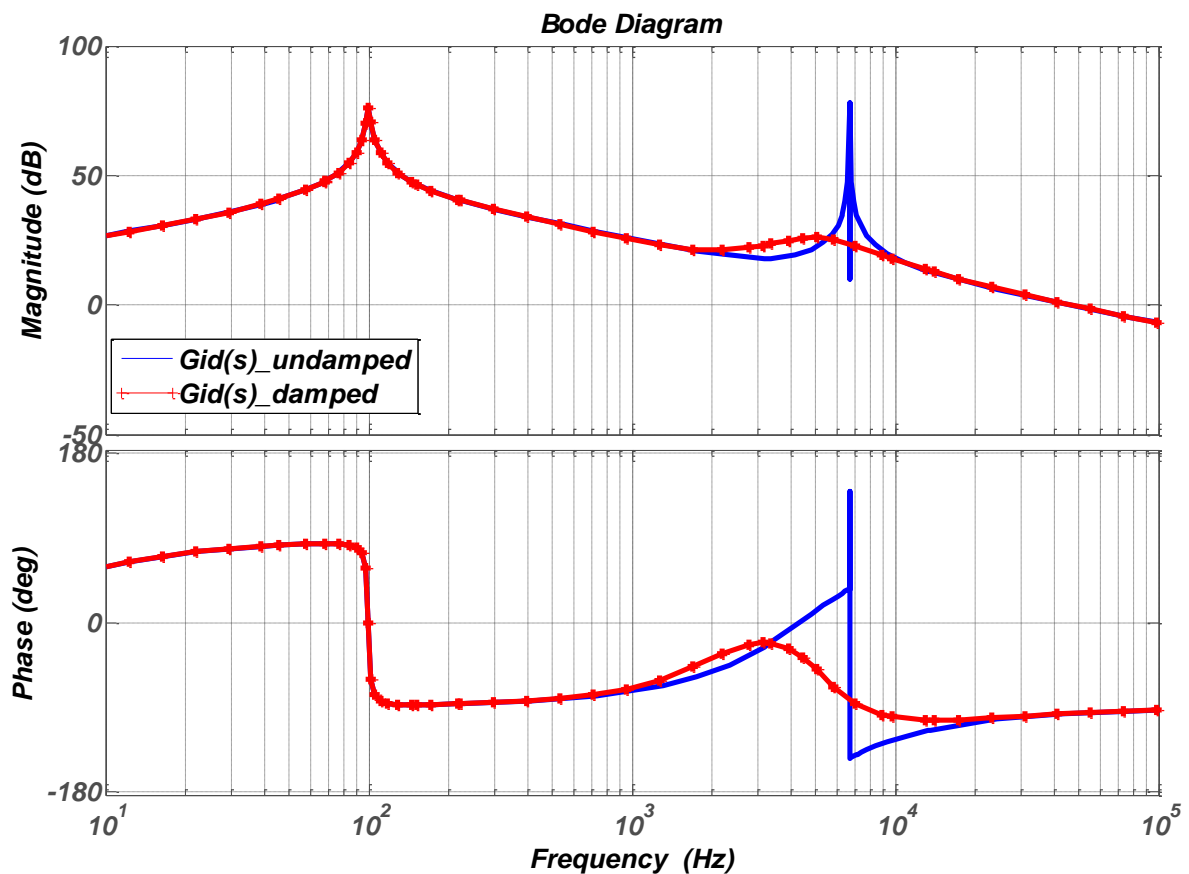
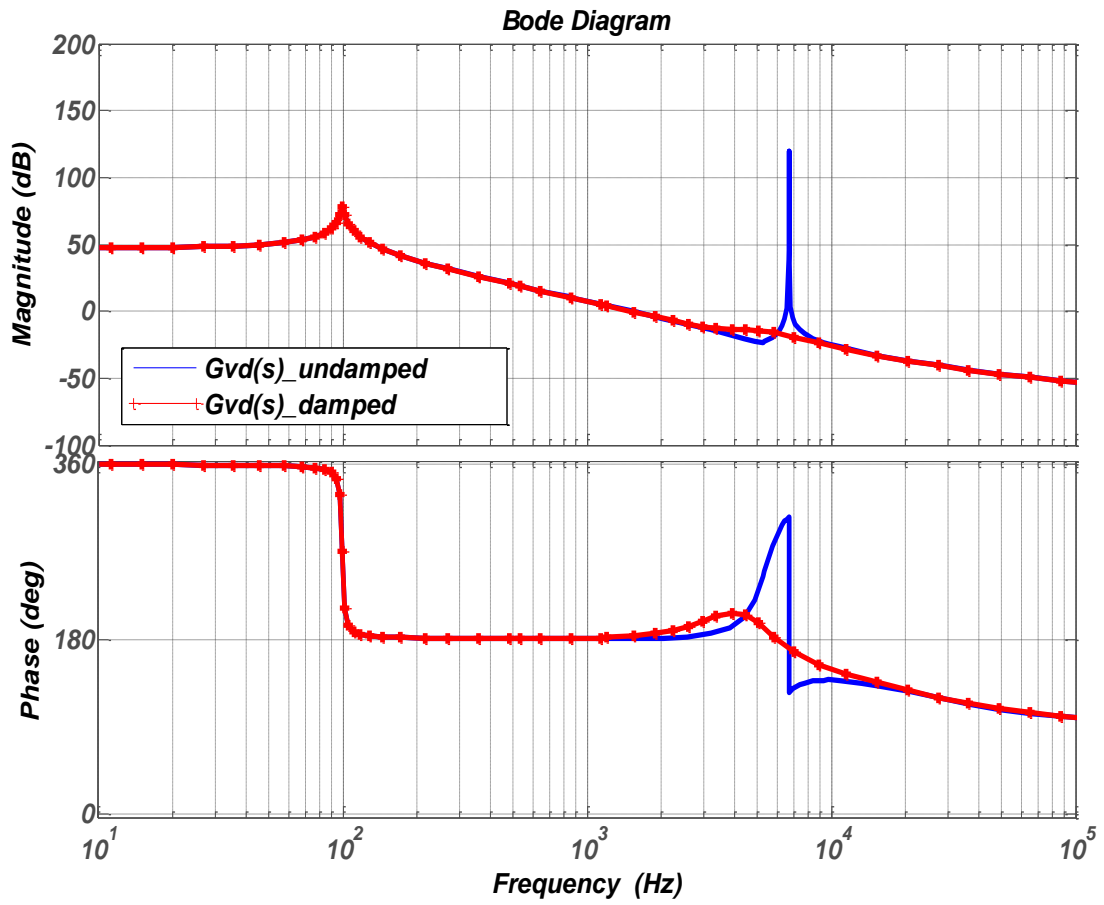


Figure 2.9 Comparison of the control-to-inductor models.



*Figure 2.10 Comparison of the control-to-output models.*

## 2.4 MODELING VERIFICATION

### 2.4.1 *Introduction to modeling verification*

Due to the complexity of the SEPIC topology, a precise modeling is required to design a suitable controller. For this reason, modeling verification to confirm the correctness of the derived model is performed in two ways.

One method is a small-signal response comparison between the derived model and the simulation model. To obtain a small signal response from the simulation, the tool PSIM and MATLAB software are used to obtain the small-signal responses of the derived model.

The second method is a comparison of simulations using the average model and the cycle-by-cycle simulation [10]. The simplified block diagrams of the simulation comparison are shown in Figures 2.11 (a) and (b). In the simulation, the proper magnitude of the input current is multiplied by a sine signal to generate the reference current with which the sensed input current will be compared. In addition, the step response will be verified at time  $t : t_{step}$ . Using the reference current step change, the responses of the simulation results will show whether the derived model matches the actual circuit system. In this stage, a simple PI controller (which might not be well-designed) is used as the current controller. In the average model simulation, the transfer function derived in (Eq. 2.28) is adopted to verify the derived model transfer function.

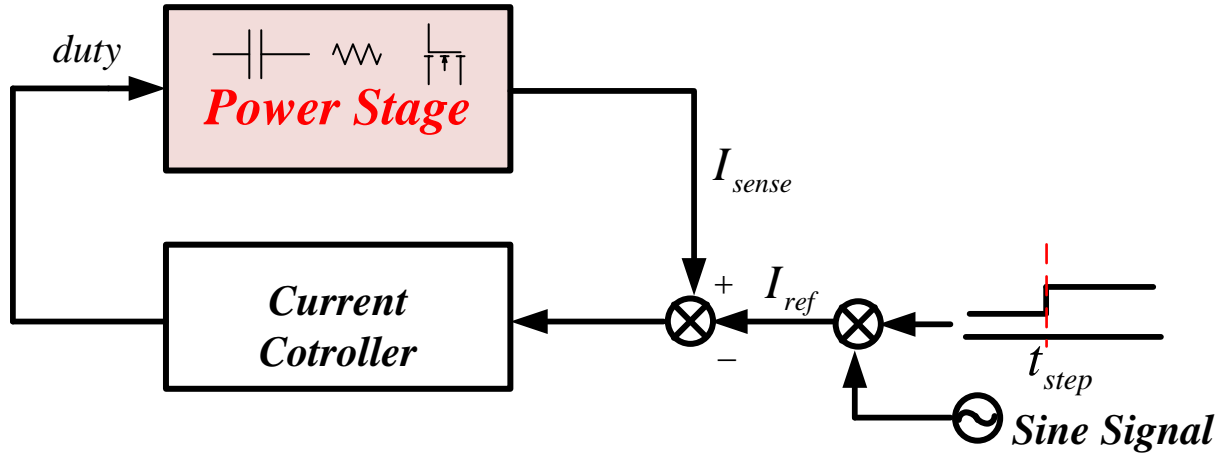


Figure 2.11 (a) Diagram of the cycle-by-cycle simulation.

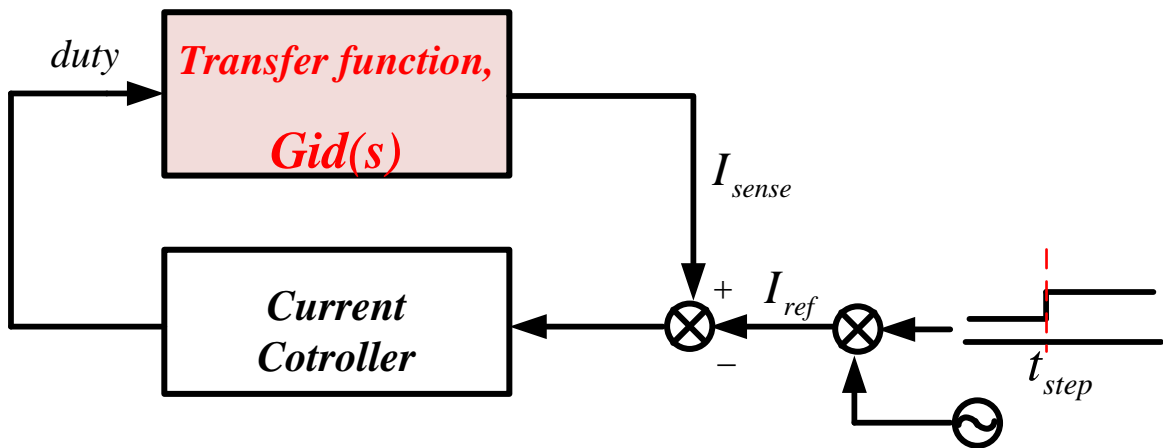


Figure 2.11 (b) Diagram of the average model simulation.

### 2.4.2 Comparison of the small-signal response result.

A comparison is made between the derived model and the simulation model. The control-to-inductor model is verified in Figures 2.12 (a) and (b). The comparison result of the magnitude response between the derived model and the simulation is shown in Figure 2.12 (a), and the phase response results of both are shown in Figure 2.12 (b). From these results, the derived model demonstrates validity.

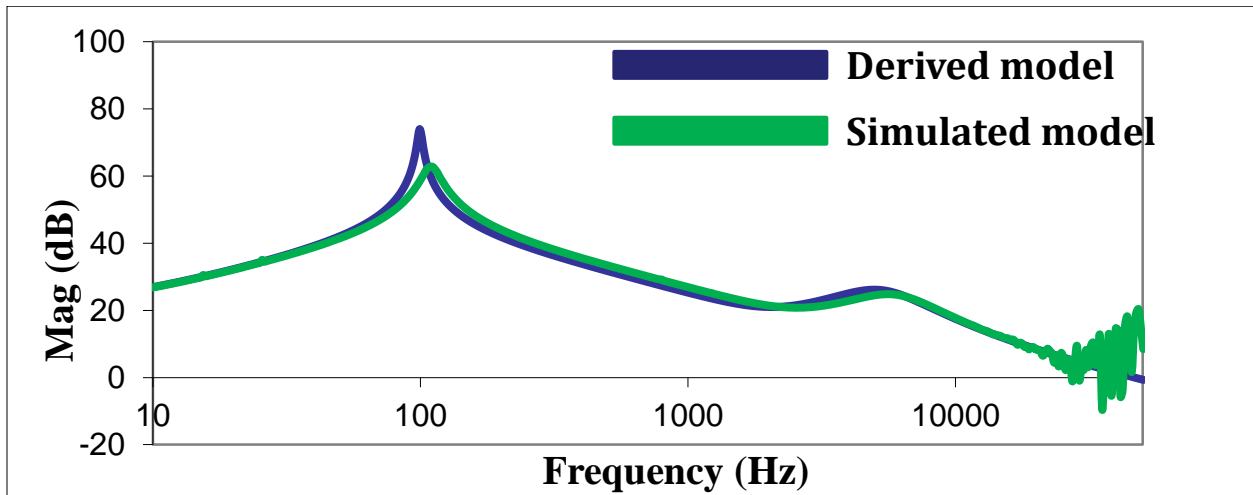


Figure 2.12 (a) Magnitude response comparison of  $G_{id}(s)$

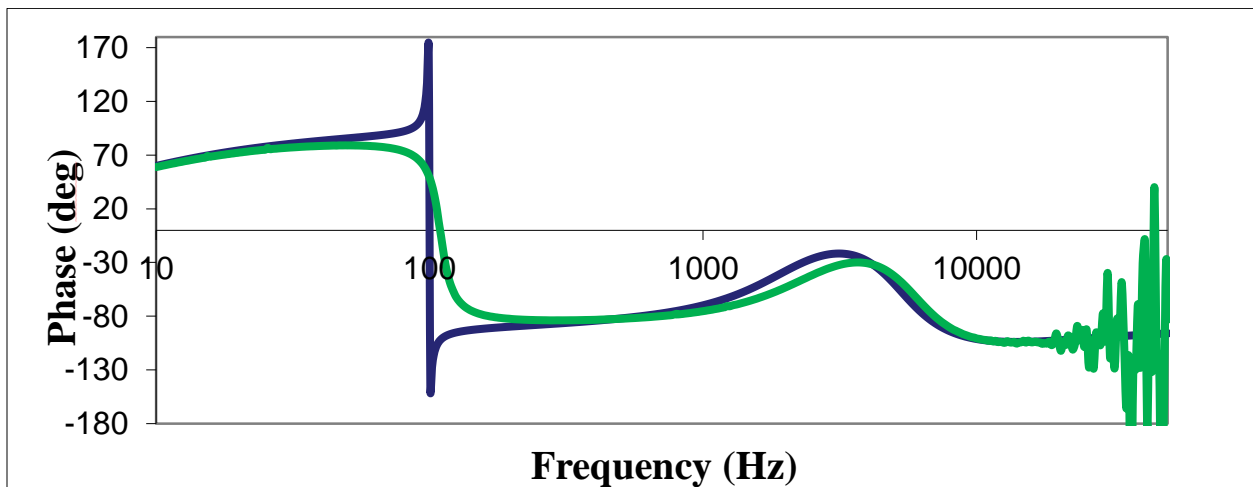


Figure 2.12 (b) Phase response comparison of  $G_{id}(s)$



The control-to-output model is verified in Figures 2.13 (a) and (b). The comparison result between the derived model and simulation are shown in Figures 2.13 (a) and (b). From these results, the derived model demonstrates its validity.

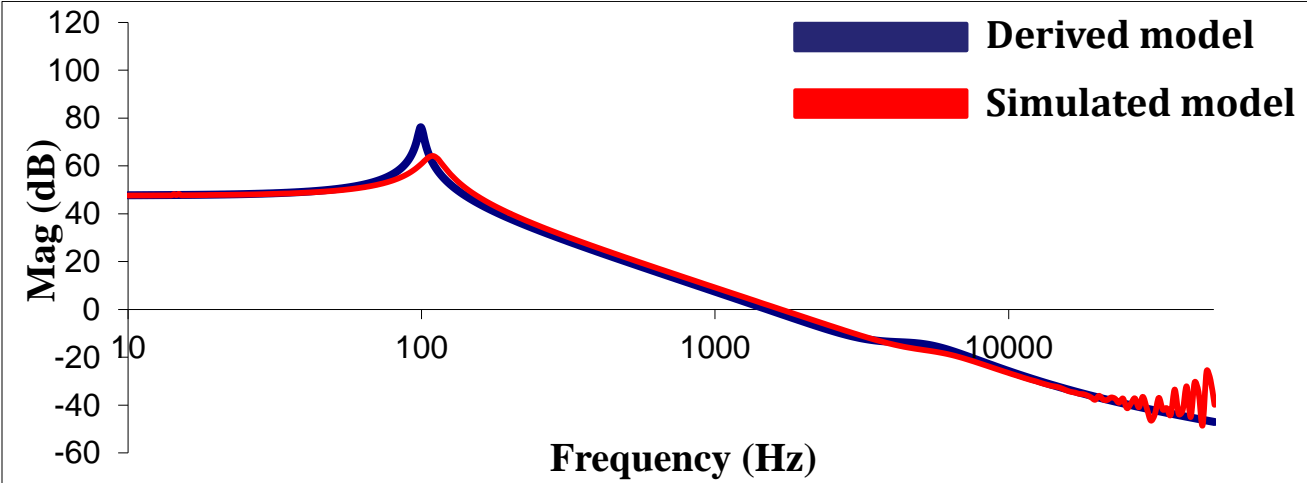


Figure 2.13 (a) Magnitude response comparison of  $G_{vd}(s)$

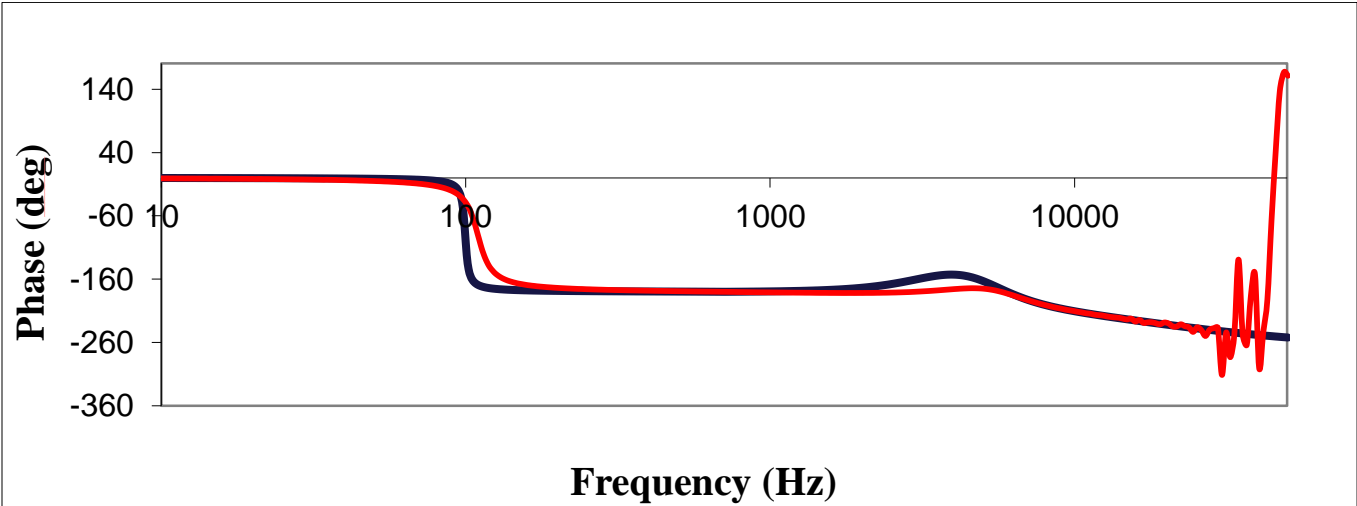


Figure 2.13 (b) Phase response comparison of  $G_{vd}(s)$

### 2.4.3 Comparison of Cycle-by-Cycle and Average Model Simulation Results

The simulation can be performed with both the cycle-by-cycle simulation and with the derived average model. The comparison result is shown in Figure 2.14. This result shows that the derived average model, which is expressed in (Eq. 2.28), matches the system circuit model, which consists of the parameters given in chapter 2.1.1 and 2.1.2. In this simulation, the given condition is the step change of the reference current at time  $t = t_{step}$ . Figure 2.12 shows an even step-response of 2 different simulations with the step change. It verifies that the transfer function of system is well-derived.

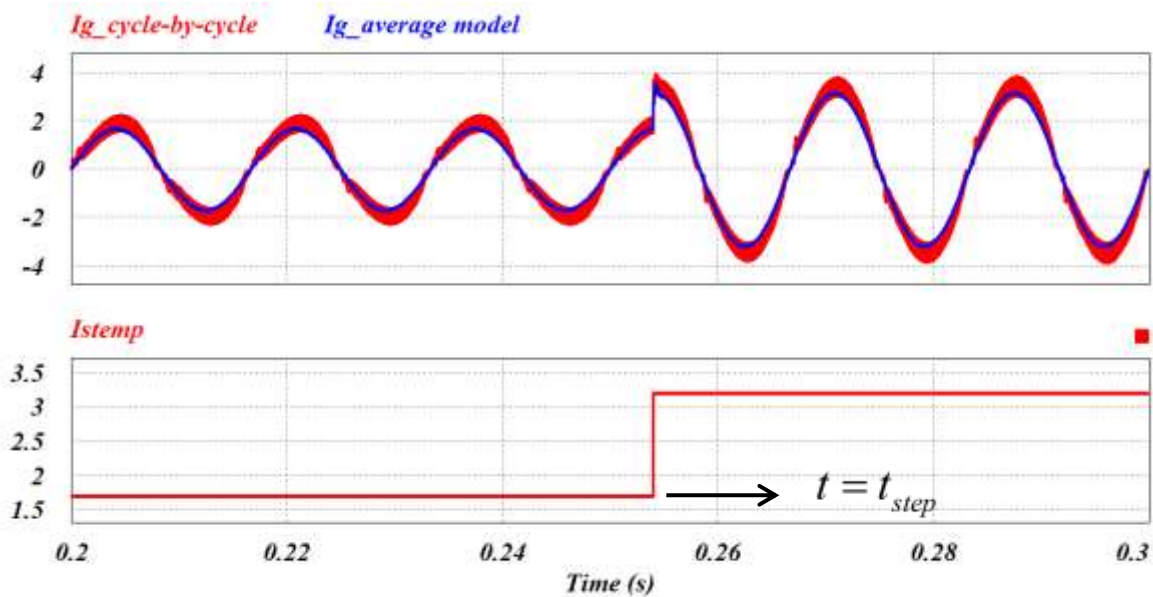


Figure 2.14 Comparison of the model simulation results.

### 3 ANALOG CONTROLLER DESIGN AND VERIFICATIONS

#### 3.1 INTRODUCTION

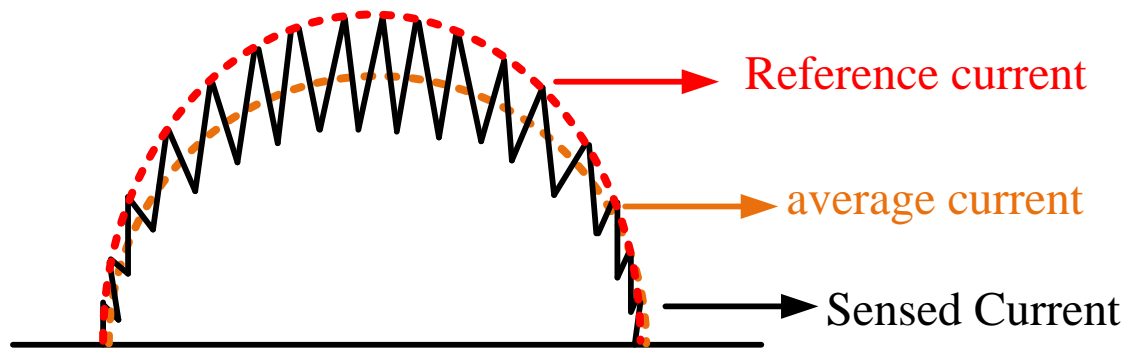
##### 3.1.1 Current control overview

Comparisons of different current control techniques performed in previous studies [23, 26, 35], find that each technique has its advantages and disadvantages. The Pros and cons of each scheme and a brief expression for the control scheme [25] are as follows:

❖ Peak current control scheme

In the peak current control method, a switch is turned on with a constant switching frequency, and a switch is turned off when the sensed current reaches the reference sinusoidal current as shown in Figure 3.1.

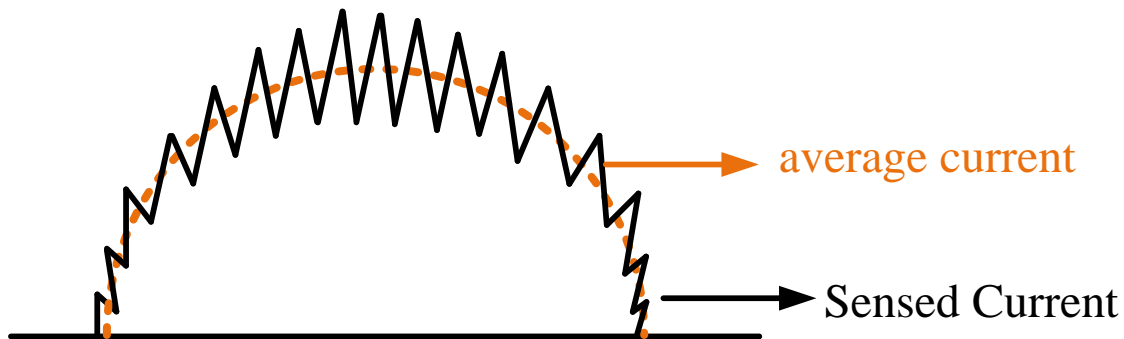
This scheme could reduce the power loss, because this method typically senses the switch current with a current transformer not a sensing resistor. A disadvantage of this method is the possibility of current distortion. In addition, this method has sensitivity to noise.



*Figure 3.1 Peak Current Control Scheme.*

- ❖ Average current control scheme

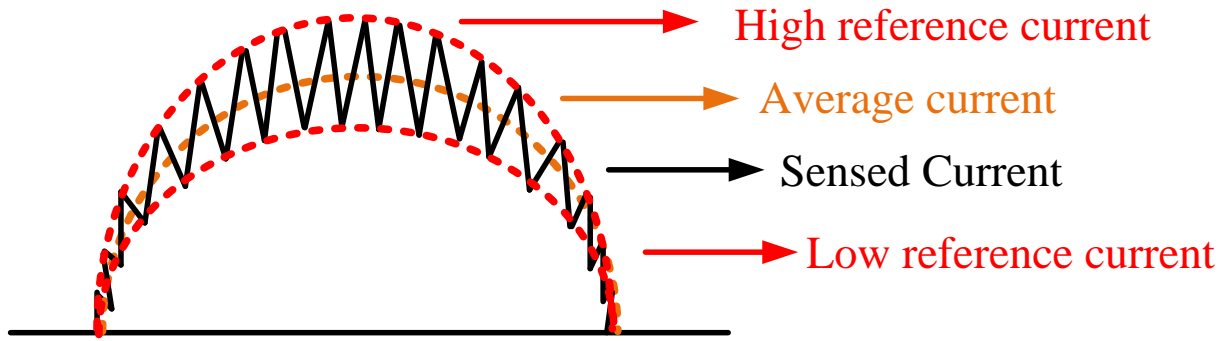
The average current control scheme usually obtains a better input current because the scheme does not require a compensation ramp. Although the inductor current must be sensed and the compensation network is needed, the better performance can be obtained at the near zero-crossing point of the input current.



*Figure 3.2 Average Current Control Scheme.*

- ❖ Hysteresis control scheme

With the hysteresis current control scheme, shown in Figure 3.3, 2 different magnitudes of sinusoidal reference currents are needed. The switch is turned on when the sensed current reaches the lower reference sinusoidal current, and the switch is turned off when the sensed current reaches a higher reference sinusoidal current. This scheme also does not require a compensation ramp. Thus, low distorted input current waveform can be obtained. However, this method has the disadvantage of sensitivity to noise.



*Figure 3.3 Hysteresis Control Scheme.*

According to above comparisons, the average current control technique is adopted to achieve better performance for the input current waveforms.

## 3.2 CONTROLLER DESIGN

### 3.2.1 Controller design overview

The average current mode control is widely used in PFC applications [26, 37]. Compared to the peak current mode control, there is less zero-crossing distortion in the average current mode control. The average current mode control method consists of two-loop compensation: the inner current loop and the outer voltage loop compensation. A simplified diagram of the average current mode scheme when applied to the bridgeless SEPIC PFC converter is shown in Figure 3.4. One of the most powerful average current mode control ICs, TI's UC3854, is used to implement the analog control scheme.

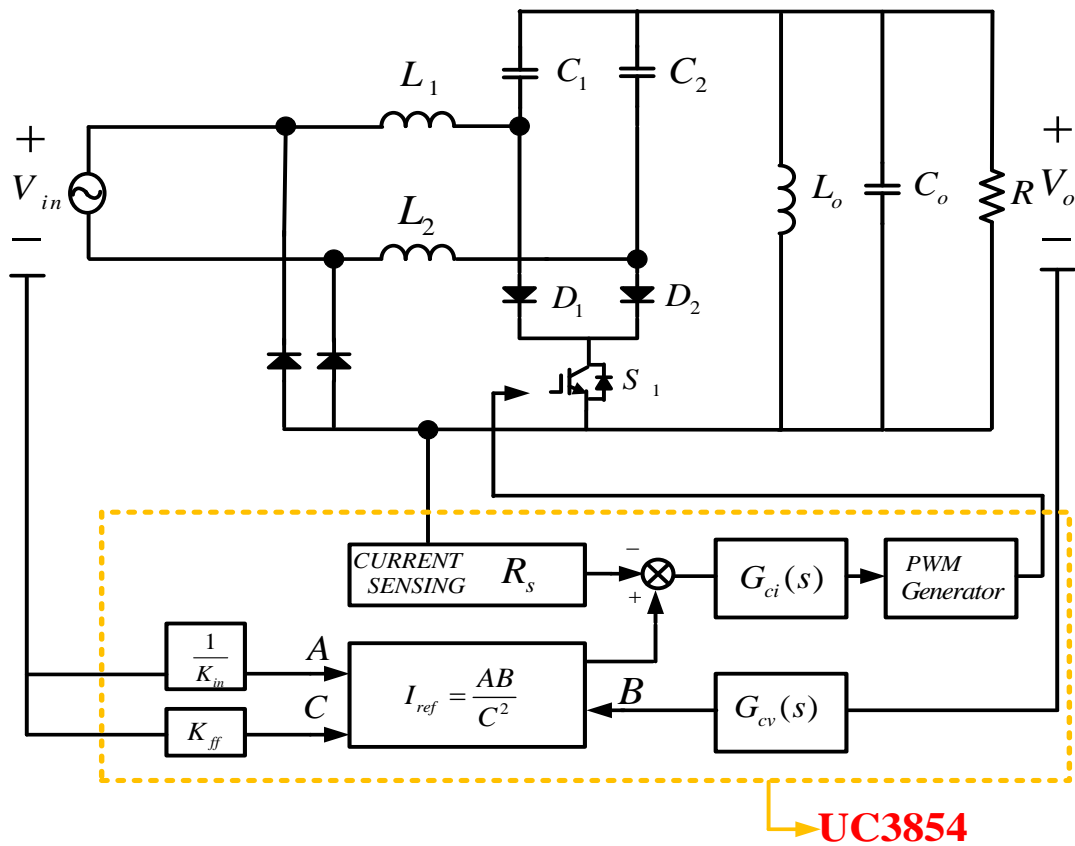
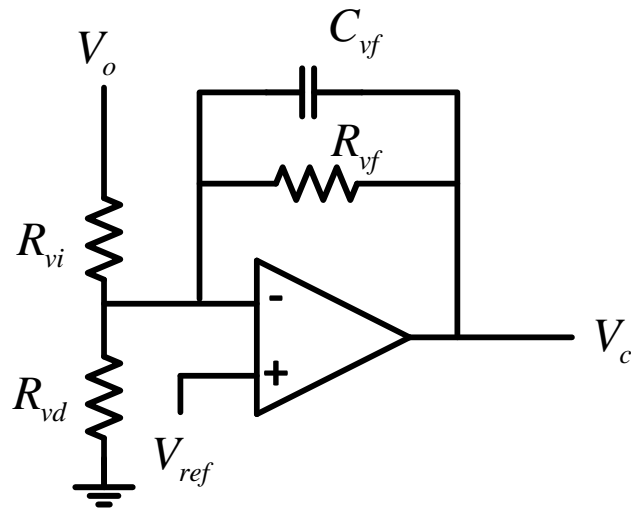


Figure 3.4 Diagram of Average Current Mode Control of SEPIC Converter.

### 3.2.2 Voltage Loop Controller

The bandwidth of the voltage loop compensator should be less than line frequency to prevent an effect of 2<sup>nd</sup> harmonic components of line current, but a bandwidth that is too small yields a poor transient response because of the low crossover frequency. The proper bandwidth needs to be determined by considering 2 effects. A TYPE II compensator, shown in Figure 3.5, a proportional plus single pole compensator [10], is used because it is good for load regulation due its high DC gain. In addition, the minimal phase shift occurs at the crossover frequency. Based on the required bandwidth, the parameters that yield a stable outer voltage loop are determined.



**Figure 3.5 Analog Voltage Error Compensator**

The Type II voltage compensator shown in Figure 3.5 the transfer function follows (Eq. 3.1):

$$G_{cv}(s) = \omega_{iv} \frac{1}{\left(1 + \frac{s}{\omega_{pv}}\right)} \quad (\text{Eq. 3.1})$$

Where,

$$\omega_{iv} = \frac{R_{vf}}{R_{vi}}, \omega_{pv} = \frac{1}{R_{vf} C_{vf}} \quad (\text{Eq. 3.2})$$

With the following voltage compensator parameters:

$$R_{vi} = 56k\Omega, R_{vd} = 10k\Omega, R_{vf} = 56k\Omega, C_{vf} = 100nF$$

The voltage error compensator Bode diagram is shown in Figure 3.6.

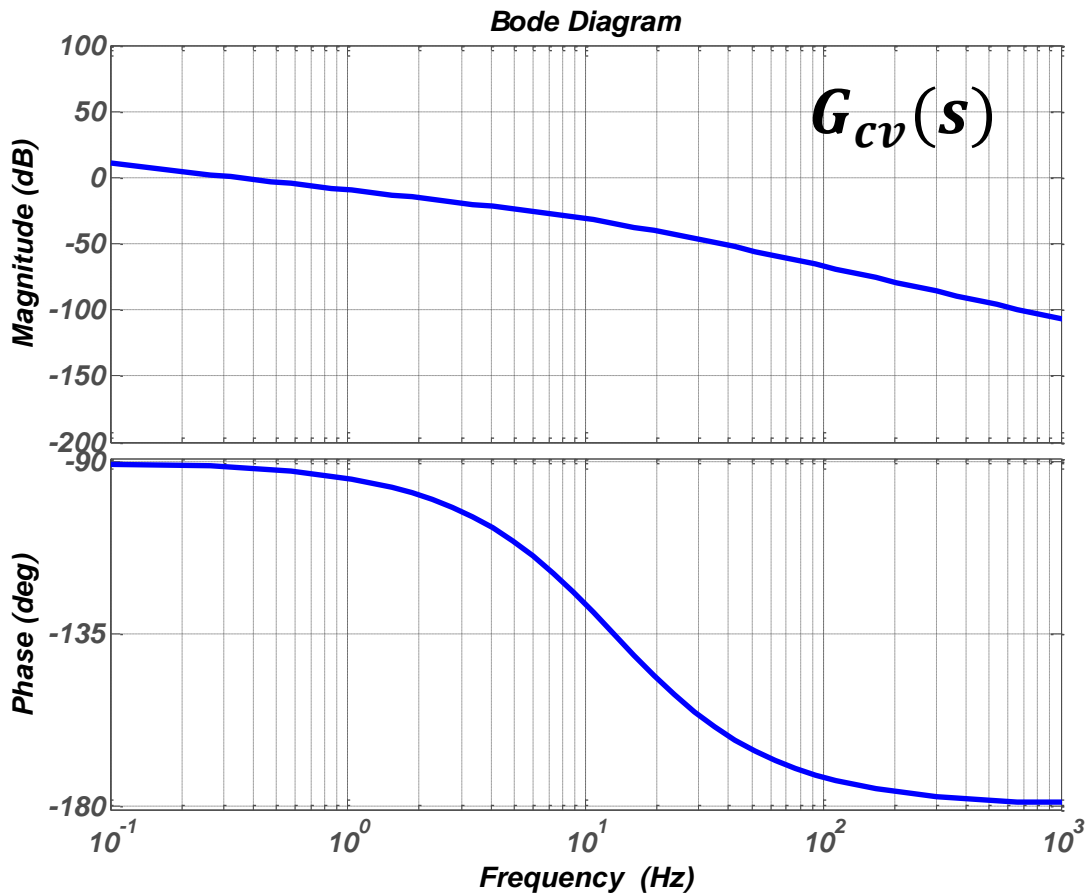


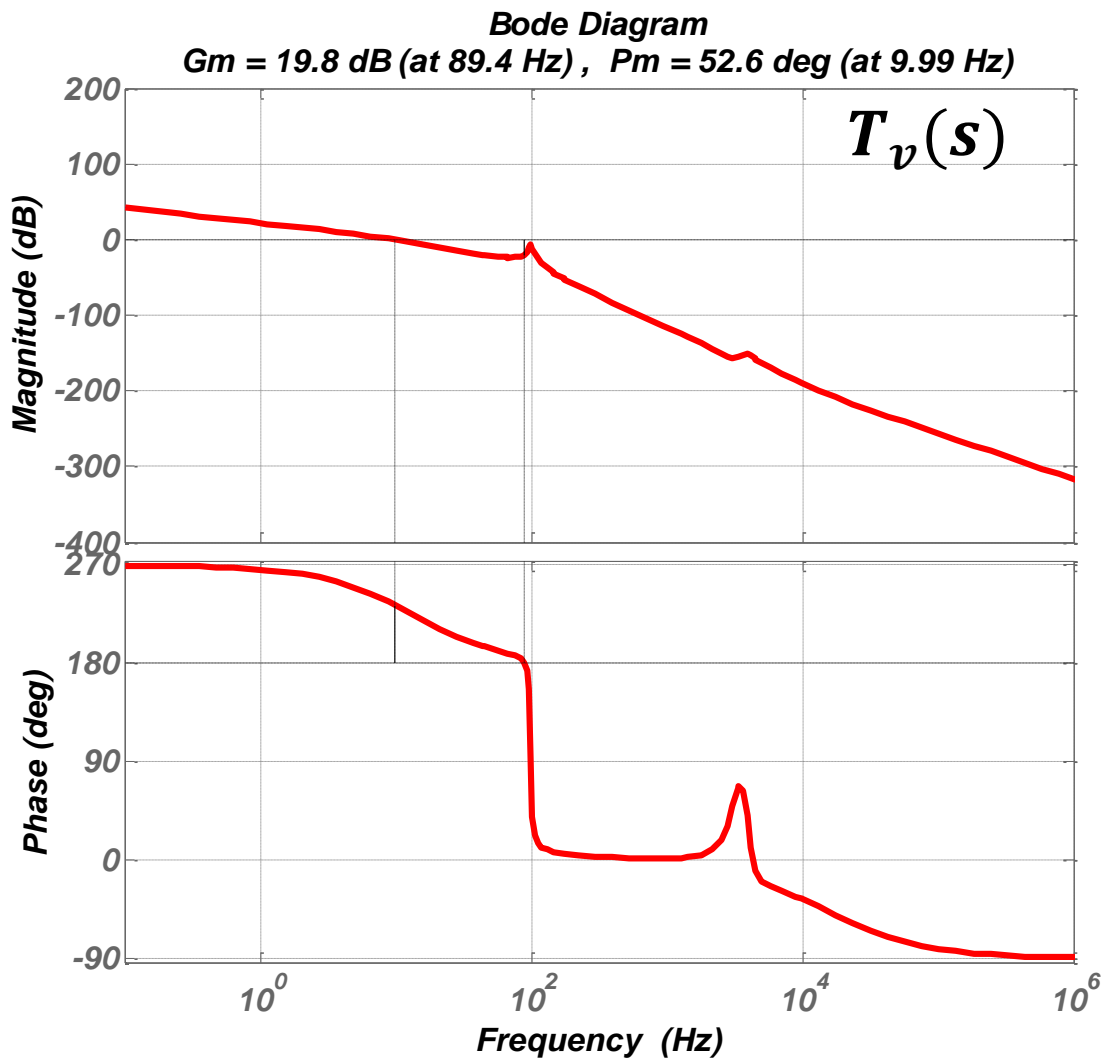
Figure 3.6 Bode diagram of Analog Voltage Error Compensator.



The voltage loop gain is described by (Eq. 3.3), and the Bode diagram of voltage loop gain is shown in Figure 3.7. As shown in the diagram, the cross-over frequency is approximately 10Hz, and the voltage loop gain has 52° of phase margin.

$$T_v = F_{vm} G_{vd}(s) G_{cv}(s) \quad (\text{Eq. 3.3})$$

( $F_{vm}$ : modulation gain)

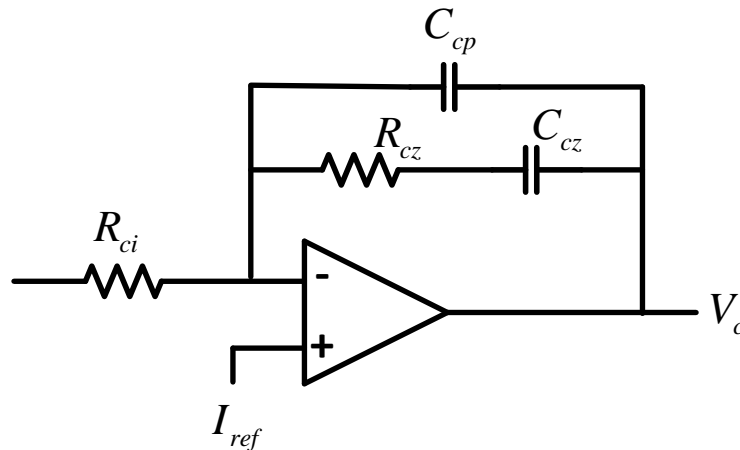


**Figure 3.7 Bode diagram of Analog Voltage Error Compensator Loop Gain.**

### 3.2.3 Current Loop Controller

❖ Feed-back controller

Specifically, the SEPIC converter has difficulty meeting required phase margin with high bandwidth, due to 2 pairs of complex poles. Although the difficulty is reduced by adding damping circuit, the controller needs to be designed with a precise model. Otherwise, the system becomes unstable because the possible bandwidth range is limited. The model, derived in chapter 2.3, is used; the Type II compensator, with two poles and one zero [10] as shown in Figure 3.8, is adopted to provide  $90^\circ$  of phase boost to meet the proper phase margin and stability. Additionally, the gain is determined by considering the bandwidth and the phase margin.



**Figure 3.8 Analog Current Error Compensator**

The Type II current error compensator transfer function is represented by (Eq. 3.4):

$$G_{ci}(s) = \frac{\omega_{ii}}{s} \frac{(1 + \frac{s}{\omega_{zi}})}{(1 + \frac{s}{\omega_{pi}})} \quad (\text{Eq. 3.4})$$

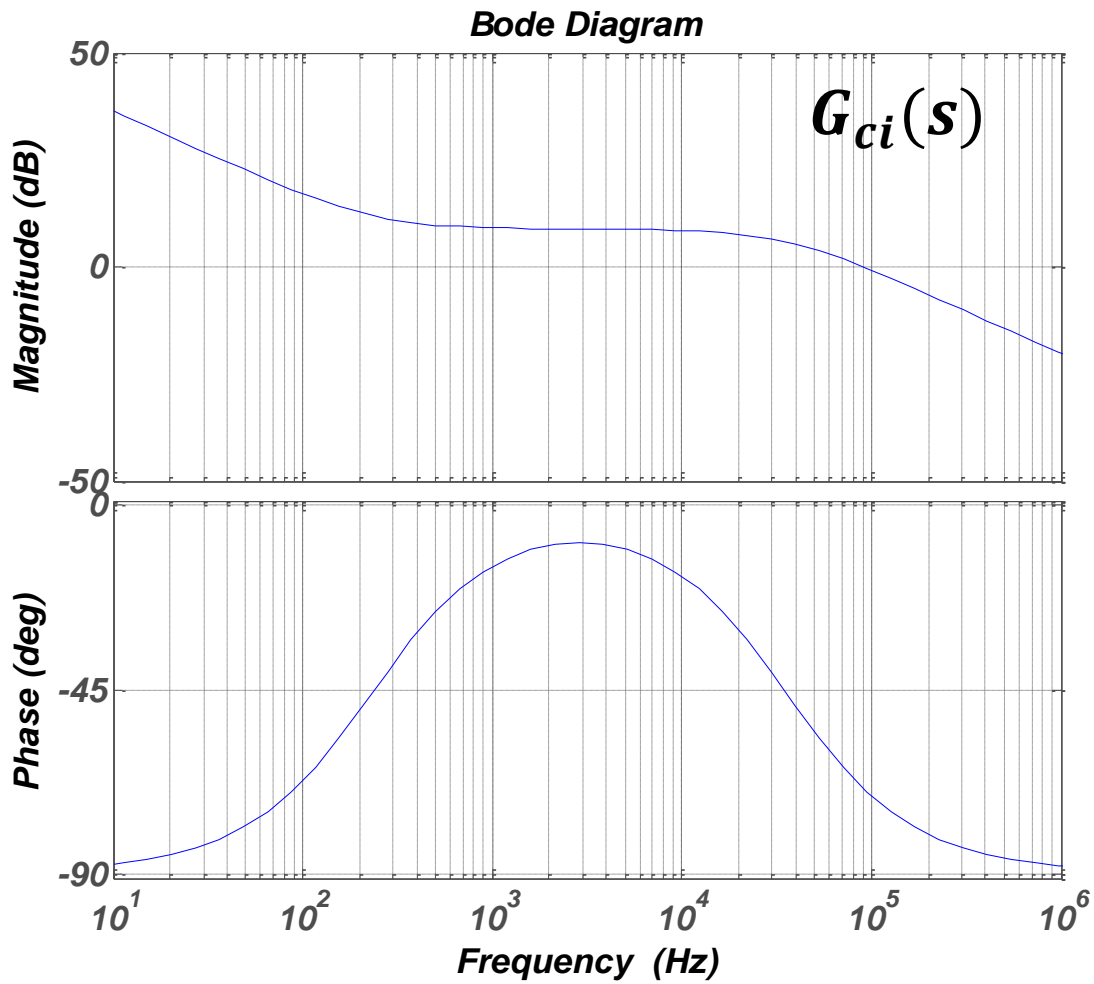
where,

$$\omega_{ii} = \frac{1}{R_{ci}(C_{cp} + C_{cz})}, \quad \omega_{zi} = \frac{1}{R_{cz}C_{cz}}, \quad \omega_{pi} = \frac{C_{cz} + C_{cp}}{R_{cz}C_{cz}C_{cp}} \quad (\text{Eq. 3.5})$$

One pole,  $\omega_p$ , needs to be located above one-half of the switching frequency, to attenuate the high-frequency switching ripple. The integrator and one zero should be determined by considering the desired phase margin and the possible range of cross-over frequencies.

The current error compensator Bode diagram is shown in Figure 3.9, using following current error compensator parameters.

$$R_{ci} = 2k\Omega, \quad R_{cz} = 5.6k\Omega, \quad C_{cz} = 120nF, \quad C_{cp} = 820pF$$



**Figure 3.9 Bode diagram of Analog Current Error Compensator**

As shown in Figure 3.10, the current loop gain is described by (Eq. 3.6). To verify the current loop gain, the sampling gain, the current sense resistor, the fixed ramp gain and the modulation gain also need to be considered, as in (Eq. 3.6). Figure 3.10 presents the small-signal block diagram of the average current mode control. In addition, Figure 3.10 describes the simplified loop gain calculations.

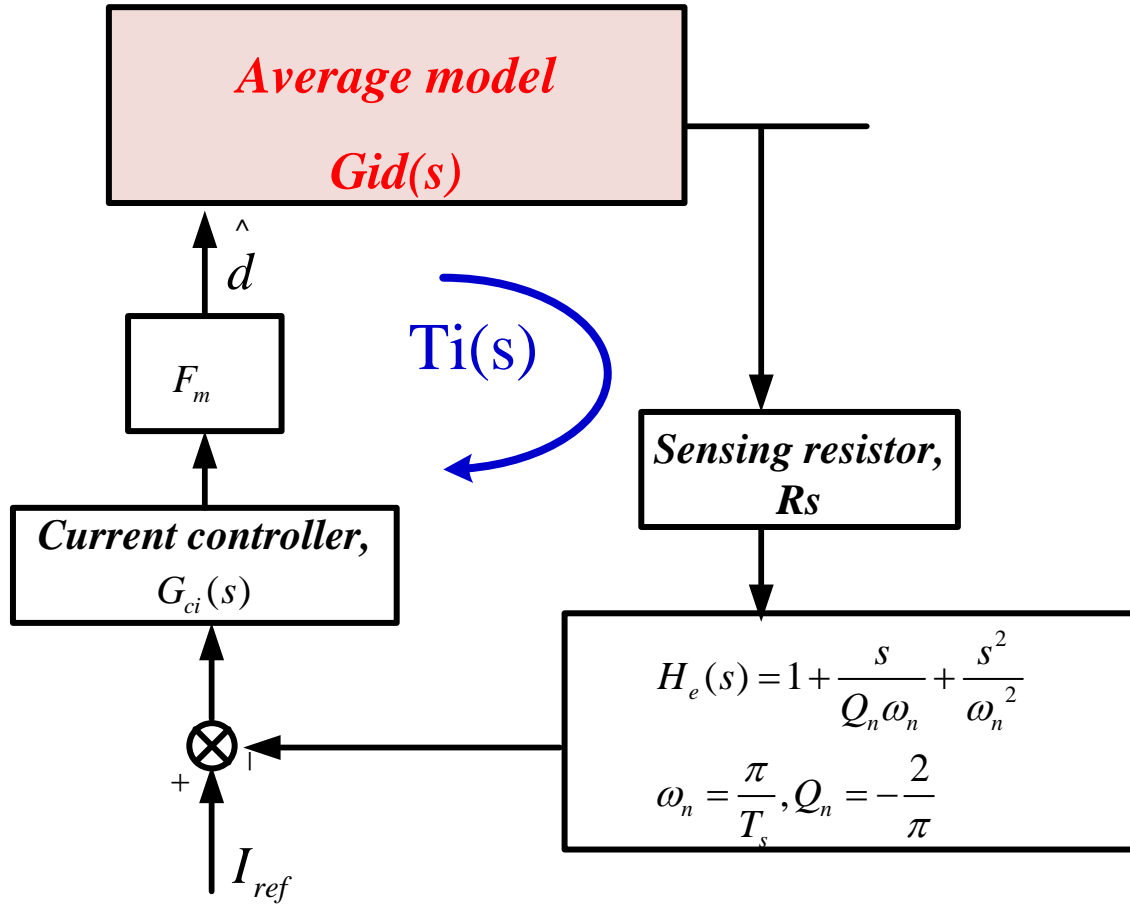


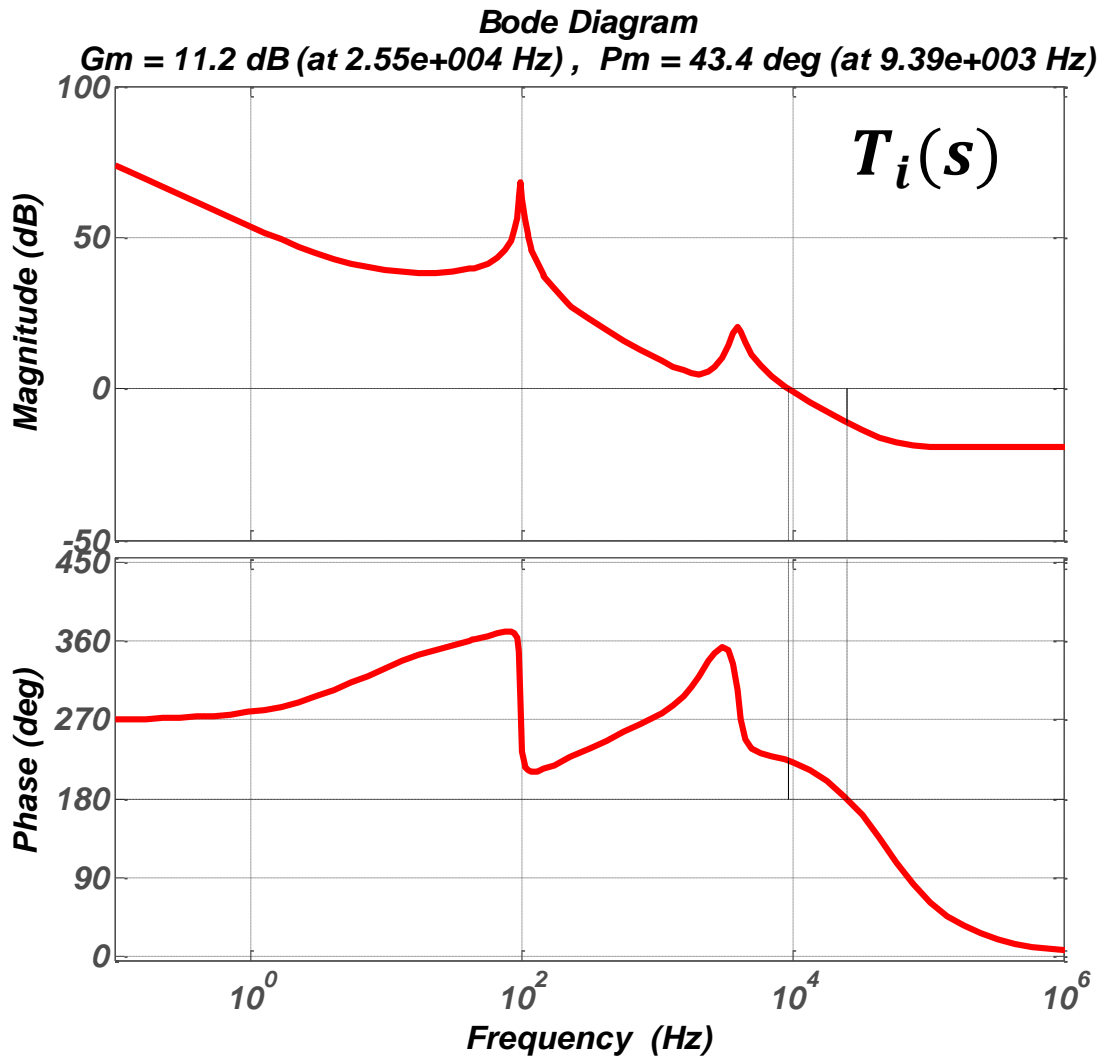
Figure 3.10 Small-signal block diagram of average current mode control.

$$T_i(s) = G_{id}(s) * R_s * H_e(s) * G_{ci}(s) * F_{mi} \quad (\text{Eq. 3.6})$$

( $R_s$ : current sense resistor)

( $H_e(s)$ : sampling gain transfer function)

( $F_{mi}$ : current loop modulation gain)



**Figure 3.11 Bode diagram of Analog Current Error Compensator Loop Gain.**

The bode diagram of current loop gain (which is calculated using (Eq. 3.6)) is shown in Figure 3.11. As shown in the current loop gain diagram, the cross-over frequency is approximately 9.4 kHz and the current loop gain obtains 43° of the phase margin. From the obtained phase margin and bandwidth, the designed controller parameters are verified and the parameters are implemented with simulations and experiments.

### 3.3 SIMULATION RESULTS

#### 3.3.1 Introduction

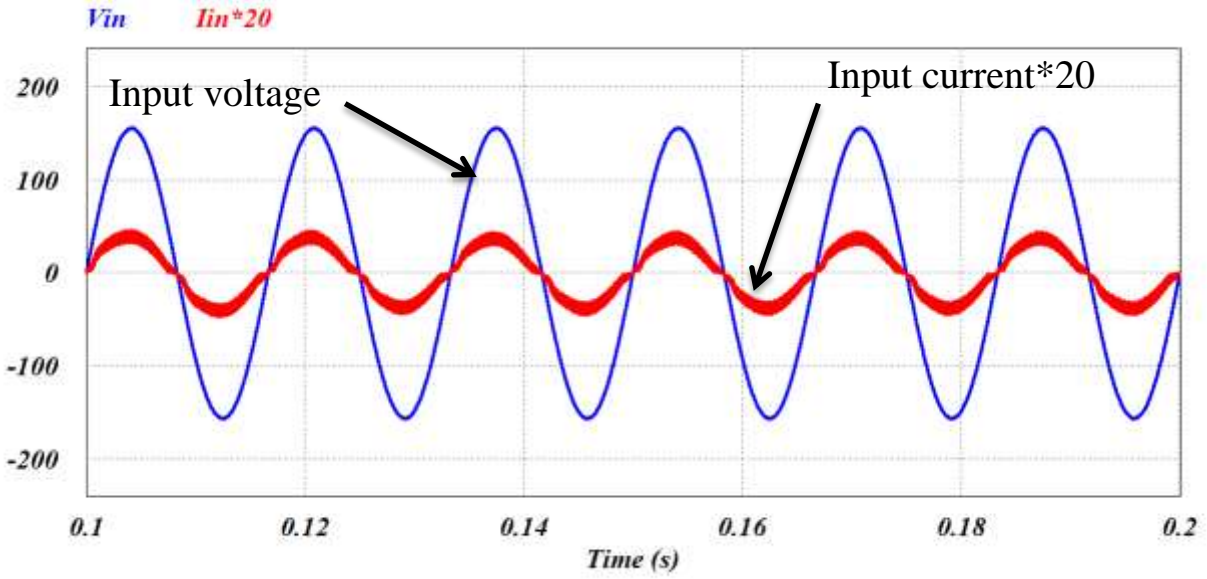
In order to verify the designed analog controller, simulations using simulation software PSIM are performed with verified parameters in chapter 3.2. In this simulation, MOSFETs and diodes are assumed as ideal devices and the other parameters of the power stage are same as design specifications.

#### 3.3.2 Simulation Result with Analog Controller

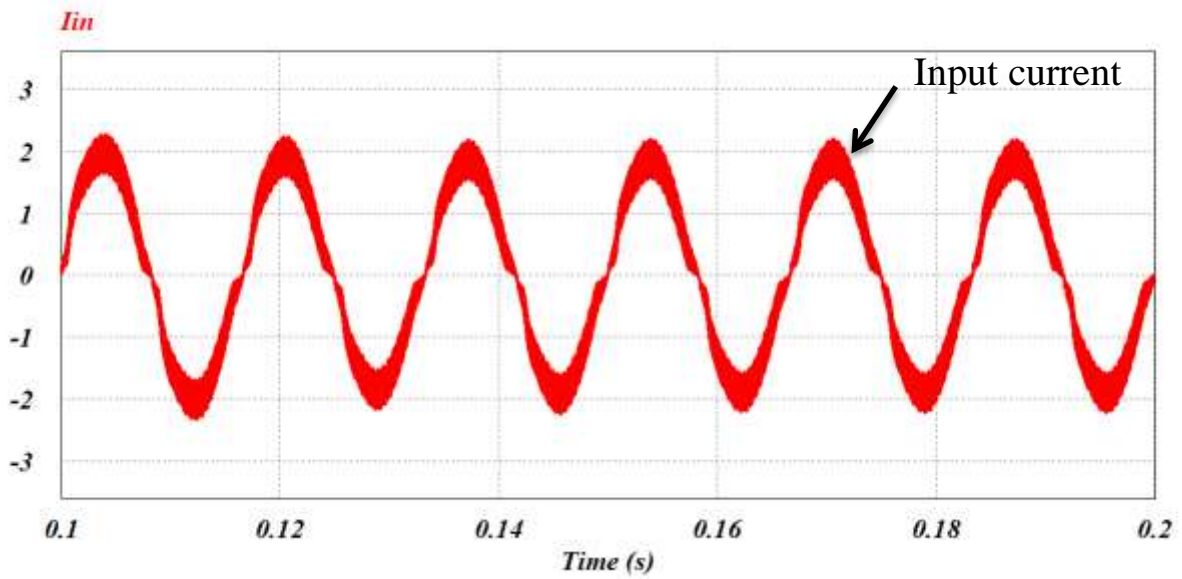
PSIM has a simulation model of the control IC, UC3854, which is used for analog controller implementations. All parameters including control parameters are shown in Table 3.1. As a result of simulation shown in Figure 3.12, a power factor of the simulation result is about 99% and total harmonic distortion is about 11%. This simulation is done with same controller parameters as designed in chapter 3.2. This simulation runs under the full-load condition.

*Table 3.1 List of components parameters of controller*

<i>Feed-Forward parameters</i>					
<b>RFF1</b>	1M $\Omega$	<b>RFF2</b>	100k $\Omega$	<b>RFF3</b>	22k $\Omega$
<b>CFF1</b>	0.1 $\mu$ F	<b>CFF2</b>	1 $\mu$ F		
<i>Input Voltage Sensing</i>					
<b>RVAC1</b>	301k $\Omega$	<b>RVAC2</b>	301k $\Omega$	<b>RB1</b>	121k $\Omega$
<i>Peak Current Limit</i>					
<b>Rpk1</b>	1.8k $\Omega$	<b>Rpk2</b>	9k $\Omega$	<b>Cpk</b>	120pF
<i>Switching Frequency &amp; reference current</i>					
<b>Rmo</b>	2k $\Omega$	<b>CT</b>	1.2nF	<b>Rset</b>	8.2k $\Omega$



*Figure 3.12 Input voltage-Input current Simulation result with Analog Controller*

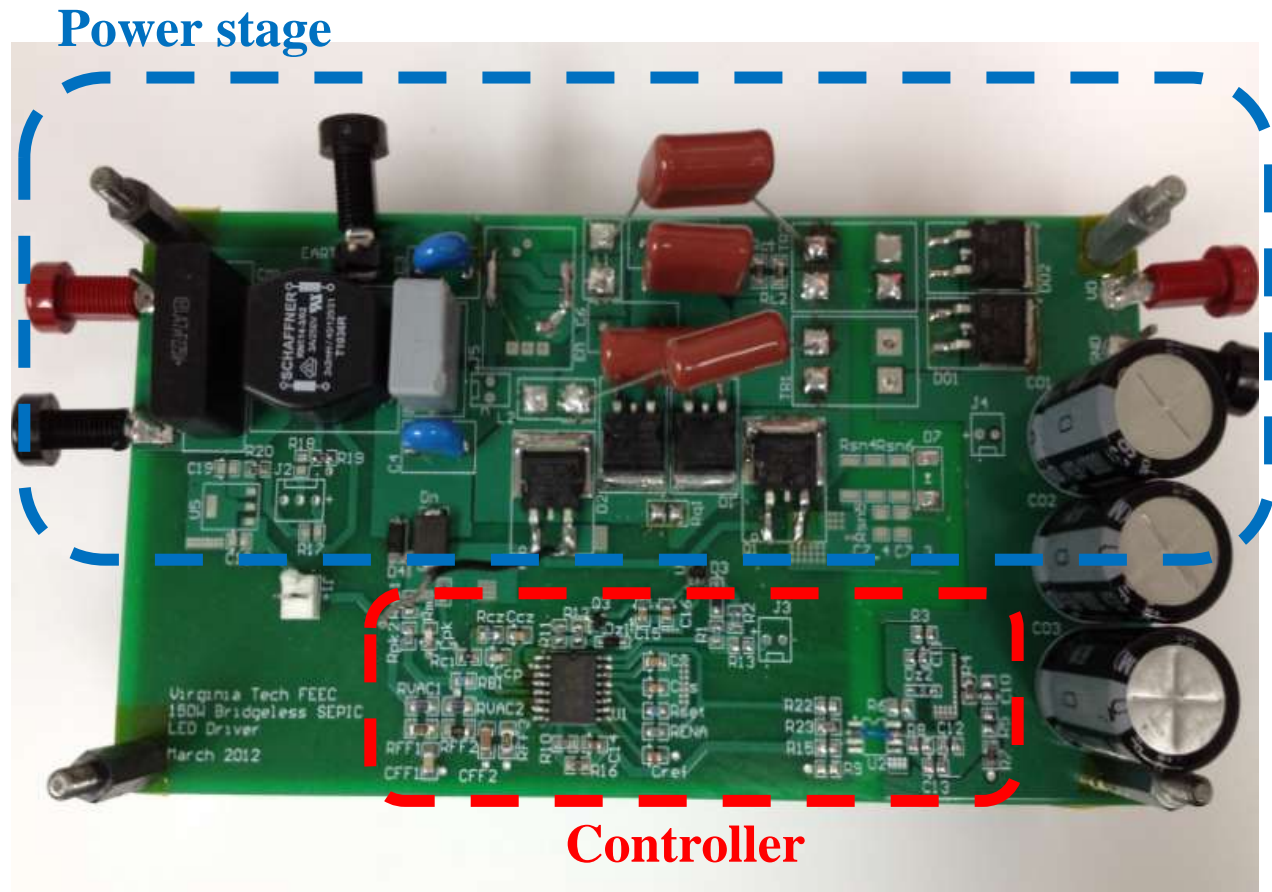


*Figure 3.13 Input Current Simulation result with Analog Controller*



### 3.4 EXPERIMENT TEST SET-UP WITH ANALOG CONTROLLER

The test board of analog controller is shown in Figure 3.14, top side is for the main power stage and bottom side is for controllers. In this thesis, a non-isolated version is tested but this board has various testing options. One of them is the isolated version test. Due to the various options, overall system efficiencies and performances can be compared under differently modified SEPIC converters.



*Figure 3.14 Analog Controller test board picture*

### 3.5 EXPERIMENT RESULTS

With same parameters as in simulations, experiments are performed. Experiment results are shown in Figure 3.15 and Figure 3.16. These experiments are done at  $V_{in\_rms} = 110V @ 60Hz$ . From Figure 3.15, the output voltage is regulated at 50V and the input current is well tracked the input voltage. Under full-load condition, the power factor and the harmonic distortion result could be analyzed from Figure 3.16. Harmonic components are shown in Table 3.2 and summarized PF and THD results are:

- Power Factor (PF): 0.9977
- Total Input Current Harmonic Distortion: 8.8%

*Table 3.2 Harmonic components of analog controller experiment result*

Harmonic (Frequency, Hz)	Fundamental (60)	3 (180)	5 (300)	7 (420)	9 (540)	11 (660)	13 (780)
A (%)	1.448A (100)	0.067A (4.6)	0.097A (6.7)	0.044A (3.0)	0.009A (0.6)	0.008A (0.54)	0.004A (0.29)

❖ Analog controller experiment waveforms

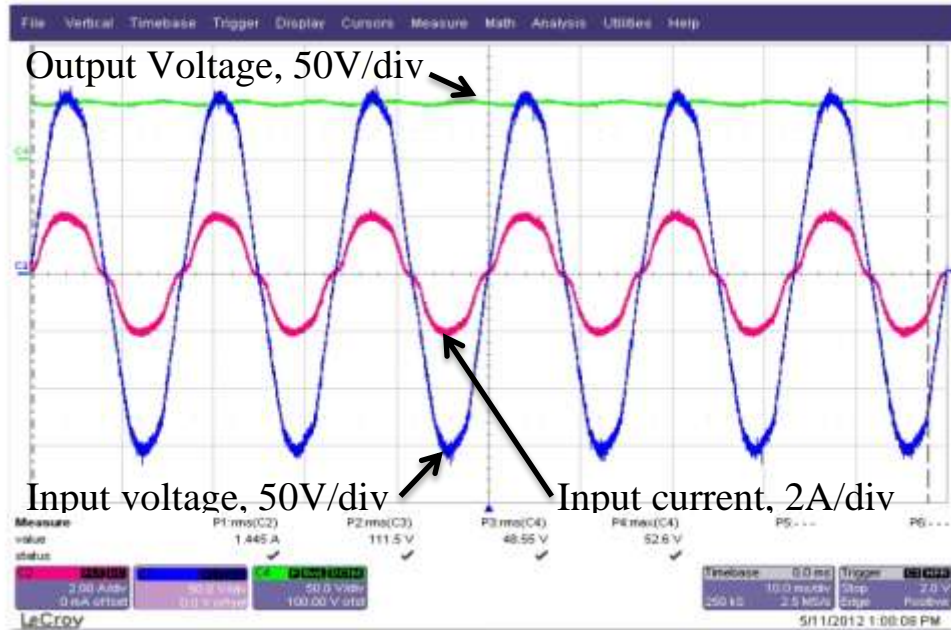


Figure 3.15 Analog Controller Experiment Result waveform 1

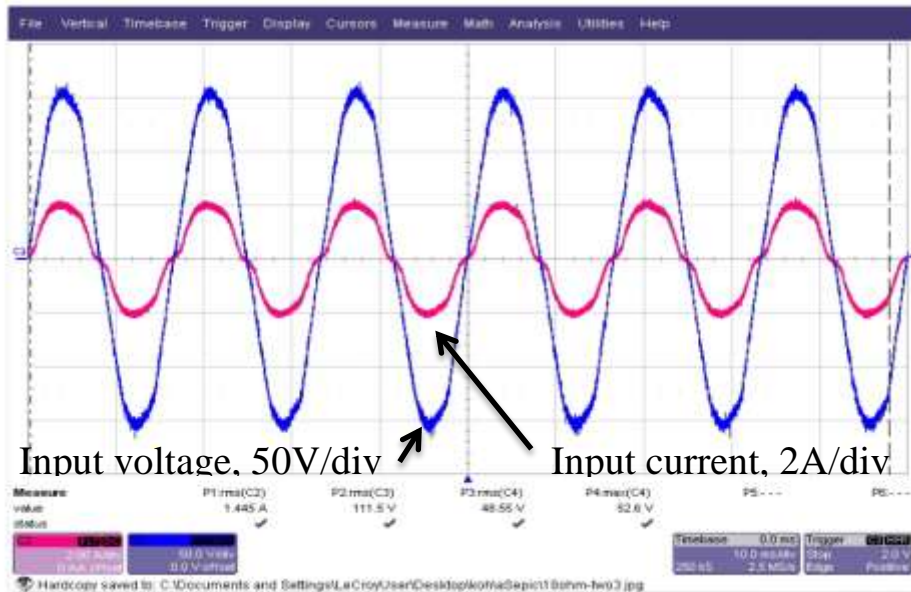
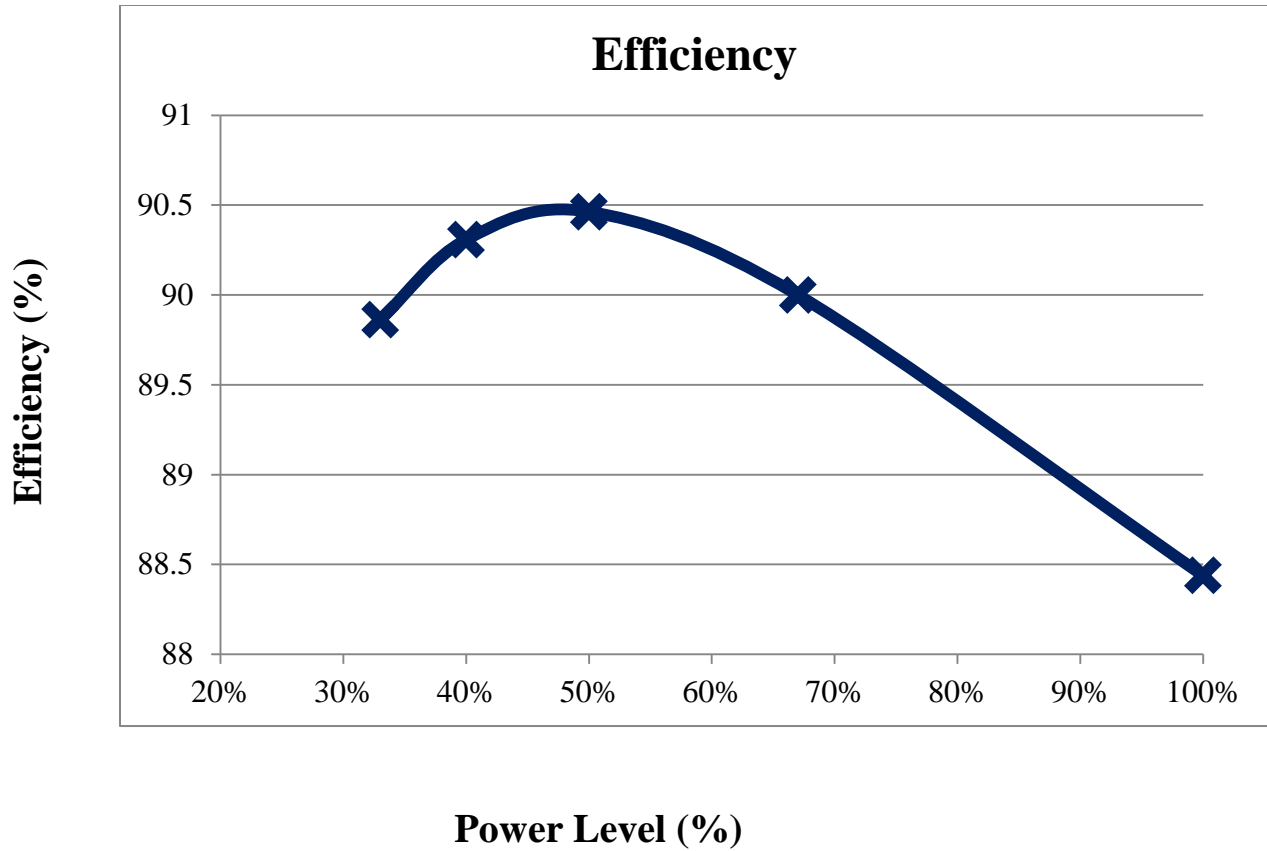


Figure 3.16 Analog Controller Experiment Result 2

❖ Measured efficiency

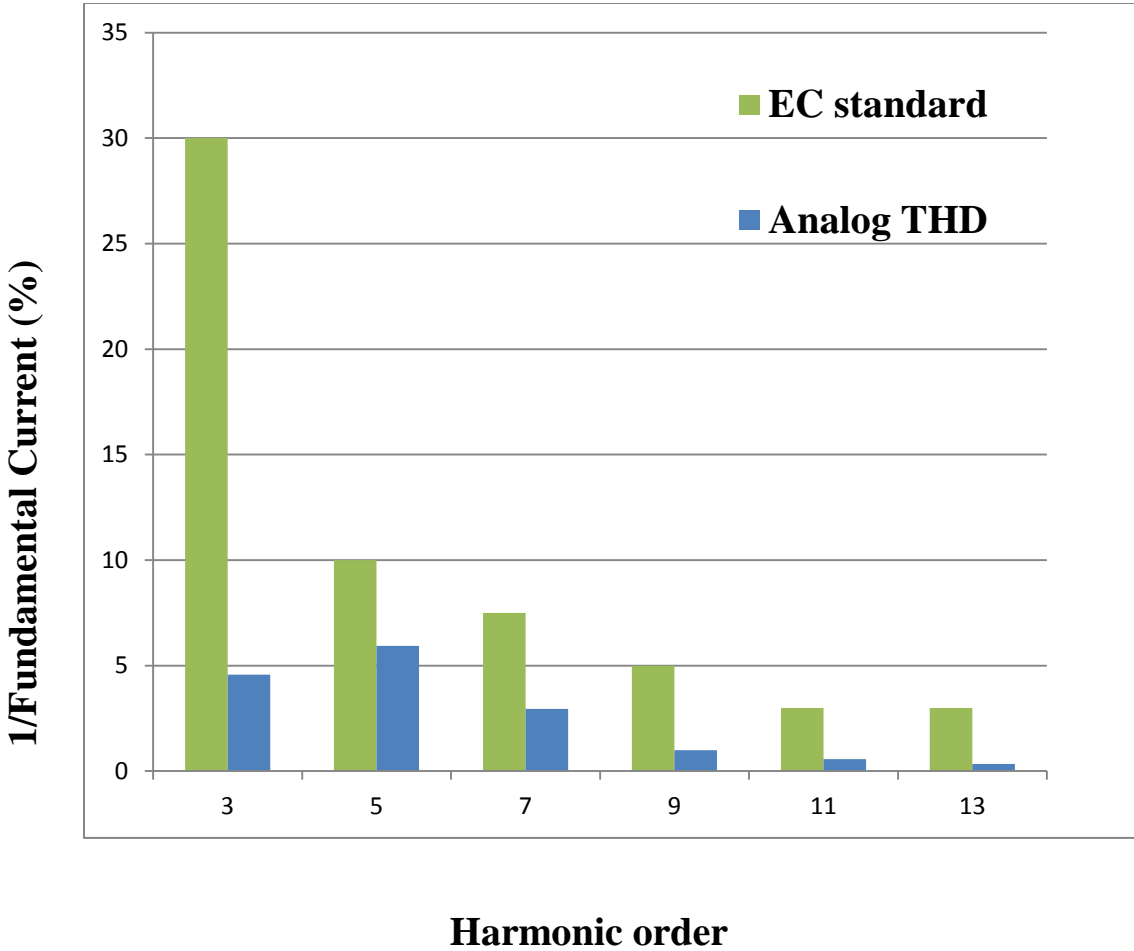
The measured efficiency under various load conditions is shown in Figure 3.17. Optimizing devices and parameters need to be done to make higher efficiency system because the overall efficiency seems lower than most of literatures [2, 12].



*Figure 3.17 Efficiency with analog controller implementation*

❖ Measured THD

The measured THD under the full-load condition is shown in Figure 3.18. Figure 3.18 compares between the measured THD and the EC 61000-3-2 Class C standard. The EC 61000-3-2 is an international standard for lighting equipment. As shown in Figure 3.18, the THD with analog controllers meets the standard.



*Figure 3.18 THD comparison with analog controller implementation*

## **4 DIGITAL CONTROLLER DESIGN AND VERIFICATIONS**

### **4.1 CONTROLLER DESIGN OVERVIEW**

Digital control has become a popular method in power electronics, and many of recent studies [29-38] are developing control algorithms using DSP. Despite the popularity of digital control, topologies for the digitally controlled PFC converter are not varied. Most of the studies in this area [12, 29, 30] that discuss digital control for PFC circuits deal with the Boost PFC converter because of its simple implementation. On the contrary, this chapter, the digitally controlled SEPIC PFC converter will be discussed.

Due to the complexity of the circuit and its control aspect, the SEPIC topology has a high sensitivity to parameter variations. This sensitivity results in difficulties designing a controller that satisfies stabilities under the various load conditions. However, with a digital controller implementation, this difficulty can be resolved.

This chapter will describe the procedure of digital controller designs and will show the results its implementations. One of the powerful digital signal processors (DSP), TMS320F28335, is used to implement the digital control algorithms due the processor's fast speed matches switching frequency of the converter. Two loop control, feed-back control and current feed-forward compensation, is implemented. In addition, phase locked loop (PLL) algorithm is implemented to generate pure sinusoidal reference current. Figure 4.1 shows the overall block diagram of digitally controlled bridgeless SEPIC PFC converter.

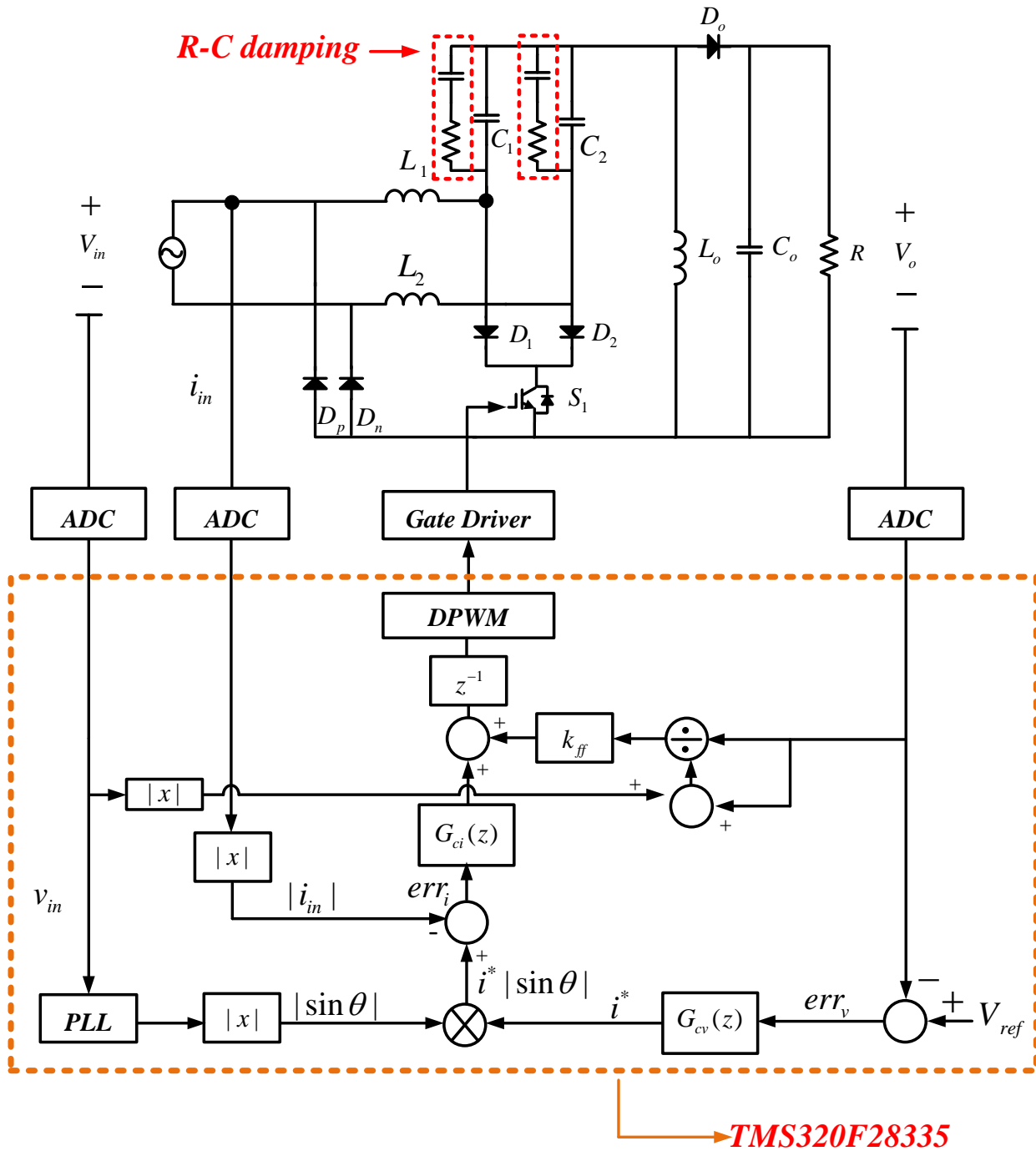


Figure 4.1 Digital controlled overall system diagram of SEPIC PFC Converter

## 4.2 Z-DOMAIN SYSTEM MODELING

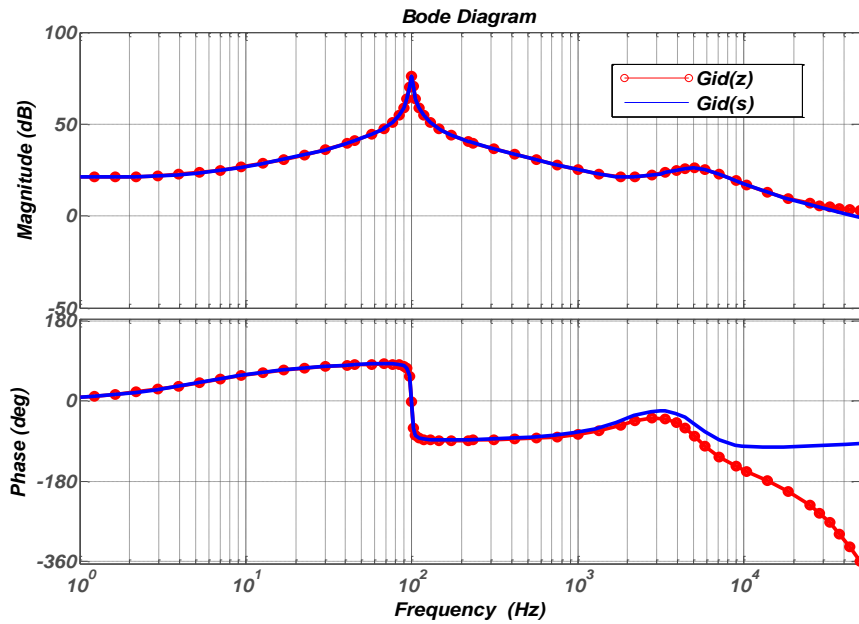
To design the z-domain controller, the z-domain system transfer functions should be obtained. Software, MATLAB, is used to convert the model from s-domain to z-domain. The ZOH method is used to convert s-domain models into z-domain models. The numerical expressions of the converted control-to-inductor model and control-to-output model are described by (Eq. 4.1 – 4.2). The zero-order-hold (ZOH) effect and a digital computation [28, 30] delay are applied to conversions. The damping circuit parameters are included in both transfer functions. In addition, the sampling frequency is selected as 100 kHz.



❖ Z-domain control-to-inductor model

Figure 4.2 shows the comparison of control-to-inductor model's small-signal responses between the s-domain model and the z-domain model. The s-domain model is obtained in (Eq. 2.29) and the z-domain model is obtained in (Eq. 4.1). As shown in Figure 4.2, z-domain system has a phase drop due to the ZOH and computation times [13]. Thus, the achievable bandwidth of the z-domain system will be reduced compared to s-domain system.

$$G_{id}(z) = \frac{3.25z^4 - 10.78z^3 + 13.19z^2 - 7.0z + 1.34}{z^6 - 4.45z^5 + 7.95z^4 - 7.16z^3 + 3.25z^2 - 0.59z} \quad (\text{Eq. 4.1})$$

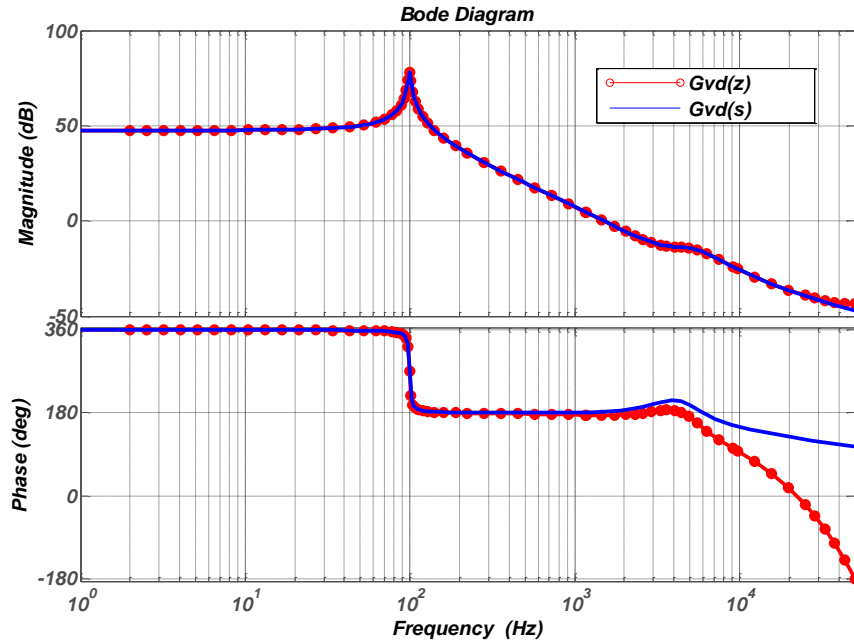


*Figure 4.2 Comparison of the S-domain model and the Z-domain model*

❖ Z-domain control-to-output model

Figure 4.3 shows the comparison of control-to-output model's small-signal responses between the s-domain model and z-domain model. The s-domain model is achieved by (Eq. 2.31) and the z-domain model is derived by (Eq. 4.2).

$$G_{vd}(z) = \frac{-0.0062z^4 + 0.036z^3 - 0.0639z^2 + 0.0457z - 0.0116}{z^6 - 4.45z^5 + 7.95z^4 - 7.16z^3 + 3.25z^2 - 0.594z} \quad (\text{Eq. 4.2})$$



*Figure 4.3 Comparison of the S-domain model and the Z-domain model*

## 4.3 DIGITAL CONTROLLER DESIGN

### 4.3.1 Voltage Loop Controller

As discussed in chapter 3.2.2 for the analog voltage controller design, the voltage control loop should have a much lower bandwidth compared to the line frequency, to minimize the input current distortion and to decrease the effect of the 2<sup>nd</sup> harmonic of the input current. The simple PI compensator, with single pole and single zero compensator, is used because it is good for load regulations, due to its high DC gain.

The z-domain transfer function of the PI voltage compensator is described by (Eq. 4.3):

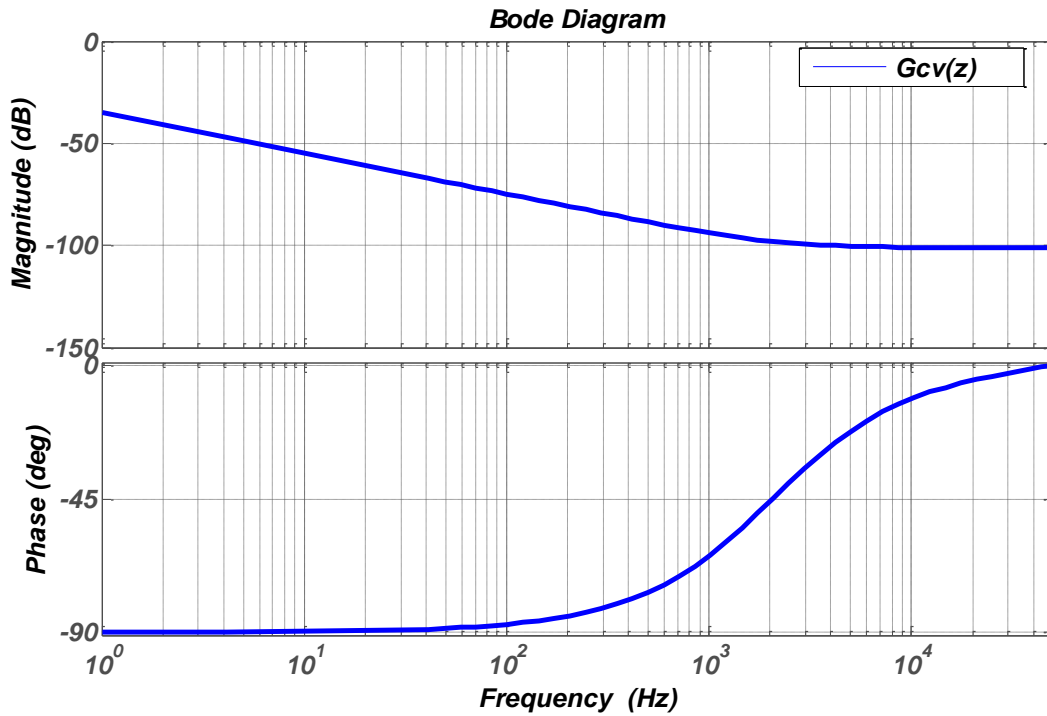
$$G_{cv}(z) = K_{pv} + \frac{K_{iv}T_s}{z-1} \quad (\text{Eq. 4.3})$$

The controller gains are determined by considering required bandwidth of the control loop using the SISO design tool and the small-signal response. The bandwidth of the voltage loop should be much lower than the inner current loop bandwidth. The numerical expression of voltage compensator is shown by the following formula:

$$G_{cv}(z) = (9.43e-6) + \frac{(1.15e-6)}{z-1} \quad (\text{Eq. 4.4})$$

where, the control gains are:

$$K_{pv} = 9.43e-6, K_{iv}T_s = 1.15e-6$$



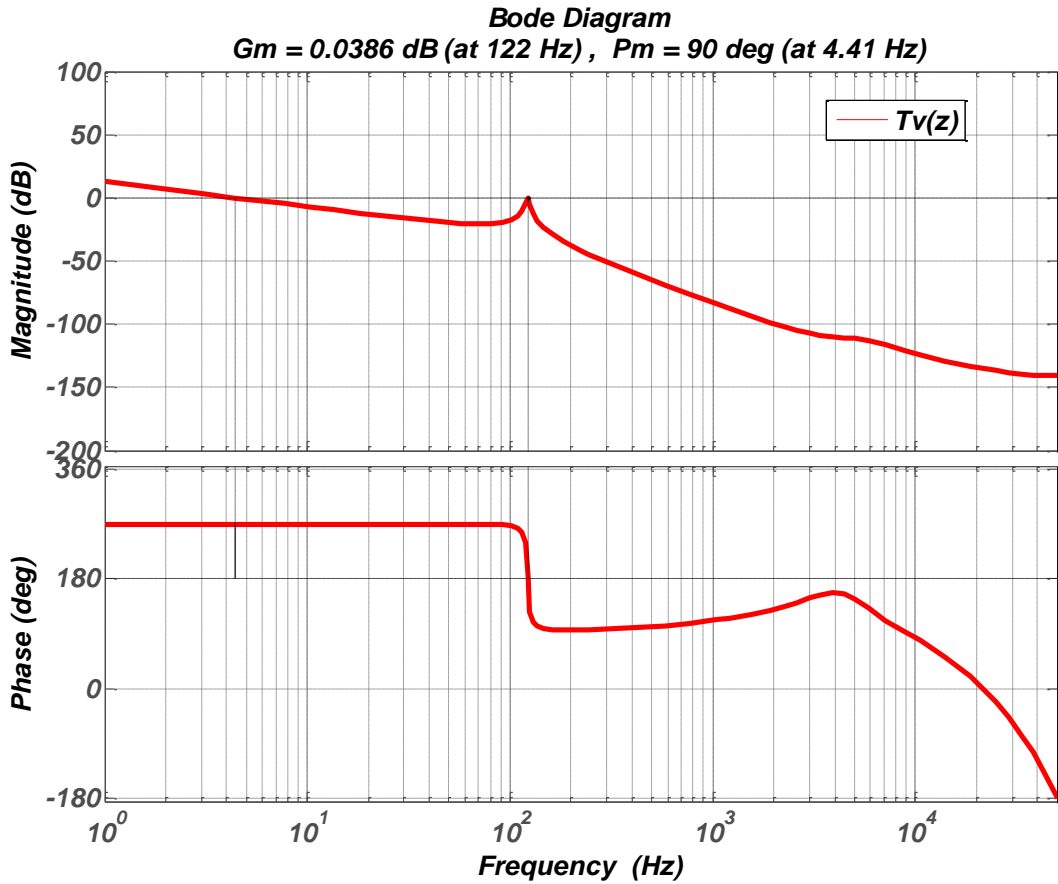
*Figure 4.4 Bode diagram of voltage error compensator in z-domain*

The bode diagram of the voltage error compensator in the z-domain is shown in Figure 4.4.

With a proper damping circuit, the simple PI controller can work as a voltage loop controller.

The voltage loop gain is described by (Eq. 4.5), and the Bode diagram of the voltage loop gain is shown in Figure 4.5. As shown in the voltage loop gain diagram, the cross-over frequency is approximately 4.4Hz and the voltage loop gain gets 90° of a phase margin.

$$T_v(z) = G_{vd}(z) \cdot G_{cv}(z) \quad (\text{Eq. 4.5})$$

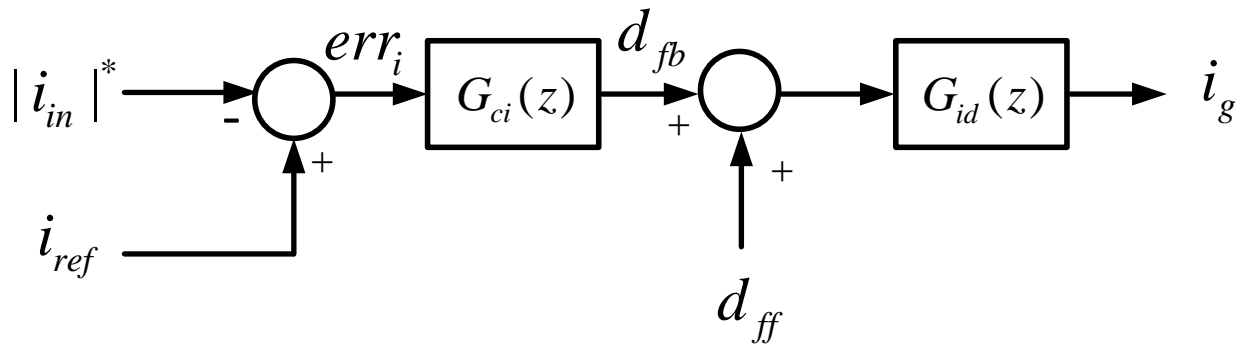


*Figure 4.5 Bode diagram of voltage loop gain in z-domain*

### 4.3.2 Current Loop Controller

As discussed in chapter 3.2, the SEPIC converter has difficulties meeting the proper phase margin with enough bandwidth because it has 2 pairs of complex poles and a complex circuit topology. Moreover, in digital controls, there is a phase drop due to the zero-order-hold (ZOH) effect of digital controls and the computation delay as shown in Figure 4.1. The ZOH effect and digital computation delays are applied into the model, which is derived in chapter 2.3 and (Eq. 3.7).

The PI controller, single pole and single zero, is adopted to provide a proper phase margin and stability. In addition, the gains are determined by considering the bandwidth and the phase margin. The SISO design tool is used to design a suitable current loop controller, and the verification is performed according to the small-signal response and the simulation results. Figure 4.6 shows a block diagram of the current control loop. As shown in Figure 4.6, there is a feed-back control and feed-forward control. The specific design procedure of current loop controllers will be discussed in 2parts: the first part is about the feed-back controller design and the second part is a about the feed-forward compensator design.



**Figure 4.6 Block diagram of current control loop**

❖ Feed-back controller design

With the proper damping circuit, a simple PI controller should be enough as a current feed-back controller. The precise control-to-inductor model in z-domain is necessary. The PI current error compensator transfer function is (Eq. 4.6).

$$G_{ci}(z) = K_{pi} + \frac{K_{ii}Ts}{z-1} \quad (\text{Eq. 4.6})$$

Following current compensator parameters are decided with considering small-signal responses and results from the SISO design tool.

$$K_{pi} = 0.05, K_{ii_{Ts}} = 0.01$$

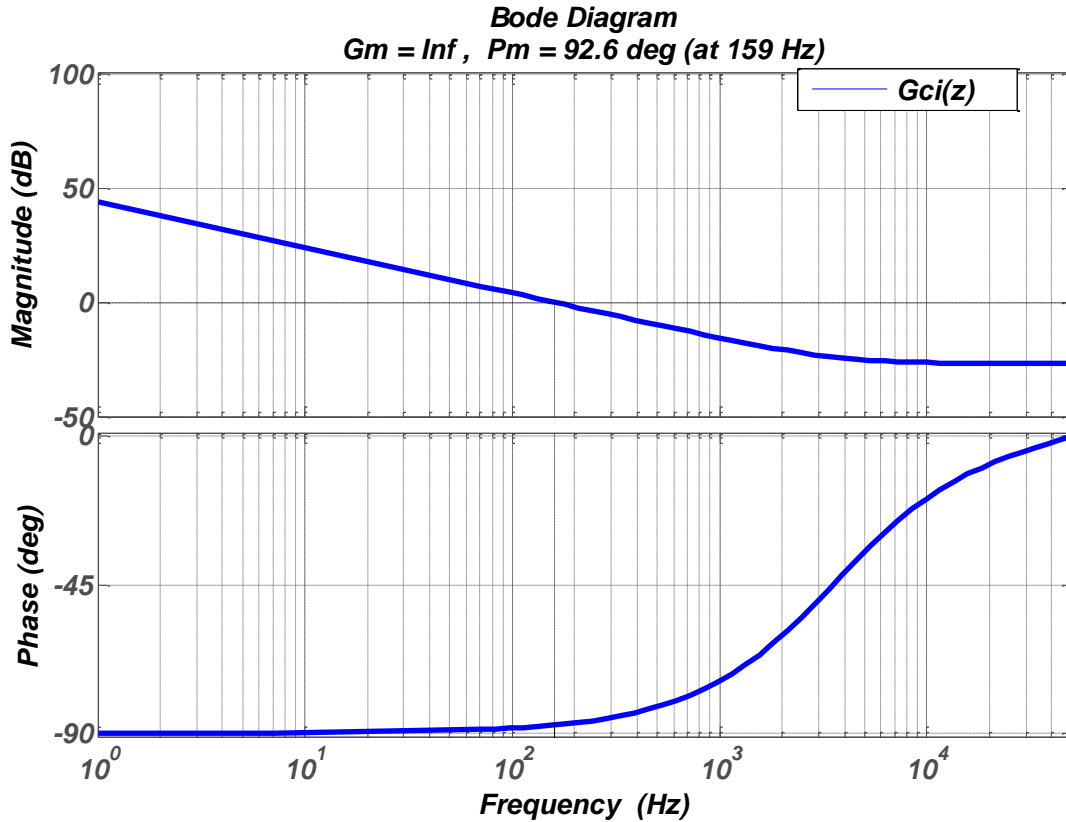
The bode diagram of the z-domain current error compensator is shown in Figure 4.7

From the Figure 4.6, the feed-back current loop gain could be described in (Eq. 4.7). To verify the current loop gain, the ZOH and digital computation delay effect is already applied into the z-domain system transfer function  $G_{id}(z)$ .

$$T_i(z) = G_{id}(z) * G_{ci}(z) \quad (\text{Eq. 4.7})$$

( $G_{id}(z)$ ): z-domain system transfer function)

( $G_{ci}(z)$ ): z-domain current compensator)

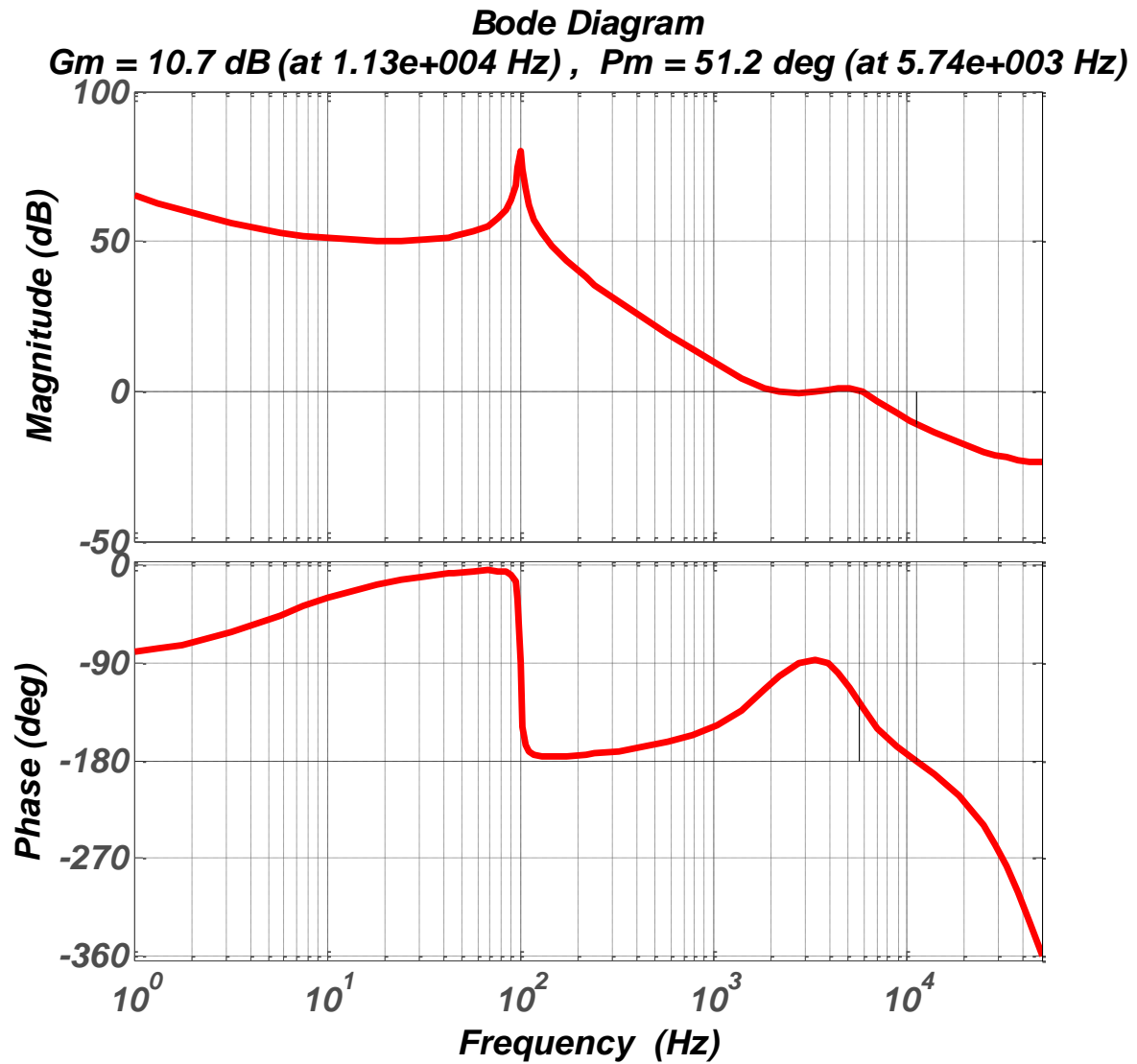


*Figure 4.7 Bode diagram of current error compensator in z-domain*

With the determined controller parameters and system component parameters, the numerical expression of the total current loop gain is expressed in (Eq. 4.8). MATLAB is used to obtain a numerical expression of the loop gain transfer function.

$$T_i(z) = \frac{0.162z^5 - 0.67z^4 + 1.1z^3 - 0.88z^2 + 0.35z - 0.054}{z^7 - 5.45z^6 + 12.4z^5 - 15.12z^4 + 10.41z^3 - 3.84z^2 + 0.594z} \quad (\text{Eq. 4.8})$$





*Figure 4.8 Digital Current Loop Gain Bode Diagram*

The Bode diagram of the current loop gain is shown in Figure 4.8. As shown in the current loop gain diagram, the cross-over frequency is approximately 5.74 kHz and the current loop gain has 51° of phase margin. From the obtained phase margin and the cross-over frequency, designed controller parameters can be implemented with simulations and experiments.

❖ Feed-forward compensator

As shown in Figure 4.6, the current feed-forward compensation is adopted to decrease input current harmonic distortions. In the most of PFC circuits which are based on a boost topology, the feed-forward term is decided as  $d_{ff\_boost} = \frac{|v_{in}|}{v_o}$ ; however, the output of SEPIC converters is higher than the input voltage. That is why the conventional feed-forward term cannot be implemented with SEPIC converters, otherwise the feed-forward term should have cases which is higher than 1. In this chapter, a feed-forward term derivation for SEPIC converters will be explained [8, 15].

The Inductor  $L_1$  current response can be derived from chapter 2. It is described in (Eq. 4.9) for the switch S1 on-time and (Eq. 4.10) for the switch S1 off-time.

$$L_1 \frac{di_{L1}}{dt} = |v_{in}| \quad (\text{Eq. 4.9})$$

$$L_1 \frac{di_{L1}}{dt} = |v_{in}| - v_{C1} - v_o \quad (\text{Eq. 4.10})$$

By averaging of input current responses through the on-time and the off-time as (Eq. 4.11),

$$d \frac{d\tilde{i}_{L1}}{dt} = |v_{in}| - \int_{dT_s}^{T_s} (v_{C1}(t) + v_o(t)) dt = |v_{in}| - (1 - d_{ff})(v_{C1} + v_o) \quad (\text{Eq. 4.11})$$

From (Eq. 4.11), the feed-forward term for SEPIC converters can be defined in (Eq. 4.12)

$$d_{ff} = \frac{v_o}{|v_{in}| + v_o} \quad (\text{Eq. 4.12})$$

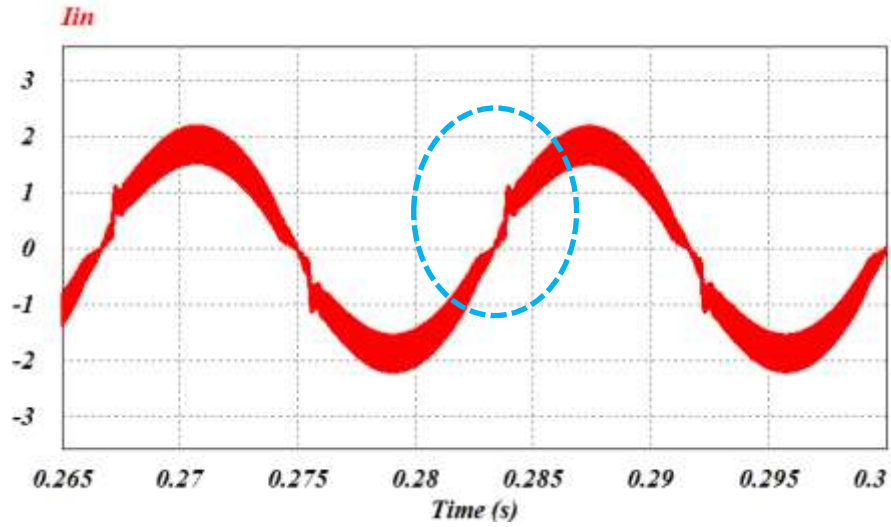
## 4.4 SIMULATION RESULTS

### 4.4.1 Simulation Result with Digital Controller

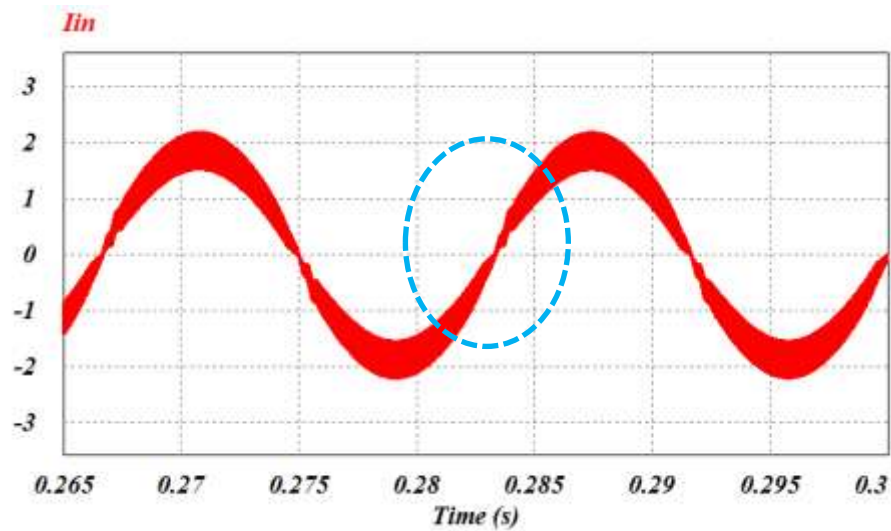
In order to verify the effect of digital controller designs, simulations using software PSIM are performed. Simulation parameters for main components of the power stage are same as the analog controlled circuit except the energy transfer capacitor C1. The C1 is modified from 1 $\mu$ F to 0.47 $\mu$ F. This modification is adopted to maximize a possible range of cross-over frequency. This reason is because of that C1 and L1 parameters are related to a resonance frequency and bandwidth. The digital PI block is implemented for the both of a voltage control loop and a current control loop. From the Figure 4.9 and the figure 4.10, the feed-forward compensation effect can be compared. Figure 4.9 shows the result with only a feed-back controller, and the input current is distorted near zero-crossing. Figure 4.10 presents the result with a feed-back controller and feed-forward compensator. In this simulation, the feed-forward term which is derived in chapter 4.3.2 is implemented. As shown in Figure 4.10, with the feed-forward compensator, the control gain can be increased without any control parameter changes. The effect of feed-forward compensator is also observed in Table 4.3, the comparison of PF and THD between 2 cases.

*Table 4.1 Feed-Forward effect comparison*

	<b>Without Feed-Forward</b>	<b>With Feed-Forward</b>
<b>PF</b>	98.43 %	99.18 %
<b>THD</b>	13.22 %	11.95 %



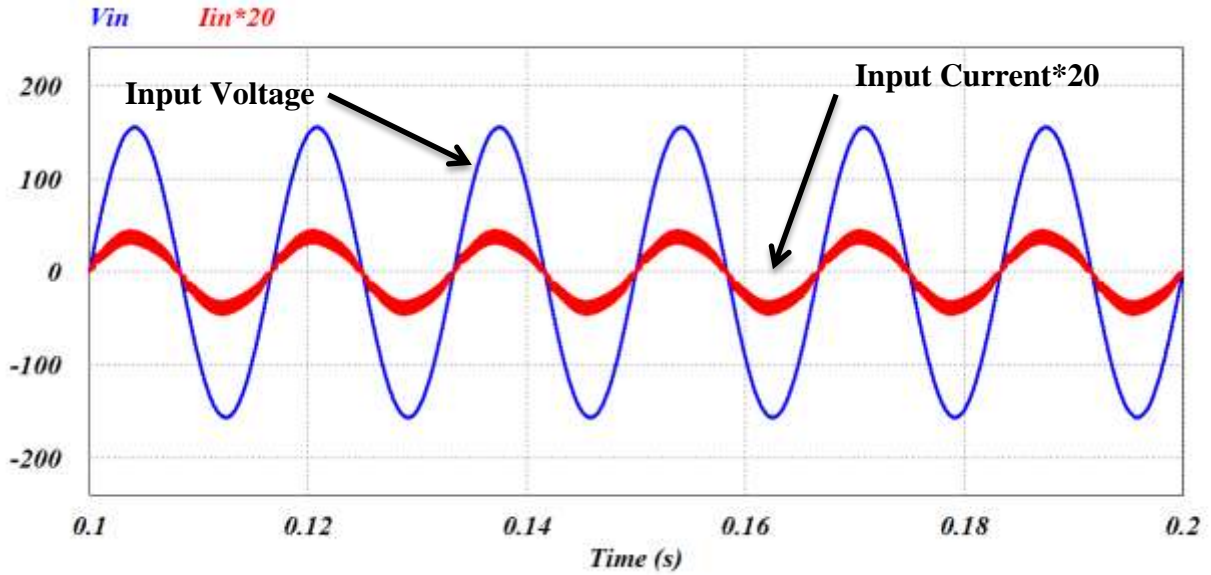
**Figure 4.9** *Input current Simulation result without feed-forward compensation*



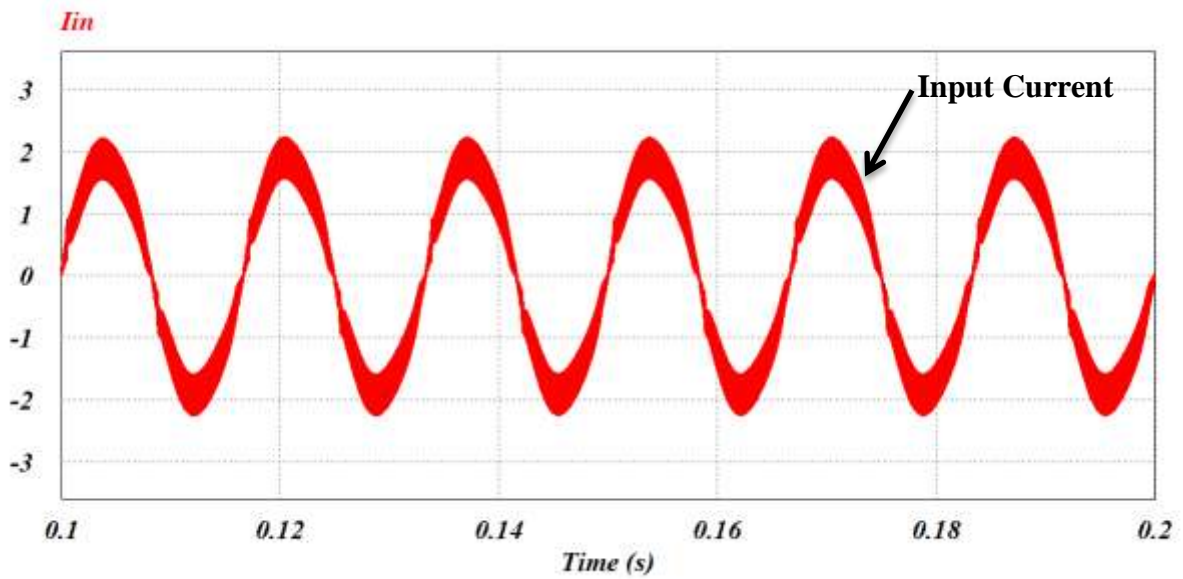
**Figure 4.10** *Input current Simulation result with feed-forward compensation.*

Final simulation results including the feed-forward compensation with decided gains are presented in Figure 4.11 and 4.12. In figure 4.11, the input current is multiplied by 20 to observe the PF and make a visible tracking between an input current and an input voltage.

As shown in Figure 4.12, PF with digital controller is above 99% and the THD is also about 10%.



*Figure 4.11 Input voltage-Input current Simulation result with Digital Controller*

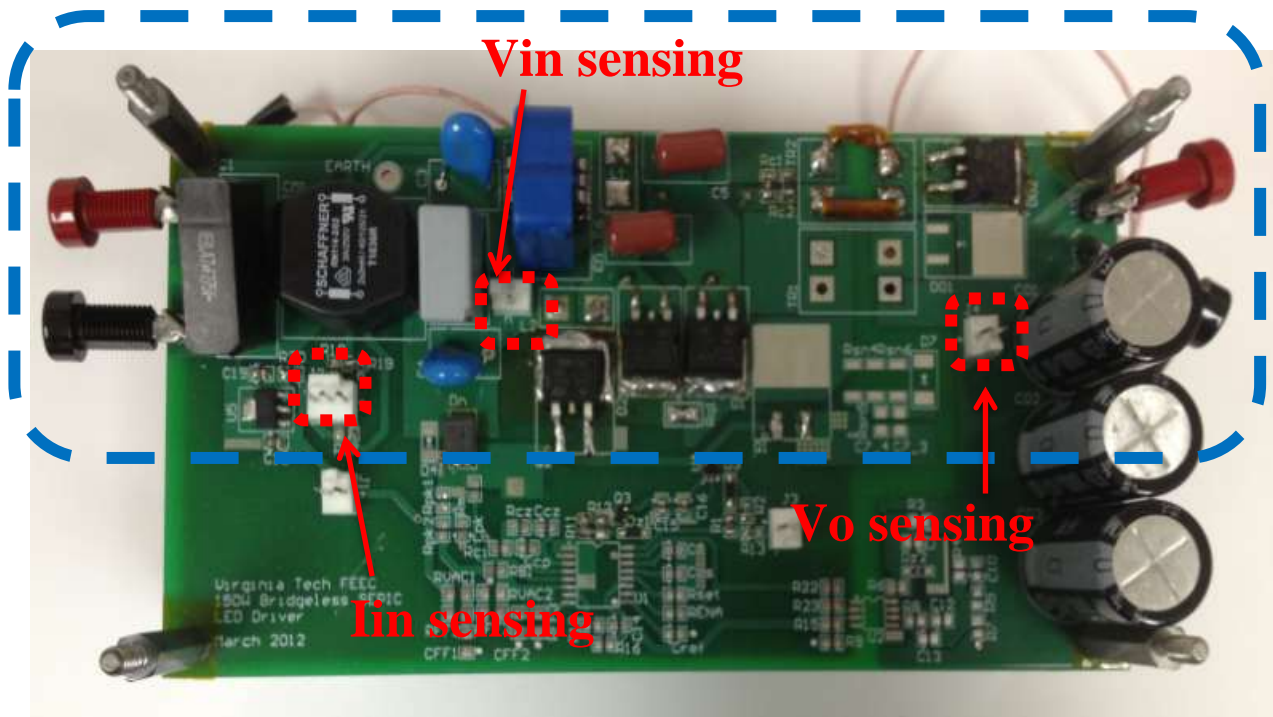


*Figure 4.12 Input Current Simulation result with Digital Controller*

#### 4.5 EXPERIMENT TEST SET-UP WITH DIGITAL CONTROLLER

The power stage test board that has interfaces to digital controllers is shown in Figure 4.13. This board is the same as the PCB used with analog controllers. This board has several options, and one of them is the possibility of digital controller implementations. Top side is for the main power stage, it has connectors for the DSP interface. The bottom side is the analog controller section, which has not been populated in this board.

### Power stage



*Figure 4.13 Digital Controller test board picture*

#### 4.6 EXPERIMENT RESULTS WITH DIGITAL CONTROLLER

With the same parameters as in simulations, the experiment results of the digital controller are shown in Figure 4.14 and Figure 4.15. This experiment is done at  $V_{in\_rms} = 110V$  @60Hz under full-load condition. From Figure 4.14, the output voltage is regulated at 50V which is desired. The input current is well tracked the input voltage and the input current shows sinusoidal waveform as expected. The PF and harmonic distortion result could be analyzed from Figure 4.15 with the same procedure in analog controller experiments. Components of harmonics are shown in Table 4.2 and summarized the PF and the THD results are:

- Power Factor (PF): 99.63%
- Total Harmonic Distortion: 4.5%

*Table 4.2 Harmonic components of digital controller experiment result*

Harmonic (Frequency, Hz)	Fundamental (60)	3 (180)	5 (300)	7 (420)	9 (540)	11 (660)	13 (780)
A (%)	1.446 (100)	0.024 (1.66)	0.016 (1.11)	0.023 (1.58)	0.022 (1.51)	0.019 (1.33)	0.014 (0.97)

❖ Digital controller experiment waveforms

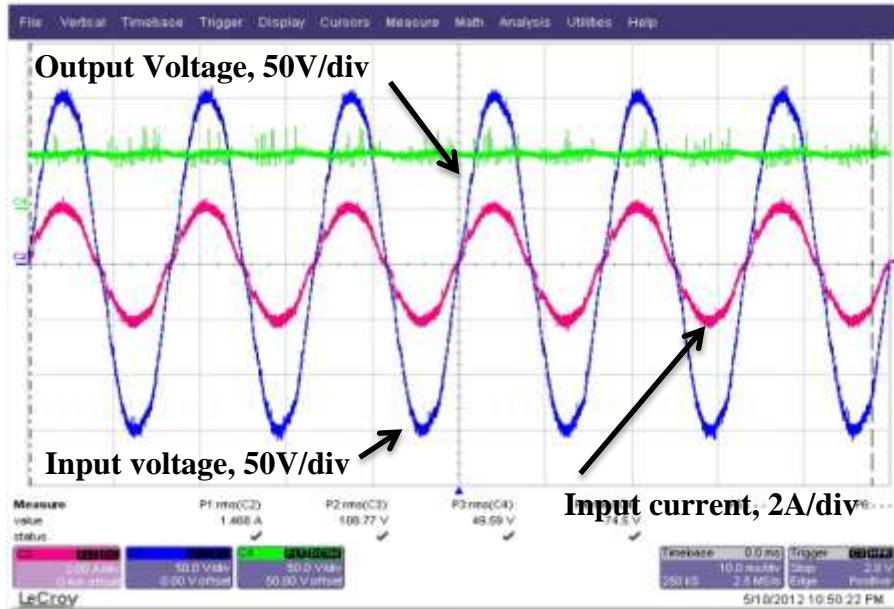


Figure 4.14 Digital Controller Experiment Result waveform 1

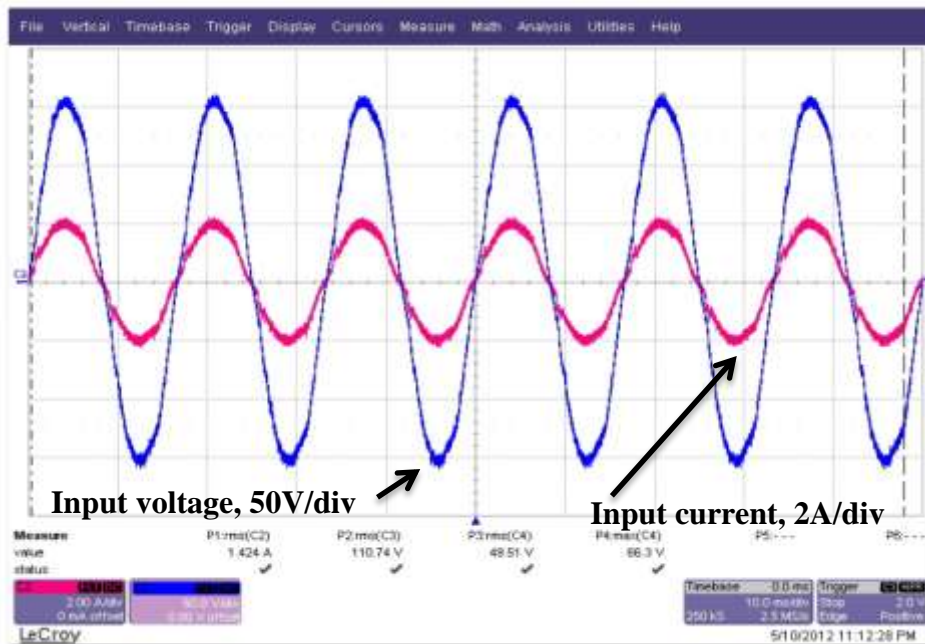
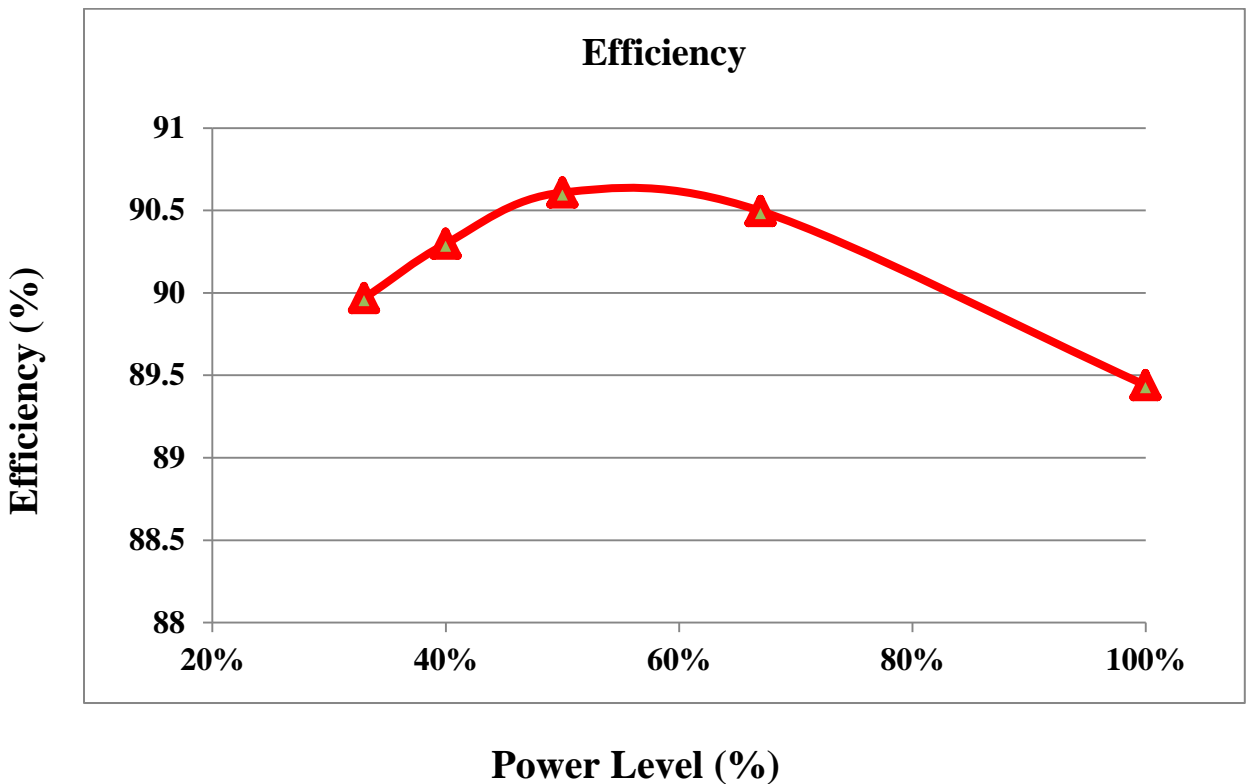


Figure 4.15 Digital Controller Experiment Result waveform 2



❖ Measured Efficiency

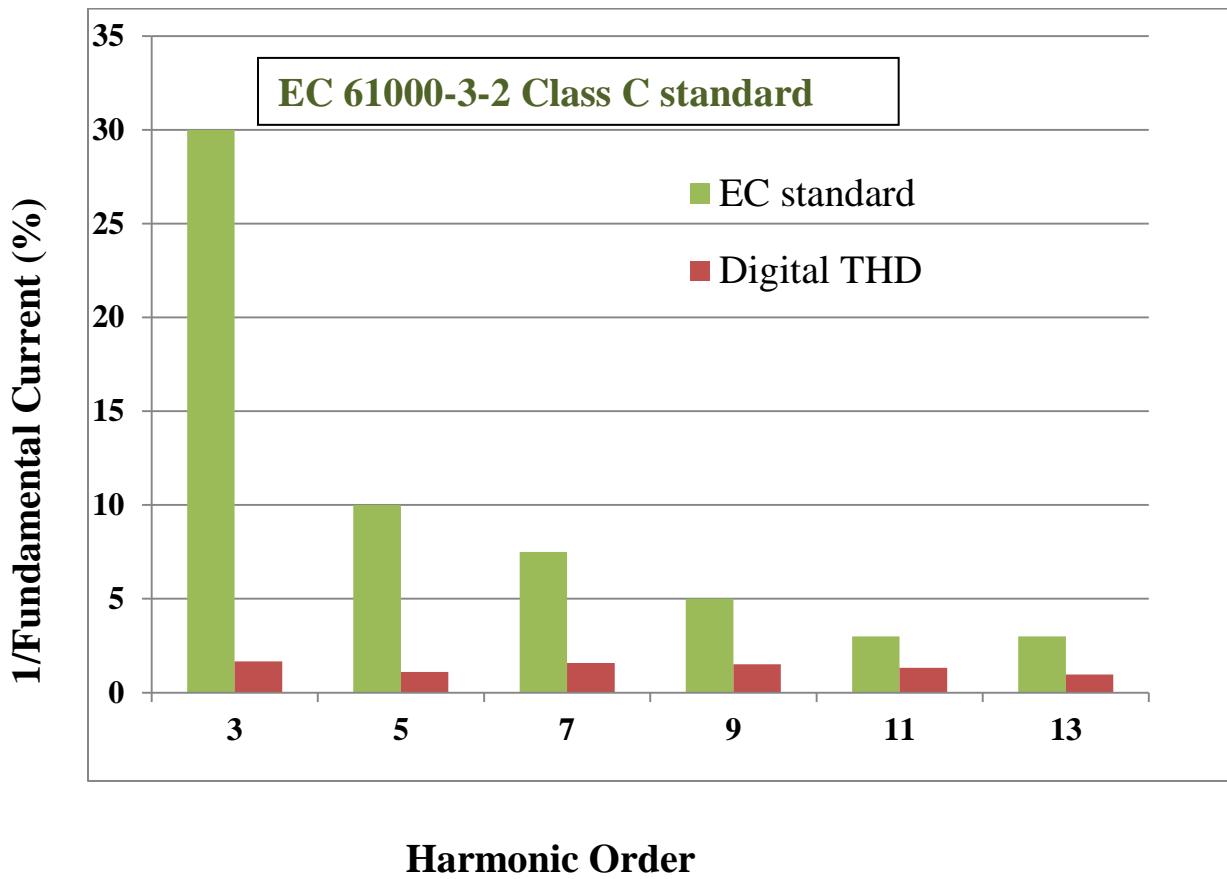
Figure 4.16 shows the measured efficiency result. In this thesis, only the simple PI controller is implemented. Other digital controllers such as fuzzy logic and neural network may be implemented to improve harmonic performance or zero-crossing compensation, which can be considered for future study. In this experiment, the overall efficiency appears to be lower than the results found in other literature [2, 12], optimizing device selection and passive component design need to be done to improve the overall efficiency.



*Figure 4.16 Efficiency Result with Digital Controller*

❖ Measured THD

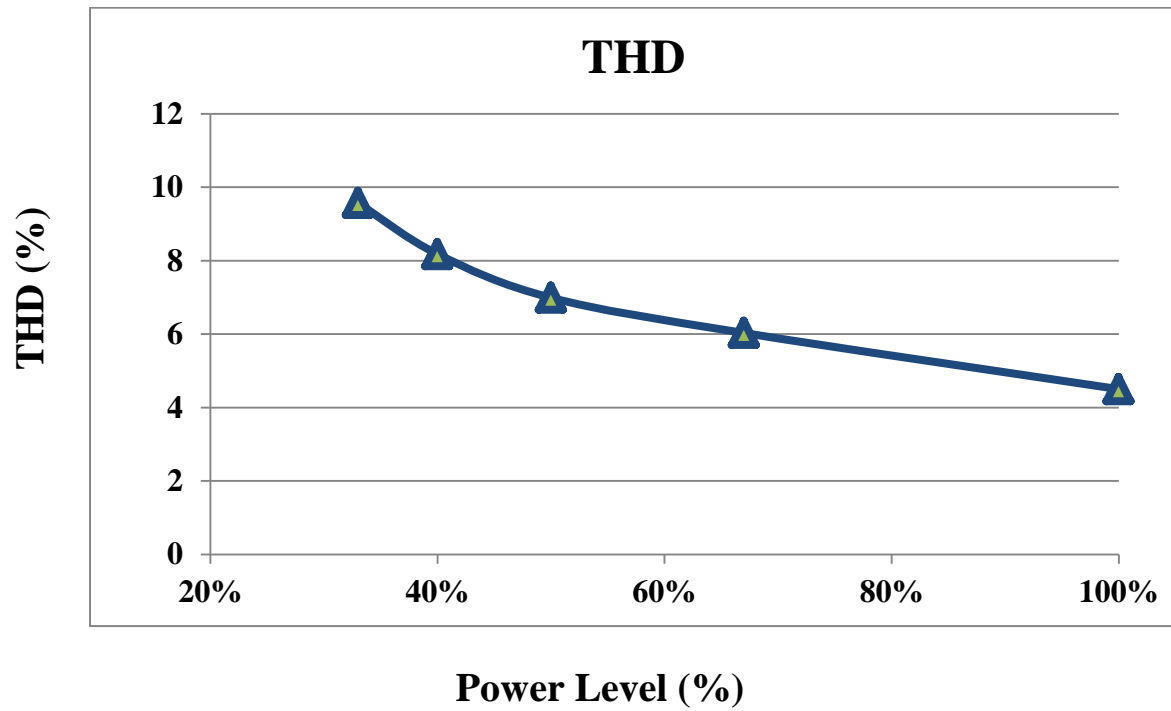
Figure 4.17 shows the comparison of input current harmonic at the full-load condition with the EC 61000-3-2 standard. As shown in Figure 4.17, the measured input current harmonic of the digital controller implementation meets the EC 61000-3-2 Class C standard for lighting equipment.



*Figure 4.17 Measured Harmonic Result comparison*

Figure 4.18 shows the measured harmonic result under various load conditions.

- Total harmonic distortion (THD) under full-load condition
  - Digital controller implementation THD : 4.5 %



*Figure 4.18 Measured Harmonic Result under various load condition*

## 5 CONCLUSION AND FUTURE RESEARCH DIRECION

### 5.1 CONCLUSION

The thesis presents the modeling and controller design of a 150W single-switch bridgeless SEPIC PFC converters for LED applications. The modeling and controller design results have been verified through simulations and experiments. A typical SEPIC converter has the complexity of a 4<sup>th</sup>-order model with an under-damped high Q-factor, which generates instability in the system, and thus the controller design of a SEPIC converter is considered more difficult than that of other dc-dc converters. However, for LED driver applications, the PFC stage with the SEPIC topology can be used as a single-stage power conversion instead of two stages because its output voltage can be lower or higher than the input voltage. The major constraint of using SEPIC converter resides on the control loop instability of. Thus, the major objectives of this thesis are to analyze the SEPIC converter plant model, to compensate the power stage with proper damping, and to design a controller that ensures stable operation for LED drivers.

#### ❖ **Modeling of complex 5<sup>th</sup>-order system by introducing damping circuit to increase stability of system**

A precise modeling is necessary to analyze the characteristics of a SEPIC converter and to design a robust controller. In this thesis, the state-space averaging method is adopted as the modeling method to complement the characteristics of the SEPIC converter, which is a complex high-order system. The modeling results indicate that a basic SEPIC converter has a resonance frequency with a high Q-factor, which is shown in Figure 2.5. This resonance frequency makes controller design difficult. As introduced in [23], a proper damping circuit design was required to comply with the given power-stage specifications and was applied to single-switch bridgeless

SEPIC PFC converter. Using the introduced damping circuit, the final complex 5<sup>th</sup>-order system model is obtained using the state-space averaging method. A significant improvement of the stability margin is illustrated in Figures 2.9 and 2.10 by frequency-domain responses. With the emphasis on accurate modeling of the SEPIC converter, modeling verification is performed by comparing the simulation model with the derived model.

**❖ Robust controller design procedure to shrink difficulty of controller design with high-order model, SEPIC converter**

The controller design of a single-switch bridgeless SEPIC converter is performed based on the exact 5<sup>th</sup>-order system model with added damping. In this thesis, a two-loop controller (voltage control loop and current control loop) is adopted. For the controller implementation, both analog and digital controllers are designed and verified with hardwares. Though many reference studies address the analog controller design of SEPIC converters, there are not many that focus on digital controller design. One of the disadvantages of the SEPIC converter is its sensitivity to parameter variations; however, analog controllers are not as flexible in this aspect. The design procedure and verification of an analog controller is described in chapter 3, and the digital controller design and implementation is presented in chapter 4 to illustrate how the SEPIC converter controller is designed using both controllers. Furthermore, the controller design is optimized with sufficient stability margin. In addition, a current feed-forward compensation, which is different from the one used in boost converters, is proposed and implemented with the digital controller.

**❖ Controller design is verified by simulation and experiment; the results meet specification and international standard for LED lighting applications.**

The simulation and experimental results are presented to verify the controller design. The results indicate that the digital controller performs better in terms of harmonic reduction or elimination than analog controller does. The main reason is a current feed-forward compensator can be added to increase the control loop bandwidth. The proposed feed-forward scheme significantly improves the harmonic performance, mainly through the zero-crossing waveform distortion reduction. The experiment results indicate that the harmonic contents are well below the limits of EC 62000-3-2, the international standard requirement for LED lighting.

### ❖ Summary

The precise modeling of a SEPIC converter is highlighted by the controller design of a single-switch bridgeless SEPIC converter. It is verified that a well-designed damping circuit reduces the high risk of system instability and its implementation makes the controller design simple. By precisely modeling a 5<sup>th</sup>-order system with a properly designed damping circuit, it is realized that a simple PI controller can be used for SEPIC PFC converters that can meet stability and international harmonic standards. This property is verified by digital controller implementation. The work involved accurate SEPIC converter modeling, proper damping design, controller design and verification with hardware implementation. In particular, the major contribution is the design and implementation of a digital controller with a single-switch bridgeless SEPIC PFC converter for LED applications.

## 5.2 FUTURE RESEARCH DIRECTION

- Optimize devices and parameters to achieve higher efficiency.
- Adopt more advanced control algorithms to take advantage of the digital control to improve zero-crossing distortion and to further reduce harmonic contents.

- Develop the entire digital controller for SEPIC PFC converter with a more cost effective micro-controller or digital controllers.

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