Application of Optimization Techniques to the Design of a Boost Power Factor Correction Converter

by

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(ABSTRACT)

This thesis analyzes the procedural approach and benefits of applying optimization techniques to the design of a boost power factor correction (PFC) converter with an input electromagnetic interference (EMI) filter at the component level. The analysis is performed based on the particular minimum cost design study of a 1.15 kW unit satisfying a set of specifications.

A traditional design methodology is initially analyzed and employed to obtain a first design. A continuous design optimization is then formulated and solved to gain insight into the converter design tradeoffs and particularities. Finally, a discrete optimization approach using a genetic algorithm is defined to develop a completely automated user-friendly software design tool able to provide in a short period of time globally optimum designs of the system for different sets of specifications. The software design tool is then employed to optimize the system design, and the savings with respect to the traditional design methodology are highlighted.

The optimization problem formulation in both the continuous and discrete cases is presented in detail. The system design variables, objective function (system component cost) and constraints are identified. The objective function is expressed as a function of the design variables. A computationally efficient and experimentally validated model of the system, including second-order effects, allows the constraint values (also as a function of the design variables) to be obtained.

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CHAPTER 1. INTRODUCTION

1.1. Motivation and Objective

The design of power electronics systems involves a large number of design variables and the application of knowledge from several different engineering fields (electrical, magnetic, thermal and mechanical). In order to simplify the design problem, traditional design procedures fix a subset of the design variables and introduce assumptions (simplifications) based on the designer's understanding of the problem. These simplifications allow an initial design to be obtained in a reasonable amount of time, but further iterations through hardware prototype testing are usually required. The ability and expertise of the designer usually leads to good, but not optimum, designs.

Mathematical optimization techniques offer an organized and methodical way of approaching the design problem. They allow the designer to use more design variables and fewer simplifications. This, in turn, reduces the number of iterations during the hardware-testing phase. The increasing speed of computer hardware and the development of faster computational models allow optimum designs to be obtained in a relatively short time. Furthermore, the application of the optimization techniques can provide a better understanding of the tradeoffs involved in the design, and may even highlight some that were initially ignored.

Several optimization algorithms can be applied to solve a design problem. Among them, the traditional gradient-based algorithms have been widely applied to solve continuous design variable problems. Other stochastic approaches such as genetic algorithms have been also successfully applied to solve both continuous and/or discrete design variable problems. The two types of algorithms present different advantages.

The aim of the present work is to study and highlight the benefits of applying these optimization techniques to the design of a low-cost boost power factor correction (PFC) front-end converter with input electromagnetic (EMI) filter, the ultimate goal being to develop a practical and user-friendly software tool able to automatically obtain within a short design time the minimum-cost designs for different sets of specifications and conditions.

Hopefully, this work will contribute to the enhancement of the design methodology in the field of power electronics, leading to automatic and faster design methods that are able to provide improved design solutions.

1.2. Review of Previous Research

Even though there is not a broad range of literature on the topic of optimization in power electronics, a few efforts have been made in the past. Some discuss the particularities and advantages of applying optimization techniques in the design of power electronics systems, and present a continuous variable optimization approach applied to the design of the power stage of buck, boost, buck-boost and half-bridge DC-DC converters [1,2,3]. Passive components, switching frequency and tefficiency are considered to be continuous design variables (several design variables related to the core and windings are considered to define the inductors). The objective function to minimize is the weight of the converter. Constraints are defined according to the design specifications and physical limitations. An optimization algorithm known as the ALAG (Augmented Lagrangian) penalty function is selected to solve the problem. Several optimum design solutions are obtained by setting the switching frequency at different values and the results are then analyzed. The switching frequency is fixed in order to alleviate convergence difficulties that might otherwise cause a substantial increase in the required computation time. Another paper introduces several improvements into the previous optimization approach in order to obtain a practical nonlinear optimization tool [4]. The methodology is demonstrated in the case of the half-bridge converter design. The paper discusses how the number of design variables can be reduced in order to simplify the design problem. Also, decoupling the design problem into two or more sub-design optimization problems is suggested whenever the interrelation of the sub-design problems is weak. In order to facilitate the use of the software developed, the equations that model the design problem are separated from the optimization algorithm codification, so that a user-friendly review of the problem formulation is allowed. Last, since the design variables are considered continuous, but real components are only available with discrete values of their defining parameters, a methodology is proposed to obtain realistic design results. This methodology consists of running the optimization, fixing the design variables of one of the components to their closest real values, and then rerunning the optimization. The process is

repeated until all the design variables contain values corresponding to available components. In a later paper [5], this tool [4] is used in the design of a boost PFC converter.

In all previous articles, the design variables refer only to those components that can be easily considered to be defined by continuous real values, such as capacitors, resistors, cores and wires. Others, such as the devices, are considered to be fixed. This is a result of the fact that the nature of the design problem is essentially discrete; therefore, the use of continuous optimization techniques has its limitations.

The definition of the efficiency as a design variable is quite questionable from a conceptual point of view. The authors introduced this design variable to avoid having to define an iterative computational method to estimate its value, since there is no explicit equation for calculating the efficiency of the system as a function of the design variables. Instead, they decided to use the optimization algorithm itself as the iterative method for obtaining the efficiency value, by defining a design variable as the efficiency and then establishing a constraint so that the calculated value of the efficiency matches the assumed value in the design variable.

As mentioned, the design of a boost PFC converter is considered in previous research [5]. But a variable hysteresis control strategy is considered for the switch, as opposed to the fixed frequency strategy considered in the present work. Additionally, since no input filter and no EMI requirements are considered in the design problem, the optimization runs, which consider the ripple allowed in the boost inductor current as a design variable, presented a discontinuous current mode solution as the optimum, since for this case the boost inductor size and weight are minimized. This forced the authors to set the ripple in the boost inductor to an estimated good value, leaving as design variables only those referring to the boost inductor configuration. A more appropriate design optimization problem formulation should therefore include the input EMI filter and the EMI requirements. On the other hand, the authors decided to set the design variable ‘efficiency’ to 95% in the optimization runs, which in the opinion of the author of the present text constitutes an unnecessary restriction on the design problem formulation.

More recent efforts toward the application of optimization techniques to the design of power converters can be found [6,7]. One proposes the use of genetic algorithms to optimize the design of the power converter [6]. The design problem is decoupled into the design of the power stage and the design of the controller, and these are optimized separately. The only design

variables considered are the passive components that define both subsystems: the resistors, capacitors and inductors. Each of these components is defined by a real number specifying the corresponding resistance, capacitance and inductance. The objective function or fitness value assigned to each design includes electrical performance information mainly.

Another paper presents a software tool developed to aid in the design of power electronics systems [7]. An expert system and knowledge base helps in the selection of power and control topologies and components. Continuous variable optimization techniques are applied in the design of magnetic components. The electrical models contained in the software tool appear to be fairly complete and detailed.

1.3. Power Factor Correction Unit Specifications

The goal is to find the lowest-cost design of a boost PFC front-end converter with input EMI filter (Figure 1.1) that meets a set of specifications. The load contains an additional EMI filter, an inrush current circuitry and an electrolytic capacitor C_{Load}. The general specifications are presented in Table 1.1, and Table 1.2 summarizes the standards with which it must comply.

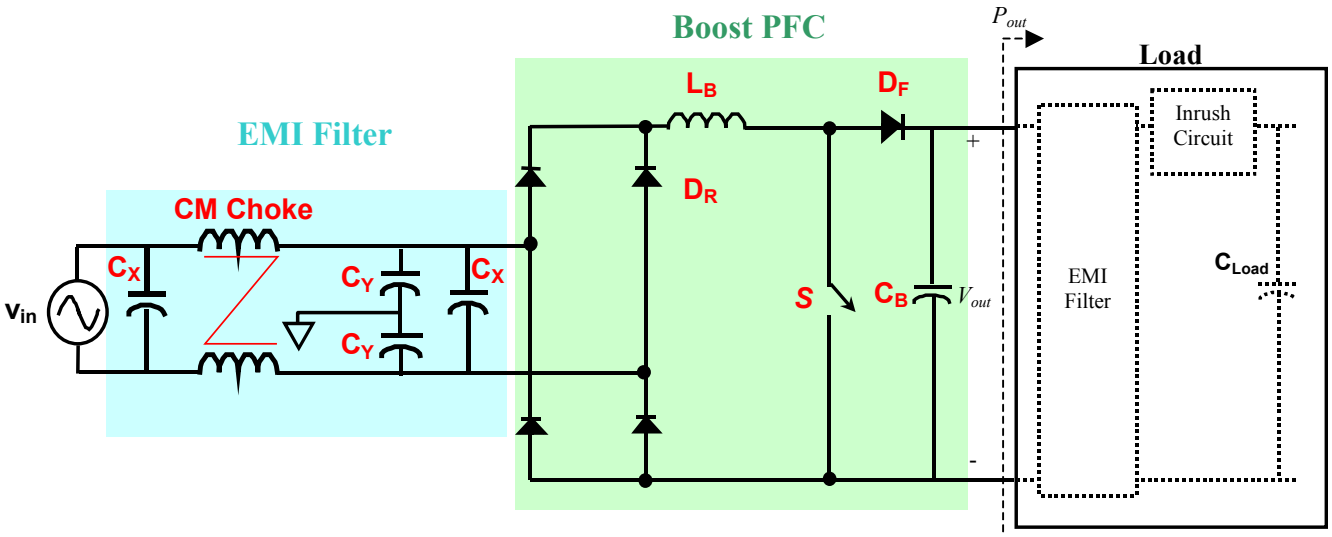

Figure 1.1. Schematic of the PFC front-end converter.

Table 1.1. General specifications.

Magnitude	Value
Vin (Vrms)	180÷264 180÷240 (Complying with IEC 1000-3-2 [8])
F_line (Hz)	47.5÷63
P_{out} (W)	1150
Lline (µH)	750
C_{Load} (µF)	624 ÷ 1060
Maximum Vout (V)	375
Vout_inrush (voltage above which the inrush resistor in load is shorted) (V)	200
Ambient temperature (°C)	Storage: -25÷80
	Nominal Operation: -10÷50*
	Operation with Current Derating: -10÷60
Maximum unit physical dimensions (mm)	130 x 105 x 40
Units per year	20000

*Initially, the maximum temperature considered was 40°C.

Table 1.2. Standards to satisfy.

Type		Standard	Level
EMC	Emission	EN 55011 IEC 61800-3(1)	Conducted: Class B (Public sector) Radiated: Class B (Public sector)
	Immunity*	IEC 61800-3 IEC 6100-4-X	61000-4-2 (Level 3) 61000-4-3 (Level 3) 61000-4-4 (Level 4) 61000-4-5 (Level 3) 61000-4-6 (Level 3) 61000-4-11 (Level 3) 61000-4-12 (Level 3)
Input harmonic current		IEC 61000-3-2 [8]	Class A

*These specifications will not be considered in the design process. They will be experimentally verified afterwards.

Other special specifications are:

- The load can change from 100% to 0% in $t \geq 1$ms, and from 0% to 100% in $t \geq 1$ms (to be considered in the control design).
- The PFC stage should be able to operate with an input voltage V_{in} = 100 Vrms and P_{out}=555 W. (This specification will not be considered in the design process. It will be experimentally verified afterwards.)
- In a hot state (after one or two hours of operation) the PFC stage must be able to provide P_{out}=1750 W for 15 seconds without any PFC and electromagnetic compatibility (EMC) requirement. (This specification will not be considered in the design process. It will be experimentally verified afterwards.)

1.4. Thesis Outline and Major Results

The thesis is organized in the following manner. In Chapter 2, a set of manual designs is generated following a traditional design methodology. In Chapter 3, optimization techniques are applied to the design problem. Formulations and solutions are presented for both a continuous variable optimization that is intended to provide insight into the converter behavior and design tradeoffs, and later, for a discrete variable optimization. A user-friendly software tool, based on the discrete optimization formulation, is presented. This software tool allows the novice designer to quickly and automatically obtain the minimum-cost designs for different sets of specifications and conditions. The best design obtained using this tool is compared to the initial ones, and the improvements are highlighted. Finally, in Chapter 4, the thesis is concluded and a brief discussion on the future of the application of optimization techniques in the design of power electronics systems is presented.

CHAPTER 2. INITIAL CONVERTER DESIGN

2.1. Single-Phase Boost Power Factor Correction Converter: Principle of Operation

Many applications require an ac-to-dc conversion from the line voltage. In its most simple form, this conversion is performed by means of a bridge rectifier and a bulk capacitor. The bulk capacitor filters the rectified voltage and provides certain energy storage in case of a line failure. But the resultant line current pulsates, causing a low power factor due to its harmonics and its displacement with respect to the line voltage. In many countries, this low quality in the power usage is not acceptable above certain minimum power levels, and the corresponding standards require improved technical solutions. One of the topologies most commonly used to deal with this problem is the so-called single-phase boost PFC (see Figure 2.1).

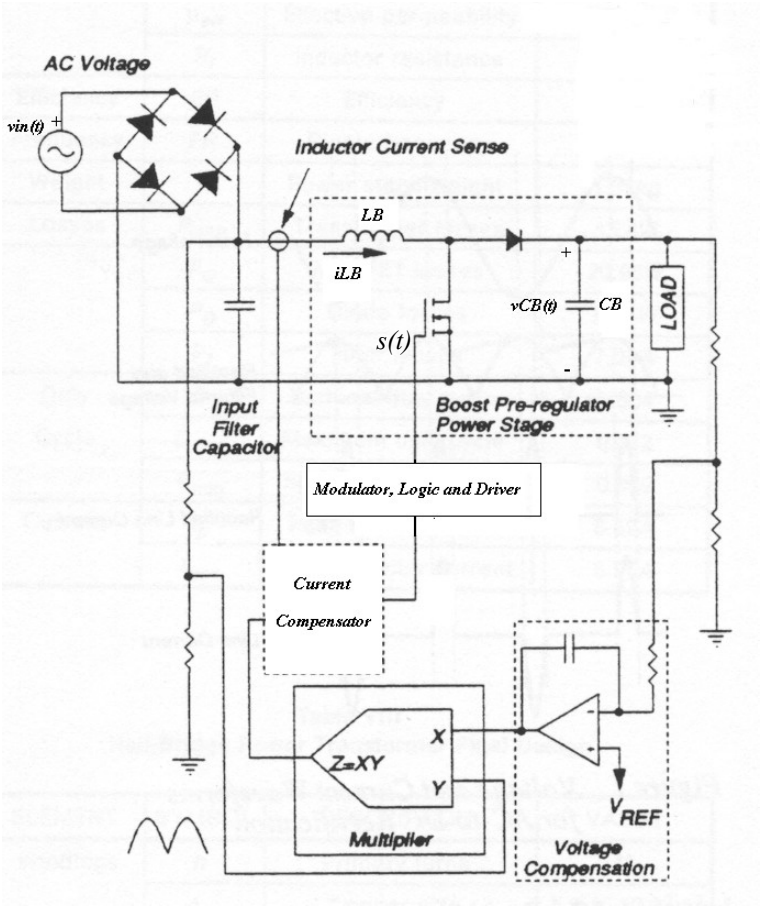

Figure 2.1. Single-phase boost PFC converter [5].

In this configuration the active switch is controlled so that the average (in a switching period) input current is shaped as a sinusoid in phase with the input voltage, therefore substantially improving the power factor. Additionally, the dc output voltage is regulated within a bandwidth of less than the line frequency. All this is achieved by sensing the inductor current, "comparing" it to a sensed rectified input voltage (scaled according to the low-frequency error in the output voltage), and using the resultant signal to generate the control for the switch [9]. The scheme is simple and reliable, and it is widely used in industry.

The main steady-state waveforms of the system are depicted in Figure 2.2. It is important to note that the average output voltage (V_{CB_dc}) must be greater than the peak input voltage (v_{in}) for the system to operate normally (providing PFC in the input). This output voltage presents a ripple of frequency twice the line frequency due to the instantaneous power imbalance between the input and the output.

The harmonics in the input current due to the switching are filtered by means of an EMI filter in order to meet the limit set by the corresponding standard.

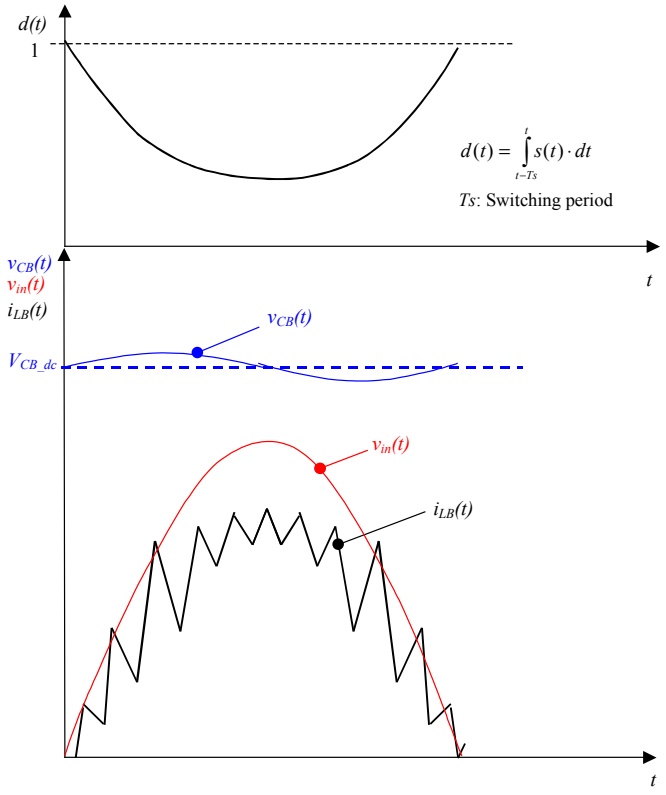

Figure 2.2. Main steady-state waveforms.

2.2. Power Stage Component Design

2.2.1. General Design Process and Considerations

The general design process followed to obtain the initial designs is summarized in Figure 2.3.

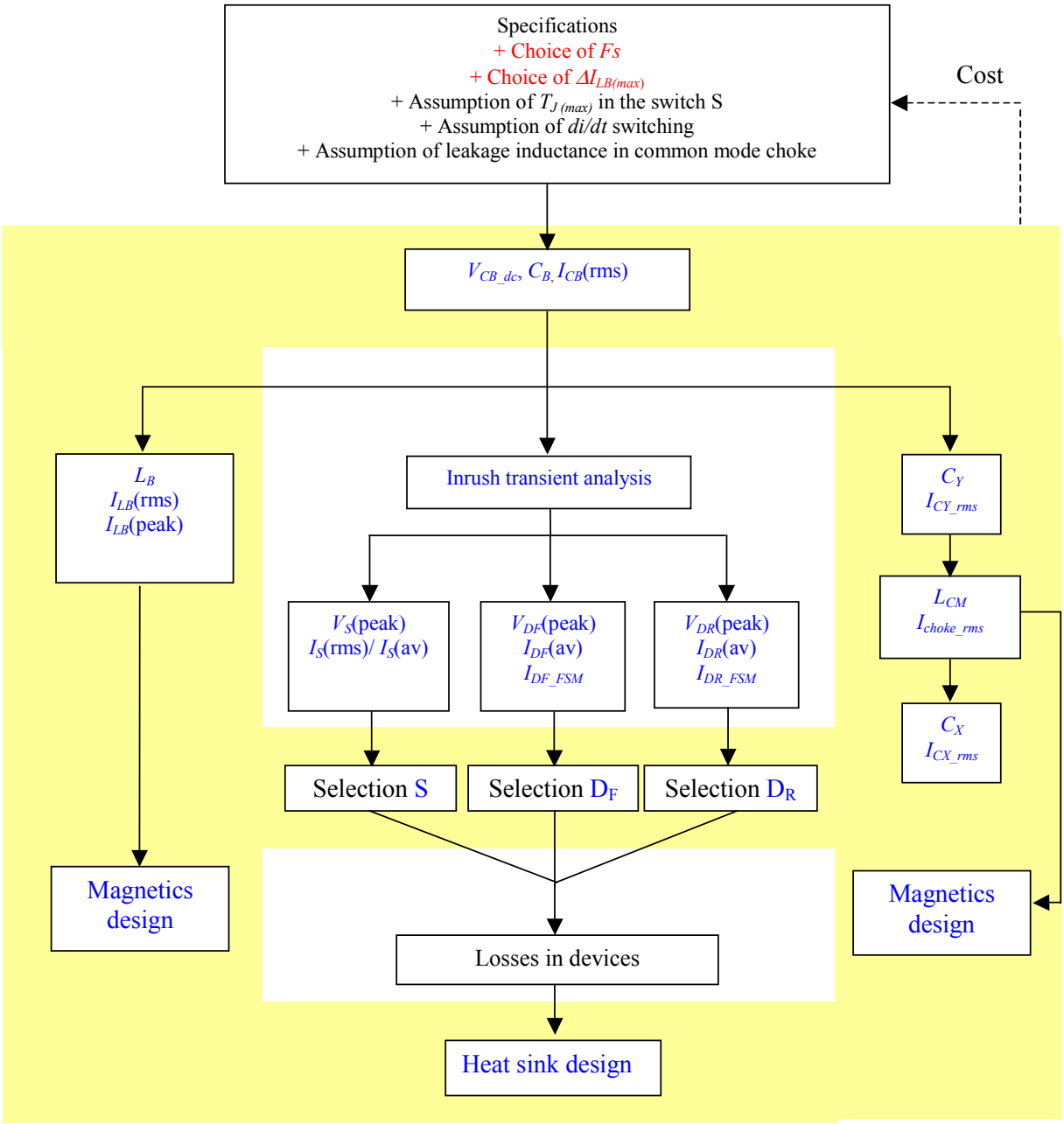

Figure 2.3. Design process diagram.

The design of the system is performed based on the worst case identified in each instance. The design process begins with the selection of switching frequency *Fs* and the maximum current ripple through the boost inductor L_B, $\Delta I_{LB(max)}$. The junction temperature of the switch S, $T_{J\,(max)}$, the value of the *di/dt* of the current through S and D_F in the switching transitions, and the leakage inductance in the common mode choke, CM Choke, must be assumed. In the next step, the average output voltage and output boost capacitance are selected according to the specifications. This selection is discussed in Section 2.2.2.1. Once these two values are determined, the rest of the components in the converter can be designed.

The boost inductor inductance and current ratings can be determined. These calculations are given in Section 2.2.2.2.

In Section 2.2.2.3, the selection of the devices is discussed. An initial study of the inrush transients and the possible design solutions to handle them is required in order to determine some of the device ratings. Once the devices are selected, the design of the heat sink can be performed from the estimation of their losses.

In Section 2.2.3, the methodology for the design of the EMI filter is presented.

Finally, the detailed design of the magnetic components (boost inductor and common mode choke) is discussed in Section 2.2.4.

In the design of the system, several tradeoffs are identified. The optimum switching frequency and boost inductor current ripple are not clear due to the existence of these tradeoffs. Therefore, in the first stage, it was decided that some designs for several pairs of values of the switching frequency/boost inductor current ripple should be explored in order to investigate the aforementioned tradeoffs and to identify the switching frequency / boost inductor current ripple range in which the cheapest design could be found.

In Section 2.2.5, a description of the designs obtained for the various pairs of switching frequency / boost inductor current ripple values is presented.

The aim of this chapter is to describe in general the design process followed and to present the results obtained. A more detailed description of the design process and the equations used can be found in a previous report [10].

2.2.2. Design of the Boost PFC stage

The boost PFC stage is designed in terms of the worst case: minimum input voltage and maximum load.

2.2.2.1. Boost Output Capacitor and Average Output Voltage

Due to the weak interaction between the design of the boost capacitor and those of the remaining components, the main goal here was to select the average output voltage and boost capacitance in order to minimize the cost of this capacitor while meeting the specifications. In the specifications, the maximum instantaneous output voltage is 375 V. The minimum average output voltage can be determined from the maximum input voltage for which the PFC standard must be satisfied, as 240 Vrms*sqrt(2) = 340 V. The tolerance in the value of the average output voltage due to the tolerances in the control IC and the output voltage divider network has been estimated to be 2.2%. To estimate the size of the boost capacitor required, it is important to remember that an internal capacitor exists in the load, which has a minimum capacitance of 624 μF.

From the analysis, it turned out that there is no boost capacitance required in this situation. The highest possible nominal average output voltage is selected to maximize the range of voltages for which PFC can be achieved. This nominal average output voltage is 359 V. The maximum input voltage for which PFC can be achieved given this nominal average output voltage is 248 Vrms. The solution selected is depicted in Figure 2.4.

Even though no need for a boost capacitor was identified, it was decided that a 68 μF boost capacitor should be chosen to avoid possible interactions between the boost power stage and the EMI filter contained in the input of the load. This capacitor also provides some additional margin in the design.

2.2.2.2. Inductance and Current Ratings of the Boost Inductor

The determination of the boost inductor inductance can be obtained from the choice of the maximum boost inductor current ripple and switching frequency. The saturation of the core is neglected, and therefore a single value of inductance is considered for the entire half line cycle.

In this situation, the maximum current ripple occurs when the duty cycle is 0.5, as shown in Figure 2.5.

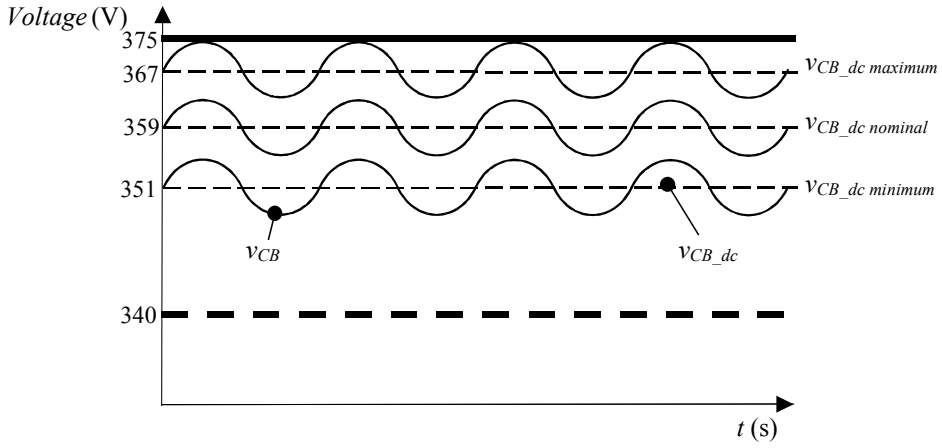

Figure 2.4. Output voltage range based upon 2.2% tolerance in the average output voltage and a 0 µF output boost capacitor.

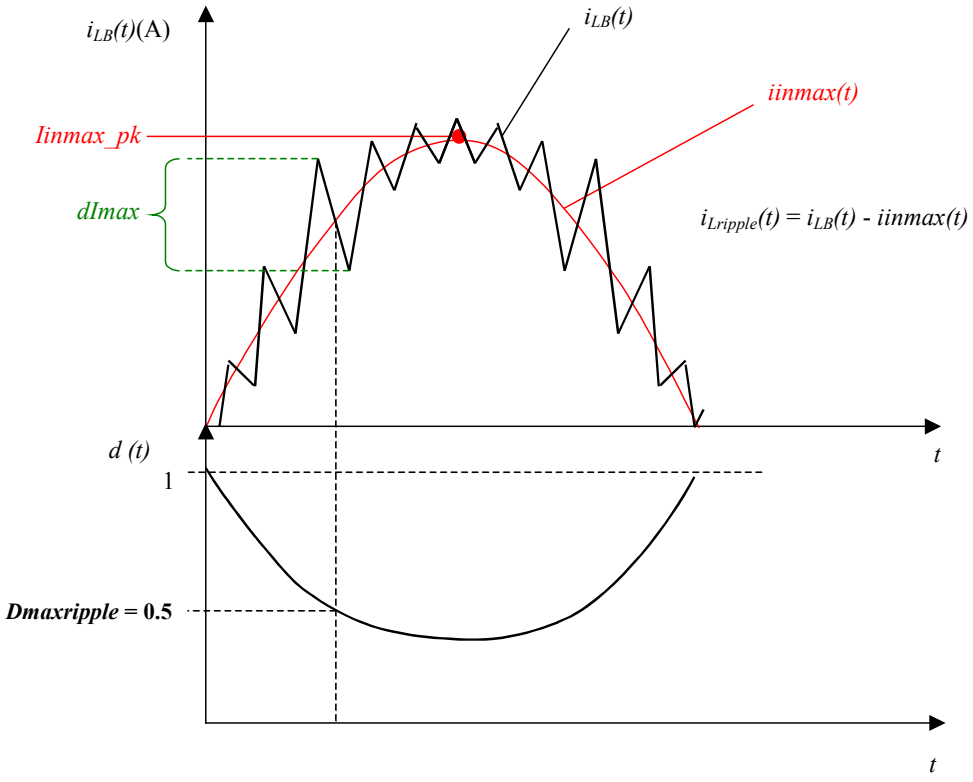

Figure 2.5. Current through L_B and switch S duty ratio.

Once the inductance has been determined, the ripple on each switching cycle is computed, and using this information, the peak and rms values of the boost inductor current are calculated.

2.2.2.3. Device Selection and Heat Sink Design

2.2.2.3.1. Inrush Transients

Inrush transients resulting from start-up and fast disconnect from / reconnect to the mains must be considered for converter layout and device selection. These transients cause both an inrush current through the diodes and boost capacitor, and an overshoot in the voltage across the boost capacitor and switch. A SABER model was developed to study these inrush transients [11]. The worst-case scenario for both inrush current and voltage overshoot was identified. In the case of inrush current, the worst case occurs during fast disconnect from / reconnect to the mains. The worst case for voltage overshoot occurs during start-up. From the results of these simulations, the recommended ratings to allow the different components to withstand these transients without any additional circuitry are as follows.

Boost Capacitor:	V_{max} = 400V I_{max} = 20Arms
Rectifier Bridge:	I_{FSM} = 150A
Fast Diode:	I_{FSM} = 150A
Switch:	V_{BR} = 500V (MOSFET)
	V_{BR} = 600V (IGBT)

Since these ratings are reasonable, it was considered to be more cost-effective to deal with the inrush transients by increasing the component ratings instead of introducing additional circuitry, which adds significant cost to the converter and which may also decrease the overall reliability.

2.2.2.3.2. Device Selection

From the boost inductor current waveform obtained in Section 2.2.2.2 without taking into account the effect of saturation of the core, the steady-state operation current ratings of the switch (IGBT: average current; MOSFET: rms current), fast diode (average current) and rectifier diodes (average current) can be obtained. Now that the current and voltage ratings have been obtained, the cheapest devices meeting these ratings can be selected from a database of components.

2.2.2.3.3. Heat Sink Design

The losses of the devices are computed, taking into account both conduction and switching losses. The detailed models can be found in Appendix A or in a previous report [10].

In the case of a switch MOSFET, a static model consisting of a resistor that is dependent on the junction temperature of the device is considered for the estimation of the conduction losses (see Figure 2.6). A dynamic model, together with the parasitic capacitance values, other specific parameters of the device (such as the threshold voltage, etc.), and the values of the voltage, on-resistance and off-resistance of the gate driver that are in agreement with the switching assumed *di/dt*, are used to estimate the switching losses that occur due to overlap of the semi-ideal (without considering voltage and current overshoots) current and voltage waveforms. The losses due to the parasitic inductance in series with the switch, which causes over-voltages during turn-off of the device, are also estimated. Finally, the losses due to the dissipation of the energy stored in the Coss (drain-to-source capacitance) during turn-on are also calculated.

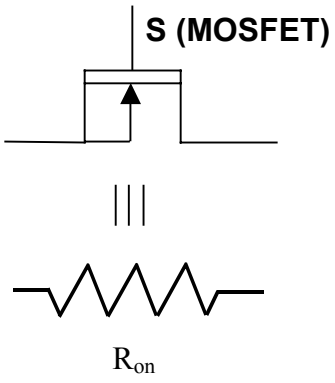

Figure 2.6. Equivalent conduction model for the MOSFET switch.

In the case of the switch IGBT, a static model consisting of a resistor in series with a voltage source (see Figure 2.7) is considered for the estimation of the conduction losses. To estimate the switching losses, the experimental parameters Eon and Eoff provided in the data sheet for a given switch current and voltage are used. These parameters specify the energy lost during the switching transitions. The parameters are scaled linearly according to the voltage and current for which the energy lost in the transitions should be estimated. This approach, based on experimental parameter information, was chosen due to the lack of a simple dynamic model able to accurately estimate these losses.

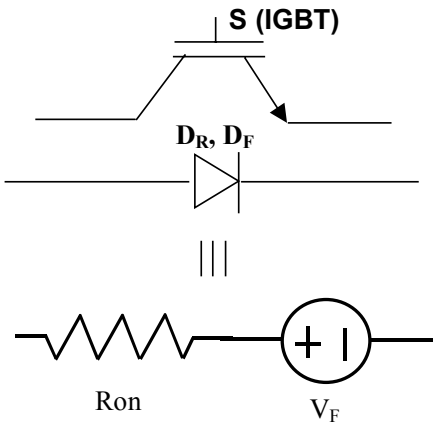

Figure 2.7. Equivalent conduction model for the IGBT switch, fast diode and rectifier diode.

In the case of the fast diode, a static model consisting of a resistor in series with a voltage source (see Figure 2.7) is considered for the estimation of the conduction losses. The switching losses due to overlap of the semi-ideal current and voltage waveforms are neglected, since in a boost configuration of the pulsewidth modulation (PWM) switch, these losses take place mainly in the switch. Estimation of the reverse-recovery losses involves use of the experimental parameter *Qrr* in the data sheet approximated as a function of the forward current and provided for a given switching *di/dt*. This parameter specifies the extra charge required to turn off the diode that results in additional losses. These losses do not exclusively take place in the fast diode. Part of the losses are dissipated in the switch. This has been taken into consideration in the models and usually a 50/50 share of the losses has been assumed.

In the case of the rectifier diode, a static model consisting of a resistor in series with a voltage source (see Figure 2.7) is considered for the estimation of the conduction losses.

From this device loss information, the heat sink can be designed. A single heat sink for all the devices was assumed in these initial designs, and the minimum heat sink size to avoid heat sink temperatures above 80 °C (maximum temperature allowed in an external heat sink) was selected. It was assumed that for a heat sink temperature of 80 °C none of the devices would have a junction temperature beyond its corresponding maximum.

2.2.3. Design of the EMI Filter

This section presents the methodology applied to the design of the EMI filter in order to guarantee compliance with the corresponding standards.

2.2.3.1. EMI Standards

BS EN 55011 [12] and CISPR 16-2 [13] are the standards relevant to the conducted EMI noise limits in the input of the converter. The former describes the limits and test conditions under which the converter must comply with regulations. The quasi-peak limit spectrum in the voltage across the LISN resistors for Class A, Group 1 and Class B, Group 1 of the apparatuses is presented in Figure 2.8.

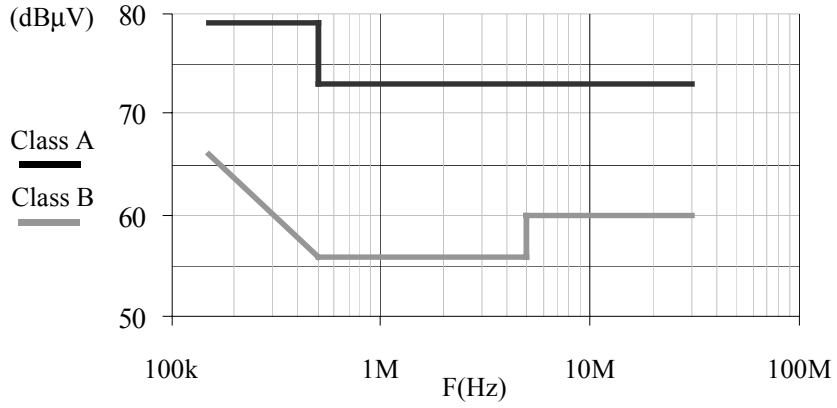

Figure 2.8. BS EN 55011 regulation limits.

For commercial sale, an input EMI filter must be added to the boost PFC stage in order to limit conducted emissions. The topology selected is shown in Figure 1.1. The common mode choke is defined by the common mode inductance (*Lcm*) and the parasitic (leakage) differential mode inductance (*Ldm*). *Cy* and *Cx* are the common and differential mode capacitances,

respectively. *Lcm* and *Cy* configure the common mode filter, and *Ldm* and *Cx* the differential mode filter. The modeling approach and design process applied to obtain the design of the EMI filter in these first manual designs is presented next.

2.2.3.2. System Modeling Approach for EMI Analysis

The design procedure is based on a frequency domain model described in other work [14, 15]. It is based on both a complete representation of possible propagation paths for differential and common mode disturbances and a frequency domain representation of conducted EMI sources present in the converter (existing in both types of propagation paths). The propagation path model takes into account CISPR 16-2 test conditions (ground plane, LISN, etc…) and a high-frequency model representation of the converter, including parasitics. By accounting for the effects of the test conditions in the filter design, the iterations in the design process are minimized.

The fundamentals of the modeling approach applied to estimate the EMI levels are presented next.

The diagram in Figure 2.9 represents all the components of the system and the parasitics considered. The circuit components are shown in black, while the circuit parasitics are shown in red. The commutation cell can be represented by an equivalent voltage source with the time domain voltage waveform shown in Figure 2.10 for only two switching periods.

In fact, the duty ratio of the switch varies for each switching period. As a result, the period of the voltage waveform Vds(t) is equal to half of the line period. But since the rectifier bridge changes the polarity of the voltage each half line period, this voltage, Vds(t), propagates to the system located before the bridge rectifier with a period equal to the line period.

This voltage source can be appropriately characterized in the frequency domain by means of the Laplace transformation, followed by application of the appropriate conversion to the Fourier representation. In essence, by means of these steps, the previous voltage waveform is represented by an addition of sinusoids, each at a multiple of the fundamental frequency (in this case, the line frequency). For each of these frequencies, and assuming that the system is symmetric between the mains and the rectifier bridge (with respect to ground), it is possible to derive from Figure 2.9 the diagram shown in Figure 2.11.

The commutation cell in Figure 2.11 has been represented as a sinusoidal voltage source (Vpert) corresponding to the harmonic of the relevant frequency. The different impedances (Z#) correspond to the system components and parasitic impedances at this frequency.

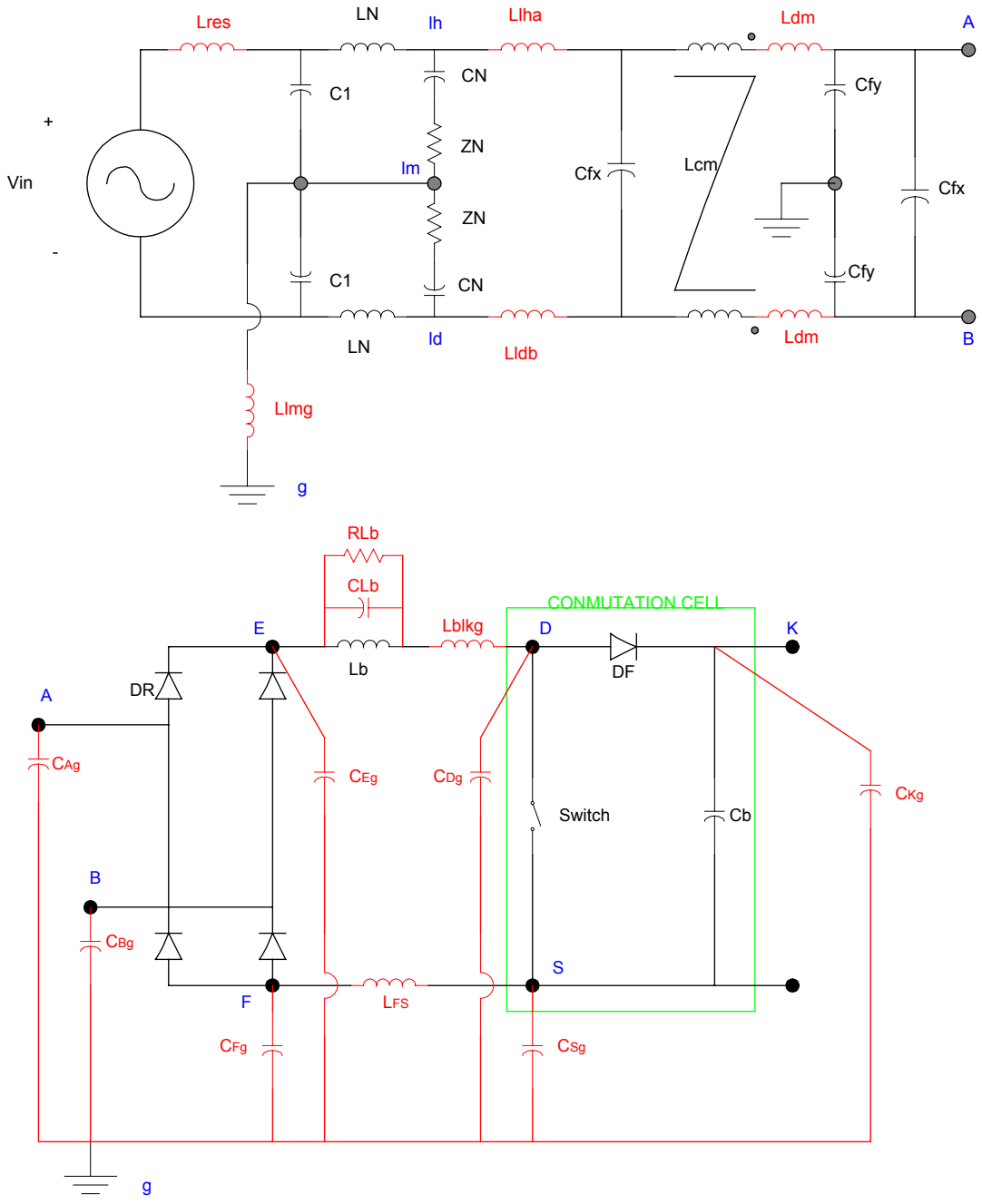

Figure 2.9. System schematic, including LISN, EMI filter and single-phase boost PFC stage.

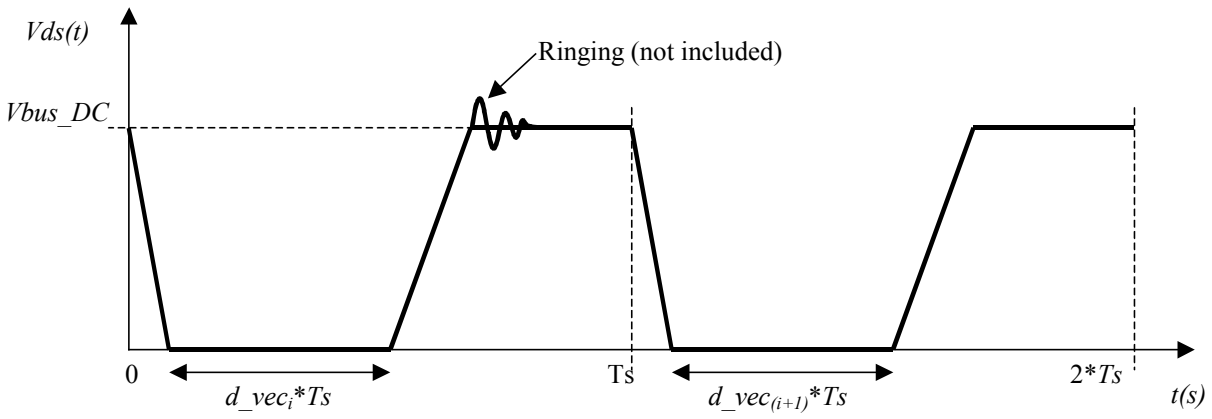

Figure 2.10. Time domain evolution of an equivalent voltage source substituting the commutation cell.

Hence, by using standard electrical network analysis methods, it is now possible to compute, for each desired frequency, the perturbation voltage levels in the LISN resistors (ZN). In this project, the quasi-peak standard limits defined for the voltage levels in the LISN resistors have been considered. A maximum voltage level is specified at each frequency. However, this maximum not only refers to the voltage harmonic at this specific frequency, but to a bandwidth of frequencies (9 kHz) around the relevant frequency. In fact, the operation of the measurement device while obtaining the quasi-peak level at one specific frequency (f_*) can be compared to obtaining the square root of the quadratic sum of all the harmonics within f_* - bandwidth/2 and f_* + bandwidth/2. Computing all harmonics to be able to precisely emulate the behavior of the measurement device would be too labor-intensive in terms of the computations involved. Only the significant levels (those at the first multiples of the switching frequency) are estimated. These estimations are obtained by computing the square root of the quadratic sum of several harmonics around some multiples of the switching frequency. To speed up the analysis, not all harmonics in the bandwidth are normally computed. The level obtained is consequently corrected by adding a certain amount of dB. This amount depends upon the number of harmonics considered. This estimation is then compared to the maximum quasi-peak level defined by the standard for the considered frequency.

In the particular topology studied here, the differential and common mode EMI levels can be easily identified, since the odd harmonics correspond to differential mode noise and the even harmonics to common mode noise. Therefore, the differential mode noise level at each multiple

of the switching frequency can be evaluated by calculating the square root of the quadratic sum of the odd harmonics around this frequency. The same approach is taken for the common mode noise level, except that the even harmonics are used in the calculations. The square root of the quadratic sum of the differential and common mode levels is equal to the total noise. The decomposition of the total noise into differential and common mode noise provides valuable information for estimating the individual performances of the differential and common mode parts of the filter, and will therefore be an aid in the design.

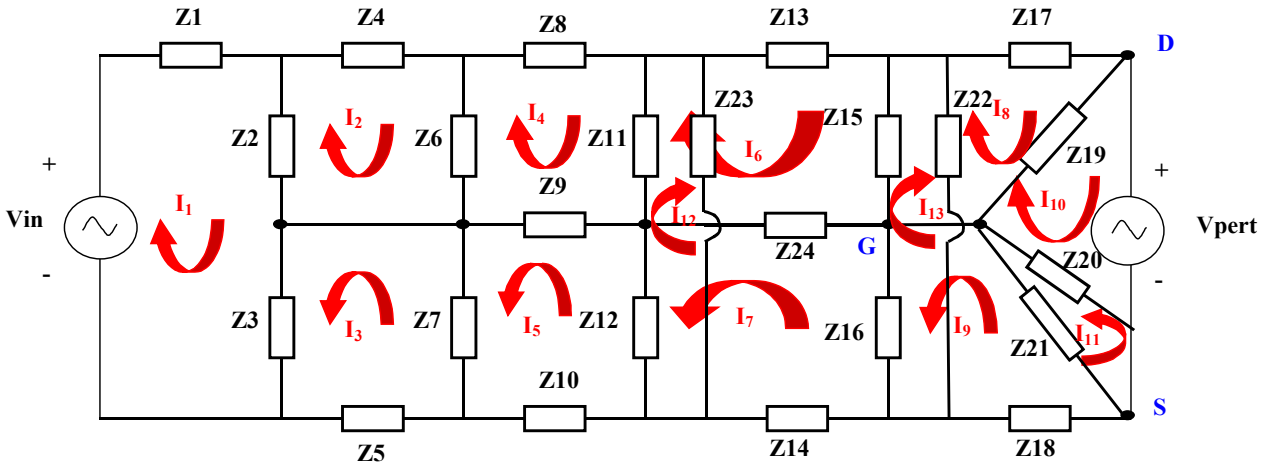

Figure 2.11. Equivalent impedance diagram of the whole system shown in Figure 2.9.

2.2.3.3. Design Process

The following design process can be performed using any of the available software tools ("Canalyze.m" and "Danalyze.m" functions implemented in MATLAB and the final OPES-PFC Boost Rectifier tool), which are described in Chapter 3 and in Appendix A, and which can be found in Appendix D.

First of all, it is important to highlight that the value of *Ldm* is dependent on the value of *Lcm*, since the former is a parasitic of the common mode choke. The *Ldm* has been assumed to be 3% of *Lcm* whenever experimental measurements of the leakage inductance were not available.

The design process can be outlined as follows:

1. Fix *Cy* to 10 nF (this is the maximum allowed value in order to limit the leakage current in the common mode capacitors). Assume some initial value for the common mode choke inductance (*Lcm*) and *Cx*.

2. The *Lcm* should be increased (if the common mode noise is above the standard) or decreased (if below the standard) until the common mode noise level reaches the limit minus 3 dB (equivalent to checking that the constraint related to common mode noise is equal to zero).

3. The *Cx* should be increased (if the differential mode noise is above the standard) or decreased (if below the standard) until the differential mode noise level reaches the limit minus 3 dB (equivalent to checking that the constraint related to differential mode noise is equal to zero).

2.2.3.3.1. Design Example

In this example, the specifications in Table 2.1 are considered. Certain components have been selected for the devices, and a certain design for the boost inductor.

Table 2.1. Specifications.

Magnitude	Value
P_{out}	1000 W
V_{out}	353 V
V_{in}	230 Vrms
Fs	40 kHz
Line inductance	200 µH

1. Initial guess: *Cy* = 10 nF; *Lcm* = 400 µH; *Cx* = 0.9 µF.

The results obtained are depicted in Figures 2.12 and 2.13. These results clearly show that this first guess is not so bad (it was chosen in order to shorten the iteration process presented here). However, both the common and differential mode levels are higher than the standard limits minus 3 dB. The total level therefore surpasses the standard limit.

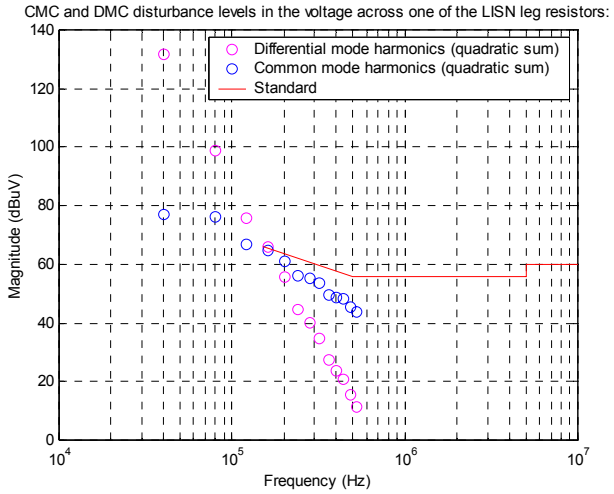

Figure 2.12. Differential and common mode disturbance levels in the voltage across resistor ZN.

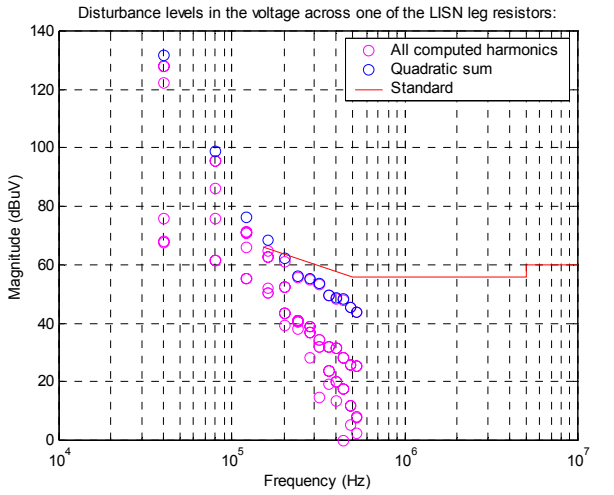

Figure 2.13. Total LISN EMI levels on resistor ZN.

2. Increase *Lcm* to 600 µH.

The results obtained are presented in Figures 2.14 and 2.15. It can be observed that both the common and differential mode levels are now at around the standard limit minus 3 dB. Figure 2.15 shows that the total EMI noise level meets the standard. Since the differential mode level is already at around the standard limit minus 3 dB, there is no need to proceed to step 3 in the design process, which would involve varying the *Cx* to adjust the differential mode level.

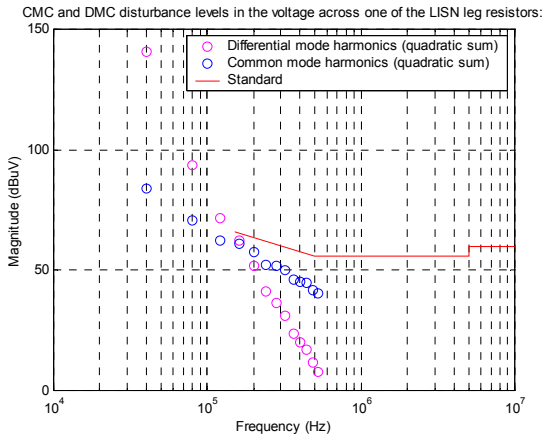

Figure 2.14. Differential and common mode disturbance levels in the voltage across resistor ZN.

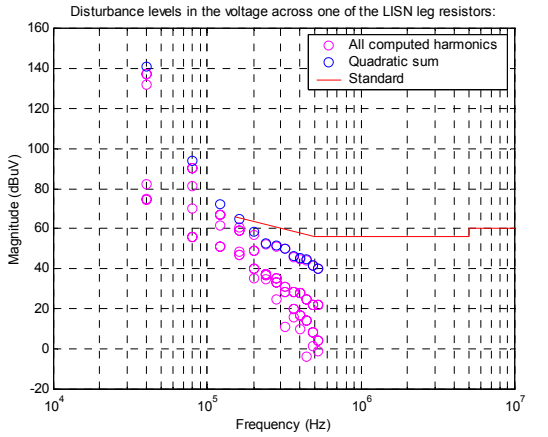

Figure 2.15. Total LISN EMI levels on resistor ZN.

2.2.3.4. Accuracy and Effectiveness of the System Model and Design Methodology Applied

It is difficult to accurately measure or estimate the system parasitics considered in the system model. This essentially implies the model's lack of accuracy in predicting the high-frequency (in the order of MHz) EMI levels. Due to the lack of accuracy in the parasitic estimation, it has been decided not to include the ringing in the model of the voltage across the commutation cell (see Figure 2.10). This ringing also affects the levels at high frequency, and is dependent on parasitic values. Therefore, the model does not provide an accurate estimation of the EMI levels at high frequencies. However, it is observed that, in general, the critical harmonics (those closer to the standard limits) that drive the design of the EMI filter are those centered at the first multiples of the switching frequency above the initial frequency for which the standards are defined (150 kHz). Consequently, a model that correctly predicts the levels at

these frequencies is, in most cases, sufficiently accurate. The modeling approach presented here has the capability of good accuracy at low frequencies. Of course, this accuracy is still dependent on the accuracy of the estimation of the parasitics (guidelines in the estimation of the main parasitics are presented in Sections 3.2.4.1.2 and 4.2.3 in a previous report [10]). This is especially critical in the case of the parasitic switch capacitance drain-to-ground (or collector-to-ground) with respect to the common mode EMI noise level. Special accuracy in the estimation of this parasitic should be pursued. If this is not possible, the design obtained by means of the design process presented will probably require some practical adjustments to tightly meet the standard levels.

The design process presented does not consider the possibility of system instability / high oscillations in the interconnection of the EMI filter and the boost PFC stage. This could occur whenever the magnitude of the output impedance of the filter is higher than the input impedance of the boost PFC stage. Should this instability / high oscillation occur, a higher value of some of the EMI filter components should be chosen in order to decrease the magnitude of the output impedance and to solve the instability / high oscillation problem. Further studies of this issue led to the conclusion that in PFC operation, instability is improbable (since the operating point is constantly varying), but that there could be significant oscillations that would imply the necessity for high current ratings in the filter components.

2.2.4. Magnetic Component Design[1]

2.2.4.1. Boost Inductor Design

Once the inductance and current ratings for the boost inductor are known, the next step is to select a core, a wire gauge and the number of turns in order to obtain a final design. A brief study (both analytical and experimental [10]) highlighted iron powder toroids as the most cost-effective choice for the core material and shape. The design process followed has been extracted from the corresponding catalog [16]. This process is described in the following subsection.

2.2.4.1.1. Design Procedure of Iron Powder Core Boost Inductors

1. Select core material permeability.

2. Compute the product of $0.5LI^2$ where: L = required inductance (μH) and I = peak value of the line frequency component of the current (A).

3. Locate the $0.5LI^2$ value on the catalog's energy storage table. Find the appropriate core size.

4. Read the nominal inductance rating, A_L, of this core size from the core data sheet.

5. From the permeability vs. energy storage curves, obtain the percentage of initial permeability, *pu*, at the energy storage.

6. Calculate the number of turns that yields the required inductance by means of the expression: $n = \sqrt{\frac{1000L}{A_L \cdot pu}}$.

7. Choose the appropriate wire size using a wire table.

This design procedure can be summarized as shown in the block diagram of Figure 2.16.

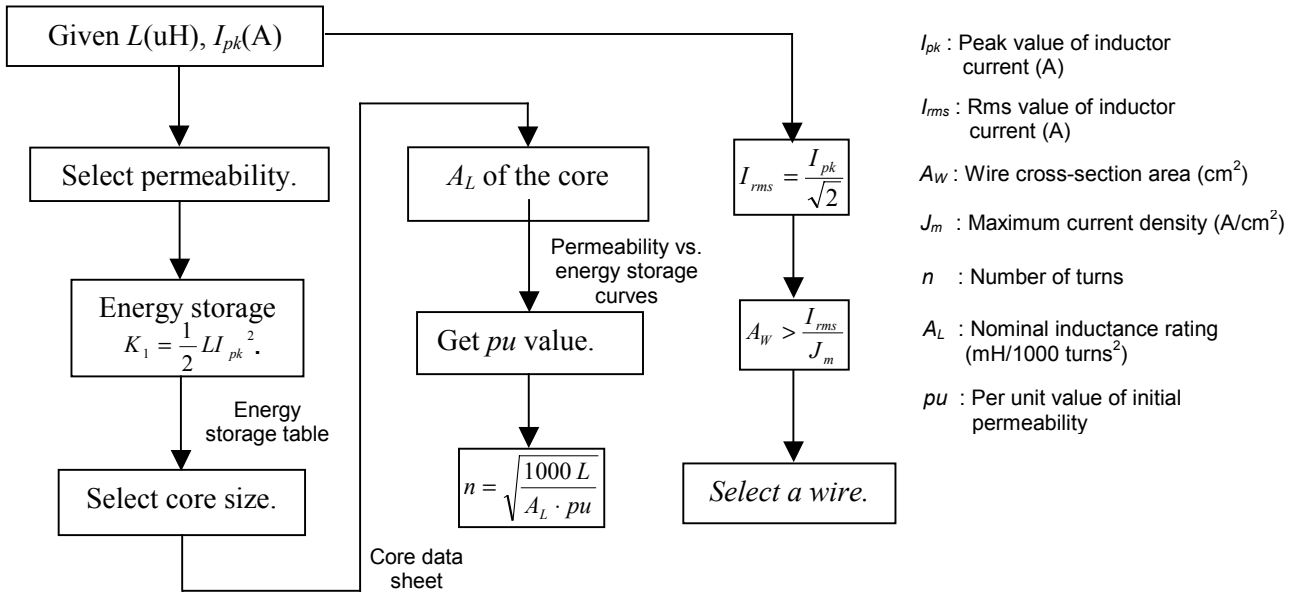

Figure 2.16. Design procedure of iron powder core boost inductors.

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[1] Work performed by Jia Wei

It is the understanding of the author that the previous design procedure leads to designs that will guarantee at least the specified inductance value over the range of operating currents, allowing a small percentage of saturation. In a PFC application, for which a precise inductance value is not required, this may lead to sub-optimal designs. Allowing a higher level of saturation to occur, even if this saturation is significant at high current levels, may generate less expensive overall system designs. This design improvement is usually achieved through experimental iterations.

2.2.4.2. Common Mode Choke Design

The design of the common mode choke is similar to that of a normal transformer with a turns ratio of 1:1. Ferrite toroid was selected as the most appropriate core material and shape for its implementation.

2.2.5. Design Results

Several values of the switching frequency and the maximum current ripple through the boost inductor have been considered in order to explore which is the optimum value range for these design variables. In the following, nine designs are presented. They all make the following assumptions:

- $T_{J(max)}$ of S = 100 °C (this value is an estimation of the junction temperature of the switch for a given external single heat sink design, such that its temperature is the maximum admissible (80 °C)).
- di/dt = 100 A/μs

These nine designs differ only in the choice of switching frequency (Fs) and the maximum current ripple across the inductor ($\Delta I_{LB(max)}$). Additionally, the designs for Fs=100 kHz and Fs = 70 kHz consider the use of a MOSFET for the implementation of the switch S, while the designs for Fs = 40 kHz and Fs = 30kHz consider the use of an IGBT. This is due to the fact that the IGBT presents lower conduction losses and higher switching losses than the MOSFET. Therefore, the former is more suitable for low switching frequencies, and the second for high switching frequencies.

Table 2.2. Total component cost for the different designs, expressed as the addition of the cost of the cores, capacitors, devices and heat sink.

***Fs* (kHz)**	**100**			**70**
ΔI_{LB}_max (%*Iinmax_pk*)	**45**	**30**	**15**	**30**
Cost* (%)	**90.7**	**93.2**	**100**	**84.1**

***Fs* (kHz)**	**40**			**30**	
ΔI_{LB}_max (%*Iinmax_pk*)	**45**	**30**	**15**	**45**	**30**
Cost* (%)	**70.5**	**71.83**	**80.5**	**68.4$^{\Delta}$**	**70$^{\Delta}$**

* This is the percentage with respect to the cost of the design at Fs = 100 kHz and ΔI_{LB}_max = 15 %.
$^{\Delta}$ Significant current oscilations in the EMI filter components were detected in these two designs.

The cost of the different heat sinks in monetary units (m.u.) has been approximated by the expression:

$$Cost\_Heat\ Sink = K_{HS} / Rth\_{HS}\ \text{(m.u.)},$$

where K_{HS} (m.u.*(°C/W)) was a constant, the determination of which was based on the cost of a typical heat sink.

Table 2.2 shows that the cheapest designs are obtained for a low switching frequency and a high boost inductor current ripple. However, designs with a significantly low switching frequency might present oscillations. The design at Fs = 40 kHz and ΔI_{LB}_max = 45 % (of *Iinmax_pk*) was finally selected for implementation.

2.2.5.1. Comments on the Results

From the results obtained for the nine designs investigated, the following observations can be made.

For a given current ripple through the boost inductor L_B, as the switching frequency decreases, the size of the boost inductance L_B increases. However, the differential part of the EMI filter (L_{DM}, C_X) and the comon mode choke (L_{CM}) decrease, and there is a decrease in losses

(lower cost of the heat sink) due to the reduced number of commutations in a line period, which suggests a possible tradeoff.

For a given switching frequency, as the desired current ripple through the boost inductor L_B increases, the size of the boost inductor is considerably reduced. Also, losses due to diode reverse recovery are reduced because current through the diode is lower during turn-on of the switch. However, the size of the differential part of the EMI filter increases, especially if the switching frequency is high, due to the fact that the EMI requirements are strict at high frequencies (if the switching frequency is low there is no significant increase in the size of the differential part of the EMI filter). On the other hand, as the current ripple increases, the copper losses in the boost inductor also increase, leading to higher boost inductor temperatures.

The boost inductor is designed based on a targeted value of the boost inductance. However, designs allowing more variation of the boost inductance value over half the line cycle (allowing more saturation to occur) might be less expensive overall.

In general, the conduction losses in an IGBT are lower than in a MOSFET, but the IGBT's switching losses are higher for the same switching frequency. MOSFETs are then more suitable for high switching frequencies, and IGBTs are more suitable for low ones. However, at intermediate switching frequencies, there is not a clear best choice; in this case the selection depends on the characteristics of the particular devices, their cost, and the cost of the heat sink per unit of power loss. On the other hand, the cheapest devices meeting the current and voltage ratings are not necessarily the optimum choice.

The optimum value of the switching frequency and boost inductor current ripple depends on the relative cost of the different elements integrating the converter, especially the boost inductor, the EMI filter components and the heat sink.

The conclusion from the information presented up to this point is that the best choice seems to keep the switching frequency as low as possible without producing significant oscillations. The optimum value of the boost inductor current ripple is not as easy to predict, and should be obtained considering the possible tradeoffs and the relative cost of the different components. This optimum value, however, seems to be relatively large.

2.3. Controller Design

The constant-frequency average-current-mode control for continuous-current-mode operation was chosen as the control strategy for the switch [17]. It was designed based upon information provided in the SGS-Thompson application note for the L4981A PFC control IC [11]. No feed-forward network was implemented to compensate for variations in the input line voltage.

2.4. Functionality

The functionality of the converter was evaluated through simulations and experiments [11]. SABER switching and average models were developed to perform the simulations. The operation of the circuit under normal conditions was verified.

Additionally, the converter operation was explored under other special conditions, according to the specifications. First, the operation of the system at input voltages in the range of 248-260 Vrms at different output loads was investigated. At these input voltages, the output voltage is less than the input line voltage during part of the line cycle. During these intervals, the converter operates as a rectifier, and the average output voltage reaches a higher level (the output voltage does not, however, reach the 375 V maximum). The rectifier behavior is caused by the fact that the voltage loop is saturated at its most negative value and consequently the switching stops. The converter resumes normal boost PFC operation during the entire line cycle once the input line voltage is reduced below the corresponding high line range (below 248 Vrms in the worst case).

Second and last, the correct operation of the system was also experimentally verified at the worst case North American line voltage range (100 Vrms) for a maximum power of 555 W, according to the corresponding specifications given in Section 1.3.

CHAPTER 3. CONVERTER DESIGN OPTIMIZATION

3.1. Introduction

The design results at the component level presented in Chapter 2 highlight the existence of several tradeoffs and possible room for improvement in the design of the power stage. To obtain the lowest-cost design that meets the specifications, the relative cost of all components in the design process must be taken into account together with these tradeoffs and considerations. Mathematical optimization techniques offer an organized and methodical way to reach this goal.

Initially, continuous optimization algorithms were applied to the design problem. Some of the design variables (such as the devices) were held constant and others (such as capacitances) were allowed to vary continuously. The objective of this effort was to acquire a better understanding of the tradeoffs involved in the design and to explore potential tradeoffs not previously identified [18].

After applying the continuous algorithms to the design problem, a genetic based discrete optimization algorithm (DARWIN) was applied to the design of the power stage. The discrete optimization algorithm is particularly appropriate for obtaining the globally optimum design. This algorithm operates directly on all the discrete variables, and there is no need to fix them or convert them to continuous variables. Software featuring a graphical user interface was developed to run the optimization code (OPES), and optimum designs were obtained for three sets of specifications. The results obtained are in accordance with the understanding of the problem acquired in the previous stage [19].

3.2. Continuous Optimization

In the continuous optimization approach for the component design of the system the output capacitor C_B and the average value of the output voltage (v_o) are fixed. This capacitor is fixed because the interaction of its design with the design of the rest of components is weak, and in case this component were introduced as a design variable and its interaction with the rest of the system were to be modeled, then a complex and computationally expensive transient should

be included in the analysis of each design in order to determine the minimum surge current that the devices need to withstand.

For the implementation of the common mode choke, it was decided to choose among commercially available designs, i.e., available discrete components.

The core shape (toroidal) and material of the boost inductor L_B represented in Figure 3.1 are fixed.

For the viability of the application of a continuous variable optimization approach, all devices (rectifier diodes D_R, fast diode D_F, and controlled switch S) are also fixed. The cheapest devices meeting the requirements of the system under study are chosen. In particular, for the controlled switch S, an IGBT with an external anti-parallel diode was selected. However, other analyses considering a MOSFET have been performed. It is possible to select either a single heat sink or separated heat sinks for all devices. In the optimization runs presented in this section, a single heat sink was selected.

The layout is also assumed fixed, and the corresponding parasitics are estimated for a more accurate prediction of the EMI levels.

3.2.1. Design Variables

The design variables in the continuous optimization approach are presented in Table 3.1.

Table 3.1. Continuous optimization design variables.

EMI filter	***Cx* (F)**	Differential mode capacitance
	***Cy* (F)**	Common mode capacitance
	***Lcm* (H)**	Common mode choke inductance
Boost inductor (See Figure 3.1)	***nturn***	Number of turns
	***Aw* (cm^2)**	Area of the wire copper
	***OD* (cm)**	Outside diameter of the core
	***ID* (cm)**	Inside diameter of the core
	***Ht* (cm)**	Height of the core

***Fs* (Hz)**	Switching frequency
***Rth_hs_amb* (°C/W)**	Thermal resistance of the single / switch* heat sink to the ambient

* A single heat sink or separated heat sinks for all devices can be considered. In the first case, the design variable corresponds to the thermal resistance of the single heat sink. In the second case, it corresponds to the thermal resistance of the switch heat sink.

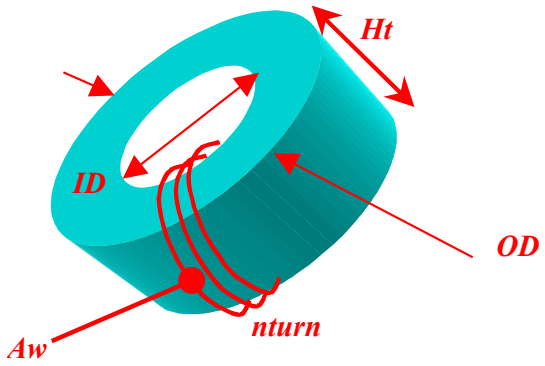


Figure 3.1. Boost inductor design variables.

3.2.2. Objective Function: Cost of the System

In an optimization problem, the design variable values that maximize or minimize a given objective function must be determined. In the case under discussion, this objective function is the cost of the system expressed as a function of the design variables (3.1). The goal is to obtain the set of design variable values that minimize this function.

$$Sys\_Cost = 2*Cost\_Cx + 2*Cost\_Cy + Cost\_Choke + Cost\_L_B\_core + \text{Cost\_}L_B\text{\_fixwiring} + Cost\_L_B\_varwiring + Cost\_HS + \text{Cost\_}S + \text{Cost\_}D_F + 4*\text{Cost\_}D_R + \text{Cost\_}C_B, \quad (3.1)$$

where *italics* denotes variable costs.

Given a set of components and their costs (see Appendix A), the cost of the different components expressed in m.u. as a function of the different design variables has been approximated in the following manner.

1. Cost of the differential mode capacitor:

$Cost\_Cx = \text{K1Cx} + \text{K2Cx}*Cx^2$,

where K1Cx, K2Cx = constants.

2. Cost of the common mode capacitor:

Cost_Cy=K1Cy+K2Cy**Cy*,

where K1Cy, K2Cy = constants.

3. Cost of the common mode choke:

Cost_Choke = K1Lcm+K2Lcm**Lcm*,

where K1Lcm, K2Lcm = constants.

4. Cost of the boost inductor core:

Cost_L$_B$_core = K1L_{Bc}+K2L_{Bc}**Vc*+K3L_{Bc}**Vc*^{2},

where K1L_{Bc}, K2L_{Bc}, K3L_{Bc} = constants, and *Vc* is the volume of the core expressed in cm^3.

5. Fixed manufacturing cost of the boost inductor:

Cost_L_B_fixwiring = constant.

6. Cost of the boost inductor wire and variable manufacturing cost:

Cost_L$_B$_varwiring = Cost_wpv**Aw***MLT***nturn*,

where Cost_wpv = constant (m.u./cm^3), and *MLT* is the mean length per turn of the core, expressed in cm.

7. Cost of the heat sink/s:

Cost_HS=K1HS+K2HS*(1/*Rth_hs_amb*),

where K1HS, K2HS = constants.

3.2.3. Constraints

The goal of the optimization procedure is to find the design variable values that minimize the objective function while satisfying all constraints. These constraints have been specified as follows.

- Geometrical constraints:

1. The internal diameter of the core must be smaller than the external diameter minus 0.5 cm.

2. The wire should fit in the available window area of the core, according to the maximum filling factor (Ku). The area occupied by the wire is assumed to be the area of a square with side length equal to the diameter of the wire.

- Temperature constraints:

3. The temperature of the boost inductor core should be lower than its maximum (determined as explained in Section 3.2.4).

4. The junction temperature of the switch should be lower than its maximum, as specified in the component data sheet (25 °C were subtracted from this maximum to be more conservative).

5. The junction temperature of the fast diode should be lower than its maximum, as specified in the component data sheet (25 °C were subtracted from this maximum to be more conservative).

6. The junction temperature of the rectifier diode (or rectifier bridge) should be lower than its maximum, as specified in the component data sheet (25 °C were subtracted from this maximum to be more conservative).

7. The temperature of the heat sink should be lower than its maximum. The maximum temperature of the heat sink is 80 °C in the case of an external heat sink, and 100 °C in the case of an internal heat sink.

- EMI constraints:

8. The differential mode disturbance level for the group of harmonics around the first multiple of the switching frequency above the minimum frequency at which the EMC standard limits are defined (150 kHz) should be lower than the standard level defined for its frequency minus 3 dB.

9. The common mode disturbance level for the group of harmonics around the first multiple of the switching frequency above the minimum frequency at which the EMC standard limits are defined should be lower than the standard level defined for its frequency minus 3 dB.

- Special constraints:

10. The maximum peak-to-peak current ripple in the boost inductor cannot be higher than 150 % of the peak average (in a switching period) boost inductor current. This constraint is set to limit the amount of time the converter operates in discontinuous current mode. The models used in the analysis are only valid for continuous current mode operation. If the computations were modified to be able to account also for the discontinuous current mode case, this constraint could be removed. However, in all runs performed this constraint was never active, which suggests that the continuous current mode operation is optimal for the problem analyzed.

11. The peak value of the flux density in the boost inductor core cannot exceed the maximum value defined for its material. This constraint can be removed if the saturation of the core is modeled in the analysis. In this case, this constraint will never be active. However, even though in the case under discussion the appropriate equations to model the saturation of the core are introduced, this constraint was retained in case new materials were considered for which the saturation models have not been not inserted in the analysis code.

12. The current density in the boost inductor wire cannot exceed the maximum current density outlined for copper. This constraint is also not needed when the copper losses in the boost inductor wire are computed and their effect on the boost inductor core temperature rise are considered. Again, this is the case under discussion, but the constraint was kept in the event that these models are removed.

- Boundaries for the design variables:

13. The minimum value of *ID*, *OD*, *Ht*, *Lcm*, *Cx*, and *Cy* is zero.

14. The minimum value of the number of turns is one.

15. The minimum bare area of the wire copper is $0.0202*10^{-3}$ cm^2 (corresponding to an AWG 44).

16. The minimum thermal resistance of the heat sink is 0.1 (value corresponding to a good water cooling system).

17. The lower boundary for the switching frequency is 20 kHz (audible range limit) and the upper boundary is 150 kHz (initial frequency for which the EMI standard limits are defined).

18. The capacitance of the common mode capacitor *Cy* should not exceed 10 nF due to the maximum leakage current allowed in the AC line for safety reasons.

All the constraints should be expressed in a normalized form (see equations in Appendix A, Section A.2.5).

3.2.4. Design Analysis Models and Assumptions

For computing the values of the various constraints as a function of the design variables, several models and assumptions have been applied. Here, the goal is to obtain a computationally efficient method of calculating the system responses, accurate enough to include all the important tradeoffs and fast enough to be able to perform a broad search of the design space in a reasonable period of time (optimization algorithms typically require that a large number of constraint evaluations be performed for different sets of design variable values).

Steady-state algebraic models for the worst-case operation were considered. The minimum input voltage and maximum average output voltage represent the worst case. The component tolerances are also taken into account in the degree desired so that anywhere from the most pessimistic to the most optimistic predictions can be obtained.

The models used for the estimation of the losses in the devices and the model to estimate the EMI levels have already been described and discussed in Sections 2.2.2.3.3, 2.2.3.2 and 2.2.3.4. The estimation of the temperature of the different devices and heat sink/s is performed through a simple static thermal lumped parameter model, in which the lost power flows through the corresponding thermal resistance and causes a temperature rise.

The models referring to the boost inductor are modified compared to the models discussed in Chapter 2. More detailed models are now taken into account. Second-order effects, such as the saturation of the boost inductor core as a function of the DC magnetizing force, AC flux density, boost inductor core temperature and switching frequency, have been included. This allows more degrees of freedom to optimize the design of the boost inductor. On the other hand, the skin and proximity effects have also been included. Losses in the wire and core are calculated

in order to predict the core temperature. This temperature is predicted by means of the following [20]:

$$TL_B\_core(^oC) = Tamb(^oC) + \boldsymbol{TLbcoef} \cdot \left[\frac{P\_coreLb(mW) + P\_copperLb(mW)}{Asurf(cm^2)} \right]^{0.833}, \qquad (3.2)$$

where

Tamb is the ambient temperature;

Tlbcoef is the correction coefficient for the estimation of the boost inductor core temperature;

P_coreLb is the power lost in the boost inductor core;

P_copperLb is the power lost in the boost inductor wire; and

Asurf is the surface area of the boost inductor.

This computation is especially important, since in Chapter 2 the core temperature was identified as a critical constraint. It is assumed that the temperature in all parts of the boost inductor is equal to the calculated temperature of the core. The coefficient *Tlbcoef* allows adjustments to be made in the predictions of different thermal scenarios (prototype exposed, prototype enclosed, use of a fan to cool down the boost inductor, etc…) and corrections to be made for the deficiencies of the models in predicting the boost inductor losses. This coefficient could have also been applied to modify the effective surface area of the boost inductor (in the equation, it could have directly multiplied *Asurf*). Several core materials are modeled: iron powder, high flux, molypermalloy, and kool Mμ. In the case of iron powder, the maximum core temperature has a limit based on reliability considerations (i.e., the thermal aging problem). Software provided by Micrometals [21] was used to obtain predictions of the lifetime of a core as a function of the initial core temperature and other factors such as the switching frequency (see Figure 3.2).

The maximum initial core temperature for which a lifetime of at least 20,000 hours was achieved was investigated. This was performed for each particular Micrometals iron powder core, by selecting a winding, a low switching frequency (worst case), and typical values for the other operating conditions, then varying the current flowing through the inductor until the

lifetime predicted was 20,000 hours (increasing the current increases the losses and therefore reduces the lifetime). Once this was obtained, from the plot of the core temperature as a function of the hours of operation (see example in Figure 3.2), the core temperature for zero hours of operation was estimated and registered as the maximum initial core temperature to guarantee a lifetime longer than 20,000 hours. The maximum temperature of the wire (to avoid damaging its coating) and the maximum temperature of the PCB were also considered. The minimum of these three values was set as the maximum core temperature in constraint number 3.

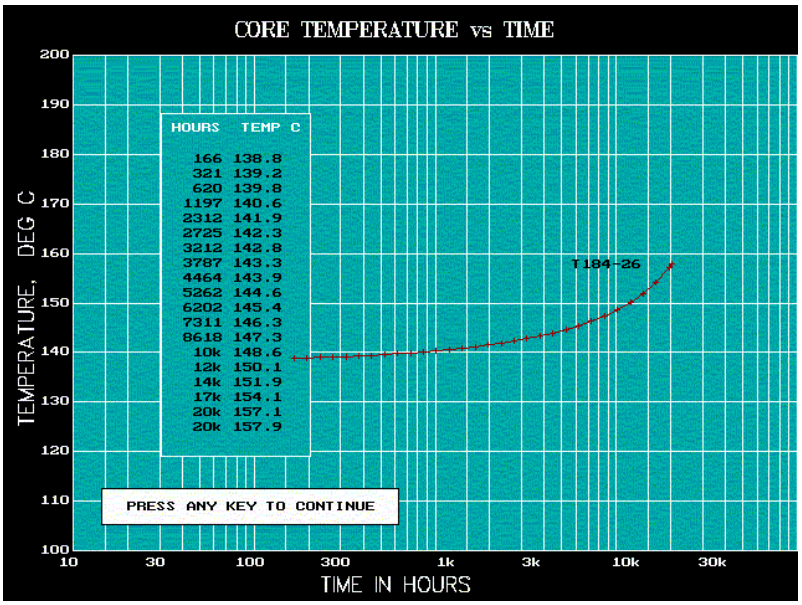


Figure 3.2. Core temperature as a function of the hours of operation for Micrometals T184-26 core. The life of the core is assumed to terminate after a certain temperature rise has been achieved.

All these models and assumptions, and the process followed to obtain the constraint values, are described in detail in Appendix A.

3.2.4.1. Calibration of the Models

3.2.4.1.1. Boost Inductor Core Temperature Prediction

The core temperature rise is dependent on the prototype thermal conditions. On the other hand, the predicted losses may not match the real ones, since the experimental data in which these predictions are based was obtained for a different operating condition (sinusoidal voltage applied to the core without any DC bias). The coefficient *Tlbcoef* allows the predictions of these

different thermal conditions and loss prediction errors to be adjusted. The value of this coefficient can be adjusted experimentally by means of the following two-step process.

1) *Tamb* determination: Run an experiment with a prototype. Measure the device's heat sink temperatures by using (for example) the thermocouples, as shown in Figure 3.3. Then, adjust the *Tamb* value in the model equations so that the model predictions for the device's heat sink temperatures match the measured values. The value of *Tamb* obtained will then represent the ambient temperature in the prototype environment to be used in Equation (3.2).

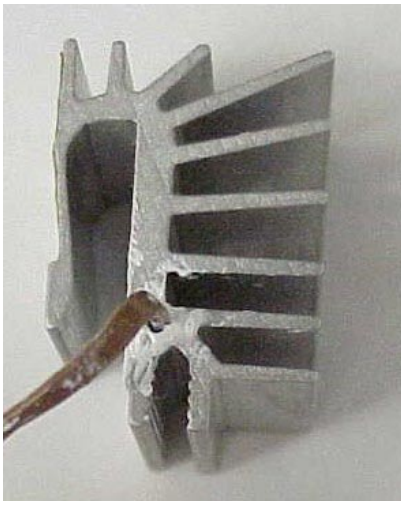


Figure 3.3. Thermocouple placement for the measurement of the device's heat sink temperature.

2) Adjust then *Tlbcoef* in Equation (3.2) so that the prediction using this equation matches the measured core temperature. This temperature can be measured by placing a thermocouple inside the winding near the core.

The value of *Tlbcoef* has been estimated to be 1.0 for a prototype with a fan cooling the boost inductor and 1.3 for a prototype without a fan cooling the boost inductor, as shown in Appendix B.

3.2.4.1.2. EMI Levels Prediction

To accurately ascertain the EMI levels, several parasitics need to be carefully measured or estimated. The most important parasitics are shown in Figure 3.4 and are described as follows.

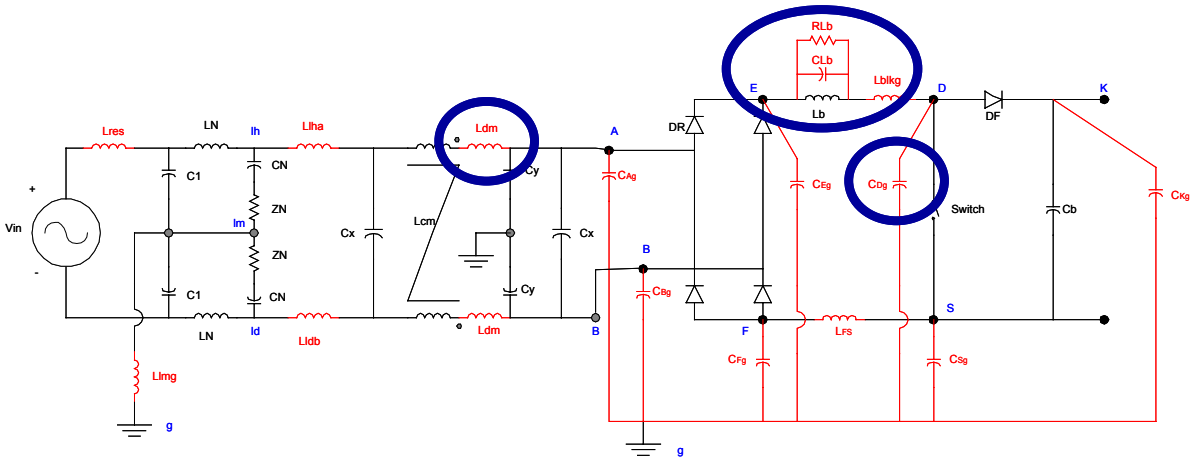


Figure 3.4. System topology including parasitics. Those circled are the parasitics to which the EMI levels are highly sensitive.

- From the common mode noise point of view:

    1. The switch drain / collector-to-ground parasitic capacitance:

    Two capacitances in parallel contribute to the total switch drain / collector-to-ground parasitic capacitance. These capacitances are shown in Figure 3.5 (C_{HM} and C_{CG}). They can be measured by means of a network analyzer selecting a series RLC configuration. The results for both capacitances are added to give the final estimation of the total switch drain / collector-to-ground parasitic capacitance. The common mode noise levels are significantly sensitive to the value of this parasitic. Therefore, an accurate estimation of its value is important. In one of the prototypes tested in Appendix B, the total collector-to-ground parasitic capacitance was 9 pF. In a second prototype it was 21.5 pF.

- From the differential mode noise point of view:

    2. The choke parasitic differential mode inductance: Figure 3.6 shows the setup required to measure the differential mode inductance of the common mode choke with a network analyzer. In the continuous optimization approach, the value of this parasitic has been assumed to be 0.2 % of the common mode inductance (*Lcm*), based on the differential mode inductance value measured for different common mode chokes.

    3. The boost inductor parasitics:

The parasitics considered in the boost inductor are those shown in Figure 3.4. The leakage inductance *Lblkg* is estimated by means of Equation (3.3), which is extracted from the manufacturer's catalog [22]:

$$Lblkg = \left(1 - \frac{TolLblkg}{100}\right) \cdot \left(292 \cdot nturn^{1.065} \cdot \frac{Ac}{lm \cdot 10^{8}}\right) \quad \text{(H)}, \tag{3.3}$$

where

TolLblkg is the tolerance in the value of the leakage inductance;

Nturn is the number of turns;

Ac is the cross-sectional area of the core (cm^2); and

Lm is the mean magnetic path length (cm).

The other two parasitics (*RLb* and *CLb*) are measured with the network analyzer, using the connection configuration shown in Figure 3.7.

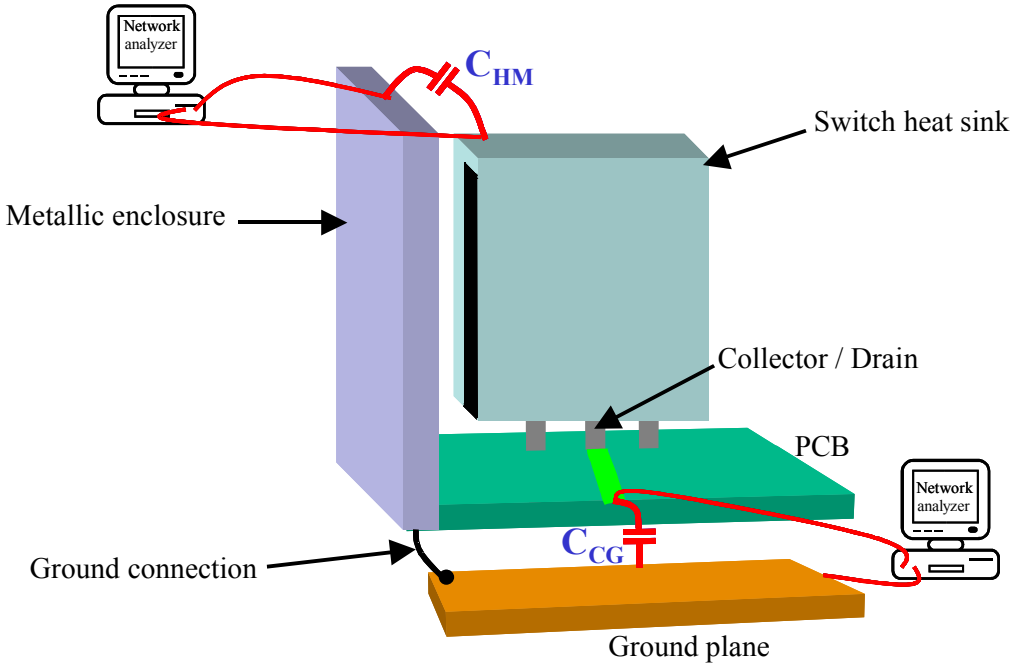


Figure 3.5. Measurement of switch drain / collector-to-ground parasitic capacitance.

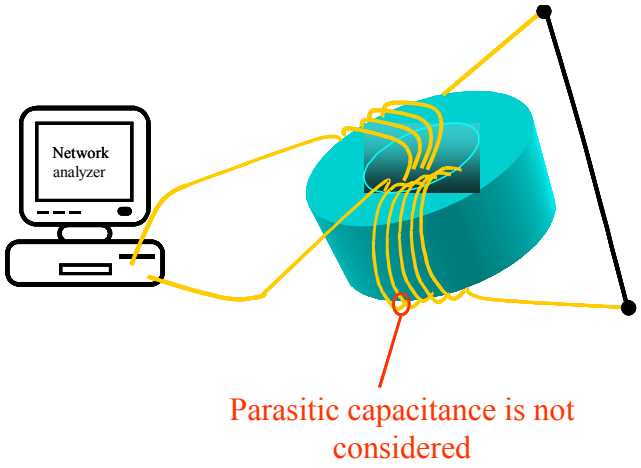


Figure 3.6. Measurement of the choke parasitic differential mode inductance.

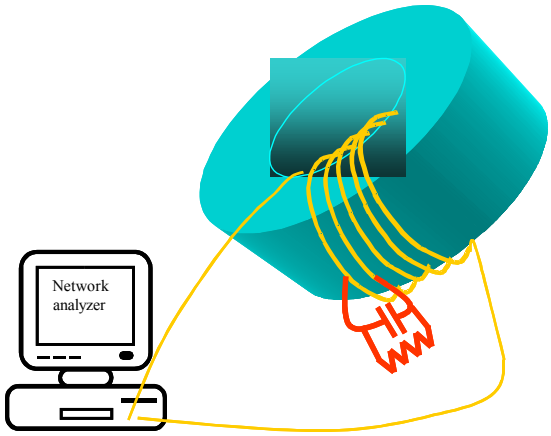


Figure 3.7. Measurement of the parasitics RLb and CLb in the boost inductor.

On the other hand, the EMI model used to estimate the EMI noise levels considers only a single value of the boost inductance over half the line cycle. Since saturation can occur, the boost inductance value varies over half the line cycle. Which value of the boost inductance should be considered in the models to estimate the EMI noise? The value of L_B in the range $L_{B\_min} \leq L_B \leq L_{B\_max}$ that better approximates a calibrating measurement will be selected. From the experience of the authors, the average value over the line cycle seems to be a good choice.

3.2.4.2. Experimental Validation

Once calibrated, the models were experimentally validated for different operating conditions. The details of the different experiments performed and the comparison between predicted and experimental results can be found in Appendix B.

3.2.5. Optimization Results

In the continuous optimization approach to the power stage design (single-phase boost PFC and EMI filter) one MATLAB function was developed: the "Canalyze(x)," available in Appendix D. This function performs the cost and electrical analysis of the system. The function receives as inputs a vector "x" (the so-called design variables) and gives as outputs the value of the cost function (the cost of the system in m.u.) and the values of the constraints defined for the problem. A summary of the specifications and additional performance information for a given set of design variables can be obtained by setting an internal variable in the program ("aff") to one.

The optimization results reported here correspond to optimization runs performed with a previous version of the MATLAB function "Canalyze(x)." In that version, the effect of the ac flux on the saturation of the core was not included. Therefore, the analysis program predicted a higher current ripple than would be expected. On the other hand, the skin and proximity effects were not included in the estimation of the losses in the boost inductor wire. This, together with the fact that the coefficient to estimate the temperature rise of the boost inductor core was too low for the conditions in which the converter operates, and that the ambient temperature was set to be 40 °C, implies that the temperature of the core predicted by the software was probably too optimistic. Finally, the fill factor was set to 0.3 and the maximum rms current through the boost inductor wire to 600 A/cm^2 (both values are too conservative). Since both corresponding constraints (wound area and maximum wire current density) were active (see

Table 3.3), these conservative values affected the result obtained for the optimum. However, even though the results obtained may not correspond to the real optimum desired, the conclusions reached are still valid since the version of the analysis function captured the essential behavior and tradeoffs of the system.

In these optimization runs, the fixed design variables were as follows.

1. Switch: IGBT + Anti-parallel diode
2. Bridge rectifier
3. Fast diode
4. Boost inductor core material: iron powder with a specific permeability
5. Boost capacitor: 100 μF, 450 V

Additionally, a single heat sink for all devices was considered.

The function "Canalyze(x)" was linked to a commercial optimization software code called VisualDOC (VMA Engineering) [23]. Both the Sequential Quadratic Programming [24] and Modified Method of Feasible Directions [24] algorithms were utilized in obtaining the present results. Constraint derivatives were computed using finite differences.

The optimization algorithms used for the present work belong to a class of optimization algorithms termed gradient-based methods. In order to begin the optimization process, these algorithms are typically provided with an initial design. Once an initial design is specified, gradients of the objective function and constraints are computed with respect to the design variables in order to compute a search direction in the design space. Next, the design space is searched along the computed direction so as to minimize the objective function while satisfying all the constraints. Gradients are then recomputed at the new design point, and the process continues until no further improvements are possible. If the design space contains several local minima, there is a possibility that a gradient-based optimizer may be trapped by a local minimum, and the answer will depend on the selection of the initial design point. In order to increase the probability of finding the point with the smallest objective function value (the global minimum), it is customary to execute the optimization algorithm from several different initial designs. In the present work, it was found that there were local minima in the design space, although in all cases studied, even the local minima were less expensive than the manual design. The results reported here correspond to the best design found during the course of the study and it is likely to be the globally optimum design.

In Table 3.2, the value of the design variables for a manual design and the design obtained by means of the optimization are presented. The cost of both designs is also specified. The manual design was obtained by initially fixing the value of the switching frequency to 40

kHz and choosing a commercial core, which seemed to be appropriate according to the results of the initial designs presented in Chapter 2 (these values correspond to one of the best designs reported). All the other design variables were adjusted manually with the aid of the developed MATLAB function, by assuming some initial value, checking the status of the constraints, and making the corrections needed in order to meet all constraints while minimizing the cost as much as possible (to design the EMI filter, the process detailed in Section 2.2.3.3 was applied).

Table 3.3 shows the statuses of the constraints for both the manual and optimized designs. A constraint is classified as active when the boundary specified on the design response is reached, inactive if the boundary specified is not reached and violated if the response value goes beyond the boundary.

Table 3.2. Design variable values and cost for the manual and optimum designs.

Design variable	**Manual design**	**Optimum design**
Cx (µF)	2.8	2.23
Cy (nF)	5	7.58
Lcm (mH)	1.50	0.97
nturn	122	88
Aw (cm^2)	$11.20*10^{-3}$	$11.41*10^{-3}$
OD (cm)	4.45	4.62
ID (cm)	2.72	2.33
Ht (cm)	1.65	1.62
Fs (kHz)	40	29.78
Rth_hs_amb (C/W)	2.20	2.38
Cost (%)[*]	100	90.7

[*] This is the percentage with respect to the manual design cost.

Table 3.3. Constraint statuses for the manual and optimum designs.

Constraint ref.	Manual design*	Optimum design*
1. ID-OD	I	I
2. W_A	A	A
3. T_core_Lb	I	A
4. Tjsw	I	I
5. Tjfd	I	I
6. Tjrd	I	I
7. Ths	A	A
8. DM	A	A
9. CM	A	I
10. dIL	I	I
11. Bpk	I	I
12. iL_rms	A	A
13-18. Bounds	I	I

* A denotes active constraint; I denotes inactive constraint.

3.2.6. Discussion

In the optimization runs performed, several tradeoffs and system behavior characteristics were identified. They are discussed next.

For a given *Fs,* there is a tradeoff among the design variables *Lcm*, *Cx* and boost inductor design variables, since all of them contribute to a reduction in the differential mode noise. The *Cy* also slightly affects the differential mode level. The relative cost-effectiveness of these components determines the optimum set of values that meet the constraint specified for the differential mode noise. Note that a variation in the design of the boost inductor would vary the optimum heat sink size due to the variation in the peak-to-peak current waveform that would in turn cause variations in the switching losses. Therefore, for the estimation of the cost-effectiveness of the boost inductor, the cost of the heat sink should be included.

Similarly, for a given *Fs*, there is also a tradeoff between *Lcm* and *Cy*, since both design variables contribute to the reduction of the common mode noise.

The selection of the optimum value of the switching frequency is not obvious. If the value of the switching frequency (*Fs*) is fixed, and the optimum design is obtained for a given set of different *Fs* values, the qualitative cost behavior sketched in Figure 3.10 could be observed for the EMI filter, heat sink and boost inductor.

The heat sink cost increases with an increase in the switching frequency, due to increased switching losses. The boost inductor cost increases as *Fs* decreases, due to an increase in the peak-to-peak current generating an increase in the copper loss and because of an increase in the core loss, both of which lead to an increase in the core temperature. Consequently, the inductance and / or inductor surface must increase to meet the constraint in the core temperature. The cost of the EMI filter depends essentially on the amplitude of the minimum-order harmonic (group of harmonics centered at multiples of the switching frequency) of Vpert (Figure 2.11, Section 2.2.3.2) that enters into the frequency range within which the standard limits are defined (150 kHz - 30 MHz). Figures 3.8 and 3.9 show the required attenuation for this harmonic as a function of the switching frequency, when all other design variables remain constant.

Typically, this minimum-order harmonic within the EMI range is placed between 150 kHz and 500 kHz, the range in which the standard limit has a slope of approximately 20 dB/dec. As *Fs* is increased, this harmonic moves towards a higher frequency at which the standard limit is lower. But since the attenuation of the EMI filter required is higher than 20 dB/dec, the resulting cost of the needed EMI filter is lower. The discontinuities in the EMI filter cost are due to the fact that, as *Fs* increases, new lower-order harmonics (with increasing amplitudes) enter into the frequency range within which the standard limits are defined. For instance, at *Fs* = 150 kHz / 7 = 21.43 kHz, the seventh harmonic needs to be limited to the standard level for 150 kHz. Similarly, for the sixth harmonic at *Fs* = 25 kHz, for the fifth harmonic at *Fs* = 30 kHz, and so on.

The minimum of the addition of the cost of the EMI filter, the heat sink, and the boost inductor as a function of the *Fs* determines the optimum value of this design variable. One of the most valuable results of this optimization is the identification of this minimum.

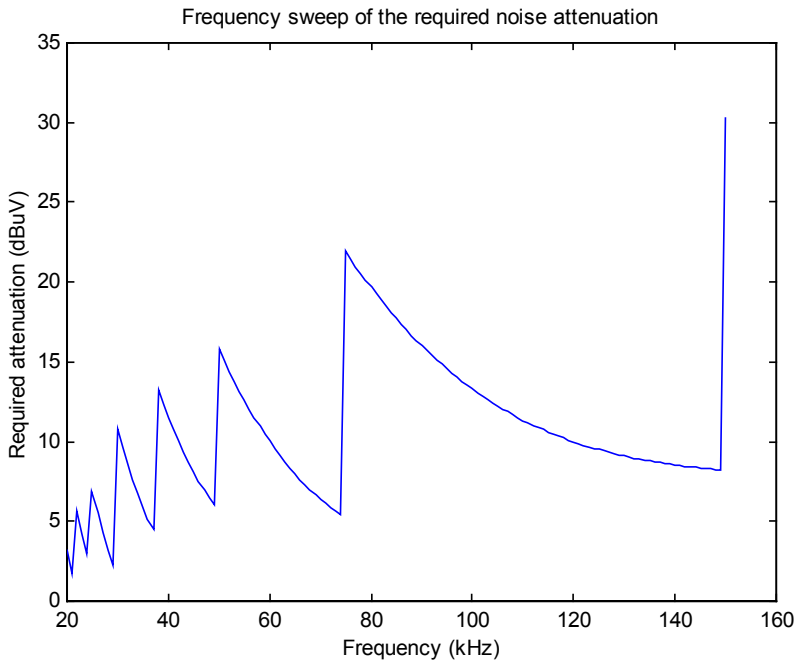


Figure 3.8. Required attenuation of the minimum-order harmonic EMI noise level as a function of the switching frequency.

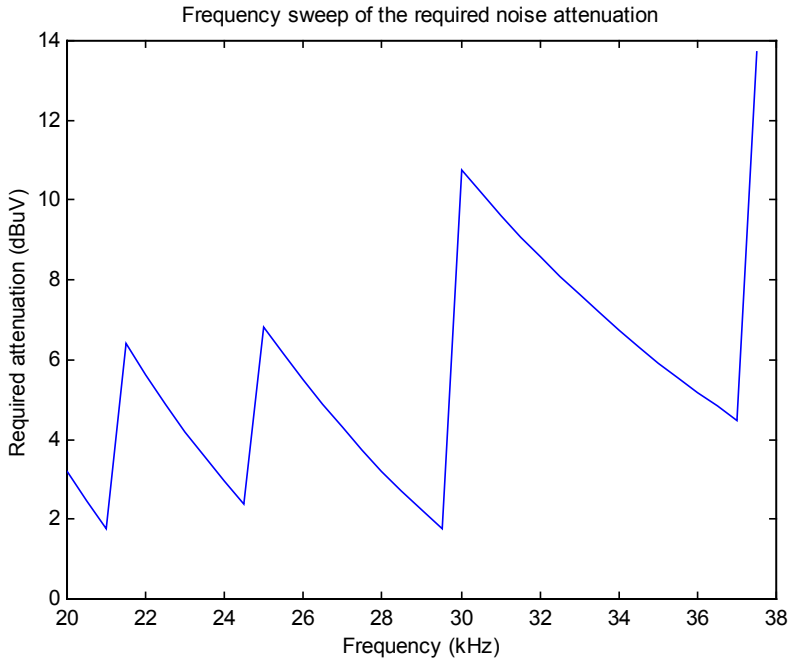


Figure 3.9. Required attenuation of the minimum-order harmonic EMI noise level as a function of the switching frequency (close-up view of low switching frequencies).

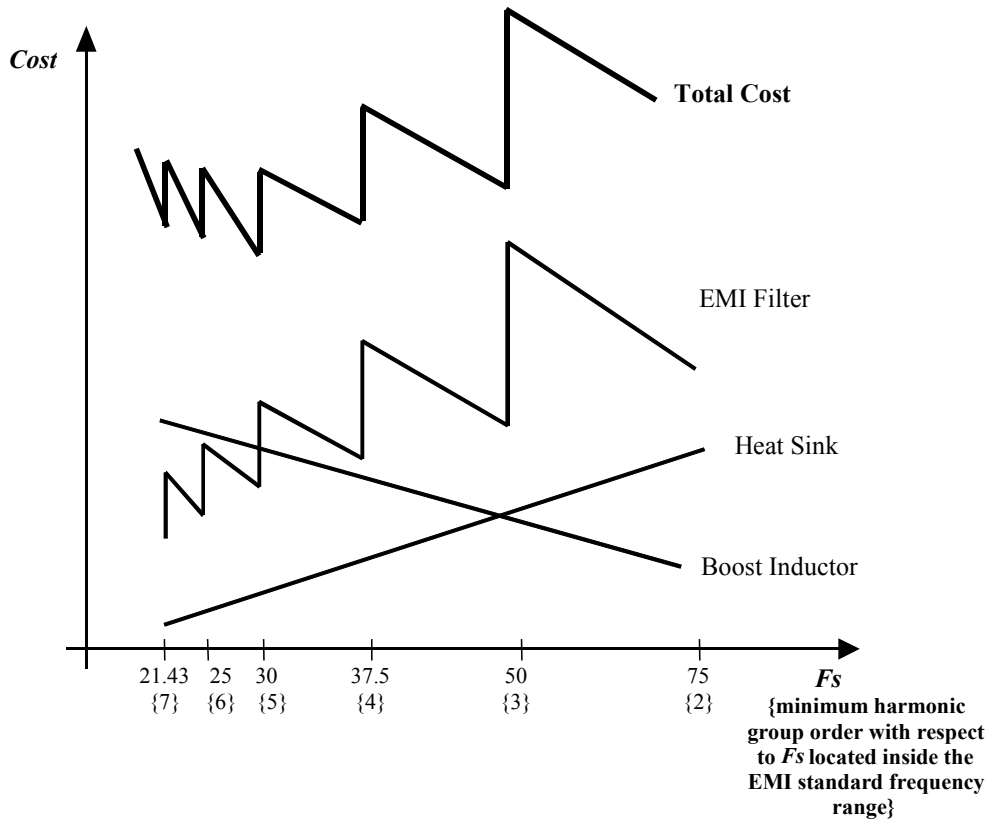


Figure 3.10. Qualitative description of the variation of the optimum design components' cost and total components' cost as a function of the switching frequency.*

* The sketch does not intend to reflect the relative cost of the three components.

In all optimization runs performed, the value of the switching frequency for the optimum design was located immediately below one of the switching frequencies at which a new harmonic entered into the range of frequencies defined by the standard; or, in other words, right before one of the corners of the cost curve for the EMI filter in Figure 3.10 (21 kHz, 24 kHz, 29 kHz, 37 kHz…). In the previous stage (Chapter 2), several manual designs were obtained for several values of the switching frequency. For instance, 30 kHz and 40 kHz were selected randomly. Figure 3.10 shows that this choice was sub-optimal, since both frequencies correspond to the peak region of the total cost. By means of the continuous optimization, an improved understanding of the system cost pattern as a function of the switching frequency was gained, which led to a reduction in the overall cost of the system.

3.3. Discrete Optimization

In the discrete optimization approach for the component design of the system, and as opposed to the continuous approach, all design variables are treated as discrete. This allows all the components in the power stage to be included as design variables. The only component that is fixed is the boost capacitor, for the reason already discussed in Section 3.2. The average value of the output voltage (v_o) is also fixed.

For the implementation of the common mode choke, it was decided to choose among commercially available designs.

The core shape of the boost inductor L_B is fixed to simplify the design problem. The toroidal core shape has been selected, since it appears to be the most cost-effective for this application. However, different core shapes could be considered by incorporating an additional design variable (core gap) and minor modifications into the graphical user interface and design analysis (see Section A.3.1 in Appendix A).

The layout is also assumed fixed, and the corresponding parasitics are estimated for a more accurate prediction of the EMI levels.

3.3.1. Design Variables

The design variables in the discrete optimization approach are presented in Table 3.4.

Table 3.4. Discrete optimization design variables.

EMI filter	Differential mode capacitor Cx
	Common mode capacitor Cy
	Common mode choke
Boost inductor	Core
	Wire
	Number of turns

Devices	Controlled switch
	Switching frequency (*Fs*)
	Bridge diode
	Fast diode
Thermal resistance of the single / switch* heat sink to the ambient (*Rth_hs_amb)*	

* A single heat sink or separated heat sinks for all devices can be considered. In the first case, the design variable corresponds to the thermal resistance of the single heat sink. In the second case, it corresponds to the thermal resistance of the switch heat sink.

Each design variable (controlled switch, bridge diode, etc… except for the heat sink thermal resistance, switching frequency and number of turns for the boost inductor) is defined by a set of parameters, which are specified in Appendix A. A database is then built by specifying the values of the parameters for each of the considered components.

The boost inductor's number of turns, the switching frequency, and the thermal resistance of the heat sink to the ambient are treated as discretized continuous variables that can have a value within a predefined range.

3.3.2. Objective Function: Cost of the System

In this case, each component contains a parameter that specifies its cost. Therefore, the total cost of the system can be computed as the simple addition of these individual costs:

$$Sys\_Cost = 2*Cost\_Cx + 2*Cost\_Cy + Cost\_Choke + Cost\_L_B\_core + \text{Cost\_L}_\text{B}\text{\_fixwiring} + Cost\_L_B\_varwiring + Cost\_HS + Cost\_S + Cost\_D_F + 4*Cost\_D_R + \text{Cost\_C}_\text{B}, \quad (3.4)$$

where *italics* denotes variable costs.

The only exceptions are for the estimation of the cost of the boost inductor wiring (which depends on the volume of wire used) and the estimation of the cost of the heat sink (treated as a discretized continuous variable). These costs expressed in m.u. are estimated as follows.

- Fixed manufacturing cost of the boost inductor:

$\text{Cost\_L}_\text{B}\text{\_fixwiring} = \text{constant}$.

- Cost of the boost inductor wire and variable manufacturing cost:

Cost_ L_B_varwiring = Cost_wpv**Aw***MLT***nturn*,

where Cost_wpv = constant (m.u./cm^3), and MLT is the mean length per turn of the core, expressed in cm.

- Cost of the heat sink/s:

The cost of the heat sink has been approximated by means of a polynomial function based on the cost information available (see Appendix A), as follows:

Cost_HS = K1HS + K2HS*(1/*Rth_hs_amb*),

where K1HS, K2HS = constants.

3.3.3. Constraints

The goal of the optimization procedure is to find the design variable values that minimize the objective function while satisfying all constraints. These constraints are specified as follows.

- Geometrical constraints:

1. The wire should fit in the available window area of the core, according to the maximum filling factor (Ku). The area occupied by the wire is considered to be the area of a square with side length equal to the diameter of the wire.

- Temperature constraints:

2. The temperature of the boost inductor core should be lower than its maximum.

3. The junction temperature of the switch should be lower than its maximum.

4. The junction temperature of the fast diode should be lower than its maximum.

5. The junction temperature of the rectifier diode (or rectifier bridge) should be lower than its maximum.

6. The temperature of the heat sink should be lower than its maximum.

- Voltage rating constraints:

7. The breakdown voltage of the MOSFET should exceed the minimum required breakdown voltage.

8. The breakdown voltage of the IGBT should exceed the minimum required breakdown voltage.

9. The breakdown voltage of the fast diode should exceed the minimum required breakdown voltage.

10. The breakdown voltage of the rectifier diode should exceed the minimum required breakdown voltage.

11. The ac voltage of the differential mode capacitor Cx should exceed the minimum required AC voltage.

12. The ac voltage of the common mode capacitor Cy should exceed the minimum required AC voltage.

- Current rating constraints:

13. The rms current in the MOSFET cannot exceed the maximum allowed rms current. This constraint is not needed if the corresponding maximum junction temperature constraint is considered (constraint 3). However, it was retained in order to monitor the current level compared to the maximum current level specified in the data sheet.

14. The average current in the IGBT cannot exceed the maximum allowed average current. This constraint is not needed if the corresponding maximum junction temperature constraint is considered (constraint 3). However, it was kept in order to monitor the current level compared to the maximum current level specified in the data sheet.

15. The average current in the fast diode cannot exceed the maximum allowed average current. This constraint is not needed if the corresponding maximum junction temperature constraint is considered (constraint 4). However, it was retained in order to monitor the current level compared to the maximum current level specified in the data sheet.

16. The average current in the rectifier diode cannot exceed the maximum allowed average current. This constraint is not needed if the corresponding maximum junction

temperature constraint is considered (constraint 5). However, it was kept in order to monitor the current level compared to the maximum current level specified in the data sheet.

17. The maximum surge current that the fast diode is able to withstand should exceed the maximum surge current determined for the system.

18. The maximum surge current that the rectifier diode is able to withstand should exceed the maximum surge current determined for the system.

19. The rms current in the common mode choke cannot exceed the maximum allowed rms current. Due to the lack of thermal models to estimate the common mode choke temperature, this constraint is set in order to indirectly take into account the limit on this temperature.

20. The rms current in the common and differential mode capacitors cannot exceed the maximum allowed rms current. Due to the lack of thermal models to estimate the capacitors's temperature, this constraint is set in order to indirectly take into account the limit on these temperatures.

- EMI constraints:

21. The differential mode disturbance level for each of the considered group of harmonics around a multiple of the switching frequency above the minimum frequency at which the EMC standard limits are defined should be lower than the standard level defined for its frequency minus 3 dB.

22. The common mode disturbance level for each of the considered group of harmonics around a multiple of the switching frequency above the minimum frequency at which the standard limits are defined should be lower than the standard level defined for its frequency minus 3 dB.

- Special constraints:

23. The maximum peak-to-peak current ripple in the boost inductor cannot be higher than 150% of the peak average (in a switching period) input current. This constraint is set in order to limit the amount of time the converter operates in discontinuous current mode. The models used in the analysis are only valid for continuous current mode operation. If the computations were modified to be able to account also for the discontinuous current mode case, this constraint could

be removed. However, in all runs performed this constraint was never active, which suggests that the continuous current mode operation is optimal for the problem analyzed.

24. The peak value of the flux density in the boost inductor core cannot exceed the maximum value defined for its material. This constraint can be removed if the saturation of the core is modeled in the analysis. In this case, this constraint will never be active. However, even though this work has introduced the appropriate equations to model the saturation of the core, the constraint was kept in case new materials were considered for which the saturation models has not been inserted in the analysis code.

25. The current density in the boost inductor wire cannot exceed the maximum current density for the copper. This constraint is also not needed when the copper losses in the boost inductor wire are computed and their effects on the boost inductor core temperature rise are considered. Again, this constraint was kept in the event that these proposed models are removed, but is unnecessary for the case under discussion.

- Boundaries for the continuous design variables:

26. The minimum value of the number of turns is one.

27. The minimum thermal resistance of the heat sink is 0.1 (value corresponding to a good water cooling system).

27. The lower boundary for the switching frequency is 20 kHz (audible range limit), and the upper boundary is 150 kHz.

These constraints should all be expressed in a normalized form (see equations in Appendix A, Section A.2.5).

Note that constraints 7-12, 17 and 18 are simply boundaries for some of the design variable parameters. Therefore, they can initially be computed for all components in the database in order to discard those not meeting the requirements.

To compute the value of all other constraints as a function of the design variables, several models and assumptions have been applied. These models and assumptions and the process

followed to obtain the constraint values are discussed in Section 3.2.4, and can also be found in detail in Appendix A.

3.3.4. Optimization Algorithm: DARWIN

3.3.4.1. Introduction

DARWIN is an advanced genetic algorithm (GA) optimization code developed by ADOPTECH, Inc. that has been tailored specifically for engineering system design. GAs are one of the few optimization algorithms that work directly with discrete design variables. GAs are also excellent all-purpose discrete optimization algorithms because they can handle non-linear and noisy search spaces by using objective function information only. Compared to traditional gradient-based optimizers, genetic optimizers are more likely to find the overall best (globally optimal) design. In addition to finding the overall best design, GAs are also capable of finding many near-optimal designs as well, providing the user with many options when selecting a final design configuration.

3.3.4.2. Genetic Algorithm Theory

Genetic algorithms use techniques derived from biology and rely on the application of Darwin's principle of survival of the fittest. When a population of biological individuals is allowed to evolve over generations, individual characteristics that are useful for survival tend to be passed on to future generations, because individuals carrying them get more chances to breed. In biological populations, these characteristics are stored in genetic strings. The mechanics of natural genetics are based on operations that result in a structured yet randomized exchange of genetic information between the genetic strings of reproducing parents. These operations consist of reproduction, crossover, and occasional mutation of the genetic strings. Genetic algorithms, developed by Holland [25], mimic the mechanics of natural genetics for artificial systems based on operations that are the counterpart of their natural ones. Although these operations may appear as a completely random search of the design space, genetic algorithms have been experimentally proven to be robust searching algorithms (see Goldberg [26]).

3.3.4.2.1. GA Coding

Applying a genetic algorithm to a search problem first requires the representation of the possible combinations of the variables in terms of integer or real valued strings, which are the counterparts of genetic strings found in nature. Typically, genes are coded using a binary alphabet showing whether a gene is active (represented by a 1) or inactive (represented by a 0). However, for the PFC boost rectifier – EMI filter design problem, each gene in the genetic string is used to model a single electrical component, and thus is given its own alphabet of integer values. This is because the number of possible choices for each component will likely be different. For example, if the first gene in the genetic string is used to represent the specific fast diode used in the system and there are 15 different fast diodes in the database, then the alphabet for the first gene will contain 15 integer values ranging from 1 to 15. The second gene may be used to represent the bridge diode for which there are eight different types. Therefore, the alphabet for the second gene would contain eight integer values ranging from 1 to 8. The continuous variables required by the PFC boost rectifier – EMI filter design problem are modeled directly in a separate real-value genetic string and do not require encoding.

3.3.4.2.2. GA procedure

The GA procedure starts by selecting an initial population of randomly chosen strings, each of which represents a design. For the PFC boost rectifier – EMI filter design problem, each design consists of a string of integers representing all of the electrical components as well as a string of real values representing the switching frequency, number of wire turns in the inductor core, and the thermal resistance of the heat sink. The size of the population remains constant throughout the genetic optimization, although the members of the population evolve over time. In order to form successive generations, parents are chosen from the current population based on their performance (designs with the best performance are given the highest probability of being selected as parents). After parents have been selected, genetic operators (see Section 3.3.4.2.3) are applied to create children. Depending on the selection procedure that is used to determine the next population of designs, selected child designs will replace their parents in the next generation (see Section 3.3.4.2.4). One generation after another is created until some convergence criterion is met. DARWIN is currently configured to run for whatever fixed number of generations is set by the user. A schematic of the GA procedure is given in Figure 3.11.

3.3.4.2.3. Genetic Operators

Each genetic operator is implemented with its own specific probability *P*. To determine whether an operator will be implemented, a uniformly distributed random number is selected and compared against the operator's probability. If the random number is smaller than *P*, the operator is applied to the genetic string.

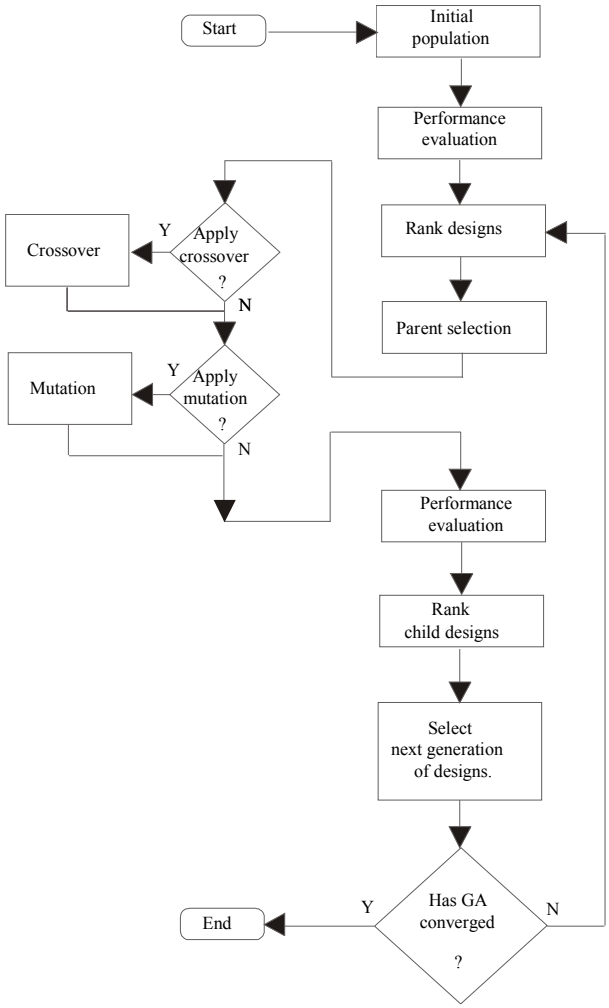


Figure 3.11. Genetic algorithm procedure.

3.3.4.2.3.1. Crossover

Child designs are created by combining a portion of each parent's genetic string in an operation called crossover. DARWIN utilizes the uniform crossover procedure, which is implemented by drawing a uniformly distributed random number for each gene in the genetic string. If the random number is less than 0.5, then the first gene in parent 1 is given to child 1 and

the first gene in parent 2 is given to child 2. If the random number is greater than or equal to 0.5, then child 1 receives a gene from parent 2 and child 2 receives a gene from parent 1. This process is repeated until two new child designs are created. DARWIN also utilizes a separate crossover operator that has been specially designed to work with continuous variables.

In general, all crossover operators are typically applied with a high probability ($0.8 \leq P_c \leq 1.0$) because they are the GA's primary means of traversing the design space. However, if crossover is not applied, then the parent strings are cloned into the child strings. Child strings are also forced to be distinct from each other. If a distinct child cannot be found after a prescribed number of iterations, then one of the parents is cloned into the child population. The crossover process is repeated as many times as necessary to create a new population of designs.

3.3.4.2.3.2. Mutation

Mutation performs the valuable task of preventing premature loss of important genetic information by occasionally introducing random alterations in the string. Mutation is also needed in case all of the possible values for each gene are not represented in the initial population. Mutation is almost always applied with a low probability ($0.01 \leq P_m \leq 0.1$), and is implemented by changing, at random, a single value in the string to any other permissible value. As with crossover, DARWIN also has an additional mutation operator that has been specially designed to work with continuous variables.

3.3.4.2.4. Selection

The GA's selection scheme is the mechanism that determines which designs from the parent population and newly created child population will be chosen to make up the next generation of designs. DARWIN utilizes elitist selection, where the child population and parent population are ranked separately. The best converter from the parent population and the worst converter from the child population are identified. To create the new population, the best design from the parent population replaces the worst design from the child population. The elitist method provides an explorative genetic search, since each successive population is provided with a large number of new designs.

3.3.5. Software Tool: OPES

In the discrete optimization approach for the component design of the system one MATLAB function was developed: "Danalyze," described in Appendix D. As in the continuous case, this function performs the cost and electrical analysis of the system. It receives as inputs the values of the design variables, and provides as outputs the cost of the system in m.u. and the value of the various constraints considered. Additional performance information for these given values of the design variables can be obtained by setting an internal variable in the program ("aff") to one. This function was then translated into FORTRAN ("pfcbr_analysis.f90") and tied to a GA (DARWIN) in order to perform the optimization. The optimization process is controlled by means of a graphical user interface (developed by ADOPTECH, Inc., in JAVA), which not only allows the execution and monitoring of the optimization process, but also provides a user-friendly environment for the management of the conditions / specifications and component database considered in the optimization, and provides detailed electrical performance information for any design desired. A demo version of the previous software, termed OPES (Optimization of Power Electronics Systems), is included in Appendix D. The main features of the software tool are described in the following sections.

3.3.5.1. Definitions of Specifications and Conditions

Figure 3.12 shows the windows available for defining the specifications and conditions for which we desire to obtain the optimum design. These conditions are classified into three categories: general, boost PFC stage and EMI filter. They contain a wide variety of parameters that can be specified, such as the output power level, input and output voltages, and the values of the different layout parasitics according to the layout selected. The user can also select the EMI standard to be considered, whether a single heat sink for all devices or separated heat sinks should be used, and how conservative the design analysis results should be.

3.3.5.2. Component Databases

The software tool also allows the user to manage the component databases that will be used in the optimization process (see example in Figure 3.13). Component databases for the EMI filter capacitors, common mode choke, switch (IGBT and MOSFET), fast diodes, bridge diodes, cores and wires have been created. The user can update and organize these databases as required.

The optimization process only considers those components selected by the user. This provides flexibility, and allows the user to perform a variety of design studies.

The user can also set the upper and lower bounds for each continuous design variable.

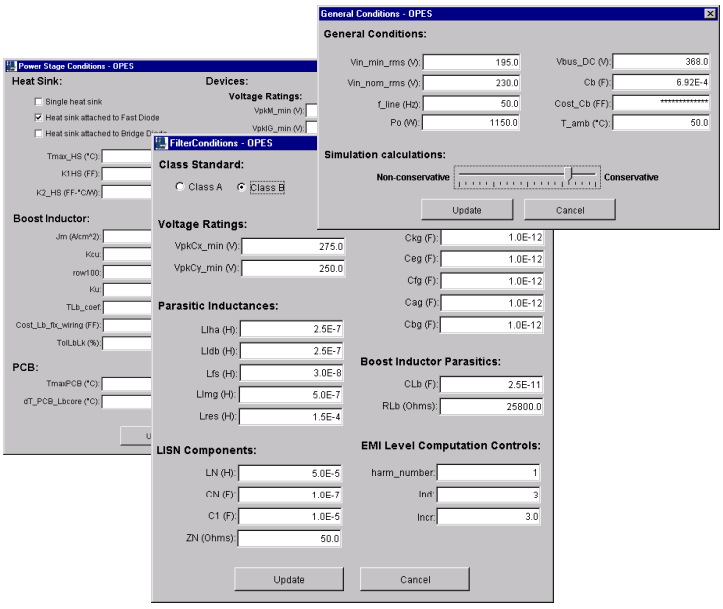


Figure 3.12. Specifications and conditions.

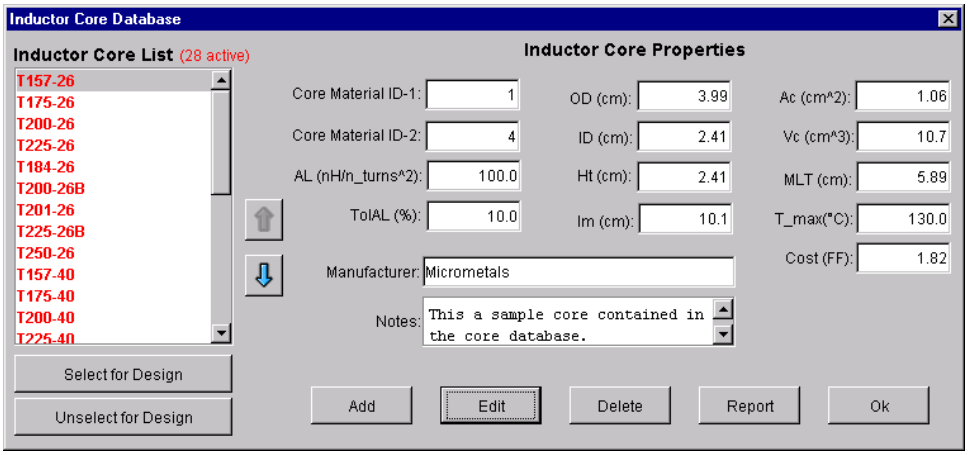


Figure 3.13. Inductor core database.

3.3.5.3. Control and Monitoring of the Optimization Process

Once the conditions and component databases have been loaded, the optimization process to find the combination of components and continuous variables that yields the cheapest design without violating any of the constraints can be controlled and monitored from the main window

shown in Figure 3.14. The optimization process population size and the number of generations must first be selected. A specified number of the best designs found by the optimizer can be displayed at any time during the optimization process. The percentage of optimization process completed is also displayed.

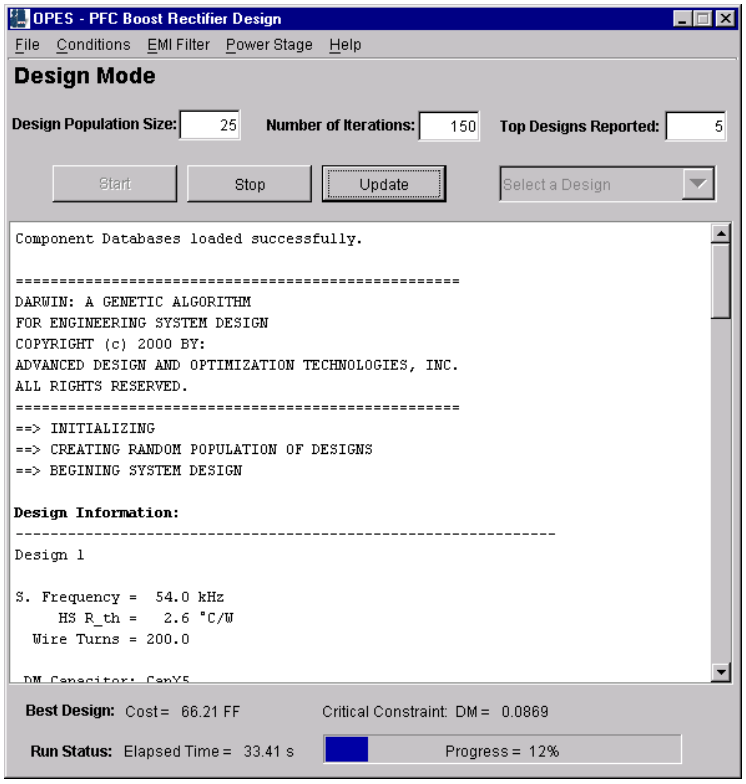


Figure 3.14. Main window.

3.3.5.4. Design Reports

After the optimization process is completed, a report can be generated that details each of the best designs found. This design report includes a detailed cost breakdown of the design, statuses of the different constraints, electrical performance information (general and specific for each component), and a set of plots containing information on the EMI levels, boost inductor current, boost capacitor voltage and duty-ratio waveforms. Figure 3.15 shows some of the windows containing this information.

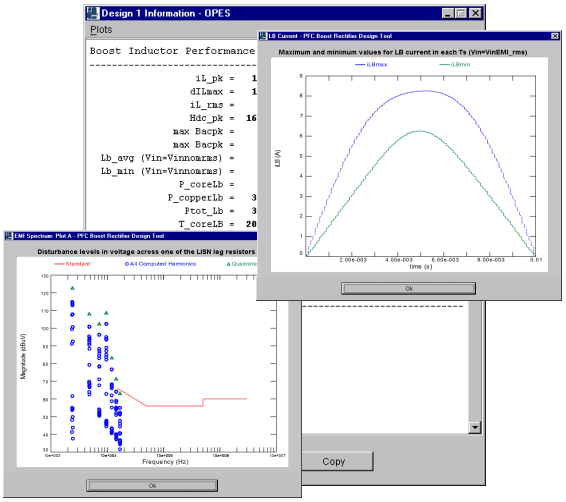


Figure 3.15. Design report information.

3.3.5.5. Single Design Analysis

Additionally, the software allows the designer to examine the response of any specified design by selecting the Single Design Analysis Mode (Figure 3.16). This mode is especially useful for tuning some of the parameters contained in the operating conditions window, as the predicted performance can be compared to the experimental results obtained from a prototype. It can also be used for educational purposes, allowing exploration of changes in the system cost and performance as a function of certain design parameters.

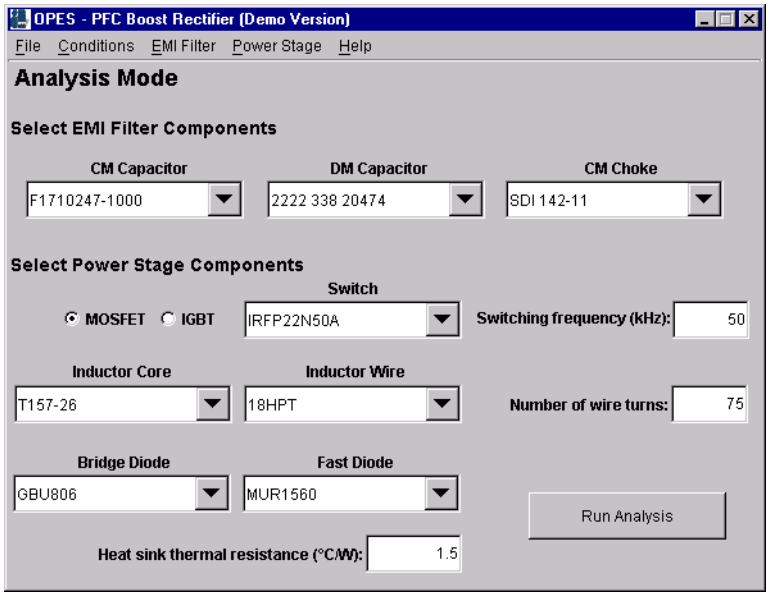


Figure 3.16. Single Design Analysis Mode.

3.3.5.6. Online Help

Online help to operate the software is available from the menu bar, and local help buttons exist in the particular windows.

3.3.6. Results

It was decided to investigate (using OPES) the optimum design for the following cases:

A) Optimum A

min Vin = 180 Vrms (except for EMI levels, checked at 230 Vrms).

B) Optimum B

min Vin = 195 Vrms (except for EMI levels, checked at 230 Vrms).

C) Optimum C

min Vin = 230 Vrms

All three optimums have been obtained assuming separated heat sinks. The bridge rectifier has been considered to be attached to the box, and it has been assumed that the box has a thermal resistance low enough to avoid over temperatures in it and in the bridge rectifier. Therefore, the design costs presented include only the cost of the switch and fast diode heat sinks.

Appendix C contains detailed information on the conditions / specifications and the size of the component database in the software used to obtain these optimums.

A two-step process has been followed to obtain the optimums, as follows.

1. First, a search of the optimum set of discrete design variables (all except for the switching frequency, the number of turns, and the thermal resistance) has been performed. For this, it is necessary to run the optimization several times and to check that almost all optimizations lead to the same set of optimum discrete components. On the other hand, in any optimization run, it is interesting to apply the smallest possible value of the “design population size” and “number of iterations” parameters in order to reduce the time required to complete the optimization process. In the runs presented here, and for the database size considered, a design

population size of 100 and a number of iterations of 500 have proven to be fairly low values, guaranteeing convergence of the discrete design variables.

2. Second, by fixing the set of optimum discrete design variables found previously (this is done by simply unselecting all the other possible components in the database), a search of the optimum values of the continuous variables (switching frequency, number of turns and thermal resistance) is performed. Again, it is necessary to run the optimization several times and to check that almost all optimizations lead to approximately the same values of the continuous design variables. In the runs presented here, and for the continuous design variable value ranges considered, a design population size of 25 and a number of iterations of 500 have proven to be fairly low values, guaranteeing convergence of the continuous design variables.

In Table 3.5, the switching frequency and average boost inductance of the optimum designs A, B and C are presented. In Table 3.6, the costs of the EMI filter, boost PFC and total cost in the conditions A, B and C are presented. The costs are expressed as a percentage of the cost estimated by the software for the selected design at Fs = 40 kHz in the initial design stage (Chapter 2) following traditional design procedures. This design meets the specifications in the conditions of the optimums B and C, but at a *min Vin* = 180 Vrms (conditions of optimum A), the temperature of the boost inductor core is too high. It can be seen that as the minimum input voltage increases, the total cost of the optimum design decreases. In these three optimums, the EMI filter is the same. Only the boost PFC design differs. In Table 3.7, the costs of the different components integrating the boost PFC stage are presented. The selection of the devices and boost output capacitor is the same for the three optimum designs. In optimum B, the same core as in optimum A is considered, but a reduction in the cost of the wiring (due to a choice of a smaller wire gage and number of turns) is experimented. The cost of the heat sinks, especially the switch heat sink, is also reduced compared to optimum A. In optimum C, a cheaper core is selected compared to optimum B. Additional savings are obtained in the heat sink, especially in the switch heat sink.

Table 3.5. Switching frequency and average boost inductance for optimum designs A, B and C.

Optimum design	A	B	C
Switching frequency (kHz)	21	24	24
Average boost inductance[*] (mH)	1.54	1.41	1.33

[*] At *Vin* = 230 Vrms

Table 3.6. EMI filter, boost PFC, and total cost for optimum designs A, B and C.

Optimum design	A	B	C
EMI filter cost (%)[*]	13.3	13.3	13.3
Boost PFC cost (%)[*]	77.5	75.3	70
Total cost (%)[*]	**90.8**	**88.6**	**83.3**

[*] Percentage with respect to the cost of the chosen design at Fs = 40 kHz in Chapter 2.

Table 3.7. Boost PFC components' cost for optimum designs A, B and C.

Optimum design	A	B	C
Devices + C_B cost (%)[*]	35.6	35.6	35.6
Core cost (%)[*]	10.0	10.0	5.8
Wiring cost (%)[*]	32.7	30.6	30.5
Heat sinks cost (%)[*]	7.0	6.7	5.2

[*] Percentage with respect to the cost of the chosen design at Fs = 40 kHz in Chapter 2.

In Table 3.8, the value of different constraints is specified for the three optimum designs. This value represents the per unit value of the distance between the response variable of the system and the corresponding limit. For example, in the case of the constraint related to the maximum temperature of the heat sink, the constraint value is defined as:

$$Cstr\_T_{HS} = \frac{T_{HS\max} - T_{HS}}{T_{HS\max}}, \tag{3.5}$$

where T_{HS} is the heat sink temperature, and T_{HSmax} is the maximum temperature of the heat sink.

Table 3.8. Different constraint values of the optimum designs A, B and C.

Optimum design		A	B	C
Constraints*	1. *Cstr_W_A* (p.u.)	-0.2749	-0.4423	-0.2580
	2. *Cstr_T_core_L_B* (p.u.)	**-0.0014**	**-0.0024**	**-0.0055**
	6. *Cstr_T_{HS}* (p.u.)	**-0.0023**	**-0.0096**	**-0.0050**
	21. *Cstr_DM* (p.u.)	**-0.0270**	**0.0030**	**-0.0237**
	22. *Cstr_CM* (p.u.)	-0.1294	-0.1123	-0.1392

* Bold denotes active constraints.

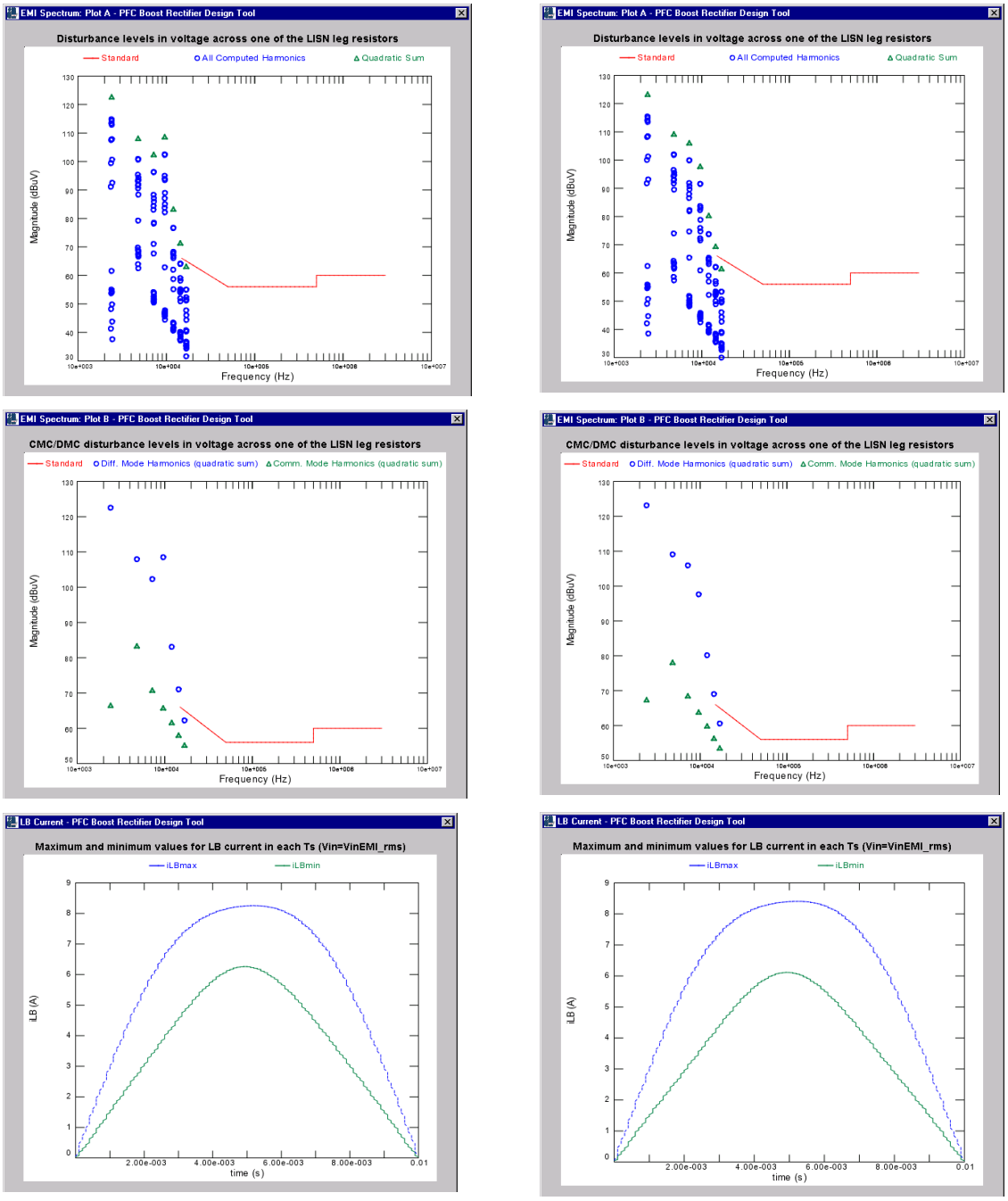
A negative value of the constraint indicates that the limit has not been trespassed (inactive constraint), a zero value indicates that the limit has been reached (active constraint), and a positive value indicates that the limit has been trespassed (violated constraint).

In all three designs, the constraint related to the maximum temperature in the boost inductor core (2. *Cstr_T_core_L_B*), the maximum temperature in the switch heat sink (6. *Cstr_T_{HS}*), and the limit in the differential mode noise (21. *Cstr_DM*) are the active constraints. All other constraints are inactive. In particular, the constraint related to the maximum amount of wire turns that can fit in the available window area (1. *Cstr_W_A*) is not active with a wide margin. This is because if the smaller (and cheaper, in this case) cores are used, either the number of wire turns needed to maintain the core temperature below the limit does not fit in the available window area or the amount of wire required is so large that the overall cost of the boost inductor is slightly higher.

Another inactive constraint is that related to the limit in the common mode noise (22.*Cstr_ CM*). This constraint is not active because the smaller common mode capacitor in the database is selected and there is a common mode choke in the database with a common mode inductance higher than required but cheaper than the common mode chokes with lower common mode inductance.

It is interesting to note that the value of constraint *Cstr_DM* is lower in optimum C than in optimum B, in spite of both designs having the same switching frequency and EMI filter, and the average boost inductance in optimum C being lower than in optimum B. Intuitively, it might seem that the result should be the opposite. However, the differential mode noise level is more

critical in optimum design B due to some resonance between the boost inductor and the EMI filter capacitors, which is not as pronounced in optimum C, as can be seen in Figure 3.17.



(a) (b)

Figure 3.17. Total EMI noise, differential and common mode noise and L_B current in the case *Vin=230* Vrms for (a) Optimum B and (b) Optimum C.

The switching frequency of the optimum designs obtained, as seen in the continuous optimization approach, has a magnitude immediately below the frequencies at which the EMI filter encounters a jump in cost (see Figure 3.18). This result boosts the confidence in the results obtained by the OPES optimization tool.

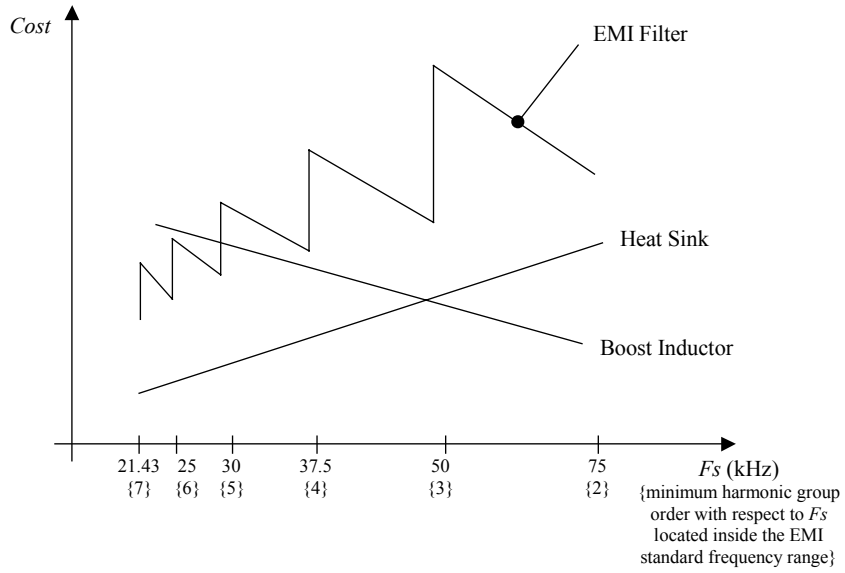


Figure 3.18. Qualitative description of the variation of the optimum design components' cost as a function of the switching frequency.*

* The sketch does not intend to reflect the relative cost of the three components.

However, in a practical implementation, the switching frequency tolerance should be considered. Otherwise, due to this tolerance, the prototype could work at a frequency higher than the closest corner frequency, and consequently, the EMI standard limits would not be met. Therefore, in a practical implementation of Optimums A, B and C, the switching frequencies should be selected according to Table 3.9.

In Chapter 2, a concern with respect to possible significant oscillations in the EMI filter component currents at low switching frequencies was raised. However, the currents through the EMI filter components for all three designs presented have been investigated by means of the analysis function developed, and no significant oscillations in these currents were detected.

Optimum B was selected and implemented. Figure 3.19 shows the prototype. Experimental tests were performed and the design proved to meet both thermal and EMI requirements (see Appendix B).

Table 3.9. Practical selection of switching frequencies for optimum designs A, B and C.

Optimum	Switching frequency
A	21.43 kHz- TolFs*
B	25 kHz - TolFs*
C	25kHz – TolFs*

* TolFs is the switching frequency tolerance, expressed in kHz.

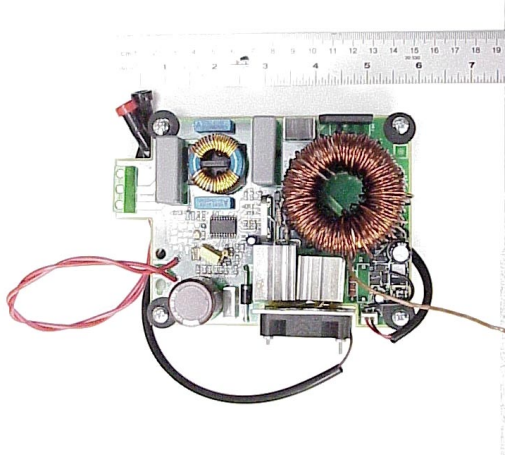


Figure 3.19. Prototype corresponding to Optimum B.

3.3.7. Conclusion

The discrete optimization approach developed and applied has proved to be a valuable tool for design. In a short design time, it led to a cost reduction in the order of 10 to 15 % with respect to the best designs obtained following the traditional methodology presented in Chapter 2, in which the switching frequency and boost inductor switching ripple were fixed based on the designer's intuitive understanding of the problem. OPES, the software tool developed, can also be used to rapidly estimate the minimum cost of the system under different design specifications and conditions, to quantitatively study the sensitivity of the cost to certain specifications or operating conditions in order to investigate possible ways of reducing the system cost, etc. Due to the short time required to obtain this information, the tool is therefore especially useful for initial project evaluations (viability, etc.).

Finally, the possibility of exploring the whole design space through the Single Design Analysis Mode in the software allows the designer to gain a better understanding of the system behavior, critical constraints, etc., conferring the tool an added educational value.

CHAPTER 4. CONCLUSION AND FUTURE OF OPTIMIZATION IN POWER ELECTRONICS

In Figure 4.1, the evolution of the cost of the different designs obtained is presented. Initially, Schneider Electric, S.A, provided a first design. In this design, a switching frequency of 100 kHz was selected. By means of the traditional design methodology described in Chapter 2, a new prototype was developed at 40 kHz that provided significant savings as compared to the previous design. From the understanding gained after applying the continuous optimization to the design of the system, it was understood that by simply choosing a switching frequency of 35 kHz instead of 40 kHz, the size and cost of the EMI filter could have been reduced without varying any other components. Finally, by means of the discrete optimization software tool, an optimal design at 24 kHz was identified, with additional savings.

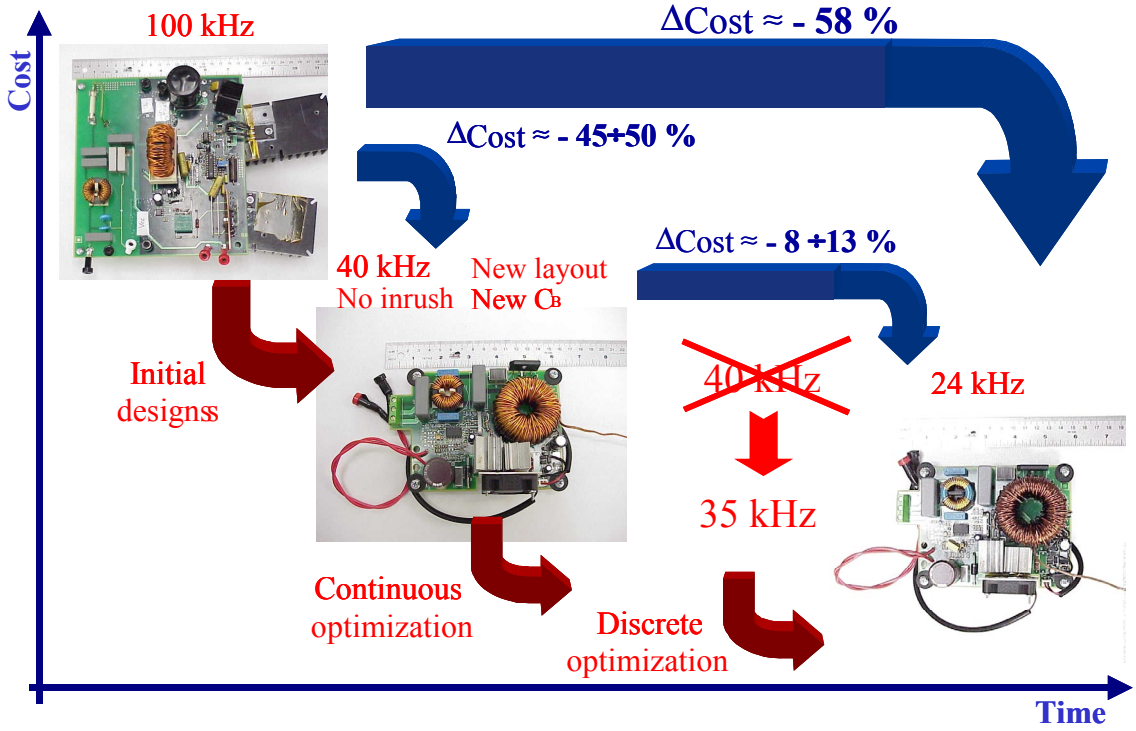


Figure 4.1. Cost evolution of the different designs.

A final estimated cost reduction of approximately 58% was achieved in the optimum design, as compared to that of its predecessor. Around 45-50% of this reduction can be attributed to the following:

- Elimination of the inrush current circuitry by selecting bridge diodes and fast diodes with enough surge current rating to withstand the possible transients.
- Reduction of the required output boost capacitance in the optimum design by prudent selection of the boost output voltage and by utilizing the dc-link capacitor in the load.
- Selection of iron powder as the core material instead of kool Mμ, and custom design of the boost inductor instead of buying a standard one from a manufacturer.
- Selection of separated heat sinks, which decreases the common mode noise levels, and therefore allows a smaller common mode choke to be selected.
- The initial design operates at a high switching frequency (100 kHz), thus requiring a more expensive heat sink and EMI filter as a result of the increased switching losses and EMI noise level.

Of the 58% improvement, the remaining 10% (approximately) can be attributed to the automated optimization design performed.

The software tool developed (OPES) for the design optimization of the boost PFC stage and input EMI filter could be invaluable in the design of future prototypes, providing in a short time low-cost designs for any desired specifications for which the topology considered is appropriate, or helping to determine the value of certain specifications / conditions that minimize the design cost.

4.1. Usefulness of Optimization in the Design of Power Electronics Systems

The use of optimization techniques in the component design of power electronics systems offers the following attractive advantages:

- Complete automated component design tools can be developed…
- …that allow improved solutions with respect to traditional design procedures, since more complexity can be considered in the design process,…
- …in a reduced design time, once the optimization problem has been specified and the appropriate tools to solve it developed.
- Quick assessment of optimum solutions for different sets of specifications, evaluation of the design objective function sensitivity with the variation of certain specifications and parameters, etc.
- The application of optimization techniques in the design has also an added educational value, since the optimization tool will highlight the critical aspects in each design scenario, allowing the user to focus his or her attention on these aspects and gain a better understanding of the system design peculiarities. In the work presented in this thesis, special insight was gained, for instance, in how to approach the design of the boost inductor and EMI filter, based on the results obtained through the optimization process.
- In a traditional design approach, each designer often follows his or her own particular design methodology which, on the other hand, is not rigorously specified anywhere. In contrary, the use of optimization techniques pushes the design team to work jointly to clearly and rigorously specify the design problem and methodology for its solution, which also allows future revisions to improve the design formulation. It provides a written and clear record of the design approach.

On the other hand, there are still several challenges to improving the practicality of optimization techniques:

- Efficient models of the system cost, performance, etc., have to be developed, fast and accurate enough for an optimization process requiring hundreds of design evaluations.
- The component data sheets do not always contain all the required information, and there are often significant differences among the data provided by each manufacturer. Some standardization would help the application of optimization techniques in the design process.
- The formulation of the optimization problem and the development of the tools to solve it require some time. The time required, however, decreases substantially once several design problems have been solved, since the component parameter definition, the component database, certain common models, etc., are already available.
- A real design process is complex, involving several considerations, some of which are hard to identify and express quantitatively. However, the author believes that once identified, they can normally be expressed in some acceptable mathematical form in order to be incorporated into the design problem formulation.

Based on previous comments, it can be concluded that the application of optimization techniques is especially recommended in those situations in which a big yield of the designed unit is desired, several designs will be needed for different sets of specifications, or in any other case for which any small improvement in the design could be important. In other situations it may be more efficient (from the design time and cost point of view) to ask an expert designer to perform the design, since a fairly good design could be obtained faster this way.

4.2. Possible Future Work

In the following, some suggestions for future work in the design of power electronics systems are presented, at both the subsystem and system design levels.

4.2.1. Subsystem Design

4.2.1.1. Component Design

The optimization work presented in this thesis belongs to this category. Some improvements and extensions in the models are still possible. For instance, the possibility of selecting different core shapes could be included in the software. This and other modifications are discussed in Appendix A, Section A.2.3.

The selection of the components for a given control scheme could also be incorporated into the optimization formulation.

4.2.1.2. Layout Design

The design variables specifying the layout geometry could also be included in the optimization formulation. This would allow improvements to be made in both the EMI and thermal models of the system (due to the strong dependence of the EMI and thermal behavior on such design variables), and exploration of the different tradeoffs involved in the layout design.

4.2.1.3. Power Stage Topologies and Control Schemes

The design optimization could be performed for different design topologies and control schemes in order to investigate which of them is optimal.

4.2.1.4. Other Applications

The design methodology presented here could also be applied to applications other than the design of a front-end converter providing power factor correction. For instance, the design of popular topologies such as the two-switch forward converter or the zero voltage switching (ZVS) full-bridge converter could be investigated. Several objective functions to minimize or maximize could be considered, depending on the application: size, weight, cost, performance, etc., or even multi-objective functions containing a combination of any of these factors.

4.2.1.5. Integrated Design

Currently, several research efforts aim to develop more integrated designs of power electronics converters, in which an integrated passive component solution and semiconductors are packaged into the same unit, rather than designing the system using discrete components. The use of optimization techniques in the design of such units could provide substantial benefits.

4.2.2. System Design

Optimization techniques can also be applied to the design of the system into which the converters are integrated as a whole, while simultaneously considering its different subsystems. Due to subsystem interactions, the design optimization of large power electronics systems as a whole will potentially improve the results obtained by optimizing individual parts of the system separately. The increased complexity of the design problem (large number of design variables and complex non-linear constraints, essentially), which causes traditional optimization approaches to be impractical or ineffective, could be handled by means of optimization methodologies such as the Global/Local [27] [28]. The methodology is based on a decomposition of the optimization problem into several hierarchical levels.

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Appendix A. Optimization Design Analysis Function Computations

A.1. Introduction

In this appendix, the computations performed by the design analysis function are described for both the discrete and continuous optimization approaches. In the continuous optimization approach of the whole system (single-phase boost PFC and EMI filter) one MATLAB function has been developed: "Canalyze.m." In the discrete optimization approach, the corresponding MATLAB function is called "Danalyze.m." This MATLAB function was then translated into Fortran ("pfcbr_analysis.f90") to be able to tie it to the genetic algorithm in charge of performing the optimization. Since the graphical user interface developed was built in the discrete optimization environment and the function "pfcbr_analysis.f90" can be modified by the user, the design analysis function computations for the discrete optimization will be the first described. The aim is to provide a friendly description of the computations performed in this function. The function computations for the continuous case are similar to those in the discrete approach. The differences, if any, are highlighted at the end of each section.

These functions receive as inputs the so-called 'design variables' and give as outputs the value of the cost function (cost of the system in m.u.) and the values of the physical constraints defined for the problem, for the given values of the design variables. Additional performance information for these given values of the design variables can be obtained by setting an internal variable in the programs, *aff*, to one.

In all functions, the layout and the boost capacitor are assumed to be fixed, concentrated parameters are considered in the models, no need for an inrush current circuitry has been assumed, and either a single or separated heat sinks can be considered.

A.2. Function Computations

In this section, a detailed description of the process and equations used for the computation of the cost function and constraints for a given value of the design variables is presented. The recommended values for the optimization runs in the case of the design

considered in this project for the different conditions, specifications and constants are also displayed. They may be used as a reference in further runs.

A.2.1. Conditions, Specifications and Constants

Table A.1. Programming constants.

Name	Description	Value
aff	The value stored in this constant determines whether the additional information with regard to the performance of the design is presented or not. A value of 1 makes this information available. Any other value prevents the presentation of the extra information.	1
Tol_eff*	Tolerance in the efficiency	0.0001
Tol_Tjsw*	Tolerance in the junction temperature of the switch	0.01
Tol_TcoreLb*	Tolerance in boost inductor core temperature	0.01

* Since there is no explicit equation for obtaining the value of the efficiency, the junction temperature of the switch and the boost inductor core temperature, some values are assumed and then are recomputed, based on the circuit equations. If the assumed and calculated values do not match, the set is assumed and the process is repeated iteratively until a match is attained.

A.2.1.1. Conditions / Specifications

A.2.1.1.1. General

Table A.2. General conditions / specifications.

Name	Description	Value
Vinmin_rms	Minimum input voltage (Figure A.1-1)	180 V
Vinnom_rms	Nominal input voltage (Figure A.1-1)	230 V
fline	Nominal line frequency	50 Hz
Po	Output power (Figure A.1-4)	1150 W

Vbus_DC	Dc value of the voltage across the output boost capacitor C_B (see Figure A.2)	368 V
Tamb	Ambient temperature	40 °C
Conservative	Degree of conservative analysis to perform: -1(Non-conservative) ≤ Conservative ≤ 1(Most conservative)	-1

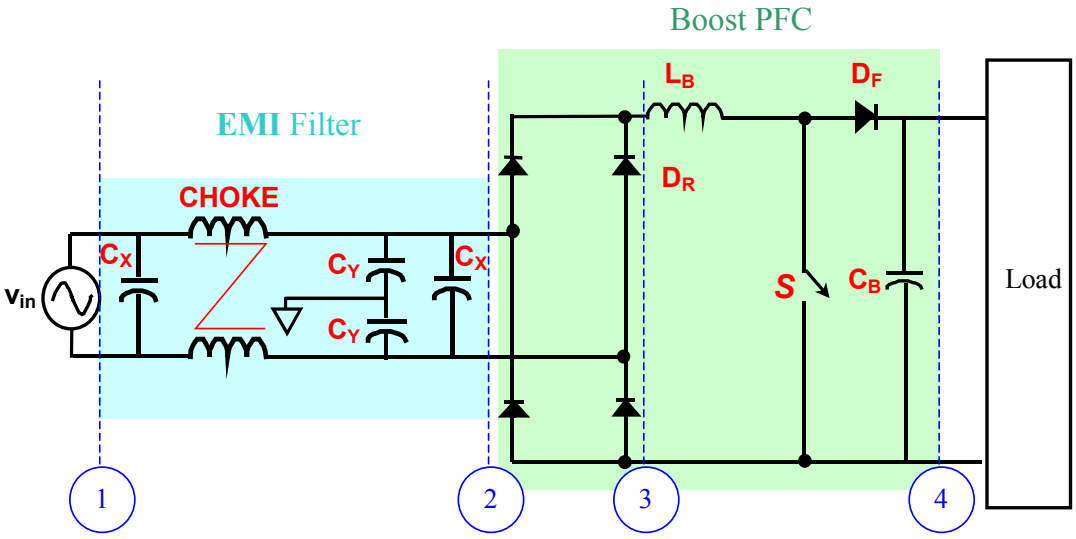


Figure A.1. EMI filter and boost PFC stage schematic.

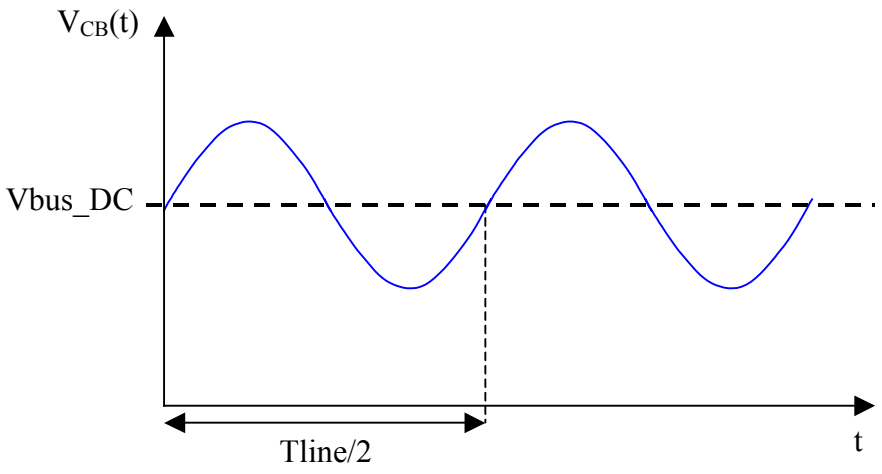


Figure A.2. Voltage waveform across C_B.

A.2.1.1.2. Single-Phase Boost PFC

Table A.3. Boost capacitor (C_B): 68μF, 450 V.

Name	Description	Value
Cb	Capacitance in PFC stage (68 μF)+ Capacitance (worst case) in load (624 μF)	692E-6 F
Cost_Cb	Cost of the boost capacitor	*** m.u.

Table A.4. Boost inductor wire.

Name	Description	Value
Jm	Maximum current density of the copper	1000 A/cm^2
Row100	Resistivity of the copper at 100 °C	2.208E-6 Ω.cm
Kcu	Temperature coefficient for the copper resistivity	0.0039 Ω.cm/°C
Ku	Maximum filling factor considering that the cross-section of the wire is a square of side *Dw* (diameter of the wire)	0.4
Cost_Lbfixwiring*	Fixed wiring cost for the boost inductor	*** m.u.

* See Section A.2.4 for a method to estimate this cost if it is not directly available.

Table A.5. Boost inductor miscellaneous.

Name	Description	Value
TolLblkg	Boost inductor leakage inductance tolerance	50 %
TLbcoef	Boost inductor temperature coefficient	1.2

Table A.6. Devices' voltage ratings.

Name	Description	Value
VpkMmin	Minimum breakdown voltage of the MOSFET	500 V
VpkIGmin	Minimum breakdown voltage of the IGBT	600 V
Vpkfdmin	Minimum breakdown voltage of the fast diode	600 V
Vpkrdmin	Minimum breakdown voltage of the rectifier diode	800 V

Table A.7. Devices' current ratings.

Name	Description	Value
IFSMmin	Minimum required surge current that the rectifier diodes and the fast diode need to withstand	150 A

Table A.8. Switch.

Name	Description	Value
Ls	Inductance in series with MOSFETs	10e-9 H
TriseIGBT	Rise time of the voltage across the switch (IGBT) (obtained from other work [29], Figure A.3)	50e-9 s
TfallIGBT	Fall time of the voltage across the switch (IGBT) (assumed to be equal to the rise time)	50e-9 s
Perswqrr	Percentage of the reverse-recovery losses dissipated in the switch	50 %

Table A.9. Driver.

Name	Description	Value
VGG	Driver source voltage	15 V
Rgon	Driver resistance in the turn-on	33 Ω
Rgoff	Driver resistance in the turn-off	10 Ω

Table A.10. Heat sink.

Name	Description	Value
SingHS	Boolean variable indicating whether a single heat sink or separated heat sinks are used (1: Single heat sink, 0: Separated heat sinks)	0
HSfd	Boolean variable indicating whether the fast diode is attached to a commercial heat sink or not (1: It is attached, 0: It is not attached)	1
HSrd	Boolean variable indicating whether the rectifier diodes are attached to a commercial heat sink or not (1: They are attached, 0: They are not attached)	0
TmaxHS	Maximum temperature of the heat sink/s	100 °C
K1HS*	First coefficient of the approximation of the heat sink cost as a function of the inverse thermal resistance	*** m.u.
K2HS*	Second coefficient of the approximation of the heat sink cost as a function of the inverse thermal resistance	*** m.u.*(W/C)

* See cost approximation equation in Section A.2.4.

Table A.11. Printed circuit board (PCB).

Name	Description	Value
TmaxPCB	Maximum temperature allowed in the PCB	125 °C
DT_pcb_Lbcore	Estimated temperature difference between the boost inductor core and the PCB (T_coreLb-T_PCB)	5 °C

A.2.1.1.3. EMI Filter

Table A.12. Standard.

Name	Description	Value
Class_type	Integer code number indicating the EMI standard to meet (0: Class B, Group 1; 1: Class A, Group 1)	0

Table A.13. Voltage ratings.

Name	Description	Value
VacCxmin	Minimum ac breakdown voltage of the differential mode capacitor Cx.	275 V
VacCymin	Minimum ac breakdown voltage of the common mode capacitor Cy.	250 V

Table A.14. LISN components.

Name	Description	Value
LN	LISN inductance	50e-6 H
CN	LISN capacitance in series with ZN	100e-9 F

C1	LISN capacitance in the mains side of the LISN	10e-6 F
ZN	LISN resistance	50 Ω

Table A.15. Parasitic elements of the propagation paths.

Name	**Description**	**Value**
Lres	Line impedance inductance	150e-6 H
Llmg	Cable or trace parasitic inductance	500e-9 H
Llha	Cable or trace parasitic inductance	250e-9 H
Lldb	Cable or trace parasitic inductance	250e-9 H
Lfs	Cable or trace parasitic inductance	30e-9 H
Csg	Parasitic capacitance from node S to ground	1e-12 F
Cdg	Parasitic capacitance from node D to ground. Common mode noise very sensitive to the value of this parasitic	21.5e-12 F
Ckg	Parasitic capacitance from node K to ground	1e-12 F
Ceg	Parasitic capacitance from node E to ground	1e-12 F
Cfg	Parasitic capacitance from node F to ground	1e-12 F
Cag	Parasitic capacitance from node A to ground	1e-12 F
Cbg	Parasitic capacitance from node B to ground	1e-12 F
CLb	Boost inductor parasitic capacitance	25e-12 F
RLb	Boost inductor parasitic resistance	25.8e3 Ω

Table A.16. Other EMI constants.

Name	Description	Value
std	Matrix containing the quasi-peak limits of the voltage across ZN in the LISN (first column: frequency; second column: voltage limit in LISN resistor (dBμV))	(see program)
nharmgr	Tis is the number of the harmonics groups multiples of the switching frequency to be considered above the minimum frequency for which the standard specifies a limit. As nharmgr increases the computation time increases.	1
ind	This is the number of harmonics multiples of the line frequency to be considered on each side of each multiple of the switching frequency. As ind increases, the accuracy of the results improves but the computation time increases.	3
incr	This is the increment in EMI levels, and represents a correction in the estimation of the EMI levels needed because not all harmonics are computed, just the ind that are more significant on each side of each multiple of the switching frequency. This value must be set according to the line frequency, the bandwidth of the measurement, and the value of ind: for fline=50 Hz , a bandwidth of 9 kHz, and ind=3 set incr=3 dB; for fline=50 Hz , a bandwidth of 9 kHz, and ind=10 set incr=2 dB; and for fline=50 Hz , a bandwidth of 9 kHz, and ind=90 set incr=0 dB.	3 dB

A.2.1.1.4. Continuous Optimization Conditions / Specifications

See discussion in Section A.2.2.12.

A.2.2. Design Variables

In the discrete optimization, most of the design variables (such as the devices) require more than one parameter to be described. Therefore, a vector corresponding to the value of the different parameters needed to define each design variable will be used. All these vectors will constitute the input of the function in charge of performing the design analysis. In the following, each of the parameters considered to define each of the design variables will be presented.

Note: whenever one of the parameters depends on the junction temperature of a device, the worst value for a junction temperature equal or greater than 100 °C is selected.

A.2.2.1. Switch

Table A.17. Switch parameters.

Parameter name	Description	Units
Switch_type$^{(MI)}$	Boolean parameter that determines the switch type: (0) IGBT, (1) MOSFET	-----
Cost_switch$^{(MI)}$	Cost of the switch (If the switch is an IGBT and does not have an internal anti-parallel diode, this cost should include the cost of the anti-parallel diode.)	m.u.
Vpksw$^{(MI)}$	Breakdown voltage of the switch	V
Iswrmsmax$^{(M)}$	Maximum rms current of the switch	A
Iswavmax$^{(I)}$	Maximum average current of the switch	A
VFsw$^{(I)}$	This is the constant conduction voltage drop, obtained as the voltage V_{CE} corresponding to a current I_{CE}=0 A, in the linear approximation of the curve I_{CE}-V_{CE} presented in the data sheet.	V

Ronsw1$^{(MI)}$	• *MOSFET:* First coefficient of the linear approximation of the switch on-resistance as a function of the junction temperature. (Ronsw=Ronsw1+Ronsw2*Tjsw); obtained from the corresponding plot in the data sheet. • *IGBT:* Conduction resistance; obtained from the curve I_{CE}-V_{CE} in data sheet. It corresponds to the slope of the linear approximation of the curve in the normal operating range of currents (I_{CE}): 1 to 10 A in this project.	Ω
Ronsw2$^{(M)}$	Second coefficient of the linear approximation of the switch on-resistance as a function of the junction temperature. (Ronsw=Ronsw1+Ronsw2*Tjsw). Obtained from the corresponding plot in the data sheet.	Ω/°C
G$^{(M)}$	dI_D/dV_{GS}. Obtained from the curve I_D-V_{GS} in the data sheet, making a linear approximation in the application range of drain currents (I_D): 0A to 10 A in this project.	A/V
Crssh$^{(M)}$	Value of Crss for a high value of V_{DG}	F
Crssl$^{(M)}$	Value of Crss for a low value of V_{DG}	F
Cissh$^{(M)}$	Value of Ciss for a high value of V_{DG}	F
Cissl$^{(M)}$	Value of Ciss for a low value of V_{DG}	F
Coss$^{(M)}$	Value of Coss at V_{DS} = 80 % of V_{DSS}	F
Vp$^{(M)}$	This is the value of the voltage V_{GS} at which the curve V_{GS} - Q_G presents a plateau for the average boost inductor current obtained from the curve I_D-V_{GS} in the data sheet.	V
VT$^{(M)}$	This is the typical threshold voltage of V_{GS}, obtained from the electrical characteristics in the data sheet.	V
VCE_E$^{(I)}$	This is the collector-emitter voltage at which Eon and Eoff are provided.	V

IC_E[I]	This is the collector current at which Eon and Eoff are provided.	A
Eon[I]	This is the energy lost in the turn-on (at VCE_E and IC_E).	J
Eoff[I]	This is the energy lost in the turn-off (at VCE_E and IC_E) (including the tail losses).	J
RSth_j_c[MI]	Thermal resistance junction-to-case	°C/W
RSth_c_s[MI]	Thermal resistance case-to-heat sink	°C/W
Tmaxsw[MI]	Maximum operating junction temperature	°C

[MI] For both MOSFET and IGBT.

[M] For MOSFET only.

[I] For IGBT only.

Note: If the switch is a MOSFET, the parameters for only the IGBT can have any value (for instance, zero). Vice-versa in the case of the IGBT.

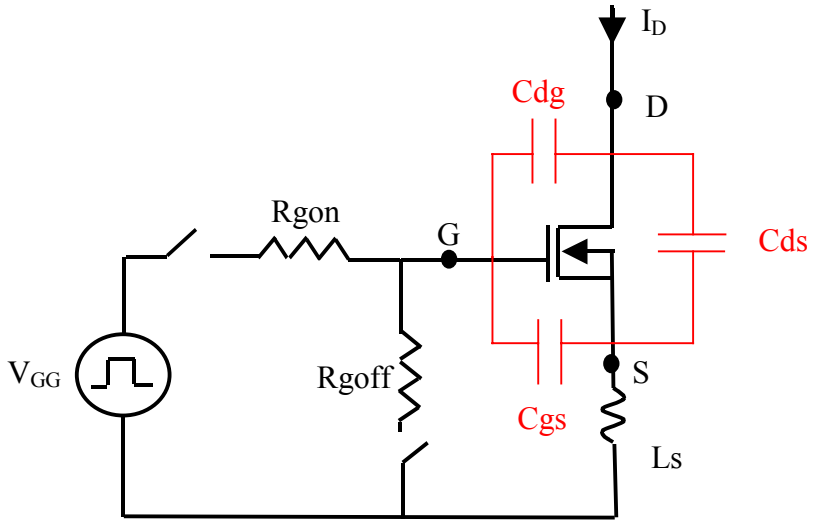


Figure A.3. Simplified representation of the MOSFET and gate driver.

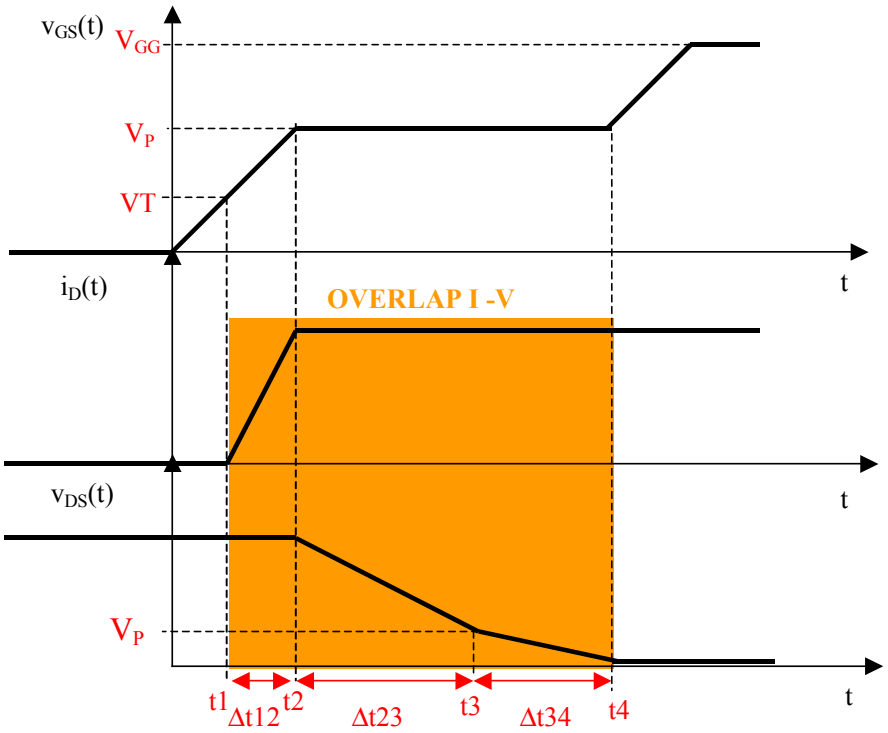


Figure A.4. Turn-on of S (MOSFET).

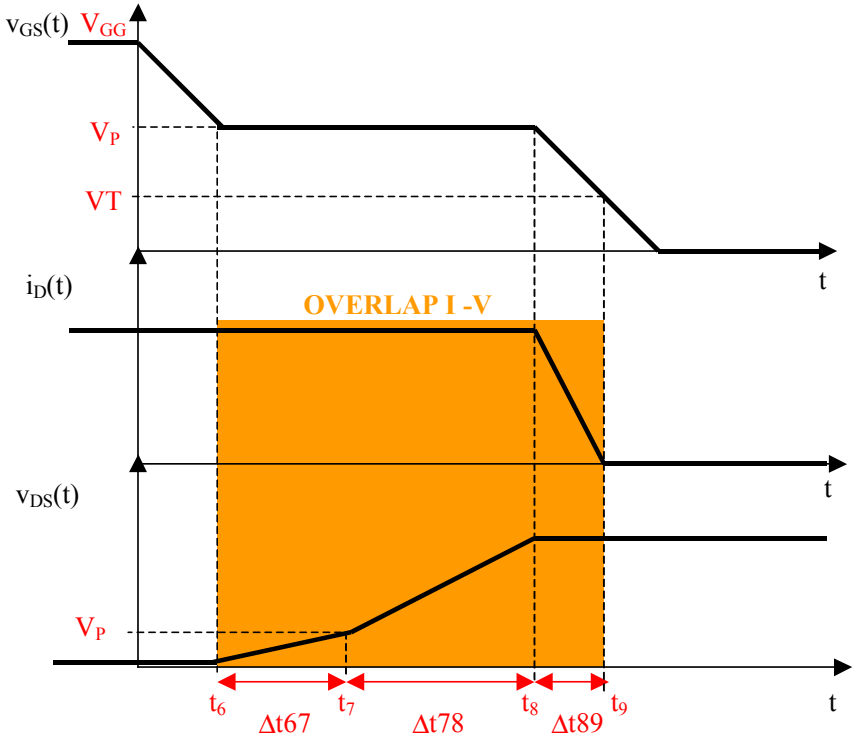


Figure A.5. Turn-off of S (MOSFET).

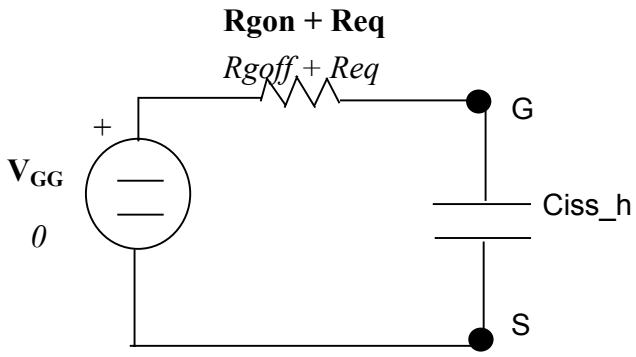


Figure A.6. Equivalent circuit diagram during t=t1→t2 (turn-on) (bold) and t=t8→t9 (turn-off) (italics).

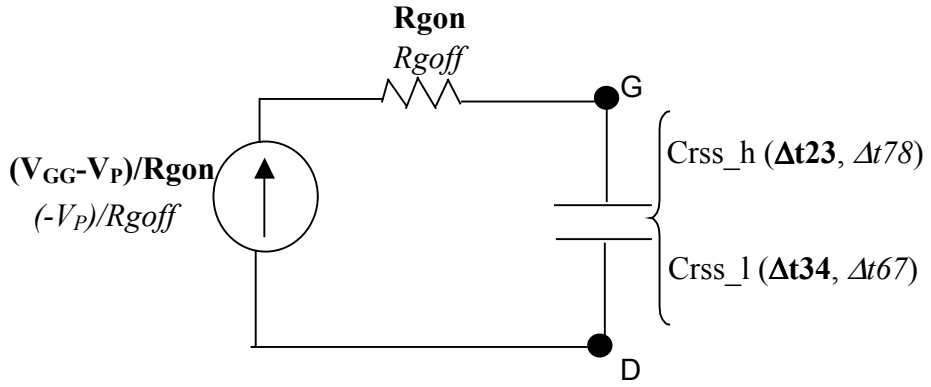


Figure A.7. Equivalent circuit diagram during t=t2→t3, t=t3→t4 (turn-on) (bold) and t=t6→t7, t=t7→t8 (turn-off) (italics).

A.2.2.2. Bridge Diode

Table A.18. Bridge diode parameters.

Parameter name	Description	Units
Cost_rectdiode	Cost of one rectifier diode	m.u.
Vpkrd	Breakdown voltage of the diode	V
Irdavmax	Maximum average current of the diode	A
IFSMrd	Maximum surge current of the diode (at the line frequency)	A
VFrd	This is the constant conduction voltage drop, obtained as the voltage V_F corresponding to a current I_F=0 A, in the linear approximation of the curve I_F-V_F presented in the data sheet.	V
Ronrd	This is the conduction resistance, obtained from the curve I_F-V_F in the data sheet. It corresponds to the slope of the linear approximation of the curve in the normal operating range of currents (I_F).	Ω
RRDth_j_c	This is the thermal resistance junction-to-case to be applied to the average (in a line period) power lost in one rectifier diode.	°C/W
RRDth_c_s	This is the thermal resistance case-to-heat sink to be applied to the average (in a line period) power lost in one rectifier diode. In a package of two/four rectifier diodes it corresponds to two/four times the Rth_c_s of the package.	°C/W
Tmaxrd	Maximum operating junction temperature	°C

A.2.2.3. Fast Diode

Table A.19. Fast diode parameters.

Parameter name	**Description**	**Units**
Cost_fastdiode	Cost of the fast diode	m.u.
Vpkfd	Breakdown voltage of the diode	V
Ifdavmax	Maximum average current of the diode	A
IFSMfd	Maximum surge current of the diode (at fline)	A
VFfd	This is the constant conduction voltage drop, obtained as the voltage V_F corresponding to a current I_F=0 A, in the linear approximation of the curve I_F-V_F presented in the data sheet.	V
Ronfd	This is the conduction resistance, obtained from the curve I_F-V_F in the data sheet. It corresponds to the slope of the linear approximation of the curve in the normal operating range of currents (I_F): 1 to 10 A in this project	Ω
Qrr1*	This is the first coefficient of the linear approximation of the diode reverse-recovery charge as a function of the forward current, assuming a certain di_F/dt (Qrr=Qrr1+Qrr2*if).	C
Qrr2*	This is the second coefficient of the linear approximation of the diode reverse-recovery charge as a function of the forward current, assuming a certain di_F/dt (Qrr=Qrr1+Qrr2*if).	C/A
RFDth_j_c	Thermal resistance junction-to-case	°C/W

RFDth_c_s	Thermal resistance case-to-heat sink	°C/W
Tmaxfd	Maximum operating junction temperature	°C

* Whenever Qrr is not directly available in the data sheet and t_{rr} (total reverse-recovery time) and I_{RM} (maximum reverse-recovery current) or t_A (initial period of time of the reverse-recovery process) are available instead, the following formula to calculate Qrr1 and Qrr2 is used:

$$Qrr = \frac{1}{2} \cdot t_{rr} \cdot I_{RM} = \frac{1}{2} \cdot t_{rr} \cdot \frac{di_F}{dt} \cdot t_A = Qrr1 + Qrr2 * i_F ,$$

where

t_{rr}: total reverse-recovery time,

I_{RM}: maximum reverse-recovery current, and

t_A : initial reverse-recovery time (until I_{RM} is reached).

Either t_{rr} or t_A is expressed as a linear function of the forward current, whichever presents a major dependence on this last one. If t_{rr} is expressed as a linear function of the forward current, t_A will be considered to be constant, and vice-versa. This constant is obtained for a forward current I_F equal to the average input current (≅ 6A in this project).

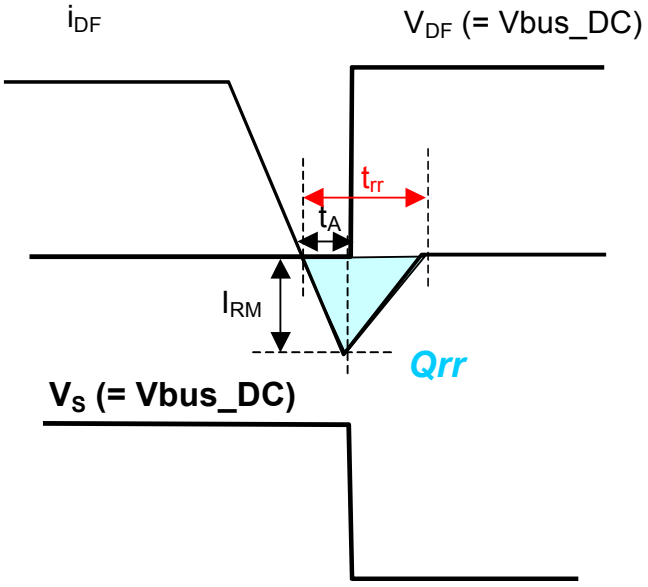


Figure A.8. Reverse-recovery phenomena model.

A.2.2.4. Boost Inductor Core

Table A.20. Boost inductor core parameters.

Parameter name	Description	Units
Cost_Lbcore	Cost of the boost inductor core	m.u.
Cid1	Integer value to codify the manufacturer / core material (see Table A.21)	-------
Cid2	Integer value to codify the types of core within a material defined in cid1, typically the different permeabilities possible (see Table A.21)	-------
AL	Inductance rating of the core (nH for one turn ≡ mH for 1000 turns)	nH/(turn^2) ≡ mH/(1000_turn^2)
TolAL	Tolerance of the value of AL	%
OD	Outside diameter of the core	cm
ID	Inside diameter of the core	cm
Ht	Height of the core	cm
lm	Mean magnetic path	cm
Ac	Cross-sectional area of the core	cm^2
Vc	Volume of the core	cm^3
MLT	Mean length per turn. (in the case of Micrometals catalog, this value can be obtained from pages 60-61)	cm
T_coreLbmax	Maximum temperature of the core	°C

Table A.21. Codification of the different core types.

Cid1: Manufacturer / Material	Cid2: Core type	
1: Micrometals Iron Powder	1: Mix 2	6: Mix 33
	2: Mix 8	7: Mix 38
	3: Mix 18	8: Mix 40
	4: Mix 26	9: Mix 45
	5: Mix 28	10: Mix 52
2: Magnetics High Flux	1: $\mu = 14$	4: $\mu = 125$
	2: $\mu = 26$	5: $\mu = 147$
	3: $\mu = 60$	6: $\mu = 160$
3: Magnetics Kool Mμ	1: $\mu = 26$	4: $\mu = 90$
	2: $\mu = 60$	5: $\mu = 125$
	3: $\mu = 75$	
4: Magnetics Molypermalloy	1: $\mu = 14$	6: $\mu = 160$
	2: $\mu = 26$	7: $\mu = 173$
	3: $\mu = 60$	8: $\mu = 200$
	4: $\mu = 125$	9: $\mu = 300$
	5: $\mu = 147$	10: $\mu = 550$

A.2.2.5. Boost Inductor Wire

Table A.22. Boost inductor wire parameters.

Parameter name	Description	Units
Cost_Lbwire*	Cost per unit of length of the wire (includes variable manufacturing cost)	m.u./ cm
Aw	Bare area of the wire	cm^2
Dw	External diameter of the wire	cm
Tmaxwire	Maximum temperature of the wire	°C

* See Section A.2.4 for a method to estimate this cost if it is not directly available.

A.2.2.6. Boost Inductor Number of Turns

Table A.23. Boost inductor number of turns.

Parameter name	Description	Units
nturn	Number of turns of the boost inductor	----------

A.2.2.7. Common Mode Choke

Table A.24. Common mode choke parameters.

Parameter Name	Description	Units
Cost_choke	Cost of the common mode choke	m.u.
Lcm	Common mode inductance	H
TolLcm	Tolerance in the value of Lcm	(%)
Ldm	Leakage inductance (differential mode inductance)	H
ICHrms_max	Maximum rms current	A

A.2.2.8. Differential Mode Capacitor Cx

Table A.25. Differential mode capacitor Cx parameters.

Parameter name	Description	Units
Cost_Cx	Cost of the differential mode capacitor	m.u.
Cfx	Capacitance of the differential mode capacitor	F

TolCx	Tolerance in the value of Cfx	(%)
ICxrms_max	Maximum rms current	A
VacCx	Maximum ac voltage	V

A.2.2.9. Common Mode Capacitor Cy

Table A.26. Common mode capacitor Cy parameters.

Parameter name	**Description**	**Units**
Cost_Cy	Cost of the common mode capacitor	m.u.
Cfy	Capacitance of the common mode capacitor	F
TolCy	Tolerance in the value of Cfy	(%)
ICyrms_max	Maximum rms current	A
VacCy	Maximum AC voltage	V

A.2.2.10. Thermal Resistance Heat Sink-to-Ambient: Rth_hs_amb (°C/W)

If a single heat sink is selected, *Rth_hs_amb* refers to the thermal resistance of this heat sink. If separate heat sinks are selected, *Rth_hs_amb* refers to the thermal resistance of the switch heat sink.

A.2.2.11. Switching Frequency: fs (Hz)

A.2.2.12. Continuous Optimization Design Variables

In the continuous optimization approach all the devices and the boost inductor core shape (toroidal) and material are fixed due to the continuous nature of the approach to obtain the optimum. Therefore, the previously explained parameters of the corresponding design variables become constants. Other discrete design variables, such as the EMI filter capacitors and the

common mode choke, become continuous and are represented by the corresponding capacitance or inductance.

The design variables are summarized in Table A.27.

Table A.27. Continuous optimization design variables.

Name		Description	Units
EMI filter	*Cfx*	Capacitance of the differential mode capacitor Cx	F
	Cfy	Capacitance of the common mode capacitor Cy	F
	Lcm	Magnetizing inductance of the common mode choke	H
Boost inductor L_B	*nturn*	Boost inductor number of turns	--
	Aw	Copper area of the boost inductor wire	cm^2
	OD	External diameter of the boost inductor core	cm
	ID	Internal diameter of the boost inductor core	cm
	Ht	Height of the boost inductor core	cm
fs		Switching frequency	Hz
Rth_hs_amb		Thermal resistance heat sink to ambient	°C/W

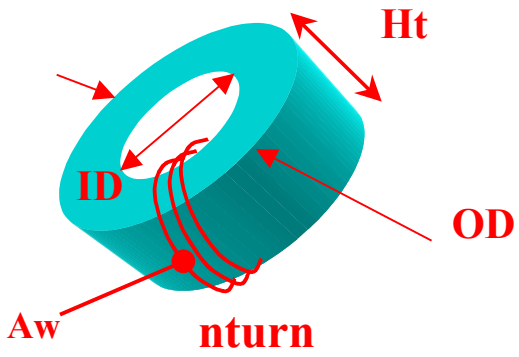


Figure A.9. Boost inductor design variables in the continuous approach.

A.2.3. Calculations

The equations and assumptions considered for the analysis of a design defined by a determined choice of the design variables are presented in the following.

A.2.3.1. Boost PFC

- **Assumptions:**

a) The switching frequency >> line frequency.

b) The input voltage magnitude in Figure A.1-1 is the same as both the magnitude of the voltage in Figure A.1-2 and the magnitude of the rectified voltage in Figure A.1-3.

c) The effect of the dc bias point of the flux density in each switching period on the core losses is neglected , according to the manufacturer's catalog [20, p. 28].

d) A di/dt =200 A/μs is assumed for the computation of the reverse-recovery losses of the fast diode.

- **Equations:**

- Number of switching periods in one half of a line cycle:

$$num = floor\left[\frac{fs}{2 \cdot fline}\right].$$

- Line and switching angular speeds and periods:

$$wline = 2 \cdot \pi \cdot fline,$$
$$Tline = \frac{1}{fline},$$

$$ws = 2 \cdot \pi \cdot fs, \text{ and}$$
$$Ts = \frac{1}{fs}.$$

- Vector containing the values of the output voltage in Figure A.1-4 in the middle of each switching period for one half of a line cycle:

$$i = 1..num,$$
$$t_i = (i - 0.5) \cdot Ts, \text{ and}$$
$$vout_i = \sqrt{Vbus\_DC^2 - \frac{Po}{wline \cdot Cb} \cdot \sin(2 \cdot wline \cdot t_i)}.$$

- Equivalent resistance in series with the gate resistance of the MOSFET due to the equivalent series inductance of the MOSFET:

$$\mathrm{Re}q = \frac{Ls \cdot G}{Cissh}.$$

- Inductance rating considering the tolerance:

$$AL\min = AL \cdot \left(1 - \frac{tolAL}{100}\right) \cdot 10^{-9} \qquad \left(\frac{H}{nturn^2}\right).$$

- Leakage inductance in the boost inductor (formula extracted from the Magnetics catalogs):

$$Lblkg = \left(1 - \frac{TolLblkg}{100}\right) \cdot \left(292 \cdot nturn^{1.065} \cdot \frac{Ac}{lm \cdot 10^8}\right) \quad (H).$$

- Window area of the boost inductor core:

$$Wa = \pi \cdot \frac{ID^2}{4} \quad (\mathrm{cm}^2).$$

- Surface area of the boost inductor, taking into account the wire (the number of external and internal layers of wire are estimated):

$$Exlay = \frac{nturn \cdot Dw}{\pi \cdot OD},$$

$$Inlay = \frac{nturn \cdot Dw}{\pi \cdot OD}, \text{and}$$

$$Asurf = \pi \cdot \left(\begin{array}{l} \frac{(OD + 2 \cdot Dw \cdot Exlay)^2 - (ID - 2 \cdot Dw \cdot Inlay)^2}{2} + \\ + (Ht + 2 \cdot Dw \cdot Exlay) \cdot (OD + 2 \cdot Dw \cdot Exlay) + \\ + (Ht + 2 \cdot Dw \cdot Inlay) \cdot (ID - 2 \cdot Dw \cdot Inlay) \end{array} \right).$$

- DC resistance of the boost inductor winding:
  - Resistivity of the copper, assuming the core is at its maximum allowed temperature:

$$row = row100 \cdot (1 + Kcu \cdot \min[T\_coreLb\max, T\max wire, T\max PCB + dT\_pcb\_Lbcore]).$$

  - DC resistance value of the winding:

$$Rcopper = row \cdot nturn \cdot MLT / Aw.$$

- Parameters needed for the estimation of the skin and proximity effects [9]:
  - Skin depth at 100 °C and at Fs:

$$deltafs = \frac{7.5}{\sqrt{fs}} \quad (cm).$$

  - Average number of layers:

$$em = \frac{nturn \cdot Dw}{lm}.$$

  - Average number of turns per layer:

$$nturnlay = \frac{lm}{Dw}.$$

- Bare diameter of the wire (copper only):

$$Dwb = 2 \cdot \sqrt{\frac{Aw}{\pi}}\,.$$

- Conductor spacing factor or winding porosity:

$$\eta = wpor = \sqrt{\frac{\pi}{4}} \cdot Dwb \cdot \frac{nturnlay}{lm}\,.$$

- Effective ratio of the conductor thickness to the skin depth:

$$\varphi = phi = \sqrt{wpor} \cdot \sqrt{\frac{\pi}{4}} \cdot \frac{Dwb}{deltafs}\,.$$

- DC resistance of a layer:

$$RcopperDC = row \cdot MLT \cdot \frac{nturnlay^3}{wpor \cdot lm^2}\,.$$

- Auxiliary functions of φ to estimate the high-frequency losses in the windings:

$$G1 = \frac{\sinh(2\cdot\varphi) + \sin(2\cdot\varphi)}{\cosh(2\cdot\varphi) - \cos(2\cdot\varphi)}, \text{ and}$$
$$G2 = \frac{\sinh(\varphi)\cdot\cos(\varphi) + \cosh(\varphi)\cdot\sin(\varphi)}{\cosh(2\cdot\varphi) - \cos(2\cdot\varphi)}.$$

- Peak voltage in Figure A.1-2:

$$Vin\_pk = Vin\_rms \cdot \sqrt{2}\,.$$

- Vector containing the values of the input voltage in Figure A.1-2 in the middle of each switching period for one half of a line cycle:

$$vin\_vec_i = Vin\_pk \cdot \sin(wline \cdot t_i)\,.$$

By assuming a certain value of the efficiency (*eff*) from 2 to 4 in Figure A.1, the junction temperature of the switch (*Tjsw*) in the case of the MOSFET, and the temperature of the boost inductor core (*T_coreLb*):

- Input power in Figure A.1-2:

$$Pin = \frac{Po}{eff}.$$

- Vector containing the values of the average (in the switching cycle) current in Figure A.1-2 in the middle of each switching cycle for one half of a line cycle:

$$Iin\_pk = \sqrt{2} \cdot \frac{Pin}{Vin\_rms}, \text{ and}$$
$$iin\_vec_i = Iin\_pk \cdot \sin(wline \cdot t_i).$$

- On-resistance of the switch:

$$Ronsw = Ronsw1 \qquad (IGBT), \text{ and}$$
$$Ronsw = Ronsw1 + Ronsw2 \cdot Tjsw \qquad (MOSFET).$$

- Vector containing the duty ratios of the switch for each switching period:

$$d\_vec_i = \frac{vout_i + VFfd + iin\_vec_i \cdot Rcopper - vin\_vec_i}{vout_i + VFfd - VFsw - iin\_vec_i \cdot Ronsw}.$$

- Vector containing the value of the dc magnetizing force in the boost inductor core for each switching cycle:

$$H\_Lb_i = 0.4 \cdot \pi \cdot \frac{nturn}{lm} \cdot iin\_vec_i \quad (\text{oersteds}).$$

- Vector containing the value of the ac flux in the boost inductor core for each switching cycle:

$$Bacpk_i = \frac{vin\_vec_i \cdot d\_vec_i \cdot Ts \cdot 10^8}{2 \cdot Ac \cdot nturn} \quad (Gauss).$$

- Saturation:

The saturation as a function of the dc magnetizing force, ac flux, boost inductor core temperature and switching frequency is estimated by using the curve-fit formulae provided by each manufacturer for each core material. The different coefficients in the formulae needed for the estimation of the saturation are contained in a matrix called *fit*. This matrix is initially stored in memory, and its size and contents differ according to the core manufacturer

/ material considered. Since the curve-fit formulae are only valid for a limited range of values of the dc magnetizing force, ac flux, boost inductor core temperature and switching frequency, and whenever in the process of optimization values of these magnitudes may go beyond these limits, some corrections are introduced to these equations to avoid unrealistic predictions or crashes of the program. For instance, if the percentage of saturation as a function of the dc magnetizing force is evaluated at a value of the dc magnetizing force higher than the maximum value for which the curve-fit equation is valid, a complex number may be obtained by evaluating the square root of a negative number, and the program will crash since the user will try to store this value in a real variable. The program would not crash if a real number were obtained, but it would still be a wrong prediction, since the value of the dc magnetizing force surpassed the maximum for which the equation was valid.

- Vector *sat* containing the per unit saturation coefficient of the boost inductor core for each switching cycle:
  - Micrometals iron powder [20]:

$$satdc_i = \left(1-\frac{Tol\_LBsatdc}{100}\right)\cdot\sqrt{\frac{asdc+csdc\cdot H\_Lb_i+esdc\cdot H\_Lb_i^2}{1+bsdc\cdot H\_Lb_i+dsdc\cdot H\_Lb_i^2}} \quad (\%),$$

$$satac_i = \left(1-\frac{Tol\_LBsatac}{100}\right)\cdot\sqrt{\frac{asac+csac\cdot Bacpk_i+esac\cdot Bacpk_i^2}{1+bsac\cdot Bacpk_i+dsac\cdot Bacpk_i^2}} \quad (\%) \quad \{Mix.=2,8,18,26,40\},$$

$$satac_i = \left(1-\frac{Tol\_LBsatac}{100}\right)\cdot\left(asac+bsac\cdot Bacpk+csac\cdot\sqrt{Bacpk}+dsac\cdot Bacpk^2\right) (\%) \quad \{Mix.=28,33,38,45,52\}, \text{ and}$$

$$sat_i = satdc_i\cdot satac_i\cdot\frac{1}{10^4} \text{ (p.u.).}$$

  - Magnetics high flux [30]:

$$satdc_i = \left(1-\frac{Tol\_LBsatdc}{100}\right)\cdot\sqrt{\frac{1+asdc\cdot\mu_r\cdot H\_Lb_i+bsdc\cdot\mu_r^2\cdot H\_Lb_i^2}{1+csdc\cdot\mu_r\cdot H\_Lb_i+dsdc\cdot\mu_r^2\cdot H\_Lb_i^2}} \text{ (p.u.),}$$

$$satac_i = \left(1-\frac{Tol\_LBsatac}{100}\right)\cdot\left(asac+bsac\cdot Bacpk_i+csac\cdot Bacpk_i^2+dsac\cdot Bacpk_i^3+esac\cdot Bacpk_i^4\right) \text{ (p.u.),}$$

$$satT = \left(1-\frac{Tol\_LBsatT}{100}\right)\cdot\left(asT+bsT\cdot T\_coreLb+csT\cdot T\_coreLb^2\right) \text{ (p.u.), and}$$

$$sat_i = satdc_i\cdot satac_i\cdot satT.$$

- Magnetics kool Mμ [31,32]:

$$satdc_i = \left(1-\frac{Tol\_LBsatdc}{100}\right)\cdot\sqrt{\frac{1+asdc\cdot\mu_r\cdot H\_Lb_i+bsdc\cdot\mu_r^2\cdot H\_Lb_i^2}{1+csdc\cdot\mu_r\cdot H\_Lb_i+dsdc\cdot\mu_r^2\cdot H\_Lb_i^2}} \text{ (p.u.),}$$

$$satac_i = \left(1-\frac{Tol\_LBsatac}{100}\right)\cdot\left(1+asac+bsac\cdot Bacpk_i+csac\cdot Bacpk_i^2+dsac\cdot Bacpk_i^3+esac\cdot Bacpk_i^4\right) \text{ (p.u.),}$$

$$satT = \left(1-\frac{Tol\_LBsatT}{100}\right)\cdot\left(100+asT+bsT\cdot TcoreLb+csT\cdot TcoreLb^2+dsT\cdot TcoreLb^3+esT\cdot TcoreLb\right)^4 \text{ (\%.), and}$$

$$sat_i = satdc_i\cdot satac_i\cdot\frac{satT}{100} \text{ (p.u.).}$$

- Magnetics molypermalloy [33]:

$$satdc_i = \left(1-\frac{Tol\_LBsatdc}{100}\right)\cdot\sqrt{\frac{1+asdc\cdot\mu_r\cdot H\_Lb_i+bsdc\cdot\mu_r^2\cdot H\_Lb_i^2}{1+csdc\cdot\mu_r\cdot H\_Lb_i+dsdc\cdot\mu_r^2\cdot H\_Lb_i^2}} \text{ (p.u.),}$$

$$satac_i = \left(1-\frac{Tol\_LBsatac}{100}\right)\cdot\left(asac+bsac\cdot Bacpk_i+csac\cdot Bacpk_i^2+dsac\cdot Bacpk_i^3\right) \text{ (p.u.),}$$

$$satFs = \left(1-\frac{Tol\_LBsatFs}{100}\right)\cdot\left(\frac{asFs+bsFs\cdot\left(\frac{fs}{10^3}\right)+csFs\cdot\left(\frac{fs}{10^3}\right)^2}{1+dsFs\cdot\left(\frac{fs}{10^3}\right)+esFs\cdot\left(\frac{fs}{10^3}\right)^2}\right)^2 \text{ (p.u.),}$$

$$satT = \left(1-\frac{Tol\_LBsatT}{100}\right)\cdot\left(1+asT\cdot\left(T\_coreLb-25\right)\right) \text{ (p.u.), and}$$

$$sat_i = satdc_i\cdot satac_i\cdot satFs\cdot satT \text{ (p.u.).}$$

- Vector containing the value of the boost inductance in each switching cycle, considering the saturation effect:

$$Lboost_i = AL\min\cdot nturn^2\cdot sat_i.$$

- Vector containing the value of the peak-to-peak ripple of the boost inductor current for each switching cycle. It is obtained by solving the differential equation on the boost inductor current during turn-on of the switch in each switching cycle (see Figures A.10 and A.11):

$$iLripple_i = \frac{vin\_vec_i - VFsw}{Ronsw + Rcopper} \cdot \left(1 - \exp\left(-d\_vec_i \cdot Ts \cdot \frac{Ronsw + Rcopper}{Lboost_i + Lblkg} - \ln\left(1 - \frac{io}{ion\max}\right)\right)\right) - io,$$

where

io : Initial instantaneous current in the switching cycle and

$ion\max$: Maximum possible current during turn - on $= \dfrac{vin\_vec_i - VFsw}{Ronsw + Rcopper}$.

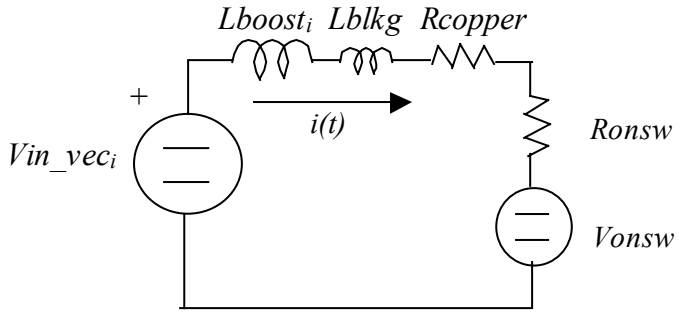
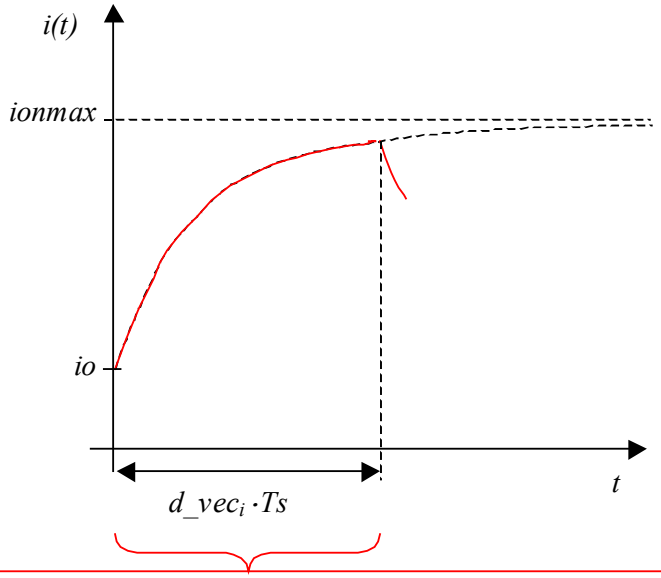


Figure A.10. Turn-on transient topology.



$$vin\_vec_i - Vonsw = (Lboost_i + Lblkg) \cdot \frac{di(t)}{dt} + (Rcopper + Ronsw) \cdot i(t)$$

Figure A.11. Turn-on transient of the current through the boost inductor.

- Vector containing the maximum value of the boost inductor current in each switching period:

$$iL\max_i = iin\_vec_i + \frac{iLripple_i}{2}.$$

- Vector containing the minimum value of the boost inductor current in each switching period (if any of the components of this vector is negative, it is set to zero):

$$iL\min_i = iin\_vec_i - \frac{iLripple_i}{2}.$$

- Computation of rms and average currents:
  - Rms value of the boost inductor current:

$$iL\_rms = \sqrt{Iin\_rms\_sq + ILripple\_rms\_sq},$$
$$Iin\_rms\_sq = \left(\frac{Iin\_pk}{\sqrt{2}}\right)^2, \text{ and}$$
$$ILripple\_rms\_sq = \frac{Ts}{0.5 \cdot Tline} \cdot \sum_i \left(\frac{iLripple_i}{2 \cdot \sqrt{3}}\right)^2.$$

  - Average current through the rectifier diode:

$$Ird\_av = \frac{Iin\_pk}{\pi}.$$

  - Rms current of the rectifier diode:

$$Ird\_rms = iLrms \cdot \frac{1}{\sqrt{2}}.$$

  - Average current through the switch:

$$Isw\_av = \frac{Ts}{0.5 \cdot Tline} \cdot \sum_i \left(d\_vec_i \cdot iin\_vec_i\right).$$

  - Rms current of the switch:

$$Isw\_rms = \sqrt{\frac{Ts}{0.5 \cdot Tline} \cdot \sum_i \left(d\_vec_i \cdot \left(iin\_vec_i^2 + \frac{1}{3} \cdot \left(\frac{iLripple_i}{2}\right)^2\right)\right)}.$$

- Average current through the fast diode:

$$Ifd\_av = \frac{Ts}{0.5 \cdot Tline} \cdot \sum_i \left((1 - d\_vec_i) \cdot iin\_vec_i \right).$$

- Rms current of the fast diode:

$$Ifd\_rms = \sqrt{\frac{Ts}{0.5 \cdot Tline} \cdot \sum_i \left((1 - d\_vec_i) \cdot \left(iin\_vec_i^2 + \frac{1}{3} \cdot \left(\frac{iLripple_i}{2} \right)^2 \right) \right)}.$$

- <u>Computation of losses</u>:

- Average conduction power loss in one rectifier diode:

$$P\_rd = VFrd \cdot Ird\_av + Ronrd \cdot Ird\_rms^2.$$

- Average conduction power loss in the fast diode:

$$P\_fd\_con = VFfd \cdot Ifd\_av + Ronfd \cdot Ifd\_rms^2.$$

- Average power loss due to the reverse recovery of the fast diode during the turn-off of the fast diode:

$$P\_qrr = \frac{2}{Tline} \cdot \sum_i \left(vout_i \cdot (Qrr1 + Qrr2 \cdot iL\min_i) \right).$$

- Total average power loss in the fast diode:

$$P\_fd\_tot = P\_fd\_con + P\_qrr \cdot \left(1 - \frac{Perswqrr}{100} \right).$$

- MOSFET:

. Average conduction power loss:

$$P\_sw\_con = Ronsw \cdot Isw\_rms^2.$$

. Switching loss (refer to Figures A.3 - A.7):

$$\mathrm{var}t12 = Cissh \cdot (Rgon + \mathrm{Re}\,q) \cdot \left(\log(VGG - VT) - \log(VGG - Vp) \right),$$

$$Ig1 = \frac{VGG - Vp}{Rgon},$$

$$\mathrm{var}\,t23_i = \frac{vout_i - Vp}{Ig1} \cdot Crssh\,,$$

$$\mathrm{var}\,t34_i = \frac{Vp - Ronsw \cdot iL\min_i}{Ig1} \cdot Crrsl\,,$$

$$Ig2 = \frac{Vp}{Rgoff}\,,$$

$$\mathrm{var}\,t67_i = \frac{Vp - Ronsw \cdot iL\max_i}{Ig2} \cdot Crssl\,,$$

$$\mathrm{var}\,t78_i = \frac{vout_i - Vp}{Ig2} \cdot Crssh\,,$$

$$\mathrm{var}\,t89 = Cissh \cdot (Rgoff + \mathrm{Re}\,q) \cdot \left(\log(Vp) - \log(VT)\right),$$

$$P\_mos\_on = \frac{2}{Tline} \cdot \sum_i iL\min_i \cdot \left(\frac{\mathrm{var}\,t12}{2} \cdot vout_i + Vp \cdot \mathrm{var}\,t23_i \right.$$
$$\left. + \frac{\mathrm{var}\,t23_i}{2} \cdot \left(vout_i - Vp\right) + \frac{\mathrm{var}\,t34}{2} \cdot \left(Vp - Ronsw \cdot iL\min_i\right) \right),$$

$$P\_mos\_off = \frac{2}{Tline} \cdot \sum_i iL\max_i \cdot \left(\frac{\mathrm{var}\,t89}{2} \cdot vout_i + Vp \cdot \mathrm{var}\,t78_i \right.$$
$$\left. + \frac{\mathrm{var}\,t78_i}{2} \cdot \left(vout_i - Vp\right) + \frac{\mathrm{var}\,t67}{2} \cdot \left(Vp - Ronsw \cdot iL\max_i\right) \right),$$

$$P\_mos\_Coss = \frac{1}{2 \cdot (0.5 \cdot Tline)} \cdot Coss \cdot \sum_i vout_i^2 \text{ , and}$$

$$P\_sw\_switch = P\_mos\_on + P\_mos\_off + P\_mos\_Coss\,.$$

- IGBT:

. Average conduction power loss:

$$P\_sw\_con = VFsw \cdot Isw\_av + Ronsw \cdot Isw\_rms^2 .$$

. Switching loss:

$$P\_igbt\_on = \frac{2}{Tline} \cdot \sum_i \left(Eon \cdot \frac{iL\min_i}{IC\_E} \cdot \frac{vout_i}{VCE\_E} \right),$$

$$P\_igbt\_off = \frac{2}{Tline} \cdot \sum_i \left(Eoff \cdot \frac{iL\max_i}{IC\_E} \cdot \frac{vout_i}{VCE\_E} \right), \text{ and}$$

$$P\_sw\_swit = P\_igbt\_on + P\_igbt\_off .$$

- Total average power loss in the switch:

$$P\_sw\_tot = P\_sw\_con + P\_sw\_switch + P\_qrr \cdot \frac{Perswqrr}{100} .$$

- Boost inductor core losses:

. Vector containing the power density of losses in the boost inductor core for each switching cycle:

- Micrometals iron powder [20]:

$$Pden\_coreLb_i = \left(1 + \frac{Tol\_LBcoreloss}{100}\right) \cdot \frac{fs}{\frac{al}{Bacpk_i^3} + \frac{bl}{Bacpk_i^{2.3}} + \frac{cl}{Bacpk_i^{1.65}}} + \left(dl \cdot fs^2 \cdot Bacpk_i^2\right) \quad \left(\frac{\text{mW}}{\text{cm}^3}\right).$$

- Magnetics High Flux [30]:

$$Pden\_coreLb_i = \left(1 + \frac{Tol\_LBcoreloss}{100}\right) \cdot al \cdot \left(\frac{Bacpk_i}{1000}\right)^{\text{bl}} \cdot \left(\frac{\text{fs}}{1000}\right)^{\text{cl}} \quad \left(\frac{\text{mW}}{\text{cm}^3}\right).$$

- Magnetics Kool Mu [31]:

$$Pden\_coreLb_i = \left(1 + \frac{Tol\_LBcoreloss}{100}\right) \cdot \left(\frac{Bacpk_i}{1000}\right)^{\text{al}} \cdot \left(\frac{\text{fs}}{1000}\right)^{\text{bl}} \quad \left(\frac{\text{mW}}{\text{cm}^3}\right).$$

- Magnetics Mollypermalloy [33]:

$$Pden\_coreLb_i = \left(1+\frac{Tol\_LBcoreloss}{100}\right)\cdot al\cdot\left(\frac{Bacpk_i}{1000}\right)^{bl}\cdot\left(\frac{\text{fs}}{1000}\right)^{cl}\quad\left(\frac{\text{mW}}{\text{cm}^3}\right).$$

. Average (in half a line cycle) power loss in the boost inductor core:

$$P\_coreLb = 10^{-3}\cdot Vc\cdot\frac{1}{0.5\cdot Tline}\cdot\sum_i Pden\_coreLb_i\cdot Ts\qquad(\text{W}).$$

- Boost inductor copper losses:

. High-frequency power lost:

$$P\_copperLbhf = iLripple\_rms\_sq\cdot em\cdot RcoperDC\cdot phi\cdot\left(G1+\frac{2}{3}\cdot\left(em^2-1\right)\cdot\left(G1-2\cdot G2\right)\right)\ (\text{W}).$$

. Low frequency power lost:

$$P\_copperLblf = Rcopper\cdot Iin\_rms\_sq\ \ (\text{W}).$$

. Total average power lost:

$$P\_copperLb = P\_copperLblf + P\_copperLbhf\ \ (\text{W}).$$

- Summary of losses:

$$P\_con = 4\cdot P\_rd + P\_fd\_con + P\_sw\_con,$$
$$P\_switching = P\_qrr + P\_sw\_swit,$$
$$P\_all\_dev = P\_con + P\_switching, \text{ and}$$
$$P\_all = P\_all\_dev + P\_coreLb + P\_copperLb.$$

- Calculated efficiency from 2 to 4 in Figure A.1:

$$eff = 1-\frac{P\_all}{Po+P\_all}.$$

- Temperatures:

- Temperature of the heat sink (the heat sink to which the switch is attached):

$$Ths = Power\_dissipated\cdot Rth\_hs\_amb + Tamb,$$

where *Power_dissipated* refers to the power flowing through the heat sink in each case.

- Calculated junction temperature of the switch:

$$Tjsw = P\_sw\_tot \cdot \left(RSth\_j\_c + RSth\_c\_s\right) + Ths\,.$$

- Junction temperature of the rectifier diode:

$$Tjrd = P\_rd \cdot \left(RRDth\_j\_c + RRDth\_c\_s\right) + Ths\_rd\,.$$

- Junction temperature of the fast diode:

$$Tjfd = P\_fd\_tot \cdot \left(RRDth\_j\_c + RRDth\_c\_s\right) + Ths\_fd\,.$$

- Calculated temperature of the boost inductor core [20]:

$$T\_coreLb = Tamb + TLbcoef \cdot \left[\frac{\left(P\_coreLb + P\_copperLb\right)\cdot 10^3}{Asurf}\right]^{0.833} \quad \text{(C)}\,.$$

- Maximum value of the peak-to-peak ripple in the boost inductor current:

$$dIL\max = \max_{\forall i}\left(iLripple_i\right).$$

- Maximum instantaneous value of the boost inductor current:

$$iL\_pk = \max_{\forall i}\left(iL\max_i\right).$$

- Peak value of the boost inductor core DC magnetizing force:
  - $Hdc\_pk = \max_{\forall i}\left[H\_Lb_i\right]$ (oersteds).

- Peak value of the boost inductor core flux density:

$$Bdc_1 = Brem,$$
$$Bdc_i = Bdc_{i-1} + Lboost_i \cdot \frac{iin\_vec_{i+1} - iin\_vec_i}{nturn \cdot Ac \cdot 10^{-4}} \text{ (T), and}$$
$$Bpk = \max_{\forall i}\left[Bdc_i + Bacpk \cdot 10^{-4}\right] \text{ (T).}$$

where *Brem* is the residual flux density in the core (value of the flux density in the crossing of the B-H curve with the axis H=0).

A.2.3.2. EMI Filter

- **Assumptions:**

a) According to the methodology used to estimate the EMI levels, only one value of the boost inductance needs to be considered. Therefore, the different values of inductance obtained can not be used due to the effect of saturation of the core. The value of the boost inductance will be assumed to be the average value of the inductance along the line cycle considering the saturation.

b) A waveform with constant slopes for the rising and falling edges has been considered for the perturbation source (see Figure A.12). The ringing has not been included.

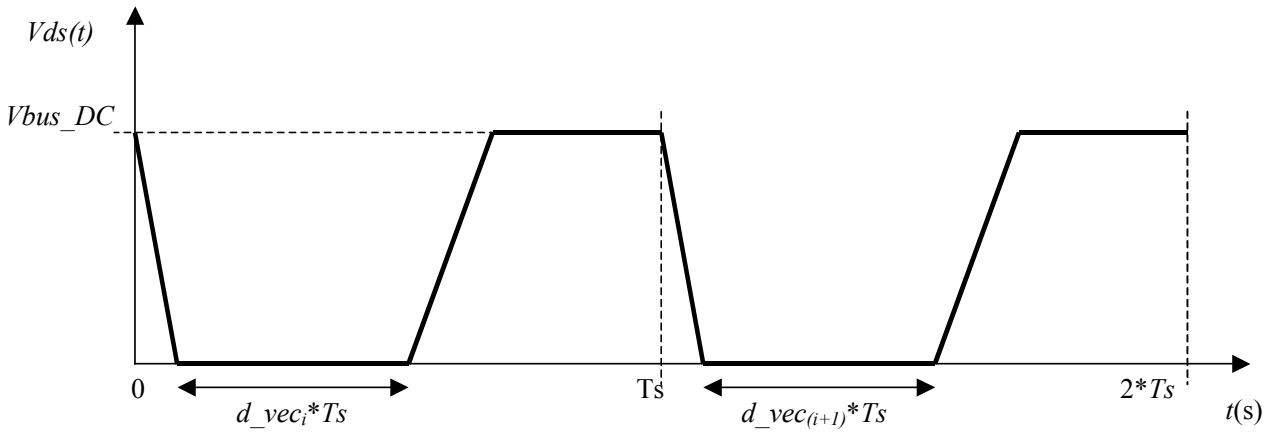


Figure A.12. Time domain evolution of the commutation cell equivalent voltage source.

c) The system configuration between mains and the bridge rectifier is assumed to be symmetrical with respect to ground.

General computation of parameters:

- Vector containing the rise time of the voltage across the MOSFET during turn-off in each switching period:

$$Trise_i = \mathrm{var}\,t78_i .$$

- Vector containing the fall time of the voltage across the MOSFET during turn-on in each switching period:

$$Tfall_i = \mathrm{var}\,t23_i .$$

- Value of boost inductance to be considered:

$$Lb = Lbav = \sum_i \frac{Lboost}{num} .$$

Spectral domain definition:

- Order with respect to the switching frequency of the first and last group of harmonics (at multiples of the switching frequency) to be considered above the initial frequency for which the standard is defined:

$$ord1stlmhgr = ceiling\left(\frac{std_{1,1}}{fs}\right), \text{and}$$
$$ordmaxlmhgr = ord1stlmhgr + nharmgr + 1.$$

- Order with respect to the switching frequency of the first group of harmonics (at multiples of the switching frequency) to be analyzed:

  For the optimization process: $indexharm = ord1stlmhgr$ and

  For design performance report: $indexharm = 1$.

- Harmonic number with respect to the line frequency corresponding to the switching frequency:

$$Fs_{hn} = floor\left(\frac{fs}{fline}\right).$$

- Frequency of the last group of harmonics to be considered:

$$F\max = fs \cdot ordmaxlmhgr\ .$$

- Number of harmonics (multiple of the line frequency) in each group of harmonics (at multiples of the switching frequency) to be considered for the estimation of the EMI levels of each group:

$$lar = 2 \cdot ind\ .$$

- Vector containing the harmonic number (with respect to the line frequency) of the harmonics to be analyzed:

$$\begin{aligned}
Spec = [&a \cdot Fs_{hn} - ind + 1, \ \ldots, \ a \cdot Fs_{hn} - 1, \ a \cdot Fs_{hn}, \ a \cdot Fs_{hn} + 1, \ \cdots, \ a \cdot Fs_{hn} + ind, \ \cdots, \\
&(a+1) \cdot Fs_{hn} - ind + 1, \ \ldots, \ (a+1) \cdot Fs_{hn} - 1, \ (a+1) \cdot Fs_{hn}, \ (a+1) \cdot Fs_{hn} + 1, \ \cdots, \ (a+1) \cdot Fs_{hn} + ind, \ \cdots, \\
&(a+2) \cdot Fs_{hn} - ind + 1, \ \ldots, \ (a+2) \cdot Fs_{hn} - 1, \ (a+2) \cdot Fs_{hn}, \ (a+2) \cdot Fs_{hn} + 1, \ \cdots, \ (a+2) \cdot Fs_{hn} + ind, \ \cdots, \\
&\vdots \\
&b \cdot Fs_{hn} - ind + 1, \ \ldots, \ b \cdot Fs_{hn} - 1, \ b \cdot Fs_{hn}, \ b \cdot Fs_{hn} + 1, \ \cdots, \ b \cdot Fs_{hn} + ind, \ \cdots],
\end{aligned}$$

where

$$a = indexharm \text{ and}$$
$$b = ordmaxlmhgr.$$

This vector contains the harmonic number of those harmonics multiple of the switching frequency to be considered until Fmax, plus several harmonics around all of them.

- Number of harmonics contained in Spec:

$$nharm = length(Spec)\ .$$

- Vector containing the Laplace operator for each harmonic in Spec:

$$p_n = wline \cdot Spec_n \cdot j \qquad \text{n=1,.., nharm.}$$

Computation of the disturbance voltage source (Vpert in Figure A.13) harmonics

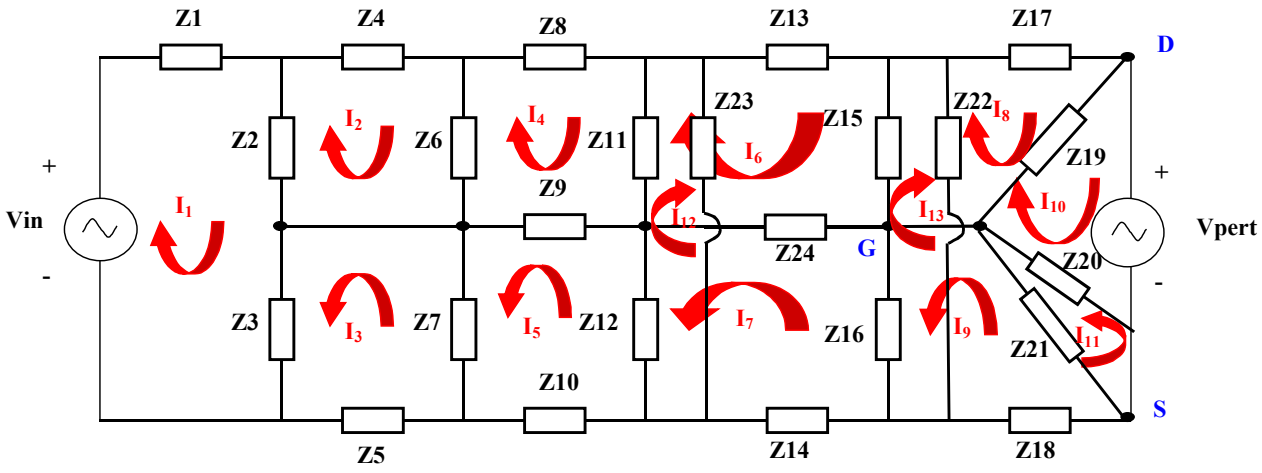


Figure A.13. Equivalent impedance diagram of the whole system (LISN + EMI filter + boost PFC stage).

- Vector containing the *nharm* harmonics specified in *Spec*:

$$C5_n = 2 \cdot fline \cdot \left[\frac{Vbus\_DC}{p_n} \cdot \left(1 - e^{\left(-\frac{Tline}{2} \cdot p_n \right)} \right) + \sum_{k=1}^{num} \left(\frac{vout_k}{Tfall_k \cdot p_n^2} \cdot \left(- e^{-(k-1) \cdot Ts \cdot p_n} + e^{-((k-1) \cdot Ts + Tfall_k) \cdot p_n} \right) + \right. \right.$$

$$\left. \left. + \frac{vout_k}{Trise_k \cdot p_n^2} \cdot \left(e^{-((k-1)+d\_vec_k) \cdot Ts \cdot p_n} - e^{-(((k-1)+d\_vec_k) \cdot Ts + Trise_k) \cdot p_n} \right) \right) \right].$$

- Vector containing the amplitude of the previous harmonics:

$$Mod_n = 2 * \left| C5_n \right| .$$

Computation of the impedance model of the system

- Impedances in Figure A.13:

$$Z1 = Lres \cdot p(n),$$

$$Z2 = Z3 = \frac{1}{C1 \cdot p(n)},$$

$$Z4 = Z5 = LN \cdot p(n),$$

$$Z6 = Z7 = ZN + \frac{1}{CN \cdot p(n)},$$

$$Z8 = Llha \cdot p(n),$$

$$Z9 = Llmg \cdot p(n),$$

$$Z10 = Lldb \cdot p(n),$$

$$Z11 = Z12 = 10^7,$$

$$Z13 = Z14 = Ldm \cdot p(n),$$

$$Z15 = \frac{1}{(Ceg + Cag + Cfy) \cdot p(n)},$$

$$Z16 = \frac{1}{(Cfg + Cbg + Cfy) \cdot p(n)},$$

$$Z17 = \frac{1}{CLb \cdot p(n) + \frac{1}{Lb \cdot p(n)} + \frac{1}{RLb} + Lblkg \cdot p(n)},$$

$$Z18 = Lfs \cdot p(n),$$

$$Z19 = \frac{1}{Cdg \cdot p(n)},$$

$$Z20 = \frac{1}{Csg \cdot p(n)},$$

$$Z21 = \frac{1}{Ckg \cdot p(n)},$$

$$Z22 = Z23 = \frac{1}{Cfx \cdot p(n)}, \text{ and}$$

$$Z24 = Lcm \cdot p(n).$$

- Defining the loop currents indicated in red in Figure A.13 allows for the derivation the impedance matrix (A) related to these loop currents, such that:

$$\vec{V} = [A] \cdot \vec{I},$$

$$\vec{I} : Vector\_of\_loop\_currents = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{13} \end{bmatrix}, \text{ and}$$

$$\vec{V} : Vector\_of\_loop\_voltage\_sources = \begin{bmatrix} V_1 = Vin \\ 0 \\ \vdots \\ 0 \\ V_{10} = -Vpert \\ 0 \\ \vdots \\ 0 \end{bmatrix}.$$

- Diagonal elements of the impedance matrix (A), descriptive of the system in Figure A.13:

$$ZC1 = Z1 + Z2 + Z3,$$
$$ZC2 = Z2 + Z4 + Z6,$$
$$ZC3 = Z3 + Z5 + Z7,$$
$$ZC4 = Z6 + Z8 + Z9 + Z11,$$
$$ZC5 = Z7 + Z9 + Z10 + Z12,$$
$$ZC6 = Z11 + Z13 + Z15 + Z24,$$
$$ZC7 = Z12 + Z14 + Z16 + Z24,$$
$$ZC8 = Z15 + Z17 + Z19,$$
$$ZC9 = Z16 + Z18 + Z20,$$
$$ZC10 = Z19 + Z20,$$
$$ZC11 = Z20 + Z21,$$
$$ZC12 = Z11 + Z12 + Z23, \text{ and}$$
$$ZC13 = Z15 + Z16 + Z22.$$

- Impedance matrix A:

A_n= [ZC1 -Z2 Z3 0 0 0 0 0 0 0 0 0 0;
-Z2 ZC2 0 -Z6 0 0 0 0 0 0 0 0 0;
Z3 0 ZC3 0 -Z7 0 0 0 0 0 0 0 0;
0 -Z6 0 ZC4 Z9 -Z11 0 0 0 0 0 -Z11 0;
0 0 -Z7 Z9 ZC5 0 -Z12 0 0 0 0 Z12 0;
0 0 0 -Z11 0 ZC6 Z24 -Z15 0 0 0 Z11 -Z15;
0 0 0 0 -Z12 Z24 ZC7 0 -Z16 0 0 -Z12 Z16;
0 0 0 0 0 -Z15 0 ZC8 0 -Z19 0 0 Z15;
0 0 0 0 0 0 -Z16 0 ZC9 Z20 Z20 0 -Z16;
0 0 0 0 0 0 0 -Z19 Z20 ZC10 Z20 0 0;
0 0 0 0 0 0 0 0 Z20 Z20 ZC11 0 0;
0 0 0 -Z11 Z12 Z11 -Z12 0 0 0 0 ZC12 0;
0 0 0 0 0 -Z15 Z16 Z15 -Z16 0 0 0 ZC13]

Computation of EMI filter capacitor currents and EMI levels

- Vector containing the voltage sources in the model of Figure A.13 for the harmonic n of frequency higher than the line frequency:

$$V_h = 0 \qquad \forall h \neq 10, \text{ and}$$

$$V_{10} = -C5_n .$$

- Matrix containing all the loop currents in Figure A.13 for the harmonics of order n:

$$R_{\ldots,n} = A_n^{-1} \cdot V_h .$$

- Variables containing the rms current of the EMI filter capacitors Cx and Cy (only computed when a design report is required):

Capacitors Cx: $ICfx1\_rms, ICfx2\_rms$ and

Capacitors Cy: $ICfy1\_rms, ICfy2\_rms$.

- LISN leg current harmonic of order n:

$$Ihf = R_{2,n} - R_{4,n} - \left(R_{5,n} - R_{3,n}\right) \cdot e^{-\frac{Tline}{2} \cdot p_n} .$$

- Vector containing the magnitude of the voltage harmonics generated in LISN leg resistance (ZN):

$$MIhf_n = \left| Ihf \cdot ZN \right| .$$

- Vector containing the square root of the quadratic sum of the odd harmonics of $Mihf_n$ around each multiple of the switching frequency, corresponding to differential mode disturbance (harmonic group numbers from *indexharm* to *ordmaxlmhgr*), adding *incr* dBμV:

$$HDQuad_m \text{ (dBμV)}.$$

- Vector containing the square root of the quadratic sum of the even harmonics of $Mihf_n$ around each multiple of the switching frequency, corresponding to common mode

disturbance (harmonic group numbers from *indexharm* to *ordmaxlmhgr*), adding *incr* dBμV:

$$HCQuad_m \text{ (dBμV)}.$$

- Vector containing the square root of the quadratic sum of all harmonics of $Mihf_n$ around each multiple of the switching frequency, corresponding to the total noise (harmonic group numbers from *1* to *ordmaxlmhgr*). Strictly, these total noise levels are the ones that should be smaller than the maximum levels specified by the standard. This vector is only computed when a design report is required.

$$HQuad_m \text{ (dBμV)}.$$

- Vector containing the required level in the LISN resistor voltage specified by the standard at each multiple of the switching frequency (from *ord1stlmhgr·fs* to *ordmaxlmhgr·fs*):

$$\mathrm{Re}\,q\_Level_q \text{ (dBμV)}.$$

- Vector containing the required attenuation in the LISN resistor voltage corresponding to differential mode noise in order for the harmonic group numbers from *ord1stlmhgr* to *ordmaxlmhgr* to meet the standard (the differential noise level must be less than the standard level expressed in V divided by $\sqrt{2}$ or, what is equivalent, the standard level expressed in dBμ minus 3 dB). The required attenuation is expressed in a per unit value:

$$\mathrm{Re}\,q\_DM\_att_q = \frac{HDQuad_m}{\mathrm{Re}\,q\_Level_q - 3} - 1 \text{ (p.u.)}.$$

- Vector containing the required attenuation in the LISN resistor voltage corresponding to common mode noise in order for the harmonic group numbers from *ord1stlmhgr* to *ordmaxlmhgr* to meet the standard (the common noise level must be less than the standard level expressed in V divided by $\sqrt{2}$ or, what is equivalent, the standard level expressed in dBμ minus 3 dB). The required attenuation is expressed in a per unit value:

$$\mathrm{Re}\,q\_CM\_att_q = \frac{HCQuad_m}{\mathrm{Re}\,q\_Level_q - 3} - 1 \text{ (p.u.)}.$$

A.2.3.3. Continuous optimization calculations

In the continuous optimization approach, the calculations are essentially analogous to the discrete approach, with the following additions:

- Core mean magnetic path length:

$$lm = \pi \cdot \left(\frac{OD - ID}{2} \right) \text{ (cm)}.$$

- Core cross-section area:

$$Ac = Ht \cdot \left(\frac{OD - ID}{2} \right) \text{ (cm)}.$$

- Core volume:

$$Vc = \left(OD^2 - ID^2 \right) \cdot Ht \cdot \frac{\pi}{4} \text{ (cm}^3\text{)}.$$

- Mean length per turn:

$$MLT = 2 \cdot Ht + \left(OD - ID \right) \text{ (cm)}.$$

- Window area:

$$Wa = \pi \cdot \frac{ID^2}{4} \text{ (cm}^2\text{)}.$$

- Inductance rating of the core:

$$AL = 10^{-2} \cdot uo \cdot ur \cdot \frac{Ac}{lm} \left(\frac{\text{H}}{\text{turn}^2} \right)$$
$$\left(uo = 4 \cdot \pi \cdot 10^{-7} \right).$$

- Wire diameter:

$$Dw = \sqrt{\frac{4 \cdot Aw}{\pi}} \text{ (cm)}.$$

- Parasitic (resulting from leakage) differential mode inductance of the common mode choke. Assumed to be 0.2% of the common mode inductance:

$$Ldm = 0.002 \cdot Lcm \ \ (\text{cm}).$$

A.2.4. Cost Function

The cost function to be minimized by the optimizer refers to the total cost of the design expressed in m.u. It is the first component of the response vector that the function provides as an output. It is as follows:

resp(1) = *Cost_HS*+*Cost_Lbcore*+*Cost_Lbfixwiring*+*Cost_Lbvarwiring*+*Cost_choke*+

+2**Cost_Cx*+2**Cost_Cy*+Cost_Cb+*Cost_switch*+*Cost_fastdiode*+4**Cost_rectdiode*.

- Boost inductor wire and manufacturing cost:

$$Cost\_Lbwire\_and\_manuf = Cost\_Lbfixwiring + Cost\_Lb\,\text{var}\,wiring$$
$$Cost\_Lb\,\text{var}\,wiring = Cost\_Lbwire \cdot nturn \cdot MLT.$$

If anyone of the coefficients *Cost_Lbfixwiring* or *Cost_Lbwire* is not directly available, the following procedure can be used to obtain an estimation of its value.

a) Select a set of boost inductors for which the total cost and the cost of the core is known. Calculate the wire and manufacturing cost by subtracting the cost of the core to the total cost. Additionally, calculate the volume of wire used in each boost inductor. In Table A.28, an example is shown.

Table A.28. Breakdown of the cost of several boost inductors.

Boost inductor	**Total cost (m.u.)**	**Cost core (m.u.)**	**Cost_Lbwire_and_manuf =Total Cost-Cost Core (m.u.)**	**Wire volume =Aw.nturn.MLT (cm^3)**
1	49.6	10.528	39.072	4.713
2	52.8	10.528	42.272	4.713
3	33.6	4.704	28.896	7.326
4	62.4	10.528	51.872	11.781
5	52.48	10.528	41.952	8.659
6	53.76	10.528	43.232	12.242
7	57.28	10.528	46.752	15.526

b) Approximate the wire and manufacturing cost by a first order polynomial function of the wire volume. For instance, in the previous example:

$$Cost\_Lbwire\_and\_manuf = K1 + K2 \cdot Volume\_wire\left(cm^3\right) \text{ (m.u.)},$$

$K1 = 35.2\ m.u.$, and

$$K2 = 0.736\ \frac{m.u.}{cm^3}.$$

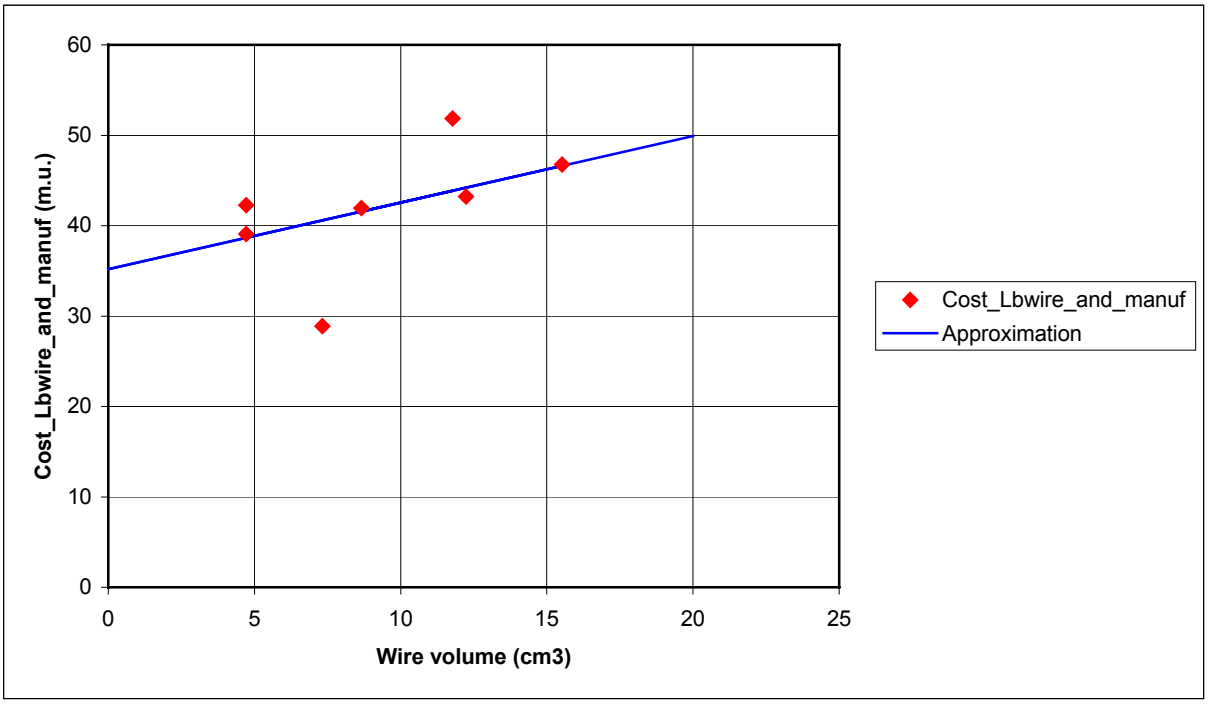


Figure A.14. Cost of the boost inductor wire and manufacturing and its approximation by a first-order polynomial function of the wire volume.

c) Finally, the coefficients sought can be estimated to be:

$$Cost\_Lbfixwiring = K1 \text{ (m.u.), and}$$

$$Cost\_Lb\,\text{var}\,wiring = K2 \cdot Aw\left(cm^2\right)\left(\frac{\text{m.u.}}{\text{cm}}\right).$$

- Cost of the heat sink:

The cost of the heat sink has been approximated by means of a polynomial function based on the cost information available. The cost of the heat sink has been assumed to be a function of its

thermal resistance to the ambient. In Table A.29, the cost information of several heat sinks specifying their thermal resistance is presented.

Table A.29. Thermal resistance heat sink-to-ambient and cost for several heat sinks.

Heat sink	
Rth_HS	*Cost* (m.u.)
7.8	4.64
5.3	4.96
3.7	5.28

Heat sink	
Rth_HS	*Cost* (m.u.)
2.3	17.6
1.4	25.92
0.7	57.6

In Figure A.15, this cost information is plotted as a function of the thermal resistance heat sink to ambient (dots).

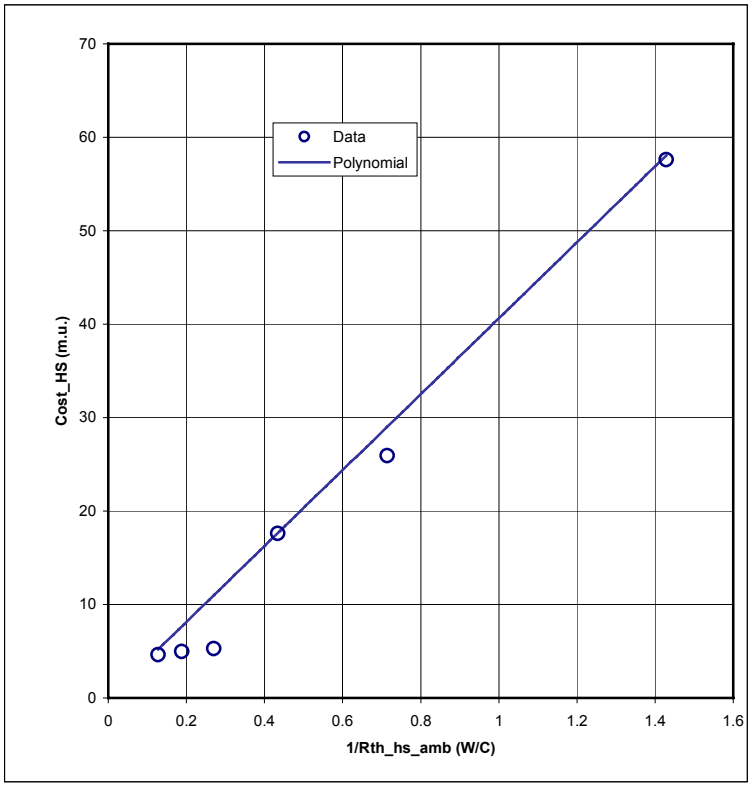


Figure A.15. Heat sink cost as a function of the inverse of the thermal resistance and polynomial approximation.

The function that approximates this data is also plotted in Figure A.15 (continuous line). The expression for this function is:

$$Cost\_HS = K1HS + K2HS*(1/Rth\_hs\_amb),$$

$$K1HS = 0 \text{ (m.u.), and}$$

$$K2HS = 40.64 \text{ (m.u.*C/W).}$$

A.2.4.1. Additional Cost Estimations for Continuous Optimization

In the continuous optimization approach, the cost of the boost inductor core, the cost of the common mode choke, and the cost of the two EMI filter capacitors must be estimated as a function of the corresponding design variables. This cost approximation has been performed by means of polynomial functions based on the cost information available, as shown next.

- Cost of the boost inductor core:

The cost of the boost inductor core has been assumed to be a function of the volume of the core. In Table A.30, the cost information of several iron powder cores specifying their volume is presented.

Table A.30. Volume and cost of several boost inductor cores.

L_B core	
Vc (cm^3)	*Cost* (m.u.)
2.16	1.536
4.28	2.304
3.55	2.112
5.78	2.88
6.84	3.456
6.41	3.264
6.16	3.072
8.31	4.032
10.7	4.992

L_B core	
Vc (cm^3)	*Cost* (m.u.)
15	6.528
21	9.024
16.4	7.296
33.2	13.824
20.7	8.832
52.3	21.696
57.4	24
33.4	14.016
86.4	36.096

In Figure A.16, this cost information is plotted as a function of the volume of the core (dots).

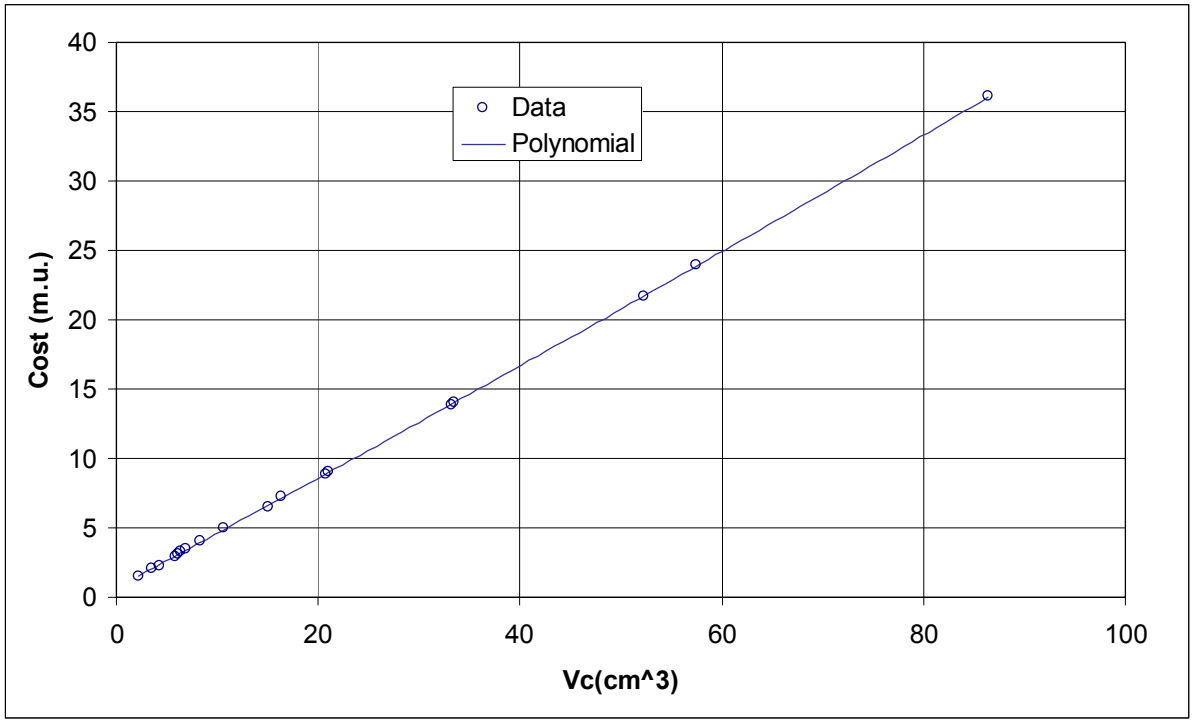


Figure A.16. Boost inductor cost as a function of the volume of the core and polynomial approximation.

The function that approximates this data is also plotted (continuous line). The expression for this function is:

$$Cost\_Lbcore = K1Lbc + K2Lbc * Vc + K3Lbc * Vc^2,$$

K1Lbc = 0.7008,

K2Lbc = 0.3904, and

K3Lbc = 0.000216.

- Cost of the common mode choke:

The cost of the common mode choke has been assumed to be a function of the common mode inductance (*Lcm*) of the component (for a given value of the rated rms current). In Table A.31, the cost information available at the time the approximation was performed is presented (only cores of 7.5 maximum rms current have been considered).

Table A.31. Common mode inductance and cost of several common mode chokes.

Common mode choke	
Lcm (H)	*Cost* (m.u.)
1.50E-03	20.8
3.30E-03	31.2

Since at that time there were only two data points available, the cost of the common mode choke was approximated by a straight line passing through them:

Cost_Lcm = K1Lcm+K2Lcm**Lcm*,

K1Lcm = 12.13, and

K2Lcm = 5777.78.

- Cost of the capacitor Cx:

The cost of the capacitor Cx has been assumed to be a function of its capacitance. In Table A.32, the cost information of several capacitors specifying their capacitance is presented.

Table A.32. Capacitance and cost of several differential mode capacitors.

Capacitor Cx	
Cfx (F)	*Cost* (m.u.)
2.20E-07	1.856
3.30E-07	2.176
4.70E-07	2.496
1.00E-06	3.52
2.20E-06	9.28

In Figure A.17, this cost information is plotted as a function of the capacitance (dots).

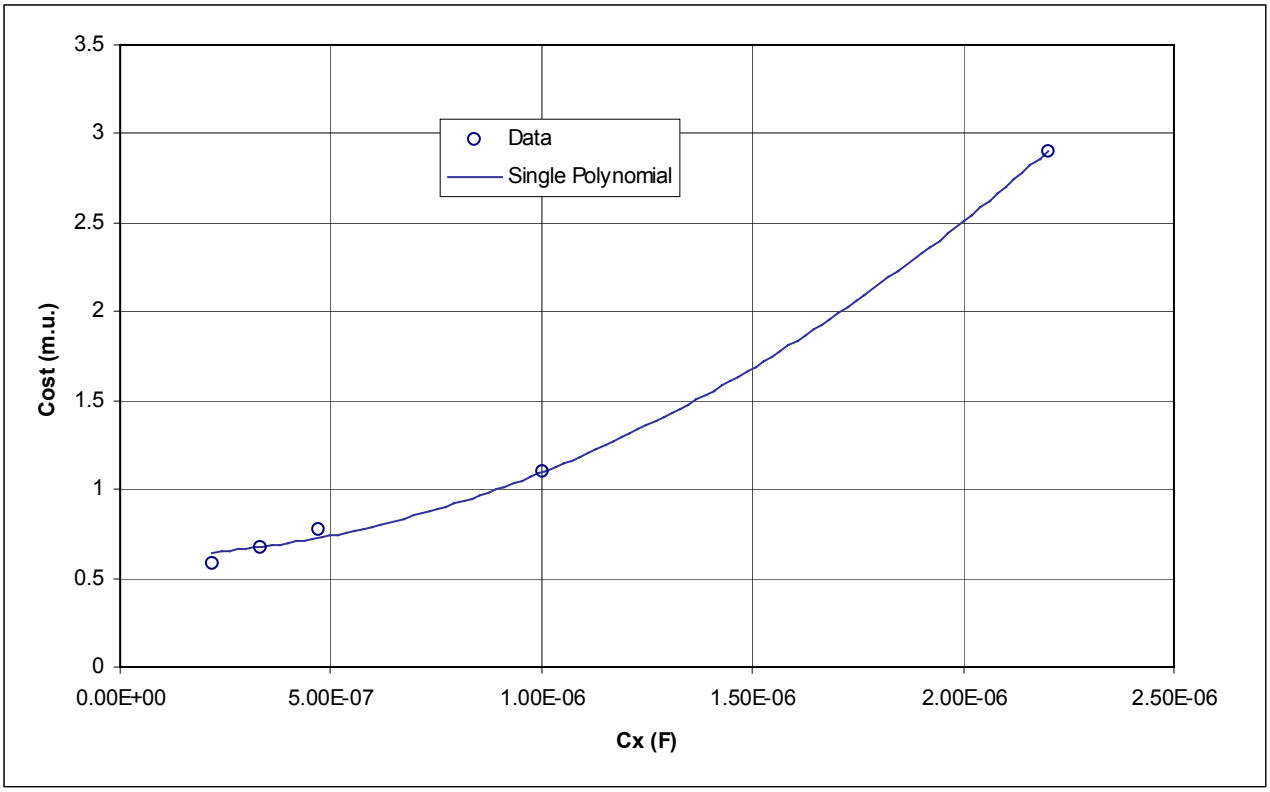


Figure A.17. Differential mode capacitor cost as a function of the capacitance and polynomial approximation.

The function that approximates this data is also plotted (continuous line). The expression for this function is:

$$Cost\_Cx = K1Cx + K2Cx * Cfx^2,$$

K1Cx = 1.9904, and

K2Cx = 1.51e+12.

- Cost of the capacitor Cy:

The cost of the capacitor Cy has been assumed to be a function of its capacitance. In Table A.33, the cost information of several capacitors specifying their capacitance is presented.

Table A.33. Capacitance and cost of several common mode capacitors.

Capacitor Cy	
Cfy (F)	*Cost* (m.u.)
4.70E-09	1.248
1.00E-08	1.472
4.70E-08	2.528
1.00E-07	3.584
3.30E-07	7.968

In Figure A.18, this cost information is plotted as a function of the capacitance (dots).

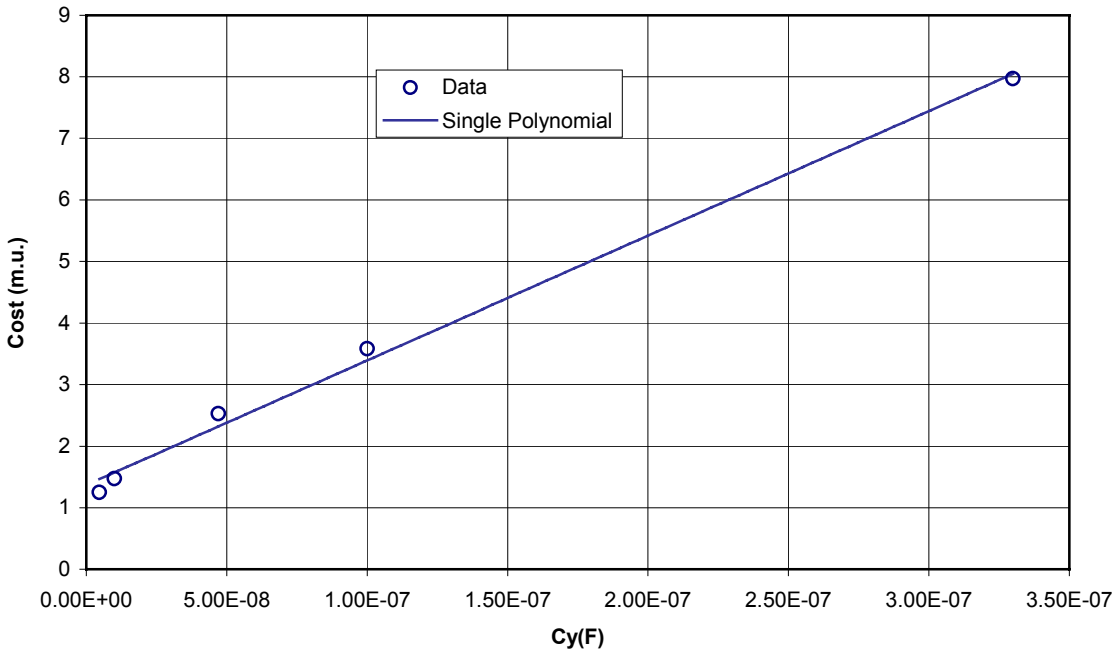


Figure A.18. Common mode capacitor cost as a function of the capacitance and polynomial approximation.

The function that approximates this data is also plotted (continuous line). The expression for this function is:

$$Cost\_Cy = K1Cy + K2Cy * Cfy,$$

$$K1Cy = 1.3696, \text{ and}$$

$$K2Cy = 2024e4.$$

A.2.5. Constraints

All the values of the constraints constitute the rest of the components of the response vector of the function (the value of the cost function is the first component of this vector). These constraints are normalized and expressed in such a way that if the corresponding component of the response vector obtained is negative then the constraint is not violated. If it is positive, the constraint is violated.

The constraints considered are the following (notice that their position in the response vector (resp) is also specified).

- The maximum peak-to-peak current ripple in the boost inductor cannot be higher than 150% of the peak average (in a switching period) input current. This constraint is set to limit the amount of time the converter is operating in discontinuous current mode:

$$resp_2 = \frac{dIL\max}{1.5 \cdot Iin\_pk} - 1.$$

- Temperature constraints:
  - The junction temperature of the switch should be lower than its maximum:

$$resp_3 = \frac{Tjsw}{T\max sw} - 1.$$

  - The temperature of the heat sink should be lower than its maximum:

$$resp_4 = \frac{Ths}{T\max HS} - 1.$$

  - The temperature of the boost inductor core should be lower than its maximum:

$$resp_5 = \frac{T\_coreLb}{\min\left(T\_coreLb\max, T\max wire, T\max PCB + dT\_pcb\_Lbcore\right)} - 1.$$

  - The junction temperature of the fast diode should be lower than its maximum:

$$resp_6 = \frac{Tjfd}{T\max fd} - 1.$$

- The junction temperature of the rectifier diode (or rectifier bridge) should be lower than its maximum:

$$resp_7 = \frac{Tjrd}{T\max rd} - 1.$$

- Voltage rating constraints:
  - The breakdown voltage of the MOSFET should exceed the minimum required breakdown voltage:

$$resp_8 = 1 - \frac{Vpksw}{VpkM\min}.$$

  - The breakdown voltage of the IGBT should exceed the minimum required breakdown voltage:

$$resp_8 = 1 - \frac{Vpksw}{VpkIG\min}.$$

  - The breakdown voltage of the fast diode should exceed the minimum required breakdown voltage:

$$resp_9 = 1 - \frac{Vpkfd}{Vpkfd\min}.$$

  - The breakdown voltage of the rectifier diode should exceed the minimum required breakdown voltage:

$$resp_{10} = 1 - \frac{Vpkrd}{Vpkrd\min}.$$

  - The maximum AC (rms) voltage of the differential mode capacitor Cx should exceed the minimum required AC (rms) voltage:

$$resp_{11} = 1 - \frac{VacCx}{VacCx\min}.$$

  - The maximum AC (rms) voltage of the common mode capacitor Cy should exceed the minimum required AC (rms) voltage:

$$resp_{12} = 1 - \frac{VacCy}{VacCy\,\min}.$$

- Current rating constraints:
  - The rms current in the MOSFET cannot exceed the maximum allowed rms current:

$$resp_{13} = \frac{Isw\_rms}{Iswrms\,\max} - 1.$$

  - The average current in the IGBT cannot exceed the maximum allowed average current:

$$resp_{13} = \frac{Isw\_av}{Iswav\,\max} - 1.$$

  - The average current in the fast diode cannot exceed the maximum allowed average current:

$$resp_{14} = \frac{Ifd\_av}{Ifdav\,\max} - 1.$$

  - The average current in the rectifier diode cannot exceed the maximum allowed average current:

$$resp_{15} = \frac{Ird\_av}{Irdav\,\max} - 1.$$

  - The maximum surge current that the fast diode is able to withstand should exceed the maximum surge current determined for the system:

$$resp_{16} = 1 - \frac{IFSMfd}{IFSM\,\min}.$$

  - The maximum surge current that the rectifier diode is able to withstand should exceed the maximum surge current determined for the system:

$$resp_{17} = 1 - \frac{IFSMrd}{IFSM\,\min}.$$

- The rms current through the common mode choke cannot exceed the maximum allowed rms current:

$$resp_{18} = \frac{iL\_rms}{ICHrms\_\max} - 1.$$

- The peak value of the flux density in the boost inductor core cannot exceed the maximum value defined for its material.

$$resp_{19} = \frac{Bpk}{B\max(cid2)} - 1.$$

- The current density in the boost inductor wire cannot exceed the maximum current density defined for the copper:

$$resp_{20} = \frac{\left(\frac{iL\_rms}{Aw}\right)}{Jm} - 1.$$

- The wire should fit in the available window area of the core, according to the filling factor (Ku) considered. The cross-section of the wire is considered to be a square of side the diameter of the wire (conservative assumption):

$$resp_{21} = \frac{nturn \cdot Dw^2}{Ku \cdot Wa} - 1.$$

- The differential mode disturbance level for each of the *nharmgr* group of harmonics around a multiple of the switching frequency considered above the minimum frequency where the standard limits are defined should be lower than the standard level defined for its frequency divided by the square root of two:

$$\text{resp}_{22} = \max_{\forall m}\left(\text{Re}q\_DM\_att_m\right) = \frac{HDQuad_m}{\left(\text{Re}q\_Level_q - 3\right)} - 1.$$

- The common mode disturbance level for each of the *nharmgr* group of harmonics around a multiple of the switching frequency considered above the minimum frequency where

the standard limits are defined should be lower than the standard level defined for its frequency divided by the square root of two:

$$resp_{23} = \max_{\forall m}\left(\mathrm{Re}\, q\_CM\_att_m\right) = \frac{HCQuad_m}{\left(\mathrm{Re}\, q\_Level - 3\right)} - 1.$$

If the previous two constraints are satisfied, then the total EMI noise level will be smaller than the standard limits.

Constraints $resp_8$ to $resp_{12}$, $resp_{16}$ and $resp_{17}$ are essentially boundaries for the design variable parameters that can be checked initially without requiring an analysis of the design. Therefore, in the OPES software all components are checked in the beginning and those not meeting these constraints are discarded.

- Special boundaries on the design variables:

  - Switching frequency boundaries:

$$20kHz \le fs \le 150kHz.$$

  - Number of turns boundary:

$$nturn \ge 1.$$

  - Heat sink thermal resistance boundary:

$$Rth\_hs\_amb > 0.$$

A.2.5.1. Continuous Optimization Constraints

In the continuous optimization approach, the constraints are essentially the same as in the discrete, except for the following.

- There is no need to check in the analysis the constraints related to $resp_8$ to $resp_{12}$, $resp_{16}$ and $resp_{17}$. By choosing the appropriate fixed devices, these constraints will be met.

- Additional constraint: The internal diameter of the core must be at least 0.5 cm smaller than the external diameter:

$$resp = 1 - \frac{(OD - ID)}{0.5}.$$

- Boundaries on the design variables:

$$ID, OD, Ht, Lcm, Cfx, Cfy \geq 0,$$
$$nturn \geq 1,$$
$$Aw \geq 0.0202 \cdot 10^{-3}\, cm^2,$$
$$Rth\_hs\_amb \geq 0.1,$$
$$20\ kHz \leq fs \leq 150\ kHz, \text{ and}$$
$$Cfy \leq 10^{-8}\ \text{F}.$$

A.2.6. User Guide to Run the MATLAB Analysis Program

Before using the program, the files "Danalyze.m", "Boost_analysis.m", "Zmodel.m" and "Ddesigndata.m" must be placed in the default folder used by MATLAB or the user should go to *File>Set Path* and specify the folder where these files have been placed. Once this is done, the file "Ddesigndata.m" must be edited to introduce the design variable parameter values. Each design variable is defined as a vector of parameters. In Section A.2.2, these design variables are presented, and their parameters are specified in the same order as they must be introduced in the vectors of the file "Ddesigndata.m." An example of input vectors containing the values of the different parameters that define the design variables can be found in this file. Once this information is edited, the file must be saved and run from the MATLAB environment by typing:

```
Ddesigndata .
```

(In this file not only are the design variable parameters introduced, but also the function "Danalyze" is called, so that the analysis of the design is performed.)

A design report including several plots will appear if the internal constant aff of the function "Danalyze" is set to 1. For a description of the information presented in the report, please refer to the OPES software User Manual. If aff is set to a value different from 1, only the vector *resp* containing the responses of the analysis will be echoed in the screen. This vector contains in its first component the estimated cost of the design in m.u. and, in all the others, the value of the constraints (refer to Sections A.2.4 and A.2.5 for more information). A negative value of the constraints means that the limit specified by the constraint has not been reached. A positive value means that it has been surpassed.

To modify any of the constants or equations previously described in the appendix, edit the file "Danalyze.m."

A.2.6.1. Continuous Optimization

In the continuous optimization approach, the guidelines for editing the design variable information and running the MATLAB analysis program are analogous to those previously presented. In this case, however, the corresponding files are: "Canalyze.m," "Boost_analysis.m," "Zmodel.m," and "Cdesigndata.m." To run the design analysis, we must now type:

```
Cdesigndata .
```

A.3. Possible Model Improvements and Extensions

In this section, some possible modifications to the component parameter definition in order to extend the capabilities of the software design tool developed will be discussed.

A.3.1. Boost Inductor Core

In the OPES software design tool, only toroidal cores can be considered. The toroidal shape was assumed to be the most cost-effective solution. However, if there was an interest in considering other core shapes, some modifications should be introduced. First of all and in general, a new continuous design variable should be introduced, i.e., the gap of the core, because some of the core shapes present this geometrical parameter as a design variable. The core parameters should also be modified, so that they are appropriate for the different core shape options. In Table A.34, a definition of these parameters is proposed.

Table A.34. Proposed new definition of the boost inductor core parameters.

Parameter name	**Description**	**Units**
Cost_Lbcore	Cost of the boost inductor core	m.u.
Cid1	Integer value to codify the core shape	-------
Cid2*	Integer value to codify the manufacturer-core material	-------
Cid3	Integer value to codify the types of core within a material defined in cid1, typically the different permeabilities possible	-------
AL	Inductance rating of the core (nH for one turn ≡ mH for 1000 turns)	nH/(turn^2) ≡ mH/(1000_turn^2)
TolAL	Tolerance of the value of AL	%

Dim1	Parameter 1 to specify a characteristic dimension of the core shape geometry	cm
Dim2	Parameter 2 to specify a characteristic dimension of the core shape geometry	cm
⋮	⋮	⋮
Dim10	Parameter 10 to specify a characteristic dimension of the core shape geometry	cm
lm	Mean magnetic path	cm
Ac	Cross-sectional area of the core	cm^2
Vc	Volume of the core	cm^3
MLT	Mean length per turn (In the case of the Micrometals catalog, this value can be obtained from pages 60-61.)	cm
T_coreLbmax	Maximum temperature of the core	°C

* Since shapes that can be gapped can be included, ferrite will now become a possible choice for the material.

With this parameter definition, the user should be able to include as many core shapes and materials as desired by simply modifying the Fortran design analysis code. No modification to the graphical user interface would be required.

A.3.2. Capacitors and Common Mode Choke

Among the design parameters for the capacitors and common mode choke, the equivalent series resistance (ESR) should be specified, so that the power lost in the component can be computed by simply multiplying this resistance by the rms current through the component. This power lost would then modify the estimation of the overall input power required for a given output power. If a thermal resistance for the component were provided, it could also be included as a parameter so that the temperature rise in the component could be estimated by simply multiplying this thermal resistance to the power lost in the component. Then, by adding the

ambient temperature, the temperature of the component could be predicted and a new constraint added that specified the limit on this temperature. This constraint would naturally replace the constraint specifying the maximum component rms current, since this constraint was set to indirectly specify the maximum temperature of the component. In this case, the component parameter specifying the maximum rms current for a given ambient temperature should be replaced by the maximum temperature of the component.

Appendix B. Experimental Verification of the Design Analysis Function Predictions

This appendix presents the tuning and prediction validation of the models by means of experimental testing for two different prototypes. The first experimental test for each prototype is used to tune the core temperature prediction by adjusting the value of the parameter TLbcoef. Also, the switch collector-to-ground parasitic capacitance (C_{DG}) is measured to adjust the common mode noise predictions in the software. The common mode noise level is significantly sensitive to the value of this parasitic.

Three different prediction values are presented for the different magnitudes investigated: *non-conservative*, *average* and *conservative*. Based on the tolerances provided by the manufacturer, these different prediction values have been obtained considering the following deviations with respect to the nominal values, and are shown in Table B.1.

Table B.1. Deviation with respect to the nominal value of different parameters and magnitudes.

Deviation (% with respect to nominal value)	Prediction		
	Non-conservative	Average	Conservative
AL	+10	0	-10
Percent permeability vs. dc magnetizing force	+10	0	-10
Percent permeability vs. ac magnetizing force	+10	0	-10
Core loss vs. peak ac flux density	-15	0	+15
Capacitance Cx	+10	0	-10
Capacitance Cy	+20	0	-20
Common mode choke inductance Lcm	+30	0	-30

B.1. Prototype 1

B.1.1. TEST 1: Model Tuning Test

Table B.2. Conditions.

Parameter	Value
Tamb_ext	23 °C
Tamb_prot*	28 °C
Vin	180 Vrms
fline	50 Hz
Po	1155 W
Vo	368 V

* This is the assumed value.

Table B.3. Measures and predictions.

Magnitude	Measured	Predicted		
		Non-conservative	Average	Conservative
Pin (W) *	1217÷1224	1203	1205	1208
Iin_rms (A) *	6.83	6.70	6.74	6.79
iL_pk (A) *	11.16	10.68	11.12	11.80
dILmax (A) Δ	4.35	2.49	3.34	4.67
Lb_min (μH)	636	863	647	471
T_coreLb (°C)	165	147	160	172
Ths_sw (°C)	78	77.3	78.0	79.2
Ths_fd (°C)	45	46.4	46.4	46.4
Ths_rd (°C)	135	134.9	135.2	135.8
C_{DG} (pF)	9	---	---	---

* The predictions do not include the power dissipated in both the PFC stage EMI filter, measured ≈ 8.9W, and load internal EMI filter and electrolytic capacitors, measured ≈ 3÷6W, globally estimated to be between 11.9 and 14.9W.
Δ Without ringing amplitude, measured ≈ 0.6 A; Setting TL_Bcoef = 1.3.

B.1.2. TEST 2: Modification of the Boost Inductor Number of Turns

Table B.4. Conditions: Modified L_B is T225-26 with **75 turns.**

Parameter	Value
Tamb_ext (^oC)	23
Tamb_prot*	28 ^oC
Vin (V)	180
Fline (Hz)	50
Po (W)	1154
Vo (V)	368.5

* This is the assumed value.

Table B.5. Measures and predictions.

Magnitude	Measured	Predicted		
		Non-conservative	Average	Conservative
Pin (W)*	1234	1210	1215	1219
Iin_rms (A)*	6.87	6.76	6.82	6.9
iLb_pk (A)	12.76	11.08	11.66	12.55
dILbmax (A)	5.83	3.20	4.30	6.01
Lb_min (µH)	444.06	675	505	367
T_coreLb (^oC)	199	192	213	233
Ths _sw (^oC)	76	78.2	79.3	80.9
Ths _fd (^oC)	49	46.5	46.5	46.6
Ths _rd (^oC)	131	135.7	136.4	137.3

* The predictions do not include the power dissipated in the PFC stage EMI filter, load internal EMI filter and electrolytic capacitors.

B.1.3. TEST 3: Modification of the Switching Frequency

Table B.6. Conditions: Modified switching frequency **Fs = 55 kHz.**

Parameter	Value
Tamb_ext (°C)	23
Tamb_prot*	34 °C
Vin (V)	180
Fline (Hz)	50
Po (W)	1156
Vo (V)	368.7

* This is the assumed value.

Table B.7. Measures and predictions.

Magnitude	Measured	Predicted		
		Non-conservative	Average	Conservative
Pin (W)*	1230	1204	1206	1209
Iin_rms (A)*	6.85	6.70	6.72	6.76
iLb_pk (A)	11.48	10.35	10.68	11.17
dILbmax (A)	3.08	1.81	2.43	3.40
Lb_min (µH)	615	754	565	412
T_coreLb (°C)	131	133	142	151
Ths _sw (°C)	100	100.1	100.9	102.2
Ths _fd (°C)	55	54.8	54.8	54.8
Ths _rd (°C)	131	141.0	141.2	141.6

* The predictions do not include the power dissipated in the PFC stage EMI filter, load internal EMI filter and electrolytic capacitors.

B.1.4. TEST 4: Variation in the Output Power

Table B.8. Conditions.

Parameter	Value
Tamb (^{o}C)	22
Tamb_prot*	30 ^{o}C
Vin (V)	180
Fline (Hz)	50
Po (W)	**740**
Vo (V)	367

* This is the assumed value.

Table B.9. Measures and predictions.

Magnitude	Measured	Predicted		
		Non-conservative	Average	Conservative
Pin (W)*	782	774	776	779
Iin_rms (A)*	4.36	4.32	4.35	4.40
iLb_pk (A)	7.6	6.97	7.29	7.78
dILbmax (A)	3.2	1.80	2.42	3.36
Lb_min (µH)	795	1204	902	656
T_coreLb (^{o}C)	140	131	144	156
Ths _sw (^{o}C)	59	61.6	62.2	63.1
Ths _fd (^{o}C)	43	41.8	41.8	41.8
Ths _rd (^{o}C)	98	94.1	94.4	94.8

*The predictions do not include the power dissipated in the PFC stage EMI filter, load internal EMI filter and electrolytic capacitors.

B.1.5. TEST 5: Validation of EMI Levels' Prediction

Table B.10. Conditions.

Parameter	Value
Tamb	27 °C
Tamb_prot*	35 °C
Vin	230 Vrms
fline	50 Hz
Po	1150 W
Vo	368 V

* This is the assumed value.

B.1.5.1. Measures and predictions for EMI Levels

I) Total noise:

I.1) Measured

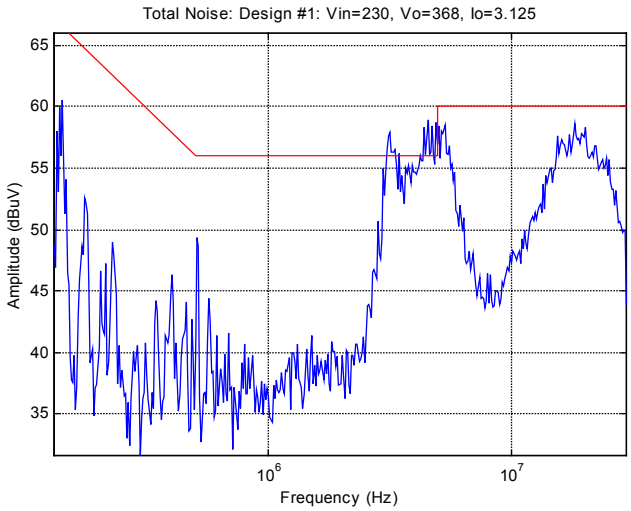


Figure B.1. Measured total EMI noise.

I.2) Predicted (considering $L_B = L_{B\_min}$):

- First limited group of harmonics:

Group of harmonics order = 5

Frequency (kHz) = 175.05

Standard level (dBuV) = 64.7173

I.2.1) Conservative:

- First limited group of harmonics:

Total noise (dBuV) = 58.4948

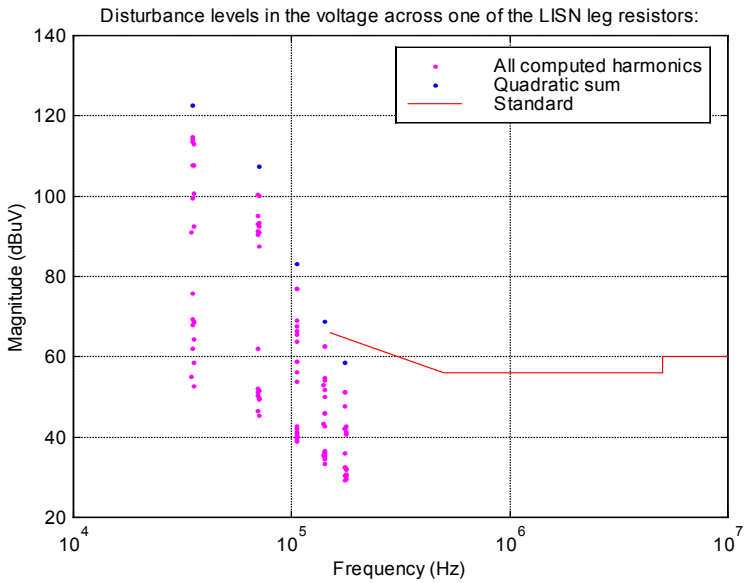


Figure B.2. Predicted total EMI noise in the conservative case.

I.2.2) Average:

- First limited group of harmonics:

Total noise (dBuV) = 53.5524

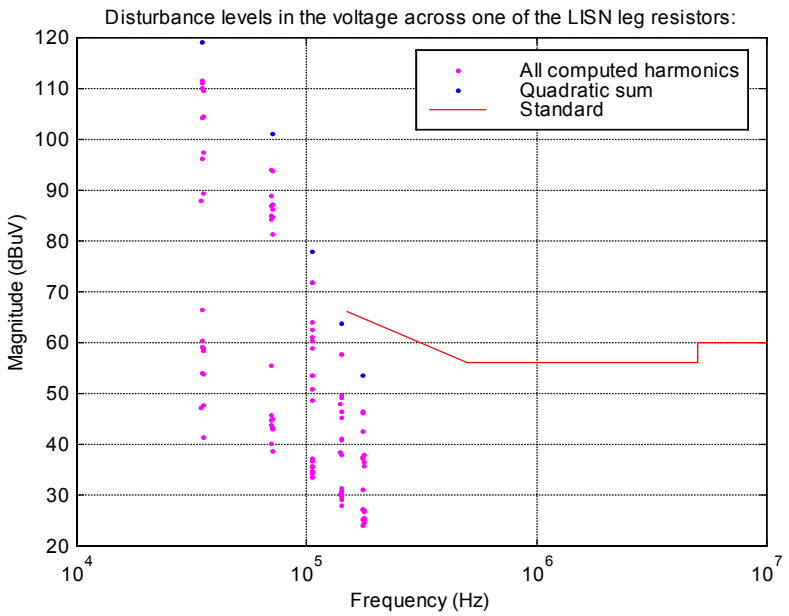


Figure B.3. Predicted total EMI noise in the average case.

I.2.3) Non-conservative:

- First limited group of harmonics:

Total noise (dBuV) = 49.265

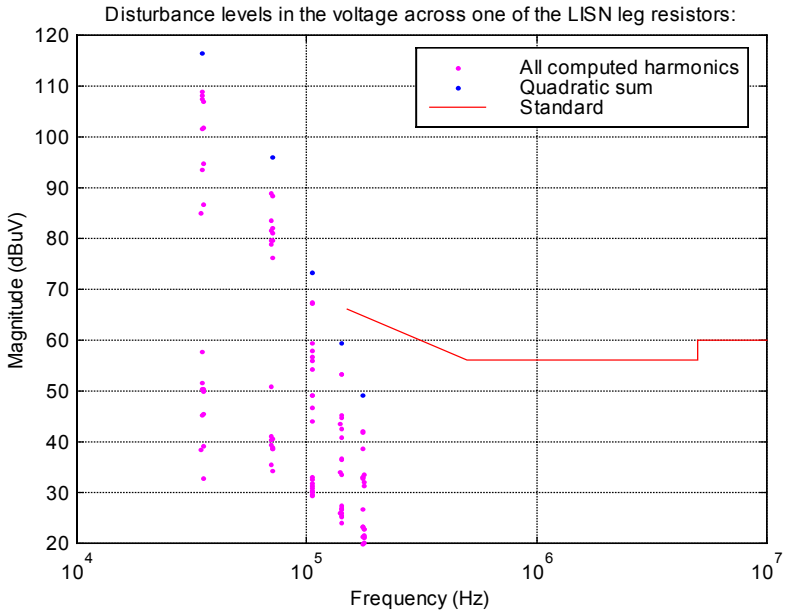


Figure B.4. Predicted total EMI noise in the non-conservative case.

II) Differential and common mode noise:

II.1) Measured

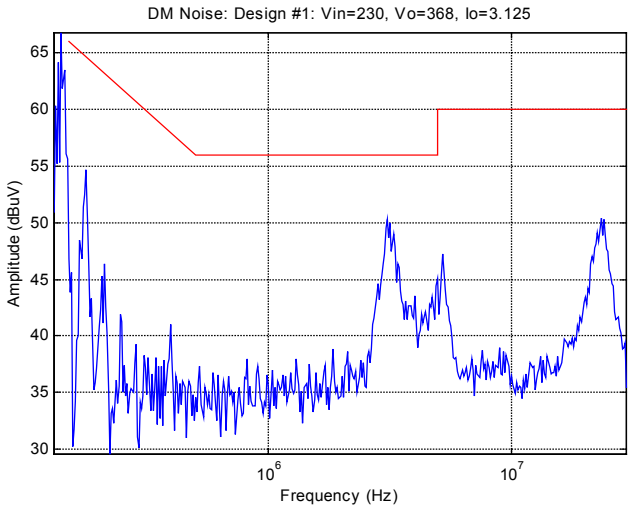


Figure B.5. Measured differential mode noise.

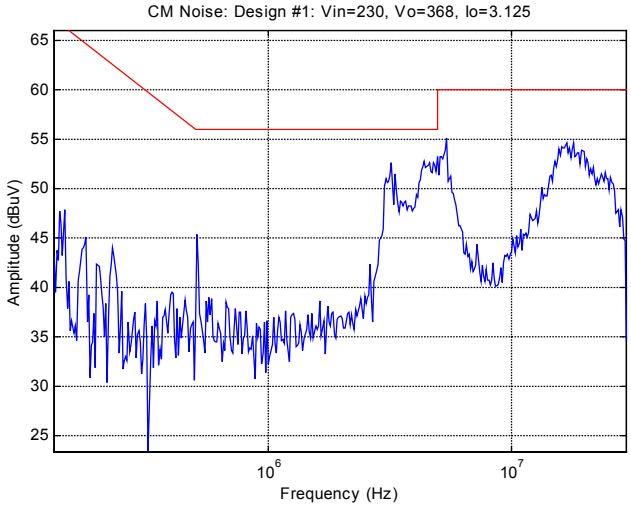


Figure B.6. Measured common mode noise.

II.2) Predicted (considering $L_B=L_{B\_min}$):

II.2.1) Conservative:

- First limited group of harmonics:

Differential mode noise (dBuV) = 57.7082. Common mode noise (dBuV) = 50.687.

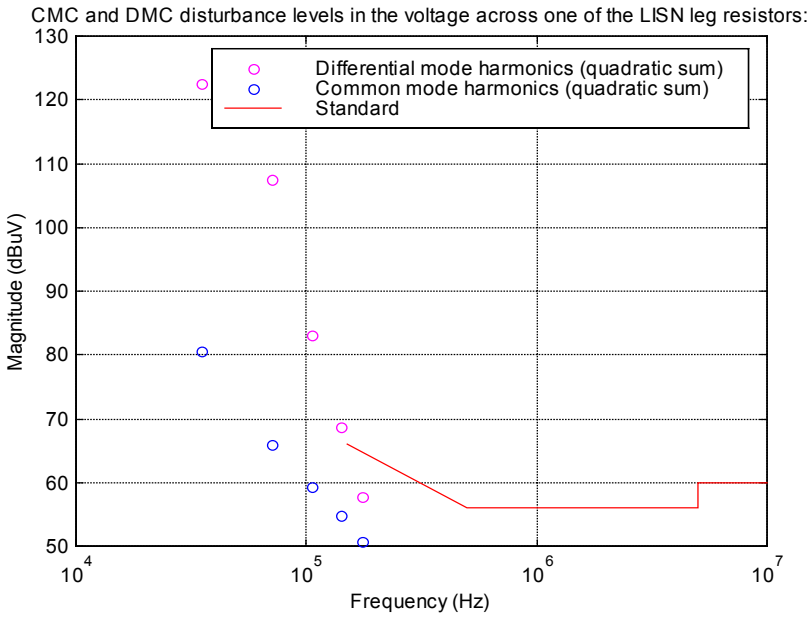


Figure B.7. Predicted differential and common mode noise in the conservative case.

II.2.2) Average:

- First limited group of harmonics:

Differential mode noise (dBuV) = 52.8139. Common mode noise (dBuV) = 45.4939.

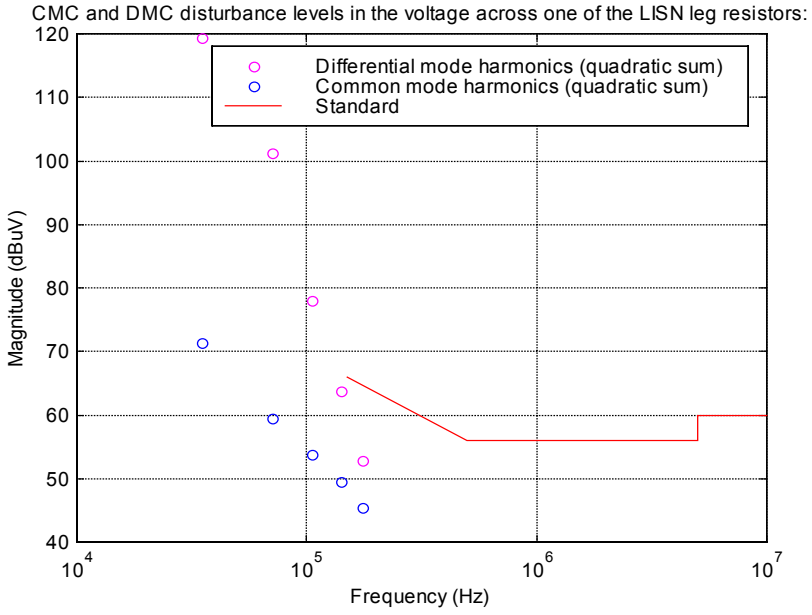


Figure B.8. Predicted differential and common mode noise in the average case.

II.2.3) Non-conservative:

- First limited group of harmonics:

Differential mode noise (dBuV) = 48.457. Common mode noise (dBuV) = 41.5638.

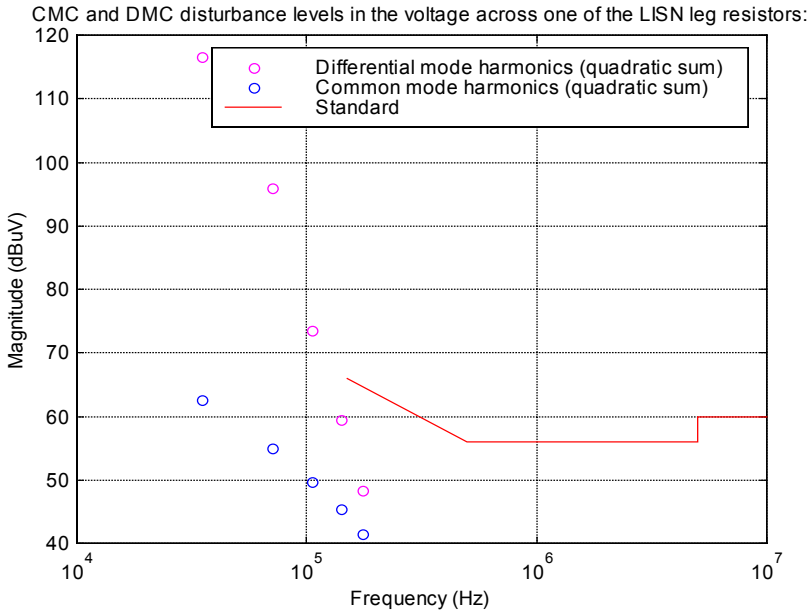


Figure B.9. Predicted differential and common mode noise in the non-conservative case.

B.2. Prototype 2

B.2.1. TEST 1: Model Tuning Test

Table B.11. Conditions.

Parameter	Value
Tamb_ext	23 °C
Tamb_prot*	50 °C
Vin	230 Vrms
Fline	50 Hz
Po	1151 W
Vo	355.7 V

* This is the assumed value.

Table B.12. Measures and predictions.

Magnitude	Measured	Predicted		
		Non-conservative	Average	Conservative
Pin (W)*	1193	1179	1179	1180
Iin_rms (A)*	5.22	5.13	5.13	5.14
iLb_pk (A) Δ	8.88	7.49	7.58	7.72
dILbmax (A) Δ	0.95	0.88	1.18	1.64
Lb_min (µH)	935	1274	957	697
Ptot_Lb (W)	10.8	7.05	7.6	8.1
T_coreLb (°C)	81	91.4	93.9	96.5
Ths_sw (°C)	86	85.4	85.6	86.0
Ths_fd (°C)	65	68.0	68.0	68.0
Ths_rd (°C)	114	120.5	120.6	120.7
C_{DG} (pF)	21.5	--------	--------	--------

* The predictions do not include the power dissipated in the PFC stage EMI filter, load internal EMI filter and electrolytic capacitors. Δ Without ringing amplitude. Setting $TL_B coef = 1.00$. This coefficient has not been reduced below 1.00 to better approximate the measured temperature of the core, because the sensor could not have been placed in the hottest spot of the core.

B.2.2. TEST 2: Validation of EMI Levels' Prediction

Table B.13. Conditions: Common mode choke is SDI 142-22 (Lcm=3.3mH).

Parameter	Value
Tamb_ext	27 °C
Tamb_prot*	50 °C
Vin	230 Vrms
fline	50 Hz
Po	1147.9 W
Vo	356.5 V

* This is the assumed value.

B.2.2.1. Measures and predictions for EMI Levels

I) Total noise:

I.1) Measured

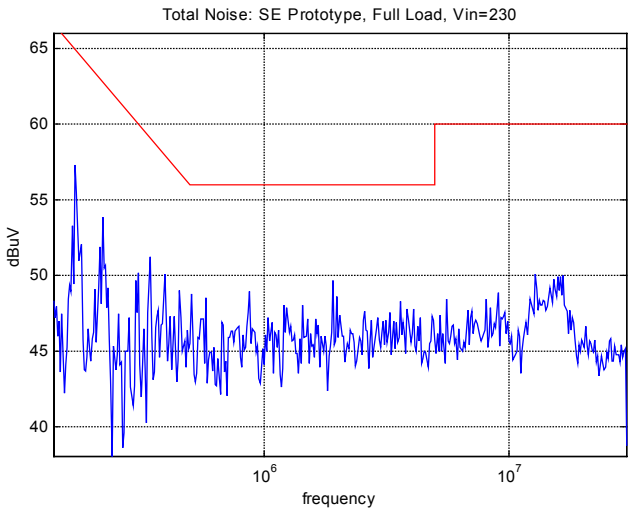


Figure B.10. Measured total EMI noise.

I.2) Predicted (considering $L_B = L_{B\_min}$):

- First limited group of harmonics:

Group of harmonics order = 4

Frequency (kHz) = 172.05

Standard level (dBuV) = 64.8609

I.2.1) Conservative:

- First limited group of harmonics:

Total noise (dBuV) = 59.53

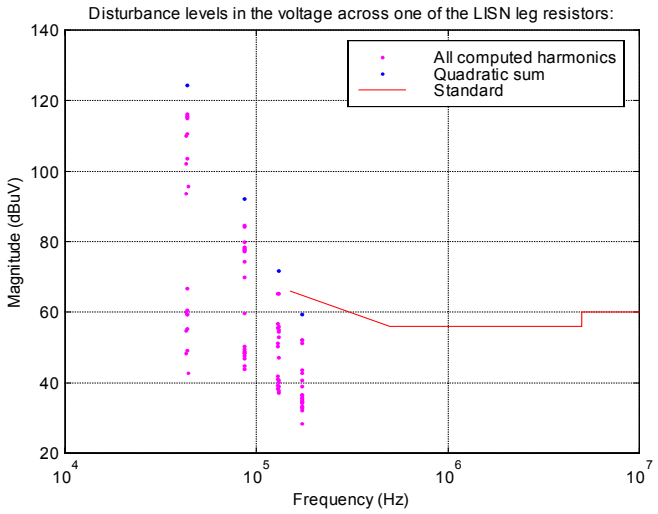


Figure B.11. Predicted total EMI noise in the conservative case.

I.2.2) Average:

- First limited group of harmonics:

Total noise (dBuV) = 54.8772

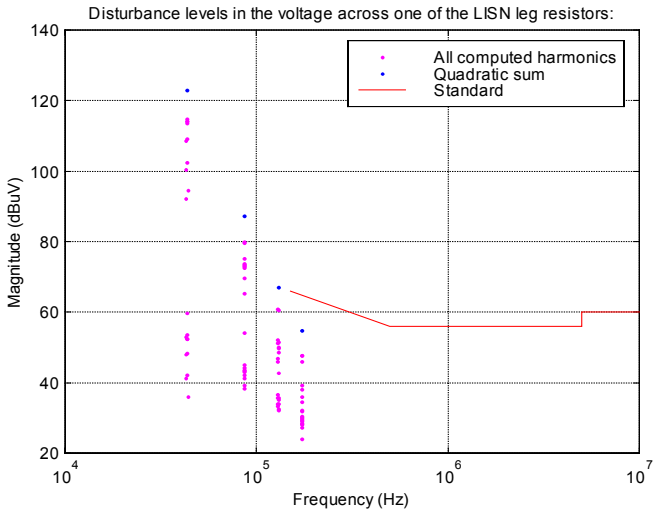


Figure B.12. Predicted total EMI noise in the average case.

I.2.3) Non-conservative:

- First limited group of harmonics:

Total noise (dBuV) = 50.9041

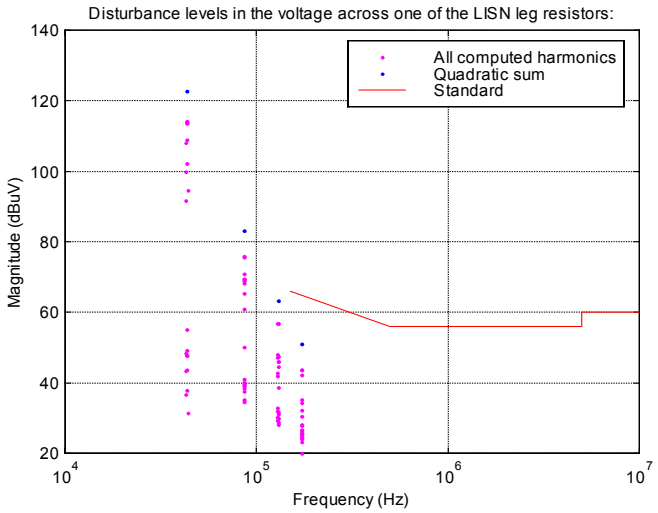


Figure B.13. Predicted total EMI noise in the non-conservative case.

II) Differential and common mode noise:

II.1) Measured

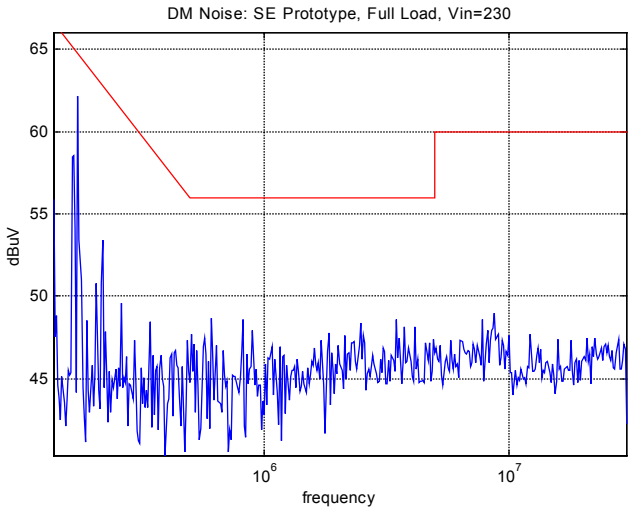


Figure B.14. Measured differential mode noise.

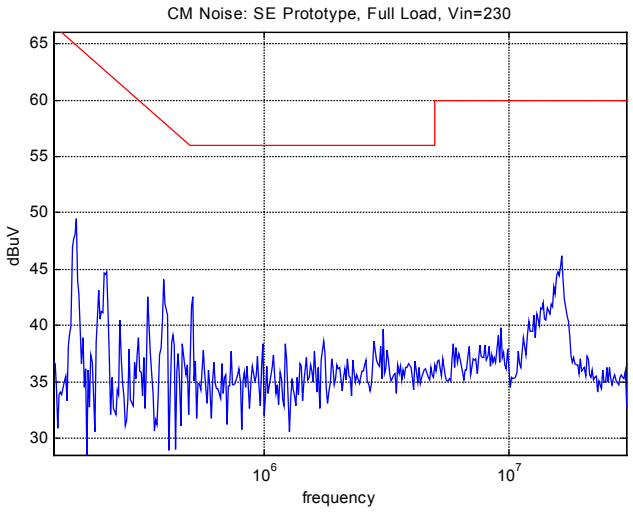


Figure B.15. Measured common mode noise.

II.2) Predicted (considering $L_B = L_{B\_min}$):

II.2.1) Conservative:

- First limited group of harmonics:

Differential mode noise (dBuV) = 58.13

Common mode noise (dBuV) = 53.91

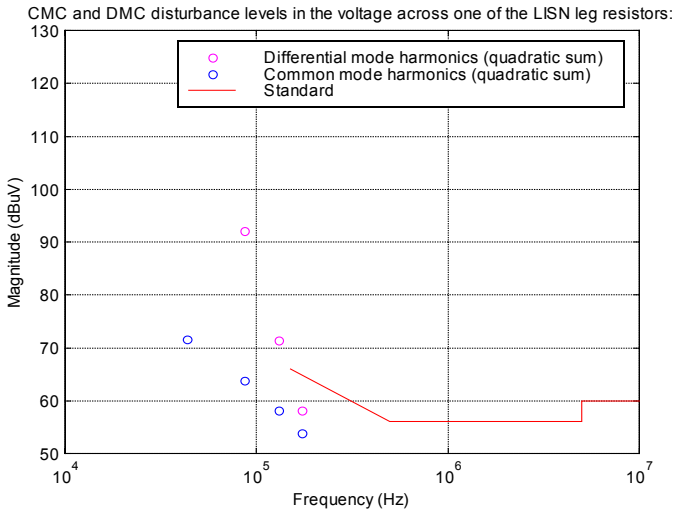


Figure B.16. Predicted differential and common mode noise in the conservative case.

II.2.2) Average:

- First limited group of harmonics:

Differential mode noise (dBuV) = 53.6348. Common mode noise (dBuV) = 48.8358.

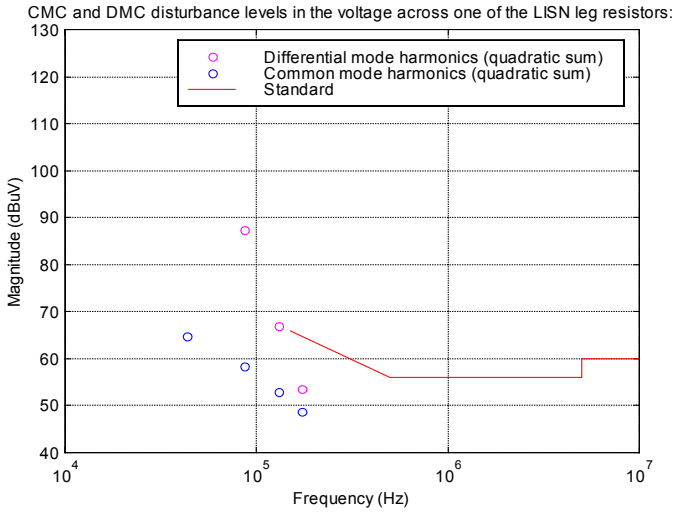


Figure B.17. Predicted differential and common mode noise in the average case.

II.2.3) Non-conservative:

- First limited group of harmonics:

Differential mode noise (dBuV) = 49.6343. Common mode noise (dBuV) = 44.9442.

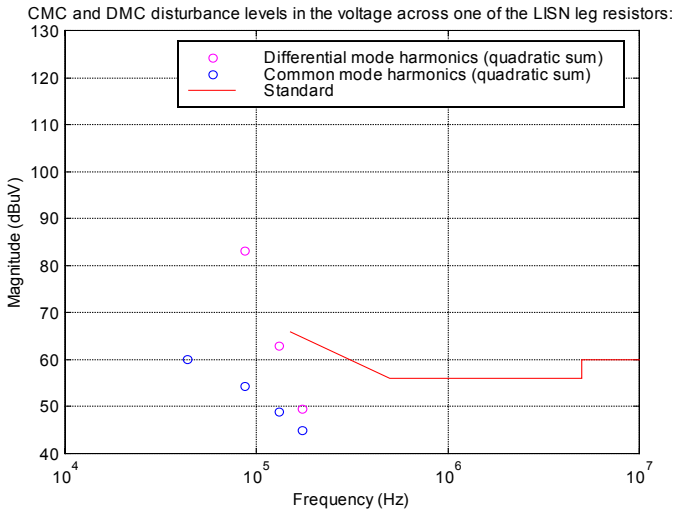


Figure B.18. Predicted differential and common mode noise in the non-conservative case.

B.3. Final Optimum Design

B.3.1. TEST 1: Thermal Measurements

Table B.14. Conditions.

Parameter	Value
Tamb_ext	24 °C
Vin	195 Vrms
fline	50 Hz
Po	1052 W
Vo	354.6V

Table B.15. Measures.

Magnitude	Measured
Pin (W)	1102
Efficiency	95.5%
Iin_rms (A)	5.67
iLb_pk (A)	9.26
dILbmax (A)	2.67
Lb_min (µH)	1067
T_coreLb (°C)	104
Ths_sw (°C)	75
Ths_fd (°C)	62
Ths_rd (°C)	134

B.3.2. TEST 2: Measurement of EMI Noise Levels

Table B.16. Conditions.

Parameter	Value
Tamb_ext	27 °C
Vin	230 Vrms
fline	50 Hz
Po	1140 W
Vo	356 V

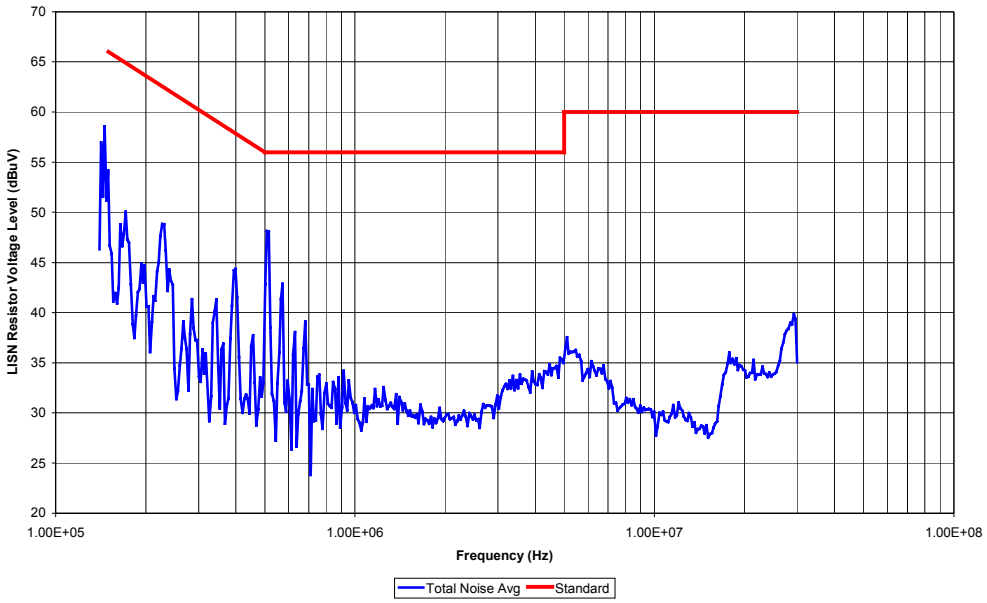


Figure B.19. Measures (total noise).

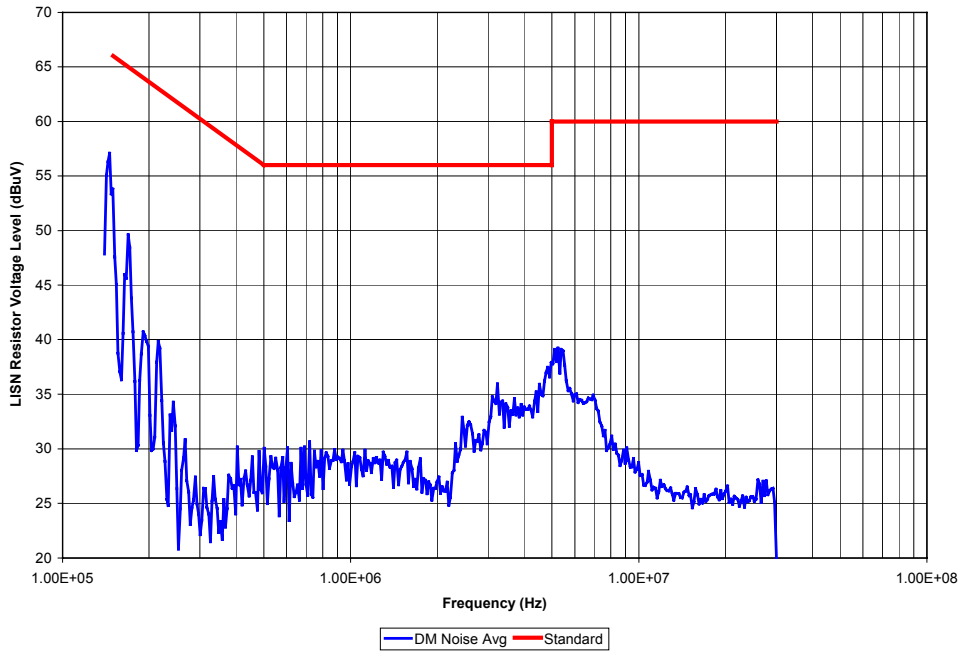


Figure B.20. Measures (differential mode noise).

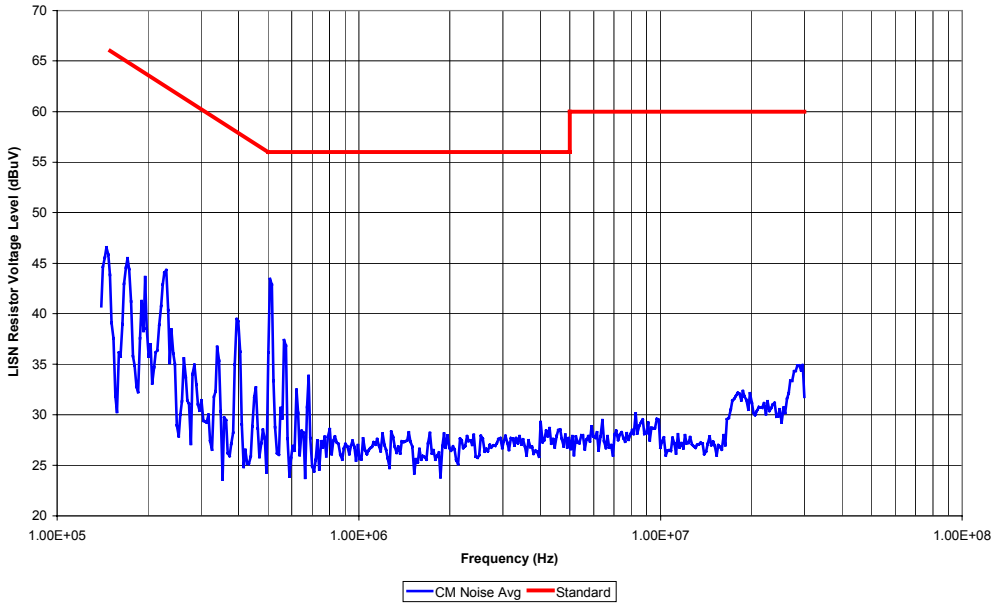


Figure B.21. Measures (common mode noise).

Appendix C. Converter Design Conditions and Component Database

In the following, the converter design conditions / specifications used to obtain the optimum designs presented in Section 3.3.6 (Discrete Optimization) and the number of components contained in the component database are detailed. The units of the different magnitudes can be found in the online help area of the software.

C.1. Converter Design Conditions/Specifications

C.1.1. General

```
vinmin_rms = 180/195/230
vinnom_rms = 230
     fline = 50
        po = 1150
   vbus_dc = 368
      tamb = 50
conservative = 1
```

C.1.2. Boost PFC

```
    singhs = 0
      hsfd = 1
      hsrd = 0
    tmaxhs = 100
      k1hs = ***
      k2hs = ***
        jm = 1000
       kcu = 0.0039
    row100 = 2.208E-6
        ku = 0.5
   tlbcoef = 1.2
cost_lbfixmanuf = ***
   tollblk = 50
   tmaxpcb = 125
dtpcblbcore = 5
        cb = 6.92E-4
   cost_cb = ***
```

```
   vpkMmin = 500
  vpkIGmin = 600
  vpkFDmin = 600
  vpkRDmin = 800
   ifsmmin = 150
        ls = 1.0E-8
  perswqrr = 50
 triseigbt = 5.0E-8
 tfalligbt = 5.0E-8
       vgg = 15
      rgon = 33
     rgoff = 10
```

C.1.3. EMI Filter

```
 Class_type = Class B, Group 1
   vaccxmin = 275
   vaccymin = 250
       llha = 2.5E-7
       lldb = 2.5E-7
        lsf = 3E-8
         ld = 1.0E-7
       llmg = 5E-7
       lres = 1.5E-4
        csg = 1E-12
        cdg = 2E-11
        ckg = 1E-12
        ceg = 1E-12
        cfg = 1E-12
        cag = 1E-12
        cbg = 1E-12
        clb = 1E-12
        rlb = 1000000
         ln = 5E-5
         cn = 1E-7
         c1 = 1E-5
         zn = 50
harm_number = 1
        ind = 3
       incr = 3
```

C.2. Component Database

Table C.1. Number of components of each type in the database.

Component type	Switch		Bridge diode	Fast diode	Boost inductor		Common mode capacitor	Differential mode capacitor	Common mode choke
	MOSFET	IGBT			Core	Wire			
Number of components in the database	6	21	11	15	28	5	5	5	11

Appendix D. Optimization Software

Figure D.1 allows access to a compressed file containing a demo version of the design software tool developed as well as the continuous and discrete MATLAB design analysis functions. The hierarchical organization of the files included is specified.

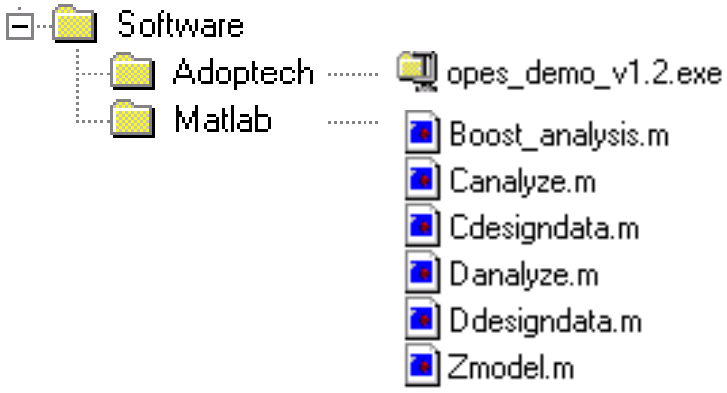


Figure D.1. Design analysis and design optimization software (Software.zip, 8,990KB).

To install the demo version of the software just double click on the file "opes_demo_v1.2.exe".

Vita

Sergio Busquets-Monge

The author was born in Barcelona, Spain, in 1974. He received the B.S. and M.S. degrees in engineering, with concentration in electricity and electronics, from the Polytechnic University of Barcelona, in June 1999. His research centered on the development of new modulation strategies for the three-level neutral-point-clamped voltage source inverter.

In fall 1999, the author enrolled at Virginia Polytechnic Institute and State University as a student working towards his master's degree. His research centered on the application of optimization techniques to the design of power electronics systems.

The author is a member of the IEEE and the Phi Kappa Phi honor society.