Modeling and Design of Planar Integrated Magnetic Components

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(Abstract)

Recently planar magnetic technologies have been widely used in power electronics, due to good cooling and ease of fabrication. High frequency operation of magnetic components is a key to achieve high power density and miniaturization. However, at high frequencies, skin and proximity effect losses in the planar windings become significant, and parasitics cannot be ignored. This piece of work deals with the modeling and design of planar integrated magnetic component for power electronics applications.

First, one-dimensional eddy current analysis in some simple winding strategies is discussed. Two factors are defined in order to quantify the skin and proximity effect contributions as a function of frequency. For complicated structures, 2D and 3D finite element analysis (FEA) is adopted and the accuracy of the simulation results is evaluated against exact analytical solutions.

Then, a planar litz structure is presented. Some definitions and guidelines are established, which form the basis to design a planar litz conductor. It can be constructed by dividing the wide planar conductor into multiple lengthwise strands and weaving these strands in much the same manner as one would use to construct a conventional round litz wire. Each strand is subjected to the magnetic field everywhere in the winding window, thereby equalizing the flux linkage. 3D FEA is utilized to investigate the impact of the parameters on the litz performance. The experimental results verify that the planar litz structure can reduce the AC resistance of the planar windings in a specific frequency range.

After that, some important issues related to the planar boost inductor design are described, including core selection, winding configuration, losses estimation, and thermal

modeling. Two complete design examples targeting at volume optimization and winding parasitic capacitance minimization are provided, respectively.

This work demonstrates that planar litz conductors are very promising for high frequency planar magnetic components. The optimization of a planar inductor involves a tradeoff between volumetric efficiency and low value of winding capacitance. Throughout, 2D and 3D FEA was indispensable for thermal & electromagnetic modeling.

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Table of Contents

List of Figures

List of Tables

Chapter 1. Introduction

1.1 Overview of Planar Magnetic Technology

In recent years, planar magnetic technology has become increasingly popular in the high frequency switch mode power supply design. The use of higher switching frequencies can result in passive component size reduction, therefore achieving higher power densities in power supplies. However, the demand of high-frequency operation caused a number of limitations in the use of conventional magnetic structures, such as the problem of increased loss due to the skin and proximity effects in the round conductors particularly at frequencies above 100 kHz [1.1]. Compared to the conventional counterparts, planar magnetic components demonstrate good performance with respect to coupling among the windings, size, repeatability and thermal management. A great deal of research work has been done previously to take full advantage of planar magnetic technology. The overview of this technology is organized as follows:

- Advantages and limitations of planar magnetic components
- Applications in power converters
- Planar magnetic components design issues

1.1.1 Advantages and limitations of planar magnetic components

The difference between conventional and planar magnetic components is in terms of orientation of winding layers, as shown in Fig. 1. It can be seen that windings in the planar magnetic component have flat, wide and rectangular cross section (typically, the width to thickness ratio is 10:1), and the core of the planar structure has lower profile than that of the conventional structure.
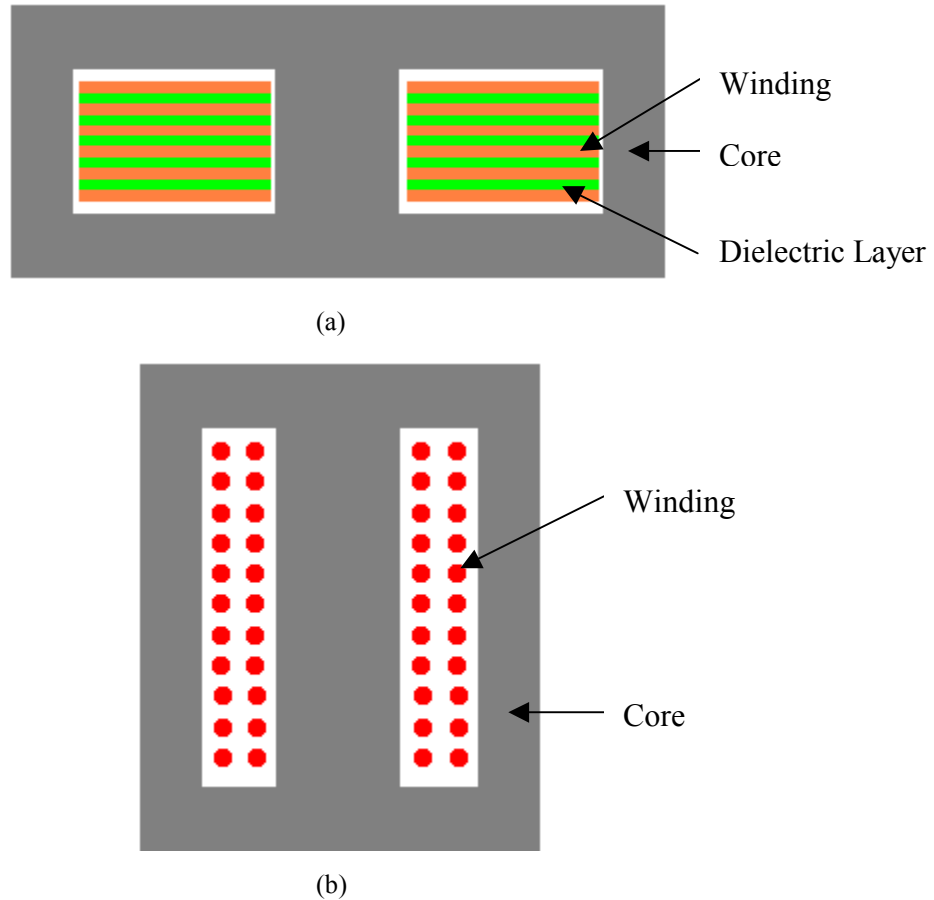
Fig. 1. Magnetic component: (a) Planar; (b) Conventional.

The principal advantages of planar magnetic components over conventional wire wound components are listed below. These include:

1) *Low profile structures*. Some studies have indicated that the low profile magnetics can have better volumetric efficiency [1.2] and higher power density [1.3] for certain applications.

2) *Lower leakage inductance*. Interleaving can be easily implemented in planar structures, which allows the minimization and control of leakage inductance within the windings [1.4].

3) *Reduced high frequency winding losses*. Skin effect is minimized by reducing the thickness of the conductor windings to one or two times the skin depth [1.5].

4) *Better thermal management*. Planar magnetic components have the greater surface area to volume ratio, thus more area contact to the heat sink. [1.6] shows that a

smaller value of thermal resistance can be obtained by using planar cores instead of conventional cores.

5) *Ease of manufacturing*. The use of Printed Circuit Boards (PCBs) gives a highly manufacturable means of implementing planar windings.

6) *Good repeatability*. The repeatability of component characteristics is very important particularly in resonant topologies [1.7].

However, the characteristics of planar magnetic components are not all advantageous. They have some limitations such as:

1) *Large footprint area*. The planar format, although improving thermal performance, increases footprint area.

2) *Increased parasitic capacitance*. The fact that windings are stacked closely has the usually unwanted effect of increasing parasitic capacitance.

3) *Low window utilization factor*. If PCB is used to implement planar windings, the window utilization factor can be quite low (typically $0.25 - 0.3$ compared to 0.4 for conventional magnetics) due to a typical interturn spacing of 150 um and minimum dielectric thickness of 100 um [1.1].

1.1.2   Applications in power converters

Planar magnetic technology has been widely used in modern DC-to-DC converters due to the advantages that it offers. The characteristics of planar structures in different applications are discussed below.

I.   Power Transformers

Transformers in high frequency switch mode power converters have to be designed to result in low volume, weight and losses. In addition, a good coupling of all windings is required to avoid parasitic oscillation. The coupling capacitance between the primary and secondary windings must be as small as possible to reduce propagation of the conducted EMI between primary and secondary windings. Besides, the isolation clearance has to satisfy the safety standard.

Planar transformers can fulfill most of the requirements stated above. The coupling of the windings can be easily increased by using multiply stacked planar windings in series or in parallel connection. Interleaving is a well-known technique used to reduce the leakage inductance and minimize high-frequency losses on the planar windings. Three different structures employing interleaving are shown in Fig. 2. The SPSP configuration has the smallest AC resistance and leakage inductance, because primary and secondary layers are fully interleaved [1.8].
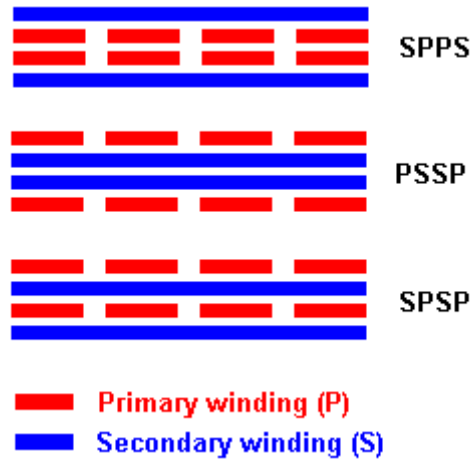
Fig. 2.   Three different configurations with interleaving.

However, the capacitive effects in planar transformers are more significant than in conventional transformers. Also, particular attention should be paid to the termination of the windings [1.9].

II.   Power Inductors

The requirements of planar power inductors can be very similar to or different from those of planar transformers, depending on the application.

When the ripple current is small, that is, the average dc current component is dominant, then high frequency effects and HF core losses can be ignored. The design of the planar inductor reduces to choosing windings with the lowest possible resistance based on the constraints of the core size and gap. Low winding resistance is then sought by maximizing the copper utilization in the core window. There exist a number of different

approaches to implementing windings, such as stamped and pinned windings [1.10], folded copper windings [1.11] and a true helical windings [1.12].

When the ac ripple current is large relative to the dc component, the design of an inductor winding is very similar to that of a transformer winding, except that there is no secondary winding that can be used to reduce the proximity effect by means of interleaving. The large AC flux component may increase core losses and also contribute to eddy current losses if the conductors and the gap are in close proximity. The use of the quasi-distributed gap technique can facilitate the design of low-AC-resistance planar inductors [1.13].

III. *Integrated Magnetics*

Integrated Magnetics (IM) technique is "mixing" of transformer and inductive functions of dynamic power conversion circuits on a single magnetic core structure [1.14]. The stacked "top-to-bottom" and "side-by-side" multi-chambered planar integrated magnetic (PIM) constructions are proposed by G. E. Bloom. These approaches require the use of core structures with more than one winding window area, and have the distinct advantages of minimal interactions between the various magnetic elements. The use of printed wiring methods for the windings can lower the height profile of the overall package. The constructions can also include planar "disks" of magnetic material to control leakage inductances in selected areas of the structures.

IV. *Integrated Electromagnetics*

In the integrated electromagnetic approach, the electromagnetic components such as transformers, inductors and capacitors are built up using successive planar layers of conducting, magnetic, and dielectric materials, so as to form part of a highly integrated "energy processing" structure [1.15]. Planar sub-components differ from normal components in the sense that they are not able to function on their own, but need other sub-components to define their circuit function. The construction of a sub-assembly can conceptually be seen as the stacking of planar sub-component layers on top of each other.

1.1.3 Planar magnetic components design issues

A.   Electrical and Magnetic Design

Most of the previous work has been done concerning the optimization of the electrical and magnetic design. A number of factors, such as materials, winding technologies, losses and leakage need to be considered carefully in the design. Many commercial software simulation tools, such as Maxwell®, InCa® and Ansys®, were developed based on numerical techniques. Throughout this work, Maxwell® developed by Ansoft [1.16] has proved to be very powerful in design optimization.

1) *Materials:* Soft magnetic materials are widely used as the core material of inductive power devices such as inductors and transformers. They can be easily magnetized but do not retain their magnetism when the external field is removed. Ideally, the planar magnetic material should have the following properties:

   - High saturation flux density;
   - Low core losses;
   - High permeability;
   - High resistivity.

   To date ferrites are the most popular materials used for magnetic components. MnZn and NiZn are the two common classes of ferrites. MnZn ferrites are characterized by rather high intrinsic permeability and resistivity [1.17]. NiZn ferrites are of lower permeability but offer much higher bulk or volume resistivity than the MnZn ferrites [1.18]. High permeability is desirable to maximize inductance and reduce reluctance in the core material. Materials with higher bulk resistivity are more suitable for use at high frequencies, where maintaining low losses is critical.

2) *Winding Technologies:* Several different technologies can be used to implement the low-profile planar windings, such as stamped-copper-foils, flexible printed circuits (copper-on-Kapton) and PCB [1.4].

   Stamped-copper-foils technique is a low cost means to implement the windings. Each layer can be built using any copper thickness. However, the insulation layers need to be added separately and the interconnections have to be provided externally.

In flexible circuit technology, an etching process is used to implement the windings. The layer insulation can be automatically provided by the substrate. Many layers of flexible circuit can be laminated together to form a rigid structure similar to a PCB but with an improved utilization factor [1.19]. Also, some appropriate folding methods can be used to eliminate the external interconnections. However, the performance consistency among samples is not that good.

The PCB winding technique is highly suitable for mass production. One of its benefits is it is easy to maintain consistent performance from sample to sample. The disadvantage of PCB is its relatively low window utilization factor.

3) *Losses:* Core losses can be divided into a) hysteresis losses and b) eddy current losses. The hysteresis losses are a function of the area enclosed in the characteristic B - H loop. The eddy current losses in the core material are significant in high-frequency applications. Copper losses are determined by the winding configuration and the frequency. Most of the analytical models for calculating the winding losses so far published can be traced back to the one-dimensional model of Dowell [1.20]. However, in many cases, a one-dimensional solution cannot be used. Two-dimensional and three-dimensional FEA approaches are therefore frequently used to estimate the winding losses, although they may consume lots of computing time.

4) *Leakage:* Within the core window, high leakage flux close to windings of high MMF results in excessive losses. Various gapping techniques [1.21] can be used to control the leakage field. However, this can increase the leakage field outside the core causing external noise problems. In a low-profile planar design the window height is reduced significantly and the window cross section increases. This may cause the window "gap" reluctance to be comparable to the gap reluctance, therefore increasing the AC-to-DC resistance ratio [1.22].

B.   Thermal Design

Thermal management becomes an increasingly important aspect of planar magnetic component design, as the operating frequency increases, and the overall size of the devices shrinks. The use of a flat core in close proximity to a heat sink or substrate can improve cooling. Planar structures are obviously suitable because they can present a

relatively large surface area for heat sinking. The addition of thermal contacts (grease, pad, glue, …) can also help in designs to spread the heat [1.23].

Temperature has an effect on most ferrite material properties. Most materials increase in permeability as the temperature increases. The Curie temperature of the ferrite is typically in the order of $140 \sim 300 \ °C$ at which an abrupt loss of magnetizing properties occurs. Therefore, it is important to know where this Curie point is and to maintain the core operating temperature below this limit. Ferrite materials are commonly optimized for operating temperature in the range of $60 \sim 110 \ °C$. Some empirical equations used to determine the temperature rise in conventional core designs may not be valid for planar structures.

C.   *Manufacturing Consideration*

Planar devices can be introduced in a manufacturing facility either as discrete components or as substrate-integrated components. Stand-alone components are available both off-the-shelf and customized. However, interconnection may cause additional losses. Substrate-integrated components overcome this problem by utilizing the main substrate of the electronic assembly as an integral part of the planar magnetic components. The drawback of substrate-integrated components is that the component is not readily testable as a separate entity. [1.1]

1.2 Aims of This Study

At high frequencies, the eddy current losses induced in planar inductor or transformer windings severely limit the performance of magnetic components. The current distributes quite unevenly across the flat, wide (or planar) windings due to the skin and proximity effects. The loss mechanisms in foils at high frequencies are analyzed and modeled using 2D and 3D FEM software [1.24]. The accuracy of FEM software is evaluated against exact analytical solutions for simple structures. The planar litz structure proposed previously to reduce the AC resistance of the planar conductor is investigated further. Lots of simulation work has been done to look into the field distribution in different winding configurations. The performance of the planar litz windings is also verified with

measurements on the experimental prototypes. Finally, a planar boost inductor design is described as an example to illustrate some important issues in planar magnetic component design.

1.2.1   Chapter 2: Eddy Current Analysis

In order to investigate the skin and proximity effect losses on the planar conductors, it is essential to understand the field distribution. Some basic electromagnetic field principles and equations are reviewed first. Based on some assumptions, the one-dimensional analytical solutions for simple structures are derived in terms of Maxwell's Equations. Two factors, Λ_F and Λ_G, are defined to quantify the skin and proximity effect contributions to winding losses as functions of frequency.

1.2.2   Chapter 3: FE Modeling

The mathematical solutions to the actual electromagnetic problems are always extremely complicated. FEM techniques have proven to be very valuable in minimizing the complexity of the solutions. Maxwell 2D and 3D simulation tools are used for analyzing the skin and proximity eddy current effects in foils. It was found that the mesh is very critical when solving finite element problems. If the mesh is too fine, then the simulation will take much long time. If the mesh is too coarse, then the accuracy of the results will not be good enough.

1.2.3   Chapter 4: Planar Litz Structure

A planar litz conductor can be constructed by dividing the wide planar conductor up into multiple lengthwise strands and weaving these strands in much the same manner as one would use to construct a conventional round litz wire. Each strand is subjected to the magnetic field everywhere in the winding window, thereby equalizing the flux linkage. Some definitions and guidelines for a planar litz conductor are presented. 3D FE modeling is performed for some simple models. The simulation results demonstrate that the planar litz conductor can result in lower AC resistance than is achieved with a solid

conductor in a specific frequency range. The planar litz conductor concept is also verified experimentally.

1.2.4   Chapter 5: Planar Boost Inductor Design

As an example, a 1 kVA, 400 kHz PFC boost inductor design is presented. The discussions of some important issues, like core selection, winding configuration, losses estimation, thermal modeling, and parasitic capacitance are included. The objective of optimization, which is application-oriented, could be volume or parasitics.

In the last chapter, conclusions and future works will be provided.

Chapter 2. Eddy Current Analysis

2.1 Introduction

In high-frequency converters, power losses in winding conductors increase substantially due to the effects of eddy currents. The specific conductor eddy current mechanisms are called the *skin effect* and the *proximity effect*. These effects alter the field and current distribution within the magnetic windings which results in an increase in AC resistance as a function of frequency.

The analysis of high-frequency conduction losses in magnetic windings is not a straightforward task. If the winding strategy is simple enough, then one-dimensional (1D) approaches can be applied to evaluate the losses in conductor windings [2.1-2.7]. However, at high excitation frequencies, the additional AC losses due to the two-dimensional (2D) edge effects are significant and can not be predicted by the one-dimensional solutions. Thus, a set of correction factors, which account for the 2D edge effects, were proposed to modify the AC resistance predicted by the 1D analysis [2.8]. Finite element analysis (FEA) techniques have proven to be very useful when complex winding strategies need to be analyzed. In this chapter, some basic theoretical analysis and mathematical derivations for simple structures will be presented. FEA techniques will be the main topic in the next chapter.

2.2 The Skin and Proximity Effects

The skin effect in a conductor is caused by the current flowing through the conductor itself. Fig. 3 illustrates a foil conductor carrying a current $i(t)$. This current induces

magnetic flux $\Phi(t)$, whose flux lines follow circular paths around the current. According to Lenz's law, the AC flux in the conductor due to the eddy current tends to oppose the original AC flux $\Phi(t)$. It can be seen that the eddy current tends to reduce the net current density in the center of the conductor, and increase the net current density near the edges of the conductor.
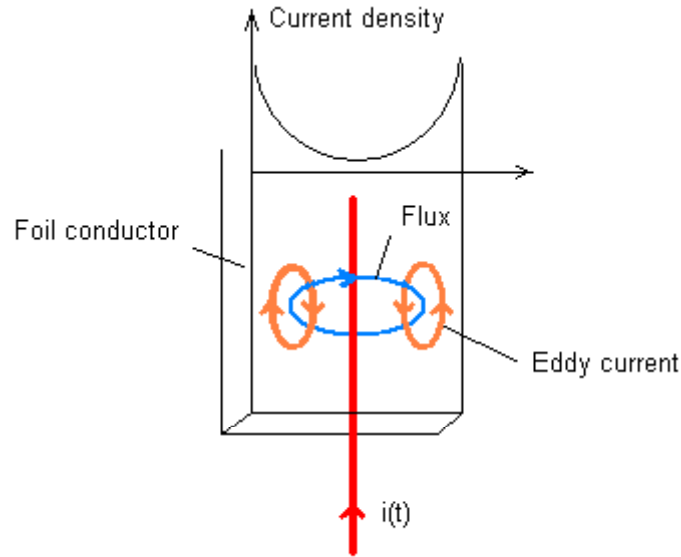
Fig. 3.   The skin effect in a single foil conductor.

The current distribution within the conductor can be found by solving Maxwell's equations. The current density is an exponentially decaying function of distance into the conductor. The penetration depth of magnetic field into the conductor, known as skin depth δ, is defined as:

$$\delta = \sqrt{\frac{\rho}{\pi \cdot \mu \cdot f}} \tag{1}$$

where ρ is the resistivity, μ is the permeability and f is the frequency of a sinusoidal current. ρ is dependent on temperature, expressed by $\rho = \rho_o[1 + \alpha(T - T_0)]$, where α is the temperature coefficient. At $100 \degree C$, the skin depth δ for a copper conductor is:

$$\delta = \frac{7.5}{\sqrt{f}} cm \tag{2}$$

where f expressed in Hz. The skin depth of copper conductors is plotted in Fig.4, as a function of frequency. The skin effect causes current crowding at the surface of the

12

conductor, and the inside of the conductor is not utilized, so the effective conductor cross-sectional area is reduced. However, the skin effect alone is not sufficient to explain the increased high-frequency conduction losses in multiple layer windings.
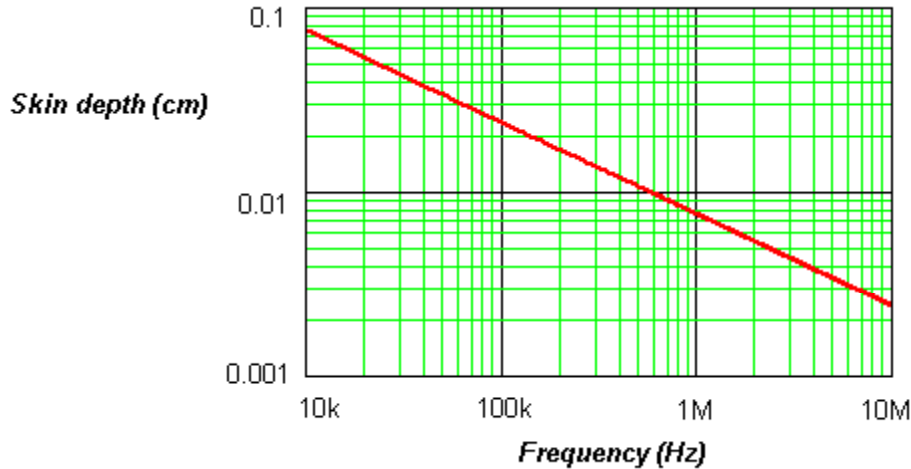
Fig. 4.   Skin depth as a function of frequency.

The proximity effect in a conductor refers to the currents that are induced by the magnetic fields generated by the adjacent conductors. Fig. 5 illustrates two foil conductors that are placed in close proximity to each other. A high-frequency sinusoidal current $i(t)$ is flowing through conductor 1. Conductor 2 is open-circuited, so that it carries a net current of zero. The current $i(t)$ in conductor 1 generates a flux $\Phi(t)$ in the space occupied by conductor 2. By Lenz's law, a current is induced in conductor 2, which tends to negate the flux $\Phi(t)$.
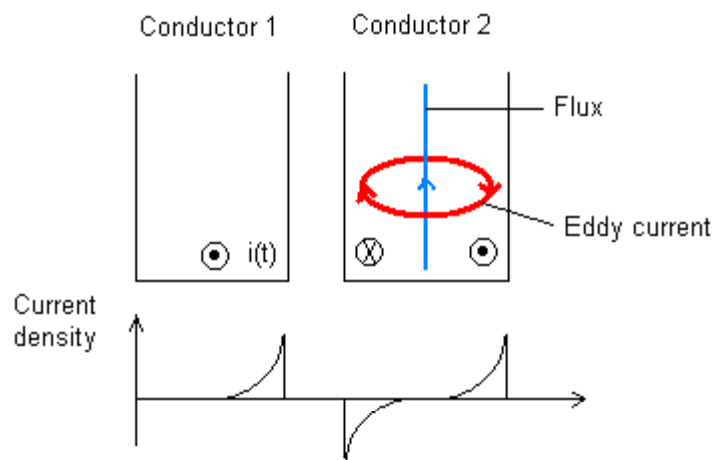
Fig. 5.   The proximity effect in adjacent foil conductors.

13

2.3   One-dimensional Analytical Techniques

One-dimensional (1D) analytical techniques are very helpful to understand the field distribution in magnetic components. The assumption of 1D approximation is that there is one main direction where the fields change and the components of fields in the other two directions are null or constant [2.9]. In the following section, some simple winding strategies are investigated where 1D analysis can be applied.

2.3.1   An isolated single foil conductor

Consider an isolated single foil conductor as shown in (Fig. 6). It is assumed that the conductor carries a peak current I, with its thickness h much smaller than its width w ($h \ll w$). It is part of an infinite loop so that its curvature is negligible and end-effects can be ignored. This implies that the magnetic fields are always perpendicular to the current flow and parallel to the flat surface of the conductor.
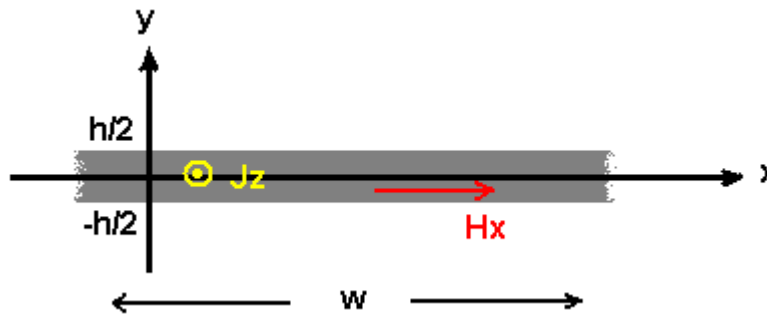
Fig. 6.   An isolated single foil conductor.

This problem can be solved using 1D field analysis [1.24]. Since the current is only in the z direction, the magnetic field equation can be written as

$$\nabla^2 H_x = j\omega\sigma\mu H_x = j\frac{2}{\delta^2}H_x = \alpha^2 H_x \tag{3}$$

where ω ($= 2\pi f$) is the radian frequency of a sinusoidal current, σ is the conductivity, δ is the skin depth, and α is defined as

$$\alpha = \frac{1+j}{\delta} \tag{4}$$

The general solution of equation (3) has the form of

$$H_x = H_1 e^{\alpha y} + H_2 e^{-\alpha y} \tag{5}$$

where H_1 and H_2 are the constants that can be determined by the boundary conditions:

$$H_x(h/2) = -H_x(-h/2) = -\frac{I}{2w} \tag{6}$$

Then the solution for the magnetic field intensity is

$$H_x = -\frac{I \cdot \sinh(\alpha y)}{2w \cdot \sinh(\alpha \cdot h/2)} \tag{7}$$

The current density J_z can be found using Maxwell's equation,

$$J_z = -\frac{\partial}{\partial y} H_x = \frac{\alpha \cdot I \cdot \cosh(\alpha y)}{2w \cdot \sinh(\alpha \cdot h/2)} \tag{8}$$

Finally, the skin-effect loss per unit length P_s can be calculated as

$$P_s = \frac{w}{2\sigma} \int_{-h/2}^{h/2} \left|J_z^2\right| dy = \frac{I^2}{4w\sigma\delta} \cdot \frac{\sinh v + \sin v}{\cosh v - \cos v} \tag{9}$$

where v is a normalized dimension which is defined as

$$v = \frac{h}{\delta} \tag{10}$$

Now suppose that an external magnetic field $H_e \cos(wt)$ is applied to the surface of the foil conductor, which has no net current. The magnetic field intensity and the peak current density becomes

$$H_x = H_e \frac{\cosh(\alpha y)}{\cosh(\alpha \cdot h/2)} \tag{11}$$

$$J_z = \alpha H_e \frac{\sinh(\alpha y)}{\cosh(\alpha \cdot h/2)} \tag{12}$$

In this situation, the skin effect is not present. So the proximity effect loss per unit length P_p is given by

$$P_p = \frac{w}{2\sigma} \int_{-h/2}^{h/2} \left|J_z^2\right| dy = \frac{w \cdot H_e^2}{\sigma\delta} \cdot \frac{\sinh v - \sin v}{\cosh v + \cos v} \tag{13}$$

The skin and proximity effect losses in 1D solutions are decoupled, due to the inherent orthogonality recognized by Ferreira [2.10]. Therefore, for a single foil conductor having a current and external magnetic field perpendicular to the current, the conduction loss per unit length P is:

$$P = \frac{1}{2\sigma} \int_A (J_s J_s{}^* + J_p J_p{}^*) dA = (\Lambda_F + 1) \cdot I_{rms}{}^2 R_{dc} + \Lambda_G \cdot w^2 H_e{}^2 R_{dc} \qquad (14)$$

$$\Lambda_F = \frac{v}{2} \cdot \frac{\sinh v + \sin v}{\cosh v - \cos v} - 1 \qquad (15)$$

$$\Lambda_G = v \cdot \frac{\sinh v - \sin v}{\cosh v + \cos v} \qquad (16)$$

where J_s and J_p represent the current density due to the skin and proximity effects respectively, R_{dc} is the DC resistance of the conductor per unit length, I_{rms} is the RMS current flowing in the conductor. To account for the skin and proximity effect losses separately, two factors, Λ_F and Λ_G are defined. Fig. 7 plots the curves of Λ_F and Λ_G as a function of v. At low frequencies, v approaches 0 ($v = h/\delta$, $h \ll \delta$), then $\Lambda_F \approx 0$, which means the skin effect can be ignored. Λ_G is greater than Λ_F with respect to the same v. These two factors increase as v (or the frequency) increases. This implies that the higher the frequency, the more significant the skin and proximity effects become. Equation (14) indicates that the proximity effect losses are proportional to the square of the external magnetic field. Therefore, proximity effect losses tend to be dominant in high magnetic field regions, such as occur in multiple layer windings.

Fig. 7. Λ_F and Λ_G as a function of v.
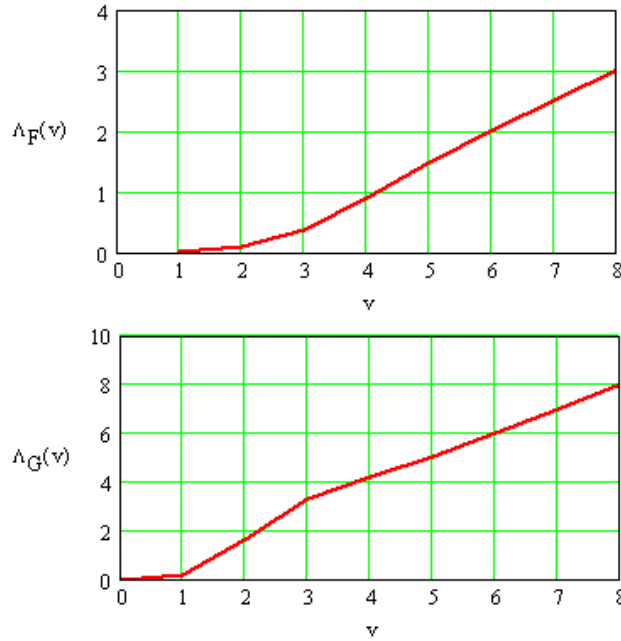
2.3.2 Multiple layer windings

Consider the power losses in a conventional transformer winding as shown in Fig. 8, where the primary and secondary windings each consist of three series-connected layers, the MMF diagram is illustrated below in the figure. Each layer has a thickness of h ($ h \gg \delta $), and carries a current with the peak value of I. It is assumed that the permeability of the core is infinite and the magnetizing current is very small.
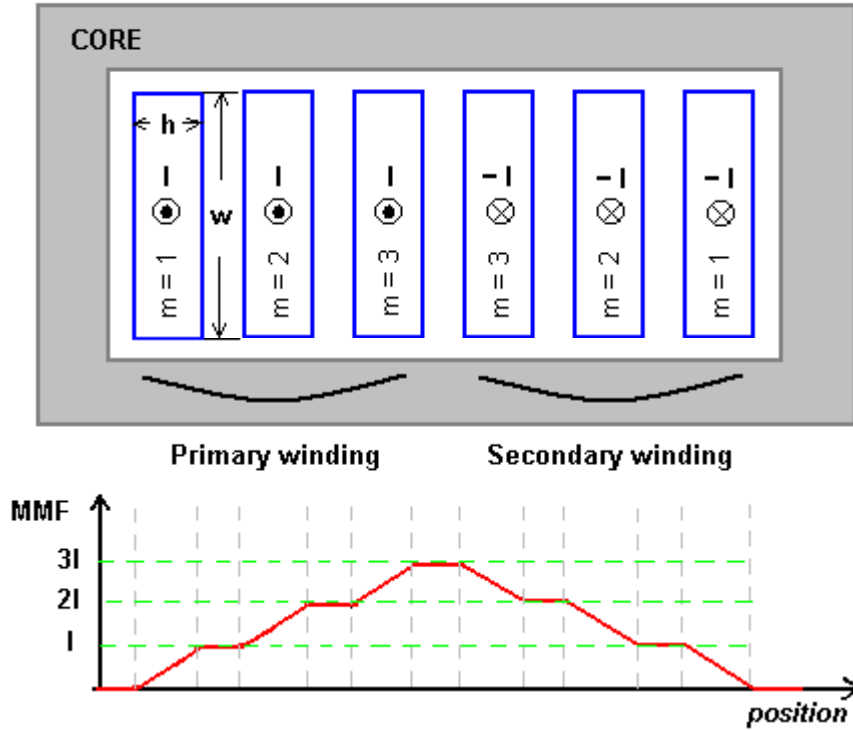
Fig. 8. A one-dimensional MMF diagram for a transformer winding.

The average magnetic field across the mth layer can be calculated by

$$H_m = \frac{(2m-1)}{2} \cdot \frac{I}{w} \tag{17}$$

By substituting (17) into (14), the losses in the mth layer is

$$P_m = \frac{v}{4} \cdot \frac{\sinh v + \sin v}{\cosh v - \cos v} \cdot R_{dc} I^2 + v \cdot \frac{\sinh v - \sin v}{\cosh v + \cos v} \cdot (\frac{2m-1}{2})^2 \cdot R_{dc} I^2 \tag{18}$$

So the equivalent AC resistance of the mth layer is

$$R_{ac\_m} = \frac{v}{2} \cdot \left[\frac{\sinh v + \sin v}{\cosh v - \cos v} + (2m-1)^2 \frac{\sinh v - \sin v}{\cosh v + \cos v} \right] \cdot R_{dc} \tag{19}$$

When $ v \gg 1 $ ($ v = h/\delta $),

17

$$\frac{\sinh v + \sin v}{\cosh v - \cos v} \approx 1, \text{ and} \tag{20}$$

$$\frac{\sinh v - \sin v}{\cosh v + \cos v} \approx 1 \tag{21}$$

So, (18) and (19) can be simplified as

$$P_m = \frac{v}{4} \cdot R_{dc} I^2 + v \cdot (\frac{2m-1}{2})^2 \cdot R_{dc} I^2, \text{ and} \tag{22}$$

$$R_{ac\_m} = \frac{v}{2} \cdot \left[1 + (2m-1)^2\right] \cdot R_{dc} \tag{23}$$

From (23), the equivalent AC resistances of layer1, layer2 and layer3 are

$$R_{ac\_1} = v \cdot R_{dc}, \tag{24}$$

$$R_{ac\_2} = 5v \cdot R_{dc}, \tag{25}$$

$$R_{ac\_3} = 13v \cdot R_{dc} \tag{26}$$

Fig. 9 illustrates the current distribution in the transformer winding, due to the skin and proximity effects. The current concentrates on the right surface of primary layer1, adjacent to layer2. The skin effect causes the copper loss in layer1 to be equal to the loss in a conductor of thickness δ with uniform current density. Therefore, the equivalent AC resistance of layer1 is increased by the factor h/δ, which is

$$R_{ac\_1} = \frac{h}{\delta} \cdot R_{dc} = v \cdot R_{dc} \tag{27}$$

the same as (24). The copper loss in layer1 is given by

$$P_1 = I^2 R_{ac\_1} \tag{28}$$
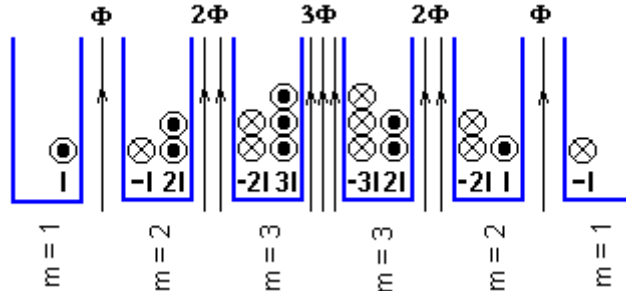
Fig. 9.　Current distribution in a transformer winding.

The proximity effect results in a current induced in the left surface of primary layer2, which tends to oppose the flux generated by the current of layer1. If the two layers are in

close proximity, and $h \gg \delta$, then the induced current will be equal to I but in the opposite direction. Since the net current in primary layer2 is I, a current of $2I$ must flow on the right surface of layer2. Therefore, the total copper loss in primary layer2 is

$$P_2 = (-I)^2 \cdot R_{ac\_1} + (2I)^2 \cdot R_{ac\_1} = 5I^2 \cdot R_{ac\_1} = 5P_1 \tag{29}$$

The AC resistance of layer2 is then given by

$$R_{ac\_2} = 5 \cdot R_{ac\_1} \tag{30}$$

Similarly, the AC resistance of layer3 can be calculated by

$$R_{ac\_3} = (2^2 + 3^3) \cdot R_{ac\_1} = 13 \cdot R_{ac\_1} \tag{31}$$

Obviously, the expression (30) and (31) agree with (25) and (26).

2.3.3 Litz wire winding

Litz wires-conductors made up of many isolated narrow strands twisted or woven together in a specific pattern as shown in Fig. 10, are commonly used to reduce the AC resistances of the windings. Litz wires are assembled so that each single strand, in the longitudinal development of the wire, occupies all the positions in the wire cross section. Therefore, not only the skin effect but also proximity effect is drastically reduced [2.4].
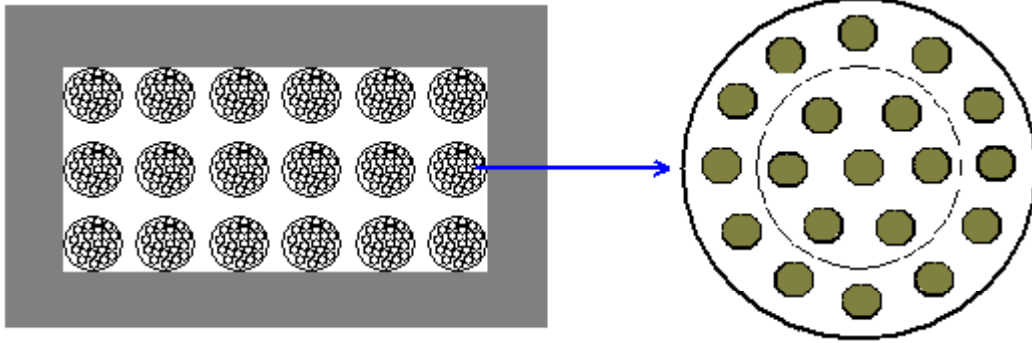
Fig. 10. Litz wire winding.

The analytical expression for the AC resistance of the litz wire winding derived by [2.4] is

$$R_w = R_{dc} \frac{\gamma_s}{2} \left\{ \frac{1}{n_s} \frac{ber\gamma_s bei'\gamma_s - bei\gamma_s ber'\gamma_s}{ber'^2\gamma_s + bei'^2\gamma_s} - 2\pi \left[\frac{4(N_l^2 - 1)}{3} + 1 \right] n_s \left(\eta_1^2 + \eta_2^2 \frac{p}{2\pi n_s} \right) \cdot \right.$$
$$\left. \frac{ber_2\gamma_s ber'\gamma_s - bei_2\gamma_s bei'\gamma_s}{ber^2\gamma_s + ber^2\gamma_s} \right\} \tag{32}$$

19

where $R_{dc} = 4\rho N l_T / n_s \pi d_s^2$ is the litz wire dc resistance, N is the number of turns of the winding, l_T is the average length of one turn of the winding, $p = N\pi r_s^2 / \pi r_o^2$ is the packing factor, r_o is the litz wire overall radius excluding the insulating layer, $r_s = d_s / 2$ is the single strand conductor radius, $\gamma_s = d_s / \delta\sqrt{2}$, $\eta_1 = d_s \sqrt{\pi} / 2t_o$ is the external porosity factor, t_o is the distance between the centers of two adjacent litz wire conductors, $\eta_2 = d_s \sqrt{\pi} / 2t_s$ is the internal porosity factor, t_s is the distance between the centers of two adjacent strands, taking into account the effective turn-to-turn, layer-to-layer, and strand-to-strand distances and the non-uniformity of the magnetic field.

The above solution is derived under the assumptions that the 1D approach can be applied, each winding layer is approximated as a foil conductor with the magnetic field parallel to the conductor surface, and the curvature of the windings is neglected.

Chapter 3. FE Modeling

3.1 Introduction

Most of the actual problems are very complicated and 3-dimensional, where 1D analytical approaches cannot be applied. Therefore, computer aided tools have been more and more involved in the magnetic component design. FEM method is one of the most popular numerical techniques. With the help of high performance computers, the simulation tools have greatly widened the range of the problems suitable to numerical analysis.

Maxwell® software developed by Ansoft is used to solve Maxwell's differential equations for quasi-static electromagnetic fields using FEM. The basic principle behind FEM is that it breaks up the problems into many tetrahedra (or elements), which are represented with separate polynomials. The collection of tetrahedra is referred to as the finite element mesh-or more simply, the mesh. A mesh is generated automatically for each model prior to computing a field solution. To obtain a precise description of the field, the system must size each tetrahedron so that it is small enough for the field to be adequately interpolated from the nodal values. Basically, there is a tradeoff between the size of the mesh and the desired level of accuracy. The accuracy of the solution depends on how small each of the individual elements is. However, for meshes with a large number of elements, it requires a significant amount of computing power and memory.

In the following, the theories on which electromagnetic, magnetostatics and eddy current solvers in Maxwell 3D rely are described. To calibrate the software, the skin and proximity effects on a single foil conductor are modeled using both 2D and 3D eddy current solvers. The simulation results show a good agreement with the analytical ones.

3.2 FEM Solvers

Maxwell 3D® consists of five solvers: 1) *Electrostatic Solver:* Computes the static electric field in a structure due to DC voltages and static charges; 2) *Magnetostatic Solver:* Computes the static magnetic field in a structure due to DC currents, external fields, and permanent magnets; 3) *Eddy Current Solver:* Computes the induced magnetic field in a structure due to AC currents and varying external fields, taking into account eddy current effects; 4) *Thermal Solver:* Computes the thermal quantities, like temperature distribution in a model; 5) *Transient Solver:* Computes the transient magnetic field of a model. The theories and equations behind the first three solvers are outlined in the following sections.

3.2.1 Electrostatic Solver

The electrostatic field simulator computes the electric potential ϕ using this equation:

$$\nabla \cdot (\varepsilon_r \varepsilon_o \nabla \phi) = -\rho \tag{33}$$

where $\phi(x, y, z)$ is the electric potential, ε_r is the relative permittivity, ε_o is the permittivity of free space, and ρ is the charge density. This equation is derived from Gauss's law, in differential form, which is,

$$\nabla \cdot D = \rho \tag{34}$$

where $D(x, y, z)$ is the electric flux density. Since in a static field,

$$D = \varepsilon_r \varepsilon_o E \text{, and} \tag{35}$$

$$E = -\nabla \phi \tag{36}$$

by substituting $-\varepsilon_r \varepsilon_o \nabla \phi$ for D, (36) can be obtained. The solver computes and stores the value of the electric potential at the vertices and midpoints of the edges of each tetrahedron in the finite mesh. After that, the system solves for the E-field and D-field using the above equations. The electric field energy is given by

$$U = \frac{1}{2} \int_V E \cdot D dV \,. \tag{37}$$

where $V \equiv Volume$

Since the energy can also be expressed as

$$U = \frac{1}{2} C \cdot V^2 \quad , \tag{38}$$

The lumped capacitance C can be calculated by

$$C = \frac{1}{V^2} \int_V E \cdot D dV \tag{39}$$

3.2.2 Magnetostatic Solver

The system computes the static magnetic field in two steps. First, a conduction simulation is performed, in which perfect or non-perfect conductors are involved. The current density J, is proportional to the electric field that is established due to a potential difference, expressed as

$$J = \sigma E = -\sigma \cdot \nabla \phi \tag{40}$$

Under the steady state conditions, the net charge leaving any infinitesimally small region must be equal to the charge flowing into that region. That is the charge density $\rho(x, y, z)$ in any region does not change with time:

$$\nabla \cdot J = \frac{\partial \rho}{\partial t} = 0 \tag{41}$$

Therefore, the equation in terms of the electric potential ϕ is

$$\nabla \cdot (\sigma \cdot \nabla \phi) = 0 \tag{42}$$

After computing the current density, the magnetostatic field solver computes the magnetic field using Ampere's Law and the Maxwell's equation:

$$\nabla \times H = J \tag{43}$$

$$\nabla \cdot B = 0 \tag{44}$$

The energy stored in a static magnetic field is given by

$$U = \frac{1}{2} LI^2 = \frac{1}{2} \int_V H \cdot B dV \tag{45}$$

The inductance L can be calculated as follows:

$$L = \frac{1}{I^2} \int_V H \cdot B dV \tag{46}$$

3.2.3 Eddy Current Solver

The eddy current field simulator assumes that the magnetic field and all other time-varying quantities are stored as phasors, which can be visualized as a magnitude and phase or as a complex quantity. After specifying all AC current sources and all necessary boundary conditions, the system computes the magnetic field as follows:

In conductors where eddy currents occur, H is calculated directly by:

$$\nabla \times \left(\frac{1}{\sigma + j\omega\varepsilon} \nabla \times H \right) = j\omega\mu H \tag{47}$$

(Since $\nabla \times H = J + \dfrac{\partial}{\partial t}\varepsilon E = \sigma E + \dfrac{\partial}{\partial t}\varepsilon E = (\sigma + j\omega\varepsilon)E$, and $\nabla \times E = -\dfrac{\partial B}{\partial t}$).

Or, H is computed from the magnetic scalar potential ϕ:

$$\nabla \cdot (\mu \nabla \phi) = 0 \tag{48}$$

Induced currents allow magnetic fields to penetrate conductors only to a certain depth, which is approximated by the formula:

$$\delta = \sqrt{\frac{2}{\omega\sigma\mu_o\mu_r}} \tag{49}$$

The AC magnetic field energy is given by:

$$U_{AV} = \frac{1}{4} \int_V B \cdot H^* dV \tag{50}$$

where H^* is the complex conjugate of the magnetic field H. Ohmic loss is used to compute the power loss in a structure, which is

$$P = \int_V \frac{J \cdot J^*}{2\sigma} dV \tag{51}$$

where J^* is the complex conjugate of the current density J. Ohmic loss can also be expressed in terms of resistance and the total current:

$$P = RI_{RMS}^{\;2} \tag{52}$$

Therefore, the resistance is:

$$R = \frac{P}{I_{RMS}^{\;2}} = \frac{\frac{1}{2\sigma} \int_V J \cdot J^* dV}{I_{RMS}^{\;2}} = \frac{\int_V J \cdot J^* dV}{\sigma I_{peak}^{\;2}} \tag{53}$$

24

where I_{peak} is the peak current.

3.3   Model Descriptions

The eddy current solver in Maxwell 2D and 3D is utilized for analyzing the skin and proximity effects on a single foil conductor. In order to evaluate the program, the simulation results of the current density distribution across the thickness of the foil conductor are compared with 1D analytical solutions discussed in the previous chapter. When defining 2D and 3D models, it is essential to satisfy the assumptions that validate 1D solutions.

3.3.1   2D Model

The first step is to define a 2D geometric model so that the assumption that the model is infinite in one direction is satisfied. Fig. 11 shows 2D-view of the models. The width of a foil conductor represented by "A" area, is $15mm$, which is much larger than its thickness of $70um$, so that 1D approximation is still correct. In the model, the target foil conductor is also surrounded by a core with the property of high permeability, represented by "B" area, and the conductor fully fills the core window width, for the purpose of minimizing the perpendicular component of the magnetic field near the ends of the conductor. "C" and "D" areas represent two perfect conductors, which form a closed current loop to provide a uniform external magnetic field on the foil.

The second step is to define materials for different objects. The conductor material is copper with its typical property ($\sigma = 5.8 \times 10^7 \ (\Omega \cdot m)^{-1}$). A self-defined material with high permeability ($\mu = 10^{10} \mu_0$) is used for the core. The background is filled with air.

This is followed by setting up boundary conditions and current sources. To investigate the skin effect on the conductor, it is assumed that a sinusoidal current with the peak magnitude of 1A flows into the foil conductor as shown in Fig. 11(a). For analyzing the proximity effect, current sources of the same magnitude in opposite direction are imposed on the top and bottom conductors instead of the foil as shown in Fig. 11(b). In both cases,

the balloon boundary condition is assumed, which means that a surface far away from the core has a magnetic vector potential of zero.
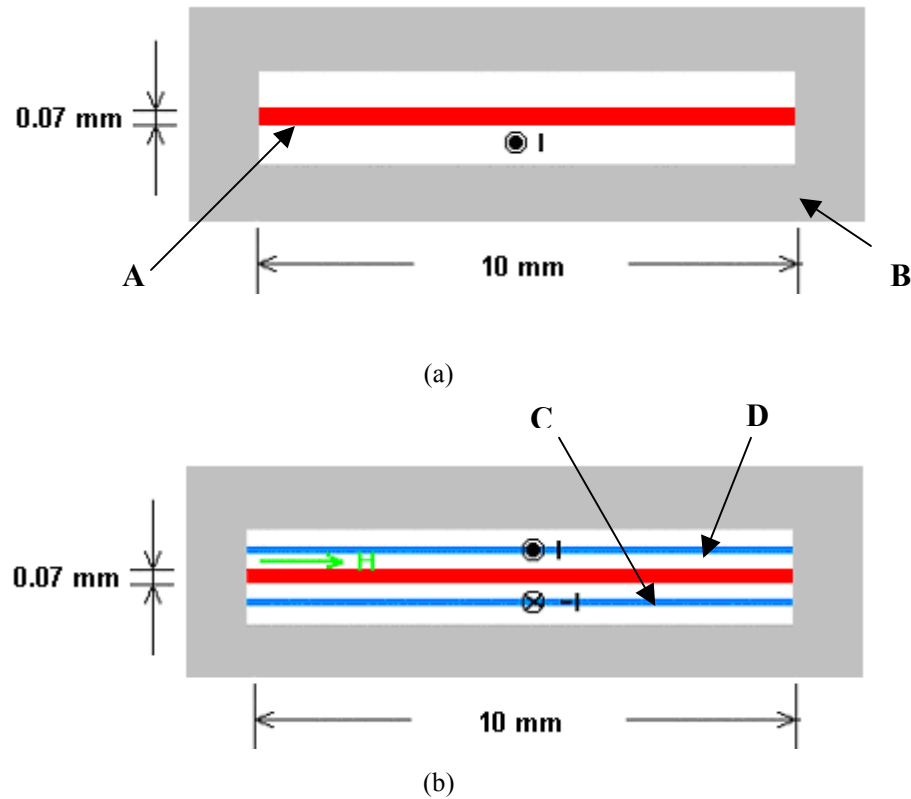

(a)

(b)

Fig. 11. 2D models: (a) Skin effect; (b) Proximity effect.

(A: foil conductor; B: high permeability core; C and D: closed current loop to generate H field)

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3.3.2 3D Model

The 3D eddy current solver can be used to analyze the skin and proximity effects on a foil conductor. Fig. 12 illustrates the 3D models that are used to investigate skin and proximity effects, which can be thought of as a small portion of a whole structure with infinite length. An odd symmetry boundary condition is assigned to the cut planes represented by the light area, in which current on one side of a plane flows in the opposite direction to current on the other side of the plane, indicating that the magnetic flux is tangential to the boundary and its normal components are equal to zero. The procedures for defining the models and material properties, and setting up boundary conditions and sources, are the same as those described for the 2D solver. In addition, a mesh is

generated manually on the foil conductor before an automatically iterative computation begins. This step is not necessary when solving 2D problems, because automatic mesh generator was found to give accurate results.

(a)

(b)
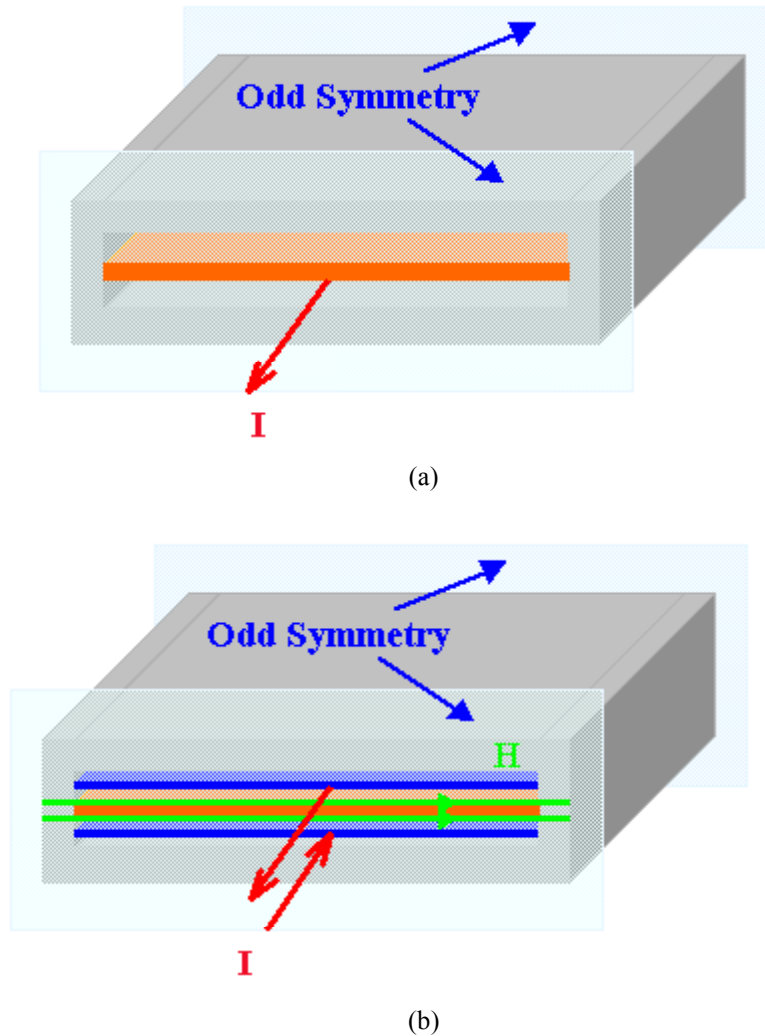
Fig. 12. 3D models: (a) Skin effect; (b) Proximity effect.

3.3.3   Simulation Results

Fig. 13 and 14 show the current density J distribution across the thickness of the foil conductor at the excitation frequency of 500 kHz, due to the skin and proximity effects respectively, where 1D analytical, 2D and 3D FEM simulation results are plotted together. It can be seen clearly that 2D FEM simulation results match the analytical solutions very well. Although there exist some discrepancies in 3D results, they are still tolerable. In

practice, 3D problems cannot be reduced to 2D. Therefore, 3D modeling is more useful in practice, despite the fact that 3D simulation is usually time consuming and the precise solution is not always obtained.
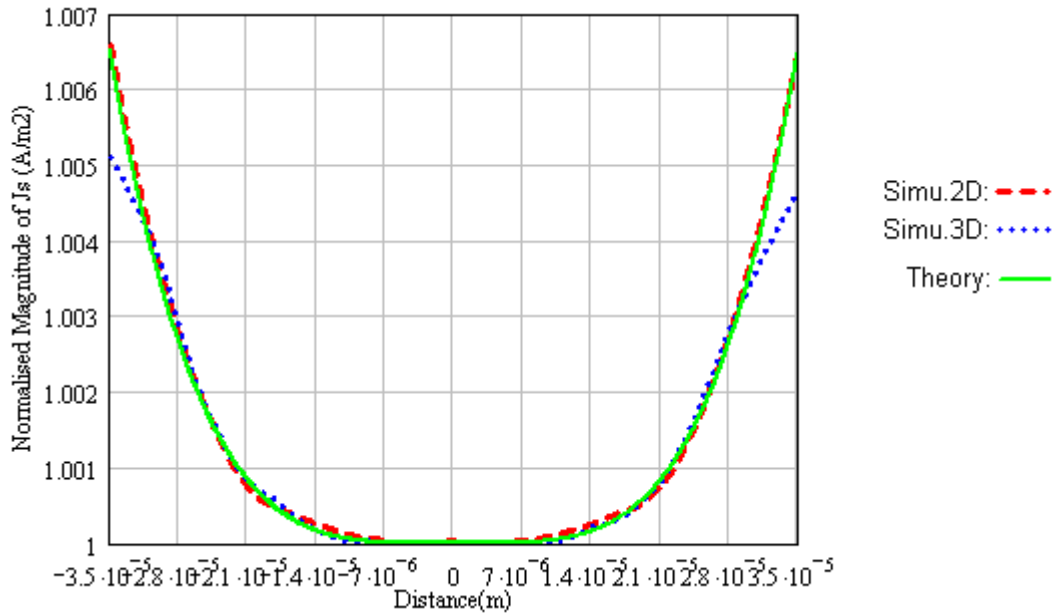
(a)
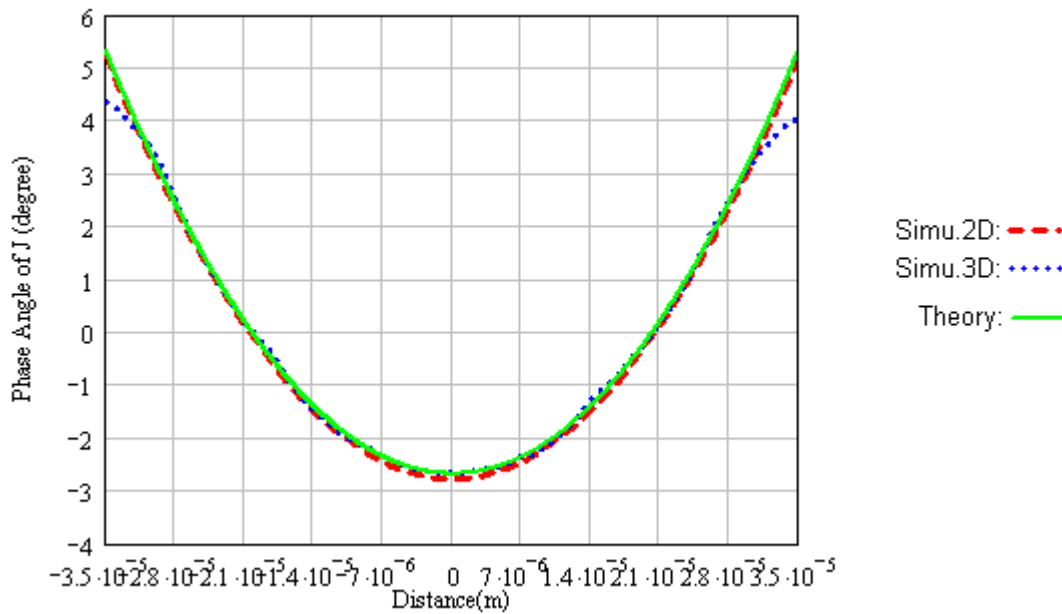
(b)

Fig. 13. Current density distribution across the thickness of the foil conductor due to the skin effect:(a) Normalized magnetude; (b) Phase angle.
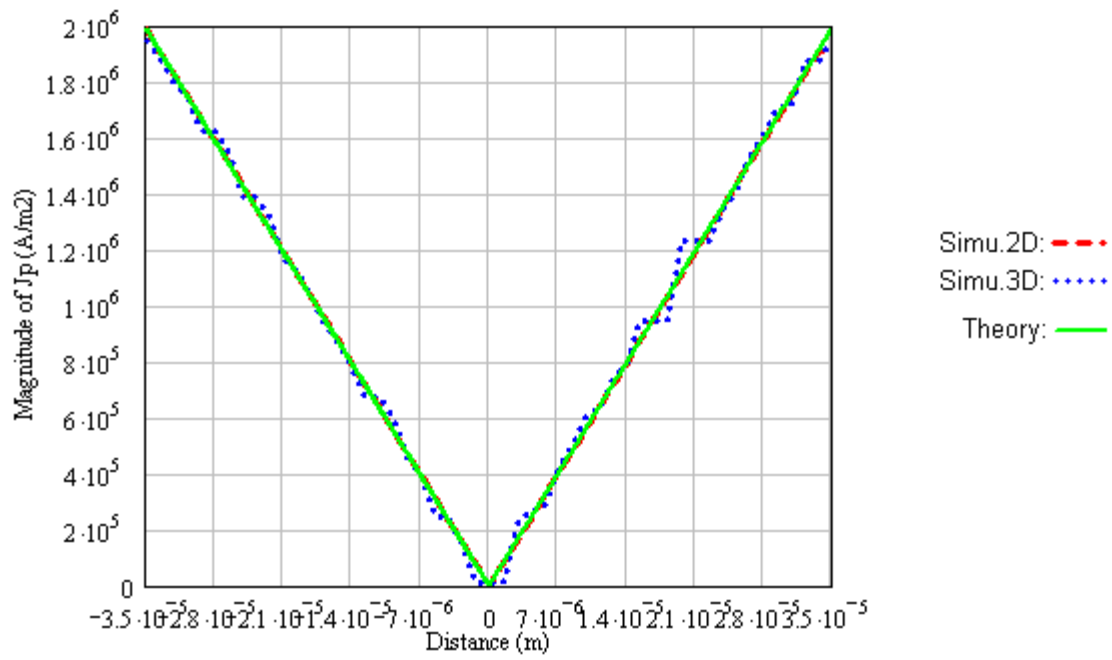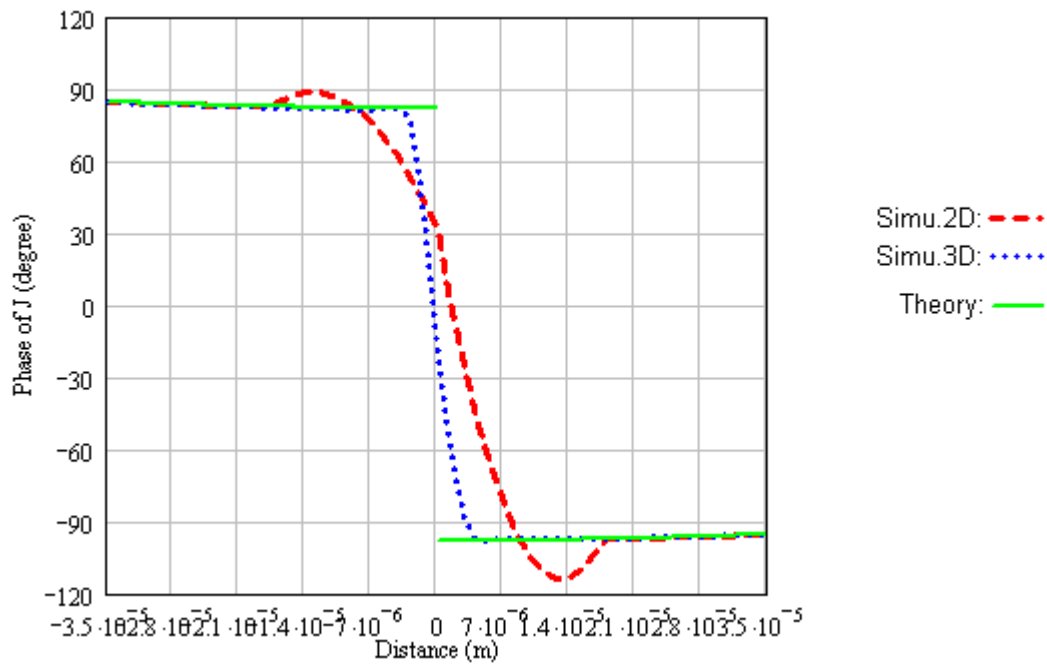
28

(a)

(b)

Fig. 14. Current density distribution across the thickness of the foil conductor due to the proximity effect: (a) Magnitude; (b) Phase angle.

Chapter 4. Planar Litz Conductor

4.1   Introduction

At high frequencies, AC losses induced in planar inductor and transformer windings become significant due to the skin and proximity effects. For round conductor, litz wires have traditionally been used to reduce the conduction losses. A litz wire is constructed so that each single strand along the length of the wire occupies all the positions in the wire cross-section. Both the skin effect and the proximity effect are thereby reduced. Inspired by the round litz wire, the planar litz structure was proposed previously [4.1] to reduce the AC resistance of the planar conductor. A planar litz conductor can be constructed by dividing the wide planar conductor into multiple lengthwise strands and weaving these strands in much the same manner as one would use to construct a conventional round litz wire. Each strand is subjected to the magnetic field everywhere in the winding window, thereby equalizing the flux linkage. 3D FE modeling is performed for some simple models. The simulation results show that the planar litz conductor can have a lower AC resistance than a solid foil conductor on a specific frequency range. The performance of the planar litz winding is also verified with measurements on experimental prototypes.

4.2   Planar Litz Conductor Concept

Winding AC resistance depends on both the operating frequency and the winding structure. For wide planar conductors at high frequencies, the current will be concentrated at the two ends of the conductor, despite the fact that the conductor thickness approaches

skin depth. In order to overcome the planar conductor inefficiency problem, a planar litz structure is introduced.

The term *litz* refers to conductors constructed according to a carefully prescribed pattern. The methods for constructing the planar litz conductor is to divide the wide conductor into many isolated lengthwise strands and then weave these strands into a thicker conductor. Some definitions and guidelines are provided below, on which the design of a planar litz conductor is based.

A.   Definitions for a planar litz conductor (Fig. 15)
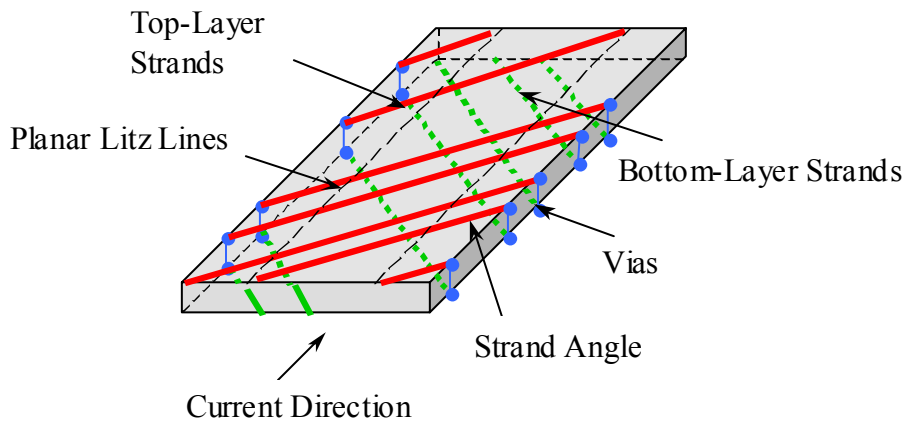

Fig. 15. Planar litz conductor definitions.

Strand/s: Narrow conductor/s used to make up a planar litz conductor

Planar Litz Conductor: A planar conductor comprised of many isolated strands that are weaved together to form a single high-frequency, higher-current-carrying-capacity conductor.

Strand Angle: The angle the strand makes with the direction of the planar litz conductor

Planar Litz Lines: The lines parallel to the direction of the conductor, which are spaced equidistant across the width of the planar litz conductor. The edges of the planar litz conductor are also defined as a planar litz line. The number of lines and the spacing between the lines will determine the maximum width of the strands, the minimum spacing between the strands, and the number of strands. The following equation gives the distance between these lines as a function of the spacing between the strands, the width of the strands and the strand angle, referring to Fig. 15,

$$w_{PLC-line} = \frac{w_{space} + w_{strand}}{\cos(\theta_{strand})} \qquad (54)$$

where $w_{PLC-line}$ is the distance between the planar litz conductor lines, w_{space} is the spacing between strands, w_{strand} is strand width and θ_{strand} is strand angle. The following equation gives the relationship between the number of lines to the number of strands:

$$n_{strands} = 2 \cdot (n_{lines} - 1) \qquad (55)$$

where $n_{strands}$ is the number of strands and n_{lines} is the number of lines.

B.   Guidelines for a planar litz conductor

1. Any **improvement** over a single planar conductor is an improvement.

2. An **extra layer** will be required, however the additional thickness that is introduced by this additional layer will not significantly increase the thickness of the layer on which it is applied due to it being manufactured as a whole. Multiple layer structures are also possible by zigzagging additional layers as shown in Fig. 16. The various layers can be inter-connected by example of making use of buried and blind vias.
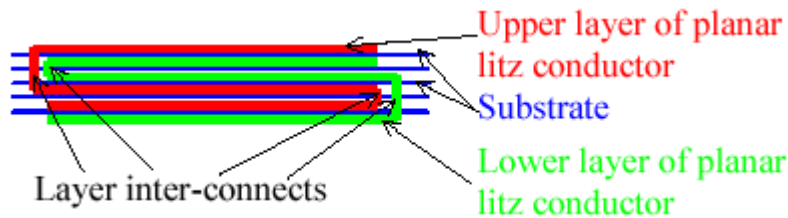

Fig. 16. Cross-section of a multi-layer planar litz conductor.

3. The **minimum number of litz strands** that can be used is three, using less has no influence on the proximity effect that the litz conductor is supposed to improve.

4. All the **litz strands must be of equal length and width** so that the impedances of each strand will be the same, and the current division between each litz strand will be equal. (some deviation is allowed in order to make the planar litz conductor realizable, as will be shown later).

5. The **skin depth** is to be used as a normalized measure of **thickness for the strands** in the planar litz conductor. The higher the operating frequency, the thinner the conductor would become.

6. Each strand could have a **different length**, due to the nature in which the planar litz conductor would have to be constructed in practice. The relationship of the **average length of a strand** $l_{strand-avg}$ to that of the planar litz conductor l_{PLC}, and strand angle θ_{strand}, is given by the following equation:

$$l_{strand-avg} = \frac{l_{PLC}}{\cos(\theta_{strand})} \tag{56}$$

7. The **isolation requirement between strands is very low**, as the voltage difference between adjacent strands would be very low with respect to the voltage applied to the total conductor. This means that the strands can be placed very close to each other. The closer the strands are placed to each other, the more effective conductor area can be created. However, the proximity effect losses among the strands become severer.

8. The **isolation requirement between the inner and outer layers of the planar litz conductor is also low** with respect to the total voltage applied to the planar litz conductor. It is however, higher than that between adjacent strands on the same layer. This is due to the criss-cross nature of the litz strand make-up and the small voltage differences that will occur between different positions of the strands. Since the voltage differences are generally small, a very thin insulating material can be used to isolate the inner and outer layers.

9. The **litz strand may zigzag** within the winding window for as many times as is realizable. The higher the number of times this occurs, the greater the improvement on the current distribution of the planar litz conductor.

10. The planar litz conductor width w_{PLC} is dependent on these factors: the width of the strands w_{strand} (assuming each strand has equal width), the spacing between the strands w_{space} (assuming equal spacing between each of the strands), the strand angle θ_{strand} and the number of the strands $n_{strands}$. The width of the planar litz conductor can be calculated as follows:

$$w_{PLC} = \frac{[(n_{strands}+1) \cdot w_{strand} + n_{strands} \cdot w_{space}] \cdot \sin(\theta_{strand})}{\cos(2 \cdot \theta_{strand} - \frac{\pi}{2})} \tag{57}$$

11. An **appropriate technique** should be used to **connect the layers** on the **outer edges of the planar litz conductor**. An example of an interconnection could be a through hole via.
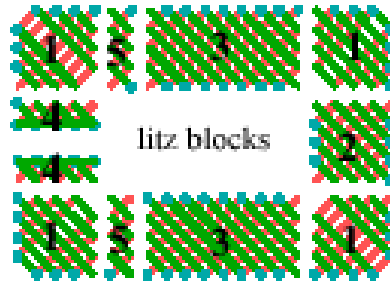

Fig. 17. Planar litz conductor sections.

In order for a planar litz conductor to adhere to the guidelines above, the design should be reduced to some discrete sections, which can realize in a swift manner the desired planar litz conductor and can quickly determine the limitations imposed when using a planar litz conductor on the design of the magnetic structure. The larger the number of strands, the more important it becomes to use a section method to reduce the risk of errors. Fig. 17 illustrates the basic sections of a planar litz conductor, which will be explained in details.

1. **A corner section.** The start position relative to the end position of a strand on a line will not be affected when using this section.

2. **A square section.** The position of the strand on a line will cross over as counted from the alternate side of the planar conductor edge. This section must be used at least an odd number of times as shown in Fig. 17. Section #2 can be placed between section #3 and #5, #1 and #3, or #1 and #5, so that guideline #4 can be complied with. The following equation describes the line position change of a strand where the strand starts in line x and ends in line y,

$$x \leq n_{lines} \tag{58}$$

$$y = (n_{lines} + 1) - x \tag{59}$$

3. **A rectangle section.** The length of this block is twice its width, so that a strand's start position relative to the end position on a line remains unaffected.

4. **A termination section.** This section is used to terminate the planar litz conductor and is used on the ends of the winding only. It can consist of any number of strand line changes, up to but not including the size of a square section.

5. **A termination compensation section.** This section is used to offset the irregular strand line crossings that have occurred with the use of a termination block and must be of the same size as the termination section. An equal number of termination compensation sections to terminations blocks must be used for a single winding.

In practice, core dimension must also be taken into account. The core aspect ratio can be adjusted to accommodate the sections sizes.

4.3   3D FE Modeling

### 4.3.1   Design of a planar litz conductor

Due to the computation limitation, a simple structure, that is, a single planar litz winding, will be modeled. However, for a single conductor, only the skin effect exists at high frequencies. A pair of gapped E cores is also added to provide the proximity effect on the winding. Fig. 18 and 19 show the top and cross-section views of the winding design. It consists of 20 strands. Between them is FR4, which is one of the typical dielectric materials used for printed circuit board (PCB) manufacturing. The core chosen is a standard planar E core using 3F3 material. Table 1 lists the parameters of the design.
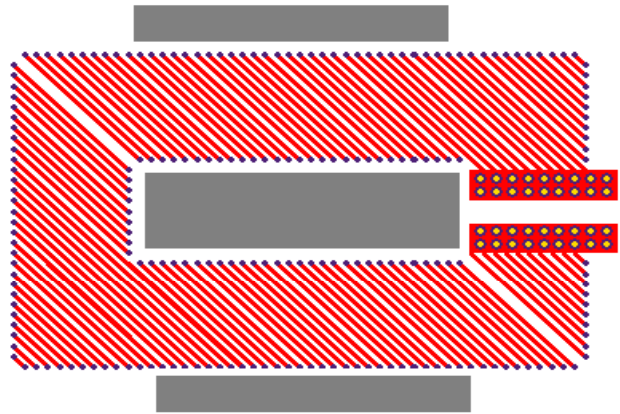
(a)
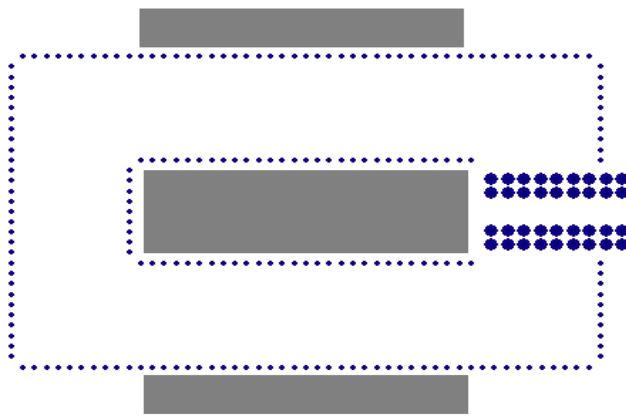
(b)
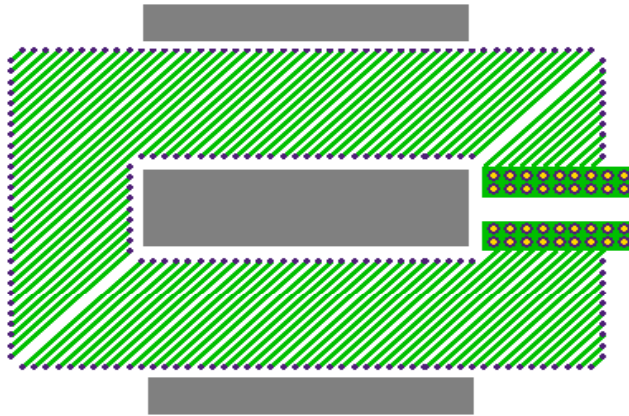
(c)

Fig. 18. Top view of a single planar litz winding with a planar E core:
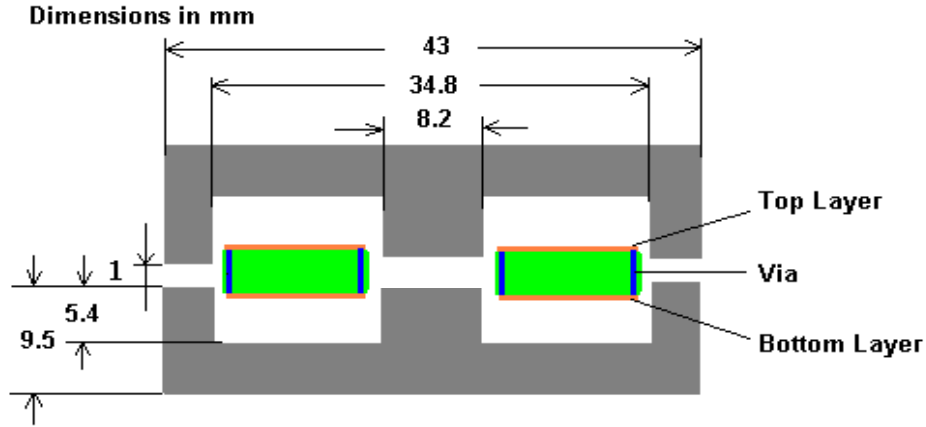(a) Top layer, (b) Via layer and (c) Bottom layer.

36

Fig. 19. Cross-section view of a single planar litz winding with a planar E core.

Table 1. Parameters of the design.

Core Size	E 43/10/28
Number of Strands	20
Strand Thickness (mil)	1.4 (1oz cu)
Strand Width (mil)	20
Strand Spacing (mil)	10
PCB Material	FR4
Material Thickness (mil)	62

4.3.2 3D FE Simulation and results analysis

The current distribution in a planar litz structure is a 3D problem that necessitates FEM numerical computation. The simple approach to this problem is to simulate a small section, as shown in Fig. 20. For it to qualify as being a representative of the whole structure, the analyzed section of the winding has 20 strands, and each strand can see every point of the cross-sectional conduction area. Therefore, its length is at least twice its width, because the strand angle is 45°. In order to compare the planar litz conductor with the conventional solid conductor, another model, shown in Fig. 21, was also developed.
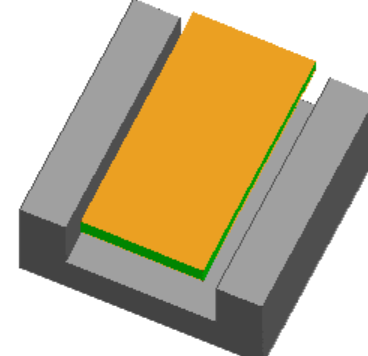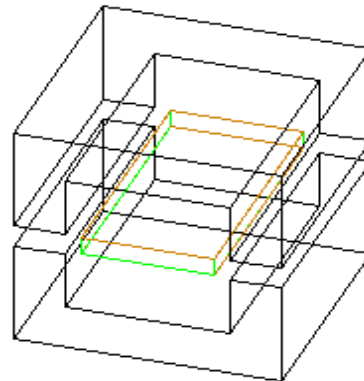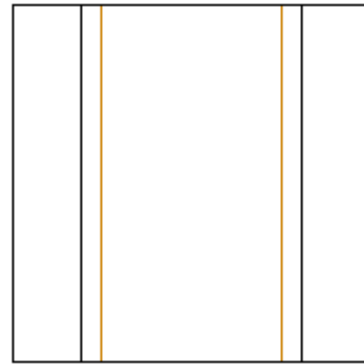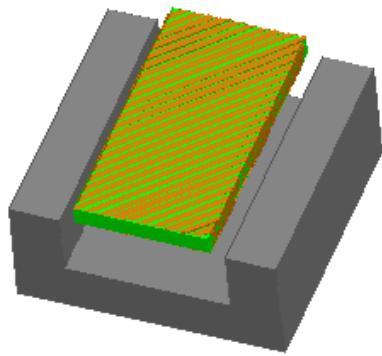
37
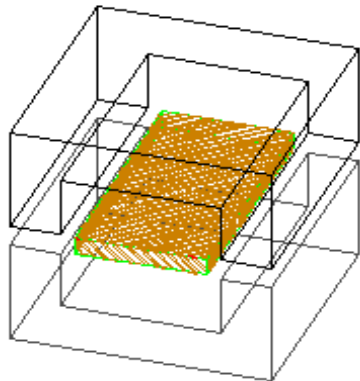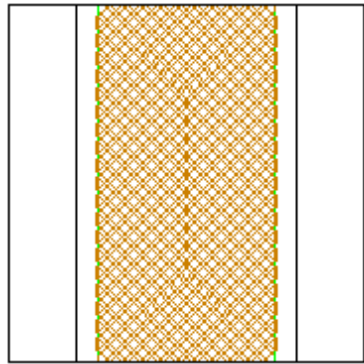
Fig. 20. 3D model of a planar litz conductor.

Fig. 21. 3D model of a solid conductor.

Fig. 22 shows the 3D FEM simulation results for normalized AC resistance of these two conductors in the frequency range from 100 kHz to 2 MHz. It can be seen clearly that, at the frequencies from 200 kHz to 1.5 MHz, the litz conductor has lower AC resistance than the solid conductor. Fig. 23 plots the current distribution on the windings at 1 MHz. At the two edges of the solid conductor, the current is highly concentrated, due

to the proximity effect. However, the current distribution on the litz conductor is nearly uniform; therefore, the effective resistance is reduced.

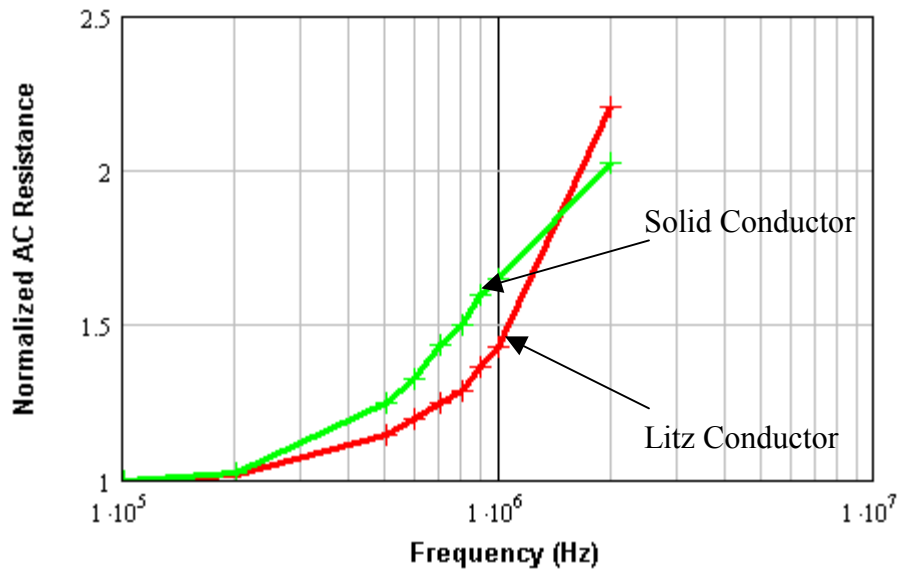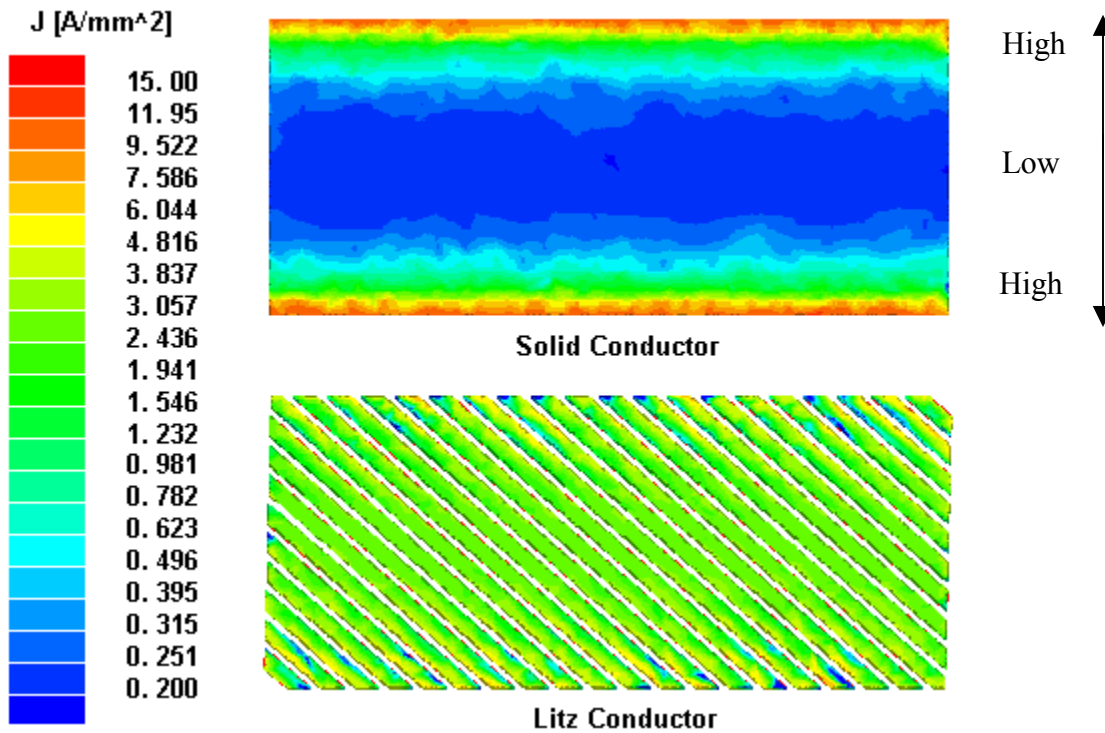Fig. 22. Simulation results of normalized AC resistance vs. frequency.

Fig. 23. Current distribution on solid conductor and litz conductor.

At lower frequencies, the litz winding is not preferred because it may reduce the window filling factor. Above some frequency, the proximity effect losses induced by the strands would compensate for all the advantages of the litz winding over the solid conductor winding. Therefore, we can only benefit from litz winding in a specific frequency range. Actually, the range largely depends on the winding configuration and the external field. 3D FEM simulation gives good insight into this problem.

4.3.3   Impact of winding configuration

To look into the impact of winding configuration on the litz performance, two planar litz conductors of equal length and width are modeled, as shown in Fig 24. Model I consists of 16 strands, and Model II has 10 strands. The conductors are designed to have the same DC resistances. The geometries of these two models are summarized in Table 2.
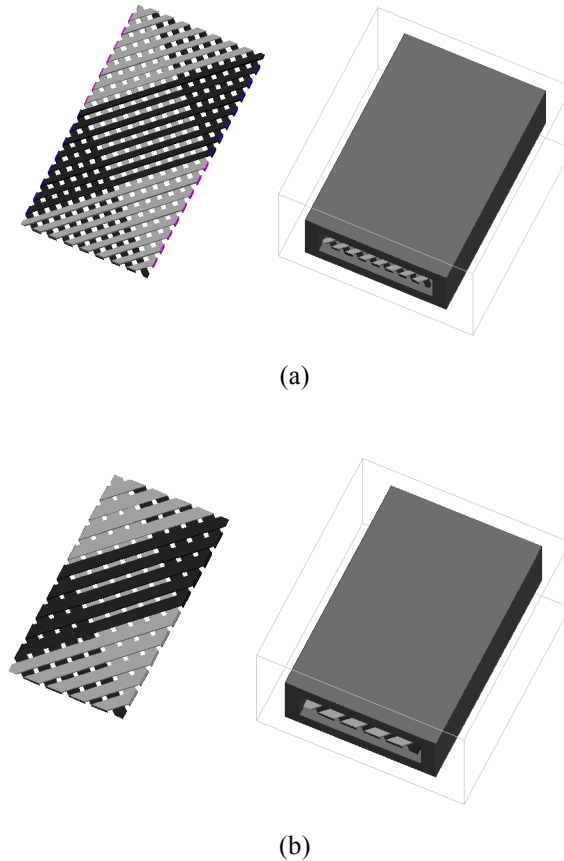

(a)

(b)

Fig. 24. 3D-view of planar litz conductors: (a) Model I: 16 strands and (b) Model II: 10 strands.

Fig. 25 shows the AC resistances of these two models. Obviously, Model II has higher AC resistance than Model I, especially at high frequencies. This indicates that the more the strands, the more effective the litz conductor (see guideline #4).
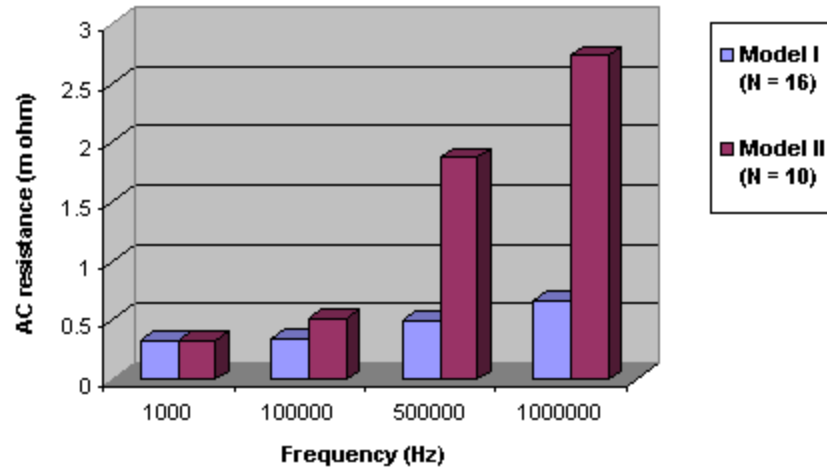

Fig. 25. AC resistances of two models.

Table 2. Geometries of the models.

Parameters	Model I	Model II
Number of strands	16	10
Strand Width (mm)	0.5	1.1
Strand Thickness (mm)	0.1	0.0727
Strand Spacing (mm)	0.5	0.5
Layer Distance (mm)	0.1	0.1
Conductor Width (mm)	8	8
Conductor Thickness (mm)	0.3	0.245
Conductor length (mm)	16	16
Inner window area of the core (mm^2)	2.3×8.6	2.3×8.6
Outer window area of the core (mm^2)	4.3×10.6	4.3×10.6
Core length (mm)	16	16

4.3.4   Impact of external magnetic field

AC resistance of the winding conductor is not only associated with its own physical structure, but also relative to the external magnetic field. Intuitively it seems that the advantages of the planar litz conductor over single solid conductor will be significant

41

when it is applied in a high magnetic field region. The impact of the external magnetic field on the litz performance can be investigated by comparing the AC resistances of the planar litz conductor and solid conductor in a non-gapped core and a gapped core configurations. Fig. 26 and 27 plot the 3D FEM simulation results.
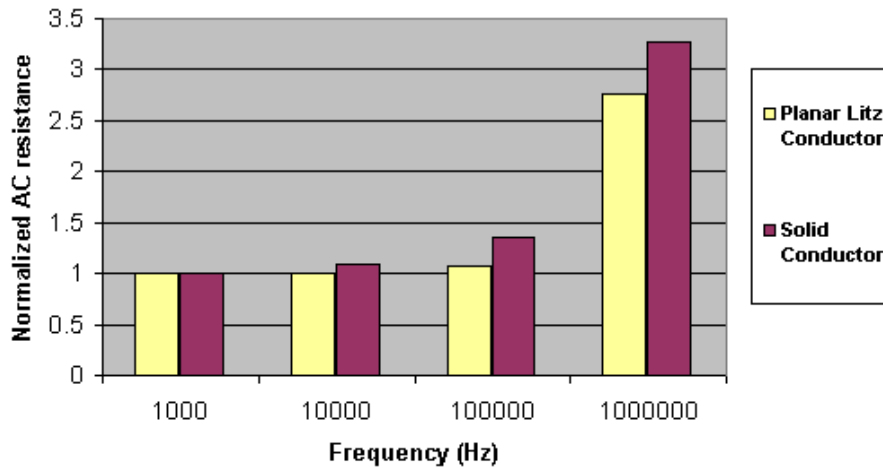
Fig. 26. Normalized AC resistances of planar litz conductor and solid conductor with a non-gapped core.
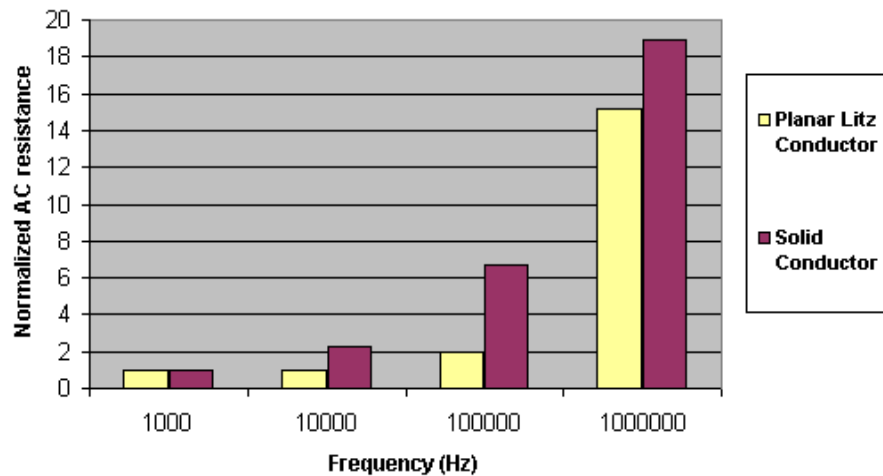
Fig. 27. Normalized AC resistances of planar litz conductor and solid conductor with a gapped core.

In the second circumstance, the gap-fringing field causes the proximity effect losses of the winding conductor to be more sever, so the importance of using a litz conductor is more dramatic. This demonstrates that the planar litz conductor is very effective in reducing AC resistance by reducing the proximity effect on the planar conductor.

4.4 Experimental Verification

The performance of the planar litz conductor needs to be verified experimentally. Two experimental prototypes, a three-turn planar litz winding and a three-turn solid conductor winding shown in Fig. 28, were constructed on the PCB. The structure of each single litz winding is identical to the model described in section 4.3.1. For comparison, the solid conductor winding is designed to have the same DC resistance as the litz winding. An Agilent 4294A precision Impedance Analyzer is utilized to measure the AC resistances of the windings with a gapped ferrite core and without a core. For the measurement with a core, different gaps are used. Fig. 29 shows the measured AC to DC resistance ratio of the planar litz winding and the solid conductor winding for four different cases. Although core loss may cause some errors in the measurement with a core, the effect can be ignored because the excitation is small, and the errors are equally induced in two windings.

<div align="center">(a)   (b)</div>
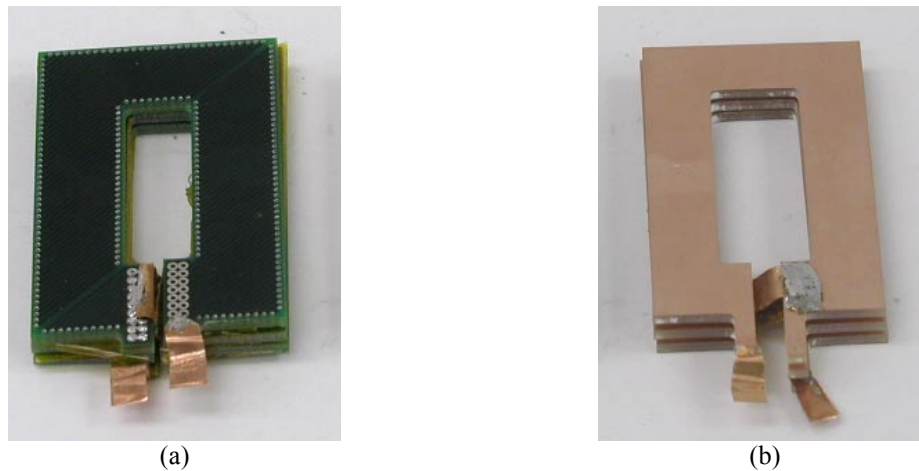
Fig. 28. Top view of experimental prototypes: (a) Litz winding and (b) Soilid conductor winding.

The measured results demonstrate that the litz winding can outperform the solid conductor winding over a wide frequency range, either with or without a core. The trend of the curves is close to the simulation results. For our specific design, the litz winding can result in lower AC resistance from 20 kHz up to 700 kHz. At 200 kHz, the reduction of AC resistance by using the litz winding instead of the solid conductor can be as high as 30%. The AC resistance of the winding with the gapped core increases more dramatically at high frequencies than does the winding without the core because of the fringing effect

around the air gap. However, the impact of the gap length on the performance of the litz winding is small.
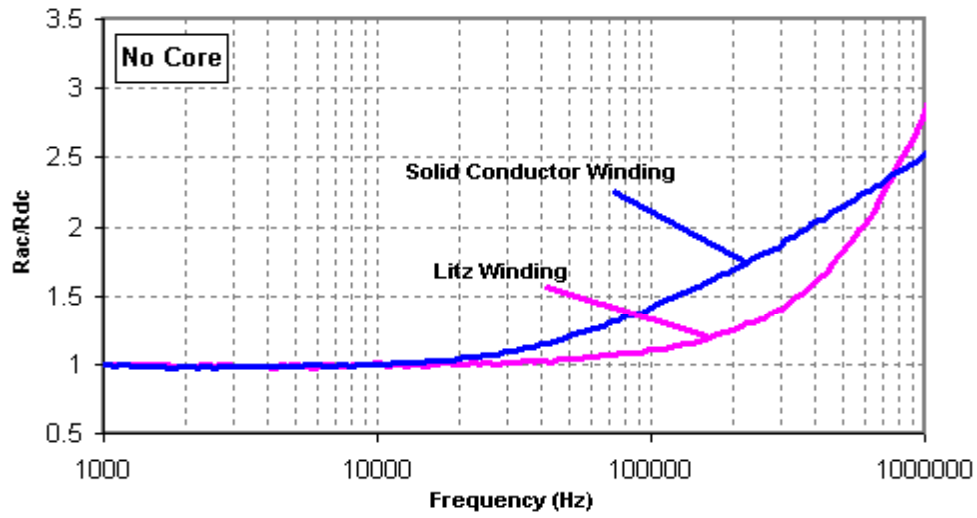
(a)
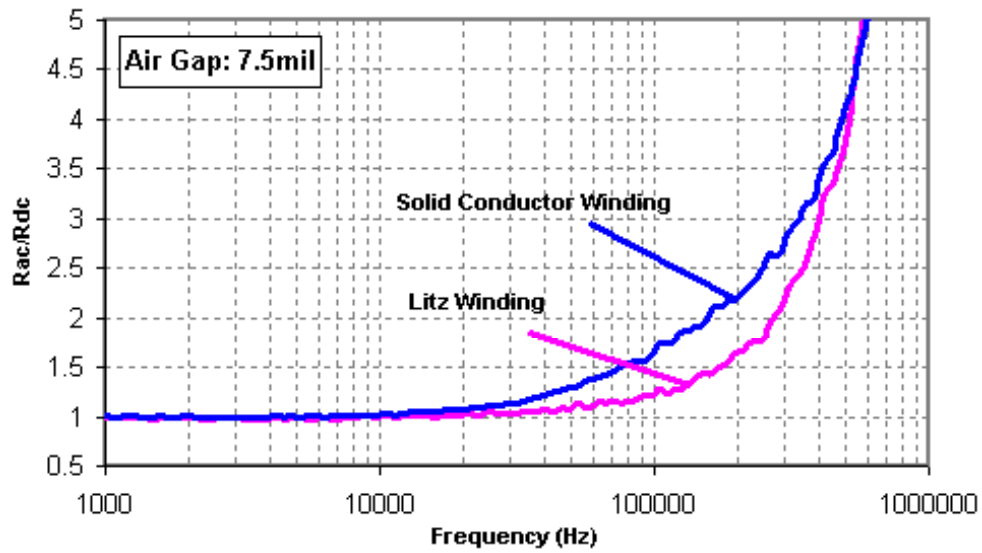
(b)
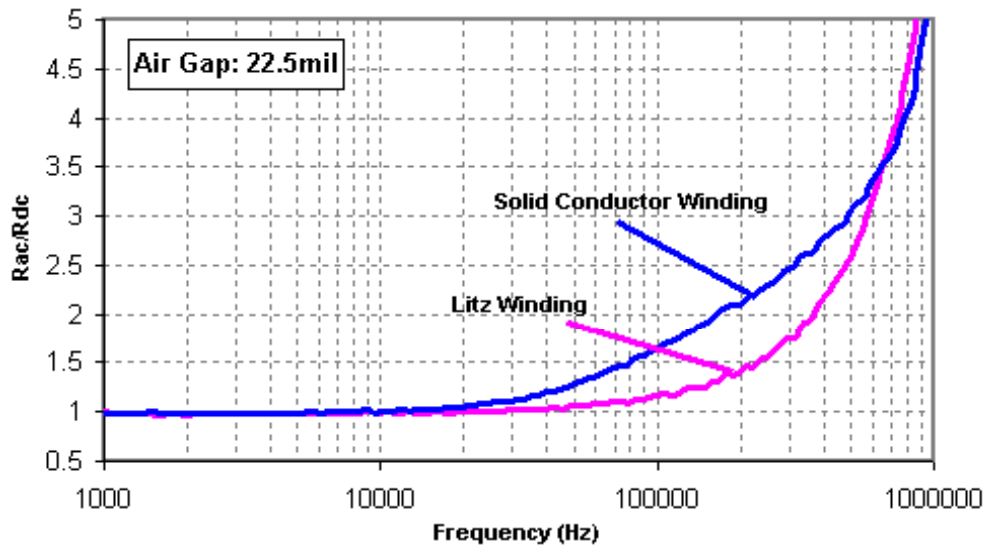
(c)
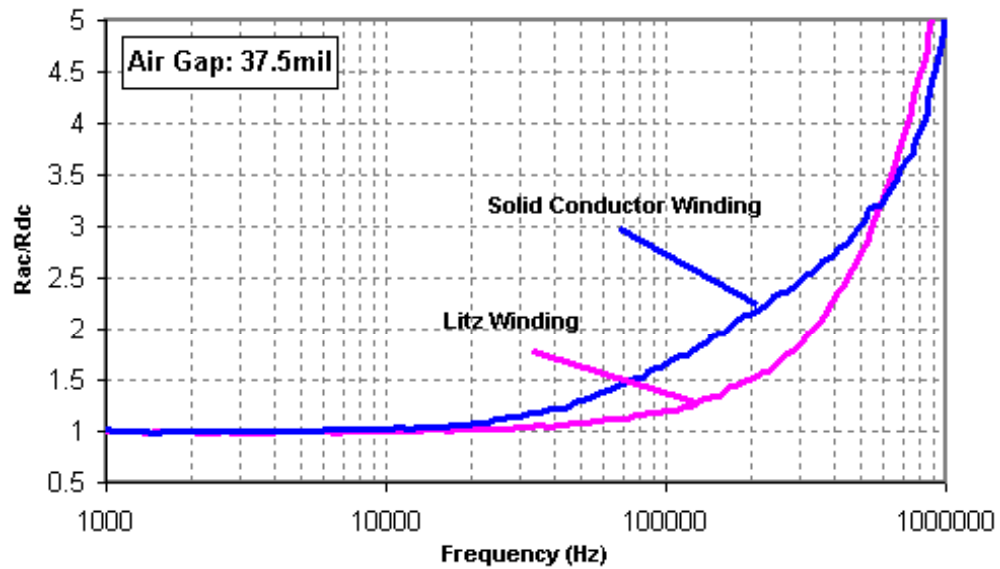
(d)

Fig. 29. Measured results of normalized AC resistance vs. frequency: (a) No core; (b) Air gap: 7.5mil; (c) Air gap: 22.5mil; (d)Air gap: 37.5mil.

4.5 Conclusions

A planar litz structure is investigated further in this chapter, aiming to reduce the high-frequency losses in the planar windings. The planar litz conductor is constructed by weaving many narrow strands along the length of the conductor in such a pattern that each strand be subjected to every point of the winding cross section. Thus, the current is distributed uniformly on the conductors. 3D FEM indicates that the planar litz structure is effective in reducing AC resistance in an appropriate operating frequency range by reducing the skin and proximity effects on the planar conductor. Experimental prototypes were also constructed. The measured results show that the reduction of AC resistance by using litz winding instead of solid conductor could be as high as 30%. Thus, the planar litz structure is very promising for applications in planar integrated magnetic component design.

Chapter 5. Planar Boost Inductor Design

5.1 Introduction

An integrated approach has been developed recently to realize power electronics components in the form of Active and Passive Integrated Power Electronics Modules (IPEMs) [5.1]. The active IPEM integrates power MOSFETs, gate drivers, protection circuits, sensors and possibly some level of control. Similarly, the passive IPEM represents the electromagnetic integration of the DC blocking capacitor, transformer and output inductors. Planar magnetic technology is utilized for the realization of high-density power passive modules [5.2]. In a power factor correction (PFC) circuit, a boost inductor is traditionally implemented by using toroid core and round wires. In order to achieve low profile and good cooling, especially facilitate the integration of input inductors for future passive IPEMs, a planar boost inductor is going to be fabricated for this application.

The design of a planar boost inductor for application in a PFC circuit operating under continuous conduction mode (CCM) is described in this chapter. Some of the important issues, like core material selection, winding configuration, loss estimation, winding parasitic capacitance and thermal modeling are discussed in detail. Finite Element Analysis (FEA) simulation is used to predict high frequency winding losses. Core losses are calculated using a modified version of Steinmetz equation, which is applicable for non-sinusoidal voltage waveforms. Two complete designs under different criteria (volume optimization and parasitic capacitance minimization) are provided. An experimental prototype is constructed in CPES packaging lab and tested on a real circuit. By comparing the performance of the planar inductor with that of the conventional toroid

one, we can find that the planar inductor could outperform the conventional one either in volume or parasitics.

5.2   Design Specifications

An ideal single phase single switch CCM PFC circuit is shown in Fig. 30. The inductor design specifications for this boost power converter are listed in Table 3.
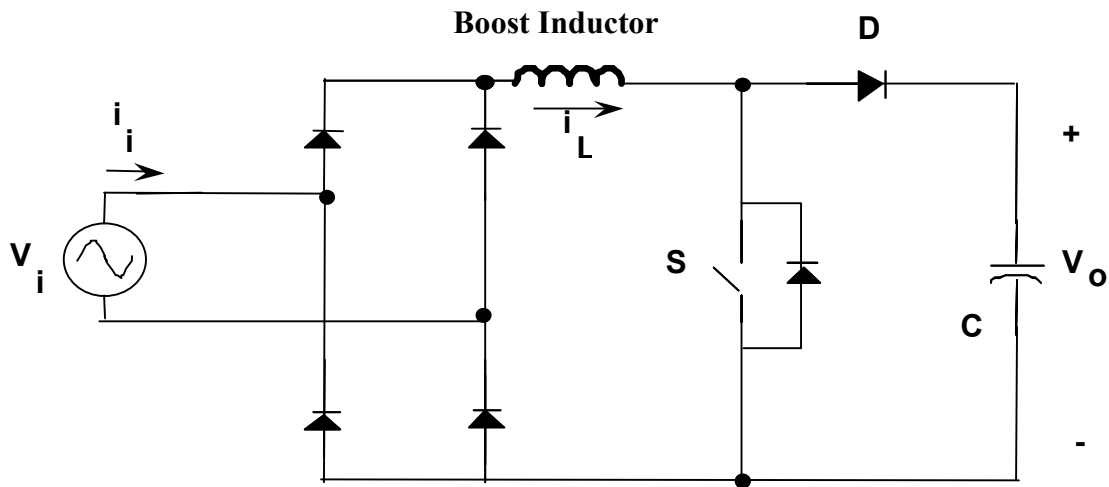
Fig. 30. Single phase single switch CCM PFC circuit.

Table 3.   Design specifications.

Parameters	Values
Input Voltage Range	176 V ~ 264 V
Output Voltage	400 V
System Output Power	1000 W
DC/DC Efficiency	92 %
System Efficiency	90 %
Switching Frequency	400 kHz
Peak Input Current	10.3 A
RMS Input Current	6.3 A
Ripple Current (Peak to Peak)	2.68 A
Inductance	96 uH

5.3   Design Procedure

5.3.1   Core Selection

Selecting the most effective material, shape and size of the core used in PFC boost converter can be complicated, since a wide variety of materials, geometries and sizes are available from many magnetic core manufacturers, like Magnetics, Armco, Arnold, Micrometals, and Ferroxcube. Different materials are optimal at different frequency ranges, operating temperature, and flux densities. Selection is largely dependent on the applications. For instance, some low-loss core materials are preferred if loss is the most important concern, even though they are expensive. A core with a high saturation flux density and low specific core loss is suitable for this application, from the standpoints of the volume and efficiency. Table 4 lists the properties of some core materials.

Table 4.   Properties of some core materials.

Material Type	Saturation Flux Density (Teslas)	Specific Core Loss @ 100 kHz (W/m^3, $B_m = 0.04$ T)
Silicon Steel	1.9-2.2	1.94×10^6
Supermendur	1.9-2.2	5.21×10^5
Magnesil	1.5-1.8	1.65×10^5
Amorphous B	1.5-1.6	1.95×10^5
Square Orthonol	1.4-1.6	1.71×10^5
48 Alloy	1.15-1.4	3.06×10^5
Powder	1.05	1.33×10^5
MPP (Powder)	0.75	5.30×10^4
Permalloy 80	0.66-0.82	3.21×10^4
Supermalloy	0.65-0.82	2.59×10^4
3B7	0.45-0.5	1.49×10^4
3E2A	0.45-0.5	1.34×10^4
3C8	0.45-0.5	2.96×10^4
Ferrite	0.35-0.5	6.51×10^3

It can be observed from Table 4 that metals have relatively high saturation flux density but also high specific core loss, which makes them impractical at high operating frequencies; ferrites do provide low core losses at high frequencies, while they have low saturation levels, therefore, for a given flux density, a larger core cross-section is needed; powder cores are in-between. So for the application frequency of 400 kHz, ferrites become more useful and practical. 3F3 from Ferroxcube is optimized for use at this frequency range.

5.3.2   Winding Configurations

5.3.2.1   Planar Inductor Winding Structures

A brief overview of planar inductors in MEMS applications will be helpful for the winding design of the planar PFC boost inductor. Basically, three types of planar inductors have been realized on silicon wafers using micromachining techniques [5.3]:
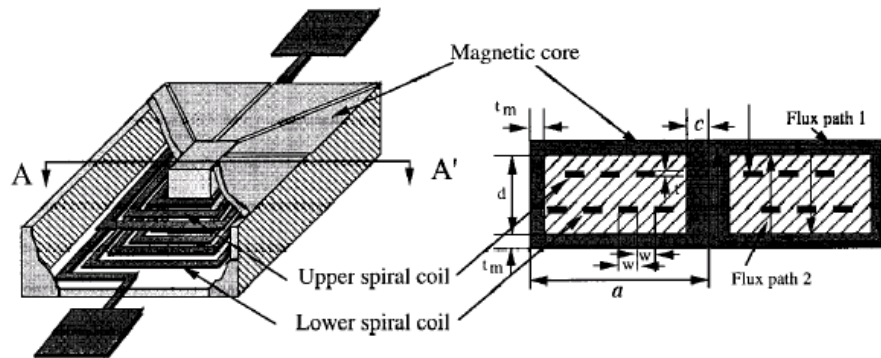
I.   Spiral-Type Inductor

Fig. 31. Spiral-type inductor.

The spiral conductor lines are completely encapsulated with an electroplated thick nickel-iron permalloy, thus achieving the closed magnetic circuits.

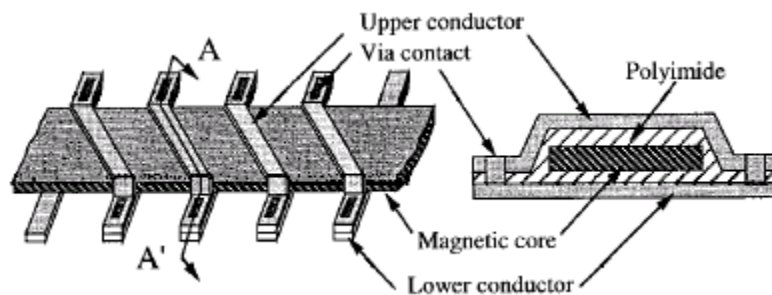II.   Solenoid-Type Inductor

Fig. 32. Solenoid-type inductor.

50

The geometry can be thought of as a planar version of the conventional toroidal inductor. The interconnected metal coils are wrapped around a magnetic core bar.

III.   *Toroidal-Meander-Type Inductor*
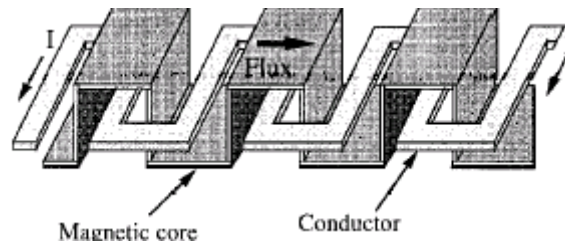
Fig. 33. Toroidal-meander-type inductor.

A toroidal-meander-type inductor is realized by interchanging the roles of the conductor wire and magnetic core in the solenoid inductor. The meander conductor lines are located on a simple plane and the meander magnetic cores are on the multilevels.

5.3.2.2 *Winding Configurations for the PFC Boost Inductor*

For the PFC boost inductor, both spiral-type and solenoid-type winding structures can be applied. Fig. 34 shows some spiral-type winding configurations within a pair of planar E cores for a given number of turns. A single layer winding (a) can reduce capacitive coupling by eliminating interlayer capacitance, while at the cost of having a larger footprint. Multiple layer windings (b and c) must include interconnections between layers. The staggered-winding configuration (c) can reduce the interlayer capacitance effectively.

(a)

(b)

(c)

Fig. 34. Spiral-type winding configurations: (a) Single layer (b) Two layers (c) Three layers.

Fig. 35 illustrates some solenoid-type winding configurations, which have the advantage of relatively low winding capacitance, but have larger volume and are more difficult to manufacture than spiral winding structures.
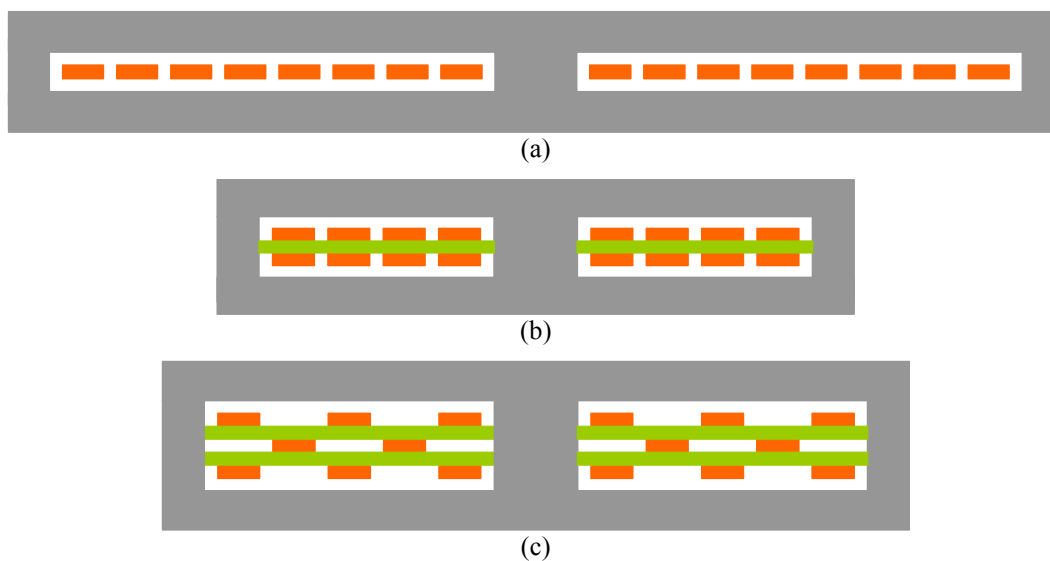

(a)

(b)
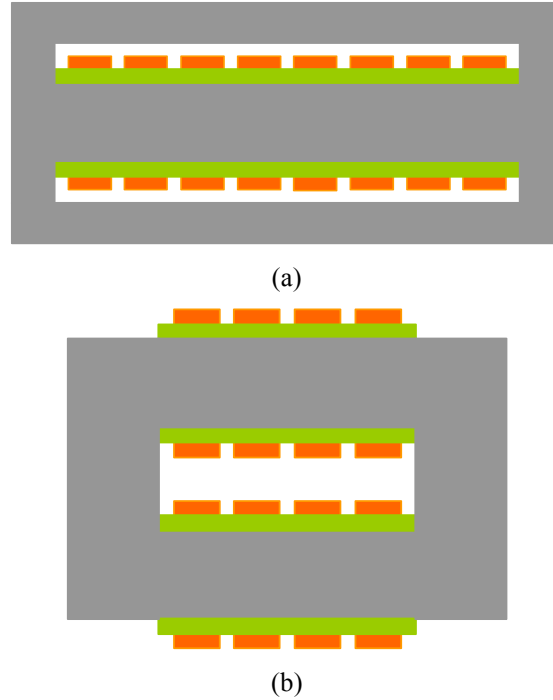
Fig. 35. Solenoid-type winding configurations: (a) Single layer (b) Two layers.

5.3.3 Loss Estimation

The total power losses mainly consist of two parts: core losses and winding losses. Core losses can be calculated by using Modified Steinmetz Equation (MSE), which accounts for remagnetization losses caused by applying non-sinusoidal waveforms. Winding high-frequency conduction losses can be estimated by taking advantage of FE simulations.

Based on the physical understanding that core loss depends on dB/dt, [5.4] develops MSE, which is given by

$$\overline{P_v} = k \cdot f_{eq}^{\alpha-1} (\Delta B / 2)^{\beta} \cdot f_r, \tag{60}$$

where $\overline{P_v}$ is the time-average power loss per unit volume, k, α, β are constants provided by the manufacturer or could be calculated from the curves of specific core loss, ΔB is

52

the peak-to-peak flux density, f_r is the repetition frequency, and f_{eq} is an "equivalent frequency" defined as

$$f_{eq} = \frac{2}{\Delta B^2 \pi^2} \int_0^T (\frac{dB}{dt})^2 dt \tag{61}$$

where $T = 1/f_r$ is the period of the flux waveform.
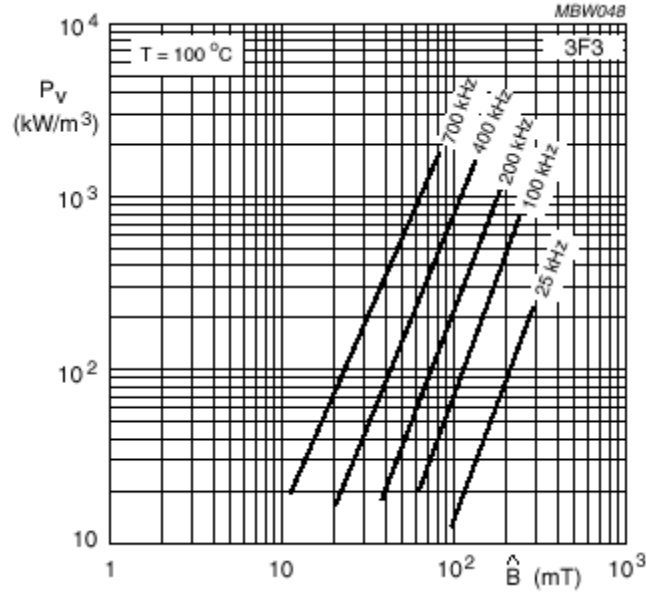
Fig. 36. Specific core loss as a function of peak flux density with frequency as a parameter.

Fig. 36 depicts the typical loss curves for 3F3 ferrite material as supplied by the manufacturer. Using curve fitting, the constants k, α, β in MSE can be determined as follows:

$$\begin{aligned} k &= 5.612 \times 10^{-4} \\ \alpha &= 2.1 \\ \beta &= 2.563 \end{aligned} \tag{62}$$

The ac flux density $\hat{B}$ is related to the ripple current i by

$$\hat{B} = \frac{L \cdot i}{N \cdot A_e} \tag{63}$$

where A_e is the effective core cross-sectional area, N is the total number of turns. So

$$\Delta B = \frac{L \cdot \Delta i}{N \cdot A_e}, \text{ and} \tag{64}$$

$$\frac{dB}{dt} = \frac{L}{N \cdot A_e} \frac{di}{dt} \qquad (65)$$

where Δi is the peak-to-peak ripple current.

For our specific application, the ripple current is a triangle waveform during each subinterval T, and the duty cycle of the PFC circuit is equal to 0.5, so the slope is a constant,

$$\frac{di}{dt} = \frac{\Delta i}{T/2} = 2\Delta i \cdot f_r \qquad (66)$$

By substituting (61) ~ (66) into (60), the power loss per unit volume is

$$\overline{P}_v = 4.2 \times 10^4 \ W/m^3 \qquad (67)$$

Due to the effect of the air gap, the calculation of the high frequency conduction losses in the windings is very complicated. Therefore, an FE simulation based approach can be adopted to estimate the winding losses. In Maxwell 2D field simulator, the winding is modeled as a structure with infinite length in the z-direction. The equivalent winding resistances (Ω/m) at low frequency (60 Hz) and high frequency (400 kHz) can be obtained by FEA methods.

5.3.4   Thermal Modeling

Thermal management becomes an integral part of the design algorithm. [5.5] proposed a one-dimensional thermal model for planar integrated reactive modules. Using the thermal conductivity, thickness and volumetric heat generation as the input with the given boundary conditions and number of layers, the software can compute 1D temperature distribution in the modules. However, the model results in an overestimate of the maximum temperature rise in the modules because it assumes that heat is only dissipated in one direction. Maxwell 2D thermal solver is a more accurate tool, since it considers both horizontal and vertical heat propagation. In the meantime, the computing time is within an acceptable level.

The power losses in the winding and the core must be calculated before using the 2D thermal solver, since they act as two heat sources. Section 5.3.3 describes the procedure to estimate the losses. To simplify the model, the equivalent heat transfer coefficients can be defined on the surfaces of the inductor.

For a certain PFC IPEM system, it is supposed that a planar boost inductor with the dimension of $40mm \times 40mm \times 12mm$ be put between the active IPEM and rectifier on a heat sink as shown in Fig. 37. The heat sink, which is designed for cooling the whole system, has the average convection coefficient h_s equal to 20 $W/m^2 \cdot C$. For the purpose of simplification, we can assume that the inductor be cooled separately by an effective heat sink area of $57mm \times 55mm$, with introducing little error to the result. The detailed dimensions are shown in Fig. 38. Furthermore, we can introduce an equivalent convection coefficient h_{bottom} on the bottom surface of the inductor, to avoid having a complex heat sink in the simulation. The value of h_{bottom} for the designed inductor can be calculated through

$$h_s \cdot A_s = h_{bottom} \cdot A_{bottom}, \tag{68}$$

where A_s is the overall exposed surface area of the heat sink, and A_{bottom} is the bottom surface area of the planar core attached to the heat sink. They can be easily obtained for a certain designed structure. Here, the equivalent convection coefficient h_{bottom} can be derived as

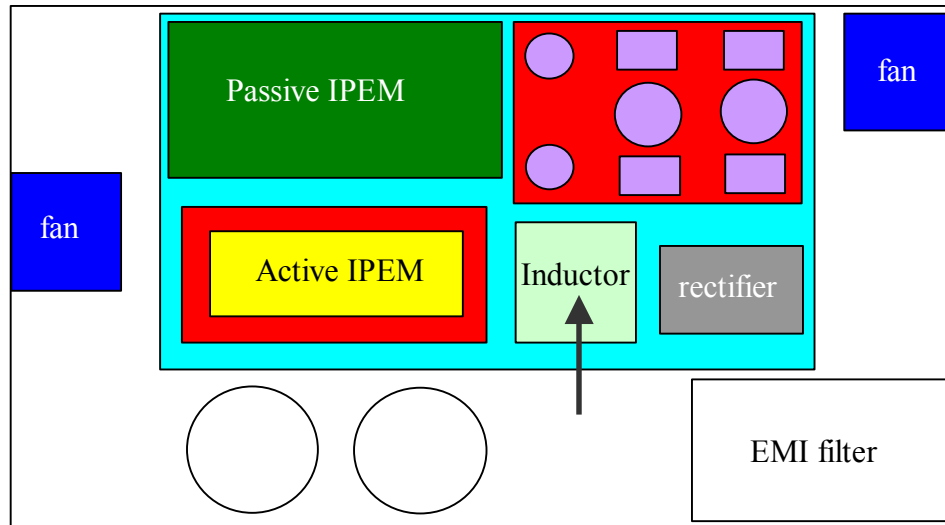$$h_{bottom} = 275 \ W/m^2 \cdot C. \tag{69}$$

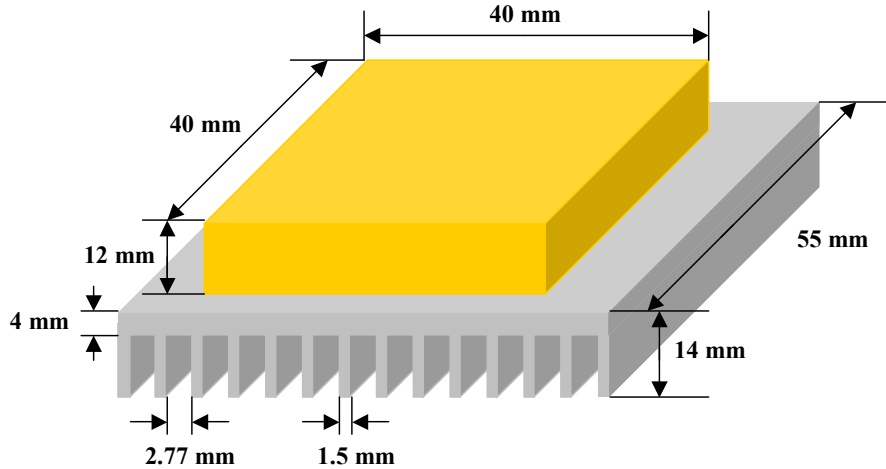Fig. 37. Layout of the whole circuit.

Fig. 38. An isolated model for calculation.

In addition, the radiation effect is also considered on the exposed surfaces of the core. Since the core is a gray object, the radiation emissivity is set to be 0.85 (1 for white objects, and 0 for black objects). All of the heat transfer coefficients of the model shown in 38 are listed in Table 5.

Table 5.   Boundary conditions in a 2D thermal model.

	Top	Bottom	Left	Right
Convection Coefficient h (W / m² · C)	20	275	2	2
Radiation Emissivity E (0 ~ 1)	0.85	0	0.85	0.85
Reference Temperature T (°C)	50	50	50	50

5.3.5   Criterion I: Volume Optimization

For the given specifications listed in Table 3, a volume-optimal design example is described in this section. A pair of air-gapped ferrite EI cores and multiple layer winding configurations are adopted in the design. As a thermal constraint, a maximal temperature rise of 50° must be also satisfied. There is no closed-form equation to estimate the temperature rise in the planar inductor, so that the FEA simulation program discussed in 5.3.4 has to be involved in an iterated procedure. Therefore, the optimization becomes more complicated and time-consuming, due to the manual adjustment of the model and input data. Since the complexity of the problem is dependent on the number of the variables, efforts must be made to reduce them.

Step I. Find a volume function

Fig. 39 demonstrates 2D and 3D views of the planar inductor. The descriptions of the symbols are summarized in Table 6. To reduce the low-frequency winding resistance, 4oz copper substrate is chosen, so that t_1 is equal to $0.15\,mm$. Moreover, the trace spacing and the thickness of the insulator layer are predetermined as: $s = 0.5mm$ and $t_2 = 0.15mm$. Although there are many unknown variables, they are not all independent of each other. The volume V should be expressed as a function of some independent variables.

Table 6. Description of symbols.

| Symbol	Description
L	Inductance
N	Total number of turns
N_{lyrs}	Total number of layers
I_{pk}	Peak input current
B_m	Peak flux density
A_e	Core cross sectional area
a	Window height
b	Window width
c	Core width
d	Core length
w_c	Width of the copper trace
s	Trace spacing
t_1	Thickness of the copper trace
t_2	Thickness of the insulator layer
w	Total width
h	Total height
l_c	Total length
V	Total volume
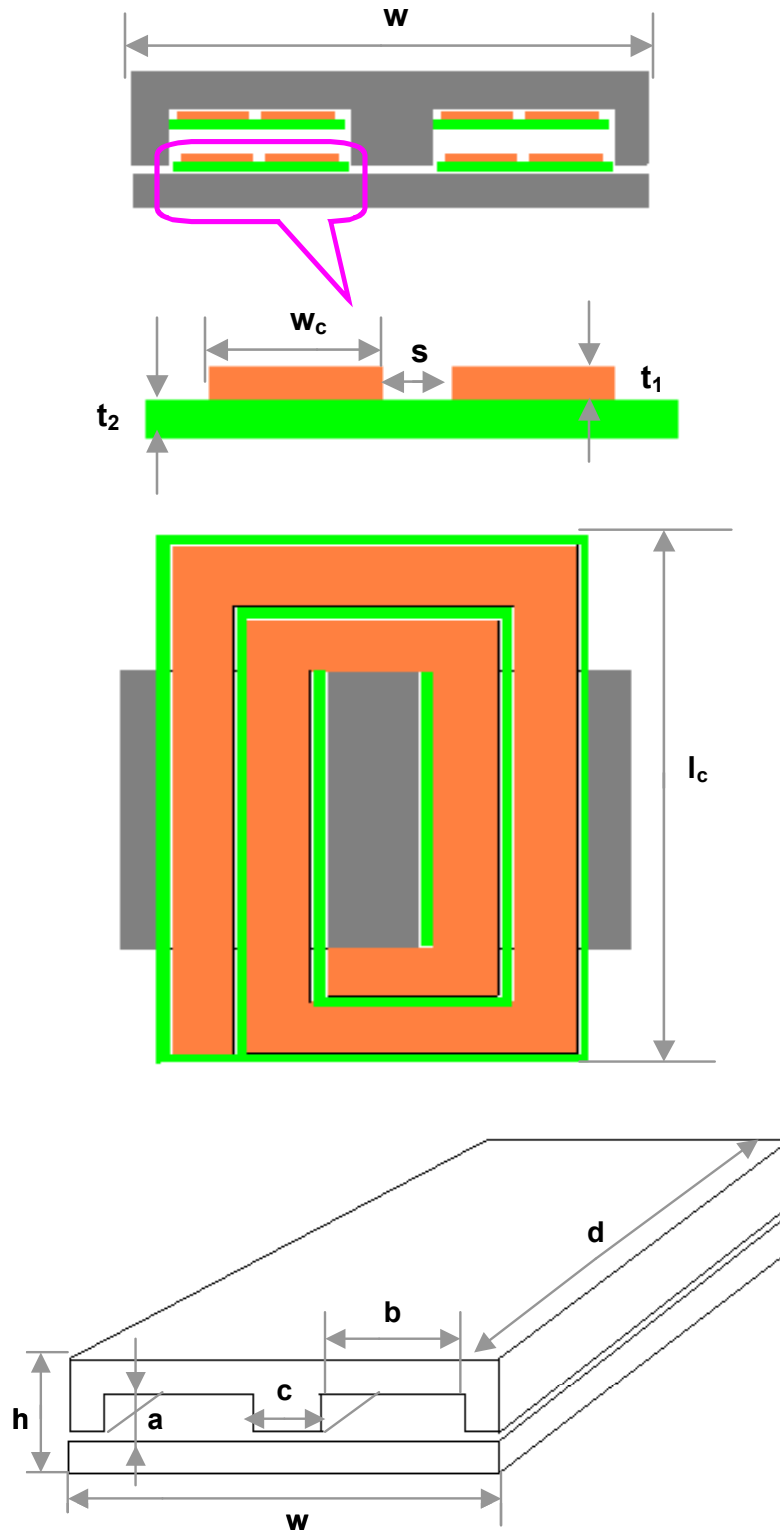
Fig. 39. 2D and 3D views of the planar inductor.

The expression of V can be derived as follows:

1. The core cross sectional area is

$$A_e = c \cdot d = \frac{L \cdot I_{pk}}{B_m \cdot N} \tag{70}$$

2. The window width is

$$b = w_c \cdot \left[ceil\left(\frac{N}{N_{lyrs}} \right) \right] + s \cdot \left[ceil\left(\frac{N}{N_{lyrs}} \right) + 1 \right] \tag{71}$$

Where ceil (x) represents a minimal integer which is larger than x.

3. The window height is

$$a = (t_1 + t_2) \cdot N_{lyrs} \tag{72}$$

4. The total length is

$$l_c = d + 2 \cdot b \tag{73}$$

5. The total width is

$$w = 2 \cdot (b + c) \tag{74}$$

6. The total height is

$$h = a + c \tag{75}$$

7. The total volume is

$$V = w \cdot l_c \cdot h \tag{76}$$

By substituting (70) ~ (75) into (76), V can be rewritten as

$$V = 2 \cdot \left\{ w_c \cdot \left[ceil\left(\frac{N}{N_{lyrs}} \right) \right] + s \cdot \left[ceil\left(\frac{N}{N_{lyrs}} \right) + 1 \right] + \frac{L \cdot I_{pk}}{B_m \cdot N \cdot d} \right\} \cdot$$

$$\left\{ d + 2w_c \cdot \left[ceil\left(\frac{N}{N_{lyrs}} \right) \right] + 2s \cdot \left[ceil\left(\frac{N}{N_{lyrs}} \right) + 1 \right] \right\} \cdot \left[(t_1 + t_2) \cdot N_{lyrs} + \frac{L \cdot I_{pk}}{B_m \cdot N \cdot d} \right] \tag{77}$$

It can be seen clearly that V is a function of N, N_{lyrs}, w_c and d, which are four independent variables.

Step II. Determine some variables

To reduce the complexity of the simulation, we try to determine some of the variables in the V function.

From (77), the volume V is a function of four independent variables, N, N_{lyrs}, w_c and d. To investigate the impact of each variable, we can fix the others. Obviously, the reduction of w_c is an effective way to reduce V. However, volume reduction is also limited by power losses and thermal constraints. The number of PCB layers N_{lyrs}, is usually some even number, like 4, 6, or 8. It is not economically feasible when $N_{lyrs} \geq 10$. Fig. 40 plots V as a function of N and d, assuming $N_{lyrs} = 8$ and $w_c = 3mm$. It can be seen that V decreases monolithically as d increases. Due to the space limitation, d cannot be larger than 40 mm. Therefore, for a volume optimal design, d is chosen to be its largest possible value, 40 mm.
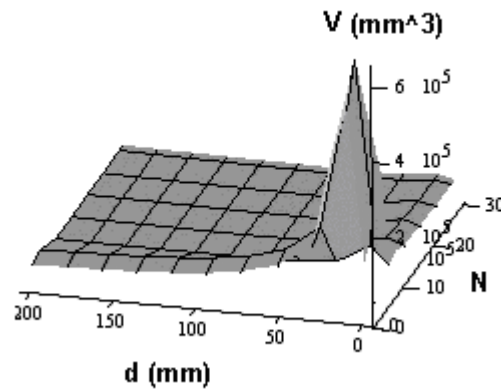

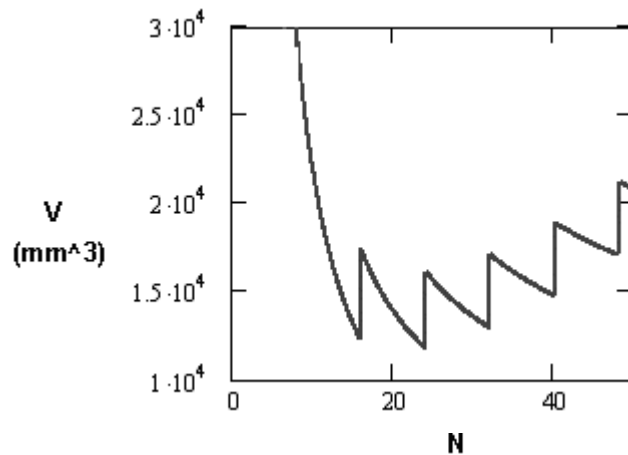Fig. 40. V as a function of N and d, for $N_{lyrs} = 8$ and $w_c = 3mm$.

Fig. 41. V as a function of N, for $N_{lyrs} = 8$, $w_c = 3mm$ and $d = 40mm$.

Fig. 41 plots V as a function of N, for $d = 40mm$, $N_{lyrs} = 8$ and $w_c = 3mm$. This indicates that a minimal V can be obtained when $N = 24$, while V increases only slightly when $N = 16$ or 32. For the given cross sectional area of the copper trace and core length, the winding losses are approximately proportional to the number of turns. As N becomes larger, the winding losses increase, but the core losses decrease. By doing rough calculation, we find that the winding losses are dominant, usually in the range of ten times the core losses. Therefore, the higher the number of turns, the larger the total losses. We should choose the smallest possible value of N for minimizing the total power losses. Here, $N = 16$ is the choice for the best inductor design.
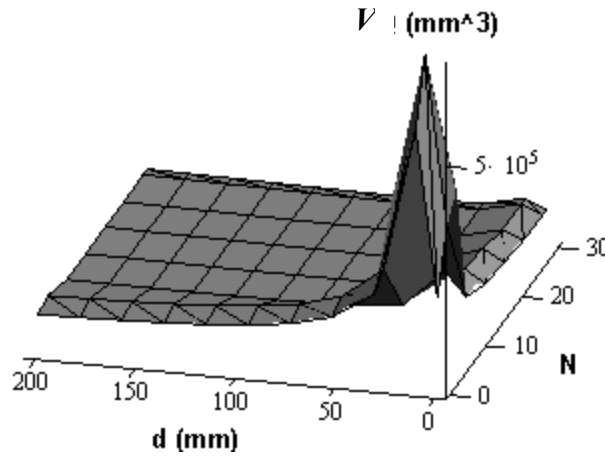

Fig. 42. V as a function of N and d, for $N_{lyrs} = 6$ and $w_c = 3mm$.

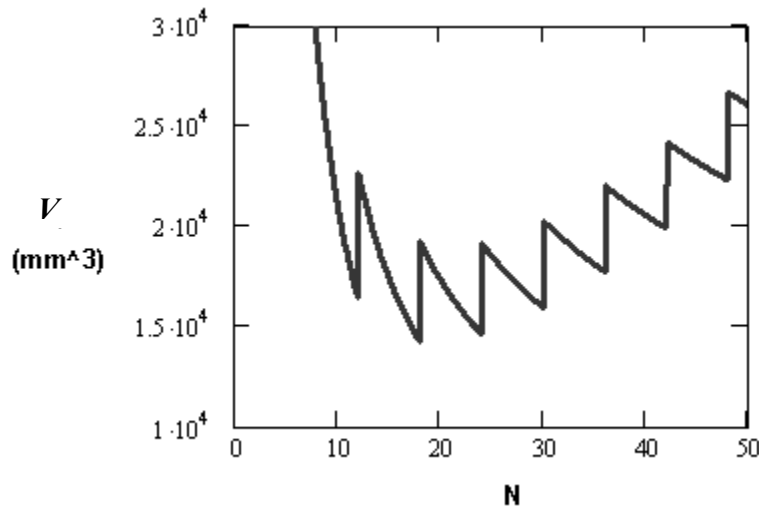Fig. 43. V as a function of N, for $N_{lyrs} = 6$, $w_c = 3mm$ and $d = 40mm$.

Next, it is assumed that $N_{lyrs} = 6$, $w_c = 3mm$, V is plotted as a function of N and d in Fig. 42. Similarly, V decreases as the increase of d. So d is still chosen to be 40 mm. Fig. 43 demonstrates V as a function of N, for $d = 40mm$, $N_{lyrs} = 6$ and $w_c = 3mm$. Clearly, it can be seen that a minimal V can be achieved when $N = 18$ or 24. However, this volume is larger than that in the previous case. Fig. 44 shows a bunch of curves of V as a function of d, for $w_c = 3mm$. The labels beside the lines represent N / N_{lyrs}. Apparently, the best choice of N_{lyrs} is 8.

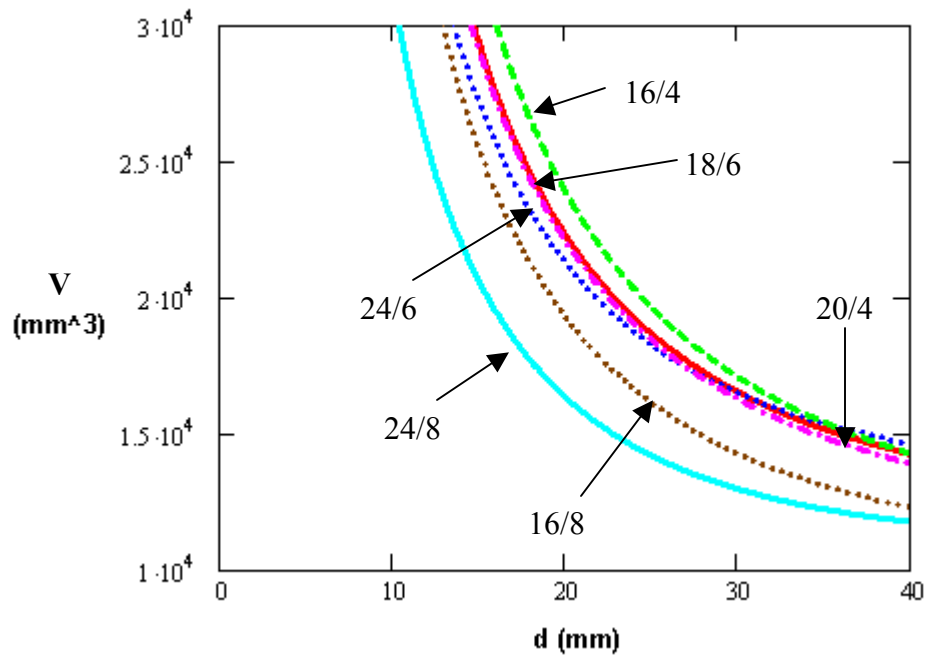Fig. 44. V as a function of d for $w_c = 3mm$.

Based on the above analysis, some variables can be determined in this step as

$$d = 40mm \tag{78}$$

$$N_{lyrs} = 8 \tag{79}$$

$$N = 16 \tag{80}$$

Step III. Determine w_c

This is the most complicated step during the design, due to the involvement of FEA programs. The design flow chart is shown in Fig. 45.
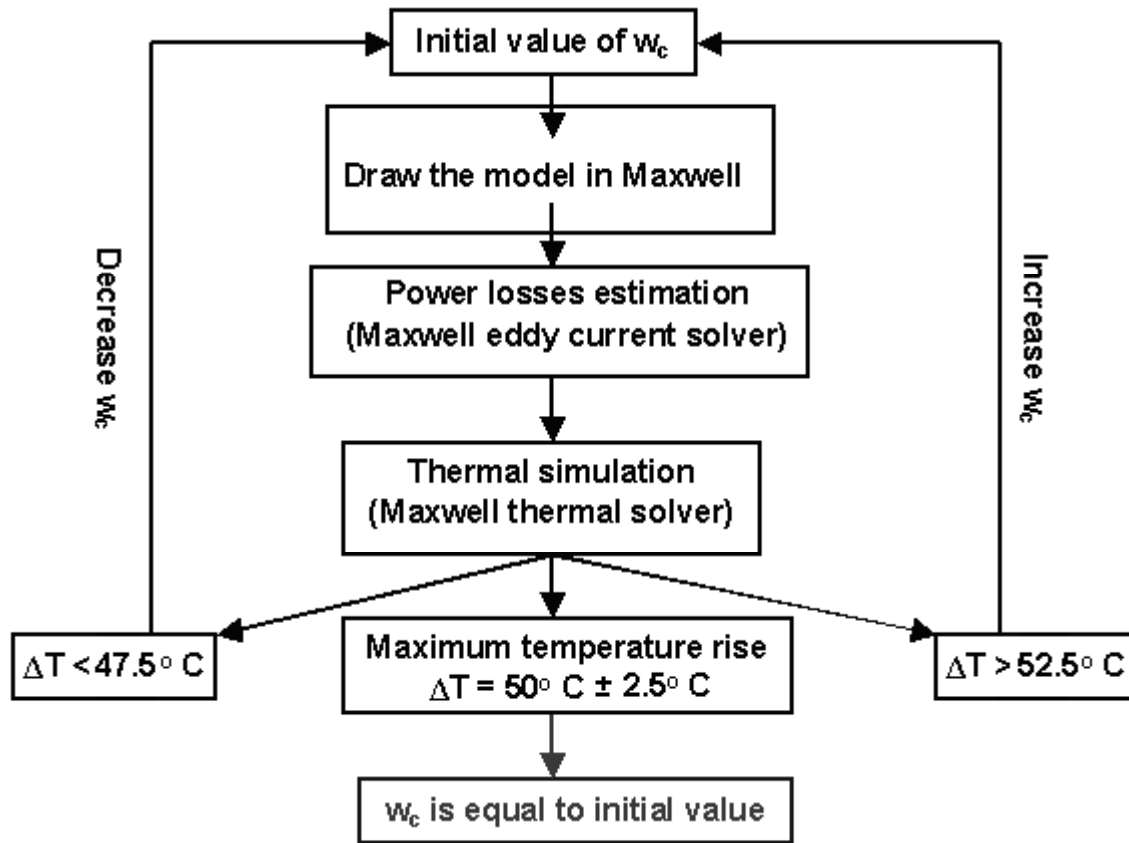
Fig. 45. Design flow chart.

As a start, we can choose an initial value of w_c arbitrarily. Then all the parameters for the model are determined, and the model is drawn in Maxwell. Core losses can be calculated by using MSE. Winding losses can be obtained in eddy current solver. These power losses will be used as input data in Maxwell thermal solver. Finally, a maximum temperature rise ΔT can be output from the post processing. If $\Delta T = 50°C \pm 2.5°C$, the design is complete. If $\Delta T < 47.5°C$, the initial value of w_c can be reduced further, and then the same procedure is repeated again. If $\Delta T > 52.5°C$, an overdesign occurs. So a smaller w_c should be used as an initial value in the next cycle. Therefore, the initial guess of w_c is critical in this iterated procedure. The more accurate the initial guess of w_c, the less the amount of iterations. In each iteration, both the model and the power losses need to be updated manually.

By doing this, a minimal w_c that can meet the thermal requirement is determined as

$$w_c = 1.8mm \tag{81}$$

Step IV. Summarize the design

Customized EI cores are needed for this design, as shown in Fig. 46. 8-layer PCB can be used to implement the windings. Fig. 47 illustrates the cross sectional view of the whole structure. Some important parameters are summarized in Table 7.
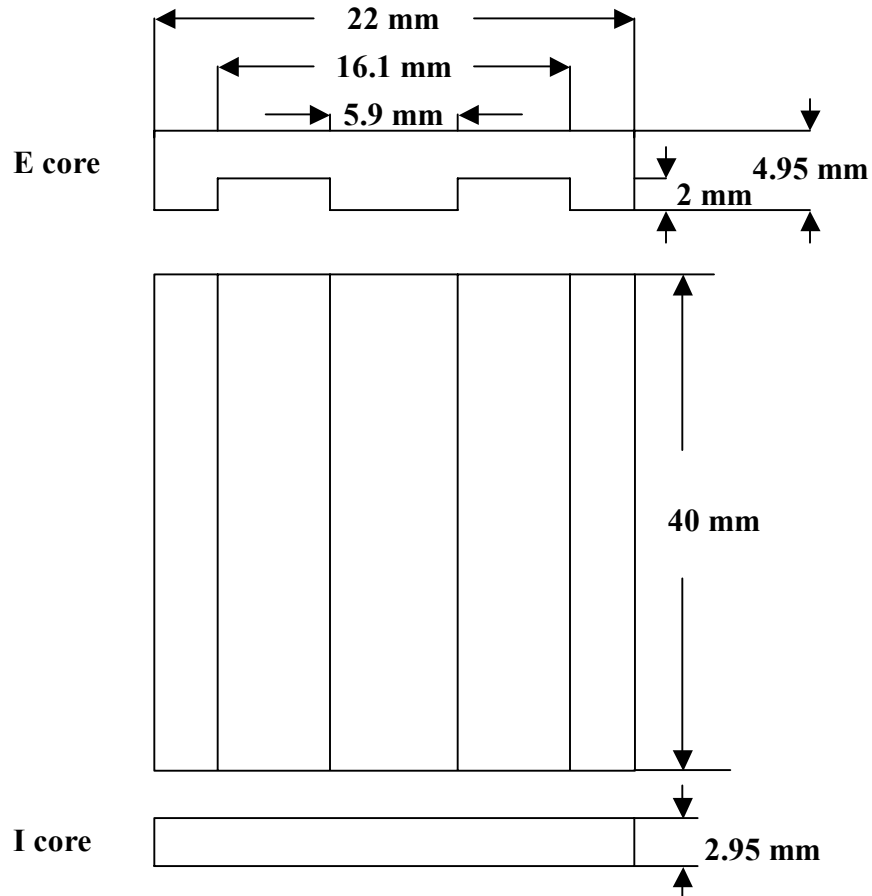

Fig. 46. Customized core design.

Fig. 47. Cross sectional view of the whole structure.

Table 7.   Parameters in the design.

Parameters	Values
Width of Copper Trace	1.8 mm
Thickness of Copper Trace	0.15 mm
Trace Spacing	0.5 mm
Thickness of Insulator	0.15 mm
Number of Turns	16
Number of Layers	8
Air Gap Length	0.4 mm (per leg)
Total Width	22 mm
Total Length	50.2 mm
Total Height	8.3 mm
Total Volume	9167 mm^3
Winding Low-frequency Losses	4.65 W
Winding High-frequency Losses	2.65 W
Core losses	0.5 W
Total losses	7.8 W
Maximum Temperature Rise	50 °C

5.3.6   Criterion II: Parasitic Capacitance Minimization

At frequencies above several megahertz, the response of inductors is very different from their low-frequency response, since the winding parasitic capacitance cannot be ignored. High-frequency behavior of the inductor will affect the electromagnetic interference (EMI) performance of the PFC circuit [5.6].

A boost PFC converter working in continuous current mode (CCM) is shown in Fig. 48. The dashed line represents the differential mode (DM) noise loop, and the dotted line is the common mode (CM) noise loop. The boost inductor L_B will have an impact on the DM noise spectrum since it is involved in the DM noise loop. For simplification, Fig. 49 illustrates the equivalent conductive DM noise loop, where Z_{LB} is the inductor's

impedance, Z_{loop} is the loop impedance, Z_{load} is the load impedance from LISN, and V_s is the equivalent noise voltage source. From basic circuit theory, the noise voltage drop on the LISN is equal to

$$V_{DM} = \frac{Z_{load}}{Z_{load} + Z_{loop} + Z_{LB}} \cdot V_s \tag{82}$$

At high frequencies, Z_{LB} is much larger than Z_{loop}, so the boost inductor will determine the DM noise spectrum.
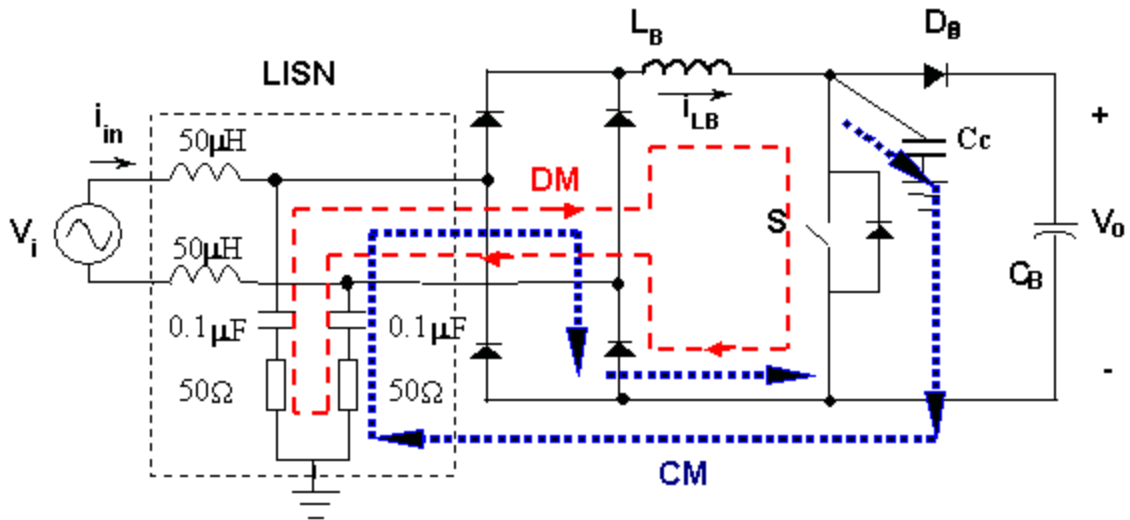
Fig. 48. Boost PFC circuit.
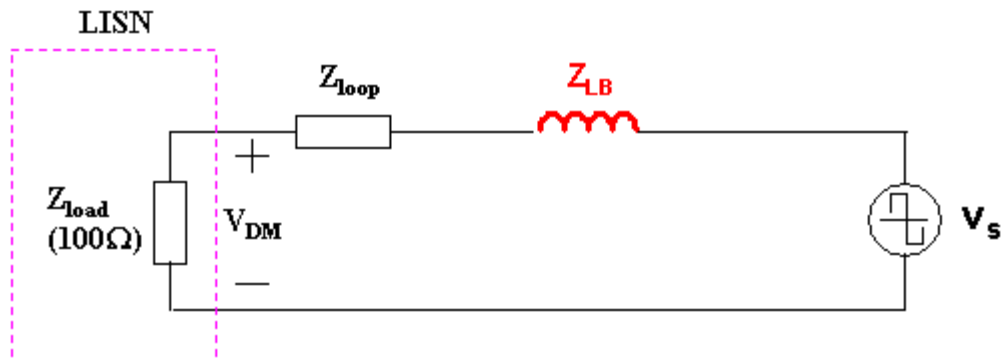
Fig. 49. Equivalent conductive DM noise loop.

Due to the existence of the winding parasitic capacitance, the inductor can act as a capacitor beyond some frequency, known as the resonant frequency. The capacitor will introduce –20dB/dec attenuation, which makes the DM noise performance worse. Therefore, to reduce the DM noise at HF, a careful design of the inductor aiming at minimizing the winding parasitic capacitance is required.

A single layer winding configuration is suitable for the reduction of the winding capacitive coupling, since no interlayer capacitances exist. Therefore, a solenoid-type structure as shown in Fig. 50 is proposed to meet this criterion. The inductor consists of a pair of u-shape ferrite cores, and some parallel-distributed winding conductor lines. If the current $i(t)$ flows in the direction indicated by the arrows, then the magnetic flux $\Phi(t)$ in the core will be anticlockwise. The air gap can be located at the center of the core legs. Predicting the winding capacitances is our next step.
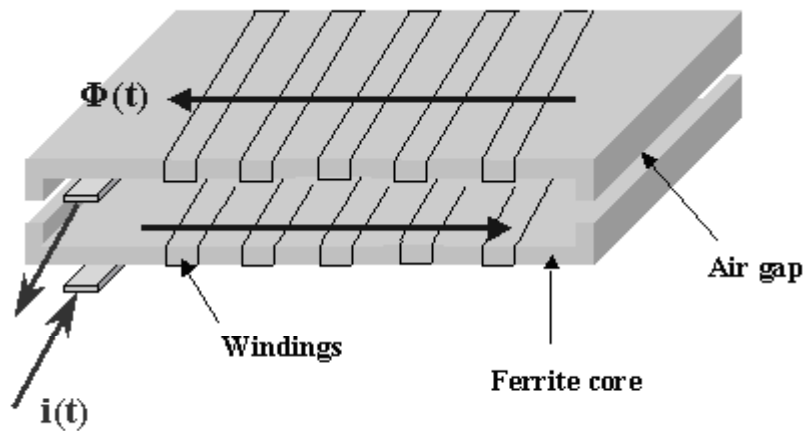
Fig. 50. 3D-view of a solenoid-type inductor.
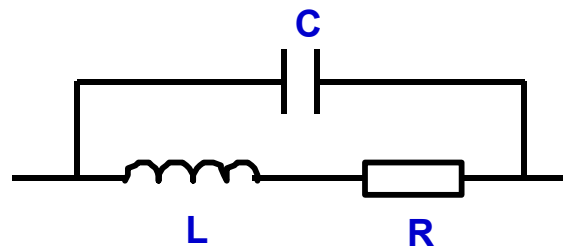
Fig. 51. Equivalent circuit of an inductor.

The inductor windings have a distributed parasitic capacitance, which can be modeled by a lumped capacitance connected between the terminals of the windings, as shown in Fig. 51. The total capacitance C is comprised of the following equivalent capacitive elements:

(1) The turn-to-turn capacitance in one layer C_1;

(2) The turn-to-core capacitance C_2;

(3) The turn-to-turn capacitance between top and bottom parts C_3;

where C_3 can be ignored, since the two parts are separated by the air at a relatively large distance.

The cross-sectional view of the half structure consisting of copper windings, an insulator layer and a ferrite core is shown in Fig. 52. The basic cell related to the turn-to-turn capacitance C_1 is shown in Fig. 53, where w_c represents the width of the copper trace, and s is the trace spacing. Maxwell 2D simulator can be used to predict C_1. Suppose that the thickness of the copper is 0.2 mm, twice the skin depth (at 400 kHz), and $s = 0.5mm$. Then the capacitances per unit (pF/m) corresponding to different w_c are listed in Table 8.
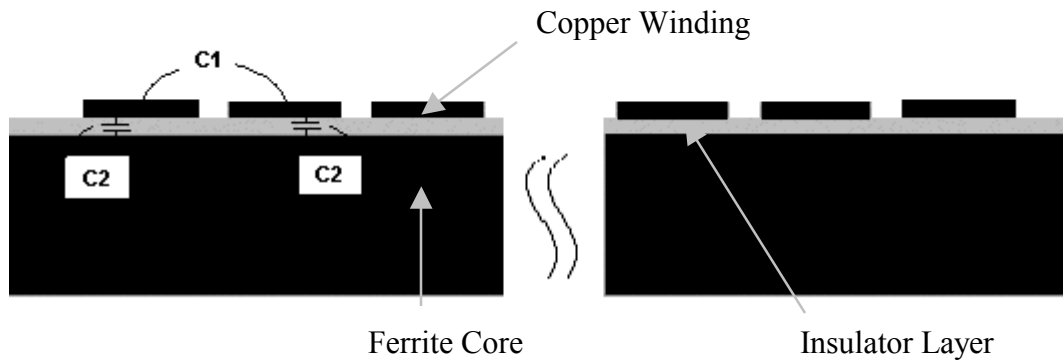
Fig. 52. Cross-sectional view of the half structure.
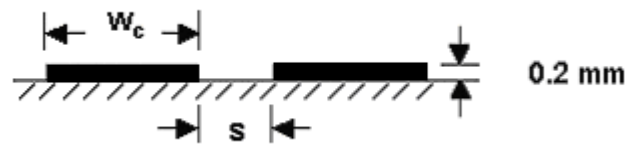
Fig. 53. Basic cell related to C_1.

The basic cell related to the turn-to-core capacitance C_2 is shown in Fig. 54, where t_2 is the thickness of the insulator layer. C_2 can be estimated by the well-known equation:

$$C_2 = \frac{\varepsilon_o \varepsilon_r \cdot w_c}{t_2} \times 10^{12} \ (pF/m),$$ (83)

where ε_o is the permittivity of the air, ε_r is the relative permittivity of the insulator.

Table 8. C_1 corresponding to different w_c.

w_c (mm)	C_1 (pF/m)
1.0	10.7
1.2	11
1.4	11.4
1.5	11.6
1.6	11.7
1.8	12
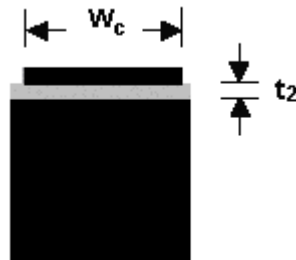
Fig. 54. Basic cell related to C_2.

In view of the high-frequency applications, the reactance of the shunt capacitances between turns is much lower than the impedance of the *RLM* branches, therefore, the inductances and resistances of each turn are neglected, and a capacitor network can be assumed as the equivalent circuit for the calculation of the overall capacitance [5.7]. For the structure shown in Fig. 52, if a conductive core is assumed, then the lumped capacitor network is illustrated in Fig. 55, where A and B represent two terminals of the windings.
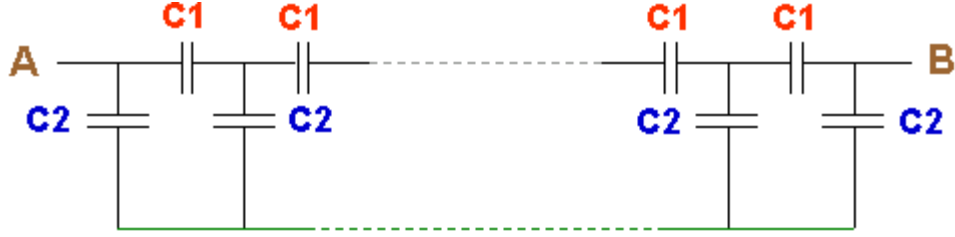
Fig. 55. Lumped capacitor network for the half structure with a conductive core .
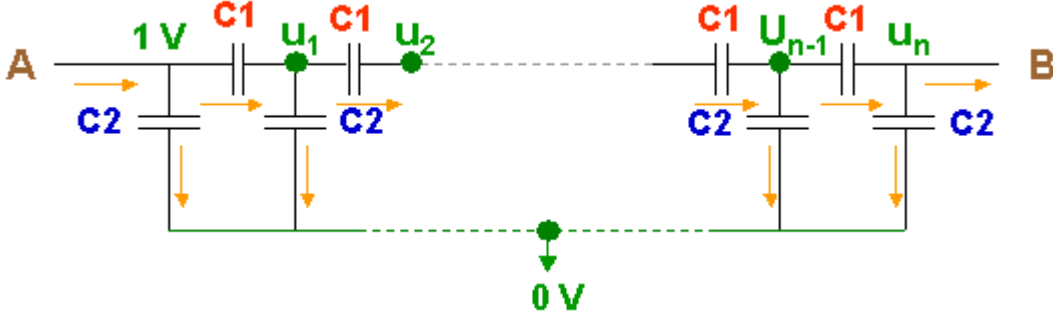
Fig. 56. Lumped capacitor network with the node voltage and reference current.

Now the equivalent capacitance from A to B must be solved. For a coil consisting of $n+1$ number of turns, the voltage at each node and the reference current at each branch are set, as shown in Fig. 56. For the convenience of computation, we assume that the voltage on the core is zero, and the voltage at terminal A is 1V. Based on the rule that the net current at each node is zero, we have the following equations:

$$1+U_1+U_2+\cdots+U_{n-1}+U_n=0$$
$$(1-U_1)\cdot C_1 = U_1\cdot C_2 + (U_1-U_2)\cdot C_1$$
$$\vdots \qquad\qquad\qquad\qquad\qquad\qquad (84)$$
$$(U_{n-2}-U_{n-1})\cdot C_1 = U_{n-1}\cdot C_2 + (U_{n-1}-U_n)\cdot C_1$$

From these n equations, the node voltages of U_1, U_2, ..., U_n are solved. Then the overall equivalent capacitance $C_{AB}(n+1)$ can be obtained by

$$C_{AB}(n+1) = \frac{C_2+(1-U_1)\cdot C_1}{1-U_n} \qquad\qquad (85)$$

For two turns, $n=1$, since $U_1=-1$, the equivalent capacitance is given by

$$C_{AB}(2) = \frac{C_2+2\cdot C_1}{2} = C_1 + \frac{C_2}{2} \qquad\qquad (86)$$

For three turns, $n=2$, by solving the equations of

$$\begin{cases} 1 + U_1 + U_2 = 0 \\ (1 - U_1) \cdot C_1 = U_1 \cdot C_2 + (U_1 - U_2) \cdot C_1 \end{cases}, \tag{87}$$

we have

$$U_1 = 0, \text{ and } U_2 = -1. \tag{88}$$

So the equivalent capacitance is

$$C_{AB}(3) = \frac{C_1 + C_2}{2} \tag{89}$$

For the large number of turns, C_{AB} can be calculated by taking advantage of the math software - MathCAD. When $n > 10$, the capacitance converges to a constant

$$C_{AB}(n) = \frac{C_1 + C_2}{2} \tag{90}$$

Therefore, in order to reduce the total winding parasitic capacitance, we should reduce C_1 and C_2 by

(1) Increasing the spacing between two adjacent copper traces;

(2) Decreasing the width of the copper traces;

(3) Increasing the thickness of the insulator layer;

(4) Using low-permittivity insulator material.

5.4 Experimental Prototype

5.4.1 Prototype Design

To verify the parasitic capacitance model, an experimental prototype needs to be constructed and measured. Considering the tradeoffs among the winding parasitic capacitance, the power losses and the total volume, we provide a complete inductor design. Some important parameters are listed in Table 9. Actually, the core material and shape have been pre-determined for the design. Here, we select common Mn-Zn ferrite material and U-shape core. Since the length of core legs is only few millimeters according to the design, the core needs to be ordered specially. Fig. 57 shows the dimension of the customized core.
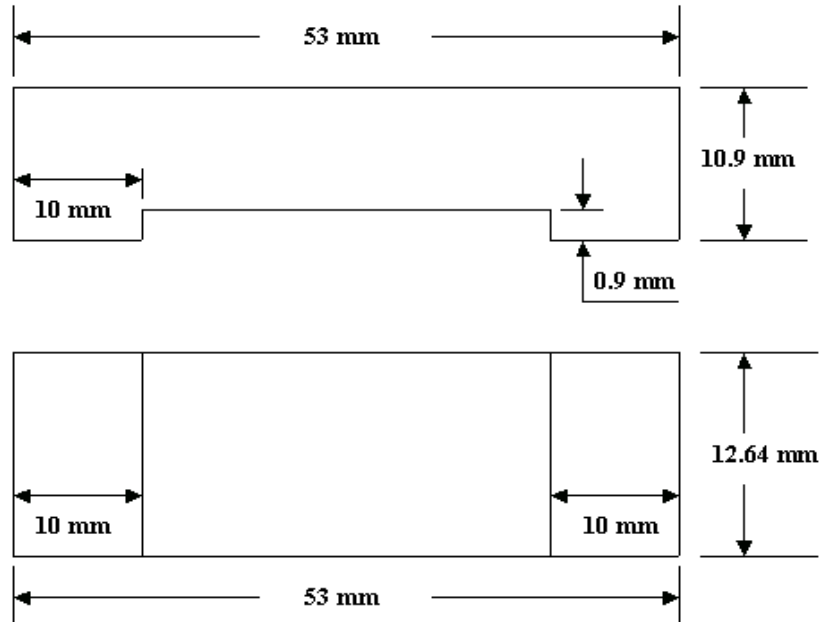
Fig. 57. Customized core design.

Table 9. Parameters in the design.

Parameters	Values
Width of Copper Trace	1.5 mm
Thickness of Copper Trace	0.2 mm
Trace Spacing	0.5 mm
Thickness of Insulator	0.5 mm
Number of Turns	30
Number of Layers	2
Air Gap Length	0.75 mm (per leg)
Total Width	14 mm
Total Length	53 mm
Total Height	22.55 mm
Total Volume	16730 mm^3
Winding Effective Length (per turn)	50 mm
Winding Low-frequency Losses	3.45 W
Core losses	1.2 W
Winding Parasitic Capacitance*	2.3 pF

* For this specific design, the value of parasitic capacitance C_1 can be obtained through Table 8 and the winding length, and the value of C_2 from equation (83), so the winding parasitic capacitance can be calculated as follows:

$$C_1 = 11.6 \times 50 \times 10^{-3} = 0.58 \ pF \tag{91}$$

$$C_2 = \frac{8.86 \times 3 \times 1.5 \times 50 \times 10^{-3}}{0.5} = 4 \ pF \tag{92}$$

$$C_{AB}(30) = \frac{1}{2}(C_1 + C_2) = 2.3 \ pF \tag{93}$$

In the next section, an experimental prototype will be constructed based on these design parameters.

5.4.2 Prototype Fabrication

The steps used in the winding process are described as follows:

Step 1: Design a photoresist mask in AutoCAD, as shown in Fig. 58, and then print it out on a transparency; (The white part in the mask is the desired winding pattern, since negative photoresist is used. The end point of the first copper line (right-hand side) and the start point of the second copper line (left-hand side) are in the same level. The similar situation is also applied for other lines. Therefore, these copper lines can form a closed coil after folding.)
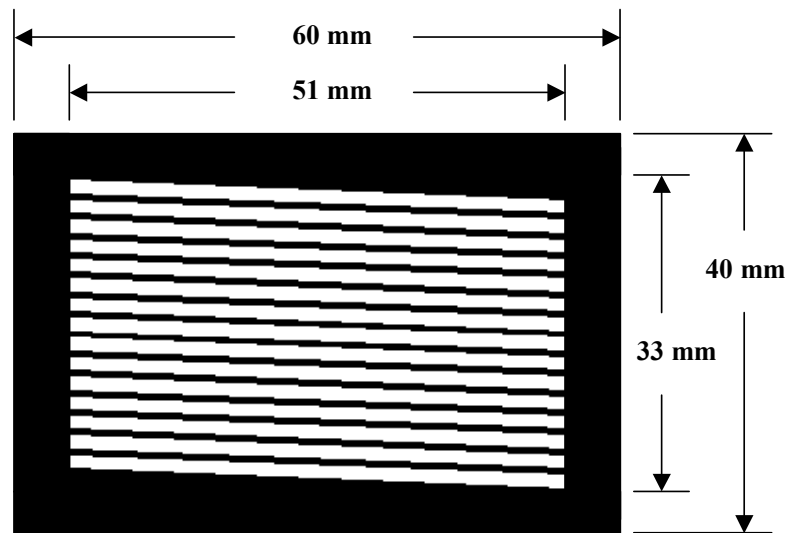
Fig. 58. Photoresist mask for the winding.

(a)
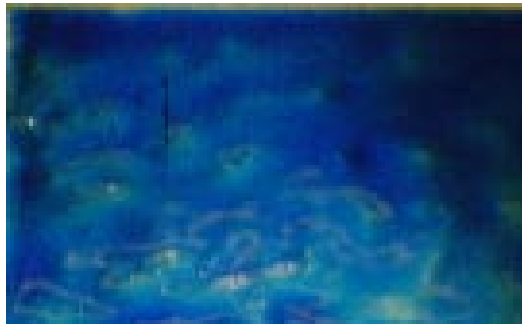
(b)
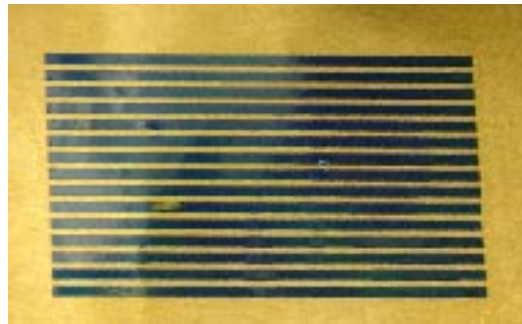
(c)
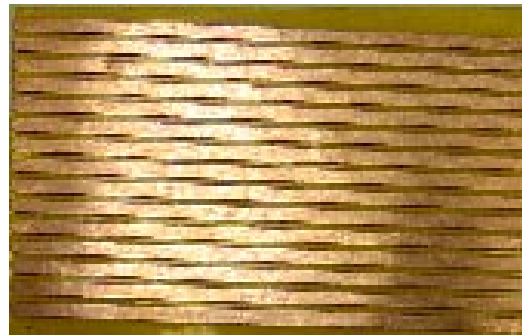
(d)

Fig. 59. Winding process: (a) Step 2; (b) Step 3; (c) Step 5; (4) Step 7.

Step 2: Cut two pieces of $40mm \times 60mm$ copper plates (or, samples) with the thickness of $0.2mm$, and then flatten them, as shown in Fig. 59 (a);

Step 3: Spread evenly a thin layer of negative photoresist on each sample, and then heat them for around 40 minutes, as shown in Fig. 59 (b);

Step 4: Put the masks on the samples, and then expose them under the light;

Step 5: Make a 700 ml mixture of acetone and water with the rate of $1:20$, and then clean the samples with the solution, as shown in Fig. 59 (c);

Step 6: Stick Kapton tape on the other side of the samples as an insulator layer,

Step 7: Etch the exposed copper from the samples, clean them up, and then cut off the insulator on the boundaries, as shown in Fig. 59 (d);

Step 8: Stick the tape on the core, layer by layer, until the total thickness of the insulator is close to $0.5mm$;

Step 9: Make the samples wrap around the cores tightly;

Step 10: Connect the copper lines by soldering.
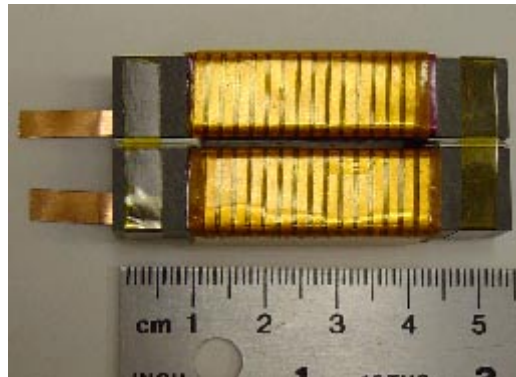
(a)
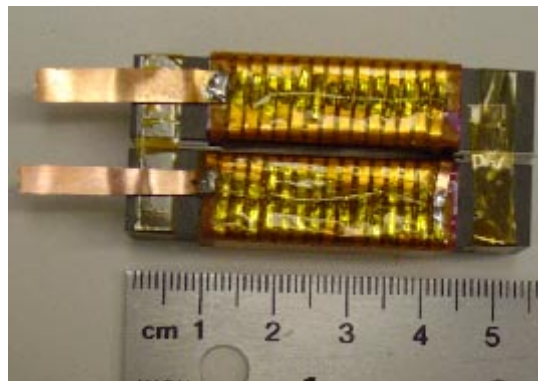
(b)

Fig. 60. 3D view of a complete planar inductor: (a) Front; (b) Back.

3D view of a complete planar inductor is shown in Fig. 60, two pins are extended for the future measurement.

5.4.3   Measured Results

An Agilent 4294A precision impedance analyzer is used to measure the small signal response of the inductor. The impedance curve obtained from this instrument is shown in Fig. 61. Clearly, it can be seen that the self-resonant frequency of the inductor is around 9.1 MHz. From Table 10, we can see that the measured impedance of the inductor is in good agreement with the calculated one.

Table 10. Comparison of the calculated and measured inductor impedances.

Parameters	Calculated Values	Measured Values
Inductance (*uH*)	96	96.8
Capacitance *(pF)*	2.3	3.1
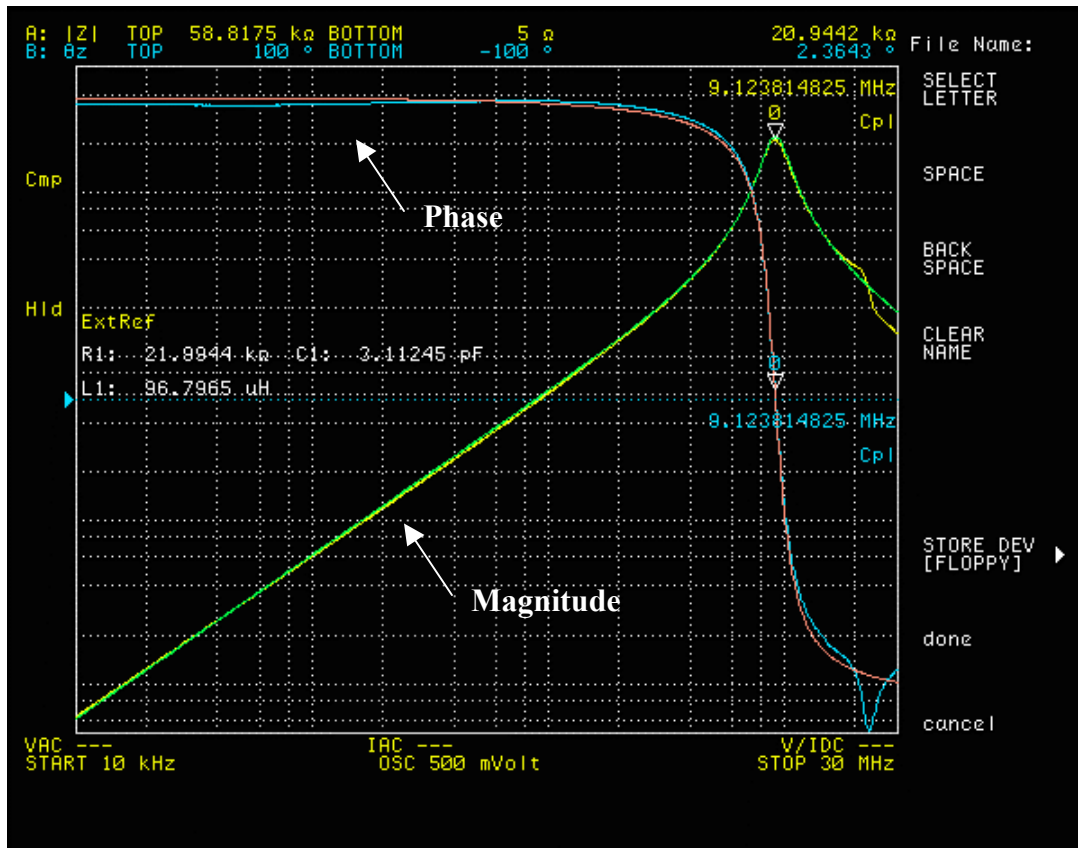
Fig. 61. Impedance curve of the planar inductor.

The measured winding parasitic capacitance is $3.1pF$, which is in the same order as the predicted value of $2.3pF$. This indicates that the capacitance network modeling in 5.3.6 is meaningful. The discrepancy between them may be caused by the fact that the permittivity of the insulator material is actually in the range of $3 \sim 4$, and the actual dimensions are not strictly equal to the designed values.

The thermal performance of the inductor is tested in the real PFC circuit. The maximum temperature rise on the inductor is around $34°C$, located at the center of the inductor.

Traditionally, the boost inductor can be implemented by using powder toroid core, as shown in Fig. 62. For the comparison study, Table 11 lists some parameters of this toroid inductor, designed for the same specifications as the planar one. Also, the impedance curve is plotted in Fig. 63.

Fig. 62. Toroid inductor.

Table 11. Some parameters of the toroid inductor.

Parameters	*Values*
Number of turns	*26*
Total Volume	*13500 mm^3*
Winding Low-frequency Losses	*1.4 W*
Core Losses	*7.1W*
Max. Temperature Rise	*38 °C*
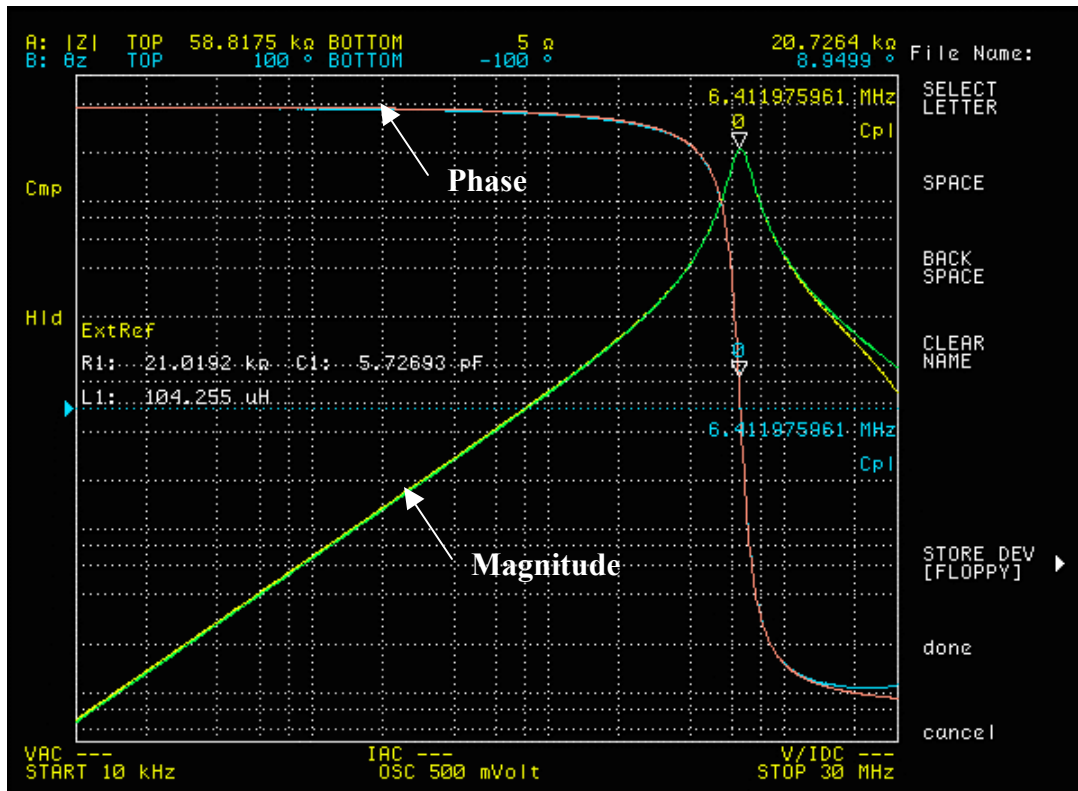
Fig. 63. Impedance curve of the toroid inductor.

From Table 9 and 11, we can find that the planar inductor has much lower core losses than the toroid inductor. That is due to the property of the core materials used in the inductors. Although the winding losses of the planar inductor are higher than those of the toroid one, its overall losses are lower. The toroid inductor has a smaller total volume, while the planar structure can result in a lower profile.

By comparing Fig. 61 and 63, we can observe that the planar inductor has a lower winding parasitic capacitance, or, higher self-resonant frequency than the toroid one. Therefore, the capability of suppressing EMI noise in the circuit will be enhanced by using the planar inductor.

5.5   Conclusions

Optimal planar boost inductor design is not an easy task. The selection of the core material is dependent on the frequency. Ferrite turns out to be a good choice for high-frequency applications due to its relatively low core losses. Winding configurations may influence the parasitic capacitance a lot. FEA simulation is very useful in the losses

estimation and thermal modeling, therefore is usually involved in the design. The target function for the optimization could be volume, losses, parasitics or cost. It has been verified that the planar inductor could have a lower winding parasitic capacitance than the conventional toroid inductor.

Chapter 6. Conclusions and Future Works

6.1 Summary of the Thesis

At high frequencies, the behavior of planar magnetic components becomes more frequency-dependent. Skin and proximity effects cause the winding resistance to increase with the operating frequency, and the parasitic capacitance or inductance can not be neglected either. In this thesis, some important issues related to the modeling and design of planar magnetic components were discussed.

First, an extensive review of planar magnetic techniques was covered in Chapter 1. The characteristics of the planar magnetic components, their applications in power electronics, and some design issues were addressed. In Chapter 2, the loss mechanisms due to the skin and proximity effects on a single foil conductor were discussed. Some closed-form expressions to calculate the HF conduction losses on multiple layer and litz wire windings were derived in 2D models. Then, 2D and 3D FE modeling were described in detail in Chapter 3. The accuracies of the 2D and 3D FEA simulation results were also evaluated against the analytical solutions. In Chapter 4, a planar litz structure was investigated. Some definitions and guidelines were presented and explained as well. A 3D FEA simulation was performed to look into the impacts of some parameters on the litz performance. In addition, an experimental prototype was constructed to verify the planar litz conductor concept. In Chapter 5, a planar boost inductor design was emphasized. All the design aspects, like core selection, winding configurations, losses estimation, and thermal modeling were included. Two complete designs were provided to meet two different criteria: volume optimization and parasitic capacitance minimization. Finally, a solenoid-type planar inductor was implemented for the measurement.

In the thesis, some simplified 2D models were adopted for the calculation efficiency. For instance, the power losses in the inductor windings were estimated in a 2D model. Both simulated and experimental results were sufficiently provided for the parametric studies or verifications. Throughout the study, FEA simulation proves to be a useful approach to predict the electromagnetic and thermal performances of the components in the design.

6.2 Future Research Topics

There are still lots of future work to be done on these discussed topics.

For the planar litz structure, we could actually design a variety of winding patterns, by alternating the strand angle, the number of layers, or the interconnections. The comparison study among these options is very valuable, even though difficult. Moreover, the problems associated with manufacturability are interesting and challenging. The applications of the planar litz structure could also be investigated.
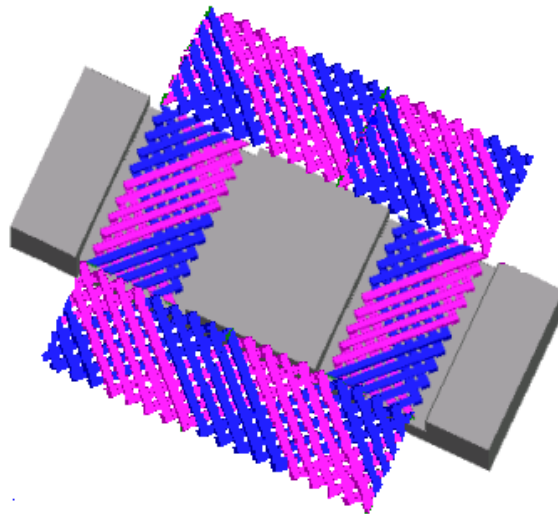
Fig. 64. Planar litz winding in the inductor application.

In my current planar inductor design, amount of manual work had to be done in the iterated simulation-based procedure. This optimization can be further improved, since the data exchange and geometry modification in the software could be realized automatically by writing programs in macro language. It can be imagined that if we use the planar litz winding in the boost inductor as shown in Fig. 64, then not only the winding high-

frequency resistance but also the winding parasitic capacitance could be reduced. Of course, the winding low-frequency resistance and the overall volume may be increased undesirably. The idea of integrating the EMI filter and the boost inductor into one module is really worth trying. Other issues, like the high-frequency winding resistance modeling and advanced thermal modeling, could also be good research topics in future.

References

Chapter 1

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