Design and Characterization of RFIC Voltage Controlled Oscillators in Silicon Germanium HBT and Submicron MOS Technologies

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(ABSTRACT)

Advances in wireless technology have recently led to the potential for higher data rates and greater functionality. Wireless home and business networks and 3G and 4G cellular phone systems are promising technologies striving for market acceptance, requiring low-cost, low-power, and compact solutions. One approach to meet these demands is system-on-a-chip (SoC) integration, where RF/analog and digital circuitry reside on the same chip, creating a mixed-signal environment. Concurrently, there is tremendous incentive to utilize Si-based technologies to leverage existing fabrication and design infrastructure and the corresponding economies of scale. While the SoC approach is attractive, it presents major challenges for circuit designers, particularly in the design of monolithic voltage controlled oscillators (VCOs). VCOs are important components in the up or downconversion of RF signals in wireless transceivers. VCOs must have very low phase noise and spurious emissions, and be extremely power efficient to meet system requirements. To meet these specifications, VCOs require high-quality factor (Q) tank circuits and reduction of noise from active devices; however, the lack of high-quality monolithic inductors, along with low noise transistors in traditional Si technologies, has been a limiting factor.

This thesis presents the design, characterization, and comparison of three monolithic 3-4 GHz VCOs and an integrated 5-6 GHz VCO with tunable polyphase outputs. Each VCO is designed around a differential -G_M core with an LC tank circuit. The circuits exploit two Si-based device technologies: Silicon Germanium (SiGe) Heterojunction Bipolar Transistors (HBTs) for a cross-coupled collectors circuit and Graded-Channel MOS (GC-MOS) transistors for a complementary (CMOS) implementation. The circuits were fabricated using the Motorola 0.4 μm CDR1 SiGe BiCMOS process, which consists of four interconnected metal layers and a thick copper (10 μm) metal bump layer for improved inductive components.

The VCO implementations are targeted to meet the stringent phase noise specifications for the GSM/EGSM 3G cellular standard. The specifications state that the VCO output cannot exceed -162 dBc/Hz sideband noise at 20 MHz offset from the carrier. Simultaneously, oscillators must be designed to address other system level effects, such as feed-through of the local oscillator (LO). LO feed-through directly results in self-mixing in direct conversion receivers, which gives rise to unwanted corrupting DC offsets. Therefore, a system-level strategy is employed to avoid such issues. For example, multiplying the oscillator frequency by two or four times can help avoid self-mixing during downconversion by moving the LO out of the bandwidth of the RF front-end.

Meanwhile, direct conversion or low-IF (intermediate frequency) receiver architectures utilize in-phase and quadrature (I/Q) downconversion signal recovery and image rejection. Any imbalance between the I and Q channels can result in an increase in bit-error-rate (BER) and/or decrease in the image rejection ratio (IRR). To compensate for such an imbalance, an integrated tunable polyphase filter is implemented with a VCO. Control voltages between the differential I and Q channels can be individually controlled to help compensate for I/Q mismatches.

This thesis includes an introduction to design flow and layout strategies for oscillator implementations. A detailed comparison of the advantages and disadvantages of the SiGe HBTs and GC-MOS device in 3-4 GHz VCOs is presented. In addition, an overview of full-wave electromagnetic characterization of differential dual inductors is given. The oscillators are characterized for tuning range, output power, and phase noise. Finally, new measurement techniques for the 5-6 GHz VCO with a tunable polyphase filter are explored. A comparison between the time and frequency approaches is also offered.

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Chapter 1

Introduction

The last few decades have witnessed continuously increasing demand for personal wireless communications services across the globe. For example, it has been reported that wireless data services in the U.S. alone will grow to $16.8 billion by 2006 [1]. This growth is a result of the necessity for sharing information (voice, data, multimedia, etc.) on demand from portable devices. This, in turn, has led to significant research and engineering advances in the field of wireless technology.

Since the first radio transmission in 1894 by Guglielmo Marconi, wireless communication equipment has changed remarkably. Radio Frequency (RF) circuits have evolved from very large multicentimeter distributed components to very tiny (few mm^2) chips of silicon or other materials. Advances in semiconductor device fabrication technology have paved the way for this miniaturization. The demand for smaller and more compact wireless devices is now pushing the integrated circuit (IC) industry to pursue System-on-a-Chip (SoC) solutions for its customers. In a key development, semiconductor manufacturers can now produce high-performance Complementary Metal Oxide Semiconductor (CMOS) and Silicon Germanium (SiGe) heterojunction bipolar transistors (HBT) in the same process [2]. This technology enables mobile communications device manufacturers, such as Motorola and Nokia, to develop smaller, and lower power products for their customers.

One critical component that must be integrated in "single chip" wireless communication transceivers is the voltage-controlled oscillator (VCO). Emerging wireless standards, as well as enhancements to existing standards, have resulted in more de-

manding spurious emission power constraints for VCO designers. For example, the newly adopted 3rd Generation (3G) GSM standard presents a challenging obstacle to the implementation of an SoC solution using the aforementioned IC fabrication advancements. WLAN and home wireless networking equipment are example communication systems that rely heavily on suitable VCO technology. The focus of this thesis project is the implementation of RF VCOs in both CMOS and SiGe HBT technologies and evaluate their relative merit in highly integrated and low-power wireless transceivers.

1.1 Process Technology

High-performance VCO design is heavily impacted by the active and passive devices available within the process technology being used. For example, designing high Q passive components minimizing thermal noise, and flicker noise in active devices, and the resulting trade-off between power efficiency and noise performance are issues that must be addressed. In this thesis, two types of active devices are analyzed: the silicon germanium (SiGe) heterojunction bipolar transistor (HBT) and the graded-channel MOS transistor. In this section, a summary of the fabrication of these devices and related performance implications will be introduced. This section will also establish some fundamental background of these devices and provide insight into how they physically operate.

1.1.1 SiGe HBTs

In recent years, SiGe HBT technology has been introduced by a number of companies. Since the first successful demonstration of the SiGe HBT in December of 1987 [3], research and development efforts have focused on combining HBT and submicron CMOS devices into a single fabrication process (i.e., SiGe BiCMOS). Major industrial foundries, including Motorola [4], IBM [5], TSMC [6], and Infineon are producing 200-mm Si wafers with SiGe n-p-n bipolar HBT devices in conjunction with CMOS technology. Meanwhile, efforts continue to push the frequency limitations of these devices higher and higher to enable new applications in wireless and optical communications.

The frequency range of an active device is typically specified by two figures-of-merit (FOM). The first FOM is the small-signal, unity current gain frequency, f_T, which represents the maximum frequency at which the device may be used as an amplifier. In an HBT, the f_T is given by [2]:

$$f_T = \frac{1}{2}\left[\frac{1}{g_m}(C_{eb} + C_{cb}) + \tau_b + \tau_e + \tau_{bc}\right]^{-1}, \tag{1.1}$$

where C_{eb} (also known as C_π) is the parasitic emitter-base junction capacitance, C_{cb} (or C_μ) is the parasitic collector-base junction capacitance, g_m is the device transconductance, τ_b is the base transit time, τ_e is the emitter delay time, and τ_{bc} is the base-collector junction depletion layer time. The second FOM is the maximum oscillation frequency, f_{MAX}, which is given by:

$$f_{MAX} = \sqrt{\frac{f_t}{8\pi r_B C_{cb}}}, \tag{1.2}$$

where r_B is the parasitic base resistance. The f_{MAX} equation incorporates f_T and is a useful measurement when comparing SiGe HBTs to other HBT families, such as those fabricated in III-V materials, [(e.g., Galium-Arsenide (GaAs) and Indium-Phosphide (InP)]. In comparison to state-of-the-art InP/InGaAs HBTs that have recently obtained an $f_T/f_{\max}$ of 377/230 GHz [7], SiGe HBTs have recently reached record $f_T/f_{\max}$ values of 375/210 GHz [8]. Therefore, SiGe HBTs offer frequency performance comparable to III-V devices for analog and RF circuits while maintaining compatibility with Si CMOS technology.

To fully understand what sets SiGe HBTs apart from traditional Si bipolar junction transistors (BJTs), some clarification on the energy band theory of bipolar devices is required. BJTs are *homojunction* devices, where the emitter, base, and collector regions all have the same bandgap, approximately 1.12 eV for silicon. The *heterojunction* structure was originally proposed by William Shockley in his 1948 transistor patent [9]. Shockley conjectured that a heterojunction transistor having *npn* junctions where either the emitter, base, or collector contained different bandgaps can improve minority-carrier flow [10]. Unfortunately, at that time, researchers did not have the technological capability to manufacture such materials. Finally, in the early 1970s Shockley's ideas were successfully implemented [9] using newly developed

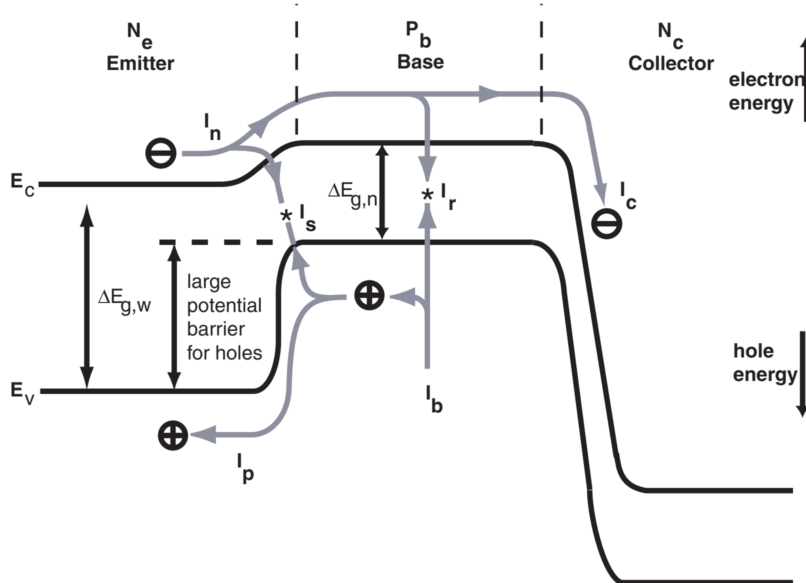


Figure 1.1: Simplified wide bandgap emitter diagram for conventional HBT biased in the active region. The positive and negative signs represent the holes and electrons, respectively (after [11])

epitaxial growth techniques.

The difference between the homo- and hetero-junction device performance lies within their respective band structures. A typical bipolar device uses injection of minority carriers into the base region to control the flow of majority carriers from the emitter to collector. In an *npn* homojunction device, the emitter, base, and collector energy bandgaps are equal. On the other hand, conventional HBTs that use III-V materials have a *wide bandgap* material for the emitter (e.g., AlInAs or InGaAs). The wide bandgap emitter of the *npn* heterostructure, shown in Figure 1.1, results in a large valence (E_v) band-edge discontinuity at the base-emitter compared to the base-collector. There are several advantages to having this energy bandgap configuration. The band-edge discontinuity provides an increased barrier against holes from the base diffusing into the emitter (also known as back-injection). This reduction in hole back-injection current (I_p) decreases the base current (I_B) of the wide-bandgap emitter transistor with respect to the collector current (I_C). Meanwhile, the conduction band (E_c) is designed to have small base-emitter discontinuities, allowing electrons to be easily diffused into the base and eventually injected through to the collector. Additionally, when reducing I_p, the emitter recombination current (I_s)

is also reduced. The decreased I_p will increase I_n and I_C, which is a key factor to increasing the current gain (β) in the device. The current gain is described by the following ratio:

$$\beta \approx \frac{I_C}{I_B} \tag{1.3}$$

Lower doping in the emitter reduces the amount of parasitic base-emitter junction capacitance C_{eb}, which in turn allows wide-bandgap emitter HBT devices to achieve a much higher f_T (equation 1.1) at a given β. Wide-bandgap emitter HBT devices can be designed with a larger emitter area to achieve higher current gain, while no longer becoming impaired by parasitic capacitance.

In addition, the higher energy barrier against hole back-injection in these devices allows for higher doping levels in the base. A higher base doping pushes the depletion regions in the base toward the base-emitter and base-collector metallurgical junctions. This results in an increase in Early voltage (V_A) due to reduced base-width modulation effects [12]. An increase in Early voltage translates to a higher output resistance of the transistor. Additionally, higher doping significantly decreases base resistance (r_B) and decreases the noise figure of the transistor (explanation of noise will be discussed in more detail in Chapter 2.) Reducing the base resistance in bipolar devices also directly increases f_{MAX} (equation 1.2) for a given β.

The structure of a SiGe HBT is significantly different than that of the conventional III-V HBT. First of all, Si and Ge are both column IV semiconductor materials. Unlike the III-V HBT, where the emitter is bandgap engineered, the *base* of a SiGe HBT is modified by introducing germanium (Ge) content. Ge has a bandgap of approximately 0.66 eV compared to pure Si, which has a bandgap of 1.12 eV [2]. Combining these two elements to form a $Si_{1-x}Ge_x$ alloy results in a material with an overall bandgap smaller than that of pure Si. The bandgap of the base material decreases by typically 75 meV per 10% Ge concentration [13]. In other words, the bandgap of the base of a SiGe HBT base is narrower than that of the emitter.

The SiGe concentration profile in both the Motorola and IBM process are unique. The SiGe base has a *graded* concentration of Ge, with the highest concentration found at the base-collector junction. Unlike wide-bandgap emitter HBTs, I_B remains unchanged by the heterostructure, since hole back-injection from the base is determined

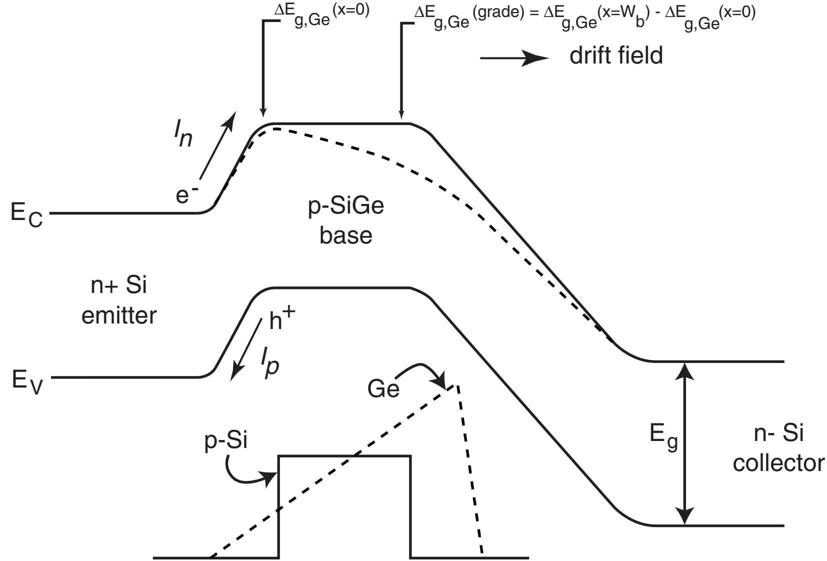


Figure 1.2: The energy bandgap diagram of the Si/SiGe HBT. The dashed line represents the changed conduction band caused by the graded concentration of the Ge in the base (see grading below bandgap diagram) (after [2]).

by the valence bands of the emitter and base which are unchanged in the SiGe HBT. Rather, the performance improvements in SiGe HBTs come from grading the concentration of the Ge within the base itself (Figure 1.2). The graded profile causes a lower potential barrier for electron injection into the base from the emitter, and an enhancement in collector current efficiency for a given emitter-base forward bias is achieved. The graded Ge profile in the base results in a *drift field,* which accelerates electrons from the emitter to the collector, lowering the base transit time τ_b. Additionally, the τ_e is also reduced, therefore increasing the f_T (Equation 1.1). Due to the higher $p+$ doping of the base, a decrease in base resistance r_B will result, with the associated benefit of lower noise.

A further discussion of the Motorola SiGe BiCMOS process employed in this thesis will be given in section 1.1.3.

1.1.2 Submicron Graded Channel MOS

Submicron CMOS devices are also candidates for the active elements within RF VCOs. A modified CMOS technology called Graded-Channel MOSFET (GC-MOSFET)

was found to be useful for RF applications. This device technology was researched and implemented extensively in recent years [14]. The f_T figure of merit for a MOS-FET is approximated by the following equation:

$$f_T = \frac{1}{2\pi} \cdot \frac{g_m}{C_{gs} + C_{gd}}, \tag{1.4}$$

where g_m is the device small-signal transconductance, C_{gs} is the gate-source capacitance, and C_{gd} is the gate-drain capacitance. Additionally, the maximum oscillation frequency is given by:

$$f_{MAX} = \frac{1}{4\pi} \sqrt{\frac{f_T}{R_g \cdot C_{gd}}}, \tag{1.5}$$

where the R_g is the gate resistance. Another important consideration in VCO design is the low frequency $1/f$ noise generated by active devices; this will be discussed in more detail in section 2.2.2. GC-MOS technology offers reduced power levels with high performance while keeping fabrication costs low [15].

The key to GC-MOS technology is in the implanted doping levels of the active layers underlying the MOS transistor gates. The "graded" doping (Figure 1.3) produces a somewhat shorter effective channel gate length, L_{eff}, than the "physical" channel length, L_{dp}, in conventional MOS, resulting in lower capacitance and faster switching speeds (Section 3.2). For example, an L_{eff} of $\sim$ 0.25 μm is achieved using an $L_p = L_{en} + L_{dp}$ of 0.5 μm. This non-uniformity within the channel profile provides a number of benefits. The transconductance is higher because of an electric field that assists the transport of carriers in the inversion layer. The output resistance is improved by the reduced charge sharing effects, considering that the source contains more doping. Lower well doping at the drain end of the channel minimizes mobility degradation and results in satisfactory hot-carrier performance [17]. In addition, compared to standard MOS 30% to 40% more saturation current, lower body effect, and better drain-induced-barrier-lowering (DIBL) have been reported in [14].

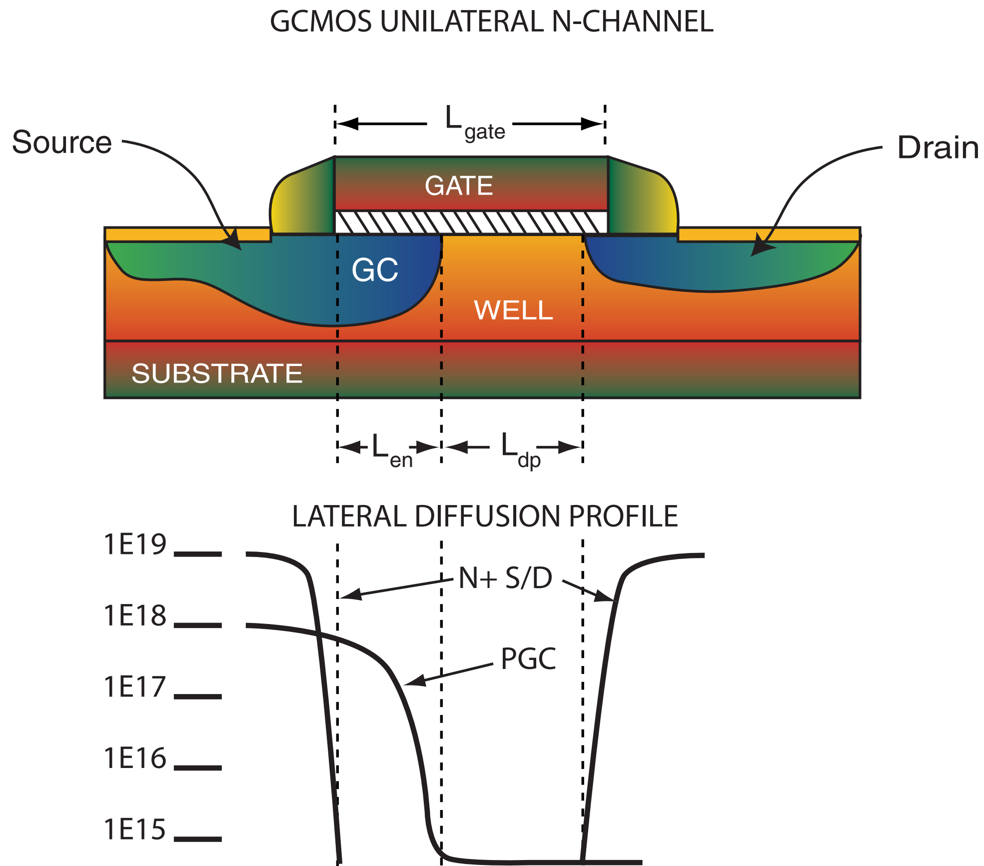


Figure 1.3: Cross sectional view of a unilateral Graded-Channel NMOS device (top) (after [14]). The "effective" channel length of a GCMOS is determined by L_{dp}, which can be much shorter than the physical gate length L_{gate}. For example, a ∼0.25 μm L_{eff} can be achieved even with a 0.5 μm physical gate length. Also shown below are the lateral diffusion profiles in the channel near the Si/SiO_2 interface (after [16]).

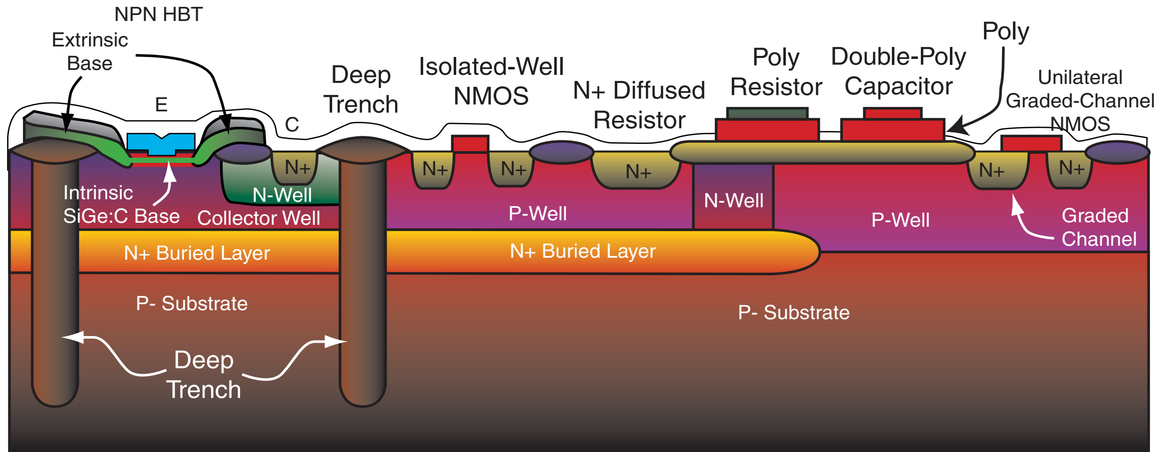


Figure 1.4: Cross-sectional illustration of Motorola's CDR1 0.4 μm L_{eff} BiCMOS (after [17] and [4]).

1.1.3 The Motorola CDR1 BiCMOS Process

Motorola is a world leader in cellular communications equipment and IC manufacturing. The Semiconductor Products Sector (SPS)[1] provides ICs and fabrication services for commercial and government markets. Motorola SiGe BiCMOS fabrication processes are currently based on 0.4 μm and 0.18 μm technology nodes [4]. This process has a total of four metal AlCu layers with a top patterned electroplated copper metallization (bump layer) and passivation for the high-performance inductors. As mentioned above, the ability to integrate both SiGe HBTs and Si CMOS devices within a single process is making wireless SoC a near-term possibility. Motorola's SiGe HBT process is designed to be compatible with the CMOS process platform thermal cycle steps, while continuing to achieve a high yield percentage of working devices. This thesis utilizes the 0.4 μm CDR1 SiGe:C BiCMOS process for circuit design and fabrication (Figure 1.4).

SiGe:C Base Specifics

Bandgap engineering of the SiGe base has been enabled by advances in semiconductor material growth. High-purity, low-defect crystal structures may be produced using

[1] Motorola SPS is now Freescale Semiconductor.

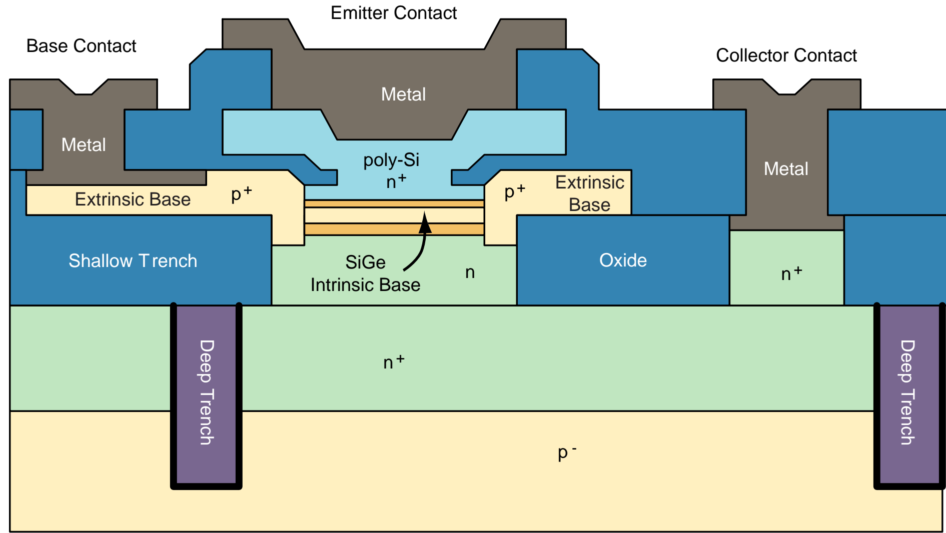


Figure 1.5: Cross section of SiGe HBT illustrating extrinsic and intrinsic SiGe base (after [20]).

molecular beam epitaxy (MBE), rapid-thermal chemical-vapor deposition (RTCVD), ultra-high vacuum chemical-vapor deposition (UHV/CVD), or reduced/atmospheric-pressure chemical-vapor deposition (RPCVD) [2]. UHV/CVD is the most typical method used in SiGe BiCMOS processes [18]. This technique allows for silicon wafers to be passivated before film growth using hydrogen while certain contaminants that are active with silicon (i.e., oxygen, water, and carbon) are selectively removed. This helps increase uniformity and yield during the CMOS integration with SiGe alloy film growth [19].

The epitaxial SiGe alloy is applied at the intrinsic base of the HBT. A "quasi-self-aligned" (QSA) N(Si)-P(SiGe:C)-N(Si) structure is formed with a non-selectively grown epitaxial SiGe intrinsic base (Figure 1.5). The 'C' represents the addition of carbon doping in the base of the HBT. Carbon significantly reduces the diffusion spreading of boron at the extrinsic base from the thermal impacts of the next process step. This is also known as transient enhanced diffusion (TED), which is the spreading of boron due to the thermal cycling of the CMOS platform technology [4]. A QSA structure is achieved through purposeful misalignment tolerances (a couple of tenths of micron) within the photolithography process during the fabrication of the extrinsic base and the emitter polysilicon. The SiGe film is produced within

HBT parameter for a 0.35μm process	
Beta β	120
Early Voltage (V)	95
BV$_{CEO}$ (V)	3.4
f_T @ 2V (GHz)	49
f_{MAX} @ 2V (GHz)	86
I_C @ Peak f_T/f_{MAX} (mA/μm^2)	~1.5
NF$_{MIN}$ @ 2GHz (dB)	0.9
Minimum W_E (μm)	0.4
Intrinsic Base R_S (Ω/sq)	1.9k

Table 1.1: Characterisics of the HBT in Motorola's CDR1 SiGe:C BiCMOS process (after [4]).

a reduced-pressure chemical-vapor deposition (RPCVD) reactor. The implanted self-aligned intrinsic collector profile is optimized to reduce parasitic collector-base capacitance. Finally, a doped polysilicon layer is deposited to form the emitter. The extrinsic base is self-aligned to the emitter to reduce the extrinsic base resistance [4].

Table 1.1 shows some reported characteristics of the Motorola CDR1 SiGe:C BiCMOS process.

Motorola SiGe:C BiCMOS Process Steps

The general sequence of steps that comprise the CDR1 SiGe:C BiCMOS process is illustrated in Figure 1.6. An outline of these steps is as follows:

1. The N^+ buried layer is formed within the highly resistive P^- substrate using a series of high-energy ion implantations. This is followed by a thin epi-silicon growth used to create the collector for the *npn* device, the well for the GC-PMOS, and the isolated-well for *n*-channel devices.

2. Polysilicon-Encapsulated Local Oxidation of Silicon (LOCOS), or PELOX, is then employed to provide isolation for the GC-MOS devices.

3. Isolation for the NPN bipolars is then accomplished with the addition of deep trenches, which minimize the parasitic collector-substrate capacitive coupling

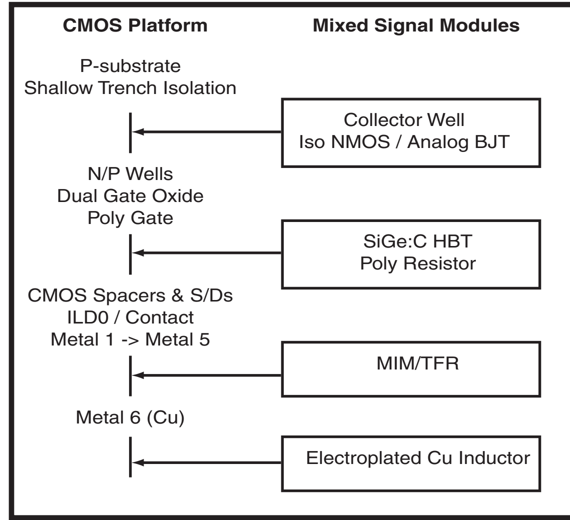


Figure 1.6: Integration of mixed signal modules with the CMOS platform technology in the Motorola CDR1 process [21]

between adjacent devices.

4. Implantation of N-well and P-well in the P-Epi layer.

5. The n-type S/D GC-MOS (GC-NMOS) devices are fabricated using a self-aligned process. Implanting graded dopings on the source side of the channel results in *unilateral* GC-NMOS, while, implanting both source and drain sides of the channel results in *bilateral* GC-NMOS. Blocking the GC implants results in the fabrication of a conventional MOS device.

6. The MOS drain and source region implantations are performed using a self-aligned poly gate (gate oxide thickness is 50Å), which sets the V_t threshold voltage. Following these implants, a rapid thermal annealing (RTA) process step is used to activate the dopants. Titanium Silicide ($TiSi_2$) is deposited over the exposed regions of the source, drain, and gate regions to reduce contact resistance, which improves performance at higher frequencies [22]. In addition, the Titanium Silicide helps facilitate the connection of the N+ and P+ polysilicon gates for contacts to the first metal layer.

7. Following the RTA for the N+ source and drain, which also includes collector well activation, the *SiGe:C HBT module* is inserted into the process flow. The

SiGe base is selectively grown epitaxially and is highly doped with boron to help reduce the base resistance R_B. The HBT module is completed by applying an *in-situ* doping at the emitter using a polysilicon deposition through an emitter window. This is then followed by an extrinsic base implant to reduce base resistance. In addition, there is final selective implant to form the collector.

8. The self-aligned boron implantation of P+ source and drain regions form the diffusion regions of the PMOS devices.

9. Spacers are applied followed by another RTA step. Next, titanium silicide ($TiSi_2$) is formed to create the poly gates preceding the deposition of metal layers.

10. The formation of the lowest AlCu metal layers (metal 1 - metal 2) and vias are applied.

11. The final two layers of metal consist of the application capacitors. The low-parasitic, highly linear metal-insulator-metal (MIM) capacitors are defined between the last two metal layers (metal 3 and 4) of the process using nitride-oxide (NO) deposition as the dielectric.

12. Electroplated copper metal is applied as the final layer. This is detailed further in Section 3.1.1.

1.2 Receiver Architectures

The objective of this work is to develop RF VCOs for highly integrated RF transceivers. A transceiver (transmitter-receiver) is a subsystem that translates radio frequency (RF) electromagnetic waves propagating in the atmosphere to (upconversion) and from (downconversion) electrical baseband information. There are two popular approaches to downconversion receivers. First, in many instances heterodyne[2] receivers convert RF signals to a lower intermediate frequency (*low-IF*). Second, homodyne[3] receivers, also known as *direct conversion receivers* (DCR), will convert RF signals to *zero-IF*.

[2] Heterodyne is derived from the Latin roots hetero (different) and dyne (to mix).
[3] Homodyne is derived from the Latin roots homo (same) and dyne (to mix).

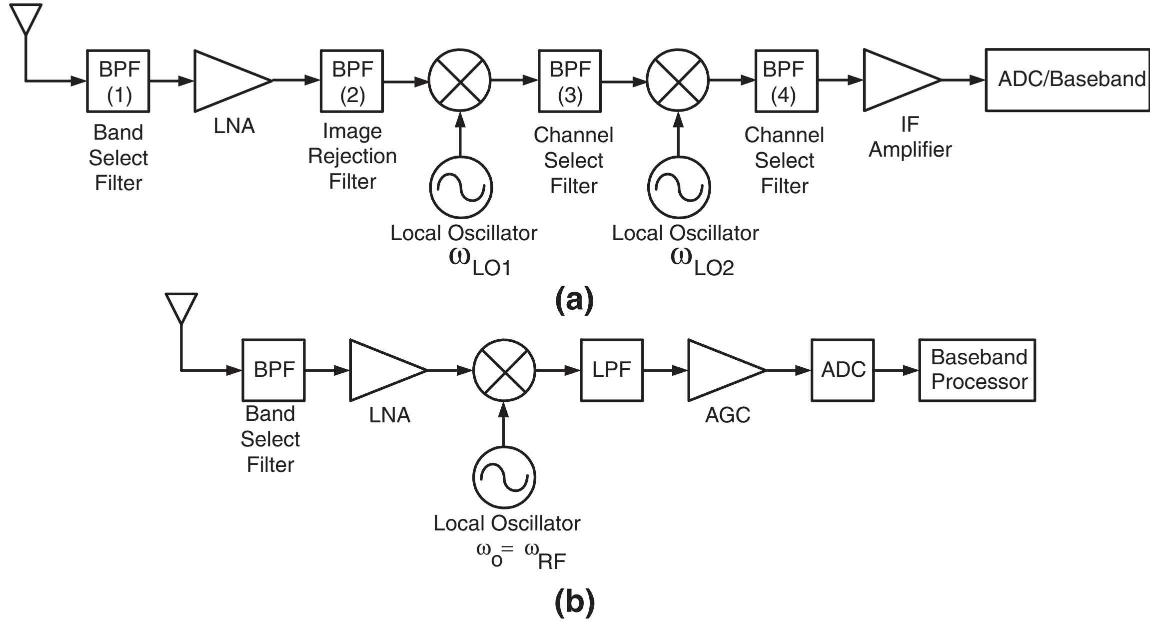


Figure 1.7: There are two major classifications for receiver architectures: (a) heterodyne requires two or more stages of mixing; (b) homodyne uses one stage of mixing and $LO = RF$ (after [23]).

1.2.1 Heterodyne Receivers

The heterodyne architecture down-converts an RF signal using two or more stages of LO mixing [Figure 1.7(a)]. Mixing an RF signal with a local oscillator results in an intermediate frequency given by:

$$f_{IF} = |f_{RF} - f_{LO}| \tag{1.6}$$

where f_{RF} is the RF signal frequency and f_{LO} is the local oscillator. An IF signal is produced after each mixing stage, which requires filtering and amplification before the next down conversion stage. The underlying premise of the heterodyne approach is to down convert the wanted spectrum in stages such that the selectivity requirements for channel select filters are eased. For a two-stage heterodyne receiver, the first LO frequency is chosen to be $f_{LO_1} = f_{RF} - f_{IF_1}$, and the second stage LO $f_{LO_2} = f_{IF_1} - f_{IF_2}$. Implementation of highly selective on-chip RF bandpass filters (BPFs) is not possible using the currently available IC technologies, and is usually accomplished with external components such as Surface Acoustic Wave (SAW) filters. Highly selective

filters require high-Q resonators to avoid high passband interference. Incorporating of such off-chip components results in higher manufacturing and packaging costs.

A major issue with heterodyne receivers is the concurrent downconversion of *image* frequencies. An image is an unwanted frequency spectrum that is mixed down into the desired band of interest. The downconversion process does not preserve the *polarity* of the frequency difference between the RF and LO (Eq. 1.6). If the RF signal is exactly one IF higher than the LO (low-side injection), the image frequency is located at:

$$f_{IMG} = f_{LO} - f_{IF} = f_{RF} - 2f_{IF}. \tag{1.7}$$

If the RF signal is exactly one IF lower than the LO (high-side injection), the image frequency is located at:

$$f_{IMG} = f_{LO} + f_{IF} = f_{RF} + 2f_{IF}. \tag{1.8}$$

The unwanted image must be dealt with by some form of *image-rejection*. One simple approach is to use image rejection filters placed before the RF mixer to attenuate any interference located at the image frequency. Because most practical receivers choose a relatively low f_{IF} frequency, employing an image rejection filter requires a very high-Q filter. Such high-Q filtering has proven to be a major challenge in today's IC processes for SoC integration. Therefore, to realize such a solution requires an off-chip filter. This also typically requires the LNA to drive a 50 Ω output into the filter component, which reduces design flexibility. Recently, popular solutions to these image rejection issues are either direct conversion or low-IF image reject receiver architectures.

1.2.2 Homodyne Receivers: Direct Conversion Receiver (DCR)

The homodyne receiver approach mixes an RF signal with an LO signal that is exactly equal to the RF carrier [Figure 1.7(b)], which directly translates the desired spectrum down to baseband (zero-IF). This is also sometimes called *direct-conversion*. The homodyne architecture permits the use of *lowpass*, low-frequency channel select filters that can be readily integrated on-chip, in contrast to the off-chip high-Q BPFs that are required for heterodyne receivers. However, by directly downconverting to a

zero-IF, the issues of image are completely eliminated.

One popular DCR receiver architecture that translates a desired spectrum uses the *quadrature* downconversion process. Quadrature downconversion entails converting an RF signal using In-Phase (I) and Quadrature-Phase (Q) channels (90° phase difference). Certain modulation schemes (i.e., BPSK, QPSK, etc.) require quadrature receivers to retrieve the wanted information. I/Q downconversion is required for recovering the positive and negative halves of the wanted spectrum. Unfortunately, quadrature downconversion can be seriously degraded by the phase and amplitude mismatch between quadrature channels. The I/Q channel errors may arise from manufacturing flaws, which lead to either unmatched phase shifts between channels or inaccurate phase outputs. For example, implementing a specific output channel that must have a 90° phase shift with some unexpected degree of error variation, may result in degradation in system performance.

There are also a few additional drawbacks that may occur specifically within homodyne receivers. First, DCRs are susceptible to undesired *DC offsets*. These extraneous offset voltages can corrupt the desired spectrum due to the presence of information content at zero-IF. These DC offsets occur by the *LO leakage* self-mixing with itself through the RF signal path. LO leakage and DC offsets are discussed further in Section 1.3.2. Finally, $1/f$ (flicker) noise or low-frequency noise from active devices can also corrupt the signal around the spectrum converted to zero-IF. Flicker noise is a severe problem in a MOS device and will be explained further in Chapter 2.

1.2.3 Low-IF or Digital IF Receivers

An alternative to the homodyne receiver is the low-IF or *digital IF* receiver. A low-IF receiver downconverts the desired spectrum directly from RF to some very low-IF (typically $<$ few 10s of MHz). The advantages of using a low-IF over a zero-IF is that this eliminates the issues of DC offsets and reduces susceptibility to $1/f$ noise. Low-IF receivers can also be highly integrated, since filtering can be done on-chip while maintaining high performance [24]. In addition, the down converted spectrum is at a low enough frequency that it can be easily sampled by low-power analog-to-digital converters (ADC), and is thus also known as digital IF. The spectrum may then be

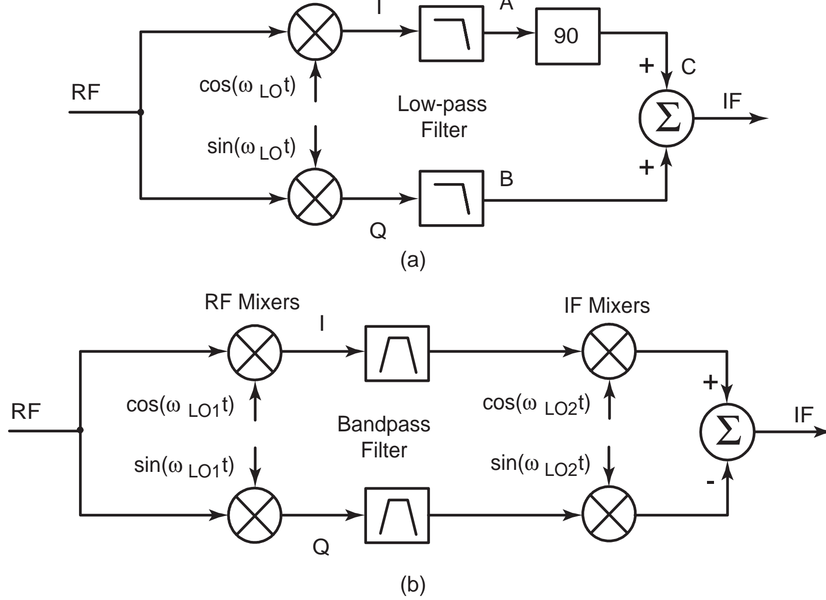


Figure 1.8: Block diagrams of the (a) Hartley and (b) Weaver image rejection architectures (after [20]).

converted to baseband using digital signal processing (DSP). However, with low-IF receivers, as with heterodyne receivers, comes the issue of image rejection. Due to the difficulties in achieving sharp-cutoff analog BPFs with low-power consumption for image rejection, designers have pursued image-cancelling architectures. Two popular image-cancellation receivers are the Hartley and Weaver architectures.

Hartley Architecture

The Hartley configuration [Figure 1.8(a)] uses quadrature downconversion with a local oscillator supplying $\sin \omega_{LO} t$ and $\cos \omega_{LO} t$ to a pair of mixers. The outputs of the mixers (I and Q branches) are first low-pass filtered, then one branch is shifted by 90° with respect to the other, and finally the branches are summed. For a single tone input, at points A and B (the outputs of the LPFs) the time-domain signals are:

$$x_A(t) = \frac{A_{RF}}{2} \sin(\omega_{LO} - \omega_{RF})t + \frac{A_{IMG}}{2} \sin(\omega_{LO} - \omega_{IMG})t \tag{1.9}$$

$$x_B(t) = \frac{B_{RF}}{2} \sin(\omega_{LO} - \omega_{RF})t + \frac{A_{IMG}}{2} \sin(\omega_{LO} - \omega_{IMG})t, \tag{1.10}$$

where ω_{IMG} is the frequency of the image component, ω_{RF} is the input signal, and ω_{LO} is the local oscillator. Following the 90° phase shift, the upper branch signal at point C is:

$$x_C(t) = \frac{A_{RF}}{2}\cos(\omega_{RF} - \omega_{LO})t - \frac{A_{IMG}}{2}\cos(\omega_{LO} - \omega_{IMG})t. \quad (1.11)$$

Summing (1.11) and (1.9) gives the desired IF with a cancelled image output:

$$x_{IF}(t) = A\sin(\omega_{RF} - \omega_{LO})t. \quad (1.12)$$

The quadrature downconversion followed by a 90° phase shift in one path produces separate paths with the same polarity for the desired signal, but opposite polarity for the image. In the frequency domain, the 90° phase shift operation multiplies the negative frequency part of $X_A(\omega)$ by $+j$ and the positive frequency part by $-j$ (Hilbert transform). The summation of $X_C(\omega)$ and $X_B(\omega)$ produces an image free IF spectrum.

The primary disadvantage of the Hartley architecture is the vulnerability to amplitude and phase mismatches between the quadrature channels. A measure of how well the image is suppressed is defined as the *image rejection ratio* (IRR). A poor IRR can be caused by inexact phase shifts, amplitude and phase mismatches between the mixers, LPFs, and summers in the two branches.

Weaver Architecture

The Weaver image rejection architecture [Figure 1.8(b)] utilizes two stages of mixing; the second stage of I and Q mixing is essentially equivalent to providing the 90° phase shift used in the Hartley approach. Figure 1.9 shows the associated frequency spectrums of the Weaver image rejection process. The RF signal (f_{RF}) and its image ($f_{IMG_1} = f_{RF} - f_{LO_1}$) are downconverted to an I channel IF ($f_{IF_1} = f_{LO_1} - f_{IF_1}$), in which both the desired signal and the image are at the same frequency (point A). Conversely, the image and desired signal are located at the same frequency and have opposite polarities on the imaginary axis (point B). A band-pass filter attenuates any secondary image ($f_{IMG_2} = 2f_{LO_2} - f_{RF} - 2f_{LO_1}$) components (points C and D), as to not allow unwanted image spectrums to infiltrate the desired mixing product

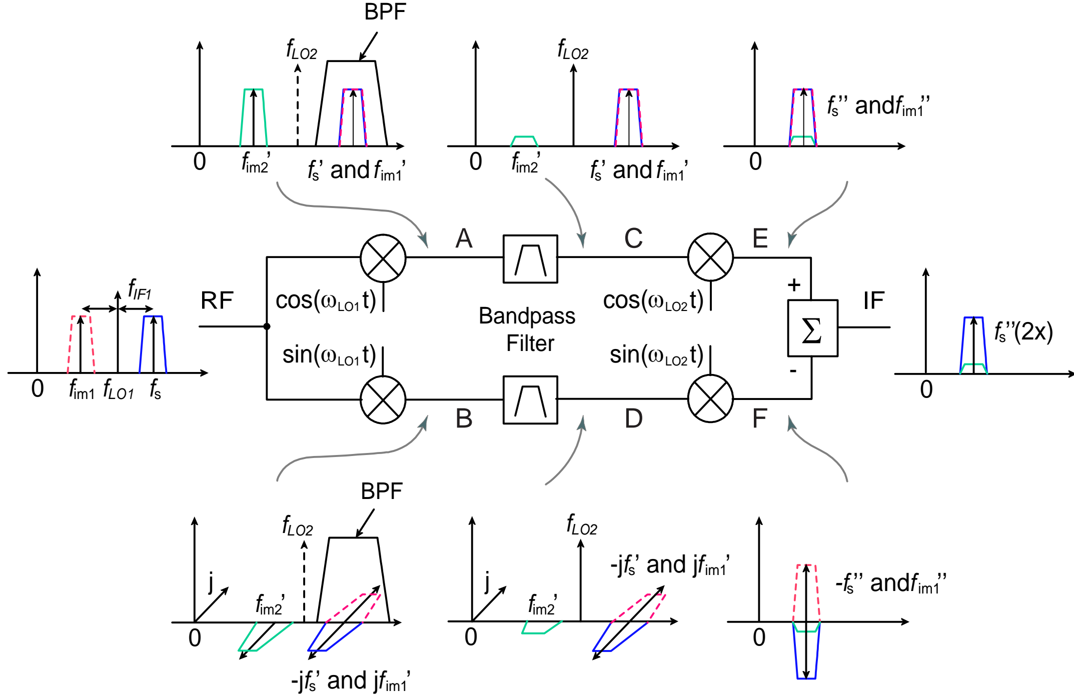


Figure 1.9: Associated spectrum for the Weaver image-rejection architecture (afer [20]).

of the second stage mixers. At point E, the second IF ($f_{IF_2} = f_{RF} - f_{LO_1} - f_{LO_2}$), the desired signal, first image, and second image have the same polarity on the I channel. On the Q channel, following the second stage of mixing is the signal, first image, and secondary image that have just been converted from the imaginary axis back to the real axis (point F). Finally, the signal and the image continue to have opposite polarity compared to the first image. The Q channel is subtracted from the I channel, which produces an *image-free* IF output. The Weaver architecture is also prone to gain and phase imbalance, which can degrade the image rejection ratio.

1.3 Thesis Objective

The objective of this thesis addresses two important issues for the various receiver architectures discussed above. First, the issue of I/Q mismatch must be dealt with to reduce I/Q demodulation errors in DCR/Low-IF receivers and to improve IRR in Weaver and Hartley architectures. Second, undesired DC offsets due to LO leakage

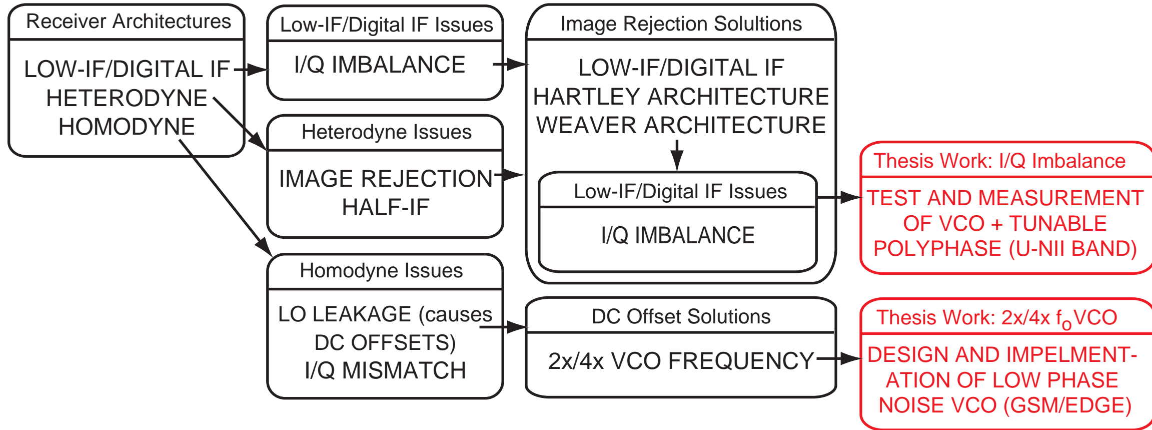


Figure 1.10: Overview of receiver issues and solutions addressed in this thesis.

that arise in zero-IF receivers must be mitigated.

1.3.1 (I/Q) Imbalance Solution: VCO with Tunable Polyphase Outputs

It is imperative that the I and Q branches in a quadrature receiver maintain a phase difference as close as possible to 90° for proper demodulation and high image-rejection. For example, both the relative gain error, ϵ, and phase error, θ, can cause the IRR to be degraded.

The Q channel VCO output can be written as:

$$x_{LO_Q}(t) = A\cos\omega_c t. \tag{1.13}$$

The corresponding Q channel downconverted RF signal with gain and phase error introduced may be expressed as:

$$x_I = a \tag{1.14}$$

$$x_Q(t) = A(1+\epsilon)\cos(\omega_c t + \theta) \tag{1.15}$$

If there is approximately 5% relative gain error and 5° of relative phase error, the IRR achieved will only be about 25 dB. However, if 60 dB IRR is required in a system with similar gain error, the phase error (θ) must equal 0.1°, a very difficult

specification to meet in practical systems [25].

To compensate for these errors, phase control between the I and Q LO signals can be accomplished using a tunable polyphase filter. One unique implementation exploits series varactors to tune the RC-CR polyphase network outputs to achieve appropriate relative phases [26]. Such a tunable polyphase is one solution that addresses the issues of I/Q imbalance for low-IF receivers [Figure 1.10]. *This thesis will present the test and measurement of an integrated VCO with a tunable quadrature polyphase designed for the U-NII band designed in previously published work [20].* With an appropriate control system implementation, this tunable polyphase VCO design could be used to alleviate phase errors due to process variations, component mismatch, and frequency tuning to achieve high levels of IRR.

1.3.2 DC Offset/LO Leakage Solution: 2x/4x Frequency VCO

While direct conversion receivers do not suffer from image problems as is the case with low-IF receivers, they must instead contend with the problems of undesired DC offsets. There are two categories of DC offsets: Type 1 and Type 2 [27] [23]. Type 1 offsets occur when the LO signal leaks back into the mixer RF or LNA input port [Figure 1.11(a)]. The leaked ω_{LO} signal can then be downconverted with itself (also called "self-mixing"), presenting a strong DC offset component overlapping the desired spectrum. Type 2 offsets occur when there are interferers mixed with the input RF signal and leaks into the LO port of the mixer [Figure 1.11(b)]. In this case, as an interfering signal ω_{int} mixes with itself, the distortion becomes proportional to the power of the interfering signal [27]. In either case, the DC offset can be time varying due to variations in environmental propagation conditions. There are a number of potential solutions for alleviating these problems. One solution is to design a network to couple the desired AC signal and block the DC; however, the major drawback to this solution is that this may result in lost in wanted DC signal. Another approach is to use modulation schemes that have low DC content or "DC-free coding", but such schemes have relatively poor spectral efficiency. Another solution is to sample the actual DC offset (typically during a "quiet" time slot) and subsequently subtract that level from the downconverted spectrum during signal reception. This typically involves an increase in the baseband digital processing, which may result in increased

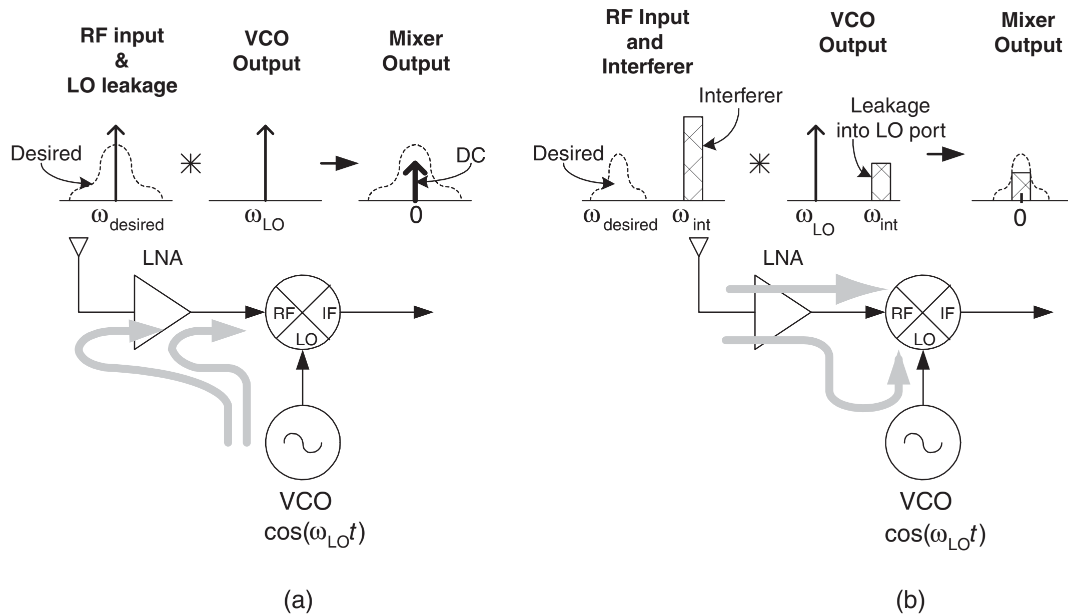


Figure 1.11: Two types of LO self-mixing that can affect a receiving system. (a) Type 1 self-mixing occurs when there is LO leakage through the antenna, and (b) Type 2 when the interferer is leaked through the oscillator (after [27] [23]).

power consumption. An attractive approach is the use of LO frequencies substantially different than the RF band (e.g., two to four times the carrier). Now, if such a higher frequency output leaks back into the RF input, it is expected that there will be less self-mixing since the RF mixer input or LNA input will be less sensitive to these frequencies. In other words, the LO leakage frequencies are moved out of band for these components. The LO output can then be divided down appropriately to pump the mixers, or a subharmonically pumped mixer can be used.

Another issue that arises within oscillators "injection pulling" [23]. This occurs when a nearby large-magnitude interferer leaks into the VCO. The LO frequency will shift toward the interferer's frequency as the interferer amplitude increases; eventually, the LO can "lock" to this frequency. The closer the interferer is to the LO frequency, the more likely it is that pulling will occur. Increasing the oscillator frequency by 2x/4x minimizes the possibility of an interferer near the RF carrier pulling the VCO.

This thesis will also present the design, characterization, and implementation of 2x/4x transmit and receive VCOs for operation in both GSM and DCS/PCS systems [Figure 1.10].

1.4 Applications

As described above, there are two main objectives of this thesis:

1. Design and characterize a 2x/4x VCO.
2. Investigate a new measurement approach for a VCO with a tunable polyphase.

These two thesis objectives are well aligned with practical applications. The quadrature VCO with tunable polyphase outputs can be utilized in systems designed for the 5-6 GHz U-NII (Unlicensed National Information Infrastructure) band. Meanwhile, the 2x/4x VCO is designed to meet specifications for a highly integrated Motorola GSM transceiver.

1.4.1 U-NII Band

The Unlicensed National Information Infrastructure (U-NII) band serves primarily as a high-speed physical layer. It lies in the 5-6 GHz range to circumvent frequency interference from other users in the 2.4-3 GHz range, which have allocated spectrum for 802.11b, Bluetooth, cordless phones, microwaves, etc. The U-NII band consists of three specific EIRP and frequency bands: 5.15-5.25 GHz (50 mW peak), 5.25-5.35 GHz (250 mW peak), and 5.725-5.825 GHz (1 W peak). The 802.11a standard specifically employs orthogonal frequency division multiplexing (OFDM), which mitigates interference between devices and fading effects. The tunable polyphase design mentioned above is also relevant to these modulation schemes because I/Q quadrature demodulation techniques must be utilized.

1.4.2 The GSM/EGSM System Transceiver

The second thrust of this thesis is the design of low-power, high-performance LC-VCOs that can be integrated within an advanced, highly integrated wireless communications transceiver architecture (Figure 1.12). This particular transceiver is being developed for the Global Systems Mobile (GSM), Enhanced Global System Mobile (EGSM), Digital Communication System (DCS), and the Personal Communication

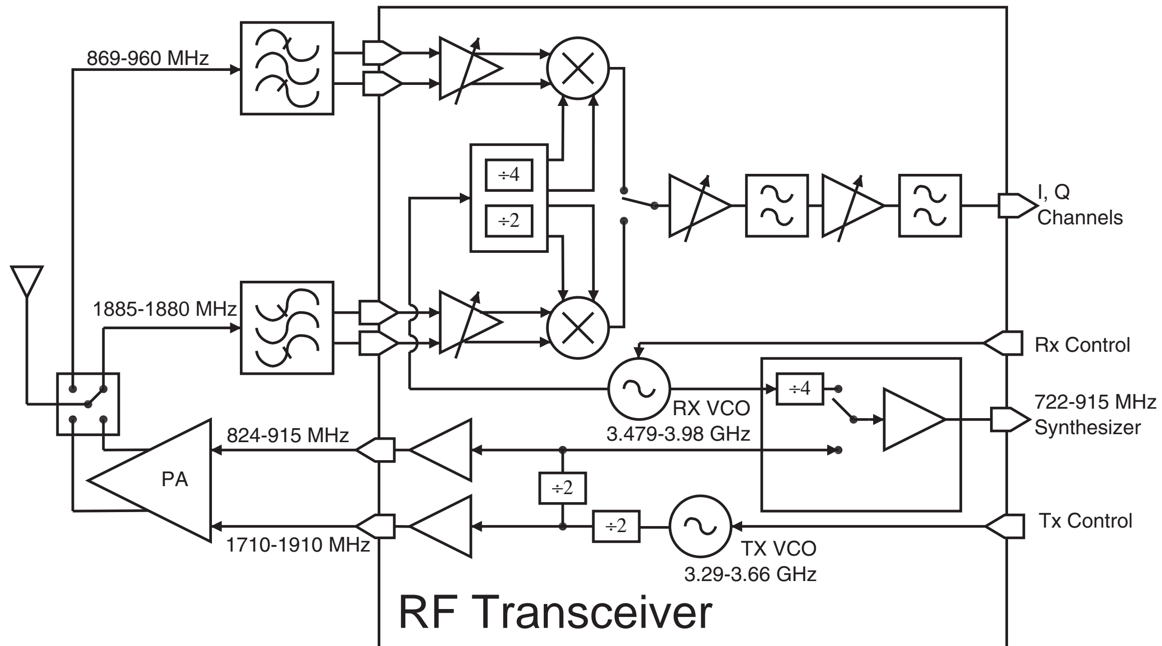


Figure 1.12: GSM RF Transceiver architecture and implementation of the integrated VCOs.

System (PCS) in both North American and European markets. These standards are part of the Third Generation Partnership Project (3GPP) and are based on backward compatibility with GSM with support for Enhanced Data Rates for GSM Evolution (EDGE). In Motorola's current low-cost cellular platform, the system is separated into several separate ICs, specifically the RF power amplifier, RF transceiver (Direct Conversion Receiver), power management IC, and a large mixed-mode block containing the ADC, synthesizers, and baseband processing. The expectation is that these components will ultimately be combined together into one highly integrated SoC.

VCO Design for GSM in a Direct Conversion Transceiver

For this system focus, the VCOs must be designed to meet specifications for both the 850/900 MHz GSM/EGSM and the 1.8/1.9 GHz DCS/PCS standards. Table 1.2 shows the specific frequency ranges for these bands. The GSM, EGSM, DCS, and PCS standards were specifically developed to increase data transmission rates while maintaining spectral efficiency [28]. The existing GSM standard will ultimately be migrated from its current circuit-switched voice network to a complete EDGE packet-

Standard	Tx/Rx	Low-side of Frequency Band	High-side of Frequency Band
GSM 850	Tx	824 MHz	849 MHz
GSM 850	Rx	869 MHz	894 MHz
E-GSM 900	Tx	880 MHz	915 MHz
E-GSM 900	Rx	925 MHz	960 MHz
DCS 1800	Tx	1710 MHz	1785 MHz
DCS1800	Rx	1805 MHz	1880 MHz
PCS 1900	Tx	1850 MHz	1910 MHz
PCS 1900	Rx	1930 MHz	1990 MHz

Table 1.2: Frequency specifications for the integrated VCOs for multi-standard applications (after [29]).

switched system. EDGE works by increasing the rate at which bits of information can be handled by the existing GSM time slot structure. Today, each standard GSM time slot offers a user data rate of 9.6 kbit/s (14.4 kbit/s in more advanced networks). With EDGE, each timeslot will be capable of providing a bit-rate of 48 kbit/s per timeslot. Therefore, with eight time slots available per frequency, EDGE offers a total data throughput of up to 384 kbit/s.

The conventional GSM system must now meet the challenge of migrating to EDGE systems through a sequence of evolutionary steps. The initial voice-only network, which also first added the short messaging service (SMS), was soon followed by high-speed circuit-switched data (HSCSD), and then later added the general packet radio service (GPRS) capability. All of these services use the same modulation format of the original GSM voice network (0.3-GMSK), and change the allocation of the bits and/or packets to improve the basic GSM data rate. A major characteristic of EDGE is that its channel allocation has identical bandwidth occupancy to the original 0.3-GMSK signal. This means that the EDGE system can leverage existing Base/Cell station equipment. The EDGE system can triple the on-air data rate while maintaining essentially the same bandwidth occupancy of the original 0.3-GMSK signal. EDGE achieves this by introducing 8-PSK (octagonal phase shift keying) modulation in addition to the GMSK [30]. 8-PSK can carry 3 bits per modulated symbol, while the standard GMSK signal allows only 1 bit per symbol. These extra bits, however, comes at the price of decreased sensitivity of the 8-PSK signal.

The challenge now is to develop mobile handheld units that can generate and receive

Noise Power Emitted	Low-side of Frequency Band	High-side of Frequency Band
-79 dBm	869 MHz	894 MHz
-71 dBm	1930 MHz	1990 MHz

Table 1.3: GSM/EDGE standard for Transmit Mode Noise Power Limit at a 20 MHz offset: The limit of noise power emitted in 100 kHz bandwidth for a mobile power emitted by the transmitter in the 100 kHz bandwidth (after [29]).

the GSM/EDGE-compatible signals. Unlike the current GMSK modulation, which has an approximate constant envelope, the EDGE signal (8-PSK) has a time-varying envelope. This means that highly nonlinear amplifiers cannot be used with such signals, which potentially degrades power efficiency. Thus, it is of interest to create the most efficient EDGE transmitter that will meet signal-quality specifications.

System Budget

The VCO designs for this application are intended to meet all GSM specifications. The specific noise power requirements for the GSM transmit standards are presented in Table 1.3; these are the most stringent requirements for the VCOs. Within a given channel bandwidth, it is important that the transmitter does not generate spurious sideband noise that could interfere with adjacent channels. Sideband noise can be caused by the *phase noise* of the VCOs and will be discussed further in Section 2.2.3. Therefore, careful attention to an oscillator phase noise performance is required when designing for such communications systems.

Figure 1.13 shows where the transmit VCO is implemented within the architecture. Here it is assumed that the *absolute* output power from the buffers (P_{o_1}) will be about 8 dBm, and the gain of the PA is approximately 25 to 33 dB. The current and most stringent GSM specification requires that the maximum output noise power at the transmitting antenna (P_{o_2}) be -79 dBm within a 100 kHz bandwidth at 20 MHz offset (ω_Δ) from the carrier. Therefore, assuming a worst case PA gain level of 33 dB, the input noise power to the PA (P_{o_1}) must be -79 dBm $-10\log 100 \times 10^3 - 33 = -162$ dBm/Hz. The term -79 dBm $-10\log 100 \times 10^3$ converts absolute power of -79 dBm within a 100 kHz bandwidth at the 20 MHz offset to noise per Hz bandwidth (spot noise) to -129 dBm/Hz at the output of the antenna (P_{o_2}). Therefore, the VCO

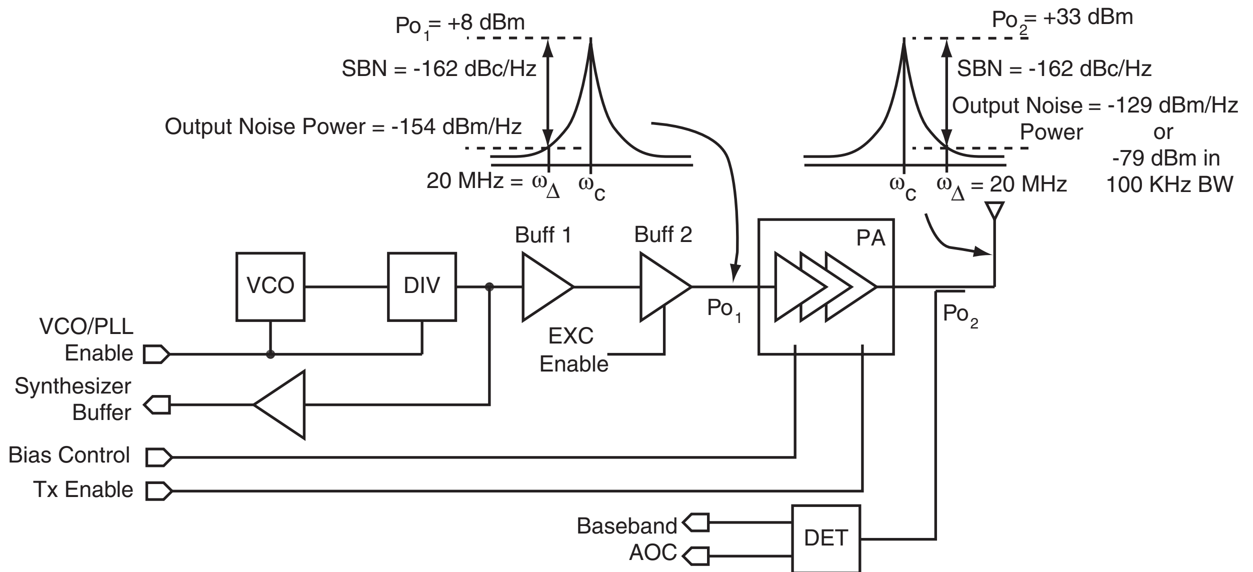


Figure 1.13: The GSM/EGSM and DCS/PCS transmitter lineup for GMSK modulation. There is also the worst case associated absolute powers and the specified phase noise at 20 MHz offsets from the carrier.

output buffer noise must be no worse than -154 dBm/Hz (-162 dBc/Hz) at the 20 MHz offset.

If the VCO is operated at 2x/4x (the frequency of interest for the reasons discussed above), frequency dividers are employed, and the phase noise requirements may be relaxed somewhat. In the worst case scenario, integrating dividers that reduce the frequency by a factor of two reduces the noise power will be reduced by approximately $20 \log 2 \approx 6$ dB. In other words, because the VCO is functioning at twice the frequency, the phase noise specification can be relaxed to -162 dBc/Hz $+6$ dB $= -156$ dBc/Hz phase noise.

Frequency Dividers

Given the benefits of employing a 2x/4x VCO with follow-on dividers, a brief discussion of frequency division circuits is in order. The design of a frequency divider must maintain low phase noise so as not to compromise the performance of the VCO output. It has been shown that an ideal noiseless digital divider with a ratio of N reduces the input phase noise by $20 \log_{10} N$ at the divider output [31]. However,

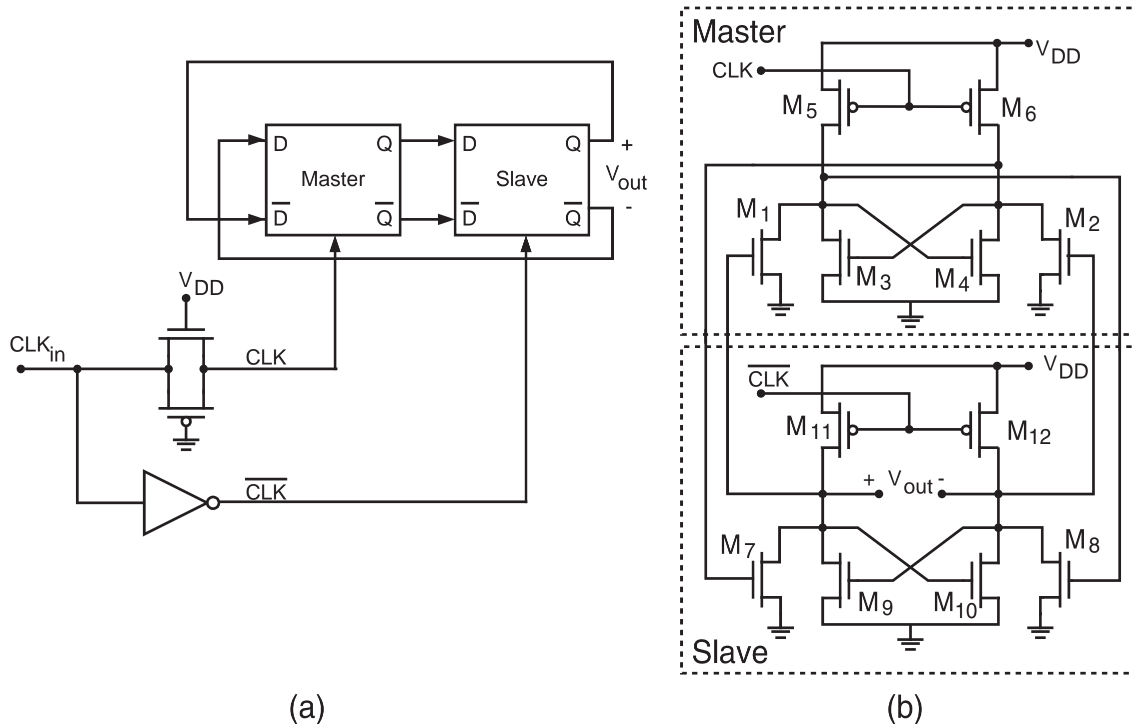


Figure 1.14: Example 1/2 frequency divider block diagram (a) and equivalent circuit (b) (after [33]).

a major negative effect of dividers is internal *crosstalk*. Crosstalk occurs when the higher harmonics input frequency appears at the output of the divider chain. Therefore, additional circuitry may be required to filter out this leakage. Furthermore, there may be some close-in carrier noise contributed mostly by the physical noise contributions of the active devices (typically CMOS) in the dividers [32].

A basic 1/2 frequency divider may be realized as two D-latches in a master slave configuration with negative feedback, as shown in Figure 1.14. This example divider circuit has been shown to operate with very low power at 13.4 GHz [33]. Each latch consists of two sensing devices (M_1 and M_2, M_7 and M_8), a regenerative loop (M_3 and M_4, M_9 and M_{10}), and two pull devices (M_5 and M_6, M_{11} and M_{12}). When the CLK is high, the master enters sense mode, while the slave stores the value presented from the masters output (when the CLK is low, this is reversed). The input to the devices is shown to be single-ended for simplicity. However, CLK and $\overline{CLK}$ can be considered the differential input from an oscillator. The differential output is the Q

latched outputs at 1/2 the output frequency. A 1/4 frequency design can be realized as a chain of input-to-outputs of two sets of D-latches.

1.5 Project Description

A primary objective of this thesis is the study and comparison of performance issues associated with SiGe and CMOS technologies for an integrated VCO design. Tables 1.4-1.6 show the frequency and voltage specifications for both GSM/EGSM and DCS/PCS standards. All specifications are required to be met for proper integration of the VCO module into both the receiver and transmitter systems. Techniques in the design, simulation, and measurement of the VCO performance will be presented. In addition, a discussion of the design, simulation, and performance of integrated monolithic inductors will also be introduced. This will tie in with an analysis of phase noise, a critical characteristic of VCO performance. Finally, a characterization of SiGe HBT VCOs with tunable polyphase outputs, designed and fabricated under previous research effort, will be presented. It is the author's hope that this thesis will serve as a resource for information on the design and testing of RFIC oscillators and associated components.

1.6 Overview of Thesis

This thesis will study LC-VCO implementations using both SiGe HBT and CMOS technologies. This chapter has introduced the technology options and presented some background on the Motorola CDR1 BiCMOS process used in this work. Also presented are the system-level issues associated with DCR and low-IF receivers. VCO specifications were also estimated to meet the GSM/EGSM and DCS/PCS standards.

The remainder of this thesis fully explains the design, simulation, and measurement of specific VCO implementations. Chapter 2 provides a fundamental background on feedback in oscillating systems and LC oscillator theory. It will also familiarize the

Parameter	Condition	Min.	Typical	Max	Unit
Supply voltage			1.5-2.25		V
VCO gain (Kv)		200		325	MHz/V
850GSM/EGSM side band noise	Δf =3 MHz offset			-128	dBc/Hz
PCS/DCS side band noise	Δf =3 MHz offset			-129	dBc/Hz
Tuning voltage		0		5	V
Minimum frequency (869×4)		3476			MHz
Maximum frequency (1990×2)				3980	MHz

Table 1.4: The GSM/EGSM and PCS/DCS receiver VCO specifications (assuming no dividers) .

Parameter	Condition	Min.	Typical	Max	Unit
Supply voltage			1.5-2.25		V
VCO gain (Kv)		200		325	MHz/V
850GSM/EGSM side band noise	Δf = 400 kHz offset			-116	dBc/Hz
	Δf = 20 MHz offset			-162	dBc/Hz
Tuning voltage		0		5	V
Minimum frequency (824×4)		3296			MHz
Maximum frequency (915×4)				3660	MHz

Table 1.5: The GSM/EGSM transmitter VCO specifications (assuming no dividers).

Parameter	Condition	Min.	Typical	Max	Unit
Supply voltage			1.5-2.25		V
VCO gain (Kv)		200		325	MHz/V
DCS/PCS side band noise	Δf = 400 kHz offset			-114	dBc/Hz
	Δf = 20 MHz offset			-154	dBc/Hz
Tuning voltage		0		5	V
Minimum frequency (1710×2)		3420			MHz
Maximum frequency (1910×2)				3820	MHz

Table 1.6: The DCS/PCS transmitter VCO specifications (assuming no dividers).

reader with the challenges associated with achieving low phase noise in the presence of active devices. Chapter 3 provides a detailed analysis of the design and implementation of integrated VCOs for GSM, and similar types of applications. This will include a complete breakdown of the passive and active device characteristics and modeling. Along with these device characteristics will be an examination of the different VCO topologies considered, and associated performance simulations. Chapter 4 focuses primarily on the characterization, test, and measurements of a SiGe HBT 2x/4x 3-4 GHz VCO. In addition, a comparison between past and newly attempted measurements of a 5-6 GHz VCO with tunable polyphase outputs will be presented. The conclusion to the thesis (Chapter 5) summarizes the results of the research performed and recommends directions for future work.

Chapter 2

Oscillator Design Theory

Oscillations occur in many different natural and man-made systems that exhibit a periodic signal at some particular frequency. For example, such signals are seen in the vibrations of a mechanical spring or the orbiting path of electrons revolving around an atom. This chapter will give an overview of the feedback loop model for oscillators, including an introduction to negative resistance oscillators and various circuit implementations. Finally, a thorough discussion of two modern oscillator phase noise models will be presented.

2.1 Feedback Systems

2.1.1 Oscillator Theory

Oscillator theory can be derived from a control system model. An oscillating electrical network can be viewed as a *positive* linear feedback system [Figure 2.1(a)], which incorporates a gain stage and a feedback loop network. The transfer function of the feedback network in Figure 2.1(a)] is given by:

$$A(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{G(s)}{1 - \beta(s) \cdot G(s)}, \tag{2.1}$$

where $A(s)$ is the closed loop gain, $G(s)$ is the open loop *amplifier* gain, and $\beta(s)$ is the feedback network transfer function. For the specific case of an LC-tuned

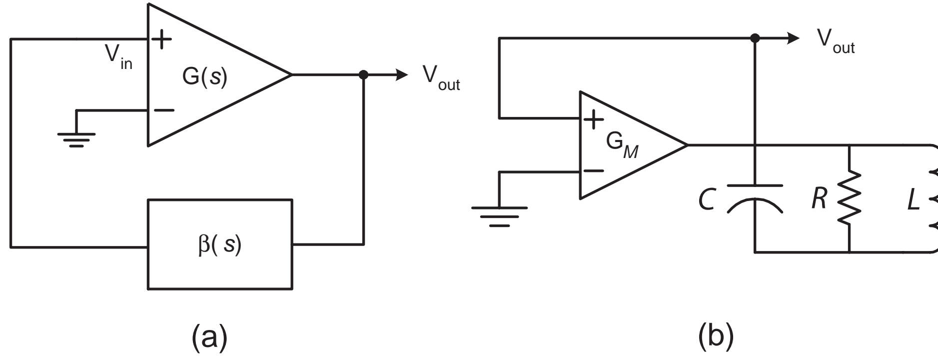


Figure 2.1: LC-tuned oscillators are modeled as feedback networks: (a) control system illustration; (b) specific representation of LC-tuned oscillator.

oscillator, the feedback $\beta(s)$ is replaced by an RLC network, as shown in Figure 2.1(b); the LC network forms a *resonator* that selects the frequency of oscillation. As will be described further below, the parallel R represents the cumulative losses of the resonator. The LC-tuned resonators circuit will essentially amplify noise in the circuit, feed back this amplified noise, and then add it back to the input. Primary sources of noise are contributed primarily by the amplifying active devices (e.g., MOS or Bipolar transistors) and the thermal noise of resistors, a topic that will be discussed further in the next section. The LC feedback network bandpass filters this amplified noise, which tends to force the system into periodic oscillation at the frequency $1/\sqrt{LC}$.

In most typical amplifying systems, such as an RF low-noise amplifier (LNA), positive feedback is avoided. Positive feedback recycles the output signal to the input of the gain stage. On the other hand, negative feedback systems will subtract the output from the input. The following equation represents the differential change of the closed loop gain A with respect to the forward gain G:

$$\frac{dA}{dG} = \frac{d}{dG}\left(\frac{G}{1-\beta\cdot G}\right) = \frac{(1-\beta\cdot G)+\beta\cdot G}{(1-\beta\cdot G)^2} = \frac{1}{(1-\beta\cdot G)^2}. \tag{2.2}$$

Substituting $A/G = 1/(1-\beta G)$ gives:

$$\frac{dA}{dG} = \frac{A}{G}\cdot\left(\frac{1}{1-\beta\cdot G}\right). \tag{2.3}$$

Rearranging this equation gives the relative variation of the closed loop gain as a function of the variation of the forward amplifier gain:

$$\frac{dA}{A} = \frac{\frac{dG}{G}}{(1 - \beta \cdot G)}. \tag{2.4}$$

In other words, a change in the closed loop gain is proportional to a change in the forward gain. Therefore, as the amplifier in the closed loop compresses, dG/G decreases, reducing dA/A, which limits the growth of the oscillation. Compression occurs when the gain approaches zero at sufficiently high input levels. Therefore, during oscillation, the signal does not grow without bound and is limited by this gain compression.

A self-sustaining oscillation requires that two conditions, known as the *Barkhausen criterion* [34], be simultaneously met. A feedback system reaches a stable oscillating condition when the closed loop transfer function $G(s)\beta(s)$ exactly equals one. This also implies that the total phase shift equals zero or $2\pi n$, where n is an integer. In mathematical terms, the Barkhausen criterion can be written as follows:

$$|G(s) \cdot \beta(s)| = 1 \tag{2.5}$$

and

$$\theta_G + \theta_\beta = 0 \text{ or } 2\pi n, \tag{2.6}$$

where the amplifier gain and feedback transfer functions are described by $|G|\angle\theta_G$ and $|\beta|\angle\theta_\beta$, respectively. This criterion also implies that if the amplifier provides a phase shift of 180°, the feedback circuit must provide an additional 180° phase shift to sustain the oscillation. The specific design of the oscillation circuit will determine the characteristics of the oscillating waveform (e.g., sinusoidal, square, or triangular).

As mentioned above, the feedback network $B(s)$ can be replaced with a simple parallel RLC tank circuit. The parallel resistance R represents the overall loss within the tank circuit. In this model, the inductor and capacitor are ideal and have no loss; reactive energy is transferred between these passive devices.

Figure 2.2 shows a simplified model representing the resonator. The circuit is excited by a current source; the energy is then passed back and forth between the voltage potential across the capacitor and the current flow in the inductor. The rate or

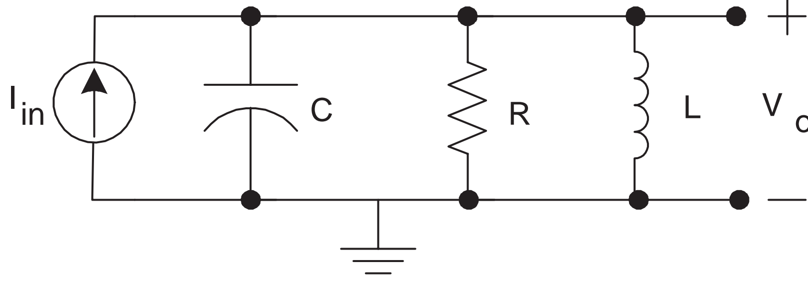


Figure 2.2: Natural RLC resonator mode circuit.

frequency at which this occurs is the resonant frequency. The response of this circuit can be written as RLC network components:

$$Z = \frac{1}{Y} = \frac{V_o}{I_{in}} = \frac{1}{(\frac{1}{R}) + (sC) + (\frac{1}{sL})} = \frac{s\frac{1}{C}}{s^2 + s(\frac{1}{CR}) + (\frac{1}{LC})}. \tag{2.7}$$

The second-order equation can be represented by the pole locations, which determine resonance and quality factor:

$$\frac{\omega_0}{Q} = \frac{1}{CR} \tag{2.8}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{2.9}$$

$$Q = \frac{R}{\omega_o L} = \omega_o RC \tag{2.10}$$

where ω_o is the resonant frequency and Q is the quality factor of the resonator. Therefore, further simplification of equation 2.7 can be written in terms of the quality factor:

$$\frac{V_o}{I_{in} \cdot R} = \frac{s\frac{1}{C}}{s^2 + s(\frac{\omega_o}{Q}) + \omega_o^2}. \tag{2.11}$$

The quality factor is a measure of the energy storage efficiency of the tank circuit, which will be detailed further in Section 2.2.1. Equations 2.7-2.10 describe the fundamental response of the parallel RLC components. Power dissipated in the circuit is a result of losses within the resonator. Real losses may include the parasitic series resistance of the lossy monolithic inductors, substrate image current loss, and RF coupling through the substrate capacitance. To overcome the losses that occur within the feedback loop, an applied energy (or negative resistance) must be introduced.

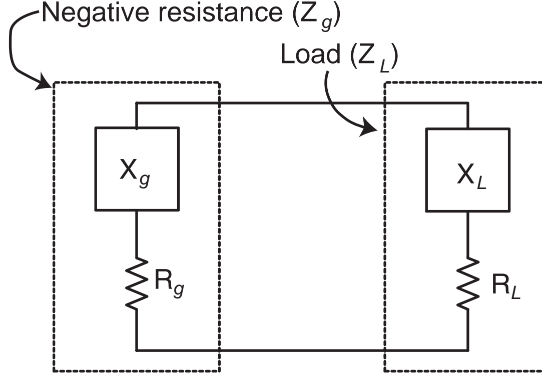


Figure 2.3: Negative resistance model of an oscillator is simplified as the energy supplied to the circuit Z_g and the inherent losses Z_L (after [35]).

2.1.2 -G$_M$ Negative Resistance Structures

As discussed above, energy is inevitably dissipated in an oscillator due to non-ideal (lossy) components in the circuit. Hence, this energy must be replenished to sustain the oscillation. This can be achieved with a negative resistance arising from the transconductance (G_M) of an amplifier. As shown in Figure 2.3, a simplified model of an oscillator circuit can be represented as a generator Z_g coupled to a load Z_L. Initially, at oscillator startup, the negative resistance will be less than the load resistance ($|R_g| < R_L$) causing an energy imbalance. As the oscillation amplitude increases, the amplifier will start to saturate, resulting in a decrease in loop gain until it equals unity (equation 2.5), thereby satisfying Barkhausen criteria. For stable oscillation, the amount of negative resistance will be no less than $|R_g| = R_L$. At equilibrium, the system will remain at the resonant frequency of oscillation where $X_g + X_L = 0$. Hence, the following relationships hold:

$$R_g = -R_L \tag{2.12}$$

$$X_g = -X_L \tag{2.13}$$

A typical method for achieving negative transconductance in RFICs is through cross-coupling of transistors. Figure 2.4(a) illustrates the input impedance seen between the collectors of cross-coupled bipolar transistors $Q_1$and Q_2. Similarly, the input impedance seen between the drains of a cross-coupled NMOS pair is shown in Figure

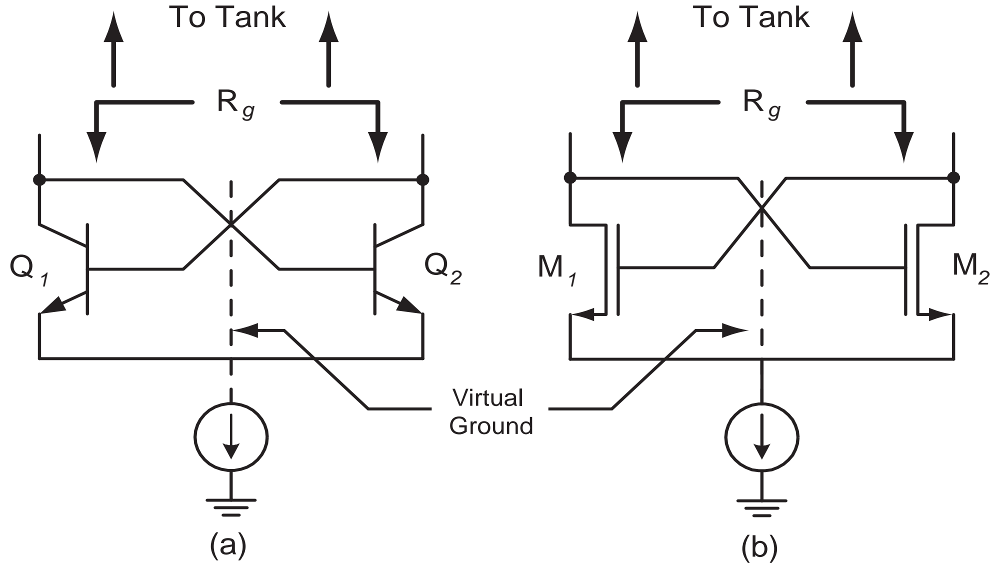


Figure 2.4: Input negative resistence looking into the cross-coupled (a) bipolar and (b) CMOS transistors.

2.4(b). In either case, the cross-coupled pair is connected to a parallel tank circuit and can be used to produce differential outputs. The differential output nodes are located at the drains of the NMOS and emitters of the bipolar, where a virtual ground divides the circuit symmetrically. Differential oscillators are typically required in RFIC transceivers because standard mixers (e.g., Gilbert Cell mixers) have differential LO inputs. Differential circuits also have the advantages of reduced common mode noise and reduced second order distortion introduced by front-end circuit components. Typical RF circuits require the use of differential signals to eliminate common-mode signals.

The general equation for the small-signal transconductance g_m of a bipolar transistor is:

$$g_m = \left.\frac{\partial i_C}{\partial v_{BE}}\right|_{Q-point} = \frac{I_C}{V_T}, \tag{2.14}$$

where the bias *Q-point* is the DC operating point, and the total current $i_C = I_C + i_c$ is equivalent to the DC collector current I_C and small-signal AC component i_c. The transconductance for a BJT is consequently directly proportional to the collector bias current I_C. Similarly, the MOSFET small-signal model transconductance is given

by:

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{Q-Point} = k_n' \left(\frac{W}{L}\right)(V_{GS} - V_t), \tag{2.15}$$

where the Q-point is a DC bias operating point at which the total gate to source voltage v_{GS} is equal to the DC V_{GS} source to gate voltage. W and L describe the MOSFET channel width and length, respectively. The process transconductance parameter k_n' is given by:

$$k_n' = \mu_n \cdot C_{ox}, \tag{2.16}$$

where C_{ox} is the gate oxide capacitance, and μ_n is the effective electron mobility in the channel. The above MOSFET equations assume that there is no body-effect (the bulk substrate is at the same potential as the source). It should be noted that these are long-channel approximations and are relevant for channel lengths $L \geq 1$ μm.

In this design the negative resistance network must be handled carefully. With too little gain, there will not be enough energy to sustain the oscillation, whereas too much gain will result in active devices drawing excess current. This requires careful analysis of the sizing of transistors, which will be discussed further in Chapter 3. In the case of the NMOS implementation, the channel W and L dimensions will determine the value of the transconductance. In addition, because of these dimensions the junction and parasitic capacitances will affect the tuning frequency of the oscillator [36].

2.1.3 Basic LC Topologies

The single transistor oscillator design has become the basis for many oscillator analyses. A basic MOS single transistor LC oscillator is illustrated in Figure 2.5(a). A key issue in such an oscillator design is the need to avoid excessive loading of the tank circuit, which can result in insufficient negative resistance to sustain the oscillation. To maintain oscillation, the transistor source (emitter) input impedance must be transformed to a higher value before the signal is fed into the tank circuit. Therefore, oscillator topologies are implemented with either a passive or active impedance transformation.

The Colpitts and Hartley topologies are based on passive impedance transformation networks. The parallel resistance R represents the collective losses within the inductors and other passive devices. For example, the Colpitts [Figure 2.5(b)] oscillator

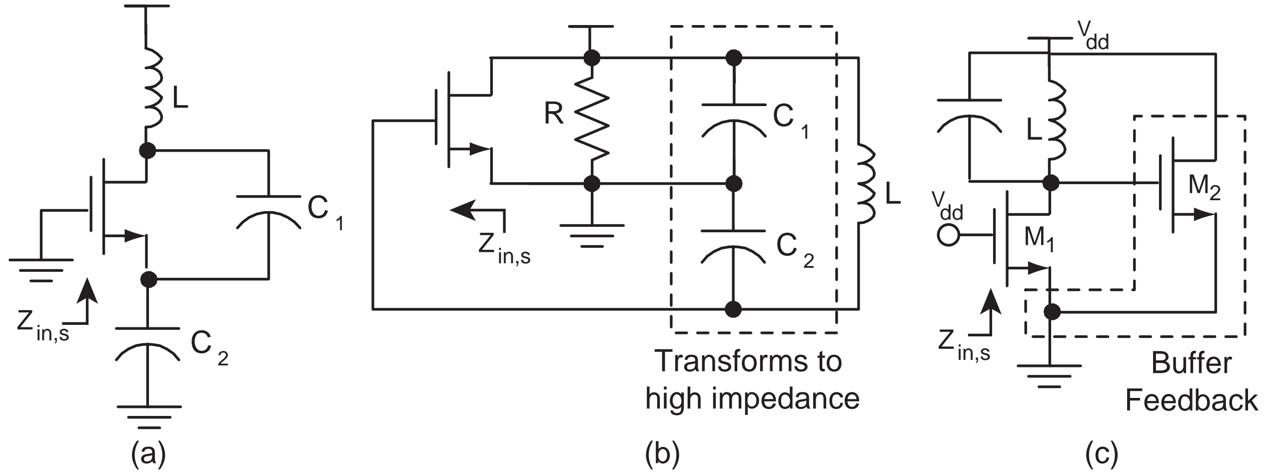


Figure 2.5: (a) A simple LC resonator oscillator with no impedance tranformation presented to the source. (b) A Colpitts oscillator uses a capacitive divider to provide an impedance transformation of the source impedence to prevent loading of the tank. (c) An implementation of a source follower buffer transistor M_2 transforms the source of transistor M_1 to a higher impedance.

relies on a capacitive divider in the feedback network to provide the required impedance transformation. (The Hartley uses inductive dividers, but is not presented here). Given that the input impedance loading into the source is $\sim 1/G_M$, the capacitors C_1 and C_2 transform the source input impedance into an equivalent parallel resistance given by:

$$R_p = \frac{\left(1 + \frac{C_2}{C_2}\right)^2}{g_m}. \tag{2.17}$$

The goal is to select the capacitor ratio C_1/C_2 such that R_p is large enough not to load down the tank. The resonant frequency for the Colpitts oscillator is found to be:

$$\omega_o = \frac{1}{\sqrt{L\left(\frac{C_1 C_2}{C_1 + C_2}\right)}}. \tag{2.18}$$

The analysis of single transistor oscillator circuits and the resulting equations are well documented in a number of references [37] [35] [23].

The drawback of the Colpitts or Hartley topologies is that they may require large capacitors or inductors to realize the desired resonant frequencies. Such passives may consume a large amount of die area and may introduce additional parasitics.

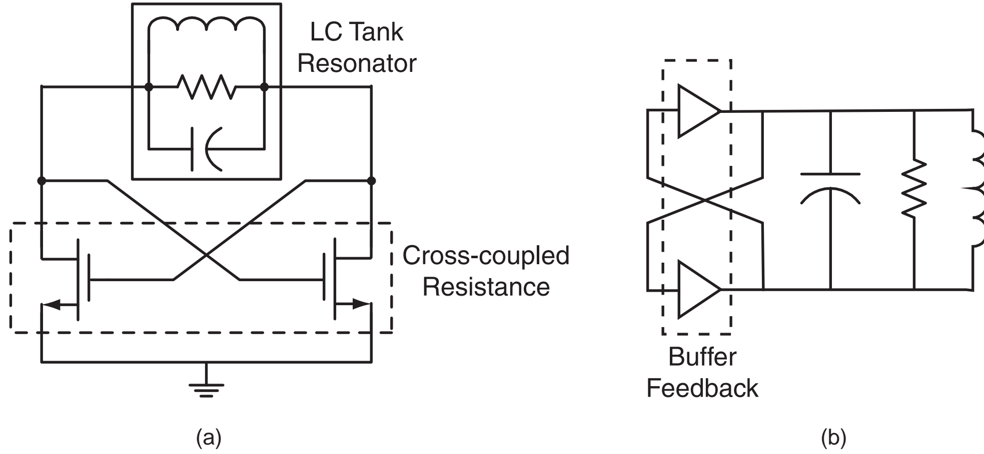


Figure 2.6: (a) Negative resistance is provided by the positive feedback of the cross-coupled NMOS transistors. (b) This can be viewed as two source-follower buffers cross-coupled in parallel with an LC tank circuit.

These trade-offs may ultimately limit the application of these types of oscillators for integrated oscillations at higher frequencies. Therefore, instead of using passive impedance transformation circuits, active buffers may be employed. Figure 2.5(c) shows an oscillator circuit with a buffer in the feedback loop implemented as a source (emitter) follower.

Another issue with the Hartley or Colpitts oscillator is that they are single-ended designs. As mentioned above, differential outputs are typically required in RFIC transceivers. On the other hand, the cross-coupled oscillator topology provides differential output signals. A cross-coupled oscillator can be thought of as an individual source-follower buffer transistor output providing positive feedback input to another source-follower buffer [Figure 2.6(a)(b)].

Consider the high-frequency, cross-coupled NMOS equivalent circuit shown in Figure 2.7(a). The output differential voltages (V_- and V_+) are ideally 180° out of phase (i.e., $V_- = -|V_+|$). A simplified model without parasitics is shown in Figure 2.7(b). Applying a test voltage V_x to the circuit, the equation of equivalent negative resistance can be computed as follows:

$$R_g = \frac{V_x}{I_x} = \frac{V_+ - (V_-)}{G_M(V_-)} = \frac{2 \cdot V_+}{G_M(-V_+)} = -\frac{2}{G_M}. \tag{2.19}$$

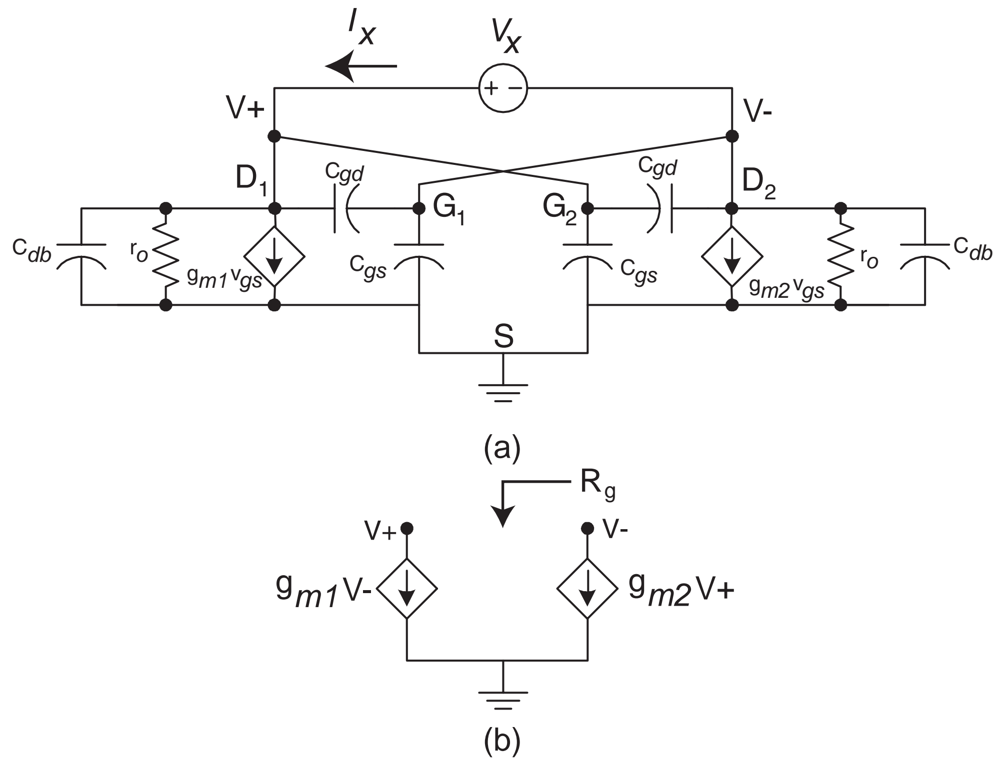


Figure 2.7: (a) High-frequency small-signal model with the applied test voltage V_x and test current I_x. (b) Simplified model of the NMOS cross-coupled network.

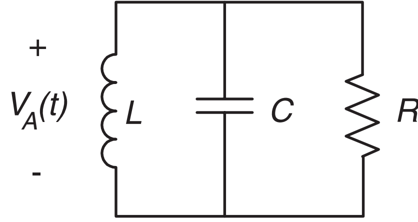


Figure 2.8: Schematic of an RLC excited with a sinusoidal waveform $V(t)$ with a peak amplitude of V_A.

As can be seen, the R_g is a function of the large-signal transconductance G_M, which is a function of the bias current.

2.2 Stability and Noise in LC Oscillators

This section introduces frequency stability and its relationship to the tank quality factor Q. The tank Q has a major impact on phase noise performance. An overview of the primary contributors to oscillator phase noise, such as thermal, $1/f$ (flicker) and shot noise, will also be addressed.

2.2.1 Quality Factor

The quality factor, Q, of the oscillator tank circuit is a major design parameter in determining oscillator performance. Three definitions and interpretations of Q will be presented here. First, the quality factor is generally defined as:

$$Q = 2\pi \cdot \frac{\text{Average energy stored}}{\text{Energy loss (dissipated) per cycle}} = 2\pi \cdot \frac{E_{stored}}{E_{loss}}. \tag{2.20}$$

In an LC tank circuit, Q is a measure of the average energy that is lost as it is transferred back and forth between the capacitor and the inductor. For example, suppose a sinusoidal voltage $V(t) = V_A \cdot \sin(\omega t)$, where V_A is the peak amplitude of the sinusoidal signal applied to a parallel RLC tank (Figure 2.8). The maximum amount of stored energy across the capacitor and inductor can be derived from the

conservation of energy, as follows:

$$E_{store} = \frac{C \cdot V_A^2}{2} = \frac{L \cdot I_A^2}{2}. \tag{2.21}$$

Meanwhile, the amount of average energy lost per cycle due to the equivalent parallel resistance of the tank (R) is represented by:

$$E_{loss} = \int_0^{\frac{2\pi}{\omega_o}} \frac{[V_A \sin(\omega_o t)]}{R} dt = \frac{\pi \cdot V_A^2}{\omega_o \cdot R}. \tag{2.22}$$

Substituting 2.21 and 2.22 in equation 2.20 gives the following:

$$Q = 2\pi \cdot \frac{\frac{C \cdot V_A^2}{2}}{\frac{\pi \cdot V_A^2}{\omega_o \cdot R}} = R \cdot \omega_o C. \tag{2.23}$$

or alternatively:

$$Q = 2\pi \cdot \frac{\frac{L \cdot I_A^2}{2}}{\frac{\pi \cdot V_A^2}{\omega_o \cdot R}} = \frac{R}{\omega_o L} \tag{2.24}$$

Combining equations 2.9 and 2.23 yields:

$$Q = R \cdot \sqrt{\frac{C}{L}} \tag{2.25}$$

A second definition of Q is based on the fact that a closed-loop system will oppose any derivations from the resonant frequency. Frequency stability is a critical attribute within a functional oscillator system because of the implications on phase noise performance (discussed in Section 2.2.3). Recall that the total phase shift around the loop must be zero to satisfy the Barkhausen criteria. If an oscillator deviates from its resonant frequency ω_o, a large resulting phase change will force the oscillation back to the correct frequency. Hence, the phase change relative to the change in frequency must remain large to maintain the frequency of oscillation at ω_o:

$$\left| \frac{d\phi}{d\omega_o} \right| \gg 0. \tag{2.26}$$

The LC tank can be viewed simply as an open-loop transfer function contributing

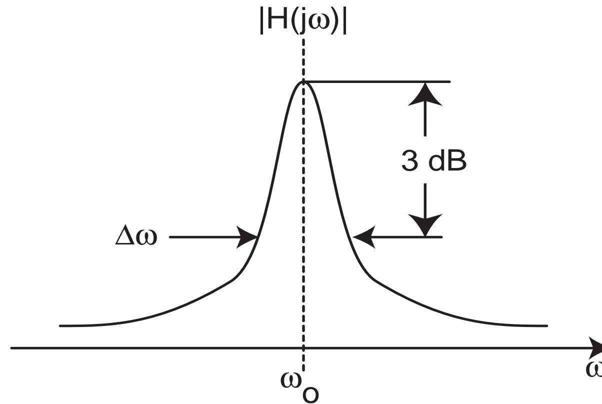


Figure 2.9: Definition of the Q factor based on the transfer function of a resonant circuit.

some phase shift. Q can also be defined as the "open-loop Q" [23], which is a measure of how much the closed-loop system is compensated by the open-loop transfer function. Therefore, the open-loop Q is defined as:

$$Q = \frac{\omega_o}{2}\left|\frac{d\phi}{d\omega}\right|. \tag{2.27}$$

The quality factor of the system is a function of the deviation of phase with respect to a change in frequency. In other words, if $\left|\frac{d\phi}{d\omega_o}\right|$ is very large and a slight frequency shift from ω_o occurs, the system will force a large phase shift to bring the oscillation back to ω_o.

The final definition of Q is given in terms of the 3 dB return loss bandwidth of the input impedance of an RLC tank. Figure 2.9 illustrates the one-port transfer response of a simple parallel RLC tank; the Q value can be calculated using the following equation:

$$Q = \frac{\omega_o}{\Delta\omega_{-3dB}}. \tag{2.28}$$

Therefore, designing a tank circuit for minimal loss reduces its bandwidth (i.e., makes it more frequency selective), which results in a signal that does not spill over as much into adjacent channels.

2.2.2 Noise Elements

This section outlines important device noise sources that are relevant in integrated LC oscillators.

Thermal Noise

One of the most pervasive noise sources in electronic circuits is the thermal noise generated by resistive elements [38]. This may arise from specific resistances embedded in the circuit design or from parasitic resistances in active (e.g., transistors) and passive (e.g., capacitors and inductors) devices. Within any resistive element, electrons experience random uncorrelated thermal agitation (Brownian motion). Thus, this phenomenon is referred to as thermal noise, and is expressed as the mean-square Thevenin equivalent RMS voltage:

$$\overline{v_{n,T}^2} = 4kTR \triangle f \tag{2.29}$$

where k is the Boltzmann's constant (1.38×10^{-23} Joules/Kelvins), T is absolute temperature (Kelvins), and $\triangle f$ is the "brick wall" bandwidth (Hz). $\triangle f$ can be normalized out to give the noise power within a 1 Hz bandwidth, also known as "spot" noise. 1-kΩ and 50 Ω resistors at room temperature produce 4 nV and 0.9 nV of rms noise per 1 Hz bandwidth, respectively. Note that the spectral density of this noise can be expressed as nV/$\sqrt{\text{Hz}}$, or as a mean-square noise density in V^2/Hz (for example, the 1-kΩ resistor gives 4 nV/$\sqrt{\text{Hz}}$ or 1.6 V^2/Hz [39]). A thermal noise source can also be represented as a Norton equivalent current source [Figure 2.10(b)]:

$$\overline{i_{n,T}^2} = \frac{\overline{v_{n,T}^2}}{R^2} = \frac{4kT \triangle f}{R} = 4kGT \triangle f \tag{2.30}$$

where $G = 1/R$. The amplitude of this noise is determined by the resistance value, and has a "white" spectral density (magnitude vs. frequency). Therefore, minimizing parasitic resistances in a circuit can help reduce this noise contribution. In addition, thermal noise is also proportional to the temperature; therefore keeping

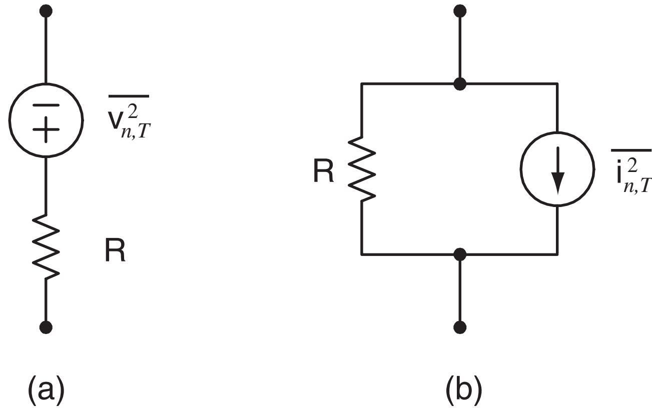


Figure 2.10: Thermal noise models of a resistor: (a) Thevenin equivalent mean-square voltage source, and (b) Norton equivalent mean-square current source.

circuit temperatures as low as possible will reduce this noise contribution[1].

Thermal noise is a dominant factor in MOSFET devices, and is also a contributor in HBTs. In MOSFETs, thermal noise arises from the resistance at the gate-channel region. Likewise, thermal noise due to resistivity within the HBT is primarily focused at the base region. Long-channel MOS devices operating in the saturation region can be expressed as the drain current noise:

$$\overline{i^2_{nd}} = 4kT\gamma g_{d0} \triangle f \tag{2.31}$$

where γ is equal to 1 (unity) when V_{DS} is zero, and g_{d0} is the transconductance of the device in saturation. However, *for long-channel devices, γ decreases to 2/3 when operating in saturation*.

In addition, short-channel NMOS devices exhibit far more noise than PMOS devices in saturation. PMOS devices inherently have much lower γ compared to NMOS devices of a similar size. Many other factors lead to a higher γ within the short-channel regime; this has been reported in [40]. For example, it has been shown that in the short-channel regime, an increase in drain-source voltage causes γ to increase. This is because scaling down the channel causes a higher drift-field in the channel region.

[1]For this reason, ultra low-noise amplifiers, such as equipment used in radio astronomy, are cryogenically cooled.

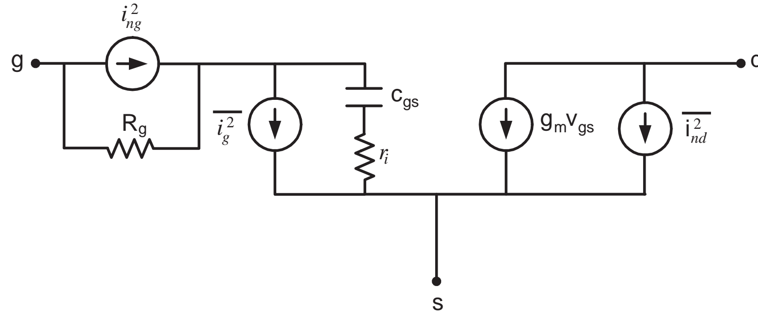


Figure 2.11: Simplified MOSFET model with both the thermal noise within the gate resistance $\overline{i_{ng}^2}$ and induced gate noise within the channel $\overline{i_g^2}$.

Two intrinsic noise sources have an influence at the gate: gate resistance noise, and "gate induced" thermal noise (Figure 2.11). Gate resistance noise $\overline{i_{ng}^2}$ is the thermal noise generated within the resistance of the gate R_g. This noise can be expressed as a Norton current source [41]:

$$\overline{i_{ng}^2} = 4kTR_g \triangle f, \tag{2.32}$$

where R_g is the intrinsic gate resistance, which is given by:

$$R_g = \frac{R_{g,sq}}{3}\frac{W}{L}, \tag{2.33}$$

where $R_{g,sq}$ is the sheet resistance of a single finger gate material, the channel width is W and length is L. The induced gate noise $\overline{i_g^2}$ is derived from the diffusion noise generated in the channel and capacitively couples itself into the gate. Channel noise and gate-induced noise are both correlated, because they both originate from the same physical noise source. The induced gate noise requires a nonquasistatic parameter that has intrinsic channel charge resistance across the channel. This is proportional to the transconductance of the gate $1/g_m$, which gives the parameter:

$$r_i = \frac{1}{5g_m}. \tag{2.34}$$

The parameter r_i accounts for the electrons at any particular point within the MOSFET channel, which is modeled as a resistive element that is capacitively coupled to the gate C_{gs}.

HBTs, on the other hand, are prone to thermal noise from the base resistance (Figure

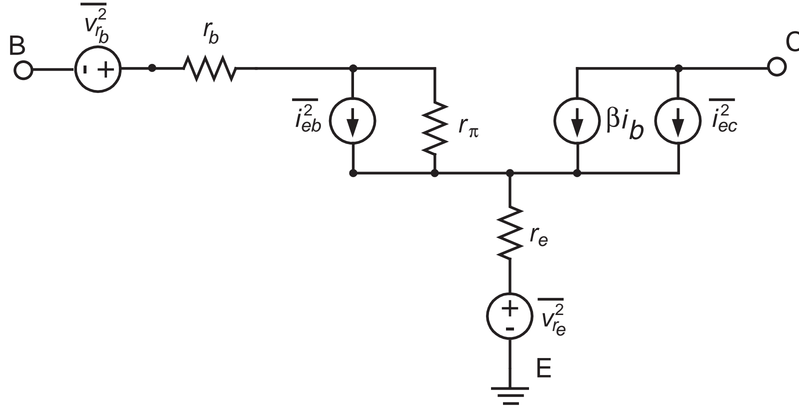


Figure 2.12: Low frequency noise model of a bipolar common-emitter configuration [42].

2.12). Although the SiGe profile discussed in Section 1.1.1 improves base transit time by the bandgap narrowing along the base region, it has a very low base-doping level. Due to the lack of doping, there is a decrease in resistance within the base r_b. The base thermal noise can be expressed as:

$$\overline{i_{r_b}^2} = 4kTr_b\triangle f.$$

The total base resistance r_b includes both intrinsic and extrinsic resistances.

$1/f$ (Flicker) Noise

A natural phenomenon that occurs in semiconductor devices (and even in other systems outside of electrical engineering) is $1/f$ or flicker noise. As the mathematical representation of flicker noise suggests, the noise spectral density increases as frequency decreases. The rms noise can be expressed as:

$$\overline{N^2} = \frac{K}{f^n}\triangle f, \tag{2.35}$$

where n is an exponent that is usually close to unity, and the empirical parameter K is device-specific and generally bias-dependent.

Noise in resistors is dominated by thermal noise, as shown in the previous section.

However, resistors can also exhibit $1/f$ noise, which can be given by:

$$\overline{v_n^2} = \frac{K}{f} \cdot \frac{R_\square^2}{A} \cdot V^2 \triangle f, \tag{2.36}$$

where $\mathrm{R}_\square^2$ is the sheet resistivity of an integrated resistor with an area of A, and V is the voltage applied across the resistor.

It has been shown that MOSFETs suffer significantly larger amounts of $1/f$ noise in comparison to bipolar devices [39]. In Section 2.2.3, the influence of $1/f$ noise and upconverted $1/f$ noise on the phase noise spectrum will be discussed. A major cause of $1/f$ noise is believed to be charge trapping. MOSFETs are horizontal devices that experience induced charge trapping caused by defects at the gate-oxide-silicon surface interface of the device. These surface defects may be caused by impurities introduced during the fabrication process of these devices. On the other hand, HBTs are vertical device structures that do not suffer as much from these charge-trapping effects. In other words, because MOSFETS are horizontal devices, the charge transport is primarily along the interface, allowing for more possibilities of trapping. In contrast, in an HBT device the transport is largely perpendicular to the interface, therefore limiting the trapping effects.

Typical bipolar devices are still not entirely immune to flicker noise. The forward-biased emitter-base junction of a bipolar transistor in the active region can contribute $1/f$ noise. This noise is proportional to the noise parameter K and is given by:

$$\overline{i_j^2} = \frac{K}{f} \cdot \frac{I}{A_j} \cdot \triangle f, \tag{2.37}$$

where A_j is the junction area; increasing A_j will reduce this noise contribution. In the HBT model, illustrated in figure 2.12, the following $1/f$ spectral densities exist [42]:

$$\overline{i_{eb}^2} = \frac{K_{eb} \cdot I_b^2}{A_e f}, \tag{2.38}$$

$$\overline{i_{cb}^2} = \frac{K_{cb} \cdot I_b^2}{A_e f}, \tag{2.39}$$

and

$$\overline{v_{r_e}^2} = I_e^2 \cdot \frac{K_{r_e} \cdot r_e^2}{A_e f}. \tag{2.40}$$

Note that K_{eb}, K_{eb}, and $K_{r_e}$are all noise parameters, and are specific for a given process. Example analysis and noise parameters are demonstrated in [42][43][44]. The $1/f$ noise spectral density of r_e is the contributed noise from the extrinsic emitter resistance.

Shot Noise

Shot noise exists in devices where electrons must overcome an energy barrier. For example, devices with *pn*-junctions are susceptible to this noise source. A DC bias current flow is required for shot noise to exist in a *pn*-junction. In a bipolar device, shot noise exists mainly at the base/collector *pn*-junction. The expression for shot noise in both the base and collector of a bipolar device is expressed as:

$$\overline{i_b^2} = 2qI_b \triangle f \quad \text{or} \quad \overline{i_c^2} = 2qI_c \triangle f \tag{2.41}$$

where q is the electronic charge (approximately 1.6×10^{-19} C) within the $\triangle f$ noise bandwidth. On the other hand, MOSFETs may exhibit shot noise at the gate. This is caused by DC gate leakage; the equation is expressed as [42]:

$$\overline{i_g^2} = 2qI_G \triangle f \tag{2.42}$$

The randomized arrival times of electrons hopping the energy barrier give shot noise a “white” spectrum.

2.2.3 Introduction to Phase Noise

The goal of a typical RF oscillator design is to produce a spectrally pure sinusoidal waveform (vs. square or triangular waves) with a minimum amount of phase noise. There has been a significant amount of research in the area of phase noise; contributors such as Leeson [45], and Hajimiri and Lee [46], have all had major impacts on the understanding of phase noise within RF oscillators.

To understand phase noise, it is useful to examine the characteristics of an ideal

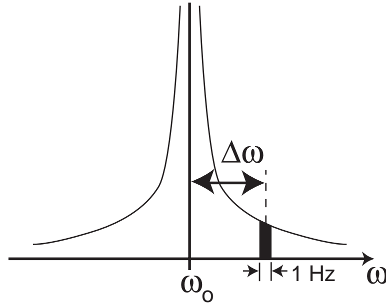


Figure 2.13: Oscillator phase noise.spectrum with a specific offset frequency $\Delta\omega$.

signal. An ideal oscillator signal can be expressed in the time domain:

$$V_{ideal} = A(t) \cdot \sin(\omega_o t + \theta(t)) \tag{2.43}$$

where $A(t)$ is the peak amplitude, w_o is the center frequency, and $\theta(t)$ is an arbitrary phase shift. Phase noise is typically described in the frequency domain. In the frequency domain, an ideal sinusoidal oscillation would appear as a Dirac impulse function at the resonant frequency. The definition of phase noise is the relative noise power in a unit bandwidth at some *offset frequency* ($\Delta\omega$) from the carrier relative to the carrier power (Figure 2.13). Therefore, a general definition for single-sideband phase noise[2] in dB is:

$$£\{\Delta\omega\} = 10{\cdot}\log\left(\frac{\text{noise power within 1 Hz unit bandwidth at frequency } \omega_o + \Delta\omega}{\text{carrier power}}\right). \tag{2.44}$$

The units of $£\{\Delta\omega\}$ are decibels relative to the carrier per Hertz (dBc/Hz).

To understand the impact of a local oscillator phase-noise spectrum consider the downconversion of a single desired RF tone. Figure 2.14(a) depicts an unwanted signal adjacent to the desired channel of interest. An LO signal with some phase noise is convolved with both tones [Figure 2.14(b)]. The final downconverted spectrum will consist of overlapping spectra of both the desired signal and the interferer with superimposed LO phase noise, which can cause significant degradation of the wanted signal [Figure 2.14(c)]. This effect is called "reciprocal mixing" [47] and can occur in any type of communications system.

[2] The £ notation is in recognition of D. B. Leeson for his pioneering work on phase noise.

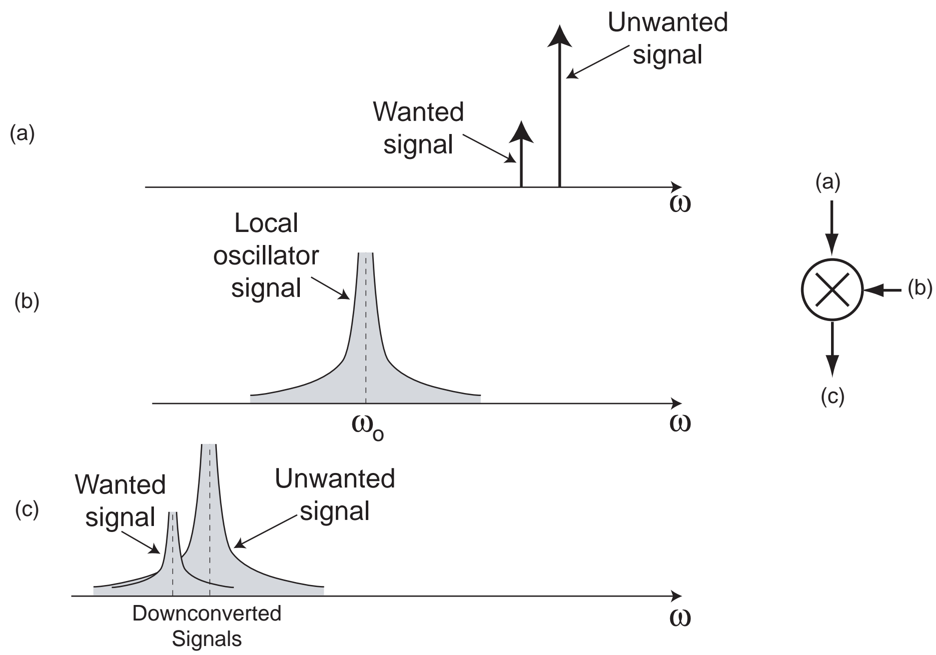


Figure 2.14: Downconversion of wanted and unwanted signals with an LO with realistic phase noise spectrum (after [23]). The wanted and unwanted signals are convolved with the LO to produce an overlapping spectra $(a) * (b) = (c)$.

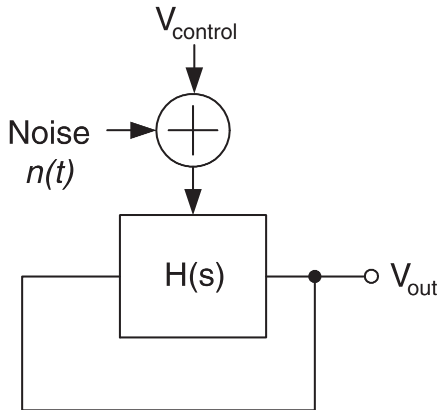


Figure 2.15: A simplified representation for producing phase noise within a VCO system by means of the frequency control path (after [23]).

There are two primary mechanisms through which phase noise can be generated within a VCO [23]: noise injected via the frequency control path; and noise injected directly into the feedback loop. These two mechanisms will be discussed in the following sections.

2.2.4 Phase Noise: Frequency Control Path

Noise can be injected into the frequency control path as represented in Figure 2.15. The control path is the variable DC input (typically a voltage) to the frequency tuning element in the VCO (typically a varactor). A changing control voltage results in a change in resonant frequency. This control voltage is often the feedback signal in a phase-lock loop (PLL). Noise that is injected into this path can be viewed as a form of frequency modulation (FM) in the oscillator output.

Introduction to Frequency Modulation

FM is fundamentally the frequency of the carrier signal that is proportional to the amplitude variation of IF information. Noise can be observed as a discrete single harmonic n that is modulated onto the carrier, and the carrier is simply the tuned oscillator resonance.

In the frequency control path phase noise mechanism, the RF instantaneous frequency $f_i(t)$ is varied by the injected noise $n(t)$. The instantaneous frequency is defined as:

$$f_i(t) = \frac{1}{2\pi} \cdot \frac{d\theta_i(t)}{dt} = f_c + k_f n(t), \tag{2.45}$$

where k_f is the *frequency sensitivity,* and $d\theta_i(t)/dt$ is the rate of change of the phase measured in radians per second. For simplicity, the injected noise is assumed to be a constant amplitude sine function representing a discrete noise harmonic:

$$n(t) = A_n \cdot \cos(2\pi f_n t). \tag{2.46}$$

In actuality, $n(t)$ will be represented as an independently random Gaussian distribution over time. Combining equations 2.45 and 2.46 gives the following resulting *instantaneous frequency* equation:

$$f_i(t) = f_c + \triangle f \cdot \cos(2\pi f_n t), \tag{2.47}$$

where

$$\triangle f = k_f A_n. \tag{2.48}$$

$\triangle f$ is the frequency deviation of the FM signal from the carrier. This deviation value is directly proportional to the amplitude of the noise signal A_n. The *instantaneous angle* of an FM signal is expressed as:

$$\theta_i(t) = 2\pi \int_o^t f_i(\tau) d\tau = 2\pi f_c t + \frac{\triangle f}{f_n} \sin(2\pi f_n t), \tag{2.49}$$

where the FM *modulation index* is

$$\beta = \frac{\triangle f}{f_n}. \tag{2.50}$$

The final FM signal expression is:

$$N_{FM}(t) = A_c \cdot \cos\left[2\pi f_c t + \beta \sin(2\pi f_n t)\right] \tag{2.51}$$

where the carrier amplitude A_c and frequency f_c are constant. For a *narrowband FM* signal, the modulation index β is very small compared to 1 radian ($\beta \ll 1$). The

narrowband $N_{NBFM}(t)$ approximation is given by [48]:

$$N_{NBFM}(t) \approx A_c \cos(2\pi f_c t) - \beta A_c \sin(2\pi f_c t)\sin(2\pi f_n t) \tag{2.52}$$

In contrast, the $\beta \gg 1$ radian is considered to be *wideband FM*, and the approximation in Equation 2.52 will no longer hold.

Modulation Due to Noise

As mentioned above, noise that is injected into the frequency control path can be considered a form of FM modulation. This can be viewed as low-frequency noise components being upconverted to a region around the carrier [Figure 2.16(a)]. In other words, the noise spectrum can be discretized into component frequencies ω_n, where each component is approximated as a sinusoid with the same average power ($V_n \cos \omega_n t$) for white noise. For simplicity, consider one discrete low-frequency noise component at some frequency $\pm\omega_n$, thus the narrow-band approximation (equation 2.52) gives rise to [47]:

$$V_{out} \approx A_c \cos(2\pi f_c t) + \frac{A_c V_n K_{VCO}}{2 \cdot 2\pi f_n}\left[\cos(2\pi f_c + 2\pi f_n)t - \cos(2\pi f_c - 2\pi f_n)t\right] \tag{2.53}$$

where the noise amplitude V_n and unit bandwidth frequency f_n are constant. The gain of the VCO, K_{VCO}, is the frequency tuning versus control voltage slope. The noise power at $\omega_c \pm \omega_n$ with respect to the resonant power at some frequency f_c is therefore approximately equal to $(K_{VCO}/2\pi f_n)^2 V_n^2/4$.

The phenomenon of FM noise, described above in the context of noise in the VCO control path, can also be caused in principle by, for example, mechanical vibrations in a discrete inductor. Additionally, such noise may become larger as offset frequency decreases. A major source of low-frequency noise is $1/f$ or flicker noise (see Section 2.2.2), which may be harmful if injected into the control path. Careful attention to the design and implementation of active devices can help minimize these issues.

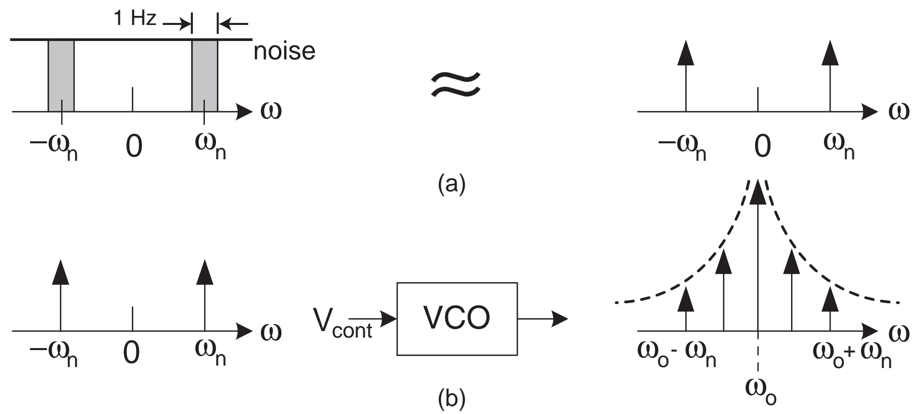


Figure 2.16: (a) Noise can be approximated as a spectrum of sinusoids. (b) The modulation of the noise in the control single line is shown as discrete components that make up the phase noise spectrum.

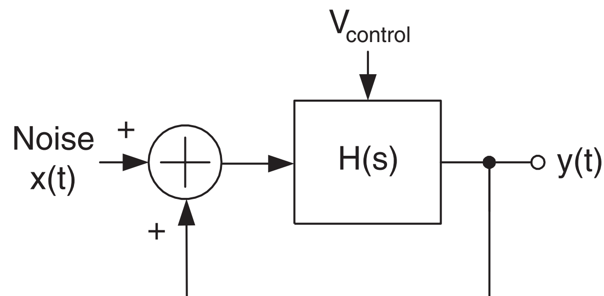


Figure 2.17: A simplified representation of noise injection into the signal path of a VCO system (after [23]).

2.2.5 Phase Noise: Signal Path

Noise can also be injected directly into the oscillator feedback loop, as shown in Figure 2.17. This feedback circuit is analyzed in [47], yielding the following noise shaping function:

$$\left|\frac{Y}{X}\left[j(\omega_o + \omega_\triangle)\right]\right|^2 = |Z|^2 = \frac{1}{4Q^2}\left(\frac{\omega_o}{\omega_\triangle}\right)^2 = \left(\frac{\omega_o}{2Q\omega_\triangle}\right)^2, \tag{2.54}$$

where ω_o is the carrier frequency, Q is the quality, and $\omega_\triangle$ is the offset frequency relative to the carrier. This expression forms the basis of Leeson's phase noise equation (to be discussed in the following subsection). As can be seen, a higher tank quality factor will result in a lower noise shaping spectrum. Within a linear feedback circuit, the active devices of the oscillator inherently inject noise into the signal path. Another important fact arises from this analysis—an increase in Q means less loss (smaller parallel equivalent resistance), requiring less power dissipation for negative resistance compensation. Therefore, extensive research and development is ongoing to increase the Q of inductor tanks in RFIC VCO by modifying the structure of the monolithic inductor designs.

Leeson's Linear Time Invariant (LTI) Approach

This section provides an introduction to Leeson's classical phase noise theory first presented in 1965. Since then, other researchers have based their studies on this analysis to formulate new approaches to predicting phase noise. Leeson was the first to accurately describe the phase noise phenomenon in positive feedback oscillators using LTI analysis.

Leeson's equation is a first approximation to phase noise, containing an ideal oscillator with the loss of the tank as the only noise contribution. Recall that the thermal noise of a resistor is represented by equation 2.29. Multiplying the mean-square noise voltage by the squared magnitude of the tank impedance (Z) gives the spectral density of the mean-square noise voltage as:

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{\overline{i_n^2}}{\Delta f} \cdot |Z|^2 = 4kTR\left(\frac{\omega_o}{2Q\omega_\triangle}\right)^2. \tag{2.55}$$

Note that an increase in tank Q reduces the noise density because of the resonator

loss. Now, a "noise-to-signal ratio" can be derived as follows:

$$\frac{N}{S} = \frac{\overline{v_n^2}}{\overline{v_{sig}^2}} = \frac{kT}{E_{store}} = \frac{2\pi kT}{QE_{loss}}, \tag{2.56}$$

where v_{sig}^2 is the root mean square voltage of the signal, which is presented in this format because it parallels the format of the fundamental definition of phase noise (noise over carrier power). The mean-square carrier power P_{sig} is equivalent to the mean-square voltage times the equivalent loss within the RLC tank $(\overline{v_{sig}^2} \cdot R)$. Therefore, by normalizing mean-square noise voltage density (Equation 2.55) by the mean-square carrier power yields the following single-sideband noise spectral density:

$$\pounds(\omega_\Delta) = 10 \log \left[\frac{2kT}{P_{sig}} \left(\frac{\omega_o}{2Q\omega_\Delta} \right)^2 \right]. \tag{2.57}$$

The equation 2.57 illuminates important issues concerning the RLC tank in an ideal oscillator. First, improving resonator Q is critical to low phase noise design. Second, increasing carrier power (signal power) will also decrease phase noise. This equation, graphically speaking, represents the $1/f^2$ region of the phase noise spectrum. The $1/f^2$ region of the phase noise "skirt" will theoretically have a slope of -20 dB/dec.

As mentioned above, equation 2.57 was derived based on an ideal oscillator with only the tank loss contributing noise. However, there is also additive noise from the active device(s) that provide the negative resistance in the oscillator circuit. Therefore, a modified equation known as the Leeson-Cutler phase noise model [49] was developed to account for the $1/f$ and thermal noise contributions from the active devices:

$$L\{\omega_\Delta\} = 10 \cdot \log \left\{ \frac{2FkT}{P_{sig}} \cdot \left[1 + \left(\frac{\omega_o}{2Q\omega_\Delta} \right)^2 \right] \cdot \left[1 + \frac{\omega_{\Delta_{1/f^3}}}{|\omega_\Delta|} \right] \right\}. \tag{2.58}$$

The most important feature of this equation is that empirical fitting parameters, F and $\omega_{\Delta_{1/f^3}}$, are now employed. F is the device noise factor, k is the Boltzmann's constant, T is the temperature. The parameters $\omega_{\Delta_{1/f^3}}$ is the approximated frequency offset where the $1/f$ is the noise corner frequency. Region 1 is the thermal noise floor that arises because of both the active devices as well as the resistive loss of the RLC tank and is expressed as $10 \log (2FkT/P_{sig})$ dB/Hz. Region 2 has the -20

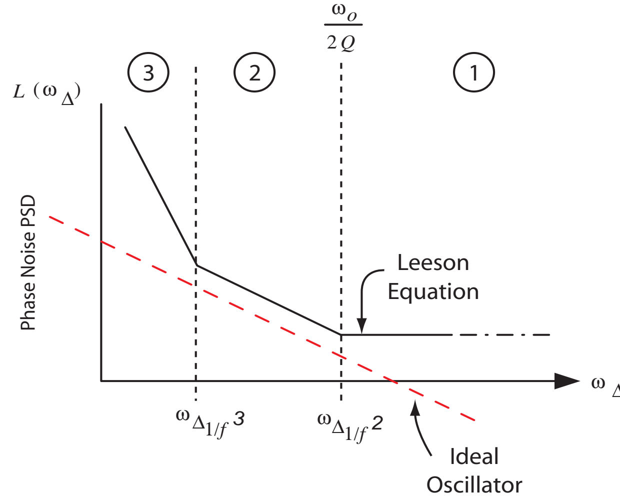


Figure 2.18: Oscillator phase noise spectrum.

dB/decade slope described by the original Leeson equation; however, it is shifted up due to active noise sources accounted for by F. This characteristic flattens off into Region 1 around the resonator 3dB bandwidth, $\omega_o/2Q$. Finally, Region 3 begins at the corner frequency $\omega_{\Delta_{1/f^3}}$, which is also an *a posteriori* parameter that is related to the $1/f$ corner of device noise.

This model clearly relies heavily on fitting parameters. However, the Leeson equation does provide some insight into the physical behavior of phase noise. First, increasing the power of the oscillating signal will reduce phase noise, which may be accomplished by increasing a voltage swing or providing more current. Second, reducing $1/f$ noise contribution can limit the close-in phase noise. Third, the quality factor Q has a major impact on phase noise as well; increasing the resonator Q value will result in improved phase noise.

However, this linear time invariant approach only applies to linear steady-state LC oscillators, which is not really the case for most practical oscillators. However, Leeson's equation does provide a very useful framework for designers to make estimations of phase noise, given some basic knowledge of the physical circuit.

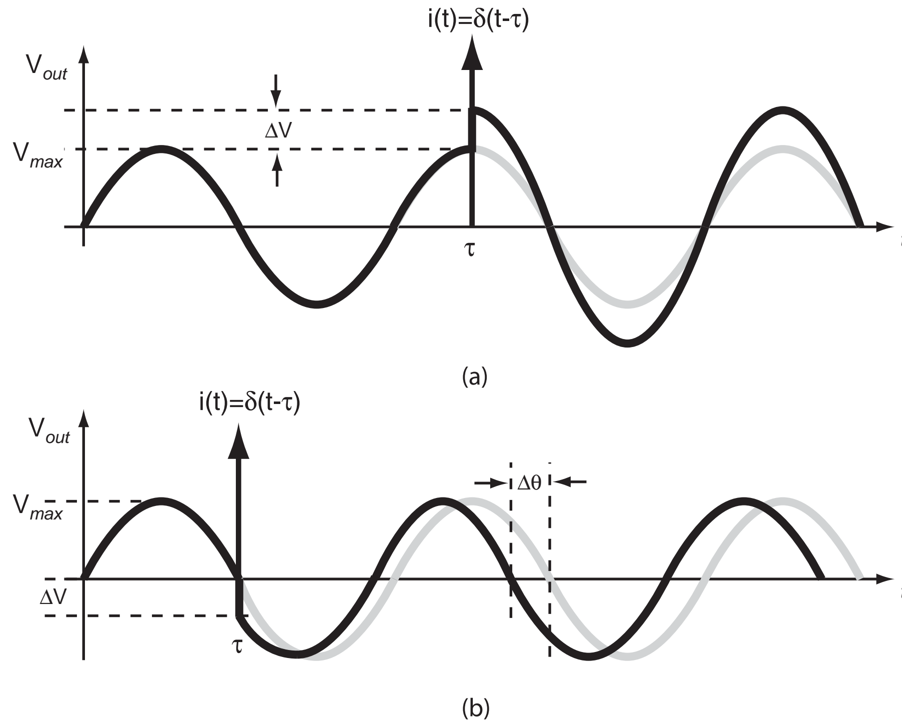


Figure 2.19: The impulse sensitivity function $\Gamma(x)$ is a measure of the variance due to both amplitude and phase noise. To describe this sensitivity, an impulse current $i(t)$ is injected into oscillator system, which causes shifts at the (a) peak of time domain and (b) zero crossing. These shifts can be interepreted as a phase noise function.

Hajimiri and Lee's Linear Time Variant (LTV) Approach

In comparison to Leeson's prior work, Hajimiri and Lee introduced a linear time *variant* (LTV) model for describing phase noise phenomenon [46]. Their approach tries to quantify phase noise within nonlinear feedback systems. Hajimiri and Lee's analysis linearizes the behavior of a steady state oscillator and describes its phase noise by means of noise impulse in time.

Suppose an injected noise source can be represented as current impulses in the time domain. If the current noise impulse occurs [Figure 2.19(a)] at the crest of the voltage waveform, the amplitude will increase abruptly. The instantaneous voltage fluctuation $\triangle V$ is related to the overall capacitance C_{tot} in the LC circuit and can be

expressed as:

$$\triangle V = \frac{\triangle q}{C_{tot}}, \tag{2.59}$$

where the total charge from the injection is $\triangle q$. Since the impulse occurs at precisely the oscillation peak, the timing of the zero crossings is not altered. However, now suppose that a noise impulse is injected at some other time. In this case, the noise affects both the amplitude *and* timing of the zero crossings [Figure 2.19(b)]. The change in timing of the zero crossing $\triangle\theta$ is considered to be the amount of phase disturbance due to injected noise. As can be seen, the assumption of time invariance does not hold. Therefore, Hajimiri and Lee assume that oscillators are linear but periodically time-varying systems.

Hajimiri-Lee introduces an impulse sensitivity function (ISF), $\Gamma(x)$, which characterizes the impact of *timing* of noise impulses on phase noise. The ISF may be determined by replacing noise sources with current impulse sources at specific times. At each impulse time τ, a measurement of amplitude and phase deviation will take place. The ISF has a period that is related to the oscillator frequency and is represented as a Fourier series:

$$\Gamma(\omega_o\tau) = \frac{c_o}{2} + \sum_{n=1}^{\infty} c_n \cdot \cos(n\omega_o\tau + \phi_n) \tag{2.60}$$

where coefficient c_n is real, and ϕ_n is the nth harmonic phase. It turns out that ϕ_n can be ignored because the phases are uncorrelated and is considered irrelevant at this level of analysis. The phase deviation is defined as:

$$\triangle\theta = \Gamma(\omega_o\tau)\frac{\triangle V}{V_{\max}} = \Gamma(\omega_o\tau)\frac{\triangle q}{q_{\max}} \tag{2.61}$$

where $\Gamma(x)$ is the ISF and is a function of both resonant frequency of the tank ω_o and current impulse time τ. The ISF is maximum at the zero crossings, and zero at the peak of the oscillation output. The maximum voltage ($V_{\max}$) across the total capacitance of the tank is equivalent to $C_{tot} \cdot q_{\max}$. As the current impulse is introduced into the LC tank, there is a voltage across the capacitor only, and zero potential across the inductor. Therefore, a simple specific ISF case for LC circuits

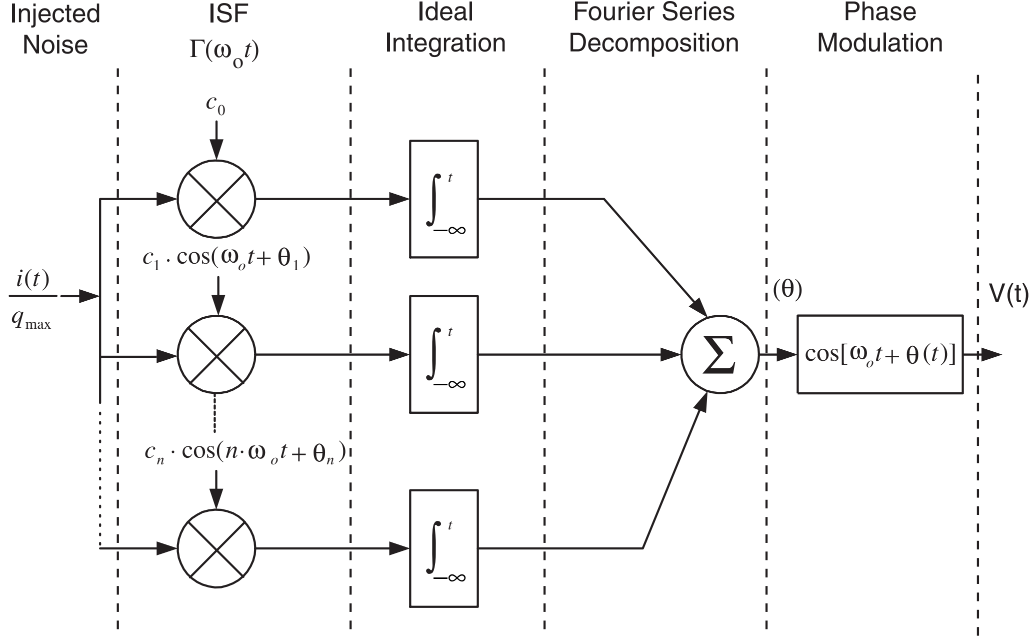


Figure 2.20: The equivalent system for ISF decomposition [46].

is given in [46] and described as (dimensionless):

$$\Gamma(x) = -\sin(x), \tag{2.62}$$

which is simply a sinusoidal function of $x = \omega_o \cdot \tau$. Thus, assuming an oscillating signal $V_{out} = \cos(\omega_o t)$, the ISF is a function that is shifted by a 90° phase from an ideal LC oscillating signal.

The Fourier components go through simultaneous downconversions (multiplications) by the local oscillator signal at all harmonics of the oscillator frequency. Figure 2.20 illustrates a sequence of downconversions of each Fourier component. Injecting a noise current $i(t)$ at a low offset ($\omega_\triangle$) frequency is expressed as:

$$i(t) = I_n \cos((n \cdot \omega_o + \omega_\triangle) \cdot t), \tag{2.63}$$

where the harmonic n is some integer multiple of the frequency, I_n is the maximum current amplitude, and it is assumed that $\omega_\triangle \ll \omega_o$. Figure 2.21(a) shows a single discrete noise harmonic for simplicity. Mixing the ISF [Figure 2.21(b)] and noise

current, integrating and summing yields:

$$\theta(t) = \frac{1}{q_{max}} \left[\frac{c_o}{2} \int_{-\infty}^{t} i(\tau) d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i(t) \cos(n\omega_o \tau) d\tau \right] \tag{2.64}$$

The summing of all integrals (superposition integral) leads to an approximation of this excess phase equation:

$$\theta(t) \approx \frac{I_n c_n \sin(\omega_\triangle t)}{2 q_{\max} \omega_\triangle} \tag{2.65}$$

Each nth value of $\theta(t)$ has dual equal sidebands at $\pm\omega_\triangle$, where n is an integer multiple of the resonant frequency ω_o. In equation 2.65, the $\theta(t)$ allows for finding the dual sideband spectrum noted as S_θ [Figure 2.21(d)]. This spectrum can be used to predict the voltage spectrum. In essence, the phase is a function of voltage and can be considered as some form of phase modulation (PM) [Figure 2.21(e)]. The noise current can be represented as a $\overline{i_n^2} / \triangle f$ [Figure 2.21(c)], which is the rms value of the peak I_n. This single-tone injection of noise creates a phase deviation that results in the sideband power of:

$$P_{SBC}(\omega_\triangle) = 10 \cdot \log \left(\frac{P_{sidebands}}{P_{carrier}} \right) = 10 \cdot \log \left(\frac{\frac{\overline{i_n^2}}{\triangle f} \sum_{n=0}^{\infty} c_n^2}{4 q_{\max}^2 \omega_\triangle^2} \right). \tag{2.66}$$

Hajimiri-Lee then develops the following equation to calculate the phase noise in the $1/f^2$ region, which is expressed as:

$$\pounds(\omega_\triangle) = 10 \cdot \log \left(\frac{\frac{\overline{i_n^2}}{\triangle f} \cdot \Gamma_{rms}^2}{2 q_{\max}^2 \omega_\triangle^2} \right) \tag{2.67}$$

where Γ_{rms} is the rms value of the ISF. Note that reducing Γ_{rms} will directly reduce phase noise at all offset frequencies.

Minimizing close-in phase noise is crucial to meet the requirements resulting from tight spectrum allocations in many wireless communications systems. While prediction of $1/f$ noise in a Leeson's LTI model is not possible, it becomes relatively easier to predict this in the LTV system [50]. Assume that $1/f$ corner frequency is described

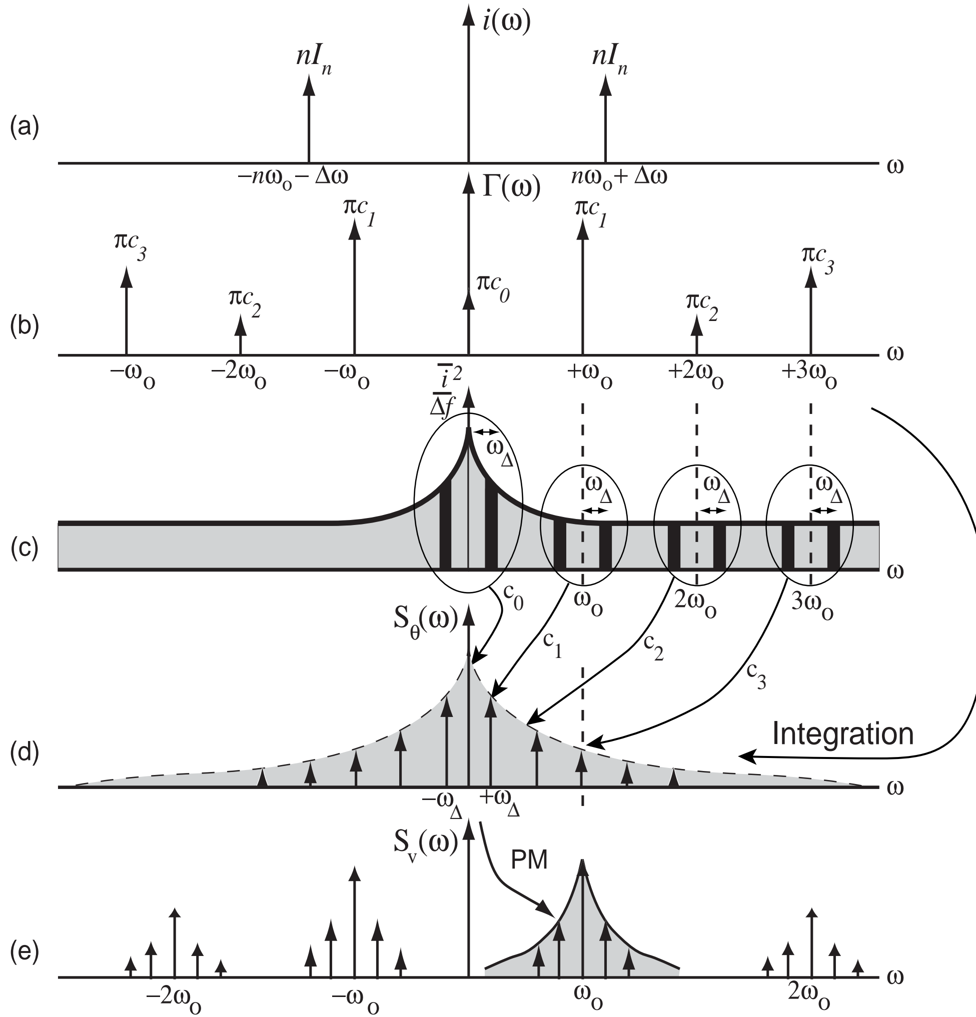


Figure 2.21: Current noise $i(\omega)$ is injected into the oscillator system. The ISF, $\Gamma(\omega)$, associated with this oscillator, can be expanded as a Fourier series with the coefficient, c_n. (a) is the approximated noise sinusoid, while (b) is the ISF function of the an ideal LC oscillator. (c) The mean-square noise spectral density $(\overline{i_n^2}/\triangle f)$ of the oscillator is the inclusion of the harmonics of the ISF. (d) The double-sideband phase noise spectrum is described as the up/downconversion of the fourier components of the ISF. (e) To discover the output voltage of the oscillator, this requires a phase-to-voltage conversion (after [50] [46]).

as:

$$\pounds(\omega_{\triangle}) = 10 \cdot \log\left(\frac{\frac{\overline{i_n^2}}{\triangle f} \cdot c_o^2}{8q_{\max}^2\omega_{\triangle}^2} \cdot \frac{\omega_{\triangle,1/f}}{\omega_{\triangle}}\right), \tag{2.68}$$

which includes the $1/f$ corner frequency equation and the c_o coefficient. It can be shown that the $1/f^3$ corner frequency is equivalent to:

$$\omega_{\triangle,1/f^3} = \omega_{\triangle,1/f} \cdot \frac{c_o^2}{4\Gamma_{rms}^2} = \omega_{\triangle,1/f} \cdot \left(\frac{\Gamma_{dc}}{\Gamma_{rms}}\right)^2, \tag{2.69}$$

where noise near DC gets upconverted and weighted by the ISF (Γ_{rms}) c_0 coefficient. Therefore, $1/f$ device noise ultimately becomes $1/f^3$ noise near the carrier. This will have a major impact on system performance at very close-in offset frequencies. The Γ_{dc} is the DC value of the ISF that is a contributing factor to $1/f^3$ close-in phase noise. Hajimiri-Lee conclude that Γ_{dc} can be minimized by maximizing the rise and fall symmetry of the devices in differential oscillators, which essentially reduces upconversion of $1/f$ noise. The complementary MOS differential oscillator is a topology with excellent rise and fall symmetry.

The time-variant model proposed by Hajimiri and Lee gives new insight into the phase noise phenomenon. While the LTI model developed by Leeson gave insight into the impact of Q and signal amplitude on phase noise, the LTV approach reveals that the timing of noise events that occur to the peaks and crests of the oscillating signal has the most impact. Finding an ISF for a particular oscillator system is quite difficult and requires very accurate models of active devices.

Summary of Models

The models presented above provide some helpful insight into various phase noise phenomenon. Leeson introduced an LTI model that described the phase noise spectrum in three different regions (thermal, $1/f^2$, and $1/f^3$). The major disadvantage of this model is that it does not really allow a priori prediction of phase noise; calculations require a posteriori fitting parameters.

Hajimiri and Lee approached phase noise with an LTV model in which the timing of noise current pulses influenced the phase noise. They derive an impulse sensitivity

function that can be used to calculate the three different regions of the phase noise spectrum. The major drawback to this approach is the difficulty in computing the ISF. Defining the ISF for the oscillating system of interest is time-consuming and depends heavily on the accuracy of the active device models. These methods, however, offer the potential for a general methodology.

2.3 Summary

This chapter has presented a foundation on LC feedback oscillators. There are two important performance parameters that must be characterized in VCO design. First is power consumption, which is generally determined by the type of active devices used (MOSFET or HBT) and their sizes. The active devices serve to generate the negative resistance. Meanwhile, phase noise is a critical attribute that can affect system performance in an overall transceiver system. Phase noise is determined by the quality factor of the resonator and the noise sources presented in the active circuit device. Equations for the thermal, flicker, and shot noise contributions within active devices have been presented. Additionally, two different phase noise models were described. Each model has particular disadvantages, but still provide useful insight that can help designers minimize phase noise in VCOs.

Chapter 3

VCO Design and Implementation

To design an integrated VCO that meets particular system specifications, a careful design methodology must be established. This chapter first discusses the fundamentals for integration of required passive components. This includes full-wave electromagnetic simulations of monolithic inductor simulations of MOS varactor C-V tuning curves. The impact of the passive components on the design and the optimization of active devices will also be detailed. This chapter will provide a summary of the resulting design synthesis flow for integrated VCOs in MOS and bipolar technologies in order to meet frequency, power consumption, and phase noise goals. Finally, simulation results for the VCO topologies analyzed, and an explanation of the advantages and disadvantages of such implementations, will be provided.

3.1 Passive Devices

There are two major considerations in the design of passive components within an integrated oscillator:

1. Selection of the output frequency (and tuning range) of oscillator $\omega_o = 1/\sqrt{LC}$.
2. Determination of the amount of negative resistance required to overcome the losses in the passive components, which in turn impacts the power consumption.

The output tuning is accomplished through integrating varactors in the LC tank circuit.

As discussed in the previous chapter, the quality factor (Q) plays a major role in VCO phase noise performance. The resonator Q will directly impact the power consumed during stable oscillation. The total quality factor of an LC tank is given as:

$$\frac{1}{Q_{tot}} = \frac{1}{Q_L} + \frac{1}{Q_C} \tag{3.1}$$

where Q_L and Q_C are the total quality factors for the inductance and capacitance of the circuit, respectively. These components must be carefully designed to achieve the desired ω_o, while achieving reasonable Q and minimizing die area occupancy.

3.1.1 Monolithic Inductors

The push toward single-chip implementations has driven the development of on-chip inductors using existing silicon-based processes. In the recent past, off-chip surface mount inductors have been used for VCO circuits. While these components typically provide much higher Q, other issues impact the circuit design and performance. For example, additional input/output bond wire inductance and resistive losses due to package and pad connections result in undesirable effects that must be tuned out or compensated for. Off-chip inductors also increase board-level complexity, and therefore, increase packaging and testing costs. Monolithic inductor development includes trade-offs between design parameters and technological issues. The major design parameters include the following:

- Geometry type (square, octagonal, circular spiral, single-ended, differential, and symmetric)
- Material properties of both inductor coils and via/metal underpass structures
- Material properties of inter-metal dielectrics (IMDs)

The technological issues that arise when taking the implementation and modification of the inductor design parameters into consideration include:

- Substrate resistivity
- Self-resonant frequency
- Parasitic capacitance and parasitic loss mechanisms

Inductor Geometry

Investigating various types of inductor geometries has been the subject of many previous publications [51] [52] [53]. A number of variations of planar spiral inductors have been studied. The primary geometrical variations are square, circular, and octagonal spiral inductors. The type of geometry is selected to fulfill the required amount of inductance, while minimizing die area. Designers must understand the material properties of the metal, whether it is electroplated copper, aluminum, or other metal, during the BiCMOS fabrication process. The most obvious and efficient structural form is the a circular spiral coil, which is a smooth continuous circular layer of metal. While a spiral coil consumes the minimal amount of die area for a given inductance, limitations in the masking process (the information used to manage and create the layers of metal during the photolithography process) typically allow only polygon shapes with angles of exactly 45° and 90°. Therefore, typically the only options are either a square or octagonal coil.

Differential Structures

Differential inductors are preferred when designing cross-coupled VCOs with differential outputs. Two popular types of differential inductor configurations can be used: the dual inductor [Figure 3.1(a)], which is two coils connected by a common node underpass; and the symmetric inductor [3.1(b)], which is a structure that contains two intertwined coils. In such designs, it is important that the VCO layout be completely symmetric to ensure that a virtual ground exists at the plane of symmetry.

Inductor Losses

There are three primary loss mechanisms in monolithic inductor structures ([20] [54]):

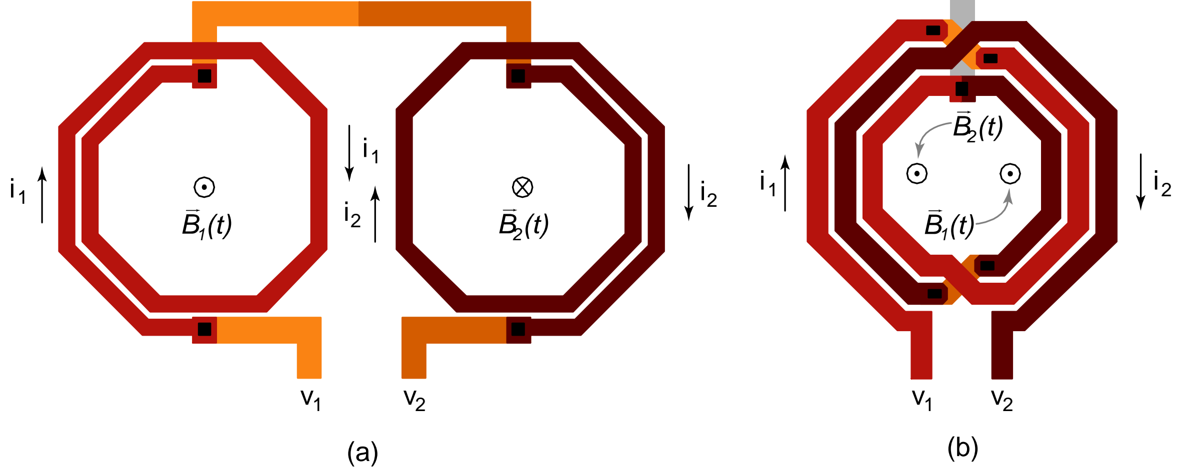


Figure 3.1: There are two types of differential inductors: (a) the dual inductor, and (b) symmetric inductor (after [20]).

1. Conductor loss
2. Capacitive (electric) substrate loss
3. Magnetic substrate loss

The amount of loss due to these mechanisms is influenced by the inductor geometry and the materials (i.e., dielectric, metal, and vias) from which the inductor is constructed.

A differential inductor of this kind can be typically characterized by an equivalent lumped element model circuit (Figure 3.2), specifically a two-port Π-network of lumped passive components. Conductor loss is represented as the series resistance R_S. The capacitive (electric) substrate loss is modeled as R_{sub}, while the magnetic substrate coupling loss is represented by $R_{sub(m)}$. Finally, C_{sub} and C_{ox} are parasitic capacitance and the shunt capacitance representing the total associated losses that couples the RF energy into the lossy substrate. The cross-under (strap) connecting the two inductor coils, and the inter-winding capacitances, are modeled together as C_p. The lumped model includes the effective inductance L_{eff}, which is the result of loss components seen across the two ports of a dual inductor. The model of L_{eff} between two series inductors with a virtual ground produces a floating impedance between ports 1 and 2 of the π-network introduced in Figure 3.2. The general equation

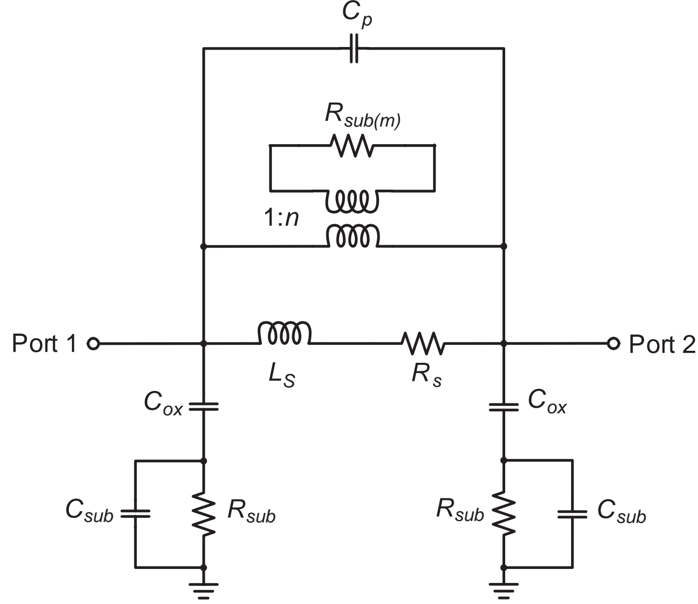


Figure 3.2: An equivalent lumped model characterizing a monolithic inductor on Si substrates (after [20] [54]).

to calculate the effective differential inductance is [20] [36]:

$$L_{eff} = \frac{X}{2\pi f} = \left(\frac{1}{2\pi f}\right)\left[\mathrm{Im}\left(\frac{Y_{11}+Y_{22}+2Y_{12}}{Y_{11}Y_{22}-Y_{12}^2}\right)\right] \tag{3.2}$$

The equation for differential Q factor is:

$$Q = \frac{X}{R} = \frac{\left[\mathrm{Im}\left(\frac{Y_{11}+Y_{22}+2Y_{12}}{Y_{11}Y_{22}-Y_{12}^2}\right)\right]}{\left[\mathrm{Re}\left(\frac{Y_{11}+Y_{22}+2Y_{12}}{Y_{11}Y_{22}-Y_{12}^2}\right)\right]}. \tag{3.3}$$

The reduction of the π-network floating impedance is

$$R + jX = \frac{Y_{11}+Y_{22}+2Y_{12}}{Y_{11}Y_{22}-Y_{12}^2} \tag{3.4}$$

A complete derivation of these equations can be found in [20][36].

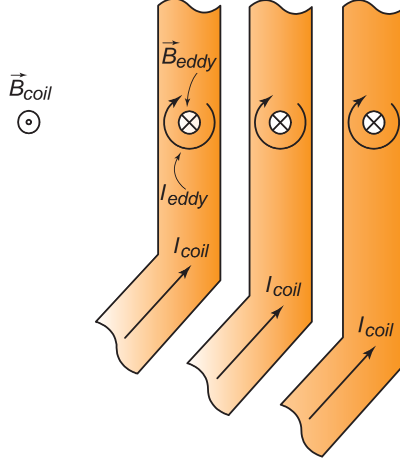


Figure 3.3: Generation of eddy currents within an octogonal planor inductor. The ⊗ and ⊙ symbols represent fields pointing into and out of the page, respectively (after [20] [52]).

1. ***Conductor Loss (*** R_S ***)*** The conductor loss of the inductor traces can be described by the following equation:

$$R_s = \frac{\rho_{film}}{t}\frac{L}{W}, \tag{3.5}$$

where ρ_{film} is the thin film resistivity of the metal, t is the metal thickness, L is trace length, and W is trace width. Some advanced BiCMOS processes contain a 3-10 μm-thick electroplated-copper (Cu) top most metal layer using a conventional thick filmed photoresist and electroplating process. This layer is also referred to as the *bump* layer (the protruding metal traces result in a bumpy surface from an otherwise planarized passivation layer). The copper bump layer is the thickest metal layer within the process, which is advantageous for lowering the series resistance of monolithic inductors.

Another source of loss is the eddy currents induced by the magnetic field penetrating the turns of the spiral (Figure 3.3), in accordance with the Faraday-Lenz law [52]. The inductor carries a current I_{coil} in the direction indicated by the arrows in Figure 3.3. This current gives rise to an associated magnetic field, $\vec{B}_{coil}$, that has a maximum intensity at the center of the spiral and is oriented perpendicular and out of the page (symbolized by ⊙). This field interacts with the turns of the spiral, inducing

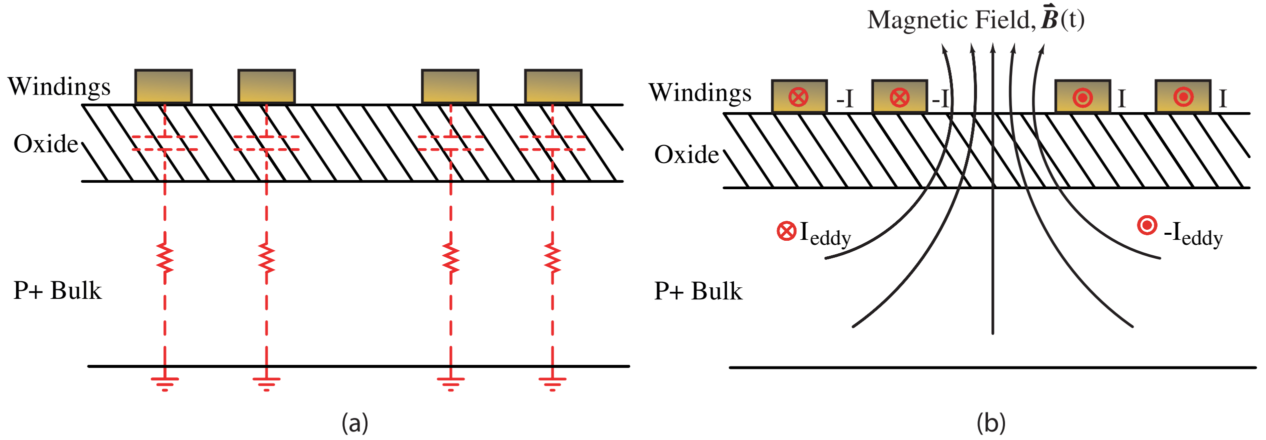


Figure 3.4: (a) Low-resistive substrate allows for RF signals to shunt through the parasitic capacitance to ground. The image currents are induced by the time varying magnetic fields of the coil. (b) The $\otimes$ and $\odot$ symbols represent currents flowing into and out of the page, respectively (after [36] [54]).

the circular eddy currents I_{eddy}. These eddy currents tend to push (or crowd) the I_{coil} current toward the inner edges of the traces. In other words, the traces have effectively smaller widths for carrying current, creating more resistive loss in the windings. This effect is more pronounced for the inner turns than the outer turns because of the $\overrightarrow{B}_{coil}$ is stronger at the center of the inductor winding; therefore, it is desirable to maximize the free space in the center of the inductor structure.

2. Substrate Loss (R_{sub}) A drawback of standard Si-based processes for monolithic inductors is the relatively low (<10-20 Ω·cm) resistivity of the substrate (compared to GaAs, or other semi-insulating substrates). The substrate can be modeled as resistances between the inductor parasitic shunt capacitance below the inductor windings and ground [Figure 3.4(a)]. In GaAs processes, the substrate resistivity ($10^5 \rightarrow 10^6$ Ω·cm) is fairly large thereby minimizing the effects of substrate loss. On the other hand, in a Si process, the low-resistivity substrate will allow RF signals to couple through the shunt capacitance to ground, significantly reducing the Q factor compared to conventional GaAs processes.

Planar inductors in Si processes also suffer from loss because of the magnetic field coupling of the windings to the substrate (also called magnetic loss). Due to the time varying RF current flow within the windings, image currents are induced in

the Si substrate [Figure 3.4(b)]. This phenomenon can be modeled as a parasitic transformer where the secondary winding is connected to a substrate resistance. Such image currents may account for 50% or more of the loss from the inductor [54] [55].

To avoid the effects of magnetic loss, patterned ground shields (PGS) may be placed between the inductor and the substrate [56]. The shield screens the inductor from the lossy substrate. The patterned slots with the shield are orthogonal to the coil windings to mitigate the image currents forming in the shield itself. Such PGS structures have been reported to increase Q factor by 33% and reduce substrate coupling between two inductors by 25 dB [51]. Given the interest in low-phase noise oscillators, patterned ground shields have become popular for VCO designs.

3. Parasitic Capacitance (C_{sub}, C_{ox}, C_p) Between the inductor windings and the substrate are layers of dielectrics with varying properties resulting in the parasitic capacitance C_{sub}, C_{ox}, and C_p shown in Figure 3.2. The capacitances have a significant effect on the self-resonant frequency (f_{sr}) of the inductor. Self-resonance occurs at a frequency where the net reactance of the inductor is equal to zero. For example, the parasitic capacitances resonate out the inductance of the coil.

The standard equation for capacitance is:

$$C = \epsilon \frac{A}{d} \tag{3.6}$$

where A is the area of the plates, ϵ is the dielectric constant ($\epsilon = \epsilon_r \epsilon_o$), and d is the distance (or dielectric thickness) between the plates. Parallel plates of metal with a dielectric of varying thickness may be found in a number of locations on a spiral inductor. Fringing field capacitance is the parasitic capacitance of the perimeter of the coil (Figure 3.5). Another example is the capacitance between the coil and the substrate. In addition, parasitic capacitance can exist between the cross-unders and spiral windings of the inductor coils.

The total area of the inductor windings and the underlying substrate can be thought of as two plates of this parasitic capacitance, as shown in Figure 3.4(a). Reducing the trace widths of the coil will reduce the amount of area of the top "plate". However, too much reduction in width results in higher series resistance. Increasing the distance between the coils and the substrate can be controlled by designing the inductor on

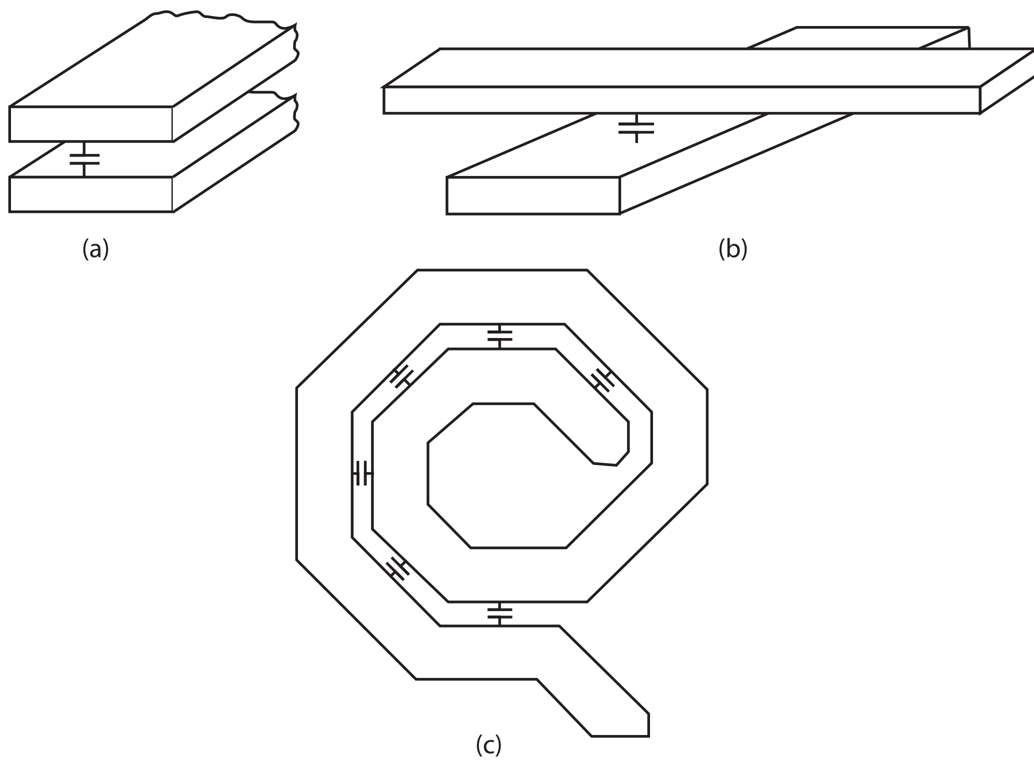


Figure 3.5: The parasitic capacitance C_p can arise from (a) metal traces separated by a dielectric, (b) cross-unders of metal layers, and (c) the fringing fields between inductor interwindings.

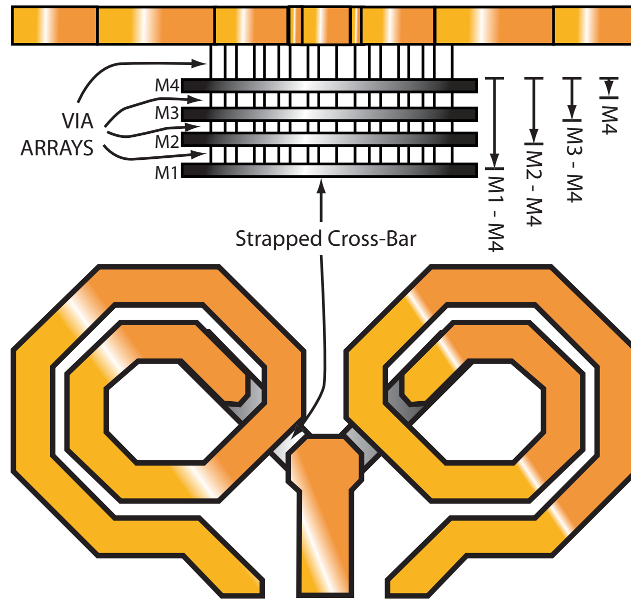


Figure 3.6: Cross sectional view of the strapped metal cross-bar to reduce resistance.

the top most metal layer. Strapping multiple metal layers together, as illustrated in Figure 3.6, reduces series resistance; however, this brings the inductor windings closer to the substrate, resulting in greater coupling to the substrate (and loss increases). Stacking the layers of metal with an array of vias is effectively lowering the sheet resistance of the cross-under structure.

Careful trade-offs between various aspects of the inductor structure must be taken into consideration to achieve the highest possible Q value for the frequency of interest. Finite element modeling (FEM) or method of moments (MoM) electromagnetic simulators can guide the design of inductors, and will be discussed further in the next section.

Inductor Selection

Determining the inductor geometry for the desired specification frequencies between 3-3.8 GHz required careful attention to all design parameters discussed in the previous sections. Therefore, to maintain a maximum 3.8 GHz tuning resonance, an inductance of approximately 520 pH was required to make an accurate comparison between the reviewed design methodologies (Section 3.17). Tuning to 3.8 GHz in-

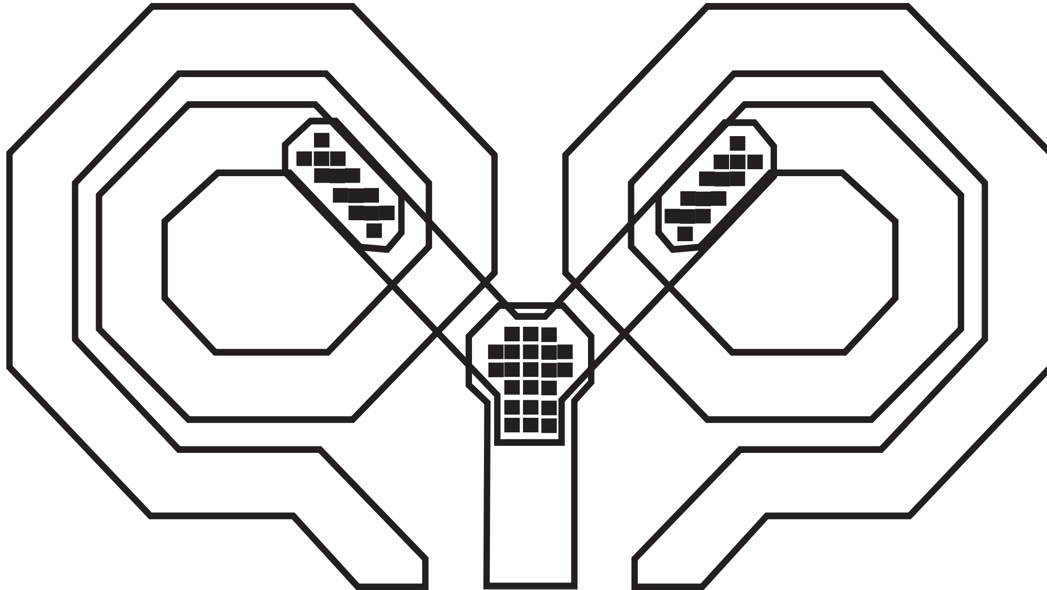


Figure 3.7: The octogonal spiral inductor geometry that was selected for the VCO desing in this work.

corporates the total capacitance of the design, which includes parasitic gate-to-source capacitance (C_{gs}) of the NMOS devices (approximately 3.42 pF) and will be discussed further in the later sections. Due to the fact that such a low inductance is required, the coil trace lengths were quite minimal, thereby eliminating the option for symmetrically wound inductors. Therefore, dual differential octagonal spiral inductors were chosen for this design.

Within the CDR1 process, the dual differential octagonal spiral inductor is the optimum structure, due to the efficiency of die area occupancy versus conductive and substrate loss. Unfortunately, dual differential inductor structures require cross-unders that capacitively couples some quantity of signal into the substrate. The inductor coil center spacing is approximately 40 μm [Figure 3.7]. The individual spirals have a trace width of 15 μm and a trace length of 470 μm. The total width and length of the differential inductor is 240×127.4 μm, which is an area of approximately 30.6 mm^2. For the CDR1 process, the thick copper bump layer enables a significant improvement in Q over thinner interconnect layers. Series resistance can be further reduced by widening the inductor traces, but was not an option for the low-inductance coil design here.

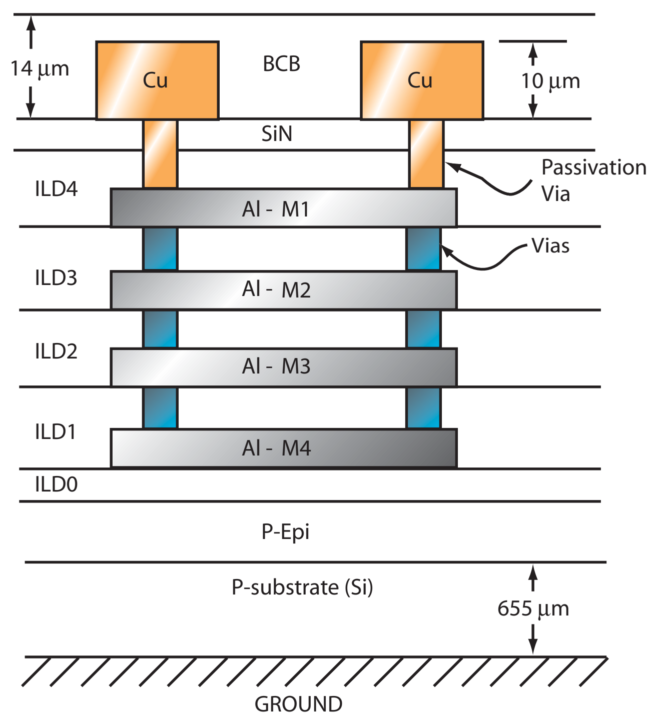


Figure 3.8: Cross-section of the CDR1 inductor layers (not to scale). The ILDs (inter layer dielectric) are actually composites of one or more dielectric layers.

The dual inductors were connected using underpasses in lower metal (Al) interconnect levels (Figure 3.8). The added resistance from both the vias and the thinner metal increases the overall loss of the inductor. To overcome this effect, additional layers were strapped together with arrays of vias to synthesize an effectively thicker layer of metal, thereby lowering total resistance [57]. Secondly, increasing the width of the trace to 15 μm while also reducing the total length of the trace reduced resistance. Series resistance loss is reduced by implementing the coils in an octagonal structure compared to the less efficient coil lengths of a square spiral.

Inductor EM Simulator Background

With the advent of more accurate and robust electromagnetic (EM) simulation tools, characterization and optimization of monolithic structures has led to the development of new design and modeling methodologies. Simulation of inductor structures in this work was conducted using two powerful full-wave electromagnetic solver packages: Momentum RF, which is integrated into the Agilent EEsof EDA Advance Design System (ADS) 2002C [58], and Sonnet EM [59]. Both are 2.5D full-wave electromagnetic solvers that employ the Methods of Moments (MoM). A 2.5D solver differs from a full 3D simulator (e.g., FEM solver) in the way metal layers are treated. Specifically, metal layers are analyzed in both MoM engines as infinitely thin strips of metals with a specific amount of conductivity (this does not include vias). Additionally, both simulators calculate numerically the Green's functions for substrate characterization. Detailed comparisons of the types of Sonnet EM computational techniques have been presented in [20] [60].

Inductor structures were laid out using the Cadence Virtuoso Layout [61] environment. The layout must pass the design rule checker (DRC) before being exported to the EM simulators. DRC is a verification tool that checks that the completed layout follows the design rules of the fabrication process. The simulators are then set up to specify vias, metal layers, and substrate information. Dielectric and thickness properties of the process layers provided by Motorola were used for the simulations of octagonal spiral inductors. However, due to the proprietary nature of information concerning the Motorola CDR1 process, specific details concerning the dielectric permittivities cannot be given in this thesis. Both EM simulators output S-parameter

files, which can be converted into SpectreRF format and subsequently used as n-port devices within the circuit-level schematic.

For the EM simulations, it is critical that all information for the physical layers of dielectric thickness, relative dielectric permittivity (ϵ_r), metal thickness, metal conductivity, and loss tangents (δ) be accurately entered into the simulation setup. In the Motorola process, the ILDs are composed of combinations of stacked dielectrics, with different permittivities and thicknesses. Therefore, for simulation purposes, a weighted average of the individual dielectrics comprising a given ILD layer was taken:

$$\epsilon_{r,avg} = \frac{\epsilon_{r_1} \cdot t_1 + \epsilon_{r_2} \cdot t_2 + \epsilon_{r_3} \cdot t_3 + \ldots \epsilon_{r_n} \cdot t_n}{t_1 + t_2 + t_3 + \ldots t_n}, \tag{3.7}$$

where the permittivity ϵ_{r_n} and the thickness t_n are those corresponding to the nth layer of the ILD. The copper (Cu) and aluminum (Al) metal layers are modeled as strips with bulk conductivities of 5.7×10^7 S/m and 2.5×10^7 S/m, respectively. The lossy Si substrate has a permittivity of 11.8 and a conductivity of 5.8 S/m (17 Ω·cm).

Inductor EM Simulations

A number of inductor structures were studied using the 2.5D EM simulations described above. Initially, square spiral *p-cell*[1] inductors readily available in the CDR1 design kit were analyzed in various VCO topologies (discussed in the next section). However, square p-cell inductors with sufficiently low value for the desired VCO designs were not available . Therefore, customized differential octagonal structures were implemented and characterized using MoM electromagnetic simulator analysis (Figure 3.7).

Both EM simulators were used to obtain s-parameters from 1Hz to 20 GHz (much higher than the desired VCO 3-3.8 GHz frequency range). The S-Parameters were converted to Y-Parameters to calculate the Q factor and L_{eff} using equations 3.3 and 3.2, respectively. The Q factor results are quite close to the desired frequency range; however, the results diverge at higher frequencies (Figure 3.10 and Table 3.1). Note that these curves do not reveal the self-resonance frequency f_{sr}, which lies well above the frequency range of interest (3-3.8 GHz). Most importantly, the simulation results

[1] P-cells are parameterized cells found in design kits for silicon processes.

Strap Configuration	Sonnet Quality Factor (Q)	Sonnet Inductance	Momentum Quality Factor (Q)	Momentum Inductance
Metal 1 - Metal 4	12.969	640 pH	12.269	516 pH
Metal 2 - Metal 4	12.325	654 pH	12.776	518 pH
Metal 3 - Metal 4	12.339	659 pH	12.091	520 pH
Metal 4	10.907	669 pH	10.536	520 pH

Table 3.1: Quality factor and inductance comparison between Sonnet and Momentem EM simulators at fsr = 3.8 GHz. Strap configuration considers the different combinations of stacked layered metal of the cross-under.

show that a single Metal 4 strap results in the lowest Q factor (although practically speaking, the difference is small). This is due to the larger series resistance for the thinner strap, which dominates over the strap distance from the substrate. The significance of the strap design is the trade-off between series resistance and parasitic capacitance of the metal to substrate. Additionally, the effective inductance shows an increasing trend as the number of layers of metal in the strap is decreased (Figure 3.9). It should be noted that typical effective inductance curves do not show an increase at lower frequencies [20]. In the simulations here, this effect may be due to the simulation accuracy for a minimal sized inductive element with large parasitic capacitances. For an $f_{sr} \gg 3.8$ GHz, there is a an average150 pH deviation between the Momentum and Sonnet simulations. This could be the result of two factors; first, there may be an artifact in how the simulations were setup to describe the physical model of the inductors. Second, there may be a computational discrepancy within the simulators. Due to the fact that there is such a minimal quantity of inductance, the resolution of the computations may have more error within this regime. Without further iterations between simulations and experimental data, the correct result is still in question.

3.1.2 Varactors

The tuning of LC VCOs is typically accomplished with integrated varactors (variable MOS capacitors). There are several methods for implementing varactors using MOS devices, which have been studied thoroughly in [62]. For this thesis, available PMOS

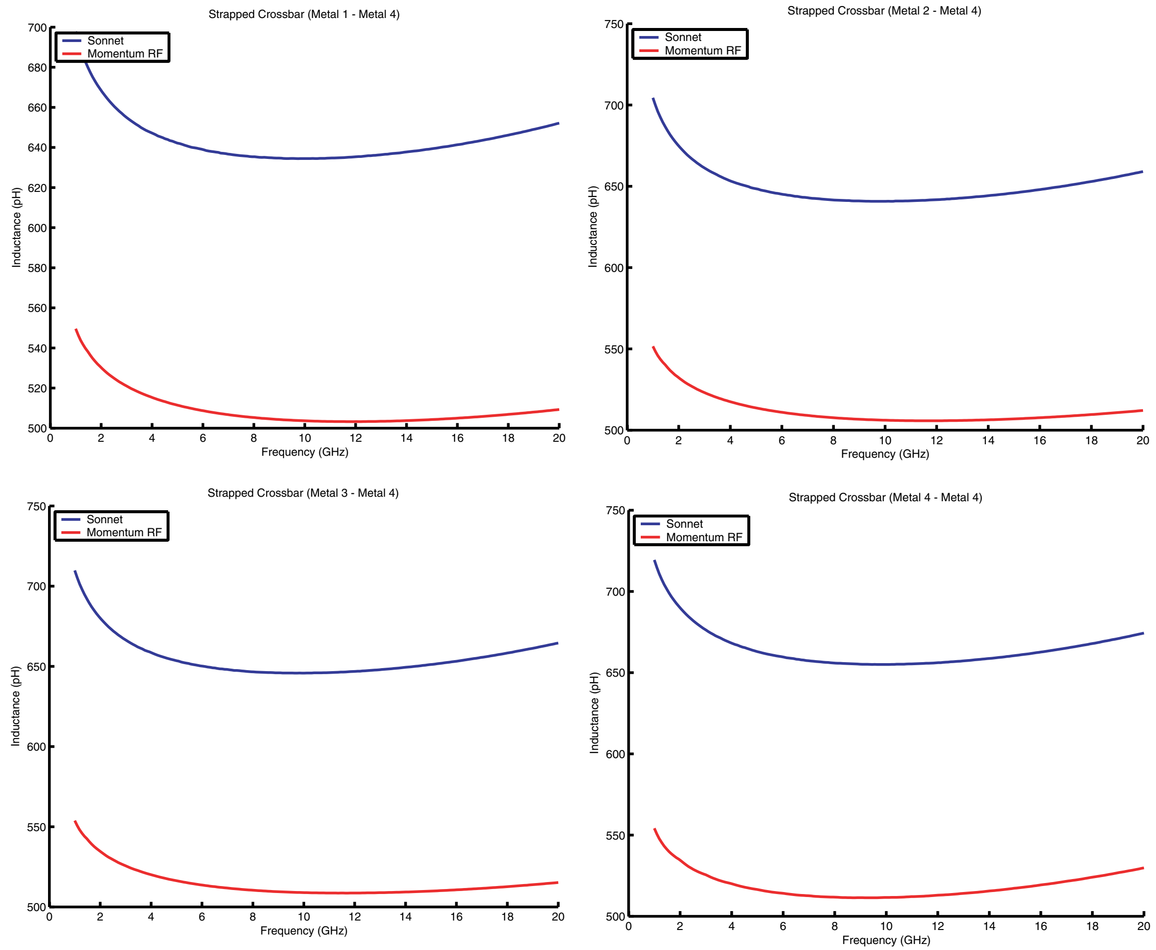


Figure 3.9: Comparison of Sonnet and Momentum EM simulators: data illustrating $f_{sr} \gg$ 3.8 GHz.

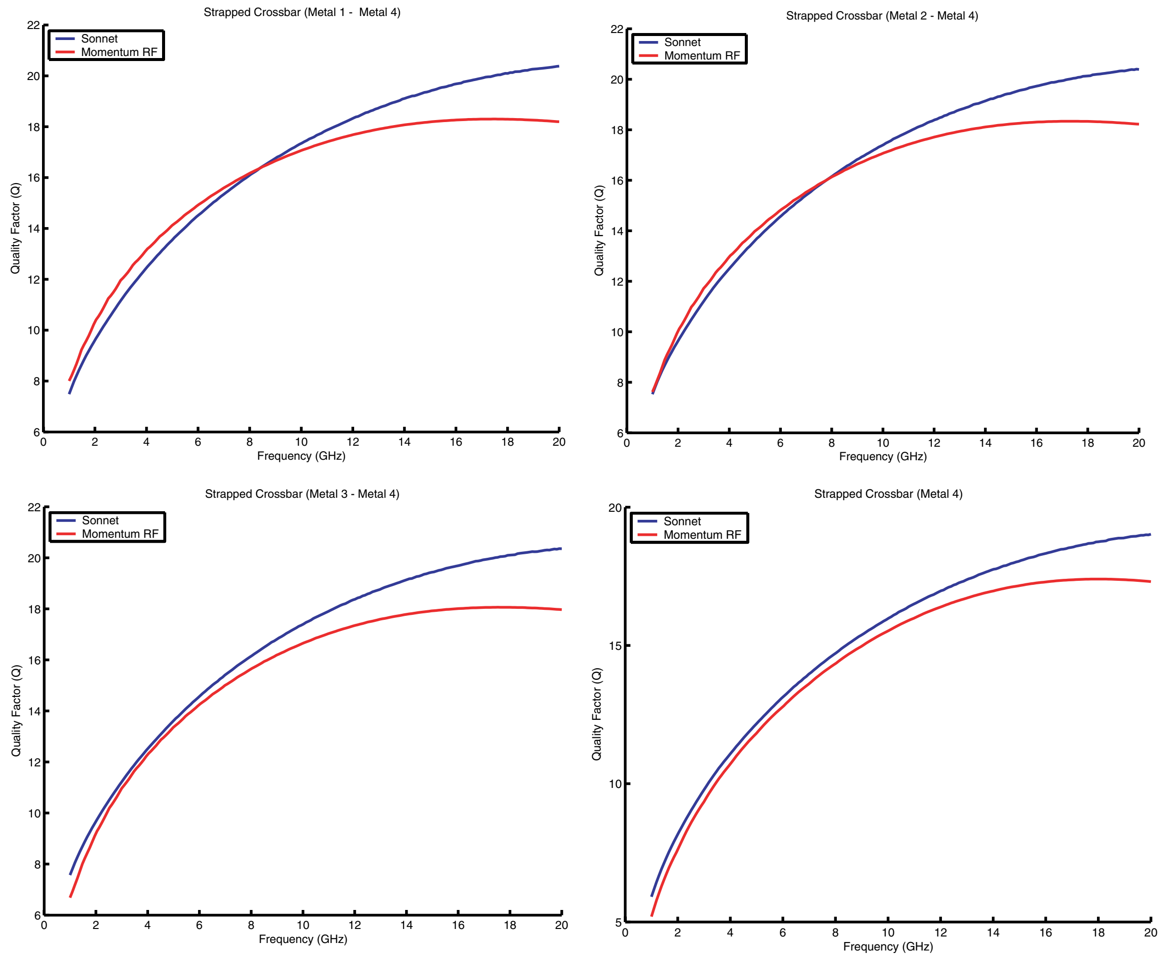


Figure 3.10: Comparison of Sonnet and Momentum EM simulators: data illustrating the Quality factor of $f_{sr} \gg 3.8$ GHz.

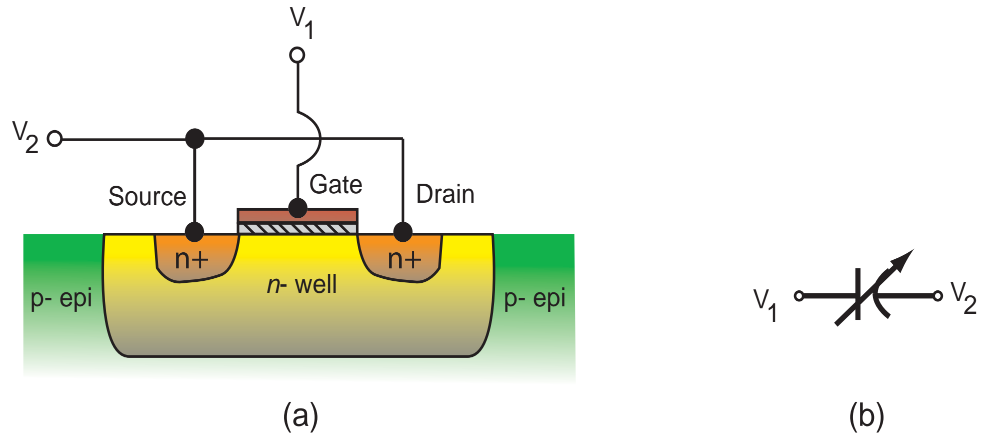


Figure 3.11: (a) Cross section of an accumulation mode varactor and (b) circuit symbol representation.

accumulation mode varactors were used (Figure 3.11). The accumulation mode arises from shorting the $n+$ drain and source diffusion regions in an n-well together to form one signal capacitor terminal. Meanwhile, the other terminal is the polysilicon gate. A bulk connection, is not required for this topology. This geometry suppresses the inherent injection of minority carriers (holes) into the channel, preventing the varactor from entering into inversion mode, such that it operates only in accumulation and depletion modes. The "DC" C-V characteristic illustrated in Figure 3.12 was simulated using BSIM3v3[2] models with an applied 10 mV small-signal at a frequency of 4 GHz at various DC tuning voltages $V_{sg.}$

The DC "small-signal" characteristic shows a slightly sharp monotonic slope gain transition, which is typical within inversion mode structures. However, the oscillator will tune to the frequency determined by the large-signal average capacitance. Large-signal averaging applies to voltage amplitudes within the oscillator that are greater than 0.5 V. The effective capacitance in the time domain has a "smoothing" effect on the DC small signal characteristic [62]. Therefore, the DC C–V characteristic will be a more gradual tuning compared to the small-signal response. The Motorola CDR1 varactor large-signal tuning is shown in Figure 3.12. The varactors used in the

[2] "BSIM" is an acronym for the University of California Berkeley Short-channel IGFET Model.

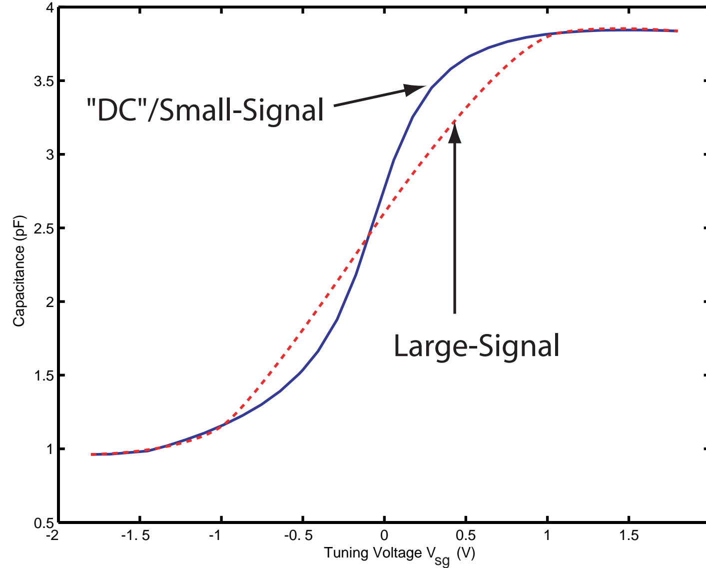


Figure 3.12: "DC" small-signal and large-signal tuning capacitance characteristic versus voltage of the inversion-mode varactor. The varactor is implemented with a channel width and length of 1 μm and 6 uμm with 30 fingers and 4 gate segments. The applied DC voltage at the V_1 node is referenced as V_{sg}.

CDR1 process have a Q factor ranging from 20-25 in the 3-4 GHz range. Varactor Q has a direct impact on total Q of the tank circuit, and in turn affects phase-noise performance. All models within the simulation utilize curve-fitting data collected from process samples. When implemented on actual silicon, such devices suffer a lower quality factor due to additional resistive losses, parasitic and fixed capacitances within the overall VCO design.

3.2 Active Devices

The design of integrated VCOs requires an in-depth understanding of the active devices to be used in the negative resistance circuit, for example, MOS transistors and SiGe HBTs. A number of recent publications have compared these types of devices for RF applications [63] [64]. Designers must understand the impact of device size, voltage bias, parasitics, etc. on VCO performance. To this end, the most accurate, reliable, and robust device models must be used.

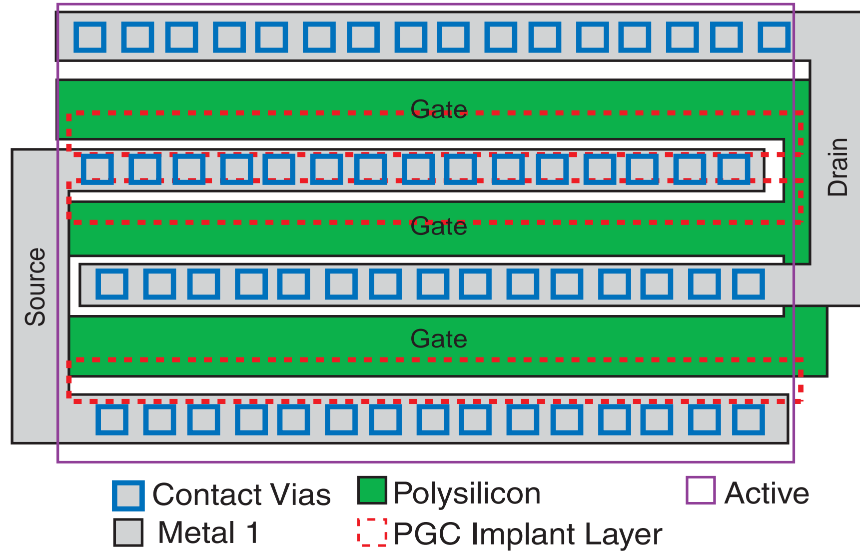


Figure 3.13: Layout of a GC-NMOS device, with shared source and multiple finger polysilicon gates.

3.2.1 Graded-Channel MOS

The Motorola CDR1 BiCMOS process is considered to be a fairly mature technology. These devices are incorporated in the design kit using the BSIM3v3 model developed at UC Berkeley. As mentioned in Section 1.1.2, the MOSFET devices used for this work are Graded-Channel MOS (GCMOS) devices that have an asymmetric structure. However, BSIM models are designed for generic MOSFET characterization, which are typically used for symmetric structures. Therefore, the model parameters are determined by statistical compilation of data sampled from on-wafer device measurements. This includes I-V characteristics, $1/f$ flicker noise, channel noise, and capacitive parasitics. All model characterizations were accomplished by statistical compilation of sampling from on-wafer probing measurements.

The GCMOS devices have a minimum drawn gate length of 0.4 μm (0.35 μm effective length) and a minimum drawn channel width of 0.5 μm. The devices can be configured to have multiple gate fingers.

Multifinger transistors can also help reduce *gate resistance* [65]. A layout is illustrated in Figure 3.13, which incorporates the PGC (profiled graded-channel) layer to describe the masking step for applying the graded channel. As will be shown in Section 3.6.2,

increasing the number of fingers can help reduce phase noise but at the expense of increased current consumption. The value of gate resistance directly impacts the minimum noise figure of the device. However, the BSIM3v3 model does not account for gate resistance, and simulations using these models do not accurately measure overall noise. Therefore, it is advisable to include a lumped resistor element at the gate for proper simulation of MOS devices in RF circuits. This gate resistance can be approximated as:

$$r_g = \frac{R_{sh,\square} W}{3NL}, \tag{3.8}$$

where $R_{sh,\square}$ is the sheet resistance of the polysilicon gate material, N is the number of fingers, and W and L are the channel width and length, respectively.

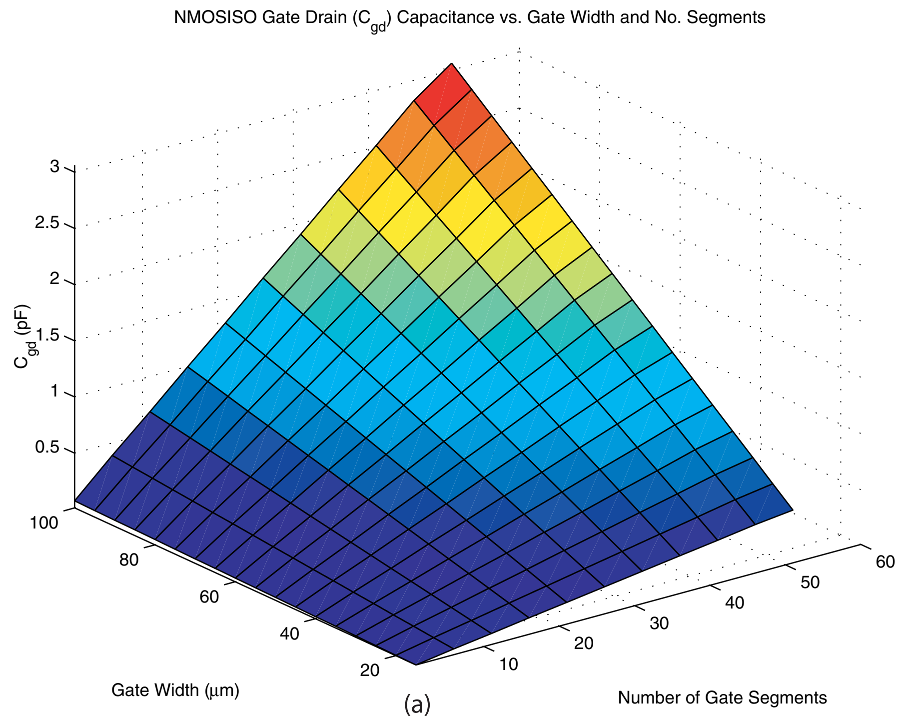
Induced gate noise is a separate phenomenon that is related to the thermal noise in the channel of the device. The channel noise capacitively couples onto the gate node and can be modeled as a gate noise current source. These thermal noise contributions can be upconverted to phase noise in an oscillator, which has the effect of increasing the phase noise at larger offset frequencies.

A major drawback to using MOS devices as compared to SiGe HBTs are the higher parasitic capacitances. Increasing the width of an NMOS device decreases phase noise due to the increase in signal power. However, larger devices suffer from larger parasitic C_{gs} and C_{gd} values, which can impact tuning the VCO over a specific frequency range. A large tuning gain (K_{VCO}) can increase phase noise due to the control voltage noise. Additionally, recall from equation 1.4 that larger C_{gd} and C_{gs} values will adversely impact the f_T performance of the MOS. Therefore, minimizing gate-source and gate-drain capacitances as much as possible will help the overall performance of the VCO.

Due to the graded-channel profile of the GCMOS, the gate-source capacitance is typically greater than the gate-drain capacitance ($C_{gs} > C_{gd}$). A larger gate overlap over the graded profile source diffusion region results in a higher C_{gs} capacitance. In saturation, these parasitic capacitances are given by:

$$C_{gs} = WL\frac{C_{ox}}{2} + WC_{ov,gs} \tag{3.9}$$

$$C_{gd} = WL\frac{C_{ox}}{2} + WC_{ov,gd}, \tag{3.10}$$



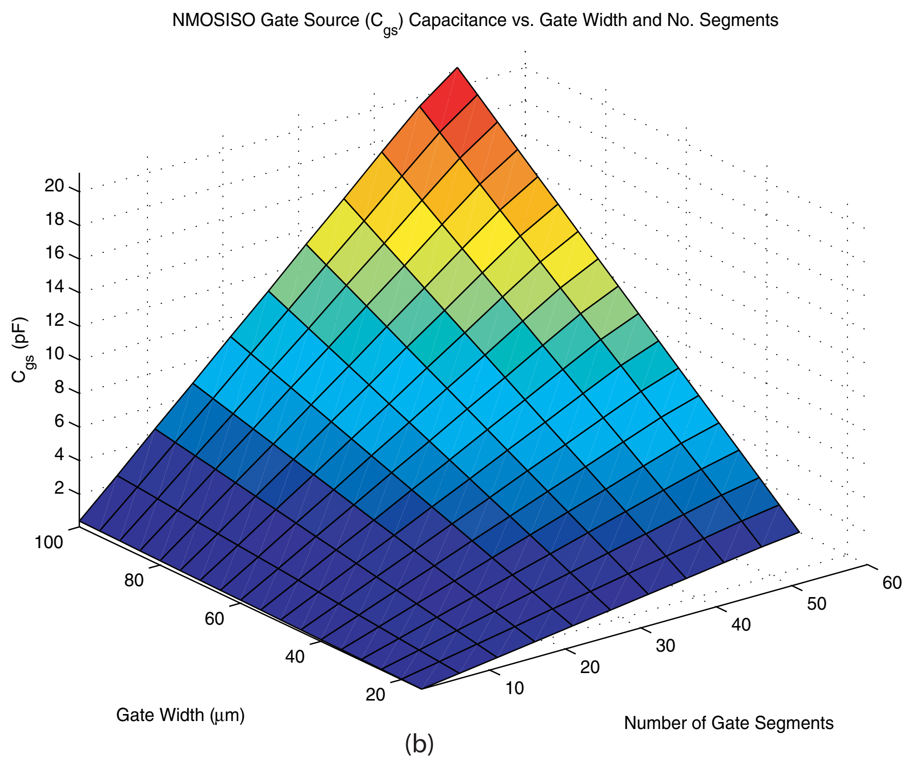


Figure 3.14: The parasitic NMOS capacitance between (a) the gate-drain C_{gd}, and (b) the gate-source C_{gs} with varying width and a fixed length of 0.35 μm.

where C_{ox} is the gate-oxide capacitance, and $C_{ov,gd}$ and $C_{ov,gs}$ are the overlap capacitance of gate poly over the drain and source regions, respectively.

A swept AC analysis was performed to determine the C_{gd} and C_{gs} versus width values of the graded-channel NMOS devices with a fixed minimum length of 0.35 μm (Figure 3.14). As is expected, the change in parasitic capacitance demonstrates a monotonically increasing trend with relation to an increase in width. These curves were extracted for the purpose of finding a proper design parameter between VCO tuning and phase noise (higher signal power).

3.2.2 Si/SiGe:C HBT

The Motorola CDR1 process also offers a SiGe HBT module for high-performance RF/analog applications. Parasitic capacitances in HBTs are typically an order of magnitude smaller than in MOS devices. In the CDR1 design kit, the SiGe HBT device is modeled using the Vertical Bipolar Intercompany Model (VBIC) [66], an improved bipolar SPICE model capable of simulating base width modulation, parasitics, and electrothermal effects.

Three major SiGe HBT parameters can be controlled by the design. First, emitter length (L_e) has a major impact on the performance of the device. Increasing emitter area can significantly improve $1/f$ noise for the input-referred base current noise [67]. Second, the number of emitter fingers can be varied to improve performance (multiplying the number of fingers by the area of the emitter) and will increase g_m. The transconductance g_m is determined by:

$$g_m = \frac{I_C}{V_T}, \tag{3.11}$$

where V_T is the thermal voltage (kT/q) and I_C is the collector current. Collector current in an *npn*-bipolar transistor is biased with a voltage V_{BE} and is given by the following equation [37]:

$$I_C = \frac{qA_eD_nn_{po}}{W_B}e^{V_{BE}/V_T}, \tag{3.12}$$

where q is a fundamental electron charge, A_e is the emitter area, D_n is the diffusion constant of electrons, n_{po} is the electron equilibrium concentration, and W_B is the

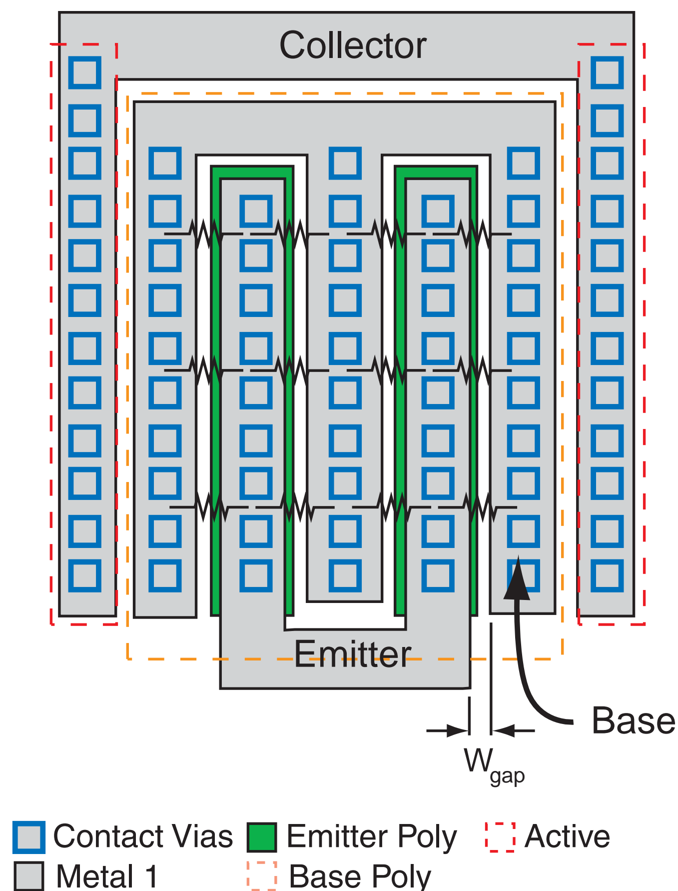


Figure 3.15: Layout and cross-sectional view of a typical SiGe:C HBT device with two emitter fingers and two collector stripes. Base resistance is a function of the W_{gap} between the base and emitter. Note that the "active" layer is for masking instruction purposes only.

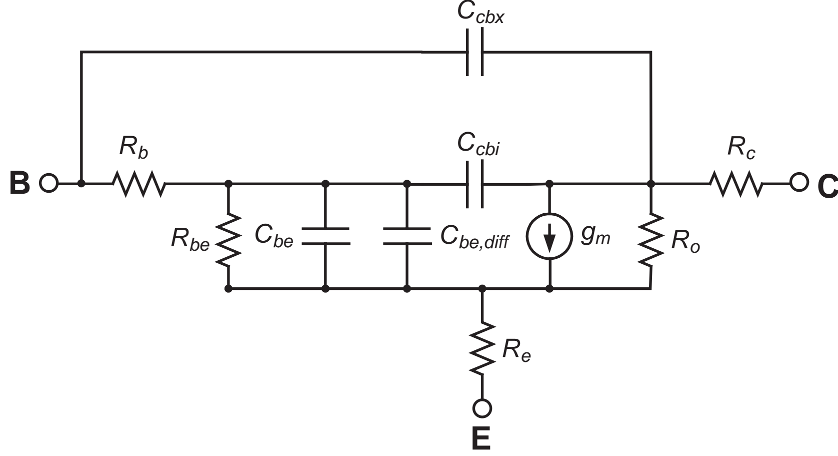


Figure 3.16: Hybrid-π small-signal equivalent circuit model of the Si/SiGe HBT, where C_{cbx} and C_{cbi} are the extrinsic and intrinsic collector-base capacitance, respectively (after [68]).

width of the base. The emitter area is a major factor in the increase current, which will also increase the peak f_T. The number of base fingers is $N_b = N_e + 1$, where N_e is the number of emitter fingers, as shown in Figure 3.15.

The final parameter that defines the HBT structure is the number of collector stripes. A maximum of two collector fingers are allowed when laying out CDR1 HBT devices. Collector resistance does have an impact on HBT performance. Implementing two collector stripes does make interconnect routing more complex. Parallel stripes reduce the amount of collector resistance compared to implementing a single "top" collector.

The base resistance R_B has a major impact on the f_{MAX}. Base resistance is largely governed by the implementation of the vertical device structure and lateral scaling of the fingers. Figure 3.16 shows the equivalent circuit model of an Si/SiGe HBT. The base resistance can be approximated by [69]:

$$R_B = \frac{\rho_b W_e}{12 L_e} + \frac{\rho_b W_{gap}}{2 L_e} + \frac{\sqrt{\rho_c \rho_b}}{2 L_e}, \tag{3.13}$$

where W_e and L_e are emitter width and length, ρ_b and ρ_c are the base sheet and contact resistivity, respectively. W_{gap} is the gap width between the emitter and base (Figure 3.15), which is controlled by the mask alignment tolerances during fabrica-

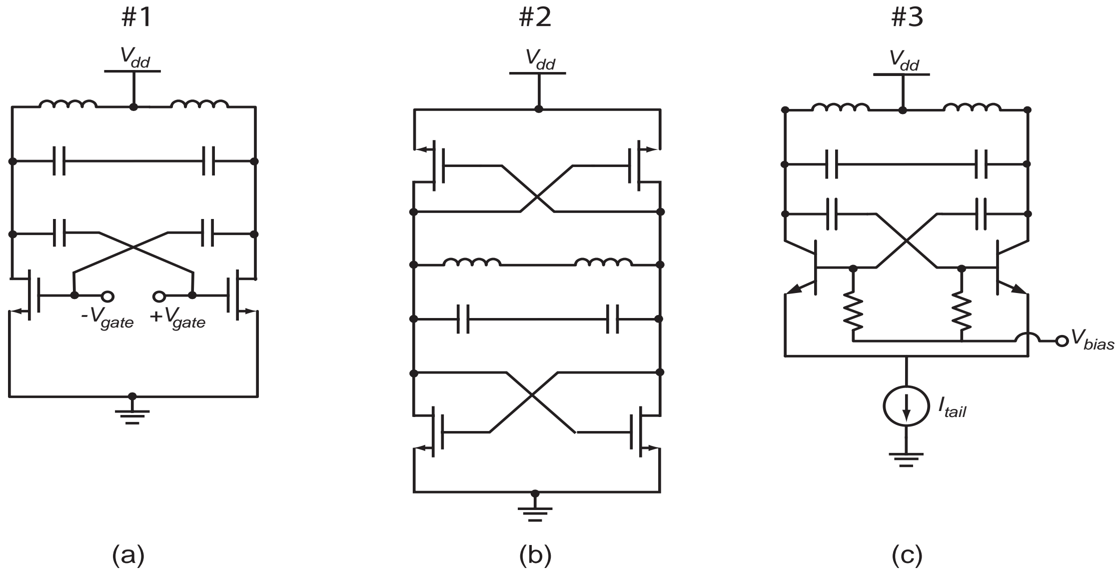


Figure 3.17: The three cross-coupled -G_M VCO topologies studied in this thesis: (a) *#1* - NMOS pair; (b) *#2* - complementary MOS pair; and (c) *#3* - HBT pair.

tion. Unfortunately, this gap dimension and the resistivities cannot be controlled by the designer; however, the ability to control the base and emitter areas will greatly influence $1/f$ noise performance and sufficient g_m transconductance in an oscillator design.

3.3 Overview of VCO Topologies

This section introduces the three basic VCO topologies that are studied in this thesis. This section also includes the design and simulation of the output buffer used for each VCO implementation.

3.3.1 The Analyzed Topologies

This thesis has studied three MOS VCO topologies: a cross-coupled NMOS pair [Figure 3.17(a)] and a cross-coupled complementary MOS pair [Figure 3.17(b)] design, as well as a cross-coupled HBT design [Figure 3.17(c)]. A major focus of this analysis was power consumption versus phase-noise performance. To ensure a fair comparison,

each design integrated similar tank circuits with the same dual inductor structure. Each design also included the same output buffer, which is discussed in Section 3.3.2.

The cross-coupled NMOS topology (MOS Topology #1) supplies a negative resistance with one pair of NMOS devices. Rather than having a tail current source, the NMOS devices are sized appropriately to provide sufficient negative resistance. Tail current sources introduce an additional required voltage drop, decreasing the head room available for achieving a particular output voltage swing. A separate circuit is required to bias the gates (V_{gate}). This design has a high-output swing and requires a capacitive voltage divider to avoid compression into the buffer circuit. Unfortunately, because of the acquiescent biasing point and the size of the devices required, this topology proved to be extremely power inefficient. Therefore, this circuit was not fabricated and exploration into more efficient topologies (#2 and #3) were studied.

The cross-coupled complementary topology (MOS Topology #2) was also considered in this work. This circuit can be realized as a cross-coupled pair of MOS inverters. Because of the reduced head room available with this circuit, less output voltage swing can be achieved. However, this circuit has been shown by Hajimiri and Lee [46] to have reduced close-in phase noise (Section 2.2.5). One issue with this design is that the PMOS devices needed to be sized appropriately so that the switching rise and fall times of the complementary devices remain symmetric. Asymmetry in the rise and fall times manifests itself as a degradation in phase-noise performance. However, increasing the size of the PMOS devices to meet rise/fall symmetry requirements tends to increase power consumption of the VCO. Additionally, currents should remain equal between both differential nodes.

Finally, a cross-coupled HBT VCO (HBT Topology #3) was analyzed. In this case, additional bias circuitry was required to set the base voltages of the negative resistance transistors. As mentioned above, HBTs do not present as much parasitic capacitance as MOS devices. Because of the higher parasitic capacitance, a relatively small inductor was needed to tune the MOS Topology #2 circuit for the specified frequency range. To make a fair comparison, the HBT design used the same inductor. Therefore, additional tank capacitance was necessary for the HBT design to achieve the same operating frequency. The HBT design demonstrated comparable simulated phase-noise results (Section 3.6.3), but consumed slightly more power than MOS Topology #2 because of the additional biasing circuitry required.

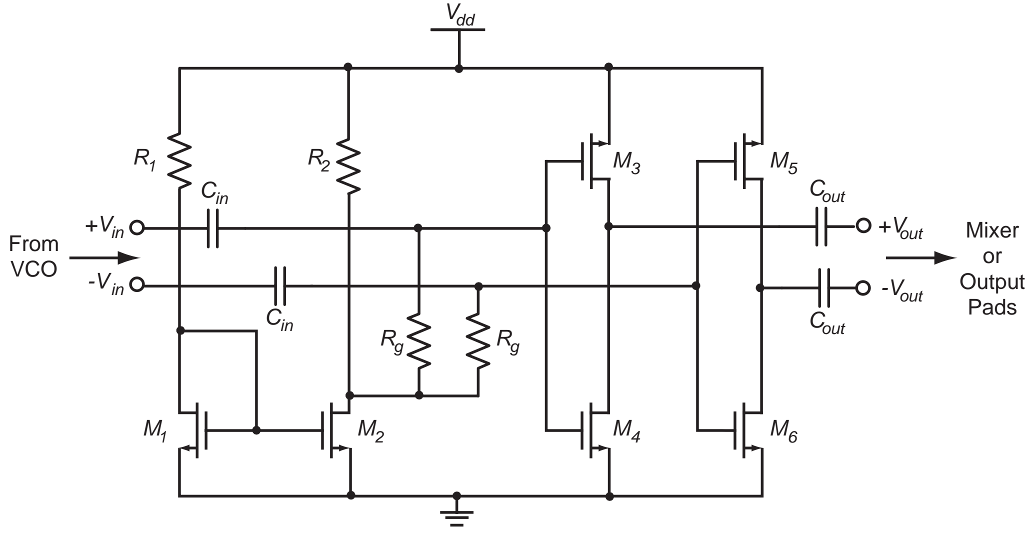


Figure 3.18: Schematic of the VCO class-B, push-pull differential output buffer.

MOS Topology #2 and HBT Topology #3 were selected for layout and fabrication.

3.3.2 Output Buffer Design

The above VCO topologies require output buffering. In this work the output buffer design serves primarily as an impedance transformer. The two stages of the buffer are the implemented as a differential class-B, *push-pull*, CMOS amplifiers. The buffer design can be viewed as a pair of inverters, one for each of the outputs of the oscillator (Figure 3.18). The resistors R_g (2.28 kΩ) set the DC gate bias voltages of the NMOS and PMOS devices (M_3, M_4, M_5, and M_6) so they operate in saturation and linear regions. Due to the relative carrier mobilities of the devices (equation 2.16), the PMOS transistor widths are sized 2x larger (W_3, W_5 = 10 μm and W_4, W_6 = 5 μm), resulting in an even fall and rise time. The buffer design operates with a supply voltage V_{dd} of 3.3 V and consumes 8 mA of current (a relatively high current consumption).

An important feature of the class-B topology is that it offers a relatively high 1 dB compression point. Simulations show that the input-referred 1 dB compression point is approximately 10.2 dBm (Figure 3.19). However, the high compression point comes at the expense of higher power consumption (22 mW). In addition, this buffer design

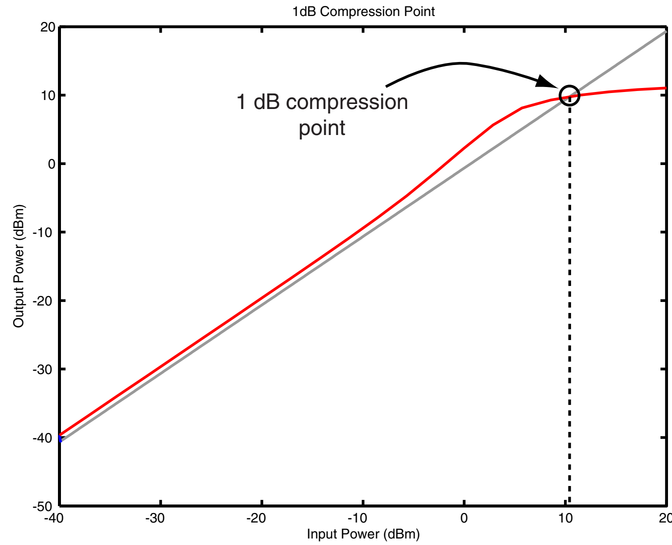


Figure 3.19: Simulation of the 1 dB compression point for the class-B, push-pull CMOS buffer.

has less than unity voltage gain since it has been designed for high-to-low impedance conversion. Simulations show that this design has a power gain of -2 dB.

3.4 VCO Design Flow

In this thesis, the complementary cross-coupled MOS VCO topology (Section 3.6.2) was implemented. An overview of the typical design flow for this topology is shown in Figure 3.20. This design flow assumes a tank circuit with cross-coupled devices in parallel. The diagram details the sequence in which a design modification takes place and the resulting effect(s) to be considered. The solid black outlined boxes represent specific design alterations and the red dash-outlined boxes are the corresponding effects. A general starting point for implementing any oscillator begins with the choice of appropriate inductance and capacitance to set a specific frequency of oscillation ($\omega_o = 1/\sqrt{LC}$). A negative resistance circuit is then designed to overcome the parallel equivalent resistance of the required LC tank. The effect of inserting the cross-coupled MOS devices, introduces parasitic capacitance. Therefore, a modifica-

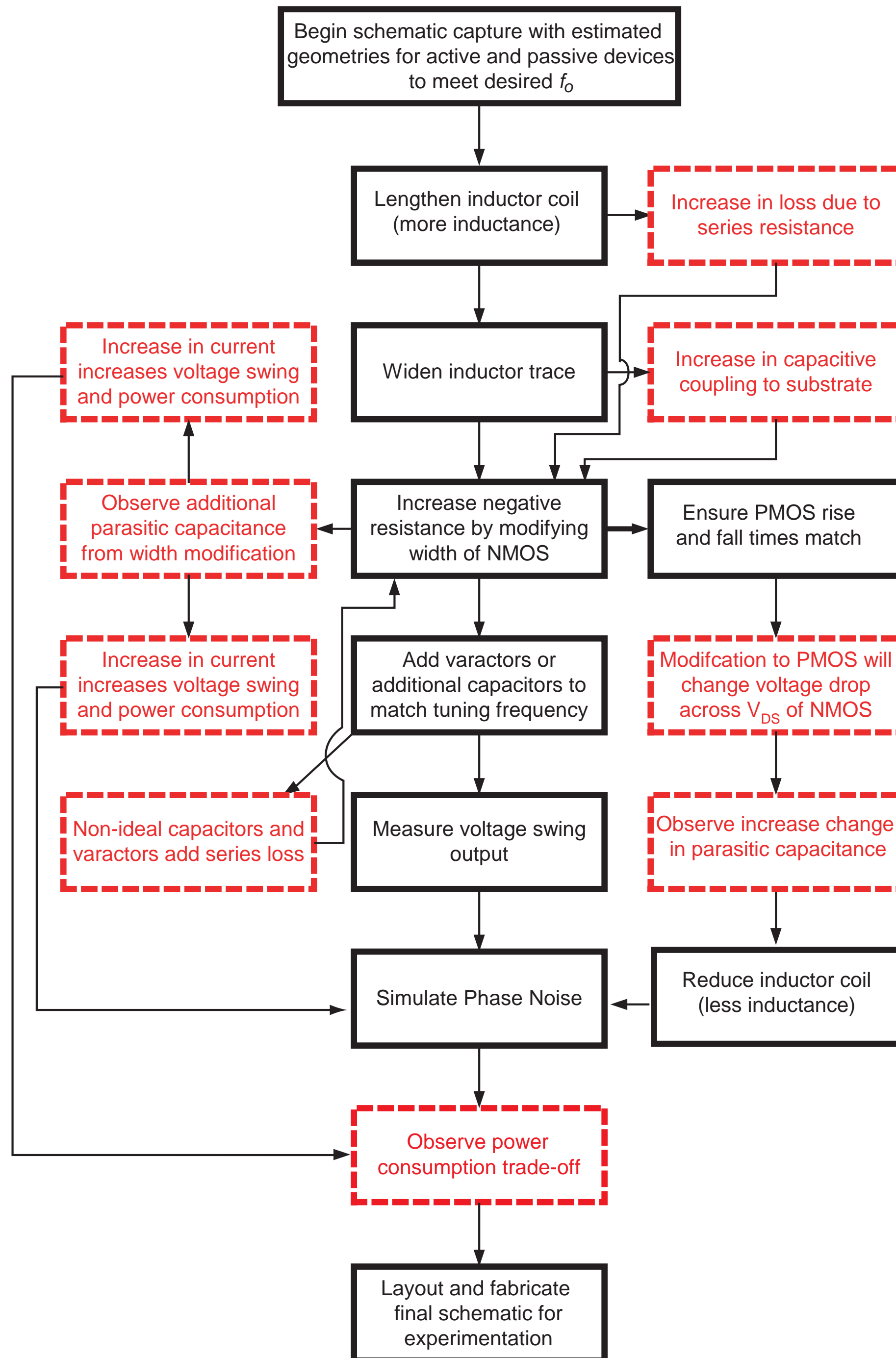


Figure 3.20: Design flow of a complementary MOS VCO implementation. The solid black outlined boxes represent a design modification, while the dashed red outlined boxes show the effect of the modification.

tion to the inductor coil length and width is required to increase inductance and bring the oscillator back to the desired resonance. At this point, additional capacitance is integrated into the tank due to parasitics of the coils. Oscillator simulations are then performed to determine if phase noise, power consumption, and output swing meet the desired specification. Note that the phase-noise simulations are not completely accurate and should only be used to get a general idea of operating trends. If voltage swing is reduced, phase noise increases; therefore, the PMOS/NMOS device channel widths and lengths are varied to increase signal power. The passive components are then modified to meet resonance goals. This cycle is repeated until the design approaches the designer's objectives.

The design flow for SiGe HBT VCOs [Figure 3.21] is slightly different, since the active devices present less parasitics. However, there is an increase in complexity due to the required bias and current source circuitry for controlling the negative resistance generation. In addition, emitter degeneration resistors are required to limit the tail current source, which can affect close-in phase noise.

3.5 Simulation Issues

One focus of this thesis was a comparison of the relative advantages and disadvantages of GCMOSs and HBTs for $-G_M$ VCO implementations. The primary goal, of course, was to realize a practical design that meets stringent phase-noise specifications while maintaining low power consumption. Such conclusions relied heavily on simulations and accurate modeling before finally submitting the design for fabrication. This section will discuss the various simulation tools used in this design process.

3.5.1 Cadence SpectreRF Periodic Steady-State Simulator

The non-linear circuit simulator used in this work was the Cadence Spectre RF Periodic Steady-State (PSS) analysis tool [70]. PSS provides a method for computing the large-signal directly from the steady state response of a non-linear circuit.

The PSS analysis is Cadence's version of simulating non-linear autonomous oscillators. Autonomous oscillators are circuits that do not have input stimulus and generate AC

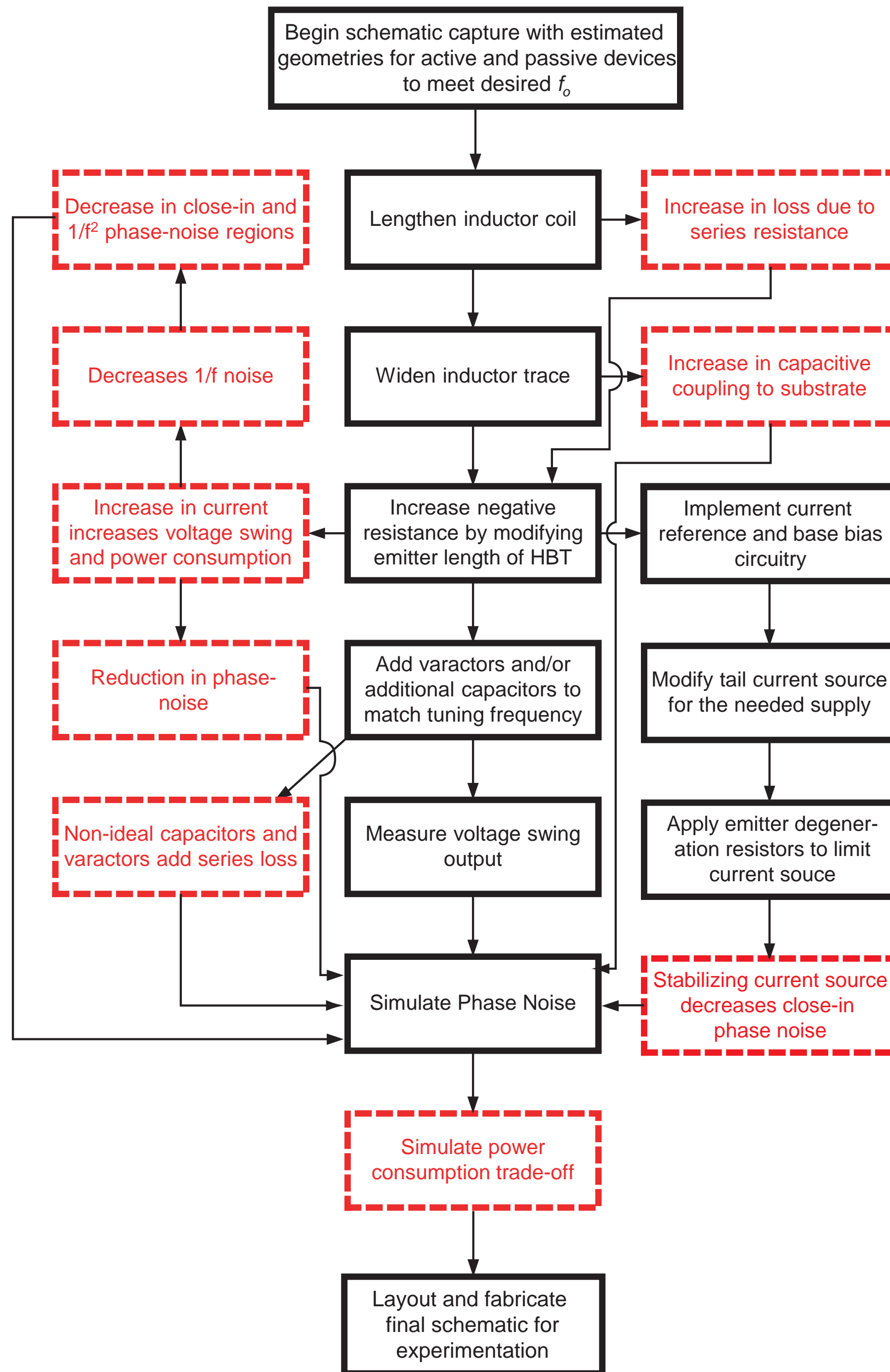


Figure 3.21: Design flow of a complementary SiGe HBT VCO implementation. The solid black outlined boxes represent a design modification, while the dashed red outlined boxes show the effect of the modification.

or RF outputs themselves. PSS relies on a proprietary shooting method algorithm to determine periodicity. The shooting method is a time domain approach to finding a steady state solution with a given set of initial conditions [70]. The PSS algorithm runs the circuit in a transient condition and analyzes the output waveform continually until it finds a steady state. For any linear time-variant (LTV) analysis to take place (phase noise, spectral analysis, etc.), the output must achieve a final *convergence* threshold. If no convergence is found, the simulator will continue indefinitely until such a condition is met or until the designer stops the simulation. Non-convergence can be an indicator of an error in the design that is limiting the circuit from oscillating in a steady state.

The SpectreRF simulator utilizes the PSS information and conditions to perform a PNOISE (phase noise) analysis. The simulator determines an LTV solution using small-signal analysis based upon the operating points calculated by PSS. The thermal, shot, and $1/f$ noise that contribute to the close-in phase noise are calculated in this analysis. A detailed explanation of how the simulator determines phase noise is given in [70].

Specific issues that users must take into consideration to obtain convergence for oscillating circuits are described briefly below:

- **Kick-Start:** An independent voltage or current source should be inserted to "kick-start" the oscillating circuit. For simulations in this thesis, a piecewise current source was used to provide a single 2 ns current pulse. It is preferred to use an initial condition for one of the passive components in the resonator; however, the passive components in the CDR1 design kit did not have this capability. In practice, an oscillator is naturally kick-started by the natural noise in the residual charges absorbed during circuit power-up.

- **Transient Simulation:** The total simulation time was typically set to about 100 ns, which provided over 300 waveform periods. It is important to run the simulation for a fairly long time since there are some cases where a steady oscillation will appear to start up but then will slowly dampen out. This behavior indicates that the tank circuit has too much loss, which means the negative resistance circuit must be revised. It is recommended that all transient simulations should have the *errpreset* set to "conservative," and the *integration method*

parameter set to “gear2only” to achieve convergence in oscillator simulations [70].

- **PSS Settings:** After confirming that a particular design has achieved a steady state oscillation with a transient simulation, large-signal PSS simulations are then conducted. In PSS, the *tstab* should be set to an appropriate length of time to give the oscillator circuit time to settle. Increasing this setting to the same run-time used in the transient simulations is recommended for achieving PSS convergence. Also, the *reltol* should be to 1e-5; this is the relative convergence tolerance option that specifies how fine the discrete stepping must be relative to the node voltage. Finally, the *vabstol* should be set to 3e-8, and the *iabstol* should be set to 1e-13.

- **PNOISE Settings:** *Maximum sidebands* should be set to 10; this sets up the analysis to include harmonics of the fundamental, which are generated from non-linearities of the oscillator and are included in the total phase-noise calculation. In addition, *reference-sidebands* should be set to 0, since the oscillators being simulated are autonomous circuits and do not require any large-signal input stimuli.

- **N-port Inductor Models:** The s-parameters for the inductors obtained from full-wave EM simulations were included as n-port cells for SpectreRF circuit simulations. For PSS simulations: *Interpolation Method* should be set to rational; *Relative error* and *Absolute error* should be set to 0.001; *Multiplier* and *Scale factor* should be set to 1; and *Rational order* should be set to 5. Cadence recommends setting the interpolation method to Spline for TRAN, DC, and SP analysis.

3.6 Simulations of VCO Topologies

Three VCO topologies were explored: two MOS designs and one HBT design. The MOS Topology #1 is a cross-coupled pair of NMOS transistors. MOS Topology #2 is a cross-coupled complementary MOS topology. HBT Topology #3 is a cross-coupled pair of SiGe HBTs. This section will discuss the simulation results of these VCO topologies.

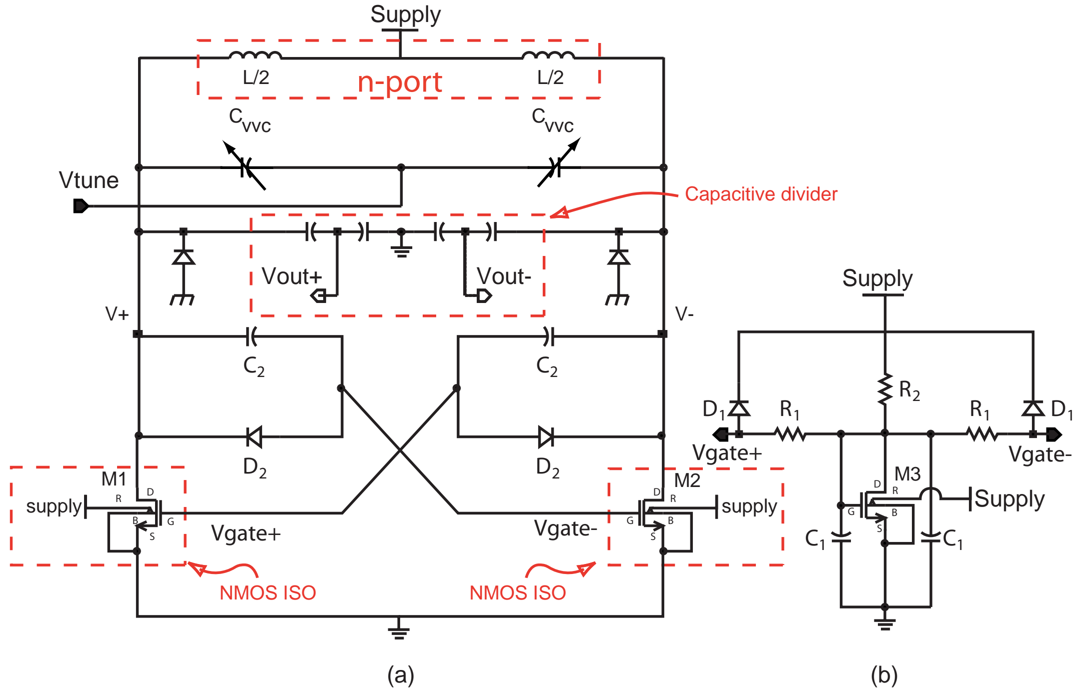


Figure 3.22: The first design attempt was (a) cross-coupled NMOS VCO with (b) an MOS biasing circuit for the negative resistance NMOS gates.

3.6.1 MOS-Topology #1: Cross-Coupled NMOS Pair

The single cross-coupled NMOS pair is advantageous over the complementary MOS topology in relieving head room to obtain a maximum voltage swing. Recall from the phase-noise equation 2.58 that an increase in signal power P_{sig} will reduce phase noise. Figure 3.22(a) shows a circuit schematic of MOS Topology #1. Figure 3.22(b) shows the gate bias network containing $p+$ diffusion in n-well diodes (D_1), poly resistors 2.65k (R_1 and R_2), and 635 fF capacitors C_1. This bias circuitry provides the appropriate operating points for the $-G_M$ devices M_1 and M_2 and are differentially connected via the $Vgate$- and $Vgate+$ pins. The diodes, D_1, are the electrostatic discharge (ESD) protection diodes to protect the gates of the device M_3. Meanwhile, the diode D_2 protects the gates of the the cross-coupled pair of NMOS ISO M_1 and M_2. A large RF-signal swings on these gates from the oscillations that occur through the differential output nodes $V+$ and $V-$. Here, the diodes will protect these gates from any negative potential. In addition, the metal-insulator-metal (MIM) capacitors, C_1, shunt any RF signals on the bias network to ground.

The NMOS ISO refers to NMOS *isolation* devices that are protected with an $n+$ diffusion in a p-well forming a diode *guard ring* into the substrate, in which the diffusion region is connected to the highest potential of the circuit (*Supply*). The node "R" refers to the protective diode ring, the "B" is the substrate bulk contact, "G" is the gate, "D" is the drain, and "S" is the source node connections.

This topology used a bigger inductor compared to topologies #2 and #3 due to a change in the comparison strategy that evolved after this design was initially created. Therefore, compared to the complementary MOS design, a higher inductance was used for the LC tuning. In this case, a total differential inductance of 0.7 nH was indicated, and implemented as a pair of 0.7 nH inductors ($L/2$). A dual inductor of this size is practical using the *P-CELLS* (primitive cells) provided in the Motorola design kit. Additionally, as explained earlier in this chapter, it is easier to get higher Q values for the frequency range of interest with inductors of this size. Larger inductors suffer higher parasitic capacitance and shift the peak Q to higher frequency ranges because of larger area overlap of the bulk substrate.

Additional capacitance was still required to tune the resonance of the oscillator to the specification frequency range. Therefore, two 2.37 pF capacitors (C_2), each occupying an area of 25.85 μm $\times$ 58 μm, were connected between the taps to the NMOS gates and the differential outputs. Both differential output nets utilize 38 individual varactors in parallel with a fully applied tuning bias voltage ($Vtune$) totalling a capacitance (C_{vvc}) of 148 pF. The number of varactors and size of the gates were chosen to meet the specified tuning range.

The primary goal of the topologies studied here was to meet the phase-noise specification of -156 dBc/Hz at 20 MHz offset from the carrier. To accomplish this, the transistors were sized to increase output signal power, at the expense of increased power consumption of the circuit. In addition, the NMOS devices are implemented with multiple fingers and decreasing gate resistance, thereby minimizing thermal noise. As mentioned in Chapter 1, the thermal noise is upconverted and contributes to the total close-in phase noise.

Figure 3.23(a) shows the drain currents of the two NMOS ISO transistors (M_1 and M_2). These devices have a gate voltage bias of 791 mV with a drain to source voltage (V_{DS}) of 2.15 V. Each device was implemented with 12 0.45μm $\times$ 20μm

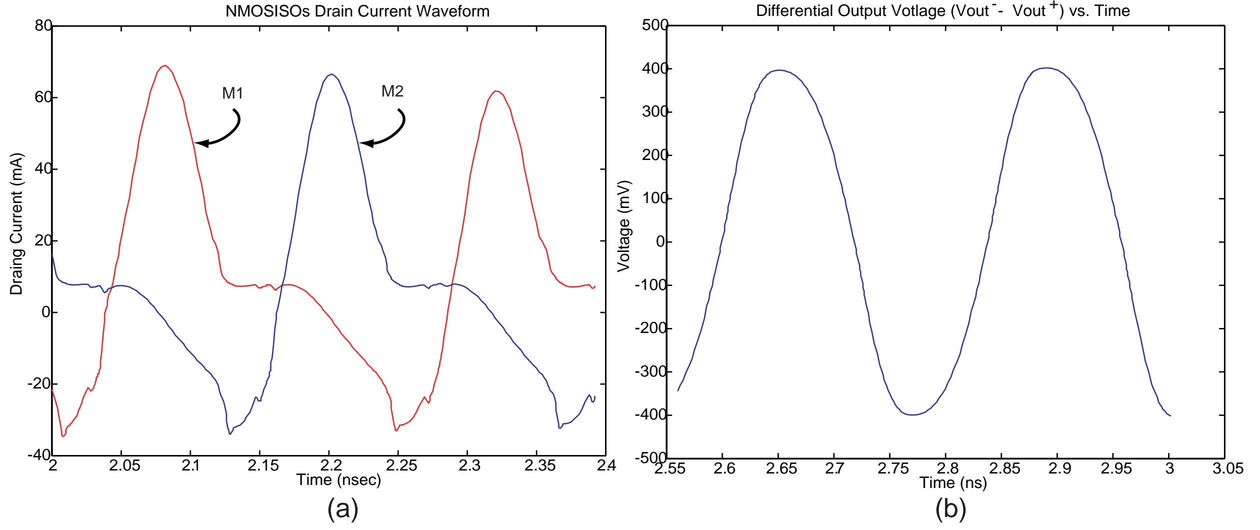


Figure 3.23: (a) NMOSISO current waveforms for both negative resistance transistors have a peak amplitude of 69 mA. (b) Topology #1 has a very high swing voltage due to the single-pair, cross-coupled NMOS transistors.

fingers in parallel. The increased DC current bias of 9.1 mA (18.2 mA overall) for each transistor resulted in an unsatisfactory 45.54 mW of power consumption. A capacitive divider network was implemented to lower the output voltage swing to avoid compression of the buffer circuit. This topology proved to have the highest voltage swing of all three types of cross-coupled topologies studied, with a peak of 4.09 V [Figure 3.23(b)]. The capacitive dividers lower the output voltage swing to approximately 400 mV. It should be noted that the output voltage waveform is not purely sinusoidal, because of the relatively low-Q LC tank circuit. This is due to the limitations of implementing an integrated high-Q LC filter circuit. A high impedance load of 1 kΩ was used in these simulations in place of a high input impedance buffer.

This topology proved to have very successful phase-noise simulation results. However, these results only illustrate the modeling of specific parasitic effects, and therefore can only be viewed as an estimation. Figure 3.24 shows the simulated phase-noise performance of this topology, which met the 20 MHz offset specification. As expected, the capacitive dividers divide the signal output sufficiently without affecting oscillator phase-noise performance. However, this performance comes with a major trade-off in power consumption. The 45 mW power consumption was deemed to be unacceptable; therefore, a second MOS topology was pursued.

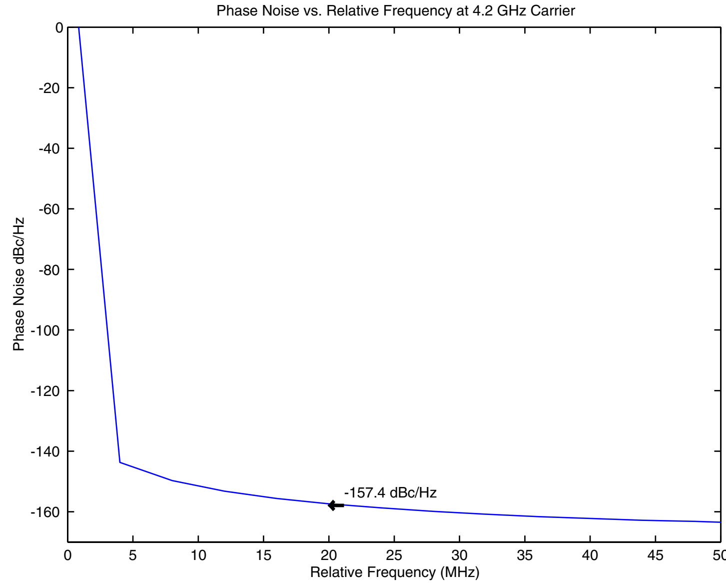


Figure 3.24: Simulated phase noise of MOS Topology #1. The design meets phase-noise requirements at 20 MHz offset.

3.6.2 MOS-Topology #2: Cross-Coupled Complementary MOS Pair

The second MOS topology considered was the complementary MOS cross-coupled pair (Figure 3.25). It was found that this type of topology served to be best in terms of power consumption and phase-noise performance trade-offs. A complementary MOS VCO can be viewed as a cross-coupled pair of inverters (Figure 3.26). Both PMOS and NMOS pairs contribute to the negative resistance $\frac{-2}{G_{M_p}+G_{M_n}}$ of the VCO. At DC, the inverter outputs are shorted to the gate inputs, creating a negative feedback loop. The bias point is controlled so that the input and output levels are the same. The PMOS device widths are sized to be twice that of the NMOS devices. This results in the input and output bias voltages being set to $\frac{V_{DD}}{2}$. The inverters now act as high-gain linear amplifiers rather than digital logic switches. The graphs in Figure 3.27 show between 10% and 90% of full-scale of V_{dd} that the rise time for the PMOS (W = 150 μm, $L = 0.9$ μm) is about 277 ps, and the NMOS ($W = 60$ μm, $L = 1$ μm) fall time is about 240 ps. The combination of rise and fall time must remain symmetric; since asymmetry contributes to phase noise (see Section 2.2.5). Therefore, increasing the size of the NMOS was achieved so that there was an effective negative resistance

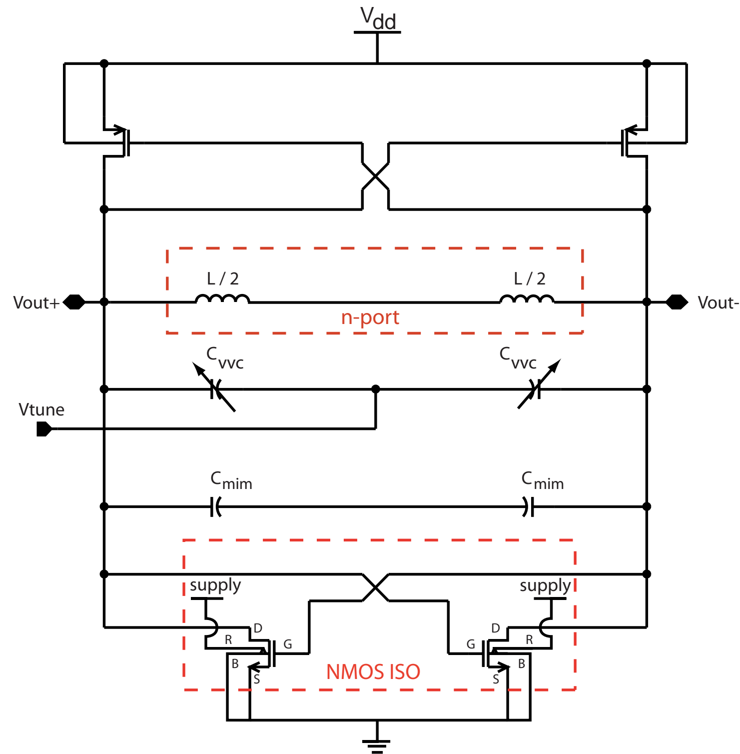


Figure 3.25: The topolgy #2 of a cross-coupled complementary MOS VCO.

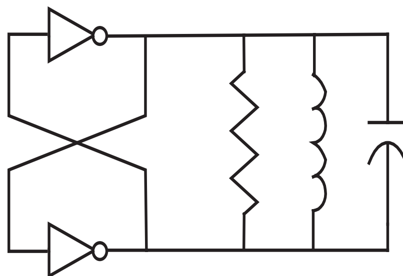


Figure 3.26: The complementary MOS pair is simply a cross-coupled pair of inverters connected to an LC tank network. The width of the devices were increased to achieve a DC bias operating point of $\frac{V_{DD}}{2}$. However, this causes a discrepancy in matching the rise and fall times of the inverter.

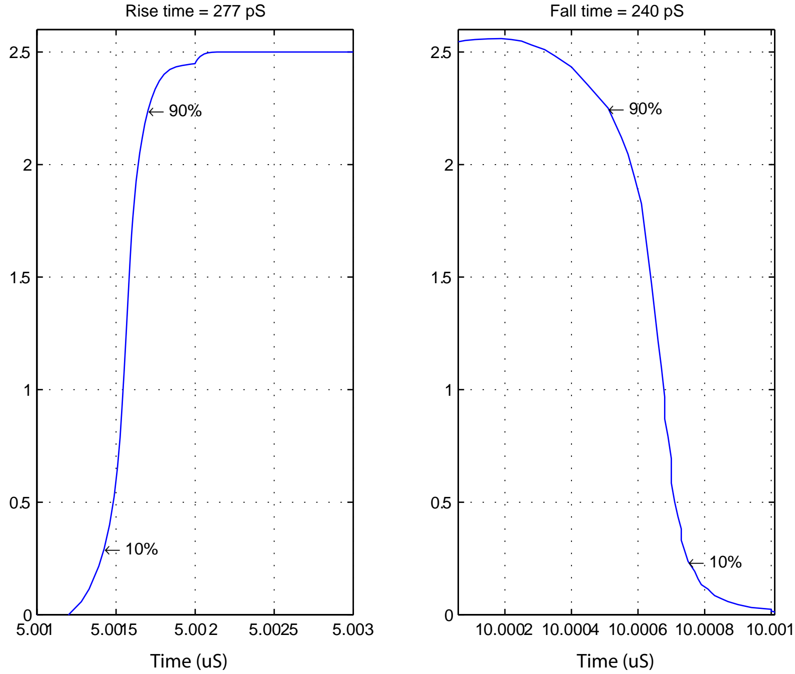


Figure 3.27: The time quantity is determined between the 10% and 90% of V_{DD}. The rise time for the PMOS 277 ps (width = 150 μm and length = 0.9 μm) and the fall time of the NMOS (width = 60 μm and length = 1 μm) is 240 ps.

and approximately equal rise and fall transition times (off by only 37 ps). No ESD protection diodes were implemented in this design.

With V_{dd} = 2.5 V, the headroom voltage allocated for both the PMOS and NMOS differential negative resistance amplifiers has an effect on the actual phase noise. Recall that signal power (P_{sig}) plays a vital role in the phase noise of an oscillator. However, the trade-off for this phase noise outcome can be seen as a significant reduction in circuit power consumption. Modifying the PMOS device width changes the DC voltage across the pull-up device and the drop across the NMOS pull-down devices. Table 3.2 describes the different types of variations explored with the PMOS device, with a fixed NMOS value of (W=60 μm, L=1 μm). These modifications inherently change the DC biasing of the negative resistance inverter amplifier. In addition, such biasing will slightly vary the operating region of the devices that is directly proportional to the current I_{DS}. For example, implementing the PMOS device with a width and length of 70 μm $\times$ 0.9 μm creates a larger voltage drop across the V_{DS} of the PMOS. Therefore, the available V_{DS} for the NMOS is only about 570 mV,

PMOS W (μm)	# Parallel PMOS	NMOS V_{DS}	Output Swing (V_{p-p})	I_{DS}
70	1	515 mV	700 mV	11 mA
70	2	609 mV	1.35 V	41 mA
100	1	534 mV	800 mV	15 mA
150	1	558 mV	2 V	47 mA

Table 3.2: Adjustments to the PMOS width will change the amount of bias current allowed to the NMOS and will also set the voltage swing of the output signal. Simulations of all modifications include NMOS ISO with width, length, and number of gates to be 30 μm, 1 μm, and 3, respectively.

Rx CMOS VCO	NMOS Width	NMOS Length	# of Gates	PMOS Width	PMOS Length	Power
	30 μm	1 μm	3	70 μm	0.9 μm	22 mW
f_Δ offset	$f_\Delta = 400$ kHz		$f_\Delta = 3$ MHz		$f_\Delta = 20$ MHz	
Phase-Nosie	-100 dBc/Hz		-130.7 dBc/Hz		-148 dBc/Hz	

Table 3.3: Simulated (carrier frequency is 3.8 GHz) the receiver (Rx) CMOS comparison of device sizes, phase noise, and power consumption.

which results in less available transconductance ($g_m \propto I_{DS}$). This results in a very low amplified output voltage swing of 700 mV peak-to-peak and a current drain of 11 mA. The final fabricated circuit containing a PMOS device with a width of 150 μm increases the voltage swing to 2 V peak-to-peak, but this increased drain current consumption to 45 mA. These figures were desired to increase signal power to reduce phase noise.

Two types of complementary MOS VCO circuits were implemented. Within both MOS VCO designs, a fixed inductor was used to maintain a constant quality factor so that an accurate comparison could be extracted for this thesis. The first design was the receiver (Rx) VCO, which utilized smaller NMOS transistors and minimized current consumption. Table 3.3 shows the detailed parameters of the active devices used for the negative resistance circuit and the corresponding phase noise and power consumption. The second design was the transmitter (Tx) VCO with the fabricated design parameters detailed in Table 3.4. The transmitter VCO required larger devices to increase the signal power of the VCO to meet phase-noise specifications that were more stringent than the receiver design. To minimize $1/f$ noise upconversion within

Tx CMOS VCO	NMOS Width	NMOS Length	# of Gates	PMOS Width	PMOS Length	Power
	60 μm	1 μm	4	150 μm	0.9 μm	26.6 mW
f_Δ offset	$f_\Delta = 400$ kHz		$f_\Delta = 3$ MHz		$f_\Delta = 20$ MHz	
Phase-Noise	-114 dBc/Hz		-138 dBc/Hz		-156.73 dBc/Hz	

Table 3.4: Simulated (carrier frequency is 3.8 GHz) the transmitter (Tx) CMOS comparison of device sizes, phase noise, and power consumption.

the output phase noise, the NMOS and PMOS devices were sized so that the switching rise and fall times were similar. Figure 3.28 compares the phase-noise performance of the receiver and transmitter VCOs, which have similar tank Q-factors. It is obvious that higher current consumption is needed to reduce phase noise at 20 MHz offset (ω_Δ) frequency. These simulations show that the phase noise for these large offset frequencies were met.

The layout of the MOS VCO topologies are exactly the same for both the receiver (3.2-3.8 GHz) and transmitter (3.4-3.8 GHz) circuits. The layout is shown in Figure 3.29, which includes the buffer, varactors, inductor, and active devices. Both MOS designs incorporated a 520 pH dual octagonal spiral inductor, as described in Section 3.1.1. While the multi layered metal cross-under was explored in this study (Section 3.1.1), only a metal 4 cross-under was fabricated to limit any parasitic coupling. The accumulation-mode varactors, C_{vvs}, were sized to have 30 fingers, with a channel length of 1.35 μm and a width of 6 μm to give a tuning range of 500 MHz. There were two major differences between the layouts of the transmitter and receiver VCO. First, the MOS receiver VCO design consisted of smaller active devices, which resulted in a significant reduction in parasitic capacitances. Second, to compensate for this reduction in parasitic capacitance, a much larger pair of fixed *metal-insulator-metal* (MIM) was inserted, which are noted as C_{mim} in the schematic. The transmitter layout, which required additional capacitance of 301 fF MIM, was designed using two parallel (*metal3-insulator-metal4*) capacitors with dimensions of 10.14 $\mu m \times 9.15$ μm. The receiver utilized a larger 4 pF MIM capacitor with two parallel capacitors with the dimensions of 50 $\mu m \times 25.3$ μm. The overall VCO layouts were implemented in completely symmetric fashion occupying an area of 1 mm x 0.943 mm (943 mm^2),

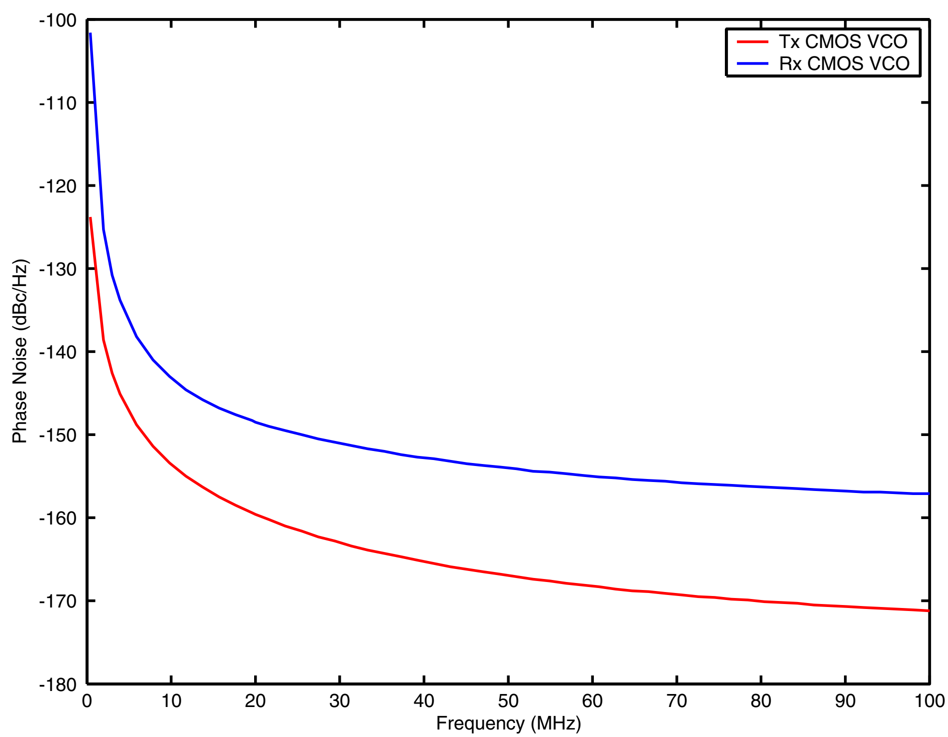


Figure 3.28: Phase-noise simulation for the CMOS transmitter and receiver VCO implementations.

including the buffer design (200 $\mu m \times 120$ μm in size).

3.6.3 HBT-Topology #3: Cross-Coupled HBT Pair

An important emphasis of this thesis was an examination of the advantages and disadvantages in using MOSFETs and SiGe HBTs for integrated RF VCOs. This comparison focuses on both power consumption and phase-noise performance. For a fair comparison, the quality factor of the tank circuit must remain equal between both the MOS and HBT topologies. The same inductor was used in HBT Topology #3 as the receiver and transmitter in MOS Topology #2. The HBT implementation is illustrated in Figure 3.30, which shows the base bias, current reference, and tail current source circuits. Due to the lack of wafer die area, only one HBT topology could be fabricated. Therefore, to challenge the performance of the MOS VCO circuits for this thesis, the HBT transmitter VCO was selected because of its more stringent phase noise specifications.

The HBT VCO topology has a dramatically lower amount of parasitic capacitance compared to the previous MOS designs. As explained earlier, the inductor should remain the same as that used in the MOS topology to provide a fair comparison. Therefore, to achieve a proper tuning range, more parallel capacitance was needed. Similar to MOS Topology #2, accumulation mode NMOS varactors (C_{VAR1} and C_{VAR2}) were used in this circuit. These varactors were designed using the same configuration of 30 finger NMOS gates with channel sized at 1.35 μm $\times$ 6 μm. To correctly shift the desired tuning range of the VCO circuit to the specified transmitter frequencies, additional 6 pF MIM capacitors (C_1 and C_2) were therefore added. A layout of the the HBT transmitter VCO is shown in Figure 3.31.

The negative resistance ($-G_m$) circuit was similar to that of MOS Topology #1, with a cross-coupling between the base and collectors. A time-domain output of this cross-coupling oscillation is illustrated in Figure 3.32. The HBT negative G_M (Q_1 and Q_2) emitter areas were sized at L_e x $W_e = 0.4$ μm $\times$ 10 μm. It has been shown that increasing emitter size can reduce $1/f$ noise [67]. However, increasing emitter size can drastically increase current consumption. In addition, large base resistances (R_B) were placed at the bases of these negative resistance devices to limit RF leakage from the oscillator into the bias circuit.

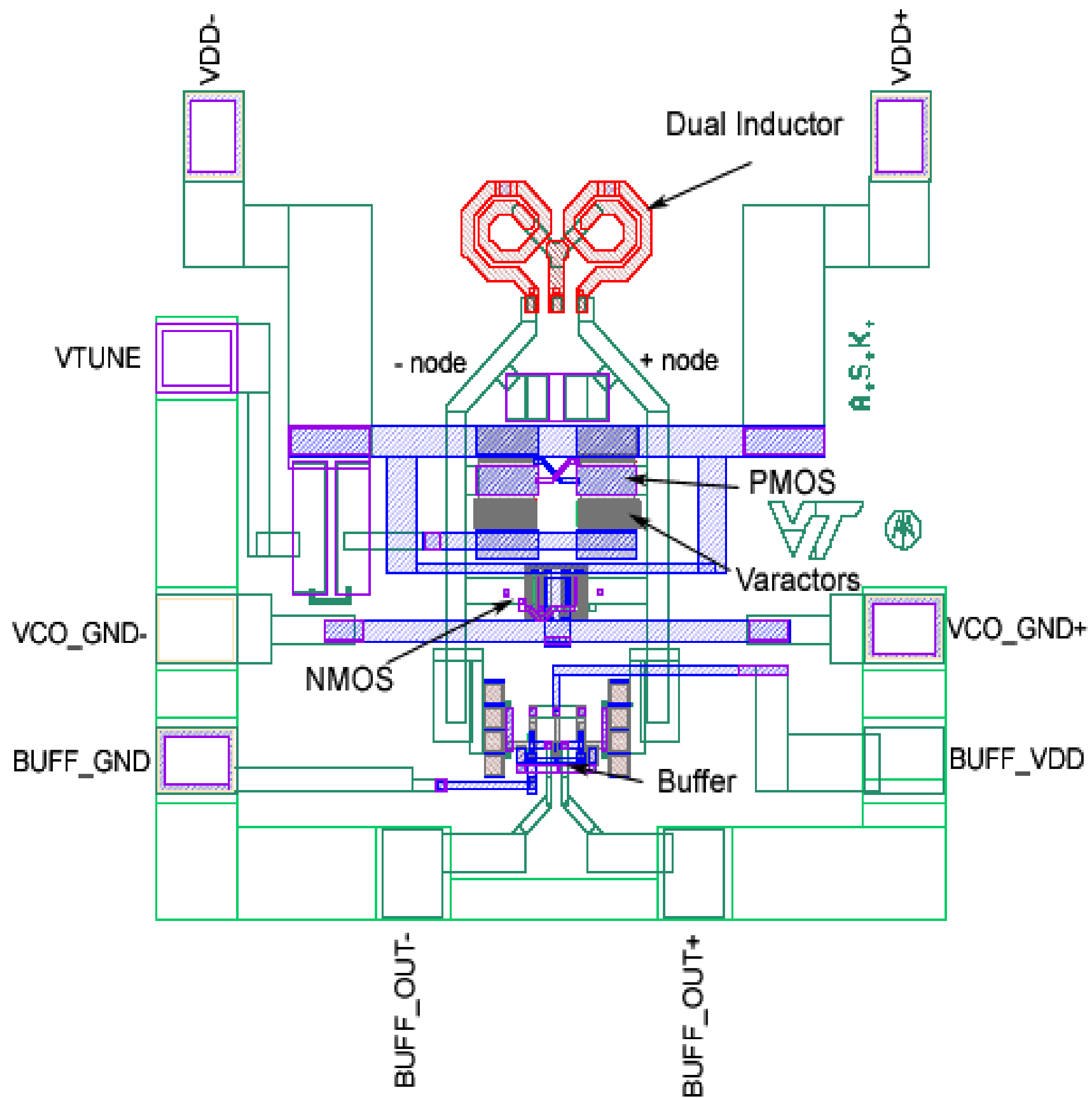


Figure 3.29: Fabricated MOS Topology #2 receiver and transmitter VCO. Layout includes buffer design at the output.

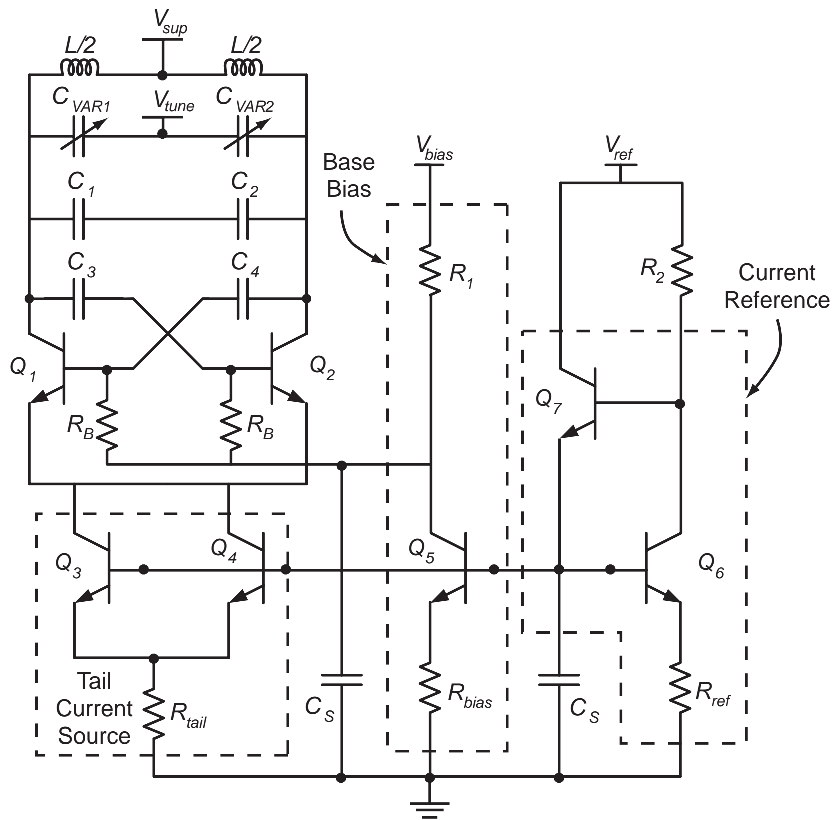


Figure 3.30: Schematic of the SiGe HBT transmitter VCO topology with tail current source, base bias, and current reference circuitry.

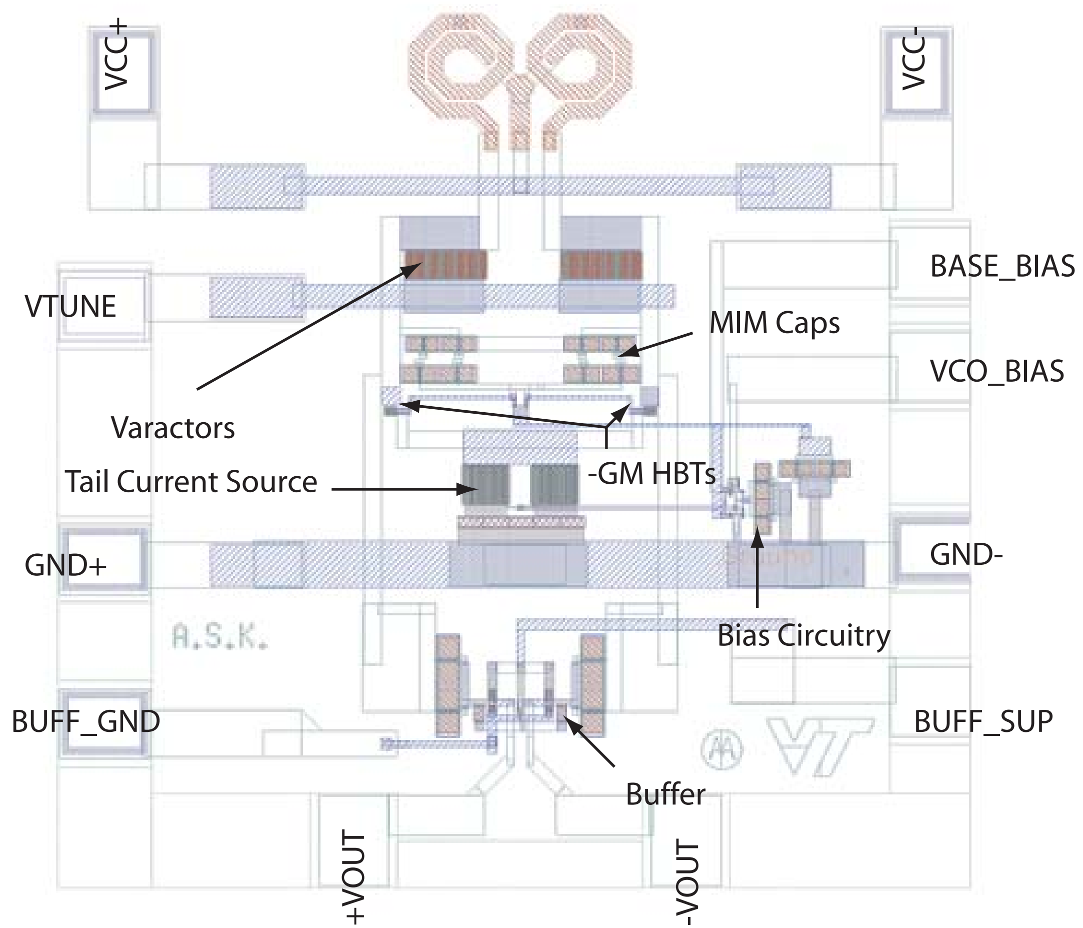


Figure 3.31: Layout of the HBT transmitter VCO topology.

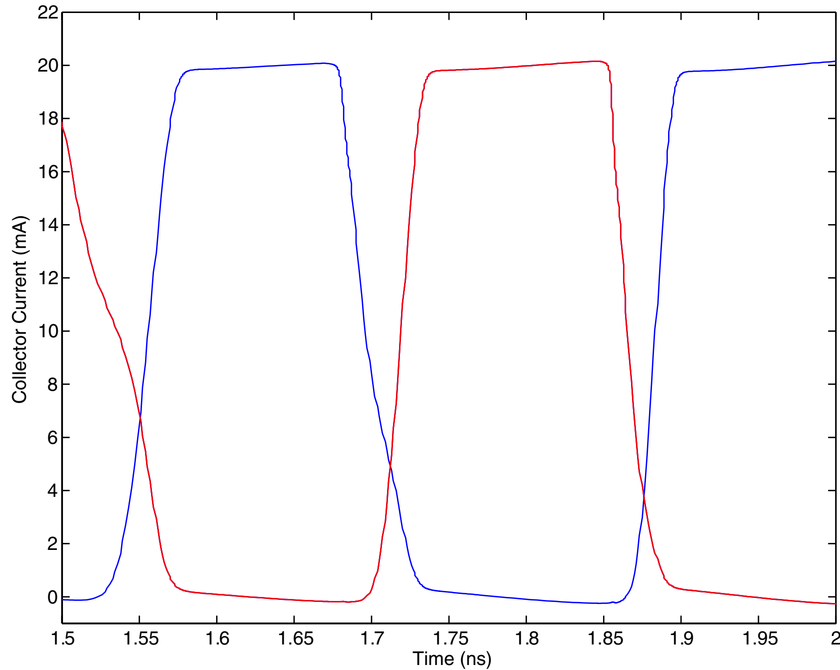


Figure 3.32: Simulated time-domain current waveforms of the HBT transmitter VCO.

The biasing of the HBT circuit requires more attention and is more complex than the MOS topologies. To maintain proper symmetry within the VCO tail bias, dual tail current sources (Q_3 and Q_4) were laid out as mirror images. This made layout much more symmetric when isolating devices between the differential nodes. The transistor Q_7 is the "beta helper" transistor and improves the gain for the mirrored in transistors Q_3, Q_4, and Q_5. The current reference is sized so that it provides proper biasing to both the base of the current sources and the negative resistance transistors. Each of these bias transistors (Q_3, Q_4, Q_5, and Q_6) were implemented with emitter degeneration resistors. The addition of emitter generation increases the output impedance of the current mirrors. Emitter degeneration has the benefit of adding additional stability at the current mirror to reduce such variations at the base bias.

Phase-noise simulations of the HBT design indicated no significant improvement at the large offset frequencies (20 MHz) compared to the MOS topologies. Simulations showed an approximately -145 dBc/Hz at a 20 MHz offset, and -119 dBc/Hz at a 400 kHz close-in phase noise were achieved (Figure 3.33). These results were achieved

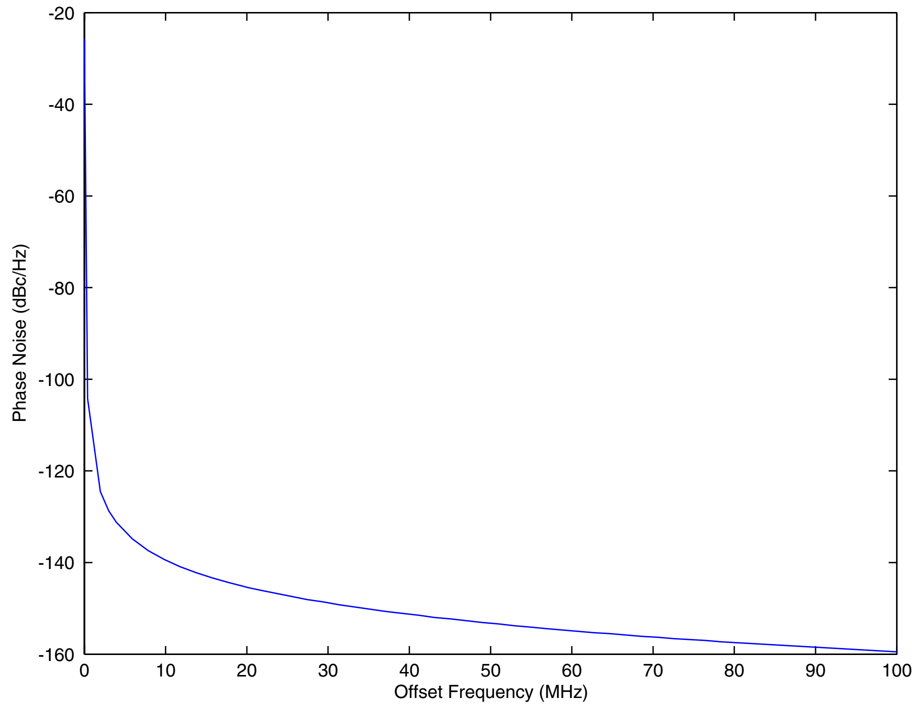


Figure 3.33: Simulated phase noise for the HBT transmitter VCO.

with roughly 17.4 mA of current consumed by the VCO core, which is much lower than the MOS designs. It was hoped that the lower $1/f$ noise from the HBT devices would result in a much lower phase noise compared to that of the MOS topologies.

3.7 Summary

This chapter has presented the design and simulation of the passive components (monolithic inductors and MOS varactors) that were used in the VCO tank circuit. This included a thorough analysis of the contributing losses within monolithic inductors and the results of full-wave electromagnetic simulations. The tuning characteristics of the available accumulation mode varactor was also illustrated. An explanation of the MOS output buffer circuit that was integrated with all designs was also discussed. Design flow charts detailing some of the causes and effects that arise when implementing a monolithic VCO were also established. A description of the non-linear simulator used to characterize the phase noise was introduced. This

includes several recommended settings for accurate SpectreRF. Finally, an overview and comparison of the VCO topologies considered was presented, including a single-pair cross-coupled NMOS design, a cross-coupled complementary MOS design, and a cross-coupled HBT design with emitter degeneration resistors.

Chapter 4

Fabrication and Measurements

The two thrusts of this thesis are the design and characterization of Si-based 3-4 GHz VCOs for GSM/EDGE applications, and exploration of a new I/Q phase measurement technique for a 5-6 GHz VCO with integrated tunable polyphase filter. All circuits in this thesis were fabricated in the Motorola 0.35 μm CDR1 SiGe BiCMOS process. Complementary MOS transmitter and receiver VCO topologies (Section 3.6.2) and a cross-coupled HBT transmitter VCO (Section 3.6.3) topology were fabricated. A microscope photograph of the fabricated reticles is shown in Figure 4.1. Stand-alone structures were also included on the reticles for on-wafer characterization of the differential dual octagonal spiral inductor design. This chapter first presents fabrication and packaging issues that arose with outsourcing the HBT VCO dies. A comparison between measured and simulated results for the inductor structure is also presented in this chapter. Finally, this chapter discusses a new time-domain measurement technique for the characterization of I/Q phase performance of polyphase filters. This method is compared to the existing s-parameter (frequency domain) approach completed in previous research.

4.1 Packaging and Test Boards

The 1 mm $\times$ 1 mm 3-4 GHz VCO dies were packaged using Amkor MicroLead Frame-2 (MLF-2) 12 pin 4 mm $\times$ 4 mm packages (2.3 mm $\times$ 2.3 mm die flags). This packaging included an encapsulation process that prevented any post-packaging rework.

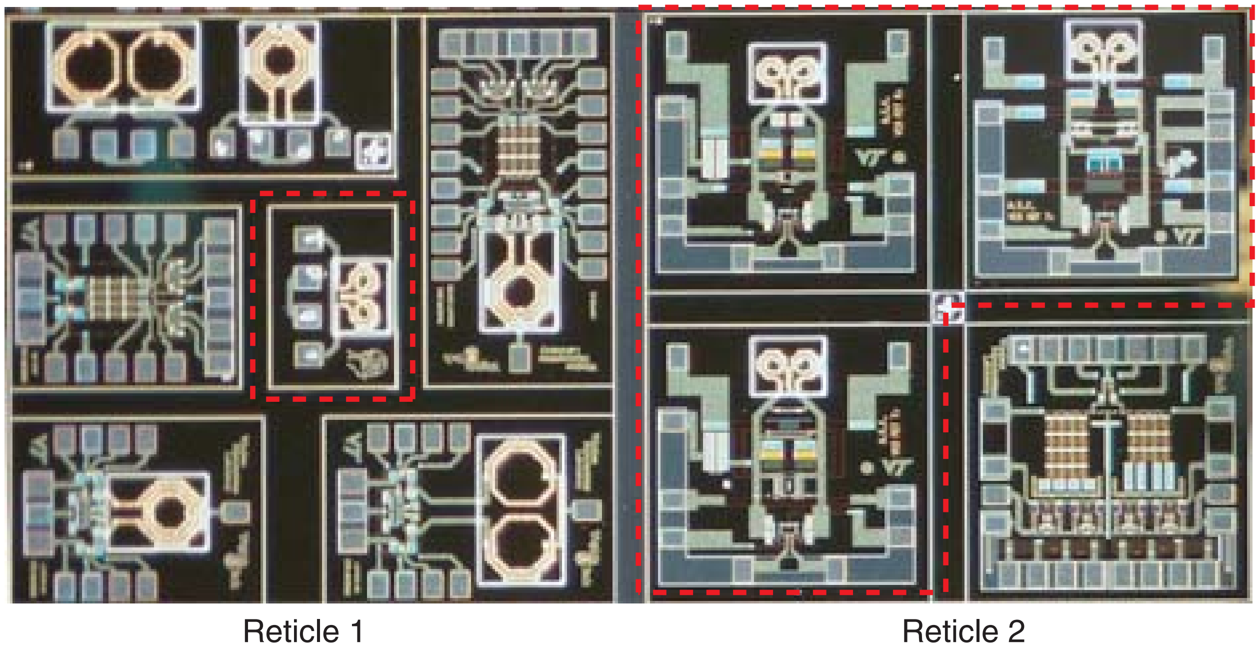


Figure 4.1: Fabricated circuits were laid out within two reticle areas on a CDR1 engineering mask. Reticle 1 contained the dual octogonal spiral structure for on-wafer probing, the 5-6 GHz tunable polyphase filter and VCO. Reticle 2 contained the 3-4 GHz GSM/EDGE VCO circuits. The red dashes are the circuits assigned to the 3-4 GHz GSM/EDGE research.

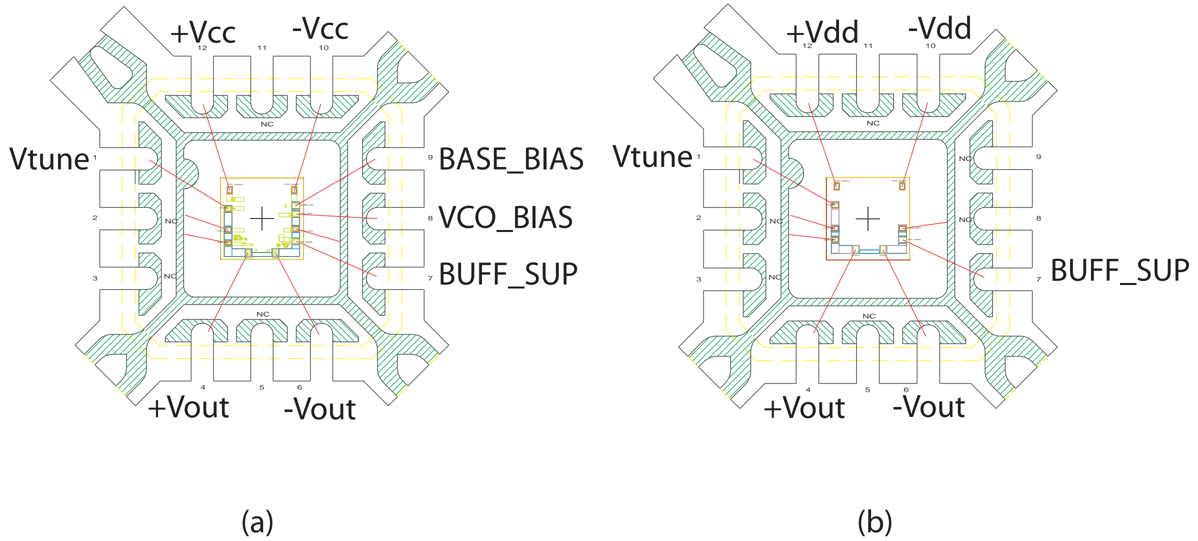


Figure 4.2: Wirebond assignment diagrams for the (a) 3-4 GHz HBT Tx VCO and (b) MOS Tx/Rx VCO, packaged in MLF-type packages.

MLF-2 packages are designed to reduce parasitics for high-frequency outputs. The wirebonding diagrams for both the HBT and MOS VCOs are illustrated in Figure 4.2(a-b).

The packaging was outsourced to Amkor by Motorola. Unfortunately, an incorrect wirebond was made on the *VCO_BIAS* pin of the packaged HBT VCO (Figure 4.3). The incorrectly ground-bonded pin resulted in the VCO bias circuitry to be permanently shorted to ground, forcing the oscillator into an off-state.

Fortunately, additional reticles were available from an unsawed section of the original wafer retained at Motorola. Consequently, a number of circuits could be used from an unsawn quarter section of the wafer, which were used following the on-wafer inductor characterizations (explained in the next section) and subsequently packaged in an open-face (nonencapsulation) MLF-type package at RFMD (Figure 4.4). The open-face package was a precautionary measure to verify that correct wirebonding was made.

Meanwhile, the VCO with tunable polyphase outputs was also intended for packaging by Amkor. However, the wafer containing these unsawn circuits were irrevocably damaged during packaging. The unsawed wafer section on hand (used for the on-

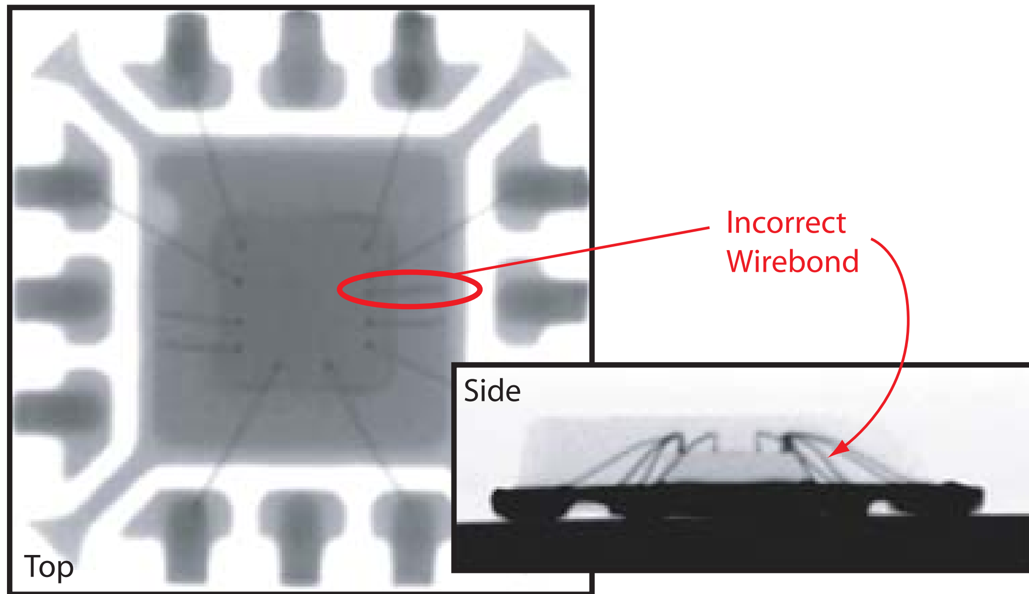


Figure 4.3: X-ray views (top and side) of the incorrectly wirebonded *VCO_BIAS* pin in the HBT Tx VCO.

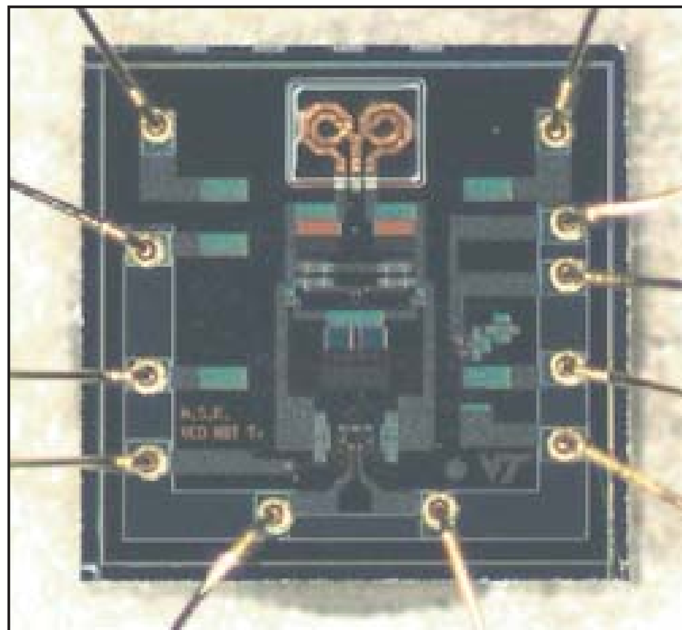


Figure 4.4: Fabricated HBT Tx VCO in an MLF open-face package.

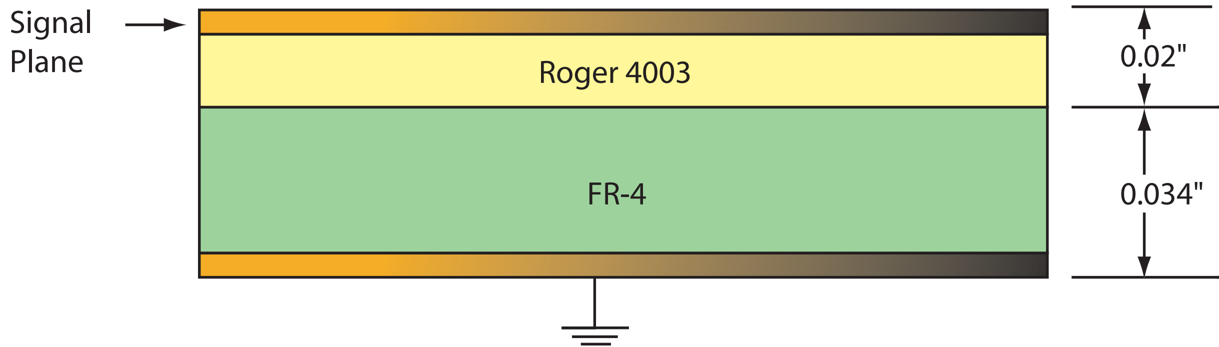


Figure 4.5: The cross-sectional representation of the board material used. Ground plane is the bottom most metal layer.

wafer inductor measurements) had several tunable polyphase VCO sites available. These sites were subsequently diced by Motorola and again packaged at RFMD.

Test boards were also designed for fabrication by Motorola SPS. The test board configuration consists of two layers: the top layer is a 0.02 inch (0.508 mm) Rogers 4003 and a 0.034 inch (0.8636 mm) FR4 bottom layer (Figure 4.5). The traces of metal are plated with 1 ounce copper. Since all three GSM VCO design layouts incorporated similar packaged pin assignments, they all used the same board design [Figure 4.6(a)]. The 5-6 GHz VCO with polyphase test board is shown in Figure 4.6(b).

4.2 On-Wafer Inductor Characterization

As mentioned above, an unsawn wafer section was set aside to support on-wafer probing of differential dual octagonal spiral inductor test structures. Measurements were accomplished using a Cascade MicroTech probe station with ACP-50 GSG RF probes coupled to an HP 8510C vector network analyzer (VNA). The network analyzer was used to collect two-port, S-parameter data from the inductor test structures. The physical layout of the inductor pads were incorrectly designed to be compatible with the SGGS probes with a 150 μm pitch [Figure 4.7(a)]. Unfortunately, the only probes available were ground-signal-ground (GSG) probes. Therefore, the two-port measurements required two GSG probes that had a floating ground connector [Figure

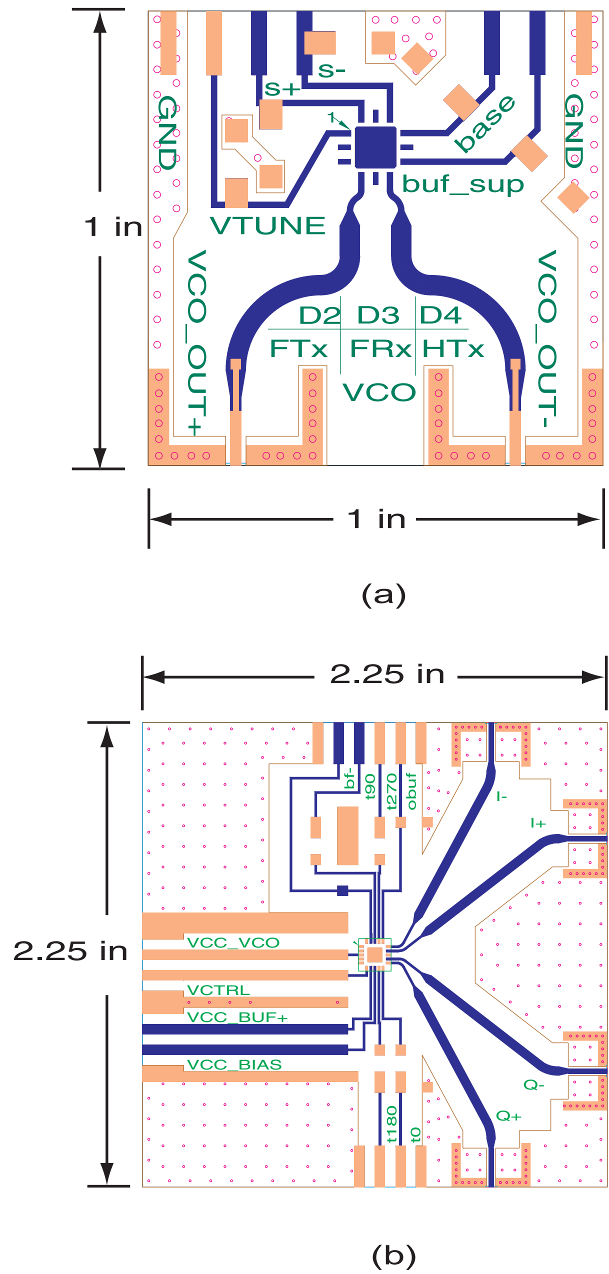
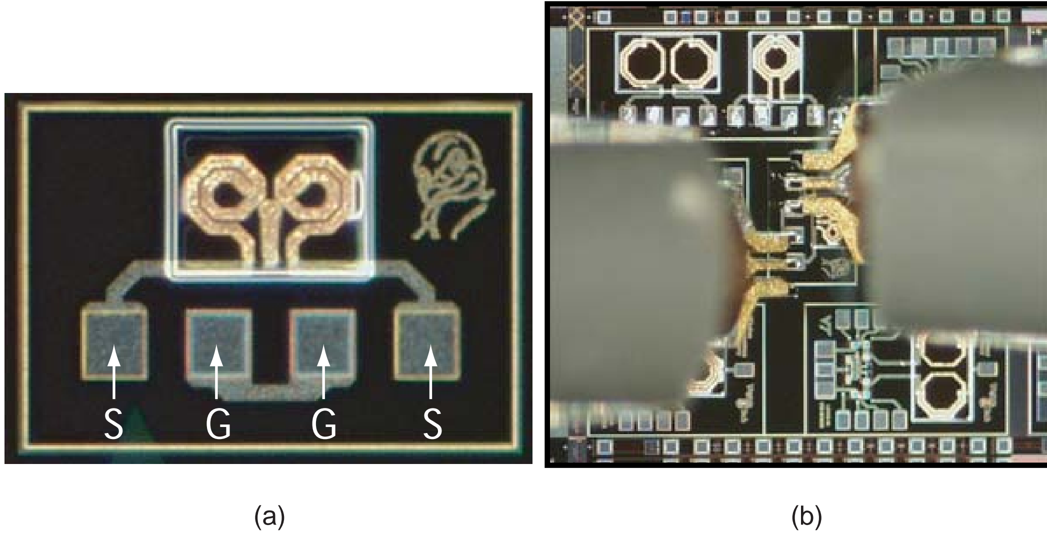


Figure 4.6: Test board layouts for the (a) Complementary MOS Tx/RX VCO and HBT Tx VCO and (b) UNII band VCO with polyphase outputs.



(a) (b)

Figure 4.7: (a) Fabricated differential dual inductor CDR1 SiGe BiCMOS structure for on-wafer testing in technology. (b) Inductor structures being probed using Cascade MicroTech G-S-G probes.

4.7(b)]. The probes themselves consist of their own unique lumped-element model that must be calibrated out using standards.

Short-Open-Load-Thru (SOLT) standards were available on the Cascade Impedance Standards Substrate (ISS) used to calibrate the VNA reference plane to the probe tips. Then two-port, S-parameter measurements were taken for the differential inductor structures. This S-parameter data includes the pad parasitic capacitance and resistance. Therefore, deembedding of the pads was necessary. Unfortunately, on-wafer structures for deembedding the pad parasitics were not included due to space limitations. Consequently, deembedding the pads was accomplished using simulated S-parameter data for the appropriate pad configurations using Sonnet EM. To accomplish the deembedding, the Y-parameters for the *open* standards, Y_{open}, derived from the Sonnet simulated pads are subtracted from the measured DUT (inductor) Y-parameter data ($Y_{DUT(open)}$) [Figure 4.8(a)]. The Y-parameters were computed from the S-parameters using Matlab code explained in [20]. Next, the Y-parameters of the *short* standards are simulated (Y_{short}). The Y-parameters of the open standards (Y_{open}) are subtracted from the simulated Y-parameters of the short standards of the Sonnet pad data, yielding $Y_{short(open)}$ [Figure 4.8(b)]. Finally, the Z-parameters of the open-corrected short standard Sonnet data ($Z_{short(open)}$) are subtracted from

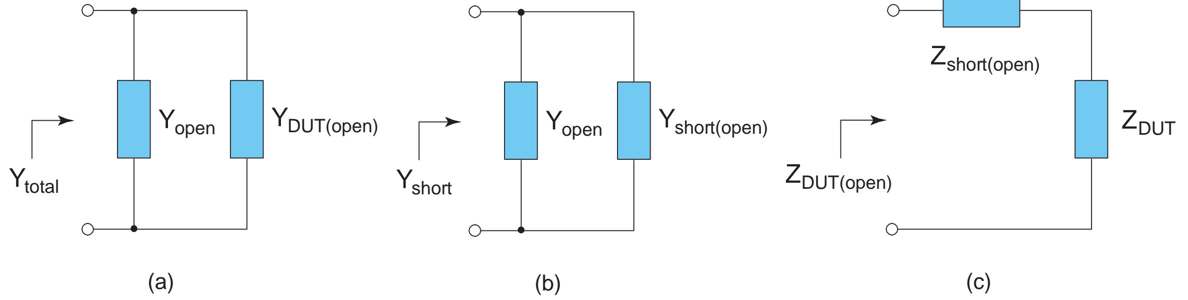


Figure 4.8: (a) Y-parameters of the open standards are subtracted from total measured data. (b) Y-parameters of the open standards are subtracted from Y-paramters of the short standards. (c) Z-parameters of the open-corrected short standard are subtracted from the Z-parameters of the open-corrected inductor structure [20].

the Z-parameters of the open-corrected measured inductor structure (Z_{DUT}) [Figure 4.8(c)]. Conversion to Z-parameters allows for the removal of the pads series loss from the open-corrected Z-parameters of the shorted pads from the open-corrected Z-parameters of the DUT.

Figure 4.9 shows the simulated and deembedded measured effective inductance and Q factor for the dual inductor structure. As can be seen, there is a significant difference between the simulation results and the actual measured values. The measured effective inductance is approximately 12% larger than that of the Sonnet simulated results over the 3-4 GHz design frequency range. A major reason for the large deviation may be the measurement sensitivity of the inductor structure to parasitics. Recall that the inductors used are relatively small structures (approximately ~ 130 μm $\times 240$ μm). Meanwhile, the probe pads are each 94.8 μm $\times$ 106.25 μm, which can contribute significant additional parasitics that dominate the measurements. Also, the deembedding process used here relied on simulated standards rather than actual measurements of calibrated pad structures. Therefore, a large error in conjunction to a very sensitive inductive structure results in large deviations from the simulations.

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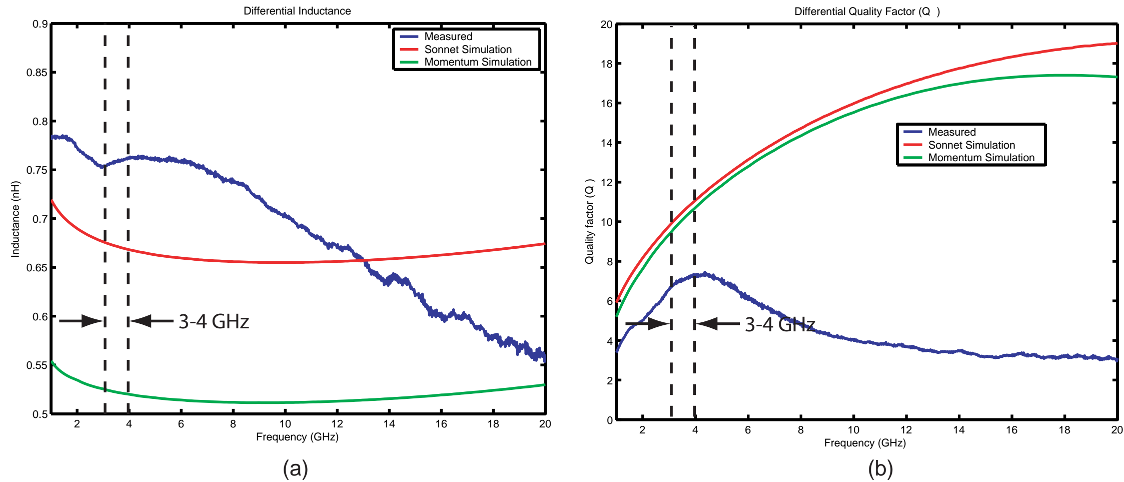


Figure 4.9: Comparison of measured and simulated (a) effective inductance and (b) Q factor versus frequency for the dual inductor structure.

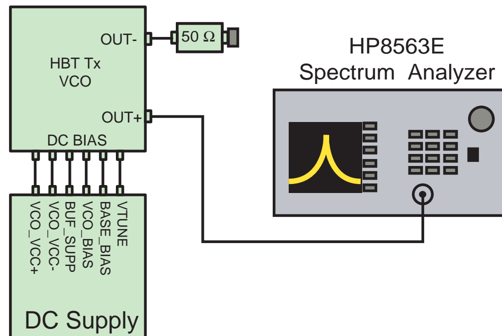


Figure 4.10: Test measurment setup for the HBT Tx VCO.

4.3 2x/4x HBT Transmitter VCO Measurements

The test measurement system for the HBT Tx VCO simply required DC power supplies and a spectrum analyzer (Figure 4.10). All DC supplies were shunted with large capacitive filters to clean up high frequency noise produced at the sources. An HP 8563E spectrum analyzer was used to measure each of the differential output signals individually. The unmeasured output was terminated with a 50 ohm load.

The measured 2x/4x HBT VCO results revealed three important issues. First, output harmonics were present at the output of the buffers (Figure 4.11). Subsequent

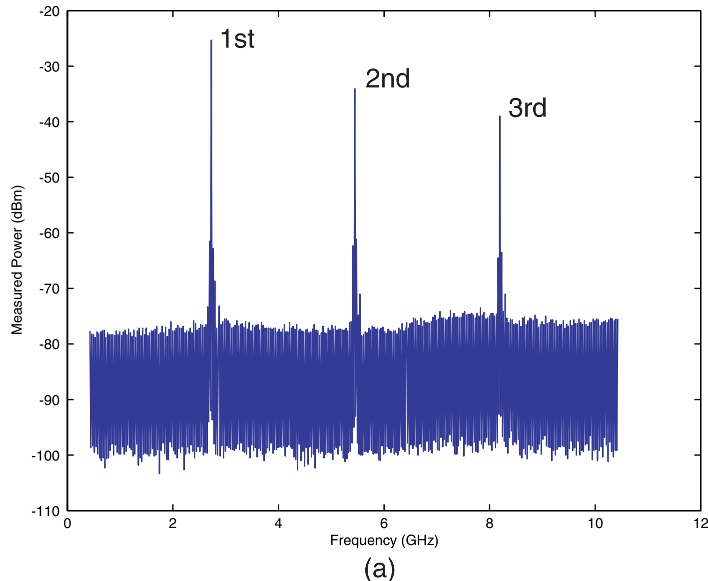


Figure 4.11: Measured VCO output spectrum (after buffer amplification).

simulations show that the VCO does not have any significant output harmonics and that the non-linearities of the buffer circuit are responsible for generating the harmonic content (Figure 4.12). Simulations show that the second harmonic produced compared to the fundamental is -17 dBc. Future designs must better control the non-linearities of the output buffers to avoid such harmonics.

The measurements also showed that the fundamental VCO frequency is shifted down to the 2.3-2.7 GHz range. It was concluded that this shift is due to excess parasitics of approximately 4.5 pF. Therefore, given that the measured effective inductance appears to be 750 pH, the resulting oscillation frequency would be approximately 2.7 GHz.

Tuning curves were taken using single-ended measurements where the -V_{OUT} pin was terminated with a 50 Ω load and the +V_{OUT} pin was connected to an HP 8563E Spectrum Analyzer. The measured oscillator tuning curve is illustrated in Figure 4.13. The slope in the linear region of the curve describes the tuning sensitivity of a VCO and can be expressed as the VCO gain:

$$K_v = \frac{\Delta f_o}{\Delta V_{ctrl}} \tag{4.1}$$

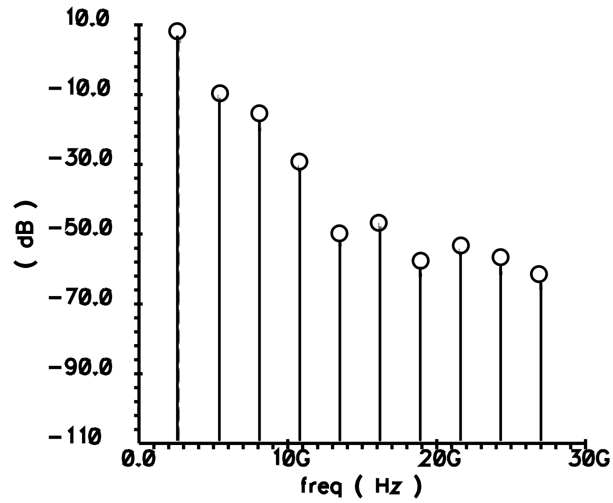


Figure 4.12: Simulated output harmonics of a stand-alone buffer.

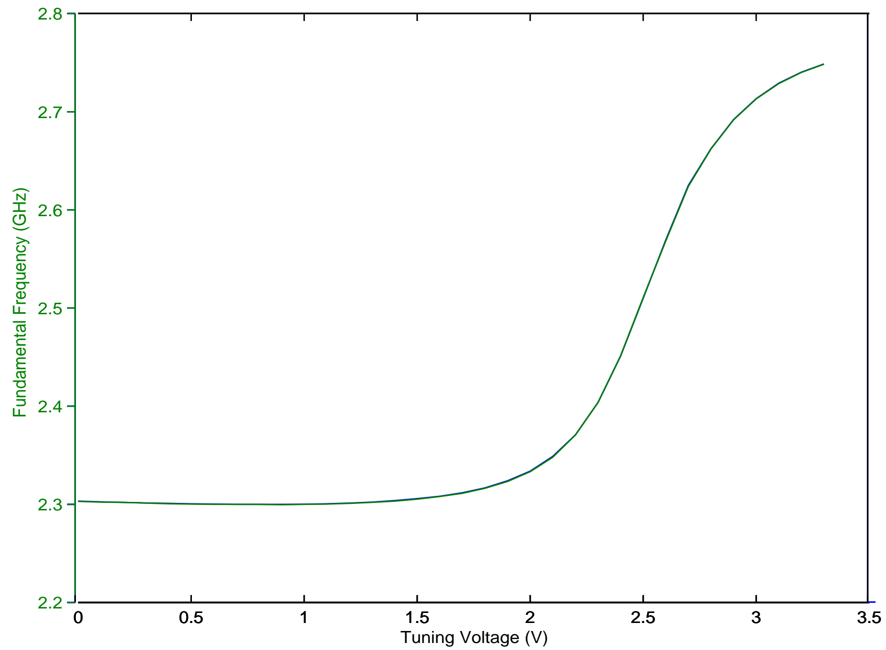


Figure 4.13: Measured HBT VCO tuning curve showing the fundamental harmonic frequency vs. tuning voltages.

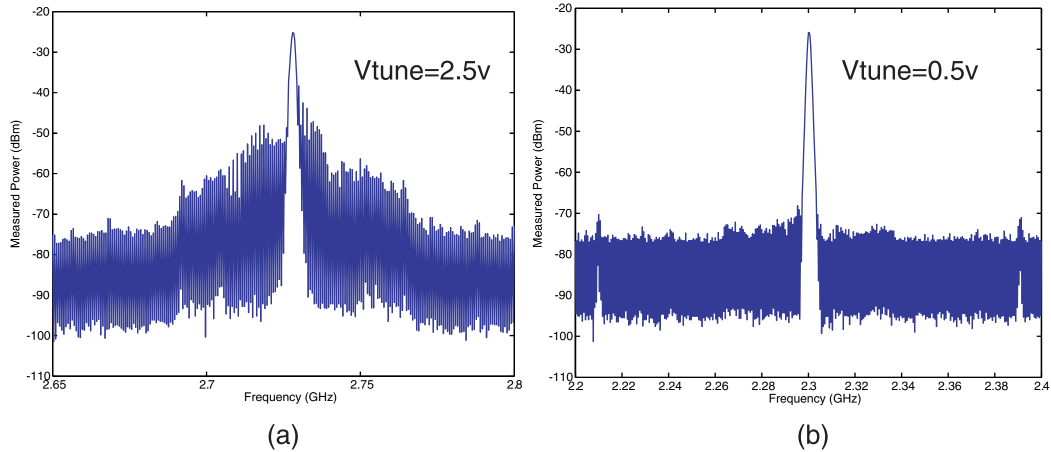
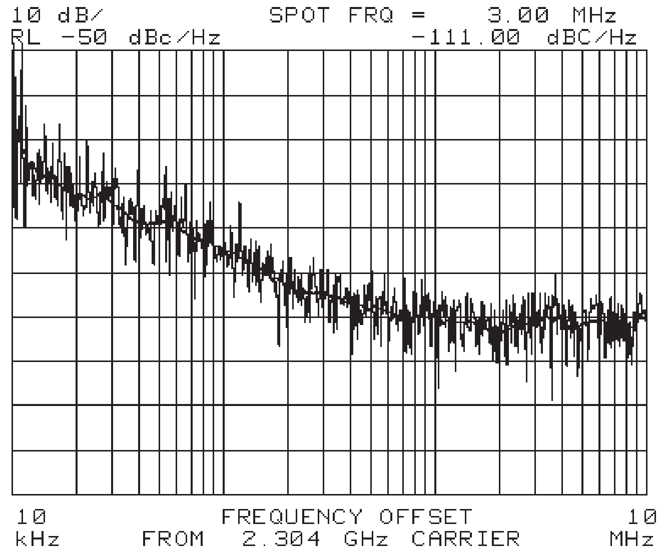


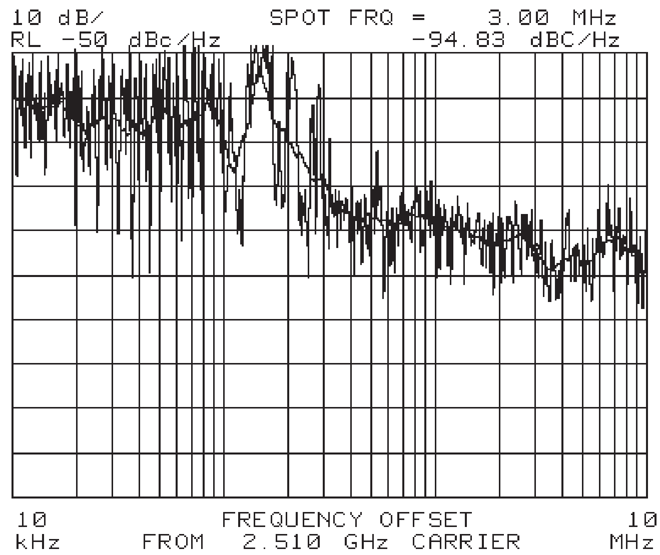
Figure 4.14: First harmonic VCO output spectrum with varactor tuning voltage of (a) 2.5 V and (b) 0.5 V tuning voltage. There is obviously a large amount of spurious sideband noise at the lower tuning voltages.

where ΔV_{ctrl} is the change in control voltage corresponding to a change in output frequency Δf_o. Measurements show that the linear slope of the tuning curve occurs between 2V to 3V, corresponding to an approximately 400 MHz frequency range. Therefore, K_v is 400 MHz/V. However, there still is the unwanted shift in the variable frequency band that does not meet the GSM specifications.

Finally, as expected, it is observed from the measurements that the varactors impact the quality factor of the tank. As can be seen, the spurious components are lower with a tuning voltage of 0.5 V [Figure 4.14(b)] versus 2.5 V [Figure 4.14(a)]. This is attributed to the fact that the varactor Q value is a function of control voltage. This quality factor variation can also be observed in the VCO phase noise. With a 0.5 V tuning voltage, the phase noise at a 3 MHz offset frequency is -111 dBc/Hz [Figure 4.15(a)]. However, the quality factor decreases as the control voltage increases. With a VCO control voltage of 2.5 V, the phase noise at a 3 MHz offset increases to -94.8 dBc/Hz almost a 16 dBc/Hz increase over the 0.5 V case [Figure 4.15(b)]. However, it should be noted that the HP 8563E Spectrum Analyzer is notoriously unreliable for performing accurate phase-noise measurements.



(a)



(b)

Figure 4.15: Phase noise plots at a 3 MHz offset frequency with a tuning voltage of (a) 0.5 V compared to (b) 2.5 V. Phase noise measurements were taken with the HP 8563E and are not considered to be reliably accurate. However, this equipment can sufficiently show the general trends in phase-noise changes.

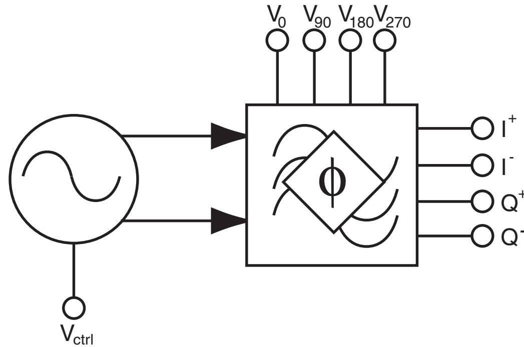


Figure 4.16: Block diagram of a differential VCO with tunable polyphase output filter (after [20]).

4.4 Time-Domain Measurement Technique for VCO with Tunable Polyphase Outputs

The second thrust of this thesis is to develop an alternative measurement technique for the VCO with tunable polyphase outputs (Figure 4.16) developed in [20]. As discussed in Chapter 1, this tunable polyphase VCO has been proposed as an analog solution for correcting I/Q imbalance in direct conversion/low-IF receivers. Prior measurement efforts involved using frequency-domain, S-parameter-based techniques. Although, this frequency-domain approach was sufficient for proof-of-concept purposes, noise and reflection issues were of concern. This has led to the development of an alternative time-domain methodology.

4.4.1 Tunable Polyphase Filter

Consider a single-pole *RC*-*CR* filter designed at a frequency of $\omega_o = 1/RC$ [Figure 4.17(a)]. A phase shift of $-45°$ results through the path of the series resistor ($V_{1,out}$) and a $+45°$ phase results through the path of the series capacitor ($V_{2,out}$). The total relative phase between the two outputs is therefore 90°. In fact, this relative phase is ideally 90° at all frequencies (although the relative amplitudes are not constant). A differential single-pole polyphase network can be realized as shown in Figure 4.17(b). In this case, the circuit is driven with a differential input at nodes $V_{1,in}$ and $V_{3,in}$, and

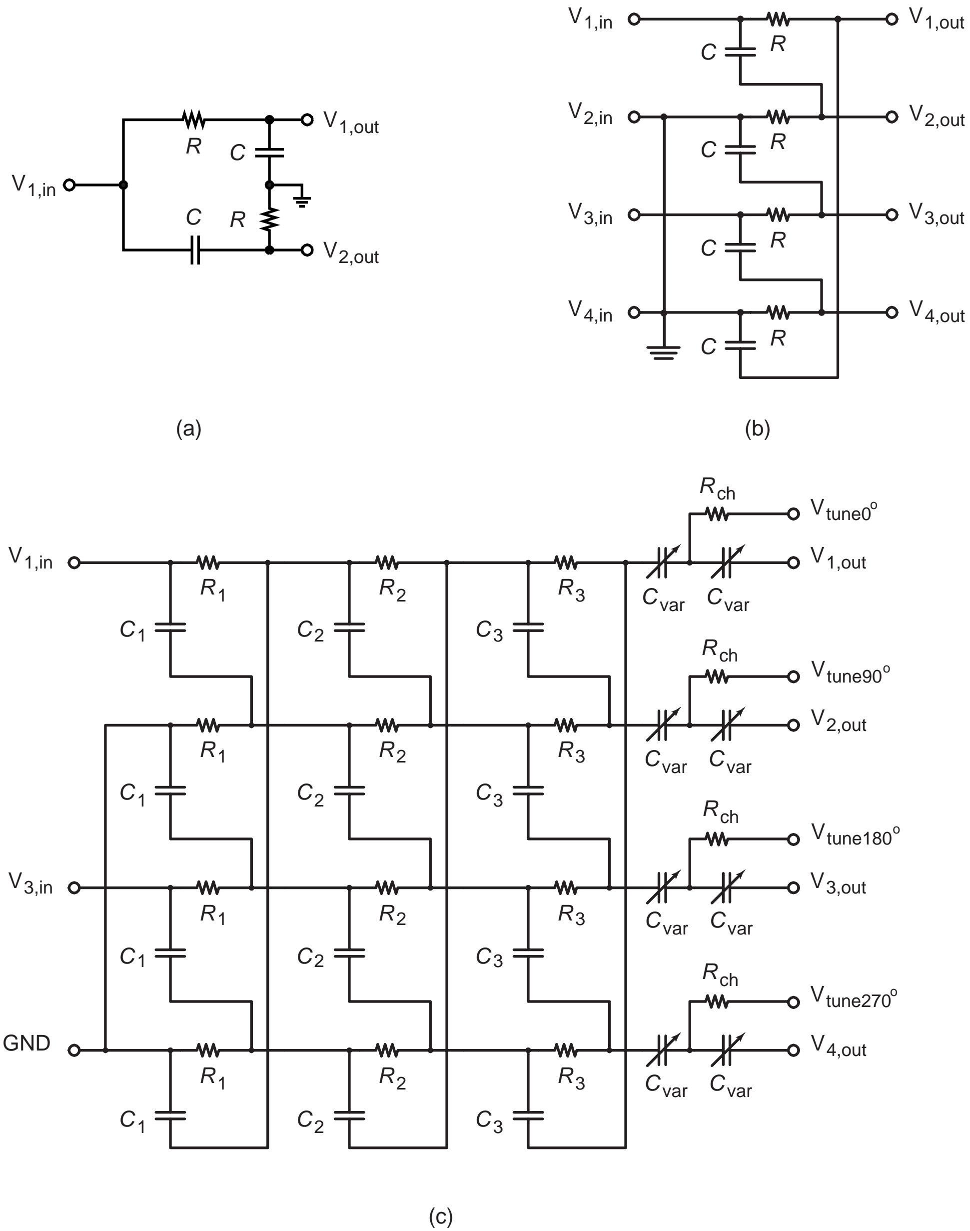


Figure 4.17: (a) A single-ended RC-CR phase-shift network shifts the output ±45° from the input (at $\omega_o = 1/RC$), while maintainting a 90° phase between $V_{1,out}$ and $V_{2,out}$. (b) A single-pole differential input polyphase network provides output phases of 315°, 45°, 135°, and 225° at $\omega_o = 1/RC$. (c) A three-pole polyphase filter with series output varactors producing tunable differential quadrature generation (after [20]).

nodes $V_{2,in}$ and $V_{4,in}$ are grounded. The phases of the four outputs at $\omega_o = 1/RC$ are:

$$\angle V_{1,out} = 0^\circ - 45^\circ = 315^\circ \tag{4.2}$$

$$\angle V_{2,out} = 0^\circ + 45^\circ = 45^\circ \tag{4.3}$$

$$\angle V_{3,out} = 180^\circ - 45^\circ = 135^\circ \tag{4.4}$$

$$\angle V_{4,out} = 180^\circ + 45^\circ = 225^\circ. \tag{4.5}$$

Phase flatness versus frequency may be improved using multiple polyphase stages. Typically, two poles are placed at the edges of the desired frequency passband, while the remaining poles are equally spaced along the logarithmic frequency axis [71]. Essentially, this pole placement gives the filter an equiripple response. However, a major drawback to multistage polyphase networks is an increase in signal loss, which in turn leads to an increase in overall power consumption due to required amplification.

The design of such a polyphase network also requires impedance buffering at the input and output of the network. Input buffers prevent preceding circuits (e.g., VCOs) from being loaded down by the polyphase filter. In addition, an output buffer is required to present a high impedance to subsequent loading circuits. However, the addition of buffers can introduce amplitude and phase distortion.

In [20], the basic polyphase design is augmented with phase tuning using series output varactors at each of the four outputs (actually two varactors in series with bias connection between) as illustrated in Figure 4.17(c). Each varactor control line (V_{tune0°, $V_{tune180^\circ}$, V_{tune90°, and $V_{tune270^\circ}$) is implemented with a series resistor ($R_{ch} = 100k\Omega$) to minimize RF leakage into the DC path. There are three ways that the phase tuning of the polyphase filter outputs can be controlled. First, applying the same voltage to all four control lines will adjust the center of the frequency band over which the output phases differ by 90° (differential quadrature outputs). Second, by fixing V_{tune0} and $V_{vtune180}$ to one voltage, while varying V_{tune90} and $V_{tune270}$ together (or vice versa), will adjust I/Q phase balance. Finally, tuning all the control lines individually results in independent relative phase tuning of all four of the output channels (I^-, I^+, Q^-, and Q^+).

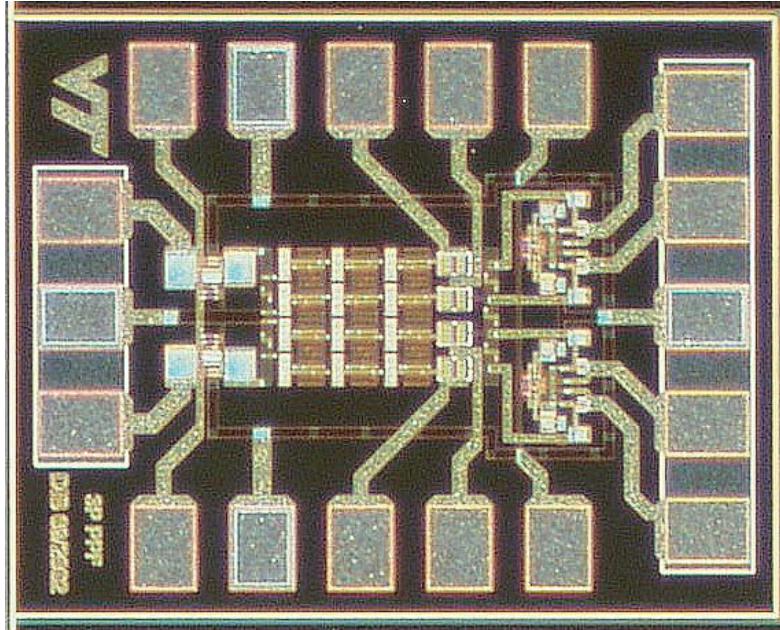


Figure 4.18: Die photograph of the fabricated stand-alone tunable polyphase network [20].

4.4.2 Stand-alone Tunable Polyphase: Frequency-Domain Measurement

Initial measurements were conducted on a prototype stand-alone polyphase design (no VCO) (Figure 4.18). In [20], S-parameter-based frequency-domain measurement approach was taken. In this case, a sequence of single-ended S-parameter measurements were taken using the HP 8510C VNA system. Post-measurement processing was required to synthesize the desired response to differential inputs from this data.

Figure 4.19 shows a single-ended input driving the In^- (negative input), and a single-ended output measurement (S_{21}) taken at Q^+ (positive output) port. Both the single-ended input In^+ and remaining output ports (I^-, I^+, and Q^-) are terminated with 50Ω loads. Similarly, a second measurement is made by terminating In^+ and measuring S_{21} to the Q^+ output port again. An average of four measurements were taken for each of these cases. Then, using superposition, a mathematically synthesized differential signal is created from the two average measurements for Q^+, which is the difference of the two individual single-ended transfer responses ($\{In^+ \longrightarrow$

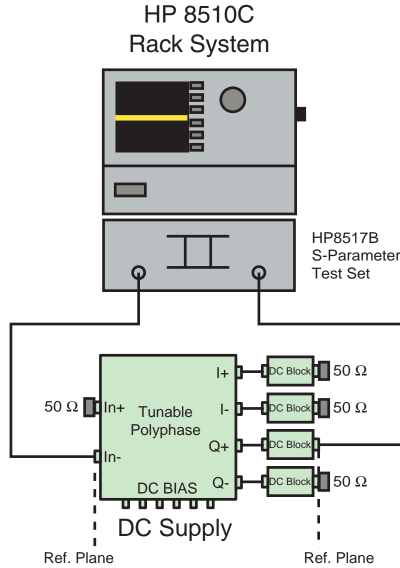


Figure 4.19: Measurement system used to take "single-ended" S-parameter measurements. These measurements are converted to differential outputs using the single-ended data by means of post-processing synthesis.

$Q^{+}\} - \{In^{-} \longrightarrow Q^{+}\})$. This process is repeated for the I^{+}, I^{-}, and Q^{-} outputs. After synthesizing the differential signals, phase differences are calculated for $(I^{-} - Q^{+})$, $(I^{+} - Q^{-})$, $(Q^{+} - I^{+})$, and $(I^{-} - Q^{-})$. For any difference that is of a negative value, 360° was added. All measurements were validated with the 360° check across the whole frequency range (equation 4.6). The measurements can be validated by the following equation:

$$(I^{-} - Q^{+}) + (I^{+} - Q^{-}) + (Q^{+} - I^{+}) + (Q^{-} - I^{-}) = 360^{\circ}, \quad (4.6)$$

For example, the sum of each phase shift should add up to equal one cycle (Figure 4.20).

Unfortunately, the resulting measurements showed significant deviation from the 90° (quadrature) regime (Figure 4.21). Several samples of the tunable polyphase design were available; however, there were also deviations in the response from sample to sample [20]. Nonetheless, an important similarity between the responses of all samples was the "kinks". These kinks may be a result of the imbalance of the 180° (differential) signal outputs.

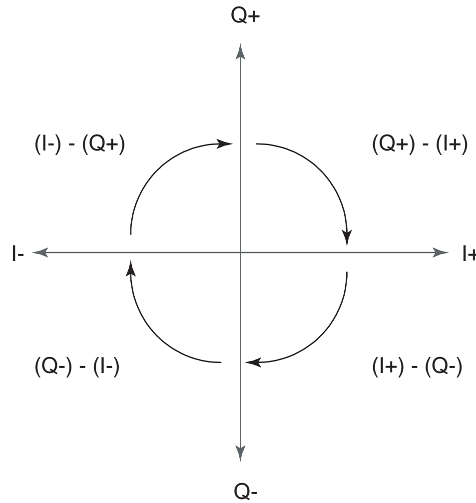


Figure 4.20: Validation of measurements can be made by summing the relative phases to equal one complete cycle 360°.

The data collected from each channel was then post-processed to determine if there was a constant 180° difference between the outputs. It was discovered that there was a significant *differential* imbalance for both the I and Q channels (Figure 4.22). The differential Q channel was closer to the required 180° over ~5.8-6.0 GHz. On the other hand, the differential I channel was closer to 180° over the 5-5.4 GHz range. This opposite response in the two differential channels is a key contributor to the kinked response.

4.4.3 Integrated VCO with Tunable Polyphase: Time-Domain Measurements

As mentioned above, the tunable polyphase and corresponding VCO were initially tested as separate stand-alone components [20]. However, a measurement technique was subsequently needed for the fully integrated VCO with tunable polyphase. Because of the device-under-test (DUT) has only an output port, the measurement of the I/Q phase error cannot be found using S-parameters. This motivated the development of an oscilloscope-based time-domain approach. However, available oscilloscopes covering lower frequencies (<500 MHz) than the VCO output frequency output range. High-speed oscilloscopes that can detect signals in the 5-6 GHz range

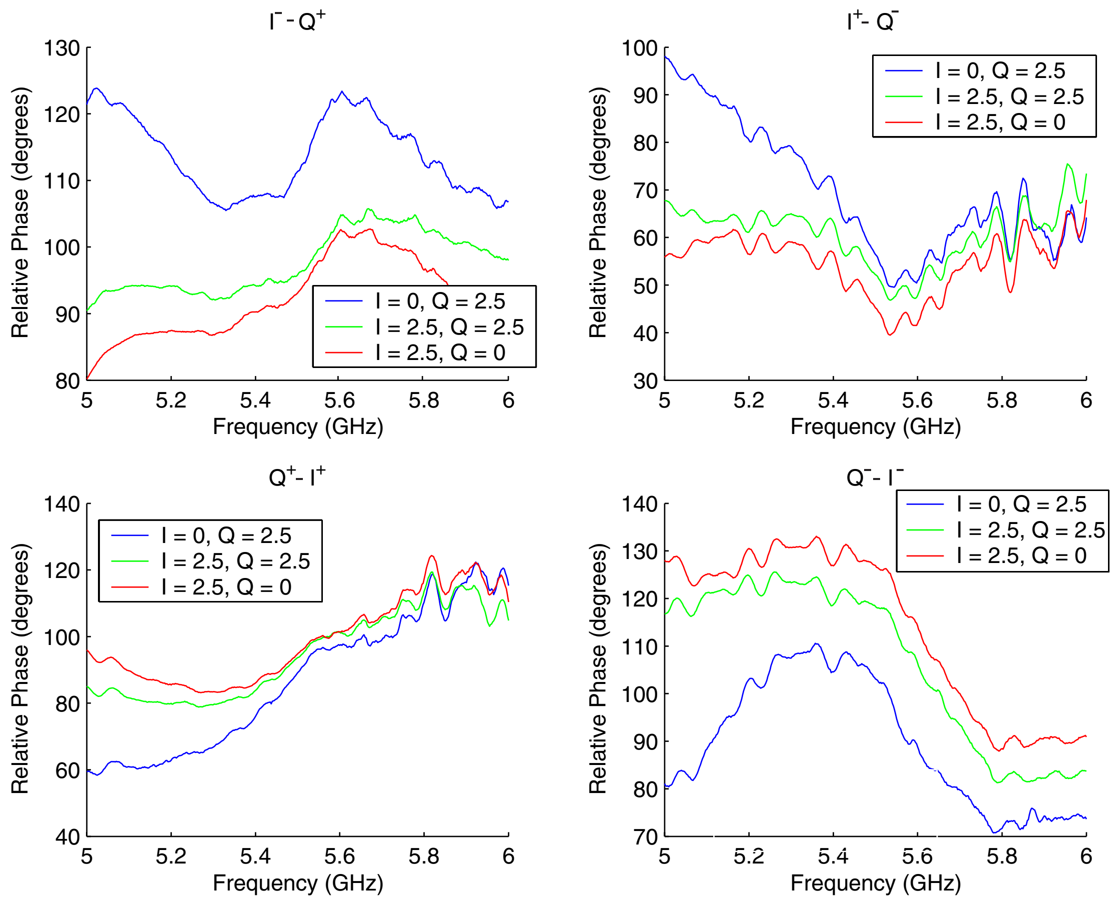


Figure 4.21: Measured I/Q imbalance of the four output signals vs. frequency and various varactor tuning voltages.

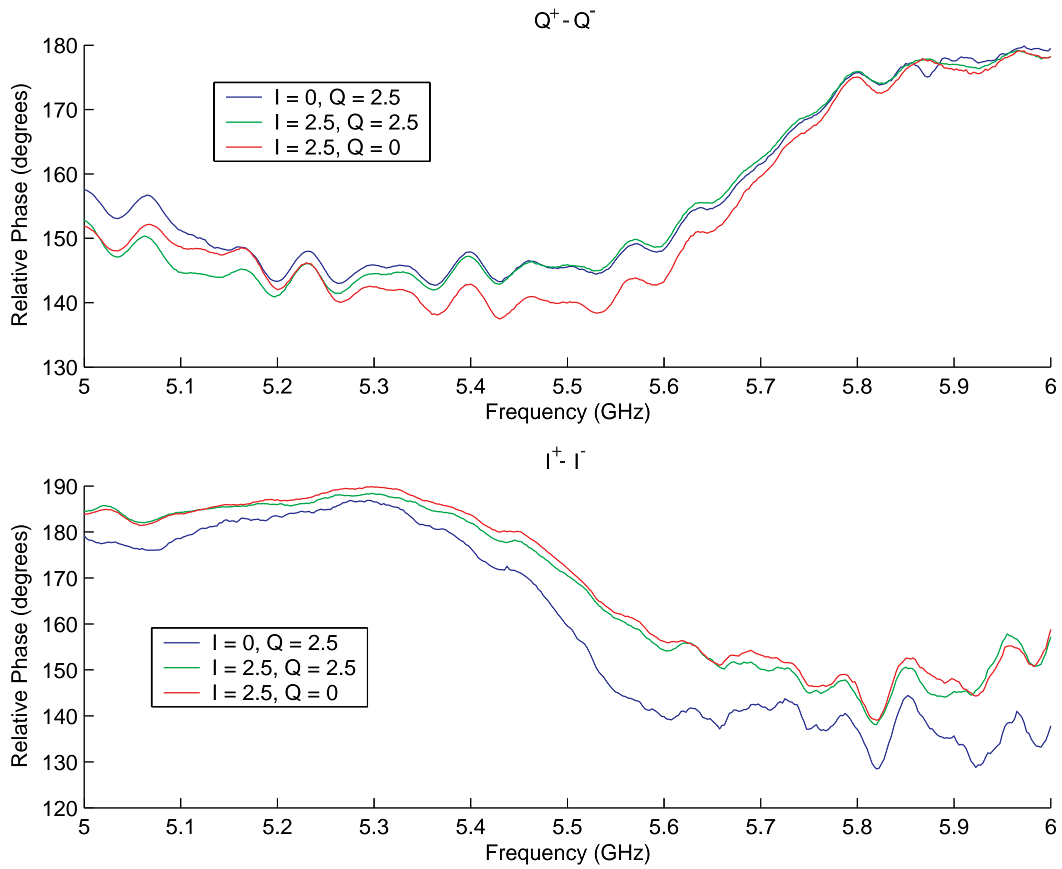


Figure 4.22: Measured differential phase imbalance for the (a) $(I^+ - I^-)$ and (b) $(Q^+ - Q^-)$ differential output channels of the tunable polyphase. Q means voltage control for both $Q^+$and Q^-, and I is control voltage for both I^+ and I^-.

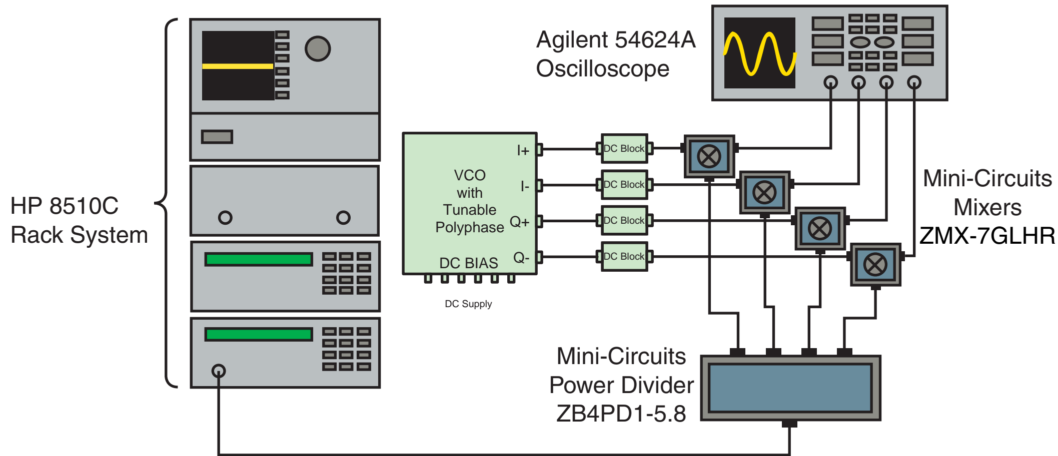


Figure 4.23: Initially proposed I/Q phase error measurement system for the VCO with tunable polyphase outputs.

are expensive and typically function using sub-sampling, which adds additional issues of synchronization to such measurements. Therefore, an alternative approach is to downconvert the high-frequency output of the tunable polyphase VCO to an appropriate lower frequency range in which the oscilloscope measurement could be made with currently available instruments.

Figure 4.23 shows the initially proposed setup for the VCO with tunable polyphase output. However, a major issue with this approach is the need to properly trigger the oscilloscope. There are two options with the available model oscilloscope: either triggering an external source, or using one of the four channel inputs to the oscilloscope. This means that an exact replica of the VCO output frequency and phase signal would be required. Unfortunately, the integrated VCOs output carrier frequency drifted at a low frequency, making locking onto measurements impossible.

However, it was still useful to evaluate the time-domain oscilloscope-based I/Q phase error measurement technique using the stand-alone tunable polyphase design described above. The triggering issue for the integrated VCO and polyphase design will be studied in future work. In addition, the phase noise of the integrated VCO and polyphase design was measured to evaluate the effects of the tunable polyphase circuit on the VCO performance. These results are discussed in the following sections.

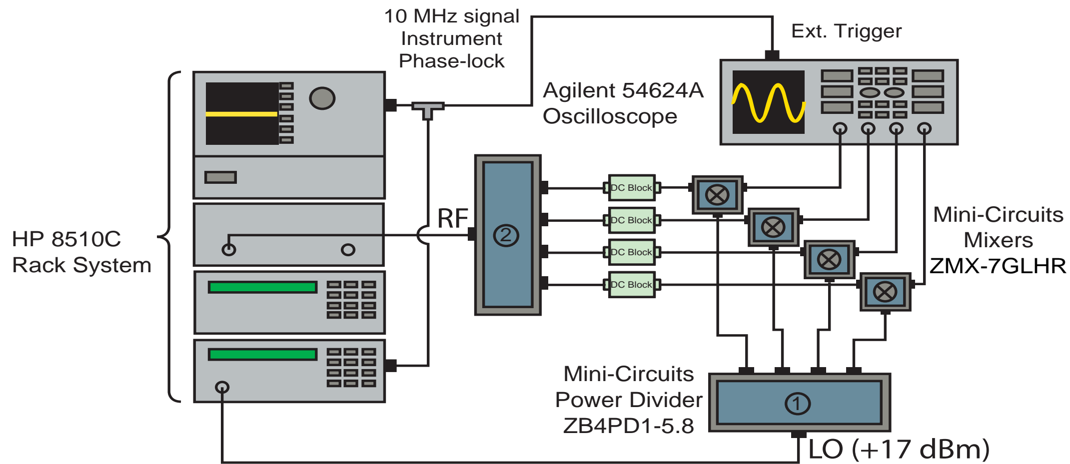


Figure 4.24: Measurement system for determining phase errors due to the mixers and power dividers.

4.4.4 Calibration

As described above, the proposed time-domain measurement requires additional components for translation of RF signals to a lower frequency range measurable by the available oscilloscope. These components themselves introduce some gain and phase errors. Therefore, these errors must be measured and calibrated out of the final measurements. The test setup for this calibration is shown in Figure 4.24.

First, the Mini-Circuits ZB4PD1-5.8 power dividers used to split the RF and LO signals to the mixers are characterized. This was accomplished using standard S-parameter measurements using the HP 8510C VNA. The phase and amplitude error measurements were stored for subsequent deembedding from the mixer calibration measurements. Figure 4.25(a) shows the data collected from this calibration procedure. The mixer calibrations were completed within the frequency range of the DUT VCO output frequency (5-6 GHz). Figure 4.25(b) shows the measured phase error of the four mixer channels with the RF power divider calibrated out.

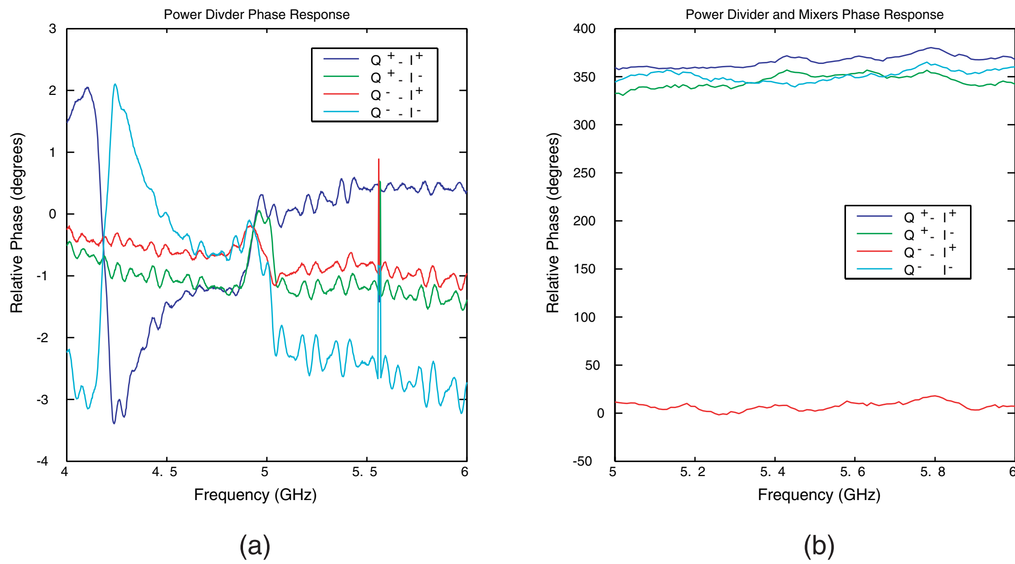


Figure 4.25: Phase response of the (a) individual power dividers and (b) the relative phase difference between the channels of the mixers with the power dividers calibrated out. Each power divider is assigned to the individual I^-, I^+, Q^-, and Q^+ channels.

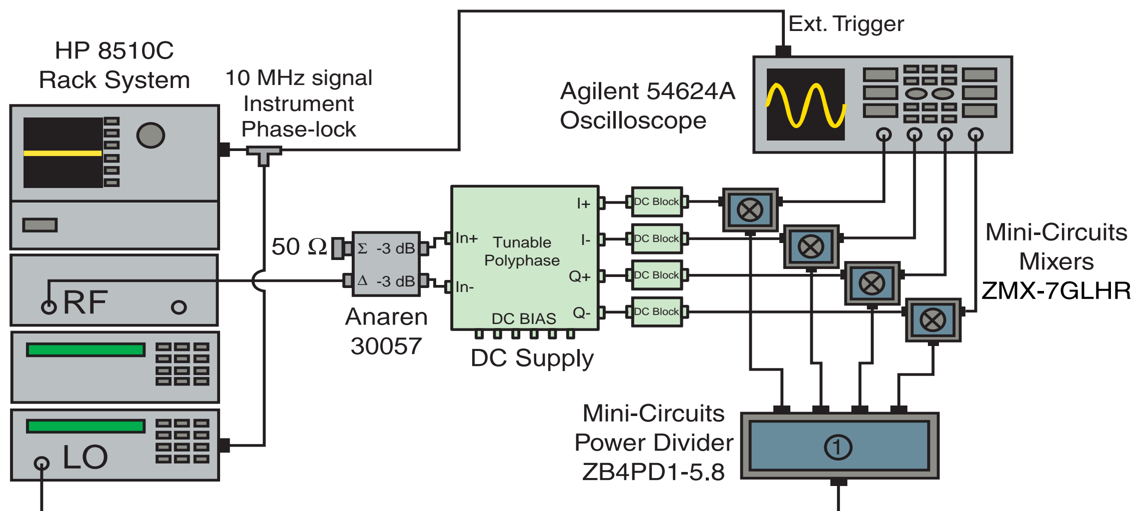


Figure 4.26: Revised time-domain measurement system for VCO with tunable polyphase outputs.

4.4.5 Stand-Alone Tunable Polyphase: Time-Domain Measurements

Figure 4.26 illustrates the I/Q phase error measurement system for the stand-alone tunable polyphase. A differential input RF frequency is supplied to the polyphase through the 180° hybrid balun with an amplitude setting to avoid input buffer compression within the DUT. An LO signal is supplied to achieve a 10 MHz output IF signal at each input frequency point, which is then fed to the oscilloscope. Meanwhile, an external 10 MHz phase-locked signal is provided by the HP 8510C between the RF and LO sources using BNC cables. In addition, the 10 MHz phase-locked signal is provided to the external trigger connection of the oscilloscope.

The time-domain phase measurements of the tunable polyphase were accomplished with automated scripts using Agilent VEE software [72]. Each measurement was completed using two combinations of tuning voltages. The first combination used a 2.5 V fixed voltage for the I-channel varactors ($V_{tune0^{\circ}}$ and $V_{tune180^{\circ}}$ pins), while sweeping the Q-channel ($V_{tune90^{\circ}}$ and $V_{tune270^{\circ}}$ pins) from 0 to 2.5V. The second combination used a fixed voltage for the Q-channel, while sweeping the I-channel. The most stable results were achieved when fixing the voltage at both the I^{+} and I^{-} at 2.5 V and the Q^{+} and Q^{-} at 0 V (Figure 4.27). Note that the validation axis is shown in Figure 4.28 to illustrate that total phases should equal 360° across all frequencies between 5-6 GHz. For the I=2.5 V and Q= 0 V configuration, the measured data does show up to ∼10° phase range difference at 5.2 GHz. However, a ripple of ±4° is observed between 5.4 to 6 GHz over the 360° validation axis. In comparison, the voltage tuning characteristics for I=2.5 V and Q = 2.5 V shows a steady increasing trend between 5 to 5.4 GHz and ripples at an average of +5° from the validation axis. Finally, the I=0 V and Q= 2.5 V combination shows a steady decreasing trend of -35° from the validation between 5 to 6 GHz. The observed monotonic ripple trends across the frequency ranges could be the results of the analog-to-digital (ADC) resolution of the oscilloscope. In addition, the error may be a result in accuracy of the phase discriminator within the oscilloscope measurement system.

A major issue that was found during measurements shows that there is an unequal

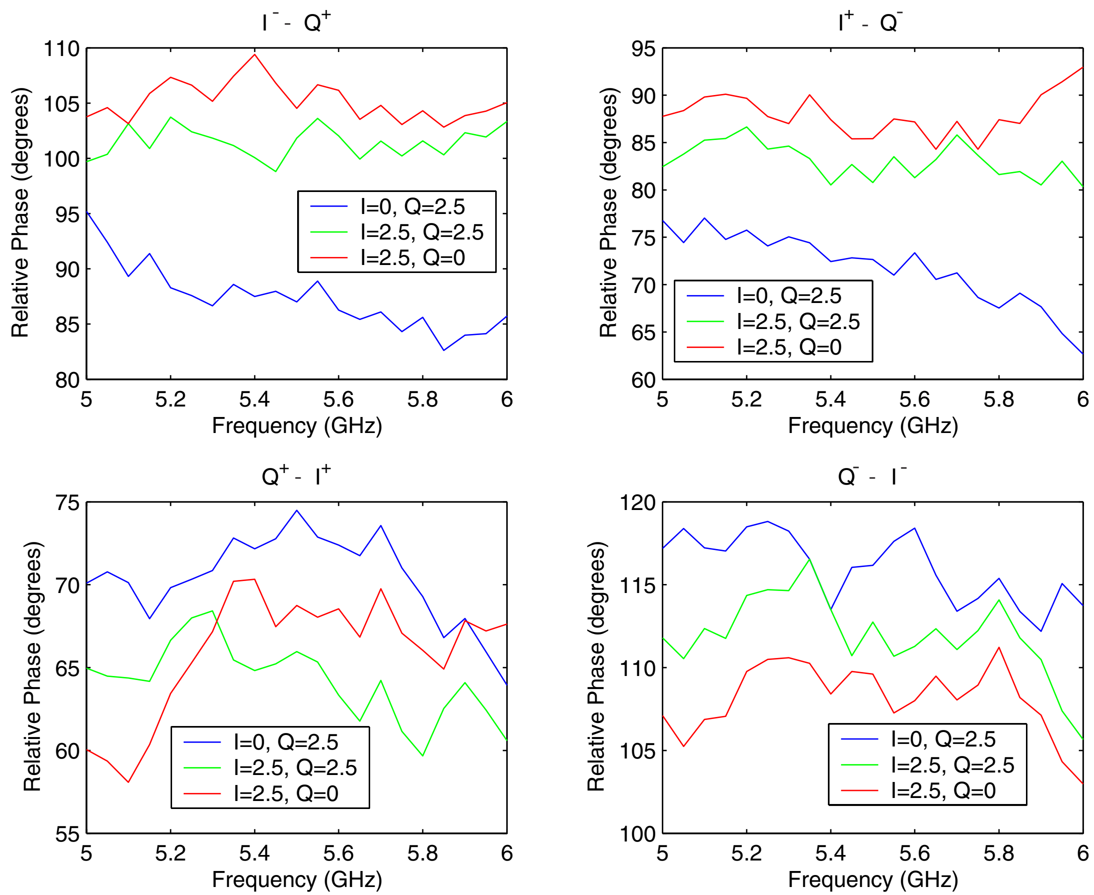


Figure 4.27: Measurements of phase change vs, frequency with applied individual tuning voltages.

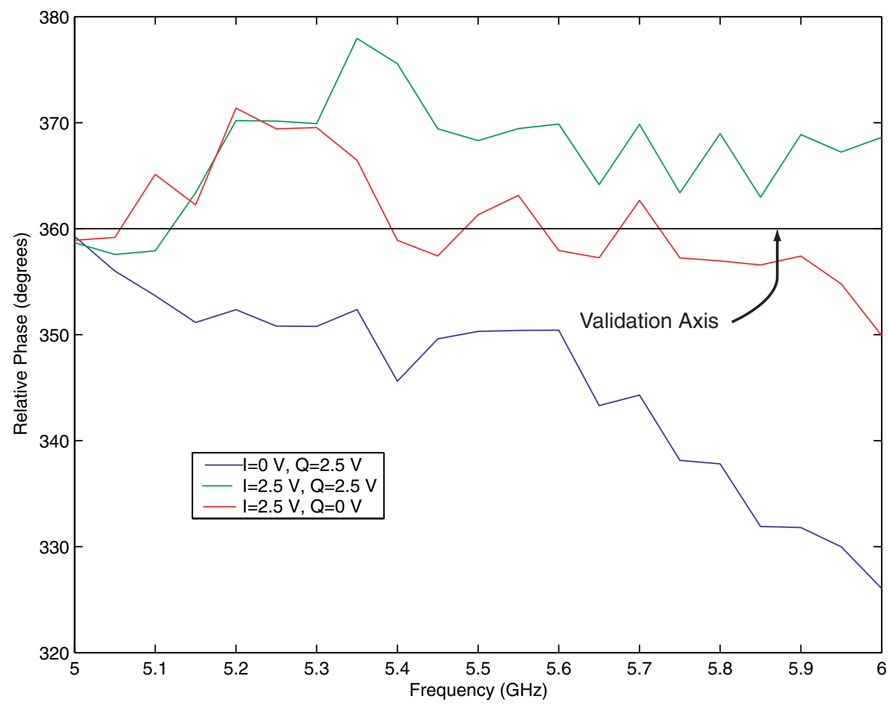


Figure 4.28: Validation of measurement results show that the phase difference between the outputs of the polyphase are close to the 360° validation axis.

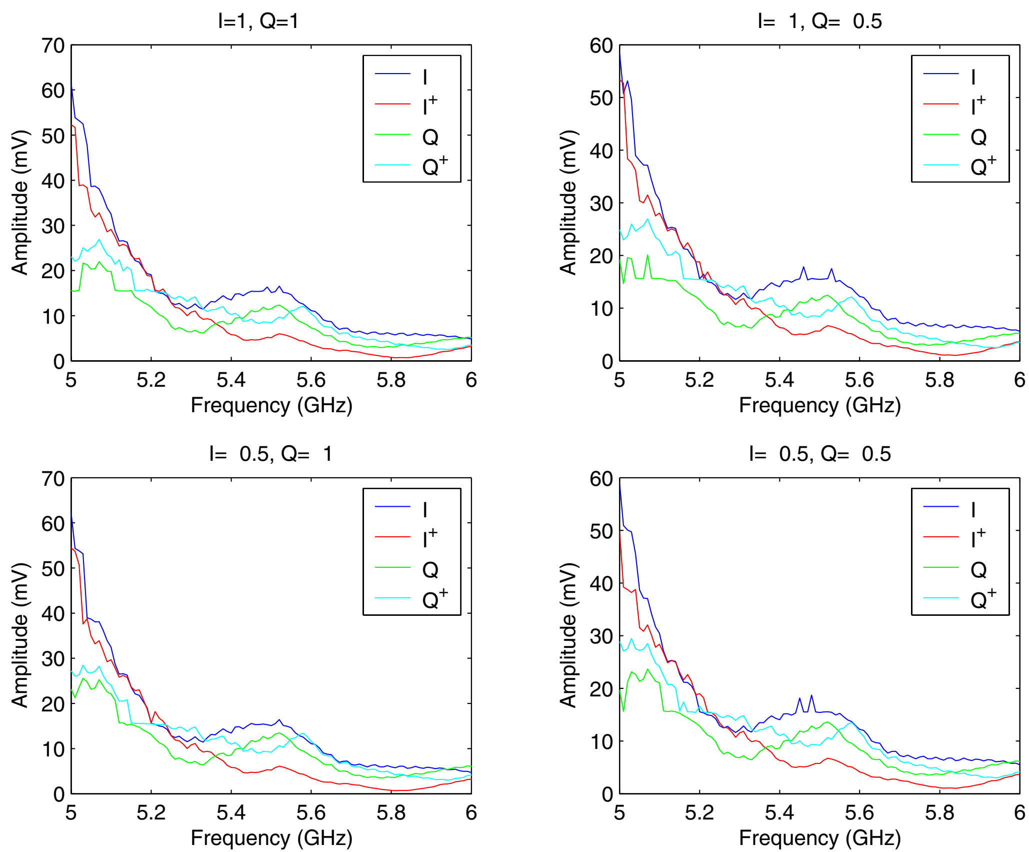


Figure 4.29: Measurement of peak voltage amplitude at the output of the tunable polyphase.

amplitude output for the I^-, I^+, Q^-, and Q^+ channels versus tuning frequency. The amplitude outputs of the four channels drop significantly as frequency increases (Figure 4.29). This trend could be related to the RC pole placement, such that the bandpass response is not at the designed frequency due to parasitics. In addition, there may be significant signal reflections at these frequencies from impedance mismatches between the tunable polyphase and the mixers. Since the mixers are matched to 50 Ω, improper matching of the tunable polyphase outputs could lead to signal degradation.

Another drawback with the time-domain approach used here lies in the oscilloscope's ability to measure relative phases. The oscilloscope detects the relative phase between signals in the I^-, I^+, Q^-, and Q^+ channels based on the zero-crossings. The accuracy of the zero-crossing measurements depends heavily on having sufficient signal amplitude. Because the amplitudes at the output of the polyphase were in the hundreds of micro-volts, the oscilloscope had difficulty properly detecting and measuring the phases. This further impaired the reliability of the time-domain measurements. Future work should include revisions to the buffer designs to alleviate this issue.

4.4.6 VCO with Tunable Polyphase Phase Noise Measurements

It was possible to perform phase noise characterization on the integrated VCO with tunable polyphase outputs as shown in Figure 4.30. The VCO core consumed approximately 3.87 mA of current (12.7 mW). The phase noise was observed at an offset frequency of 1 MHz. The phase noise measurements were accomplished using the Agilent E5500 instrument system. The E5500 has a sophisticated system for self-calibration to achieve the best possible phase-noise measurement. Any internal noise from the measurement equipment is excluded from collected data. A drawback to this system is that it requires an input power of +15 dBm to properly measure phase noise. This required an RF amplifier to boost the signal from the VCO by 35 dB for measurements. Recall that the Q channels exhibited higher output amplitude than the I channels; therefore, phase noise measurements using the E5500 could only be accomplished using the Q+ channel. With the varactor biased on the Q-channel (V_{tune90° and $V_{tune270^\circ}$ pins) at 1 V, the E5500 measured approximately -96 dBc/Hz

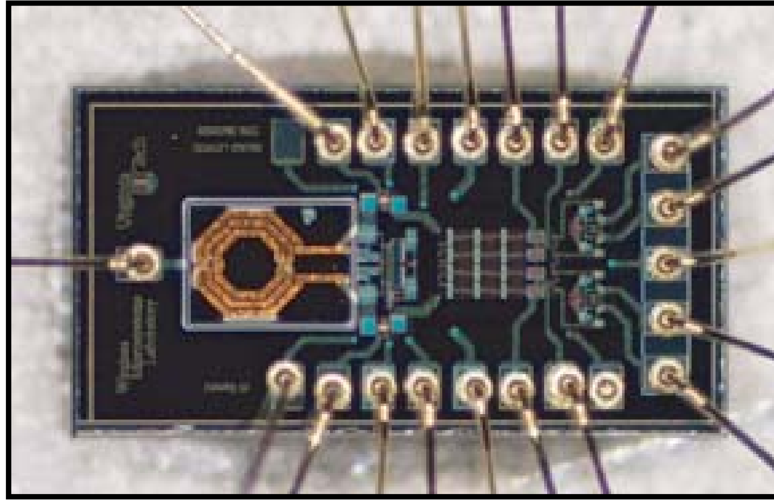


Figure 4.30: Wirebond photo of the symmetric inductor VCO with tunable polyphase.

at a 1 MHz offset from $f_o = 5.4$ GHz (Figure 4.31). In addition, the voltage tuning of the VCO did not significantly affect phase-noise at the 1 MHz offset. However, measured results reported in [20] show that the stand-alone VCO with a symmetric differential inductor demonstrated approximately -114 dBc/Hz at the 1 MHz offset from a $f_o = 5.4$ GHz. The degradation in the phase-noise of the VCO with tunable polyphase is approximately 18 dB from that of the stand-alone VCO. This degradation could be a result of the integrated buffers between the VCO and the tunable polyphase filter design.

4.5 Summary

This chapter has presented measured data for the various circuits fabricated in conjunction with this work. This included on-wafer measurements of the tank circuit inductor used in the fabricated VCO designs. These measurements revealed that the inductor had a relatively poor Q value and an effective inductance (L_{eff}) that deviated from the simulated results. In addition, multiple harmonics were generated at the output due to non-linearities in the buffer design. This resulted in a VCO that did not meet frequency and phase-noise specifications for GSM applications.

This chapter also discussed the development of I/Q phase error measurement tech-

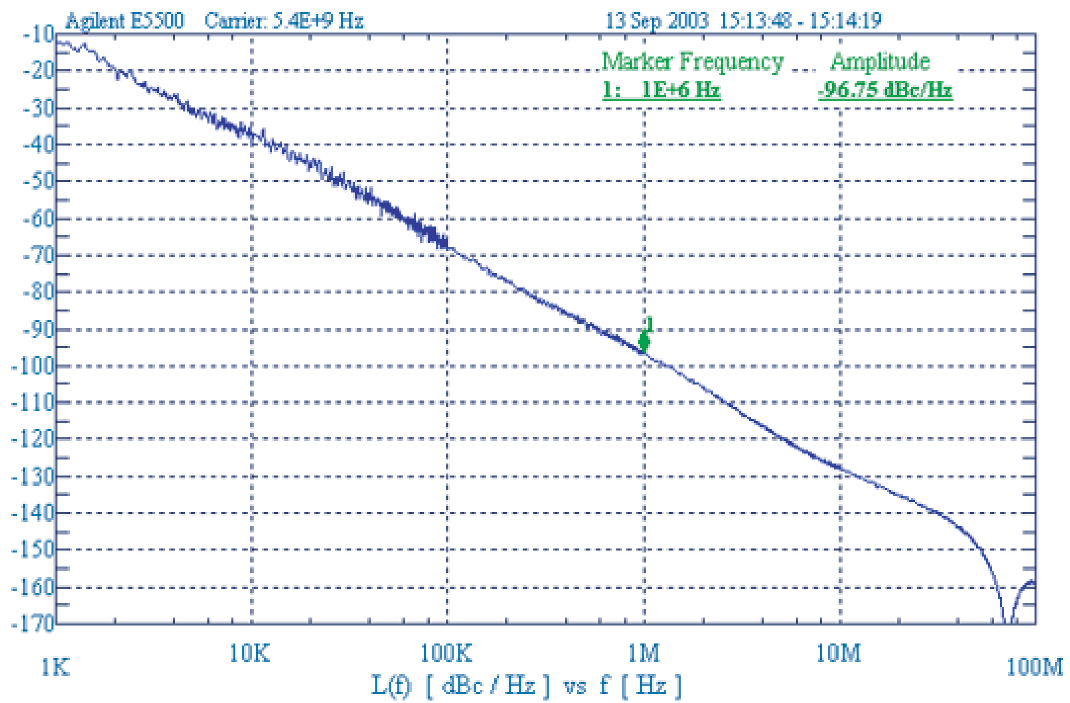


Figure 4.31: Phase noise measurement VCO with tunable polyphase Q^+ output using the Agilent E5500 instrument. V_{tune90° and $V_{tune270^\circ}$ are both set to 1 V.

niques for tunable polyphase circuits. The time-domain approach reveals that introducing power dividers and mixers into the test setup will cause some variability in relative phases. However, when calibration techniques were taken into consideration, the results show that the summation of relative phases do not equal 360° over the frequency range of interest. The primary problem with the proposed time-domain approach is that the low-IF signal levels at the oscilloscope are too small in amplitude for accurate phase detection. In addition, there are limitations in the oscilloscope capabilities in measuring the relative phase differences with minute amplitudes from the four I^-, I^+, Q^-, and Q^+ channels. On the other hand, the frequency-domain approach achieves the 360° validation, indicating that accurate phase detection is achieved at the available signal levels. The frequency-domain measurements reveal that there are issues with differential phase imbalance in the I/Q outputs of the polyphase. This results in a degradation in the measured I/Q phase flatness versus frequency. Proposed solutions to these problems are presented in the next chapter.

Chapter 5

Conclusion and Future Work

This thesis covers two important components of communications receiver and transmitter systems. First, an extensive study has been made on LC-VCO implementations using both SiGe HBT and CMOS technologies. This included observations of trade-offs between the power consumption and phase noise. This incorporated design, simulation, and characterization of dual spiral inductor structures. In conjunction, a study of time-domain measurement alternatives for tunable polyphase filters was also explored. Consequently, this task revealed the limitations in downconversion mixers and relative phase-measurement capabilities of low-frequency oscilloscopes. This section provides a broad range of alternatives for future work for both the VCO designs and tunable polyphase measurements.

5.1 Conclusions: 2x/4x Frequency VCO

The following paragraphs describe the various conclusions that arose from the study of the 2x/4x frequency VCO and the inductor structure.

- Standalone dual octagonal spiral differential inductors were fabricated and tested using on-wafer characterization. However, the lack of appropriate pad deembedding structures led to questionable inductance and Q measurements. Also, due to the small size of the inductors used, it is quite possible that the parasitic capacitance of the pads swamp out the true inductance. Improvement in

the quality of these measurements may be accomplished by including on-wafer calibration standards for correct pad structures in future design iterations.

- The tuning frequency range of the HBT VCO was shifted down to an undesired band. The circuit was characterized for an oscillator that is tuned to a specified frequency range using a 512 pH inductor. The inductor structure was characterized using EM simulations, which do not provide an exact solution for effective inductance. The small variation in inductance moved the tuning range to approximately a 1 GHz lower frequency range.

- Varactor tuning also has an effect on the quality factor of the oscillator LC-tank circuit. A lower tuning voltage (approximately 0.5 V) decreased single sideband phase noise compared to higher voltages (2.5 V); in other words, varactor Q decreases at higher tuning voltages. Note that VCO simulations do not show this behavior; improvements in the modeling of the Q of the accumulation mode varactors is required.

- The two fabricated complementary MOS VCO designs (Tx and Rx) did not operate correctly upon fabrication: in both cases the RF output ports (RF- and RF+) appeared to be shorted to ground. It is possible that ESD protection diodes included in the designs are responsible for the short-circuit issue. However, further investigation is required. On the other hand, the HBT VCO designs did not include ESD protection circuits and were successfully measured at RF.

- The VCO output buffer circuits suffered from significant non-linearities. These non-linearities resulted in unwanted harmonics of the VCO output frequency. Future designs should focus on reducing the demands on the buffer circuits.

- Measuring phase noise with particular instruments is critical when trying to achieve accuracy. The Agilent E5500 phase-noise measurement system recorded a 3 dB better measurement than the HP 8563E spectrum analyzer. However, to make proper measurements requires an input power of approximately +15 dBm into the E5500. While a 35 dB gain amplifier may be used to drive the instrument system, future circuits that are intended for accurate phase noise measurements must have sufficient output power following the buffers.

5.2 Conclusions: VCO with Tunable Polyphase

An alternative time-domain methodology was developed to measure the phase error of a tunable polyphase filter. Conclusions drawn from these results are as follows:

- The S-parameter-based frequency-domain measurement approach is a valid technique that can be used to test the I/Q phase error in tunable polyphase circuits. Due to the lack of precise 180° baluns, a mathematically synthesized differential measurement could be made from single-ended data points. An advantage to using the VNA-based system is that the instrument is sensitive enough to detect phase errors with relatively low output signal levels.

- The frequency-domain measurements also show that the I and Q channels of the fabricated design have poor differential balance over portions of the 5-6 GHz frequency range. With control voltages for the I channel set at 2.5 V and those for the Q channel set at 0 V maximum results in ∼10° phase tuning difference. However, there is a ripple of ±4° around the 360° validation axis between 5.4 to 6 GHz. The largest phase change was found for the I channel set at 0 V and the Q channel set at 2.5 V, a steady decreasing trend of -35° from the validation axis between 5 to 6 GHz. The cause of these differential imbalances requires future investigation.

- The time-domain technique demonstrated in this work requires additional components, which themselves introduce phase and amplitude errors. While the RF outputs of the tunable polyphase are within the 5-6 GHz frequency range, the available oscilloscope was limited to a 100 MHz measurable bandwidth. Therefore, mixers were used to translate the 5-6 GHz outputs to a low IF (10 MHz) detectable by the oscilloscope. Additional calibration steps were required to factor out the phase effects of both the mixers and power dividers. Therefore, the time-domain approach used here is a more complex measurement scheme compared to the frequency-domain approach.

- During the time-domain measurements, the output amplitudes of the I^-, I^+, Q^-, and Q^+ channels from the tunable polyphase deviate dramatically from each other. This is due to process variations that may have affected the differential I/Q channel paths. In fact, the amplitude decreases to 500 μV_{p-p},

which results in unreliable oscilloscope measurements. Therefore, this measurement system requires adequate (IF) output amplitudes to be practical, since the oscilloscope used has difficulty detecting signal phase measurements if the amplitudes are below a minimum threshold.

- Another drawback to the time-domain measurement approach is that the system requires an external trigger signal to make accurate relative phase measurements. The trigger signal must be related directly to the RF input. Therefore, the signal used for phase-locking the RF and LO sources was used as the oscilloscope trigger.

5.3 Improvements and Future Work

This section describes several proposed improvements to the VCO designs and I/Q phase error measurement techniques presented in this thesis.

5.3.1 2x/4x Frequency VCO

- On-wafer inductor measurements could be improved by including a complete set of on-chip open and short standards for calibrating out the pads. In this work, Sonnet EM simulation data was used as a backup option; consequently, the deembedding of pad parasitics from the inductor test structure measurements was still not completely accurate.

- The inductor should be redesigned in a symmetric differential configuration. In addition, a revised inductor design could also utilize a *patterned ground shield* (PGS) to minimize electric and magnetic coupling to the lossy substrate and reduce the magnetic image current loss [51]. Such designs can be implemented with a ground shield that has slots orientated perpendicular to the current from within the inductor windings (Figure 5.1).

- The complementary MOS design in this thesis incorporated ESD protection diodes for reliability purposes. These diodes may have contributed to the operational failure of this VCO design. In the future, research prototypes should

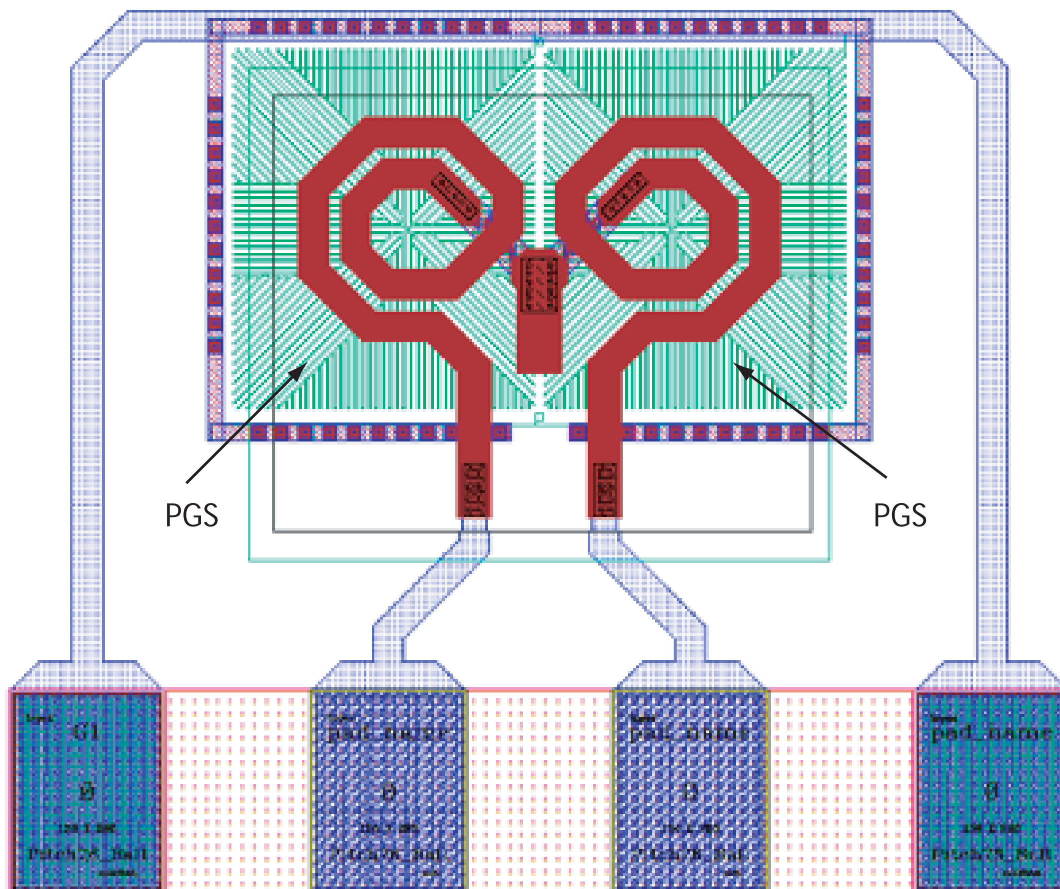


Figure 5.1: Patterned ground shielding blocks coupling to the substrate while interrupting the magnetic fields created by the inductor windings. Thereby, reducing substrate loss and improving the quality factor of the inductor.

minimize use of such components, unless ESD protection is being specifically investigated.

- More attention should be paid to device modeling and optimization to reduce phase noise in RF VCOs.

5.3.2 VCO with Tunable Polyphase

- Future I/Q measurements for the VCO with tunable polyphase could be accomplished by incorporating reference signal outputs. As discussed above, the time-domain measurement system relies heavily on a shared phase reference. An issue that arose during testing is that the VCO output has a low-frequency drift. This means a fixed external reference signal is not beneficial, since the oscilloscope relies on a trigger that is related to the source signal to make accurate phase measurements. A possible solution is to downconvert the direct VCO output to provide a reference that the oscilloscope can utilize for triggering during phase measurements. This would require a redesigned integrated polyphase VCO with an additional differential output reference signal [Figure 5.2(a)]. The differential reference signal could then be mixed down to an IF frequency that is compatible with the oscilloscope [Figure 5.2(b)]. Therefore, an additional mixer and a five-way power divider would be needed to complete the test measurement system.

- Another benefit from having measurable outputs directly after the VCO as well as after the tunable polyphase would be the ability to directly acquire phase noise measurements from the VCO integrated with the polyphase. In this work, phase-noise measurements for the VCO with tunable polyphase were compared to those made on the standalone VCO in [20]; that is, the comparison is made between two different VCO samples. In contrast, measuring the phase noise from the output path of the VCO as well as after the tunable polyphase allows for direct comparison of results from the same sample. This approach may lead to a better understanding of how the tunable polyphase and associated buffers may impact phase-noise performance in such a circuit.

- A problem with the proposed time-domain measurement in this work is that

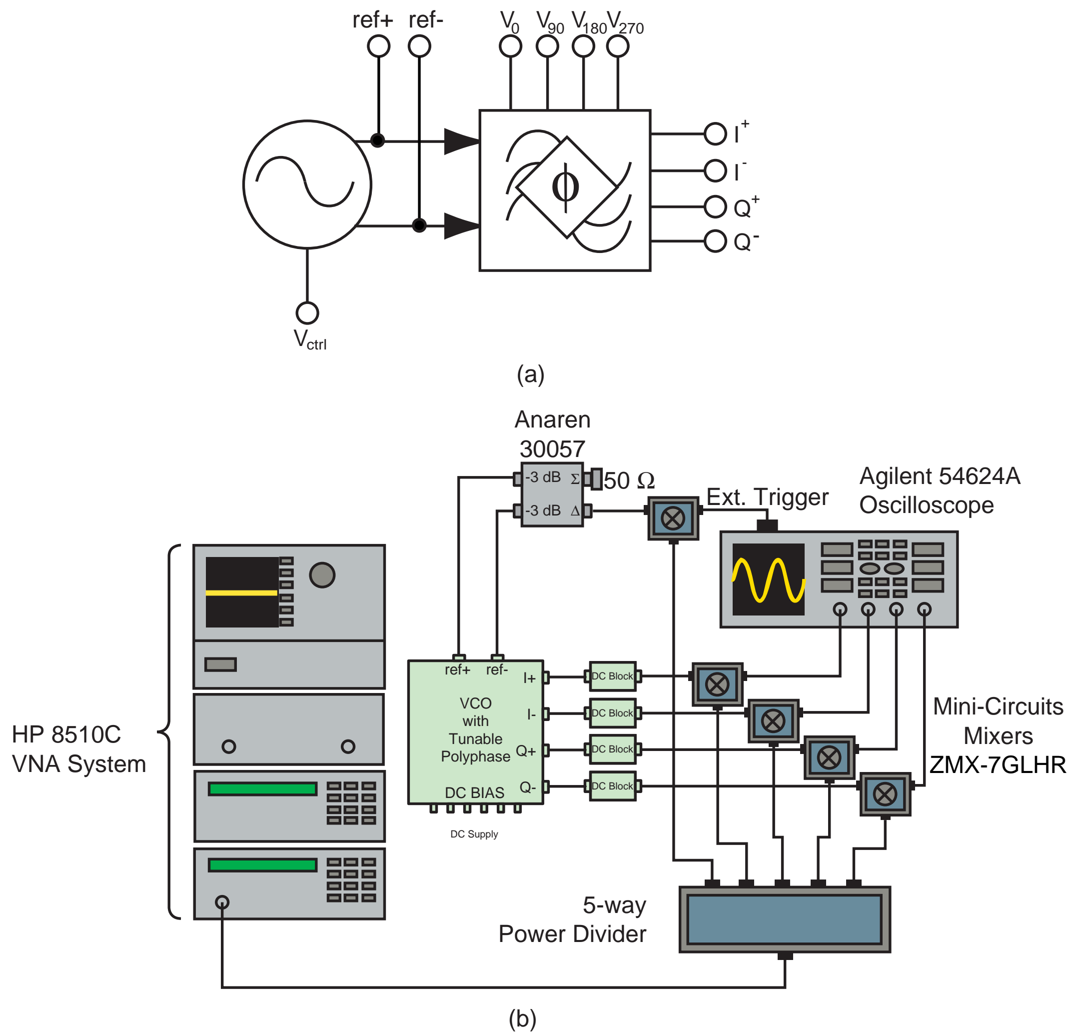


Figure 5.2: (a) Integrated polyphase VCO with two additional outputs for a differential reference signal (ref^+ and ref^-). (b) Measurement system using the source signal (direct VCO output) for a triggering reference.

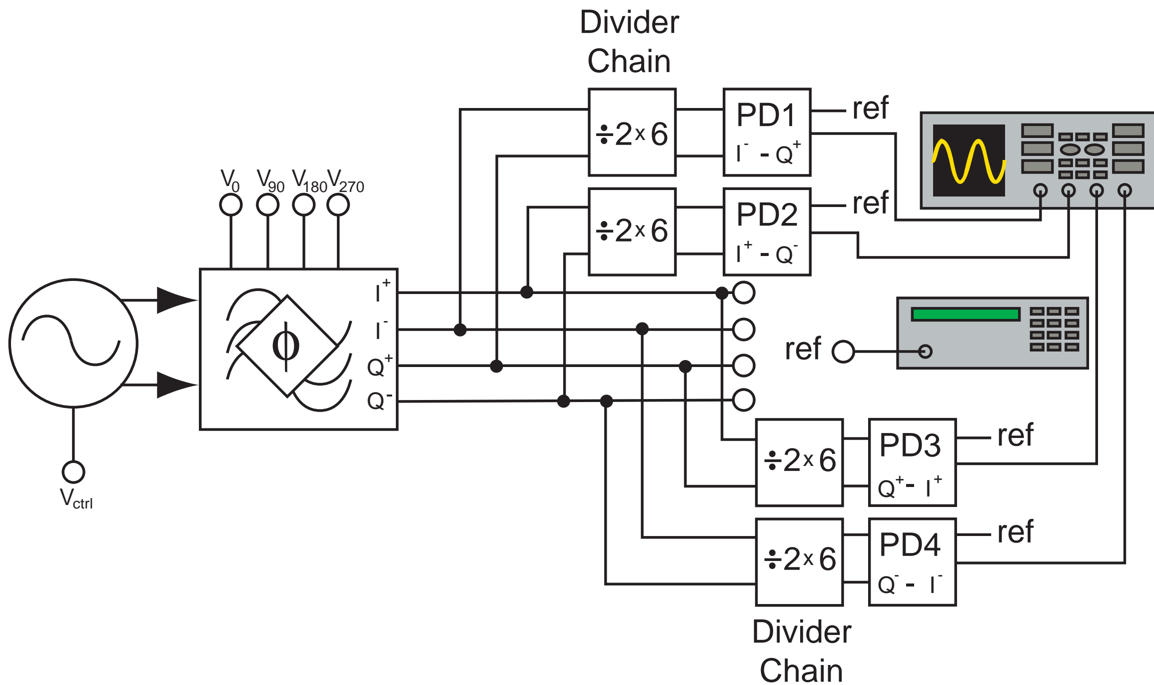


Figure 5.3: An overall system incorporating frequency dividers and the charge-pump phase detectors.

mixers were used to downconvert the measured output. Calibration issues and degraded signal amplitudes arriving to the oscilloscope resulted in inaccurate phase error measurements. Therefore, a revised setup would eliminate mixers all together and utilize *phase detectors*. A phase detector (PD) simply measures the difference in phase between two signals and outputs a voltage proportional to the phase difference. There are many different types of phase detector topologies, however, the charge-pump topology is practical for this kind of measurement [73]. The charge-pump PD will output a voltage that is directly proportional to the difference in phase. The outputs are averaged using a sample and hold circuit, which will output a proportional voltage corresponding to the phase change. In the 5-6 GHz design, the output of the polyphase filters will need to be divided by a chain of six 1/2 frequency dividers, followed by the phase detector itself (Figure 5.3). The output of the phase detector can be measured on a typical oscilloscope.

- Development of self-correcting VCO circuits that measure output I/Q phase

error and feed this back for dynamic corrections for low bit error rate (BER) or high-image rejection communications systems.

Appendix A

Matlab Code

A.1 plot_polyphase_vna.m

```
clear all;
close all;
% ASK's path
p_prefix = 'k:\08.27.2003\E2p_';
n_prefix = 'k:\08.27.2003\E2n_';
tuneI = 0:0.5:2.5;
tuneQ = 0:0.5:2.5;
freq = 5:0.00125:6;
%DIS's path
% p_prefix = 'E:\users\rms\cat\together\E2p_';
% n_prefix = 'E:\users\rms\cat\together\E2m_';
% tuneI = [0.5 1.5 2.5];
% tuneQ = [0.5 1.5 2.5];
% freq = 4.5:0.005:6.5;
```

```
for i = 1:length(tuneI)

% In+ -> I+ I sweep with fixed Q 2.5

t = dlmread([p_prefix 'I+_I' num2str(tuneI(i)) 'V_Q2.5V.csv'],',',1,1);

realval = t(:,1);

imagval = t(:,2);

INp_Ip_Is_Qf(:,i) = complex(realval,imagval);

% In+ -> I- I sweep with fixed Q 2.5

t = dlmread([p_prefix 'I-_I' num2str(tuneI(i)) 'V_Q2.5V.csv'],',',1,1);

realval = t(:,1);

imagval = t(:,2);

INp_In_Is_Qf(:,i) = complex(realval,imagval);

% In+ -> Q+ I sweep with fixed Q 2.5

t = dlmread([p_prefix 'Q+_I' num2str(tuneI(i)) 'V_Q2.5V.csv'],',',1,1);

realval = t(:,1);

imagval = t(:,2);

INp_Qp_Is_Qf(:,i) = complex(realval,imagval);

% In+ -> Q- I sweep with fixed Q 2.5

t = dlmread([p_prefix 'Q-_I' num2str(tuneI(i)) 'V_Q2.5V.csv'],',',1,1);

realval = t(:,1);

imagval = t(:,2);

INp_Qn_Is_Qf(:,i) = complex(realval,imagval);

% In- -> I+ I sweep with fixed Q 2.5

t = dlmread([n_prefix 'I+_I' num2str(tuneI(i)) 'V_Q2.5V.csv'],',',1,1);

realval = t(:,1);

imagval = t(:,2);
```

```
INn_Ip_Is_Qf(:,i) = complex(realval,imagval);
% In- –> I- I sweep with fixed Q 2.5
t = dlmread([n_prefix 'I-_I' num2str(tuneI(i)) 'V_Q2.5V.csv'],',',1,1);
realval = t(:,1);
imagval = t(:,2);
INn_In_Is_Qf(:,i) = complex(realval,imagval);
% In- –> Q+ I sweep with fixed Q 2.5
t = dlmread([n_prefix 'Q+_I' num2str(tuneI(i)) 'V_Q2.5V.csv'],',',1,1);
realval = t(:,1);
imagval = t(:,2);
INn_Qp_Is_Qf(:,i) = complex(realval,imagval);
% In- –> Q- I sweep with fixed Q 2.5
t = dlmread([n_prefix 'Q-_I' num2str(tuneI(i)) 'V_Q2.5V.csv'],',',1,1);
realval = t(:,1);
imagval = t(:,2);
INn_Qn_Is_Qf(:,i) = complex(realval,imagval);
end
for i = 1:length(tuneQ)
% In+ –> I+ Q sweep with fixed I 2.5
t = dlmread([p_prefix 'I+_Q' num2str(tuneI(i)) 'V_I2.5V.csv'],',',1,1);
realval = t(:,1);
imagval = t(:,2);
INp_Ip_Qs_If(:,i) = complex(realval,imagval);
% In+ –> I- Q sweep with fixed I 2.5
t = dlmread([p_prefix 'I-_Q' num2str(tuneI(i)) 'V_I2.5V.csv'],',',1,1);
```

```
realval = t(:,1);
imagval = t(:,2);
INp_In_Qs_If(:,i) = complex(realval,imagval);
% In+ -> Q+ Q sweep with fixed I 2.5
t = dlmread([p_prefix 'Q+_Q' num2str(tuneI(i)) 'V_I2.5V.csv'],',',1,1);
realval = t(:,1);
imagval = t(:,2);
INp_Qp_Qs_If(:,i) = complex(realval,imagval);
% In+ -> Q- Q sweep with fixed I 2.5
t = dlmread([p_prefix 'Q-_Q' num2str(tuneI(i)) 'V_I2.5V.csv'],',',1,1);
realval = t(:,1);
imagval = t(:,2);
INp_Qn_Qs_If(:,i) = complex(realval,imagval);
% In- -> I+ Q sweep with fixed I 2.5
t = dlmread([n_prefix 'I+_Q' num2str(tuneI(i)) 'V_I2.5V.csv'],',',1,1);
realval = t(:,1);
imagval = t(:,2);
INn_Ip_Qs_If(:,i) = complex(realval,imagval);
% In- -> I- Q sweep with fixed I 2.5
t = dlmread([n_prefix 'I-_Q' num2str(tuneI(i)) 'V_I2.5V.csv'],',',1,1);
realval = t(:,1);
imagval = t(:,2);
INn_In_Qs_If(:,i) = complex(realval,imagval);
% In- -> Q+ Q sweep with fixed I 2.5
t = dlmread([n_prefix 'Q+_Q' num2str(tuneI(i)) 'V_I2.5V.csv'],',',1,1);
```

```
realval = t(:,1);
imagval = t(:,2);
INn_Qp_Qs_If(:,i) = complex(realval,imagval);
% In- –> Q- Q sweep with fixed I 2.5
t = dlmread([n_prefix 'Q-_Q' num2str(tuneI(i)) 'V_I2.5V.csv'],',',1,1);
realval = t(:,1);
imagval = t(:,2);
INn_Qn_Qs_If(:,i) = complex(realval,imagval);
end
for i = 1:length(tuneI)
Ip_diff_Isweep_phase(:,i) = angle(INp_Ip_Is_Qf(:,i)-INn_Ip_Is_Qf(:,i));
In_diff_Isweep_phase(:,i) = angle(INp_In_Is_Qf(:,i)-INn_In_Is_Qf(:,i));
Qp_diff_Isweep_phase(:,i) = angle(INp_Qp_Is_Qf(:,i)-INn_Qp_Is_Qf(:,i));
Qn_diff_Isweep_phase(:,i) = angle(INp_Qn_Is_Qf(:,i)-INn_Qn_Is_Qf(:,i));
end
for i = 1:length(tuneQ)
Ip_diff_Qsweep_phase(:,i) = angle(INp_Ip_Qs_If(:,i)-INn_Ip_Qs_If(:,i));
In_diff_Qsweep_phase(:,i) = angle(INp_In_Qs_If(:,i)-INn_In_Qs_If(:,i));
Qp_diff_Qsweep_phase(:,i) = angle(INp_Qp_Qs_If(:,i)-INn_Qp_Qs_If(:,i));
Qn_diff_Qsweep_phase(:,i) = angle(INp_Qn_Qs_If(:,i)-INn_Qn_Qs_If(:,i));
end
Ip_In = (Ip_diff_Isweep_phase - In_diff_Isweep_phase);
Qp_Ip = ((Qp_diff_Isweep_phase - Ip_diff_Isweep_phase)*(180/pi));
Ip_Qn = ((Ip_diff_Isweep_phase - Qn_diff_Isweep_phase)*(180/pi));
In_Qp = ((In_diff_Isweep_phase - Qp_diff_Isweep_phase)*(180/pi));
```

```
Qn_In = ((Qn_diff_Isweep_phase - In_diff_Isweep_phase)*(180/pi));

for i = 1:length(tuneI)

figure(i);

plot(freq,unwrap(In_Qp(:,i)+(In_Qp(:,i)<0)*360));

hold on;plot(freq,unwrap(Qn_In(:,i)+(Qn_In(:,i)<0)*360),'r');

plot(freq,unwrap(Ip_Qn(:,i)+(Ip_Qn(:,i)<0)*360),'c');

plot(freq,unwrap(Qp_Ip(:,i)+(Qp_Ip(:,i)<0)*360),'k');

title(['I = ' num2str(tuneI(i)) ' V Q=2.5 V']);

legend('I^–Q^+','Q^–I^-','I^+-Q^-','Q^+-I^+');

end

check1 = unwrap(In_Qp(:,i)+(In_Qp(:,i)<0)*360) + unwrap(Qn_In(:,i)+(Qn_In(:,i)<0)*360)
+ unwrap(Ip_Qn(:,i)+(Ip_Qn(:,i)<0)*360) + unwrap(Qp_Ip(:,i)+(Qp_Ip(:,i)<0)*360);

check2 = (In_Qp(:,i)+(In_Qp(:,i)<0)*360) + (Qn_In(:,i)+(Qn_In(:,i)<0)*360) + (Ip_Qn(:,i)+(Ip_Qn(:,i)
+ (Qp_Ip(:,i)+(Qp_Ip(:,i)<0)*360);
```

A.2 plot_polyphase_timedomain.m

```
%******************************FORMAT******************************

%RFfreq LOfreq IFfreq ch1-ch2 ch1-ch3 ch1-ch4 ch2-ch3 ch2-ch4
ch3-ch4

%******************************************************************

% Ch4 = I-

% Ch3 = I+

% Ch2 = Q-

% Ch1 = Q+

% data col = 8 -> ch1 - ch2 Qp-Qn

% data col = 9 -> ch1 - ch3 Qp-Ip
```

```
% data col = 10 -> ch1 - ch4 Qp-In
% data col = 11-> ch2 - ch3 Qn-Ip
% data col = 12-> ch2 - ch4 Qn-In
% data col = 13-> ch3 - ch4 Ip-In
% data col = 4-> ch1 amp
% data col = 5-> ch2 amp
% data col = 6-> ch3 amp
% data col = 7-> ch4 amp
clear all;
close all;
%%*************** Calibration Data **********************************%%%
PD_1_P1 = dlmread('K:\07.28.2003\PD_1_P1_S21.csv',',',1,0);
PD_1_P2 = dlmread('K:\07.28.2003\PD_1_P2_S21.csv',',',1,0);
PD_1_P3 = dlmread('K:\07.28.2003\PD_1_P3_S21.csv',',',1,0);
PD_1_P4 = dlmread('K:\07.28.2003\PD_1_P4_S21.csv',',',1,0);
PD_2_P1 = dlmread('K:\07.28.2003\PD_2_P1_S21.csv',',',1,0);
PD_2_P2 = dlmread('K:\07.28.2003\PD_2_P2_S21.csv',',',1,0);
PD_2_P3 = dlmread('K:\07.28.2003\PD_2_P3_S21.csv',',',1,0);
PD_2_P4 = dlmread('K:\07.28.2003\PD_2_P4_S21.csv',',',1,0);
PDFREQ=4:0.0025:6;
ch1ch2 = unwrap(PD_1_P1(:,3)-PD_1_P2(:,3));
ch1ch3 = unwrap(PD_1_P1(:,3)-PD_1_P3(:,3));
ch1ch4 = unwrap(PD_1_P1(:,3)-PD_1_P4(:,3));
ch2ch3 = unwrap(PD_1_P2(:,3)-PD_1_P3(:,3));
ch2ch4 = unwrap(PD_1_P2(:,3)-PD_1_P4(:,3));
```

```
ch3ch4 = unwrap(PD_1_P3(:,3)-PD_1_P4(:,3));

PD = [ch1ch2 ch1ch3 ch1ch4 ch2ch3 ch2ch4 ch3ch4];

MIXPD_temp = dlmread('K:\09.05.2003\mixerr_Phase_error4.csv',',',1,0);

MIXPD = MIXPD_temp(:,4:9) - PD(401:20:end,:); %subtract out powerdivider #1 from
mixer calibration

MIXPD = unwrap(MIXPD+(MIXPD<0)*360);

MIXPDFREQ=5:0.1:6;

TUNEMIXPD1 = dlmread('K:\09.05.2003\calculated.data.csv',','); %read in 0 -> 2.5V

RFfreq1 = 5:.05:6;

tunestep1=0:2.5:2.5;

% TUNEMIXPD2(:,8:13) = TUNEMIXPD2(:,8:13) + (TUNEMIXPD2(:,8:13)<0)*360;

% TUNEMIXPD2(:,8:13) = TUNEMIXPD2(:,8:13) + (TUNEMIXPD2(:,8:13)<0)*360; %
again

data1 = TUNEMIXPD1;

count = 1;

for i = 1:4:length(TUNEMIXPD1)

data1(i:i+3,8:13) = TUNEMIXPD1(i:i+3,8:end) - repmat(MIXPD(count,:),4,1);

data1(i:i+3,8:13) = data1(i:i+3,8:13)+(data1(i:i+3,8:13)<0)*360;

data1(i:i+3,8:13) = data1(i:i+3,8:13)+(data1(i:i+3,8:13)<0)*360; % do it again

count = count+1;

end

% data1(:,8:13) = data1(:,8:13)+(data1(:,8:13)<0)*360;

% data1(:,8:13) = data1(:,8:13)+(data1(:,8:13)<0)*360; %do it again

%%%*********************** DATA 1 ******************************%%%

figure(1);

plot(RFfreq1,unwrap(data1(1:4:end,9)));
```

```
hold on;plot(RFfreq1,unwrap(data1(2:4:end,9)),’r’);
plot(RFfreq1,unwrap(data1(3:4:end,9)),’g’);
plot(RFfreq1,unwrap(data1(4:4:end,9)),’c’);
xlabel(’Frequency (GHz)’);ylabel(’Relative Phase (degrees)’);
title(’Qˆ+ - Iˆ+’);
legend(’I=0, Q=0’, ’I=0, Q=2.5’, ’I=2.5, Q=0’, ’I=2.5, Q=2.5’);
figure(2);
plot(RFfreq1,unwrap(data1(1:4:end,10)));
hold on;plot(RFfreq1,unwrap(data1(2:4:end,10)),’r’);
plot(RFfreq1,unwrap(data1(3:4:end,10)),’g’);
plot(RFfreq1,unwrap(data1(4:4:end,10)),’c’);
xlabel(’Frequency (GHz)’);ylabel(’Relative Phase (degrees)’);
title(’Iˆ- - Qˆ+’);
legend(’I=0, Q=0’, ’I=0, Q=2.5’, ’I=2.5, Q=0’, ’I=2.5, Q=2.5’);
figure(3);
plot(RFfreq1,unwrap(data1(1:4:end,11)));
hold on;plot(RFfreq1,unwrap(data1(2:4:end,11)),’r’);
plot(RFfreq1,unwrap(data1(3:4:end,11)),’g’);
plot(RFfreq1,unwrap(data1(4:4:end,11)),’c’);
xlabel(’Frequency (GHz)’);ylabel(’Relative Phase (degrees)’);
title(’Iˆ+ - Qˆ-’);
legend(’I=0, Q=0’, ’I=0, Q=2.5’, ’I=2.5, Q=0’, ’I=2.5, Q=2.5’);
figure(4)
plot(RFfreq1,unwrap(data1(1:4:end,12)));
hold on;plot(RFfreq1,unwrap(data1(2:4:end,12)),’r’);
```

```
plot(RFfreq1,unwrap(data1(3:4:end,12)),'g');
plot(RFfreq1,unwrap(data1(4:4:end,12)),'c');
xlabel('Frequency (GHz)');ylabel('Relative Phase (degrees)');
title('I^- - Q^+');
legend('I=0, Q=0', 'I=0, Q=2.5', 'I=2.5, Q=0', 'I=2.5, Q=2.5');
figure(5)
plot(RFfreq1,unwrap(data1(1:4:end,8)));
hold on;plot(RFfreq1,unwrap(data1(2:4:end,8)),'r');
plot(RFfreq1,unwrap(data1(3:4:end,8)),'g');
plot(RFfreq1,unwrap(data1(4:4:end,8)),'c');
xlabel('Frequency (GHz)');ylabel('Relative Phase (degrees)');
title('Q^+ - Q^-');
legend('I=0, Q=0', 'I=0, Q=2.5', 'I=2.5, Q=0', 'I=2.5, Q=2.5');
figure(6)
plot(RFfreq1,unwrap(data1(1:4:end,13)));
hold on;plot(RFfreq1,unwrap(data1(2:4:end,13)),'r');
plot(RFfreq1,unwrap(data1(3:4:end,13)),'g');
plot(RFfreq1,unwrap(data1(4:4:end,13)),'c');
xlabel('Frequency (GHz)');ylabel('Relative Phase (degrees)');
title('I^+ - I^-');
legend('I=0, Q=0', 'I=0, Q=2.5', 'I=2.5, Q=0', 'I=2.5, Q=2.5');
figure(8);
subplot(2,2,1);
p = polyfit(RFfreq1', unwrap(data1(2:4:end,10)), 6); y = polyval(p, RFfreq1);
plot(RFfreq1,unwrap(data1(2:4:end,10))); hold on;
```

```
p = polyfit(RFfreq1', unwrap(data1(4:4:end,10)), 6); y = polyval(p, RFfreq1);
plot(RFfreq1,unwrap(data1(4:4:end,10)),'g');
p = polyfit(RFfreq1', unwrap(data1(3:4:end,10)), 6); y = polyval(p, RFfreq1);
plot(RFfreq1,unwrap(data1(3:4:end,10)),'r');
xlabel('Frequency (GHz)');ylabel('Relative Phase (degrees)');
title('I^- - Q^+');
legend('I=0, Q=2.5', 'I=2.5, Q=2.5', 'I=2.5, Q=0');
subplot(2,2,2);
p = polyfit(RFfreq1', unwrap(data1(2:4:end,11)), 6); y = polyval(p, RFfreq1);
plot(RFfreq1,unwrap(data1(2:4:end,11))); hold on;
p = polyfit(RFfreq1', unwrap(data1(4:4:end,11)), 6); y = polyval(p, RFfreq1);
plot(RFfreq1,unwrap(data1(4:4:end,11)),'g');
p = polyfit(RFfreq1', unwrap(data1(3:4:end,11)), 6); y = polyval(p, RFfreq1);
plot(RFfreq1,unwrap(data1(3:4:end,11)),'r');
xlabel('Frequency (GHz)');ylabel('Relative Phase (degrees)');
title('I^+ - Q^-');
legend('I=0, Q=2.5', 'I=2.5, Q=2.5', 'I=2.5, Q=0');
subplot(2,2,3);
p = polyfit(RFfreq1', unwrap(data1(2:4:end,9)), 6); y = polyval(p, RFfreq1);
plot(RFfreq1,unwrap(data1(2:4:end,9)));hold on;
p = polyfit(RFfreq1', unwrap(data1(4:4:end,9)), 6); y = polyval(p, RFfreq1);
plot(RFfreq1,unwrap(data1(4:4:end,9)),'g');
p = polyfit(RFfreq1', unwrap(data1(3:4:end,9)), 6); y = polyval(p, RFfreq1);
plot(RFfreq1,unwrap(data1(3:4:end,9)),'r');
xlabel('Frequency (GHz)');ylabel('Relative Phase (degrees)');
```

```
title('Q^+ - I^+');
legend('I=0, Q=2.5', 'I=2.5, Q=2.5', 'I=2.5, Q=0');
subplot(2,2,4);
p = polyfit(RFfreq1', unwrap(data1(2:4:end,12)), 6); y = polyval(p, RFfreq1);
plot(RFfreq1,unwrap(data1(2:4:end,12)));hold on;
p = polyfit(RFfreq1', unwrap(data1(4:4:end,12)), 6); y = polyval(p, RFfreq1);
plot(RFfreq1,unwrap(data1(4:4:end,12)),'g');
p = polyfit(RFfreq1', unwrap(data1(3:4:end,12)), 6); y = polyval(p, RFfreq1);
plot(RFfreq1,unwrap(data1(3:4:end,12)),'r');
xlabel('Frequency (GHz)');ylabel('Relative Phase (degrees)');
title('Q^- - I^-');
legend('I=0, Q=2.5', 'I=2.5, Q=2.5', 'I=2.5, Q=0');
figure(9);
for i=1:4
check3(:,i)=unwrap(data1(i:4:end,9))+unwrap(data1(i:4:end,10))+...
unwrap(data1(i:4:end,11))+unwrap(data1(i:4:end,12));
end
plot(RFfreq1,check3(:,2:4))
hold on; plot(RFfreq1, ones(1,length(RFfreq1))*360,'k');
legend('I=0, Q=2.5', 'I=2.5, Q=2.5', 'I=2.5, Q=0');
xlabel('Frequency (GHz)');ylabel('Relative Phase (degrees)');
check4=MIXPD(:,1)+MIXPD(:,3)+MIXPD(:,4)+MIXPD(:,5);
```

Bibliography

[1] International Data Corporation, "Lucent smells demand for mobile data," 2003. http://www.idc.com.

[2] J. D. Cressler, "SiGe HBT technology: A new contender for si-based RF and microwave circuit applications," *IEEE Trans. on Microwave Theory and Techniques*, vol. 46, no. 5, pp. 572–589, May 1998.

[3] G. L. Patton, S. S. Iyer, S. L. Delage, S. Tiwari, and J. M. C. Stork, "Silicon-germanium-base heterojunction bipolar transistors by molecular beam epitaxy," *IEEE Electron Device Letters*, vol. 9, pp. 165–167, April 1988.

[4] J. P. John, F. Chai, D. Morgan, T. Keller, J. Kirchgessner, R. Reuter, H. Rueda, J. Teplik, J. White, S. Wipf, and D. Zupac, "Optimization of a SiGe:C HBT in a BiCMOS technology for low power wireless applications," *IEEE Bipolar/BiCMOS Circuits and Technology Meeting 2002*, pp. 193–196, 2002.

[5] B. Jagannathan, M. Khater, F. Pagette, J. S. Rieh, D. Angell, H. Chen, J. Florkey, F. Golan, and G. Freeman, "Self-aligned SiGe NPN transistors with 285 GHz fmax and 207 GHz ft in a manufacturable technology," *IEEE Electron Device Letters*, vol. 23, pp. 258–260, May 2002.

[6] TSMC, "$TSMCProcessTechnology : SiGeBiCMOS$," 2003. Available: http://www.tsmc.com/english/technology/t0108.htm.

[7] W. Hafez, J. Lai, and M. Feng, "Submicron InP-InGaAs single heterojunction bipolar transistor with f_T of 377 GHz," *IEEE Electron Device Letters*, vol. 24, pp. 292–294, May 2003.

[8] J. Rieh, B. Jagannathan, H. Chen, K. Schonenberg, S. Jeng, M. Khater, D. Ahlgren, G. Freeman, and S. Subbanna, "Performance and design considerations for high speed SiGe HBTs of f_T/f_{max}=375GHz/210GHz," in *International Conference on Indium Phosphide and Related Materials, 2003. May 12-16, 2003*, pp. 374–377.

[9] H. Kroemer, "Heterostructure bipolar transistors and integrated circuits," *Proceedings of the IEEE*, vol. 70, pp. 13–25, Jan. 1982.

[10] J. S. Yuan, *SiGe, GaAs, and InP Heterojunction Bipolar Transistors*. New York: John Wiley and Sons, Inc., 1999.

[11] H. Kroemer, "Theory of wide-gap emitter for transistors," *Proceedings of the Institute of Radio Engineers (IRE)*, vol. 45, pp. 1535–1537, Nov 1957.

[12] J. M. Early, "Effects of space-charge layer widening in junction transistors," *Proc. IRE*, vol. 40, pp. 1401–1406, 1952.

[13] A. J. Joseph, J. D. Cressler, D. M. Richey, R. C. Jaeger, and D. L. Harame, "Neutral base recombination and its influence on the temperature dependence of early voltage and current gain-early voltage product in early voltage and current gain-early voltage product in SiGe heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 44, pp. 404–413, March 1997.

[14] J. Ma, H. Liang, D. Ngo, E. Spears, B. Yeung, B. Courson, D. Spooner, D. Lamey, J. Alvarez, T. Teraji, J. Ford, S. Cheng, "Silicon RF-GCMOS IC technology for RF mixed-mode wireless applications," *IEEE MTT-S Digest*, pp. 123–127, 1997.

[15] J. A. Babcock, C. E. Gill, J. M. Ford, D. Ngo, E. Spears, J. Ma, H. Liang, D. J. Spooner, and S. Cheng, "$1/f$ noise in graded-channel MOSFETs for low-power low-cost RFICs," *Device Research Conference Digest*, vol. 55, pp. 122–123, 1997.

[16] J. Ma, H. Liang, M. Kaneshiro, C. Kyono, R. Pryer, K. Papworth , and S. Cheng, "A graded-channel MOS (GCMOS) VLSI technology for low power DSP applications," in *ISLPED 1996 Monterey CA*, 1996.

[17] F. K. Chai, C. Kyono, V. Ilderman, M. Kaneshiro, D. Zupac, S. Bigelow, C. Ramiah, P. Dahl, R. Braithwaite, D. Morgan, S. Hildreth, G. Grynkewich, "A

cost-effecive 0.25 μm L_{eff} BiCMOS technology featuring graded-channel CMOS (GCMOS) and a quasi-self-aligned (QSA) NPN for RF wireless applications," *IEEE BCTM*, pp. 110–113, 2000.

[18] S. Subbana, D. Ahlgren, D. Harame, and B. Meyerson, "How SiGe evolved into a manufacturable semiconductor production process," in *1999 IEEE International Solid-State Circuit Conference*, pp. 66–67, 446, 1999.

[19] D. L. Harame, J. H. Comfort, J. D. Cressler, E. F. Crabbe, J. Y.-C. Sun, B. S. Meyerson, and T. Tice, "Si/SiGe epitaxial-base transistors: Part I – materials, physics, and circuits," *IEEE Trans. Electron Devices*, vol. 40, March 1995.

[20] D. I. Sanderson, "A 5-6 GHz silicon-germanium VCO with tunable polyphase outputs," Master's thesis, Virginia Polytechnic Institute and State University, Blacksburg, VA, May 2003.

[21] J. Kirchgessner, S. Bigelow, F. K. Chai, R. Cross, P. Dahl, et. al., "A 0.18 μm SiGe:c RFBiCMOS technology for wireless and gigabit optical communication applications," *IEEE BCTM*, pp. 151–154, 2001.

[22] J. P. John, V. Ilderem, C. Park, J. Teplik, K. Kevin, and S. Cheng, "A low voltage graded-channel MOSFET (LV-GCMOS) for sub 1-volt microcontroller application," *Symposium on VLSI Technology Digest of Technical Papers 1996*, pp. 178–179.

[23] B. Razavi, *RF Microelectronics.* Prentice Hall PTR, 1998.

[24] J. Crols and M. J. Steyaert, "Low-IF topologies for high-performance analog front ends of fully integrated receivers," *IEEE Trans. on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 45, pp. 269–282, March 1998.

[25] B. Razavi, "Design considerations for direct-conversion receivers," *IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 44, pp. 428–435, June 1997.

[26] D. Sanderson and S. Raman, "5-6 GHz SiGe VCO with tunable polyphase output for analog image rejection and IQ mismatch compensation," in *2003 RFIC Symposium Digest*, (Philadelphia, PA), pp. 683–686, June 8-10 2003.

[27] M. Faulkner, "DC offset and IM2 removal in direct conversion receivers," *IEE Proceedings*, vol. 149, pp. 179–184, June 2002.

[28] Ericsson, "EDGE: Introduction of high-speed data in GSM/GPRS networks," *White Paper*, 1999.

[29] 3rd Generation Partnership Project, *3GPP TS 0.05 V8.11.0 (2001-08): Technical Specification Group GSM/EDGE*, 1999.

[30] T. Halonen, J. Romero, and J. Melero, *GSM, GPRS, and EDGE Performance: Evolution Towards 3G/UMTS.* New York: John Wiley & Sons, 2002.

[31] W. P. Robins, *Phase Noise in Signal Sources.* London: Peregrinus, 1982.

[32] U. L. Rohde, *Microwave and Wireless Synthesizers.* John Wiley & Sons, Inc., 1997.

[33] B. Razavi, K. F. Lee, and R. Yan, "A 13.4-GHz CMOS frequency divider," in *1994. Digest of Technical Papers. 41st ISSCC.*, pp. 176 –177, 1994.

[34] A. Grebene, *Bipolar and MOS Analog Integrated Circuit Design*, vol. ISBN 0-471-08529-4. New York: J. Wiley Sons, 1984.

[35] B. Parzen, *Design of Crystal and Other Harmonic Oscillators.* John Wiley & Sons, 1983.

[36] R. L. Bunch, "A fully monolithic 2.5 GHz LC voltage controlled oscillator in 0.35 um CMOS technology," Master's thesis, Virginia Polytechnic Institute and State University, Blacksburg, VA, 2001.

[37] A. S. Sedra, *Microelectronic Circuits.* New York: Oxford University Press, 1998.

[38] W. Chen, *The VLSI Handbook.* IEEE Press, 1999.

[39] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits.* Cambridge University Press, 1998.

[40] D. P. Triantis, A. N. Birbas, and D. Kondis, "Thermal noise modeling for short-channel MOSFET's," *IEEE Transactions on Electron Devices*, vol. 43, pp. 1950–1955, Nov. 1996.

[41] T. Manku, "Microwave CMOS - device physics and design," *IEEE Journal of Solid State Circuits*, vol. 34, pp. 277–285, March 1999.

[42] B. Van Haaren, M. Regis, A. Gruhle, M. Mouis, O. Llopis, L. Escotte, J. Graffeuil, adn R. Plana, "Nose properties of SiGe heterojunction bipolar transistors," in *Silicon Monolithic Integrated Circuits in RF Systems, 1998. Digest of Papers. 1998 Topical Meeting on , 17-18 Sept. 1998*, pp. 24–32, Sept 1998.

[43] J. G. Tartarin, R. Plana, M. Borgarino, H. Lafontaine, M. Regis, O. Llopis, and S. Kovacic, "Noise properties in SiGe BiCMOS devices," in *High Performance Electron Devices for Microwave and Optoelectronic Applications, 1999. EDMO. 1999 Symposium on , 22-23 Nov. 1999*, pp. 131–136, Nov 1999.

[44] J. Moller, B. Heinemann, and F. Herzel, "An improved model for high-frequency noise in BJTs and HBTs interpolating between teh quasi-thermal approach and the correlated-shot-noise model," in *Bipolar/BiCMOS Circuits and Technology Meeting, 2002. Proceedings of the 2002 , 29 Sept.-1 Oct. 2002*, pp. 228–231, Sept 2002.

[45] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," *Proceedings of IEEE*, vol. 54, pp. 329–330, Feb 1966.

[46] A. Hajimiri, T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE Journal of Solid State Circuits*, vol. 33, pp. 179–194, Feb 1998.

[47] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 331–343, March 1996.

[48] S. Haykin, *Communication Systems.* John Wiley & Sons, Inc., 4th ed., 2001.

[49] L. S. Cutler and C. L. Searle, "Some aspects of the theory and measurement of frequency fluctuations in frequency standards," *Proceedings of IEEE*, vol. 54, pp. 136–154, 1966.

[50] T. H. Lee and A. Hajimiri, "Oscillator phase noise: A tutorial," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 326–336, March 2000.

[51] C. P. Yue and S. S. Wang, "On-chip spiral inductors with patterned ground shields for Si-based RF IC's," *IEEE Symposium on VLSI Circuits Digest of Technical Papers*, pp. 56–86, 1997.

[52] J. Craninckx and M. J. Stayaert, "A 1.8 GHz low-phase-noise CMOS VCO using optimized hollow spiral inductors," *IEEE Journal of Solid State Circuits*, vol. 32, pp. 736–744, May 1997.

[53] A. M. Niknajad and R. G. Meyer, "Analysis, design, and optimization of spiral inductors and transformers for Si RF IC's," *IEEE Journal of Solid State Circuits*, vol. 33, pp. 1460–1481, October 1998.

[54] P. Arcioni, R. Castello, L. Perregrini, E. Sacchi, and F. Svelto, "An innovative modelization of loss mechanism in silicon integrated inductors," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 46, pp. 1453–1460, Dec 1999.

[55] J. Craninckx and M. Steyaert, *Wireless CMOS Frequency Synthesizer Design.* Norwell, MA: Kluwer Academic Publishers, 1998.

[56] C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF IC's," *IEEE Journal of Solid State Circuits*, vol. 33, pp. 743–843, May 1998.

[57] J. N. Burghartz, M. Soyuer, and K. A. Jenkins, "Microwave inductors and capacitors in standard multilevel interconnect silicon technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 44, pp. 100–104, Jan 1996.

[58] Agilent Technologies, 395 Page Mill Road, Palo Alto, CA 94304, U.S.A., *Advanced Design System 2002C*, 2002.

[59] Sonnet Software, Inc., Sonnet Software, Inc., Liverpool, NY, 2002, *Sonnet Em Suite 9.01 Beta*, 2003.

[60] J. Rautio, "A conformal mesh for efficient planar electromagnetic analysis." *to be published* in *IEEE Transactions on Microwave Theory and Techniques*, 2003.

[61] Cadence Design Enviornment, Cadence Design Systems, San Jose, CA, 2000, *Cadence Design Enviornment, IC 4.4.6*.

[62] R. L. Bunch and S. Raman, "Large-signal analysis of MOS varactors in CMOS -g_m LC VCOs," *IEEE Journal of Solid State Circuits*, vol. 38, pp. 1325–1332, Aug. 2003.

[63] L. E. Larson, "Integrated circuit technology options for RFIC's - present status and future directions," *IEEE Journal of Solid State Circuits*, vol. 33, March 1998.

[64] D. Wang and X. Wang, "The performance comparison of CMOS vs. bipolar VCO in SiGe BiCMOS technology," in *2003 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, (Philidelphia, PA), June 2003.

[65] B. Razavi, R. Yan, and K. F. Lee, "Impact of distributed gate resistance on the performance of MOS devices," *IEEE Transactions on Circuits and Systems*, vol. 41, pp. 750–754, Nov 1994.

[66] VBIC, "VBIC - vertical bipolar intercompany model web page," 2000. Available: http://www.designers-guide.com/VBIC/.

[67] L. S. Vempati, J. D. Cressler, J. A. Babcock, R. C. Jaeger, and D. L. Harame, "Low-frequency noise in UHV/CVD epitaxial si and SiGe bipolar transistors," *IEEE Journal of Solid State Circuits*, vol. 31, pp. 1458–1467, Oct 1996.

[68] L. E. Larson, "Silicon technology tradeoffs for Radio-Frequency/Mixed-signal "systems-on-a-chip"," *IEEE Trans. on Electron Devices*, vol. 50, pp. 683–699, March 2003. Invited Paper.

[69] M. Rodwell, M. Urteaga, T. Mathew, D. Scott, D. Mensa, Q. Lee, J. Guthrie, Y. Betser, S. C. Martin, R. P. Smith, S. Jaganathan, S. Krishnan, S. I. Long, R. Pullela, B. Agarwal, U. Bhattacharya, L. Samoska, and M. Dahlstrom, "Submicron scaling of HBTs," *IEEE Trans. on Electron Devices*, vol. 48, pp. 2606–2624, Nov 2001.

[70] Cadence Design Systems, Inc., *Affirma RF Simulator (SpectreRF) Theory.* San Jose, CA.: Cadence Design Systems, Inc., June 2000.

[71] F. Behbahani, Y. Kishigami, J. Leete, and A.A. Abidi, "CMOS mixers and polyphase filters for large image rejection," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 873–886, June 2001.

[72] *Agilent VEE 6.0.* Agilent Technologies, Santa Clara, CA. 2002.

[73] W. F. Egan, *Phase-Lock Basics.* New York: John Wiley and Sons, 1998.

Vita

Adam Sherman Klein was born on March 24, 1978 in San Francisco, California. He spent half his life living in Clayton Valley before moving to Lafayette in 1989. He graduated from Compolindo High School in 996, and began his studies in Electrical and Computer Engineering at California Polytechnic State University, Pomona in Fall 1996.

While attending his undergrad at Cal Poly, he worked part time for 1 1/2 years at NASA Jet Propulsion Laboratories in Pasadena, California. At JPL, he worked within the Center for Wireless Telecommunications Research, where he focused his efforts on the design of a command receiver for the Mars Rover Project. This consisted implementation of a 10 kb/s digital demodulator using FPGA technology. He graduated from Cal Poly in 2001, and went on to pursue his Master's Degree in Electrical Engineering at Virginia Tech.

After spending two semesters at Tech, he attended a co-op Summer 2002 at the Motorola Semiconductor Product Sector (SPS) facility in Tempe, Arizona. At Motorola, he worked within the Wireless Broadband Systems Group, where he began designing VCOs for the next generation GSM cell phones. He continued the VCO circuit design at Tech, which soon transformed into his research that is presented in this thesis. Adam will have completed the requirements for the degree of Masters of Science in Electrical Engineering in August, 2005.