Modeling and Control of a Six-Switch Single-Phase Inverter

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Thesis submitted to the Faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

MASTERS OF SCIENCE

in

Electrical Engineering

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August 5, 2005

Blacksburg, VA

Keywords: single-phase inverter, transient performance, power electronics, six-switch, state space control

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Abstract

Distributed generation for consumer applications is a relatively new field and it is difficult to satisfy both cost and performance targets. High expectations coupled with extreme cost cutting to compete with traditional technologies make converter design difficult. As power electronics mature more opportunities arise for entry into this lucrative area. An excellent understanding of converter dynamics is crucial in producing a well performing and cost competitive system.

The six-switch single-phase inverter proposed in this thesis is a prime candidate for use in single households and small businesses. Its compact size and compatibility with existing electrical standards make its integration easy. However, little work is available on characterizing the system from a controls point of view. In particular balancing the two outputs with an uneven load is a concern. This thesis uses nodal and loop analysis to formulate a mathematical model of the six-switch single-phase inverter. A non-linear time invariant model is constructed for circuit simulation; details found in real circuits are added.

A hardware-in-the-loop (HIL) configuration is used for more accurate simulation. In fact, its use makes for an almost seamless transition between simulation and hardware experimentation. A detailed explanation of the HIL system developed is presented.

The system is simulated under various load conditions. Uneven loads and lightly loaded conditions are thoroughly examined. Controllers are verified in simulation and then are tested on real hardware using the HIL system. DC bus disturbance rejection and non-linear loads are also investigated. Acceptable inverter performance is demonstrated without expensive current sensors or high sampling frequency.

Acknowledgements

I would like to express gratitude towards a number of individuals and organizations that have helped me in choosing my career path and growing as an engineer. Without their help I would still be hopelessly torn between several appealing fields.

First, I would like to thank my family who always pushed me to do my best, work through things, and congratulated my achievements. I would like to thank my friends whose interesting ideas and comic relief has helped make it through the difficult times.

I would like to thank Dr. Jason Lai whose trust and wisdom has helped me learn a lot about power electronics. His hands on approach and willingness help out on a moments notice were extremely valuable in many situations. His insistence on real circuits has taught me much that I would have otherwise missed.

I would like to thank Dr. Doug Nelson and the Hybrid Electric Vehicle Team who got me started in power electronics. Dr. Nelson's work with the group has helped numerous students find out how things really work. Steve Gurski, Mike Ogburn, and countless others both kept me entertained and pushed me forward.

I would like to thank the other graduate students at Dr. Lai's Future Energy Electronics Lab: Elton Pepa, Damion Urciuoli, Jeremy Ferrell, Troy Nergaard , Leonard Leslie, Amy Johnson, Andy McLandrich, Mike Schenck, Huijie Yu, Xudong Huang, Changrong Liu. As well, I would like to thank Jerry Francis who was always willing to help out even if he didn't have the answer, yet. Also, I would like to thank Mike Gilliom. Without his extensive help I would not have been able to develop the hardware in the loop system shown in Chapter 3. In fact, the sensor and power board was almost entirely designed by Mike. In addition, I would like to thank Dr. William Baumann whose patience helped me make a somewhat late entry into the controls field.

Lastly, I would like to thank Fairchild Controls whose means helped extensively in finishing this work, and Jeff Graham, whose persistence helped me see the project through.

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Chapter 1 - Introduction

Generating clean AC power for household and small business use is on the rise [25]. Systems such as Uninterruptible Power Supplies (UPS), AC power generators, and active filter line conditioners are just a few examples of power electronic systems that make use of some type of inverter circuit. As with any consumer application, economic concerns play a large factor in system design. With the rise of computer processing power, complex control is used as a tool to decrease overall system cost. This work presents a six-switch inverter, a hardware-in-the-loop (HIL) control system, and several system controller designs. The controllers are evaluated in simulation and then with actual hardware. The power converter system was designed to be highly cost effective. The controller solution was designed to provide maximum design flexibility. The combined system allows the best performance with the use of inexpensive components.

1.1. Background

The inverter used in this work was designed to power a typical residential or small business site. Standalone power sources such as a fuel cell, micro turbine, or solar cells could provide the power. As mentioned in [6] a single-phase three-wire output should be adopted because this is the standard practice for home connection to the grid. In a typical utility system a single-phase from the three-phase high voltage available at the pole is down converted to 120/240V with a center-tapped transformer as in Figure 1.

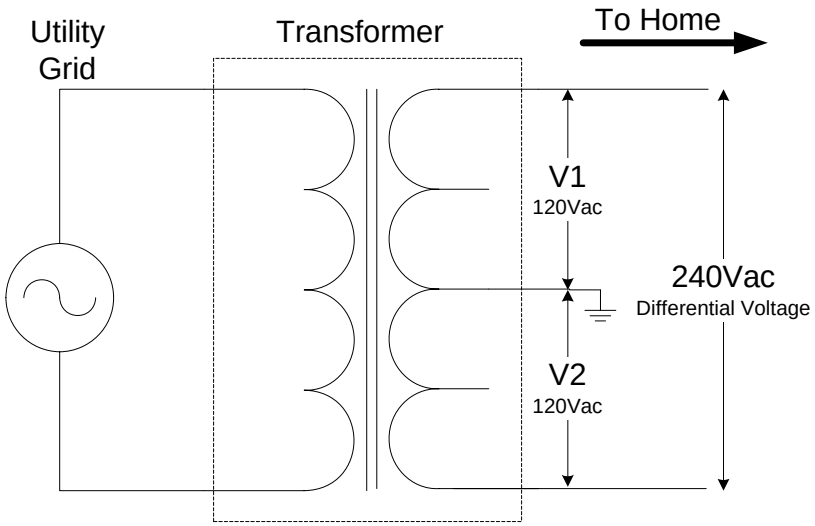


Figure 1. Typical single-phase three-wire transformer. This type of transformer is used by utility companies to interface a single phase of the grid voltage to a single-phase three-wire setup used in residential systems.

The single-phase three-wire approach is used for several reasons. First, it allows the consumer two separate voltage levels: 120V for smaller devices, 240V for larger appliances and HVAC systems. Secondly, it offers twice the load capacity with only 1.5 times the conductors [7].

To fit the existing systems the inverter designed will need a single-phase three-wire output. One important item to note is that many power sources such as fuel cells do not provide a high voltage output. Therefore several stages may be required. The first option would be to design a standard single-phase inverter and couple it to the home with a center-tapped transformer similar to that shown in Figure 1. The turns ratio may be adjusted to step up the voltage, see Figure 2. While this approach is well established the use of the 60 Hz transformer adds cost, size, and inefficiency to the system [7], [27]. There are also issues with voltage regulation and no possibility to tie the inverter to the grid. Additionally, most distributed systems have a DC output and would not directly connect to the inverter. The second approach is to use a DC-DC which steps up the voltage and then an inverter that directly generates both 120V outputs, V_1 and V_2, also in Figure 2.

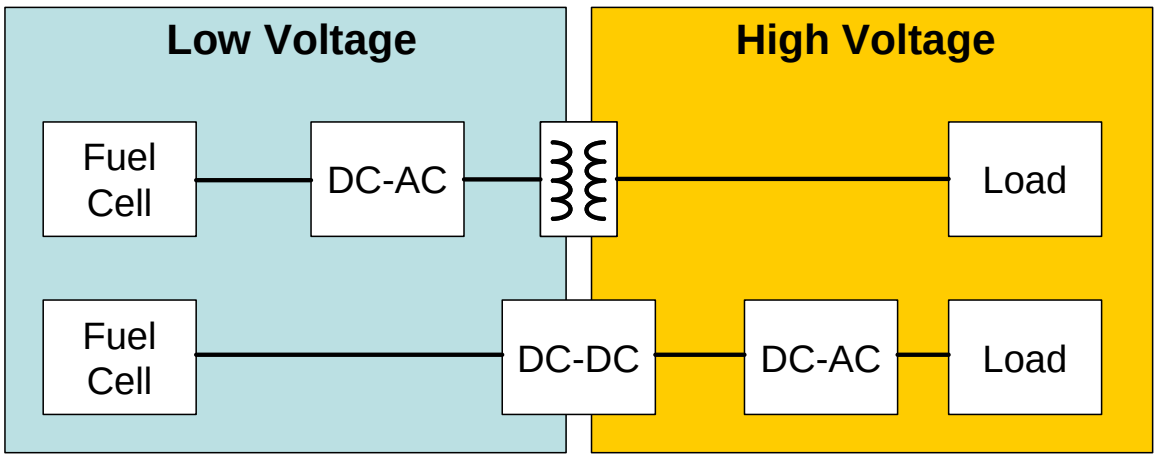


Figure 2. Low voltage power sources need a step up voltage transition. The top system uses a 60 Hz transformer to make the stop from low voltage to high voltage. The lower system uses a high frequency transformer or DC/DC to form a high voltage bus.

Many possible topologies exist but few are commercially practical and reasonably controllable for a high power converter [27]. One commonly used topology is a standard H-bridge inverter. This topology will work in a balanced case but when the load is unbalanced it acts as a voltage divider across the 240Vac. The result is depicted in Figure 3. When the loads are unbalanced V_1 and V_2 are skewed so that neither output has the correct voltage.

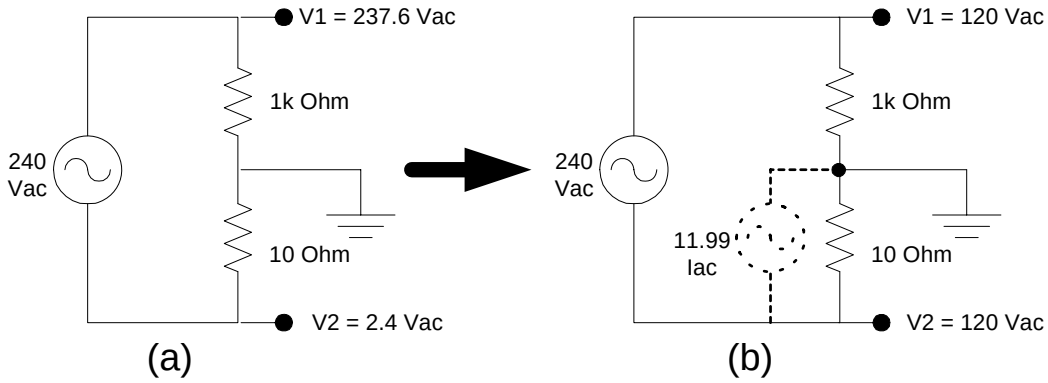


Figure 3. Unbalanced operation and balanced operation. In (a) the system is unbalanced due to a voltage divider effect. In (b) a current source is added which balances the output voltage.

One solution is to form two voltage sources and run the inverter from those, see Figure 4. This option has several problems. First, it requires two regulated sources. This further complicates the power source. One option is to use one voltage source and split the bus with two capacitors. This can work with light loads but under extreme unbalances the capacitors are not stiff enough to maintain the proper regulation. If the capacitors are not adequately overrated this

can even damage the capacitors. The addition of a controlled current source can also balance the output, as in Figure 3b. A new topology is needed to form the current source.

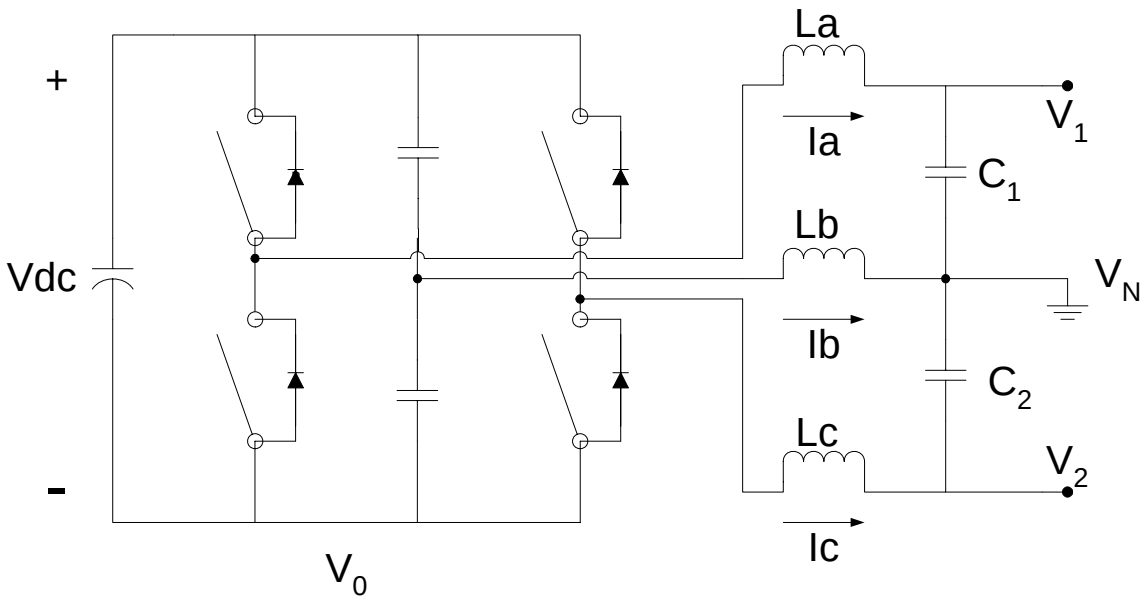


Figure 4. The split capacitor H-bridge. The split capacitors are used to form a loosely regulated center point to balance the output voltages.

1.2. Circuit Topology Overview

This six-switch inverter uses two additional switches and an inductor to form a controllable current source. The inverter is shown in Figure 5 and its parameters are summarized in Table 1. The six-switch inverter is very similar to a six-switch inverter used in three-phase applications except that the center leg is connected to ground instead of a phase of the output with a capacitor. Three-phase four-wire systems also use a similar topology. They also have an extra phase leg for a total of 4 phase legs [28]. The extra phase leg controls neutral current.

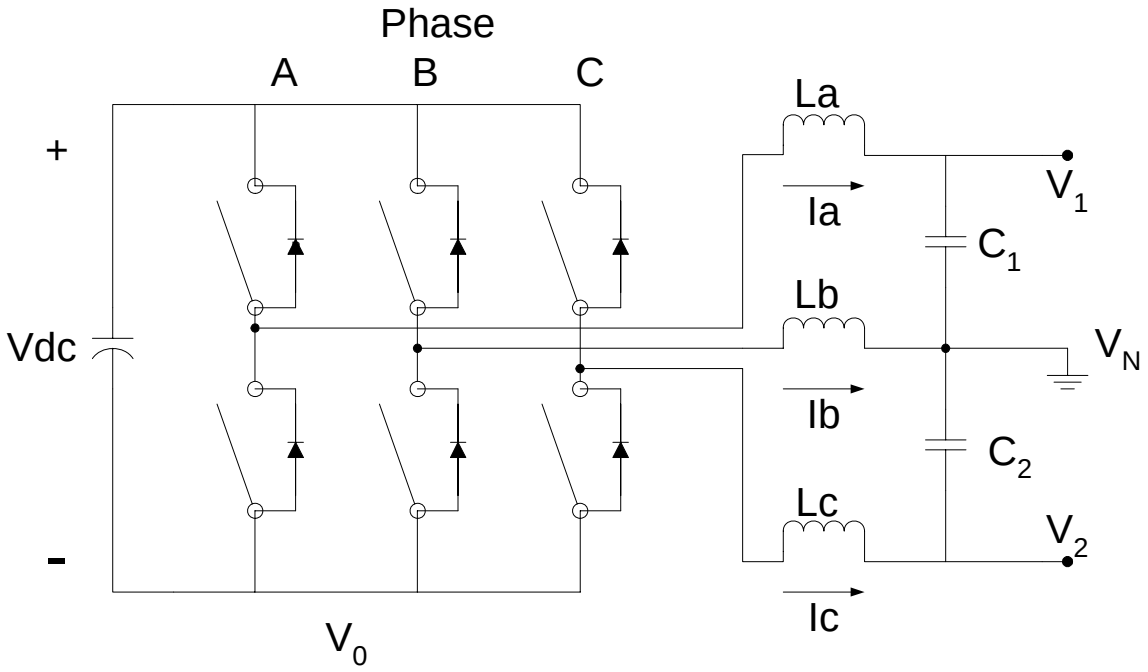


Figure 5. Six-switch three-wire inverter. An additional center leg forms a current source which if controlled correctly can balance the output voltages during an unevenly loaded condition.

Table 1. Important circuit parameters.

Circuit Element	Value
L	310 uH
L_{esr}	20 mΩ
C	60 uF
V_{DC}	400 V
f_s	10 kHz
Max Power	10 kW

An increased number of switches is an obvious disadvantage of this system. However, the extra two switches allow current source injection. This extra controllability is able to balance an uneven load. In general, phase A and C switches control the differential voltage while phase B switches control the balance between the V_1 and V_2, the common voltage. This work will concentrate on the control of these two system variables, the common mode voltage and the differential mode voltage.

1.3. Controller Overview

The intent of the controller is to achieve the highest performance out of the most economical system. Generally speaking the highest performance means low total harmonic distortion (THD) of the sinusoidal output. Output impedance for any type of voltage source is always important. Here low output impedance insures that the output waveform will exhibit low THD and accurate RMS voltage value under a variety of load conditions [22]. Output filter selection is an important part of the system design. A smaller output filter provides lower output impedance, but at the expense of higher harmonics and distortion due to voltage ripple from inadequate attenuation of the switching frequency [9], [17]. In general a voltage source would be better with a larger capacitor at the output, but peak IGBT currents necessitate the need for a reasonably sized output inductor.

The simplest way to control the inverter is as an open-loop system. The PWM modulator is fed a sine wave reference, and encodes the reference into the gate signals. In steady state with a linear load this control technique produces the best possible waveform. For the single-phase thee-wire inverter the phase A and phase C switch pairs receive complementary duty cycles, and the center phase can be modulated at 50 percent duty cycle continually. This type of control is susceptible to two main problems. First, if the output inductor's impedance is significant compared to the load impedance (at the fundamental frequency) there is a significant drop across the inductor. An increasing load creates more drop across the inductor and less output voltage. Second, there is no consideration for a changing DC bus voltage. Most forms of raw power aren't particularly well regulated [27]. Solar, turbine, fuel cell, flywheel, and generator sources exhibit a varying output voltage. A power supply's ability to reject disturbance on its input voltage is known as audiosusceptibility [11]. The disturbance can range from a low frequency sag caused by loading down the DC power source to a relatively high frequency (120 Hz and higher) ripple caused by rectifying an AC source.

A simple solution to the problems listed above is to employ a relatively slow feedback mechanism. The RMS voltage of the output waveform is calculated and then fed back around through an integrator. Low frequency disturbances in the input or output voltage are compensated. This control strategy takes several cycles to handle a disturbance, but maintains a good average value on the output waveform. This type of controller can be easily implemented

with analog components as a standard proportional-integral (PI) controller. Some analog controllers even employ feed-forward compensation to account for a quickly changing DC bus voltage [16]. Analog PI controllers have attempted to follow a sine wave reference, but due to the high gain necessary to maintain tracking usually become unstable at light load [21]. A lightly loaded inverter has no damping and forms a high Q network, which easily resonates.

Dual nested loop systems have proved useful in resonant situations. A current sensor is used to sense the inductor current. A closed-loop current controller can be closed at a higher frequency due to the fact that from duty cycle to inductor current the plant is only a first order system. The inductor current reference is created by the outer voltage loop. Closed loop current control is valuable but often economic concerns prohibit the actual current sensor.

The increased flexibility of a digital controller has many benefits in an inverter system. More complex controllers can be implemented. Pole zero cancellation with pole placement can be used to shape the system for the desired response. Multiple input multiple output (MIMO) controllers and state space systems are easier to implement. Non-linear type controllers are also easier to implement. Multipliers used in control loops are often difficult in an analog system. Optimal controllers such as deadbeat controllers must use a sampled controller. Observer based systems are also usually implemented in combination with a digital controller. Finally, digital controllers have added value in that a microprocessor or DSP can usually also take care of side tasks such as a simple user interface or communication interface.

The most practical controller is often a combination of many factors. In this case the controllers job is not necessarily to follow the reference, but to have good disturbance rejection. A reduced gain at the inverter reference frequency can be compensated with a pre-filter because phase is not a concern in a stand-alone system. The load can be modeled as an output disturbance and the DC bus ripple can be modeled as an input disturbance. Systems with low input sensitivity and low output sensitivity perform well under these disturbances. In a general sense, controllers with high open-loop gain have low sensitivity functions. As previously mentioned high gain controllers are difficult to use in a lightly loaded system. Sampling delay places zeros in the right half plane. As the gain is increased closed-loop poles are pulled to the right half plane where they cause the system to go unstable. Increasing the sampling frequency obviously decreases the sampling delay. However, controller computation speed, switching

frequency, and available analog-to-digital converters (A/Ds) hold the sampling frequency to a realistic value.

Practically, an important part of the controller is how intuitive its use is. The best controller in the world is useless if the user can't see what is happening during its operation. Items such as inaccurate plant parameter estimation, state saturation or integrator wind-up [21], fixed-point overflow, and other non-linear effects complicate the practical operation of a system. Most of these items can be simulated, but no simulation is 100% accurate. Because of this complicated controllers often need adjustment and this can be troublesome. In addition problems such as sampling delay restrict controller performance no matter how innovative the controller.

Chapter 2 will cover the simulation of the theoretical analysis or mathematical model formulation. From there, Chapter 3 will go into the HIL system used and its construction. Next, Chapter 4 covers the simulation and experimentation with the hardware. Finally, Chapter 5 summarizes the contribution and suggests future work.

Chapter 2 - Theoretical Analysis

2.1. System Formulation

The six-switch single-phase three-wire inverter is a variant of the more commonly known voltage source inverter (VSI). As in many power electronics systems establishing an operating point to linearize around is difficult when system parameters are constantly changing. In this case the load and input voltage are non-constant. Thus the best alternative is to use an average model and switch the converter at a much higher frequency than any of the other system dynamics [22]. As stated above in Table 1 the switch frequency for the inverter is 10 kHz. This switching frequency is over an order of magnitude higher than the inverter's fundamental frequency. The average model is derived below using standard nodal and loop analysis and techniques similar to those seen in [7]. Figure 6 shows the same system as in Figure 5 with the switches replaced with the average model.

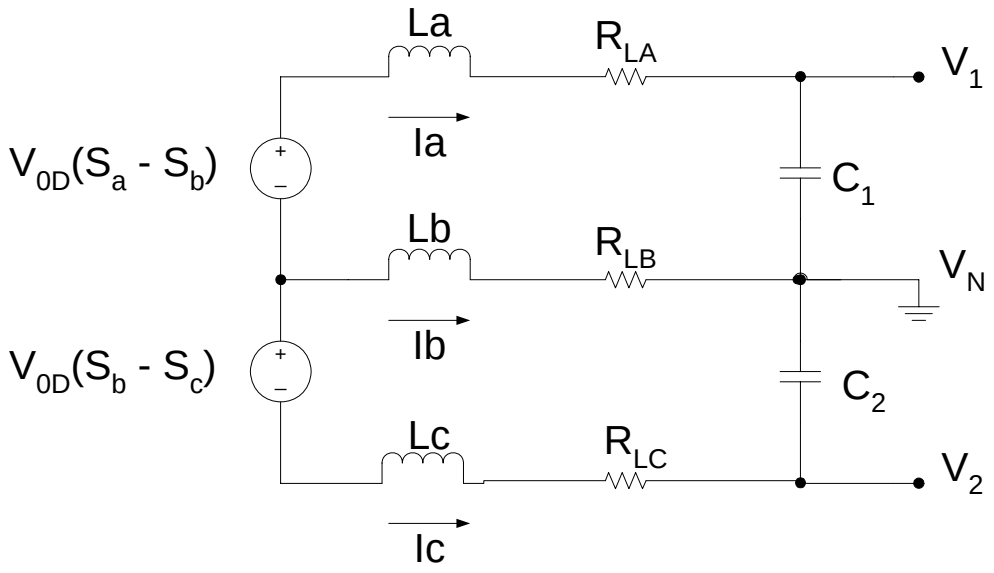


Figure 6. Inverter average model. The pulse width modulated (PWM) switches are replaced with voltage sources representing their average value.

KVL:

$$V_{OD}(S_a - S_b) - L_a \frac{dI_a}{dt} - V_{RLa} + V_{RLc} - V_{1N} + V_{2N} + L_c \frac{dI_c}{dt} = 0 \qquad (1)$$

$$V_{OD}(S_b - S_c) - L_b \frac{dI_b}{dt} + V_{2N} - V_{RLb} + V_{RLc} + L_c \frac{dI_c}{dt} = 0 \quad (2)$$

KCL:

$$I_a - C_1 \frac{dV_{1N}}{dt} - \frac{V_{1N}}{R_1} = 0 \quad (3)$$

$$I_c - C_2 \frac{dV_{2N}}{dt} - \frac{V_{2N}}{R_2} = 0 \quad (4)$$

$$I_a + I_b + I_c = 0 \quad (5)$$

Taking the derivative of (5) gives:

$$\frac{d(I_a + I_b + I_c)}{dt} = 0 = \frac{dI_a}{dt} + \frac{dI_b}{dt} + \frac{dI_c}{dt} \quad (6)$$

Next substituting (6) into (1) and (2) gives:

$$V_{OD}(S_a - S_b) - V_{1N} + V_{2N} - V_{RLa} + V_{RLc} - L_a \frac{dI_a}{dt} - L_c \frac{dI_a}{dt} - L_a \frac{dI_b}{dt} = 0 \quad (7)$$

$$V_{OD}(S_b - S_c) + V_{2N} - V_{RLb} + V_{RLc} - L_b \frac{dI_b}{dt} - L_c \frac{dI_a}{dt} - L_c \frac{dI_b}{dt} = 0 \quad (8)$$

To find the state space equations for the system we need to define the derivative of states in terms of the states. But first we need to define the states in our system. Our system has 5 energy storage elements so it has a possibility of 5 states. However, in the six-switch inverter the currents must sum to zero (5). This fact means that the currents are not linear independent. Any two of the currents can be linear independent but not all three. Therefore our system will have 4 states: V_{1N}, V_{2N}, I_a, I_b. Equations (7) and (8) contain the derivative I_a and I_b terms but they must be solved before they are useful. Krammer's rule is used to solve for I_a and I_b derivative terms. First, the equations are put in the following form, $ax_1+bx_2 = c$. Where, $x_1 = dI_a/dt$, $x_2 = dI_b/dt$.

$$(L_a + L_c)\frac{dI_a}{dt} + L_c \frac{dI_b}{dt} = V_{OD}(S_a - S_c) - V_{1N} + V_{2N} - V_{RLa} + V_{RLc} \quad (9)$$

$$L_c \frac{dI_a}{dt} + (L_c + L_b)\frac{dI_b}{dt} = V_{OD}(S_b - S_c) + V_{2N} - V_{RLb} + V_{RLc} \tag{10}$$

Finally, the equations are solved and we have:

$$\frac{dI_a}{dt} = \frac{(-L_b - L_c)V_{1N} + (L_b)V_{2N} + (L_bV_{OD} + L_cV_{OD})S_a - (L_cV_{OD})S_b - (L_bV_{DO})S_c + (L_b + L_c)V_{RLa} - (L_c)V_{RLb} - (L_b)V_{RLc}}{L_aL_b + L_aL_c + L_bL_c} \tag{11}$$

$$\frac{dI_b}{dt} = \frac{(L_c)V_{1N} + (L_a)V_{2N} - (L_cV_{OD})S_a + (L_aV_{OD} + L_cV_{OD})S_b - (L_aV_{DO})S_c - (L_c)V_{RLa} + (L_a + L_c)V_{RLb} - (L_a)V_{RLc}}{L_aL_b + L_aL_c + L_bL_c} \tag{12}$$

Equations (3), (4), (11), and (12) are used to form the state space equations. The standard $\dot{x} = Ax + Bu$ form is used. All inductor equivalent series resistor voltage drops are also replaced with the appropriate IR. Also, for simplicity L_t is defined as follows.

$$L_t = L_aL_b + L_aL_c + L_bL_c \tag{13}$$

$$\dot{x} = A \qquad x + B \qquad u$$

$$\begin{bmatrix} \dot{V}_{1N} \\ \dot{V}_{2N} \\ \dot{I}_a \\ \dot{I}_b \end{bmatrix} = \begin{bmatrix} \frac{-1}{R_1C_1} & 0 & \frac{1}{C_1} & 0 \\ 0 & \frac{-1}{R_2C_2} & \frac{-1}{C_2} & \frac{-1}{C_2} \\ \frac{-L_b - L_c}{L_t} & \frac{L_b}{L_t} & \frac{-R_{La}(L_b + L_c) - L_bR_{Lc}}{L_t} & \frac{L_cR_{Lb} - L_bR_{Lc}}{L_t} \\ \frac{L_c}{L_t} & \frac{L_a}{L_t} & \frac{L_cR_{La} - L_aR_{Lc}}{L_t} & \frac{-R_{Lb}(L_a + L_c) - L_aR_{Lc}}{L_t} \end{bmatrix} \begin{bmatrix} V_{1N} \\ V_{2N} \\ I_a \\ I_b \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ \frac{V_{0D}(L_b+L_c)}{L_t} & \frac{-L_cV_{0D}}{L_t} & \frac{-L_bV_{0D}}{L_t} \\ \frac{-L_cV_{0D}}{L_t} & \frac{V_{0D}(L_a+L_c)}{L_t} & \frac{-L_aV_{0D}}{L_t} \end{bmatrix} \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \tag{14}$$

In this system we our concerned about regulating the inverter output voltage so our outputs are defined as V_{1N} and V_{2N}, see (15). Alternatively, the system can also be defined as the difference in the voltage outputs and the addition of the outputs as in (16).

$$y = C \qquad x$$

$$\begin{bmatrix} V_{1N} \\ V_{2N} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{1N} \\ V_{2N} \\ I_a \\ I_b \end{bmatrix} \tag{15}$$

$$\begin{bmatrix} V_{diff} \\ V_{com} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 & 0 \\ 1 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{diff} \\ V_{com} \\ I_a \\ I_b \end{bmatrix} \tag{16}$$

2.2. System Analysis

The bode plots for three loading cases are shown in the following plots. One should note that the gain from S_a to V_{1N} is high while S_c to V_{1N} low. S_b affects both V_{1N} and V_{2N}. This type of symmetrical pattern is followed throughout the system. As would be expected the full load system (blue) is heavily damped while the no load is very under damped (red). Also, the gain on all the current plots is heavily dependent on load. MATLAB m-files for the system listed in (14) and (15) are shown in Appendix A.

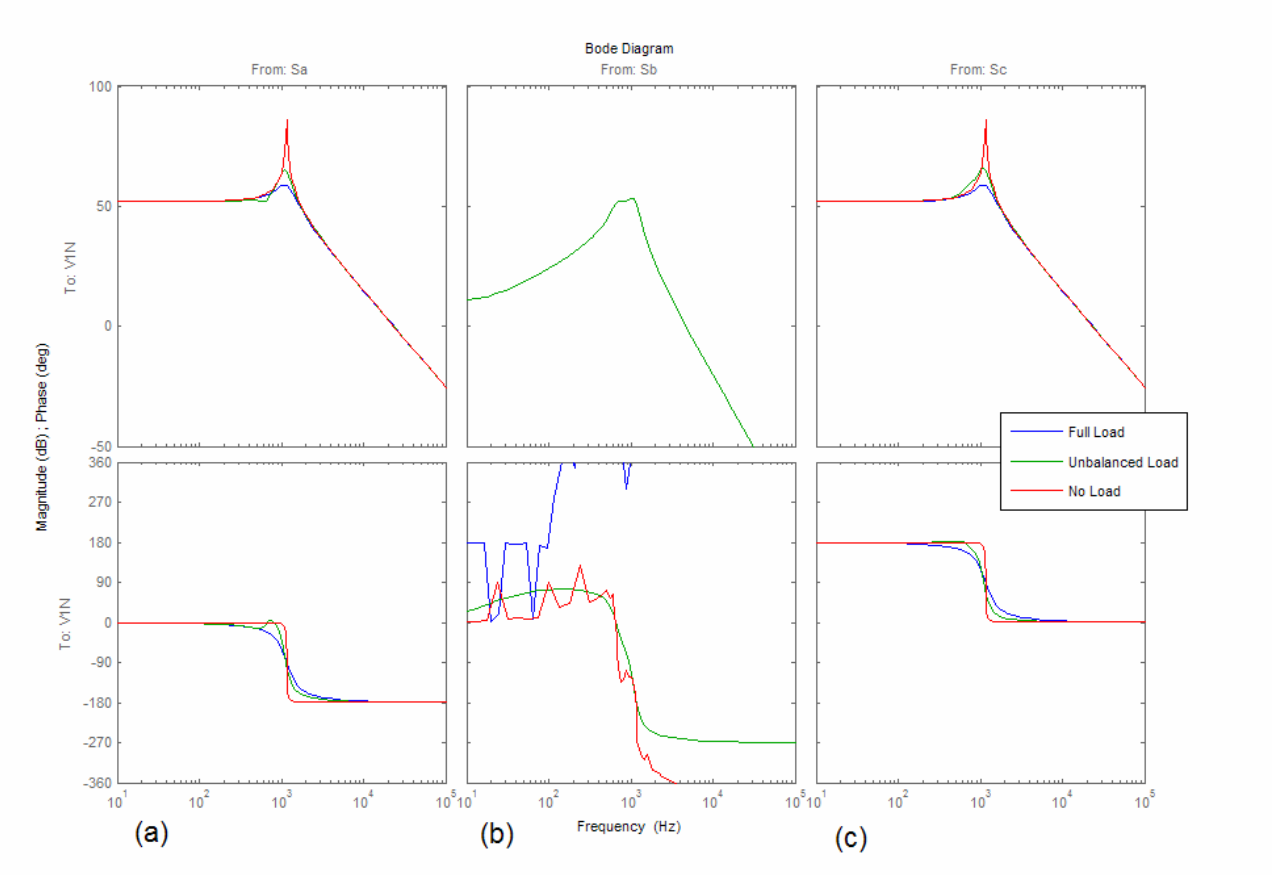


Figure 7. Input to V_{1N} bode plots. Column (a) shows the magnitude and phase from the Sa input to the V1 output. Column (b) is Sb to V1 and column (c) is Sc to V1. The unbalanced load case has full load on V1N and no load on

V2N. Column (b) has very low magnitude (≈ -250 dB) for the full load and no load case. This causes numerical errors in the corresponding phase plot.

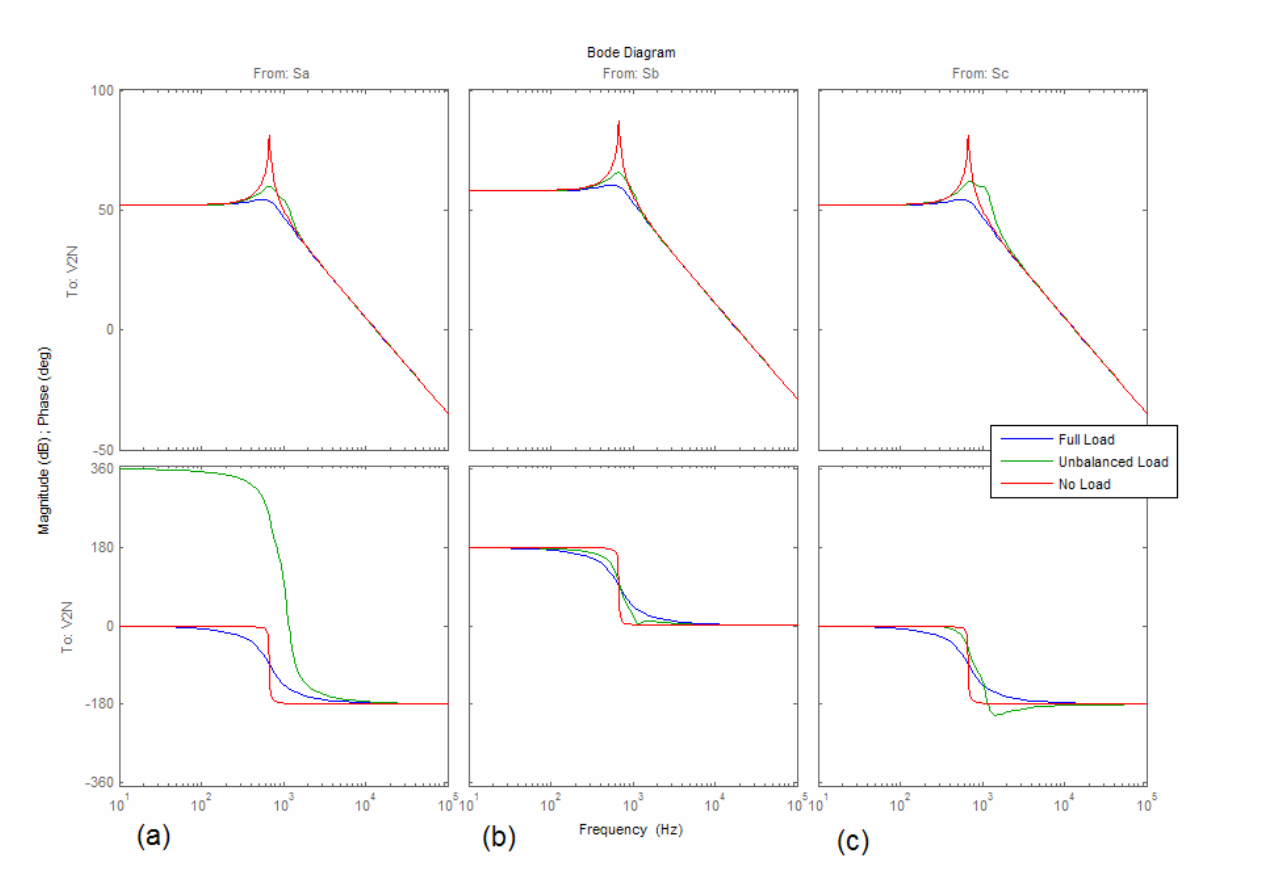


Figure 8. Input to V_{2N} bode plots. Column (a) shows the magnitude and phase from the Sa input to the V2 output. Column (b) is Sb to V2 and column (c) is Sc to V2.

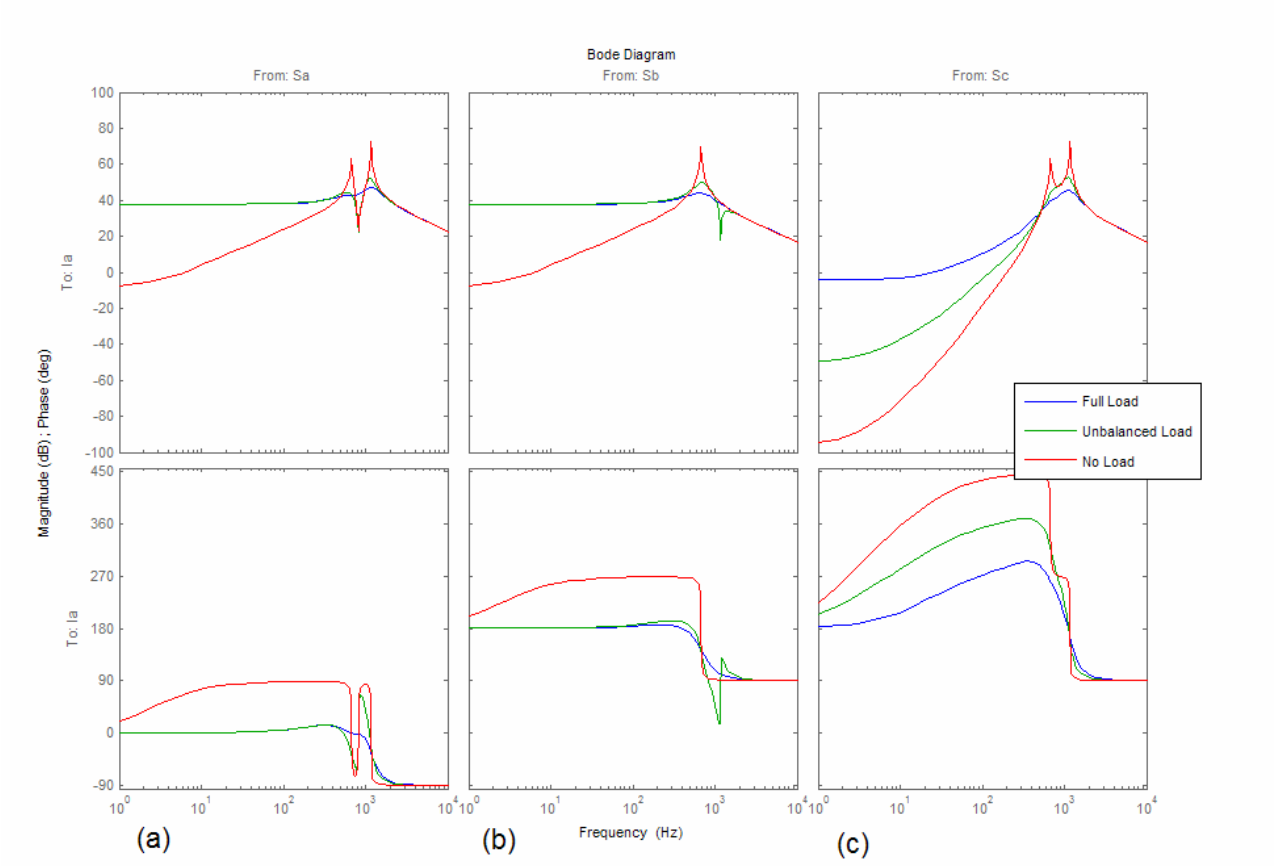


Figure 9. Input to I_a bode plots. Column (a) shows the magnitude and phase from the Sa input to the Ia output. Column (b) is Sb to Ia and column (c) is Sc to Ia.

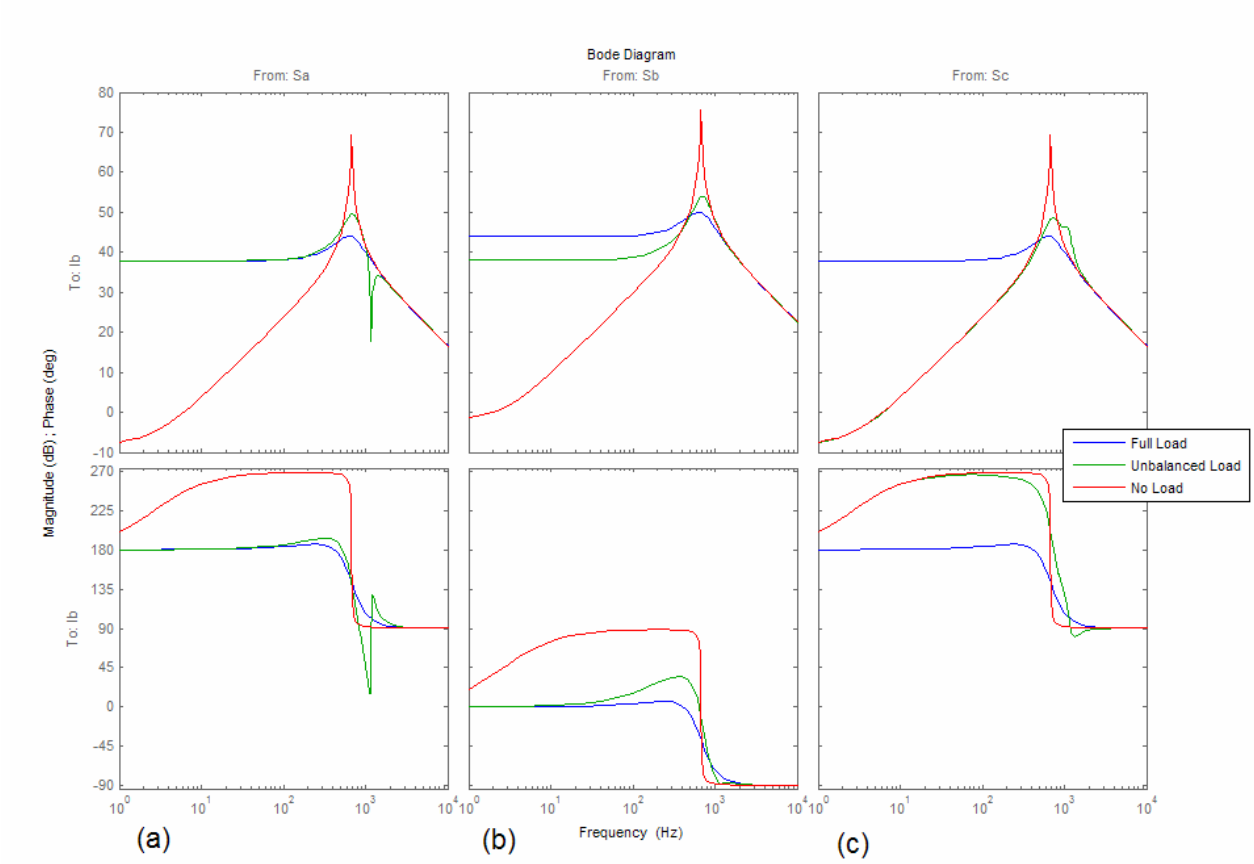


Figure 10. Inputs to I_b bode plots. Column (a) shows the magnitude and phase from the Sa input to the Ib output. Column (b) is Sb to Ib and column (c) is Sc to Ib.

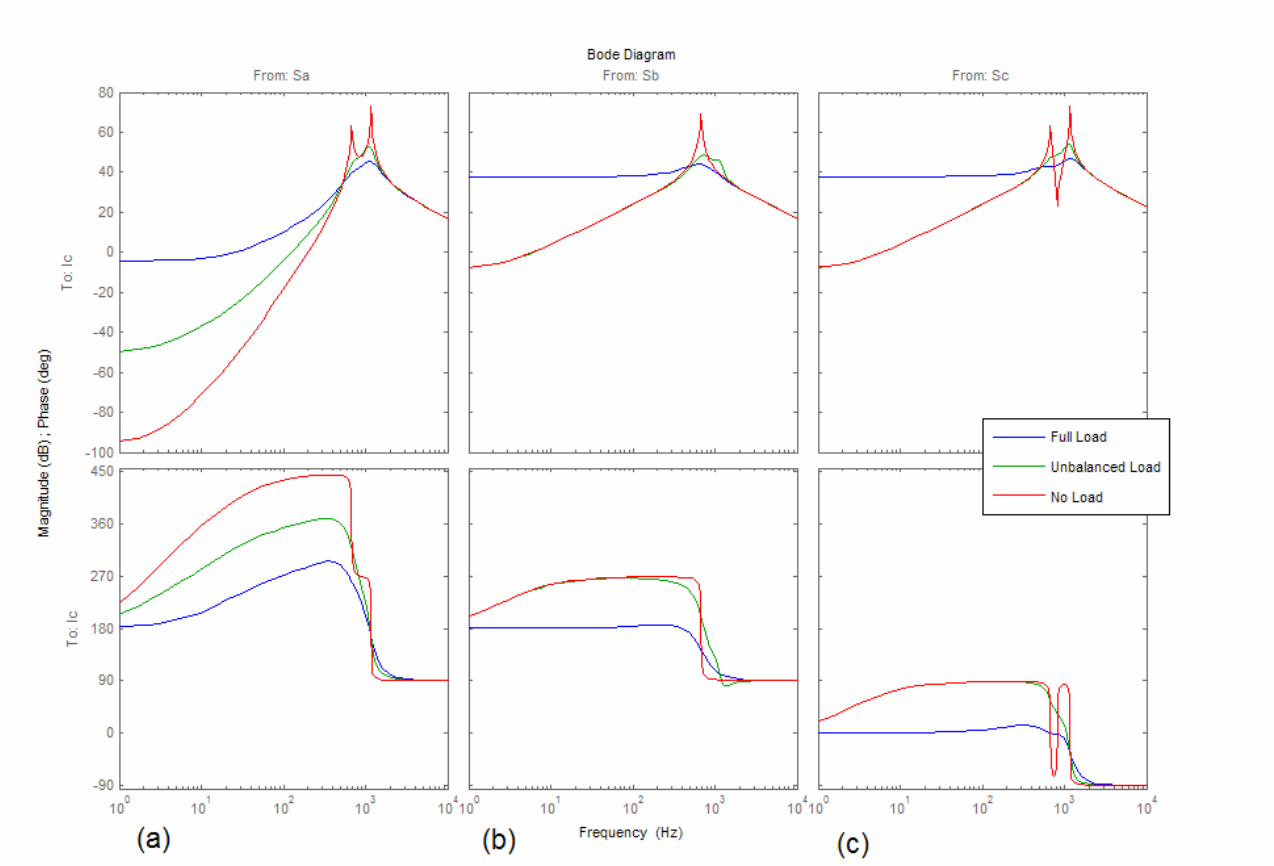


Figure 11. Inputs to I_c bode plots. Column (a) shows the magnitude and phase from the Sa input to the Ic output. Column (b) is Sb to Ic and column (c) is Sc to Ic.

Figure 12, below, shows how the duty cycle to output voltage gain changes as a function of DC bus voltage. In-fact it appears to be an entirely linear gain. This can be compensated for by inverting the DC bus voltage and applying it as a gain.

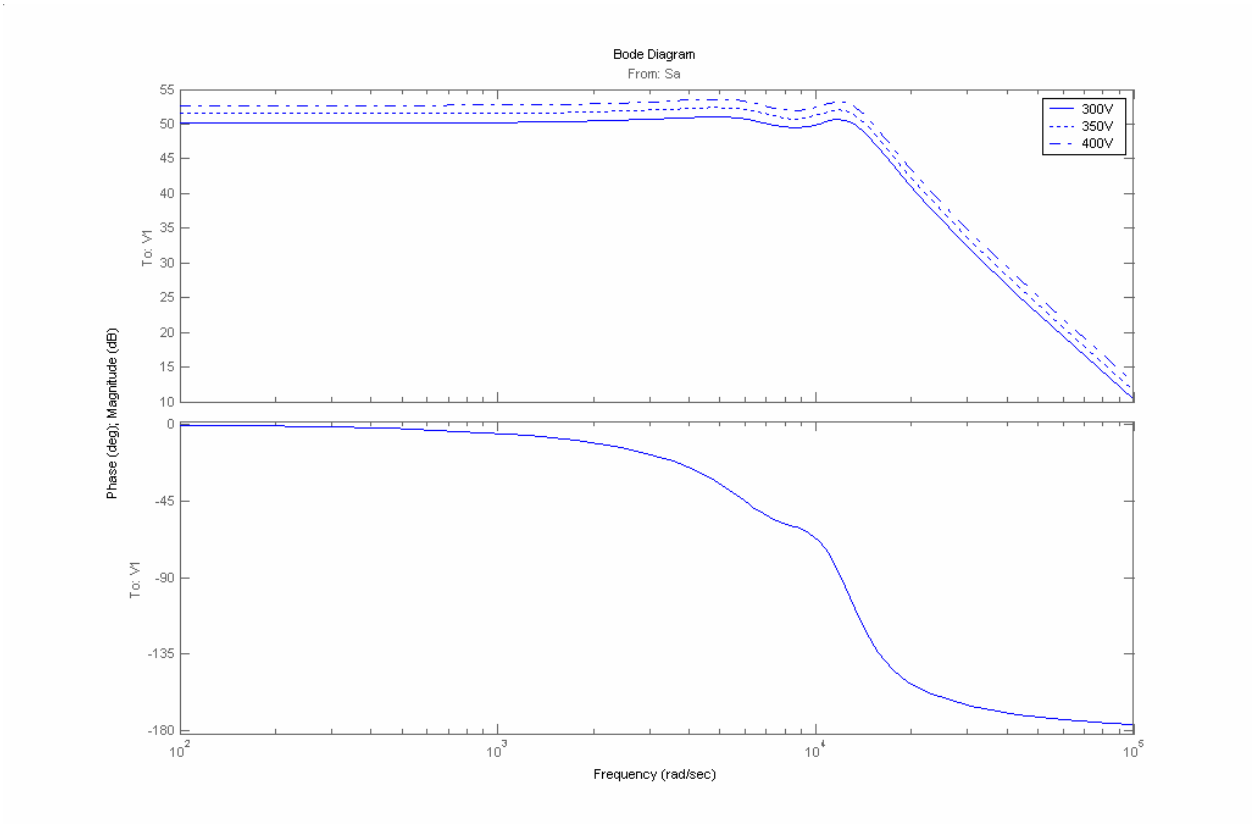


Figure 12. Inverter system with changing V_{0D} bus voltage. The bus voltage changes the open loop gain of the system.

Now that we have a state space system describing the inverter we can check for observability and controllability. Equation (17) is used to test for controllability. Since the rank is 4 it means that all 4 states are controllable. Equation (18) tests for observability. Again, since the rank is 4 it means that all 4 states are observable.

$$\text{Controllability:} \qquad \text{Rank}\left(\begin{bmatrix} B & AB & A^2B & A^3B \end{bmatrix}\right) = 4 \tag{17}$$

$$\text{Observability:} \qquad \text{Rank}\left(\begin{bmatrix} C \\ CA \\ CA^2 \\ CA^3 \end{bmatrix}\right) = 4 \tag{18}$$

However, an item of immediate concern is the A matrix. In (14) it can be seen that the upper left corner of the A matrix contains R_1 and R_2. Any change in load will cause a system change and render our controllability and observability tests moot.

A standard observer will only be as good as its estimation of the system. Our system is not only time variant, but also unpredictable due to random load changes. This type of problem calls

for a special observer. Since output voltage is directly measurable the current states are the ones that we need to observe. The inductor current can be calculated by integrating the voltage across the inductor. Integrating (11) leads us to:

$$I_a = \int \frac{(-L_b - L_c)V_{1N} + (L_b)V_{2N} + (L_bV_{OD} + L_cV_{OD})S_a - (L_cV_{OD})S_b - (L_bV_{DO})S_c + (L_b + L_c)V_{RLa} - (L_c)V_{RLb} - (L_b)V_{RLc}}{L_aL_b + L_aL_c + L_bL_c} dt + c \quad (19)$$

Several terms in the above equation present a problem. First, the resistive drop across the inductor is based off of the observed current itself. Second, the constant term after the integral could be unknown in certain situations. This observer is particularly hard to implement in reality because the resistive drop across the inductors can change with temperature, the voltage drop across the semiconductors is also not constant, and zero order hold produces an almost constant error. These small sources of error are integrated over time and accumulate to a significant low frequency error.

2.3. Decoupling

Careful study of the B matrix shows that there exists quite a bit of cross-coupling in the duty cycle inputs. No duty cycle affects one inductor current and no inductor current is affected by only one input. A decoupling matrix can be applied to the inputs so that one input affects only one current and vice versa. The desired B matrix is first formulated, which will be denoted B_T. The standard input to a state space system is denoted as some gain matrix B multiplied by an input vector u.

$$\dot{x} = Ax + Bu \quad (20)$$

The input u must be multiplied by a transformation matrix T before it is passed to the plant as a modified input u'. Therefore,

$$\dot{x} = Ax + BTu \text{ and } B_T = BT \quad (21)$$

B_T and B are known but B must be an invertible matrix. Since in our system B is not invertible the B_T equation is an under constrained system. The equation is shown below in (22). In the B matrix all three inductances have been set equal. Also, the input to voltage section has been deleted since there are no terms present.

$$B_T = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} \frac{2}{3}\frac{V_{0D}}{L} & \frac{-1}{3}\frac{V_{0D}}{L} & \frac{-1}{3}\frac{V_{0D}}{L} \\ \frac{-1}{3}\frac{V_{0D}}{L} & \frac{2}{3}\frac{V_{0D}}{L} & \frac{-1}{3}\frac{V_{0D}}{L} \end{bmatrix} * T \tag{22}$$

The B and B_D matrices are augmented with random values so that the system is fully constrained. T is solved for using the equation (23) below.

$$T = B^{-1}B_T = \begin{bmatrix} \frac{2}{3}\frac{V_{0D}}{L} & \frac{-1}{3}\frac{V_{0D}}{L} & \frac{-1}{3}\frac{V_{0D}}{L} \\ \frac{-1}{3}\frac{V_{0D}}{L} & \frac{2}{3}\frac{V_{0D}}{L} & \frac{-1}{3}\frac{V_{0D}}{L} \\ 1 & 1 & 1 \\ \\ \end{bmatrix}^{-1} * \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 0 & 0 \end{bmatrix} = \frac{V_{0D}}{L}\begin{bmatrix} 1 & 0 \\ 0 & 1 \\ -1 & -1 \end{bmatrix} \tag{23}$$

Finally, because u must be between 0 and 1 a 0.5 offset is added to u before it is input into the plant. This does not affect the plant because it is a constant offset.

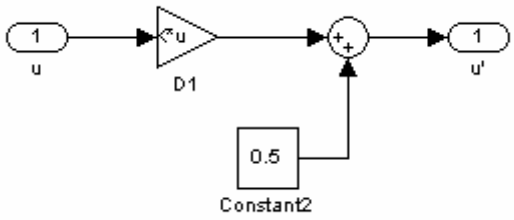


Figure 13. Decoupling Matrix. The decoupling matrix block implements the following equation u'=Du+0.5

Chapter 3 - Hardware Setup: Rapid Prototype System

Control design for high power converters is a difficult process. High power, high voltage, and high current can quickly become dangerous if uncontrolled, and insuring system safety and integrity can be challenging—especially while exploring new topologies and control strategies. These challenges often impede the combination of rapid prototyping and high power systems.

This system uses a FPGA to manage a hardware in the loop (HIL) system, connecting a standard x86 based processor to a high power converter. This combination provides high flexibility and a large amount of processing power. In addition, the use of MATLAB's xPC Target system as the controller's operating system and software makes the user interface straightforward.

xPC Target offers its users the ability to change controller parameters on-the-fly. It gives the designer complete visibility of the system, including any inputs, outputs, or states, and provides an easy-to-use interface from which the designer can make any type of change simply and easily. Using xPC Target to close the loop in a switching power converter gives you an excellent debug and development tool.

3.1. Overview

The traditional MATLAB xPC Target system is divided into two parts: a host and a target computer [19]. The target computer is the system controller. It is placed in the loop where it receives data from the system sensors, and reacts to them in real time. The host is the user interface to the target, where the controller is designed, simulated, and adjusted on the fly. During the setup phase, the host sends a compiled binary of the system diagram to the target. When instructed to begin, the target receives system inputs, calculates control variables, sends output signals, and updates the control parameters. The target can also generate a display of any system variable, displaying them locally or sending them back to the host.

To take full advantage of the capabilities that xPC target provides, we must carefully weigh its strengths and weaknesses. While the target can compute complex control variables, matrix multiplications, and state machines, it lacks the ability to create fundamental high-speed building blocks like counters, comparators, and shift registers required for PWM signals and digital signal interfaces. Additionally, considerable care must be taken in actuating and acquiring signals from the high power system. The data acquisition system is designed for high power isolation, scalability, and flexibility.

The system is broken up into three major pieces, which are outlined in the following sections and also organized in Figure 14 and physically shown in Figure 15.

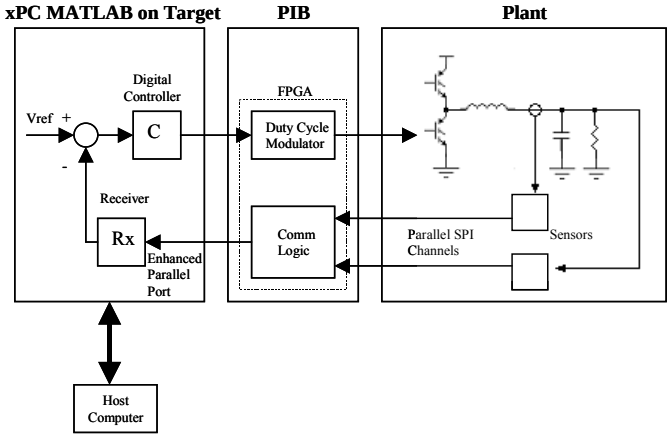


Figure 14. The HIL system diagram. The controller uses the PIB to interact with the power system's power devices and high power sensors. Complex control algorithms can be altered in real time on the controller while the PIB takes care of high-speed tasks such as PWM patterns.

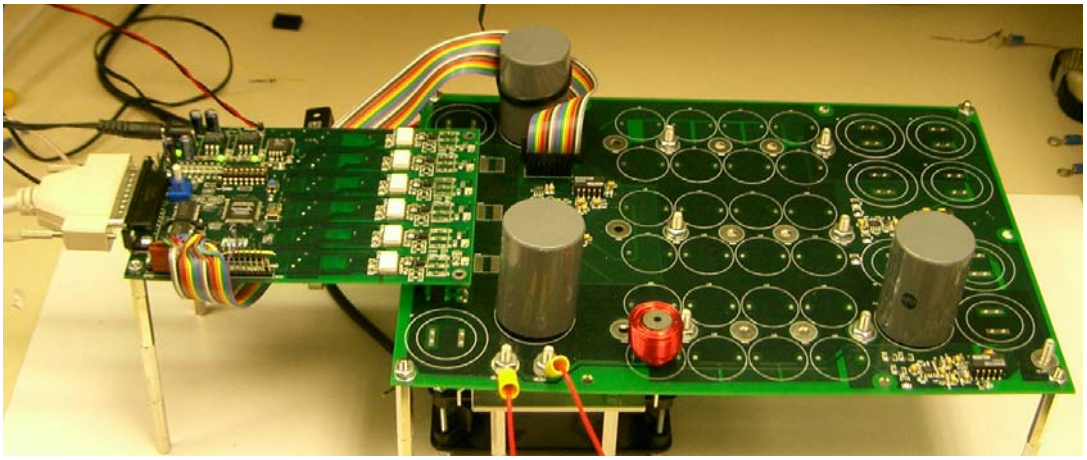


Figure 15. The assembled HIL system. The system is designed for maximum flexibility. Various output filters and sensor configurations can be used.

3.2. Power Interface Board (PIB)

As previously mentioned the PIB's primary tasks are isolation and high-speed signal interface. In particular almost all power electronic system will need PWM generators, isolated gate drives, IGBT fault protection, high voltage sensors, and high current sensors. All of these

except the actual sensors are included on the PIB. A block diagram level schematic is shown in Figure 17, and a picture of the actual PCB is shown in Figure 16.

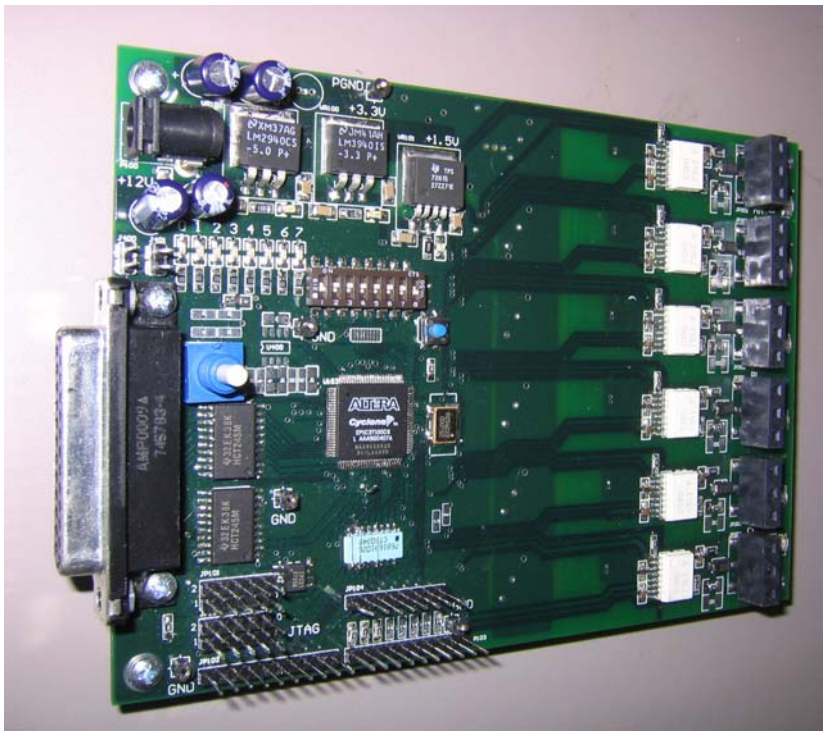


Figure 16. A picture of the actual PIB. The digital interface electronics are on the left while the high voltage gate drives are on the right.

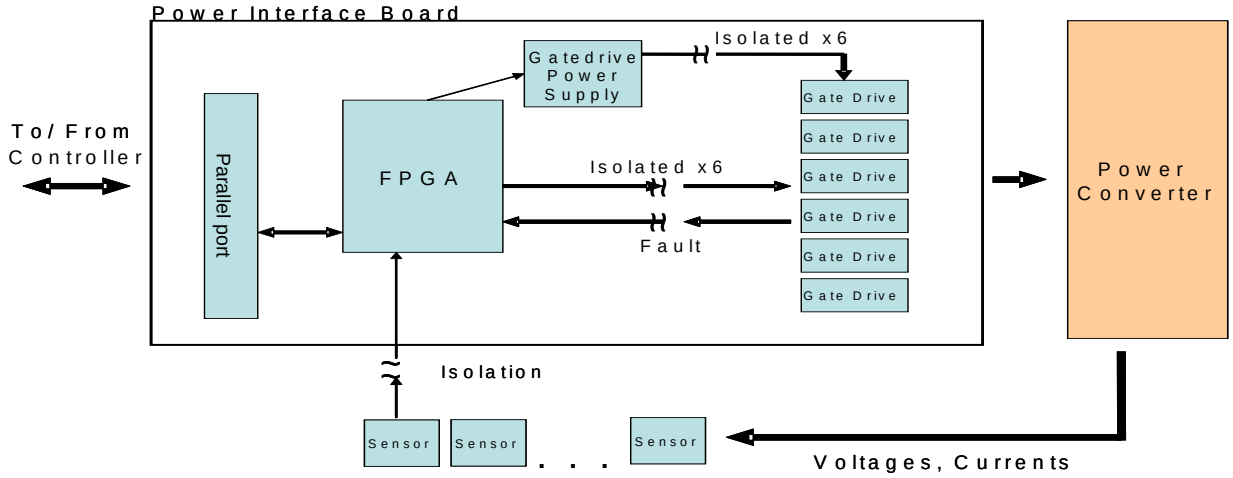


Figure 17. PIB system diagram. The power interface board is the backbone of the digital control system.

The sensors are attached to the power converter, where the signals are conditioned, digitized, and isolated. The signals are serially shifted into the FPGA through an SPI-like interface. This type of interface allows the signals to be digitized before they can become susceptible to noise. Additionally, the digital signals noise immunity can be further improved using differential pairs or an optical interface.

The PIB also includes six isolated and shoot-through protected gate drives sized for a converter in the 10-20 kW range.

At the heart of the PIB sits a 50 MHz, 3,000 block Field Programmable Gate Array (FPGA). The FPGA's speed, flexibility, and parallel processing capabilities offer many advantages in this system. Any imaginable type of PWM patterns can be configured. Also, any digital sensor signal can be acquired and sent to the target PC. The PIB to controller communication uses an enhanced parallel port interface, which is available on most personal computers.

The FPGA code is written in Verilog [4]. Verilog is similar to C but is structured towards the parallel nature of FPGAs. Two blocks of code can be processed simultaneously and their results fed into another block. The code is compiled and simulated in Altera's design software, Quartus II. Quartus is available free of charge from Altera's website [2], but is still quite powerful. The high-level system design is organized in a schematic type diagram. Blocks in the schematic represent pieces of handwritten code. Schematic entry is advantageous because one can easily look at the schematic diagram and see how individual pieces of code relate to each other and get a better overall understanding of the system. A system block diagram is shown in the Figure 18, below.

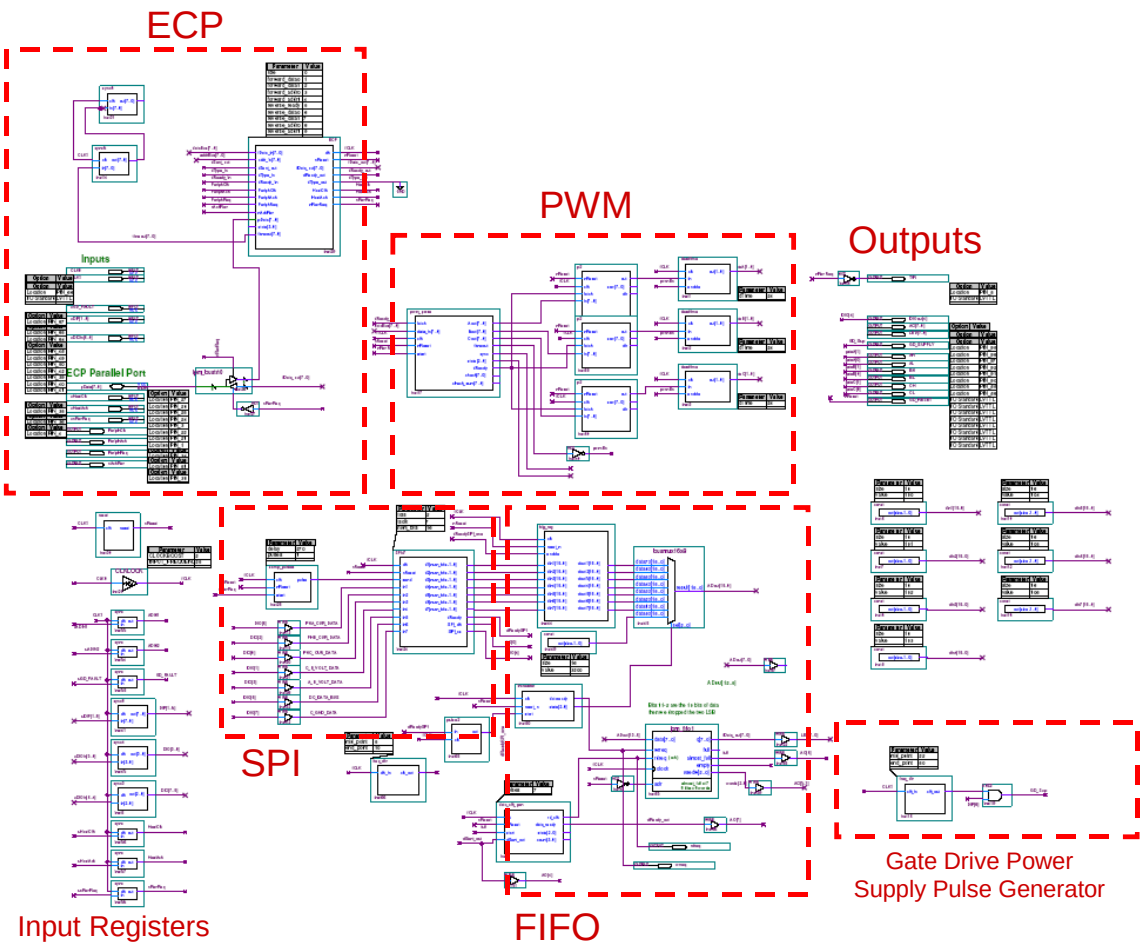


Figure 18. Internal FPGA schematic. The FPGA system consists of a series of connected Verilog blocks. The individual sections will be covered below.

The parallel port interface has 8 bi-directional data bits and 9 control bits [3]. The Enhanced Capabilities Port (ECP) specification had 4 states: data forward, data reverse, address forward, and address reverse. The xPC target driver only makes use of the data states. Each state also has sub states that take care of the handshaking between the FPGA and PC. An actual capture of the data cycle is shown in Figure 20 and the detailed view of the ECP block is shown in Figure 19.

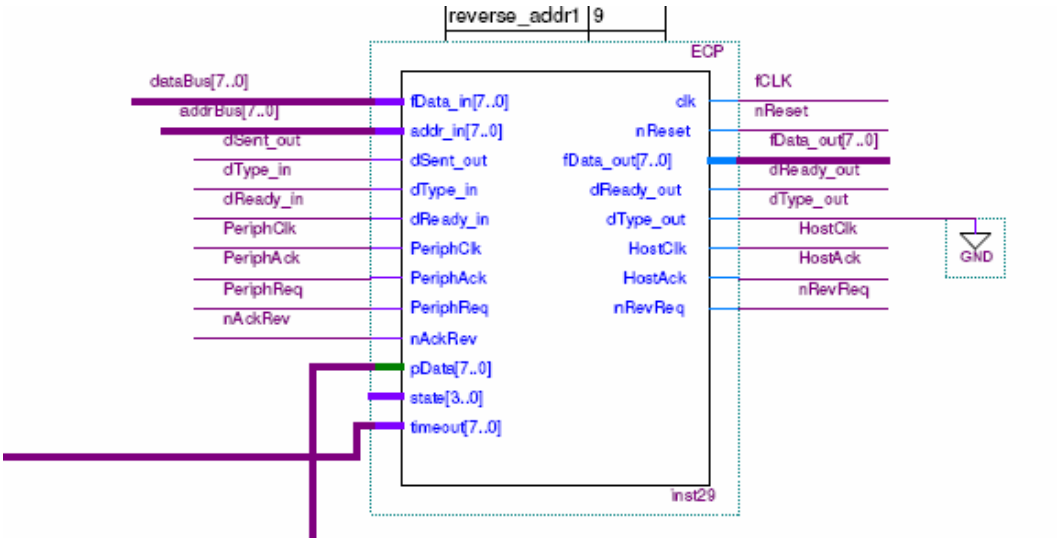


Figure 19. The ECP section. The ECP block and its associated signal connections can exchange data at 2 MB/s..

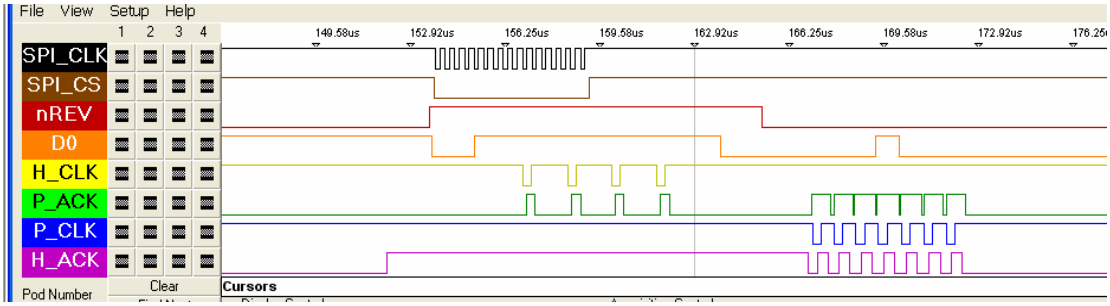


Figure 20. A typical data transfer cycle. Data (D0) is placed on the data bus, the H_ACK line is raised to signal a data transfer, H_CLK is lowered to show data is ready, the peripheral acknowledges the valid data by raising P_ACK, H_CLK is raised and the data is latched in, and finally the peripheral lowers P_ACK to signal the end of the transfer.

The data bus's direction is controlled by the nRevReq signal. This signal is asserted low by the host to tell the peripheral it is allowed to send data. When the host brings the line low the FPGA sends any available data it has queued up. From a system perspective this is when the previous cycle's samples are stored and sent into the PCs FIFO buffer. When the host's sampling interrupt trips and the window for receiving data is over then it asserts the nRevReq line high and the FPGA knows that it is not allowed to place data, but rather should be ready to receive data.

The PWM signals are sent from the PC to the FPGA during the next part of the communication sequence. Each duty cycle is transmitted as a single byte followed by one

checksum byte for the previous three bytes. The PWM parse block receives these chunks of data from the ECP block, saves each of the three to a register, tests the checksum, and passes any valid data to the PWM blocks. Additional, timeout logic makes sure that the duty cycle is updating continually. If the block receives a bad checksum then the previous cycle's duty cycles are used. If no new duty cycles are received within 0.4 ms then the duty cycles are set to zero. This prevents any loss of communication from causing a problem in the power stage. These blocks are shown below in Figure 21.

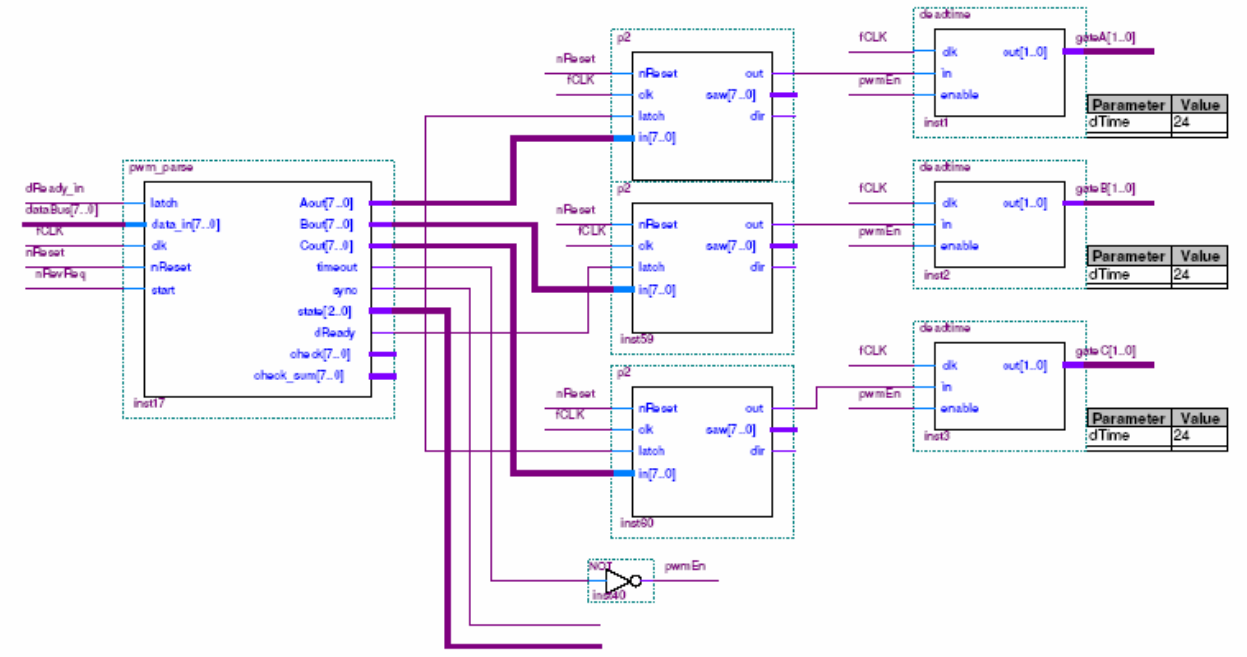


Figure 21. The PWM section. The PWM signals received and are generated with deadtime using these series of blocks.

The 8-bit duty cycle values are sent to their respective PWM modulator blocks. For a classic six-switch bridge three PWM blocks are used. All three blocks use the same code, but constitute three separate modulators within the FPGA. The PWM block switching frequency can be changed through compile time parameters. A center aligned PWM was eventually used because it eliminated simultaneous switching edges and reduced EMI on other circuitry. Other modulation schemes such as interleaved PWM could be implemented and could easily replace the center aligned PWM block used here.

Next the PWM signal was sent to a deadtime generator block. The deadtime used was a compile time parameter and could easily be changed if necessary. The block outputs two

complimentary gate signals with deadtime. The deadtime block also contains an enable input for any case where the gate signals needed to be shutdown.

The data acquisition half of the FPGA provides up to seven serial peripheral interface (SPI) channels. The power stage sensors utilize digitally isolated serial analog to digital converters (A/D). On a rising nRevReq edge the samp_pulses block generates a query signal for the sensors. The SPIx7 block generates one set of clock, and chip select lines for all seven sensors. Additionally it simultaneously shifts seven lines of data into the FPGA from the sensors.

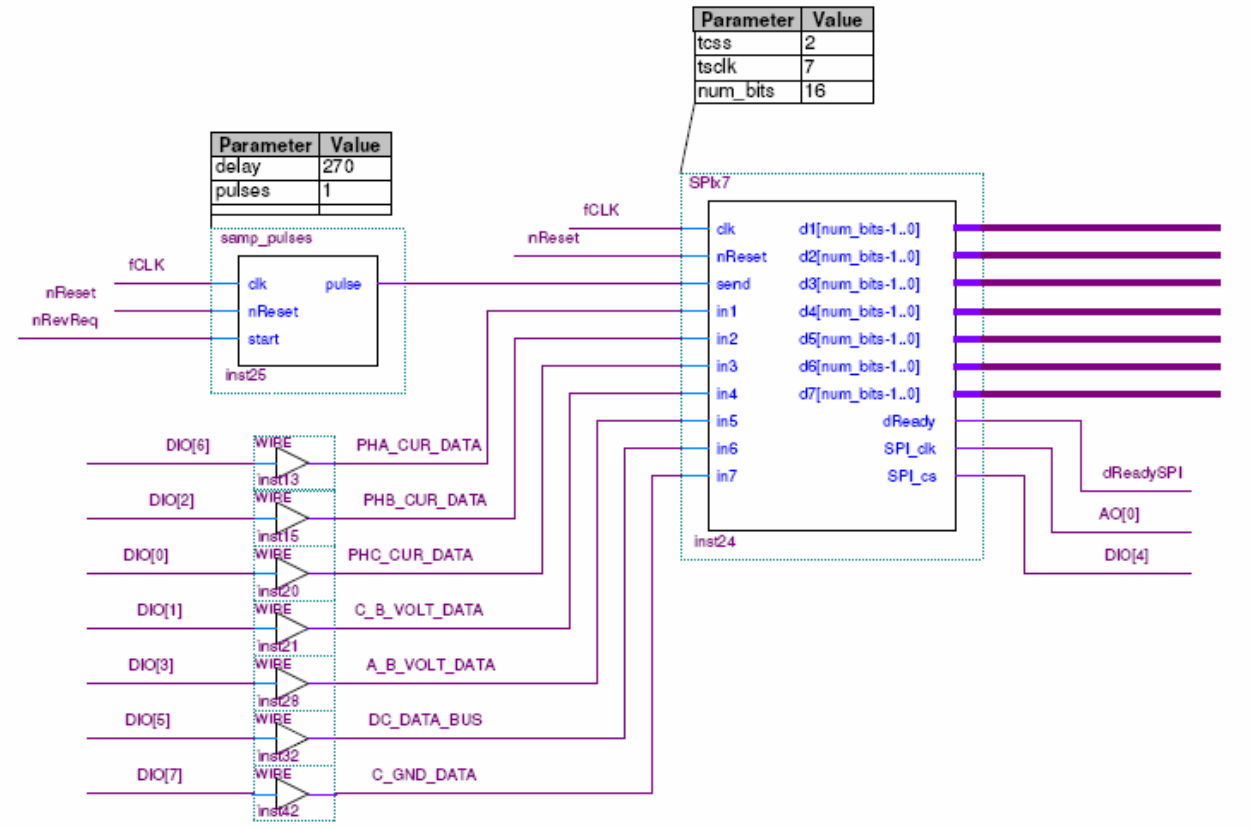


Figure 22. The SPI section. The SPI portion of the FPGA reads in the sensors and passes the info on to the FIFO.

The big_reg block is a large parallel latch the grabs the output from the SPI block and holds it until the next sample cycle is available. The seven values are then muxed into a FIFO block so that they can be passed to the parallel port block one at a time when it is ready to send data to the PC. Figure 23 shows the detail view of these blocks.

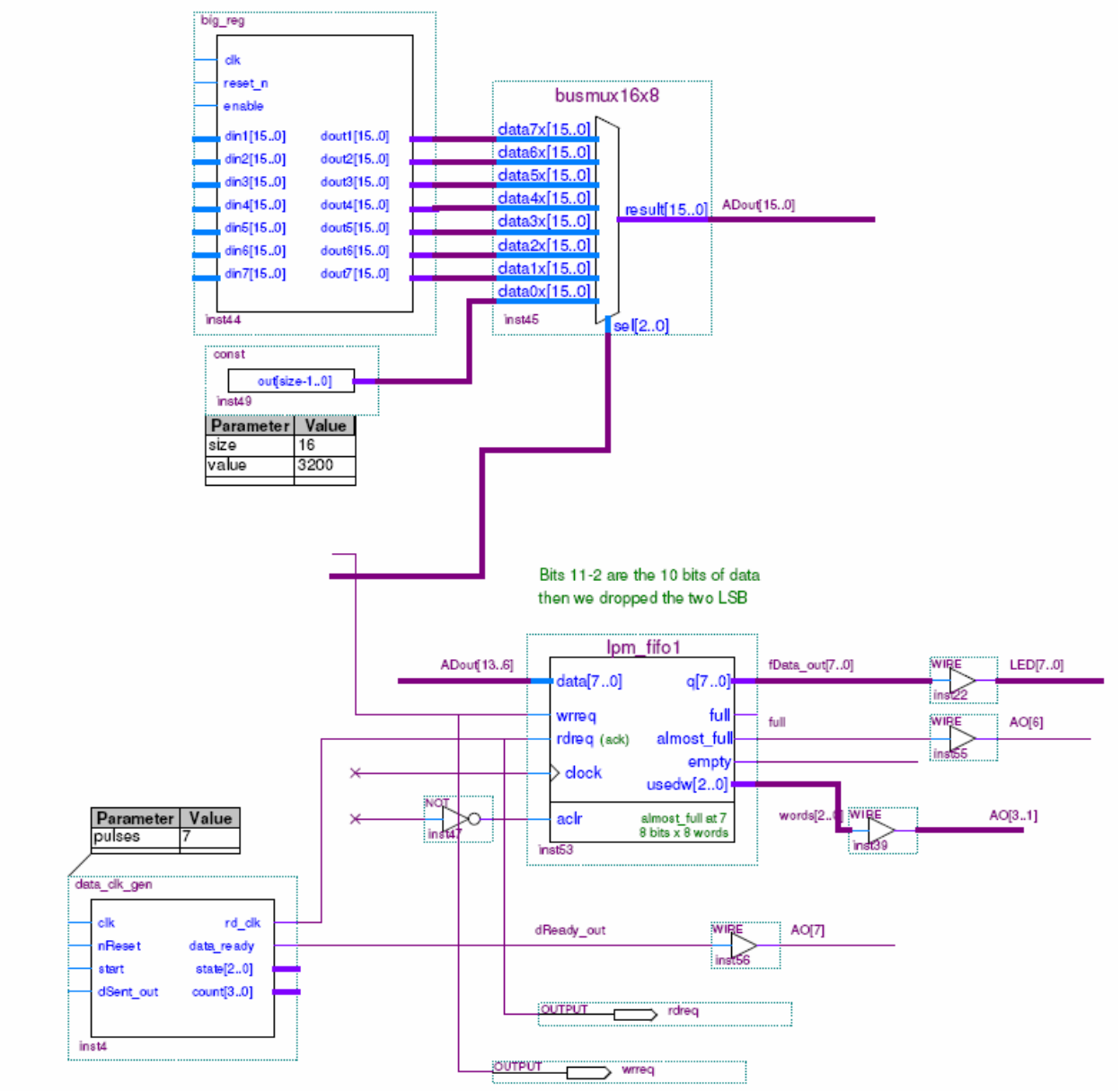


Figure 23. The FIFO section. The mux passes its data one at a time to the FIFO. The FIFO waits for the data exchange cycle to pass its data to the parallel port block.

Several other blocks also exist on the diagram shown in Figure 18. A freq_div block is used to divide the 50 MHz system clock down to something slower. One use for this is the gate drive power supply. A forward converter with six isolated secondaries is also on the PIB board, and is shown in Figure 24. A 500 kHz, 44% duty cycle gate drive signal is sent form the freq_div block. This gate drive power supply can also be turned off or on from within the FPGA. Here it is mapped to a simple external dip-switch. Switches and LEDs are included on the board for

diagnostic purposes such as those mentioned above. Lastly, every input to the FPGA must pass through a synchronizer to prevent any metastabilty issues [1]. Metastabiltiy occurs when an input changes state without adequate setup time. A synchronizer consists of two flip-flops in series and insures that the output is correctly synchronized with the system clock.

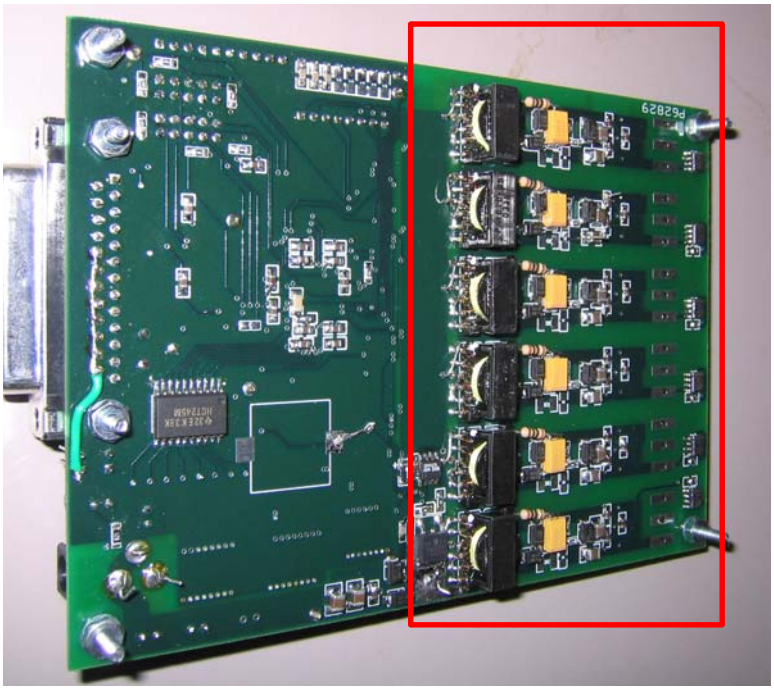


Figure 24. The isolated gate drive power supply. The forward converter (circled above) provides power to the isolated gate drives.

3.3. Controller

The controller consists of an x86 based PC running its own MATLAB propriety xPC Target operating system. The control code is generated from Simulink, MATLAB's graphical system simulation environment. Since Simulink can generate standard C code the target could also be a microprocessor or a micro controller. In a prototyping system the x86 target affords many advantages. The processing power of a state-of-the-art PC is virtually unlimited compared to a simple microprocessor. The additional processing power gives the user the ability to experiment with more complex controllers and refine the design before passing the code along to a chip more likely to appear in an embedded system. Also, the PC target allows the user to attach target PC scopes to the controller for displaying system variables on the target's monitor in real-time. Parameters can be adjusted on the fly through Simulink or a web browser interface.

Simulink has the capability to create many types of controllers. A simple controller, like a PID, is easy. Fixed-point scaling can be added to further emulate a real system. Modern control theory and matrix operations can be used to create highly optimized state space systems [24]. Also, state diagrams can be used to create adaptive controllers.

The Simulink interface allows the use of a model based design approach. Before the system is tested at the hardware level a theoretical model of the plant can be tested with the controller. Later, the block representing the theoretical model can be removed and the actual system inserted in its place. In the real world the input to the plant is the PWM gate signals sent to the converter and the output would be the current and voltage sensors. Once the block is inserted the data exchange for the input parameters and output signals is transparent to the user.

Once the plant block is opened up there is a substantial amount of communication present. The xPC target to FPGA communication uses a standard PC parallel port. Specifically, it uses the Enhanced Parallel Port (ECP) standard. The ECP standard is the third major revision to the common Centronics DB25 standard found on early PCs, and is about 10 times faster than the original parallel port specification. All handshaking is done in hardware, which requires fewer CPU cycles to transfer a byte. This reduction in I/O overhead improves the cycle time that a given PC can run. Also, the ECP has a first in first out buffer (FIFO) for pooling up data. In our case this is used for bringing in all of the samples from the previous cycle [3].

The driver for xPC target is written in C code and compiled into a standard Simulink S-function [18]. Control of the parallel port is done through a basic I/O port library provided by xPC target. The “rl32eOutpB” function is used for writing a 32-bit word to a specific I/O port and the “rl32eInpB” function is used for reading 32-bits from a specific port. The parallel port base address resides at 0x378 in a standard PC. Data is passed to and from this address as well as 5 other registers which control additional port parameters such as direction. The basic structure of the driver is as follows and can be seen in Figure 25:

1. Initialize port
2. Clear FIFO
3. Read sensor data from FIFO
4. Set port to output mode
5. Output A, B, and C duty cycles
6. Output checksum for duty cycles
7. Set port to input mode
8. Goto 3 above

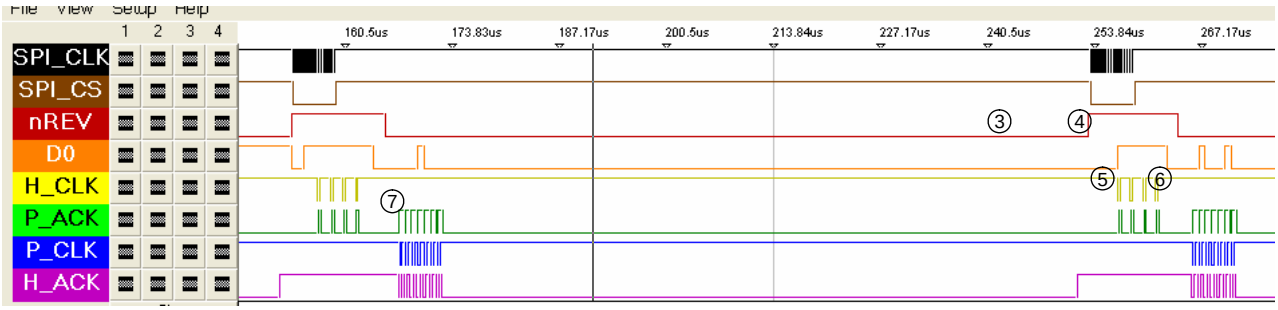


Figure 25. The data exchange cycle. The data from the previous cycle is pulled from the FIFO at the beginning of each sampling cycle.

3.4. Power System and Sensors

The power system consists of a standard six-switch IGBT bridge on a PCB configured to allow maximum flexibility for different topologies. Footprints for extra capacitors and inductors have been added. Nearly all useful currents and voltages have been instrumented, see Figure 26.

The power board has been designed as a proof of concept and is capable of running at about 5 kW. Sensors have been designed for high bandwidth and are good up to around 50 kHz. Communication channels allow for simultaneous sampling of all 7 sensors.

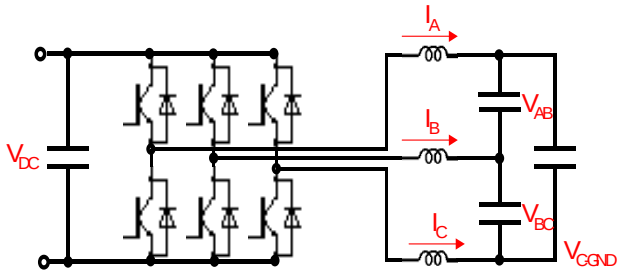


Figure 26. Power Board Topology and Sensors. The power board consists of a six-switch topology and seven sensors.

The power board, see Figure 27 below, can be configured for a variety of topologies, such as, interleaved buck or boost, power factor correction, multi-phase inverter, motor drive, and resonant topologies. Various PWM patterns for these converters are also easily implemented on the PIB.

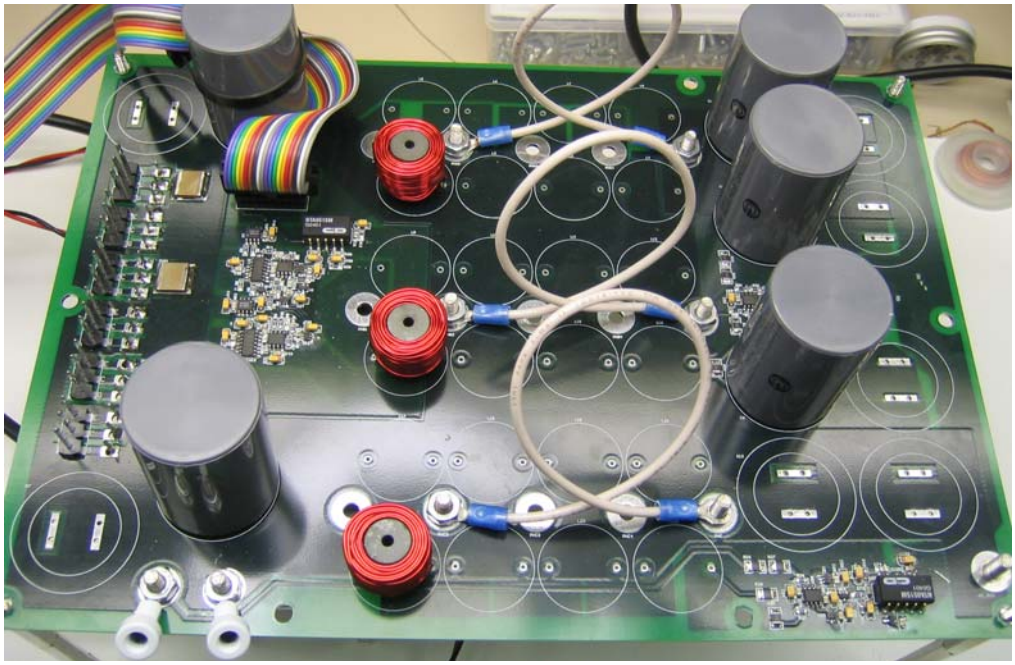


Figure 27. The power board. The power board was designed for maximum flexibility allowing a variety of different topologies to be implemented by easily removing and adding circuit components.

The sensor schematic is shown in Figure 28 below. The high voltage is first divided down to a usable value with a resistive divider. This is then brought into a differential amplifier (OPA2277UA) and then over to the serial A-to-D (ADCS7476). The A/D is a 10-bit A/D capable of 1 million samples per second. The communication from the A/D to the FPGA is electrically isolated through the high speed digital isolator (HCPL-0930). Isolated power is supplied through a small (1 Watt) DC/DC. The current signals are acquired in a similar fashion except the hall effect sensors are already electrically isolated so there is no need for the extra high speed digital isolator.

The system actually used in testing has several limitations. First the current sensors were not used in the controller because it was decided that a low-cost controller probably wouldn't use them. They were used for visual analysis while the system was running but not in an actual controller. Second, the bus voltage used was a 300 volts. Limited availability of programmable DC supplies meant the full bus voltage (400V) wasn't available. A step-up transformer and a diode rectifier were used. This setback was actually helpful because the output voltage could be scaled down and it added DC bus ripple that made it easy to analyze audiosusceptibility.

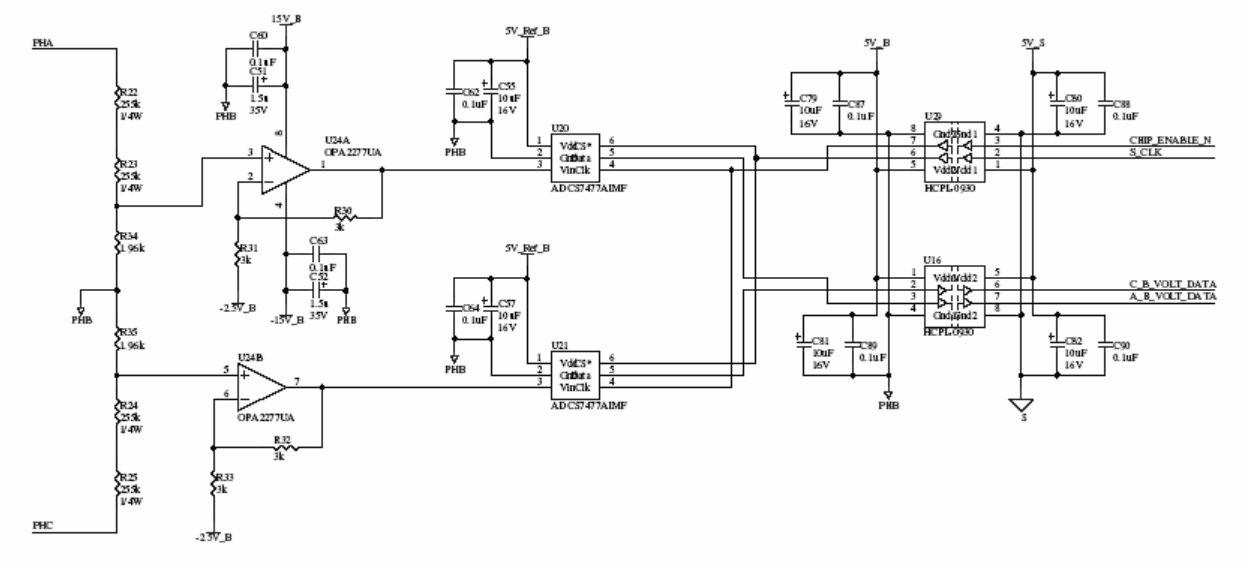


Figure 28. Isolated high voltage sensors. The voltage sensors use serial A/Ds and high speed digital isolators to maintain a clean noise free signal.

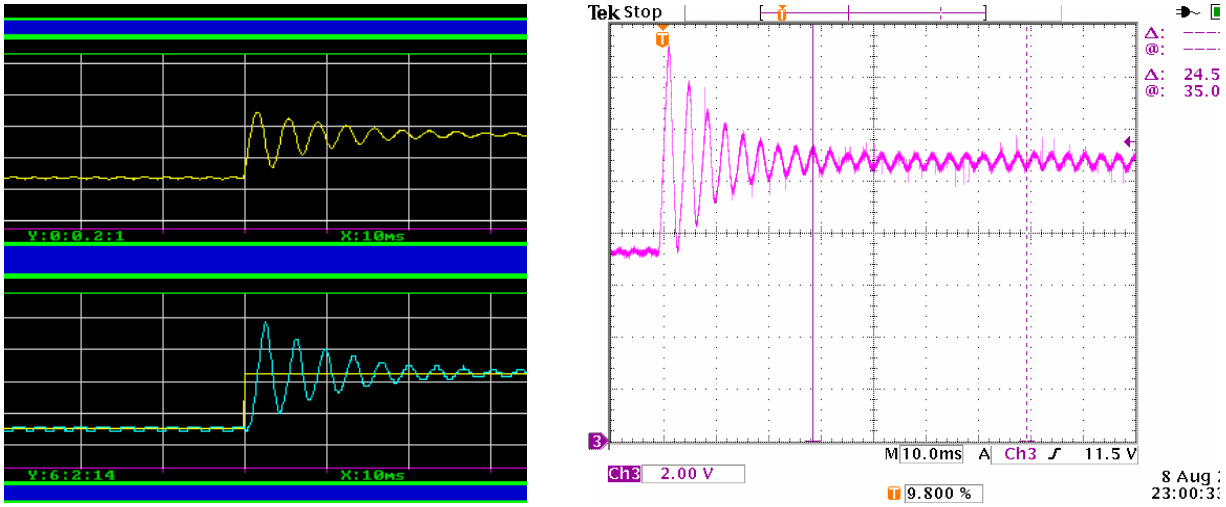
3.5. User Interface

One of the most useful things about the rapid prototyping system is the user interface. Unique systems can be quickly implemented and a variety of system data can be rapidly brought together for examination. A typical design cycle would progress as follows:

1. Create or find a mathematical model of the system
2. Setup a Simulink model based upon the mathematical model
3. Simulate the system and verify stability and desired operation
4. Configure the physical power system to match the converter to be tested
5. Compile and download controller code to target
6. Run system and analyze data
7. Reconfigure and reanalyze

Steps 1 and 2 were shown in Chapter 2. Steps 3 through 7 are shown in Chapter 4. The xPC target system is responsible for most of the functionality in the last few steps. Its documentation thoroughly outlines the tools used in steps 5 through 7 [19]. After a good simulation is put together and tested the user is ready to move on to the actual hardware. Compiling the code is as easy as selecting a menu item in Simulink. The compiled code is automatically downloaded to the target. After download the system is ready to run.

While the system is running the target displays data on its attached monitor. xPC target scopes are added to the Simulink diagram, see Figure 33 in orange. Figure 29 shows an example of a target scope capture and a matching real scope capture. The overshooting output voltage in the bottom scope pane on the left (blue) is also shown on the right. You can see that both are nearly identical. With this setup an actual scope is barely necessary at all. In fact the target scope can even show non-real data such as D or Q currents in a rotating reference frame controller. In addition, data can be captured for post processing.



(a) xPC Target Scope (b) Actual Scope

Figure 29. A comparison of the xPC target scope and a real scope capture. (a) This plot shows what the user would see on the target PC's screen. (b) This plot is nearly identical and shows what the user would see on an oscilloscope.

Once the user understands how the system is behaving they will most likely need to adjust parameters. Items such as gains, offsets, matrix coefficients, and run times can be adjusted on the fly. In the event of a major change the system usually needs to be recompiled.

3.6. Summary

As previously mentioned the HIL control system was designed for maximum flexibility. The setup time required to develop or verify new control schemes can be minimized with this system because many of the usual problems associated with digital control are eliminated. Fixed-point issues, complicated coding, processor computing power, non-linear functions, and system

visibility are all simplified. This leaves time for developing better controllers which can minimize power converter size and cost as well as help in the overall design and testing phase.

The system shown could be arguably faster than an optimized DSP based arrangement. However, the real advantage is in the total time necessary to design and verify the controller. Design iteration time is reduced which leaves time to improve the algorithm or explore different controller options. Once the best control scheme is determined any number of inexpensive microprocessor based solutions could be implemented.

Chapter 4 - Circuit Simulation and Hardware Experimentation

4.1. Plant Model

Circuit simulation was performed in Matlab's Simulink software package. While Simulink is not typically used for circuit simulation it performs very well for controller design. The state space system from Chapter 2, see (14)(15)(16), was modeled as a non-linear time invariant system. Parameters in the A matrix like resistance (R_1 and R_2) were allowed to change with respect to time. This would happen during a step change in load. Also, input voltage (V_{0D}) was allowed to change with time. These additional details provided an accurate model of the plant and allowed the controller to be simulated and tested for stability over varying operating points.

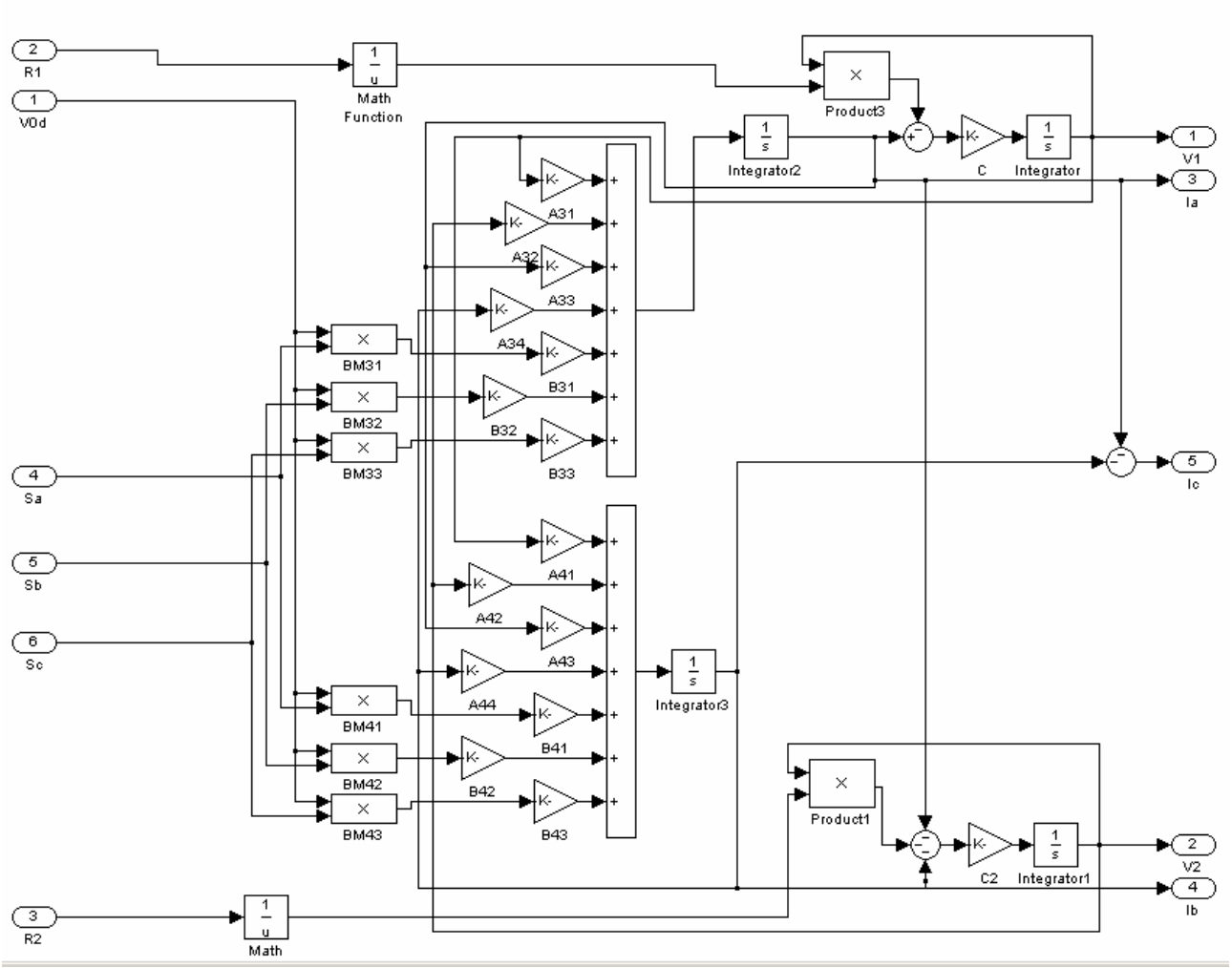


Figure 30. The Simulink Plant Model. The Simulink diagram for the plant model is shown above. Gains from the A and B matrix are shown in the middle and are denoted by names like A34 for A matrix row 3, column 4, also from **(14)** in Chapter 2.

The duty cycle inputs into the plant were modeled with effects that would typically be seen in a digital controller, see Figure 31. The quantization delay is present because the 8-bit digital PWM modulator uses a time step size of $F_s*(1/2^8)$. The quantization represents the fact that the digital PWM modulator must change its pulse width in discrete time steps. The dead zone block represents the lack of response with very small duty cycles (near zero). This lack of response shows up because dead time is used to prevent cross conduction in complementary switch pairs. With a finite turn-on and turn-off time the IGBTs minimum pulse width is limited. This phenomenon is also known as minimum pulse elimination. The dead zone is active from five percent to zero. The zero-order hold block represents the fact that the duty cycle can only be

changed at discrete time intervals or once per switching cycle. Lastly the saturation block represents the fact that the converter can only implement zero to one-hundred percent duty cycle.

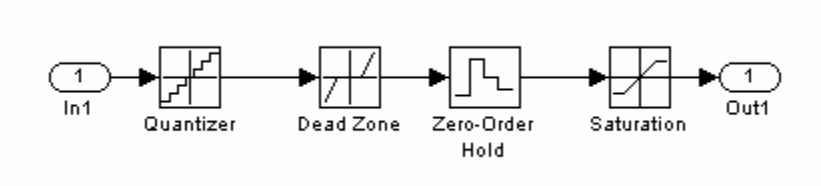


Figure 31. Plant input non-linearities. Plant inputs were modeled with effects typically seen in a digital system.

The plant outputs in a digital controller also have some discrete sampling effects that need to be modeled. Quantization and the zero-order hold are present in any sampled digital system. In our system we use 8-bit 500 volt sensors. The associated quantization is modeled with a $500*(1/2^8)$ step size. The analog to digital converters (A/Ds) are sampled once per switching cycle. The zero-order hold uses the switching time as its delay time.

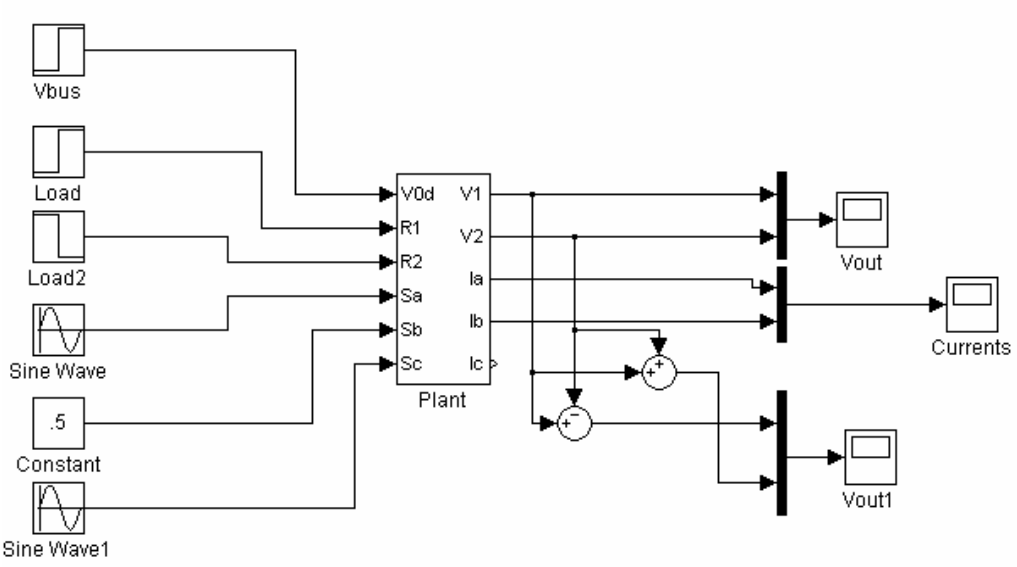


Figure 32. Plant model. A typical open-loop simulation is shown above. V_{0D}, R_1, and R_2 can be stepped or otherwise perturbed to vary the operating point.

Once the open loop model is built and tested the designer can begin to work on the controller. The remainder of this chapter will focus on various controllers and their advantages and disadvantages.

4.2. Controller

The first controller type examined is a simple closed-loop voltage controller with a sinusoidal reference. The basic system is shown below in Figure 33. The system contains a differential controller and a common controller. The differential controller controls the differential voltage or the 240 VAC. The common controller makes the addition of V_{1N} and V_{2N} always equal to zero. This is the same as saying that they are equal and opposite voltages.

For controller design the linear system plant model shown in Equation 14 is used. The decoupling matrix from above is multiplied by the B matrix to form a new B matrix. The operating point used in the design is full DC bus voltage and fairly light load. This point is the hardest to control because the full DC bus voltage acts as a high gain and the light load (100 ohms) provides a very resonant second order system. These properties can be seen in Figure 8 and Figure 12. The "zpk" command is used to find the transfer function from the differential input to differential voltage output. The output is shown in (24) below.

$$\frac{43e9\,(s^2 + 295.7s + 1.794e7)}{(s^2 + 295.7s + 1.794e7)\,(s^2 + 295.7s + 5.378e7)} \qquad (24)$$

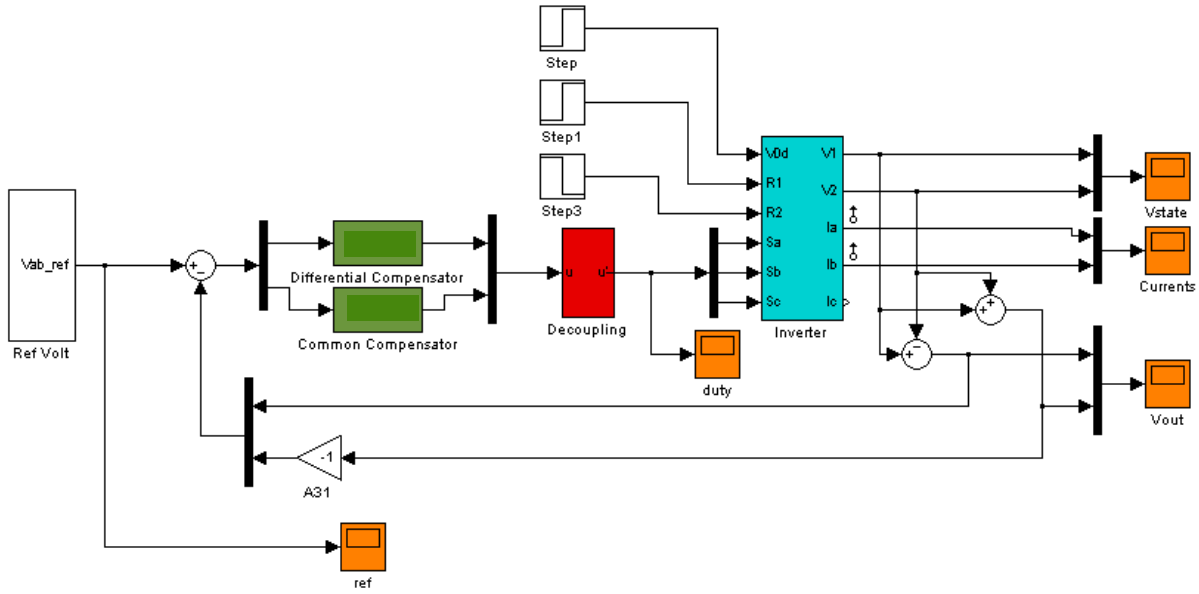


Figure 33. Complete System. The closed-loop voltage controller with a sinusoidal reference.

For a complete linear system one must also take into account the sampling delay. A first-order Pade approximation is used to represent the sampling delay. MATLAB's "pade" command easily calculates the necessary linear system to represent the delay. The "rlocus" command or "sisotool" command is used to show the poles and zeros of the system along with the sampling delay, see Figure 34. The poles shown in Figure 34 will move away from the imaginary axis under more load. Moving the poles away from the imaginary axis means the controller can have more gain and still be stable. Appendix A shows the script file used to execute the commands above.

Controller design started with canceling the two complex poles with zeros. The canceling zeroes were added slightly to the left of the existing poles since a load change would bring the poles in that direction anyway. Then two poles were added at the origin for steady state tracking of a sine wave reference. Next two complex zeros were added to pull the closed loop poles emanating from the origin toward the left half plane. Finally two more real poles were added so that the system had a high frequency roll off. The final compensator is shown in (25) below. The gain was raised as high as possible with a few decibels of gain margin. This gave a crossover frequency of 350 Hz.

$$\frac{359\text{e-}6\,(s^2+1990s+1.083\text{e}6)(s^2+499s+5.34e7)}{s^2\,(s+2597)\,(s+4901)} \qquad (25)$$

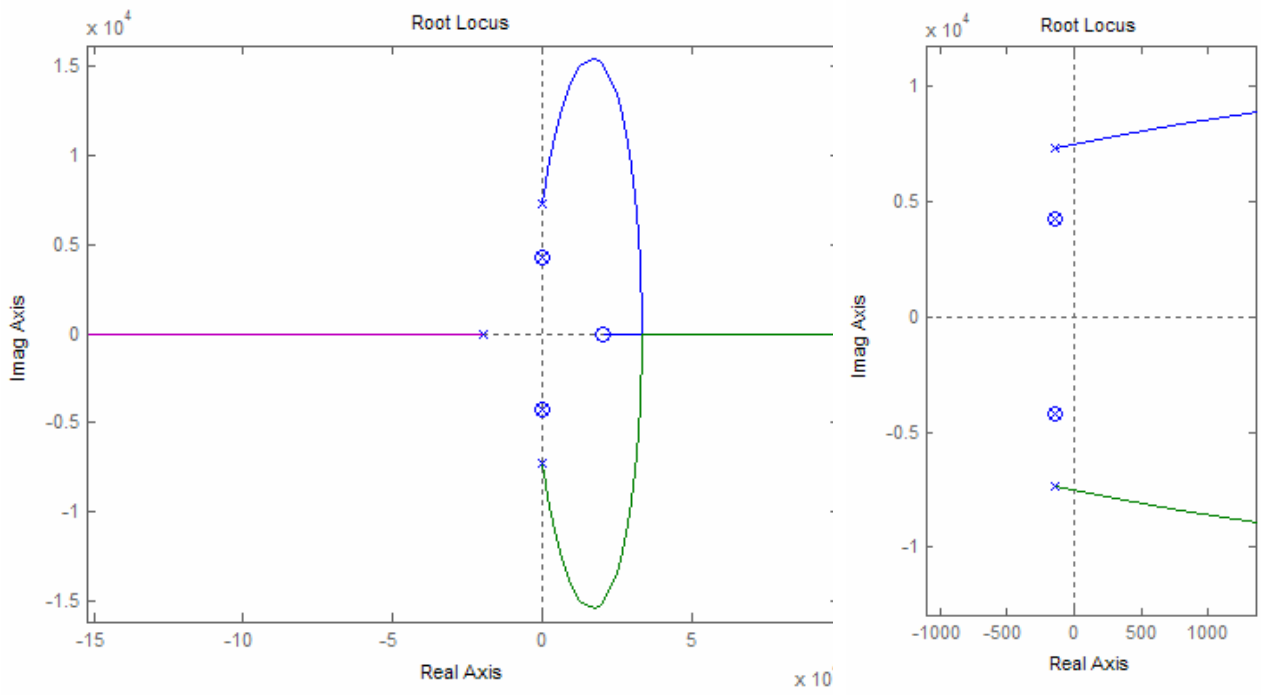


Figure 34. d_{diff} to V_{diff} root locus. The closed loop root locus of d_{diff} to V_{diff} with sampling delay in the feedback loop is shown above. The compensator is set to unity gain. The right-hand plot shows a more detailed picture of the poles near the imaginary axis.

In order to simplify troubleshooting the system was first run with only a differential compensator. Any interactions that might be present between the controllers were eliminated and the differential voltage regulation was verified at several operating points. Figure 35 and Figure 36 show the simulation and actual response for the differential voltage and the common voltage during a load change. Simulation and experimental data match very well. The differential voltage regulates fairly well. The output voltage is fairly steady, but does show some audiosusceptibility due to the rectifier supplied DC bus. The input voltage can be seen in the top left panel of Figure 35 and Figure 36. The bus has a 30-volt ripple unloaded and a 50-volt ripple under load. The ripple frequency is twice the input rectifier frequency, but contains many higher order harmonics during the rising edge. Since the controller does not have any gain above 350 Hz it can't entirely eliminate the effect of the input ripple. Lastly, the unregulated common voltage obviously needs a controller. Figure 38 shows the common voltage on the output, and about 20 volts of error is present.

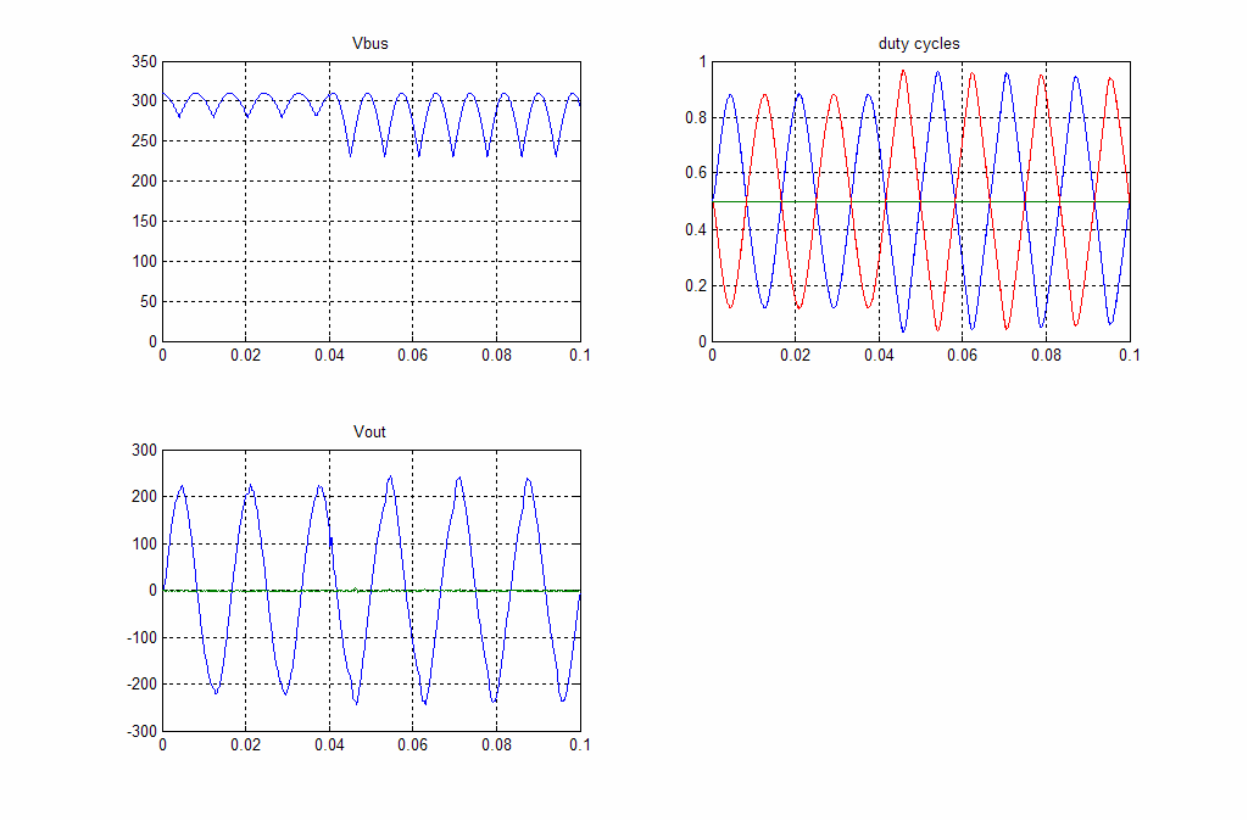


Figure 35. V_{diff} controller simulation. The load step (at 40 ms) causes the bus to drop more and the duty cycles increase to maintain the same differential voltage.

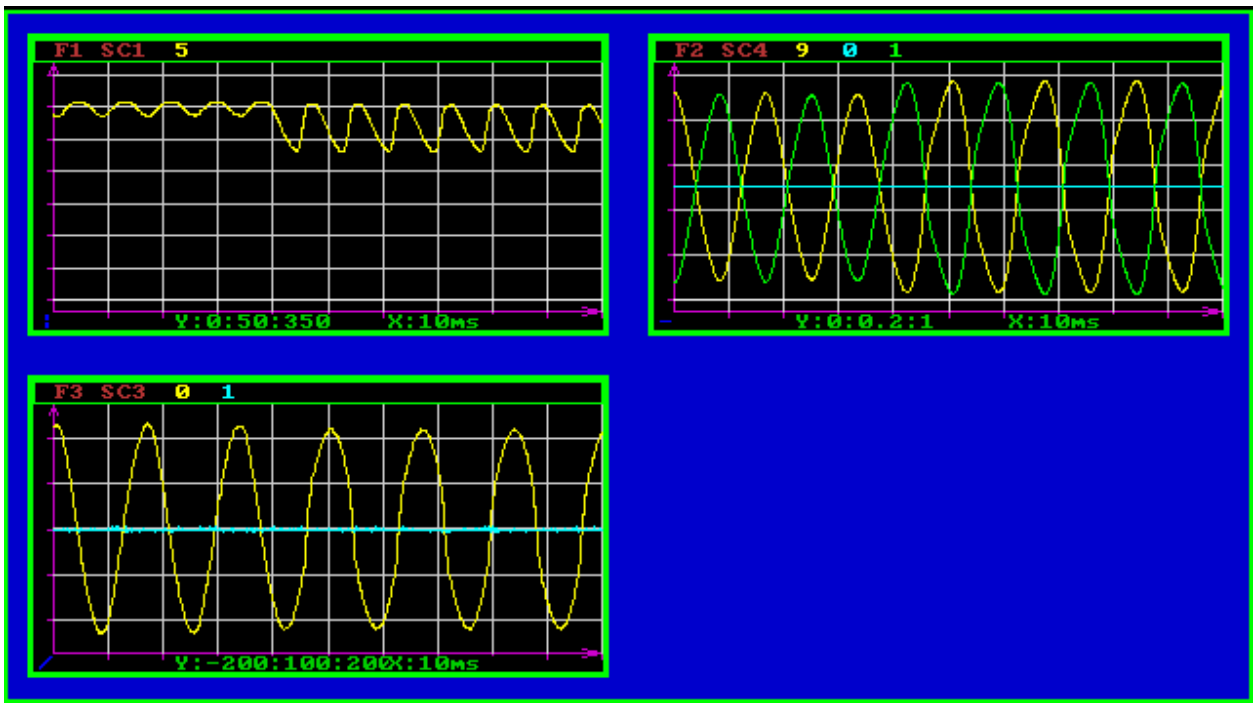


Figure 36. V_{diff} controller experimentation. The xPC Target capture above shows the system during a load step from no load to a moderate load across both V_{1N} and V_{2N}. The upper left is the DC bus, upper right the duty cycles, lower left the output voltages.

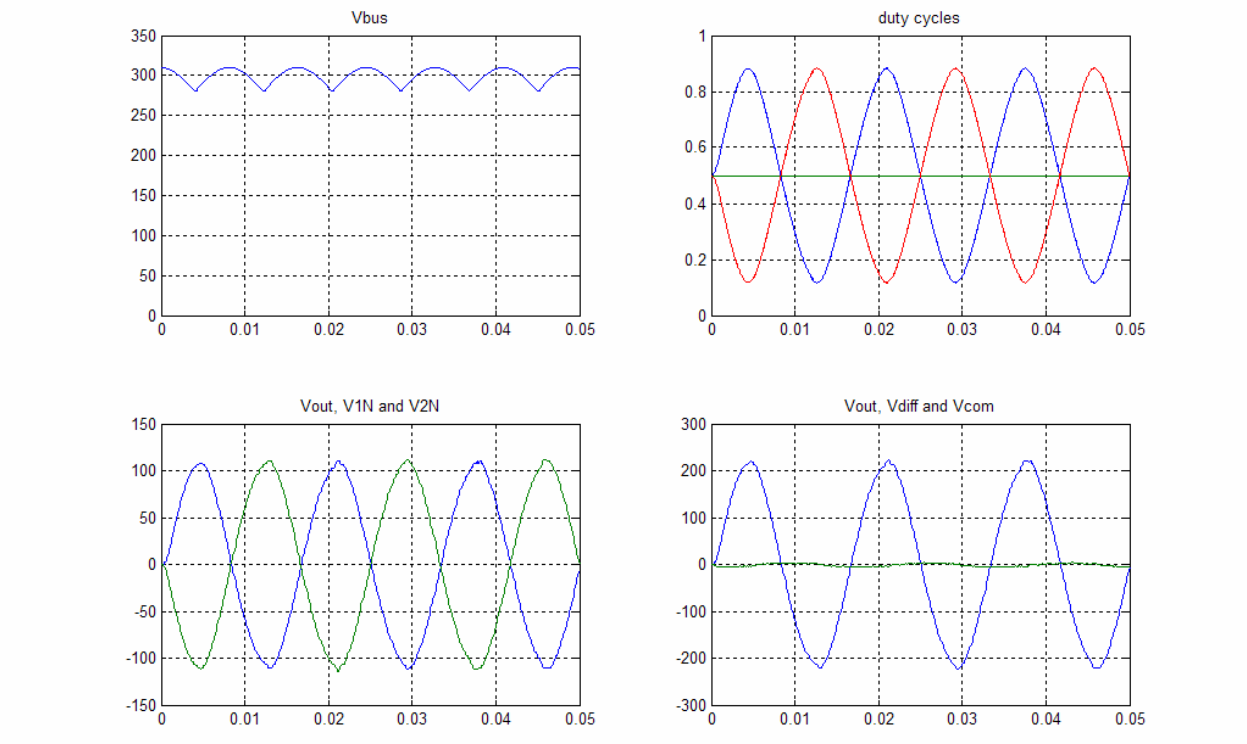


Figure 37. Unevenly loaded system simulation. During uneven load the common mode voltage varies. In the lower right plot one can see the line does not stay at zero as it should.

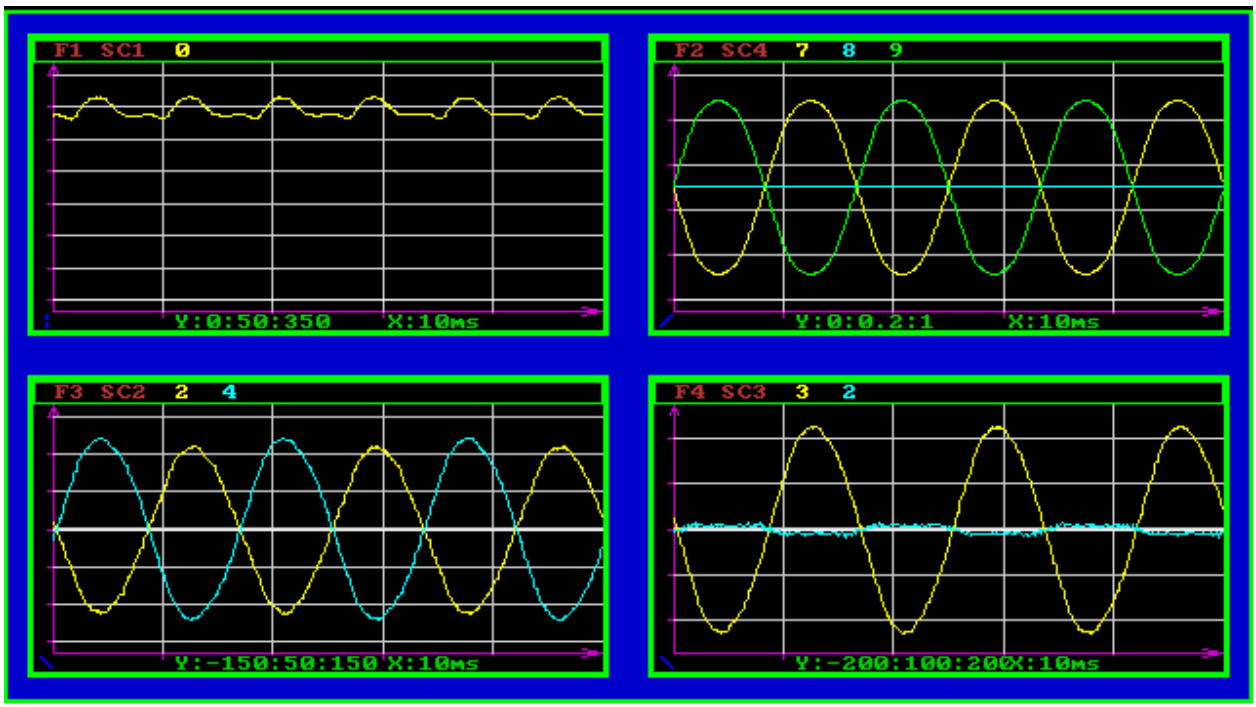


Figure 38. Unevenly loaded experimentation run. The scope capture shows the system running with an uneven load. Upper left is the DC bus, upper right the duty cycles, lower left the output voltages (V_{1N} and V_{2N}), and lower right the same output voltages again (V_{diff} and V_{com}).

The transfer function from common input to common output is shown below in (23) and the closed loop root locus is shown in Figure 39. It should be noted that the negative sign in the transfer function gives a 180-degree phase shift at low frequency.

$$\frac{-21.505e9\,(s^2 + 295.7s + 5.378e7)}{(s^2 + 295.7s + 1.794e7)\,(s^2 + 295.7s + 5.378e7)} \qquad (26)$$

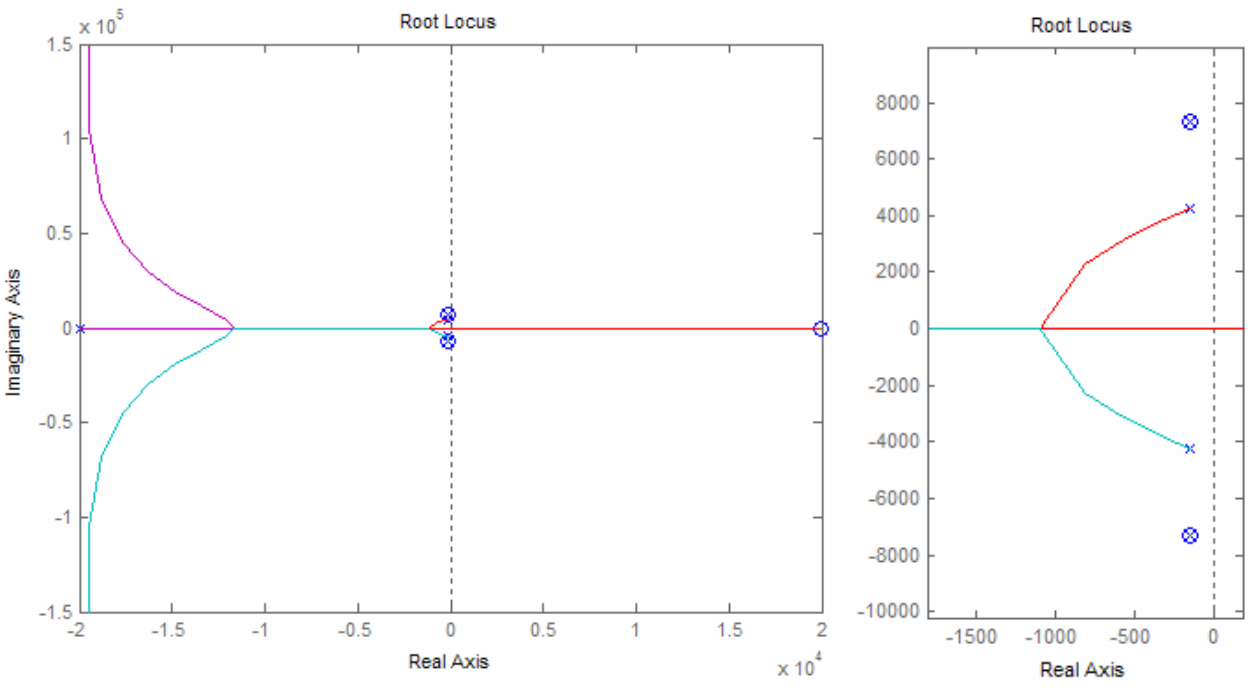


Figure 39. d_{comm} to V_{diff} root locus. The closed loop root locus of d_{comm} to V_{comm} with sampling delay in the feedback loop is shown above. The right-hand plot shows a more detailed picture of the poles near the imaginary axis.

The differential mode controller started with setting the feedback to positive feedback since the plant naturally had a 180-degree phase shift. Next two poles at zero were added for tracking with a sine wave disturbance. Two zeros were added to cancel the poles shown in Figure 39. One more pole was added to bring the closed-loop pole trajectories emanating from the origin to the left-hand side. Finally a zero was added to make the system practical at high frequencies. The root locus and open loop bode are shown in Figure 40, and the step response and closed-loop bode are shown in Figure 42. The closed-loop bode shows that the system has fairly flat response up to 317 Hz where it crosses over. One problem is the slight resonance at crossover. This effect is seen in the step response simulation, see Figure 42, which has a high frequency oscillation. The phase shift is also important because the system needs to track well at the disturbance frequency of 60 Hz. The final zpk form of the common compensator is shown above in (24).

$$\frac{395e-3\,(s\,+72.6)(s^2+647.3s+1.821e7)}{s^2(s+3884)} \qquad (27)$$

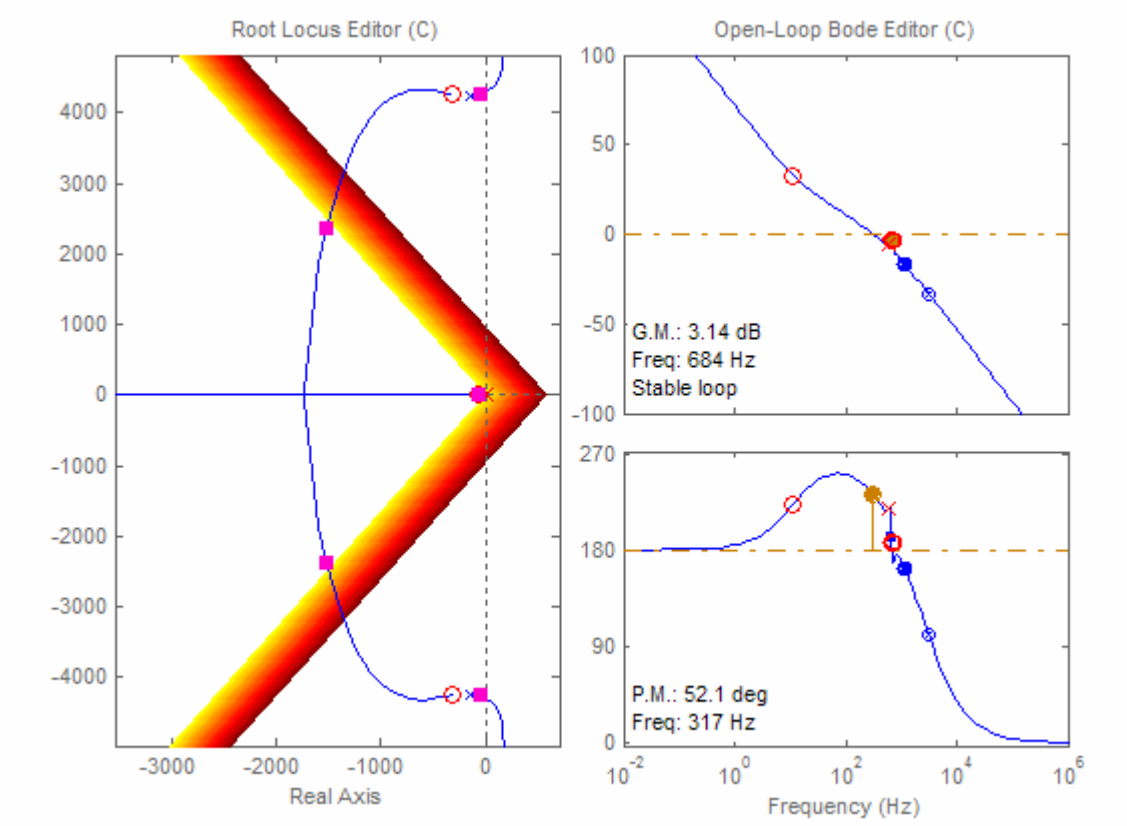


Figure 40. d_{diff} bode plot and root locus. The root locus and open loop bode for the differential mode controller are shown above. The shaded area on shows the region that the closed-loop poles must stay inside to minimize the overshoot during a step. The system has 317 Hz of bandwidth.

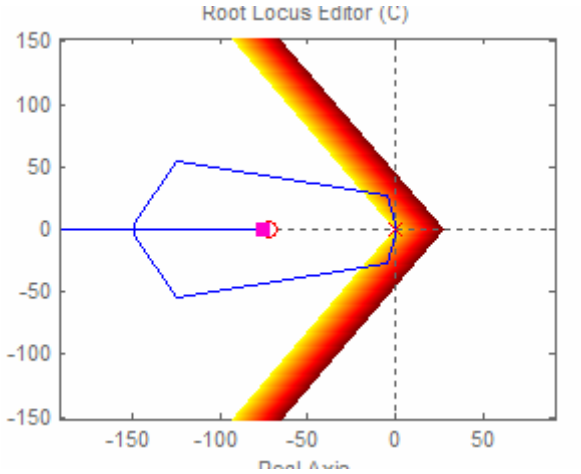


Figure 41. d_{diff} detailed root locus. A more detailed view of the center shows two poles at the origin and a zero at –75.

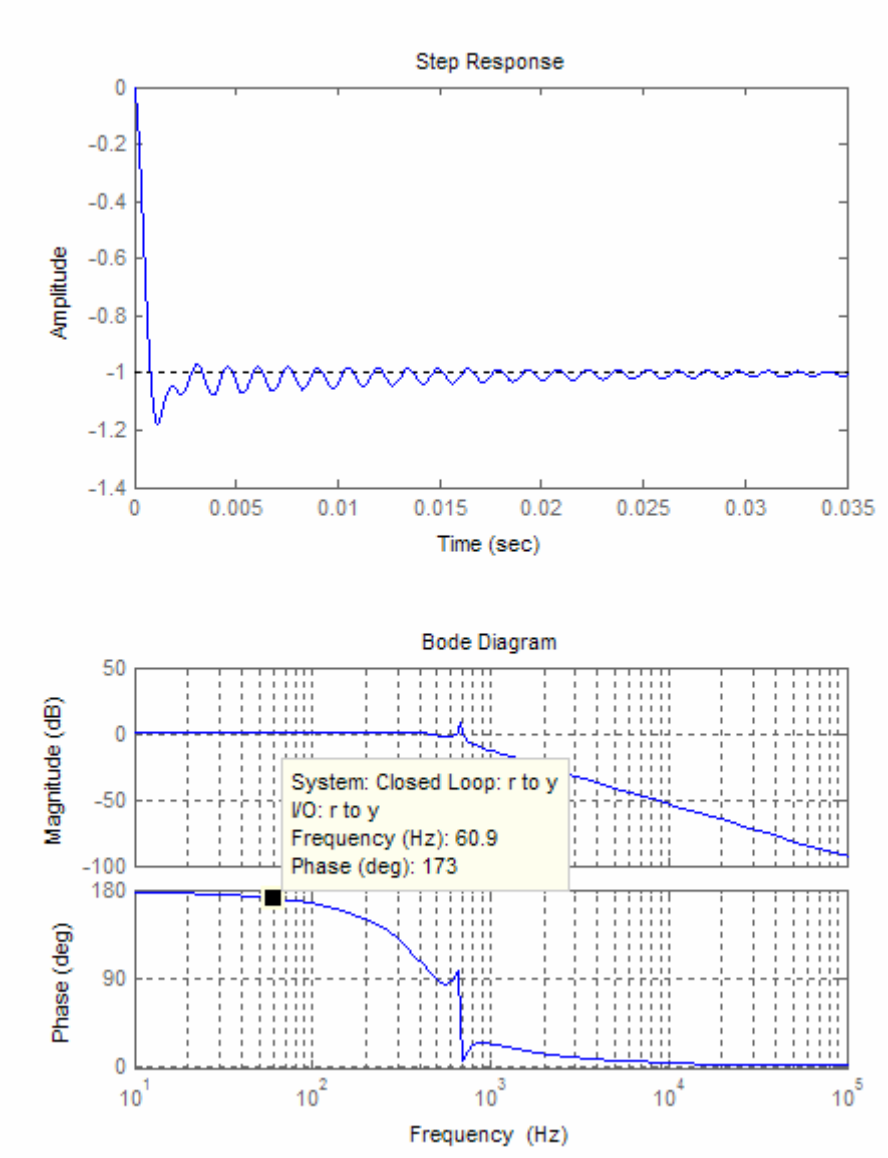


Figure 42. Closed loop bode and step response. The overshoot is less than 20 percent and the phase shift at 60 Hz is only 7 degrees.

The final closed loop system behaved fairly well under varying types of load steps as well as unbalanced loads. Figure 44, below, shows the system running with an unbalanced load. The top right panel shows the duty cycles and it is evident that the center leg duty cycle is being adjusted to compensate for the disturbance in V_{com}.

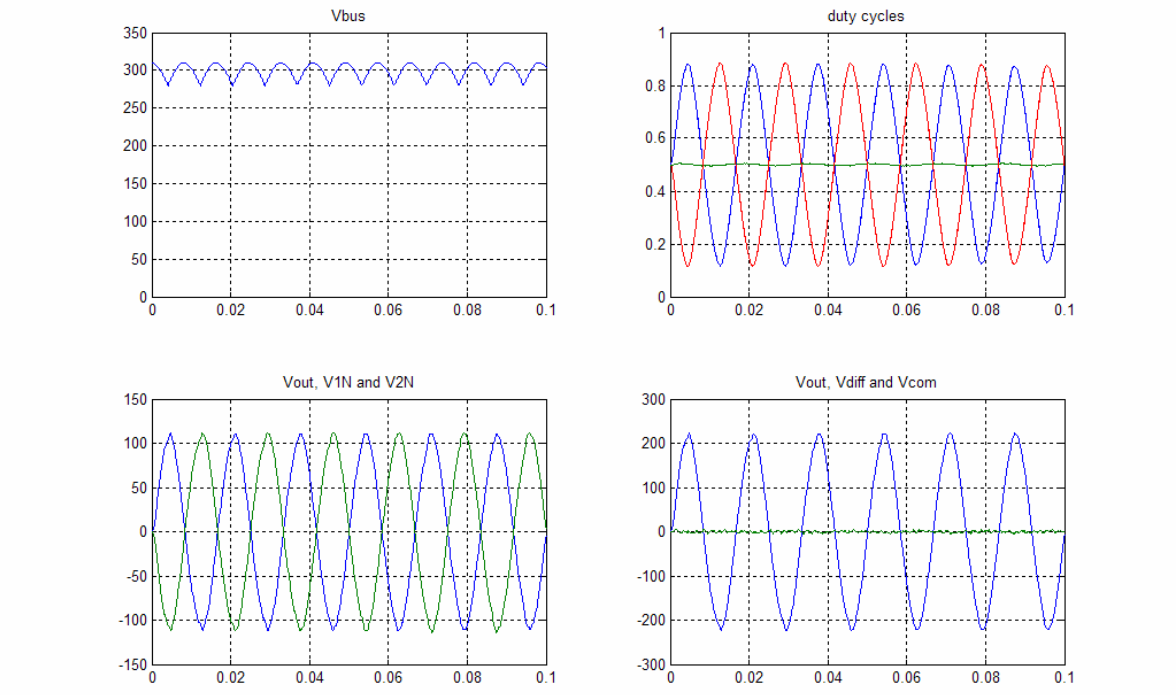


Figure 43. Simulation of both V_{diff} and V_{com}. With controllers working the common mode voltage is greatly reduced and the differential voltage is tightly regulated.

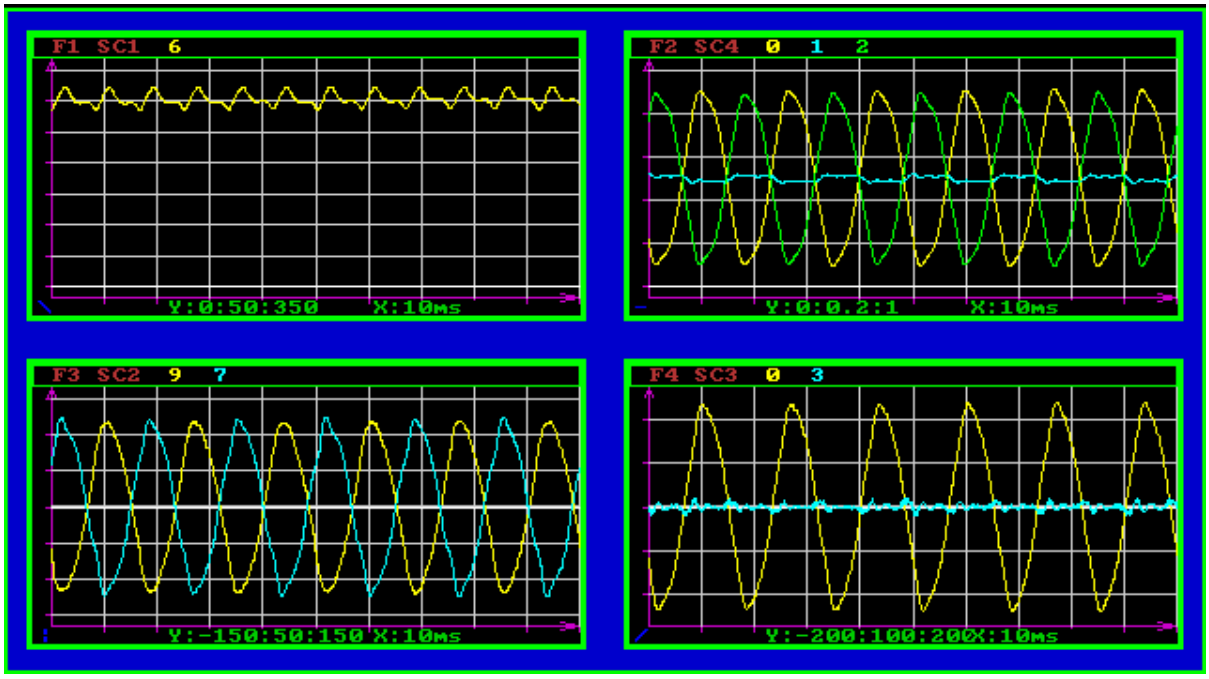


Figure 44. Experimentation using both V_{diff} and V_{com} controllers. The scope capture above shows the system with both the V_{diff} and the V_{com} compensator in the loop. The load is unbalanced however the common output voltage stays fairly close to zero. Upper left is the DC bus, upper right the duty cycles, lower left the output voltages (V_{1N} and V_{2N}), and lower right the same output voltages again (V_{diff} and V_{com}).

One area where the system did not perform well was with a non-linear load. A rectifier with a DC load was attached across V_{12}. This type of load presents several problems. First, it pulls high currents at the peak of the sine wave and no current at all during the remainder of the waveform. This behavior causes high frequency components in the load current that can excite resonance in the controller or just distort the output voltage waveform. Secondly, with a capacitor on the rectifier output even higher surge currents exist on start-up. Figure 46 shows the system during this condition. Half way through the scope capture the non-linear load is added. The DC bus begins to dip as does the output voltage. In response the duty cycles are increased and eventually are completely saturated for parts of several line cycles. When the capacitor is fully charged the controller finally starts to recover but still cannot respond quickly enough to the surge current to prevent the output voltage from dipping at the peak of the sine wave. This case was not too bad but several others did not recover from duty cycle saturation and the system went unstable. A controller with a higher bandwidth would certainly be able to deal with this type of load better. Unfortunately, because of the 10kHz sampling limitation the gain can only be increased so far before the system is not stable.

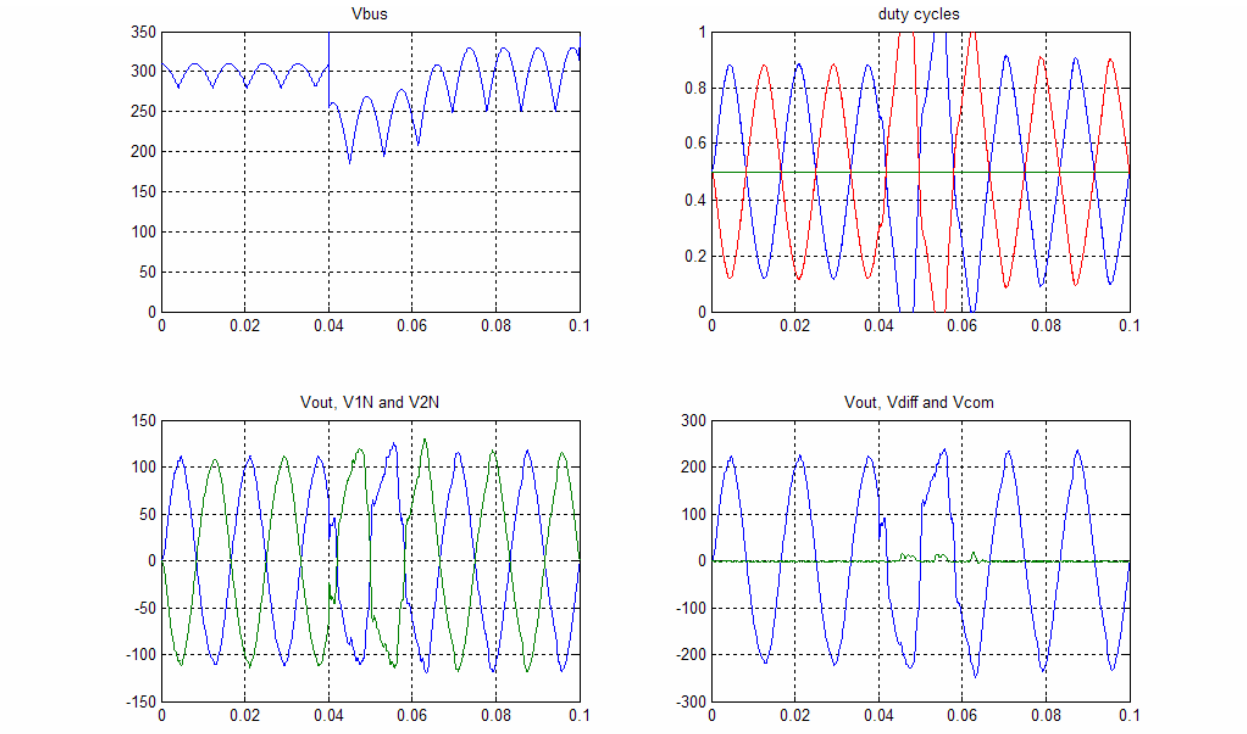


Figure 45. Uncharged rectifier simulation. A rectifier consisting of four diodes and a capacitor on the output is placed across the Vdiff output. The inrush current causes a large surge in power.

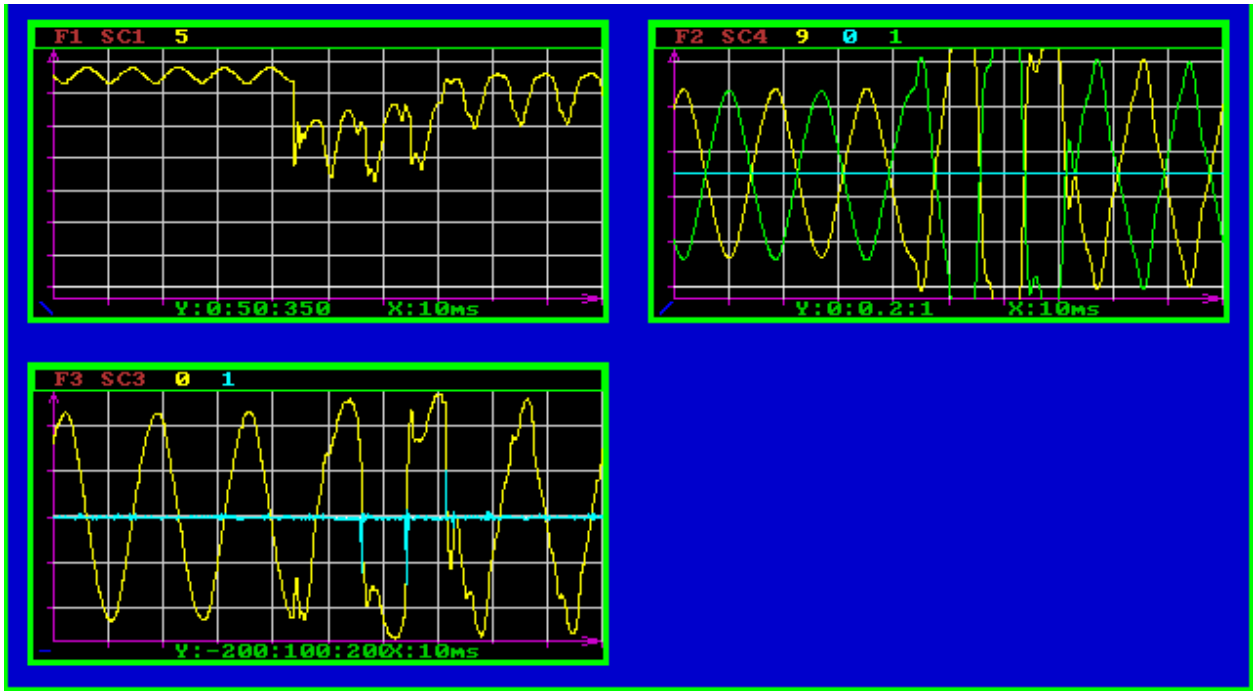


Figure 46. Uncharged rectifier experimentation. This scope capture shows the addition of a non-linear rectifier load across V_{12}. Upper left is the DC bus, upper right the duty cycles, lower left the output voltages (V_{diff} and V_{com}). The system is stable during this large transient event but does have some high frequency harmonics present after the load step.

The audiosusceptibility problem is still unsolved. Another optimization that can be used is a feed forward term. With the previous set of controllers the only feedback term is the output voltage. Any disturbance due to the DC bus voltage ripple can only be handled after it is already evident in the output voltage. A better solution would be to watch the DC bus and actively adjust the duty cycles for any change in bus voltage. A common solution is to linearly increase the duty cycle as the bus decreases. The inverse of the DC bus voltage is found and then a gain term for nominal bus voltage is used to normalize the duty cycles around the nominal bus value. The feed forward controller should work relatively well except for the fact that it the same gain across all measurable frequencies. Any noise that makes its way into the system will immediately affect the duty cycles. A low pass filter was added with a -3dB point of 1.8 kHz. This allowed the higher frequencies present in the bus voltage ripple to pass but blocked a spurious one sampling cycle blip in the output voltage. Figure 47 shows the solution implemented in Simulink, and Figure 49 shows the scope capture during operation. The top right panel in Figure 49 shows the duty cycles, which are fairly distorted to deal with the bus

ripple. The two lower plots show a much smother sine wave output than in previous controllers, see Figure 36.

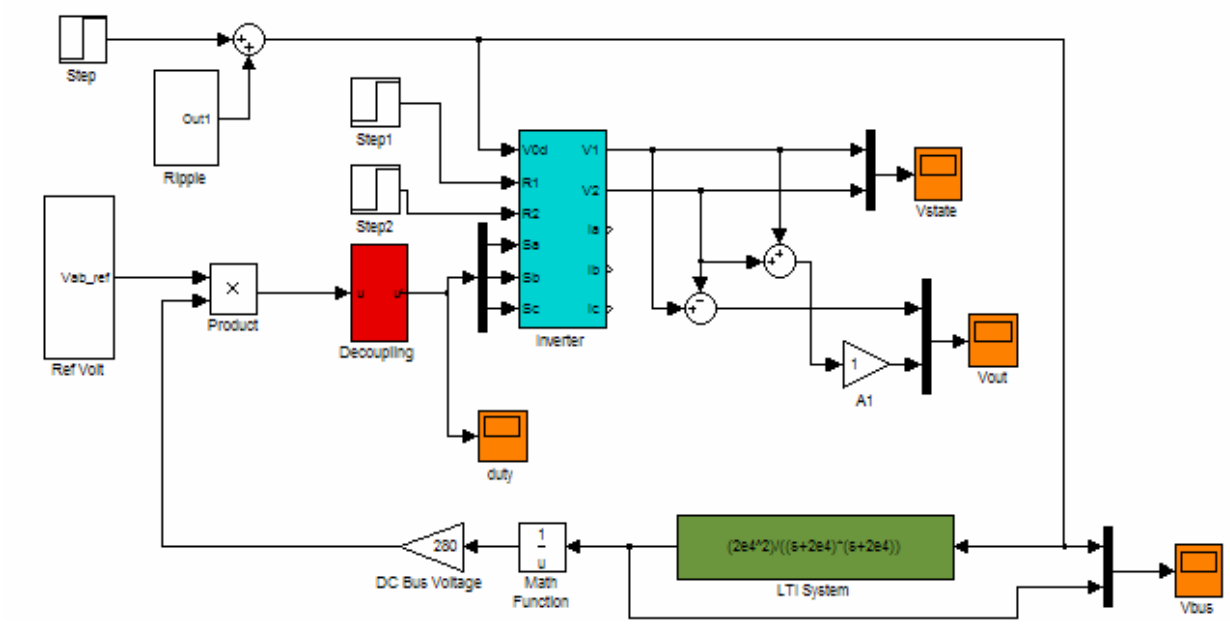


Figure 47. Feed forward controller. The feed forward controller simulation diagram.

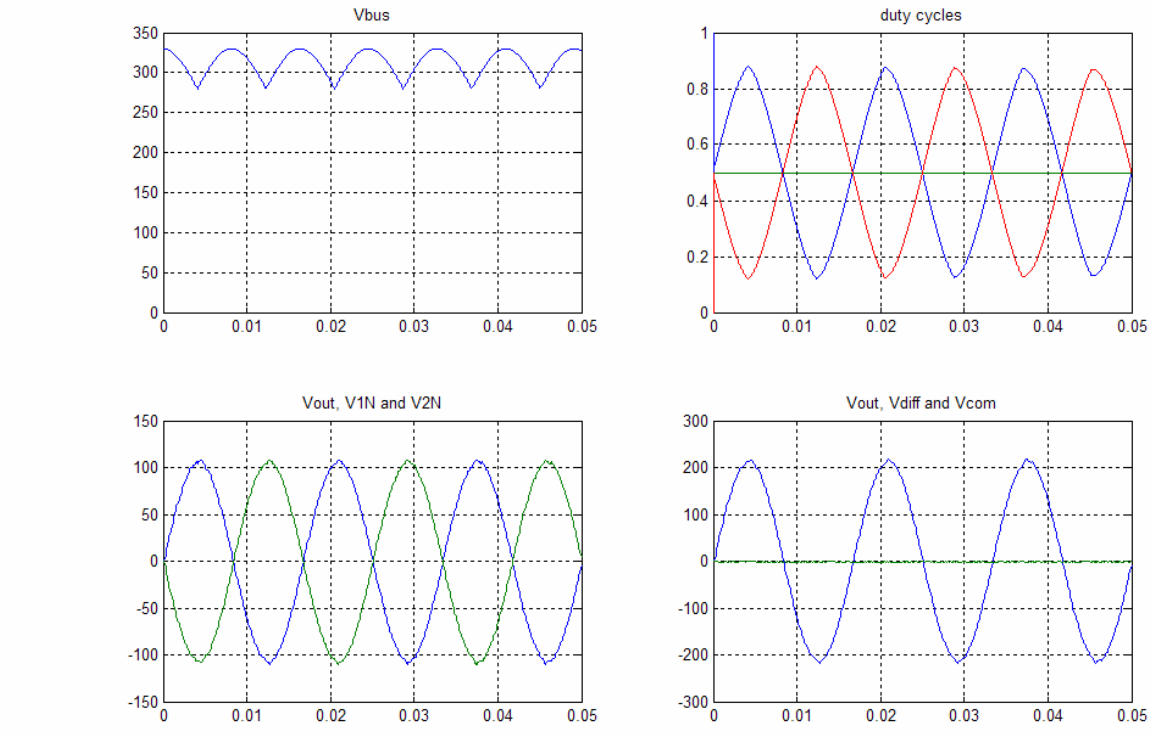


Figure 48. Feed forward controller simulation. The feed forward controller lets the system deal with high frequency input voltage fluctuations.

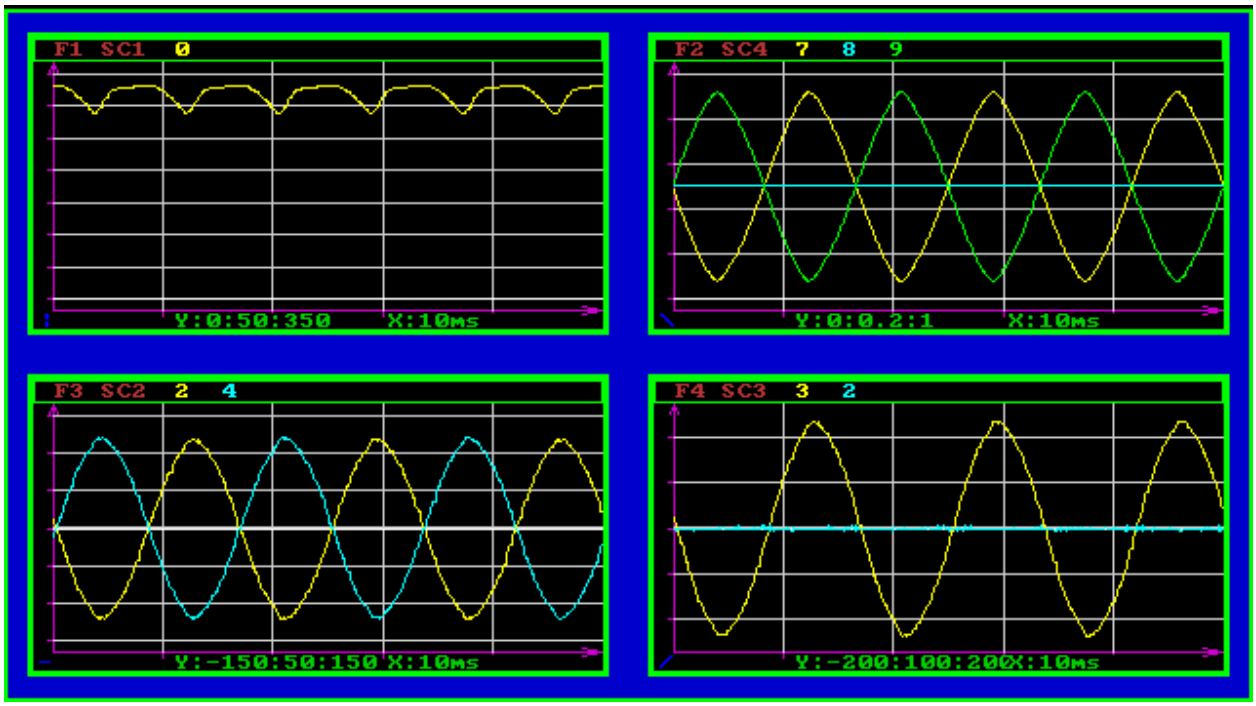


Figure 49. Feed forward controller experimentation. The scope capture above shows the feed forward controller in operation. Upper left is the DC bus, upper right the duty cycles, lower left the output voltages (V_{1N} and V_{2N}), and lower right the same output voltages again (V_{diff} and V_{com}).

Other types of controllers were tried with limited amounts of success. A Linear Quadratic Regulator (LQR) controller was simulated but did not fair well under light load because it includes only proportional gain terms. The controller gain could not be adjusted to work at low frequency but attenuate the resonant frequency as the controller above. In general SISO control methods lend themselves to frequency domain analysis, while in MIMO systems it is often difficult.

Observer systems were used to find the inductor current but had two main problems. First the observer mentioned in Chapter 2 was based upon integration of the inductor voltage. Because of inaccuracies in calculated inductor voltage vs. actual inductor voltage there was a low frequency error in the observer current. Secondly, since the sampling frequency was relatively low it was difficult to accurately estimate inductor current. Several controllers with the high frequency component of the inductor current used as feedback were tried. This has some success but in general the feed forward term was just as effective.

A controller with state transformation similar to a DQ type was investigated but encountered a numerical problem. The output voltage was divided by a reference sine wave voltage to get a DC value, which could be fed back into a controller. This idea worked fine during most of the sine wave, but at the zero crossing the sensitivity to error became extremely high as the output term approached infinity.

Chapter 5 - Conclusion

The six-switch single-phase inverter has been shown useful for distributed energy and fuel cell power conditioning systems typically found in household applications. Output regulation with unbalanced loads is a known problem for systems of this configuration. The third leg in the six-switch inverter was used to balance the outputs during an unbalanced load. Little work existed on this topology so a complete circuit analysis was used to formulate a mathematical model of the inverter and output filter. The system was first expressed in state space form and was further developed into a very accurate Simulink system simulation.

Various controllers were designed and verified in simulation. A decoupling block was designed to separate the MIMO system into differential and common voltage sections. Next, a controller for the differential section was designed and simulated. Once the differential section showed satisfactory performance the common voltage section was completed. Additionally, a feed-forward controller was also designed. This controller was useful in dealing with the DC bus fluctuations that are often seen due to various types of non-ideal power sources. Using the rapid prototyping systems controllers that appeared promising were directly converted to run with a small-scale bench-top power converter. Simulation matched the actual power converter surprisingly well. The differential and common voltages were shown to be controllable and robust to both input voltage disturbances and load steps. Also, the controller did not use expensive current sensors or a high sampling frequency. On the down side, performance with a non-linear load could have been better. Extreme fluctuations in the DC bus voltage did affect the output voltages.

While reduced sampling frequency and lack of current sensors can be an advantage, they also are extremely useful in pushing the system performance and the controller's bandwidth higher. More open loop gain at a higher frequency would have undoubtedly reduced audiosusceptibility and increased the ability to deal with high frequency load disturbances. Overall, the sampling frequency and its associated limit in controller gain was a restrictive factor in just about every controller examined. A well-put example is trying to drive a car too fast with windshield wipers that are too slow. The controller just can't see what's happening often enough to react quickly.

Most of the hardware was available for pushing the sampling frequency much higher. However, the xPC target display and user interface began to suffer above 10 kHz. More work could be done in optimizing the system. Perhaps, with the price of PCs falling daily, a faster

system could be used as the target. Also, noise in the communication interface between the host PC and the target PC was an issue. In a more distributed higher power system, a different interface than the parallel port could be used. A PCI card in the target PC with an FPGA and several optical transceivers would make an ideal communication module. Gate drives and sensors would probably need to be separated both because of the electrically noisy environment near the power switches and the physical location to the sensors. All in all the parallel port interface was a quick and easy way to harness the power of Matlab's xPC target system. In fact a newer revision of the PIB would probably fix almost all of the communication problems and make a superb lab test bench.

Transients like those seen in Figure 46 do still meet the CBEMA curve [15]. So even though the waveform is not ideal; the inverter performance is acceptable. The underlying model and controller hardware is sound and the power is there to make even more complex systems. As a final thought, a useful tool for an even more accurate system model would be to measure the control-to-output transfer function on the actual hardware. The system could be excited through the duty cycle input and output sensors could collect data at an extremely fast sampling rate. Inaccuracies in the model and subtle details in the system could be identified and the controller further customized and refined.

In summation, the contribution of this thesis includes the following:

- Model formulation for uncommon six-switch single-phase inverter topology
- Non-linear time-variant simulation for six-switch single-phase inverter topology
- Multiple controller closed loop system with input decoupling for MIMO system
- Direct from simulation flexible Hardware in the Loop system
- Closed loop design for six-switch single-phase inverter system with satisfactory performance during transients and input voltage disturbances
- Feedforward control design for waveform quality improvement

Future work may include:

- Increased sample speed for better performance
- Closed loop current controller with multiple nested loop controllers
- Improved higher speed and highly noise robust communication interface
- Hardware in the loop system identification to verify modeling efforts
- Using unique system flexibility with higher power and more sophisticated systems

Appendix A, MATLAB work files

```
% MATLAB setup file for six-switch single-phase
% Author:  Chris Smith
% Date: 6/5/2005

clear all;
s = tf('s');

Ts = 1/10e3; % sampling frequency

La = 310e-6;
Lb = 310e-6;
Lc = 310e-6;

Rla = 0.04;  % inductor esr
Rlb = 0.04;  % inductor esr
Rlc = 0.04;  % inductor esr

C1 = 60e-6;
C2 = 60e-6;

% Resonance = 1/(2*pi*sqrt(La*C1))

Vd = 400;  % DC bus voltage

R1 = 100; % load resistance on V1N
R2 = 100; % load resistance on V2N

Lt = La*Lb+La*Lc+Lb*Lc;

%        V1n          V2n         Ia                        Ib
sysA = [ -1/(R1*C1),  0,          1/C1,                     0                          ;  % V1n
          0,          -1/(R2*C2), -1/C2,                    -1/C2                      ;  % V2n
         (-Lb-Lc)/Lt, Lb/Lt,      (-Rla*(Lb+Lc)-Lb*Rlc)/Lt, (Lc*Rlb-Lb*Rlc)/Lt         ;  % Ia
         Lc/Lt,       La/Lt,      (Lc*Rla-La*Rlc)/Lt,       (-Rlb*(La+Lc)-La*Rlc)/Lt ] ;  % Ib

%        Sa                Sb                Sc
sysB = [ 0,                0,                0            ;  % V1n
         0,                0,                0            ;  % V2n
         (Vd*(Lb+Lc))/Lt,  (-Lc*Vd)/Lt,      (-Lb*Vd)/Lt  ;  % Ia
         (-Lc*Vd)/Lt,      (Vd*(La+Lc))/Lt,  (-La*Vd)/Lt ];  % Ib

 %      V1n V2n  Ia Ib
sysC = [ 1,  -1, 0,  0  ; % Vdiff
         1,  1,  0,  0  ; % Vcom
         0,  0,  1,  0  ; % Ia
```

```
         0,  0,  0,  1 ]; % Ib

% original system
sys1 = ss(sysA,sysB,sysC,0,'statename',{'V1' 'V2' 'Ia' 'Ib'},'inputname',{'Sa' 'Sb'
'Sc'},'outputname',{'V1N' 'V2N' 'Ia' 'Ib'});

% bode plot from input to output voltages, see Figure 5 and 6
bode(sys1(1:2,:))

% bode plot from input to inductor current, see Figure 7, 8, and 9
bode(sys1(3:4,:))

% decoupling matrix system
T = [2/3 -1/3 -1/3; -1/3 2/3 -1/3];
D = [T; 1 1 1]^-1*[1 0; 0 1; 0 0];
sys2 = ss(sysA,sysB*D,sysC,0,'statename',{'V1' 'V2' 'Ia' 'Ib'},'inputname',{'d_diff'
'd_com'},'outputname',{'Vdiff' 'Vcom' 'Ia' 'Ib'});

% observer for currents, possibly different ESR for inductor
ORla = 0.04;  % inductor esr
ORlb = 0.04;  % inductor esr
ORlc = 0.04;  % inductor esr
%         Ia                        Ib
obsA = [ (-ORla*(Lb+Lc)-Lb*ORlc)/Lt, (Lc*ORlb-Lb*ORlc)/Lt      ;  % Ia
         (Lc*ORla-La*ORlc)/Lt,     (-ORlb*(La+Lc)-La*ORlc)/Lt ];  % Ib

%        Sa*Vd        Sb*Vd        Sc*Vd       V1n           V2n
obsB = [ (Lb+Lc)/Lt,  -Lc/Lt,      -Lb/Lt,     (-Lb-Lc)/Lt,  Lb/Lt;  % Ia
         -Lc/Lt,      (La+Lc)/Lt,  -La/Lt,     Lc/Lt,        La/Lt, ];  % Ib

obsC = eye(2);
obsD = zeros(2,5);

obs_cont = ss(obsA,obsB,obsC,obsD);
obs_disc = c2d(obs_cont, Ts);

% pade delay for ZOH in sisotool
[delay_num, delay_den] = pade(Ts,1);
delay = tf(delay_num, delay_den);

% d_diff to Vdiff loop design
sisotool(sys1(1,1),1,delay,1);

% d_com to Vcom loop design
sisotool(sys1(2,2),1,delay,1);

% compensators in use
Vdiff_comp = (359e-6*(s^2 + 1990*s + 1.083e6)*(s^2 + 499*s + 5.34e7))/(s^2*(s+2597)*(s+4901));
```

```
Vcom_comp = (0.00039524 * (s+72.6)*(s^2 + 647.3*s + 1.821e007))/(s^2*(s+3884));

% filters for feedforward, etc
high_pass = c2d(eye(2)*(s/(s+1000)),Ts);
low_pass = c2d(2e4^2/((s+2e4)*(s+2e4)),Ts);
```

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Vita

Chris was born in Cherry Point, North Carolina on February, 1979. After graduating from Oak Ridge High School in 1996 he attended Virginia Tech.

In the Fall of 1998, Summer 1999, and Fall 2001 he worked as a coop student at Ericsson Mobile Phones and Base Stations in Lynchburg, Virginia. While there he worked in a variety of positions including the product verification group. His responsibilities included troubleshooting a variety of analog and digital circuit failures associated with manufacturing. In between semesters cooping he enjoyed working with the Hybrid Electric Vehicle Team at Virginia Tech. There he gained experience in a variety of areas such as fuel cells, traction drives, compressor drives, battery storage systems, and hybrid vehicle controls. In his final undergraduate year he served as the electrical team leader.

In 2001 he graduated with a Bachelor of Science in Computer Engineering and was accepted into the masters program in Electrical Engineering, also at Virginia Tech. During this time he worked as a graduate research assistant under Dr. Jason Lai in the Center for Power Electronic Studies and later the Future Energy Electronics Laboratory.

In 2003 having completed his course work for his Masters he started work with Fairchild Controls Corporation in Frederick, Maryland. At Fairchild he worked on several Mil Spec high speed motor drives, both permanent magnet and AC induction. He also worked extensively on 400 Hz power factor corrections circuits.

Chris is a member of the IEEE Power Electronics Society. His interests include motor drives, alternative energy conversion, hybrid vehicles, FPGAs, and control systems.

