Switching-Loss Measurement of Current and Advanced Switching Devices for Medium-Power Systems

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Thesis submitted to the faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

Master of Science
in
Electrical Engineering

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August 10, 2011
Blacksburg, Virginia

Keywords: Device Testing, Cree Z-FET, Switching Loss, CoolMOS, SupreMOS, MDMesh

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Abstract

The ultimate goal for power electronics is to convert one form of raw electrical energy into a usable power source with the lowest amount of loss. A considerable portion of these losses are due to the use of switching devices themselves. Device losses can be apportioned to conduction loss and switching loss. It is commonly known and practiced that conduction loss can be reduced by driving MOSFETs and IGBTs harder with gate voltages closer to the maximum rating. This lowers the voltage across the device in the path of the amplified current and ultimately reduces power dissipated by the device. However, switching losses of these devices are not as easily characterized or intuitive for power electronics designers. This is mainly due to the fact that the parasitic reactive elements are non-linear and not as readily documented as I-V characteristics of a given power device. For example, non-linear parasitic capacitances in the device are given for a fixed frequency across a voltage sweep. Parasitic inductance is typically not even mentioned in the datasheet.

The switching losses of these devices depend on these mysterious reactances. A functional way to obtain estimates of switching loss is to test the device under the conditions the device will be used. However, this task must be approached carefully in order to accurately measure the voltage and current of the device. Measurement devices also have parasitic impedances of their own that can add or subtract to switching energy during turn on or turn off and create misleading results. Preliminary testing was performed on multiple devices. After preliminary testing and deliberation, a device-measurement printed circuit board was made to easily replace switching devices of the same package.

This thesis presents switching loss measurements of medium-power capable devices in the tens of kW range. It also aims to attribute characteristics of switching voltage and current waveforms to the internal structure of the devices. The device tester designed is versatile since the output buffer of the gate drive is comprised of D-PAK totem pole BJTs. This is able to drive both current and voltage driven devices, i.e. SiC J-FETs (current-driven) and other voltage-driven devices (i.e. MOSFETs and IGBTs). It also allows for TO-220 and TO-247 packaged power diodes.

Acknowledgements

I would like to thank Dr. Jih-Sheng Lai for his generosity and willingness to help throughout my time at Virginia Tech. His knowledge and experience have been so helpful. Dr. Lai most certainly leads by example. As a result the Future Energy Electronics Center has been a great place to learn. Dr. Wensong Yu has also been very helpful with his advice and experience. His mechanical and electrical intuition are gifts that he is willing to share. I would like to thank Dr. Wayne Scales for his most excellent Electromagnetic Fields II lectures and notes. This class speaks of the foundations of electrical engineering and Dr. Scales conveyed the material in a tangible and intuitive manner. Thank you, Dr. Kathleen Meehan, for helping me imagine and think about what is going on with the devices I tested. It has opened up a different perspective of power electronics. Knowledge of devices is crucial to more efficient power electronics. Gary Kerr has extended his handy knowledge as well. His prototyping experience has been insightful and I will use them in the years to come. Thank you, Kim Medley, for your help in ordering the very much needed parts and boards for our lab.

I would also like to thank my parents, Dae Hyang Kim and Jung Ae Rho, for their support. The time and effort spent to nurture my interests is most appreciated. Thanks to my sister, Connie, as well for her guidance and advice.

Thanks to Thomas LaBella for your candid thoughts about electrical engineering concepts. Your insights and perspectives have been as helpful as they have been fun. Thank you, Younghoon Cho, for your guidance and advice on my academic and professional career. They say that imitation is the highest form of flattery and your DSPs and coding have proliferated and multiplied throughout the lab. Thank you, Hide Miwa, for sharing your sage-like experience and intuition; and also for discussions about packaging and design in general. Thank you, Chris Hutchens, for your shared excitement for electrical engineering, help with parasitic inductance simulations, and ballpark figures; as well as discussions about packaging and layout parasitics and theory in general. Thank you, Bret Whitaker, for your help and efforts throughout the lab. Thank you, Ben York, for your help with the active-clamp flyback when I first joined the lab and also letting me borrow your semiconductor books. Thank you, Wei-Han Lai, for helping me find equipment in the lab and sharing your experience. Thank you, Ethan Swint, for sharing your experience and answering questions I had about motors and other topics. Thank you, Nathan Kees, for your time in discussing the basics. Thank you, Jason Dominic, for asking questions and being curious; it's nice to see this inquisitive and open-minded nature. I would also like to thank all of the members of the FEEC for their combined help, support, and time.

I would like to thank Matthew Welch for helping me choose electrical engineering as my field of practice and his help and friendship throughout my undergraduate experience. I would also like to thank Michael Fraser, Josh Deng, John Caldwell, Preston Taylor, and Thomas LaBella once again for making the undergraduate experience all the more rewarding in electrical engineering. If I have forgotten to mention you; know that your time, effort, and perspective have been much appreciated.

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0. Motivation and Scope of the Thesis

The field of power electronics leverages low-loss switch-mode regions of device operation to convert input power to a desired output power efficiently. The low-loss regions of operation include rectification with low leakage-current in the device and conduction with low voltage across the device. The devices used for power electronics primarily include MOSFETs (Metal-Oxide Semiconductor Field-Effect Transistor) and IGBTs (Insulated Gate Bipolar Transistor), and less frequently involve BJTs (Bipolar Junction Transistor), JFETs (Junction Field Effect Transistor), MCTs (Metal-Oxide Controlled Thyristor), GTOs (Gate Turn-off Thyristor) and IGCTs (Insulated Gate Controlled Thyristor). Generally speaking, thyristors dominate the high power market, while IGBTs and power MOSFETs reign over the medium power arena. MOSFETs control the low power domain as well. Applications in the high-power region include power conversion for utilities, rail guns, and high power communication. Medium-power devices are used in inverters for alternative energy sources, motor drives, battery charging, and more. Computer power supplies, audio amplifiers, lighting, and power for small handheld electronics create demand for low-power devices [1,2]. For a more thorough overview of devices the Bose paper is highly recommended [1]. The product of the rectifying voltage and current conduction capabilities gives a rough idea of the power capacity of the device and the result is shown in many documents and books; the figure below is an example.

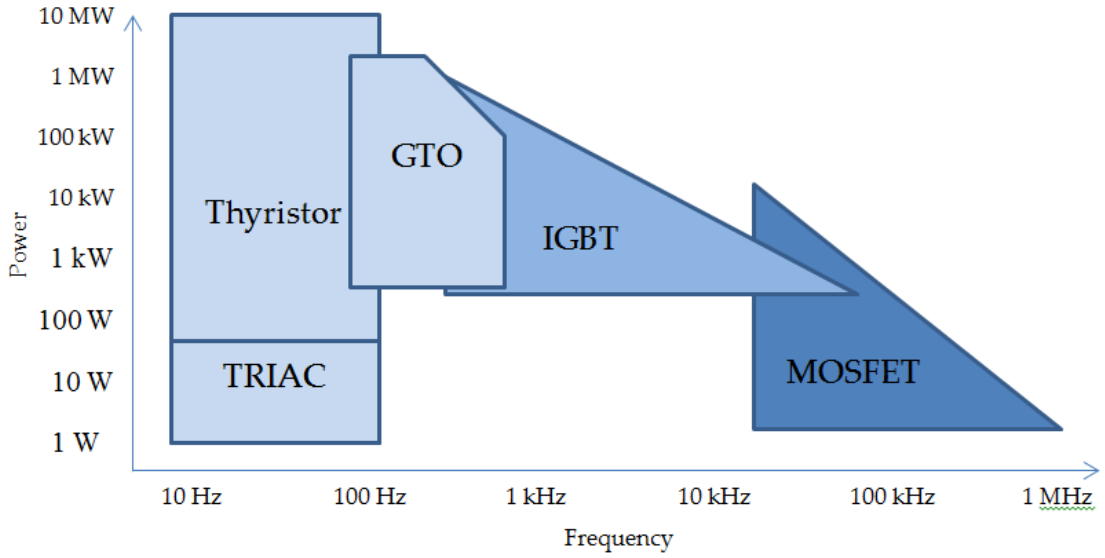

Figure 1: Typical power level and frequency of devices found in Electrical Engineer's Reference book [2], [3]

This thesis will focus on medium-power MOSFETs. Most medium-power switch-mode devices are MOSFETs and IGBTs. Both of these technologies approach low-loss switch-mode conditions in two different ways. The MOSFET commands a unipolar or majority-carrier attitude, while IGBTs advance with a bipolar, minority-carrier air. Bipolar and minority carrier devices inject carriers into regions where they are the minority charge carrier (n-type donors are injected into p-type acceptor regions and vice versa). To further generalize, field-effect driven devices are majority-carrier, unipolar devices and devices with minority carriers injected into majority-carrier regions (p-type carriers injected in n-doped area and

vice versa) are bipolar, minority-carrier devices. IGBTs can obtain lower conduction loss through a lower voltage across the device at higher currents due to its bipolar characteristic. However, at lower currents power MOSFETs generally incur lower power loss [4].

This thesis will focus on field-effect driven, majority-carrier devices. MOSFET structure has evolved to suit the need of power electronics. These structures come in two different flavors: lateral or vertical assemblies. Lateral devices direct current along the plane of the device or horizontally or laterally. Vertical devices create current normal to the plane of the device, or vertically. It has been stated that lateral devices have lower on-resistances and device capacitances. However vertical devices can sustain higher breakdown voltages and are easier to parallel and create larger devices. Super-junction technology has also allowed devices to rectify higher voltages and provide lower than previously expected Si-device resistance. The device geometries manipulate inherent device characteristics like terminal to terminal capacitances and device resistances. The processes in order to create these geometries vary and create varying device performances as well.

Wide-bandgap materials like GaN (gallium nitride) and SiC (silicon-carbide) are so appealing due to their wide-bandgap energies. Discoveries in material physics have stated that materials must possess a certain energy level in a given range of energy levels order to conduct and also another energy level in another range of energy levels to insulate, rectify or decrease the number of defects or broken bonds. The energy levels at which materials conduct fall into a certain conduction band or range of energy levels. When energy levels are in the valance band, the material maintains a molecular structure that is not significantly conductive. The difference in these two bandgap levels is called bandgap. Wide-bandgap materials have a greater difference in the conduction energy levels and the insulating energy levels. The greater distinction allows greater voltage-withstand capability, so thinner materials can be used instead. As a result device resistance can drop. Lower permittivity would allow lower device capacitances and faster devices.

Power electronics engineers strive for low loss and high power efficiency. The goal of this thesis is to evaluate switching loss of a benchmark MOSFET and competing devices in the 650 V 40-80 A range, as well as Cree's SiC 1200V 33A Z-FET. The device tester that has been developed uses a more mechanically stable and accurate voltage sensing technique with a BNC adaptor. It also allows universal device testing with TO-247 package MOSFETs as well as TO-220 and TO-247 diodes.

Thesis Outline

This thesis will achieve its goal through four sections; it will begin with a test setup description going into detail of equipment ratings, specifications, and requirements. It will follow with switching-loss measurement. Preliminary testing results will be presented. A PCB (printed circuit board) is designed to create more uniformity and quicker replacement of switches. The results of this testing setup will be presented. The document will then be summarized and along with conclusions from the data obtained and future work.

I. Test Setup

A block diagram of the setup can be seen in the following diagram and it will be explained from left to right and top to bottom. It is common practice for power electronics designs with a DC input to have a stiff DC bus. A stiff voltage source is a voltage source that allows significant current to be drawn without much change in voltage. Capacitors are devices with considerable voltage inertia and large capacitors are excellent candidates to provide stiff voltage sources; more time, movement of charge or both are required to change the voltage of larger value capacitors. The device-testing unit was composed of switching devices soldered together with copper sheets and later the copper was replaced with a PCB (printed circuit board). A high-voltage probe was used to measure the device voltage. The current in the device was first measured with a Rogowski current probe and then by a BNC (Bayonet Neil-Concelman) current shunt. The current was measured on the source pin with the Rogowski and in series with the source using the shunt. These devices were interpreted by waveforms on the oscilloscope.

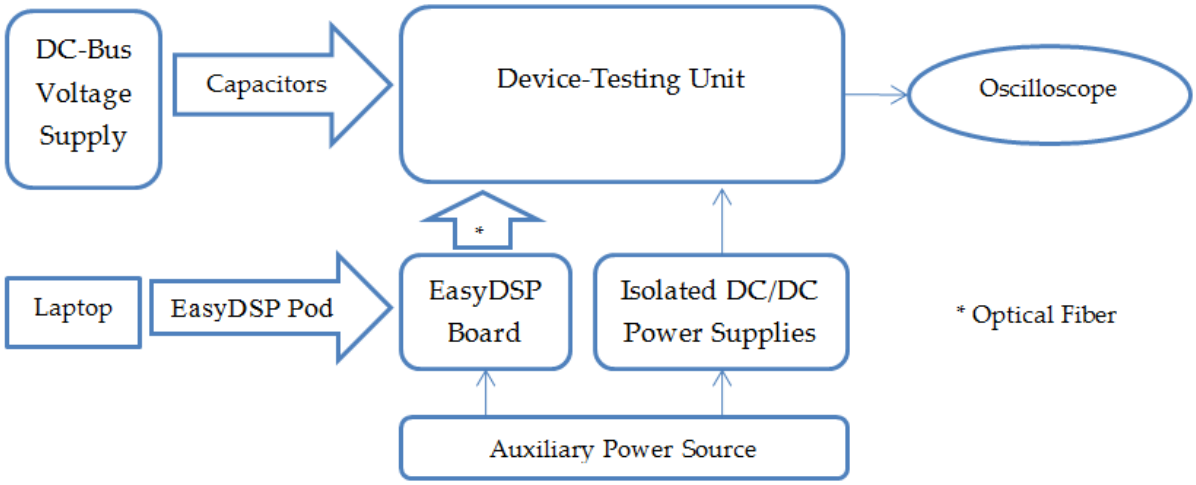

Figure 2: Device-testing setup block diagram

EasyDSP is a combination of software and hardware that allows the experimenter to change parameters in a DSP real-time through a laptop and EasyDSP pod. This allows the experimenter to change the duration of gating pulses and effectively set the device current. The easyDSP board contains the DSP and appropriate D/A (Digital/Analog) converters to provide the gating signal to a fiber-optic transmitter. This signal is provided to the device-testing unit with galvanic isolation. Fiber-optic gating has been used for safely operating high-voltage switches from relatively far away; the cable that was used is 5-m long. Previous device testing setups have had problems with common-mode noise due to circulating ground current [5]. This would cause the ground reference to look like it was oscillating around ground on the scope screen. To circumvent this problem the device-testing unit is isolated from the auxiliary power supply by fiber-optics and high-voltage isolated (low common-mode capacitance) power supplies.

The following is a description of the device-testing unit that was used to measure the device current and voltage in order to calculate switching loss. The freewheeling diode should ideally be a Schottky diode or ultra-fast recovery diode to remove reverse-recovery loss from interfering with the bottom-device

switching-loss estimations. Schottky diodes are majority-carrier and unipolar devices, so carriers do not have to move into complementary regions. As a result commutation time is much faster and reverse recovery does not exist in the Schottky diode. However, the junction capacitance will still oscillate with the other parasitic reactances.

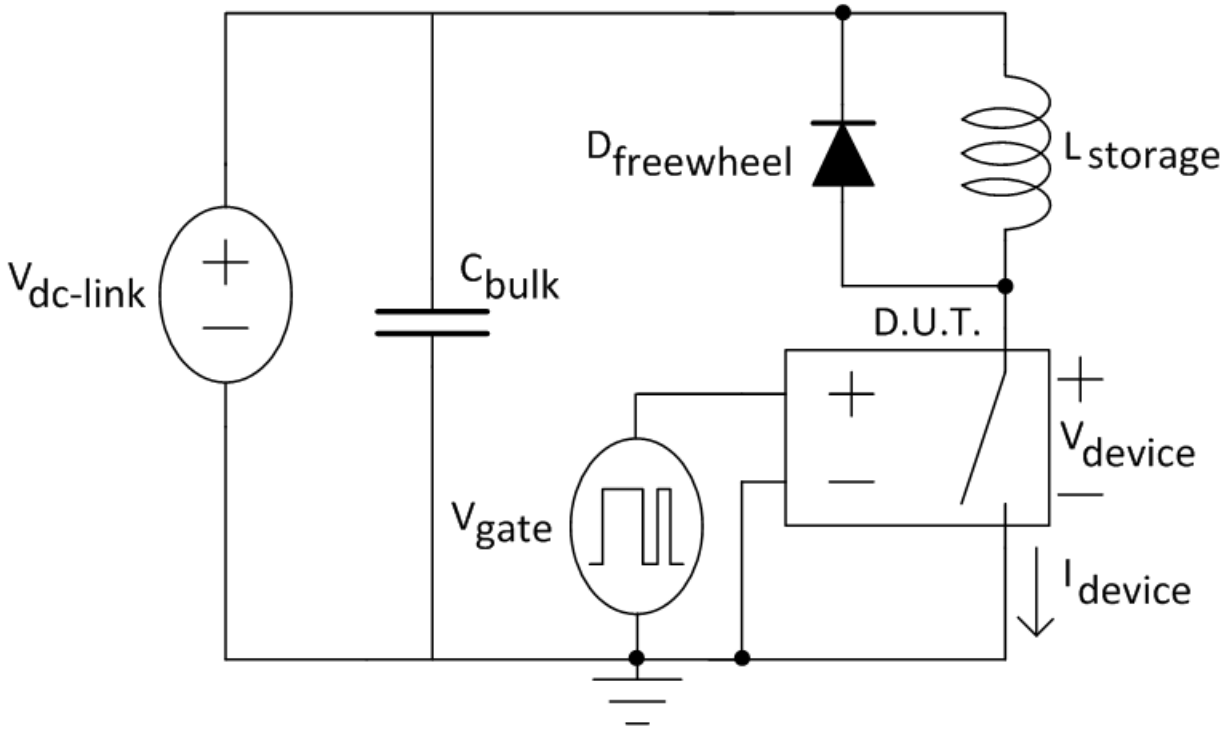

Figure 3: Device-testing unit circuit

The storage inductor sizing will be discussed below after explaining circuit operation. The dc-link voltage was picked to be about 50-80% of the device rating, which is a typical derating when choosing a device. The voltage source must be connected to the circuit of interest and this connection inherently contains a parasitic inductance. This small inductance combined with a large change in current in a short amount of time will cause a large voltage spike on the dc-link bus when the device turns off. Therefore a bypass capacitor with low inductance should be placed at the cathode of the diode and at the source of the

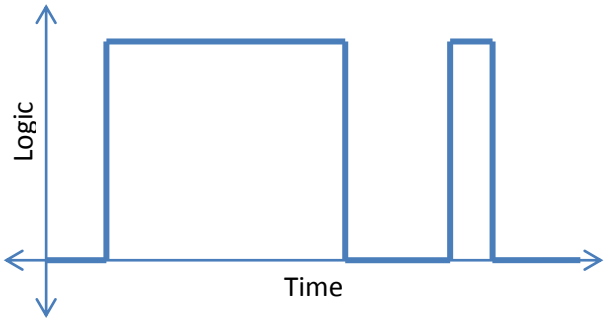

Figure 4: DSP-generated logic

MOSFET. Vishay's Orange Drop or AVX's FFB polypropylene capacitors can be used for this purpose. Without these considerations, the device voltage will have a large overshoot when it is turned off and decrease the device's safety margin. These following waveforms are not drawn to scale in order to emphasize certain points. The gating signal will be explained to further the explanation of the test setup.

When the device is turned on, current will rise through the inductor at a rate of the dc-link voltage divided by the inductance of the storage inductor ($V=L\left(\frac{di}{dt}\right)$) . Once the current rises to a predetermined level, the device is turned off. The inductor will not allow current to change its state of inertia quickly; as a result the voltage across the inductor will reverse in sign or commutate and passively turn on the freewheeling diode. Current will circulate only through the diode and inductor while the device is off. Since there is parasitic resistance in this circuit, the energy will dissipate as heat during this off time and current will decrease. The desired behavior of the storage inductor is to act as a current source of a predetermined level. So the off state should be kept to a minimum to keep the current from varying from the preselected level.

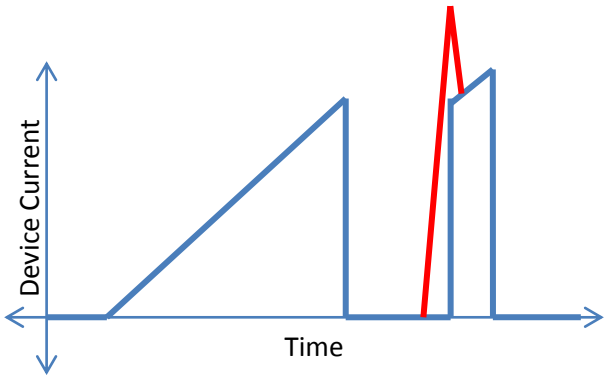

Figure 5: Device current as an effect of generated logic

The following pulse will reverse bias the freewheeling diode and passively turn it off. Due to semiconductor physics and the bipolar nature of the diode, time is required for minority charge carriers to return to their respective majority regions. During this time the diode is still continues to conduct and current will flow in the cathode to anode or reverse-biased direction. This period is called reverse recovery time and will be presented in captured waveforms. This trait is shown in red above and is undesirable since it creates more stress for the device under test, resulting in less reliable operation. A fast recovery diode or Schottky diode can minimize or eliminate this problem and cause less distortion to the duty cycle. The reverse-recovery effect can be shown to lengthen the on-time of the device by delaying device turn off.

The length of the second on time should also be as short as possible. Otherwise the inductor will continue to magnetize and increase current and again deviate from the preset current. This double pulse does repeat itself, but not until a considerable amount of time has passed to let the current in the inductor

dwindle to 0 A. The value of the inductance should be as high as possible to keep the slope of the current as low as possible. This will result in behavior that is more identical to a current source. The tradeoff is that higher inductances can make cores more susceptible to saturation at a given current. In addition, the time it takes for the current to dissipate will be longer.

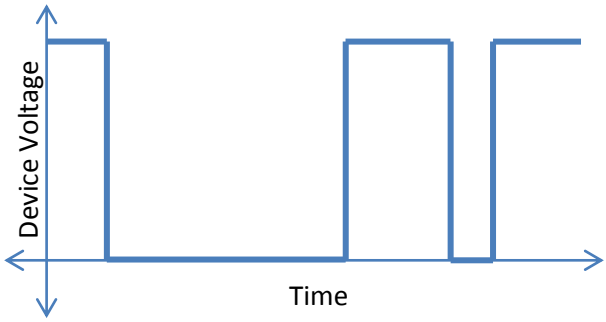

Figure 6: Device voltage as an effect of generated logic

In summary the first pulse to turn on the device is long enough to pump the current up to a preselected level. The following off period is short to sustain the current. The final pulse is short as well for the same reason. The final off time is used to allow current through the inductor to drop back down to zero. The second pulse is used to obtain turn-on and turn-off switching loss of the device.

The information of the second pulse can be shown below. This diagram is focused on the second current pulse. The current pulse can be shown in red, while the voltage is shown in blue. This diagram is not to scale either and emphasizes the stressful transitions where device voltage and current are both non-zero.

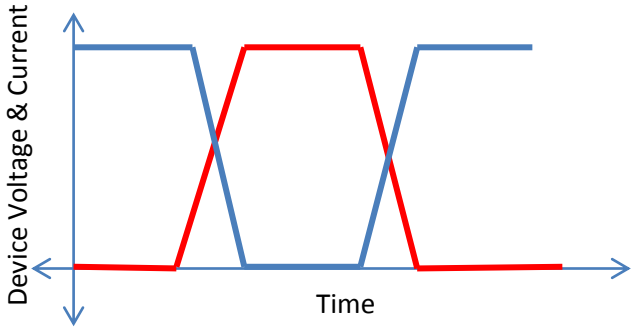

Figure 7: Diagram of switching loss; red is current and blue is voltage

The product of the current and voltage measured during this pulse is used to find instantaneous power of the switching loss. A trapezoidal Riemann sum of the instantaneous power is then used to calculate the area under the instantaneous power, resulting in energy loss in Joules. The LeCroy 6030A oscilloscope

was employed along with a 5-kV rated voltage probe and a Rogowski current probe to capture current and voltage during preliminary testing.

Detailed Explanation of Device-Testing Unit Operation

This explanation will begin with the basic circuit. The DC bus voltage will be tested from about 17% to 67% of the breakdown voltage rating of the MOSFET. In this case it is 100 - 400 V. The bypass capacitor is actually in parallel with many large capacitors to sum to 5 mF.

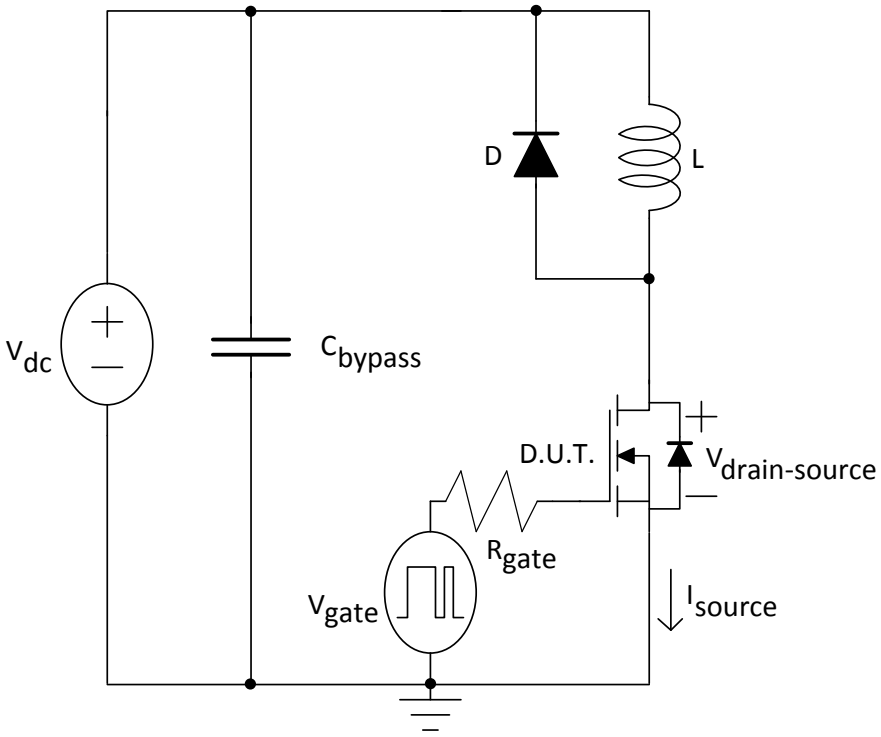

Figure 8: Device-testing unit with drain-source voltage and source current measured

To further the explanation of this circuit, a useful model including parasitic components of the MOSFET is shown below. The letters d, g, and s stand for drain, gate, and source respectively. The capacitances of the MOSFET are physical attributes of the semiconductor die. The inductances mostly come from the leads that attach to the die. This can include wire bonds, copper straps, thick copper, and other connections. The circuit will first be explained with the capacitances. Parasitic components are shown in grey, current paths are red, and element voltages and commutating polarities are shown in blue.

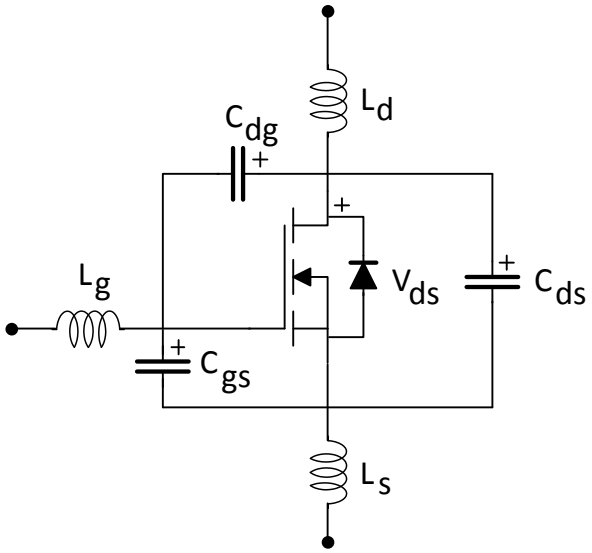

Figure 9:MOSFET model with practical parasitic impedances

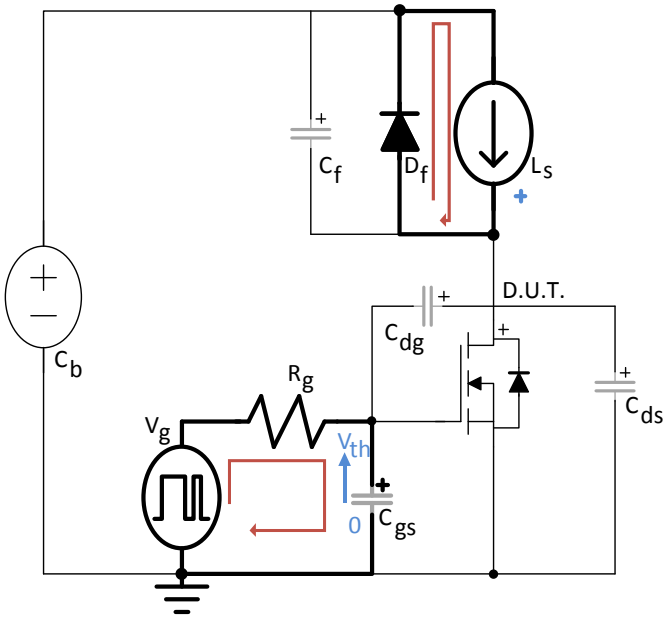

Figure 10: Charging the MOSFET when it is rectifying; components in lighter color are parasitic components

C_b can represent all of the capacitors in parallel with the V_{dc}. It is assumed that this capacitance is much larger in magnitude (C_b is a couple mF and the other parasitic capacitors are in the nF and hundreds of pF range or 6 to 7 orders of magnitude less) than any other voltage-inertial element. With this assumption it will be treated as a voltage source. The storage inductor will be under the same assumption (it is about 833 µF, while the parasitic inductors are in the tens of nH range or 4 to 5 orders of magnitude less).

It is assumed that both large sources have been energized. C_b is energized to 400 V and L_s has 20 A of current. Typical gate voltage maximums are about 20 to 30 V, so the logic high can be 15 V and the logic low can be 0 V. The MOSFET has been turned off for a while and is rectifying the entire 400 V. The

antiparallel freewheeling diode, D_f, is placed to create a path for current when the MOSFET is off or rectifying. To turn on the device the gate is driven to logic high and C_{gs} begins to charge to the threshold voltage of the MOSFET [6].

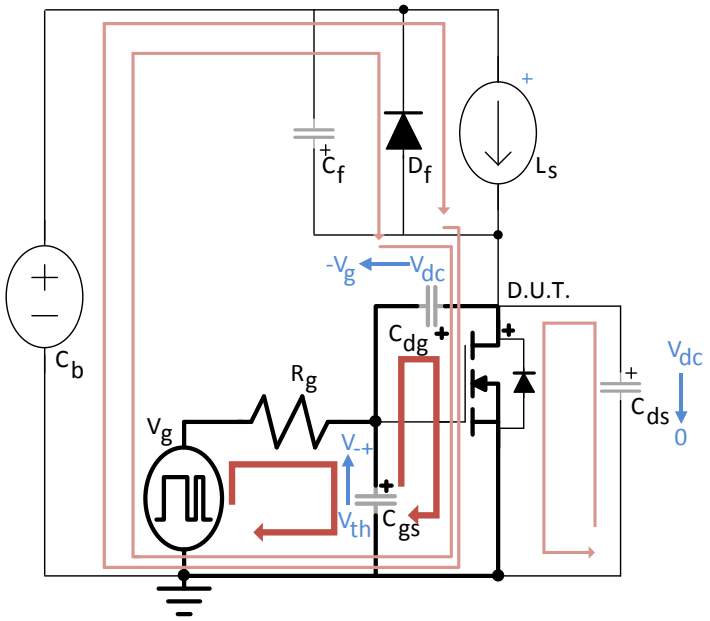

Figure 11: Charging Miller effect

Once the threshold voltage is reached, lots of current paths appear and some capacitors begin to charge and discharge. C_{dg}, or the Miller capacitance, has been fully charged and must discharge as the gate is charged. This pair is in conflict. This conflict is exacerbated by the large voltage swing across C_{dg}.The formula $I = C\frac{dv}{dt}$ can emphasize the point being made. Since the dv is 415 V and the dt ~ 1-10ns the Miller current will slow the current that charges the field-effect capacitance,C_{gs}. Since only a small amount of current is present in the C_{gs}, the voltage rise will also slow down enough to look like a plateau before C_{dg} completely commutates and charges to $-V_g$.

Since the device threshold voltage has been reached, a channel will form from source to drain and current will form in the device as shown in Figure 14. The inductor will commutate as a result of a falling current and reverse-bias the diode. If D_f has poor switching characteristics, current will shoot through the power diode and switch. This is one of the reasons why the extremely fast-switching characteristics of Schottky diodes are so desirable in power electronics. This is also why C_b should be relatively large. A large capacitance will not allow the DC supply to instantaneously short. D_f will recover and commutate. The junction capacitance of this diode can help describe this process. Once the junction capacitance charges up to $-V_{dc}$, the diode will fully rectify with the exception of usually negligible leakage current.

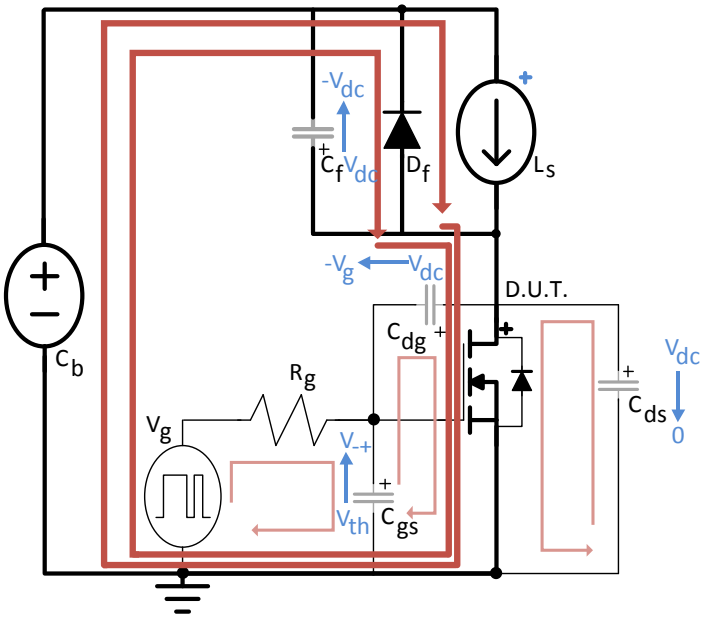

Figure 12: MOSFET turn-on and device current rise

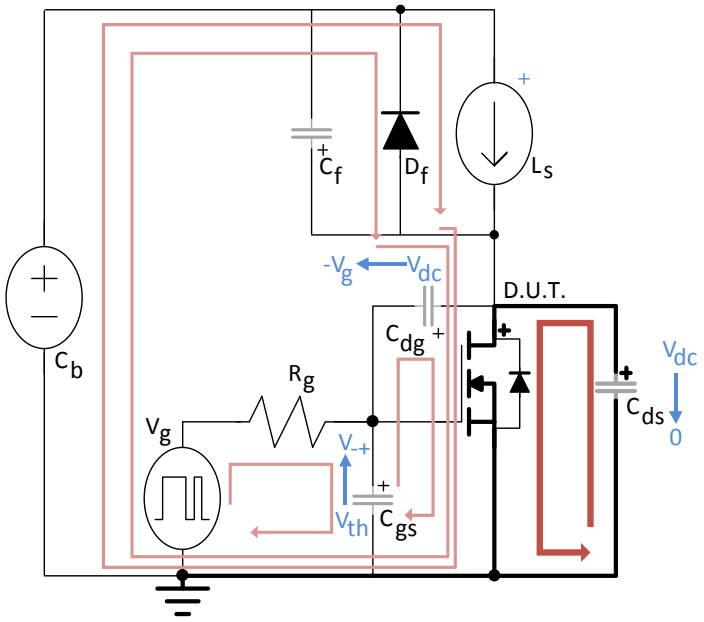

Figure 13: Device turn-on loss

C_{ds} has been charged to the dc bus and that energy will dissipate as heat in the switch. This is the minimum turn-on energy loss. Other contributions of turn-on loss include the shoot-through reverse current from the poor diode. The Miller capacitance is also in the path of the device, so its energy must also be dissipated by the switch. Since internal current is flowing through the channel and C_{ds}, it cannot be measured downstream after the source. This results in an underestimation of the switching loss of the switch as mentioned by Chen [6].

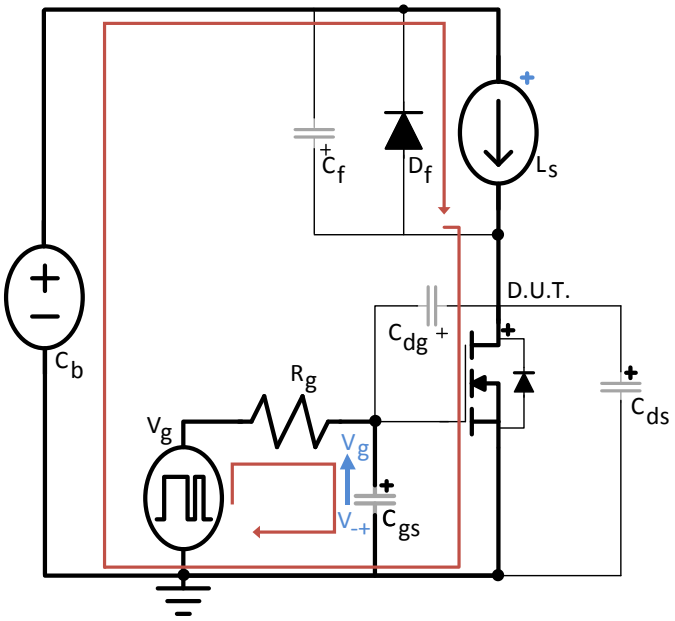

Figure 14: Optimized R_{ds} reached

Once the Miller capacitance has discharged, the gate can reach V_g and the device can reach its minimum R_{ds} and fully conduct.

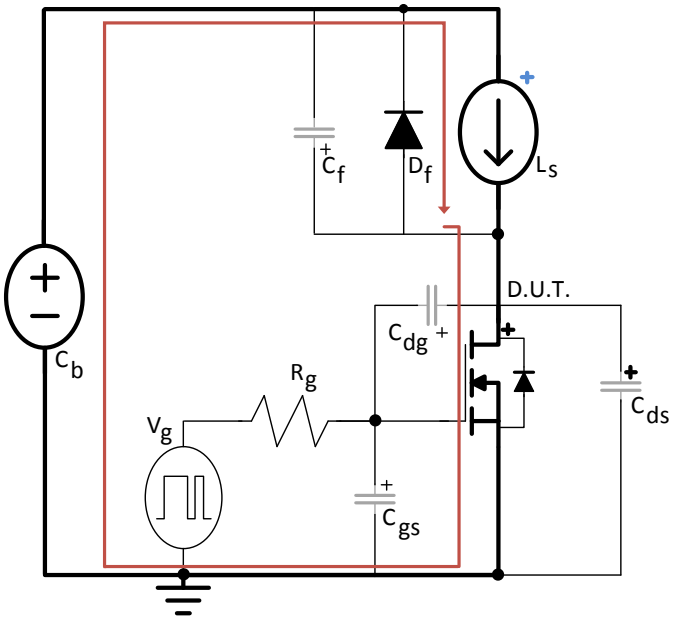

Figure 15: Full conduction

The device must eventually turn off and will follow the process starting with Figure 18.

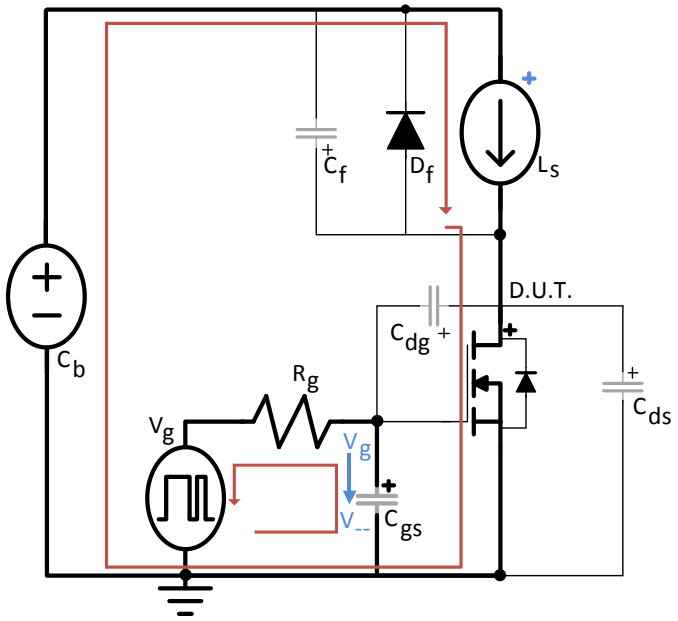

Figure 16: Gate discharge

Gate voltage drops toward 0 V and C_{gs} begins to discharge.

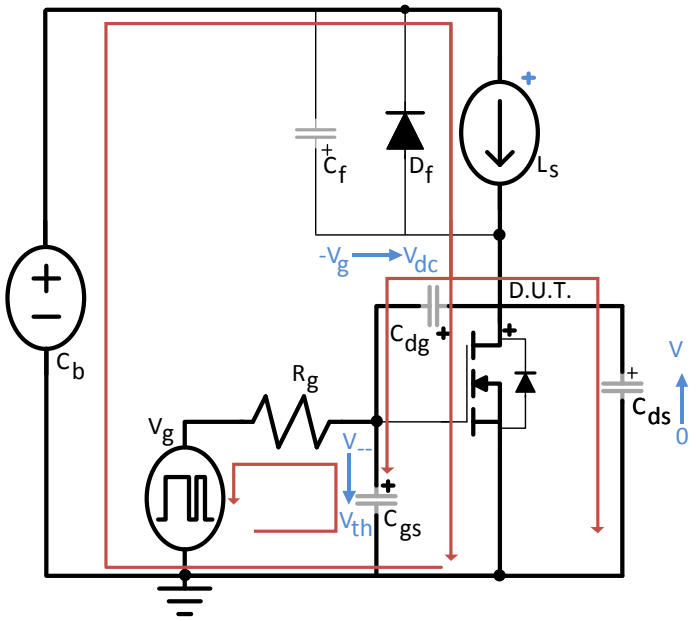

Figure 17: Discharge Plateau

The Miller capacitance must now charge from $-V_g$ to the dc voltage. This causes another slowdown in the gate voltage rate of change. The gate voltage comes to another standstill and creates another plateau.

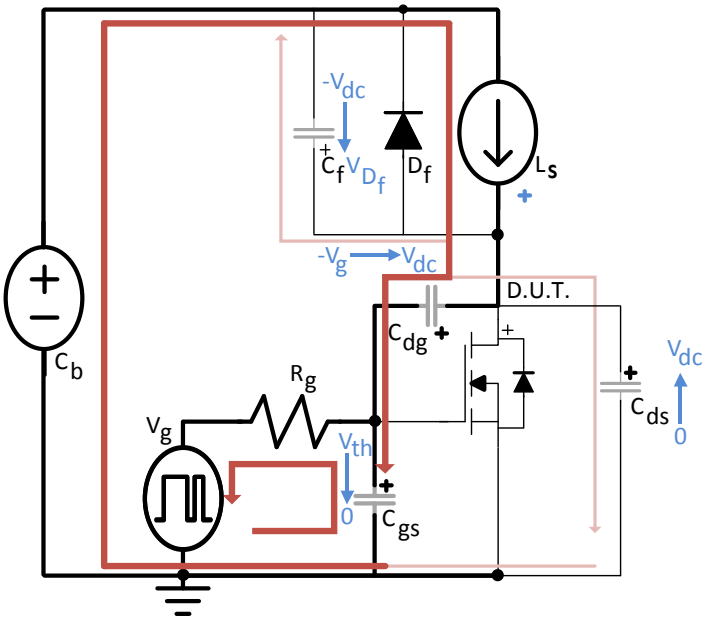

Figure 18: Discharging Miller effect

The device turns off since the threshold voltage has been breached. The current slows down and the inductor voltage reverses once again. Current must find a path, so it first charges the Miller capacitance.

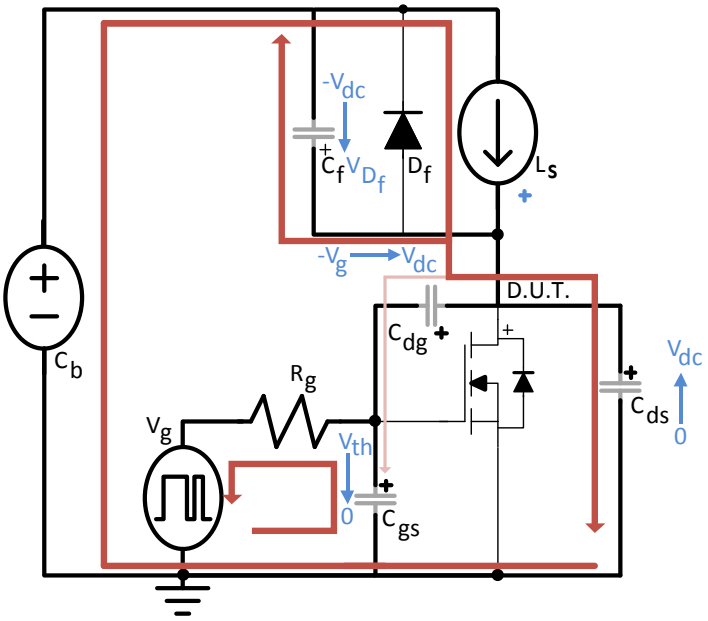

Figure 19: Diode commutation and C_{ds} energization

The Miller capacitance is fully charged so the gate can freefall to 0V, naturally limited by its own RC circuit of course. The commutation of the inductor forward biases the freewheeling diode; however, its junction capacitance must discharge. C_{ds} energizes once again.

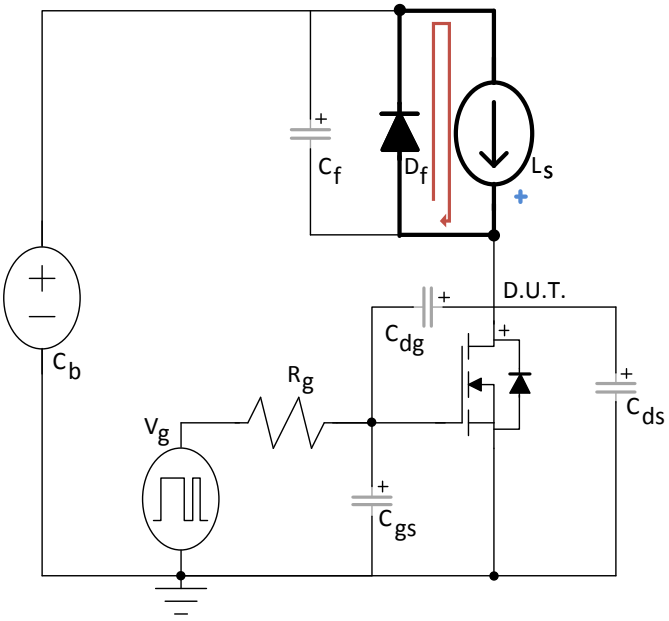

Figure 20: Full rectification

The device is now fully off and the inductor freewheels its current with the diode once more. This has been an explanation of the turn-on and turn-off processes of a MOSFET with only parasitic capacitance. This was to ease explanation of the circuit and provide some intuition. Inductances just add oscillation with the device capacitances, extra delay, and some negative feedback like the Miller capacitance.

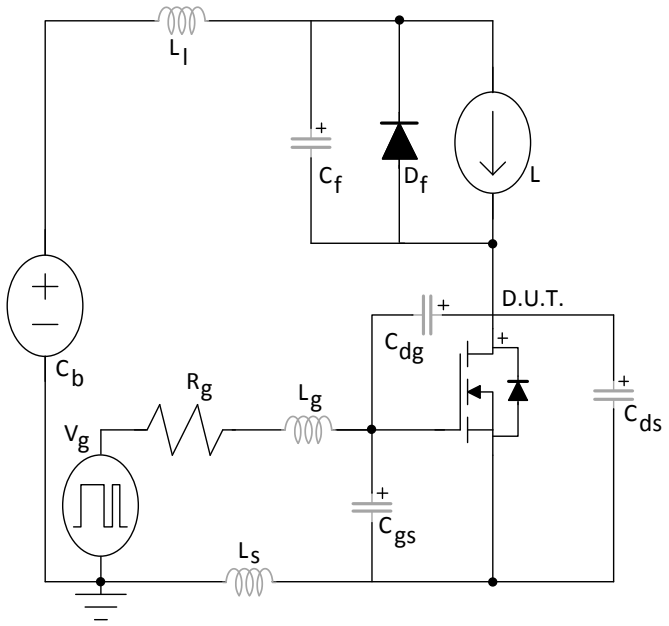

Figure 21: Device-testing unit with parasitic inductances

The package inductances includeL_s, L_g, L_d. L_l represents the high-current loop inductance. This lumps together L_d, connection inductance (PCB traces or other connections), and the ESL (effective series inductance) of the capacitors.

Voltage Probe Calibration

It is important to keep the voltage probe calibrated. This is easily accomplished by using the calibration tab on the oscilloscope. Measuring this point should result in a 0-to-1 V peak square wave and the results can be seen below.

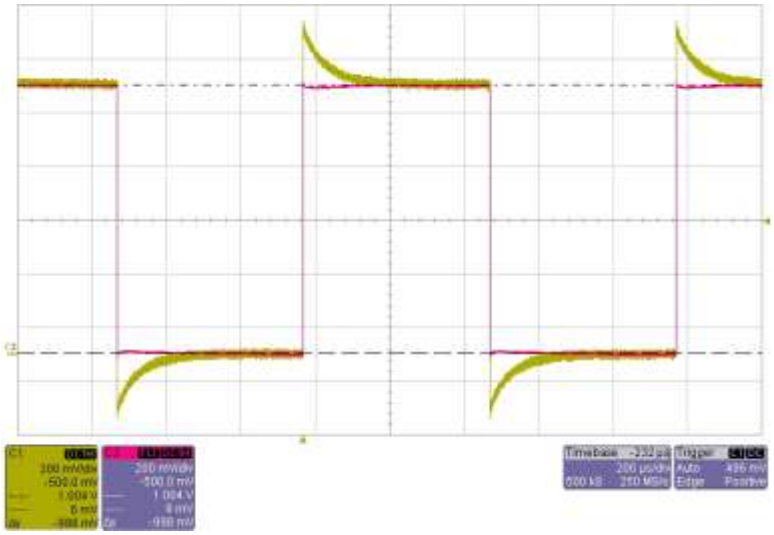

Figure 22: Uncalibrated voltage probe is shown in yellow and calibrated probe is shown in red at 200mV/div. and 200µs/div.

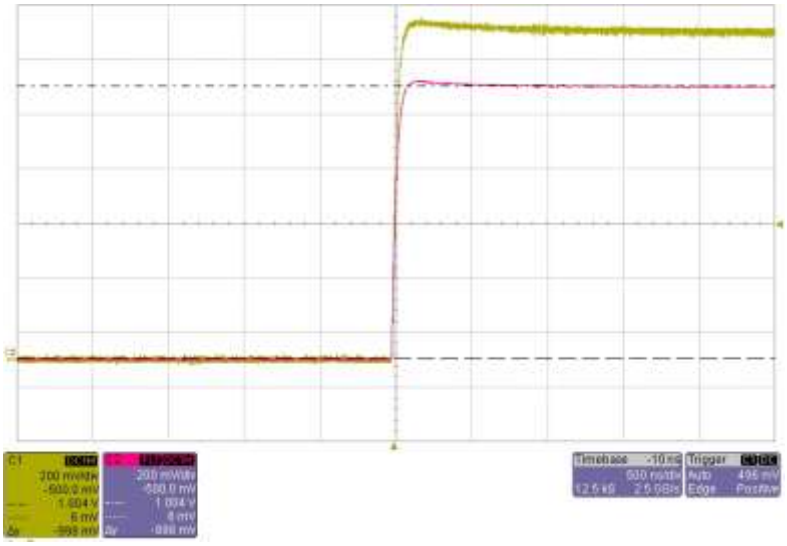

Figure 23: Uncalibrated voltage probe is shown in yellow and calibrated voltage probe is seen in magenta at 200 mV/div. and 500 ns/div.

Both channels are measuring the calibration tab on the oscilloscope. Channel 1 is uncalibrated and shows a 20% overshoot that takes 200 μs to reach a steady state. Since the square wave is 0-to-1 V peak, the experimenter can just multiply this waveform by the dc-link voltage to estimate what the measurement will look like. That is the measurement across the device can be up to 1.2 times the voltage that is actually present across the device. At a voltage of 600V, this is 120V more than expected! This could easily overestimate switching losses and if the probe is over damped, then switching losses can be underestimated. Therefore a properly calibrated voltage probe is necessary for accurate loss estimation. Adjusting screws where the probes meet the scope allows the experimenter to adjust the damping of the probe.

Even among non-isolated probes there are variants. A 5-kV rated voltage probe was used in this case to measure the device voltage, since the next lowest voltage rated probe was rated at 600 V. The specifications of the probes are shown below and are taken from LeCroy's datasheets on their website [6], [7]. Further explanation of the parameters can be found in Application Note 016 [8] on LeCroy's website.

	5-kV Probe (PPE 5 kV)	600-V Probe (PP005)
Resistive Divider Ratio	100:1	10:1 ± 1%
Bottom Resistance of Resistive Divider, MΩ	50	10 ± 1%
Input Capacitance, pF	<6	11 ± 0.5
Bandwidth (-3 dB), MHz	400	500 typical

Table 1: Probe Specifications

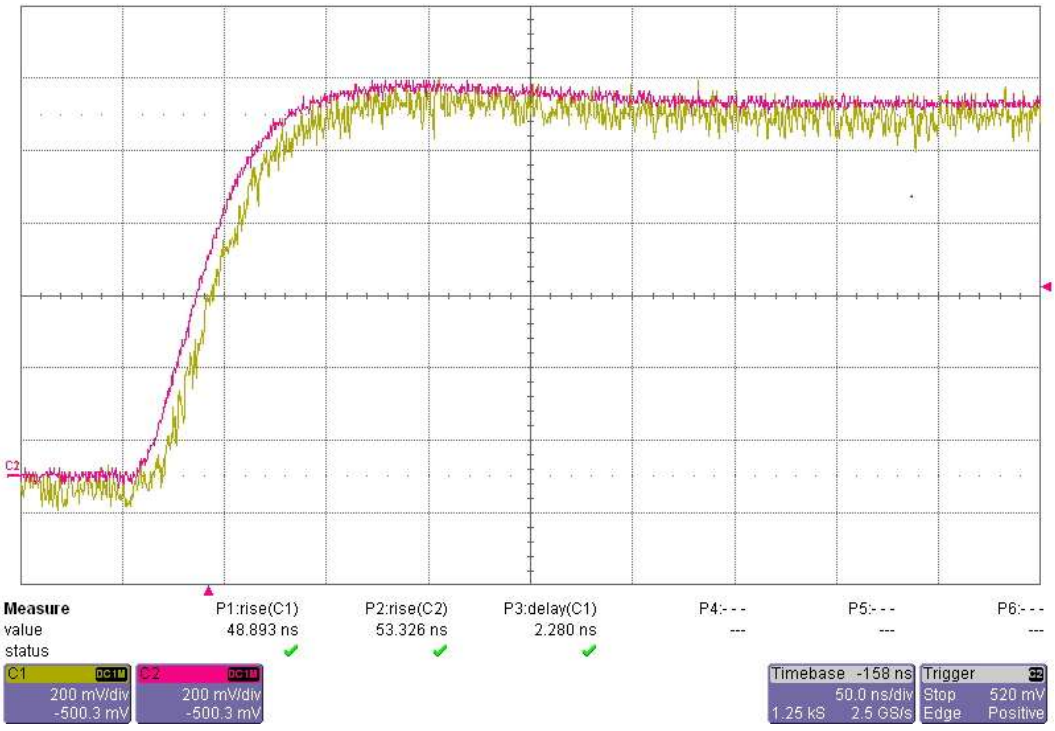

Figure 24: Rise time comparison of 5-kV probe (magenta) and 600-V probe (yellow)

Both probes have been calibrated to see the differences in time response between the two probes. Rise time was similar for both probes. The 600-V probe is shown in magenta and the 5-kV probe is shown in yellow. Rise time was about 50 ns, either probe could be ahead by 1 or 2 ns; however, the 5-kV was usually faster. Rise time is harder for the scope to accurately calculate since the noise is larger with respect to the signal. Noise appears to be about 80 to 100 mV for the 5-kV probe, while the noise on the 600-V probe was about 40 mV. Also, the experimenter noticed more offset changes as the voltage scale was adjusted. For example the signal low would appear to be at 0 V at 500 mV/div for the 5-kV probe, but at 200 mV/div some negative offset appeared as shown below. The 5-kV probe also has a delay of about 1-2 ns.

The fall time comparison can be seen below. Similar results were found for the fall time.

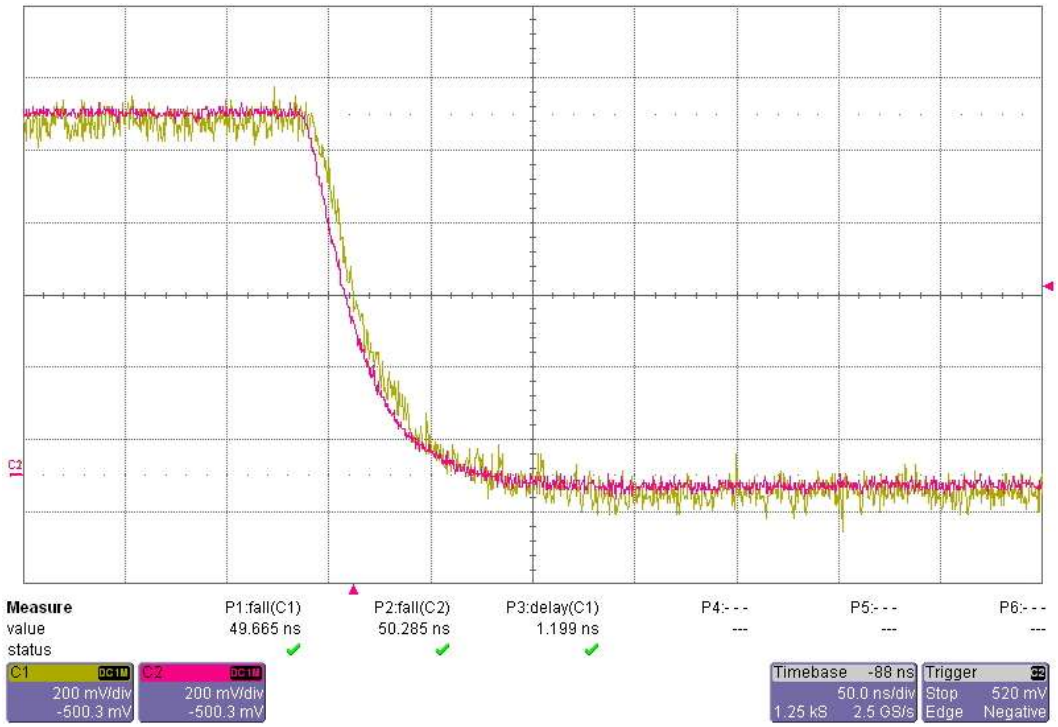

Figure 25: Fall time comparison of 5-kV probe (magenta) and 600-V probe (yellow)

Current Measurement Analysis

Current throughout the preliminary section was measured with the Powertek CWT03, a Rogowski current probe. The Pearson current monitor model 411 was used as a comparison to analyze the Powertek's performance. The results can be seen in the figures below for a 15-A square wave driven by the CoolMOS. Please note that the test setup must be altered to accommodate the Pearson current monitor. Additional circuit inductance had to be added, so more pronounced and sustained ringing is present on the waveforms.

The Pearson current monitor is about 10-40 ns faster than the Rogowski current probe. However, the Rogowski current waveform is consistently longer than the Pearson. It can also be seen that the turn-on

current is negative for a short period of time with the Rogowski. This does not occur for the Pearson. Another difference is in the turn-off current. The Rogowski current probe measures an increased spike in current when the device turns off. The Pearson does not see this current at all; however, it experiences a higher magnitude in ringing, once the device is off.

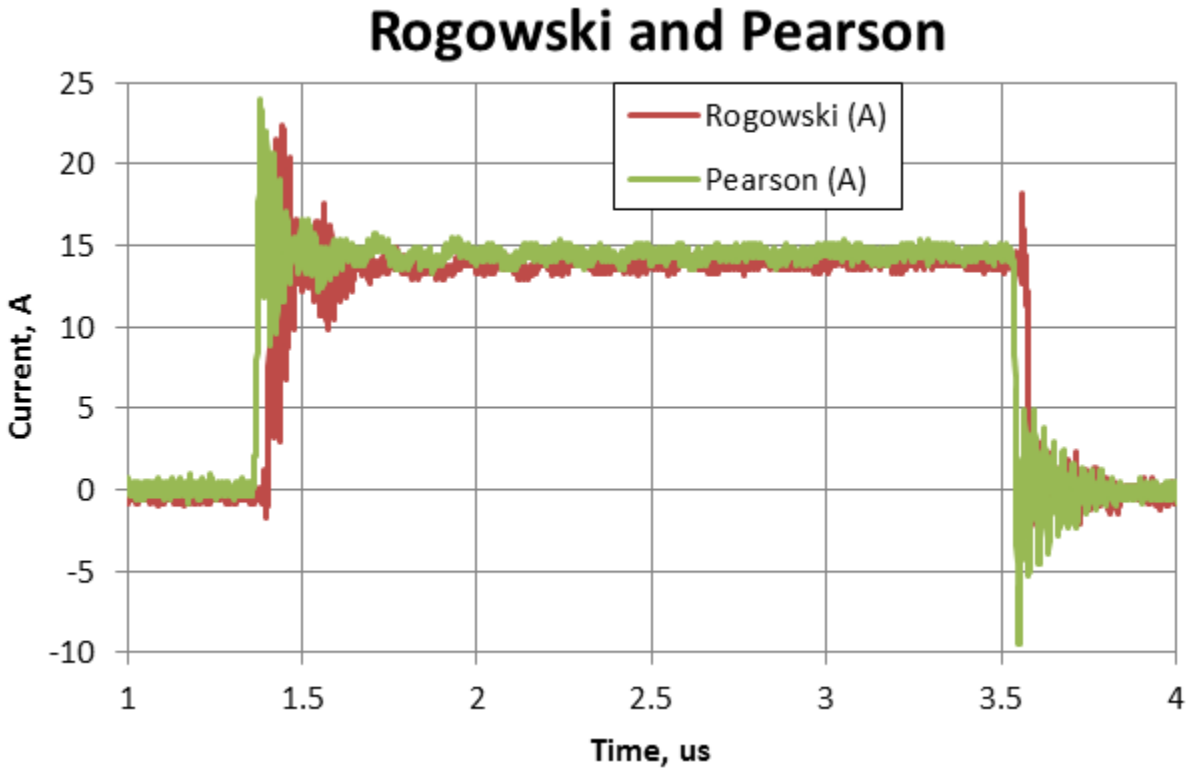

Figure 26: Rogowski and Pearson current measurement comparison

The Rogowski current probe shows larger oscillations and is delayed about 30 ns.

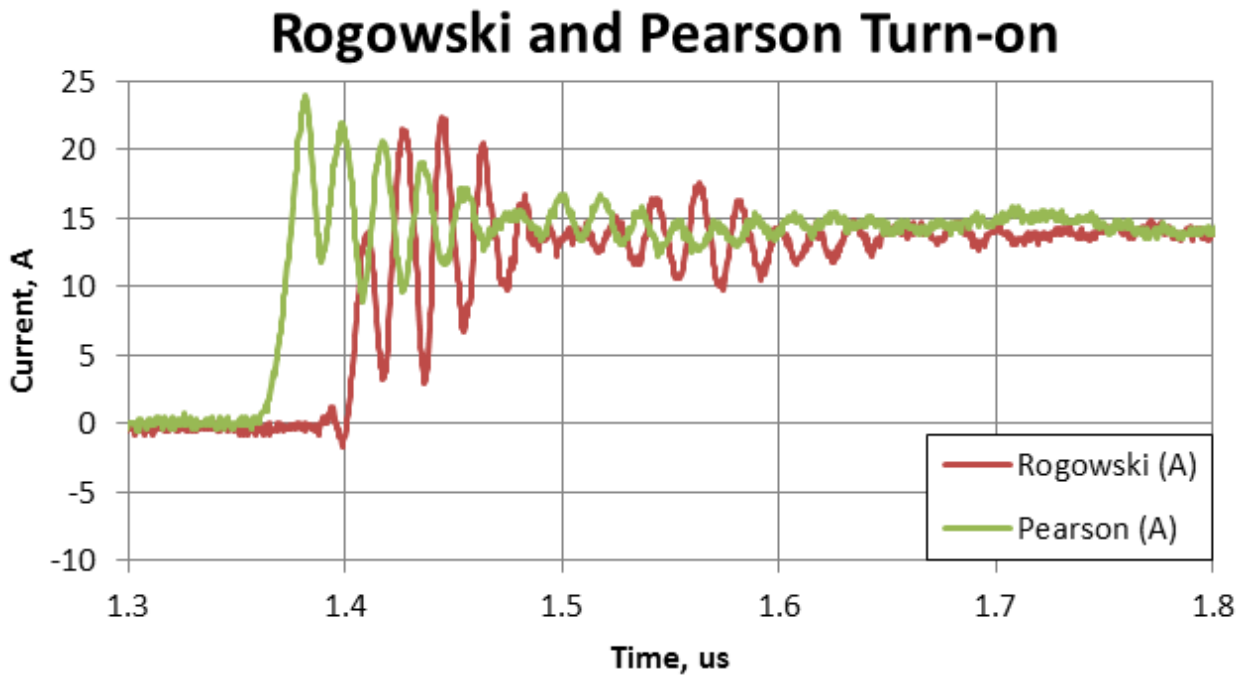

Figure 27: Turn-on current of Rogowski and Pearson current porbes

The turn-off current appears to look similar.

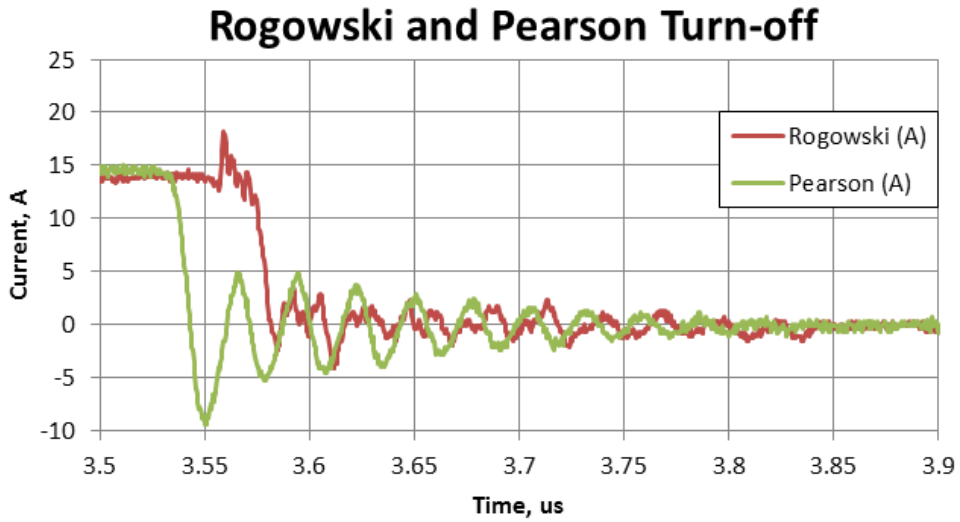

Figure 28: Turn-off current comparison of Rogowski and Pearson current probes

The Pearson current transformer has a faster transient response as seen in both graphs. The Rogowski lags Pearson current measurement from about 10 to 40 ns. Also the information conveyed by each probe is not without conflict. The Pearson shows larger ringing at turn-off current, while the Rogowski shows larger ringing at turn-on current. The Rogowski also expresses a turn-off spike that is not shown on the Pearson. The Pearson is not implementable without increasing test setup inductance and cannot be

practically used in device testing. However, Cree has used it in their experimental setup with an additional but smaller current transformer in order to eliminate the added inductance [10].

The delay of the Rogowski and the non-sinusoidal result, especially seen in the turn-off figure, indicate that the Pearson is the better current monitor. The ringing should be somewhat sinusoidal since only parasitic inductances and capacitances are involved to contribute to the ringing. There should not be so much distortion or increased harmonic content.

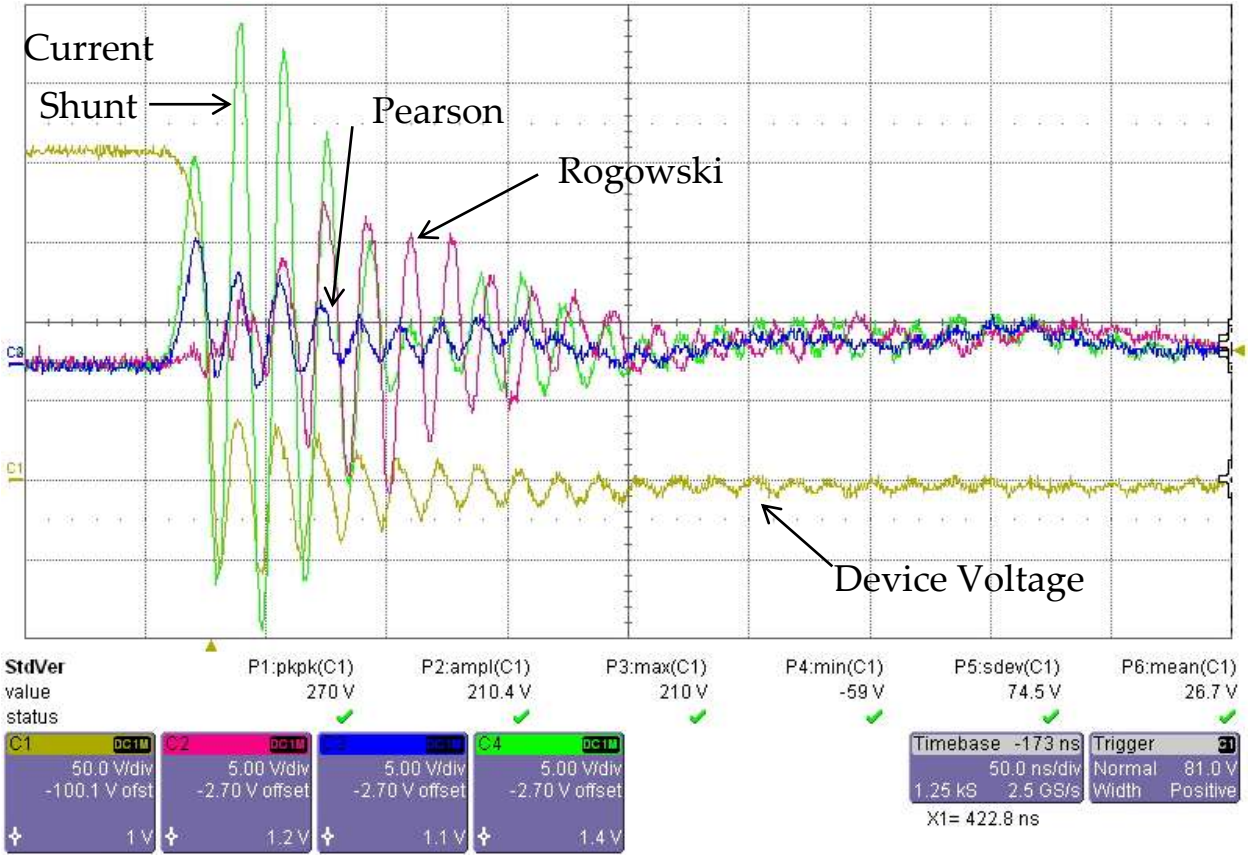

Figure 29: Current measurement comparison of the current shunt, Pearson current transformer monitor, and Rogowski coil measurement

An experiment was run to measure current from the CVR (current view resistor or current shunt), Pearson, and Rogowski. The result can be shown above. The homemade test setup increased circuit inductance which made it difficult to keep the MOSFET under the avalanche breakdown voltage. This is why the waveform is shown at 200 V with little current.

Switching-Loss Measurement

Switching-loss measurement and analysis was performed by saving waveforms from the oscilloscope and importing the time and amplitudes of the device voltage and current into Excel. Raw data from the oscilloscope contained offsets for device voltages and currents. The device voltage and current contained

these offsets most likely due to limited resolution of the sensed parameters. It is assumed that higher voltages and currents would cause greater offsets. The offset can be seen in the raw data shown below. The conduction and rectifying regions of operation were not areas of interest in this thesis, so the conduction region and rectifying region of operation was averaged and subtracted to set these conditions to zero. The instantaneous power is then calculated by multiplying current and voltage. This is then summed and divided by the sampling rate to find the trapezoidal Riemann sum, and ultimately the energy of the turn-on and turn-off loss. This allowed the turn-on loss and turn-off loss of a MOSFET to be clearly seen in an energy calculation as shown in the following PSIM simulation results. In theory the device should have an energy loss graph with four general slopes. There should be a small slope where leakage current and rectified voltage create negligible loss. A larger slope while the device is saturated with a slope of $R_{DS\,on}$. Two large slopes should also exist for turn-on loss and turn-off loss. However, in practice these slopes are not as clear especially during low sampling periods and ringing due to circuit parasitics.

List of Equipment

- Measurement instrumentation
    - LeCroy 6030A 350 MHz 2.5 GS/s Oscilloscope
    - PPE 5-kV voltage probe
    - Rogowski current waveform transducer CWT 3B UM
    - Pearson current monitor Model 411
    - SDN-414-10 CVR (current view resistor or current shunt) 100 mΩ

- Gate signal information
    - EasyDSP Pod
    - EasyDSP Board
    - Laptop with EasyDSP software
    - 5-m fiber-optic cable

- Device testing unit
    - Inductor bank – 8 inductors 833 μH, 65 mΩ, 50 turns of wire on 6 parallel C058195A cores
    - Capacitor bank – 8 capacitors (4x2 PEH200OO427AMBA 5 mF 840V total)

- Devices to test

- Power supplies
    - Fisher Biotech FB452 (0 – 800 V low current power supply)
    - Tenma 72-6905 (Quad output power supply)

- Thermal equipment

- Fluke II thermometer with thermocouple
- Fluke Ti40 thermal camera
- Proheat PH-1100 heat gun
- Copper sheets and Kapton tape

II. Preliminary Device Testing

Preliminary switch-loss testing included taping up sheets of copper with Kapton tape and assembling devices together to create low parasitic inductances. Also 20 mil thick sheets of copper were used to connect a 50 μF capacitor to test setups including ultrafast recovery or Schottky diodes and the device under test.

Figure 30: Vishay GLI capacitor with CoolMOS and ultra-fast EPU06 diode and Vishay Orange Drop bypass capacitor

Switching energy loss has been studied for four devices. The following tests were accomplished in order to get a feel for the testing procedure and also to gain a reference of switching loss of large and small devices. One IGBT, two MOSFETs, and a normally-off SiC superjunction transistor have been tested. The 60R045CP is a superjunction device from Infineon's CoolMOS series. It is rated for 650V and 60A and can

be considered as a benchmark device. Breakthroughs in superjunction technology have allowed devices to break the silicon device resistance minimum, allowing for greater breakdown voltages and higher current-handling capabilities; which ultimately increasing the operating range of the device [9]. Infineon also makes the FZ200R65KF1, an IGBT rated at 6.3kV and 400A at room temperature; this device is used to demonstrate the importance of Schottky diodes. Cree has made a new SiC MOSFET rated at 1200V and 33A. GeneSiC has created an IGBT packaged with a SiC antiparallel diode. GeneSiC has also created an interesting SiC normally-off superjunction JFET transistor variant rated at 1.2kV and 10A. Some device ratings and specifications can be seen in the table below.

	A-GA10JT12	IPW60R045CP	CMF20120D	GA100XCP12-227	FZ200R65KF1
Breakdown Voltage, V	1200	650	1200	1200	6300
Maximum Device Current, A	10	60	33	100	400
Total Gate Charge, nC	Not listed	150	90.8	400	2800

Table 2: Device characteristics at 25°C, except for GA100XCP12-227 current (105°C)

The importance of silicon carbide is that it provides up to 100-200 fold reduction in on-resistance and higher achievable breakdown voltages according to Baliga [3]. He also states that the advent of the IGBT and advances in different semiconductor chemistry may cause a second electronic revolution allowing higher power conversion efficiency.

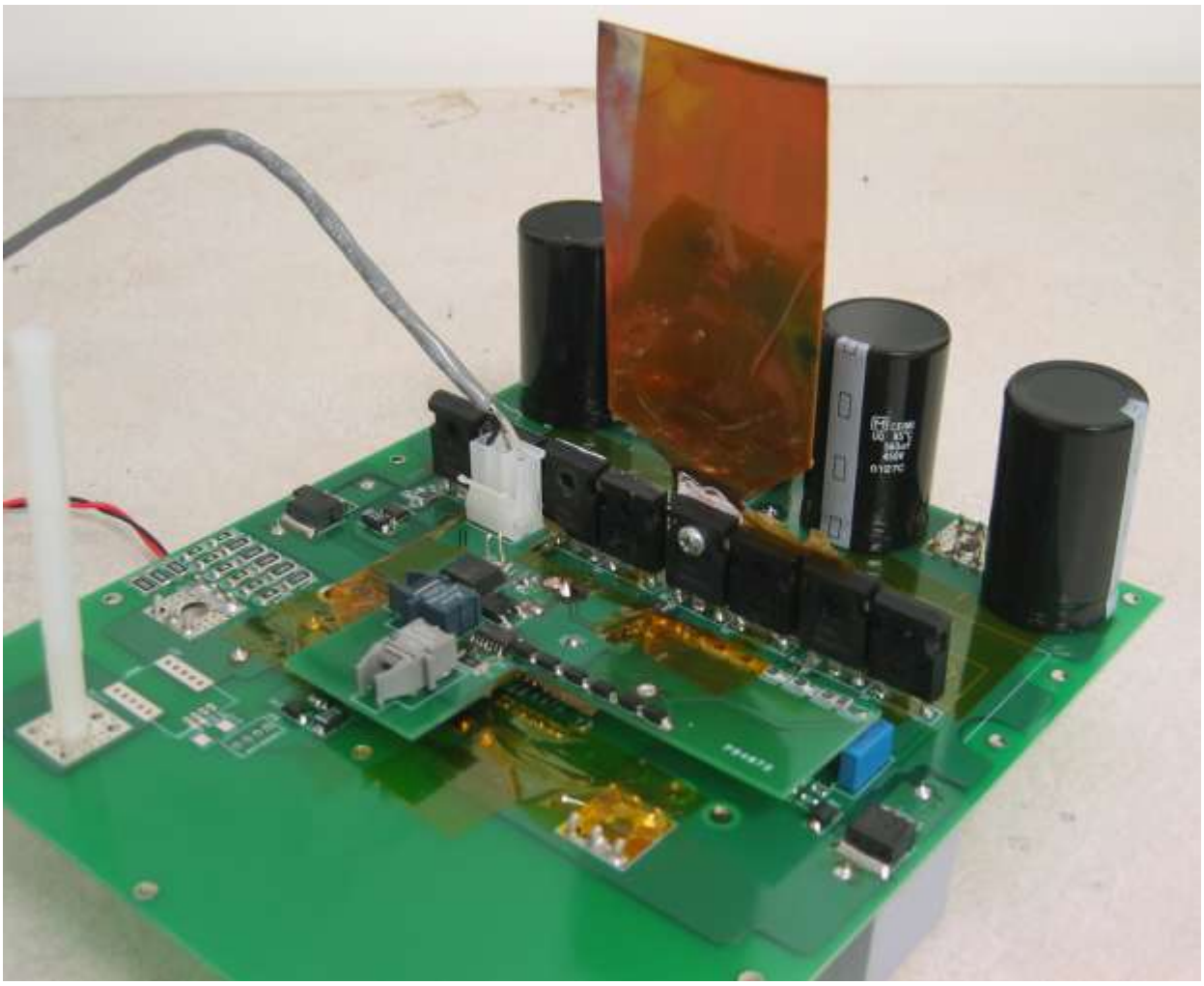

Figure 31: Device driver with CoolMOS, ultra-fast EPU06 diode, four aluminum electrolytic capacitors, and FFB film bypass capacitor (not shown)

A-GA10JT12 (1200V 10A SiC Super Junction Transistor)

Turn-on loss and turn-off loss for this device can be seen in the chart below. The trends that can be discerned from this chart are that at higher current and higher voltages, switching loss increases. The device would probably be used around 700 V and the energy loss at this level can range from 0.25 mJ to 0.75 mJ. Turn-on loss is slightly higher than turn-off loss in this device.

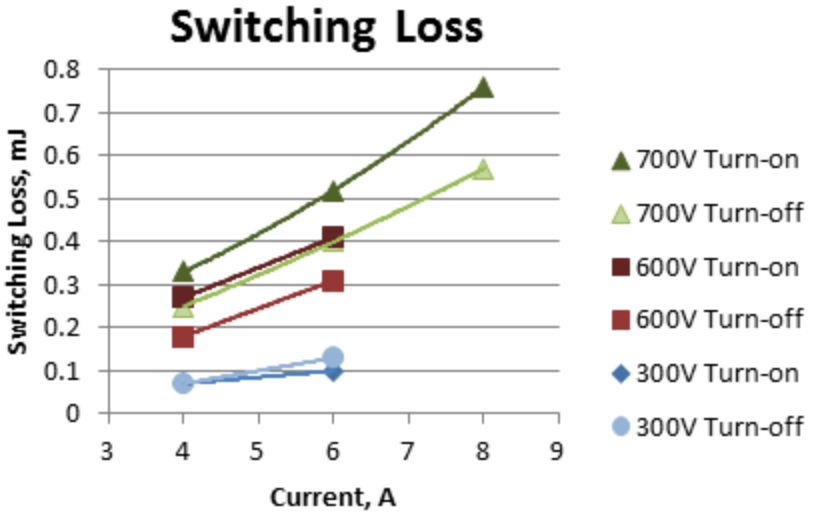

Figure 32: Switching loss of normally-off SJT

This setup used the antiparallel SiC Schottky diode from the GA100XCP12-227 as the freewheeling diode. The device current is interesting to study, as there is some additional current when the device first turns on. Turn-on dv/dt was found to be -3,260 V/µs, turn-off dv/dt was 2,980 V/µs, and turn-on and the magnitude of the di/dt for turn on and turn off was found to be about 160-170 A/µs. These were found by measuring the slope of the steepest turn-on and turn-off waveforms.

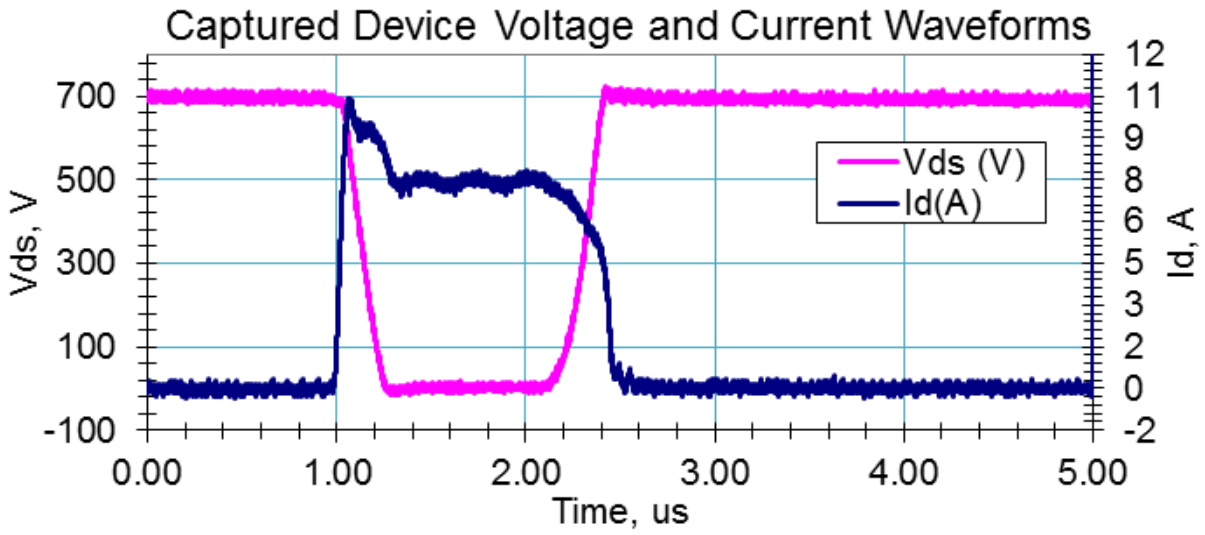

Figure 33: Normally-off SJT switching waveform

IPW60R045CP (650V 60A CoolMOS CP)

The discharge of the diode junction capacitance can be seen in this captured waveform. The diode used in this setup was the 60EPU06 an ultrafast soft recovery diode. The reverse-recovery current has been added about 24A to the expected current. Current rate of change was about 850-870 A/µs. Voltage rate of change was about -17,400 V/µs and 32,800V/µs.

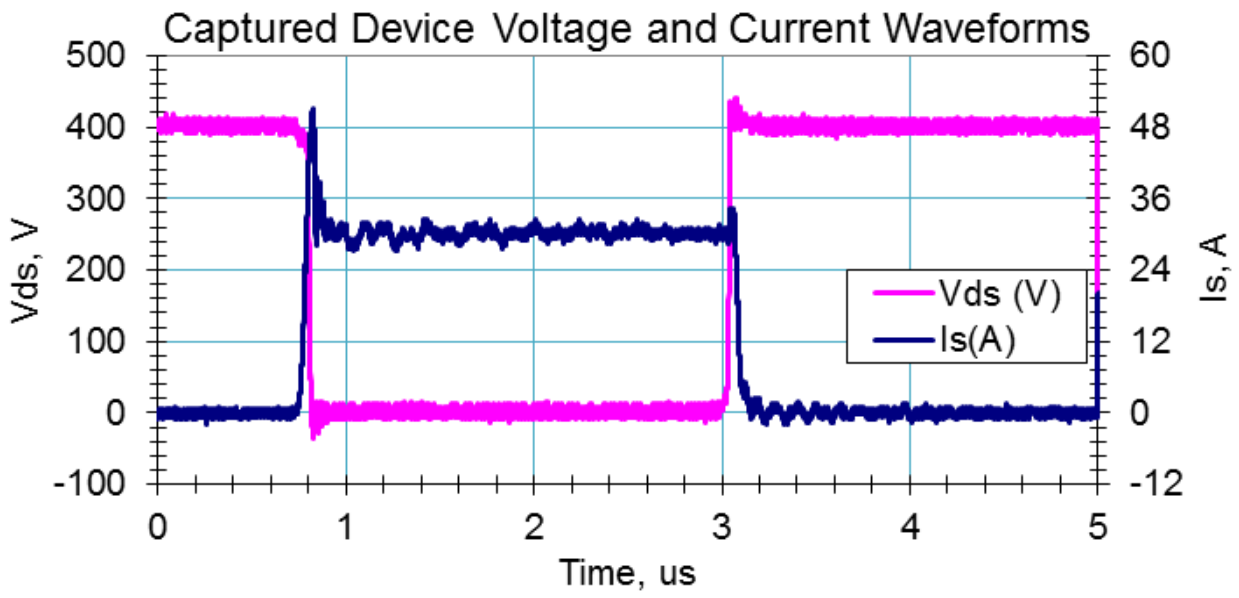

Figure 34: CoolMOS switching waveform

Turn-on switching loss is temperature dependent compared to turn-off loss. As temperature increases, turn-on loss slightly increases and this can be seen in the chart below.

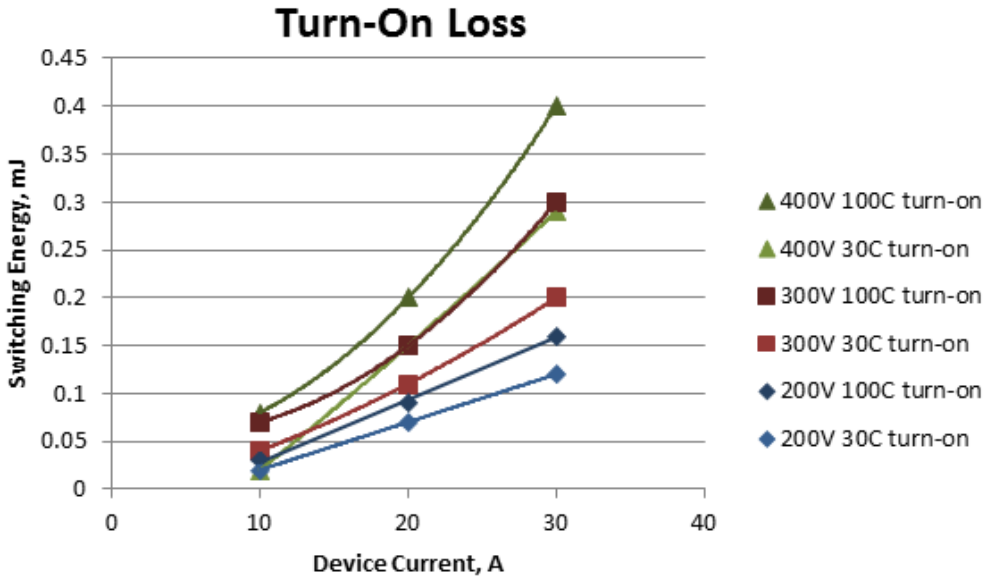

Figure 35: Turn-on loss of CoolMOS

Turn-off loss does not seem to be affected by temperature and this can be shown in the chart below. The turn-off losses seem to be higher for this device and zero-current switching would show more advantageous gains in efficiency [10].

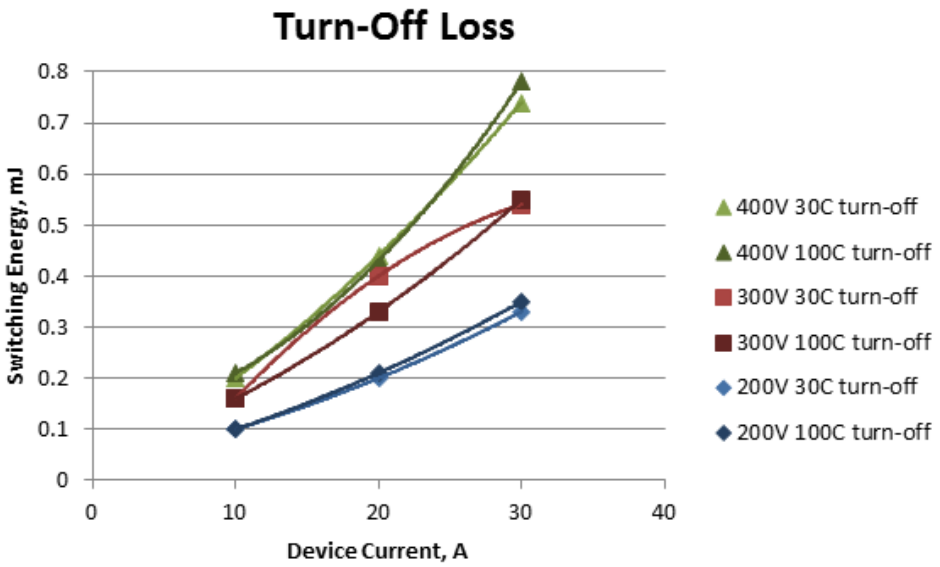

Figure 36: Turn-off loss of CoolMOS

A fast turn-off diode was placed antiparallel to the gate resistor in an effort to decrease switching loss. This result was a success. Turn-on switching loss was not affected by this addition, but turn-off was decreased by almost 50% at currents of 40 A. Lower current showed diminishing returns and at 10 A, loss does not seem to change in value. The turn-off switching loss does not seem to be affected by change in temperature. Testing of the CoolMOS 60R045CP resulted in greatest losses at higher voltages, higher currents and higher temperatures.

CMF20120D (1200V 33A SiC MOSFET)

The device waveforms can be shown below. One can notice more severe ringing of the turn-off current in this device. A pair of C2D10120 1200V 10A Schottky diodes was used to freewheel the large inductor current. Turn-on voltage fell at 8,500 V/µs while turn-off voltage rose at about double the rate of 15,600 V/µs. Current rose at about 450 A/µs and turned off at around the same rate at 513 A/µs. The rise and fall rates were slower compared to the CoolMOS device, but losses seem to be lower. The two cannot be compared directly since the voltage rating for this device is twice that of the CoolMOS. However, this SiC Z-FET device shows similar turn-on loss at 700V as opposed to 400V.

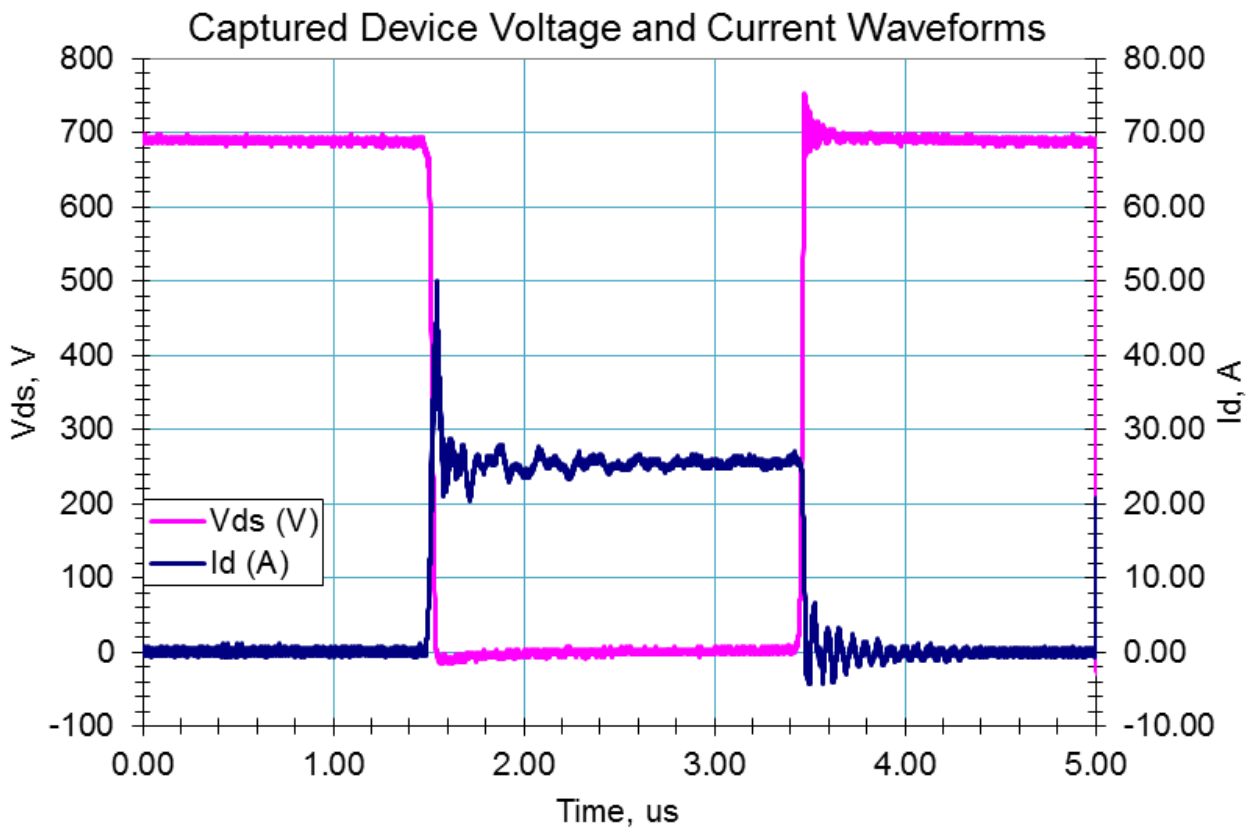

Figure 37: SiC Z-FET switching waveforms

The loss characteristics of this device are interesting to study since turn-on losses and turn-off losses are similar in magnitude. Turn-on loss for this device may be considered temperature independent. The changes in loss are relatively small and can be shown in the chart below.

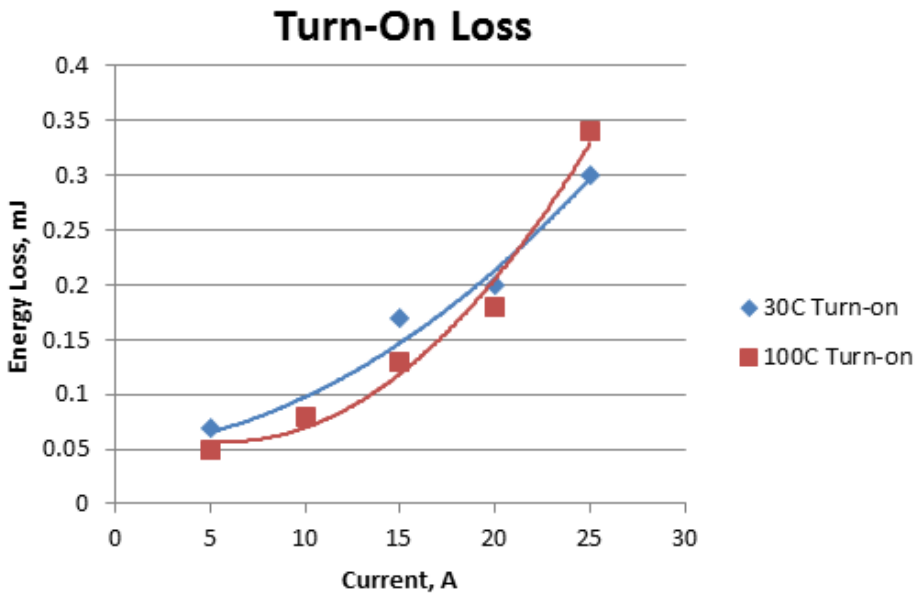

Figure 38: SiC MOSFET turn-on loss

Changes in turn-off loss are also minor, but show a stronger trend. As temperature increases, turn-off losses increase as well. Under these testing conditions it seems that zero-voltage switching would be more advantageous for gains in efficiency.

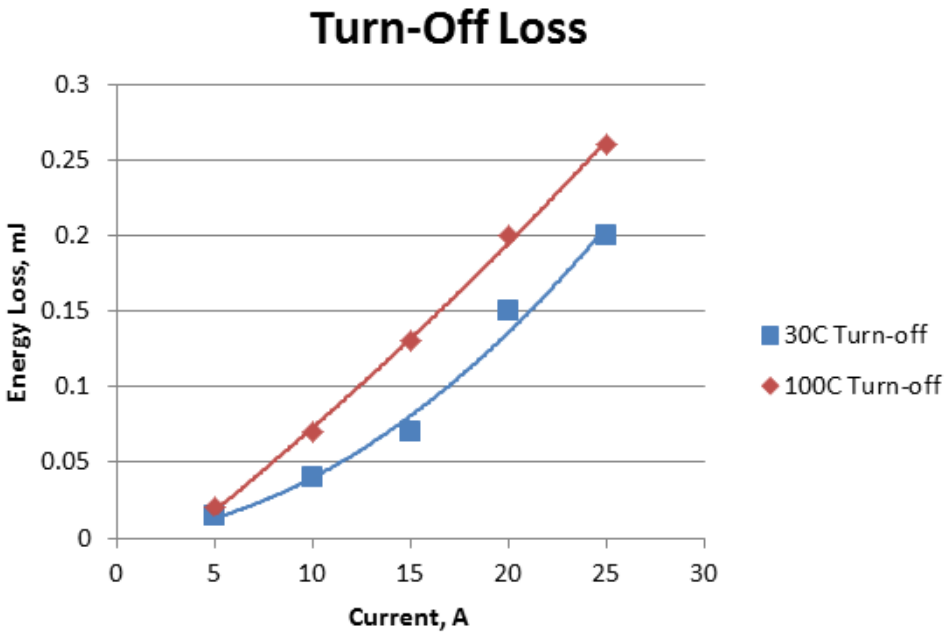

Figure 39: SiC MOSFET turn-off loss

GA100XCP12-227 (1200V 100A IGBT w/copack SiC antiparallel diode)

These device waveforms have been close to ideal. The current waveform shows no sign of diode-junction capacitance discharge while the turn-off voltage across the device appears stiff. Two things can be noticed on this waveform. One is in the turn-on region. When the device turns on the voltage falls quickly and then creates a voltage tail. The turn-off current is fairly slow as expected with an IGBT. The current tail can clearly be seen. The turn-off inductive spike is about 60V. Turn-on current rose at about 1,900 A/µs, while turn-off current fell at a maximum of 1,200 A/µs. Voltage turned on at 11,300 Vµs and turned off at about 7,000 V/µs.

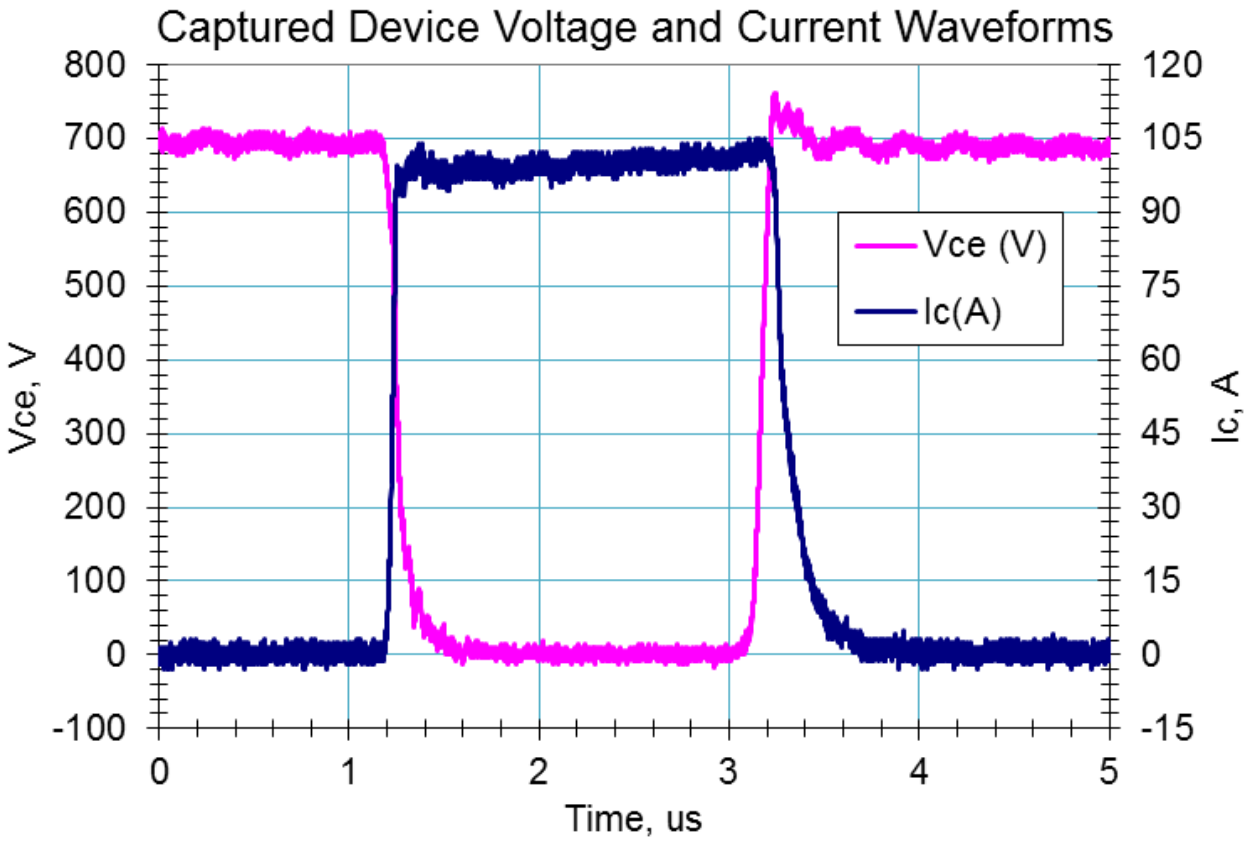

Figure 40: GeneSiC IGBT switching waveforms

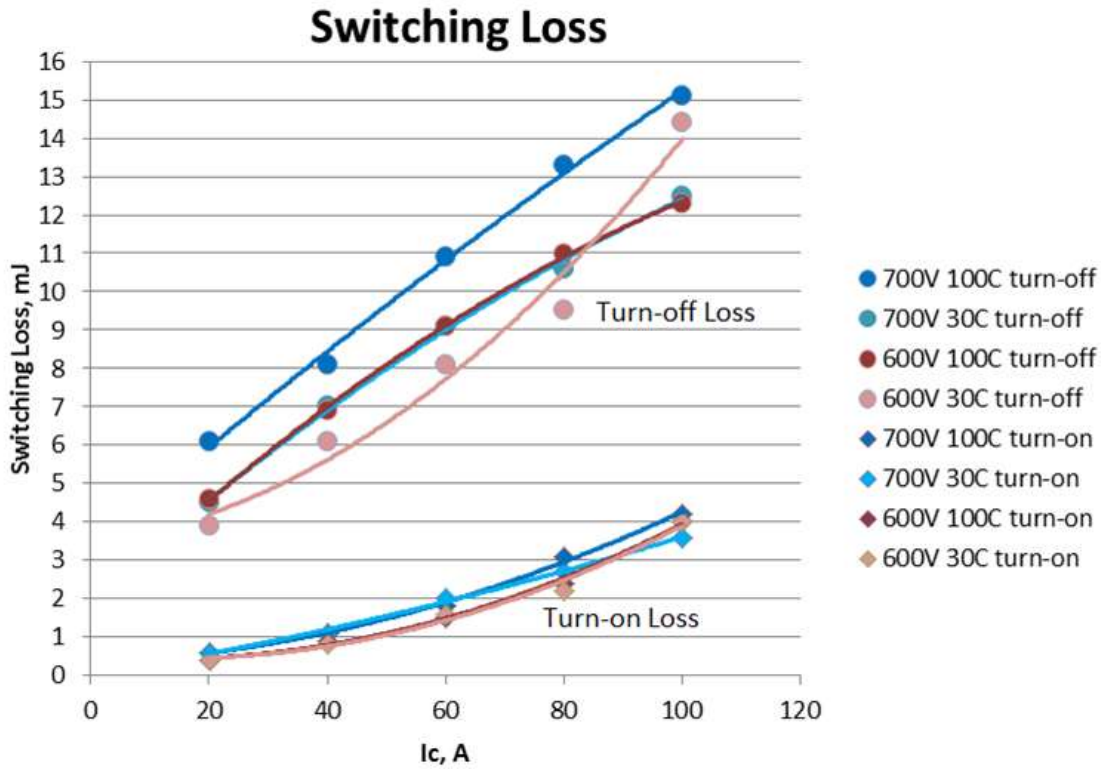

Figure 41: GeneSiC IGBT switching waveforms

Turn-off loss is significantly higher than turn-on loss and infers that using zero-current switching would be a more effective way to utilize this device. The device was tested at 30°C and 100°C. Turn-on loss seems to be temperature independent when looking at the chart above. Voltage levels are in similar colors and higher temperatures are indicated with a darker shade. However turn-off loss increases 1.5 to 3.0 mJ at 700 V and various currents.

FZ200R65KF1 (6.3kV 400A)

This IGBT shows similar characteristics to the GeneSiC IGBT. The turn-on voltage exhibits a tail as well as the turn-off current. The diode used in this case was the DSEP30-12A, a FRED device. The reverse recovery current approaches 100A.

This device was used to emphasize the effects of reverse recovery. The diode that was freewheeling must begin to block voltage at some point; however, this process does not happen instantaneously and part of the result is reverse-recovery current that is now added to the device current. This can be shown in the current spike below. The current spike adds stress to the IGBT and limits operating conditions. Series SiC Schottky diodes can be used to decrease the reverse recovery current and extend useful operating conditions of the device.

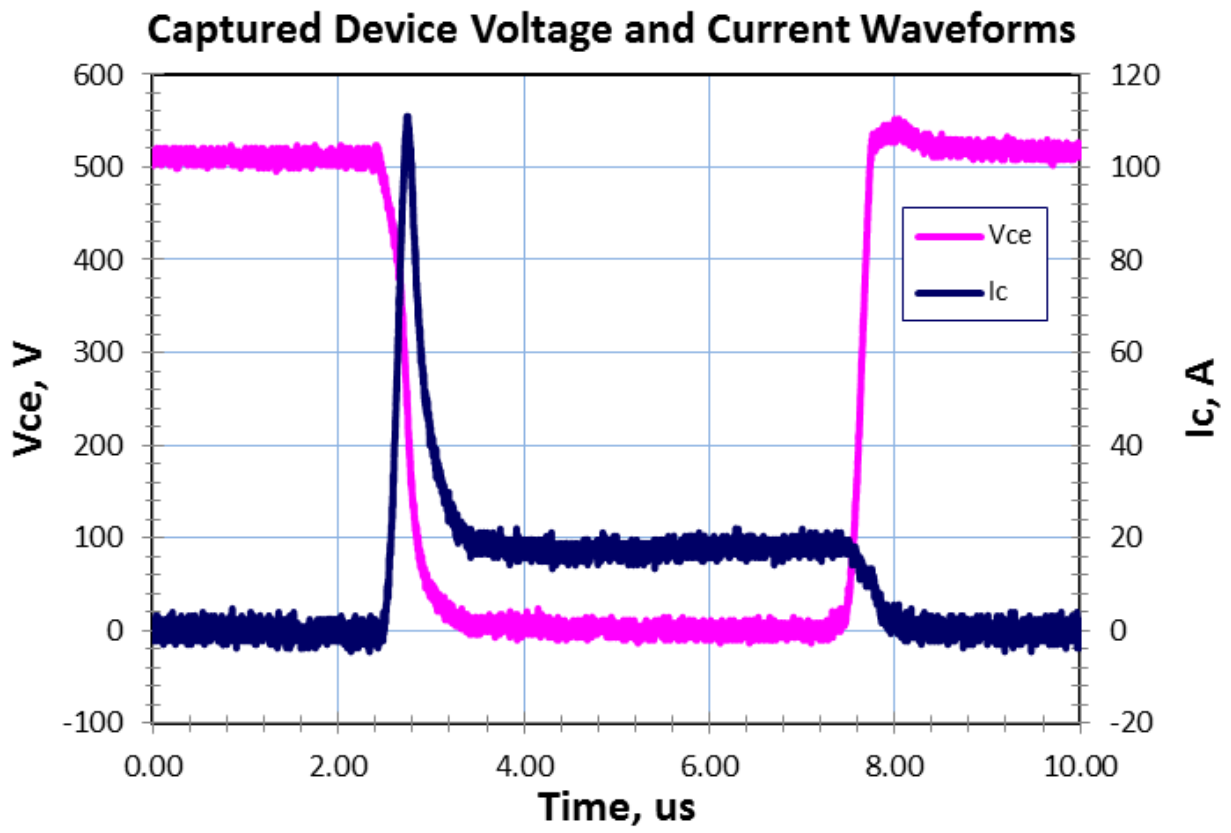

Figure 42: Infineon high-voltage IGBT switching waveform

Summary & Conclusions of Preliminary Testing

	A-GA10JT12	IPW60R045CP	CMF20120D	GA100XCP12-227
Breakdown Voltage, V	1200	650	1200	1200
Maximum Device Current, A	10	60	33	100
Total Gate Charge, nC	Not listed	150	90.8	400
Turn-on; Turn-off dv/dt, V/μs	3,260; 2,980	17,400; 32,800	8,500; 15,600	11,300; 7,000
Turn-on; Turn-off di/dt, A/μs	160; 170	850; 870	450; 513	1,900; 1,200
Turn-on Loss Range, mJ	0.1 – 0.8	0.05 – 0.4	0.05 – 0.35	0.5 - 4.0
Turn-off Loss Range, mJ	0.1 – 0.6	0.1 – 0.8	0.02 – 0.25	4.0 – 15.0
Total Loss, mJ	0.2 – 1.4	0.15 – 1.2	0.07 – 0.55	4.5 – 19.0

Table 3: Table of device losses

The SiC MOSFET exhibited slower rates of change in voltage and current, however it seems to exhibit lower switching loss than the CoolMOS, especially for turn-off loss. The CoolMOS was the fastest device that was tested. Again, these two devices are not directly comparable, since the SiC device was tested at 700 V and the CoolMOS was tested at 400 V.

It was confirmed that the IGBT is a slower device compared to MOSFETs, but the device operates under conditions MOSFETs simply cannot. The table above shows that increased gate charge results in increased switching loss, but this relationship is not linear. Testing of devices has generally shown that higher voltages, higher currents, and higher currents result in higher loss. Turn-on loss does not seem to vary with temperature for the GeneSiC IGBT and the SiC MOSFET. It appears that turn-on loss might even be slightly lower for the SiC MOSFET when temperature increases. Turn-off loss does not seem to be temperature dependent for the SiC SJT as well.

The test setup showed that a large low-inductance polypropylene capacitor can provide a path of low-inductance localized path and decrease large voltage overshoot. Also Schottky rectifiers decrease or eliminate reverse recovery current. Both of these considerations anticipate the non-ideal behavior of switching devices and will result in more robust and reliable design.

This may seem obvious, but switching loss occurs when voltage across the device and current through the device are present at the same time. The way to reduce this loss is to reverse the occurrence of events. Turn-on loss occurs since current rises before voltage falls. If voltage falls before current rises during device turn on, then switching loss has been reduced. The opposite is true for turn-off loss.

With hindsight these loss numbers could be slightly off. The large voltage probe probably has a significant delay; it should be accounted for by using the deskew feature on the oscilloscope. This feature allows the user to shift time scales and accommodate for part of the probe's non-idealities.

III. PCB Device Testing

Device testing setup can be seen below:

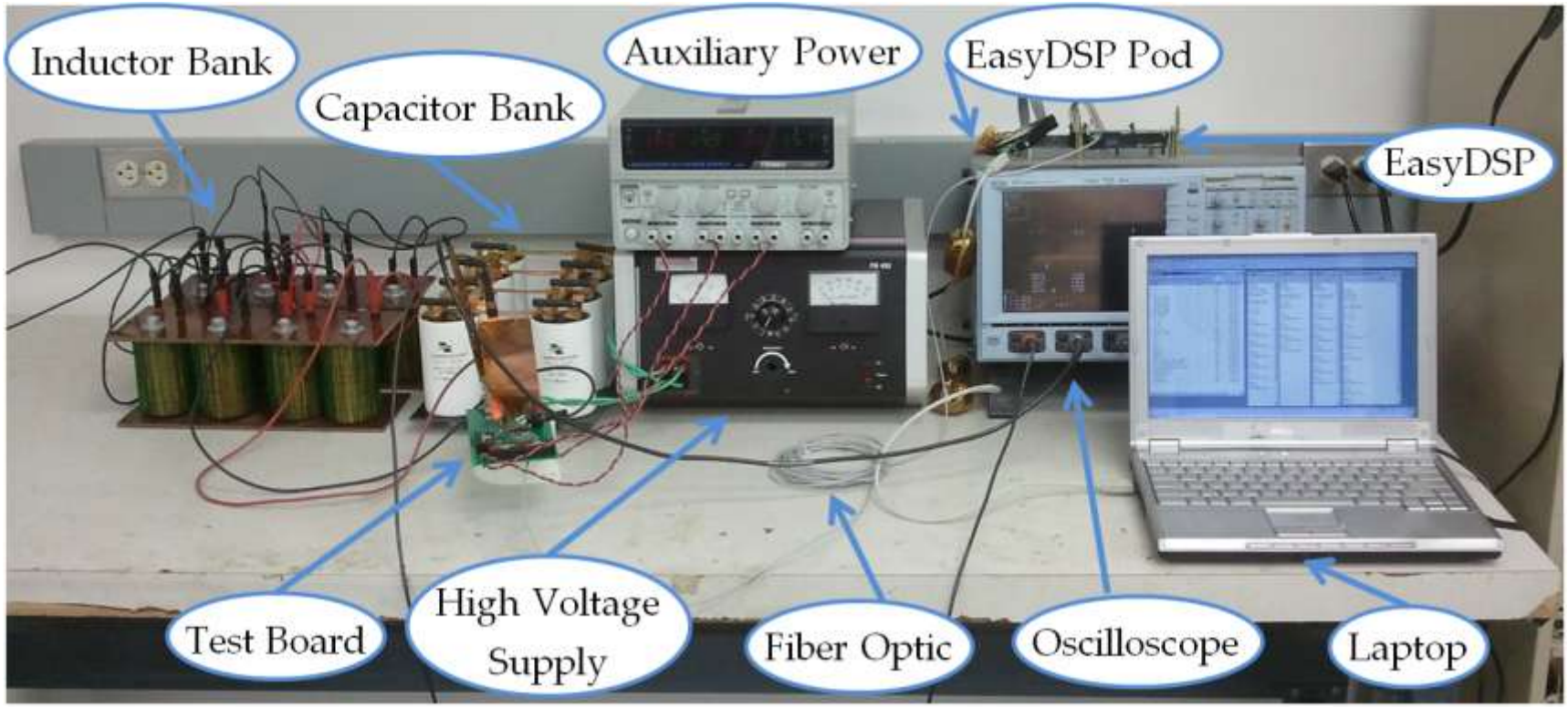

Figure 43: Device testing setup with board

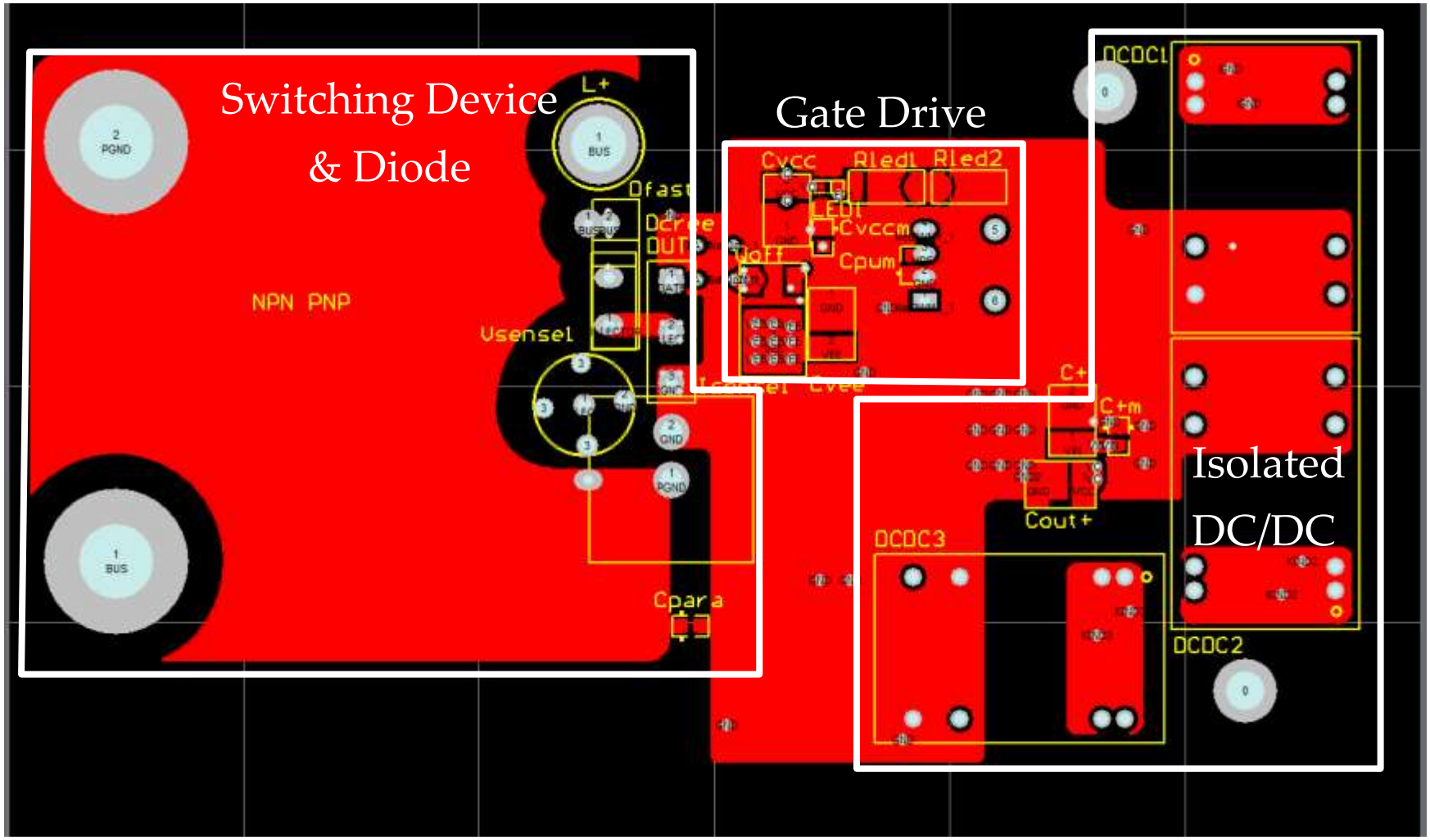

Figure 44: Top layer of device test PCB

In order to standardize testing conditions a device-testing measurement board was made to replace the homemade testing setup. The board design has been presented above and below. The figure above is the top layer of the board. The top layer includes the device-measurement setup on the left side of the board. Part of the gate drive circuitry is also included in the middle of the board. The gate drive is powered by isolated DC/DC supplies on the right side of the board. A zoomed in screenshot is shown below. The top layer is used to provide large ground planes. With proper consideration and planning this can decrease parasitic inductance if the return path is right above or beneath the signal or power trace [13].

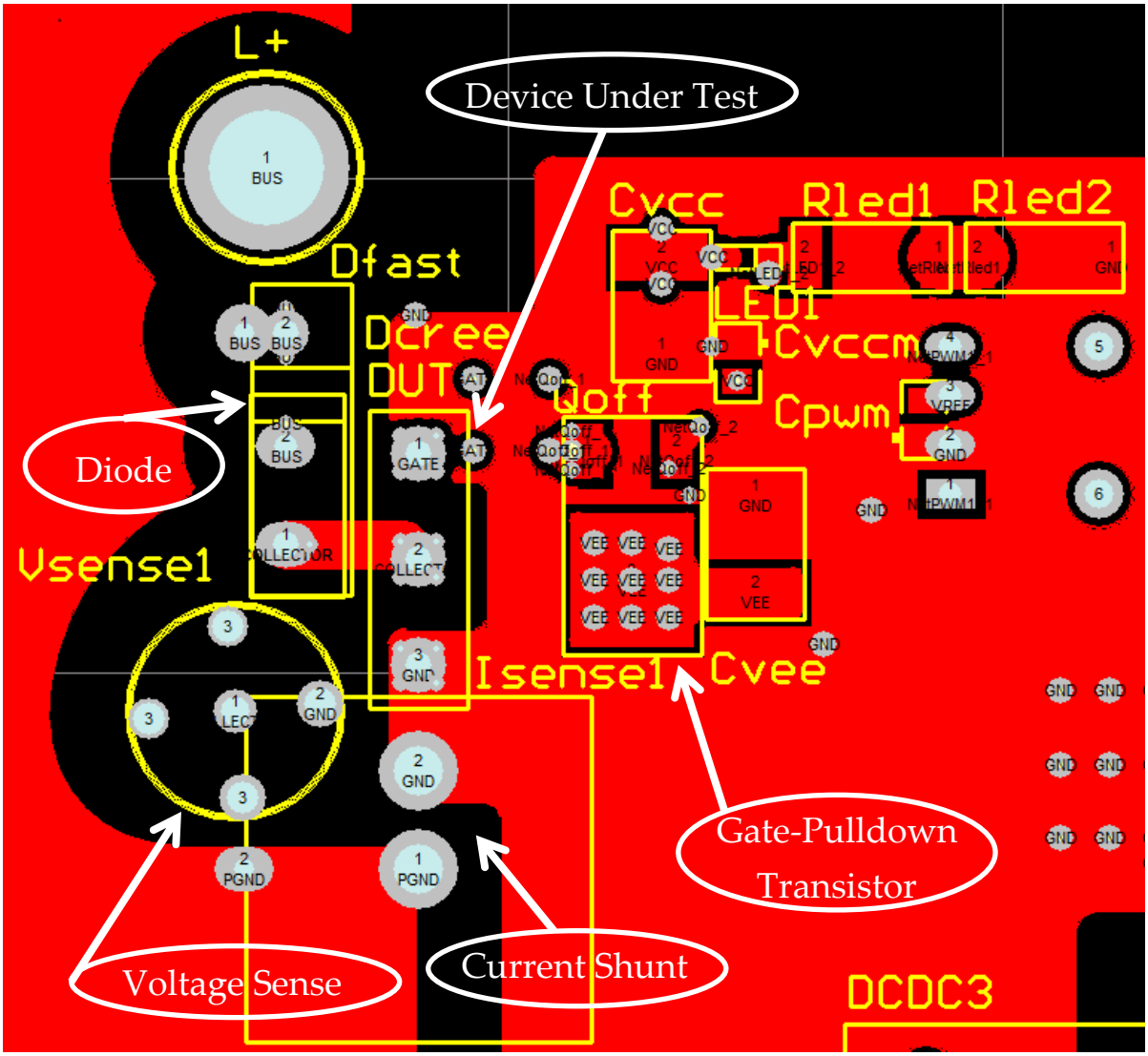

Figure 45: Zoomed in top layer of device test PCB

The zoomed-in figure shows more detail of the board. The main segments of the tester are shown including the freewheeling diode, device under test, the voltage sensing output and current shunt. Some special things to note are that the diode footprint allows either a two-pin TO-220 or any TO-247 diode to be used. The voltage sense footprint is actually a BNC footprint. A probe to BNC adapter was found and implemented to avoid the use of the ground clip of the probe. It has been documented that this ground

clip can add parasitic inductance and gives less accurate voltage measurements [5]. The L+ hole is a hole for a female banana jack. The inductors just plug right into the board in this fashion. The other end of the inductor is then connected to the drain tab of the MOSFET itself. This was done in order to avoid adding another hole or other component and keep this power circuit as close together as possible and effectively reducing as much parasitic inductance as possible.

There are some undesirable characteristics of this layout though. The placement of the Vsense1 BNC actually slightly increases the loop inductance, since clearance is required between the collector node and pretty much anything else. This was deemed to be the better compromise. If the BNC was moved to the other side of the current shunt, then the length of the gate driving loop would have had to be increased. Another trade-off was made when the turn-off BJT, Q_{off}, was placed on the top of the board. This decreased the length between the gate drive and the MOSFET, but came at the price of breaking the ground plane. Looking back on this design placing the BJT on the bottom of the board with the rest of the gate drive components might have been the better choice. This may have been slightly longer, but the continuous ground plane may have hedged against that. Finally the current shunt BNC has been the fastest responding current sensor tested; however, the leads of the SDN-414-10 do add parasitic inductance. There should be a better way to decrease the insertion inductance.

The bottom layer of the board can be seen in the following figure. The bulk capacitor is the Vishay film GLI-series capacitor. More information about it can found on the datasheet [13]. It is pretty massive and can act as a base as well. The bypass capacitor has been placed directly across the series pair of the diode and MOSFET. Most of the gate drive circuitry was placed on the bottom of the board. The DC/DC supplies actually go to a positive and negative linear regulator. With this setup, the positive and negative driving voltage can be customized. The gate drive chip that was implemented, ST's TD350 [14], requires 11 V to function, but can withstand up to 28 V total. The negative voltage rail can be changed from -15 V to 0 V.

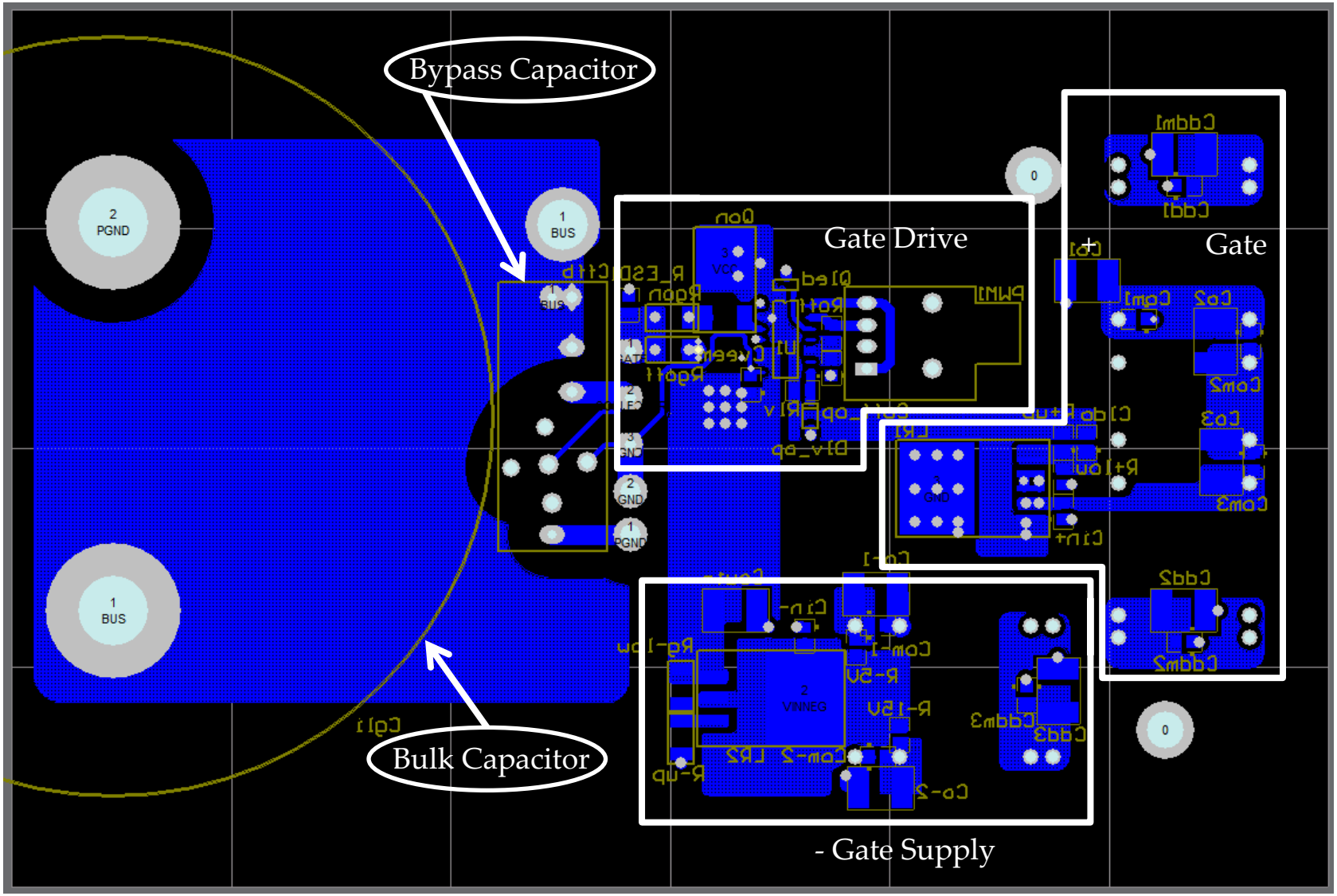

Figure 46: Bottom layer of device test PCB

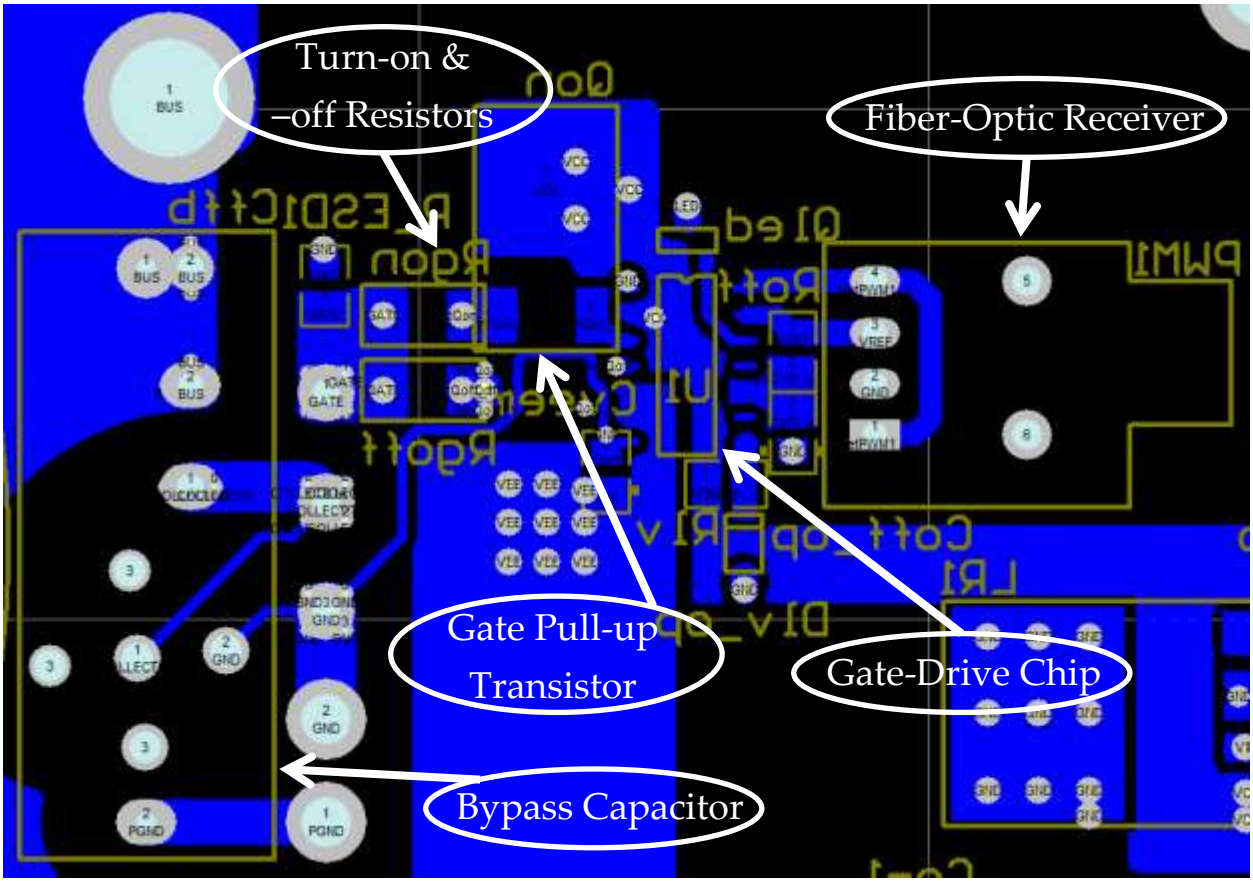

Figure 47: Zoomed in bottom layer of device PCB

Standardizing Testing Procedure

To somewhat standardize the test procedure, the CoolMOS was used first. The C2D1020 Schottky diode was used in all of the PCB testing in order to standardize the procedure. It is a Schottky diode so reverse-recovery loss will not be an issue. Device testing should result in mostly device losses and not diode switching behavior. Device testing commenced with changes in gate drive voltages. Three gate voltages were used and the results can be seen below. As gate voltage is increased, turn-on switching loss decreased while turn-off losses increased. As a result 15 V was used as a compromise between turn-on loss and turn- off loss. In order to keep the current drive capability the same, turn-on and turn-off resistors were changed according to the drive voltage. The initial drive current was calculated by just dividing the drive voltage by the gate resistance. This assumed that the capacitor voltage was initially 0 V and estimated the initial drive-current capability. Since resistors are made in discrete sizes, the exact voltage drive to resistor ratio could not be matched.

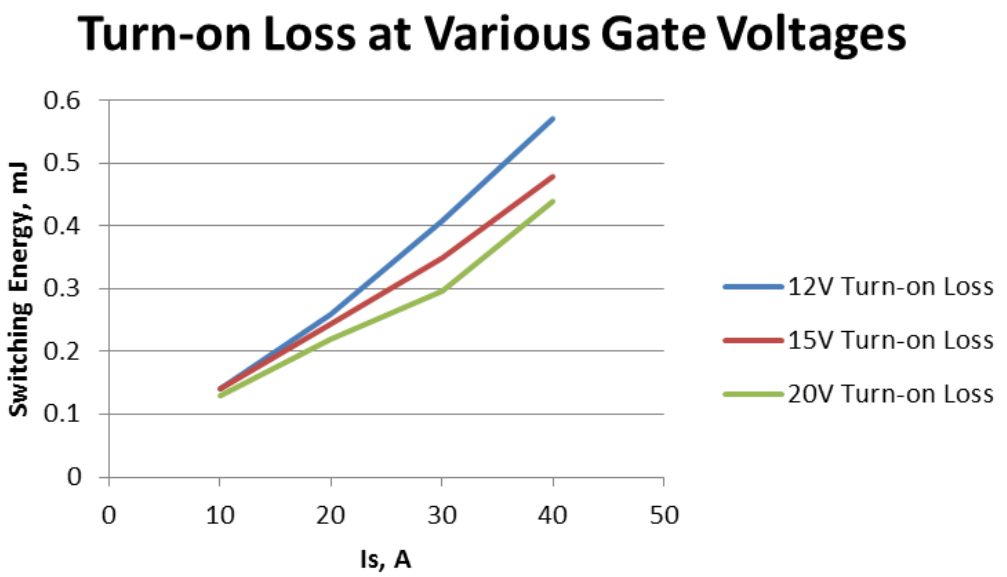

Figure 48: Turn-on switching loss at different gate voltages

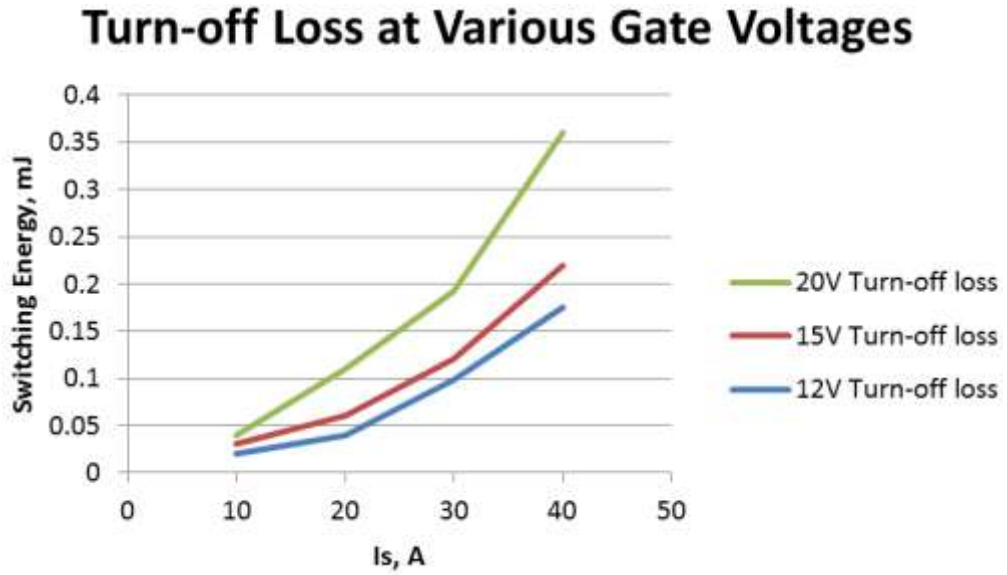

Figure 49:Turn-off switching loss at different gate voltages

After a drive voltage of 15 V was chosen; gate drive resistors were selected based on transient current at turn on and transient voltage at turn-off. The voltage spike was kept below the breakdown voltage in order to stay within the safe operating area of the device. The transient current of the device has the freedom to be larger. In this device setup, turn-on was chosen to decrease switching loss as much as possible. The turn-off resistance vs. loss and turn-on resistance vs. loss has been tested and shown below.

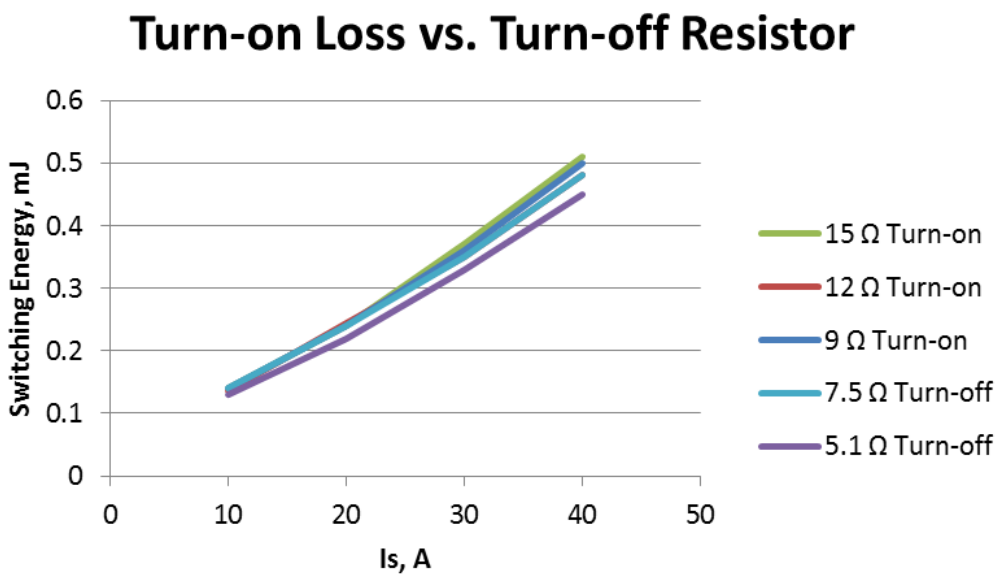

Figure 50: Turn-on switching loss as turn-off resistance is changed

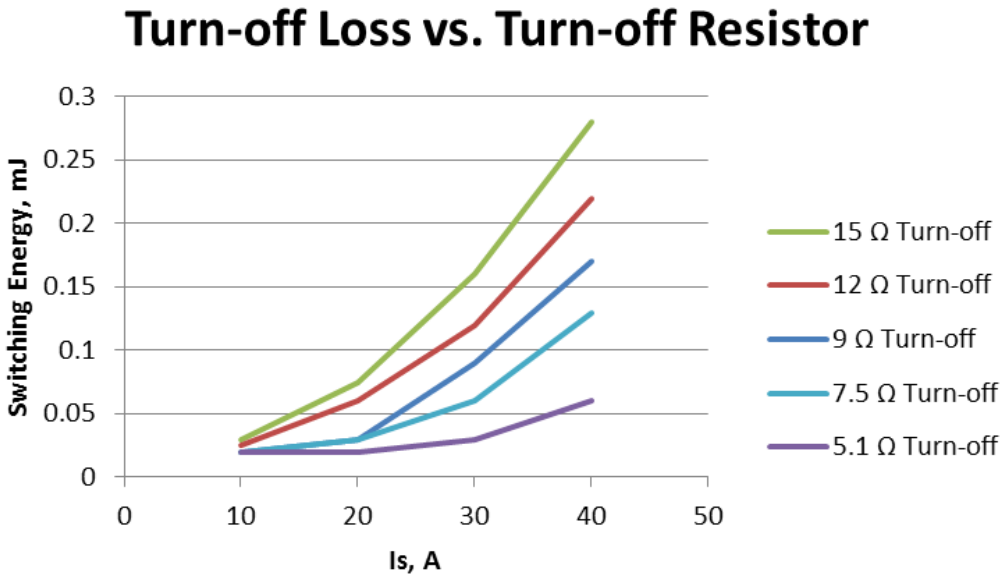

Figure 51: Turn-off switching loss as turn-off resistance is changed

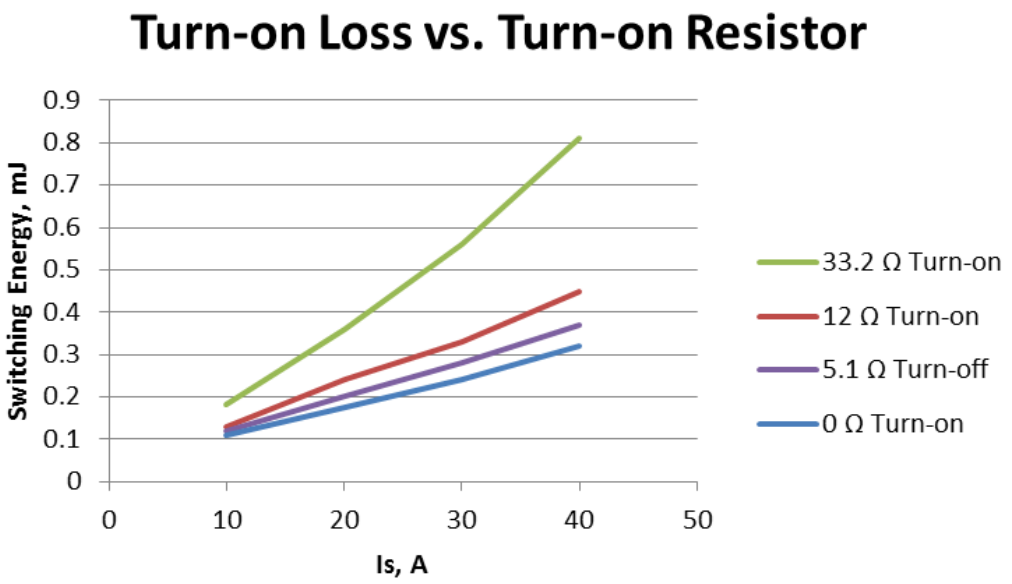

Figure 52: Turn-on switching loss as turn-on resistance is changed

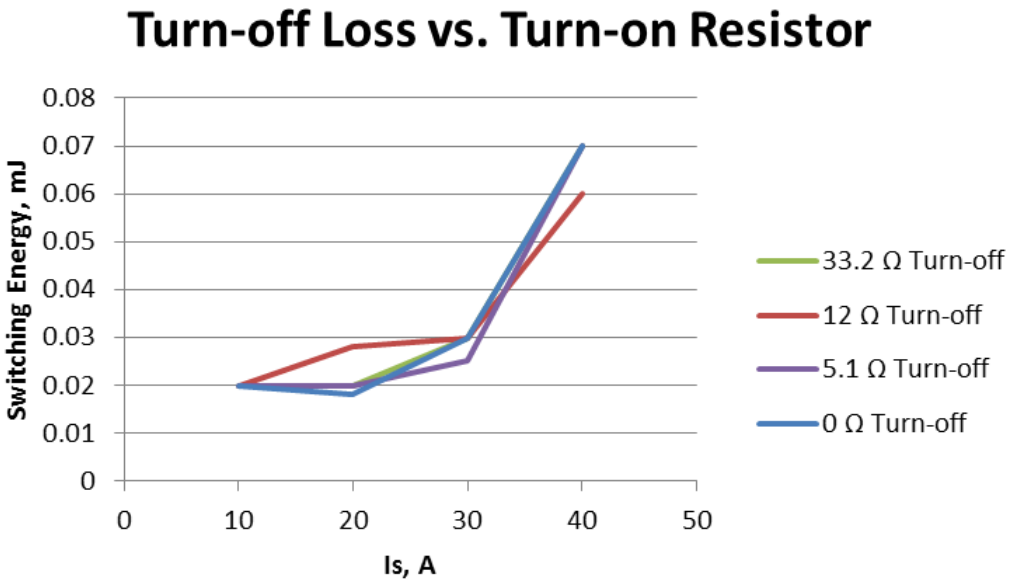

Figure 53: Turn-off switching loss as turn-on resistance is changed

The devices that were tested were based on the current benchmark MOSFET. Infineon's CoolMOS comes in a TO-247 package with a hole in the center, which limits die size. Based on an idea of die size and voltage and resistance capabilities, the following devices have been selected; as well as the SiC Z-FET.

	Z-FET CMF20120D	MDMesh STW77N65M5	SupreMOS FCH76N60N	CoolMOS IPW60R045CP	Vishay SiHG47N60S
Breakdown Voltage, V	1200	650 Min.	600	600	600
$R_{ds(on)}$, mΩ	110 20V 25C	38 10V 34.5A 25C	36 10V 38A	45 10V 44 A	70 10V 30A
Maximum Device Current, A (25C)	33 25c vgs20V	69 25C	76	60 25C	47 25C
Total Gate Charge, nC	90.8 -2 to 20V 800V 20A	200@10V 520 V 34.5 A	218@10V 380V 38A	150@10V 400V 44A	180@10V 400 V 20 A
C_{iss}, nF $V_{ds} = 100V$	1.9 800 V	9.8	9.3	6.8	6.6
C_{oss}, pF $V_{ds} = 100V$	120	200	195 380V	320	220
C_{rss}, pF $V_{ds} = 100V$	13	6	3.1 100V	4.4	7

Table 4: Datasheet values [15], [16], [17], [18], [19]

Note that the input, output, and reverse capacitances change with voltage across the device in a non-linear matter; the input capacitance does not vary much compared to the output and reverse capacitances, which start out with nF capacitances and reduce to the pF range. The devices have been shown in order of voltage overshoot from highest to lowest with the exception of the Cree, which is shown first.

SiC Z-FET: CMF20120D

The Cree Z-FET is a SiC device and was tested at a gate voltage of 20 V and -3.3 V with gate drive resistances of 9.1 ohm for turn on and 6.8 ohm for turn off. These are both low resistances that allow fast turn-on and turn-off of the MOSFET. It should be noted that the Cree has been tested at higher gate turn-on and turn-off resistances and will as a result show inflated turn-on and turn-off losses compared to the other Si MOSFETs shown in this document.

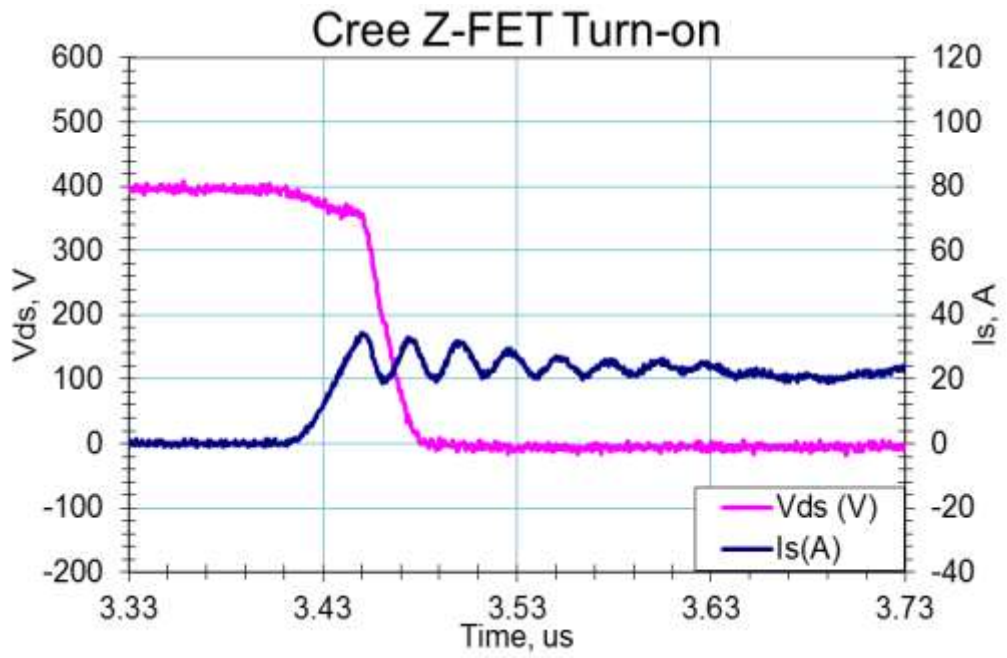

Figure 54: Cree Z-FET turn-on waveform

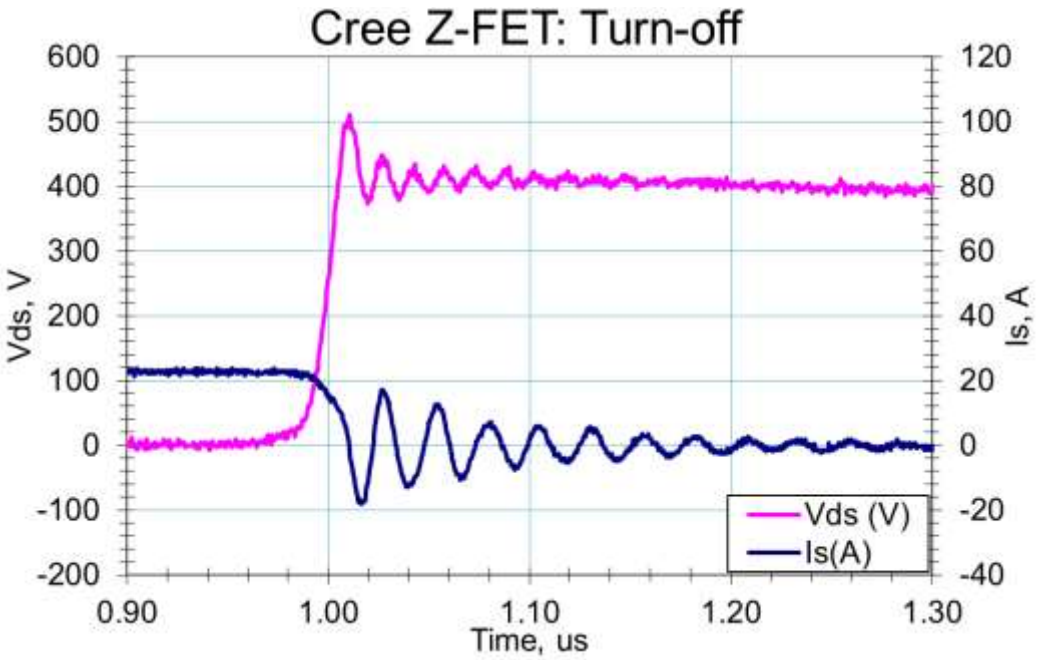

Figure 55: Cree Z-FET turn-off waveform

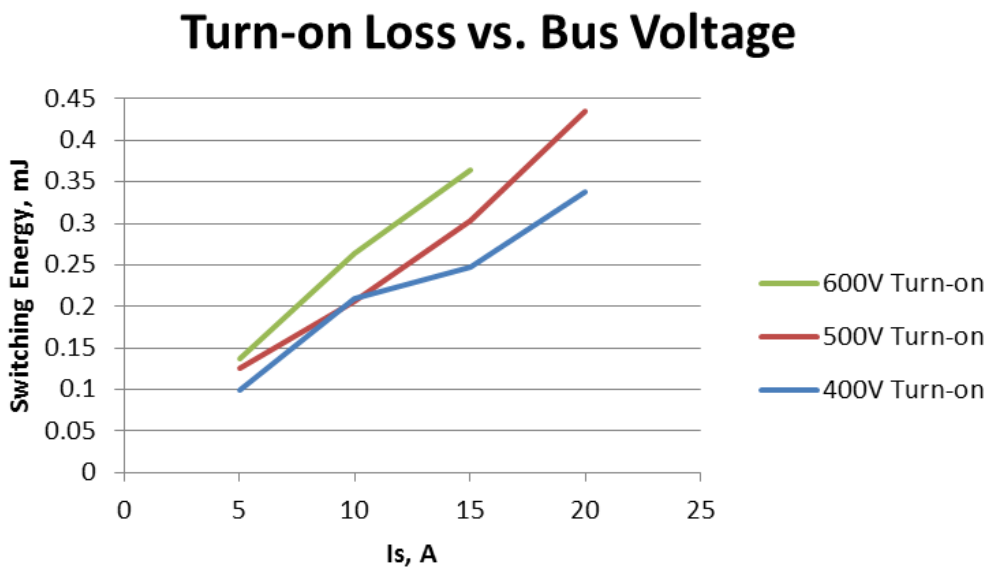

Figure 56: Cree Z-FET turn-on loss, device was overcurrented before 600 V, 20 A rating

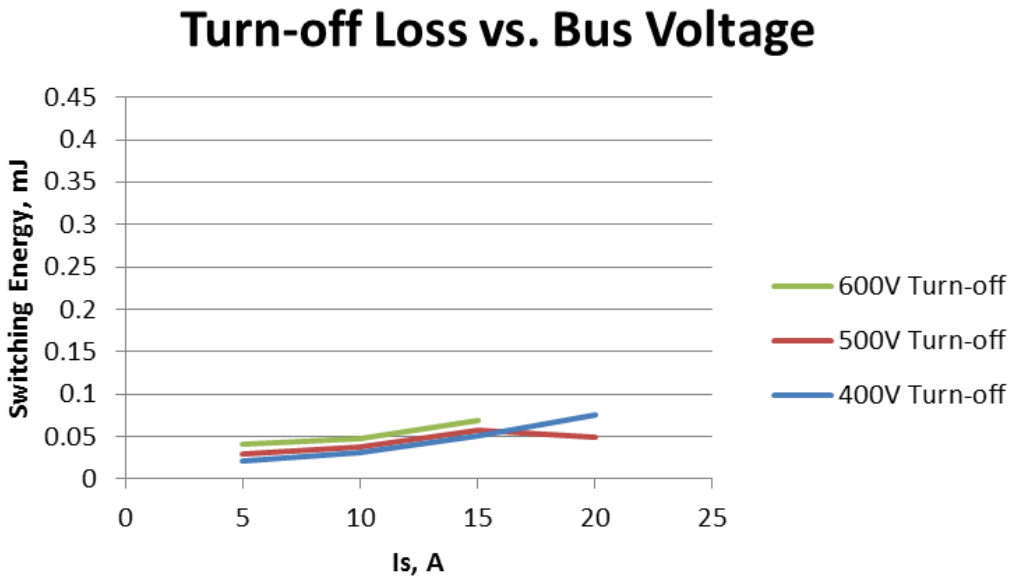

Figure 57: Cree Z-FET turn-off loss, device failed before 600 V, 20 A testing

MDMesh: STW77N65M5

The ST waveform has been captured and shown below.

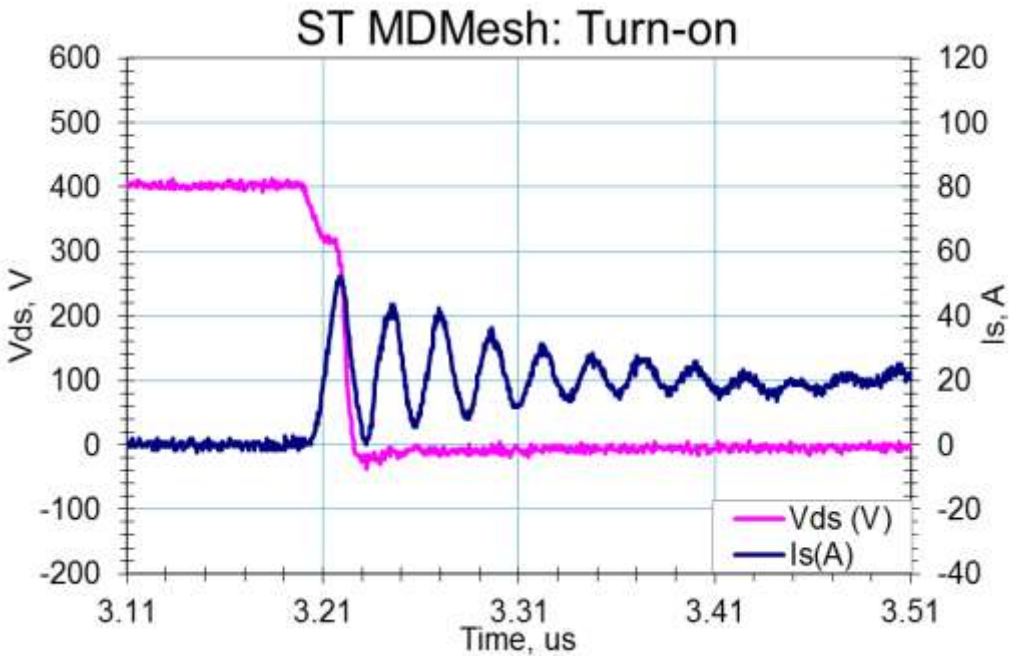

Figure 58: ST MDMesh turn-on

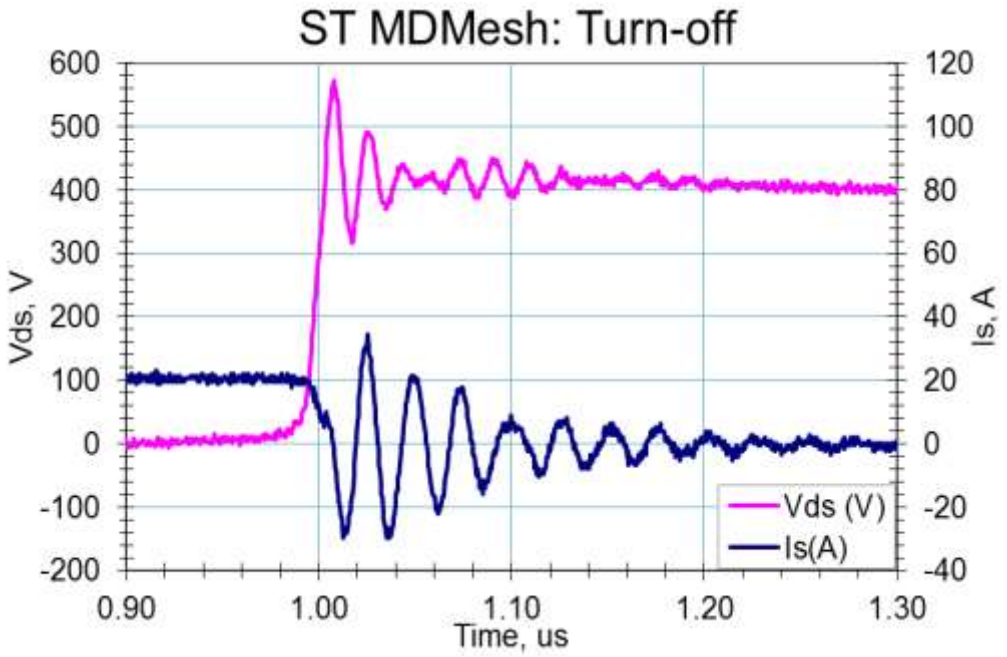

Figure: ST MDMesh turn-off

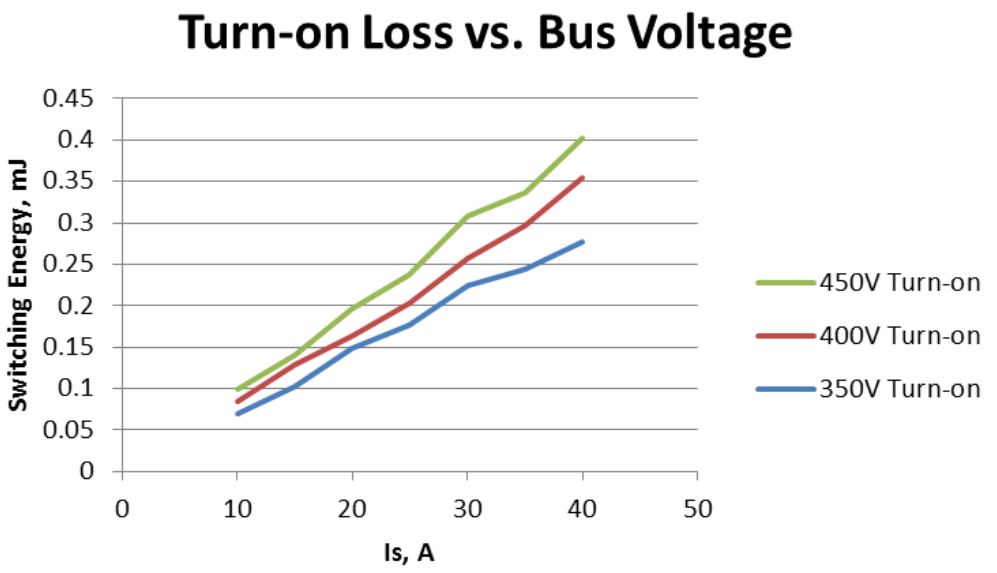

Figure 59: ST MDMesh turn-on energy loss

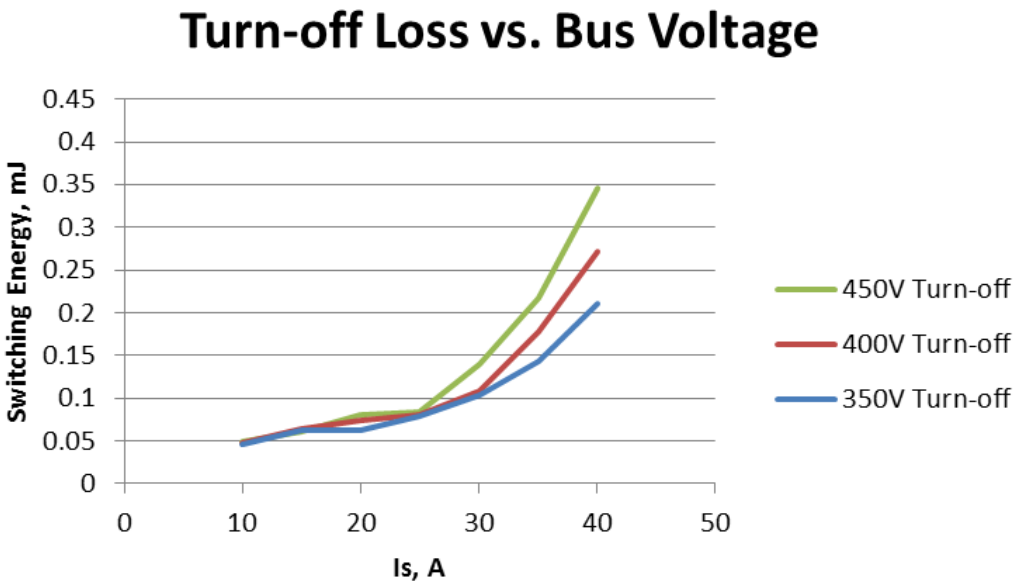

Figure 60: ST MDMesh turn-off energy loss

SupreMOS: FCH76N60N

The Fairchild SupreMOS has been tested and the waveforms and loss trends have been shown below.

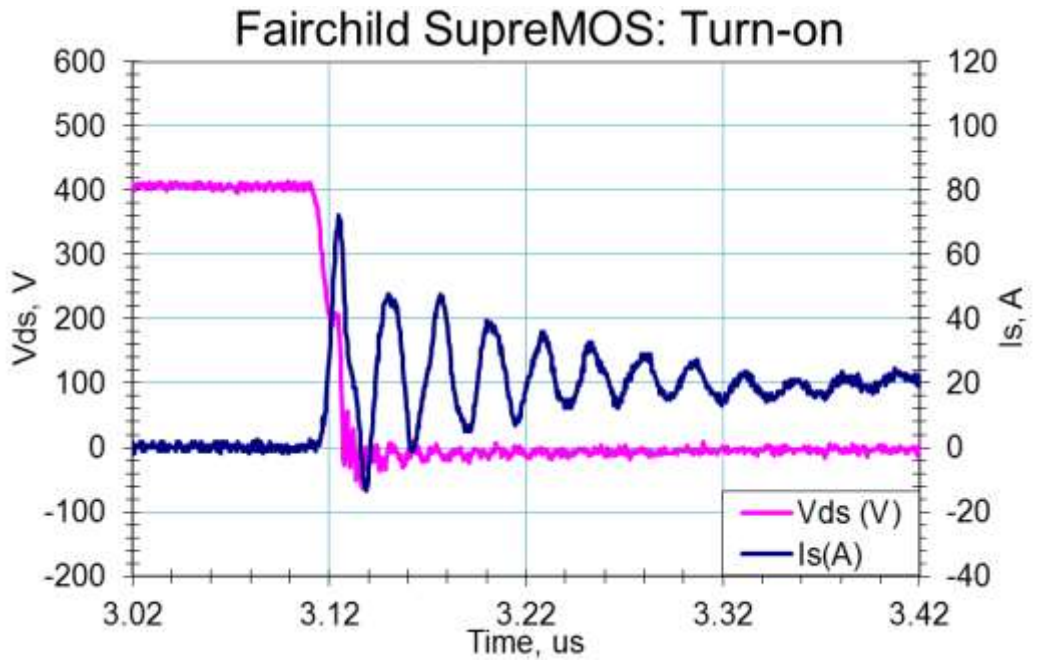

Figure 61: Fairchild SupreMOS turn-on waveform

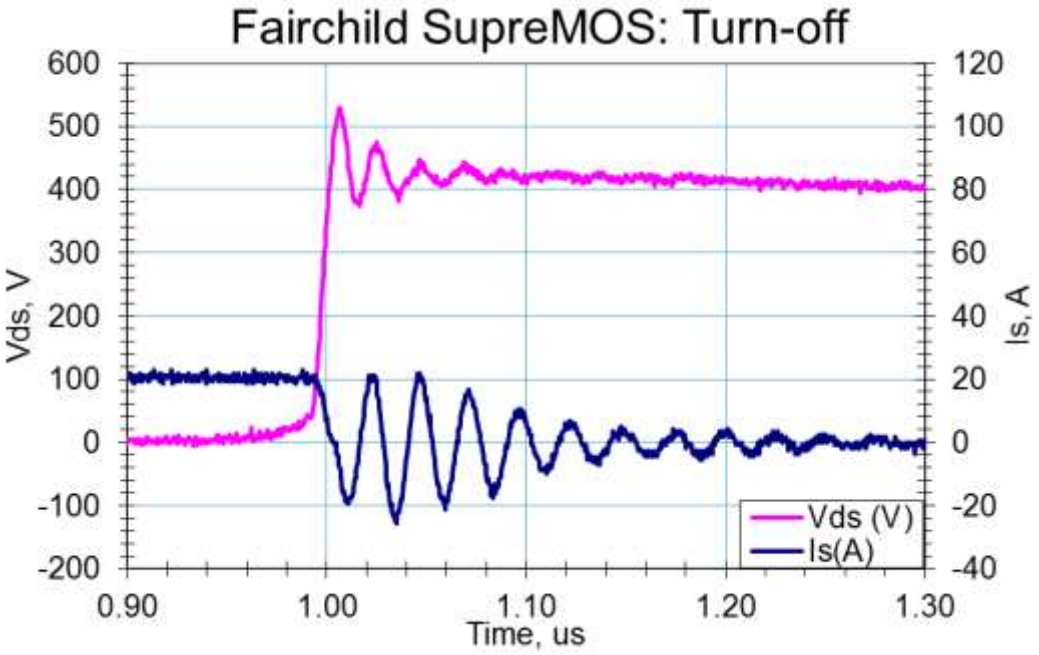

Figure 62: Fairchild SupreMOS turn-off waveform

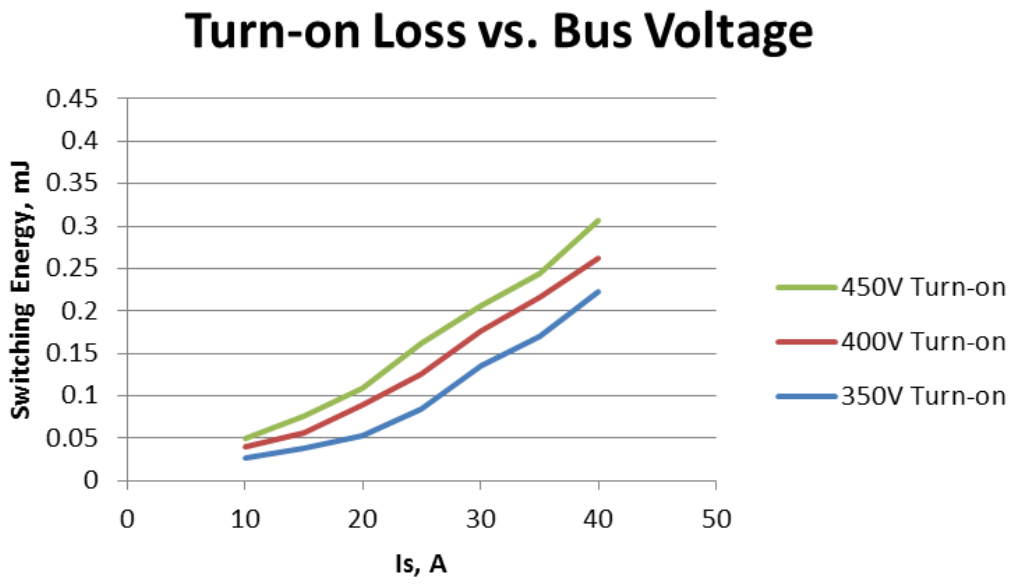

Figure 63: Turn-off switching energy of the SupreMOS device is shown.

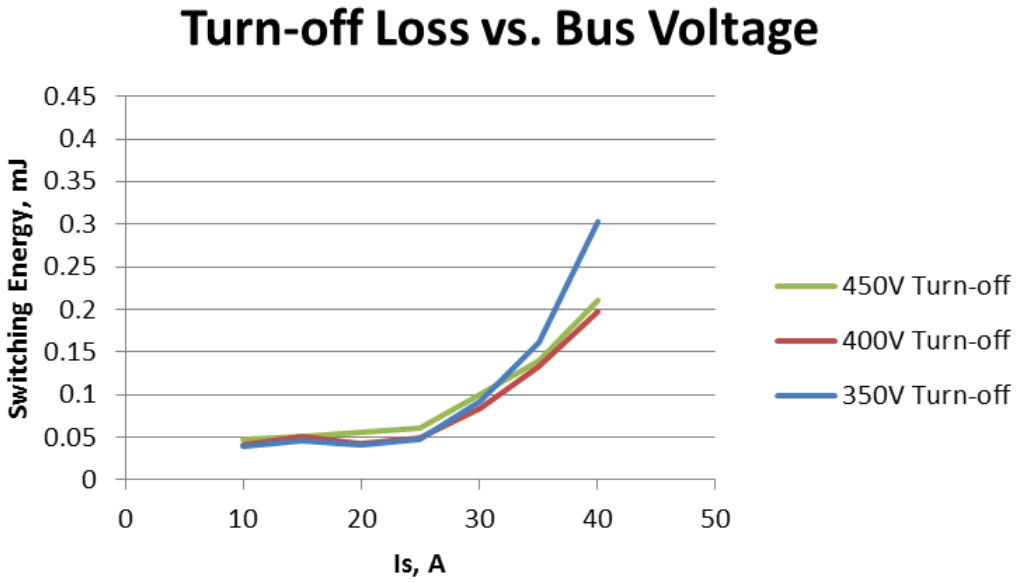

Figure 64: Turn-off switching energy of the SupreMOS device is shown.

CoolMOS: IPW60R045

The benchmark MOSFET, Infineon CoolMOS, has been tested. The voltage and current waveforms ring for the longest time compared to the other switched, but is also the most sinusoidal out of the bunch.

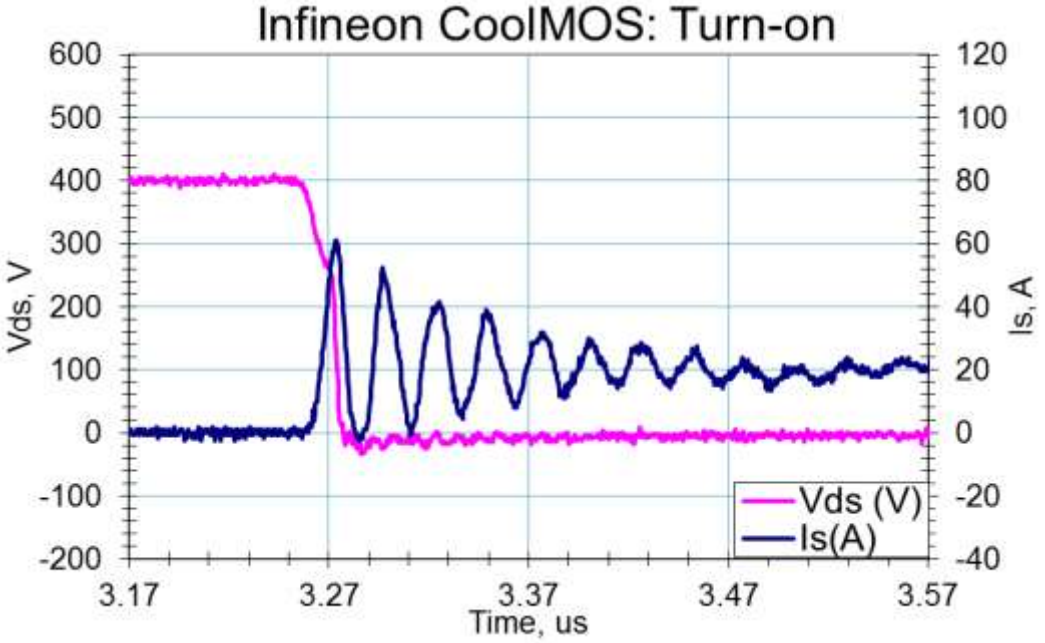

Figure 65: Infineon CoolMOS turn-on waveform

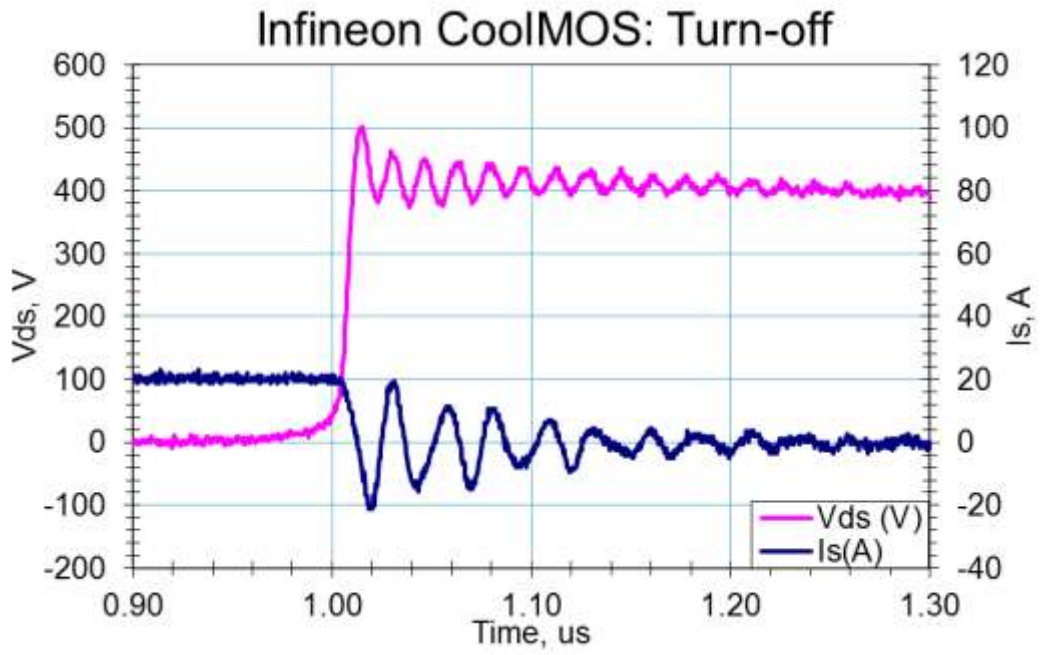

Figure 66: Infineon CoolMOS turn-off waveform

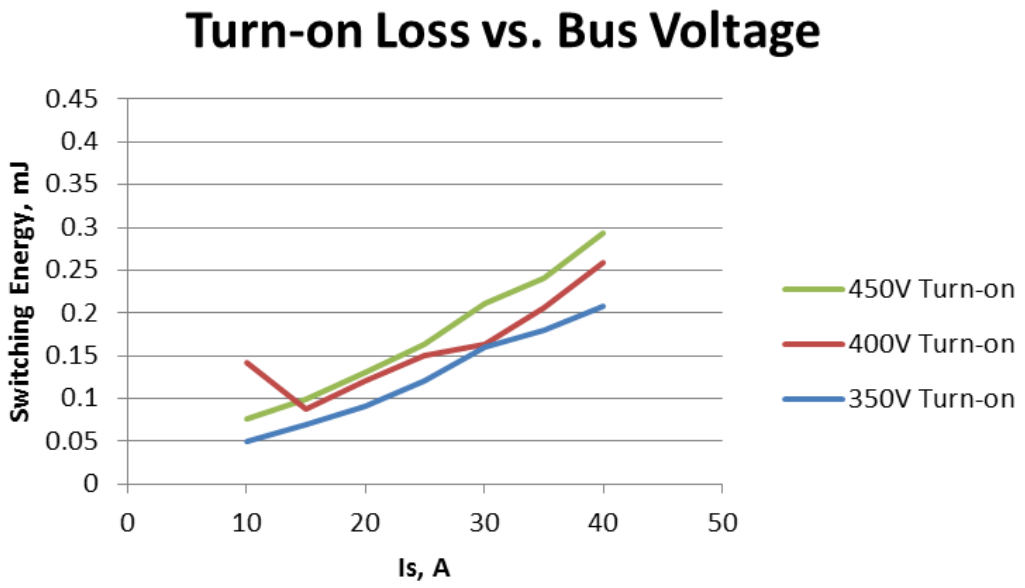

Figure 67: Turn-on switching energy of the CoolMOS device

The turn-on loss oddly went down and then back up during the test. The voltage dip that usually occurs when the device turns on, did not appear during this capture. Further testing may show that the 400 V 10 A case to actually be around .06 mJ.

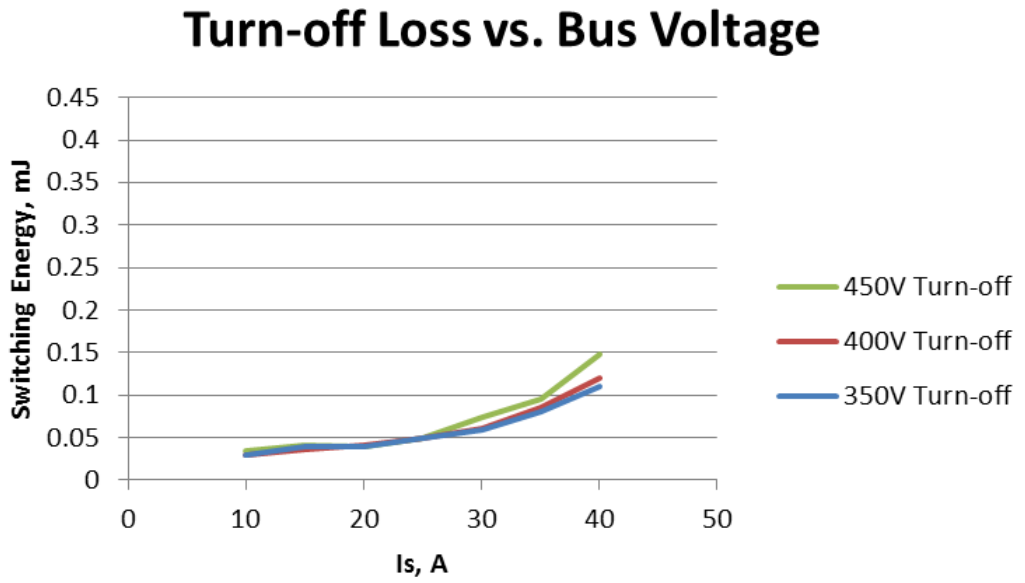

Figure 68: Turn-off switching energy of the CoolMOS device

Vishay Siliconix: SiHG47N60S

Vishay's device rings for the least amount of time on the turn-off waveform. The results turned out consistently

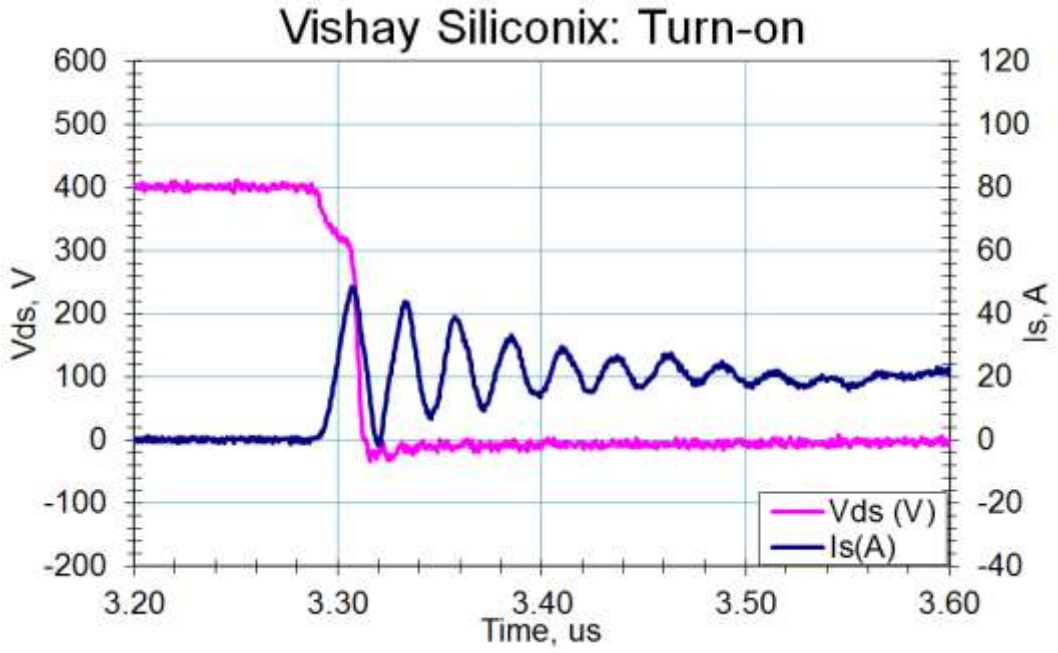

Figure 69: Vishay Siliconix turn-on waveform

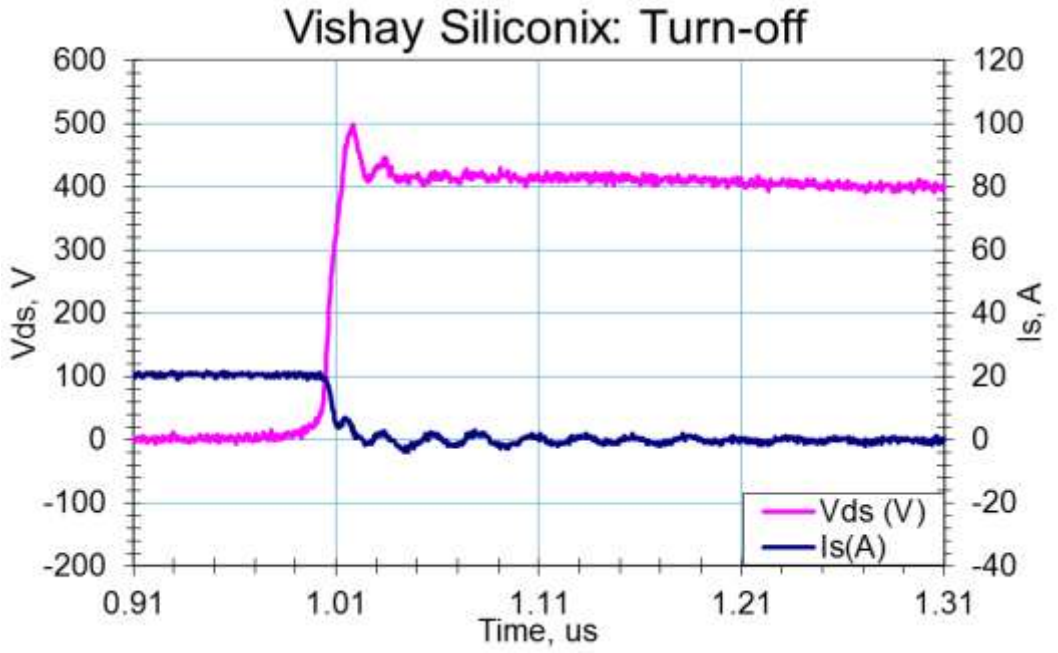

Figure 70: Vishay Siliconix turn-off waveform

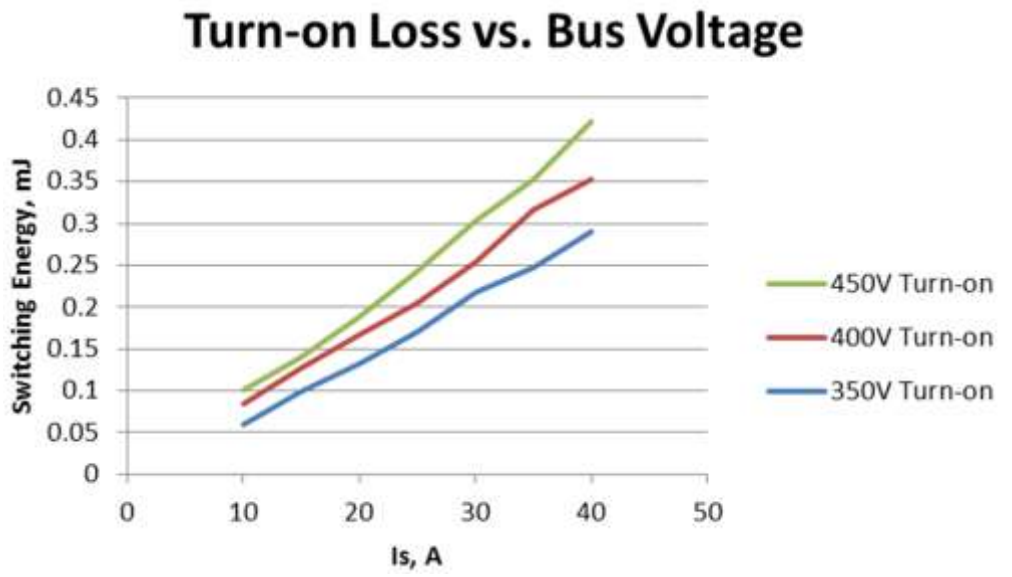

Figure 71: Turn-on switching energy of the Vishay device is shown.

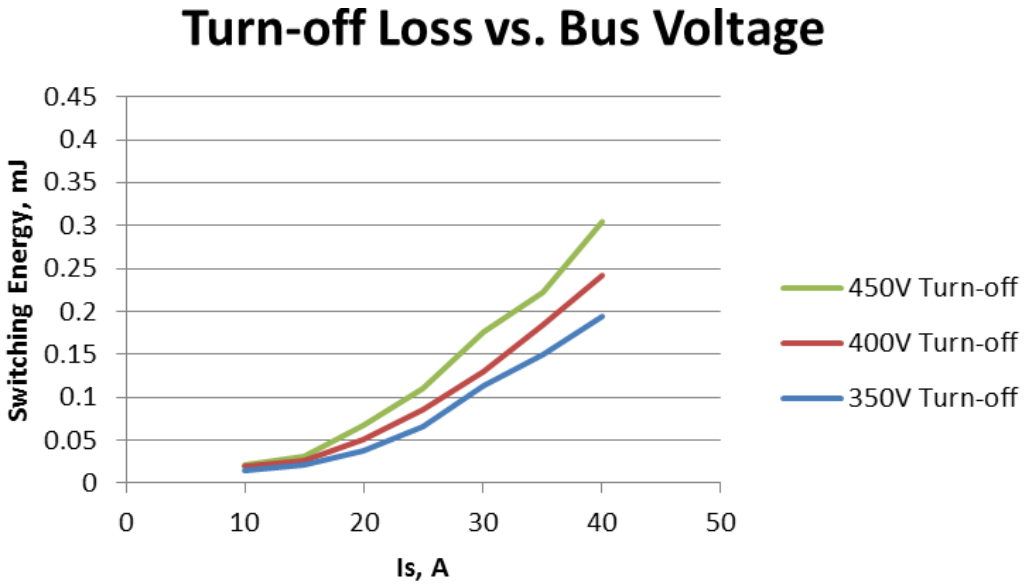

Figure 72: Turn-off switching energy of the Vishay device is shown.

Body Diode Reverse-Recovery Characteristics

Although reverse-recovery datasheets state reverse-recovery times as hundreds of ns, the actual consequences of the device switching is shown below. It should be noted that the turn-off resistance is 94 Ω and is unreasonably large. The purpose of this record is just to emphasize that reverse recovery can increase rectifying time or device-off time and enlarge turn-on time a significant amount. It is stated in power-electronics courses that Schottky devices should be chosen and it has been emphasized why this is the case with a large turn-off resistor. A smaller turn-off resistor would increase the current spike even more. The datasheets for these devices can be seen on Infineon's website [18], [20]. The second waveform shows the faster body diode; however it seems that the device turns on slower than the regular CoolMOS in the drain-source voltage waveform for the sake of a lower and softer current spike.

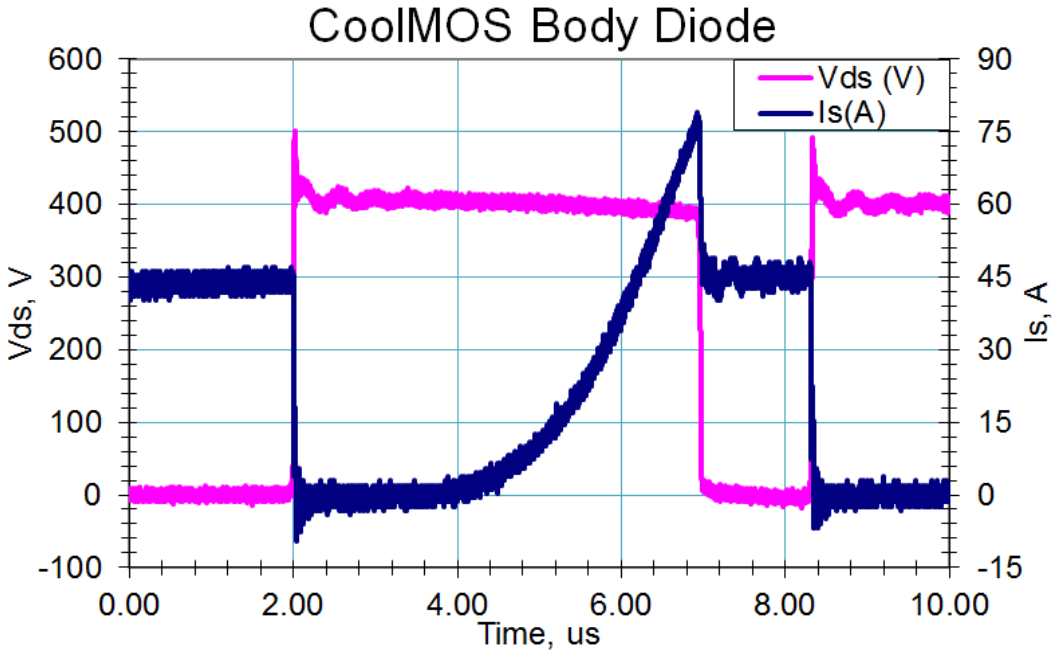

Figure 73: CoolMOS body diode reverse recovery

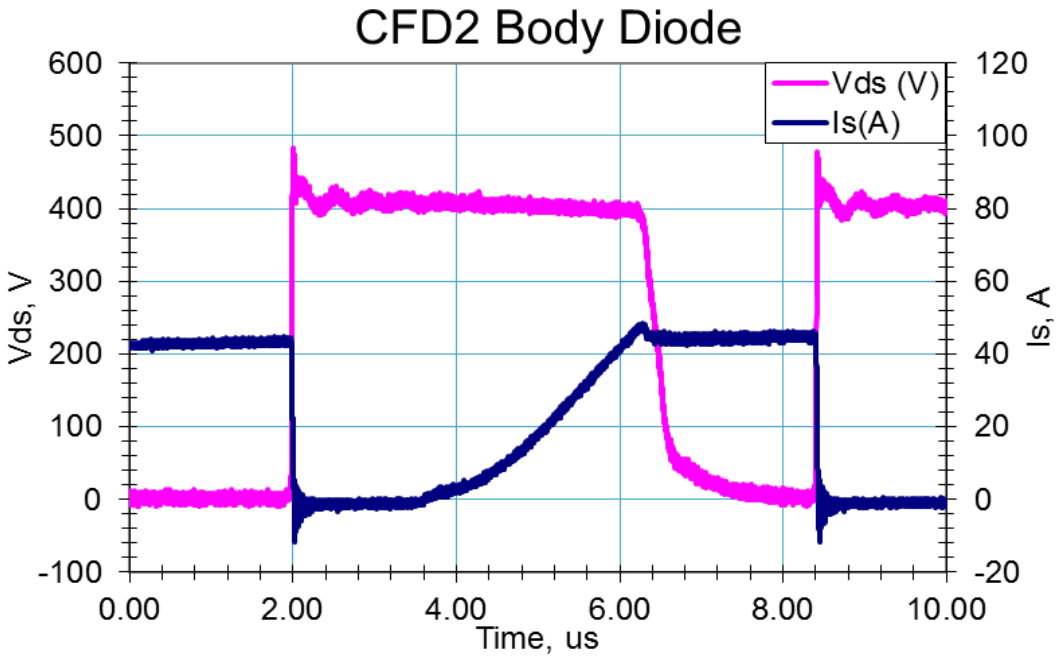

Figure 74: CFD2 body diode reverse recovery

Summary & Conclusions of PCB Testing

	Z-FET CMF20120D	MDMesh STW77N65M5	SupreMOS FCH76N60N	CoolMOS IPW60R045CP	Vishay SiHG47N60S
Turn-on dv/dt, V/ μs	-12,700	-35,700	-23,100	-57,400	-49,300
Turn-off dv/dt, V/ μs	21,700	38,100	37,400	41,800	37,200
Turn-on di/dt, A/μs	930	4,040	8,260	4,170	2,470
Turn-off di/dt, A/μs	-3,310	-1,110	-2,720	-2,610	-1,260
Turn-on Loss Range, mJ	0.10 – 0.43	0.07 - 0.40	0.03 – 0.31	0.05 – 0.29	0.06 – 0.42
Turn-off Loss Range, mJ	0.02 – 0.08	0.05 – 0.35	0.04 – 0.30	0.03 – 0.15	0.01 - 0.30
Total Switching Losses, mJ	.12 – 0.51	0.12 – 0.75	0.07 – 0.61	0.08 – 0.44	0.07 – 0.72

Table 5: Table of device losses, loss ranges are given for devices under 400V and 10-40A switching conditions (Z-FET is under V_{gs}^{+}=20V, V_{gs}^{-}=-3.3V, $R_{g\ on}$ = 9.1 Ω, and $R_{g\ off}$ = 6.8 Ω. All other switches under V_{gs}^{+}=15V, V_{gs}^{-}=0V, $R_{g\ on}$ = 0 Ω, and $R_{g\ off}$ = 5.1 Ω) di/dt and dv/dt have been measured at 400V 20A

CoolMOS defended its title as the benchmark Si MOSFET, at least when 15-V $V_{gs\ on}$, 0-V $V_{gs\ off}$, 0 Ω turn-on resistance, and 5.1 Ω turn-off resistance. It should be noted that the Cree Z-FET was not tested under the same conditions as the other devices. Its V_{gs} and R_g were both higher than Si MOSFET testing

conditions. In fact, if the device were tested under similarr $\frac{V_{gs}}{R_g}$ conditions, it may be even more competitive than the CoolMOS device. This device was tested at 20.2-V $V_{gs\ on}$, -3.3-V $V_{gs\ off}$, 9.1 Ω turn-on resistance, and 6.8 Ω turn-off resistance.

The PCB allowed the experimenter to replace and compare multiple devices under the same gating conditions. This came at a cost of higher loop inductance. Previously the pins of each component were directly soldered to the necessary components. This resulted in lower parasitic inductance and higher ringing frequencies. When the test setup was run with the FFB capacitor that was previously used, the power loop inductance L_l was still too great and created voltage spikes that tested the safe rectifying voltage of the switches.

Lower inductance was necessary so paralleled ceramic capacitors were used to decrease the high-current series inductance contributed by the FFB capacitor. The FFB was eventually taken out and 5 1000V 0.1 μF ceramic capacitors were used in parallel to reduce the inductive voltage spike to a safer operating area.

IV. A Reflection on Device Testing & Future Work

Careful design of the testing circuit must be taken into consideration in order to obtain accurate and meaningful results. This was achieved through short traces, traces that overlapped their respective return paths (reduces parasitic series inductance), high isolation (low common-mode capacitance) to prevent ground loops, voltage probe measurement and calibration, and proper current probe selection. A high-voltage capable voltage probe was measured against a BNC cable from a function generator to find the difference in measurement delay. The delay was taken into account in order to obtain meaningful switching-loss information. Three different current monitors were compared to find the most accurate measurement device. The Rogowski coil, Pearson, and CVR were all used to measure the same current. It was decided that the CVR had the quickest response or highest bandwidth. Combining these two with a high sampling-rate oscilloscope enabled the experimenter to take voltage and current measurements with confidence. This device tester allows both current-controlled and voltage-controlled power switching devices. It also allows for package flexibility and various gate voltages; featuring separate high and low-side regulators and allowing zero or negative gating.

Major Findings

1. **Turn-on Loss:** Turn-on is slowed down by L_s and C_{dg}, since the di/dt creates a voltage that opposes gate charging and the Miller capacitance tries to discharge the gate. Most of the ringing is caused by L_s, L_l, and C_j of the freewheeling diode.

2. **Turn-off Loss:** The turn-off is slowed down by L_s and C_{dg} because the di/dt causes a voltage that fights gate discharge and the reverse capacitance attempts to energize the gate. The oscillation's source is the resonance between L_l and C_{ds}.

3. **Parasitic Effects:** Even though the current shunt itself has little parasitic inductance, it has leads that add insertion inductance. Adding the shunt into the device testing unit also adds insertion inductance since the current shunt must be added to the high current path. In order to decrease device lead inductance, the wider pants of the leads were thinned in order to place the devices closer to the board. This also decreases the likeness of the device test setup to implementation in the field. Future work could include research in current measurement techniques with lower insertion inductance. It has been determined that the preliminary switching configurations can provide the least loop inductance; however, this provides configurations that are not practical in mass-produced design. It would not be cost-effective and possibly not as reliable. For this reason a PCB was made to emulate reasonable circuit design in power circuits. Parasitic inductance has been described in **[6]**. Chen states that the gate inductance is the greatest in magnitude followed by the source inductance and lastly the drain inductance. This statement is supported by the finding in Figure 75. This shows that there is no bonding present between the drain pin and the tab. Figure 76 shows the difference in wire bonding between the source pin of the Vishay device and the ST device. The small mark on the Vishay device shows that the wire bond is smaller in

width than the ST bond. Wider wires and traces should describe lower resistance and lower inductance paths. This explains the higher turn-on di/dt of the ST device than the Vishay.

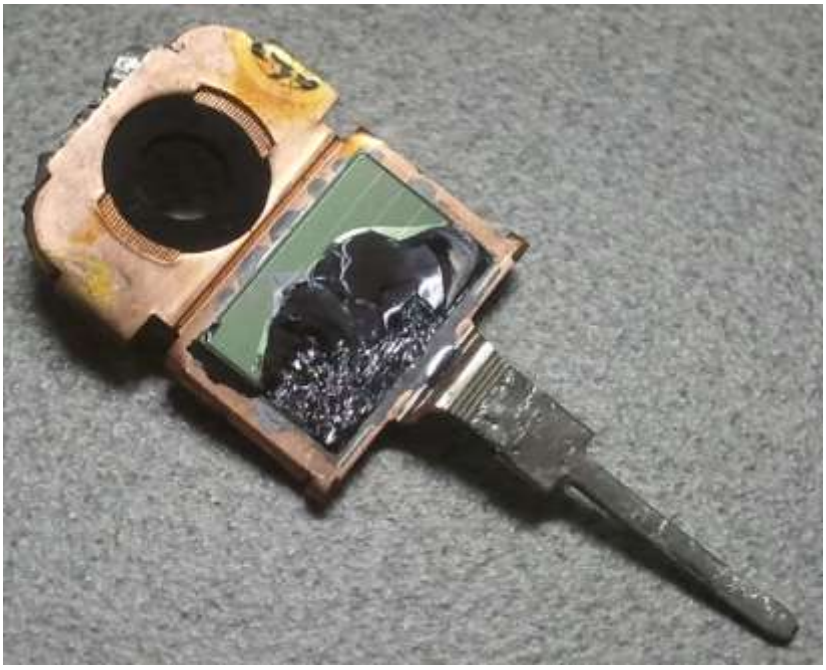

Figure 75: Drain pin attached to tab with damaged die

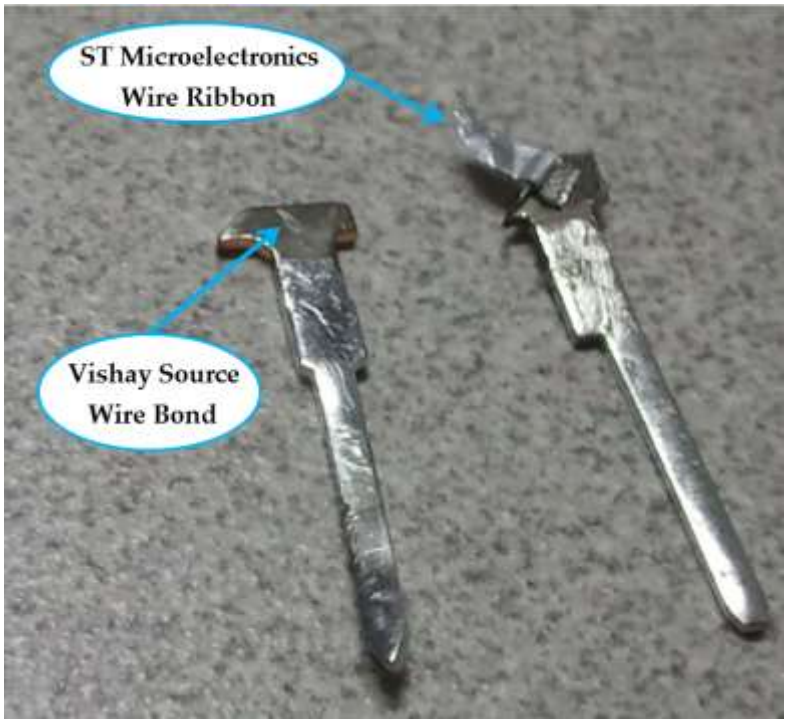

Figure 76: Source legs of TO-247 MOSFETs, the ribbon on ST's source pin is 55 mil across, 5 mil thick, and 155 mil long

Although each TO-247 package was installed in the same manner and since the packages look similar with similar leads. These competitors have different wire-bonding technologies. These affect switching performance through differences in inductive overshoot, as well as decreased gate charging ability. This level of scrutiny could provide semiconductor companies with a more competitive edge, but only if they can advertise their advantages with detailed and concise application notes. Cree has done the best job of informing the reader, but still can provide more detailed and improved device knowledge. If the manufacturers of these devices can market this level of detail; it would most certainly makes it an easier sell. Although ballpark figures can be given for lengths of traces and inductance; actual inductance measurements written in the device datasheet could instill greater confidence in using the product. That would circumvent this issue of pulled traces. If the board were to be redone, the holes should be larger to accommodate the pant width and the device would be dropped in totally flush with the board without modification. Larger through holes would ease swapping devices. Ceramic bypass capacitors would also be placed on board in place of the film capacitor.

Major Contribution to the Power Electronics Field

- Switching behavior of SiC devices has been characterized for recently (within last 6 months) commercially available devices
    - Cree Z-FET 1200V, 33A, 80mΩ
    - GeneSiC GA100XCP12-227 1200V, 100A IGBT with co-pack SiC diode
    - GeneSiC A-GA10JT12 1200V, 7A normally-off superjunction transistor
- Benchmark Si superjunction power MOSFETs have been characterized under the same conditions and compared to each other
    - ST MDMesh STW77N65M5 650V, 69 A, 38 mΩ
    - Fairchild SupreMOS FCH76N60N 600V, 76 A, 36 mΩ
    - Infineon CoolMOS IPW60R045 600V, 60 A, 45 mΩ
    - Vishay Siliconix SiHG47N60S 600V, 47 A, 70 mΩ

Future Work

The same device tester can be used to rate ultrafast-diode or body-diode switching performance as well. This could clearly show increases in turn-on loss due to reverse-recovery or evaluate the junction capacitance of the diode.

More studies can be performed on device failure. After much study, one could possibly describe the tendencies of the switch to fail with overvoltage, overcurrent, or gating issues. Horrowitz and Hill have shown ESD (electrostatic discharge) failures of the gate [23]. It would be interesting to find out which failure occurs most often and how to circumvent this. This could include device degradation studies over the lifetime of the device and include which gate drive techniques are most robust and which gate voltage is the best compromise between gate drive loss, switching loss, and lifetime of the system. Fixing the switching and freewheeling device and focusing on gate drive technologies and aspects along with finite

element simulation could decide whether a standardized gate drive layout can be made to drive MOSFETs.

This setup can also be created for use with surface mount devices. However this would amplify the effects of adding parasitic inductance, since the parasitic inductances would be low to start with compared to TO-247/medium-power devices. Some packages that would be interesting to test would include NXP's LF-PAK (loss-free pak) [22] and IXYS's DE-package [23] with field canceling effects for use in the MHz range.

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