

# **Microstructural Evolution in Thermally Cycled Large-Area Lead and Lead-Free Solder Joints**

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by  
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## **Abstract**

Currently, there are two major driving forces for considering alternative materials to lead-based products, specifically interconnections, in electronics applications, including the impending legislation or regulations which may tax, restrict, or eliminate the use of lead and the trend toward advanced interconnection technology, which may challenge the limits of present soldering technology. The reliability of solder joints is a concern because fracture failures in solder joints accounts for 70% of failures in electronic components. Lead-free solders are being investigated as replacements for lead solders currently used in electronics. Thermo-mechanical properties describe the stresses accumulated due to thermal fatigue as a result of CTE mismatch within the system. By understanding the failure mechanisms related to lead-free solders, the application of lead-free solders could be more strategically designed for reliability.

The objective of this thesis is to observe microstructural change in large-area solder joints caused by thermal cycling and relate these changes to reliability issues in large-area lead and lead-free solder constructed semiconductor power devices. This study focused on the microstructural changes within the solder alloy of a large-area solder joint under thermal cycling conditions. Two primary observations were made from this research, they are: 1) due to a combination of testing conditions and material properties, the lead-free solders, Sn/3.5Ag and Sn/Ag/0.7Cu, sustained the most severe damage as compared to Sn/37Pb solder alloy, and 2) the most severe damage was observed at the solder/substrate interface in a simulated power semiconductor device sample due to elevated stresses gradients across the solder layers.

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# 1 Introduction

## 1.1 Motivation

The driving forces for the microelectronics industry today involve the increasing circuit density at the semiconductor level, environmental and health issues over the life of the devices, and global competition in quality, reliability and cost. The increase in the use of electronics within industry as well as personal use has been growing exponentially over the past few decades. Today many electronic devices, most specifically consumer devices, are considered disposable because of the introduction of newer, faster technologies each year. Hence, these devices generally end up in landfills. Even with recycling or reclaiming programs, most circuit boards are too complex to disassemble to reclaim the materials. The trend being set by some of the major countries in the world is to eliminate the use of lead in consumer products for health and environmental reasons.

Contained within most electronics is the element lead related to the solders and finishes on the electronic components. There is a concern that these materials are considered toxic because there is the potential for leaching from landfills into water sources becoming a hazard to human health and the surrounding environment. The most aggressive and well-known effort is the European Union's Directive for Waste Electrical and Electronic Equipment (WEEE) proposed to come into effect 1 January 2006.<sup>i,ii</sup> This legislation will limit the disposal of hazardous materials by eliminating certain materials from electrical and electronics products. The Japanese Environmental Agency has proposed that lead-containing scrap must be disposed of in sealed landfills to prevent lead leaching. In addition, the Japanese Ministry of International Trade and Industry and the Japan Automobile Industries Association have called for a 50% reduction of lead in vehicles (excluding batteries) by 2001 and a 33.3% reduction by 2003.<sup>iii</sup> Consequently electronics sold by the United States and other worldwide electronics producers to these countries must meet lead-free standards to maintain trade.

The United States is the largest consumer of lead in the world. Globally, about 100,000 tons is produced per year and about 60% goes into electronics.<sup>iv</sup> Of that statistic, the United States uses 40%, or 24,000 tons, annually.<sup>iv</sup> However, the total annual statistic shows that the United States electronics industry uses less than two percent of the world's lead consumption and electronics manufacturing accounts for only 0.6% of the annual lead consumption.<sup>iii</sup> Nevertheless, the trend being set by some of the major countries in the world is to eliminate the use of lead in consumer products for health and environmental reasons.

The electronics industry is concerned with the elimination/reduction of the use of many important materials. The Institute for Printed Circuits (IPC) board of directors issued a statement

regarding their position on lead-free electronics in response to “scientific evidence and US government reports indicating that lead used in US printed wiring board (PWB) manufacturing and electronic assembly produced no significant environmental or health hazards.”<sup>iii</sup> The statement follows that “nonetheless, in the opinion of IPC, the pressure to eliminate lead in electronic interconnections will continue in the future from both the legislative and competitive sides. IPC encourages and supports research and development of lead-free materials and technologies.”<sup>iii</sup>

The proposed WEEE Directive was drafted for the intent of protecting human health and the environment as required by Article 174 of the European Community Treaty (EC Treaty).<sup>i, v</sup> The WEEE Directive seeks to minimize the use of certain dangerous substances (including lead), to increase the use of recyclable materials, to design for upgrade, reuse, ease of disassembly and recycling, to set up systems for free take-back at end-of-life, and to insure that the cost of collection, treatment, recovery and environmentally sound disposal is borne by the producers.<sup>vi</sup> The proposal essentially requires that lead must be replaced with alternative materials in the production of electrical and electronic products. Specifically for the electronics manufacturing industry, this has required much research and modification to existing processes. A prospective paper was written on the WEEE Directive proposed legislation found in Appendix D.

Currently, the industry is in compliance with existing legislation internationally (US EPA, Australia, Denmark, Sweden), which addresses environmental and health issues associated with lead.<sup>iii</sup> Since the request for the WEEE Directive in 1986, trade and research organizations within the industry began to create task forces to research the issues of replacement of lead (IPC, EIA, NCMS, NEMI, NIST, PCIF, ITRI).<sup>iii</sup> Thus far, the industry and other organizations have determined that there are no viable alternatives available for complete, direct material replacements.<sup>vii,iii, viii</sup>

Because lead in the electronics industry is so widely used, the push to remove lead from electronics is an extensive, international issue. The most efficient solution would be to find a direct substitute for leaded solders. The compositions for lead-free solders as replacement for eutectic 63 Sn- 37 Pb solder have been proposed and generally accepted by industry thus far. The National Electronic Manufacturers Institute (NEMI) has recommended for use by industry as a standardized lead-free solder alternative: Sn/3.9Ag/0.6Cu for reflow soldering and Sn/0.7Cu or Sn/3.5Ag for wave soldering processes.<sup>ix, iii, x</sup> However, there is a general lack of engineering information about lead-free alloys with respect to manufacturing and reliability/performance in electronics applications.<sup>ix, iii, x</sup>

The reliability of solder joints within electronic systems is an issue that affects all aspects of production and use stages. The ability to predict the reliability and lifetimes of solder joints is a

priority, specifically with the introduction of new solder compositions. Fracture failures in solder joints accounts for 70% of failures in electronic components.<sup>xi</sup> As a result, the mechanisms of failure are of interest. Many reliability issues in electronics relate to mechanical strengths, fatigue resistance, coefficient of thermal expansion, microstructural changes and intermetallic compound formation. Specifically, the area of thermo-mechanical reliability is an issue in which more research is needed so that industry may understand and implement lead-free solders into electronic devices.<sup>iii, xi, vii</sup> Thermo-mechanical properties describe the stresses accumulated due to thermal fatigue as a result of CTE mismatch within the system. The effects of solder properties and microstructures, which vary with composition, with temperature and strain during the life of the component must be predictable. Hence, by understanding the failure mechanisms related to lead-free solders, the application of lead-free solders could be more strategically selected and designed for specific applications.

Dislocations inherently exist in all materials; therefore, the root cause of reliability issues in electronics, specific to this study of solder joints, can be related to the behavior of materials. However, because dislocations are a natural part of crystalline materials, the dependent factor that can be controlled is the applied stress (Figure 1.1-1). An understanding of plastic deformation and the relationship between dislocations and applied stress will better relate these effects, cracking, to the operational issues or the reliability related to the function of the material in its application. Hence, the study of microstructural evolution under specific conditions will contribute to this understanding.

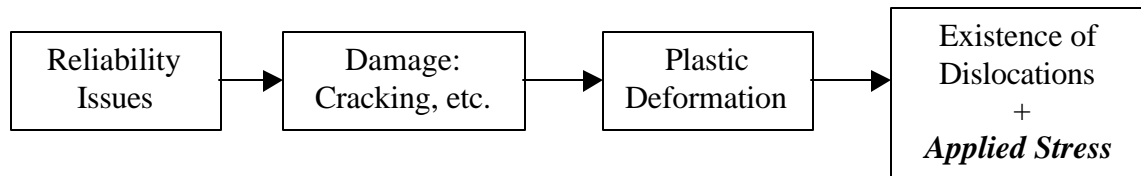


Figure 1.1-1: Schematic of the relationship between reliability issues and material behavior.

## 1.2 Objective

The objective of this thesis was to observe microstructural change in large-area solder joints caused by thermal cycling and relate these changes to reliability issues in large-area lead and lead-free solder constructed semiconductor power devices. This study focused on the microstructural changes within the solder alloy of a large-area solder joint under thermal cycling conditions.

## 2 Procedures

### 2.1 Sample Preparation

#### 2.1.1 Device Construction

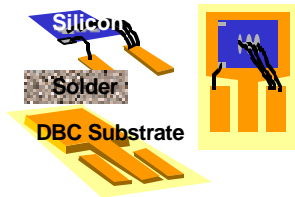
Several types of samples were created during this study. All of the samples focused on the study of a variety of solder types. The sample types ranged from bulk samples in the form of large solder balls to working packaged power devices to solder reflowed alone on a DBC substrate. The reflow processes for each of the sample types was the same. The materials used for each of the sample types were all from the same original materials ordered. For instance, the solders used for each of the samples from the solder balls to the power devices were from the same supply sent by Kester Solder. The sample construction types are outlined in Table 2.1-1.

**Table 2.1-1: Sample construction types used in this study.**

Sample Type	Solder Alloy	Substrate Material	Comment
Solder Ball	37Pb Sn/3.5Ag Sn/Ag/0.7Cu Sn/5Sb CASTIN	No Substrate	Bulk Samples
Solder/DBC	Sn/37Pb Sn/3.5Ag Sn/Ag/0.7Cu	Ni-plated DBC	No Silicon Die
1 <sup>st</sup> Generation Power Device	37Pb Sn/3.5Ag Sn/Ag/0.7Cu Sn/5Sb CASTIN	Plain Copper DBC	A silicon die was attached to the DBC using various solders.
2 <sup>nd</sup> Generation Power Device	37Pb Sn/3.5Ag Sn/Ag/0.7Cu	Ni-plated DBC	A silicon die was attached to the DBC using various solders.

The power semiconductor packages that were constructed are simple structures each built with a single MOSFET die and either a plain Cu DBC substrate or a Ni-plated DCB substrate (Figure 2.1-1). The MOSFET and DBC substrates were obtained from IXYS Corporation. Five different solders were used as the variation for the reliability study obtained from Kester. Nickel-plated DCB substrate was chosen to reduce intermetallic growth generated during the reflow of solder to the substrate.<sup>xii</sup> The devices were wirebonded at the Orthodyne Corporation with 10 mil aluminum wires, using an ultrasonic wirebonding method. To protect the silicon die surface from environmental and mechanical damage during testing, the devices were

encapsulated. The encapsulant was a low viscosity epoxy selected from the Loctite electronic encapsulation products: 3532 and 3534, which cured at 90°C for approximately 30 minutes.



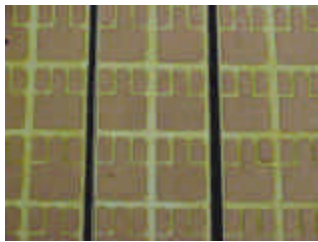
Solder Alloy	Melting Point
Sn/37Pb	183°C
Sn/3.5Ag	221°C
Sn/3.8Ag/0.7Cu	217-220°C
Sn/5Sb	232-240°C

**Figure 2.1-1: Device assembly schematic.**

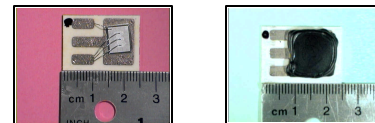
Device construction followed a typical schedule. Designing and producing the substrate pattern, placing the solder and die on the substrate, reflowing the solder, wirebonding, and encapsulating. There were numerous cleaning processes done throughout the construction of these devices. The major steps during the construction process are listed in order in Table 2.1-2.

**Table 2.1-2: Major steps in the construction process listed in relative order.**

Construction Steps	
1) Create photo etch pattern	7) Placement of MOSFET and solder
2) Etch copper on the DBC (Figure 2.1-2)	8) Reflow Process
3) Cut substrates apart – laser cutting	9) Clean modules
4) Clean DBC	10) Wire bond (Figure 2.1-3)
5) Cut and clean perform solder	11) Encapsulate (Figure 2.1-3)
6) Apply flux to solder	



**Figure 2.1-2: DBC substrate after pattern has been etched.**



**Figure 2.1-3: (Left) Device after wirebonding; (Right) Device after encapsulation**

A belt oven was used for the reflow process (Figure 2.1-4). The oven was characterized using thermocouples to create thermal profiles for each solder reflow schedule in coordination with the solder manufacturer’s recommendations. Figure 2.1-5 shows, on the left, the profile provided by Kester for eutectic Sn/37Pb solder. On the right is the profile used to reflow the devices containing Sn/37Pb solder for this research. In addition, visual verifications of the reflow process were used to gauge the success of the profile. A piece of solder, with flux, was placed on a plain piece of copper DBC and run through the profile. The solder was expected to

burn off the flux prior to reaching 180 °C and melt at the peak temperature ranging from 180 °C to 215 °C for eutectic Sn/37Pb. The melt was also supposed to appear as though a wave of heat went across the solder. So the edge of the solder that moved onto the hottest portion of the belt first would melt first. This reflow characterization process was repeated for each of the solder alloy used in this study to determine the reflow profiles.

The samples were all cooled in air over a fan-cooled heat sink located at the end of the belt oven. A nitrogen atmosphere was used for the first generation power devices, however, there did not seem to be much of a different in the sample construction with the second-generation devices that were reflowed in air. This may have been due to the fact that the belt oven used did not have a sealed cover for the nitrogen atmosphere.



Figure 2.1-4: Reflow belt oven.

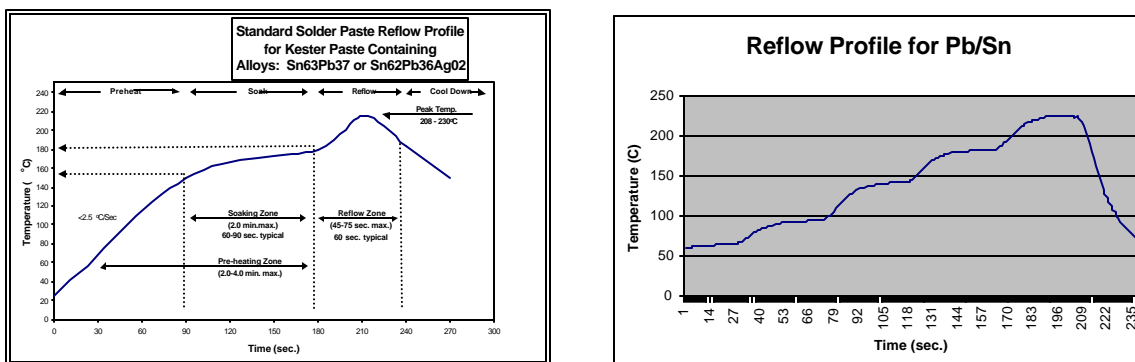


Figure 2.1-5: (Left) Manufacturer's suggested reflow profile for Sn/37Pb; (Right) Profile used for this research when processing Sn/37Pb soldered devices.



## 2.1.2 Metallurgical Sample Preparation

The devices constructed for this study were sectioned and polished for observation under optical microscopy, SEM, and Electron Microprobe. For the majority of the observations made, a flat, clean, scratch-free surface was required. Metallographic sample preparation techniques were developed for these samples. A discussion of the electron beam analysis techniques is in the Appendix C.

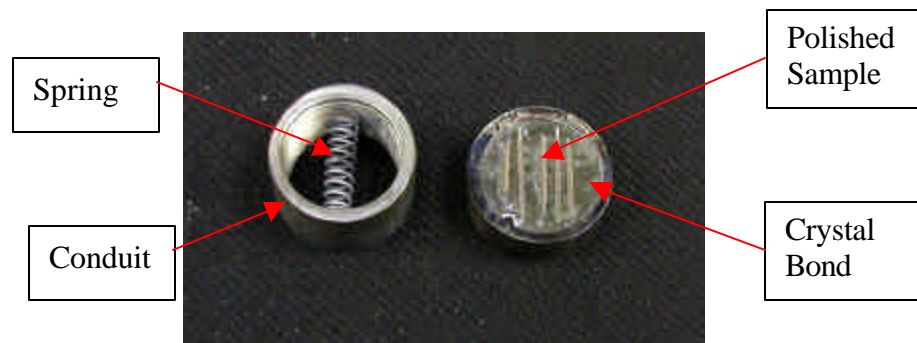
The samples are essentially composites containing both hard and soft materials in contact. Therefore, the challenge of the sample preparation was to focus on the material of interest, in this case the solder layer. The solder layer was composed of an Sn-based, soft material approximately 0.005 mm thick. The adjacent materials were silicon and copper of .82 mm and 0.32 mm thick respectively with a layer of alumina, 0.635 mm thick below the copper layer. For composite samples of both soft and hard materials, degrading fixed abrasives should be used for the grinding steps.<sup>xiii</sup> Bonded fixed abrasives should not be used for soft materials. Since the material of interest in this study is a soft solder layer, silicon carbide and aluminum oxide abrasives for both grinding and fine polishing, respectively, were chosen. Diamond abrasives were used for the rough polishing steps.

### 2.1.2.1 Sectioning and Mounting

The devices were sectioned using a slow speed diamond saw using moderate pressure for cutting. The devices were sectioned with the silicon against the blade. The assumption was that this would put more compressive like stresses on the silicon while cutting to avoid cracking in this brittle layer. The blade would cut through the layers in the following order: silicon, solder, copper, alumina, and copper. Since the assumption was that the first layers would see more compressive like stresses, than the final layers would likely see tensile stresses. This was evident in the condition of the final copper layer after sectioning. The copper layer would generally have an elongated edge where the material was stretched prior to breaking.

During the first processes of sample preparation, the samples were mounted in a permanent, slow-cure, two-part epoxy. Because the samples were to be thermally cycled, there was concern that the epoxy mounts could not survive testing and would impose excess stresses on the samples. So, for the final preparation process that was established, the samples were then mounted in a specially designed mount. These mounts used Crystal Bond as the molding material, which could easily be disassembled by dissolving away the Crystal Bond in acetone.

The mounts were made of electrical conduit, which had been cut in half and polished smooth on one side (Figure 2.1-6). The conduit was found to fit into the automatic polishing fixture perfectly. Springs were then placed across the diameter of the conduit inside to keep the samples vertical. The samples were placed vertically in the springs with the side of interest facing up. Kapton tape was placed over the top of the conduit. The whole assembly was then flipped and the side with the Kapton tape was placed on a flat surface. Tweezers were used to manipulate the samples such that the side of interest was against the flat surface. The tape held the sample in place and the spring kept the samples from tilting off vertical. The crystal bond was then heated in a beaker on a hotplate to approximately 150 °C, or until fully melted. The sample assembly containing the samples was placed on the hotplate for approximately 15 seconds to warm the metal conduit and the spring. The Crystal Bond was then poured over the samples until all spaces between the samples and the conduit were filled. The Kapton tape kept the Crystal Bond from running out of the bottom of the assembly. The whole assembly was then promptly removed from the hotplate and placed on a flat block of aluminum until cooled. In total the assemblies were on the hotplate for no longer than 45 seconds. The tape was then removed and the samples were ready to be polished. Crystal Bond was chosen as the mold material because the samples could be removed by placing the whole assembly in acetone. The Crystal Bond would dissolve away and the samples could be retrieved.



**Figure 2.1-6: Specially designed sample preparation mounts, (left) conduit and spring assembly, (right) assembly ready for polishing containing five samples and Crystal Bond.**

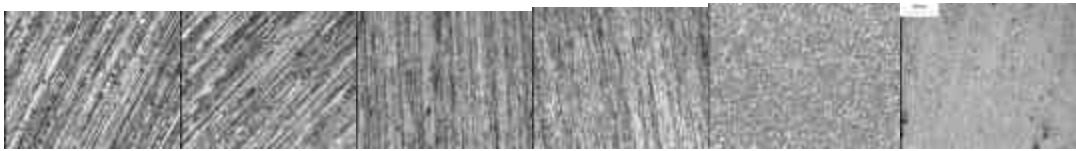
### *2.1.2.2 Grinding and Polishing*

Each sectioned device was then mounted, ground until flat, polished and then attach polished to reveal some of the microstructure details. Several methods and techniques were tried before an appropriate process was developed for these samples. In all cases an Isomet Buehler Diamond Saw and an Ecomet Buehler Automatic Polisher was used for preparation. Through

experience, settings such as speeds and pressures were determined for the preparation of these samples.

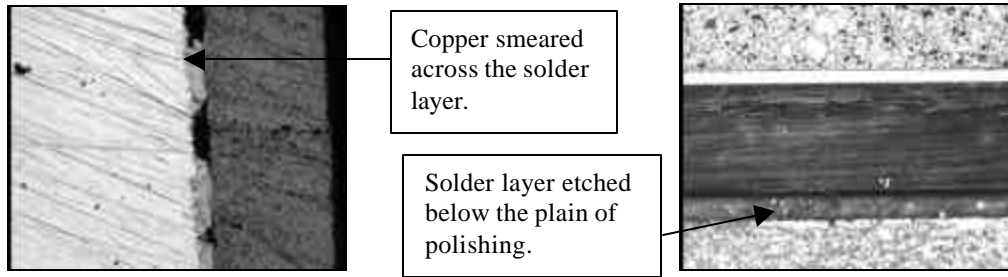
Grinding and polishing steps should be controlled such that deformation from previous steps is removed. Decreasing abrasion and polishing rates at each step through the control of grinding and polishing surface, abrasive, pressure, speed, and chemical reactivity, for example pH, accomplish this.<sup>xiv</sup> Both grinding and polishing produce the same basic phenomena: the production of scratches or grooves, material removal, and the production of a plastically deformed layer at the immediate surface. The difference between grinding and polishing is the extent to which these features are produced.

Initially, several samples containing 92.5Pb/Sn were prepared. These samples were sectioned as mentioned above, mounted in a slow-cure epoxy using a vacuum impregnation process. They were ground using 320-grit to 600-grit paper. The samples were then polished using 9 micron then 3 micron diamond pastes on a low to medium nap polishing cloth and an alumina/water solution as lubricant. The samples were then fine polished using a 1 micron then a 0.5 micron alumina/water solution on a tight weave cloth. Finally, several etchants for Pb and Sn-based materials were tested. Figure 2.1-7 illustrates the process of grinding and polishing with the reduction in damage from coarse grinding from 400-grit to fine polishing.



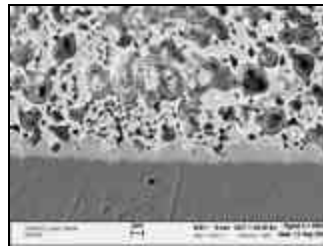
**Figure 2.1-7: Optical micrograph images at 10x magnification of the grinding and polishing steps for Sn/37Pb alloy. (Left to Right: 400 grit, 600 grit, 3 micron, 1 micron, 0.05 micron, attach polish)**

Several problems arose with the techniques used for this preparation attempt. Initially the pressures and speeds for the grinding stage were too aggressive and the copper layer was found to smear over the solder layer (Figure 2.1-8). In addition, the etchants were too aggressive for these composite like samples and the solder layers were corroded to well below the polished surface such that they could not be seen with the optical microscope (Figure 2.1-8 and Figure 2.1-10). It was later determined that the copper layer in the samples was likely causing accelerated corrosion through Galvanic corrosion. Copper is more cathodic while tin and lead are more anodic, so the copper in the samples drove the corrosion process of the etchant forward. Therefore, the pressures and speeds for grinding and polishing were modified and etchants were not used in future methods.



**Figure 2.1-8: Optical image of the layered power device with smearing of the copper layer, (left to right) copper, solder, silicon.**

**Figure 2.1-9: Optical image of the layered power device, which has been etched, (top to bottom) epoxy, silicon, solder, copper.**

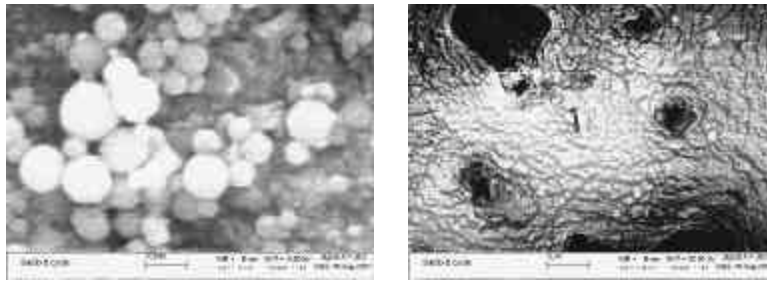


**Figure 2.1-10: SEM image of eutectic SN/37Pb solder after etching; (top) solder, (bottom) copper.**

In addition, it was found that when using the automatic polishing equipment, the samples should remain in the holder for the entire time from grinding through polishing. Traditionally, in order to monitor grinding and polishing progress, the samples are viewed under an optical microscopy between steps. However, when in the fixture for the automatic polisher the samples cannot be viewed under the higher magnification microscope. A lower magnification microscopy was available; however, it did not reveal details during the polishing phase. Therefore, in order to develop a process for polishing using an automatic polishing extra time must be taken initially to determine the process because the samples must be fully prepared before observations could be made.

Several of the first generation samples were sent for preparation at Buehler in order to obtain a second opinion. The samples were mounted in a slow-cure epoxy and then sectioned, sample an epoxy together. They were then ground using 600 grit paper until flat, polished using 9 micron and 3 micron diamond paste. Then an attach polish was used containing 80 ml H<sub>2</sub>O, 100 ml of a colloidal silica solution (Mastermet 2), 20 ml NH<sub>4</sub>OH (ammonia), and 3 drops of 30% H<sub>2</sub>O<sub>2</sub> (peroxide). The samples were viewed using both optical microscopy and SEM with little problem. However, when this process was repeated for several different solder types, the colloidal silica solution became an issue. Even after several cleaning processes, a layer of colloidal silica remained on the surfaces of the lead-free solder alloys. This was not detected using optical microscopy; however, under the SEM the silica would heat up under the electron

beam. The silica was heated such that the solder underneath would melt leaving holes. Hence the attach polish was modified to be used without the colloidal silica (Figure 2.1-11).



**Figure 2.1-11: Colloidal silica on the surface of the solder layer (Sn/5Sb alloy) imaged at 300kx (left) and 30kx (right).**

### 2.1.2.3 Process Developed for this Work

The final process that was developed for the metallurgical preparation of the power devices in this study is as follows (Table 2.1-3):

**Table 2.1-3: Sample preparation process used in this study.**

Step	Abrasive	Surface	Lubricant	Force (lb/sample)	Speed (RPM)	Rotation	Time (min:sec)
Grinding	400 grit		Water	4	220	Contra	Until planar
Grinding	600 grit		Water	5	220	Contra	15:00
Rough Polishing	9 micron	Texmet 1000	Diamond extender	7	120	Contra	8:00
Rough Polishing	3 micron	Texmet 1000	Masterprep*	6	240	Comp	7:00
Fine Polishing	0.05 micron	Texmet 1000	Masterprep*	5	120	Contra	5:00
Attach Polish	0.05 micron	Chemomet	Attach solution				2:30

\* Masterprep is a water-based 0.05 micron alumina polishing solution.

The initial grinding process with 400 grit abrasive usually took 5 or 6 sessions of 30 minute polishes to ensure that all of the samples were planar. Keep in mind that six mounts containing 2 to 4 samples were placed in the automatic polishing fixture. All samples had to achieve the same level, or quality, prior to moving on to the next step. No sample mount could be removed from the polishing fixture until all steps of grinding and polishing were complete.

For the majority of the steps, the samples were rotated in the contrary direction, or rotation of the samples opposing the direction of the polishing media. When grinding in the contrary direction, the unidirectional damage that results is more severe producing a greater stock removal of material.<sup>xiii</sup> During these steps the wheel rotation was kept at 'slower' speeds because the severity of the material removal would have been amplified by an increase in the removal rate controlled by the speed. During the 3 micron polishing step, the samples were rotated in the same direction as the polishing media, the complementary direction. With the increase in speed, removal rates were high due to the speed but the damage to the surface was lowered using the complementary direction of rotation.

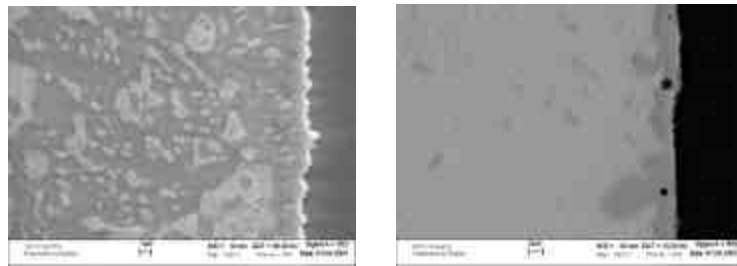
The Texmet 1000 cloth is a medium nap cloth. This cloth is used for all stages of polishing. The polishing cloth trap and supports the abrasive against the sample and must also contain the abrasive so that the abrasive is not rapidly thrown from the wheel. A napped cloth was used to carry the polishing abrasives without the most severe damage, which would occur with a plain smooth surface.<sup>xiii</sup> For rough polishing a low-nap cloth is preferred in order to produce the maximum abrasive contact, high cutting rates, and low relief.<sup>xiv</sup> For the fine polishing that was done in this experiment, a chemical solution was used, so a napless, microporous, chemically resistant cloth was used.

The 9-micron diamond material that was used was a mixture of the diamond oil-based extender solution and the diamond grit. On the other hand, the 3 micron diamond paste that was used required a separate lubricant which was a 0.05 micron alumina solution (Masterprep). The Masterprep solution was also used for the 0.05-micron polishing step.

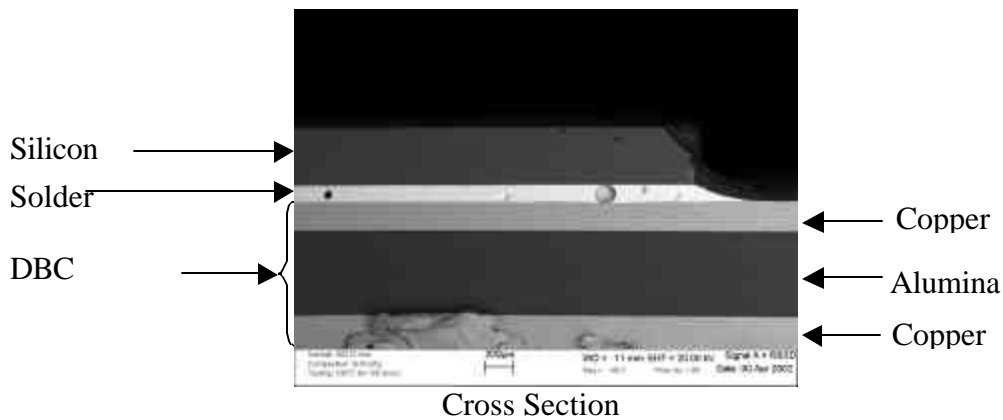
It is considered coarse polishing when the abrasive is 30 to 31  $\mu\text{m}$  and fine polishing is below 11  $\mu\text{m}$ .<sup>xiv</sup> Diamond abrasives are the most widely used rough polishing abrasive and alumina abrasives are the most commonly used for fine polishing. Rough polishing is usually accomplishing using diamond pastes and fine polishing generally uses alumina slurries. The diamond polishes are used as an intermediate step between the harsh grinding and the fine polishing. The diamond abrasive is more aggressive with material removal while the alumina creates less severe scratches, more advantageous at the fine polishing stage.<sup>xiii</sup>

The attack polish was used for the final polishing in this experiment. This process was done by hand because of the nature of the chemical solution. The chemical was to be used under a fume hood because of the ammonia fumes. The samples were left in the polishing fixture to be polished all together. The attack polish solution formula was 80 ml  $\text{H}_2\text{O}$ , 20 ml  $\text{NH}_4\text{OH}$ , 3 drops 30%  $\text{H}_2\text{O}_2$ , and 100 ml Masterprep. An attack polish is simply a dilute chemical etchant added to the polishing media.<sup>xiv</sup>

Between each grinding and polishing step the samples, still in the automatic polishing fixture, were placed in an ultrasonic water bath to be cleaned. The samples could not be cleaned with alcohol or acetone between each step because of the crystal bond mould material. However, after being removed from the mounts, the samples were cleaned with acetone then alcohol and a cotton ball was used to wipe the polished surfaces. The images taken after being prepared with this preparation process revealed microstructural details and intermetallics generated between the solder and the copper substrate during reflow (Figure 2.1-12). Figure 2.1-13 is an SEM image of the cross-section of a tri-layered sample. The SEM images that were taken throughout this document have this orientation at various magnifications.



**Figure 2.1-12: SEM images of Sn/37Pb solder (left) and Sn/3.5Ag solder (right) after sample preparation (solder on the left and copper substrate on the right).**



**Figure 2.1-13: SEM image of the cross-section of a tri-layer sample.**

## 2.2 Testing Procedures

The test samples created for this study were tested via thermal cycling or isothermal aging. outlines the construction of the different samples tested and how they were tested. There were two types of geometries, power devices with MOSFET silicon devices attached to either plain copper DBC or Ni-plated DBC substrates, tri-layer construction. The second geometry was a dual-layer construction with a solder/Ni-plated DBC construction, similar to the power devices

without a silicon die. All of these geometries were tested either via thermal cycling or isothermal aging.

The samples were initially sectioned and polished, prior to testing. This was due to the limited number of samples available. Both the thermally cycled and the isothermally aged samples were removed from the thermal chamber or the oven, respectively, periodically to be imaged using SEM. Therefore, the same samples were imaged multiple times. These imaging periods are outline in .

A scanning electron microscope (SEM) was used to image the samples. Electron dispersive spectroscopy (EDS) was used to qualitatively analyze the composition of the materials of interest. An electron microprobe with wavelength dispersive spectroscopy (WDS) capabilities was also used to study the composition of the materials in this study. A more detailed discussion of these electron beam analysis techniques and some of the findings are discussed in Appendix C.

The thermally cycled samples were testing in a Tenney Chamber, which was programmed to cycle at the maximum rate for the temperature range. The chamber was cycled between -55°C and 125°C with 5-minute hold times at the extremes. Liquid nitrogen was used for some of the cycles during this test. The nitrogen was released into the chamber to accelerate the cooling process. However, the life of one tank was limited, so the use of nitrogen was discontinued. This changed the cycle times from approximately 50 minutes with the liquid nitrogen to approximately 70 minutes without the nitrogen (Figure 2.2-1). In addition, with long-term use of the chamber the cycle times began to increase. At the end of the 350 cycles, the cycle times were closer to 90 minutes (Figure 2.2-2). This may have been due to the fact that as the chamber thermally cycles the samples, it was thermal cycling itself. This has been observed to happen in other Tenney Chambers as well. The isothermally aged samples were placed in small ovens set at a specified temperature. Thermocouples and thermometers were used to monitor the temperature over the testing period. The samples were placed in a preheated oven.

Initially, working devices were created to be power cycled as the method for thermally cycling the materials used in the construction. Problems with the operation of the devices forced the power cycle testing to be discontinued. The details of this work along with a failure analysis of the problems are explored in the Appendix B. Testing for the current work was continued through direct thermal cycling to thermally cycle the materials used in the construction of the devices.



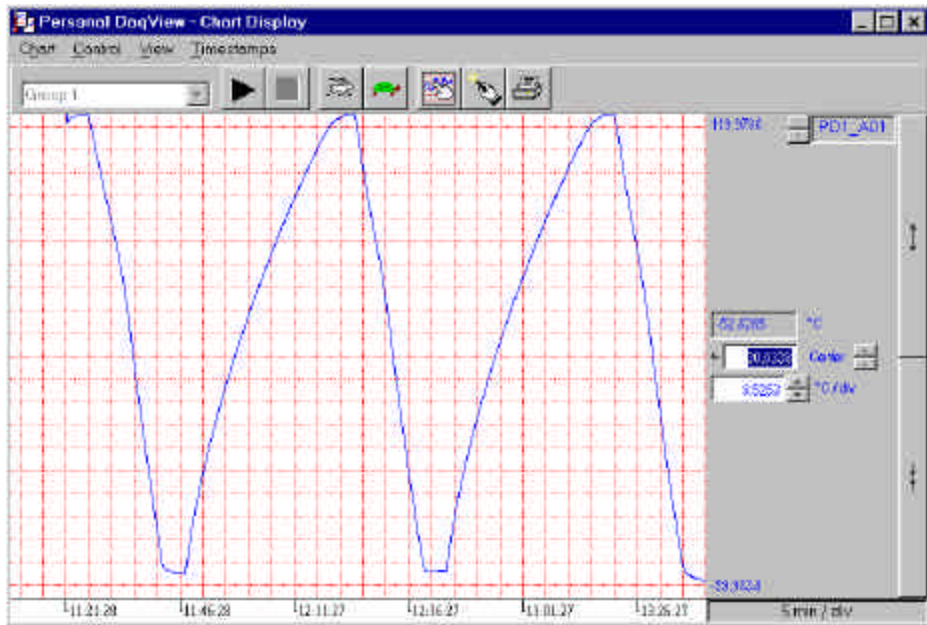


Figure 2.2-1: Initial thermal cycling profile where one cycle is approximately 50 minutes.

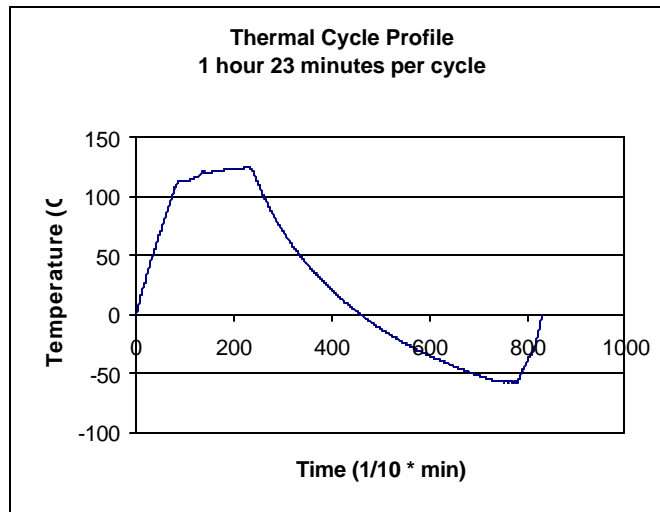


Figure 2.2-2: Final thermal cycling profile where one cycle is approximately 90 minutes.

Table 2.2-1: Outline of sample geometries and testing conditions.

Sample	Solder Type	DBC	Silicon Die	Test Method	Images Taken At
A 07 end	Sn/37Pb	Ni-plated	Yes	TC	60, 120, 350 cycles
A 07 mid	Sn/37Pb	Ni-plated	Yes	TC	0, 60, 120, 350 cycles
A end	Sn/37Pb	Ni-plated	No	TC + Iso	0, 60, 120 cycles + 100, 250 hours @ 125°C
A mid	Sn/37Pb	Ni-plated	No	TC	0, 60, 350 cycles
10313 end	Sn/37Pb	Plain Cu	Yes	TC	0, 230 cycles
10313 mid	Sn/37Pb	Plain Cu	Yes	Iso	100, 250 hours @ 100°C
AI end	Sn/37Pb	Ni-plated	No	Iso	100, 250 hours @ 60°C
AI mid	Sn/37Pb	Ni-plated	No		
A20I end	Sn/37Pb	Ni-plated	Yes	Iso	100, 250 hours @ 125°C
A20I mid	Sn/37Pb	Ni-plated	Yes	Iso	100, 250 hours @ 100°C
B 08 end	Sn/3.5Ag	Ni-plated	Yes	TC	0, 60, 350 cycles
B 08 mid	Sn/3.5Ag	Ni-plated	Yes	TC	0, 60, 120, 350 cycles
B end	Sn/3.5Ag	Ni-plated	No	TC	0, 60, 120, 350 cycles
B mid	Sn/3.5Ag	Ni-plated	No	TC + Iso	0, 60 cycles + 100, 250 hours @ 125°C
50313 end	Sn/3.5Ag	Plain Cu	Yes	TC	0, 230 cycles
50313 mid	Sn/3.5Ag	Plain Cu	Yes	Iso	100, 250 hours @ 100°C
C 17 end	Sn/Ag/0.7Cu	Ni-plated	Yes	TC	0, 290 cycles
C 17 mid	Sn/Ag/0.7Cu	Ni-plated	Yes		0, 60, 290 cycles
C end	Sn/Ag/0.7Cu	Ni-plated	No	TC	0, 60, 290 cycles
C mid	Sn/Ag/0.7Cu	Ni-plated	No	TC + Iso	0, 60 cycles + 100, 20 hours @ 125°C
CI end	Sn/Ag/0.7Cu	Ni-plated	No		
CI mid	Sn/Ag/0.7Cu	Ni-plated	No	Iso	100, 250 hours @ 100°C
C20I end	Sn/Ag/0.7Cu	Ni-plated	Yes	Iso	100, 250 hours @ 60°C
C20I mid	Sn/Ag/0.7Cu	Ni-plated	Yes	Iso	100, 250 hours @ 125°C

\* TC = Thermal Cycling

\*\* Iso = Isothermal Aging

## 3 Results and Discussion

### 3.1 Introduction

The driving force for the damage observed in the solder materials during this study was due to several factors related to thermal cycle testing and isothermal aging conditions imposed on the samples. The thermal cycling between -55 °C and 125 °C introduced deformation mechanisms such as CTE mismatch stress and creep. The isothermal aging at 60 °C, 100 °C, and 125 °C produced long-term exposure conditions contributing to creep and diffusion within the materials. Damage of the solder layers was seen in all samples tested regardless of the construction type or solder material. Much of this damage can also be related to the overall performance of the materials, specifically the solder layer, and then to the reliability of the electronic package.

The following discussion is split into two sections, the primary and the secondary observations. The primary observations relate directly to the overall conclusion and defense of the thesis. Within this section, observations made during this study are revealed to support the development of an overall conclusion. The secondary observations highlight discoveries made during this study that did not have a significant role in the overall conclusion. Though these observations may be of interest to the continued study of large area lead and lead-free solder joints.

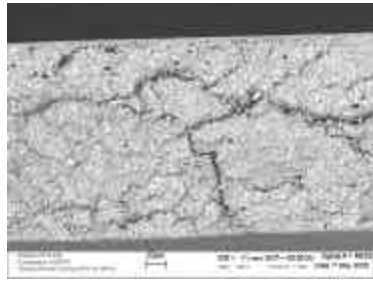
During the discussion of the observations the term “damage” is used. The term “damage” in the context of this document will mean that there has been a visible change in the microstructure of the sample, which may include cracking, visible slip bands, extrusions or intrusions, thermal pitting, and phase coarsening. The term microstructure normally covers the structural features of a solid material from the atomic size (0.3 nm) up to the external shape of the specimen ranging in size from millimeters to meters. These features include composition, crystal structure, grain size, size and distribution of phases, and more. Damage was seen at all levels from microscopic changes, to evidence of plastic deformation, to severe catastrophic failure in the solder layers.

## 3.2 Primary Observations

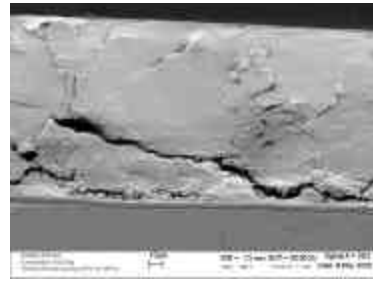
### 3.2.1 Damage Observations

Damage was found in the thermally cycled samples as early as 60 thermal cycles; though, cracking was not found until after approximately 200 thermal cycles. Damage was also seen in the isothermally aged samples; however, no cracking occurred. Generally, similar diffusion mechanisms occurred in the isothermal and thermal cycle testing. However, with the addition of mechanical stresses due to cyclic loading under the thermal cycling conditions damage is greatest.<sup>xv</sup> Appendix A contains representative SEM images of the samples at various intervals throughout testing. Comparing the samples within each chart in Appendix A, it can be concluded that with increasing testing times the damage increases whether during thermal cycling or isothermal aging. Some of the samples were re-polished, as indicated in the chart as (Re). These samples were used to understand the nature of the damage beyond any surface effects. Further, comparing the samples between the tri-layer and the dual-layer samples, the tri-layered samples sustained more damage overall. Likewise, comparing the thermally cycled samples and the isothermally aged samples, the samples that were thermally cycled accumulated the most damage. Finally, comparing the solder types was a more complicated task. It was apparent, however, that the lead-free solder alloys, Sn/3.5Ag and Sn/Ag/0.7Cu, had the most severe failures during this study.

Cracking was consistently found in the lead-free samples with the tri-layer construction, Si-die/solder/DBC, that underwent thermal cycling conditions. Though damage was seen in all samples, the most severe cracking was found only in the lead-free alloys. The samples constructed with eutectic Sn/Pb solder did not have severe cracking (Figure 3.2-1). Likewise, there was no cracking observed in the dual-layer samples, nor in the isothermally aged samples (Figure 3.2-2 and Figure 3.2-3). The cracking may have happened as a brittle failure or a build up of stress leading to plastic deformation in the lead-free alloys. The isothermally aged samples did not experience CTE mismatch in a severe manner because there was enough time for the materials to relax.

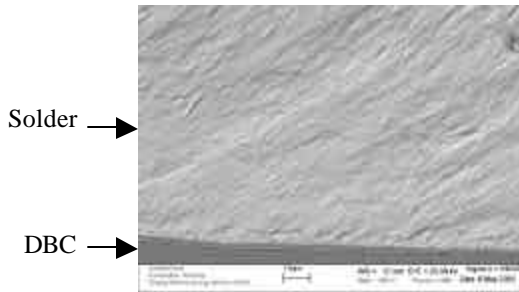


Composition	Sn/37Pb
Magnification	SEM 500x
Comments	350 thermal cycles



Composition	Sn/3.5Ag
Magnification	SEM 500x
Comments	350 thermal cycles

**Figure 3.2-1: Severe cracking was not observed in the Sn/37Pb samples.**

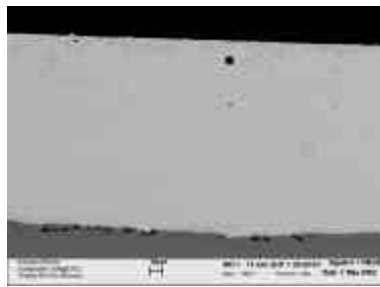


Composition	Sn/3.5Ag
Magnificatio	SEM 1000x
Comments	350 thermal cycles Dual-layer

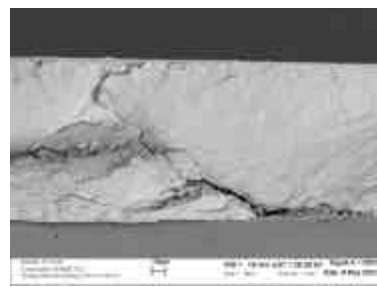


Composition	Sn/3.5Ag
Magnificatio	SEM 1000x
Comments	350 thermal cycles Tri-layer

**Figure 3.2-2: Cracking did not occur in the solder/DBC, or dual-layer, constructed samples.**



Composition	Sn/3.5Ag
Magnification	SEM 500x
Comments	250 hours aging



Composition	Sn/3.5Ag
Magnification	SEM 500x
Comments	350 thermal cycles

**Figure 3.2-3: Cracking was not found in the isothermally aged samples.**

Figure 3.2-4 is an illustration representing the stresses experienced by the samples during thermal cycling with hold periods, which allow for relaxation, and at constant temperatures, which again allow for relaxation. As compared with thermal cycling, which also experienced a brief relaxation period.

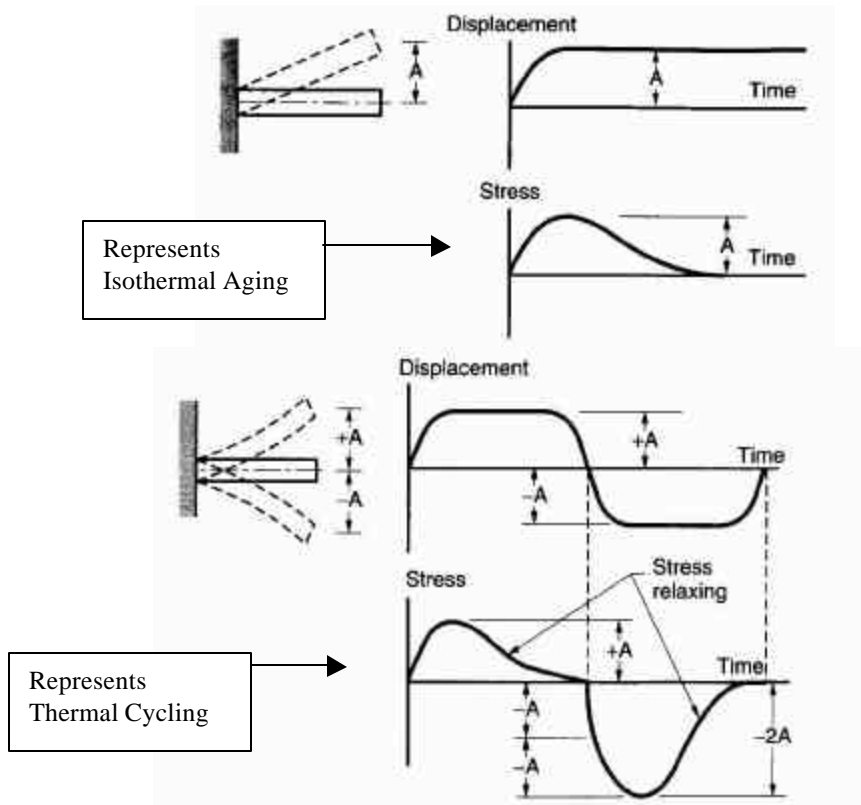


Figure 3.2-4: Effects of cyclic stress loads.<sup>xvi</sup>

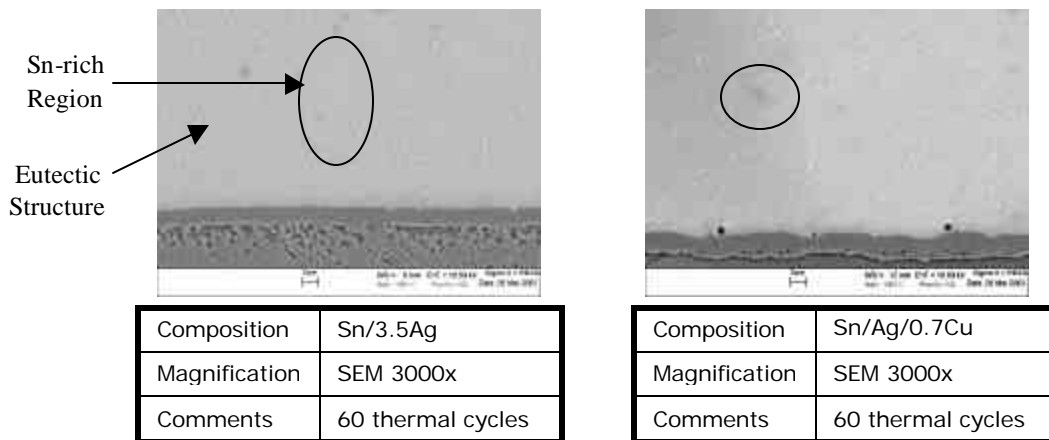
The dual-layer constructed samples did not constrain the solder layer between two dissimilar materials as in the tri-layer samples. The materials in the dual-layer samples were only fixed at the interface and were free to expand in the other directions; hence, there was less stress in the solder layer of these samples. Finally, the lead-free solder alloys are considered to be ‘harder’ solders as compared with eutectic Sn/Pb. Jun He, et. al. found that because the interfacial shear and peeling stresses are proportional to the solder yield strength that cracks are more likely to grow in “hard” solders than in “soft” solders. However, “soft” solders are more subject to creep.<sup>xvii</sup> Because thermal cycling during this study went to only ~300 cycles, the issues of creep and other factors for failure may not have had time to affect the outcome. Though results revealing damage at a low number of cycles does identify a potential reliability issue to be addressed.

## Conclusion

Damage was found in all of the samples regardless of construction type (dual or tri-layer construction) or solder type (Sn/37Pb, Sn/3.5Ag, or Sn/Ag/0.7Cu). The most severe damage, in the form of surface penetrating cracks, was in the thermally cycled, tri-layered, lead-free solder samples. The Sn/37Pb samples did not have any deep cracking as was seen in the lead-free solder samples. Likewise cracking was only observed in the thermally cycled samples, not in the isothermally aged samples. Also, cracking was not seen in the dual-layered samples. Hence, a combination of material properties and sample geometry were likely the source of the damage.

### 3.2.1.1 Dendritic Microstructure

Because the damage observed in the samples was different for the different solder types, observations were made of the microstructure of these materials. A distinctive microstructure was formed in the lead-free solder alloys. It has been identified as dendrites. The microstructure is made up of distributed circular patterns of Ag-phases (Figure 3.2-5). The areas in the middle of the Ag-phase circles are where the eutectic structure is located, or the Sn-rich regions. These regions do not contain the Ag phase.



**Figure 3.2-5: Circular microstructure pattern due to dendrites.**

Figure 3.2-6 illustrates the formation of dendrites in an off-eutectic system. Dendrites are also possible in a eutectic system depending on the heating and cooling rates. Figure 3.2-7 is a plot for an aluminum alloy of cooling rate versus dendrite size. For faster cooling rates, there is less time for the dendrites to form. The samples created for this study were cooled in air; unfortunately, the rate was not recorded. It is assumed that since dendritic structures were observed, the cooling rate would have been sufficiently long.

As the liquid cools, the  $\alpha$ -phase is precipitated out rejecting the remaining liquid consisting of the eutectic composition, as seen in Figure 3.2-6. Once the eutectic temperature is reached, the remaining liquid being the eutectic composition solidifies leaving regions of the  $\alpha$ -phase and regions of the eutectic phase. During this process protrusions develop into long arms or cells, which grow parallel to the direction of heat flow.<sup>xix</sup> Secondary arms will develop from the primary arms at fairly low temperature gradients.

The solidified microstructure of the binary eutectic Sn-3.5%Ag consists of Sn and the intermetallic  $\text{Ag}_3\text{Sn}$  in the form of thin platelets. In other cases the microstructure of the same alloy will consist of a  $\beta$ -Sn phase with dendritic globules and inter-dendritic regions with a eutectic dispersion of  $\text{Ag}_3\text{Sn}$  precipitates within a  $\beta$ -Sn matrix.<sup>xviii</sup>

Since temperature gradients and growth rates are not individually controllable, the variable that can be controlled is the rate at which heat is conducted away from the solidifying alloy, or the cooling rate. The process by which the solder joints were created may have caused these dendrites or cells to form. The solder was reflowed above the alloy's melting point and then air-cooled using a belt reflow oven. The samples were assembled prior to reflow, placed on the belt that was moving at a set speed across a series of heated plates. Through visual observation of the reflow process, I noticed that as the device moved from one plate to the next, a "melting gradient" was created across the sample. The front edge of the solder would begin to reflow, or melt, before the back half of the sample. A wave of heat was moving across the solder. It was likely that a similar event happened at the end of the process during solidification, when the sample was moved onto an air-cooled heat sink by the belt.



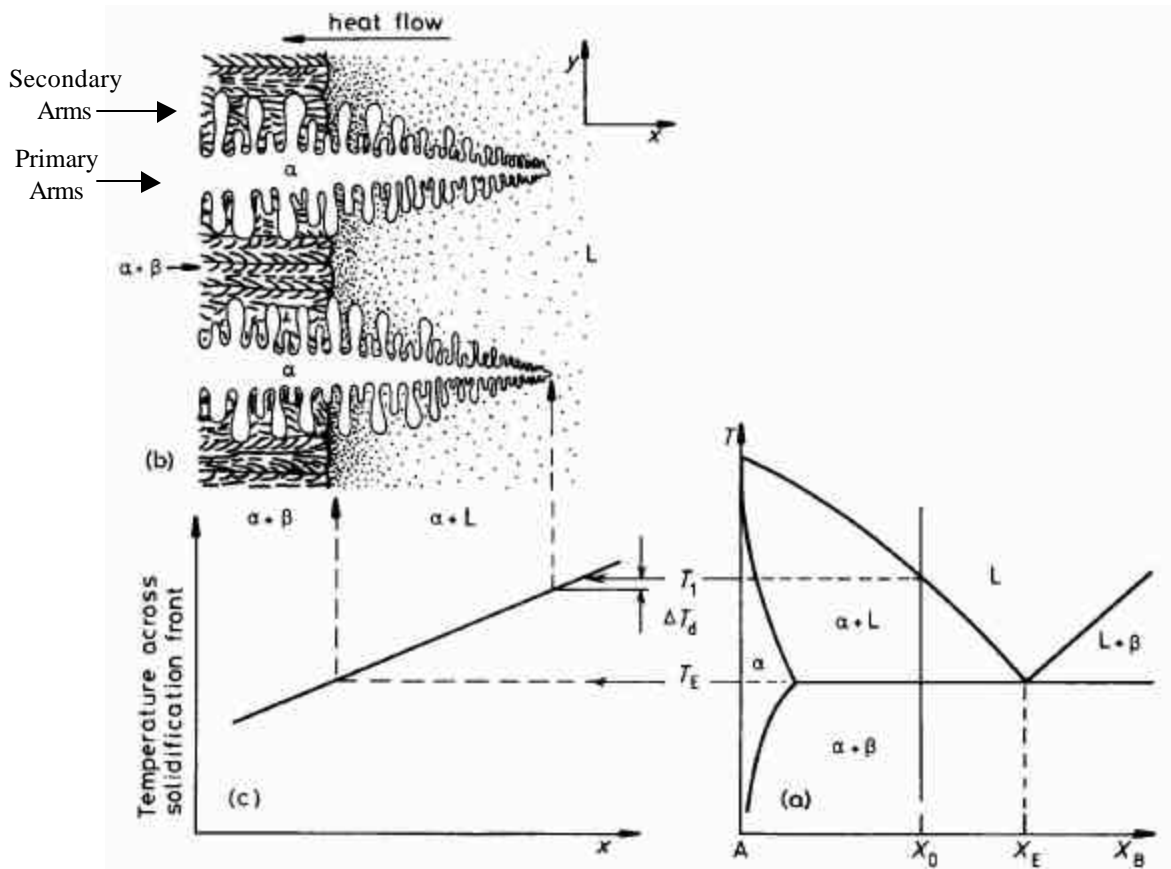


Figure 3.2-6: Schematic of a binary, off-eutectic alloy in a temperature gradient.<sup>xix</sup>

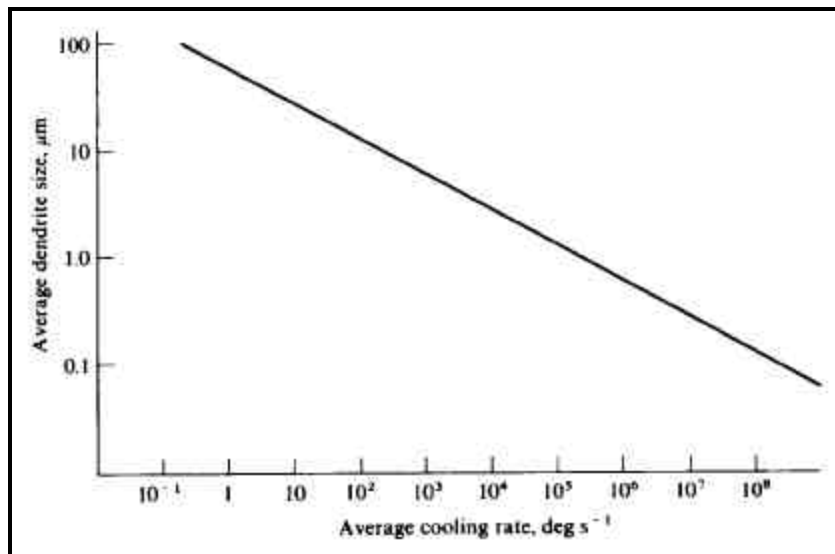
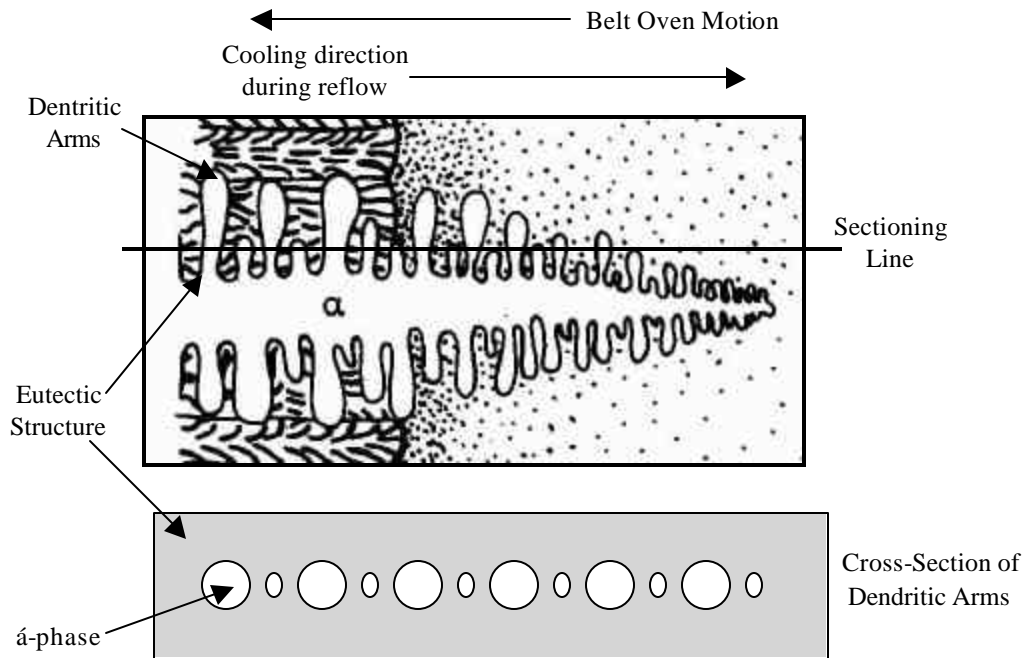


Figure 3.2-7: Plot of dendrite size versus cooling rate for an aluminum alloy.<sup>xx</sup>

The samples were sectioned perpendicular to the heating gradient reflow. The microstructure of the solder was viewed two dimensionally; hence, the circular patterns are likely a cross-section of the dendrite arms as illustrate in Figure 3.2-8.



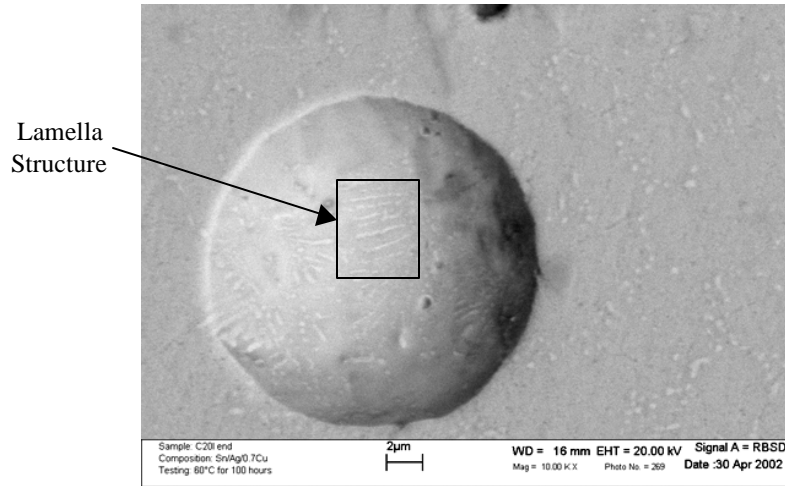
**Figure 3.2-8: Illustration of a cross-section through the dendritic arms, resulting in a 2-D image.**

The Sn/Ag/0.7Cu solder alloy had the most consistent and distinguishable dendrites. These structures appeared to change with testing. During thermal cycling it was observed that the Sn-rich phases would act as individual grains. The damage due to testing would occur around these phases (Figure 3.2-9). In addition, there was a lamella-like structure that was observed in many of the voids in the lead-free solder alloys as seen in Figure 3.2-10. The lamella microstructure consists of a fine structure of alternating Sn-rich and  $Ag_3Sn$  phases.<sup>xxi</sup>



Composition	Sn/Ag/0.7Cu
Magnification	SEM 3000x
Comments	60 thermal cycles

**Figure 3.2-9: Damage due to thermal cycling.**



Composition	Sn/Ag/0.7Cu
Magnification	SEM 10kx
Comments	60 thermal cycles

**Figure 3.2-10: Lamella structure observed at the surface of the void region.**

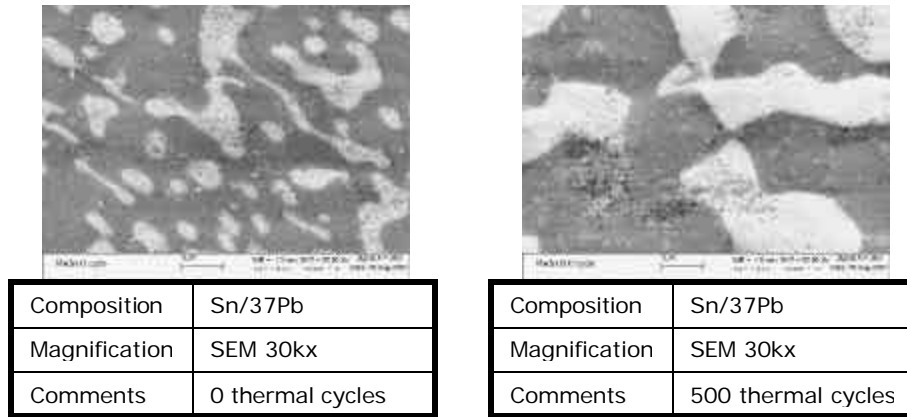
## Conclusion

In the majority of the lead-free solder samples; circular patterns in the microstructure were identified as dendritic structures. The circular patterns were a result of cross-section the samples and observing a 2-D view of the dendritic structures. After thermal cycle testing, the circular patterns acted as separate grains. These circular “grains” were Sn surrounded by the eutectic microstructure.

### 3.2.1.2 Phase Coarsening

Phase coarsening was detected in the Sn/37Pb solder alloy as predicted. Much research has been published on microstructural coarsening.<sup>xxii, xxiii, xxiv, xxv</sup> Coarsening is most obvious in Sn/37Pb solder alloys, unlike lead-free solder alloys, which have fine stable microstructures, due to the formation of small dispersed particles such as in Sn/3.5Ag.<sup>xxiv</sup> Solder balls were made with the Sn/37Pb alloy used in the construction of the dual and tri-layered samples. The surface of the solder balls were imaged using the SEM, one at 0 cycles and one at 500 thermal cycles (Figure 3.2-11). These thermal cycles occurred over the temperature range of 0 °C to 100 °C with 10-minute cycles and no hold times. A drastic phase coarsening was observed in the solder ball samples. A study by Kailasam et. al. concluded that neither surface diffusion nor volume diffusion was uniquely limiting the microstructural coarsening process for Sn/37Pb alloys.<sup>xxv</sup> In other words, the process by which phase coarsening takes place is more complicated relating to

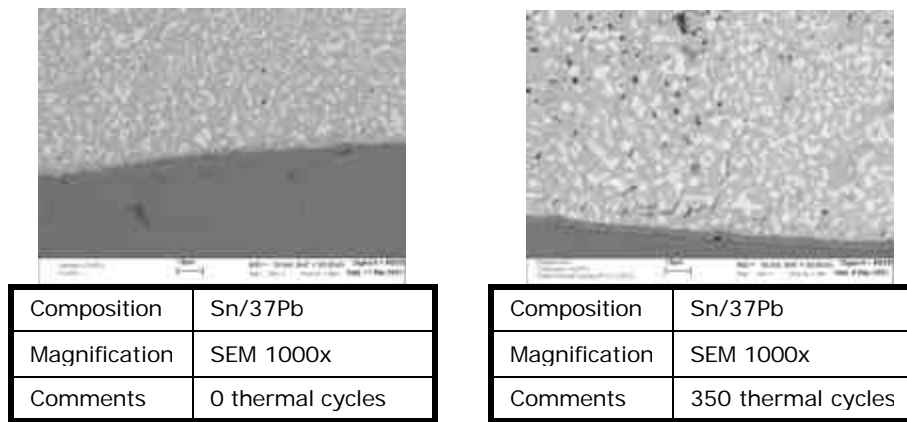
various conditions such as temperature or applied stresses and strains. Many studies have found that coarsening is more specifically due to temperature and with increasing aging temperature and time there will be an increase in coarsening.<sup>xxvi</sup>



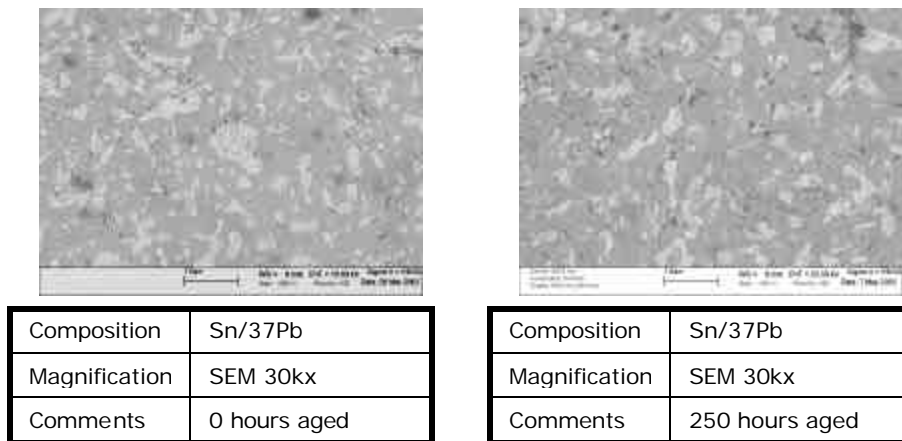
**Figure 3.2-11: Thermally cycled solder ball samples illustrating phase coarsening.**

However, phase coarsening was not as drastic in the dual and tri-layered samples, tested over the range of -55 °C to 125 °C with approximately 1-hour cycles and 5-minute hold times at the extremes (Figure 3.2-13). There appeared to be more large Pb-phases in the thermally cycled samples. In the isothermally aged samples with Sn/37Pb solder, coarsening was only slight (Figure 3.2-13). These were unexpected results because it was assumed that the driving force was diffusion for phase coarsening and at elevated temperatures for long periods of time, diffusion would be favorable. Isothermal aging of the samples did not reveal microstructural change in this study. Research in literature, noted observations of phase coarsening at elevated temperatures for longer periods of time. Hence, aging studies can provide information on microstructural stability, its evolution as a function of time and temperature, and potential joint failure mechanisms.<sup>xxvii</sup>

Phase coarsening was observed only as a slight change during this study and therefore was not a significant factor. This may have been due to equipment error with respect to the SEM imaging analysis. There appeared to be variations between different sets of data collected. The magnifications did not seem to be repeatable, which may have been related to the working distance of the detectors in the SEM being different during different data collection sessions. In addition, a change in the experimental procedure by imaging the samples at higher magnification may have resulted in images that would have been more easily comparable. Nonetheless, some images were successfully obtained as seen in Figure 3.2-11 and Figure 3.2-13, which illustrate the slight coarsening found during this study.



**Figure 3.2-12: Slight phase coarsening in a tri-layered sample after 350 thermal cycles.**



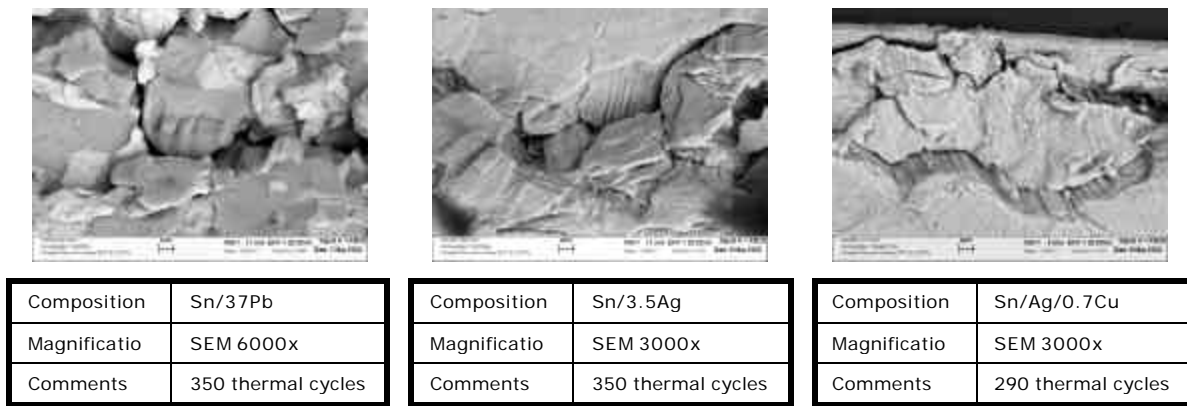
**Figure 3.2-13: Slight phase coarsening in a tri-layered sample after 250 hours of aging at 100 C.**

## Conclusion

Phase coarsening was only seen as a slight change in the microstructure of the Sn/37Pb samples. Earlier work showed substantial change in thermally cycled bulk samples. Further study with more samples and more consistent analysis may be able to quantitatively determine phase coarsening.

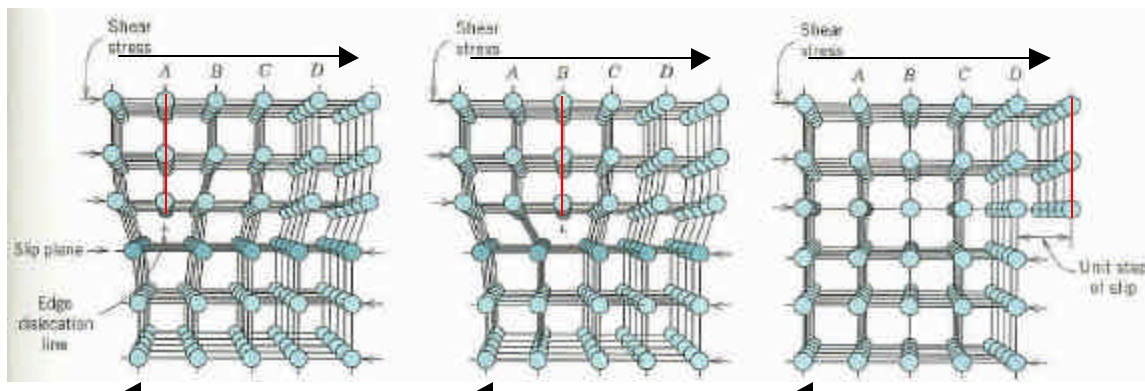
### 3.2.1.3 Slip bands

The un-polished surfaces of all of the solder alloys dislocation motion in the form of slip bands, extrusions and intrusions, and grain boundary sliding were observed (Figure 3.2-14). As discussed in the previous section, dislocations lead to the plastic deformation and the damage resulting from the plastic deformation in the samples were also revealed after polishing.



**Figure 3.2-14: Extrusions observed for all three of the solder alloys tested under thermal cycling conditions.**

Plastic deformation is the permanent or non-recoverable deformation left after release of the applied load or shear stress.<sup>xxviii</sup> It corresponds to the motion of large numbers of dislocations where there are permanent atomic displacements. A dislocation is a linear crystalline defect around which there is atomic misalignment.<sup>xxviii</sup> Slip in turn is the term for the dislocation motion resulting plastic deformation, where the crystallographic plane along which the dislocation line traverses is the slip plane. A slip band is a group of closely spaced slip lines that appear to be a single large slip line at low magnification.<sup>xxxii</sup> Macroscopic plastic deformation simple corresponds to permanent deformation that results from the movement of dislocations, or slip, in response to an applied shear.<sup>xxviii</sup> Figure 3.2-15 illustrates an edge dislocation as it moves through the lattice.



**Figure 3.2-15: Dislocation motion of an edge dislocation.**<sup>xxviii</sup>

Dislocation theory says that a slip band can shift from plane to plane and produce a notch or an extrusion through a series of slip dislocations movements as discovered in Figure 3.2-14. Extrusions are small-localized deformations that are a consequence of dislocation motion during fatigue. They have a depth or a height on the order of  $10^3$  m.<sup>xxxii</sup> These are sometimes called

persistent slip bands (PSB) when these bands continue to reappear after polishing, as was the case in the solder alloys observed under thermal cycling conditions.

Cottrell and Hull suggested that Frank-Read sources on two intersecting slip planes might coordinate to produce an intrusion-extrusion pair on the same side of the specimen.<sup>xxix</sup> If the cyclic slip is repeated the depth and the length of the notch and the ridge would become deeper but the width would not increase.<sup>xxix,xxx</sup> This is illustrated in Figure 3.2-16 where a series of cyclic moments activates the slip bands and produces an extrusion and an intrusion. The cyclic movements, which create the extrusions and intrusions, can thus grow into cracks that propagate because of stress concentrations associated with the newly formed flaw.<sup>xxx,xxx</sup> Figure 3.2-17 is another illustration of an extrusion and an intrusion.

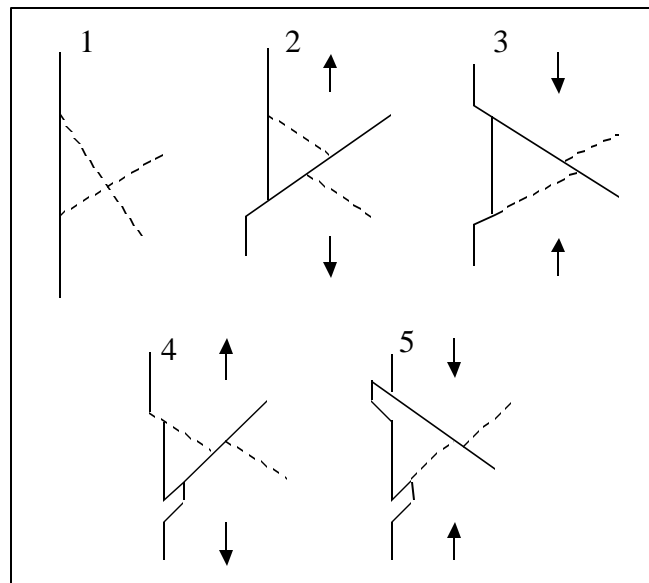


Figure 3.2-16: Sequence of slip movements producing an extrusion and an intrusion.<sup>xxx,xxx</sup>

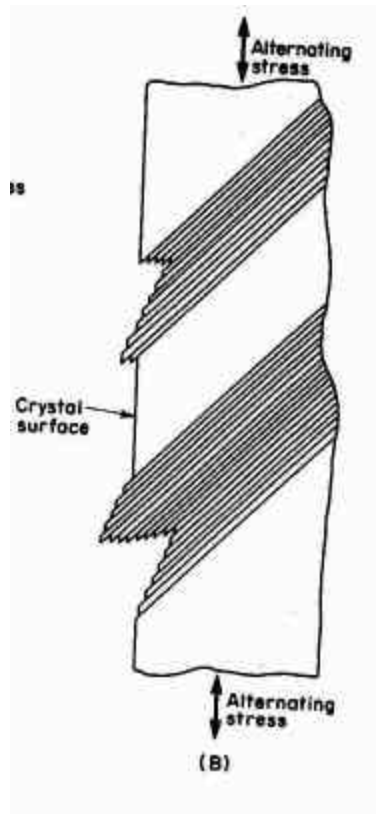


Figure 3.2-17: The difference in surface contour where slip bands intersect the surface.<sup>xxxii</sup>

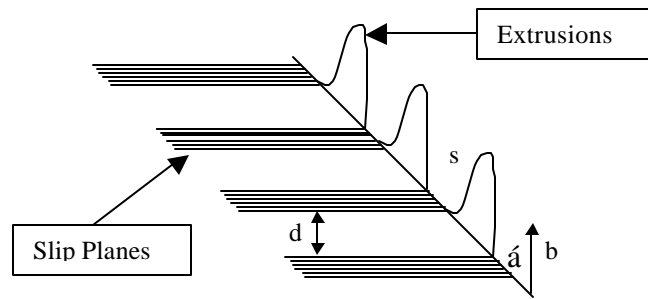
Persistent slip bands (PSBs) have also been referred to as surface relief. Polák et. al. discuss the formation of surface relief on a surface that was originally flat due to cyclic plastic straining as representing the first step in nucleation of a fatigue crack.<sup>xxxiii, xxxiii</sup> The evolution of the surface relief in cycling with constant plastic strain amplitude is characterized by the appearance of persistent slip bands that emerge on the surface as prominent extrusions and intrusions.<sup>xxxiii</sup>

The bowing of dislocation segments and their extension accommodates the high plastic strain amplitude within the PSB until edge segments reach the neighboring walls, i.e. extrusions keep growing until they run into each other. The relationship between surface relief and dislocation arrangement in PSBs is given by:

$$s = \frac{d}{\cos \alpha}$$

where  $s$  is the spacing between the extrusions,  $d$  is the spacing between the slip bands and  $\alpha$  is the intersecting angle between the Burger's vector,  $b$ , and the primary slip plane.





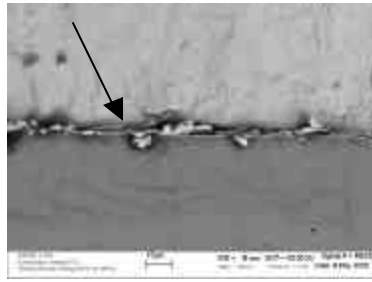
**Figure 3.2-18: Schematic of the relation between the internal structure of dislocations and the surface relief in a fatigued crystal.**

For every extrusion there are two intrusions into the material that are created. Sharp intrusions are stress raisers because the stress and strain concentration in the tip of an intrusion is comparable with that of a crack of the same dimension. The high stress concentration in the tip of an intrusion gives rise to local slip mechanism along the primary plane, since the intrusions are lined up with the slip planes by definition. The irreversibility of slip in the tip of the intrusion can result in micro-crack nucleation.<sup>xxxiii</sup>

Wen and Keer presented a fatigue theory, which attributed persistent slip bands (PSBs), which form under cyclic loading conditions to be the contributing cause for fatigue cracking. The following describes the logic in their theory:

By looking at the physical damage process, the fatigue theory assumes the following: persistent slip bands (PSB) form in solder under cycling loading, and thereafter microcracks form within the PSB due to the increment of dislocation density or along grain boundaries because of the impingement of the PSB. These microcracks evolve by increasing the total number and thus cause the material to deteriorate in a percolating manner until certain point is reached. At that point these microcracks coalesce and create one or several dominant microcracks that fracture of the solder structure.<sup>xxxiv</sup>

Several types of extrusions were observed in the samples tested under thermal cycling. Figure 3.2-20 is an illustration of some types of extrusions that may occur. Figure 3.2-19 are some images taken of the extrusions observed during this study. The majority of the extrusions seen were the block-type extrusion where the newly created edges perpendicular to the polished surface of the sample show the alternating slip bands.

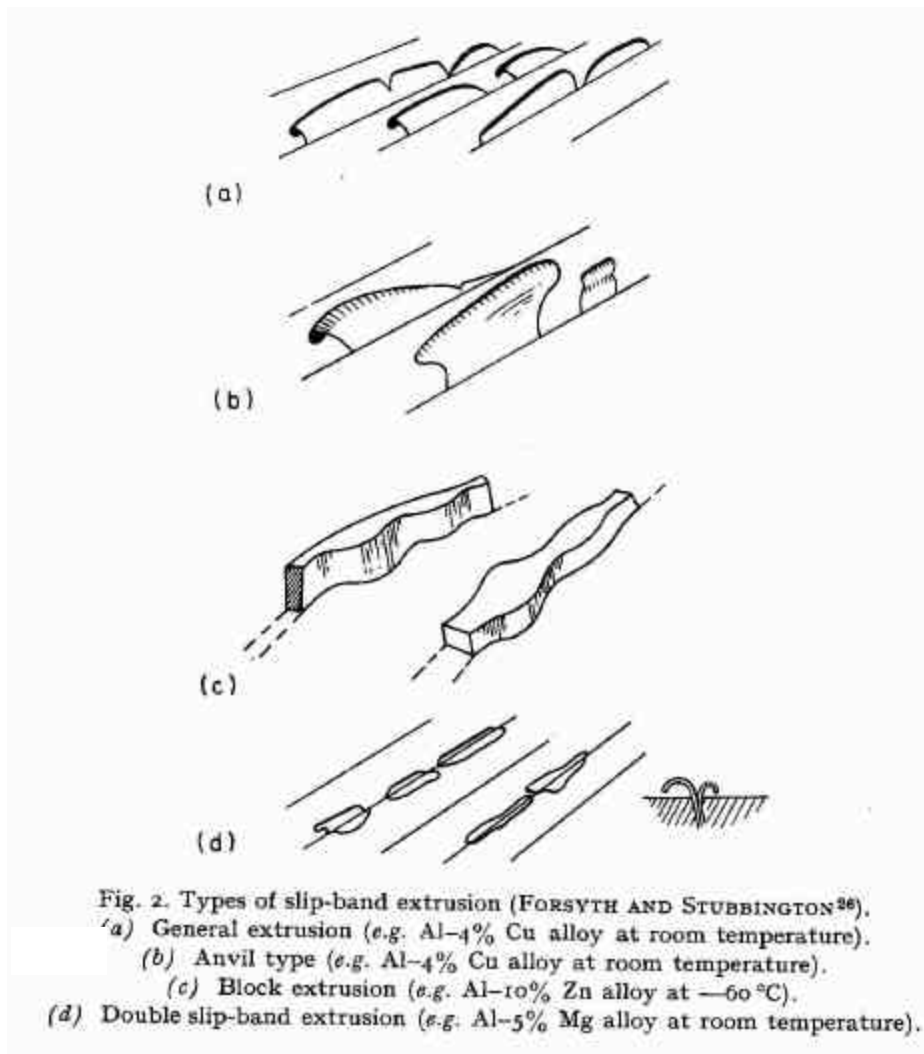


Composition	Sn/3.5Ag
Magnification	SEM 1000x
Comments	350 thermal cycles



Composition	Sn/3.5Ag
Magnification	SEM 3000x
Comments	350 thermal cycles

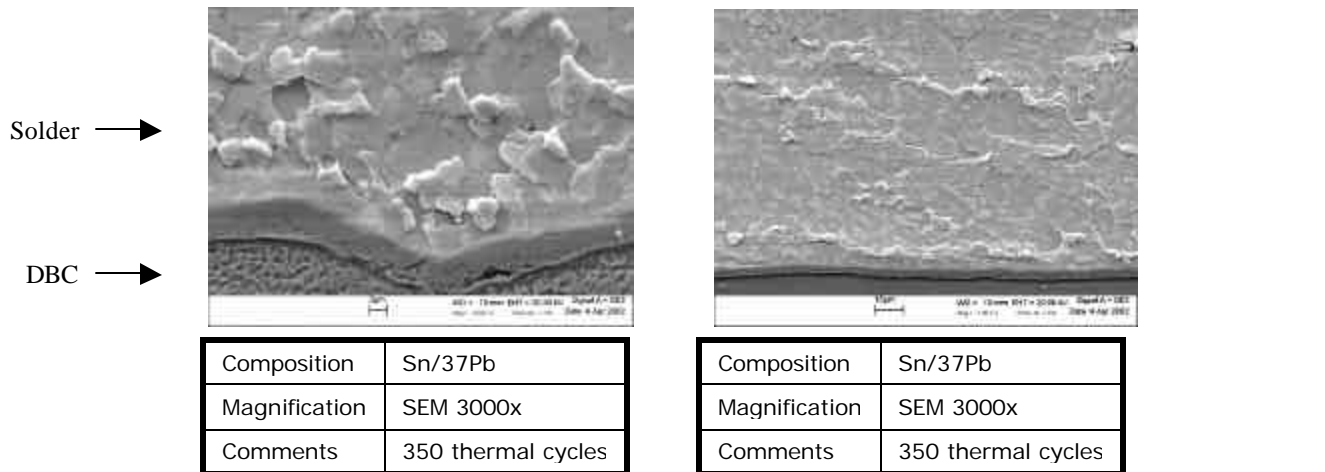
**Figure 3.2-19: Extrusions observed after thermal cycling in this study.**



**Figure 3.2-20: Illustration of some types of extrusions.<sup>xxxi</sup>**

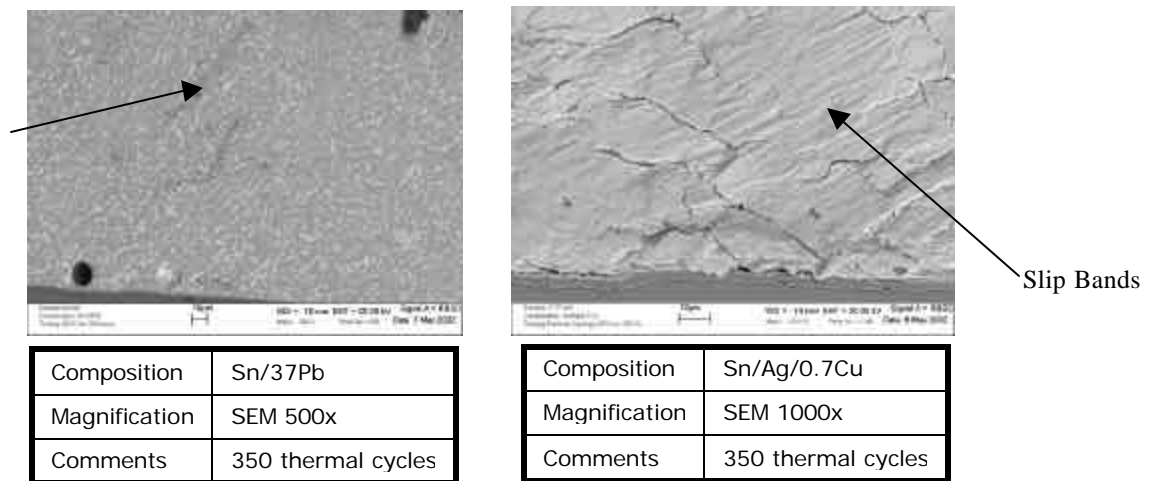
Grain boundary sliding was most obvious in the Sn/37Pb solder alloy. The boundaries between the Sn and Pb-phases are where the sliding occurred as seen in Figure 3.2-21. Grains being pushed out from the surface and roughening indicated plastic deformation.<sup>xxiii, xxxv</sup> A study

by Lee and Stone discuss the fact that the sliding between colonies in the eutectic structure of Sn/37Pb plays a significant role in the rheology of the solder joint, or the deformation and flow of material in the solder joint.<sup>xxxv</sup> Because their tests were at 1/hr cycling frequency and grain boundary sliding is a low strain rate phenomenon, it was determined that the presence of this phenomenon would be found during thermal or mechanical cycling at frequencies lower than 1/hr. However, grain boundary sliding would not occur under high frequency cycling conditions.

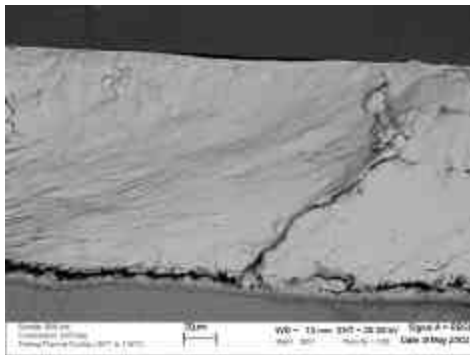


**Figure 3.2-21: Evidence of grain boundary sliding in the Sn/37Pb solder alloy.**

Slip bands on a polished surface take on a wavy pattern when cross-slip within the material is easy called wavy glide.<sup>xxxvi</sup> Slip bands were seen on the surface of the lead-free solder alloys. In the lead-free alloys studied the slip bands appeared to be wavy and angled across the solder layer. These wavy slip bands were both perpendicular and parallel to the cracks seen in the lead-free alloy samples (Figure 3.2-22 and Figure 3.2-23). Likewise, after re-polishing, the Sn/37Pb samples showed evidence of damage with the same characteristics as the slip bands observed in the lead-free alloys (Figure 3.2-22). This may be in an indication that the ratcheting action of the stresses during thermal cycling caused damage in both directions. These characteristics were observed in both the dual-layer and tri-layer sample constructions.



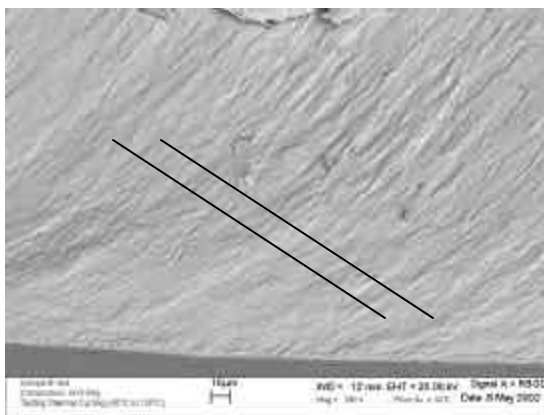
**Figure 3.2-22: Slip bands seen on the surface of a thermally cycled sample.**



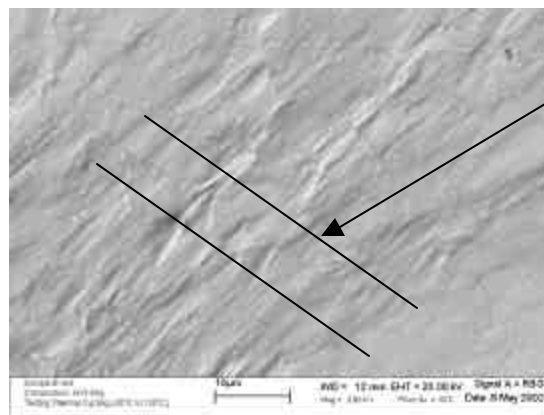
Composition	Sn/3.5Ag
Magnification	SEM 500x
Comments	350 thermal cycles

**Figure 3.2-23: Slip bands across a tri-layer Sn/3.5Ag sample.**

A closer look revealed that the Ag phases in the lead-free samples appeared to follow a diagonal pattern perpendicular to the wavy slip bands (Figure 3.2-24). These characteristics were observed mostly in the dual-layer sample constructions. Figure 3.2-25 is an SEM image of a tri-layer, Sn/Ag/0.7Cu sample with a similar lined pattern of the Ag phases. Within the pattern are also elongate oval shapes outlined by the Ag phases. These are likely evidence of a dendritic structure.



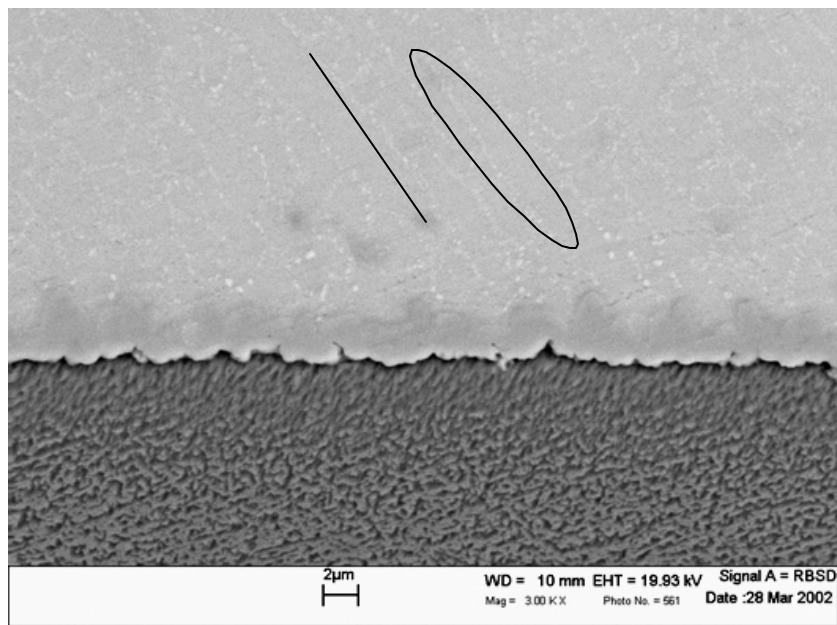
Composition	Sn/3.5Ag
Magnification	SEM 500x
Comments	350 thermal cycles



Pattern of Ag phases.

Composition	Sn/3.5Ag
Magnification	SEM 2000x
Comments	350 thermal cycles

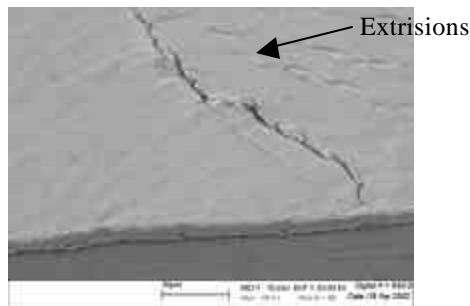
**Figure 3.2-24: The Ag phases in the lead-free solder alloys were found in straight-line patterns.**



Composition	Sn/Ag/0.7Cu
Mag.	SEM 3000x
Comments	350 thermal cycles Re-polished

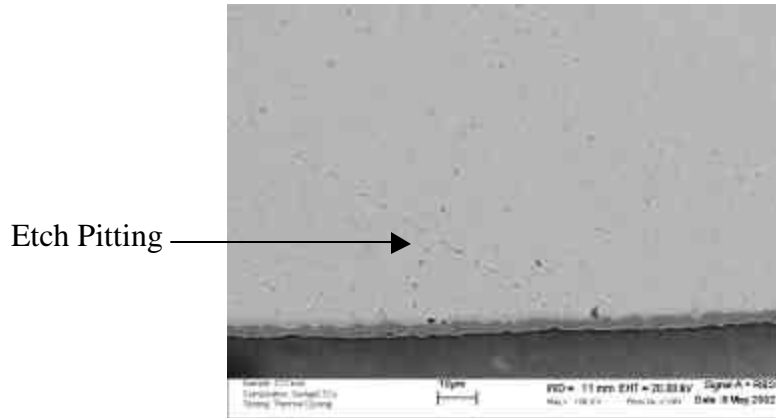
**Figure 3.2-25: Ag phase patterns in a tri-layer Sn/Ag/0.7Cu sample.**

There were also some variations on the slip bands observed in the lead-free alloys samples. Figure 3.2-26 illustrates two different variations in slip bands at the surface. The image on the left is of a triangular shaped dislocation and on the right are dislocations, which could be considered extrusions. After re-polishing some of the samples, dislocations were identified in the lead-free solder samples. Figure 3.2-27 shows two intersecting dislocations, or pitting representing dislocations. Cross-slip is a phenomenon that occurs in a crystal when there are two or more slip planes with a common slip direction.



Composition	Sn/3.5Ag
Magnification	SEM 3000x
Comments	120 thermal cycles

**Figure 3.2-26: Dislocations found the Sn/3.5Ag solder samples.**



Composition	Sn/Ag/0.7Cu
Mag.	SEM 1000x
Comments	350 thermal cycles Re-polished

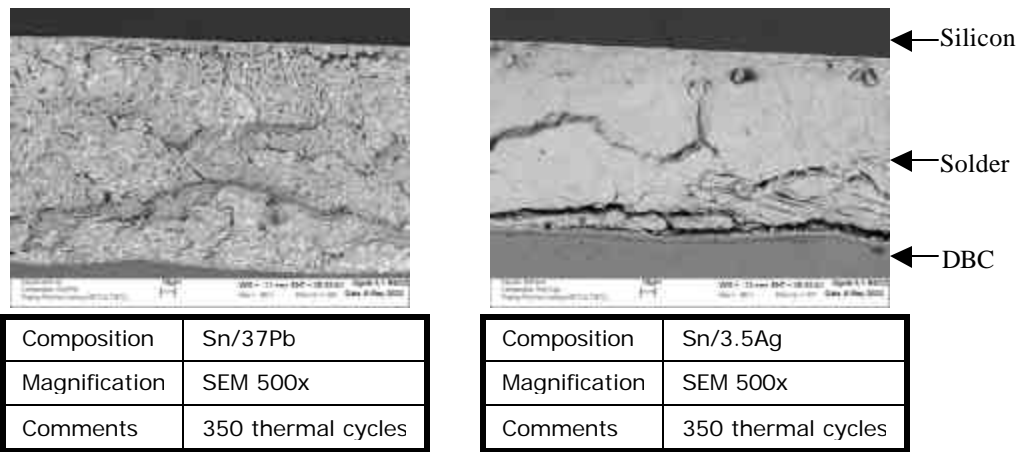
**Figure 3.2-27: Crossing dislocations.**

## Conclusion

Plastic deformation in the form of slip bands, wavy glide bands, extrusions and intrusions, and grain boundary sliding was observed in the all of the samples. The Sn/37Pb solder exhibited extrusions and intrusions as well as grain boundary sliding. The two lead-free solder alloys had wavy glide bands, slip bands, and extrusions and intrusions after testing. These indicators of plastic deformation were more easily identifiable in the thermally cycled sample.

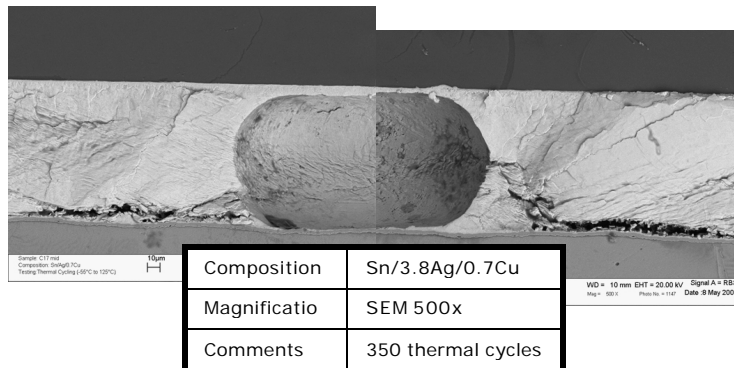
### 3.2.2 Nature of the cracking

Fatigue stresses resulting in damage such as cracking, slip bands, and extrusions/intrusions in the solder layers were seen in the thermally cycled samples. The majority of the damage occurred near the solder/DBC interface consistently in all of the samples regardless of the solder type or sample construction (Figure 3.2-28). Other studies of solder joint interconnections have discovered that failures occur at the solder/substrate interface.<sup>xxi,xxxvii,xxxviii</sup> Through rough simulations and estimated calculations it was determined that the majority of the stresses in did concentrate in the DBC area of the sample. The purpose of these calculations was to identify relative stresses, which may have lead to the eventual plastic deformation observed at the solder/DBC interface.

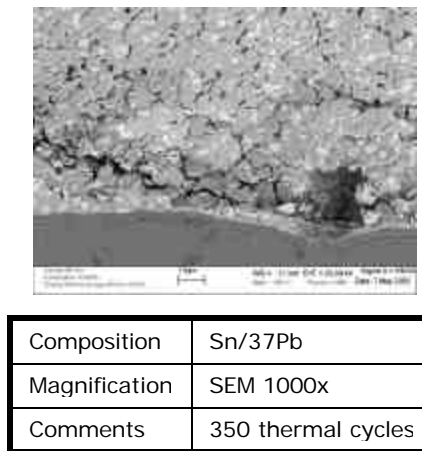


**Figure 3.2-28: SEM images of Sn/37Pb and Sn/3.5Ag samples at 350 thermal cycles.**

It was also observed that in many cases when voids were present in the solder layer, the cracks would either propagate through or from the voids (Figure 3.2-29 and Figure 3.2-30). It would make sense that a crack would move through a weak area in the solder. Likewise, the voids may have been stress raisers in the solder layer where cracks could initiate.



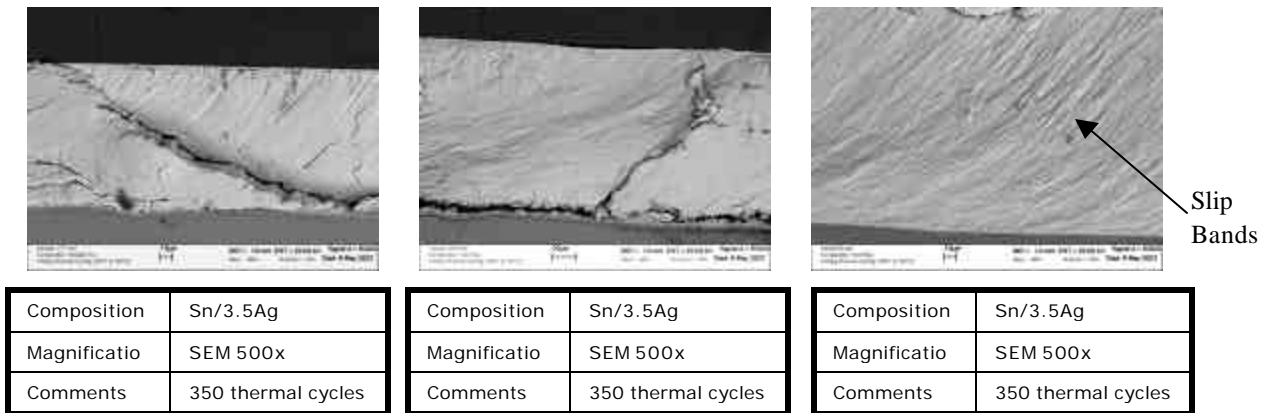
**Figure 3.2-29: SEM image of a crack propagating through a void in an Sn/Ag/0.7Cu solder layer.**



**Figure 3.2-30: SEM image of a crack propagating through a void in an Sn/37Pb solder layer.**

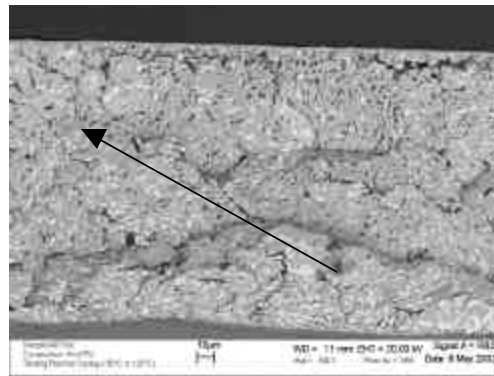
Cracks were also found to propagate across the thickness of the solder layer at a 45-degree angle (Figure 3.2-31). Slip bands were observed also at 45-degree angles across the solder layer as well (Figure 3.2-31 and Figure 3.2-32). This suggests shear stress as a result of plane stress in the solder layer. This was most likely due to the CTE mismatch between the silicon die and the DBC substrate. If it is assumed that the tensile stresses were in the x-direction, the shear stress components will resolve to be at a 45° angle to the x-direction (Figure 3.2-33). Since slip bands were found at similar angles to the interface, it could be assumed that the angled cracking would occur due to stresses below the maximum shear. Hence due to the direction of the stress, which has not been determined, these angled cracks may be plane stress shear fractures. Plane stress is associated with the maximum toughness and a slant fracture.

The solder layer is meant to be a ‘buffer layer’ between the silicon and the DBC; hence, the solder layer absorbs the damage. Upon heating, the lower CTE materials (silicon and alumina) would expand at a slower rate than the higher CTE materials (solder and copper). This would put the solder in a compressive state, while upon cooling the opposite would occur and the solder would be in tension. These stresses would also be applied at different rates from either side of the solder layer for the tri-layer samples. Shear stresses would likely have been effective both at the interfaces as well as across the entire solder layer.



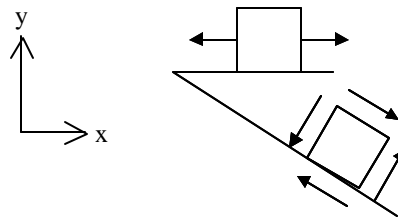
**Figure 3.2-31: Cracks and slip bands at a ~45° angle across the solder layer.**





Composition	Sn/37Pb
Magnification	SEM 500x
Comments	350 thermal cycles

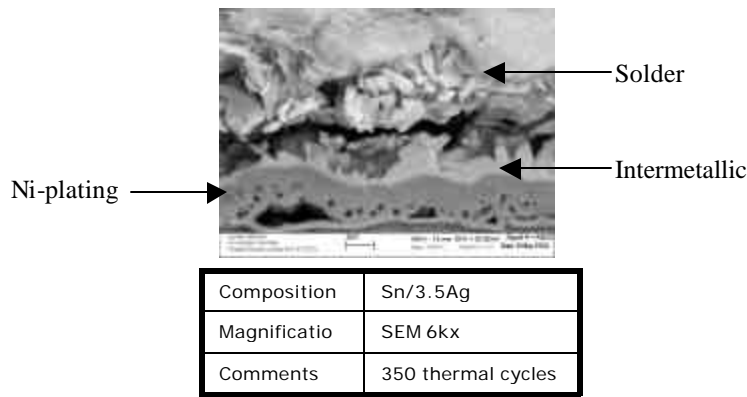
**Figure 3.2-32: Damage across the interface of an Sn/37Pb solder layer.**



**Figure 3.2-33: Illustration of the shear stress as a result of tensile stress in the x-direction.**

The interface between the solder matrix and the intermetallic was the site of the most severe crack propagation, indicating that the highest stress was located closest to the DBC substrate. This was consistent with all samples. Most all of the severe damage was mostly located at the solder/substrate interface.

The solder was the material to crack rather than the intermetallic compound, which is considered to be a more brittle material.<sup>xxxix, xxvii</sup> Figure 3.2-34 is a close-up view of cracking that was seen in the lead-free solder alloys. The intermetallic layer retained its original shape while the solder matrix pulled away from the intermetallic. Comparing the material properties of the solder alloys with their intermetallics, which form during reflow, the intermetallics are found to be stiffer, harder, and less compliant materials (Table 3.2-1). The Young's modulus and shear modulus values of the intermetallic compounds are twice that of the solder materials. In addition, the CTE values for the intermetallics are closer matched to the Cu (17.1  $\mu$ strain/K) and Ni (12.9  $\mu$ strain/K) substrate metallization.<sup>x1</sup> There is also some evidence that silver segregates to the interface and weakens the solder joint by "poisoning."<sup>xli</sup> However, during this study EDS and WDS work was not able to identify accumulations of significant amounts of silver at the interface.

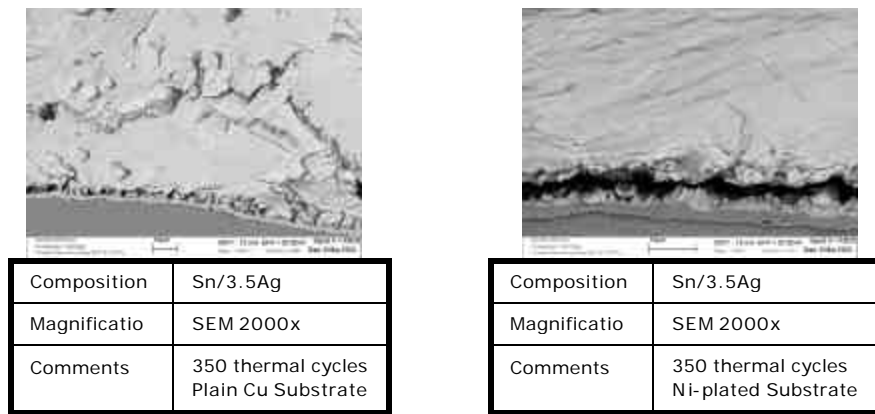


**Figure 3.2-34: Crack propagating through the solder material adjacent to the intermetallic.**

**Table 3.2-1: Material properties for two solder alloys and their intermetallics.<sup>xl</sup>**

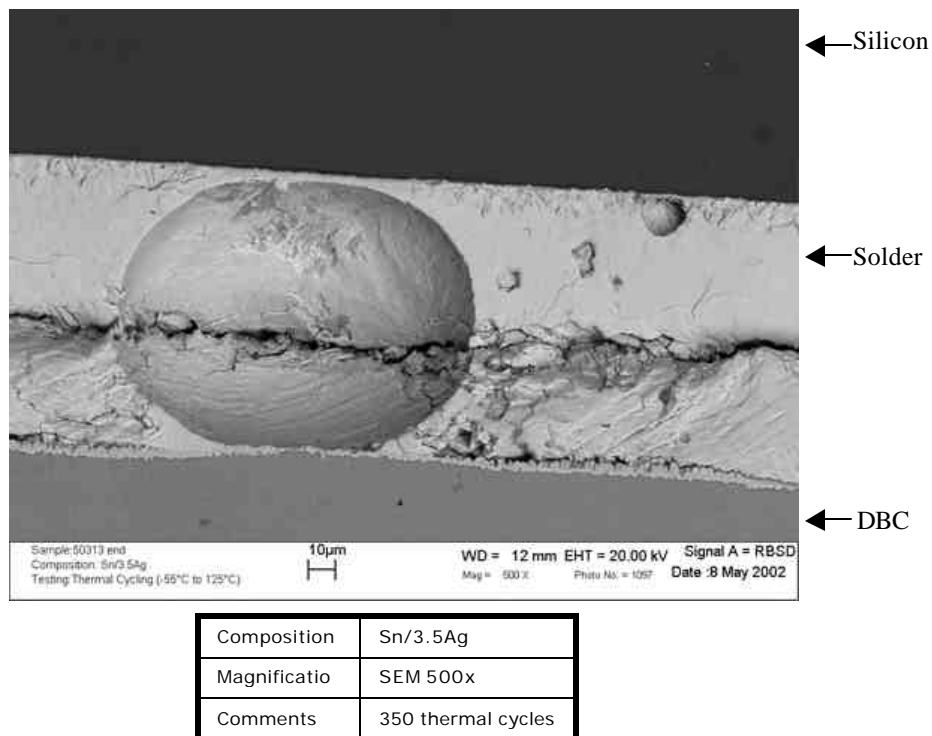
Composition	Young's Modulus	Shear Modulus	CTE	Hardness
Solder				
Sn/37Pb	30-40 GPa	10-15 GPa	23.5-26 µ strain/K	10-22.5 HV
Sn/3.5Ag	50-60 GPa	15-25 GPa	20-30 µ strain/K	10-20 HV
Intermetallic				
Cu <sub>6</sub> Sn <sub>5</sub>	85.56 GPa	50.21 GPa	16.3 µ strain/K	378 kg/mm <sup>2</sup>
Cu <sub>3</sub> Sn	108.3 GPa	42.41 GPa	19.0 µ strain/K	343 kg/mm <sup>2</sup>
Ni <sub>3</sub> Sn <sub>4</sub>	133.3 GPa	45.0 GPa	13.7 µ strain/K	365 kg/mm <sup>2</sup>

Intermetallics are created as the interconnection between a solder and the constituents it is bonding together, i.e. the reaction layer. Intermetallic layers were created on both the plain copper and the Ni-plating DBC surfaces in the samples created for this study. The intermetallics have been identified as having a compositional gradient across its thickness. The intermetallics predicted for the plain copper substrate are Cu<sub>6</sub>Sn<sub>5</sub> and Cu<sub>3</sub>Sn. The intermetallics predicted for the Ni-plated substrate are Ni<sub>3</sub>Sn<sub>4</sub>. However, the intermetallic composition and substrate surface did not seem to have an influence on whether or not cracking would occur (Figure 3.2-35). The observations were consistent across all samples regardless of the substrate surface metallization. Cracking occurred adjacent to the intermetallic compound in the solder matrix material.



**Figure 3.2-35: Cracking adjacent to the intermetallic regardless of the substrate surface metallization.**

The damage observed was most consistently located near the solder/substrate interface. This is evident in Figure 3.2-36 where a crack has propagated through the middle of the solder layer. This crack has separated the layer into two regions, which due to the crack should theoretically separate the stresses such that there is no influence from either region on the other. In the lower portion of the solder layer, below the crack, cracking at the intermetallic and slip bands at 45-degree angles can be seen. In the upper region, there is little cracking and few slip bands visible. This further suggests that the CTE mismatch within the tri-layer samples is concentrated at the substrate interface during thermal cycling. A numerical model was developed to estimate the relative stresses in the various layers of the tri-layer samples.



**Figure 3.2-36: Crack propagating through the middle of the solder layer separating two regions of differing stress.**

### 3.2.2.1 Numerical Model

Initially it was thought that the greatest stresses would be concentrated at the solder/Si-die interface because of the larger CTE mismatch between the two materials,  $\sim 30 \text{ ppm/mm } ^\circ\text{C}$  and  $\sim 3 \text{ ppm/mm } ^\circ\text{C}$  respectively, whereas the CTE of the DBC is approximately  $8.1 \text{ ppm/mm } ^\circ\text{C}$ <sup>xlvii,xliii</sup>. The CTE differences between the materials within the structure are related to the stresses seen in the materials depending on temperature.

$$\mathbf{s}_{Thermal} = E\mathbf{a}(\Delta T)$$

where  $\sigma$  = stress magnitude,  
 $\alpha_1$  = linear coefficient of thermal expansion,  
 $\Delta T$  = change in temperature ( $T_o - T_f$ )

It follows that if  $T_f > T_o$  than the material is considered to be in compression and the stress is negative. If  $T_f < T_o$  than the material is considered to be in tension and the stress will be positive.<sup>xliiii</sup> In addition, the thermal strain,  $\epsilon$ , can be derived from the thermal stress using the fact that stress and strain are related by the elastic modulus,  $\mathbf{s} = E\mathbf{e}$ .

$$\mathbf{e}_{Thermal} = \mathbf{a}(\Delta T)$$

This prompted the development of a simplified model to understand the relative stresses visually observed in each layer. Broad assumptions were used to qualitatively compare stresses experienced by each layer in a tri-layer sample. The simplified model of the samples used in this study was made to calculate the stresses due to temperature change.<sup>xliv</sup> These stresses were used as a *qualitative measure* of where the stresses were most concentrated. The purpose of these calculations was to identify relative stresses, which may have lead to the eventual plastic deformation observed in the samples under test conditions. Simple elastic models were used to model the stresses in the x-direction of the device during thermal cycling. This is an indication of where stresses were elevated during thermal cycling.

The model looked at a symmetrical section of a layered sample resembling the soldered devices (Figure 3.2-37). The model represents each major layer in a tri-layer sample, where the labeled layers are as follows: 1= silicon die, 2= solder, 3=copper, 4=alumina. Each layer has a height,  $h$ , and there is a force,  $P$ , imposed on each layer as a function of the CTE mismatch.

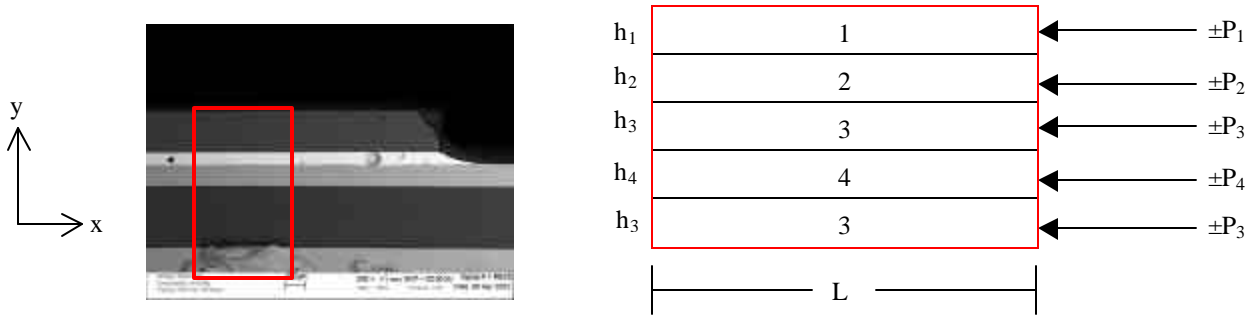


Figure 3.2-37: SEM image at 100x magnification of a cross-sectioned device (left) and a schematic of the model used to calculate the stresses in each layer (right).

Hooke's law was used to determine the strains in each layer. Assuming an isotropic material, since uniform thermal strains can occur in all directions, thermal strain can be added to the definition of Hooke's Law.<sup>xliii</sup>

$$\mathbf{e}_x = \frac{1}{E} [\mathbf{s}_x - \mathbf{n}(\mathbf{s}_y + \mathbf{s}_z)] + \mathbf{a}(\Delta T)$$

Since the model was assumed to be symmetrical, the stresses and strains in the x- and y- directions were found to be equal respectively and the stresses and strains in the z-direction were set to zero. Therefore, a single strain calculation for each layer is needed.

$$\mathbf{e}_x = \mathbf{e}_y, \quad \mathbf{e}_z = 0, \quad \mathbf{s}_x = \mathbf{s}_y, \quad \mathbf{s}_z = 0$$

$$\mathbf{e}_i = \frac{1}{E} [\mathbf{s}_i(1 - \mathbf{n})] + \mathbf{a}_i(\Delta T)$$

where the subscripts denote the layer in the model.

It was assumed that there were no external forces on the system only CTE stresses within the material, so the sum of the forces was determined to be zero. Additionally, the strains were all equal because the layers were assumed to be perfectly bonded.

$$\sum P_i = 0 \quad \mathbf{e}_1 = \mathbf{e}_{21} = \mathbf{e}_3 = \mathbf{e}_4$$

The definition of a stress is a force divided by the cross-sectional area. Therefore, the force could be related to the stress in each layer by the area, or height times the length of the layer. However, since the length is the same for each layer of the model the length, L, will fall out of the equation when the forces are summed.

$$P_1 = \mathbf{s}_1(h_1L)$$

where  $P_1$  = the force on layer 1,  $\mathbf{s}_1$  = the stress in layer 1,  $h_1$  = the height of layer 1, and L is the length of layer 1.

Therefore, to determine the effective stresses in each of the layers there will be four equations to be solved with four unknowns.

Four equations:

$$\mathbf{e}_1 = \mathbf{e}_2$$

$$\mathbf{e}_2 = \mathbf{e}_3$$

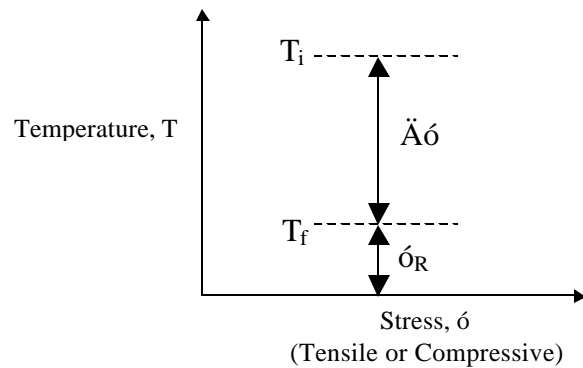
$$\mathbf{e}_3 = \mathbf{e}_4$$

$$\mathbf{s}_1 h_1 + \mathbf{s}_2 h_2 + \mathbf{s}_3 h_3 + \mathbf{s}_{31} h_{31} = 0$$

Four unknowns:

$$\acute{\sigma}_1, \acute{\sigma}_2, \acute{\sigma}_3, \acute{\sigma}_4$$

This calculation assumes that the sample is symmetrical and will have free expansion, i.e. none of the sides are fixed. This calculation also does not take into account any plastic deformation or creep that may occur. These calculations are related to the elastic strains occurring in the sample due to thermal fatigue. In addition, all of the materials are assumed to be in equilibrium at room temperature. The results from this calculation will determine an effective stress,  $\ddot{\sigma}$ , because the initial residual stresses,  $\acute{\sigma}_R$ , in the materials are unknown, as illustrated in Figure 3.2-38.



**Figure 3.2-38: Illustration of the change in stress over a temperature range, where the residual stress,  $\acute{\sigma}_R$ , is unknown.**

The material properties used for these calculations are listed in Table 3.2-2. The properties used were assumed at room temperature; however, these properties will change as the temperature drastically increases or decreases.<sup>xlv</sup>

**Table 3.2-2: Material properties used in stress calculations.**<sup>xlvi, xlvii, xlviii</sup>

Material	Modulus, E (GPa)	Poisson's Ratio, $\acute{\nu}$	CTE, $\acute{\alpha}$ (ppm/mm C)
Silicon	162	0.22	3
Solder	30	0.4	24
Cu	76	0.35	17
Al <sub>2</sub> O <sub>3</sub>	303	0.21	5

Further calculations at various temperatures with these modified properties may give more accurate information at various temperatures. However, since this model is a simplified case and so many assumptions have been made, this exercise is valid in qualitatively estimating the relative stresses in each layer. These stresses can be compared to identify the regions of highest stress. The experimental samples were tested under free expansion conditions because they were placed in the cycling chamber with no fixtures; therefore, a free expansion model is an acceptable assumption. In addition, damage was found throughout the solder layers from the center portions to the edges both in the x and y-directions. This suggests that the assumption of a symmetrical model with infinitely wide layers is representative of the observations made at 20 μm and less.

### 3.2.2.2 Results of the Calculations

A simplified model with broad assumptions was used to qualitatively compare stresses experienced by each layer in a tri-layer samples as a means to better understand the damage visually observed during this study. It was determined that upon heating from room temperature to 125 °C, the solder layer and Cu layers would experience compression while the silicon and alumina layers would be under tension. This follows reason that if the layers were assumed to retain the same shape at all temperatures that upon heating the solder and copper, with higher CTE values, would attempt to expand at a faster rate than the silicon and alumina layers. The silicon and alumina layers, with lower CTE values, would attempt to hold these layers back putting them in compression. Hence, the silicon and alumina layers would be in tension for the opposite reason. The case of cooling to -55 °C was also calculated. The resulting effect was the opposite of heating the samples where the solder layer experienced tension as the temperature decreased. The numerical values for the change in stress, Δσ's, show the following trend on heating and cooling, where the stress in the copper layer was the greatest in compression and in tension.

$$\sigma_{Cu} > \sigma_{solder} > \sigma_{silicon} > \sigma_{alumina}$$

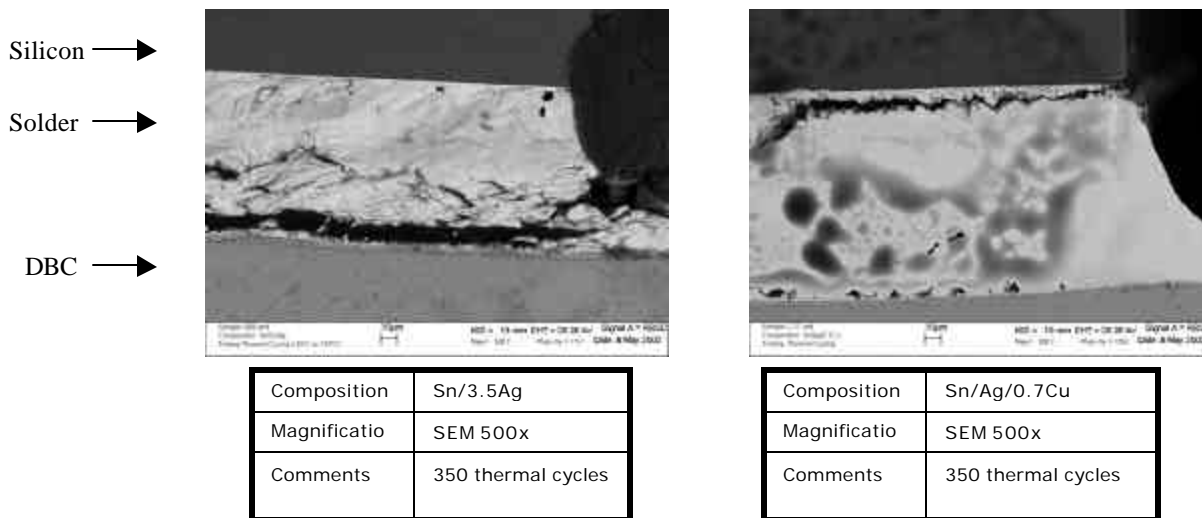
### 3.2.2.3 Computer Generated Finite Element Model

A finite element model of the samples was made with the same information as above. This model was run using IDEAS and ABAQUS.<sup>xlix</sup> These models were also used to qualitatively verify the regions of highest stress. The results used a plane strain model and assumed that the bottom of the sample was fixed. Similar to the above calculations, the model could not identify what was happening at the interfacial boundaries so the boundaries were assumed to be perfectly bonded. The model calculated stresses for the scenario that the temperature completed one thermal cycling beginning at 125 °C, cooling to -55 °C, and then returning to 125 °C. As discussed in Section 3.2 in Figure 3.2-4, it can be assumed that the

stresses in the materials in the samples were relaxed at the elevated temperatures. The thermally cycled samples were held for five minutes at the maximum temperature. Therefore, the calculated  $\bar{\sigma}$  will be the dominant stress.

In the case of strain, it was found that the highest strains would be in the solder layer closest to the edge (Figure 3.2-40). Hence, the conclusion from this models is that the material would first fail in the solder material rather than at the interface due to the assumptions. The stress results indicate that the concentration of stress for the whole structure is in the DBC (Figure 3.2-41). This is an indication that the stresses closest to the solder/DBC interface where the greatest damage was observed resulted from the elevated stresses in the DBC as compared with the rest of the structure. Von Mises stresses and strains were used in Figure 3.2-40 and Figure 3.2-41, where the principal stresses,  $\sigma_1$ ,  $\sigma_2$ ,  $\sigma_3$ , are used to calculate the effective stress.

$$\bar{\sigma}_H = \frac{1}{\sqrt{2}} \sqrt{(\sigma_1 - \sigma_2)^2 + (\sigma_2 - \sigma_3)^2 + (\sigma_3 - \sigma_1)^2}$$



**Figure 3.2-39: Images of cracks found at the edge of the solder under at the point of highest calculated strains.**



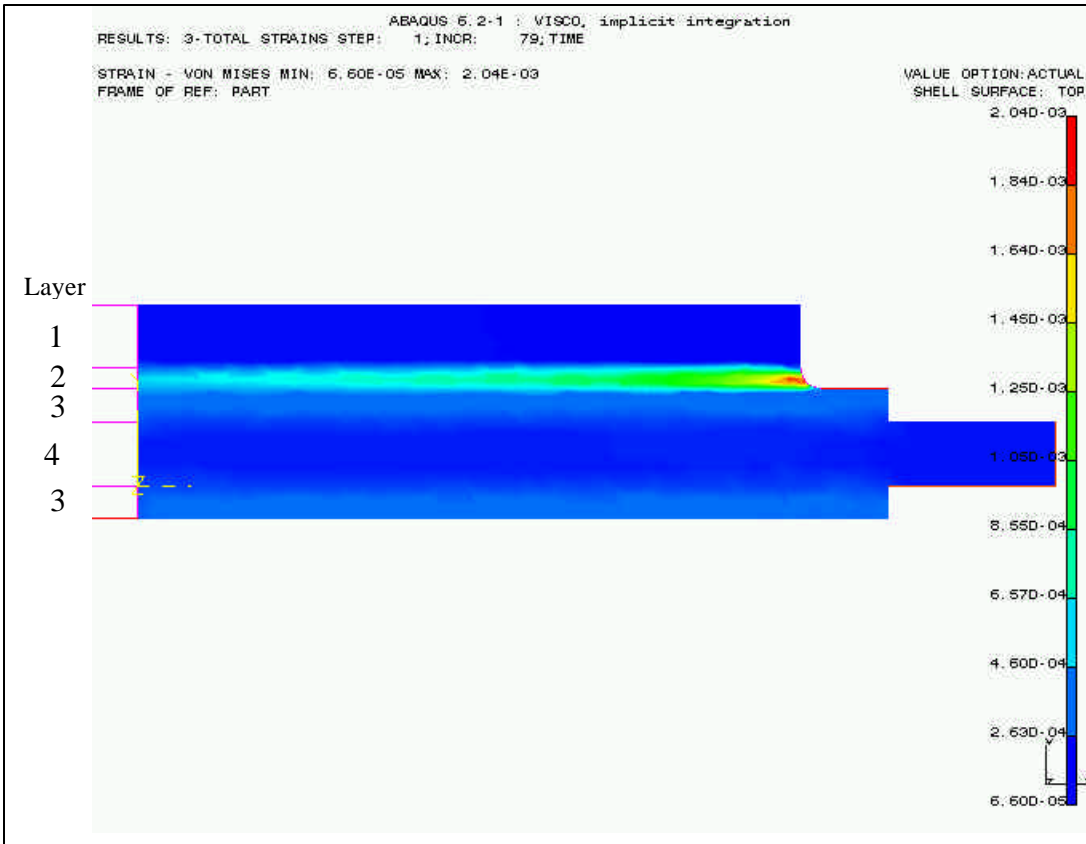


Figure 3.2-40: Von Mises strains calculated for a layered power device temperature cycled between 125 C and -55 C.

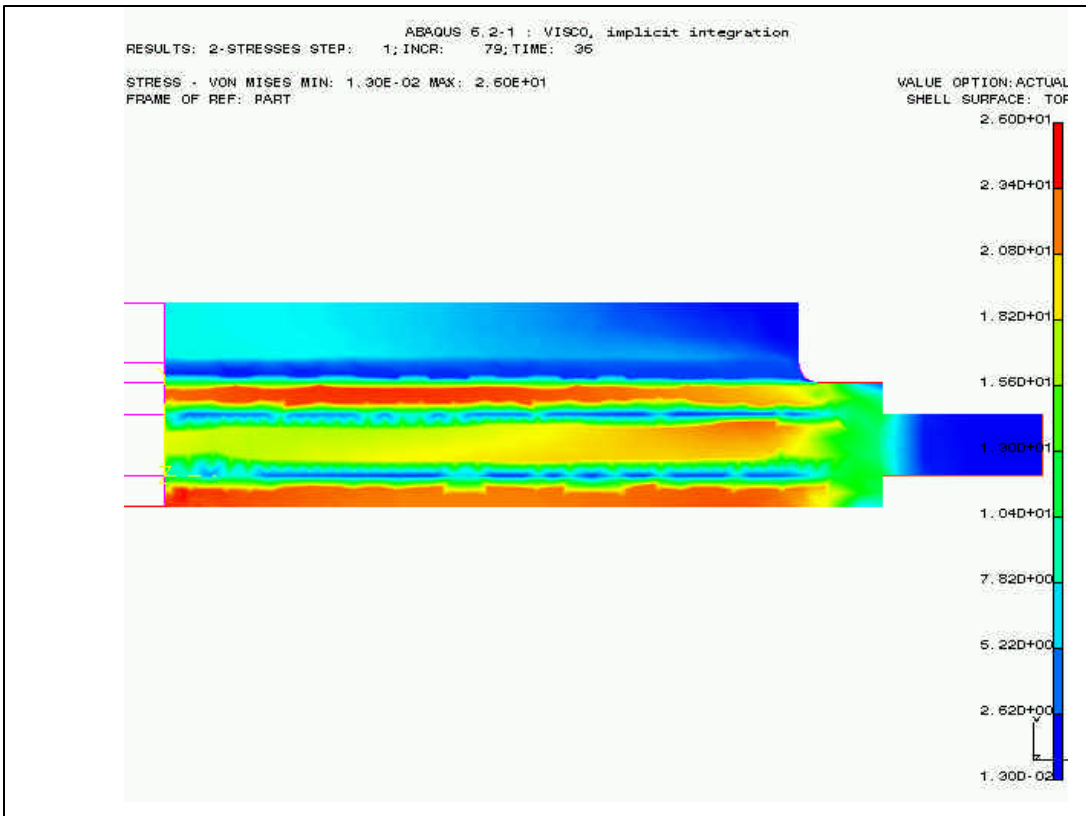


Figure 3.2-41: Von Mises stresses calculated for a layered power device temperature cycled between 125 C and -55 C.

A closer look at the solder layer reveals that the stresses in the x-direction are higher than in the silicon layer. Figure 3.2-42 illustrates the stresses upon heating and cooling in the x-direction. The red in the images indicates higher tensile stresses while the blue indicates higher compressive stresses. Upon heating, the solder and the copper are found to be in compression with respect to the rest of the structure. Upon cooling, the solder and the copper layers are found to be under tension with respect to the rest of the structure. This is in agreement with the numerical model calculated earlier, further indicating that the highest stresses are concentrated towards the DBC layers. This can account for the greater damage being observed in the solder at the solder/ DBC interface.

Finally, previous work has shown that silicon dies have a region of elastic deformation, which allows for the material to flex under a limited amount of stress.<sup>1</sup> The gradient across the silicon layer in Figure 3.2-42 may be an indication of this. Hence, the silicon would impose less stress on the solder layer because it would be able to absorb a certain amount of the deformation rather than sending them to the solder layer. This is in contrast to the DBDC substrate, which is a more rigid component and does not flex under any given stress.

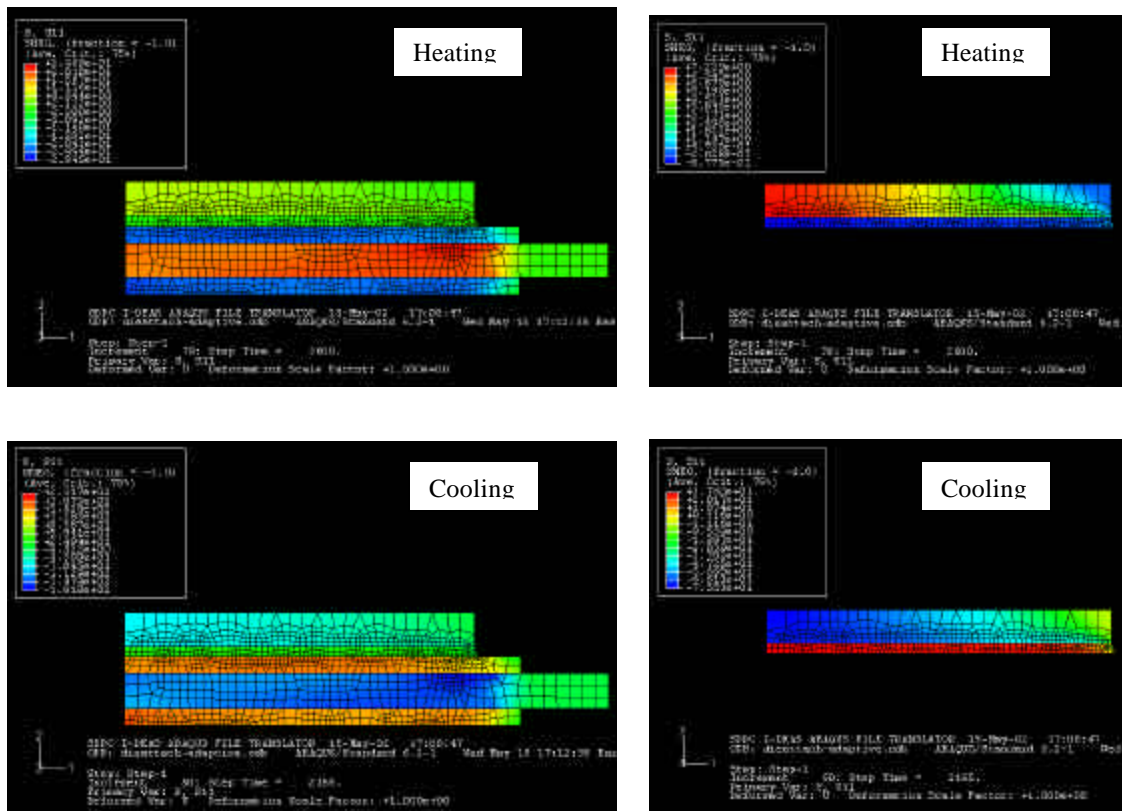
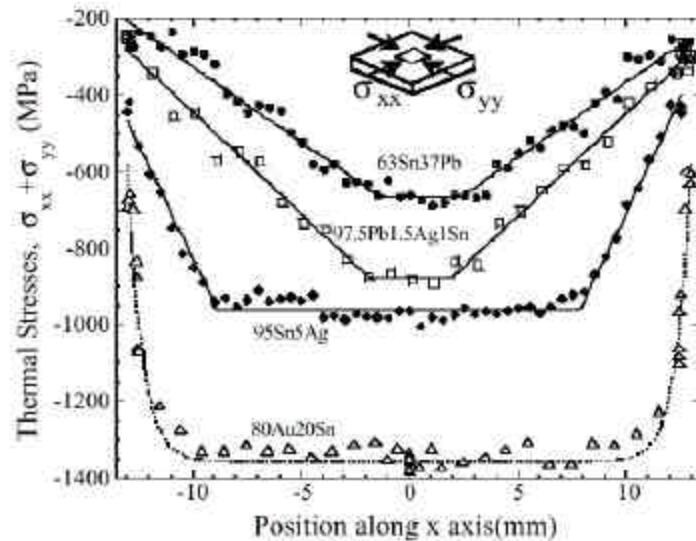


Figure 3.2-42: Stresses for heating (top) and for cooling (bottom) in the x-direction. The images on the left are of the whole modeled structure. The images on the right are close-up evaluations of the silicon and solder layers.

Jun He, et. al. studied the effect of thermal expansion mismatch and silicon die size to the reliability of large-area surface mount assemblies.<sup>xvii</sup> They found that thermal stresses in the overall device will increase closer to the edge of the die and will decrease with a decrease in the size of the die. In addition, different solder compositions will have an effect on the thermal stress distribution in the silicon die (Figure 3.2-43). As discussed earlier, the stresses in the silicon were observed to have transferred to the solder layer. Hence, the stress distribution across the silicon may resemble the fact that there is a stress distribution within the solder layer.



**Figure 3.2-43: Stress distributions in silicon die attach on copper after fabrication.**<sup>xvii</sup>

The “hard” solders such as 80Au/20Sn and 95Sn/5Ag were found to exhibit elastic behavior with a larger shear lag zone and a rapid increase at the edge of the die. The shear lag zones being defined as the horizontal portions in the plot. With the “softer” solders such as 63Sn/37Pb and 97.5Pb/1.5Ag/1Sn, the shear lag zone is concentrated in a small region at the center of the die and the stresses towards the edge of the die increase with distance to the edge. In addition, they also studied the peel strength of the solder materials and found that because the interfacial shear and peeling stresses are proportional to the solder yield strength that cracks are more likely to grow in “hard” solders than in “soft” solders. However, “soft” solders are more subject to creep. They conclude by stating, “the magnitude and distribution of these thermal stresses are governed by the CTE mismatch, the elastic and geometric properties of the device, substrates and most importantly by the solder shear yield strength  $\hat{\sigma}_y$  and creep rate.”<sup>xvii</sup> The yield strengths and other material properties of the solders observed in this study are listed in Table 3.2-2. The tensile yield strength of the Sn/37Pb solder on average is higher than for Sn/3.5Ag, therefore, the Sn/37Pb has a higher stress accommodation. In addition, the Young’s Modulus and the Shear Modulus for Sn/3.5Ag is generally higher than for Sn/37Pb supporting the “hard” solder label for the Sn/3.5Ag alloy. As the modulus value increases, the stiffer the material, or the smaller the elastic strain.

Table 3.2-3: Material properties of the solders used in this study. <sup>li, lii, xviii</sup>

Composition	Yield Strength	Young's Modulus	Shear Strength <sup>liiii</sup>	Shear Modulus	CTE	Hardness
Sn/37Pb	43 MPa	30-40 GPa	28.4 MPa	10-15 GPa	23.5-26 µ strain/K	10-22.5 HV
Sn/3.5Ag	22.5 MPa	50-60 GPa	32.1 MPa	15-25 GPa	20-30 µ strain/K	10-20 HV

Building on the simple model described previously and the behavior of the materials in the simple model, additional complexities to the behavior of the samples can be explored. Since the silicon was determined to have a finite range of "flexibility" there may have been bending in the silicon. This would have created a bending moment in the solder layer. However, since the DBC was the rigid component the solder adjacent to the DBC would not have been allowed to bend. Assuming that the bending was concave, or the edges of the silicon bent away from the DBC, the solder closest to the DBC would have been in tension and the solder closest to the silicon would have been in compression (Figure 3.2-44). Hence the shear cracking observed in the solder layers most recognizable, as a diagonal crack was likely due to tensile stresses. Likewise, at the edges of the same where the stresses were predicted to be highest would have the greatest tensile stresses pulling on the solder layer. Consequently, cracking in these regions was found to be both at the solder/DBC and solder/silicon interfaces. Additionally, because of the repeated thermal cycling, both the tensile regions and compressive regions with respect to the bending moment would have contributed to the crack growth. Therefore, a factor in the stress gradient observed across the solder layer as well as in localized regions may have been due to the bending in the silicon and the non-bending in the DBC.

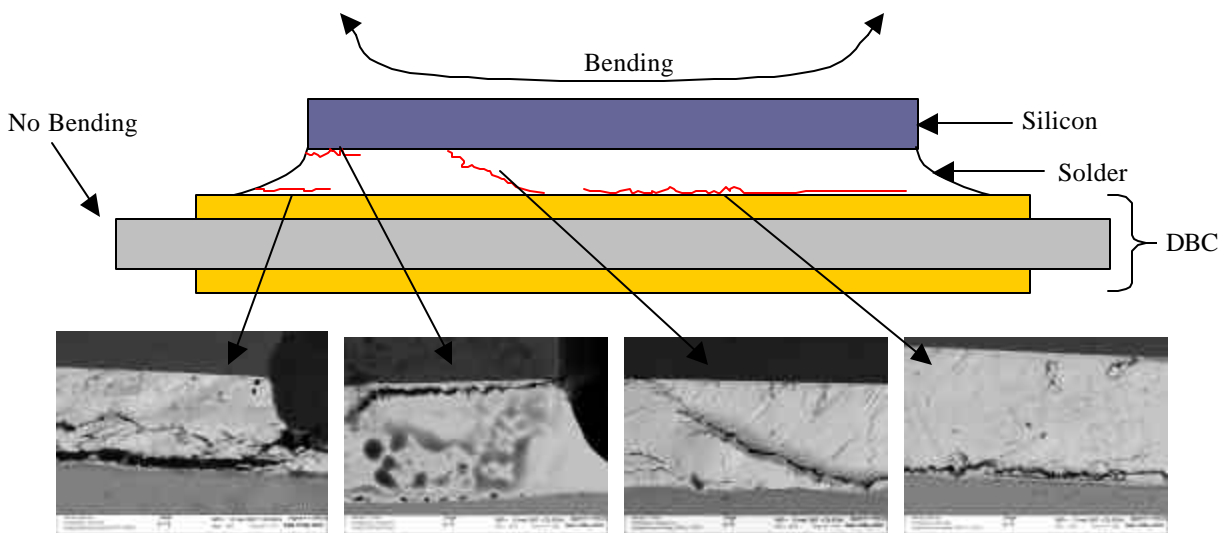


Figure 3.2-44: Cracking characteristics across a sample.

## Conclusion

A computational model was designed and tested under similar boundary conditions and assumptions as for the numerical calculations. The computational model calculated stresses for the scenario that the temperature completed one thermal cycling beginning at 125 °C, cooling to 55 °C, and then returning to 125 °C. The relative results agreed with the numerical models for where the highest and least stresses would be found within the structure. In addition, it was noted that elevated stresses would occur at the edge of the solder region. This was in agreement with the observations where severe cracking between both the solder/DBC and solder/silicon interfaces. In addition, it was determined that upon heating the solder layer would experience a more compressive force while on cooling it would experience more tensile forces.

The conclusion was drawn that the silicon had a finite range of “flexibility” for which the computational model illustrated. The silicon had a range of stresses throughout the sample upon cooling and heating. In addition, the DBC was found to have experience a more content stress that was calculated to be the highest. Because of the nature of the cracking observed and the results of the calculations, it was determined that the cracking at the DBC/solder interface was most likely. Further, it could be concluded that because of the “flexibility” of the silicon and the rigidity of the DBC, the solder may have experienced forces in the y-direction with respect to a bending moment in the silicon. This correlates with the 45 degree angle shear cracking within the thickness of the solder layer and the extreme cracking at the edges of the solder.

### 3.2.2.4 Intermetallic Changes

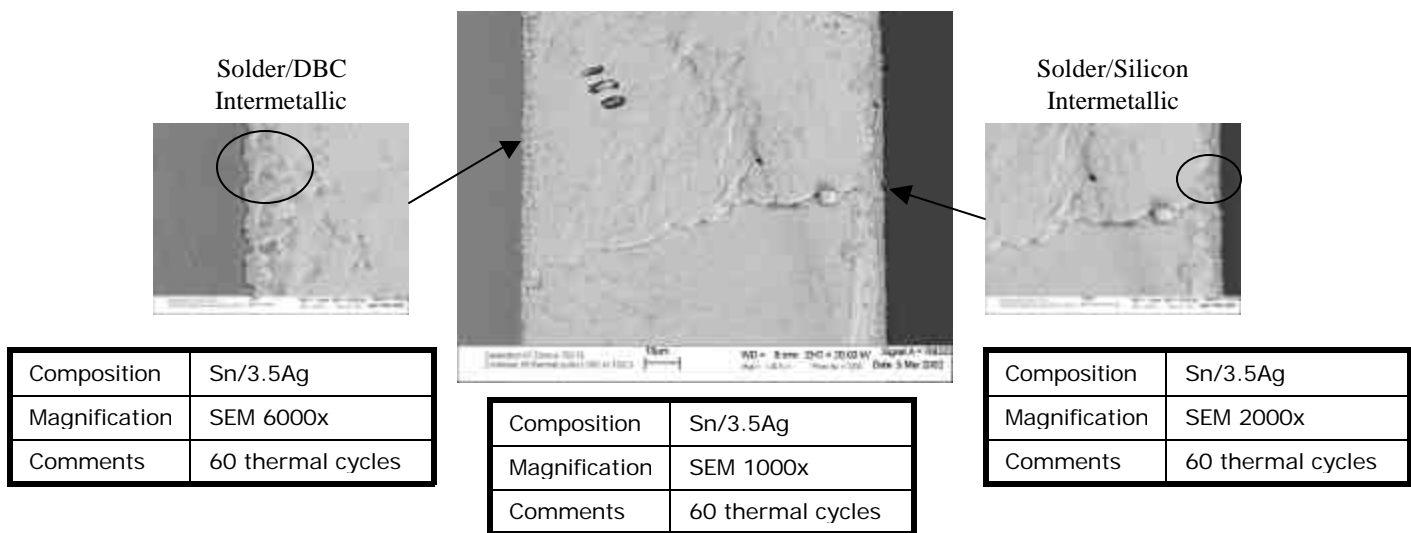
When a molten solder comes in contact with a Ni or Cu surface metallization, the solder will wet the surface and react to form interfacial intermetallics, or reaction layers. Figure 3.2-45 contains images taken during this study of a cross-section of a tri-layer sample containing the Sn/3.5Ag solder alloy. The kinetics of growth is different for different solder alloys. Initial intermetallic layer thickness is a function of reflow temperature and time.<sup>liv</sup> These intermetallics will grow out into the solder as rods, or plates, and will continue to grow when the solder is solid.<sup>xxi</sup> With increasing reflow time the thickness will increase while the number of “hills and valleys” of the intermetallic will decrease.<sup>liv</sup>

The formation and growth of intermetallics has been described as being influenced through solid-state diffusion flux, grain boundary diffusion during soldering, and through the ripening effect during soldering.<sup>lv</sup> Most previous works have shown that intermetallics will change with time and this change, or growth, can be a source of mechanical and electrical weakness.<sup>xxii</sup> Therefore, intermetallic interfaces created upon the reflow of solder joints can be related to reliability within electronic packages.

On a copper surface, Sn-rich alloys will form a two phase intermetallic of  $\text{Cu}_6\text{Sn}_5$  adjacent to the solder and  $\text{Cu}_3\text{Sn}$  adjacent to the copper.<sup>liv,xxi,lv,lvi</sup> On a nickel surface, Sn-rich alloys will form an intermetallic consisting of  $\text{Ni}_3\text{Sn}_4$ . Solders containing silver may contain a layer adjacent to the solder of  $\text{Ag}_3\text{Sn}$ .<sup>xxi</sup>

The intermetallic layers were found to have a gradient composition across thickness from the solder to the surface metallization for all of the sample constructions. These gradients were illustrated using an electron microprobe with wavelength-dispersive spectroscopy.

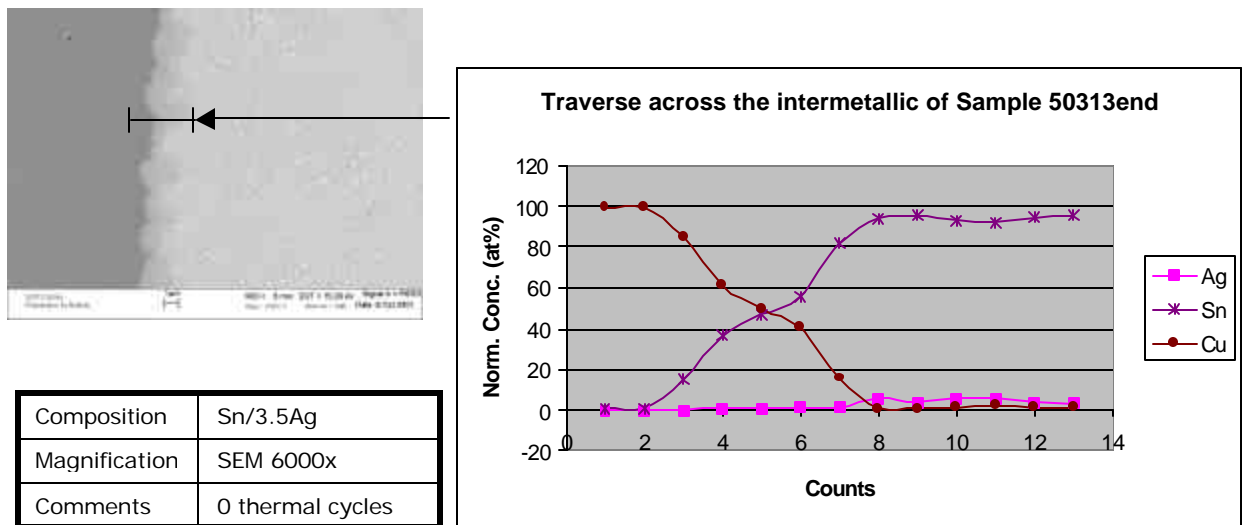
Figure 3.2-46 is a plot of the composition across the intermetallic between a plain copper DBC substrate and the Sn/3.5Ag solder. The silver in the solder alloy did not combine with the copper because the diffusion of Sn and Cu was preferential.



**Figure 3.2-45: Intermetallic growth adjacent to the DBC substrate on the left and adjacent to the silicon on the right.**

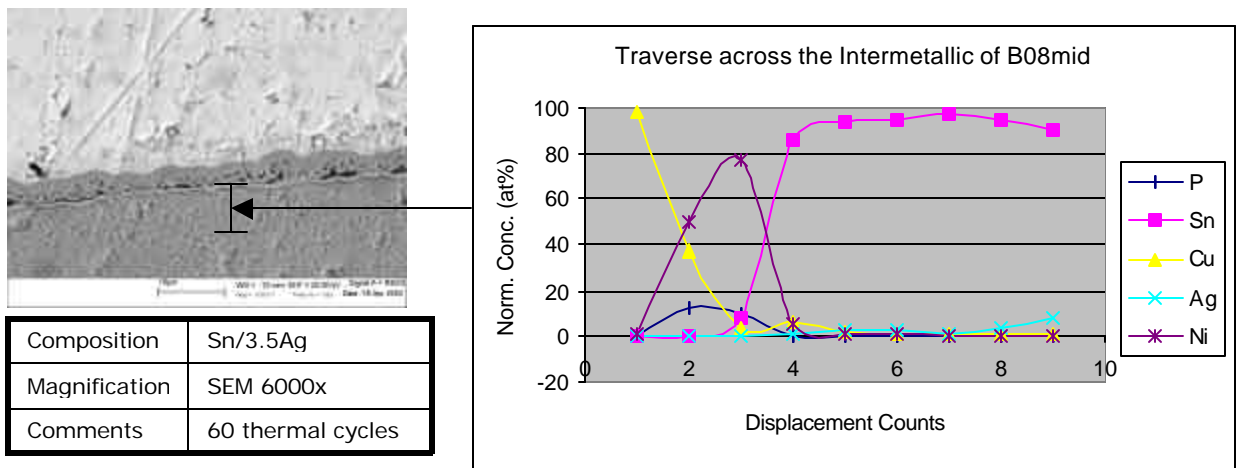
The intermetallic in the Sn/37Pb samples is either  $\text{Ni}_3\text{Sn}_4$  when soldered to the Ni-plated surface or a combination of  $\text{Cu}_6\text{Sn}_5$  and  $\text{Cu}_3\text{Sn}$  when soldered to the plain copper surface, the  $\text{Cu}_3\text{Sn}$  compound being closest to the Cu substrate.<sup>xxii</sup> The lead-free samples contained similar intermetallic layers. Since the MOSFET silicon die was Ni-plated for solderability, the intermetallic at that interface was also found to be  $\text{Ni}_3\text{Sn}_4$ .

In the samples containing Ni-plated DBC, again the Ag was not a major component; however, the diffusion of Sn and Ni was preferential over Sn and Cu. Therefore the intermetallic does not contain Cu as shown in Figure 3.2-47. These results are in agreement with work presented in literature studying the effectiveness of the Ni layer as a diffusion barrier between the Sn and Cu of the solder and the substrate, respectively. The research presented in literature determined that the Ni-plated layer was an effective diffusion barrier even after 500 hours of aging at 160 °C.<sup>lvii</sup>



**Figure 3.2-46: Traverse of the intermetallic formed between a Sn/3.5Ag solder and a plain copper DBC substrate.**

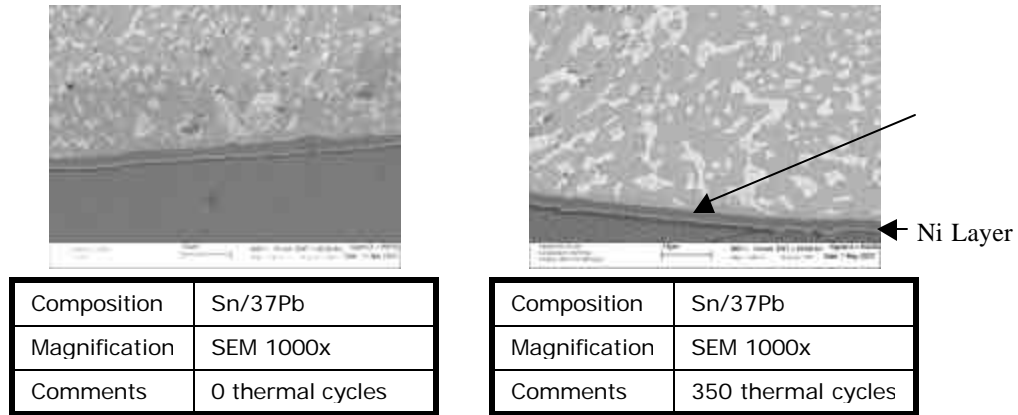
It was also found during the current research that the Ni-plating contained a large amount of phosphorous. This was expected because during the processing of the DBC substrate, Ni is generally added for a more cosmetic finish. Consequently, during the construction of the samples a vacuum reflow process was attempted for soldering. However, the process was not successful, which may have been due to the large amount of phosphorous present in the Ni-plated surface. Additional evaluations of the intermetallic regions are discussed further in the Appendix 6.2.



**Figure 3.2-47: Traverse of the intermetallic formed between a Sn/3.5Ag solder and a Ni-plated DBC substrate.**

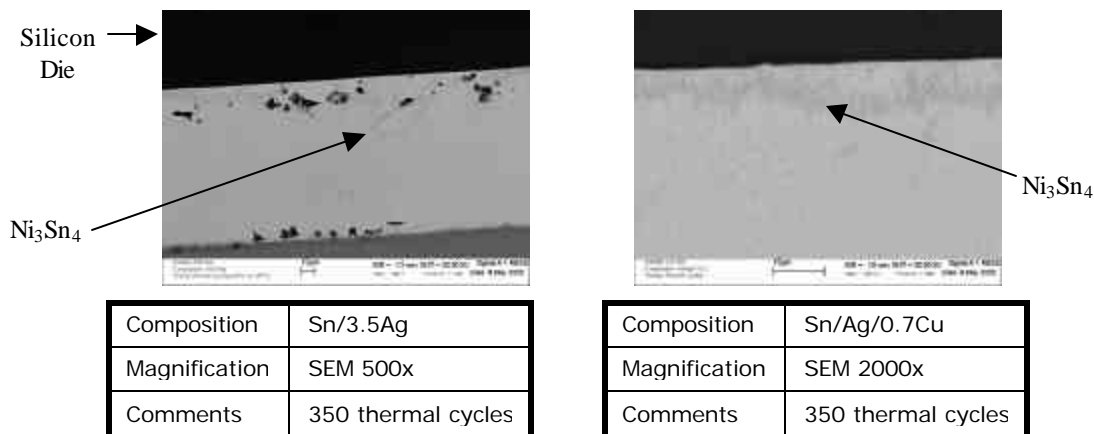
The intermetallic in the Sn/37Pb solder was not apparent in the untested samples; however, it became more visible with aging (thermal cycling and isothermal aging (Figure 3.2-48)). The growth of intermetallic layers is influenced by four factors for Sn/37Pb: (a) the Pb-

rich phase accumulation at the intermetallic layer/solder interface, (b) the intermetallic layer thickness, (c) the  $\text{Cu}_6\text{Sn}_5$  particles, and (d) the number of interface boundaries encountered by the diffusing species.<sup>lv, xxii</sup> A closer look at the intermetallic regions in Figure 3.2-48 reveals that there is an abundance of the Pb-phase in that region. In addition, the Ni-plating between the Cu and the solder is a diffusion barrier, which influenced any changes in the  $\text{Cu}_6\text{Sn}_5$  intermetallic compound.



**Figure 3.2-48: Illustration of the intermetallic layers between the Sn/37Pb solder and a Ni-plated surface.**

An unusual observation was that the Ni-plating from the Si-die in the lead-free alloys migrated into the solder as seen in Figure 3.2-49. The movement of the intermetallic compound did not seem to follow along with cracking or damage. In addition, the same intermetallic compound at the solder/substrate interface did not seem to migrate into the solder. There are two major differences between the solder/silicon intermetallic and the solder/DBC substrate intermetallic. First, the Ni-plating at the silicon die is likely not as well bonded as that at the copper DBC substrate. Second, the geometry of the samples meant that the silicon was always placed in the testing chambers facing up. Gravity may have been a factor in the movement of the Ni-plating down into the solder.



**Figure 3.2-49: Intermetallic migrating into the solder layer.**



The  $\text{Ni}_3\text{Sn}_4$  and  $\text{Cu}_6\text{Sn}_5$  intermetallic layers in the lead-free solders formed into peninsula-like shapes protruding up into the solder layer (Figure 3.2-50). These formations became more pronounced with aging time and thermal cycling. In the Sn/37Pb solder samples; this growth of the intermetallic into the solder layer was not as drastic.

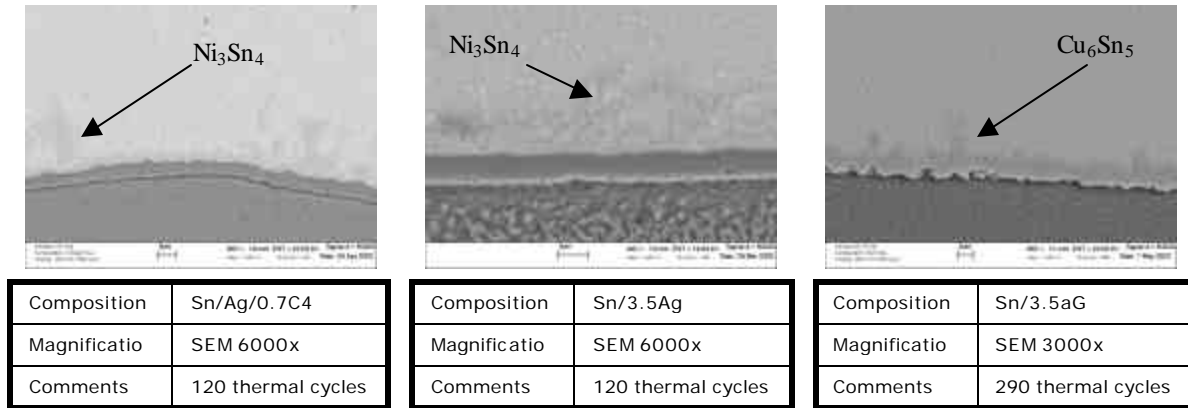


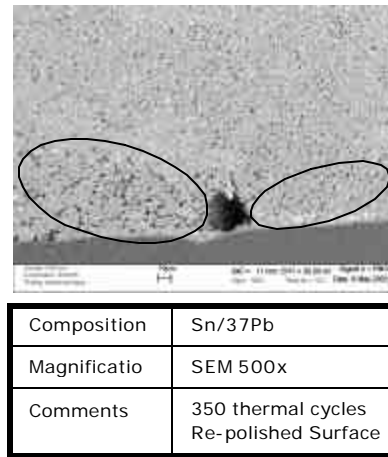
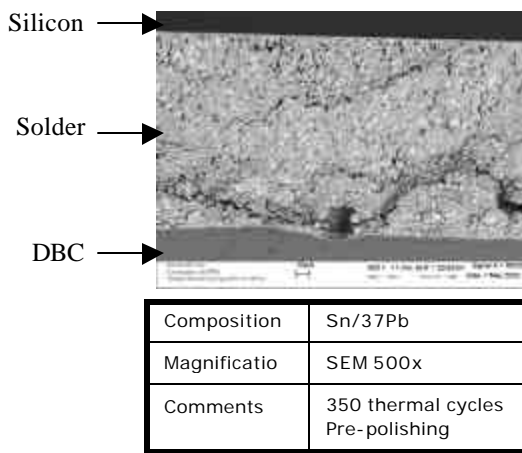
Figure 3.2-50: The  $\text{Ni}_3\text{Sn}_4$  intermetallic layer.

## Conclusion

Intermetallics between the solder and metallizations of the DBC and silicon die were formed upon reflow of the solder alloy. The intermetallics formed from a Sn-based solder and a Cu surface to the solder  $\text{Cu}_6\text{Sn}_5$  is formed and closest to the Cu,  $\text{Cu}_3\text{Sn}$  is formed. With a Ni surface, the intermetallic formed with an Sn-based solder is  $\text{Ni}_3\text{Sn}_4$ . With time the intermetallics at the DBC substrate grew slightly in overall thickness. The most prevalent changes were irregular finger-like growth moving up into the solder. In addition, the intermetallics formed at the silicon interface were found to move away from the interface down into the solder. This is still an unexplained observation.

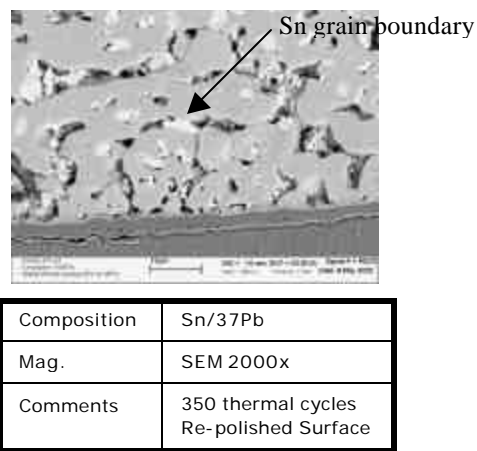
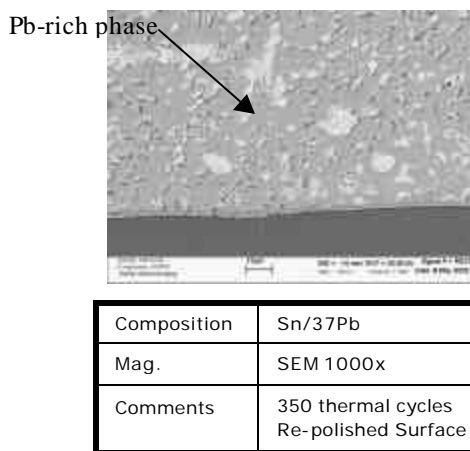
### 3.2.2.5 Pitting

A number of the samples were re-polished periodically to observe the damage that occurred due to testing without any surface effects. This revealed pitting in the Sn/37Pb samples that was observed to follow general damage patterns. Figure 3.2-51 illustrates the same region of an Sn/37Pb tri-layer sample before and after polishing. The pitting in the re-polished sample appears to be concentrated adjacent to the intermetallic region close to the void. The pitting also seems to have a directional pattern that reflects the damage seen in the sample prior to polishing. A shallow crack propagates at an angle adjacent to and away from the intermetallic layer through the void in the un-polished sample. The concentrated pitting follows the same pattern.

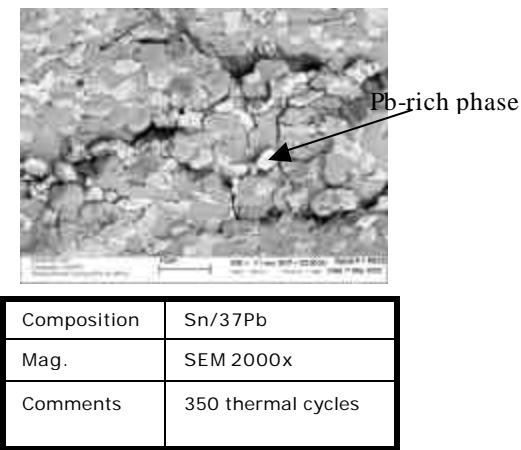


**Figure 3.2-51: Damage visible in the same sample at 350 thermal cycles before and after polishing.**

The pitting in the Sn/37Pb samples appeared to mainly be in the tin-rich regions. In addition, much of the pitting formed around the Pb-rich phases. Figure 3.2-52 illustrates the pitting after re-polishing in the samples. This reflects the observations made prior to polishing as illustrated in Figure 3.2-53. Dislocation motion, which promoted cracking in the material, followed along the phase boundaries between the Sn and Pb-rich phases.

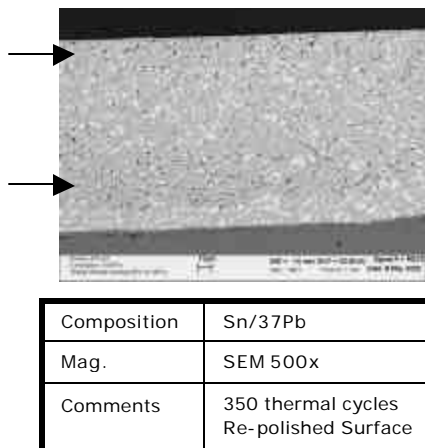


**Figure 3.2-52: Re-polished Sn/37Pb samples where the pitting is occurring in the Sn-rich regions and around the Pb-rich areas.**

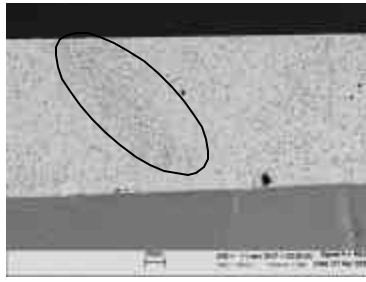


**Figure 3.2-53: A Sn/37Pb sample prior to polishing, illustrating the damage after testing.**

The pitting followed patterns within the solder layer close to the interfaces between the solder and the DBC or the solder and the silicon (Figure 3.2-54). In addition, patterns of the pitted regions were found to follow diagonal paths across the solder layer (Figure 3.2-55). These indicated that the pitting might be due to the damage that developed mostly through thermal cycling. The thermal cycling test condition caused the greatest damage in all of the sample constructions. Specifically, the tri-layer samples experienced the greatest CTE mismatch causing the most severe damage. The diagonal patterns are similar to the diagonal cracking seen in the un-polished, lead-free solder samples at 45-degree angles to the interfaces.



**Figure 3.2-54: The pitting was found in patterns on the surface of the re-polished Sn/37Pb samples.**



Composition	Sn/37Pb
Mag.	SEM 500x
Comments	350 thermal cycles Re-polished Surface

**Figure 3.2-55: Pitting pattern found at a diagonal in the solder layer.**

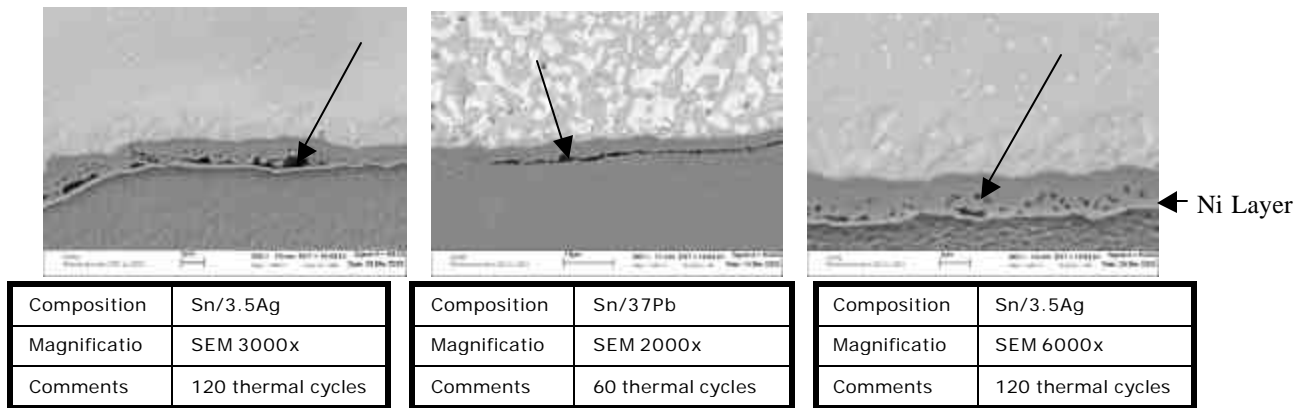
## Conclusion

The pitting that was observed in the Sn/37Pb solder samples after re-polishing the tested samples are evidence of damage. The pitting in many cases was found to follow patterns similar to the patterns of damage observed prior to polishing. The patterns revealed pitting concentrated close to the solder/DBC interface and angular patterns across the solder layer thickness.

### 3.3 Secondary Observations

#### 3.3.1 Kirkendall Effect

The observation was made that within the Ni-plating there were unusual voids, which in many cases increased in number, evolved into larger voids, and/or generated a crack between the Ni metallization and the Cu DBC surface. These changes were seen with increased testing times and thermal cycling as seen in Figure 3.3-1. These voids were identified to have developed due to the Kirkendall Effect. The Kirkendall effect is defined as the formation of voids by diffusion across the interface between two different materials. The formation of voids is a result of a disproportional diffusion rate between two neighboring materials. The voids occur in the material having the greater diffusion rate into the other.<sup>lviii, lix</sup> Figure 3.3-2 shows the production of voids, or porosity, ever 1 minute and 15 minute periods.



**Figure 3.3-1: Voids and cracks between the Ni metallization and the Cu substrate due to the Kirkendall effect.**

An electron microprobe was used to evaluate the compositional nature of the solder/substrate intermetallic regions of the dual and tri-layered samples. Figure 3.3-3 is a plot of a compositional traverse data collection across the intermetallic region from the DBC substrate to the solder, left to right respectively. Only the Ni and Cu components have been shown in this plot. There is gradient composition across the Ni-plated layer and the voids, or porosity, observed in the SEM images would be located to the left within this plot.

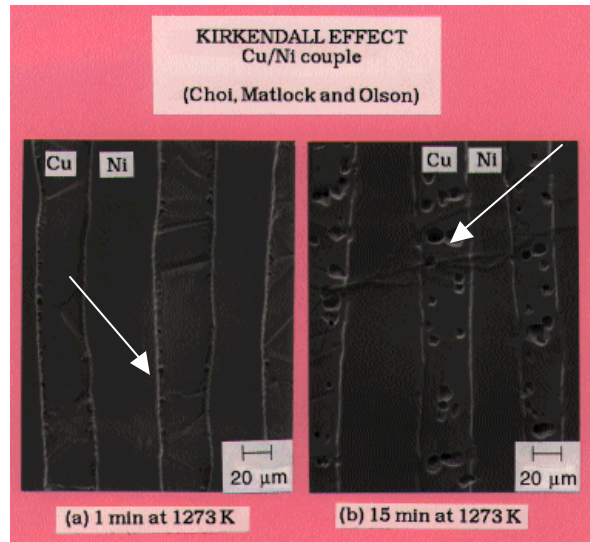


Figure 3.3-2: Kirkendall effect observed in a Cu/Ni couple over 1 minute and 15 minute periods at 1000 °C.

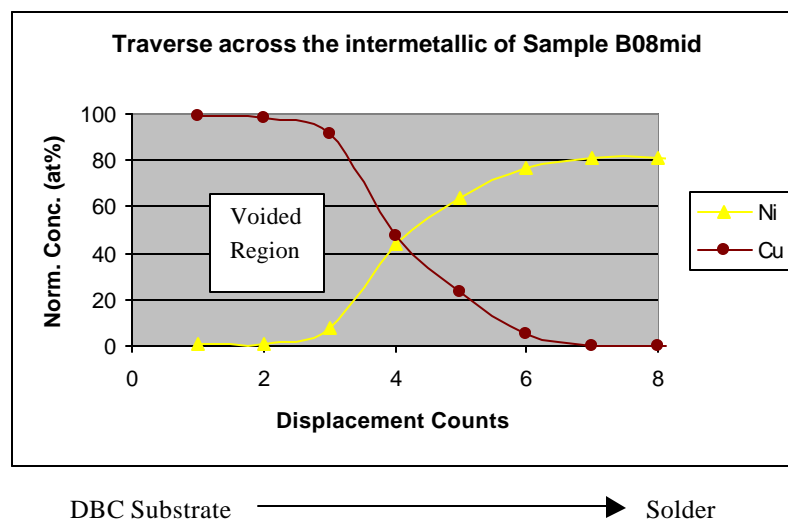


Figure 3.3-3: The Ni and Cu components of a compositional traverse across the intermetallic between a Cu DBC substrate and Sn/3.5Ag solder.

Fick's first law with respect to interdiffusion between two differing materials, A and B, can be written as, Darken's Equations:

$$J'_A = -\tilde{D} \frac{\partial C_A}{\partial x} \quad \text{and} \quad J'_B = -\tilde{D} \frac{\partial C_B}{\partial x}$$

where  $\tilde{D}$  is the interdiffusion coefficient,  $J'_A$  and  $J'_B$  are flux as a function of composition,  $C_A$  and  $C_B$ , and position,  $x$ . The interdiffusion coefficient is defined as:

$$\tilde{D} = X_B D_A + X_A D_B$$

where  $D_A$  and  $D_B$  are the diffusion of components A and B; and  $X_A$  and  $X_B$  are the compositions of the components.<sup>xxxii, xix</sup>

The vacancies, which are detected as porosity, are created and travel with the diffusing material. Hence, in Figure 3.3-4 the flux for component B is greater than for A. The vacancies are created in material B and move into material A, i.e. porosity is found in the material with the highest diffusion rate.

In Cu-Ni alloy systems,  $D_{Cu}$ ,  $D_{Ni}$ , and  $\tilde{D}$  are all composition dependent, increasing as  $X_{Cu}$  increases.<sup>xix</sup> Figure 3.3-5 illustrates the increase in the inter-diffusion between the materials as the amount of Cu increases. This suggests that the voids should be found in the Cu material. As seen in Figure 3.3-3, the porosity was discovered in the Cu-rich region across the Ni-plating.

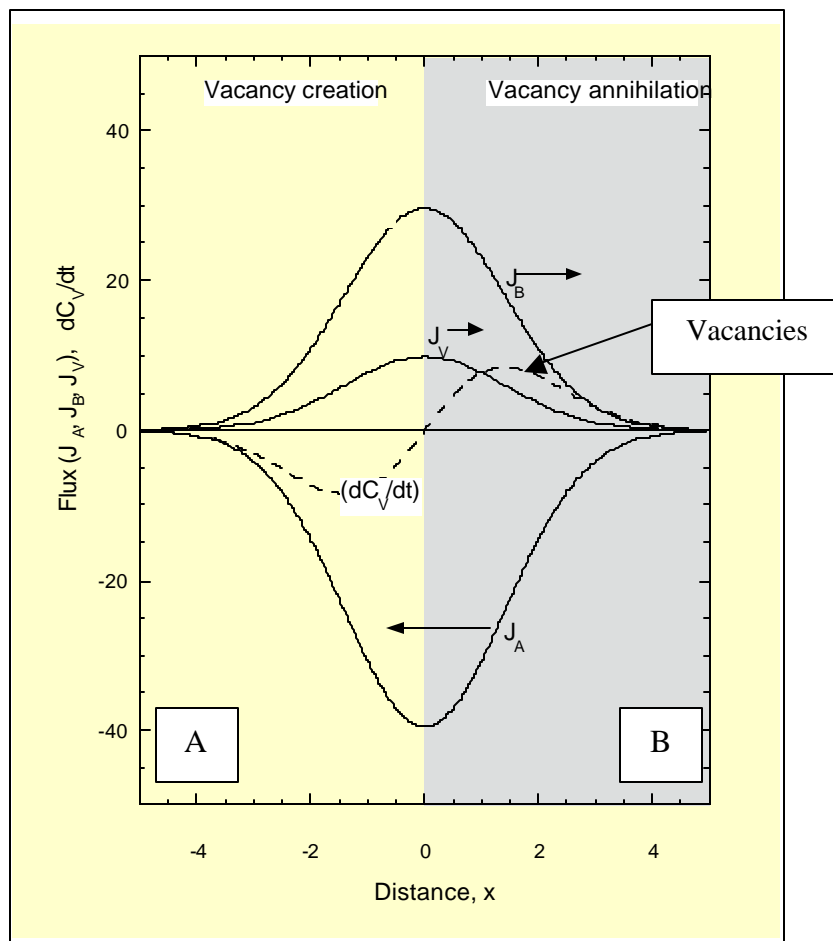


Figure 3.3-4: Fluxes representing Cu, Ni and the vacancies created during diffusion.<sup>xix</sup>

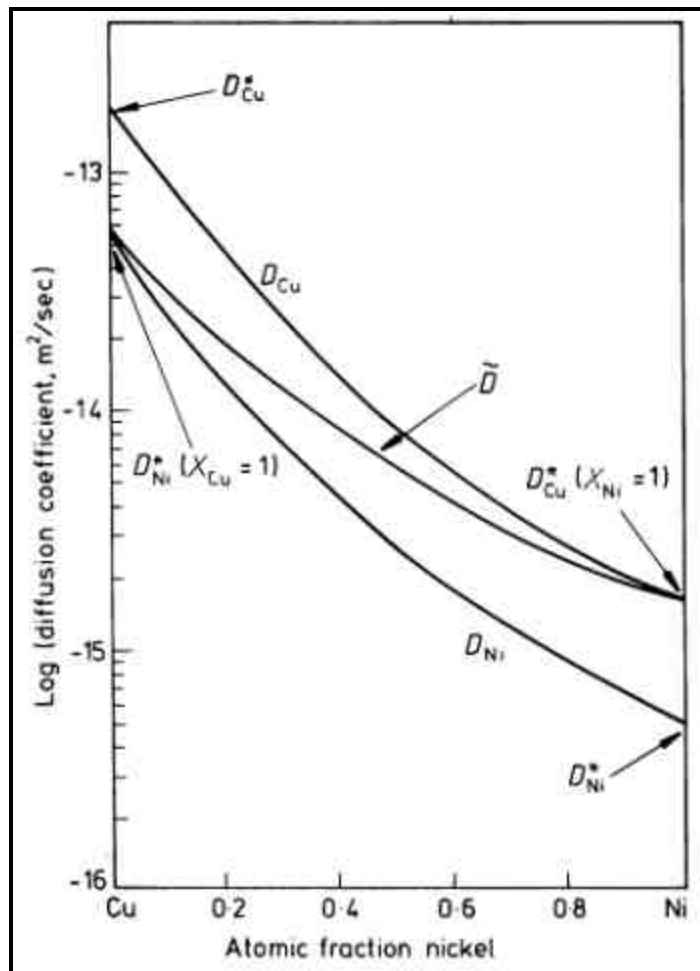


Figure 3.3-5: The relationship between the various diffusion coefficients in the Cu-Ni system at 1000 C.<sup>xix</sup>

Further Figure 3.3-6 shows that the self-diffusion and creep diffusion activation energies for Cu are higher than for Ni. Again, the porosity was found in the Ni layer closest to the Cu side of the layer. Other studies with respect to electronic interconnects have been done and have show that Kirkendall porosity can be found between other materials. Figure 3.3-7 is an image of Kirkendall porosity as seen in the intermetallic of a solder joint with Sn/Ag solder alloy. The porosity was found in the Cu<sub>3</sub>Sn region of the intermetallic adjacent to the Cu substrate. This indicates that the Cu<sub>3</sub>Sn compound has a higher diffusion rate, though pure Sn has a lower activation energy for diffusion than Cu (Figure 3.3-6).



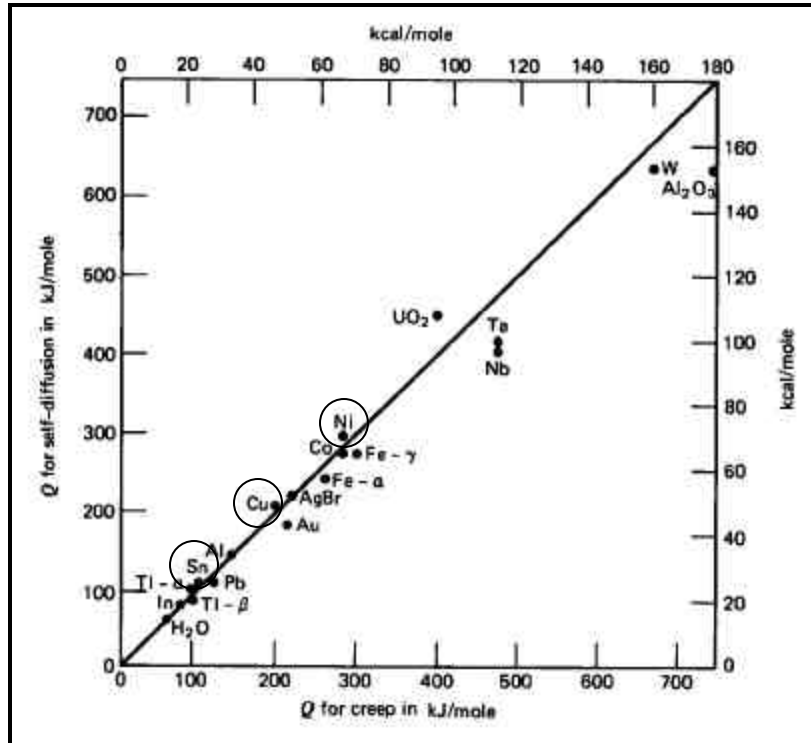


Figure 3.3-6: Correlation of the activation energy for self-diffusion versus creep diffusion for various metals and ceramics.<sup>xxxvi</sup>

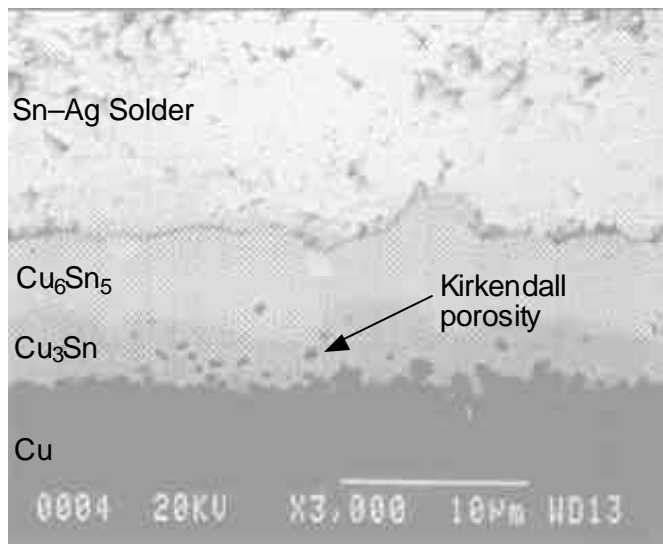
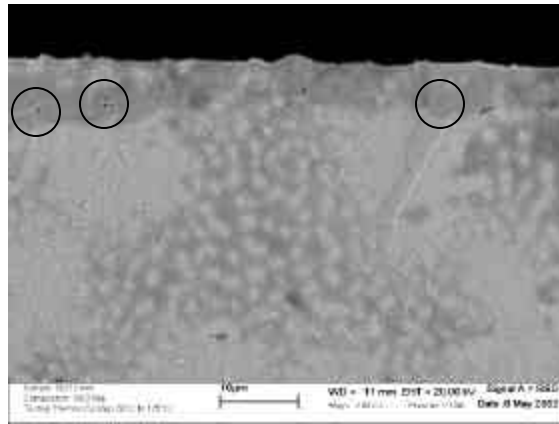


Figure 3.3-7: Kirkendall porosity in the intermetallic layer.<sup>lxi</sup>

The Ni-plating on the silicon die was found to migrate into the solder layer. Kirkendall porosity was found in the migrating Ni-rich layer as seen in Figure 3.3-8.



Composition	Sn/3.5Ag
Magnificatio	SEM 2000x
Comments	290 thermal cycles

**Figure 3.3-8: Kirkendall porosity found in the intermetallic formed between the Sn-rich solder and the Ni metallization on the silicon die.**

## Conclusion

Within the Ni plating on the DBC substrate, Kirkendall porosity was identified. This was a result of the fact that Cu diffuses faster than Ni. These voids were initially formed during the plating process; however, with time the porosity, or voiding, increased in size and population. In some cases the voids formed into the crack separating the Ni from the Cu DBC. Also, the Ni-plating that has migrated away from the silicon die, Kirkendall porosity was observed.

### 3.3.2 Tin whiskers

In the lead-free solder alloys tin whiskers were observed (Figure 3.3-9). “Whiskering” is a naturally occurring phenomenon. Whiskers can be defined as a single-crystal growth resembling fine wire that can extend up to 0.64 mm high.<sup>xviii</sup> They are spontaneous and these whiskers can become large enough to short leads and cause equipment malfunction and are, therefore, a reliability concern.<sup>lxii</sup>

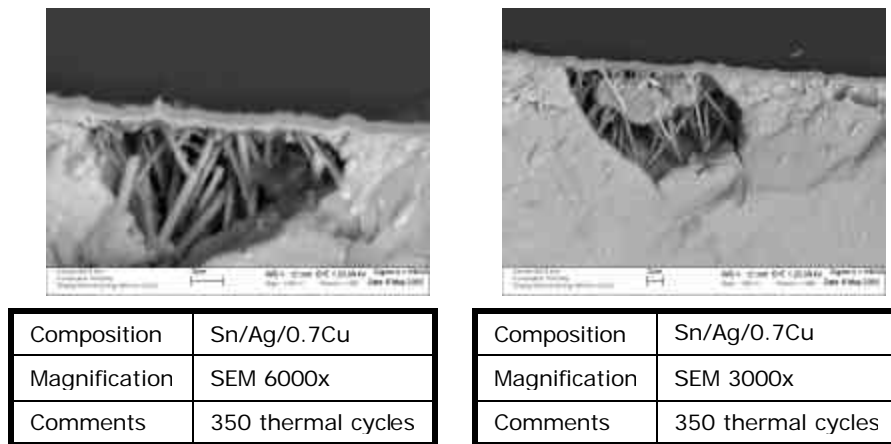
The whiskers are tetragonal b-tin that may grow in response to tinernal stress in the material or external loads.<sup>xviii</sup> Rapid whisker growth in tin occurs at about 51°C and is influenced by plating conditions and substrate property.<sup>xviii</sup> Whiskers do not affect solderability

nor do they cause deterioration of the tin coatings. However, longer whiskers may cause electrical shorts in PC board assemblies. Elements such as lead suppress whisker growth in tin, and virtually no whisker growth is encountered in eutectic tin-lead solder.<sup>xviii</sup>

Tin whiskers are a problem specific to the microelectronics industry. Rockwell Electronics identified three reasons why tin whiskers are a problem:

- 1) Miniaturization of electronics - as devices get smaller and smaller, the potential for catastrophic failure due to shorting as a result of "whiskers" greatly increases.
- 2) Spontaneous growth - there are no known reason for "whiskers" to grow. They've been known to grow in variable environmental conditions including high and low temperature and under vacuum.
- 3) Variable incubation period - there is no known time after which "whiskers" won't grow. They've been known to grow in days and in other cases took as much as 8 - 10 years to occur.<sup>lxiii</sup>

The Tin Whisker Test Method Standardization Project, organized by the National Electronics Manufacturing Initiative (NEMI) is addressing the problem of "tin whiskers" in lead-free assemblies. This project is aimed at understanding the causes of the tin whiskering phenomenon and predicting their occurrences.<sup>lxii</sup>



**Figure 3.3-9: Tin whiskers, which developed in a Sn/3.5Ag solder sample.**

## Conclusion

Tin whiskers were found to have formed in a voided region of Sn/Ag/0.7Cu solder samples. The lead-free solder alloys contain more than 90% Sn and tin whiskering is most associated with high tin content. This phenomenon is not typically seen in the Sn/37Pb solder alloy. Part of the reason that the electronics industry uses Sn/37Pb is the reduction of the potential for tin whiskering.

## 4 Conclusions

The objective of this project was to identify microstructural change in large-area solder joints caused by thermal cycling and relate these changes to reliability issues in large-area lead and lead-free solder constructed semiconductor power devices. This study focused on the microstructural changes within the solder alloy of a large-area solder joint under thermal cycling conditions. Samples were created to simulate the CTE mismatch experienced in power semiconductor devices in application, i.e. tri-layered samples. In addition, samples were made to verify the issue of CTE mismatch by eliminating one of the material components in the samples, i.e. dual-layered samples. These samples were tested either via thermal cycling or isothermal aging to identify reliability issues related to long-term operation or frequent, short-term operation such as a laptop computer. The reliability of a large-area solder joint for this study was determined by the amount of damage generated during the testing. Total failure was identified as severe deep cracking through any part of the solder joint. For an operational device, this would disrupt electrical connections.

There were two primary findings made during this study. First, that the lead-free solder alloys, Sn/3.5Ag and Sn/Ag/0.7Cu, sustained the most damage in the form of cracking. It can be assumed that with enough time all of the samples would have failed. Consequently, during this study the lead-free solder alloys sustained severe damage sooner than the lead solder samples. The Sn/37Pb solder samples showed ductile-type damage, while the lead-free solder samples sustained deep cracking due to accelerated slip band movement during thermal cycling.

The second significant finding was that the damage and cracking found after thermal cycling was most concentrated at the solder/DBC substrate interface in the tri-layered samples. The highest stresses were found to be concentrated in this region regardless of the fact that the highest CTE mismatch between adjacent materials was located at the solder/silicon interface. The geometry of the large-area solder joints, the materials used in construction, and the testing conditions all contributed to the damage accumulation in the samples. For example, the geometry restricted the movement of the solder and adjacent copper layers. The silicon die on the other hand was bounded on only one side, the side adjacent to the solder. Since silicon is known to relax upon heating, this unrestricted layer did not inflict as much stress on the solder layer as predicted by the CTE values.

The majority of the damage was observed at the solder/DBC interfacial region consistently within almost all of the samples. Several other trends were also observed. Severe cracking was only observed in the lead-free solder alloys. When a void was present in the solder layer, the cracks were observed to propagate through, or propagate from, the void. Cracking was

also found to propagate diagonally across the thickness of the solder layer stretching from the silicon to the solder. The damage observed in the Sn/37Pb also followed similar trends. The Sn/37Pb solder alloy is considered a “soft” solder as compared to the lead-free alloys in this study. This can explain the difference in the extent of damage in each solder type. The build up of slip bands and the lower toughness of the lead-free alloys likely lead to crack initiation and propagation.

The cracking occurred in the solder material adjacent to the intermetallic. The intermetallic compounds are stronger materials than the solder. As the sample experiences stresses due to CTE mismatch, the solder layer is designed to be the component in the package, which absorbs most of this stress, sparing the components, i.e. silicon, from damage. The stresses in the solder layers during this study absorbed stress beyond their plastic deformation limits. Therefore, stress relief in the form of slip bands, extrusions and intrusions, grain boundary sliding and cracking occurred as a result.

Simplified calculations and computer simulations were performed to identify the largest change in stress between the different layers of the sample structures. These methods showed that the stresses were highest in the substrate layer. This may be related to the fact that the DBC is a rigid component in the structure. Though the silicon is considered a brittle material there is an elastic zone for silicon within which the material is able to flex. The brittleness is due to the fact that when the strength of the material is reached there will be catastrophic failure hence no plastic deformation. The plastic deformation of the solder material on the other hand is utilized to absorb the majority of the stress in the package. If the solder were too strong and was not able to “give” with the imposed stresses, these stresses would be more distributed through out the sample. That would mean that the silicon die might be required to absorb mechanical energy normally deflected by the solder layer. Hence the solder is designed to take the brunt of the stresses, so the damage observed during this study was expected but the nature of the damage was not known.

The calculations also revealed the compressive and tensile nature of the stresses imposed by the CTE changes in the x-direction. During heating the materials will attempt to expand at different rates. The solder will be under compression, because it would prefer to expand at a faster rate and to a greater extent than the adjacent materials. The same is true but opposite for cooling. The solder layer will be in tension. This can help explain the cracks which were observed at a diagonal across the solder layers. Materials will typically fail at a 45-degree angle to the direction of applied tensile or compressive stresses, in this case the x-direction. In addition, slip bands in the lead-free solder materials were oriented at an angle across the solder layers.

The damage gradient which was observed across the solder layers, specifically the tri-layer samples, was likely a result of a combination of factors. The CTE differences between all of the layers during thermal cycling imposed cyclic tensile and compressive stresses on the solder layer. These stresses or the build up of stress obviously exceeded the yield strength of the solder materials causing plastic deformation. Due to the fact that the silicon is able to elastically deform and the DBC was found to be the most rigid component, the solder layer experienced varying stresses across the thickness. The silicon was able to flex with the changes in thermal expansion. While the SBD, though having a higher CTE value than silicon, was not able to absorb additional stress that the solder was forced to absorb.

In addition to the simplified model, which observed linear elastic strains, assumptions were made that a bending moment may have been produced due to bending in the silicon die and the rigidity of the DBC. This may have caused the solder layer to be pulled in different directions during the cyclic loading promoting crack growth and shear stresses due to tension. Hence, combination of material properties of the layers in the samples and the geometry of the constructed samples were identified as the leading factors in the failure of the solder joints.

## 5 Future Work

The driving forces for the move from lead solders in the electronics industry are due to environmental concerns being addressed by legislation, increasing complexity of electronic devices, and higher demands for reliability in solder joints. With this change, the industry may want to view this as an opportunity to redefine interconnection technologies. The direct replacement of lead solders in electronics is a short-term goal; however, focusing on the redesign of products to utilize the advantages of alternative lead-free interconnects is a more long-term solution, which will advance technology in the future.

This study was performed to observe microstructural changes under thermal cycling conditions of large-area lead and lead-free solder joints. The results from this study have established preliminary data that has verified that damage occurred during thermal cycling in large-area solder joints. This damage is directly related to the reliability of electronics packages and therefore electronic devices. Future work may include repeating these experiments with a greater number of samples and/or including additional solder alloys. By repeating these experiments with a greater number of samples may produce a life prediction for the different solder alloys. In addition, future experiments could provide for separate samples at each data collection set (SEM imaging). This would mean that the samples would not be sectioned prior to testing, eliminating potential surface effects.

Further investigation of the stress gradients across the solder layer would lend to understanding of the failures observed during this study. Currently, little work has been done to experimentally identify localized stresses within the solder joint on a microstructural level. The question has also been raised about how the direction of heat dissipation through the solder joint may affect the microstructure of the solder material.

The existence of voids in solder layers is a reliability issue. Voids represent a discontinuity in conduction of electrons and/or heat. This adversely affects the performance of a packaged device. This study identified that cracks either propagated through or form voids. By identifying crack initiation with solder joints, design issues of the manufacturing of a device or the solder alloy could be modified. Further, the modification of solder alloys by introducing precipitate particles or nano-oxide particles may be able to address cracking issues. Hence by controlling the plastic deformation of solder alloys, reliability and life times may be more predictable. In addition, the interface between the intermetallic formed upon reflow may be addressed by solder modifications. By controlling processing, a gradient of material across the solder thickness could eliminate the cracking that was observed in this study.

Further modeling integrated with stress and strain evaluations would expand the knowledge of solder joint reliability. These evaluations may be explored using techniques such as distributed sensors or grid mapping to evaluate the stresses and strains within each area of the device. For instance a grid could be attached or printed onto the polished surface of a sectioned device. Using a camera the grid could be imaged before and then after thermal cycling for comparison. Further, a video or IR camera could be used to image changes in real time. This method could also be accomplished by attaching an array of sensors such as optical sensors along the sample using an epoxy. However, the sensors may be less precise because of physical limitations. The grid would be able to measure on a smaller scale.

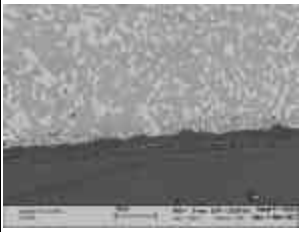
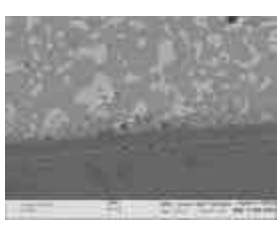
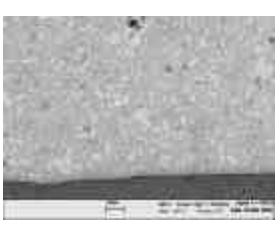
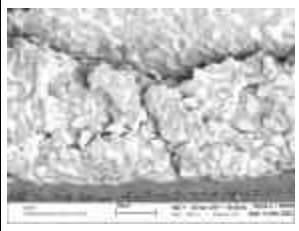
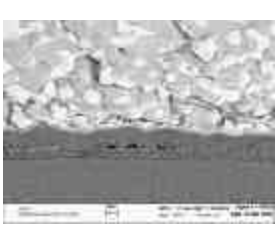
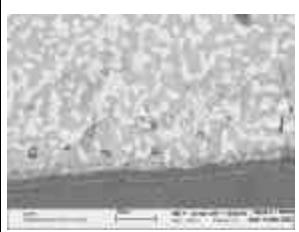
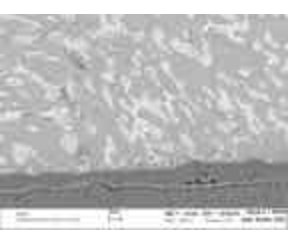
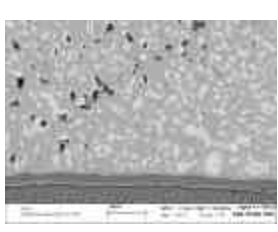
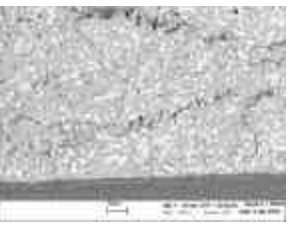

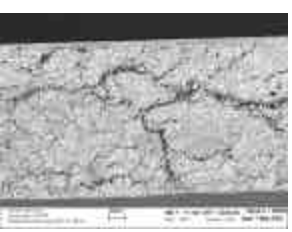
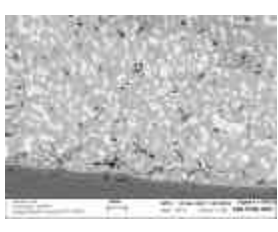
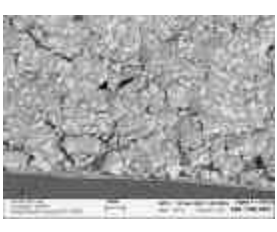
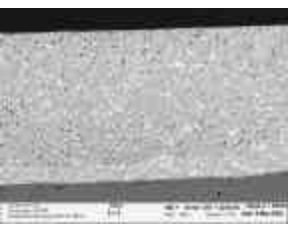
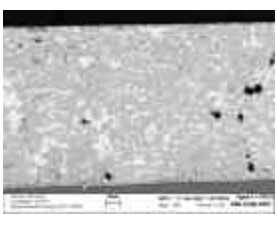
Several interesting discoveries were made during this study such as Kirkendall porosity and tin whiskering could potential be studied as reliability issues. The Kirkendall porosity observed during this study was found in some cases to cause cracking between the Ni-plating and the Cu substrate. The tin whiskering has been identified within the electronics industry as a reliability issue, due to the potential for the whiskers to short components. NIST has recently begun a study of tin whiskers because of the move to higher tin-based solders as replacements for leaded solders and lead coatings. Hence the short-term problems in the replacement of leaded solders may give rise to the opportunity for re-examining the functional requirements of commonplace interconnect technology and open the way for new innovative alternatives. Alternative technologies are currently being explored in related fields such as in MEM.



## 6 Appendix

### 6.1 Appendix A: Charts

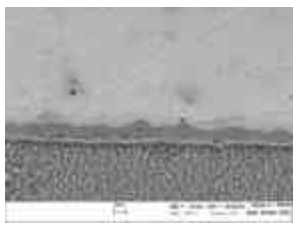
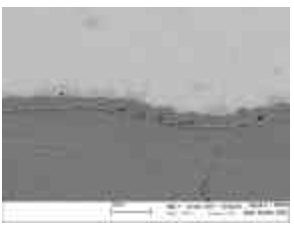
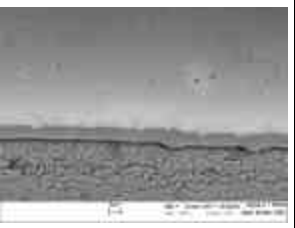

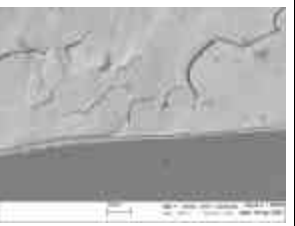
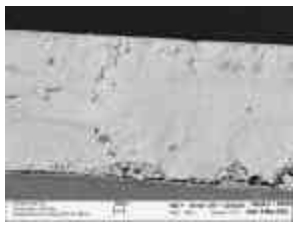
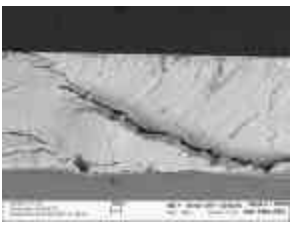
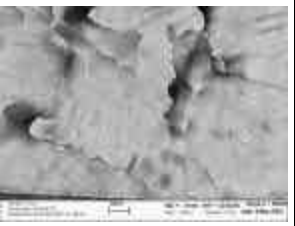

Table 6.1-1: Thermally cycled Sn/37Pb samples.

	A07 mid	A07 end	A mid	10313 end
0 cycles				
60 cycles				
60 cycles (Re)				
120 cycles				
350 cycles				
350 cycles (Re)				

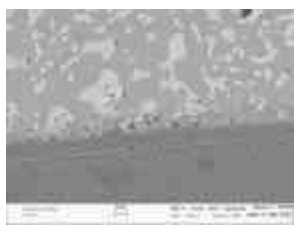
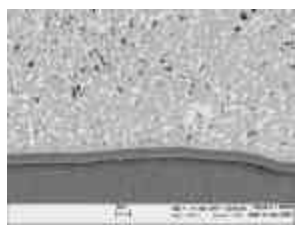
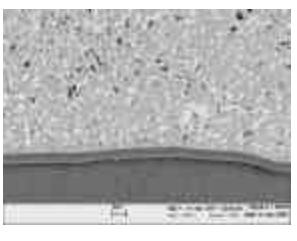
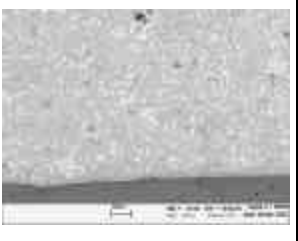

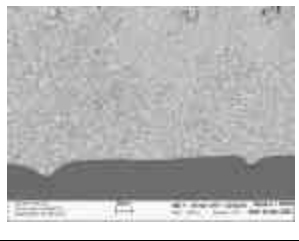
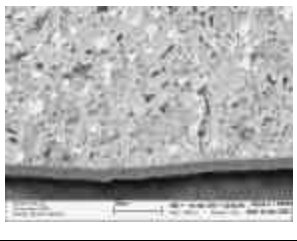
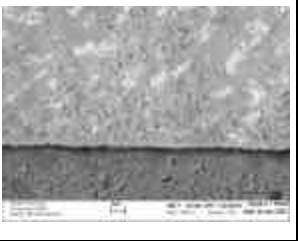
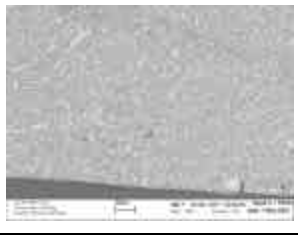
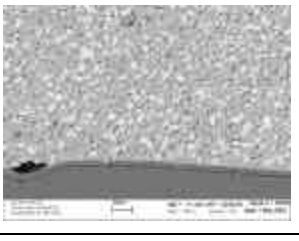
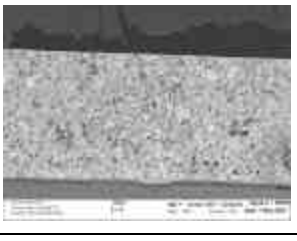
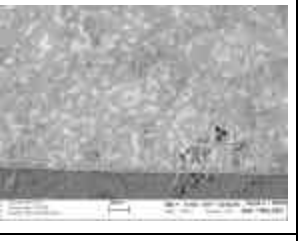
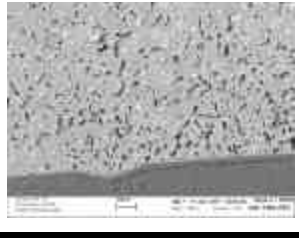
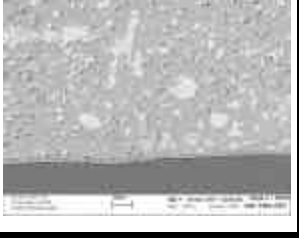
**Table 6.1-2: Thermally cycled Sn/3.5Ag solder samples.**

	B08 end	B08 mid	B end	50313 end
0 cycles				
60 cycles				
60 cycles (Re)				
120 cycles				
120 cycles (Re)				
350 cycles				
350 cycles (Re)				


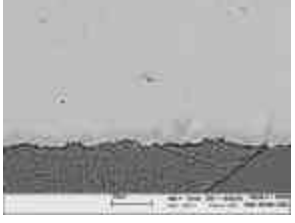
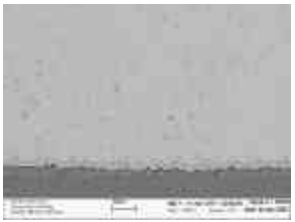
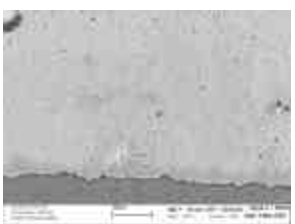
**Table 6.1-3: Thermally cycled Sn/Ag/0.7Cu solder samples.**

	C17 end	C17 mid	C end
0 cycles			
60 cycles			
290 cycles			
290 cycles (Re)			

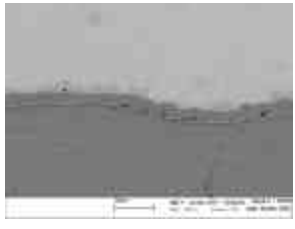
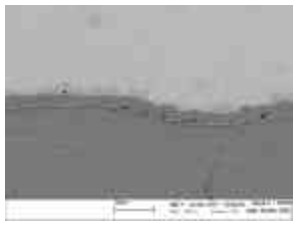
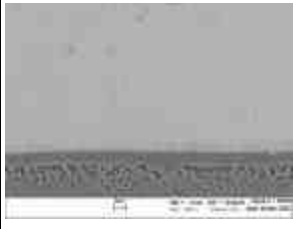
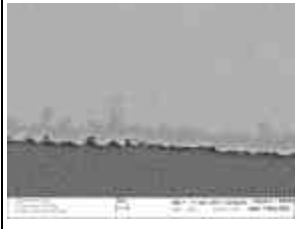
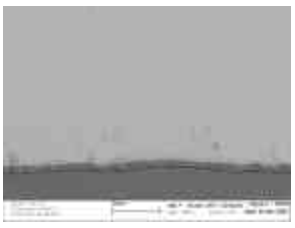
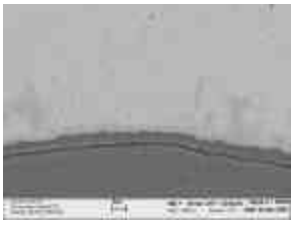
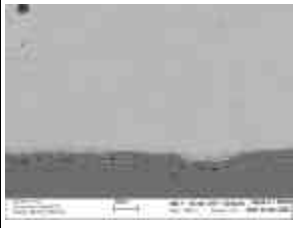
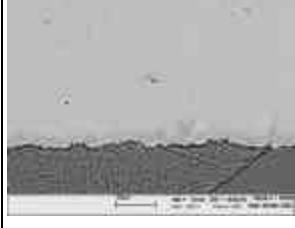
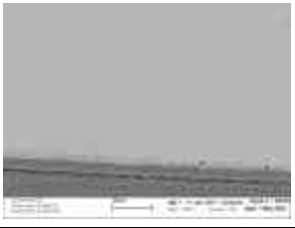
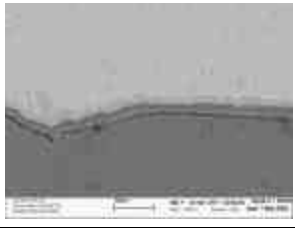
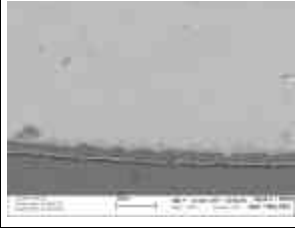
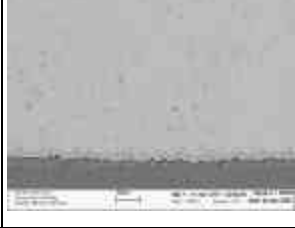
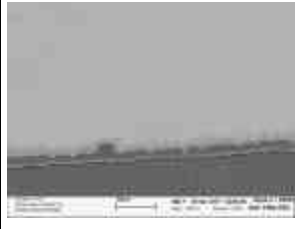
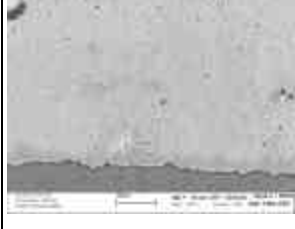
**Table 6.1-4: Isothermally aged Sn/37Pb solder samples.**

	AI end	A20I mid	A20I end	10313 mid
0 cycles				
Temp	60°C	100°C	125°C	100°C
100 hours				
250 hours				
250 hours (Re)				

**Table 6.1-5: Isothermally aged Sn/3.5Ag solder sample.**

	50313 mid
0 cycles	
Temp	100°C
100 hours	
250 hours	
250 hours (Re)	

**Table 6.1-6: Isothermally aged Sn/Ag/0.7Cu solder samples.**

	C20I end	C20I mid	CI mid	50313 mid
0 cycles				
Temp	60°C	100°C	125°C	100°C
100 hours				
250 hours				
250 hours (Re)				

## 6.2 Appendix B: Failure Analysis

### Introduction:

During the progress of this research time was taken to do a failure analysis on the devices that were built for the study. A paper was presented at the 2002 CPES Seminar on this subject entitled, “A Failure Analysis Study of Semiconductor Power Device Construction.” The results indicated that there were material selection issues with the construction of the devices. This section will discuss the failure analysis approach taken, the techniques used for the analysis, and the results from this study.

The original reliability project that prompted the failure analysis study is entitled, “A Comparative Physics of Failure Study of Lead and Lead-free Solder Alloys for Large Area Bonding in IPEMS.” This study is being conducted in the CPES Packaging Lab here at Virginia Tech and supported by the ERC Program of the National Science Foundation, Award Number EEC-9731677.

The overall objective of the reliability study to understand the microstructural changes affecting the reliability of the die attach solder layer of an IPEM under power cycling conditions, comparing different lead-free solder alloys. This project combines the results of a microstructural evolution study with the work being done by Dimos Katsis on the same samples to characterize the reliability of large-area die attach solder layers within IPEM’s. The devices that were originally constructed for this study were intended for reliability testing and a microstructural study under power cycling conditions. This experiment was patterned after a reliability study conducted on commercially developed power semiconductor packages.<sup>lxiv</sup> However, failures occurred in the packaged devices delaying the reliability study. A failure analysis of a power semiconductor device package was consequently conducted to identify the root cause of the failures.

### Overview of the Reliability Study:

Power semiconductor devices in applications that require extreme environments and reliability requirements, such as in the automotive and avionics industries motivated the reliability testing. Table 6.2-1 describes the requirement profile of microelectronics over various industries. Many of these requirements come down to processing, material selection, and testing issues.

**Table 6.2-1: Requirement Profiles for Various MicroTechnologies.**<sup>1xv</sup>

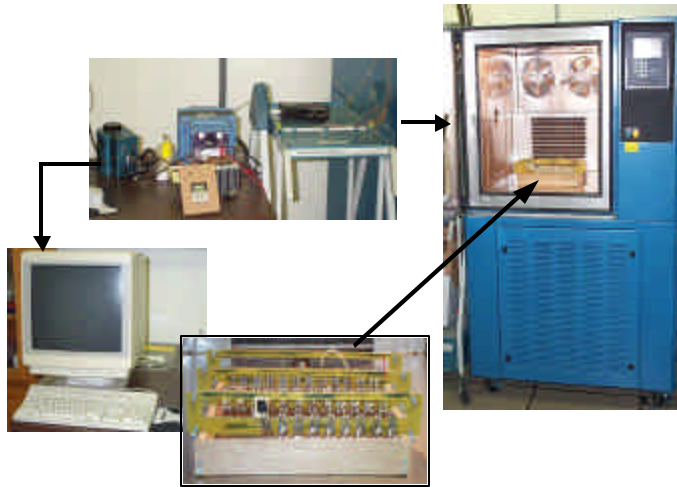
<b>Application</b>	<b>Automotive</b>	<b>Military/ Avionics</b>	<b>Consumer/ PC</b>
Computation Power	Low to Medium	High	Medium to High
Costs	Low	Typically High	Low to Medium
Environment	Harsh to Severe	Harsh to Severe	Moderate
Reliability Requirements	Stringent	Stringent	Moderate

In order to meet the goals of the reliability project, modules were built in the CPES Packaging Lab using various lead and lead-free solders. These packaged devices were intended for power cycling testing from -50C to 100C. During which periodic inspections of the device's functionality (electrical, thermal impedance performance and SAM observations) and material characteristics of the solder (microstructural observations using SEM and optical microscopy) would be taken. Preliminary electrical, thermal impedance, SAM and SEM data was taken and the goal was to power cycle these devices.

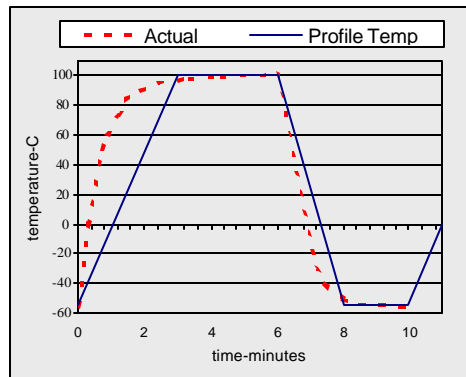
**Testing Methods:**

These devices were then subjected to a power cycle procedure that used a DC current to heat the series-connected MOSFETs to 100°C by forward biasing their integral body diodes. The devices were contained in a temperature chamber, which was maintained at -55°C. The DC current passing through the MOSFET diode heated each package to a steady state temperature of 100°C. Simple radiation and convection from the air circulation in the temperature chamber then cooled the devices when the DC current was turned off. The temperature of the samples was monitored by five thermocouples placed on random devices. Figure 6.2-1 illustrates the power cycle set up. The devices were connected in series in a fixture created for use during testing and for SAM analysis. A time controller managed the power cycles. The cycles were profiled by measuring the time to reach the maximum temperature and then reverse and reach the minimum temperature. Hence, the current would be turned on once the minimum temperature had been reached and would be turned off at the maximum temperature. This process was characterized to identify the accuracy of the cycles to that predicted (Figure 6.2-2).





**Figure 6.2-1: Power cycle set up.**



**Figure 6.2-2: Power Cycle Profile for 100° C to -50°.**

#### Results of Initial Testing:

The now constructed devices were subjected to initial testing and thermal cycle profiling prior to long-term testing under power cycling conditions. Electrical testing of the device was to check the functionality of the device. The samples were then thermal impedance tested as a measure of the device's performance, which would be compared to later measurements after testing. Finally, the devices were placed in the temperature chamber and connected to the current source in order to determine a profile for the cycling schedule. Essentially, the times between current on and off were determined.

After the first five power cycles after profiling, many of the first generation devices failed open. The loss of continuity interrupted the power cycling test until the failed devices were removed. Of the original 50 samples 28 were lost: 5 were lost during wire bonding, 14 were lost during initial thermal impedance testing, and 14 were lost during power cycle profiling (Table 6.2-2). Hence, the first generation modules were not tested under power cycling conditions.

A second-generation set of modules was constructed using similar materials and techniques. Again failures occurred. In response to the failures of the Gen. I and Gen. II devices, a failure analysis study was conducted.

**Table 6.2-2: Summary of failures in Gen. I CPES constructed power devices.**

Group	Number Made	Failed Initial Electrical Tests	Failed Thermal Impedance	Failed Power Cycling
A (Sn/37Pb)	16	2	5	4
B (Sn/3.5Ag)	17	3	4	2
C (Sn/Ag/0.7Cu)	16	2	4	2
D (Sn/5Sb)	12	2	3	2
Total	61	9	16	10

#### Failure Analysis Approach:

The application of electronics is dependent on the reliability of the electronics packages. Electronics packages are required to provide interconnection capabilities as well as protection to environmental extremes such as temperature, vibration and moisture. Materials for the construction of electronics packages are chosen for their specific electrical, thermal, and mechanical properties. The failure analysis of electronics packages must consider all of these aspects. This failure analysis study was motivated by the desire for CPES to understand device construction processes.

Failure analysis techniques involve a methodology of process steps, which build on information obtained from previous steps. Generally, the methodology begins with non-destructive techniques and then proceeds to the more destructive techniques, allowing the gathering of unique data from each technique throughout the process.<sup>lxvi</sup>

The failure analysis approach began by identifying four areas and investigated with the techniques listed in Table 6.2-3.

**Table 6.2-3: Failure Analysis Study Methodology.**

<u>Failure Analysis Approach</u>	<u>Failure Analysis Techniques</u>
• Failure Modes	1. External Visual Inspection
• Failure Site(s)	2. Electrical Tests
• Failure Mechanism(s)	3. Non-destructive Evaluation
• Root Cause	4. Destructive Evaluation

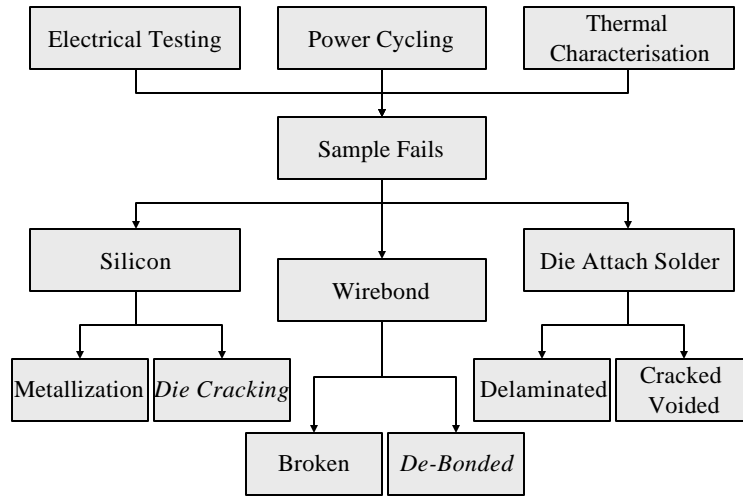
The analysis procedure begins with an external visual examination to observe any signs of obvious mechanical damage.<sup>lxvii</sup> The failure is then confirmed with electrical tests, which may be conducted over a range of temperatures. Once the unique data using non-destructive evaluations are obtained, destructive techniques can be used.

#### Failure Modes

Failure modes identify the way a device has failed. A flow chart was created (Figure 6.2-3) to indicate failure modes found during this investigation of the CPES devices. In this case there were three actions upon the devices, which revealed (and possibly caused) a device to fail: electrical testing, power cycling, and thermal characterization. It was determined that the failure was most likely in one of three areas in the device, the silicon chip, the wirebonds or the solder joint. Of these areas there were characteristic failures that typically occur. For example, the most common failures that may occur in wirebonds are breakage along the wire or the wire is no longer bonded to the device or the substrate. It was determined through further inspection that the failures were mostly found to be wirebond de-bonding from the substrate and die cracking.

The initial visual inspections did not reveal mechanical failures such as cracks or melting of any of the exterior materials. A diode continuity test was performed to find open devices. The remaining devices were then tested electrically at different temperatures. It was discovered that at low temperatures,  $\sim -50^{\circ}\text{C}$ , some devices showed an open circuit. Once they returned to room temperature most devices regained continuity. The devices that did not regain continuity were again operational when pressure was applied to the top of the encapsulant. These failures indicated that the wire bonds were not in contact with either the substrate or the semiconductor die. Hence, it was determined that the devices should be destructively tested for further investigation. The non-destructive analysis technique, Scanning Acoustic Microscopy (SAM) would not have enough resolution to identify potential failures so destructive evaluation was

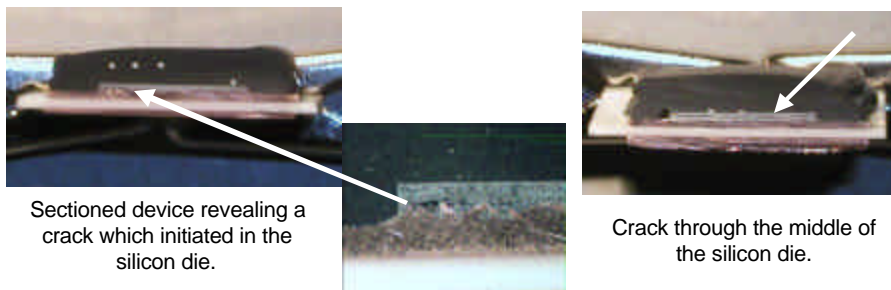
performed. The destructive evaluation consisted of microsectioning and chemically de-encapsulating a number of devices.



**Figure 6.2-3: Flow chart indicating potential failure paths. The features discovered during this study are indicated in italics.**

### Failure Site

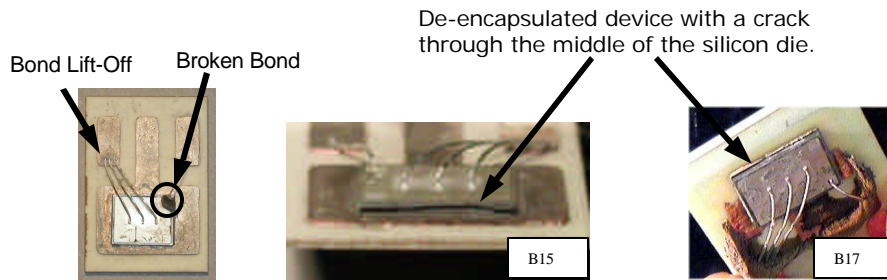
The failure site indicates where a failure has occurred. The devices were first sectioned using a diamond saw to reveal any possible damage. Cracks were found through the silicon dies as seen in Figure 6.2-4.



**Figure 6.2-4: Sectioned devices**

The devices were then de-encapsulated. Several techniques were used to determine the best method for de-encapsulation. The de-encapsulation confirmed that there was die cracking (Figure 6.2-5). This technique also revealed that the wire bonds had be-bonded from the Ni-

plated DBC surface. However the wires were firmly bonded to the top of the silicon die, indicating that the wirebond failure must have occurred at the DCB substrate surface.



**Figure 6.2-5: De-encapsulated Devices**

### Failure Mechanisms

The failure mechanism(s) identify the physical phenomena involved in the failure. Therefore, our attention turned to the materials used for the construction of these devices. The CTE of the various materials used in the construction of the devices were noted. Table contains the CTE information provided by the manufactures and segregate data of the materials used in the construction of the devices. It was narrowed to the epoxy encapsulant being suspect. The larger expansion of the epoxy material could have created elevated stresses on the silicon dies and the wirebonds. Consequently, the epoxy was directly in contact with the identified failure sites. The difference in CTE of the encapsulating material, at 20 ppm/°C and the CTE of the silicon die, at 3 ppm/°C could indicate a failure mode. The larger expansion of the epoxy material would create elevated stresses along the surface and the sides of the silicon device.

**Table 6.2-4: List of materials and properties used in the construction of the power semiconductor devices.**

<u>Material</u>	<u>Physical Property: CTE</u>	<u>Source</u>
Alumina DBC	8.1 ppm/°C (50°C to 200°C)	IXYS**
Epoxy Encapsulant	20 ppm/°C (25°C to 100°C) 72 ppm/°C (160°C to 240°C)	Loctite: 3532 dam. 3534 fill*
Aluminum	24ppm/°C @ 20°C	Pure Alumin um***
Solder (general)	~30 ppm/°C	Kester
Silicon	3ppm/°C	IXYS**

\* Loctite Sata Sheet. Product 3532 and Product 3534. Electronics Products, October 1998.

\*\* IXYS Corporation Data Sheet. Product: Direct-Copper-Bonded (DBC) Substrate. 2000. pp. J-23 – J-24

\*\*\* MATWEB. The Online Materials Information Resource. [www.matweb.com/SpecificMaterial.asp?bassnum=MEA100](http://www.matweb.com/SpecificMaterial.asp?bassnum=MEA100)

## Background

The coefficient of thermal expansion (CTE) is a materials issue of great concern for electronics packages because of the composite-type structure inherent in these devices. The reliability study for which these devices built were going to be tested under stress conditions from temperature cycling. One of the major proponents would have been the CTE mismatch between the different materials. The hope was to cause failure in the solder layer. However, we have discovered that the CTE mismatch may have been too good. This was an opportunity for us to connect materials issues to bigger issues within the construction of power devices. The CTE is a material property that indicates the extent to which a material expands upon heating<sup>xxviii</sup>:

$$\frac{\Delta l}{l_o} = \alpha_l \Delta T \quad \text{and} \quad \frac{\Delta V}{V_o} = \alpha_v \Delta T \quad \text{Eq. 1}$$

where  $\alpha_l$  = linear coefficient of thermal expansion

$\alpha_v$  = volume coefficient of thermal expansion

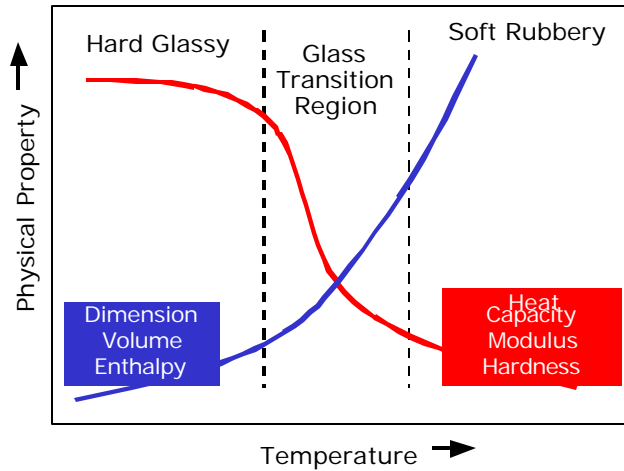
$\Delta T$  = temperature change

$\Delta l$  and  $l_o$  = original and change in length

$\Delta V$  and  $V_o$  = original and change in volume

## Material Properties

The epoxy encapsulant was first suspect. This was because the devices were tested once they had returned from being wire bonded. It was not until after encapsulation and testing began that the failures appeared. Studying the chemistry of epoxy material it was found that stress related failures in electronics packages due to changes that occur in the encapsulant's mechanical properties or viscoelastic properties can be seen during thermal cycling. Consequently, below -20°C, the traditional chemistry for epoxy materials cause an increase in modulus, becoming subsequently more rigid or increase in modulus.<sup>lxviii</sup> Also, the hardness of these materials can increase when exposed to temperatures above the glass transition temperature,  $T_g$ , (~130°C on average) for any length of time. This hardening is due to the additional crosslinking within the epoxy material. Additionally, at temperatures below the  $T_g$  the modulus of the material can increase where the material may become more rigid, i.e. the hardness of the material may increase. This change in material properties above and below the  $T_g$  is illustrated in figure. Above the  $T_g$ , these materials change volume and dimension due to CTE effects. Likewise below the  $T_g$  the material's modulus increases along with it's hardness.



**Figure 6.2-6: General property changes in encapsulants.**<sup>lxix</sup>

The combination of limiting  $T_g$  ( $139^\circ\text{C}$ ), very high modulus below the  $T_g$  (6.07 GPa at  $25^\circ\text{C}$ ) and thermal age hardening of the epoxy encapsulant materials causes a dramatic increase in stress on electronic components. The change in material properties with different conditions such as temperature is also common in many of the other materials in an electronic package, as seen in Table 6.2-5. For instance, the modulus,  $E$ , of alumina and Silicon will remain constant while the CTE may change with temperature unlike for solders. Again, materials such as the epoxy used can have drastically different material properties at different temperatures (Table 6.2-4). It was found that the CTE of the epoxy could drastically change from  $20 \text{ ppm}/^\circ\text{C}$  between  $25^\circ\text{C}$  and  $100^\circ\text{C}$  to  $72 \text{ ppm}/^\circ\text{C}$  above  $160^\circ\text{C}$  or above the  $T_g$ .

**Table 6.2-5: Material properties related to electronics packaging.**<sup>lxx</sup>

Material	Temp. ( $^\circ\text{C}$ )	Modulus (GPa)	CTE ( $10^{-6}/\text{K}$ )
Sn/37Pb	-70	38.1	24.0
	20	30.2	24.0
	140	19.7	24.0
Alumina	-55	303	3.9
	22	303	4.5
	100	303	6.7
Silicon Chip	-73	162	1.40
	27	162	2.62
	127	162	3.23

#### Root Cause

The root cause in a failure analysis determines the design, defect, or loads, which led to the failure. The stresses imposed on the silicon die in the CPES packaged devices were evident after microsectioning. Cracks found in the silicon indicate that there were high stresses,

exceeding the strength of the silicon due to the surrounding package. The shear stress imposed on the die is dependent on the stress magnitude, which takes into account the testing conditions ( $\Delta T$ ), the CTE mismatch between the two materials and the elastic modulus of the material in question.

$$s_o = E\alpha_1(T_o - T_f) \quad \text{Eq. 2}$$

where  $\sigma_o$  = stress magnitude, E = modulus of elasticity,  
 $\alpha_1$  = coefficient of thermal expansion, and  $T_o$  and  $T_f$  = initial and final temperatures.

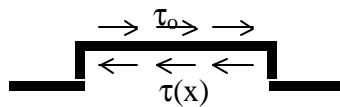
### Background

Huang, et. al investigated the failure of layered materials such as silicon dies due to failure under thermal cycling conditions, where cracking in a brittle layer is caused by ratcheting in adjacent ductile layers.<sup>lxxi</sup> For instance, for a structure composed of an organic substrate, such as an epoxy encapsulant, directly attached to a silicon die, cracking often occurs.<sup>xii</sup> This is due to the CTE mismatch between the layered silicon die and the epoxy.

Huang et. al found that after temperature cycling, the aluminum pad on the surface of the layered silicon die no longer supported the shear stresses,  $\tau_o$ , imposed on the film by exterior stresses as shown in **Figure 6.2-7**. Therefore, the  $\tau_o$  was fully sustained by the silicon. Consequently the stress magnitude,  $\sigma_o$ , in the silicon could build up to high levels, which may cause cracking due to thermal cycling.<sup>lxxi</sup> In addition, the strain also increases with increasing semiconductor die size.<sup>xii, lxxii</sup> However, above a certain die size, this trend reverses and the strains do not increase.<sup>lxxiii</sup>

$$s_o = \frac{t_o L}{2t} \quad \text{Eq. 3}$$

where t = thickness of the SiN film, and  
L = length of the aluminum pad.



**Figure 6.2-7: Free body diagram of shear stresses imposed on the surface of a silicon die.**



## Results

During the de-encapsulation process, several chemicals were tried to remove the epoxy. One of the chemicals did not dissolve the epoxy, however, the encapsulant released from the substrate and the cracked silicon die broke away. Figure 6.2-8 shows the de-encapsulated devices and the detached encapsulant. The arrow labeled 'A' indicates the encapsulant that released from the substrate. The arrow labeled 'B' indicates the piece of the silicon die that stayed attached to the encapsulant. This also occurred during microsectioning.



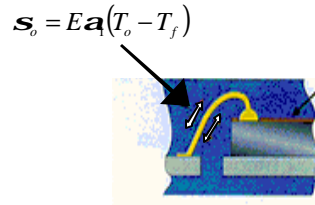
**Figure 6.2-8: De-encapsulated devices using various chemicals.**

The epoxy encapsulant was directly in contact with the silicon die and the aluminum wirebonds. This direct contact emphasized the CTE mismatch between the silicon, the wirebonds, and the epoxy; due to the fact that the epoxy did not bond as well to the substrate as to the silicon die surface. This meant that the silicon die received most of the stress caused by the CTE mismatch; therefore, cracking and/or wirebond lift-off.

## Summary of Evidence

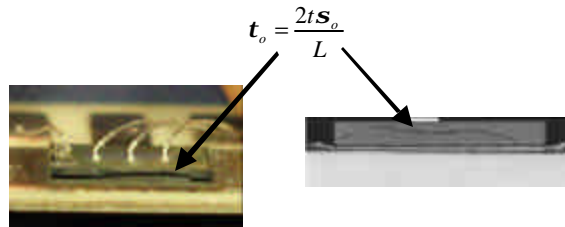
The evidence collected during this failure analysis investigation indicated that material properties might have been the underlying issue. The wire bonds were found to have lifted off the Ni-plated DBC surface. In addition a few were found to have broken. Cracks were found within the thickness of the silicon dies. This was an indication that there were large stresses imposed on the dies. Because the encapsulant showed good adhesion to the surface of the dies as compared to the DBC substrate, it was concluded that the Si die was carrying the bulk of the stress load.

Wirebond lift-off was considered one of the two potential failure modes. The CTE mismatch between the aluminum wire bonds and the encapsulant may have caused excessive shear forces leading to wire bond liftoff from the nickel-plated substrate surface (Figure 6.2-9). This was most likely the cause for the open circuits observed during continuity testing. Once pressure was applied to the top surface of the encapsulant, the contact was re-established. This failure mode was likely related to material selection issues, DBC surface metallization and/or epoxy encapsulant. Another issue may have been the cleaning methods used on the DBC surfaces prior to wire bonding.



**Figure 6.2-9: The CTE of the encapsulant is normally matched to the wirebonds to reduce thermal stresses.**<sup>lx</sup>

Die cracking was considered the other failure mode. This occurrence can be found throughout literature for a number of different reasons, not the least of which is during thermal cycling. The image on the right in Figure is from an automotive application. This cracking was attributed to thermal cycling stresses. The image to the left in Figure is a device from this study, which was de-encapsulated.



**Figure 6.2-10: (Left) De-encapsulated CPES constructed device; (Right) Silicon die of a power semiconductor with Cu heat sink cracked due to thermomechanical stresses.**<sup>lxv</sup>

It has also been discussed that as the die size is increased, there is a greater potential for cracking. It is well known among power semiconductor manufacturers that the larger the surface mounted power semiconductor is, the more vulnerable it is to die stresses during manufacture and during the surface mounting process. The dies used in this application would be considered large dies; hence, there was a greater potential for die cracking.

Die cracking can also occur during processing (ramp rates during reflow processes) and during thermal cycling due again to ramp rates. Thermal shock can occur within these materials if the material is not allowed to adjust to the temperature changes. Finally, any edge cracks in the silicon or defects are initiation points and typical thermal cycling can propagate cracks. During processing the temperature ramps could have imposed thermal shock on the dies. In addition, the size of the dies is considered to be large and could have contributed to the potential for cracking to occur. However, no significant failures were detected prior to thermal cycling, indicating that the construction of the devices, up to encapsulation, is not the first suspect.

During temperature cycling, again there could have been ramp rates that imposed thermal shock conditions on the Si-dies. However, power cycling was also conducted on industry-

constructed devices. Those devices have now survived over 10,000 cycles. This indicates that there was another problem with the construction of the CPES devices.

Finally, the de-encapsulation process required that the devices soak in a chemical, which was held at approximately 110 C for several hours. The devices were periodically rinsed with DI water and alcohol. There may have been a thermal shock issue if the process was not done with care. However, the sectioned devices also revealed die cracking, which indicates that the cracking occurred somewhere between device encapsulation and the destructive investigations.

## Conclusions

Wirebond liftoff was therefore considered one of the two potential failure modes. This was likely related to material selection issues, DBC surface metallization and/or epoxy encapsulant. The other failure mode was silicon die cracking. This was found during microsectioning and de-encapsulation, revealing that the silicon die suffered damage. Though the root cause was determined to be the epoxy encapsulant chosen for this application. Hence, material selections should take into account the primary requirements in using rigid encapsulants: first, match the CTE of the encapsulant to the wirebond and second, minimize shear stress on the silicon die.

This study revealed materials issues related to packaging construction. Many packages are required to withstand extreme environments and mechanical stresses during use. Hence, material selection is essential in package reliability. Our first attempts at reliability testing exposed many materials and packaging issues. Therefore, our study of the reliability of an electronics package through failure analysis methodologies identified best practices for future device construction.

In order to identify best practices for future projects there are three important aspects for success in packaging:

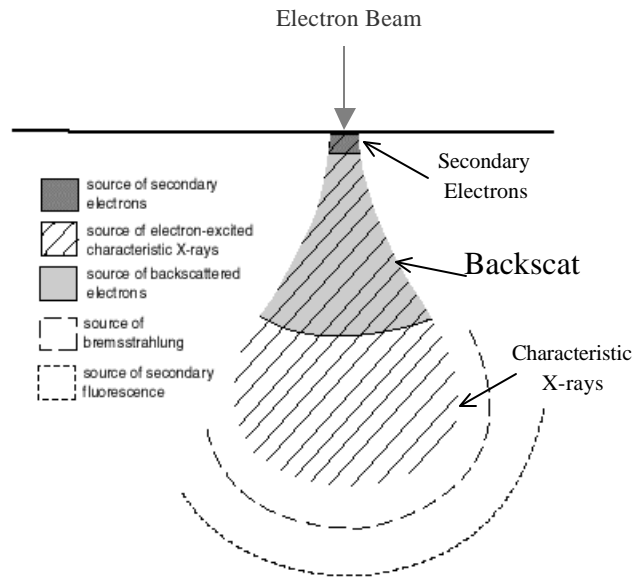
- Process Control
- Material Selection
- Identify Appropriate Testing Conditions

Another set of 6 devices has been created for thermal cycle testing using a silicon gel type encapsulant. Future results from these new devices may confirm the findings in this failure analysis study. As of April 26, 2002, these new devices have survived 2000 power cycles, indicating more conclusively that the encapsulant was the culprit in this failure analysis study.

## 6.3 Appendix C: Electron Beam Analysis Techniques

### Introduction

There are many types of signals produced when an electron beam impinges on the surface of a specimen including secondary electrons, backscattered electrons, Auger electrons, characteristic x-rays, and photons of various energies (Figure 6.3-1). These emissions can be used to examine many characteristics of a material such as composition, surface topography, and crystallography.<sup>lxxiv</sup>



**Figure 6.3-1: Effect produced by electron bombardment of a material.**<sup>lxxv</sup>

Elastic scattering of primary electrons from the generated electron beam results in the production of backscattered electrons (BSE). These are electrons, which have entered the sample, struck the positive nucleus of an atom, and were forced to change momentum. Potentially detectable backscattered are high-energy electrons, which escape the specimen as a result of multiple elastic scattering by achieving an optimum scattering angle.

Inelastic scattering means that kinetic energy is lost from the impinging electron, resulting in several processes including phonon excitation, plasmon excitation, secondary electron excitation, continuum X-ray generation, and ionization of inner shells.<sup>lxxiv</sup> Secondary electrons are produced as a result of the primary electron beam interacting with weakly bonded conduction-band electrons within the specimen, i.e. the beam electrons transfer kinetic energy to the specimen electrons. These are low energy emissions as compared with backscattered

electrons and are only emitted from the surface.<sup>lxxvii</sup> Secondary electrons are commonly used for SEM imaging techniques.

Characteristic x-rays are emissions of electromagnetic radiation from the specimen. Primary beam electrons interact with specimen atoms, ionizing an inner electron shell by releasing an electron.<sup>lxxvii</sup> An outer electron will shift to fill the inner shell, producing radiation that is characteristic of the atom's electron shells' energy level. There are two common techniques for analyzing characteristic x-ray emissions for compositional analysis, energy-dispersive spectroscopy (EDS) and wavelength-dispersive spectroscopy (WDS).

### Technique Descriptions

In the scanning electron microscope (SEM), the signals of greatest interest are the secondary and backscatter electrons. These signals are used as imaging tools revealing the differences in surface topography and elemental differences as the electron beam sweeps across the surface. Hence, for each point that the electron beam hits on the specimen, the portion of the backscattered and secondary electrons generated will give direct information on the surface of the sample. The secondary electron emissions are confined to the volume near the beam's impact area, permitting images to be obtained at relatively high resolution, 2-5 nm.<sup>lxxiv</sup> In addition, the three-dimensional appearance of SEM images is a result of the large depth-of-field and shadow-relief the secondary and backscatter electron contrasts create. The backscattered electron emissions penetrate deeper into the surface of the sample to approximately 100 nm.<sup>lxxvi</sup> These high-energy emissions are a function of the specimen's atomic number; so the higher the atomic number, the brighter the image.<sup>lxxvii</sup> The SEM is one the most versatile instruments for examining and analyzing the microstructural characteristics of solid objects.

The electron microprobe is an instrument used for quantitative, non-destructive chemical analysis of solid materials utilizing the capabilities of SEM imaging, WDS and EDS analysis. In the electron microprobe, or the electron probe micro analyzer (EPMA), the characteristic x-ray is of primary interest. The characteristic x-rays are emitted as a result of the electron beam bombardment on the surface of the specimen. These emissions are used for qualitative identification and quantitative composition with a spatial resolution on the order of 1 μm.<sup>lxxiv</sup> One of the features of EPMA is the capability of obtaining compositional mapping with the characteristic x-rays. The x-ray maps show the distribution of different elements across the area of interest. The benefit of this analysis tool is the ability of correlating the micro-compositional information with light-optical and electron metallography.<sup>lxxiv</sup>

An energy-dispersive spectrometer (EDS), or a lithium-drifted silicon Si(Li) solid-state x-ray detector, is a commonly used tool for x-ray analysis.<sup>lxxiv</sup> The detected x-rays are the x-rays generated from inelastic scattering. The basic detection process is the conversion of photon energy into an electrical signal (Figure 6.3-2). The Si(Li) crystal is an intrinsic semiconductor and a good radiation detector. It will not conduct current in an applied electric field unless it absorbs energy causing electrons to be promoted into the conduction band, leaving holes behind. When the x-ray photons generated from the specimen strike the Si(Li) crystal, a current is produced. The characteristic x-rays generated from the elements in the specimen have a unique energy, which in turn produces a unique current used to identify the element.<sup>lxxiv</sup>

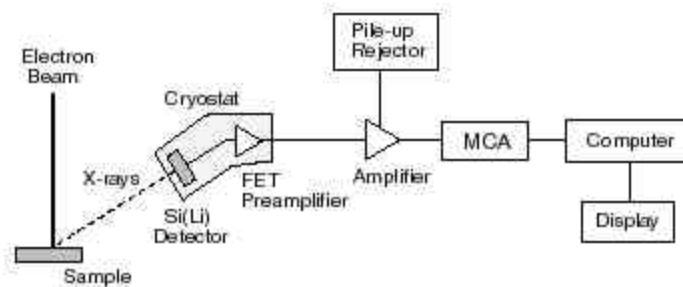


Figure 6.3-2: Schematic of an EDS system (bottom).<sup>lxxiv</sup>

The wavelength dispersive spectrometer (WDS) is mostly used for x-ray spectral characterization. Each element generates a unique x-ray, which are isolated for quantitative measurement. In order for the spectrometer to precisely distinguish the x-rays of interest it is focused, or calibrated, to the element of interest. As with a radio tuner, the spectrometers in a wavelength-dispersive detector need to be tuned to the wavelength of the element of interest's characteristic x-ray.<sup>lxxvii</sup> The impinging x-rays from the specimen are then selectively filtered due to their characteristic wavelengths. X-rays that successfully scatter, i.e. have the appropriate wavelength for the given d-spacing and angle of the analyzing crystal, will be detected. Relative compositional amounts are then determined by the intensity, or count, of the x-rays detected.

A small portion of the x-ray signal generated from the specimen as a result of inelastic scattering strikes the analyzing crystal, or a standard (Figure 6.3-3). This crystal consists of a regular array of atom and is oriented in such a way that a selected crystallographic plane of these atoms is parallel to its surface. The spectrometer is a high precision mechanical system that positions the analyzing crystal at a critical Bragg angle with the specimen and between the detector and the analyzing crystal.<sup>lxxiv</sup> Using Bragg's Law, there is a particular d-spacing,  $d$ , and wavelength,  $\lambda$ , there exists an angle,  $\theta$ , at which the x-rays are most favorably scattered.<sup>lxxiv</sup>

$$n\lambda = 2d \sin \theta$$

where  $\lambda$  = x-ray wavelength

$d$  = interplanar spacing of the crystal

$\theta$  = angle of incidence of the x-ray beam on the crystal

A WDS system, has a depth resolution of approximately 1  $\mu$ m and can potentially detect elements with atomic numbers greater than or equal to 5 (Boron). Analysis crystals used in x-ray microanalysis typically have smaller d-spacings, which cannot detect elements lighter than Fluorine. A quantitative analysis is successful for atomic numbers greater than or equal to 11 (sodium).<sup>lxxix</sup> Hence, the x-ray photons of interest in x-ray microanalysis will generally be in the energy range from 0.185 keV (Boron K) to about 15 keV.<sup>lxxviii</sup> The elements present in concentrations of at least 0.1 wt% can usually be quantified to within  $\pm 1\%$  of the measured abundance.<sup>lxxix</sup>

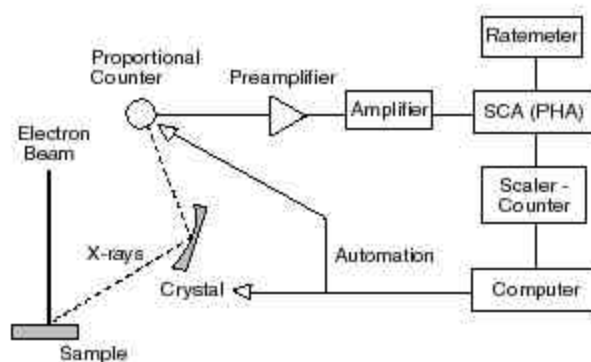


Figure 6.3-3: Schematic of a WDS system (top).<sup>lxxiv</sup>

## Comparison of EDS and WDS

Wavelength dispersive spectrometers are the most qualitative analysis techniques having a high resolution and a high peak-to-background ratio as compared with the energy-dispersive spectrometers.<sup>lxxiv</sup> WDS has a high-count rate capability and high-energy resolution at a few hundred nanometers. The EDS, on the other hand, has a low peak-to-background ratio, or signal-to-noise ratio, resulting in poor spectral resolution.<sup>lxxvii</sup> The resolution of the EDS is about 30 times poorer than that obtainable with WDS even at high voltage. However, it is more time consuming to analyze using the WDS as compared with the EDS. The EDS is a quick easy way to qualitatively identify which elements are present.

Specifically, the sensitivity, or minimum detectability limit for a given element of x-ray measurement for WDS, is 100 ppm, while the sensitivity for EDS it is 1000 ppm.<sup>lxxvii</sup> This is limited to the electron scattering in the specimen and not the focused electron beam diameter. In other words, the analysis is not dependent on the resolution size but the quality of the emission detection. EDS can be used to measure the characteristic peaks of the light elements, while WDS is better used for heavier elements because of the shorter wavelengths.

### Sample Preparation

These quantitative analysis techniques (EDS and WDS) are limited to flat, polished specimen surfaces. Specifically, metal specimens must be prepared according to the type of information required for the analysis. Table 6.3-1 indicates the required surface condition for specific types of analyses.

**Table 6.3-1: Surface condition requirements for specific types of electron dispersive analysis methods.**

<b>Analysis Method</b>	<b>Detector type</b>	<b>Required Surface Condition</b>
Surface Topography	SEM	Clean and Undamaged
Microstructural and Microchemical Analysis	Light-Optical Microscope	Polished Flat, Scratch-Free, Etched Surface
Microstructural and Microchemical Analysis	SEM or EPMA	Polished Flat, Scratch-Free, Surface (no etching)

In addition, nonconductive specimens will generally charge under the influence of the electron beam, resulting in poor quality images or x-ray analysis. To avoid this specimens are generally sputter coated with a conductive metal (Au, Pd, or Pd/Au) for high-resolution imaging or with evaporated carbon for x-ray analysis.<sup>lxxvii</sup> This may be an issue even with metal specimens because of the common metallurgical preparation techniques. Many times metal specimens are encased in an epoxy-type material mount, which is not conductive, insulating the metal.

### Analysis Methods

This study used a LEO 1550 Field Emission SEM for imaging analysis. This equipment is located in the Center for Science and Technology (NSF) owned by the Materials Research Institute at Virginia Tech. The LEO 1550 has a resolution of 1 nm at 20 kV with a magnification range of 20x to 900,000x. It is capable of acceleration voltages of 200V to 30kV and a probe current of 4 pA to 10nA. The analysis features include BSE and SE imaging and EDS analysis.



A CAMECA SX-50 Electron Probe Micro Analyzer (EPMA) was used for the compositional analysis. This equipment is located in the Department of Geological Sciences at Virginia Tech. The CAMECA is capable of:

- Analysis of areas as small as 1-3  $\mu\text{m}^2$
- BSE and SE imaging
- 4 multi-crystals available for simultaneous WDS analysis
- PGT energy-dispersive spectroscopy (EDS)
- Quantitative analysis of elements N through U
- Analog compositional mapping using WDS

The SEM and EPMA studies were used to characterize large-area solder joint specimens. The materials of interest were various solder alloys, Sn/37Pb, Sn/3.5Ag, Sn/Ag/0.7Cu, Sn/5Sb, and CASTIN. The following discusses the analysis techniques and methods employed for this study and the results they relate to the use of the equipment.

The SEM was used for image analysis of the solder joints, mainly the intermetallics formed between the solder and the metallization on the direct-bond copper (DBC) substrate in the electronics package. Specifically, this discussion will focus on the Sn/37Pb and Sn/3.5Ag solder alloys and two metallization layers, plain copper and Ni-plated copper. The EPMA was used to analyze the composition intermetallic layer.

## Imaging

The LEO 1550 has a BSE detector and two SE detectors. The SE2 detector is offset from the sample. Surface topography is enhanced by the SE2 technique due to the fact that the electron detector is at an angle to the sample. Intensity differences are relative to the amount of electrons that bounce from the surface to the detector. Electrons reflecting off topographical features angled away from the detector will be imaged as a shadow. The InLens detector is an SE detector parallel to the electron beam. Electrons reflecting directly off the surface at a 90 degree angle will be detected. This technique is more sensitive to the elemental differences in the specimen than the topography. However, the BSE detector is most sensitive to the elemental differences due to the detection of high-energy backscattered electrons. Backscattered SEM images provide direct information on compositional heterogeneity because of the atomic number contrast. Even slight differences in atomic number can be detected with some experience. The number of electrons counted by the detector is dependent on the atomic number of the elements in the sample. Lighter areas indicate elements higher atomic number.

The compositional contrast in the secondary-electron signal is very sensitive to the condition of the sample's surface. The topographic contrast actually observed depends on the

detector used and its placement relative to the specimen and on the exact mix of backscattered and secondary electrons detected.<sup>lxxiv</sup> For topography with the secondary-electron detector, the angle of incidence varies because of the local inclination of the specimen surface features. Images 1a and 3a in Figure 6.3-4 illustrate the 3-D and shadowing of the SE2 detector. The darker regions are where the electrons from the specimen were directed away from the detector. Hence, the sense of topographic contrast is reversed, so that shapes appear “inside out” compared with the low angle detector.<sup>lxxiv</sup> The images taken with the BSE detector reveal elemental differences such as in images 1a, 2a and 3a in Figure 6.3-4.

In order to excite enough electrons penetration depth of the beam must be controlled. This is a function of the angle of incidence of the primary beam, the magnitude of the beam current, the acceleration voltage of the beam, and the average atomic number of the specimen. The depth of electron penetration of the electron beam is described as the excitation volume. This is where the characteristic emissions are generated in the specimen; therefore, elements in this region will be analyzed. Figure 6.3-5 illustrates the change in the excitation volume with respect to the atomic number,  $Z$ , and the acceleration voltage of the beam,  $E$ . This also shows the difference in methods for studying different elements. For this study heavier elements, Sn, Pb, Ag, Cu, and Ni were of interest, so a high acceleration voltage was used in order to achieve a larger count rate. The difference in imaging capability can be seen in Figure 6.3-6. The benefits of a high voltage are improved imaging depth and resolution. With increasing voltage the elemental differences became clearer using the BSE detector. However, this improved resolution is offset by the fact that this voltage level caused increased damage in a shorter amount of time.

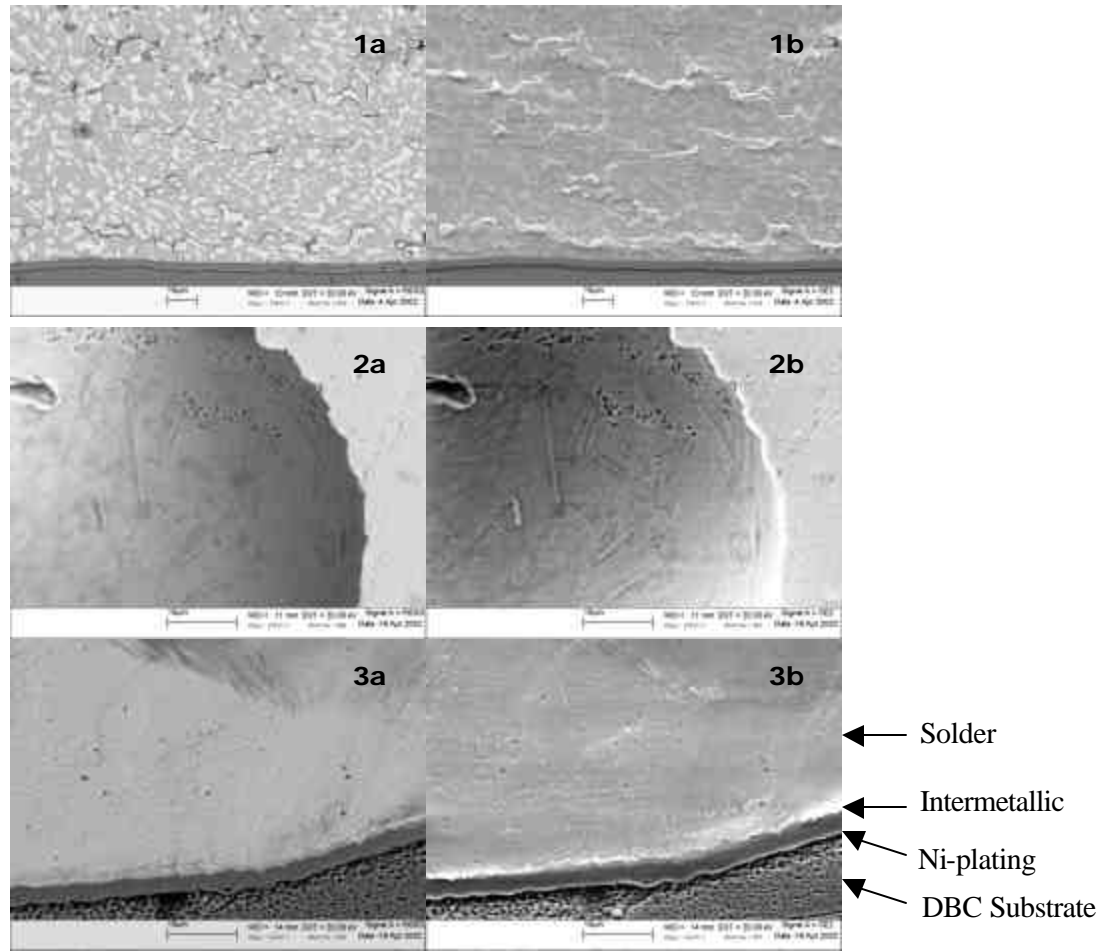


Figure 6.3-4: The images on the left (1a, 2a, and 3a) were taken with the BSE detector while the images on the right (1b, 2b, and 3b) were taken with the SE2 detector. Images 1a and 1b are of Sn/37Pb and images 2a, 2b, 3a and 3b are of Sn/3.5Ag.

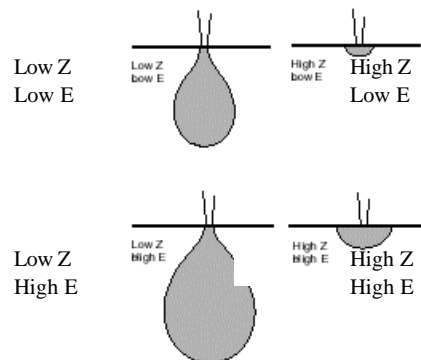
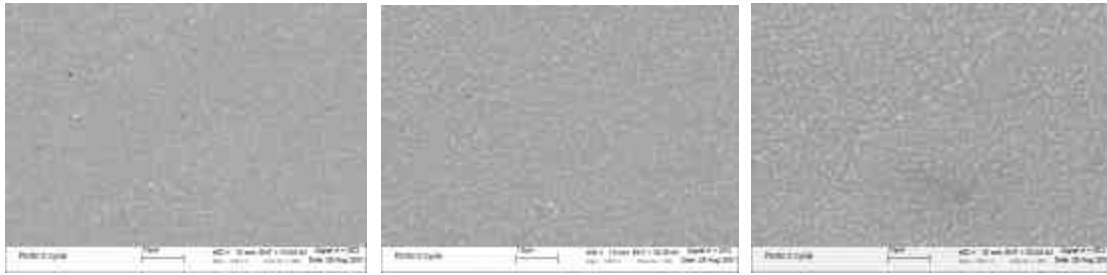
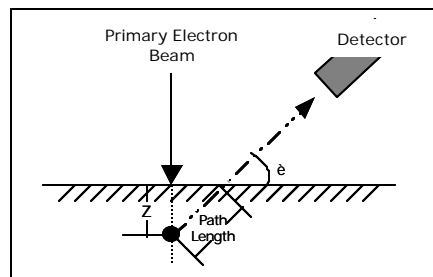


Figure 6.3-5: Comparison of atomic number and acceleration voltage to interaction volume.



**Figure 6.3-6: The same area of a Sn/37Pb solder specimen was taken at different acceleration voltages at 10 kV, 20 kV and 30kV, left to right respectively.**

The take-off angle is also important for imaging depth and resolution. The take-off angle for the CAMECA SX-50 is  $40^\circ$ . This is the maximum angle that can be achieved because it is limited by the physical design of the equipment. The geometry of the beam-specimen-detector interactions defines the take-off angle,  $\theta$ , as seen in Figure 6.3-7. The larger the take-off angle, the shorter the path length in the specimen; hence, by increasing the take-off angle the absorption of the generated x-rays back into the specimen will be minimized. In addition, a higher take-off angle will minimize the effects of surfaces, which deviate from  $90^\circ$  with the electron beam. In order to reduce the path length the depth of excitation,  $Z$ , should be decreased. Using minimum electron beam energy,  $E_0$ , the path length can be reduced. However, the trade-off for using a lower acceleration energy is the lower x-ray count. Hence, penetration depth, resolution, and count rate all require slightly different settings for optimization, so the user must weigh the benefits and drawbacks for each specimen.



**Figure 6.3-7: General diagram illustrating the measurement of the take-off angle.**

### Point Analysis

Analyses were made on the intermetallic layer of the solder/metallization in the specimens using the WDS system in the Electron Microprobe. For the elements of interest (Sn, Cu, Ag, Pb, and Ni), analyzing crystals that could be calibrated to detect these elements were carefully chosen (Table 6.3-2). Using the SEM capability of the CAMECA, I chose points

where the analysis should be done. All of the point analyses were taken on or adjacent to the intermetallic layers of the specimens.

**Table 6.3-2: The assignment of elements to the available crystals in the CAMECA.**

<b>Crystal</b>	TAP	PET	PET	LIF
<b>Element</b>	Cu	Ag	Sn and Pb	Ni

The point analyses that were taken did not seem to remain consistent. This was due to the variations in the regions analyzed and the surface condition of the specimen at each point. The point analyses are tabulated in Table 6.3-3. Specimen 10313 contains Sn/37Pb solder on a plain copper DBC and specimen 50313 contains Sn/3.5Ag on a plain copper DBC. Specimen A07mid contains Sn/37Pb solder on a Ni-plated DBC. However, according to these analyses, specimens 10313 and 50313 contain a small amount of Ni. I used these analyses as preliminary data to identify areas of interest.

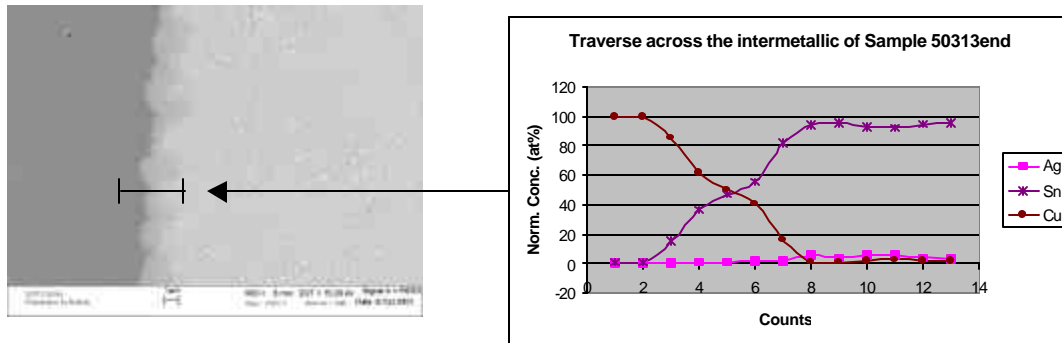
**Table 6.3-3: Normalized concentration in atomic % for the point analyses taken during this study (average error ~ 5%).**

<b>Point</b>	<b>Specimen</b>	<b>Sn</b>	<b>Cu</b>	<b>Ag</b>	<b>Pb</b>	<b>Ni</b>	<b>P</b>
1	10313	14.2791	85.3106	0.0013	0.2330	0.1760	N/A
2	10313	17.6745	81.3340	0.00	0.4321	0.5595	N/A
3	10313	21.6447	77.0378	0.0066	0.6420	0.6688	N/A
4	A07mid	4.7043	0.00	0.0049	0.5399	94.7510	N/A
5	A07mid	1.6875	0.00	0.0603	0.2948	80.8459	17.1114
6	50313	52.5633	44.20095	0.8698	0.0500	2.3073	0.00

### Multi-Point Analysis

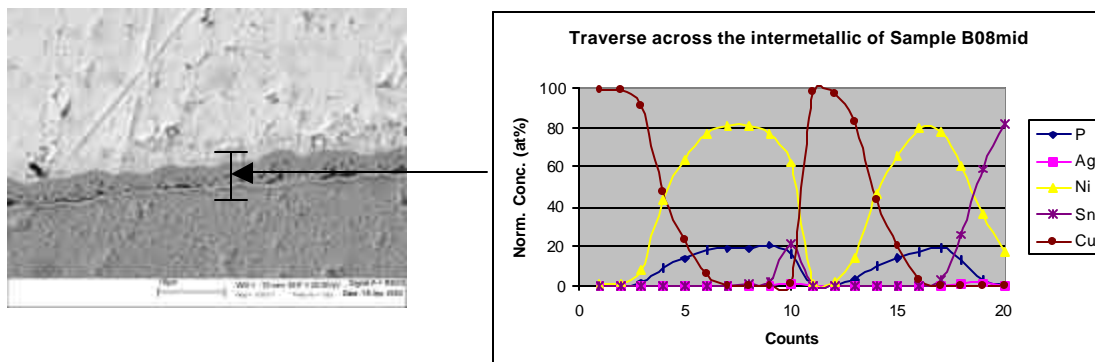
The intermetallic formed when the Sn-based solder was melted on the Cu or Ni-plated surface. This activated a phase formation preferentially between the Sn and the Cu or Ni. In order to observe the compositional gradient across the intermetallic in the specimen I performed a multi-point analysis. This consists of multiple point analyses. The region of interest was chosen within which a specified number of analyses were performed. In addition, I chose a scan rate weighing the benefits of resolution versus testing length. Each automated analysis consisted of 13 to 20 points and took approximately 45 minutes to 1 hour to perform. Figure 6.3-8 and illustrate the multi-point analysis that I performed across the intermetallic layers. The specimen Figure 6.3-8 contains an intermetallic containing Sn and Cu formed between Sn/3.5Ag solder and a plain copper DBC substrate. As you can see, there is a variation across the intermetallic

where the two materials diffused together during formation. It is estimated that closer to the copper the intermetallic composition will be closest to  $Cu_3Sn$  and closer to the solder the intermetallic composition will be approximately  $Cu_6Sn_5$ . The silver did not form with the copper so little to no silver will be found in the intermetallic.

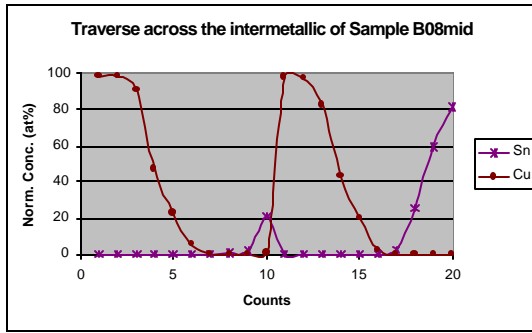


**Figure 6.3-8: Traverse of the intermetallic formed between a Sn/3.5Ag solder and a plain copper DBC substrate.**

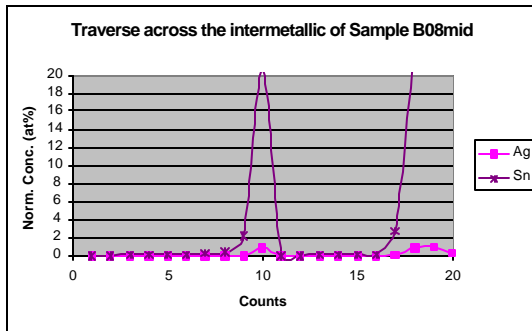
Figure 6.3-9 is a graphs of a traverse across the Sn and Cu intermetallic formed between Sn/3.5Ag solder and a Ni-plated DBC substrate. Due to the condition of the surface at the time of the scan, the data appears irregular. The scratches and holes in the surface affected the readings from the WDS. Figure 6.3-10 is a close up view of the significant areas in Figure 6.3-9. The plot indicates that the Ag component did not combine with the Cu but remained alloyed with the Sn in the solder. In addition, a high level of phosphorous was discovered along with the nickel. During the manufacturing of the Ni-plated DBC phosphorous is added to achieve a shiny finish to the nickel plating. During the construction of the power devices, I had problems with using a vacuum reflow chamber for soldering. It had been suggested that too much phosphorous could have caused these problems. The evidence in now proves that this indeed could have caused reflow problems.



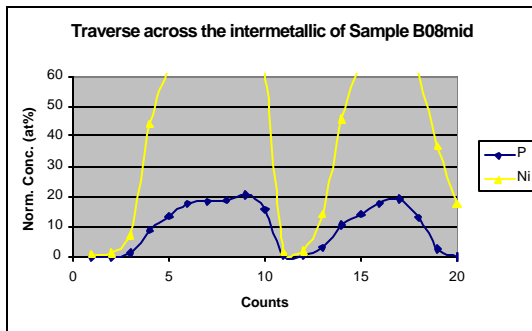
**Figure 6.3-9: Traverse of the intermetallic formed between a Sn/3.5Ag solder and a Ni-plated DBC substrate.**



It is evident that the scan was done over a rough area on the sample, creating a non-uniform traverse analysis across the intermetallic.



However, it is worth noting that the maximum amount of silver was found in the same regions where the tin was found to have maximum concentration. This reflects the solder alloy composition of Sn and Ag.



Likewise, the amount of phosphorous was maximum where the nickel was found to be concentrated.

Figure 6.3-10: Data of specific elements from the traverse analysis of B08mid specimen.

Images were taken of the same samples after thermal cycling to 350 cycles. Because the results of the traverses were limited to a few sets of data and the variation in the sample surfaces, the data could not be directly compared. Figure 6.3-11 is a collection of traverse data across the intermetallic of a sample with a Ni-plated DBC substrate and Sn/3.5Ag solder. This plot more clearly identifies that the intermetallic created during soldering is between Ni and Sn. The compositional gradients across the Cu/Ni and Ni/Sn interfaces are more apparent.

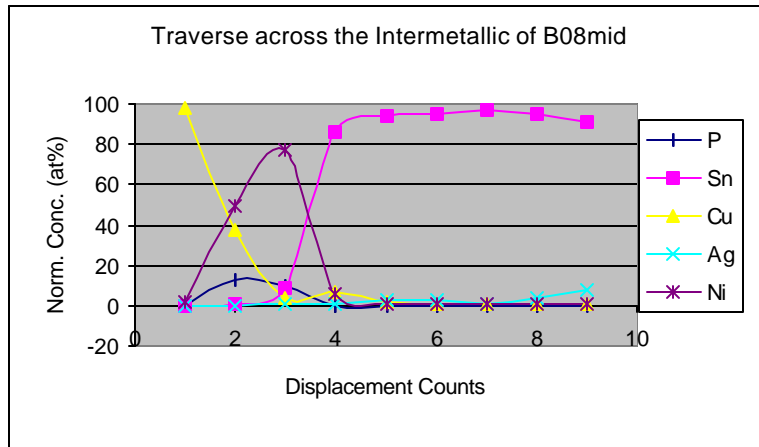


Figure 6.3-11: Traverse of sample B08mid after 350 thermal cycles.

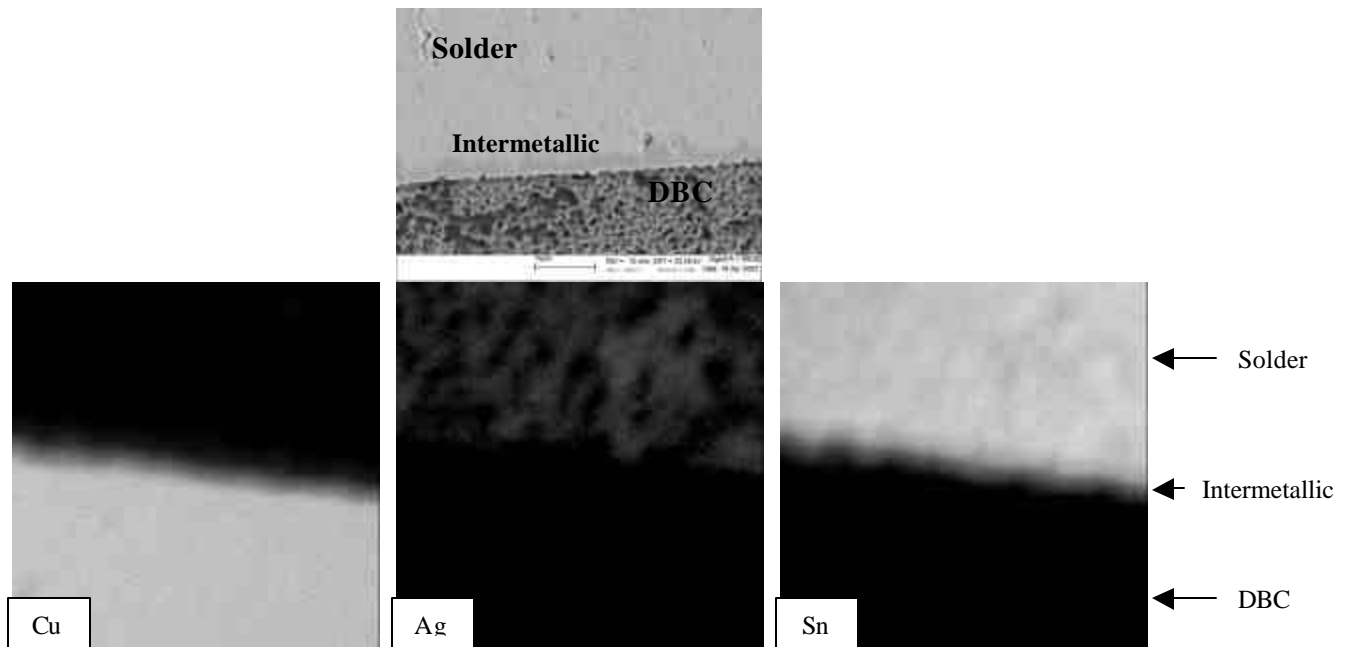
### Image Mapping Analysis

Digital compositional mapping involves the systematic collection of count-rate data (characteristic x-rays), which will then be quantitatively analyzed at every pixel scan.<sup>lxxiv</sup> Each pixel is analyzed with a selected count-rate and the beam is rastered over a specified number of pixels. Many times there are multiple wavelength-dispersive spectrometers available, therefore, measurements of multiple elements can be performed simultaneously with each spectrometer on a different element. For a more qualitative analysis, an EDS unit maybe used to analyze the entire spectrum at once, allowing for elements not initially expected to be in the specimen. The WDS technique can be used to identify specific elements and their compositions quantitatively. I used the WDS technique for this work to identify the composition and location of elements present.

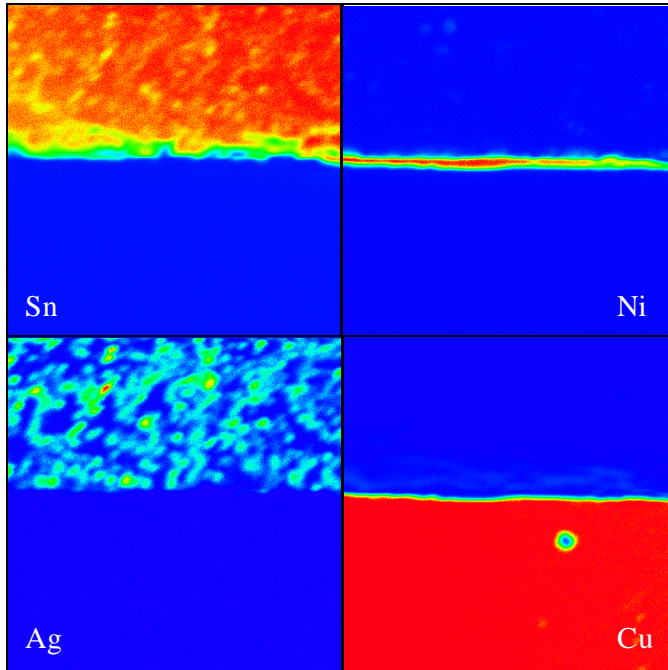
The beam is rastered across an area of the specimen as done during imaging (SEM); however, the x-rays are collected either by the WDS unit. Because of the low x-ray signal rate generated compared to the backscattered electron signal rate, the mapped image accumulation rate must be made over a longer period of time than for typical SEM imaging. In addition, in order to generate a sufficient x-ray signal, or maximize the count rate, a high beam energy is generally chosen. The beam energy I used for this work was 15 kV and the data was collected over an hour. For elements of interest that are present at a level of 10 wt% or more, the count rate can be reduced to an average count of  $10^6$  x-rays accumulated in 200s. However, for constituents present at a level of 1 wt%, the scanning time would have to be increased to 2000s.<sup>lxxiv</sup> Figure 6.3-12 shows the results of the data collected for a specimen of Sn/3.5Ag solder on a plain copper DBC substrate. The top image is an SEM image of a similar region on the specimen as the compositional mapping images below. Notice that the silver is again only associated with the tin. Also, the region where the intermetallic is located indicates that the Cu



and Sn diffused together in this region, so a gradient is visible across the intermetallic. Refer back to Figure 6.3-8. Figure 6.3-13 is an image map taken after 350 cycles of a lead-free solder sample with a Ni-plated DBC substrate. The image was digitally enhanced with color to identify the comparative concentrations of elements in the same region.



**Figure 6.3-12: Digital image mapping of the Sn/3.5Ag solder on a plain copper DBC substrate (scale 96 microns by 96 microns square).**



\* Red indicates highest concentration and Blue is the lowest concentration.

**Figure 6.3-13: Digital image maps of the elements across the intermetallic of a sample containing a Ni-plated DBC substrate and Sn/3.5Ag solder (scale 96 microns by 96 microns square).**

## 6.4 Appendix D: Policy Brief

Currently, there are two major driving forces for considering alternative materials in electronics applications, including the impending legislation or regulations which may tax, restrict, or eliminate the use of lead and the trend toward advanced interconnection technology, which may challenge the limits of present soldering technology.<sup>vii</sup> The Directive for Waste Electrical and Electronic Equipment (WEEE) is proposed to come into effect 1 January 2006, which will limit the disposal of hazardous materials by eliminating certain materials from electrical and electronic products.<sup>i, ii</sup> The electronics industry is concerned with the elimination/reduction of the use of many important materials. Specific to this discussion is lead, a major component in solder alloys used in most all electronics today. The contradiction is that in efforts to focus on the environmental and health issues associated with such materials, implementation actions may be requiring alternatives, which overlook direct and indirect health and environmental effects associated. This paper explores the current legislation proposed by the European Commission and discusses potential strategies for understanding and implementing actions to address the issues.

The proposed WEEE Directive was drafted for the intent of protecting human health and the environment as required by Article 174 of the European Community Treaty (EC Treaty).<sup>i, v</sup> The WEEE Directive seeks to minimize the use of certain dangerous substances (including lead), to increase the use of recyclable materials, to design for upgrade, reuse, ease of disassembly and recycling, to set up systems for free take-back at end-of-life, and to insure that the cost of collection, treatment, recovery and environmentally sound disposal is borne by the producers.<sup>vi</sup> The focus of the Directive's proposed actions in achieving these goals is to eliminate hazardous materials, which have the potential to cause health or environmental damage. However, these alternatives have not been specified within the Directive. It has been left to the industry to determine these replacements. Through industry experience and research, there have been numerous economic and environmental factors identified that may contradict the theory that replacement materials will be the best solution.

The proposal essentially requires that lead must be replaced with alternative materials in the production of electrical and electronic products. Specifically for the electronics manufacturing industry, this has required much research and modification to existing processes. Table 1 found in the Appendix illustrates the issues surrounding the Directive from the environmental, economic, and social perspective regarding the replacement of lead in solder materials.

The most common material used to create connections for conductors in an electronic assembly is tin/lead solder. "After many decades of effort, highly engineered systems have been

developed, consisting not only of the solder, but also of metal finished, fluxes, design rules, manufacturing protocols, testing, repair, and reliability.<sup>xi</sup> Hence, there is a lack of data on alternative materials in the electronics industry as compared to lead-based solders, which have been used in the industry for over 50 years.<sup>xi</sup> Therefore, there is a large base of data on the reliability, performance, and properties of these lead-based materials in specific applications to the electronics industry. Consumer satisfaction and the health of the industry is a concern. Some of the changes include, higher processing temperatures, which may affect adjacent manufacturers such as component manufacturers, PCB board producers, chemical suppliers, and so forth.

Likewise, some of the issues facing the manufacturing industry may also become environmental issues in the life span of electrical and electronic products. For instance, the higher processing temperatures required by these alternative solder alloys require more energy and release waste heat. Many of these alternative alloys require stronger chemicals for processing such as flux chemicals for production and cleaning processes.<sup>lxxx</sup> In addition, the WEEE Directive is concentrated on the end-of-life of electronic and electrical equipment, leaving out external effects from mining and production of the replacement materials.<sup>vi</sup> It has been determined that the mining of these alternative materials may increase the demand on scarce resources and create a surplus of waste lead for the fact that many of the alternative materials such as the base material tin are mined in conjunction with lead.

Since the WEEE Directive specifically identifies materials of concern but does not suggest alternative materials, there is concern that there could be a future ban on the alternative materials chosen. Many of the suggested alternatives for lead-based solder can be just as hazardous with the same concerns as lead during incineration and land filling. For instance, antimony is a concern in the Netherlands because of incinerations practices, while silver in high concentrations is also toxic in drinking water.<sup>lxxxi</sup> With an increase in demand of some of these alternative materials, potential for environmental damage related to increased/new mining activities and health risks due to an increase in exposure potential is eminent.

The industry is in compliance with legislation internationally (US EPA, Australia, Denmark, Sweden), which addresses environmental and health issues associated with lead.<sup>lxxxii</sup> The Japanese Ministry of Industry and Trade Institute (MITI) has proposed legislation, which emphasizes recycling and only “suggests” that reducing the use of lead as a part of the increased recycling.<sup>lxxxiii</sup> Since the request for the WEEE Directive in 1986, trade and research organizations within the industry began to create task forces to research the issues of replacement of lead (IPC, EIA, NCMS, NEMI, PCIF, ITRI).<sup>lxxxiii</sup> Thus far, the industry and other organizations have determined that there are no viable alternatives available for complete material replacements.<sup>xi,lxxxiii, iii</sup>

In light of evidence that the replacement of lead-based solders in electronics by alternative materials may not be a direct improvement and may not fully address the Directive's objectives, further options should be reviewed in order to obtain a sustainable policy as suggested by Articles 174 and 175 of the EC Treaty.<sup>i, v</sup> The vision of the policy is far reaching in the future with respect to recycling and disposal actions; however, the implementations proposed create present issues. In other words, the sustainable ideas proposed address the vision of the Directive ideally but the proposed actions put the "cart before the horse."

Fundamentally, "politics influence the present and future activities of others," including business, economic, political, social, environmental, and military organizations.<sup>lxxxiii</sup> Therefore, "policy implies, first and foremost, the authority to cause changes in our social environment.<sup>lxxxiii</sup>" Addressing the fear of hazardous materials such as lead is politically, socially, and environmentally acceptable in a fundamental way. However, the resulting effects such as electronic product changes (cost, reliability, etc.), disposal options (take-back programs), and world trade will need to be addressed in order for such policies to be successful.

The characteristics of a policy can be broken into two major parts, the directive and the implementation. The policy directives establish the goals of the implementation function.<sup>lxxxiii</sup> Hence, the policy defines a cause and effect scenario. Issues of concern are identified and the desired outcome is stated in the directive. Then the actions associated with the implementation are proposed.

In the case of the WEEE Directive, the implementation actions are stated along with the desired outcome. Hence, the WEEE "Policy" can be broken apart into the two areas: goals and actions. The fundamental objectives of the WEEE Directive are sound: first to reduce the amount of waste electronics, specific to hazardous materials contained within, from entering the waste stream, whether to landfill or incineration. Secondly, because of the potential for human health and environmental impact, there is request for more control over "hazardous" waste associated with electronic and electrical equipment. There are many ways to address the Directive's objectives.

The WEEE Directive addresses the issues of hazardous materials in the municipal waste stream and potential for health and environmental damage by eliminating the use of certain materials, specifically lead discussed in this paper. There are four recommendations concluded from this study:

1. Recycling

Focus on improving recycling technology and take-back programs to address present and near future problems, such as stock piled computers waiting for disposal.<sup>i, lxxxiv</sup> By creating

programs for the recycling of past and present technologies, future products can be easily incorporated.

## 2. Research and Development

Create incentives for the reduction and elimination of certain material in future products and/or increase study on recycling processes, which will be focused on industry R&D and academic research. By taking advantage of the inherent properties in alternative materials, new technologies may develop rather than replacing older technologies. The proposed Directive creates focus on present technology changes rather than future development of the industry.

## 3. Incorporate Recycling and Redesign

Incorporate recycling with these new and newly redesigned products. Hence, as old products and technologies go out and new products come in, there will be a framework established for recycling.

## 4. Life Cycle Studies and Methodologies

Prepare a study of the alternatives to determine risk and establish methodologies for identifying and proposing actions for waste disposal issues.<sup>vi, lxxxiv</sup> In order to address these issues it must be recognized that products can be broken down into two major components the materials and the application. By understanding the products to be disposed of more thoroughly rather than just the action of disposal, the potential for health and environmental contamination can be drastically reduced

**Table 6.4-1: Issues related to the replacement of lead-based solder in electronics with alternative materials.**

Issue	Environment	Economics	Social
Human Health	<ul style="list-style-type: none"> <li>• Incineration releases from burning certain hazardous materials could be reduced</li> <li>• Some of the suggested alternatives for lead-based solder can be just as hazardous with the same concerns during incineration or land filling</li> </ul>	<ul style="list-style-type: none"> <li>• There is potential that the alternative materials have just as many health impacts as lead in varying quantities</li> </ul>	<ul style="list-style-type: none"> <li>• Lead has become a public concern, affecting children most often and with replacements these concerns will be addressed</li> </ul>
Waste Disposal Options / Recycling	<ul style="list-style-type: none"> <li>• Potential for environmental contamination, leading to health issues</li> <li>• Stock piled and production of new electronic products containing lead-based solders will at some point enter the waste stream</li> <li>• Generally electronics are not pretreated prior to land filling or incineration</li> <li>• In larger quantities, the alternative materials have the potential for polluting</li> <li>• Chemical processes and energy are used to recover. There is an optimum amount of material to be recovered compared to energy spent.</li> <li>• With replacement material, the alloy stream to be recovered will become more diverse and therefore harder to separate</li> <li>• It is speculated that the alternatives may have an equivalent impact on the environment as with lead materials</li> </ul>	<ul style="list-style-type: none"> <li>• Extra costs to treat this defined hazardous waste will increase with time (stock piles and new)</li> <li>• Reduction in production costs using recycled or secondary material</li> <li>• Disposal costs are saved with recycling</li> <li>• With an increase in recycling, there will be a reduction in recycling and re-use costs.</li> <li>• The diverted materials would then be reintroduced in to the economic cycle, promoting a more sustainable use of resources.</li> <li>• Cost to recover such small amounts of material from the amount of total waste likely will not be efficient</li> <li>• Assemblies containing multiple materials due to the replacement of Sn/Pb will create a mixed metal stream that will decrease the recyclability and increase the amount that goes to landfill</li> </ul>	<ul style="list-style-type: none"> <li>• There is concern in many countries over land filling versus recycling with respect to the efficiency and effectiveness of recycle programs</li> <li>• Recycling is a positive action for many people; however, policies and facilities are not in place to make this process a part of everyday life</li> </ul>
Manufacturing	<ul style="list-style-type: none"> <li>• Higher temperature processing</li> <li>• Mining activities</li> <li>• Alternative material resources more scarce</li> </ul>	<ul style="list-style-type: none"> <li>• Lack of reliability data</li> <li>• Higher manufacturing costs                             <ul style="list-style-type: none"> <li>• Higher temperature</li> <li>• Material cost</li> <li>• Component damage</li> <li>• Change of other processes</li> <li>• Mining scarce resources</li> </ul> </li> <li>• There is a concern that the alternative alloys being considered may potentially fall under a future ban.</li> </ul>	<ul style="list-style-type: none"> <li>• Consumers respond to “lead-free”</li> <li>• Sony introduced a lead-free mini-disk which increased in sales by 11%</li> <li>• Consumers are unaware currently of the issue; however, will become aware</li> </ul>

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## Vita

Kelly Stinson-Bagby was born on January 16, 1975 in Salem, Virginia, United States. She began pursuing a career in engineering by receiving an Associates Degree in Engineering at Virginia Western Community College located in Roanoke, Virginia in 1997. She went on to earn her Bachelor's Degree in Material Science and Engineering at Virginia Polytechnic Institute and State University in Blacksburg, Virginia in 2000. In Summer 2002, she defended her master's thesis. She was accepted into the Engineering and Public Policy Program at Carnegie Mellon University and was offered an open acceptance while she works. So following she has accepted a position as a Materials Research Engineer with Luna Innovations located in Blacksburg, VA.

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