UBM Formation on Single Die/Dice for Flip Chip Applications

By

Suwanna Jittinorasett

Thesis submitted to the Faculty of the

Virginia Polytechnic Institute and State University

in partial fulfillment of the requirements for the degree of

Master of Science

in

Electrical Engineering

Dr. Aicha Elshabini (Chairman)

Dr. James E. McGrath

Dr. Ioannis M. Besieris

Dr. Jerry E. Sergent

August 25, 1999

Blacksburg, Virginia

Keywords: Flip Chip, Under Bump Metallurgy (UBM),

Solder bump, Single die

Copyright 1999, Suwanna Jittinorasett

UBM Formation on Single Die/Dice for Flip Chip Applications

by

Suwanna Jittinorasett

Committee Chairman: Dr. Aicha Elshabini

Electrical Engineering

Abstract

This thesis presents the low cost process for UBM formation on aluminum pads of single die/dice for Flip Chip applications. The UBM (Under Bump Metallization) is required in solder bump structure to provide adhesion/diffusion barrier layer, solder wettable layer, and oxidation barrier layer between the bonding pads of the die and the bumps. Typically, UBM is deposited on the whole wafers by sputtering, evaporation, or electroless plating. These deposition techniques are not practical for UBM formation on single die/dice, thus preventing Flip Chip technology to be applied in applications where the whole wafers are not available. The process presented in this thesis has been developed to overcome this problem. The developed UBM formation process allows the UBM layer to be deposited on a single die, thus eliminating the requirement to have the whole wafer in the deposition process. With the combination of the UBM formation process developed in this work and a suitable bump formation technique, solder bumping on a single die can be achieved, thus making Flip Chip technology available for use in low volume applications and prototyping stages.

The developed UBM formation process consists of two major steps; temporary die attach process and UBM deposition process. The first process is developed using thermoplastic adhesive film. The second process is developed using electroless nickel plating, followed by gold immersion. It has been demonstrated in this thesis that the developed process can be used to form the UBM layer on the die successfully regardless of the die size and the complexity of the die pattern, and that this process does not damage nor affect electrically the sensitive die.

Acknowledgments

I am grateful to Dr. Aicha Elshabini for being my advisor and for her guidance throughout this thesis. I also would like to thank her for her advise and the financial support provided during my graduate studies.

I would like to thank Dr. James McGrath, Dr. Ioannis Besieris and Dr. Jerry Sergent for serving on my graduate committee.

I am grateful to all of the microelectronics lab members for their helps in my thesis and my lab work. I would like to thank Fred Barlow for his endless efforts supporting my work, Alex Lostetter and Richard Hoagland for helping me learn the lab equipment operation and for their assistance through my thesis and all of my work.

I would like to thank Prinya Atiniramit for his friendship and understanding.

Finally, I dedicate this work to my mother and my only sister.

Table of Contents

CHAPTER 1 INTRODUCTION 1

1.1 Statements of Problems 1

1.2 Objective of Research Work 1

1.3 Techniques Used 2

1.4 Structure of Thesis 2

CHAPTER 2 LITERATURE REVIEW 4

2.1 Introduction 4

2.2 Chip Level Interconnects 5

2.2.1 Wirebonding 5

2.2.2 Tape Automated Bonding (TAB) 6

2.2.3 Flip Chip Bonding 7

2.3 Solder Bump Structure for Flip Chip Interconnect 10

2.3.1 Under Bump Metallurgy (UBM) 10

2.3.2 Solder Bump 13

2.4 Electroless Nickel UBM 20

2.4.1 Techniques for Electroless Nickel Plating on Aluminum 20

2.5 Conclusions 22

CHAPTER 3 FLIP CHIP ASSEMBLY 24

3.1 Introduction 24

3.2 Flip Chip Placement 24

3.2.1 Fully-Automatic Flip Chip Placement 25

3.2.2 Semi-Automatic Flip Chip Placement 28

3.3 Solder Reflow 31

3.3.1 Forced Convection Reflow System 32

3.3.2 Hot Plate Reflow System 32

3.3.3 Reflow Systems for Low Volume Flip Chip Assembly 32

3.4 Flip Chip Underfill 33

3.4.1 Functions of Underfill 33
3.4.2 Underfill Process 34
3.5 Conclusions 37

CHAPTER 4 UBM FORMATION TECHNIQUE FOR SINGLE DIE/DICE 38
4.1 Introduction 38
4.2 UBM Deposition Process 38
4.2.1 Concept 38
4.2.2 Process Flow and Results 41
4.3 Temporary Die Attach Process 52
4.3.1 Concept 52
4.3.2 Experimental Procedure 53
4.3.3 Experimental Results and Discussions 54
4.4 Conclusions 58

CHAPTER 5 APPLICATION OF THE DEVELOPED UBM FORMATION PROCESS IN FLIP CHIP BONDING OF A SINGLE DIE 60
5.1 Introduction 60
5.2 Objectives of the Work 60
5.3 Overview of the Work 61
5.4 Solder Bump Formation 63
5.4.1 Bump Formation Procedure 63
5.4.2 Bump Formation Results 64
5.5 Flip Chip Bonding 66
5.5.1 Substrate Design 66
5.5.2 Flip Chip Bonding Procedure 67
5.5.3 Results and Discussions 69
5.6 Conclusions 70

CHAPTER 6 CONCLUSIONS 72
6.1 Summary 72

6.2 Conclusions 73
6.3 Future Work 73

REFERENCES 75

VITA 80

List of Tables

Table 2.1 Integrated Circuit (IC) trends 4

Table 2.2 The Comparison of Three Wirebonding Methods 6

Table 4.1 Specifications of the Experimental Thermoplastic Adhesive Flims. 53

Table 4.2 Summary of Bonding Parameters in the Adhesive Bonding Step and Experimental Results/Data 55

Table 4.3 Summary of Selected Solvents in the Adhesive Cleaning Step and the Experimental Results 56

List of Figures

Figure 2.1	Solder Bump Structure	10
Figure 2.2	Solder Evaporation Process	17
Figure 2.3	Solder Printing Process	17
Figure 2.4	Solder Electroplating Process	18
Figure 2.5	Stud Bumping	19
Figure 2.6	Solder Transfer Process	19
Figure 3.1	Flip Chip Process after Bump Formation and Dicing	24
Figure 3.2	A 2"×2" Waffle Tray	26
Figure 3.3	The Table Top Flip Chip Placement System-Model 850	28
Figure 3.4	The 4"×4" Pick-Up Stage	30
Figure 3.5	The Flux Stage and Doctor Blade	30
Figure 3.6	Cross Section of an Underfilled Flip Chip	33
Figure 4.1	Thickness VS. Time – Comparison between Electroless and Immersion Deposition	39
Figure 4.2	SEM Photograph of a 4 Mil × 4 Mil Aluminum Pad of the Test Die	42
Figure 4.3	EDX Analysis of an Aluminum Pad of the Test Die	42
Figure 4.4	SEM Photograph of an Aluminum Pad after the First Zincation	44
Figure 4.5	SEM Photograph of an Aluminum Pad after Electroless Ni Plating with Single Zincation Treatment	45
Figure 4.6	SEM Photograph of an Aluminum Pad after the Second Zincation	45
Figure 4.7	EDX Analysis of a Large Zinc Particle from the First Zincaiton	45
Figure 4.8	EDX Analysis of Zinc Layer after the Second Zincation	46
Figure 4.9	SEM Photograph of Two Aluminum Pads on the Same Test Die after Electroless Ni Plating with Double Zincation Treatment	47
Figure 4.10	EDX Analysis of Nickel on an Aluminum Pad	47
Figure 4.11	EDX Analysis of Two Spots around the Pad	48
Figure 4.12	SEM Photograph of Aluminum Pad of Diode Die after Electroless Ni Plating with Double Zincation Treatment	49
Figure 4.13	EDX Analysis of a Nickel Plated Aluminum Pad of the Diode Die	49
Figure 4.14	SEM Photograph of a Nickel Plated Aluminum Pad of the Power Die	50
Figure 4.15	EDX Analysis of Nickel Plated Aluminum Pad of the Power FET Die	51

Figure 4.16 Thickness Measurement Results of an Aluminum Pad of the Power FET Die 51
Figure 4.17 SEM Photograph of the Backside of a Debonded Test Die 56
Figure 4.18 SEM Photograph of the Backside of Die A after Debonding and Cleaning 57
Figure 4.19 SEM Photograph of the Backside of Die B after Debonding and Cleaning 58
Figure 5.1 Dimensions of the Power FET Die 62
Figure 5.2 The Assembly of the Power FET Die 62
Figure 5.3 Metal Traces around the Edge of the Power FET Die 65
Figure 5.4 Substrate Pattern 67

Chapter 1 Introduction

1.1 Statement of Problems

With many advantages of Flip Chip bonding, it has been used in an aggressive way in the electronic packaging industry, especially to achieve high I/O count and high electrical performance applications. Among the various types of bumps, the solder bump is by far the most common for Flip Chip bonding. In the solder bump structure, UBM (Under Bump Metallurgy), a multilayer of thin film interface metals, is one of the most important components to obtain reliable connections. UBM can be deposited by sputtering, evaporation, or electroless plating. These available techniques are suitable for UBM deposition on wafers. However, it is not practical, or even impossible in certain cases, to deposit UBM on single die/dice with these techniques. This limitation of UBM deposition process prevents Flip Chip technology to be applied in low volume applications and in prototyping stages where the whole wafers are not essentially available.

To make Flip Chip technology available and compatible for low volume applications, the UBM formation process for single die/dice needs to be developed.

1.2 Objective of Research Work

This thesis presents a process to deposit UBM on aluminum pads of a single die. UBM layer is developed to be compatible with solder bump structure, especially eutectic lead/tin solder which is by far the most used solder for Flip Chip bonding. In addition, to make this process suitable for low volume applications, the process is developed to be a low cost and simple process without requiring any specific facilities or specialized equipment.

Furthermore, this thesis seeks to illustrate applications of the developed UBM formation process in Flip Chip bonding of a single die.

1.3 Techniques Used

The UBM formation technique developed in this thesis consists of two major processes; temporary die attach process and UBM deposition process. The first process, considered as the most important, is to temporarily attach the bare die to a substrate so that the UBM deposition process can be performed on the die. This process is developed using thermoplastic adhesive as a die attach material. The second process is to deposit a UBM layer on aluminum pads. Electroless nickel plating, followed by gold immersion, is used. This technique is suitable for UBM deposition on a single die since it is a maskless process and it can be achieved with simple and low cost facilities. The process also provides a good UBM structure for eutectic solder bumps. The UBM deposition process consists of double zincation to pretreat aluminum surface before plating, nickel electroless plating, and gold immersion, respectively.

SEM and EDX detector are the spectroscopy tools used in this work to verify the process. SEM is used to observe the results of each processing step, and EDX detector is used to analyze elemental compositions of the deposited materials.

1.4 Structure of Thesis

This thesis is organized into six Chapters. The Chapter 1 is an Introduction. Chapter 2 presents a literature review of topics relevant to this thesis. The topics include microelectronics packaging trend, chip level interconnect techniques, trends of Flip Chip packaging, solder bump structure and solder bumping techniques, UBM structure and UBM deposition techniques, electroless nickel UBM, and techniques for electroless nickel plating on aluminum.

Chapter 3 presents Flip Chip assembly process flow after solder bumping. The Chapter focuses on commercial machines and procedures used in each process. First, Flip Chip placement process including die feeding, fluxing, alignment and die placement,

are described, respectively. Next, solder reflow process, and Flip Chip underfill process are presented in this Chapter.

Chapter 4 presents the UBM formation process for a single die developed in this work. The first part of this Chapter discusses the UBM deposition technique which consists of double zincation, electroless nickel plating, and gold immersion processes. Results of the processes including SEM photographs and EDX analysis are illustrated and discussed. The second part of this Chapter describes temporary die attach process. Experimental procedure for die attachment using thermoplastic adhesive films, and experimental results and discussion are presented.

Chapter 5 presents an application of the developed UBM formation process in Flip Chip bonding of a single die. The purposes of this application and bonding procedure are described. Finally, the success of applying the developed UBM formation process in Flip Chip bonding of a single die is discussed.

Chapter 6 presents the summary and conclusion of this thesis, providing future directions.

Chapter 2 Literature Review

2.1 Introduction

Microelectronic packaging depends upon the development of integrated circuits (ICs). As IC technologies achieve higher levels of integration, advanced packaging and interconnect technologies need to be developed to answer the new demands resulted from advanced IC technologies.

Table 2.1 Integrated circuit (IC) trends.

Year	1995	1998	2001	2004	2007
Feature size (μm)	0.35	0.25	0.18	0.12	0.10
Transistors/chip	800K	2M	5M	10M	20M
Chip size (mm^2)					
Logic/Microprocessor	400	600	800	1,000	1,250
DRAM	200	320	500	700	1,000
Max. power (W/Die) (High-performance)	15	30	40	40-120	40-200
Power supply (V) (Portable)	2.2	2.2	1.5	1.5	1.5
Number of I/Os	750	1,500	2,000	3,500	5,000
Performance (MHz) (On-chip)	200	350	500	700	1,000

Source: Semiconductor Industry Association (SIA)'s IC Technology Roadmap

With the development of IC technologies, the device/circuitry density (number of transistors per chip), chip size, performance (IC operating frequency), I/O count (number of input-output pins), and IC power dissipation will all increase. These quantities depend on the type of IC devices and electronic products [1,2]. Table 2.1 illustrates trends of some IC devices. The increase of these quantities of IC devices results in the demand of advance packaging and interconnect technologies, especially chip level interconnects, that provide higher density, and better electrical and thermal performance with

competitive cost, good yield, and high reliability. Flip Chip technology is the chip level interconnect developed to achieve the above requirements of advanced electronic packaging. Flip Chip overcomes the limitations of the conventional wirebonding and tape automated bonding.

2.2 Chip Level Interconnects

The most common methods of chip level interconnects or first level interconnects are wirebonding, tape automated bonding (TAB), and flip chip bonding [3,4].

2.2.1 Wirebonding

Wirebonding is the dominant method for chip level interconnect. In this method, the thin gold or aluminum wires are used to make connection between the bonding pads on the chips and the metallization on the substrates. The chip is attached to the substrate face up before the wirebonding process starts. In the bonding process, the wire is passed through the hole in a capillary, and for ball bonding, the small ball is formed at the end of the wire by electrical discharge. In wedge bonding, no ball is needed in this step. Next, the wire is brought into contact with the bonding pad following a first bond search level and the metallurgical bond between the wire and the bonding pad is formed by applying pressure, heat, and/or ultrasonic energy. After the first bond is finished, the capillary is moved to the second bonding position and metallurgical bond is formed between the wire and the metallization on the substrate again following a second bond search level. Next, the wire is cut just following the second bond. The first bond can be ball bond or wedge bond depending on the processes, but the second bond will be essentially wedge bond.

There are there types of wirebonding; thermocompression wirebonding, thermosonic wirebonding, and ultrasonic wire bonding. Table 2.2 illustrates the comparison of these three methods.

Wirebonding does not required additional wafer processing and the process is well understood. However, this process provides peripheral interconnect. Thus, fine pad pitch is required to achieve higher I/O count and very high density (exceeding 1000 I/O

counts) cannot be achieved. Other limitations are the low throughput of the process and the high parasitic components resulting in high propagation delay. These limitations preclude wirebonding from high density and high performance packaging.

Table 2.2 The comparison of three wirebonding methods.

Wirebonding method	**Normal type of metal wire**	**Force applied to form the bond**	**The type of the first bond**
Thermocompression	Gold wire ***Wire diameter:*** 0.0007"-0.002"	Heat and pressure	Ball bond
Thermosonic	Gold wire ***Wire diameter:*** 0.001" or less	Heat, pressure and ultrasonic energy	Ball bond
Ultrasonic	Aluminum wire ***Wire diameter:*** 0.0007"-0.002", and 0.005"-0.02" for high current applications (Gold wire can also be used with wire diameter of 0.002" or larger.)	Pressure and ultrasonic energy	Wedge bond

2.2.2 Tape automated bonding (TAB)

In this technique, the copper lead pattern on polymer tape are used to form connection between bonding pads of bare chips and substrates. The process sequence consists of bump formation, inner lead bonding, and outer lead bonding, respectively.

• *Bump formation:* The bumps are formed on the bonding pads of the die or on the tape. Prior to the bumps formation, the interface metallurgy is deposited to improve adhesion and serve as diffusion barrier. Gold is the most common bump metallurgy used in the process. Bumps can be formed with various techniques such as electroplating, ball bonding, or bump transfer.

• *Inner lead bonding:* This process is to bond the patterned copper leads on the tape to the bumped pads of the chip. The copper leads are either Au or Sn plated. For Au plated

leads, thermocompression or thermosonic bonding is used to bond the leads to the gold bumps. Bonding can be gang bonding (all leads are bonded to the die simultaneously) or single-point bonding. For Sn plated leads, the leads can be gang soldered to the Au or Sn/Pb bumps. After inner lead bonding process is performed, both test and burn-in can be performed on the devices.

• *Outer lead bonding:* First, the die is cut from the tape with the leads protruding from the edge of the die. Then, the die is attached to the substrate either face up or face down. Next, the leads are soldered or bonded to the substrate metallization. Soldering can be used for both Sn and Au plated leads. Thermocompression and thermosonic bonding are used for bonding Au plated leads with Au substrate metallization.

The advantages of TAB technique is that it provides ability to test and burn-in devices prior to assembly, that is, it permits to test for Known Good Die, provides better electrical performance, and higher circuit density compared to wirebonding. The disadvantages of TAB is that it requires the additional process to bump the devices or the tapes and the specially designed tape for each die. Similar to wirebonding, TAB provides peripheral interconnect. Even though the area array interconnect can be achieved using multilayer TAB tape, the cost of this method is relatively expensive.

2.2.3 Flip Chip bonding

In Flip Chip bonding, solder bumps provide connections between bonding pads of the chips and the metallization on the substrates. Bumps can be formed either on the chips or on the substrates. The process starts with depositing under bump metallurgy (UBM) on the bonding pad of the wafers. UBM provides good adhesion between the bonding pads and the bumps, and serves as a diffusion barrier, a solder wettable layer, and an oxidation barrier. After UBM deposition, solder bumps are formed on the UBM. Eutectic lead/tin (Pb/Sn) alloy is by far the most used solder. There are various solder bump formation techniques. Most of the bumping techniques are used to form the bumps while the chips are still in the wafer form. Only some techniques are practical for bump formation on single chips. Solder bump structure, UBM deposition techniques, and solder bump formation techniques will be discussed in the next topic. After bumps are formed, the chips are diced and placed face down to the substrate. Mostly, flux is applied

either on the bumps or on the substrate prior to placing the chips onto the substrate. Flux helps keep the chips in place on the substrate and helps the reflow process. Next, solder bumps are reflowed to form the bonds between the bonding pads of the chips and the substrate metallization, and the flux residue is cleaned. The coefficient of thermal expansion (CTE) mismatch between the die and the substrate can result in solder fatigue and failure due to stress during thermal cycling. This problem can be solved with underfill process. In underfill process, liquid epoxy is dispensed along one or two sides of the die to fill the gab between the die and the substrate. Epoxy underfill helps spread the force and protect the solder bumps.

Advantages of Flip Chip bonding [5,6]

- Flip chip provides the highest packaging density.
  Flip chip is the only chip level bonding technique that offers area array interconnects. In area array interconnect, the entire device area can be used for I/O pads resulting in high packaging density without requiring fine pad pitch. Area array also optimizes signal propagation delay and power and ground distribution.
- Flip chip offers the best electrical and thermal performances.
  The parasitic inductance, capacitance, and resistance of solder bump are much less than those resulting from the wirebond process. The parasitic inductance of solder bump is less than 10% of a wirebond. The less parasitic components result in the shorter propagation delay time of signal and higher IC operating frequency.
- Low cost assembly
  Flip chip is the lowest cost assembly technique for high volume, high I/O density, and large die-size packaging.
- Good reliability

Disadvantages of Flip Chip

- Flip chip requires additional wafer processing to form solder bumps, limiting the available chips for this process.
- Flip chip is difficult to inspect since the devices are faced down.
- High cost for low volume and low I/O count packaging.

2.2.3.1 Trends of Flip Chip packaging [7]

Among the three chip-level bonding techniques, wirebonding is the dominant methods. However, with the trends of IC technologies to achieve higher I/O counts, higher performance and better functionality, flip chip will be used more aggressively while the use of wirebonding will be expected to decrease. Flip chip is likely to be the only technique that can meet the requirements of IC packaging in the future. Conventional peripheral interconnects are not expected to survive for high density packaging beyond the year 2000. Based on reasonable projection, processor devices in the year 2000 will require 50 μm pitch if peripheral wirebonding is used [6].

Flip chip is being developed for both interconnect in a package and for direct mounting on a substrate. Many companies are using flip chip bonding in their products. Most of the flip chip devices are in the packages since the industry infrastructure is not developed sufficiently for direct flip chip on board. Hence, the majority growth will be flip chip in packages such as ball grid array packages (BGAs) and chip scale packages (CSPs). There are a lot of companies involved in flip chip industry including, but is not limited, bumping service companies, flip chip bonder and equipment suppliers, underfill material suppliers, and test socket suppliers.

The market of flip chip is expanding and it is expected to be greater than 1.1 billion per year by the year 2000. Flip chip will be used in various products and electronic applications. The largest market for flip chip will be computer and related peripherals products such as mainframes, notebooks, and PC cards. These products are expected to share 36-38 percent of the total market. Automotive applications such as engine control modules and sensors will account for more than 25 percent of the market. Watch modules are expected to use 20 percent of flip chip devices. Telecommunication products such as portable phones, pagers, and switching modules will use 10-12 percent of flip chip devices. LCD will use flip chip devices to mount driver ICs to glass panel (chip-on-glass) and will count for 3-8 percent of the market. Military applications are expected to share less than one percent of the market.

2.3 Solder Bump Structure for Flip Chip Interconnect

Solder bump structure consists of the following,

- Under bump metallurgy (UBM)
- Solder bump

Figure 2.1 shows the solder bump structure.

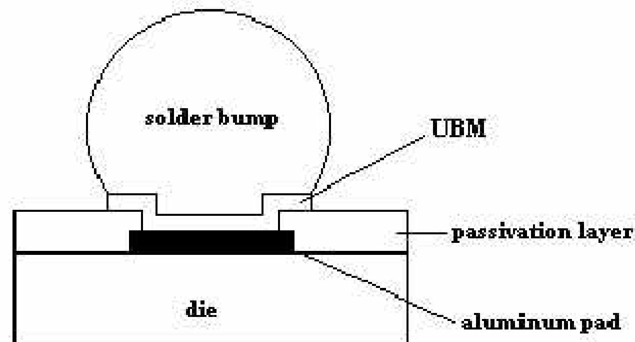


Figure 2.1 Solder bump structure[13].

2.3.1 Under bump metallurgy (UBM)

Solder cannot bond directly to aluminum. The UBM, the interface metals between aluminum pads and solder bumps, is required to provide adhesion, diffusion barrier, and solder wettable layers. UBM is a necessary structure to achieve reliable solder bump interconnects.

2.3.1.1 Requirements of UBM

UBM should have or provide the following capabilities [8],

- Good adhesion to bonding pad metallization and wafer passivation

  UBM must adhere well to both the bonding pad metallization and the passivation layer of wafers. Aluminum is common IC metallization. Typical passivation materials are nitride, oxide, and polyimide. It is important that the passivation layer is pin hole free since pin holes can cause damages to the IC circuit underneath during UBM

deposition process.

- Good ohmic contact to bonding pad metallization

  To achieve good ohmic contact, aluminum oxide on bonding pad surface has to be removed by back sputtering or chemical etching before UBM deposition.

- Solder diffusion barrier

  UBM must provide a diffusion barrier between the solder and the bonding pad Metallization.

- Solder wettable surface

  The final layer of UBM structure must be solder wettable. This is the layer that bond to the solder bump.

- Oxidation barrier

  To assure good solderibility, UBM must not oxidize during solder bump formation process.

- Minimum stress on silicon

  UBM structure must not cause excessive stress on the silicon underneath it. The excessive stress can cause the fracture and cratering of underlying silicon. Cratering of silicon is considered to be a reliability defect.

2.3.1.2 UBM structure

UBM are multilayer thin films. Typically, UBM consists of three layers [4,9,10,11,12].

- Adhesion and diffusion barrier layer.

  Function: Form strong bond with bonding pad metallization and IC passivation layer and prevent diffusion between bonding pad metallization and solder bumps.

  Typical metals used: Chromium (Cr), titanium (Ti), titanium/tungsten (Ti/W), nickel (Ni), palladium (Pd), and Molybdenum (Mo).

  Typical thickness: ~0.15-0.2 μm.

- Solder wettable layer

  Function: provide surface for solder bump to adhere to.

  Typical metals used: Copper (Cu), nickel (Ni) and palladium (Pd).

  Typical thickness: ~1-5 μm.

• Oxidation barrier layer

Function: prevent UBM structure from oxidation.

Typical metals used: Gold (Au).

Typical thickness: ~0.05-0.1 μm.

There are many possible combinations of thin film layers for UBM such as Ti/Cu/Au, Ti/Cu, Ti/Cu/Ni, TiW/Cu/Au, Cr/Cu/Au, Ni/Au, Ti/Ni/Pd, and Mo/Pd. However, the structure of UBM affects greatly the reliability of UBM itself. For example, it has been reported that Ti/Cu/Ni (electroless Ni) UBM has better adhesion strength than Ti/Cu UBM [12]. UBM structure also has effects on reliability of connections between UBM and bonding pad and between the UBM and the solder bumps. To achieve reliable connection between UBM and solder bumps, UBM must be compatible with the solder alloys used for solder bump. UBM suitable for high lead solders may not work well with high tin solders (eutectic solders). For example, Cu is a good solder wettable layer for high lead solder with 3-5% of tin, but it is not suitable for high tin solder since Sn react rapidly with Cu and form Sn-Cu intermetallic compound. If Cu is completely consumed, solder will dewet from the bond pads [8,9,10].

2.3.1.3 UBM deposition techniques

UBM can be deposited by sputtering, evaporation or electroless plating [5].

• *Sputtering:*

In this technique, thin film layers sequentially sputtered on the entire wafer. Next, photolithography process is performed to pattern the UBM. All UBM will be etched away except over the boding pads.

• *Evaporation:*

Thin film layers are successively evaporated on the entire wafer and patterned using photolithography process. The other method is evaporation with the use of a mask. In this method, the metal mask or photoresist is used to cover the entire wafer except the bond pads and UBM is selectively deposited on the opening area of the mask. The later method is suitable when solder bumps are formed by evaporation since both UBM and solder bumps can be formed using the same mask.

• *Electroless plating:*

Normally, electroless plating is used to deposit nickel UBM. Electroless nickel plating is a wet chemical and maskless process. Nickel is selectivelly formed on the aluminum pads. However, aluminum surface must be prepared before plating. Zincation is the common used process to pretreate aluminum. Electroless plating is a low cost process since it requires fewer processing steps and no patterning or vacuum facility is necessary. Electroless nickel plating process will be discussed in detail in a later topic.

2.3.2 Solder bump

The most common use solder for solder bump is lead/tin(Pb/Sn) alloy since it offers the fully reflowable solder bumps. The fully reflowable solder bump have the capability of self-alignment and collapse during reflow. Self alignment reduces the required accuracy for the process of placing the bare chips onto the substrate. Hence, no special placement machine is required. The collapse property reduces the non-planarity problem [8]. High Pb solders such as 95Pb/5Sn or 97Pb/3Sn have high reflow temperature (~330-350 °C). For applications that require low operating temperature such as flip chip on organic substrates, high Sn solders will be used. High Sn solders such as eutectic solder (37Pb/63Sn) have reflow temperature at ~200 °C [10]. However, since lead is toxic, lead-free solder alloy needs to be developed.

2.3.2.1 Solder bumping techniques

• ***Evaporation***

In evaporation process, a metal mask is used to pattern both UBM and solder bump deposition. First, UBM thin films are sequentially evaporated and deposited on the bond pads through the openings of the metal mask. Next, solder is evaporated and the bumps are formed on the bond pads. The deposited bumps have cone shape with the height about 100-125 μm. The bump height depends on the volume of evaporated solder which is a function of the distance between the metal mask and the wafer and the mask opening size. Since lead has higher vapor pressure than tin, lead deposits first, followed by tin. This results in the bump with Pb rich solder at the bottom and Sn rich solder on the top [5,13]. After the evaporation process is achieved, solder is reflowed to homogenize Pb-Sn

layer and to form the ball-shape bump. Figure 2.2 shows the process flow of solder evaporation using metal mask to pattern the UBM and the bumps. An alternative to evaporation using metal mask is lift-off process [4,14]. In lift-off process, photoresist is used instead of metal mask. Thick layer of photoresist is spin coated and patterned with opening on the bond pad area. Then, solder is evaporated and deposited on the bond pads and on the top of photoresist. The deposited solder on the bond pads and on the photoresist is not connected. Next, photoresist is stripped which will also lift off the deposited solder on the top.

• ***Printing***

First UBM is deposited and patterned. Then, solder paste is printed in the same way as conventional printing for thick film materials [5,13]. Both stencil and screen can be used. The volume and the height of the printed paste are determined by the opening size and the thickness of the stencil. Since the opening size of stencil is limited by the pad pitch, the stencil should be as thick as possible to increase the volume of printed paste. However, the higher thickness increases the wetted area of the stencil, thus increasing the chance that the solder will clog the stencil. Hence, it is important to select the proper stencil geometry[15]. After printing, the printed solder is reflowed to form the ball bumps and flux residues are cleaned. Figure 2.3 shows solder printing process flow.

• ***Electroplating***

In electroplating process [5,16,17], UBM is used as a seed layer for plating. First, UBM is deposited on the entire wafer. Then, thick photoresist is coated and patterned such that there are openings on the bond pad area. The photoresist determines the shape and the height of the plated bumps. Before electroplating, the photoresist residues on the openings are removed by plasma etching. The photoresist residues can reduce the adhesion of the bumps, increase contact resistance, and cause an inhomogeneous growth of the electroplated layers [18]. Next, the wafer is electroplated in a plating solution with the current applied and the wafer as the cathode. The plated solder has a mushroom shape. For electroplating, compared to other deposition processes, it is difficult to control the composition and the height of the plated bump [19]. After plating, photoresist is stripped. UBM is removed by wet etching using plated solder as etching resist, then,

solder is reflowed into ball shape. The other method is to reflow the plated bump first, and etch the UBM later. Figure 2.4 shows the process flow of electroplating.

• ***Stud or ball bumping***

Stud bumping uses the standard wirebonding process to form the bumps. Both gold wire and Pb based wire can be used. The process of stud bumping is the same as that of wire bonding. The only difference is that after the ball is formed at the tip of the wire and bonded to the bond pad, the wire is broken just above the ball as shown in Figure 2.5. UBM compatible with the wire used is required. After bumping, the bump can be reflowed into sphere or coined to get the flat surface with uniform bump height. Typically, stud bump is used with conductive adhesive (both isotropic and anisotropic conductive adhesive) or additional solder [5,20].

• ***Ball placement***

In this method, preformed solder balls are used to form the bumps. First, flux is applied on the bond pads. Then, solder balls are placed using special techniques and machines [21,22,23] and held in place on the pads by the tackiness of flux. Next, the balls are reflowed and bonded to UBM on the pads.

• ***Solder transfer***

In this process, solder bumps are formed on carriers, and then transferred to the bond pads [14,24]. Carriers must be the materials that are nonwettable with solder such as silicon wafer, heat-resistant glass sheet. First, the bumps are formed on the carrier using evaporation process. The bumps are formed such that the patterns of the bumps are exactly the same as those of the chip pads. Both metal mask and lift-off process can be used to pattern the carrier. A thin layer of gold about 1000 A° thick may be deposited prior to bump deposition. This gold layer is used to promote the adhesion between the solder and the carrier, thus help prevent separation of the solder from the carrier during processing and increase the time period before the solder is molten and separate from the carrier so that it has enough time to wet to the UBM on the chip pads. The next step is the transfer process. If the bumps are transferred to the wafer, the carrier will be singulated and placed on fluxed wafer. If the bumps are transferred to the individual die, the die will be placed on fluxed carrier. Then, the reflow process is performed and the bumps are dewetted from the carrier and bonded to the target pads. The carrier still sticks

to the bumps due to flux residue. Finally, the flux residues are cleaned and the carrier is separated. Figure 2.6 shows the solder transfer process flow.

Among these bumping techniques, the first three techniques can be used to form the bumps on wafer only, whereas the remaining techniques can be used for both the wafer and the single chip bumping.

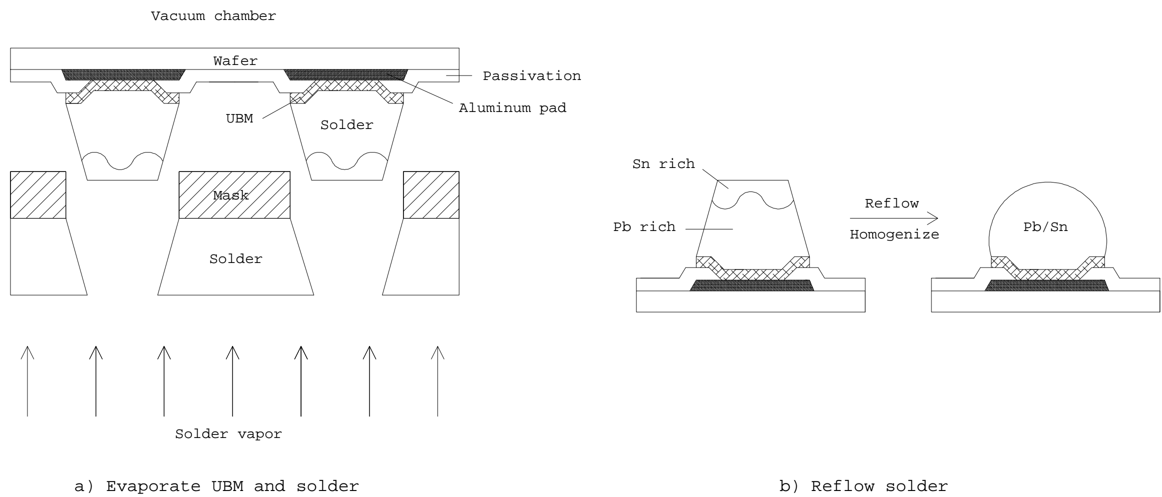


Figure 2.2 Solder evaporation process[5,13].

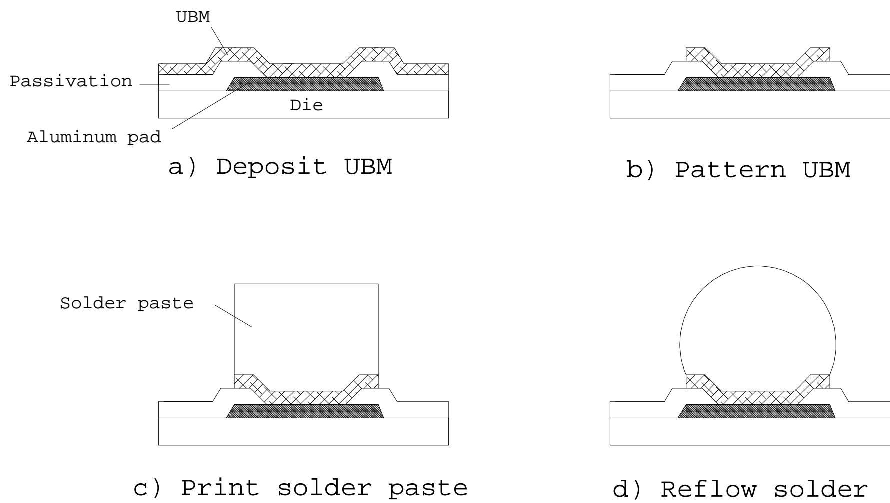


Figure 2.3 Solder printing process[5].

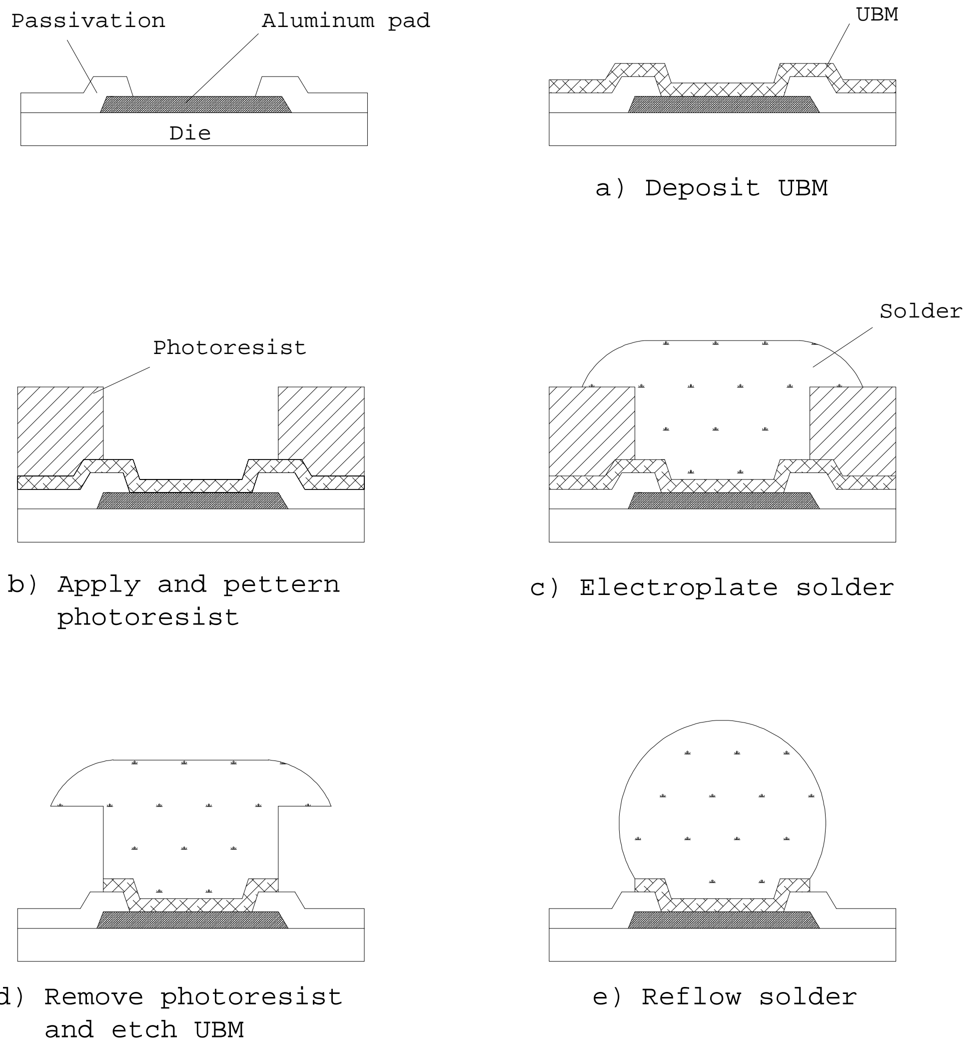


Figure 2.4 Solder electroplating process[5].

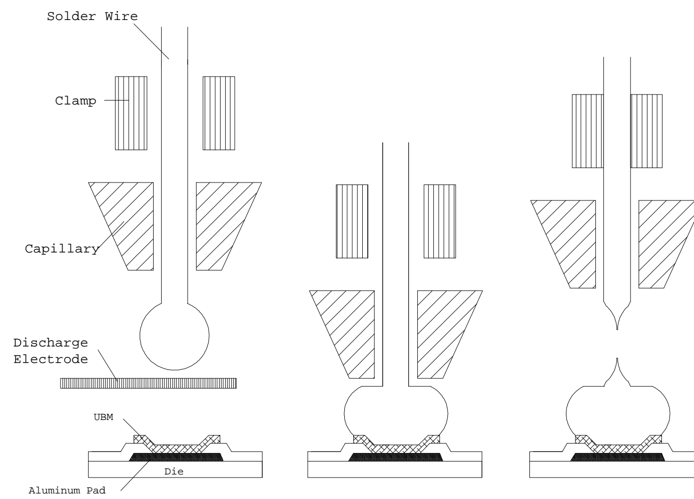


Figure 2.5 Stud bumping[13].

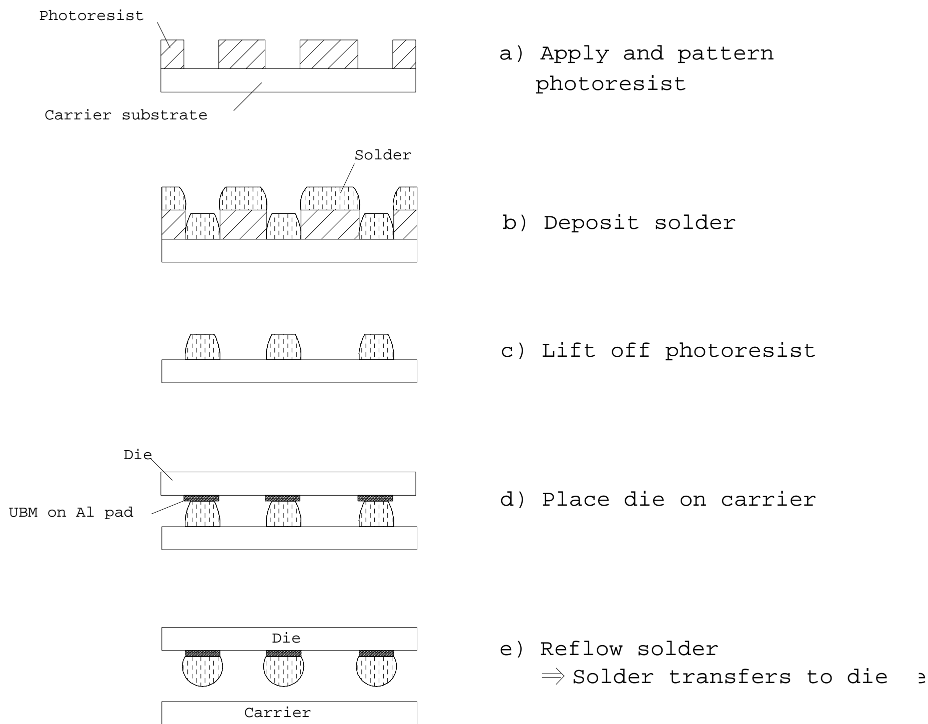


Figure 2.6 Solder transfer process[14].

2.4 Electroless Nickel UBM

Electroless nickel plating has been used for both UBM deposition and bump formation for flip chip applications [15,25,26]. For electroless nickel as the UBM, nickel provides adhesion /diffusion barrier layer and also solder wettable layer. Nickel has small diffusion rate and reaction rate with solder. Nickel also has slow reaction rate with tin, thus it is a suitable UBM for eutectic solder [10]. Amorphous electroless nickel has no grain boundary for diffusion path resulting in good diffusion barrier [11,12]. The height of nickel UBM is in the range of 1-15 μm. The UBM with 5 μm in height is recommended to provide good reliability with solder bumps. For electroless nickel as the bumps, typically electroless nickel bumps are used with conductive adhesive (both isotropic and anisotropic conductive adhesive). Electroless plating is an anisotropic deposition. Nickel grows in every direction at the same rate. As a result, the maximum bump height is limited by the pad spacing. The maximum bump height has to be less than half of the pad spacing distance. The normal bump height is on the order 15-40 μm.

After nickel plating, gold immersion is performed to coat a thin layer of gold about 0.05-0.1 μm on the nickel layer. Gold protects nickel from oxidation, thus keeps it solderable.

2.4.1 Techniques for electroless nickel plaiting on aluminum

Plating cannot be performed on aluminum without proper treatment since an aluminum oxide layer on aluminum surface prevents plated metal from sticking. The treatment process is required to remove aluminum oxide and prepare aluminum surface to be ready for the plating process. The most common aluminum treatment technique is zincation process [27,28]. Other available techniques are palladium (Pd) activation [29], nickel displacement, and direct nickel plating [30,31].

2.4.1.1 Zincation process

In this technique, zinc layer is deposited on aluminum surface to protect it from oxidation. The sequential processing steps are as follows,

• Cleaning step:

This step is to clean contaminants and light soils on the aluminum surface. Normally an alkaline cleaner is used for this purpose.

• Etching step:

This step is to remove micro constituents and oxide from the aluminum surface. A diluted acid ethcant such as sulphuric acid, nitric acid, or mixture of nitric-hydroflluoric acid is used.

• Zincating step:

This step is to deposit a thin layer of zinc on aluminum surface. Aluminum is dipped in zincate bath which is a strong alkaline solution typically composed of Zn(OH)2, NaOH and Fe, Cu or Ni to improve nucleation. During zincating, zinc is deposited on aluminum surface and at the same time, aluminum oxide as well as aluminum are etched. Zinc layer protects aluminum from re-oxidation. The thickness of zinc layer is small and depends on the compositions of zincate solution, condition of bath, temperature, time, alloys of aluminum. A thin and uniform zinc layer is required to achieve smooth and uniform electroless nickel layer. It has been shown that the first zincation produces a coarse and nonuniform zinc layer with large zinc particles (3-4 μm) surrounded with small particles (less than 1 μm). The nonuniform zinc layer results in rough electroless nickel in subsequent plating process [25]. This problem can be solved by using double zincate process. In this process, the zinc film from the first zincation is removed with diluted nitric acid. Then, the second zincation is performed. Double zincate process provides a thin and unifrom layer of zinc.

One disadvantage of zincation is that aluminum is etched in zincate solution. This problem is more critical for double zincate process where 0.3-0.4 μm of aluminum can be etched off. Hence, aluminum with thickness at least 1 μm is required for this process.

• Plating step:

After zincating, aluminum is immersed in electroless nickel plating solution which is an acidic solution of nickel sulfate with sodium hypophosphite or hydroboron as a reducing agent.

Before plating, the backside of the wafer must be covered with resist to protect nickel plating. Nickel can also grow on silicon. Hence, nickel with poor adhesion will plate on

the silicon which is not passivated such as on the scribe line. This poor adhered nickel may be lifted off causing shorts in fine pitch circuits.

2.4.1.2 Palladium activation process

In this process, aluminum is pretreated by palladium. First, aluminum is cleaned and etched to remove oxide using the same process as that for zincation technique. Aluminum is then immersed in palladium solution and palladium is selectively deposited on aluminum. Next, aluminum is immersed in electroless nickel plating bath.

2.4.1.3 Nickel displacement process

Nickel displacement which is the displacement between nickel ions in displacement plating bath and aluminum is used to pretreat aluminum. The process starts with cleaning and etching aluminum. Then, aluminum is dipped in displacement bath, followed by immerging in electroless nickel plating bath.

2.4.1.4 Direct nickel plating process

In this process, aluminum is cleaned and etched. Then, aluminum oxide is removed by activators. Activation process is performed with nitrogen purging. Then, aluminum is immersed in plating bath immediately after activation treatment.

2.5 Conclusions

Projections of high I/O counts and more advanced functionality for integrated circuit force the electronic packaging industry to seek for interconnect and assembly technologies to meet the future requirements of high density, and good electrical and thermal performance. Among available chip level interconnect technologies, Flip Chip interconnect is the only technology that can fulfill all the future needs of advanced packaging.

Flip Chip requires additional processes to form solder bumps on the bond pads of the chips. These additional processes include UBM deposition and solder bump

formation processes. The UBM is necessary to improve the reliability of the connection between the solder bumps and the bond pads. In the past few years, many UBM structures are developed to achieve better connection reliability. At the same time, several bumping techniques are innovated to be suitable for different electronic applications and to achieve lower processing cost, better yield, and better reliability. Most of the bumping techniques are developed for wafer-level bump formation. However, some of them can also be applied for chip-level bump formation.

Chapter 3 Flip Chip Assembly

3.1 Introduction

In Flip Chip packaging, after the solder bumps are formed on the chips, with various possible bumping techniques as discussed in Chapter 2, the bumped chips are passed through several processing steps before the Flip Chip bonding is complete. These processes include Flip Chip placement, reflow, cleaning, and underfill. Figure 3.1 shows the process steps after the wafer is bumped and cut into individual dice.

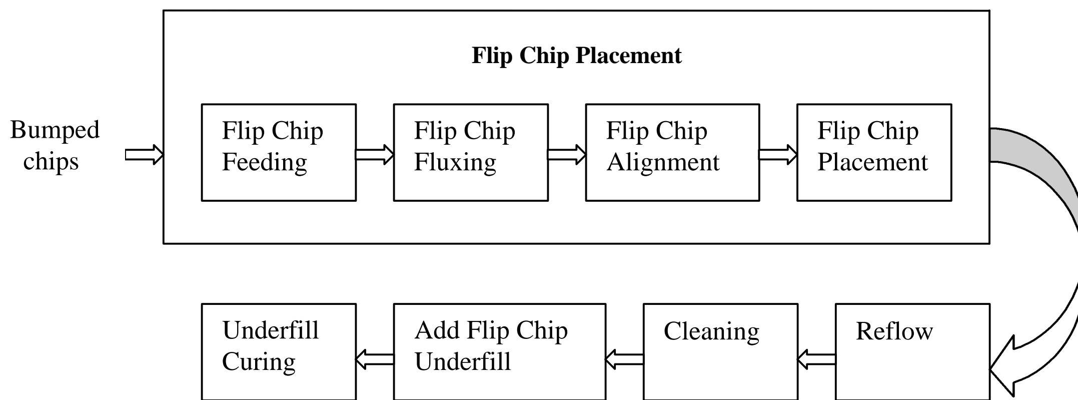


Figure 3.1 Flip Chip Process after bump formation and dicing [32].

This Chapter focuses on machines and procedures used in Flip Chip placement process including die feeding, fluxing, alignment, and die placement, solder reflow process, and underfill process including underfill dispensing and underfill curing.

3.2 Flip Chip Placement

In Flip Chip placement process, a special placement machine is used to perform each step including die feeding and pick-up, fluxing, alignment, and die placement, sequentially. The placement machine can be either fully automatic or semi-automatic.

The accuracy of the placement machine is very important. Currently, many applications are using Flip Chip bonding with the bump pitch of 6 mils to 10 mils. A rule of thumb for the accuracy of the placement machine is that the accuracy of the machine must be higher than 16 percent of the bump pitch. For example, if the bump pitch is 8 mils, the displacement of the machine should be less than 1.28 mils (32 μm) [32].

3.2.1 Fully automatic Flip Chip placement [32]

For this type of placement process, the machine performs all the work since the beginning of the process until the placement process is complete.

3.2.1.1 Die feeding and pick-up

In this step, the bumped chips are fed into the placement machine and the placement head, which is a vacuum nozzle, travels down to pick the chip, and travels back up. The bumped chips can be fed into the placement machine in several options including waffle trays, gel paks, tape-and-reel, and direct die feed from wafer. Both waffle trays and gel paks are suitable for low volume applications. These two formats arrange the chips in two-dimensional array and can contain from 25-400 chips per pack, depending on the chip size [4]. Waffle trays house the chips in a grid of small cells slightly larger than the chip size. The common sizes of waffle trays are 2"×2" and 4"×4". Figure 3.2 shows the picture of 2" × 2" waffle tray. After all chips are picked, the empty tray is removed and replaced with the fully loaded tray. Automatic feeders that can hold a stack of waffle trays can also be used to reduce the reloading time. The disadvantage of this feeding format is that the chips can move within the cells resulting in longer alignment time during the placement operation or miss picks. The die movement problem can be solved with the use of gel paks. For gel pak format, tacky gel is used to hold the chips in place. To release the chips from the gel, a vacuum is applied to the bottom of the gel pak. The vacuum pulls the gel against a fabric mesh, reducing contact area of the chips to the gel, and releasing the chips from the gel. For high volume assembly where component feeding time is critical, the tape-and-reel formats are preferred. The tape contains cavities into which the chips are placed. The bottom of the cavities is coated with a pressure sensitive adhesive. The tape is wound on a reel for automatic feeding and can

contain 5,000 or more dice [4]. An alternative feeding method for high volume assembly is the direct die feed from the wafer. This method can eliminate the cost of component taping in tape-and-reel formats. However, this feeding method is suitable only when the wafer yield is higher than 75 or 85 percent (75 percent for the assembly done at the wafer fabrication site, and 85 percent for the assembly done at another site) [33]. In the feeding process, the direct die feeder is used to pick the die which is mounted on a plastic sheet coated with a pressure sensitive adhesive. The feeder machine has the ability to distinguish between good dice and bad dice by detecting ink dots and can also support a wafer-mapping file that supplies coordinates of good dice.

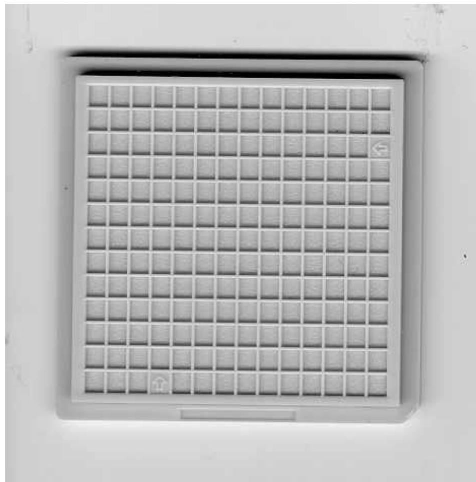


Figure 3.2 A 2”×2” waffle tray.

3.2.1.2 Fluxing

The fluxing step is necessary for the Flip Chip placement since flux helps hold the die in place on the substrate prior to the reflow process and helps solder to wet the bond pads on the substrate. There are two ways to apply the flux; dip fluxing which apply the flux onto the bumped die, and dispensing which apply the flux onto the substrate.

• *Dip fluxing*

In this method, a flux station is located inside the placement machine. The flux is prepared on a planar surface using a doctor blade to spread and level the flux. The typical thickness of the flux film is on the order 20-60 mm. The required thickness can

be achieved by adjusting the level of the doctor blade. In the fluxing process, the die with bumps faced down is dipped into the flux film and is pulled up after a short period of time. Dip fluxing is an additional step in the placement process, resulting in longer processing time. Hence, this method is not suitable for high volume applications.

• *Dispensing*

Dispensing method is used in high volume applications since in this method, there is no additional fluxing step in the placement process. This process is achieved using a dispenser to apply the controlled volume of flux onto the chip sites on the substrate prior to the substrate entrance to the placement machine.

3.2.1.3 Alignment

For the fully-automatic placement machine, the proper combination of illumination, optics, and vision algorithms is necessary for accurate alignment. Software algorithms are used to recognize the bump patterns and determine the center of the bumps. The sufficient contrast between the bumps and the die passivation or background layer is an important factor to get the proper recognition. The required contrast can be achieved by side lighting the chip with the lighting angle of 7° to 10° instead of lighting beneath the chip. Also, the resolution of the recognized image must have sufficiently high solution to achieve proper alignment. Three pixels are required on and between each bump to properly align the chip.

3.2.1.4 Die placement

After alignment, the die is placed onto the substrate using machine positioning systems. A low friction, linear motor-driven machine is the most common positioning system for the placement machine. The placement machine with this positioning system meets the accuracy, repeatability, and cleanliness requirements of Flip Chip assembly (The generated contaminants can be as few as 558 particles per cubic meter). Another type of positioning system is a lead screw shaft with belt drive. However, the limited pitch for this type of machine is 200 μm and the generated contaminants are between 15,000 to 20,000 particles per cubic meter [33].

During placement, due to the die fragility, depending on the die thickness, it is important to control the speed at which the die contacts the substrate to prevent damaging the die. After the die is placed on the substrate, force is applied by placement head before the head moves back up. The applied force must be controlled such that the force is sufficient to ensure the contact between all the bumps and the substrate bond pads without deforming the bumps or damaging the die. Normally, the applied force ranges from 4 to 10 g per bump, depending on the number of bumps per die.

3.2.2 Semi-automatic Flip Chip placement [34]

In this type of placement process, the machine is semi-automatic. An operator performs some parts of the processing step such as moving workstages to the position under the placement head, alignment, and initiating work cycles. One sample of semi-automatic placement machine is the table top Flip Chip placement system-model 850 (Figure 3.3) from Semiconductor Equipment Corporation. The accuracy of this machine is within 24 μm and the throughput is up to 200 placements per hour [35].

Figure 3.3 a) The table top Flip Chip placement system-Model 850 (from Semiconductor Equipment Corporation).

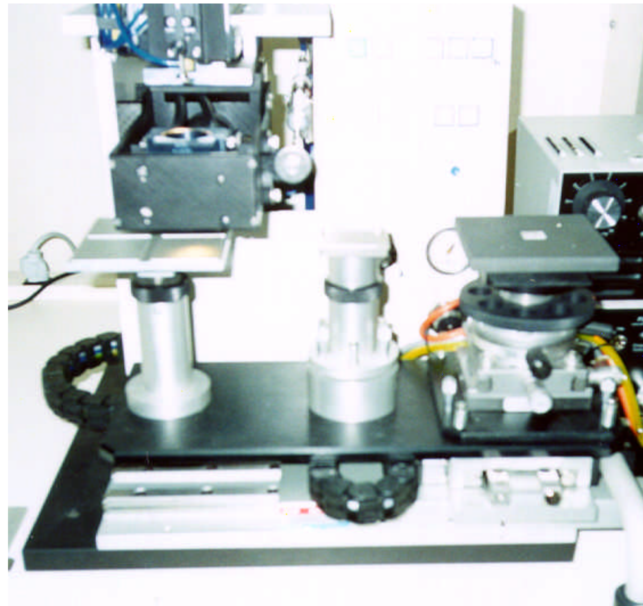


Figure 3.3 b) Three workstages of the placement machines: pick-up stage (left most), flux Stage (middle), and placement stage (right most).

3.2.2.1 Die feeding and pick-up

The bumped die can be fed to the placement machine in several formats. The most common format is waffle tray with the bumped die faced down to the bottom of the tray. In the case that the bumped die faced up is required, an additional tool called inverter is used. The inverter picks up the die, turns it over, and passes it off to the placement machine. In the pick-up step, the operator places the waffle tray on the pick-up stage of the placement machine. Figure 3.4 shows the 4” × 4” pick-up stage. This stage can hold four 2” × 2”-waffle trays or one 4” × 4”-waffle tray. Next, the operator moves the pick-up stage to stay under the placement head and adjust the stage position such that the center of the target die is in the position of the placement head. After adjusting the stage position, the operator initiates the pick-up cycle. In the pick-up cycle, the placement head travels down to the stage, picks up the target chip with vacuum, and travels back up.

Figure 3.4 The 4”×4” pick-up stage.

3.2.2.2 Fluxing

The dip fluxing method is used. First, the flux film is prepared on the flux stage. The operator places a small amount of flux on the flux stage and uses manual doctor blade to spread and level the flux. The flux stage and the doctor blade are shown in Figure 3.5. Next, the operator moves the prepared flux stage to the position under the placement head and initiates the fluxing cycle. In the fluxing cycle, the placement head travels down to the flux stage, dips the chip into the flux film with a slight pause, and travels back up without releasing the chip. In the dipping step, the proper thickness of the flux film is important. If the flux film is too thick, when the chip is dipped into the flux, it may adhere to the flux and may be pulled off of the placement head.

Figure 3.5 The flux stage and doctor blade.

3.2.2.3 Alignment

Alignment of the bumped die and the substrate can be achieved using a cube beam splitter, a color camera with zoom lens, and a color monitor to present the real-time images of the bumps and the substrate bond pads superimposed on each other. The separate, adjustable illuminators are used to provide sufficient lighting for both the die and the substrate. To begin the alignment operation, the operator places the substrate on the placement stage. Next, the operator moves the placement stage into the position under the placement head and carefully adjusts the position of the stage until the bumps and the substrate bond pads are perfectly aligned.

3.2.2.4 Die placement

After alignment, the operator initiates the placement cycle. In this cycle, the placement head travels down to the substrate and places the die onto the die site of the substrate with force applied by the placement head. The head remains in this down position for a set amount of time before it travels back up. The amount of applied force and time are set before the placement cycle starts. To ensure good reflow, the applied force must be sufficient to make all bumps touch the substrate bond pads.

3.3 Solder Reflow

After Flip Chip placement process is finished, the solder reflow process is performed. Reflow temperatures vary with the bump metallurgy. Typically, soldering is performed at 30 °C to 40 °C above the solder melting point [36]. Pure lead (Pb) melts at 327 °C, while pure tin (Sn) melts at 232 °C. The melting point of lead/tin solder alloy depends on the ratio of lead to tin of that particular alloy. For example, 95Pb/5Sn melts at 315 °C, and 63Sn/37Pb melts at 183 °C [37]. The reflow temperatures of 95Pb/5Sn and 63Sn/37Pb are 350 °C and 230 °C, respectively.

Several reflow systems are compatible for Flip Chip reflow process, including forced convection, hot plate, and other reflow systems for low volume Flip Chip assembly [38].

3.3.1 Forced convection reflow system

Forced convection is the most commonly used reflow system. This system provides the best heat distribution for reflow process. Heat is supplied by moving hot air or nitrogen. Forced convection reflow machines can be as simple as batch convection ovens, or as sophisticated as in-line convection ovens with computer control. Normally, the machines consist of heating zones which are typically sealed to support the reflow process in nitrogen atmosphere if required, and cooling zones to quickly solidify the solder after reflow. Each zone is separated by air or nitrogen curtain so that adjacent zones can be operated at different temperature. Typically, the Flip Chip components are carried through the machine by a stainless steel flexible belt allowing the hot air or nitrogen to pass freely.

3.3.2 Hot plate reflow system

Hot plate is one of the simplest reflow systems. However, the temperature is not as even as that of forced convection system. The reflow machines consist of a series of hot plates. Temperature of each plate can be adjusted separately. During the reflow process, the components are moved at controlled speeds over the hot plates set at the appropriate temperatures. Heat is transferred by conduction through the substrate to the solder on the top surface. Hence, the substrate must have high enough thermal conductivity and must be able to withstand high temperature. This requirement limits some types of substrates that can be used with the hot plate system.

The hot plate system can be combined with the convection system to form bottom-up conduction and top-down convection heating system which provides better heat distribution. The temperature of the bottom conduction plate and the upper convection plate in each heating zone can be individually controlled.

3.3.3 Reflow systems for low volume Flip Chip assembly [34]

For low volume applications, the reflow process can be achieved on the Flip Chip placement machine with hot gas reflow system. Normally, in soldering process, this reflow system is used for repair and rework. In the Flip Chip reflow process, after the bumped chips are placed onto the substrate, the substrate is moved to the reflow position

of the placement machine. Then, the hot gas is blown through the heating nozzle onto the chips. This system can reflow only a few chips at a time. The reflow time is controlled, and the hot gas is shut off after the solder is reflowed.

Hot gas cannot be used to reflow small, lightweight chips since the velocity of the hot gas is too high for the lightweight chips. In this case, either a Xenon lamp system with the visible light being delivered through a fiber optic bundle or an infrared laser system is used [34].

3.4 Flip Chip Underfill

Underfill process is the process to fill encapsulating material which is epoxy into the space between the die and the substrate. Underfill process is necessary to improve the long-term reliability of mounted Flip Chip devices. A Flip Chip package with properly dispensed and cured underfill results in 30-50 time improvement in solder fatigue life compared to an unencapsulated package [39]. Figure 3.6 illustrates the cross section of an underfilled Flip Chip.

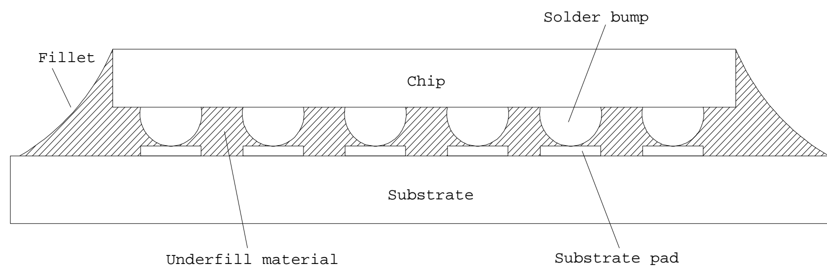


Figure 3.6 Cross section of an underfilled Flip Chip.

3.4.1 Functions of underfill

The main function of underfill is to relieve the Coefficient of Thermal Expansion (CTE) mismatch between the semiconductor die and the substrate to which it is attached.

The CTE mismatch between the die and the substrate results in stress on the solder joint during thermal cycling and power cycling in normal operation. This stress leads to solder fatigue and failure. The CTE mismatch problem is more severe for Flip Chip on organic substrate since the CTE of the organic substrate such as FR4 (15.8 ppm/°C) is much greater than that of Si (2.6 ppm/°C). The problem of fatigue and failure also increases with increasing the die size which is the trend of IC industry. The CTE mismatch problem can be solved by underfill process. The underfill helps spread localized stress uniformly over the encapsulating material, preventing the forces generated by the CTE mismatch from shearing the solder bumps.

Other functions of underfill are to prevent of solder creep and to increase the stiffness of the Flip Chip package [39]. Since solder creeps under stress, it will move laterally into any available space. By completely surrounding each solder joint with epoxy, there is no space for the bumps to move. Therefore, the shape of the bump is maintained and the risk of solder creep is reduced. Also, the cured underfill increases the stiffness of the package, thus limits the potential for bending of the package which can lead to broken interconnects and/or crack of the die.

3.4.2 Underfill process

Underfill process can be performed at two points in the Flip Chip assembly process; after die placement and before die placement [40].

3.4.2.1 Underfill after die placement

This underfill process is performed at the last step in the Flip Chip assembly process. After die placement, solder reflow, and cleaning processes are finished, a needle is used to dispense a controlled amount of epoxy along one or more sides of the chip perimeter. Epoxy may be loaded with fillers such as ceramic fillers to improve the thermal conductivity and adjust the CTE of the epoxy. Epoxy flows into the gab between the die and the substrate by capillary action and surrounds the bumps as it moves. Once the underside of the chip is completely filled, the epoxy will continue to flow and will form a fillet around the perimeter of the chip (flow-out). The fillet serves as underfill reservoir which helps compensate for normal variations in the volume of space to be

filled between the die and the substrate, and reduce the stress concentration. After dispensing, the epoxy is cured. The goal of the curing process is to develop epoxy to its optimum mechanical, electrical, and environmental properties with the shortest curing time.

The important parameters for this underfill process include dispense volume, dispensing pattern, and dispensing temperature.

• *Dispense volume*

In underfill process, it is important to calculate the amount of epoxy to be dispensed. The improper amount of epoxy may result in incomplete underfill (some solder bumps are not protected) or excess underfill. Incomplete underfill may lead to die crack and excess underfill may flow into area on the substrate where it can damage other circuit features. The dispense volume of epoxy depends on the volume of the space to be filled, and the volume of the fillet around the die. The volume of the space is the volume of the gab between the die and the substrate minus the volume of the solder bumps.

The accuracy of dispense volume depends on the accuracy of the pump used to move the epoxy into the dispensing needle. The most accurate pump for underfill dispensing is the linear positive displacement pump (LPDP) [40].

• *Dispensing pattern*

The dispensing pattern affects greatly the possibility of air bubble trapping which will become voids in the cured underfill. The best way to avoid the trapping of bubbles is to dispense underfill along a single side of the die. However, this dispensing pattern results in the longest underfill time due to the long travel distance of underfill. The solution for shorter underfill time and low possibility of trapping is to dispense epoxy along one entire side and part of an adjacent side known as L-pass [40].

• *Dispensing temperature*

The dispensing machine must have a thermal management system to control temperature in each dispensing step, including preheating before dispensing, temperature profile during dispensing, and post-heating. Since the flow speed of epoxy depends on temperature of the substrate, before the dispensing process starts, the substrate must be preheated to the optimal flow temperature of underfill. The dispensing needle should also

have heating feature to assist the flow characteristics of the epoxy. The post-heating temperature profile is important for completion of epoxy flow-out.

Disadvantage of underfill process after die placement is that the underfill dispensing time and underfill curing time are time consuming process. This process appears to be a major bottleneck in Flip Chip assembly, resulting in low throughput and high cost of the overall Flip Chip packages. Dispensing process is time consuming since underfill dispensing with the needle is a point-to-point process (dispense onto one chip site at a time), and the capillary flow process of underfill into the gap is very slow.

3.4.2.2 Underfill process before die placement

This process can overcome the problem of long dispensing and curing time of the previous process, resulting in higher throughput and lower cost for Flip Chip assembly [41].

In this process, a special underfill material that can serve as both a flux for reflow soldering and an underfill is used. Before the die is placed onto the substrate, underfill material with a fluxing agent is applied onto the chip sites of the substrate. Either point-to-point or area-oriented dispensing process can be used. The point-to-point process uses dispensing needle, similar to that used in the previous underfill process, to apply the underfill onto the chip site, one site at a time. The area-oriented process uses stencil printing to apply the underfill material onto the substrate, thus the underfill is applied to all chip sites at the same time. After the underfill is applied, the chips are placed onto the substrate and the bumps are forced into the underfill, making contact with the substrate metallization. Next, the reflow process is performed. At this step, both solder reflow and underfill curing are accomplished simultaneously.

With this process, the dispensing time and the curing time are significantly reduced since the underfill can be applied to all chip sites at the same time, the slow capillary flow process of underfill is eliminated, and the curing step occurs at the same time as the reflow step.

3.5 Conclusions

Flip Chip assembly for the bumped chips consists of several processing steps, including Flip Chip placement, solder reflow, cleaning, and underfill, respectively. The reliability of each step depends mostly on the capabilities of machines and the efficiency of processing procedures being used. The processing machines can be as simple as the manual machines for low volume Flip Chip assembly or as sophisticated as the fully automatic machines for high volume assembly. The development of processing machines and procedures to obtain better results in each step is very important to achieve better reliability, higher throughput, and lower cost of the overall Flip Chip assembly.

Chapter 4 UBM Formation Technique for Single Die/Dice

4.1 Introduction

This chapter presents a technique developed in this thesis for UBM deposition on aluminum pads of single die/dice. The developed technique consists of two major processes; temporary die attach process and UBM deposition process. The purpose of the former process is to temporarily attach the bare die to a substrate so that the UBM deposition process can be performed on these dice. This process is developed using thermoplastic adhesive as a die attach material. The later process entails the deposition of the UBM layer on aluminum pads of the die using electroless nickel plating, followed by gold immersion.

The first part of this chapter discusses the UBM deposition process and the second part discusses the temporary die attach process. The processing and experimental procedures as well as the experimental results and analysis results are also discussed in details.

4.2 UBM Deposition Process

4.2.1 Concept

Among the two major processes of this work, UBM deposition technique was developed first. This is attributed to the fact that conditions required in UBM deposition process are necessary for developing temporary die attach process. Electroless nickel plating, followed by gold immersion, was selected in this work since it is a maskless process which makes it very suitable for UBM deposition on a single die. This process also provides a good surface for Flip Chip soldering without requiring any expensive nor additional facilities. In this UBM structure, nickel provides adhesion/diffusion barrier layer and solder wettable layer. Nickel serves a good diffusion barrier since it has a low diffusion rate and a low reaction rate with solder. Nickel also has slow reaction rate with

tin, thus making it a suitable UBM for eutectic solder. On the other hand, gold provides oxidation barrier layer.

The UBM deposition process consists of three steps; double zincation, electroless nickel plating, and gold immersion, respectively. Among these three processes, the first process and the last process are immersion deposition, whereas the second process is electroless deposition [42].

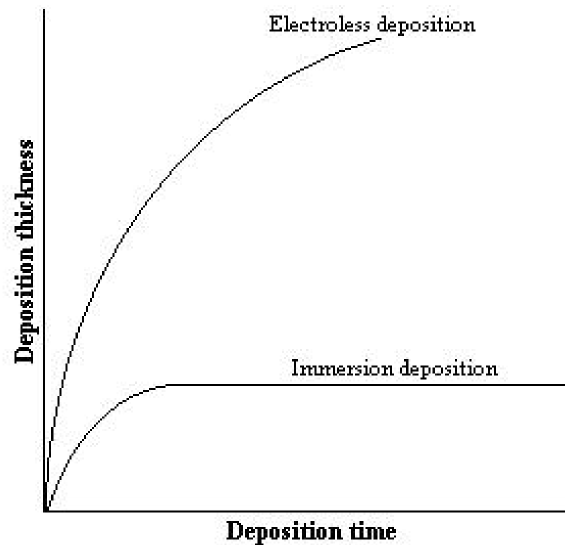


Figure 4.1 Thickness vs. time - comparison between electroless and immersion deposition [42].

• The immersion deposition:

The immersion deposition is the process of metal displacement reaction where the target metal atoms dissolve and, at the same time, are displaced by the deposit metal atoms in the plating solution. The displacement continues until the deposit metal covers the entire target surface. After the entire surface is covered, the reaction stops. The immersion deposition produces deposit metal layer with limited thickness on the order of a few microns.

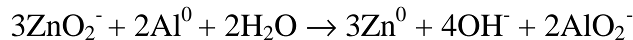
• The electroless deposition:

The electroless deposition is caused by the selective reduction reaction of the metal ions in the plating solution at the surface of the catalytic target metal. The deposition process

is conducted through the autocatalytic action resulting in continued deposition of the plating metal on the target surface. Ideally, the thickness of deposit metal increases indefinitely with deposition time. The electroless plating solution requires a reducing agent. This constituent is not required in the immersion solution. Figure 4.1 illustrates the relation of the deposit thickness and the deposit time comparison between the electroless deposition process and the immersion deposition process.

4.2.1.1 Zincation

Since aluminum oxide on aluminum surface prevents metal being plated from sticking, pretreatment process is required prior to plating to prepare clean aluminum surface and to ensure good adhesion of the plated metal to aluminum. Zincation is the most common technique to pretreat aluminum surface. A zincate bath is an alkaline solution basically composed of zinc oxide (50 to 100 g/L) and sodium hydroxide (NaOH) (250 to 500 g/L). In the zinc bath, aluminum oxide is removed and the zinc layer is formed on the aluminum surface by the displacement between aluminum atoms and zinc atoms in the zincate solution. The reaction can be presented as follows,



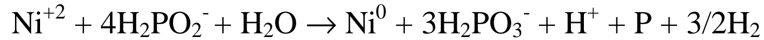
$$3ZnO_2^- + 2Al^0 + 2H_2O \rightarrow 3Zn^0 + 4OH^- + 2AlO_2^-$$

The zinc layer protects aluminum from re-oxidation and keeps the surface readiness for plating. The zinc layer will be etched away in the nickel plating bath and the plating proceeds on the clean aluminum surface.

4.2.1.2 Electroless nickel plating

Electroless nickel plating solutions can be either acid or alkaline solutions. However, most of commercial electroless nickel plating solutions are acid plating baths operated in the PH ranging from 4.5-6.0. The most common nickel source in nickel plating bath is nickel sulfate ($NiSO_4$). Other nickel sources, such as nickel chloride and nickel acetate, are used for very limited applications. Another important component in the nickel plating solution is a reducing agent. Reducing agent is the chemical that helps to conduct reduction reaction of nickel ions in the solution. The reducing agent can be sodium hypophosphite ($NaH_2PO_2 \cdot H_2O$), sodium borohydride ($NaBH_4$), dimethylamine borane ($(CH_3)_2NHBH_3$), or hydrazine ($N_2H_4 \cdot H_2O$). Nickel deposition reaction of the

plating bath with nickel sulfate as a nickel source and sodium hypophosphite as a reducing agent can be represented with the following equation,



$$Ni^{+2} + 4H_2PO_2^- + H_2O \rightarrow Ni^0 + 3H_2PO_3^- + H^+ + P + 3/2H_2$$

It can be seen from the equation that the reaction yields nickel and phosphorus.

4.2.2 Process flow and results

The UBM deposition experiments were performed mostly on test chips with eight 4 mil × 4 mil aluminum pads and six 4 mil × 5 mil aluminum pads. The size of the test chips was 1.28 mm × 1.28 mm. Some experiments were performed on diode dice and power FET dice. Figure 4.2 shows SEM photograph of a 4 mil × 4 mil aluminum pad of the test chip. The scratch mark in the center of the pad was caused by probing performed by the manufacturer of the test chip. This scratch mark existed on every pad of the test chips. Figure 4.3 shows EDX analysis result of the pad illustrated in Figure 4.2. The analysis result confirms that the metal on the pad is aluminum or aluminum alloy.

In these experiments, the test die was permanently attached to a 1" × 1" ceramic substrate using epoxy adhesive. In the final process, this step was replaced by temporary die attach process using thermoplastic adhesive film. The adhesive holds the die and also protects the die backside from the immersion and electroless plating solution during the deposition process.

A Scanning Electron Microscope (SEM) and an Energy Dispersive X-ray (EDX) detector were the tools used in this work to verify and validate the process. The SEM was used to observe the results of each process, and the EDX detector was used to analyze elemental compositions of the results. EDX analysis in this work was performed using spot mode which means the detector analyzed at the target spot only and the analysis results show elemental compositions of the target spot. EDX detector can analyze the material up to the depth to which the primary electrons penetrate (1-5 µm). Hence, EDX detector is not strictly a surface analysis tool [43]. In addition, EDX detector cannot detect oxide, nitride, and carbon.

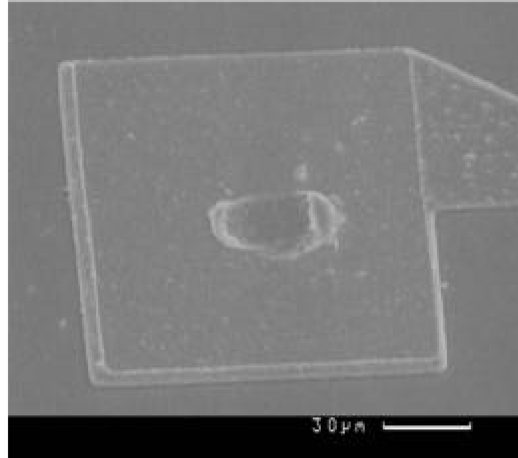


Figure 4.2 SEM photograph of a 4 mil × 4 mil aluminum pad of the test die.

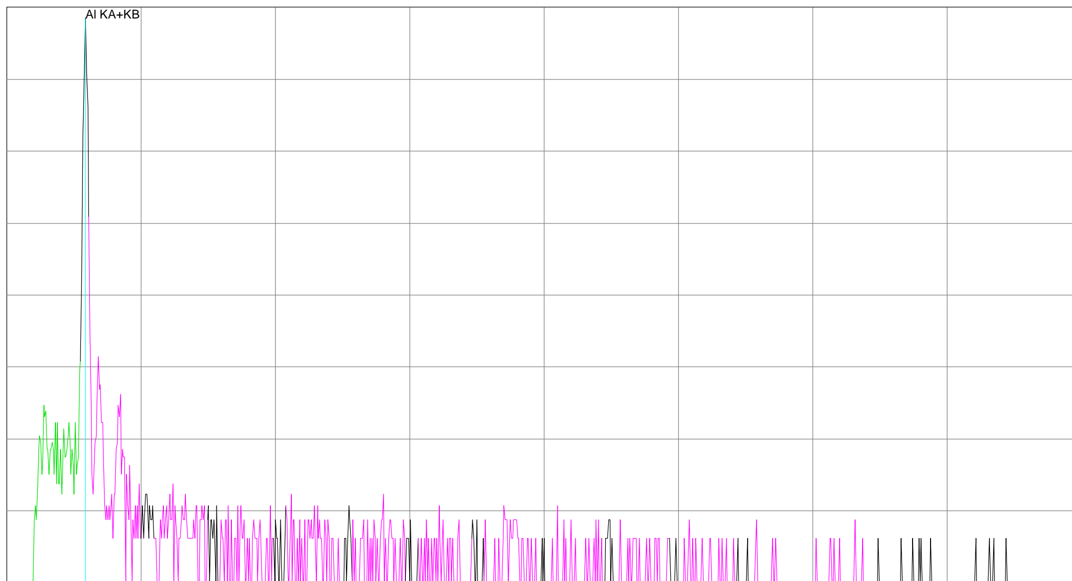


Figure 4.3 EDX analysis of an aluminum pad of the test die.

4.2.2.1 Double zincate process

A) *Process flow*

In the zincate process, a commercial zincate solution was used. The zinc solution was an alkaline solution with PH of 12. The zincate process steps were as follows,

1) Cleaning step.

Purpose: to clean organic contaminants and light soils on the aluminum surface.

Procedure: dip the die in mild alkaline cleaning solution based on sodium hydroxide (NaOH) at room temperature for 30 seconds.

2) DI water rinse.
3) Etching step.

Purpose: to remove aluminum oxide and alloying elements on aluminum surface. This step provides a uniform aluminum-rich surface for plating.

Procedure: dip the die in 50% v/v nitric acid (HNO_3) at room temperature for 5 seconds.

4) DI water rinse.
5) First zincation.

Purpose: to deposit the first zinc layer.

Procedure: dip the die in zincate solution at room temperature for 30 seconds.

6) DI water rinse.
7) Etching step.

Purpose: to strip off the first zinc layer.

Procedure: dip the die in 50% nitric acid at room temperature for 5 seconds.

8) DI water rinse.
9) Second zincation.

Purpose: to deposit the second zinc layer.

Procedure: dip the die in zincate solution at room temperature for 30 seconds.

10) DI water rinse.

After the zincate process, the die was observed with SEM and analyzed with EDX detector.

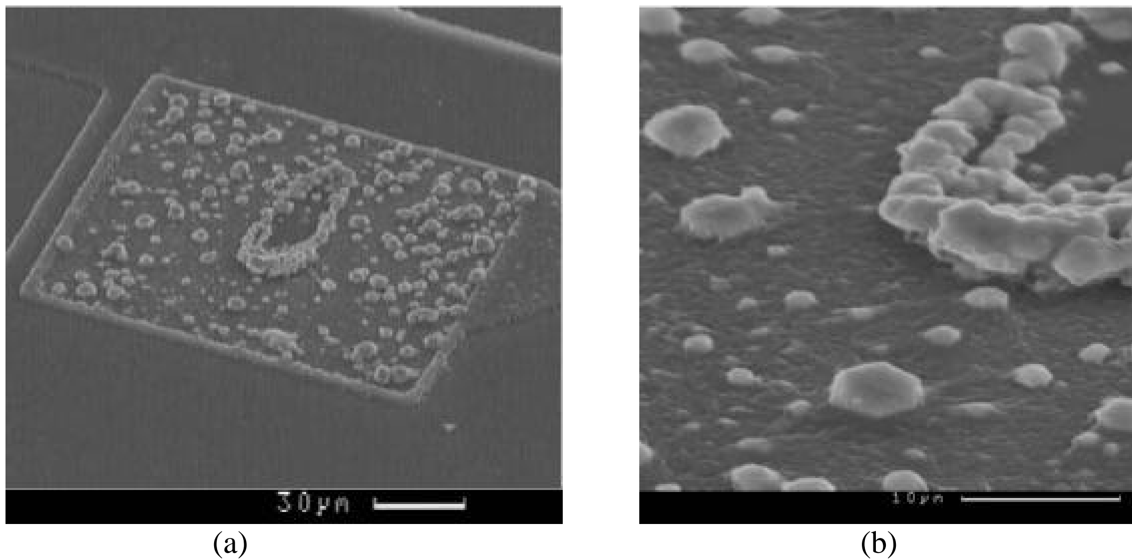
B) Results and discussions

From observation of the SEM micrographs, the first zincation (single zincation) produces a coarse and nonuniform zinc layer, as shown in Figure 4.4. It can be seen from Figure 4.4b that the zinc layer consists of zinc particles with the sizes ranging from less than 1 μm to 4μm. This nonuniform zinc layer results in rough electroless nickel layer in the subsequent plating process, as shown in Figure 4.5. This problem can be solved by double zincate process where the zinc film from the first zincation are removed with

diluted nitric acid, followed by the second zincation. Double zincate process provides a very thin and uniform layer of zinc with the thickness on the order of a few thousand angstroms [19]. Figure 4.6 shows an aluminum pad after double zincate process.

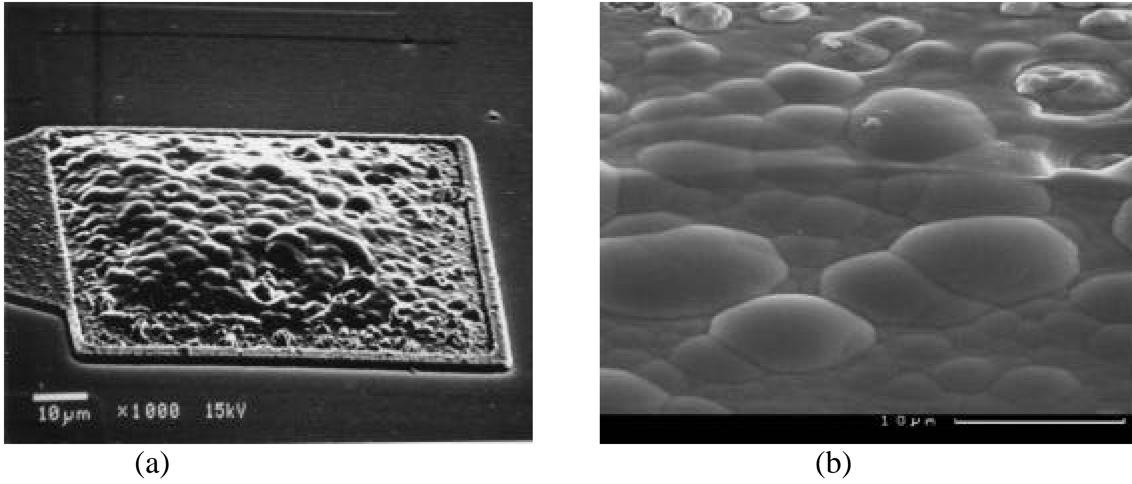
Figure 4.7 illustrates the EDX analysis result of a large zinc particle on the aluminum pad after the first zincation. The result shows zinc, aluminum, and silicon peaks. Figure 4.8 illustrates the EDX analysis result of the aluminum pad after the second zincation. The result does not show any zinc peak. The unexistence of the zinc component in the analysis result after the second zincation is likely to result from the fact that the second zinc layer is very thin and is too thin to be detected with EDX analysis.

In addition, the analysis results of aluminum pads both after the first zincation and after the second zincation show the silicon peak which does not exist in the analysis result of the aluminum pad before zincation (Figure 4.3). The reason of this effect seems to be contributed to some aluminum (can be as much as 0.3-0.4 μm) [27] is etched away during the zincate process resulting in a thinner aluminum layer on the pad. Hence, silicon under the aluminum pad is also detected with EDX detector.



(a) (b)

Figure 4.4 SEM photograph of an aluminum pad after the first zincation.



(a) (b)

Figure 4.5 SEM photograph of an aluminum pad after electroless Ni plating with single zincation treatment.

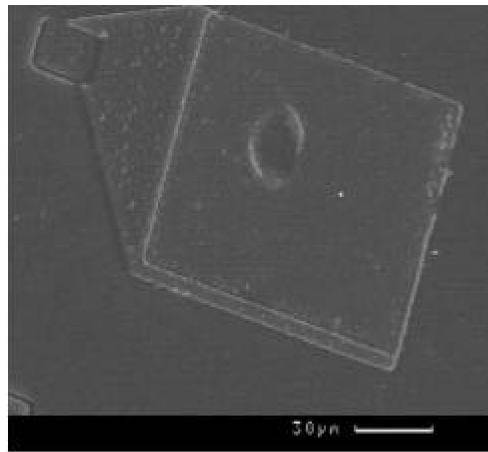


Figure 4.6 SEM photograph of an aluminum pad after the second zincation.

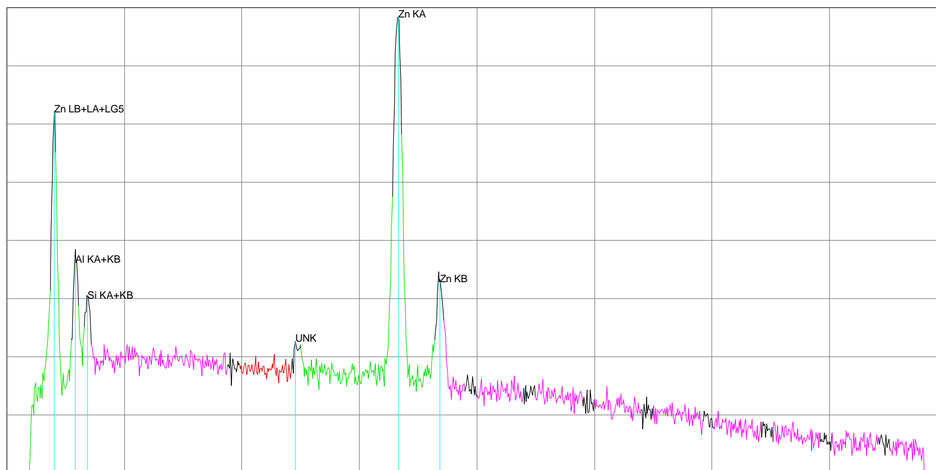


Figure 4.7 EDX analysis of a large zinc particle from the first zincation.

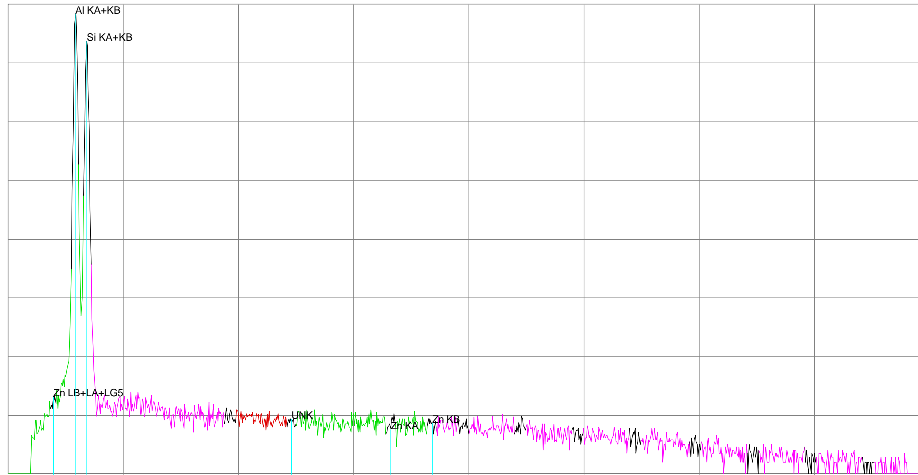


Figure 4.8 EDX analysis of zinc layer after the second zincation.

4.2.2.2 Electroless nickel plating process

A) Process flow

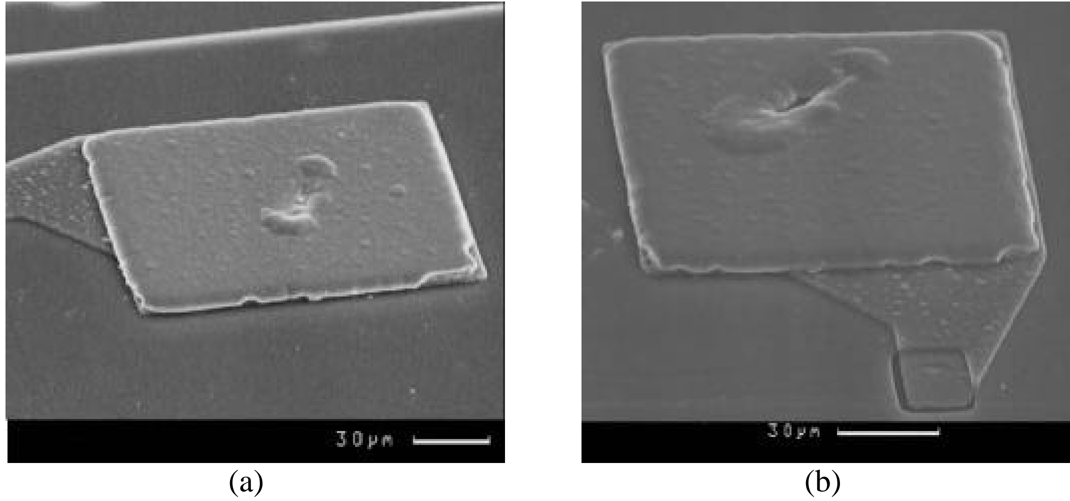
After double zincation, the die was ready for plating. A commercial electroless nickel plating solution with nickel sulfate as a nickel source and sodium hypophosphite as a reducing agent was used. The deposition rate of this plating solution was about 0.8 mils/hour (1 μm/ 3 minutes). The required thickness of the nickel layer for UBM structure in this work was on the order 5 μm. The plating was operated at 191 °F (88 °C) and PH of 5 for 15 minutes. After plating, the die was rinsed with DI water.

Similar to the zincate process, the SEM and EDX detector were used to observe and verify the plating process.

B) Results and discussions

Figure 4.9 shows SEM photograph of a nickel layer on aluminum pads of the test die. It can be seen that electroless nickel plating after double zincation results in a uniform layer of nickel. The EDX analysis result of the nickel plated pad is shown in Figure 4.10. The analysis clearly shows the presence of only nickel and phosphorous peaks. The presence of phosphorous is typical for electroless nickel plating with sodium hypophosphite as a reducing agent since phosphorous is one of the products from nickel deposition reaction. EDX analysis was also performed on two spots around the pad (point A and B in Figure 4.11a). The analysis results of point A and B are illustrated in Figure 4.11b and Figure 4.11c, respectively. The elemental compositions of point A are

aluminum (Al) and silicon (Si). Si component should come from passivation layer on the top which can be SiO_2. Al component should come from aluminum trace under the passivation layer. The elemental composition of point B is silicon. This Si component should come from passivation layer, or passivation layer on the top with silicon underneath. The analysis results confirm that nickel plates only on aluminum pad area, since there is no nickel peak in the analysis of the spots around the pad.



(a) (b)

Figure 4.9 SEM photograph of two aluminum pads on the same test die after electroless nickel plating with double zincation treatment.

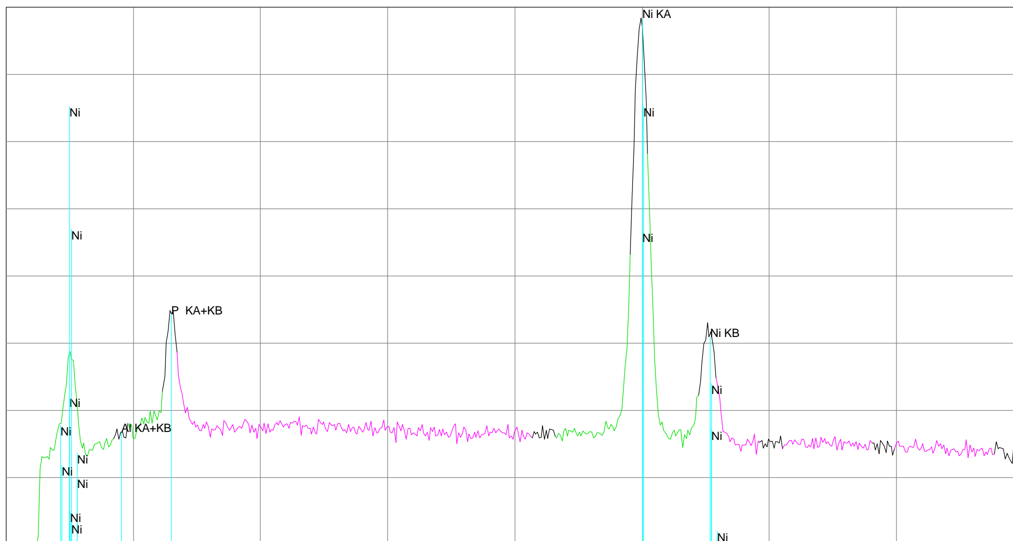
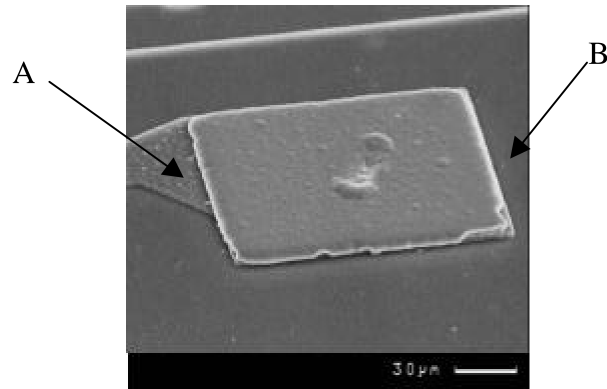
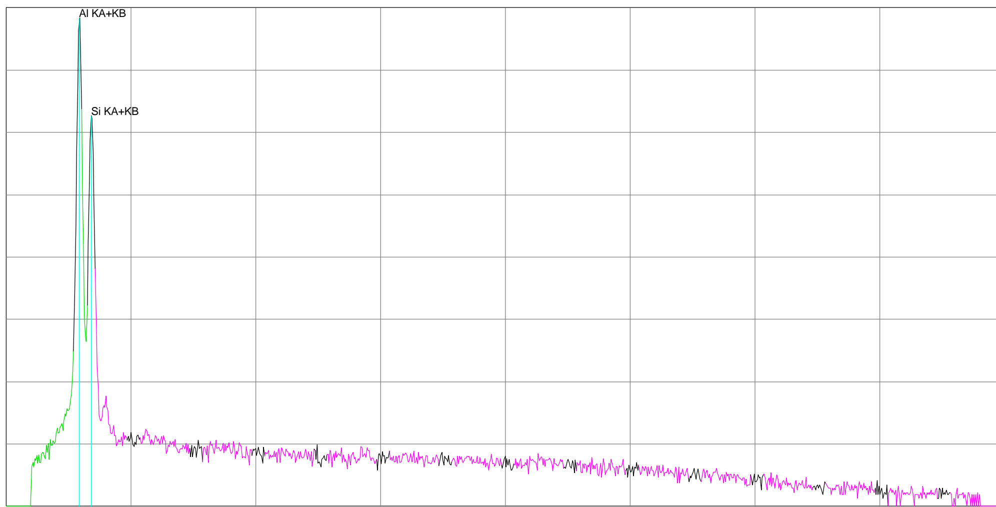


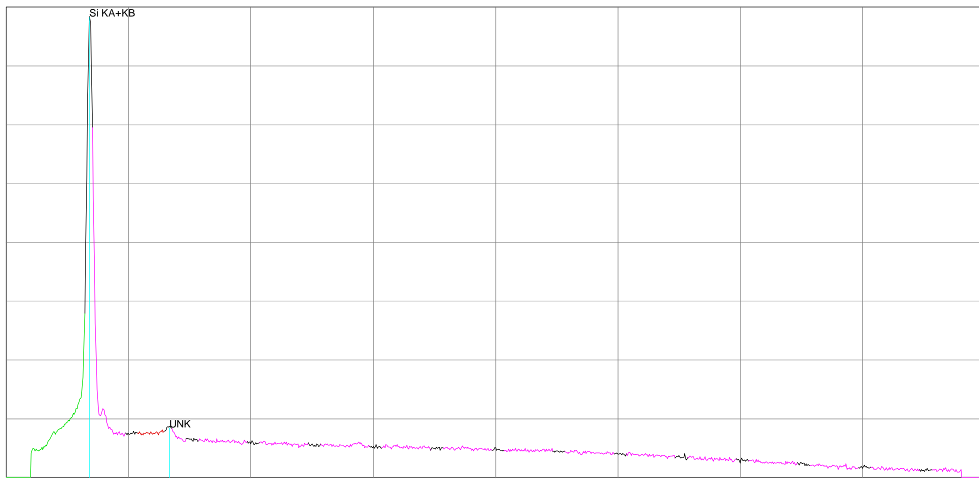
Figure 4.10 EDX analysis of nickel layer on an aluminum pad.



(a)



(b)



(c)

Figure 4.11 a) analyzed spots around the pad, b) EDX analysis of spot A, c) EDX analysis of spot B.

In order to verify that the electroless nickel plating process with double zincation produced a uniform nickel layer regardless of the pad area, the plating process was experimented further on a diode die with a 480 μm × 480 μm aluminum pad and the die size of 670 μm × 670 μm. The double zincation, followed by electroless nickel plating, was performed. The process resulted in a uniform nickel layer as shown in Figure 4.12. The EDX analysis result of this pad shows nickel and phosphorous peaks as shown in Figure 4.13.

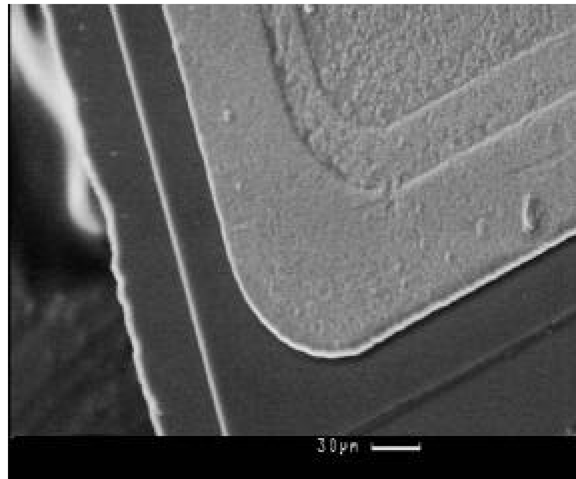


Figure 4.12 SEM photograph of aluminum pad of diode die after electroless nickel plating with double zincation treatment.

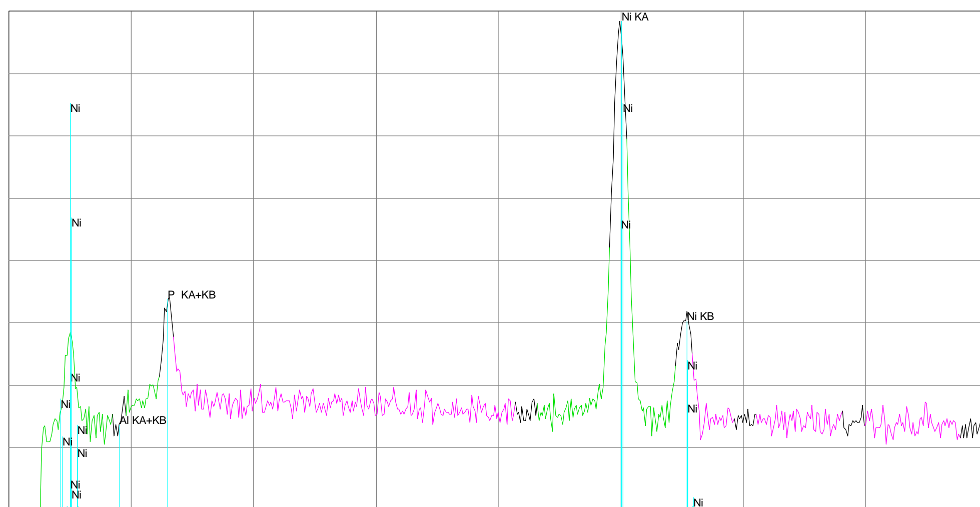


Figure 4.13 EDX analysis of a nickel plated aluminum pad of the diode die.

C) Thickness measurement of plated nickel

A profilometer surface analyzer was used to measure the thickness of nickel plated layer. The double zincation, followed by electroless nickel plating with plating time of 15 minutes was performed on a power FET die. The power FET die was used since the pad size (930 µm in diameter) and the die size (6.4 mm × 7.5 mm) were large enough for measuring with the profilometer. Figure 4.14 shows SEM photograph of a nickel plated aluminum pad of the power die and Figure 4.15 shows the EDX analysis result of this pad. In Figure 4.14, the nickel layer cannot be seen on the top of the pad since the passivation layer of this die was thicker than 5 µm which is expected to be the thickness of nickel plated layer.

The thickness measurement results of the aluminum pad before and after electroless plating are illustrated in Figure 4.16a and Figure 4.16b, respectively. Before plating, the pad surface is 9.3 µm below the passivation surface and the level of surface is even all over the pad. However, after plating, the level of the pad surface is not even. The lowest level is 3.8 µm below the passivation surface, and the highest level is 2.6 µm below the passivation surface. In the average, the surface of nickel layer is 3.2 µm below the passivation surface. Thus, the thickness of the nickel plated layer is 5.1 µm which is very close to the required thickness.

The thickness measurement result shows uneven thickness of the nickel plated layer. This result was not observed with the test chips and the diode die which was experimented previously.

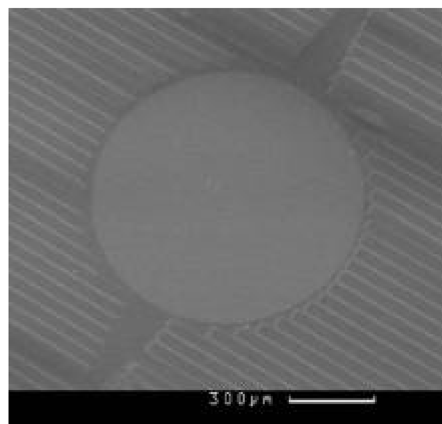


Figure 4.14 SEM photograph of a nickel plated aluminum pad of the power die.

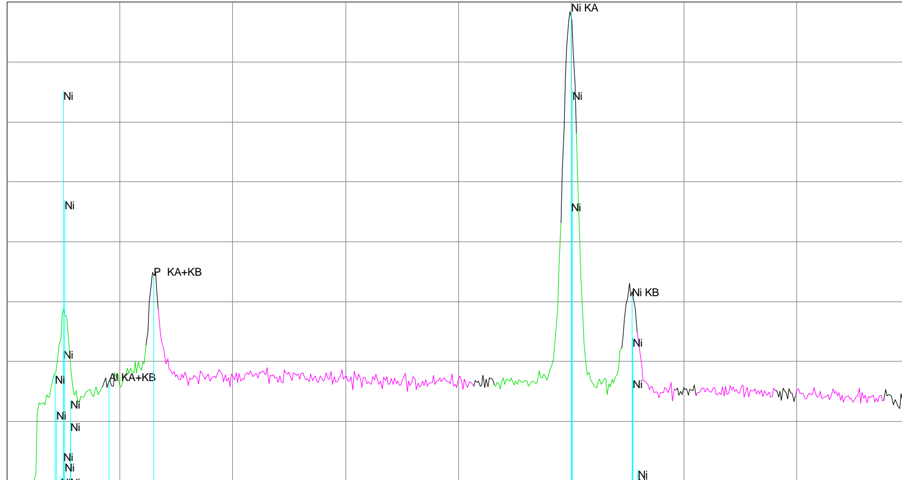
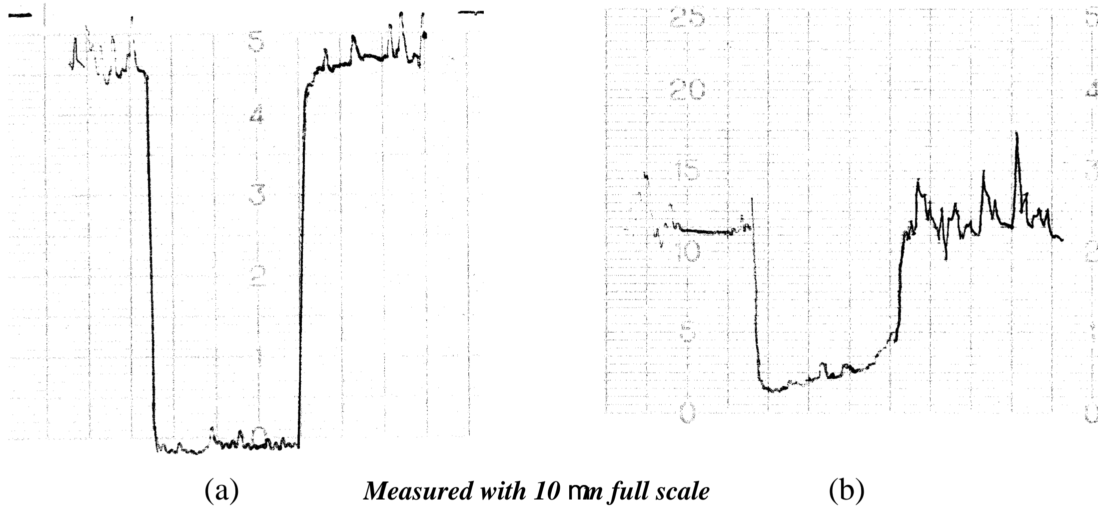


Figure 4.15 EDX analysis of nickel plated aluminum pad of the power FET die.



(a) ***Measured with 10 μm full scale*** (b)

Figure 4.16 Thickness measurement results of an aluminum pad of the power FET die: a) before electroless nickel plating, b) after electroless nickel plating.

4.2.2.3 Gold immersion process

The last step of the UBM deposition process was to coat a thin layer of gold on the electroless nickel to protect nickel from oxidation. Gold immersion was performed in a commercial solution at 90 °C with PH of 7-9 for 1 minute period of time. It was important to control the PH of the bath during the process. The continued use of the bath resulted in decreasing of the PH level which leaded to poor adhesion of gold plated layer. The PH of the bath can be increased to an operating level by adding amonium hydroxide.

In conclusion, the developed UBM deposition process can be used to form the UBM layer on aluminum pads of a single die without any difficulty. Double zincate process produces a thin uniform zinc layer which lead to a uniform nickel layer in the subsequent electroless nickel plating process. The plating process produces a pure nickel layer with the required thickness of 5 μm.

4.3 Temporary Die Attach Process

4.3.1 Concept

The purpose of this process is to temporarily attach a single die to a substrate so that the UBM deposition process can be performed on the die. Required properties of die attach material for this process are the following 1.) the material must be able to hold the die successfully during the UBM deposition process, 2.) the material is debondable, and 3.) the material residues can be perfectly removed. For the first requirement, the attachment material must be able to withstand high temperature, acidic and alkaline conditions for a certain period of time. (Temperature up to 90 °C and PH ranging from 5-12). The last requirement is necessary to eliminate any problems that may result from the material residues. The material residues at the die backside can cause problem in Flip Chip assembly process and can degrade the thermal performance of the die. In addition, the lack of adhesive residues is important if solderability of the die backside is required.

Thermoplastic adhesives are well known as reworkable die attach materials. Since polymer chains of thermoplastic are not chemically bonded to each other, but are bound by hydrogen bonding and polymer chain entanglement, thermoplastic has the ability to soften and re-melt when heated and return to solid state when cooled. When heated, polymer chains have enough energy to slide freely past one another resulting in melting of the thermoplastic. When cooled, the chains are not able to move and change to solid form. Since there is no chemical reaction between the chains, the melting and freezing process are completely reversible. As a reworkable die attach material, after attaching, the attached die can be removed by heating thermoplastic to the temperature above its melting temperature [44]. In addition, some of thermoplastic adhesives are claimed to have

property of debonding without leaving residues. With its properties, thermoplastic adhesive seems to be a prospective candidate for this process. In this work, two commercial thermoplastic adhesives were experimented.

4.3.2 Experimental procedure

Two types of commercial thermoplastic adhesives were experimented in this work. These two adhesives were available in film and paste forms. The film form was selected due to its convenience to be applied on the substrate. The detailed specifications are summarized in Table 4.1.

Table 4.1 Specifications of the experimental thermoplastic adhesive films.

Typical properties	**Adhesive typeA**	**Adhesive typeB**
Filler material	None	None
Attach temperature range	160°C-275°C	100°C-150°C
Continuous use range	-65°C-150°C	-65°C-100°C
Maximum excursion temperature	300°C	200°C
Glass transition temperature	≥98°C	≥16°C

The experiments were set to find out the appropriate bonding conditions of the thermoplastic adhesive films, and the proper cleaning procedure to remove the adhesive residues at the die backside. The experiments were performed on the same test chips used in UBM deposition process (the size of the test chips was 1.28 mm × 1.28 mm). The experimental procedure was as follows,

1) The adhesive film was cut in to a small piece with the area a little bit larger than the die area.

2) The adhesive film was placed on a 1"× 1" clean ceramic substrate.
3) The test die was placed on the adhesive film.
4) The die was bonded to the ceramic substrate at certain specified bonding conditions. The parameters examined in the bonding step were bond temperature, bond time, and applied pressure. (These three parameters were adjusted and optimized until the proper bonding conditions were set for the adhesive to be able to hold the die throughout the plating process). The pressure was applied using metal weight with the weight, according to the die area, resulting in the required pressure.
5) The test die was passed through the UBM deposition process including double zincation, electroless nickel plating, and gold immersion.
6) After the UBM deposition, the test die was debonded from the substrate. To debond the die, the substrate was heated to the bond temperature and the die was manually removed.
7) The adhesive residues were removed with a devised cleaning procedure. To remove the adhesive residues, the debonded die was placed in selected solvents at room temperature for a certain period of time. The solvents selected for the cleaning process were isopropyl alcohol, acetone, trichloroethane, and xylene.

After cleaning, an optical microscope and a scanning electron microscope were used to observe the existence of the adhesive residues. Experiments and experimental results in bonding step and cleaning step are summarized in Table 4.2 and Table 4.3, respectively.

4.3.3 Experimental Results and Discussions

The experimental results showed that adhesive film type A can hold the die throughout the UBM deposition process and the bonding conditions are proved to be not very critical. The 200 °C bond temperature, and 40s bond time without applied pressure are the sufficient bonding conditions. However, this adhesive cannot be removed by any of the selected solvents. Since it cannot be cleaned off, the adhesive film type A cannot be used as a temporary die-attach material for this work.

For the adhesive film type B, the bonding conditions for the adhesive to be able to successfully hold the die throughout the UBM deposition process are very critical. This

is due to the fact that the maximum continuous use temperature of this adhesive is just a little bit above the temperature required in the plating process. In the bonding step, the maximum bond temperature and an amount of applied pressure are required. The 150 °C bond temperature, 50s bond time, and pressure applied with 2g load are the sufficient bonding conditions for this adhesive. After debonding, the residues of this adhesive can be perfectly removed with acetone at room temperature. The adhesive is cleaned off in 10-15 minutes depending on the amount of the adhesive left on the die backside after debonding. Figure 4.17a and Figure 4.17b illustrate SEM photograph of the backside of a debonded test die before cleaning and after cleaning, respectively. It can be seen that before cleaning there are adhesive residues all over the die backside, but after cleaning all adhesive residues are removed and the die backside are clean.

Table 4.2 Summary of bonding parameters in the adhesive bonding step and experimental results/ data.

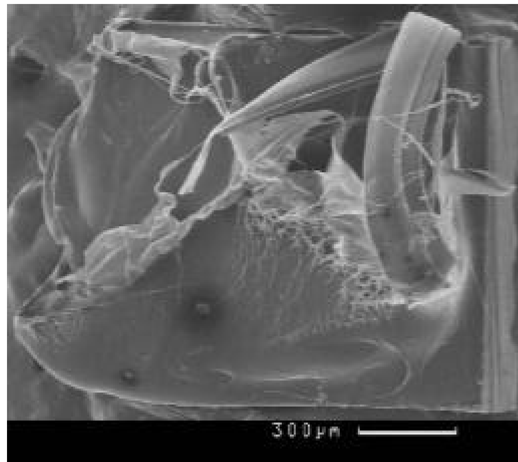
Bond time	**Bond temperature**	**Applied load**	**Experimental result**
Type A			
40s	180°C	None	Fail
40s	200°C	None	Succeed
Type B			
40s	130°C	None	Fail
40s	130°C	2g load	Fail
50s	150°C	None	Fail
50s	150°C	2g load	Succeed

Fail →Adhesive film falls out during Ni plating.
Succeed →Adhesive film successfully holds the die throughout the deposition process.

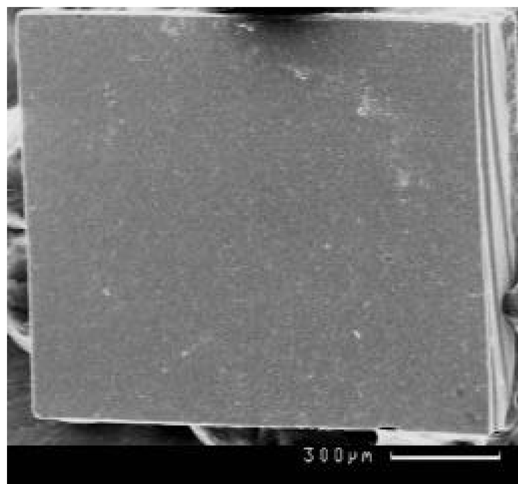
Table 4.3 Summary of selected solvents in the adhesive cleaning step and the experimental results.

Solvent	Adhesive typeA	Adhesive typeB
Isopropyl alcohol	Fail	Fail
Acetone	Fail	Succeed (10-15minutes)
Trichloroethane	Fail	Fail
Xylene	Fail	Fail

Fail→Solvent cannot remove adhesive after one hour.
Succeed→Solvent can remove adhesive.



(a)



(b)

Figure 4.17 SEM photograph of the backside of a debonded test die: a) before cleaning, b) after cleaning.

In this work, the adhesive type B was experimented further on other dice with different die areas to verify the success of the developed die attach process when different die areas are used. The bare dice with three different die areas (die A: 0.67mm × 0.67mm, die B: 1.6mm × 2.31mm, and die C: 6.3mm × 7.3mm) were passed through the same experimental procedure used previously with the test chips. The bonding conditions were 150 °C bond temperature, 50s bond time, and pressure applied with 1g load for die A, 2g load for die B, and 10g load for die C were used. The applied loads were selected according to the die areas. The experimental results showed that this bonding condition works well for die B and C which have die area larger than the test die (1.28mm × 1.28mm). However, for the smaller area die (die A), the adhesive fell out during the electroless nickel plating in some experiments. This problem could be solved by increasing the pressure. The applied load was then increased to 2g load. With the adjusted bonding condition, the adhesive succeeds in holding the die during the deposition process. The experiments show that the bonding conditions of the adhesive are more critical for bonding a small area die than it is for a large area die. This is due to for the small area die, the die surface which is pressured and attached to the substrate is small, thus more applied pressure is required for adhesive to be able to hold the die successfully.

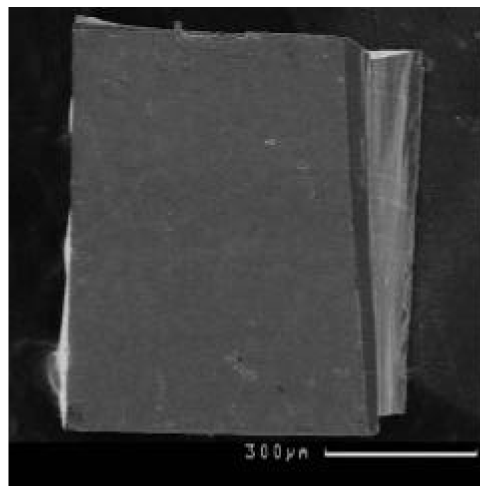


Figure 4.18 SEM photograph of the backside of die A after debonding and cleaning.

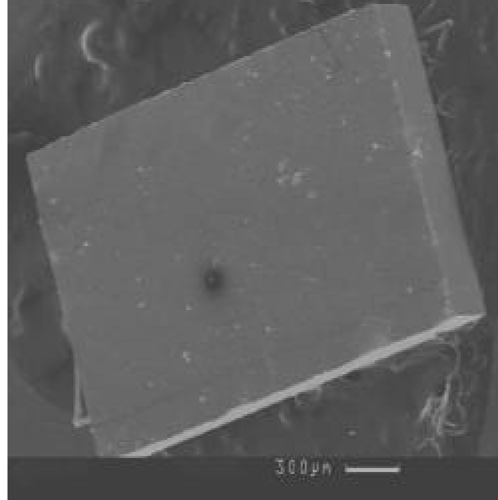


Figure 4.19 SEM photograph of the backside of die B after debonding and cleaning.

After the UBM deposition, die A, B, and C were debonded and then cleaned with acetone for 10-15 minutes. Figure 4.18 and Figure 4.19 illustrates SEM photograph of the backside of die A and die B after debonding and cleaning, respectively. The photographs show a clean surface of die backside without any adhesive residues.

It can be concluded that the developed die attach process using thermoplastic adhesive film type B has all of the attributes required in the temporary die attach process of this work. In addition, with proper bonding conditions of the adhesive film, this die attach process works successfully regardless of the die area.

4.4 Conclusions

The UBM formation process on a single die has been developed in this work. It has been demonstrated that electroless nickel plating followed by gold immersion is a suitable process for UBM deposition on a single die, and that the temporary die attach process can be achieved with the use of thermoplastic adhesive acquiring suitable specifications and proper bonding conditions of the adhesive. The developed process provides a pure nickel layer for UBM structure and a clean die backside surface without

any adhesive residues. This process allows Flip Chip bonding to start from a single die, thus making Flip Chip technology more practical for low volume microelectronic applications.

Chapter 5 Application of the Developed UBM Formation Process in Flip Chip Bonding of a Single Die

5.1 Introduction

This chapter presents an application of the UBM formation process developed in this work in Flip Chip bonding of a single die. The main purpose of this chapter is to illustrate the potential of the developed UBM formation process to be used in Flip Chip applications without encountering potential problems.

The bonding process starts from depositing a UBM layer on the die using the developed process. After the UBM deposition, solder bumps are formed on the pads of the die using a ball placement technique. Then, the bumped die is Flip Chip bonded to the substrate and the assembly is tested for evaluation. The bonding procedure, problems that needed to be addressed in the process, the methods and techniques devised to solve the problems, and testing results are discusses in details. Finally, the potential of the developed UBM formation process to be used in Flip Chip bonding of a single die is discussed.

5.2 Objectives of the Work

The work presented in this chapter is an application of the developed UBM formation process in Flip Chip bonding of a single die. The objectives of this work are as follows,

1) To illustrate an application of the UBM formation process developed by the researcher in Flip Chip bonding of a single die.
2) To verify that the developed UBM formation process does not damage nor electrically affect the sensitive die.
3) To verify that the deposited UBM layer makes good connections with the aluminum pads of the die and with the solder bumps.
4) To verify that the die backside after adhesive residues cleaning is solderable.

For future directions, the objectives of this work are to test the reliability of the UBM layer and the connections of the UBM to the bumps, and to test the performance of the device assembled with Flip Chip bonding technique. However, the current main goal of this work is to illustrate the potential of the developed UBM formation process to be used successfully in Flip Chip bonding of a single die.

5.3 Overview of the Work

This work was to achieve assembly and connections of a single die using Flip Chip bonding technique. The UBM was deposited using the developed UBM formation process, and the solder bumps were formed using preformed solder balls. The assembly procedure was developed and performed on functional power FET devices. The power FET is an N-type FET. The die has three terminals; gate, source, and drain. The gate and the source terminals are at the front side of the die and the drain terminal is located at the backside of the die. The dimensions of the power FET die is illustrated in Figure 5.1.

The power FET die was used in this work due to the following reasons,

1) It is easy to check damage or faults in the die and to test electrical functionality of the die. Damage of the power FET can be tested by checking a short circuit between the gate-source, the drain-source, and the gate-drain terminals. The short circuit between terminals of the FET indicates permanent damage of the device.
2) Power FET is a sensitive device, thus making it suitable for verifying the damage caused by the process.
3) The drain terminal of the power FET is at the die backside. This die structure can be used to verify solderability of the backside of the die.
4) The size of the die (170 mils × 227 mils) and the size of the pads (gate terminal: 20 mils × 29 mils, source terminal: 37mils × 49 mils) are relatively large, thus making it easier to handle the die and to conduct various processes on the die.

Dimension in mm (mil)

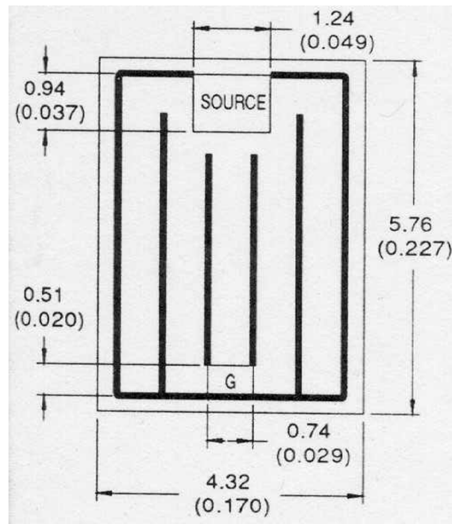


Figure 5.1 Dimensions of the power FET die.

The assembly of the power FET was designed as shown in Figure 5.2. The gate terminal and the source terminal of the FET were connected to the substrate metallization with solder bumps. The drain terminal was connected to the substrate metallization with copper strap soldered to the backside of the die.

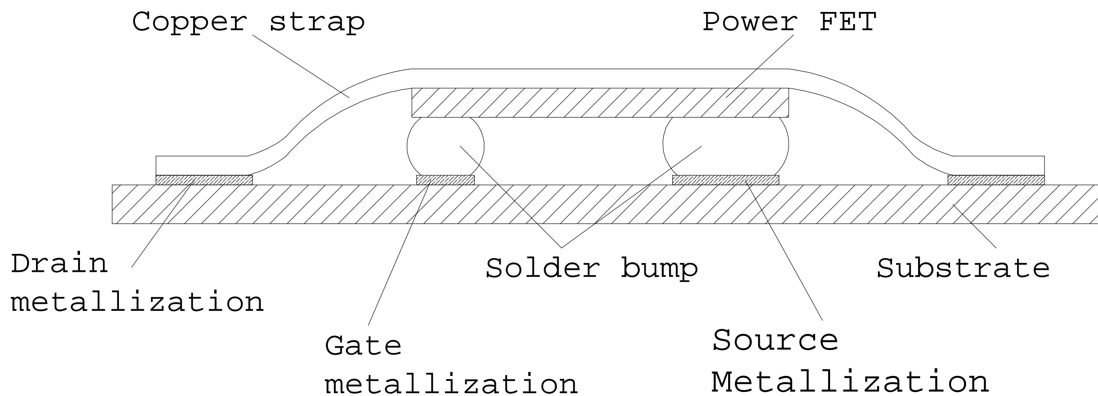


Figure 5.2 The assembly of the power FET die.

Since the power FET is a static sensitive device, it was necessary to prevent damage on the die caused by static charge. In the process of this work, every workstation and an operator were electrically grounded at all times to avoid static charge during operation, and the die was carried from one workstation to another workstation with a metal tray to avoid static charge and discharge during handling.

5.4 Solder Bump Formation

The preformed solder balls were used in this work to form the bumps on the gate and the source terminal of the die. The solder ball was 63Sn/37Pb eutectic solder with the ball diameter of 30 mils. The melting point of 63Sn/37Pb eutectic solder was 183 °C. Since the area of the source terminal (37 mils × 49 mils) was approximately three times larger than that of the gate terminal (20 mils × 29 mils), in order to obtain the equal bump height at both terminals after reflow the ball, three balls were used at the source terminal and one ball was used at the gate terminal to form these bumps.

5.4.1 Bump formation procedure

Prior to bump formation, the UBM formation process, as presented in Chapter 4, was performed to deposit nickel/gold UBM layer on the pads of the die. As a reminder, the brief process flow for UBM formation was as follows,

1) The die was temporarily attached to 1" × 1" ceramic substrate using thermoplastic film type B. The bonding conditions of the adhesive for this power FET die was 150 °C bond temperature, 50s bond time, and pressure applied with weight 10g.
2) The UBM deposition process was performed. The process steps consisted of double zincation, nickel electroless plating for 15 minutes, and gold immersion, respectively.
3) After the UBM deposition, the die was debonded from the substrate and was cleaned in acetone for 10-15 minutes to remove adhesive residues at the die backside.

After the UBM layer was formed and the adhesive residues were cleaned off, the die was ready for bump formation. In the ball placement process, first, the solder balls

were dipped in a thin layer of 5R flux which is a suitable flux for soldering gold surface. After fluxing, the balls were manually placed on the terminals of the die, three balls on the source terminal and one ball on the gate terminal. Then, the balls were reflowed on hot plate reflow system. The highest temperature of the plate was set to 230 °C, and the travelling speed over the hot plate was 10 inches/min. After the reflow process, the flux residue was removed with 1,1,1 trichloroethane.

5.4.2 Bump formation results

After reflow, the balls wet all over the pad areas both at the gate and the source terminals. At the source terminal, the three balls melt and form one large bump on the pad. The height of the bump at the source terminal is a little bit less than that of the bump at the gate terminal.

5.4.2.1 Problems in bump formation process

A) Short circuit between the gate and the source terminal

After the bump formation, the die was probed to check the damage of the die. The probing result indicates a short circuit between the gate and the source of the die. To find out the processing step that caused the short, the bump formation process was performed once again and the gate terminal and the source terminal were probed after each processing step including after die attachment, electroless nickel plating, gold immersion, debonding, adhesive cleaning, and after reflow the balls.

The probing results indicate that the short circuit between the gate and the source occurred after reflow the balls. The results confirm that the problem is not caused by the UBM formation process and that none of the processing step in UBM formation process destroys the die.

The die was investigated further and it was found that in the pattern of the die, there are three metal traces around the edge of the die as shown in Figure 5.3, and one of these metal traces connects to the source terminal. It is likely that the metal trace connected to the source terminal is the primary cause of the short circuit. Since this metal trace is very closed to the gate terminal, and it is possible that after the ball is reflowed, the ball bonds to the gate terminal and also bonds to the metal trace, thus

making a connection between the gate and the source. This problem was solved by coating a thin layer of dielectric material at the edge of the die to cover the metal trace, thus preventing the connection between the metal trace and the solder bump at the gate terminal. The dielectric material used in that regard was a non corrosive, flowable silicon rubber. This material was cured by allowing it to expose to moisture at room temperature for 24 hours.

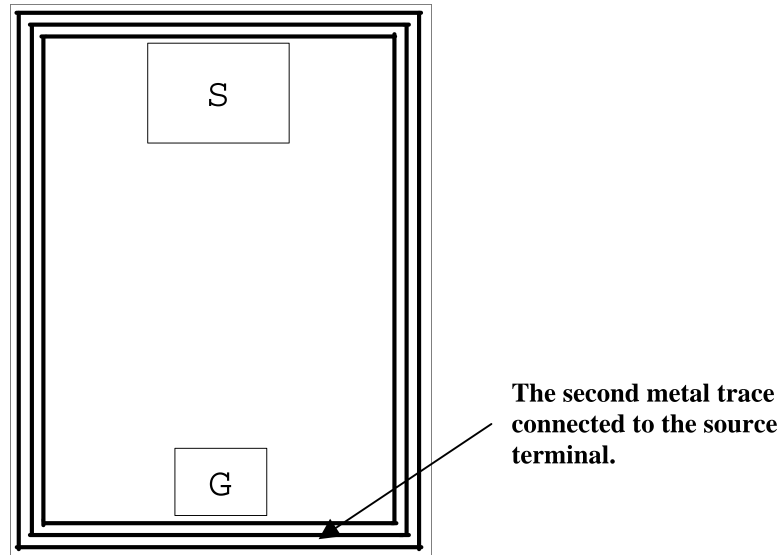


Figure 5.3 Metal traces around the edge of the power FET die.

In the bump formation process, first, the UBM formation process was performed. Next, the adhesive residues were cleaned off and the die was air dried. Third, the silicon rubber was applied at the edge of the die by brushing. The silicon rubber was coated twice to ensure a good dielectric layer coating. After the first coating, the die was positioned on the grounded station for two hours to allow the first silicon rubber layer to cure and stop flowing. Then, the second layer of silicon rubber was applied. After the second coating, the die was positioned on the grounded station for 24 hours to allow the silicon rubber to cure and turn to a rubbery solid form. Next, the balls were dipped in 5R flux, placed on both terminals, and reflowed at 230 °C temperature.

After bump formation, the die was probed. The probing result indicates that there is no short circuit between the gate and the source terminals. The results confirm that the metal trace around the die is the reason contributing to the short between the gate and the source terminals and that the dielectric coating method can basically solve this problem.

B) Imbalance of the die pattern

Another problem occurred after the bump formation, namely, the leveling of the die. Since this die had only two bumps in the middle of it, after it was flipped down, the balls could not hold the die in level and one side of the die fell down. This problem can be solved in the process to place and bond the die to the substrate. This problem can be solved in the die placement and Flip Chip bonding process using four extra balls at the die corners to hold the die in one level. More details about this approach will be discussed in later section.

5.5 Flip Chip Bonding

5.5.1 Substrate design

The substrate used in this was a Printed Circuit Board (PCB). The pattern of the substrate was designed as shown in Figure 5.4. Since the drain terminal of the die was connected to the substrate metallization with the copper strap which extends beyond the die body, it is important to balance the weight of the copper strap by having the strap extended equally at both side of the die. Hence, the substrate was designed to have two metal traces to be connected to both sides of the copper strap.

In addition, the substrate was designed to have four extra pads (corner pads). These four pads were designed such that the positions of the pads were at the corners of the die when the die was placed on the substrate. In the bonding process, four balls were placed on these pads, one ball on each pad. These four balls served the purpose of holding the die in one level when the die was placed on the substrate.

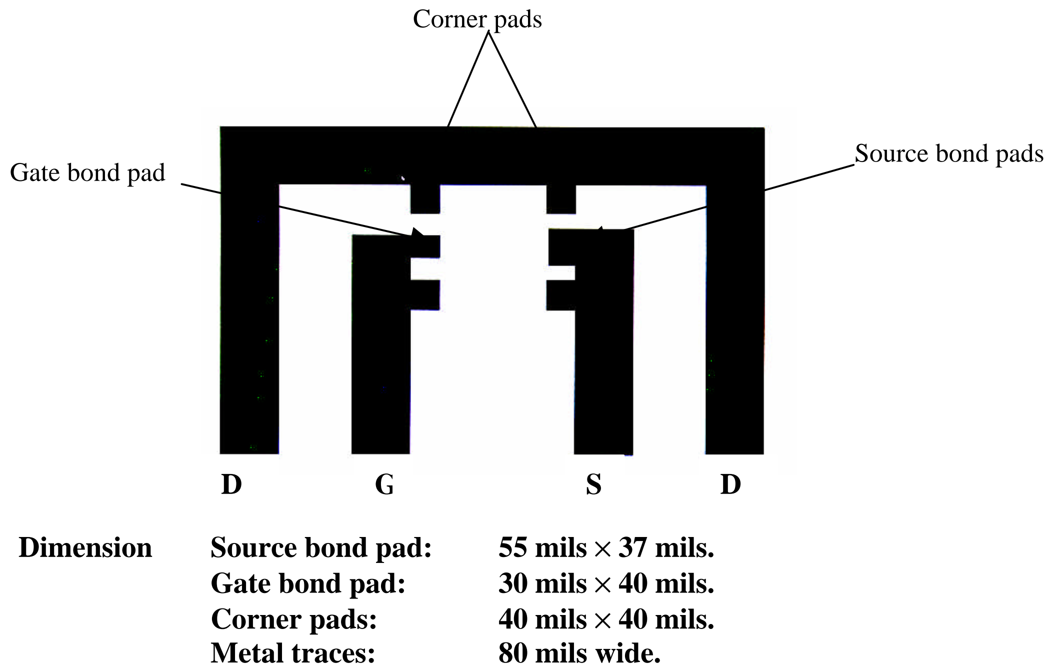


Figure 5.4 Substrate pattern.

5.5.2 Flip Chip bonding procedure

The bonding procedure consisted of four major steps; UBM formation, copper strap bonding, bump formation, and Flip Chip bonding, respectively. In the copper strap bonding step, the strap was bonded to the die backside using 96.5Sn/3.5Ag solder preform. The melting point of this solder was 221 °C which is higher than the melting point of the 63Sn/37Pb solder balls (183 °C). Thus, in the process, the 96.5Sn/3.5Ag solder preform was used first so that this solder will not reflow again in the subsequent reflow process of the 63Sn/37Pb solder balls.

The Flip Chip bonding procedure of the power FET die was as follows,

<u>UBM formation</u>

1) Attach the die to 1" × 1" ceramic using thermoplastic adhesive film type B. The bonding conditions of the adhesive for this power FET die was 150 °C bond temperature, 50s bond time, and pressure applied with weight 10g.

2) Deposit the UBM layer on the die. The deposition processes were double zincation, nickel electroless plating for 15 minutes, and gold immersion, respectively.
3) Debond the die from the substrate and dip it in acetone for 10-15 minutes to remove adhesive residues at the die backside.

Copper strap bonding

4) Cut a 4-mil thick copper sheet into a suitable size strap with the width a little bit larger than the die width, and the length just long enough to connect to both sides of the drain metallization on the substrate.
5) Cut 96.5Sn/3.5Ag solder preform into a piece with the size equals to the die size.
6) Dip the preform in 5RMA flux. The excess of the flux was removed with a clean cloth.
7) Place the solder preform on the copper strap, adjust the position of the preform to be at the middle of the strap, then place the die on the preform.
8) Place the assembly on a ceramic substrate and reflow on hot plate reflow system with the highest plate temperature of 260 °C and a travelling speed of 10 inches/min.

Dielectric coating

9) Coat silicon rubber around the edge and at the four corners of the die. The silicon rubber was coated at the four corners of the die to protect the die surface in the position touched with the four extra balls used to hold the die when the die was placed on the substrate.
10) Allow the first silicon layer to cure for 2 hours.
11) Coat silicon rubber again around the edge and at four corners of the die.
12) Allow the second silicon layer to cure for 24 hours.

Bump formation

13) Dip the solder balls in a thin layer of 5R flux.
14) Place the balls on the terminals of the die, three balls on the source terminal and one ball on the gate terminal.

15) Reflow the balls on hot plate reflow system with the highest plate temperature of 230 °C and a travelling speed of 10 inches/min.

Flip Chip Bonding

16) Dip four solder balls in a thin layer of 5RMA flux.
17) Place the balls on the four corner pads of the substrate, one ball on each pad.
18) Apply 5RMA flux on the gate pad and source pad of the substrate.
19) Align the die with the substrate pattern and place the die on the substrate. A semi-automatic Flip Chip placement machine was used in this step. The details of this machine operation were already presented in Chapter 3, Section 3.2.2. First, the bumped die was placed faced down on the pick-up stage and the PCB substrate was placed on the placement stage. Then, the position of the pick-up stage was adjusted such that the center of the die was in the position of the placement head. After the stage was set in the proper position, the pick-up cycle was initiated. The placement head traveled down to the stage, picked up the die with vacuum, and travel back up. Next, the placement stage was moved into the position under the placement head, and the position of the stage was carefully adjusted until the bumps and the substrate pattern were perfectly aligned. After alignment, the placement cycle was initiated. The placement head traveled down, and placed the die on the substrate with certain applied force. In the die placement step, the four balls at the corners of the die helped to hold the die in level.
20) Reflow the assembly on the hot plate reflow system with the highest plate temperature of 230 °C and a travelling speed of 10 inches/min.
21) Clean the flux residue using 1,1,1 trichloroethane.

5.5.3 Results and discussions

After the bonding process, the assembly was tested by measuring the resistance value between the die terminals. The resistance results are as follows,

Resistance between gate and source (Rgs) = Open circuit

Resistance between gate and drain (Rgd) = Open circuit

Resistance between drain and source (Rds) = 2.4 MΩ

There is no short circuit detected between any of the die terminals.

Next, the assembly was tested by applying 15 volts DC at the gate and 0 volt at the source to turn on the FET, and the resistance value between source and drain (Rds) was measured. The resistance results are as follows,

With 15-volt Vgs (FET on), Rds = 0.8 Ω

With 0-volt Vgs (FET off), Rds = 2.4 MΩ

The results indicate that the die functions properly as an N-type FET. The low resistance path is formed between the drain and the source terminal when the voltage at the gate terminal is made positive with respect to the voltage at the source terminal.

From the test results, one can conclude the following facts,

1) Since there is no short circuit between any of the die terminals, it can be concluded that the die is not damaged nor affected after the assembly process. This confirms that none of the processing step in the assembly process would cause damage to the die.
2) Since the die functions properly after assembly process and the value of Rds is reasonable, it can be concluded that all of the connections between the die terminals and the substrate metallization are formed properly. This confirmed that the UBM layer at the source and the gate makes good connections to the die terminals and the solder bumps, and that the backside of the die makes good connection to the copper strap.

5.6 Conclusions

The application of the developed UBM formation process in Flip Chip bonding of a single die has been illustrated in this work. It has been proved that the developed UBM formation process does not cause any damage to the sensitive die, and that the UBM layer makes good connections to the aluminum pads of the die and to the solder bumps. It has also demonstrated that the backside of the die after adhesive cleaning is basically

solderable. The solderability of the die backside will be useful for any Flip Chip applications that require electrical connections from the backside of the die.

The Flip Chip assembly of a power FET die performed in this work has illustrated that the developed UBM formation process has a great potential to be used successfully in Flip Chip applications. However, this work is not optimized, and further work can be achieved to analyze and improve the reliability issue, electrical and thermal performance of the assembly. The assembly procedure can also be improved to reduce the assembly and processing steps, assembly time, and to achieve more reliable assembly.

Chapter 6 Conclusions

6.1 Summary

The objectives of this thesis were to develop a low cost process to deposit UBM layer on aluminum pads of single die/dice, and to illustrate an application of the developed process in Flip Chip bonding of a single device.

Chapter 1 presented a general introduction to this thesis. The statement of problem, objective of this thesis, and thesis structure were described in this Chapter.

Chapter 2 presented a review of the topics relevant to this thesis including Flip Chip trends, solder bump and UBM structure, UBM deposition techniques, and bump formation techniques. Electroless nickel plating technique which was used in this work to deposit UBM layer was also discussed.

Chapter 3 provided an overview of the Flip Chip assembly process flow. The common procedure and the industrial equipment used in each processing step were discussed. The semi-automatic placement machine used in this work was also presented.

Chapter 4 presented UBM formation process on single die/dice developed in this work. The UBM deposition process using electroless nickel plating, followed by gold immersion, and the temporary die attachment process using thermoplastic adhesive were discussed, respectively. Experimental results and analysis results of each processing step were presented and discussed.

Chapter 5 presented an application of the developed UBM formation process in Flip Chip bonding of a single die. The Flip Chip assembly procedure, the problems encountered in the process and the solutions devised were discussed. Finally, the test results were presented and the conclusions based on the test results were discussed.

6.2 Conclusions

The process for UBM formation on single die/dice has been developed. The result presented in this thesis demonstrated that electroless nickel plating, followed by gold immersion is a suitable technique to deposit a UBM layer on aluminum pad of the single die. The electroless nickel plating produce a uniform layer of pure nickel. The results also showed that with suitable specifications and proper bonding conditions of the adhesive, thermoplastic adhesive can be used to temporarily hold the die during plating process. The results also show that the adhesive residue at the die backside can be perfectly removed.

The developed process can be used successfully to deposit UBM layer on the single die regardless of the die size, pad size, and the complexity of the die pattern.

It was illustrated in the work presented in Chapter 5 that the developed process does not cause any damage to the sensitive die. The results also showed that the UBM makes good connection with the aluminum pads and with the solder bump, and that the backside of the die is solderable. The developed UBM formation process has great potential to be used successfully in Flip Chip applications.

6.3 Future Directions

Further research work will be focused on Flip Chip assembly of a single die using the develop UBM formation process to deposit UBM layer and using ball placement techniques to form solder bumps. The future plan will be to work further on Flip Chip assembly of the power FET device presented in Chapter 5. The objectives of the work would be to improve assembly procedure, test reliability of the assembly, and analyze electrical and thermal performance of the assembly. The assembly procedure can be improved to reduce processing steps and processing time, and to achieve more reliable assembly. Also, underfill process needs to be performed to improve reliability and performance of the assembly.

Since this device is a power device, it is also necessary to evaluate the reliability of the assembly under high power environments.

References

1. J. H. Lau, "Electronics Packaging Technology Update: BGA, CSP, DCA, and Flip Chip", The International Electronic Manufacturing Technology Symposium and The International Microelectronics Conference, IEMT'/IMC, pp. 32-36, 1997.

2. J. H. Lau, "Ball Grid Array Technology", McGraw-Hill, New York, 1995, Chapter 1

3. J. E. Sergent and C. A. Harper, "Hybrid Microelectronics Handbook", McGraw-Hill, New York, Chapter 6, 1995.

4. P. E. Garrou and I. Turlik, "Multichip Module Technology Handbook", McGraw-Hill, Chapter 8, 1998.

5. D. S. Patterson, P. Elenius and J. A. Leal, "Wafer Bumping Technology-A Comparative Analysis of Solder Deposition Processes and Assembly Considerations", Advances in Electronic Packaging, Vol. 1, pp. 337-351, 1997.

6. C. L. Lessen, "Global Technical and Commercial Developments with Flip Chip Technology", Electronic Components and Technology Conference, pp. 1056-1058, 1996.

7. E. J. Vardaman and T. Goodman, "Flip Chip Market Trends and Infrastructure Limitations", The International Electronic Manufacturing Technology Symposium and The International Microelectronics Conference, IEMT/IMC, pp. 37-40, 1997.

8. P. Elenius, "Flex on Cap-Solder Paste Bumping", Electronic Components and Technology Conference, pp. 248-253, 1997.

9. S. Y. Jang and K. W. Paik, "The Study on the Under Bump Metallurgy (UBM) and 63Sn-37Pb Solder Bumps Interface for Flip Chip Interconnection", Materials Research Society (MRS) Symposium Proceedings, Vol. 515 (Electronics Packaging Materials Science X), pp. 67-72, 1998.

10. S. J. Hong, T. M. Korhonen, M. A. Korhonen and C. Y. Li, "Under Bump Metallization Development for Eutectic Pb-Sn Solders", Materials Research Society (MRS) Symposium Proceedings, Vol. 515 (Electronics Packaging Materials Science X), pp. 73-77, 1998.

11. K. L. Lin and W. H. Chao., “Material Interactions of Solder Bumps Produced with Fluxless Wave Soldering”, IEEE Transactions on Components, Packaging, and Manufacturing Technology, CPMT-B, Vol. 21, No. 1, pp. 59-64, 1998.

12. K. L. Lin and J. W. Chen, “Manufacturing the Ti/Cu/Electroless Nickel Bump on Si”, International Journal of Microcircuits and Electronic Packaging, IJMEP, Vol. 22, No. 1, pp. 1-5, 1999.

13. G. A. Rinne, "Solder Bumping Methods for Flip Chip Packaging", Electronic Components and Technology Conference, pp. 240-247, 1997.

14. H. Tsunetsugu et al., "Flip Chip Bonding Technique Using Transferred Microsolder Bumps", IEEE Transactions on Components, Packaging, and Manufacturing Technology, CPMT-C, Vol. 20, No. 4, pp. 327-334, 1997.

15. J. Kloeser et al., "Fine Pitch Stencil Printing of Sn/Pb and Lead Free Solders for Flip Chip Technology", Electronic Components and Technology Conference, pp. 254-264, 1997.

16. J. H. Lau, "Flip Chip Technologies", McGraw-Hill, New York, Chapter 3, 1996.

17. T. Akashi et al., "Eutectic Solder Bumped Flip Chip Development", IEEE/CPMT International electronics manufacturing technology symposium, pp. 319-325, 1997.

18. J. H. Lau, Flip Chip Technologies, McGraw-Hill, New York, Chapter 15, 1996.

19. K. L. Lin and S. Y. Chang, "Approaching a Uniform Bump Height of the Electroplated Solder Bumps on a Silicon Wafer", IEEE Transactions on Components, Packaging, and Manufacturing Technology, CPMT-B, Vol. 19, No. 4, pp. 747-751, 1996.

20. L. Levine, "Ball Bumping and Coining Operations for TAB and Flip Chip", Electronic Components and Technology Conference, pp. 265-267, 1997.

21. G. Hotchkiss et al., "Tacky Dots™ Transfer of Solder Spheres for Flip Chip and Electronic Package Applications", Electronic Components and Technology Conference, pp. 434-441, 1998.

22. A. Beikmohamadi et al., "Tacky Dots™ Technology for Flip Chip and BGA Solder Bumping", Electronic Components and Technology Conference, pp. 448-453, 1998.

23. G. Motulla et al., "A Low Cost Bumping Process for Flip Chip-Technology Using Electroless Nickel Bumping and Solder Ball Placement", The International Electronic Manufacturing Technology Symposium and The International Microelectronics Conference, IEMT'/IMC, pp. 174-181, 1997.

24. K. J. Puttlitz, K. A. Stalter and P. A. Totta, "Solder Transfer Technique for Flip-Chip and Electronic Assembly Applications", IEEE Transactions on Components, Packaging, and Manufacturing Technology, CPMT-C, Vol. 21, No. 3, pp.182-188, 1998.

25. A. F. J. Baggerman and D. Schwarzbach, "Solder-Jetted Eutectic PbSn Bumps for Flip-Chip", IEEE Transactions on Components, Packaging, and Manufacturing Technology, CPMT-B, Vol. 21, No. 4, pp. 371-381, 1998.

26. R. Aschenbrenner et al., "Flip Chip Attachment Using Anisotropic Conductive Adhesive and Electroless Nickel Bumps", IEEE Transactions on Components, Packaging, and Manufacturing Technology, CPMT-C, Vol. 20, No. 2, pp. 95-100, 1997.

27. C. Vanhorn, R. Oberle and G. Shawhan, "Plating Technologies for Flip Chip Applications", Proceedings of the Technical Program: NEPCON West, Vol. 1, pp. 336-359, 1997.

28. R. L. Macary, "Better Plating of Electroless Nickel on Aluminum", Products Finishing, Vol. 52, No. 1, pp. 52-63, 1987.

29. K. Yamakawa et al., "Maskless Bumping by Electroless Plating for High Pin Count, Thin, and Low Cost Microcircuits", The International Journal for Hybrid Microelectronics, Vol. 13, No. 3, pp. 69-84, 1990.

30. H. Honma, H. Watanabe and T. Kobayashi, "Direct Nickel Plating on Aluminum Substrate for Microbump Formation", Journal of the Electrochemical Society, Vol. 141, No. 7, pp. 1791-1795, 1994.

31. H. Watanabe and H. Honma, "Electroless Nickel Plating", Journal of the Electrochemical Society, Vol. 144, No. 2, pp. 471-476, 1997.

32. T. Foley, "Step by Step: Die Placement", Advanced Packaging, Vol. 8, No. 2, pp. 50-54, February 1999.

33. R. Boulanger, J. Carbin and D. Viza, “Flip Chip Assembly: Equipment and Process”, Advance Packaging, Vol. 8, No. 3, pp. 28-32, March, 1999.

34. D. Moore, "Flip Chip Attachment", Advanced Packaging, Vol. 6, No. 4, pp. 39-42, July/August 1997.

35. Manual for the Table Top Flip Chip Placement System-Model 850 from Semiconductor Equipment Corporation.

36. W. G. Petefish et al., “High-Performance Laminated Chip Package Technology”, The Magazine of High-Density Interconnect, HDI, Vol. 1, No. 7, pp. 20-27, November 1998.

37. R. R. Tummala and E. J. Rymaszewski, "Microelectronics Packaging Handbook", Van Nostrand Reinhold, New York, Chapter 6, 1989.

38. R. W. Woodgate, "The Handbook of Machine Soldering SMT and TH", John Wiley & Sons, New York, Chapter 11, 1996.

39. J. W. Carbin, “Better Flip Chip Underfill Throughput”, The Magazine for Electronic Assembly, SMT, Vol. 13, No. 1, pp. 64-68, January 1999.

40. A. J. Babiarz, “Underfill Provides Flip Chip Protection”, Advanced Packaging, Vol. 7, No. 7, pp. 34-36, September/October 1998.

41. N. W. Pascarella and D. F. Baldwin, “Cost Analysis of Low Cost High Throughput Next Generation Flip Chip Assembly”, The International Journal of Microcircuits and Electronic Packaging, Vol. 20, No. 4, pp. 571-577, 1997.

42. G. O. Mallory and F. B. Hajdu, "Electroless Plating: Fundamentals and Applications", American Electroplaters and Surface Finishers Society, Orlando, Florida, Chapter 1, 1990.

43. S. Wolf and R. N. Tauber, "Silicon Processing for the VLSI Era - Volume 1: Process Technology", Lattice Press, California, Chapter 17, 1986.

44. P. R. Harper, “Thermoplastic Die Attach For Hermetic Packaging”, The International Journal of Microcircuits and Electronic Packaging, IJMEP, Vol. 17, No. 4, pp. 408-413, 1994.

Vita

Suwanna Jittinorasett was born in Bangkok, Thailand on August 19, 1975. She received her Bachelor Degree in Electronics Engineering from King Mongkut's Institute of Technology Ladkrabang (KMITL), Bangkok, Thailand in May 1996. After graduating from KMITL, she participated in IC fabrication technology and IC design training program at Submicron Thailand for one year. She joined the Master of Science program in Electrical Engineering at Bradley Department of Electrical and Computer Engineering, Virginia Polytechnic Institute and State University (Virginia Tech), Blacksburg, Virginia in Fall 1998. Since Fall 1998, she has been working in Microelectronics Lab at Virginia Tech where she has been involved in design, processing, and development of microelectronics packaging. Her research interests include array area interconnect and Flip Chip technologies, and reliability and performance testing of Flip Chip assembly.