Polymer-Supported Bridges for Multi-Finger AlGaN/GaN Heterojunction Field Effect Transistors (HFETs)

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Abstract

Current AlGaN/GaN Heterojunction Field Effect Transistors (HFETs) make use of multiple sources, drains, and gates in parallel to maximize transconductance and effective gain while minimizing the current density through each channel. To connect the sources to a common ground, current practice prescribes the fabrication of air bridges above the gates and drains. This practice has the advantage of a low dielectric constant and low parasitic capacitance, but it is at the expense of manufacturability and robust device operation.

In the study described below, the air bridges in AlGaN/GaN HFETs were replaced by a polymer supported metallization bridge with the intention of improving ease of fabrication and reliability. The DC, high frequency, and power performance for several polymer step heights were investigated. The resultant structures were functional and robust; however, their electrical performance was degraded due to high source resistance. The cause of the high source resistance was found to be thinning of the metallization at the polymer step. The effect was more pronounced for higher step heights.

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1) Introduction

Aluminum nitride (AlN), gallium nitride (GaN), and indium nitride (InN), collectively referred to as the III-nitrides, have been the focus of intense scrutiny due to a host of unique properties that make them well suited for numerous applications. The III-nitrides are unique primarily because of their large band gaps. Additionally, it is possible to modify the band gap of a device based on the III-nitride system practically continuously from 1.9 to 6.2 eV. As a consequence of their large band gaps, GaN and AlN have high breakdown fields and low intrinsic carrier concentration. They also have a high theoretical electron drift velocity and a saturation current density. While not without their disadvantages and challenges, the III-nitrides are among the most promising materials to extend the capabilities of semiconductor devices.

Among many of the devices fabricated using the III-nitrides, the AlGaN/GaN Heterojunction Field Effect Transistors (HFETs) has the potential to fill critical future technology niches that require high frequency operation above 100 GHz, high power, high current density, or high temperature. In the literature, HFETs are sometimes cited as High Electron Mobility Transistors (HEMTs); in the interests of consistency and clarity, the former terminology will be used throughout. As the name suggests, the most critical and novel feature of AlGaN/GaN HFETs is the heterojunction interface. At the interface, crystal lattice mismatch and piezoelectric effects spontaneously form a two-dimensional, high-mobility electron gas; consequently, charge carrier transport is vastly improved over bulk crystals.

For high-power, high-frequency transmitter and amplifier applications, practical integrated circuits incorporating AlGaN/GaN HFETs are necessary. In order to achieve sufficient power densities, multi-fingered HFETs have been used in the past to maintain a relatively small chip area but increase the gate length and the maximum output power. In order to provide interconnects to all of the elements, multi-finger HFETs have required air-bridge structures. Historically, the air-bridge structures are difficult to fabricate and unreliable. Furthermore, the structures prevent or limit top-side cooling. Looking forward to eventual commercial implementation, air bridge structures are not a viable solution. This thesis describes an alternative process that simplifies the fabrication, improves the reliability, and allows for topside cooling of AlGaN/GaN HFETs.

2) Literature Review

2.1) III-Nitrides

The III-nitrides, consisting of AlN, GaN, and InN, differ fundamentally in physical, crystallographic, electric, optical, and piezoelectric properties from traditional group IV and III-V semiconductors. For example, Figure 1 below illustrates two of the most important differences which set III-nitrides apart: basal lattice constant and band gap. In general, the III-nitride have a comparatively large band gap and small basal (a_o) lattice constant. The emission band from 1.65 eV to 3.1 eV denotes the approximate energies of the visible electromagnetic spectrum. The figure also infers a strong correlation between crystallographic and electrical properties that will be discussed in detail in the subsequent sections.

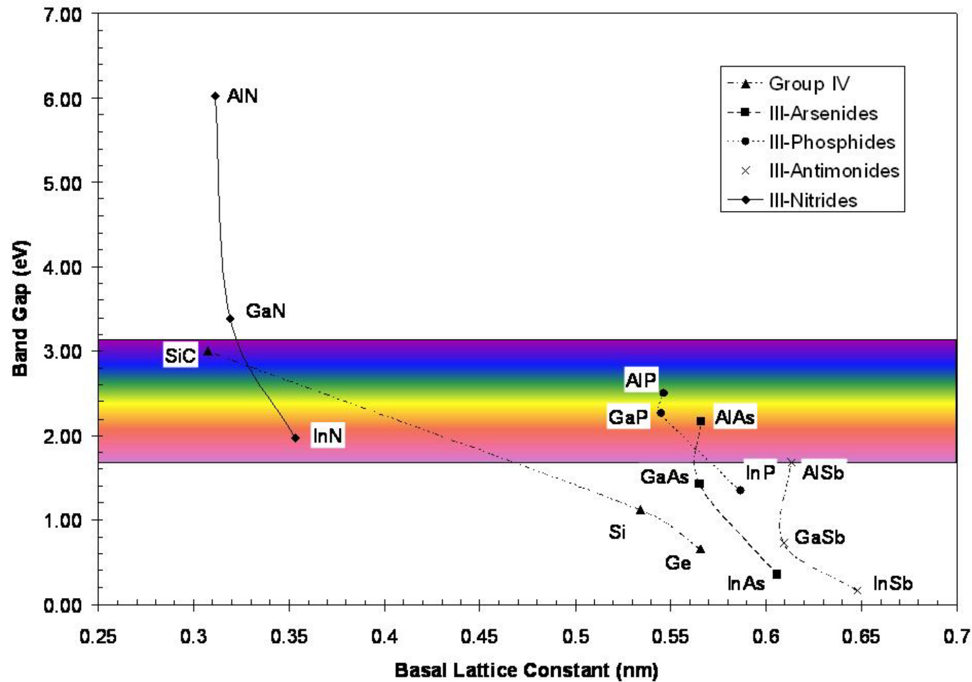

Figure 1: Band Gap vs. Basal Lattice Constant for Common Semiconductors[1,2]

2.1.1) Crystal Properties and Alloying Among III-Nitrides

In contrast to more widespread III-V semiconductors pictured on the right in Figure 1, the III-nitrides most stable crystal structure is a wurtzite hexagonal structure (space group $P6_3mc$). Figure 2 shows a schematic of the wurtzite structure in GaN, but AlN and InN crystal structure would look identical. The crystal schematic is oriented with the c-plane perpendicular to the

page, as indicated by the Miller index on the left. Furthermore, the figure is an example of a Ga-faced crystal. Because the $P6_3mc$ does not have inversion symmetry, the inverse case is called N-faced and is not crystallographically equivalent.[4]

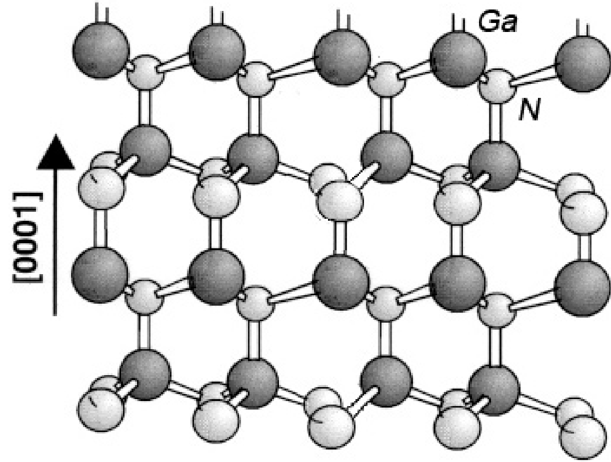

Figure 2: GaN Wurtzite Structure [4]

The structure differs from the zincblende cubic structure (space group F43m) only in its orientation to the growth plane and stacking order. The stacking order in the <0001> direction of a wurtzite crystal is ABABAB, whereas the stacking order is ABCABCABC in <111> zincblende crystals. Because of these similarities, it is common to find coherent zincblende structures in bulk wurtzite crystals because of stacking faults. Furthermore, specific growth conditions and substrates can induce bulk growth of zincblende crystals, but the crystal quality of zincblende III-nitride thin films tends to be inferior. This review will only concern itself with the properties of hexagonal III-nitrides because virtually all III-nitride devices are constructed on the wurtzite allotrope. Some of the salient crystallographic properties of the III-nitrides are summarized in Table 1.

Table 1: III-Nitride Wurtzite Crystal Properties [3,4]

	AlN	GaN	InN
Lattice Constant, a_o (nm)	0.3112	0.3189	0.3540
Lattice Constant, c_o (nm)	0.4982	0.5185	0.5705
c_o/a_o	1.6010	1.6259	1.6116
Thermal Conductivity ($Wcm^{-1}K^{-1}$)	2.85	2.1	0.45
Thermal Expansion (K^{-1})	$4.2x10^{-6}$	$5.59x10^{-6}$	$3.8x10^{-6}$
Binding Energy (eV)	2.28	2.20	1.98

For structural and electrical reasons, the solubility of the III-nitrides in one another also becomes important in the construction of devices. Figure 3 is a compilation of data by Ambacher from various sources showing the lattice constants and band gaps of various III-nitride alloys. Researchers have had considerable success in fabricating AlGaN and GaInN alloys across the entire compositional range. Other factors, such as growth temperature, crystal quality, and film stress, can limit the compositions applicable to practical devices, but there still remains flexibility to optimize material composition and properties for specific applications.

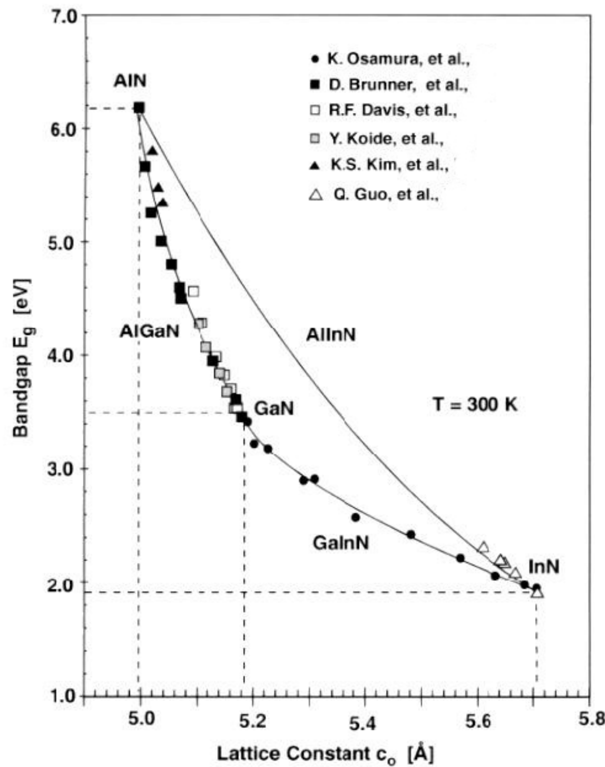

Figure 3: Band gap vs. Lattice Constant for III-Nitrides[4]

However, InAlN alloys are only realizable in dilute solutions. Theoretical studies based on Gibbs free energy of mixing predict a broad miscibility gap even at nominal growth temperatures that makes single phase solutions difficult to fabricate.[5] Fortuitously, most of the projected applications of III-nitride HFETs do not require InAlN alloys. An implementation of the CMOS architecture in HFETs could require InAlN for p-channel HFETs, but most potential applications require high frequency switching which favors the conventional n-channel implementation that requires only AlGaN alloys.

2.1.2) Electrical and Optical Properties

In addition to being structurally distinct, the III-nitrides offer a unique set of electrical and optical properties that enable a broad range of applications. Some of the most important electrical properties of the III-nitrides are summarized in Table 2 below. Silicon (Si) and gallium arsenide (GaAs) are included for comparison.

Table 2: Electrical Properties of III-Nitrides, Si, and GaAs at 300K [1-3]

	AlN	GaN	InN	Si	GaAs
Band Gap (eV)	6.03	3.28	1.97*	1.12	1.424
Direct/Indirect Bandgap	Direct	Direct	Direct	Indirect	Direct
Dielectric Constant	8.5	8.9	15.3	11.7	12.9
Electron Effective Mass (m_o)	0.3	0.20	0.14	0.19	0.063
Breakdown Field (Vcm^{-1})	1.8×10^6	5.0×10^6	-	3.0×10^5	4.0×10^5
Electron Mobility ($cm^2V^{-1}s^{-1}$)	135	1000	1900	1400	8500
Electron Saturation Velocity (cms^{-1})	1.9×10^7	2.0×10^7	3.4×10^7	1.0×10^7	1.2×10^7
Peak Velocity (cms^{-1})	6.0×10^7	2.5×10^7	4.5×10^7	1.0×10^7	2.2×10^7
Intrinsic Carrier Concentration (cm^{-3})	~0	2.9×10^{-9}	300	1.0×10^{10}	2.1×10^6

*There is some controversy over the bandgap of InN

Two applications where the III-nitrides are making the biggest impact are in optoelectronics and RF power electronics. In both cases, the application is dependent on the fundamental properties listed above. In the case of optoelectronics, the III-nitrides and their alloys are direct, large band gap materials, and they allow for the fabrication of efficient photon emitters and detectors across the entire visible spectrum and well into the ultraviolet. For RF power electronics, the high electron peak velocity, high breakdown field, low intrinsic carrier concentration, and relatively high thermal conductivity are particularly attractive. The first two properties are necessary for the very definition of RF electronics, high frequency and high power. The latter two properties, thermal conductivity and intrinsic carrier concentration, are directly related to heat management in power devices. The III-nitrides can not only dissipate more heat than comparable GaAs devices, but they can also function at higher temperatures. Furthermore, the III-nitrides exhibit superior performance at high electric fields. Figure 4 is the result of Monte Carlo simulation based on a three-valley model for the conduction band of various semiconductors, and it shows that the peak electron saturation velocity for the III-nitrides occur at much higher electric fields than in GaAs. The saturation velocity peaks at 65 kV/cm, 140 kV/cm, and 450 kV/cm for InN,

GaN, and AlN, respectively. Silicon has no velocity overshoot because it is an indirect band gap semiconductor.

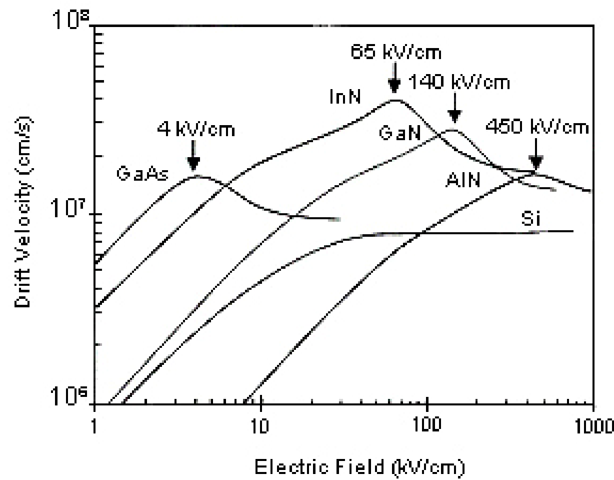

Figure 4:Drift Velocity vs. Electric Field for Various Semiconductors [6]

2.1.3) Spontaneous and Piezoelectric Polarization

Also critical to the performance of AlGaN/GaN HFETs are the coupled effects of structural and electric properties. Because of the lack of inversion symmetry, the wurtzite III-nitrides have piezoelectric properties. However, both spontaneous and piezoelectric polarization, particularly in AlN, is much stronger than in other semiconductors. The salient spontaneous polarization, piezoelectric polarization, and elastic constants for the III-nitrides are listed below in Table 3.

Table 3: Experimental Polarization and Elastic Constants for the III-Nitrides[7-9]

	AlN	GaN	InN
Spontaneous Polarization (C/m^2)	-0.081	-0.029	0.032
Piezoelectric Constants:			
e_{33} (C/m^2)	1.46	0.73	0.032
e_{31} (C/m^2)	-0.60	-0.49	0.97
Elastic Constants:			
E_{11} (GPa)	345	374	190
E_{12} (GPa)	125	106	104
E_{13} (GPa)	120	70	121
E_{33} (GPa)	395	373	182

In Figure 2, with the (0001) planes aligned perpendicular to the page, the planes containing exclusively group III or group V are visible and this arrangement is responsible for the spontaneous polarization. The piezoelectric polarization occurs when the crystal is strained, either by mechanical means or external electric field. For small strains, it is possible to derive a simple mathematical relationship for wurtzite crystals, assuming the crystallographic directions in the basal plane react isotropically:

$$P_{PZ} = e_{31}\varepsilon_z + e_{33}\left(\varepsilon_x + \varepsilon_y\right)$$

Equation 1 [7]

Where e_{31} and e_{33} are the piezoelectric constants listed in Table 3, and ε_x, ε_y, and ε_x are the strain in the x, y, and z directions, respectively. The Poisson relationship in wurtzite crystals given by:

$$\frac{c - c_o}{c_o} = -2\frac{E_{13}}{E_{33}}\frac{a - a_o}{a_o}$$

Equation 2 [7]

Where E_{13} and E_{33} are the elastic constants listed in Table 3, a_o and c_o are the relaxed lattice constants, and a and c are the strained lattice constants. Combining Equation 1 and Equation 2 yields the expression:

$$P_{PZ} = 2\frac{a - a_o}{a_o}\left(e_{31} - e_{33}\frac{E_{13}}{E_{33}}\right)$$

Equation 3 [7]

The total polarization is the sum of the spontaneous and piezoelectric polarization. The role of polarization in AlGaN/GaN HFETs will be discussed in section 2.3.2) Spontaneous Polarization and 2DEG.

2.2) GaN/AlGaN Growth

Marsuka and Tietjen first began growing crystals of gallium nitride in 1969. A number of crystal growth challenges restrained research into potential applications for the III-nitrides until approximately the last decade. Some problems, such as a suitable growth apparatus, large-scale two dimensional crystal growth, and a mechanism for p-doping, have been practically solved for most applications. While significant progress has been made in the areas of background concentration of n-dopant impurities, non-native substrate growth, and crystal quality, they continue to challenge research and development of III-nitrides. [10]

2.2.1) Epitaxial Growth

In order to react bulk gallium with diatomic nitrogen to form a GaN melt and grow boules via the traditional Czochralski method, the temperature of the reaction chamber must be over 1600°C. Furthermore, nitrogen is a volatile molecule, and the partial pressure of nitrogen at 1600°C inside the growth vessel would have to be over 15 kbar to prevent desorption of nitrogen from the melt.[11] These conditions are prohibitively difficult and expensive to achieve; therefore, commercial quantities of bulk crystal GaN are unobtainable via traditional crystal growth methods. Alternatively, modern epitaxial techniques can provide very good crystal purity, crystal quality, and flexibility. The primary methods employed are Metal-Organic Vapor Phase Epitaxy (MOVPE) and Molecular Beam Epitaxy (MBE).

Molecular beam epitaxy (MBE) initially enjoyed significant advantages over other methods of fabrication. MBE takes place in a chamber under ultra-high vacuum (approximately 10^{-10} bar). The solid reactants are supplied by elemental targets, where atoms are excited through thermionic or electron beam emission. The flux rate is primarily controlled by the energy input from an RF coil or an electron beam. Reactants can also be injected in the gas phase through mass control valves. The resultant "molecular beams" are directed on to a heated substrate and react to form the desired film. The various sources can be shut of and turned on rapidly using shutters, allowing MBE to comfortably make abrupt composition changes within a monolayer. Because the system is at ultrahigh vacuum, MBE had the first in-situ thickness measurements using an electron beam technique, reflection high-energy electron diffraction (RHEED). Additionally, the growth temperature for GaN in MBE is approximately 400 degrees Celsius less than MOVPE, so there is additional flexibility in creating novel structures. However, MBE has several inherent drawbacks. The ultra-high vacuum requires multi-stage cryogenic vacuum systems. Deposition rates for MBE are approximately 500 nm per hour, relatively low compared to MOVPE. Furthermore, source material replacement and maintenance inside the ultra-high vacuum chamber is tedious and time consuming. Despite being very competitive with MOVPE in layer quality, all of the drawbacks of MBE contribute to a low throughput for MBE growth, and MOVPE is currently the dominant means of producing III-nitride compact thin films. [12]

With the maturation of the technology, MOVPE has overcome many of its initial limitations while maintaining its inherent advantages over MBE. A schematic of a single wafer

MOVPE system for III-nitride growth is shown in Figure 5. The group III elements are delivered by organic molecules with low vapor pressures. The most common molecules have three methyl groups bonded to a central group III atom. The group III reactants are stored as liquids, and the carrier gas, usually hydrogen or nitrogen, is bubbled through the liquid. The typical dopants can either be delivered as a gas, in the case of silane (SiH_4), or as a liquid suspended in the carrier gas, in the case of biscyclopentadienyl magnesium ($MgCp_2$). When the group III reactants and dopants reach the reaction chamber, they are mixed with ammonia. Ammonia is almost always the nitrogen source because it is inexpensive and relatively safe, but the stability of the molecule is also a disadvantage. In order to crack the N-H bonds in ammonia, the substrate temperature must be approximately 1000°C. The gas mixture is flowed over the heated substrate, where it reacts to form the epitaxial film. The reaction products, unused reactants, and carrier gases are removed and burned in a disposal unit. The cooling water prevents the reaction vessel walls from heating up sufficiently to allow crystal growth on the walls of the reactor, rather than on the substrate. Wafers are inserted and removed from the far end of the reaction vessel. To keep the environment free from contaminants, the end of the tube is often contained in a positive pressure nitrogen glove box. Therefore, it is possible to insert and remove wafers without directly exposing the reaction vessel to ambient air. [11]

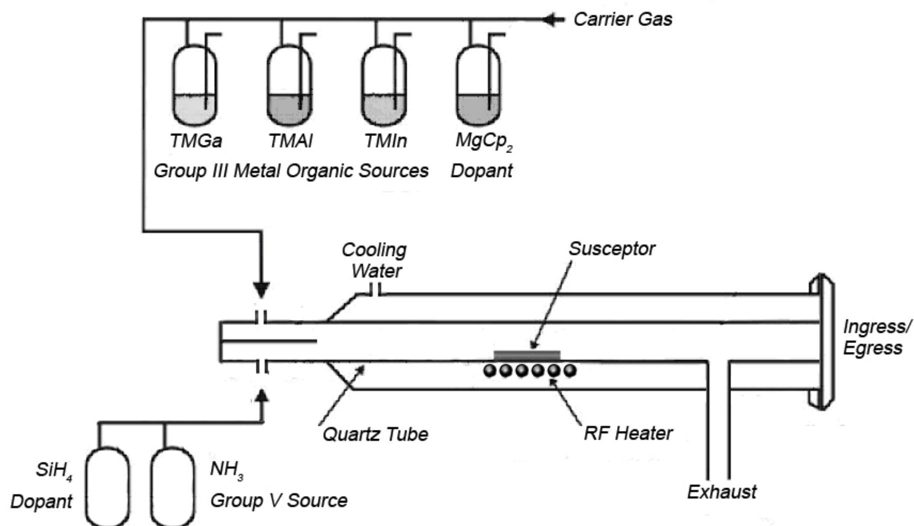

Figure 5: Schematic of a Single Wafer MOVPE System Configured for III-Nitride Growth [11]

MOVPE has inherent advantages over MBE because it is typically done at near atmospheric pressure (300-700 torr). Vacuum systems are simplified and the reaction vessel is a high-purity quartz tube rather than a pressure vessel. The source materials are kept outside of the sealed environment and transferred to the reaction chamber in small amounts as needed. When the canister runs out of reactant, it is a quick and straightforward process to replace the canister with a new one. Deposition rates of 1-5 μm per hour are readily obtained because of the higher concentration of reactants and higher reaction temperature than in MBE growth. However, MOVPE is not without its drawbacks. The reactants are very expensive compared to the sources for MBE, and the reactants for MOVPE tend to be volatile, flammable, and toxic, which creates major safety concerns. Additionally, the process control for MOVPE is far more complex than for MBE because there are many more variables. Computer modeling has had some success anticipating the flow over the substrate and the reaction kinetics on the surface of the substrate, but much of the process control for MOVPE is empirically determined.

Some of the initial drawbacks of MOVPE involving single atomic layer control and in situ monitoring have been resolved. Early in the development of MOVPE, it was difficult to change the composition of the film abruptly. Increased knowledge of the process and general improvements in technique have made abrupt composition changes possible without major modification to the basic MOVPE design. One of the most tangible advantages that MBE had early on was the ability to observe the film in situ using an electron beam. This option was not available for MOVPE because the electron beam would attenuate in the near atmospheric pressure environment. Optical ellipsometry is the most common method for detecting film thickness in-situ for MOVPE. In order to make a thickness measurement, the indexes of refraction for the ambient, the epitaxial film, and the substrate must be known. The incident polarized light is reflected at various intensities according to the quality of interface and the angle of incidence. The reflected light from each interface interfere constructively and destructively in a periodic pattern, and a three phase model (air/epitaxial layer/substrate) is applied to determine the epitaxial layer thickness. Other techniques, like x-ray diffraction, have been coupled to the growth chamber to extract more in-situ information about the crystal quality and surface condition of the epitaxial film. [11]

The thermodynamic driving force for the creation of III-nitrides on the substrate at growth temperature is very large. For example, the enthalpy of formation for GaN at 1000^oC is

estimated at 80 kcal/mol. However, the actual reactions on the surface are more complex and strongly dependent on reactant adsorption, product desorption, surface diffusion, and kinetics. All of these variables have Arrhenius-type dependencies on temperature. Each has a different rate constant, so they manifest as different regimes as the growth temperature changes, as Figure 6 illustrates conceptually. The thermodynamically limited growth rate decreases with temperature because the formation of GaN is an exothermic process, and by the Le Chatelier principal, the system will resist adding more thermal energy. However, the surface kinetics growth rate increases as the temperature increases because it makes chemical interactions more favorable. Because mass transport is primarily determined by flow rate and partial pressures of the reactant gases, it is relatively insensitive to temperature. Therefore, the optimum temperature to get the highest deposition rate is neither too high, limiting the thermodynamic case, nor too low, limiting the surface kinetics case. [12]

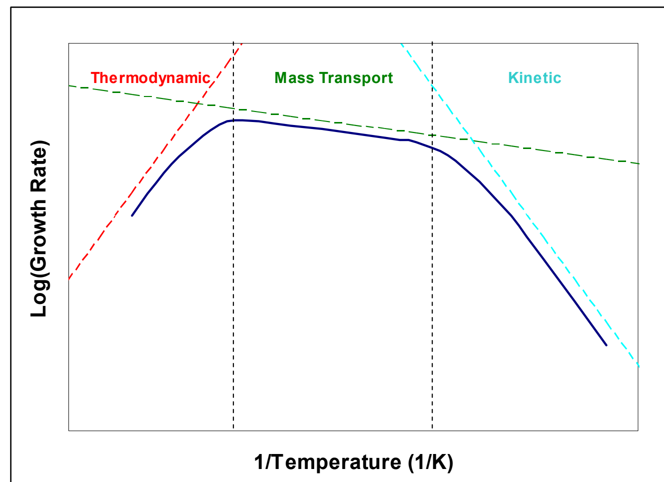

Figure 6: Arrhenius Dependence of Growth Rate on Different Growth Modes [12]

Studies have shown that the rate-determining step at optimal growth temperature is primarily driven by mass transport, more specifically the arrival of the group III element on the surface of the substrate. Therefore, in order to ensure a compact, relatively defect-free layer, MOVPE is most often done in a nitrogen-rich gas mixture.

2.2.2) Substrates

Due to the difficulty in fabricating native GaN substrates, III-nitride devices are grown on non-native substrates. There are several important factors that contribute to selecting a III-nitride substrate, and no material is ideal for every application. Among the most important, the lattice

parameter of the substrate must closely match the epitaxial film. Furthermore, the substrate material must be chemically and mechanically stable at 1000-1100°C in an ammonia atmosphere, the typical growth conditions for GaN. Ideally, the coefficient of linear expansion of the substrate and GaN should also be closely matched. After deposition, the III-nitride film and substrate are cooled from 1000-1100°C to room temperature. Even small differences in expansion coefficient causes additional stress and can result in the film cracking, a phenomenon well documented in III-nitride growth. Additional constraints on the substrate are due to end use and device considerations. In order to make production-scale devices possible, a substrate should be readily available in 50 mm or larger wafer size at relatively low cost. A substrate with a high thermal conductivity increases device lifetime and allows devices to operate at higher power densities. For optoelectronic applications, the substrate should have a large bandgap and a high index of refraction so the photons generated in the active layers of the film are not absorbed by the substrate. For most applications, an electrically insulating or semi-insulating substrate is best, but certain optoelectronic applications could benefit from an electrically conductive substrate. Table 4 introduces several of the substrates that have been investigated, and GaN is listed in the last column as a reference.

Table 4: Properties of Substrates for III-Nitride Growth [1,4,13-16]

	Sapphire	6H-SiC	Si	ZnO	GaN
Space Group	R3c	$P6_3mc$	Fd3m	$P6_3mc$	$P6_3mc$
a_o (nm)	0.4759	0.3081	0.5430	0.3252	0.3189
c_o (nm)	1.299	1.512	-	0.5213	0.5185
Thermal Conductivity ($Wcm^{-1}K^{-1}$)	0.28	3.3	1.3	1.35	2.1
Thermal Expansion Coefficient (10^{-6} K^{-1})	7.3	4.46	3.59	2.9	5.59
Bandgap	-	3.0	1.12	3.2	3.28
Index of Refraction	1.7	2.5	3.42	2.2	2.3

Zinc oxide (ZnO) offers the best lattice match with GaN, but ZnO reacts with GaN above 500°C. Using alternative growth processes like pulsed laser deposition and atomic layer deposition, it is possible to create compact films, but the quality is not competitive with gas phase processes. Molecular beam epitaxy can create excellent quality GaN films on ZnO, but

scalability to commercial level processing is still an issue.[14] Furthermore, there is no pre-existing market for single crystal ZnO wafers, so they are difficult to obtain in any size and quantity. Silicon carbide (6H-SiC) is very stable over the growth temperature and offers an excellent fit with the properties of GaN, including lattice mismatch and thermal expansion coeffiecient. It also has a high thermal conductivity, large bandgap, and semi-insulating. However, wafers of SiC are currently limited to 50 mm and are expensive. Silicon carbide is used in a small number of devices where high current densities and resistive heating are a major concern. Silicon (Si) is the antithesis of SiC in virtually every respect. It was investigated because of the availability Si wafers up to 300 mm with very low cost, and successful growth on Si could lead to more inexpensive and versatile "system on a chip" (SOC) applications. Unfortunately, the large lattice mismatch and the smaller thermal expansion coefficient cause relatively poor quality layers despite elaborate surface preparation techniques. Sapphire (Al_2O_3) is most common substrate for most applications because it offers a compromise on ease of use, cost, and film quality. Despite the relatively large lattice mismatch and differential in thermal expansion coefficient, modern growth techniques, like two-step growth described in the next section, allow the growth of good quality epitaxial layers. The main disadvantage of the sapphire substrate is the low thermal conductivity, which causes heat management concerns for high current density devices.[4,16]

2.2.3) Two-Step Growth

The lattice mismatch and the difference in thermal expansion coefficients between the GaN film and non-native substrates cause large internal stresses that are relieved through the formation of dislocations. Before the advent of two step growth by Amano and Akasaki in 1988, the dislocation density of GaN epitaxial films exceeded 10^{11} cm^{-2}. [17] The dislocations can have either edge or screw character, but they are typically aligned normal to the surface of the film. The dislocations are typically modeled as one dimensional charged bodies that impede free carrier mobility. They also act as electron/hole recombination centers, contributing to a longer wavelength parasitic emission, referred to as yellow luminescence. All of these effects reduce overall efficiency of the device.[4,19]

The most common method of improving wetting and relieving a portion of the lattice mismatch is to deposit a 10-50 nm nucleation layer of GaN or AlN at a lower temperature (550-

650°C) between the substrate and the bulk GaN layers, grown at 1000-1100°C. The low temperature AlN or GaN layer grows first as three dimensional islands, which eventually coalesce to form a suitably flat layer with a lower surface energy that aids high quality two-dimensional growth at the higher growth temperature.[17] A GaN nucleation layer grown on sapphire, imaged with a transmission electron microscope (TEM), is shown in Figure 7 below. The nucleation layer islands are visible, but they have coalesced to form a contiguous layer. Compared to the sapphire substrate, the nucleation layer has a relatively low crystal quality, and the various coherent and non-coherent phases present in the nucleation layers have been documented by a number of detailed studies.[20]

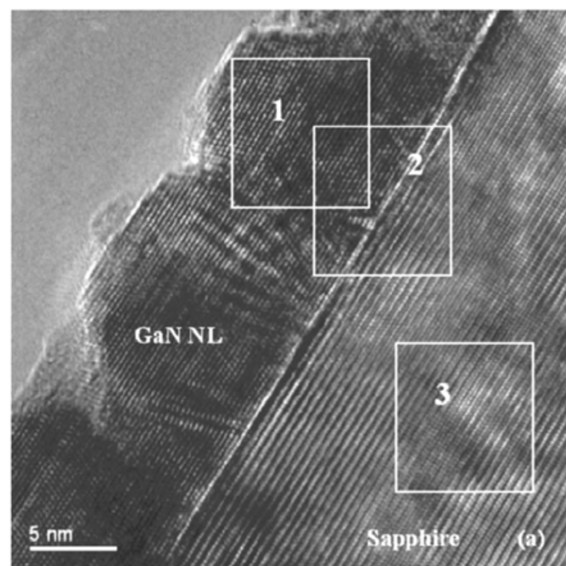

Figure 7: GaN Nucleation Layer Grown on Sapphire [20]

Two-step growth has reduced the dislocation density in GaN thin films to approximately 10^{8} cm^{-2}. Despite this additional growth step, atomic level defects, particularly stacking faults, are common due to the initial non-correlated growth of islands. The islands have the same crystal structure, but not necessarily the same stacking order. Stacking faults act as initiation sites for dislocations which propagate through the subsequent GaN layers.[20] Despite these defects, two-step growth was a major advance in the development in the growth of III-nitride devices.

2.2.4) Doping and Background Impurities

In order to make devices, chemical dopants on the order of parts per million are deliberately added to obtain desired electronic properties. The typical n-type dopant in the III-

nitrides is silicon (Si). The typical p-type dopant is magnesium (Mg). Because the partial pressure of ammonia is higher than the other reactant gases during film growth, vacancies are statistically more probable at the group III lattice sites. Gallium nitride, like many other compound semiconductors, suffers from self-compensation; therefore, low resistivity in GaN is often difficult to achieve. At high dopant concentrations, the nitrogen vacancy becomes more energetically favorable and can negate any effect of increased dopant concentration. Despite this, n-doping with silicon is relatively straightforward in the III-nitrides. However, p-doping in the III-nitrides remained elusive until 1989.

Even though special care is taken to use the purest reactants and the cleanest equipment in MOVPE, impurities inevitably are included in the film as they grow. Many have deleterious effects on the electrical properties, creating traps against electron flow that interfere with efficient operation of the device. The most common undesirable impurities are oxygen, hydrogen, and carbon. The oxygen inclusions come primarily from the small quantity ambient atmosphere that inevitably leak into the reactor. Carbon and hydrogen are in the group III reactants. Hydrogen is also present in the nitrogen source, ammonia. Oxygen and carbon are troublesome inclusions because they create discrete energy levels near the center of the bandgap where electrons and holes can recombine but not emit a photon. As long as these inclusions are kept to a minimum, the device can still function; however, hydrogen inclusions can actually prevent the device from working at all. In p-type GaN, the intentional dopant, magnesium atoms, are neutralized by the hydrogen impurities.[21]

Amano, Kito, Hiramatsu, and Akasaki were the first to produce p-doped GaN by scanning an epitaxial film with magnesium in a scanning electron microscope. After the GaN was imaged, the resistivity of the treated film dropped several orders of magnitude to 35 Ω-cm and the hole carrier concentration was $2x10^{16}$ cm^{-3} after treatment.[22] Another group, consisting of Nakamura, Mukai, Senoh, and Iwasa, quickly followed up with an alternative. They were able to anneal magnesium doped GaN films at $700^{o}C$ in a nitrogen atmosphere and produce even better quality p-doped GaN with a hole concentration was $3x10^{17}$ cm^{-3}.[23] The mechanism behind this was finally put forward by a group consisting of Van Vechten, Zook, Horning, and Goldenburg. They cite the fact that gallium nitride will self-compensate through the most energetically favorable means. At MOVPE growth temperatures and partial pressures, the most energetically favorable is the formation of an H^{+} antisite defect to compensate for the

magnesium acceptors. The electron beam treatment and the thermal treatment around 700°C are enough energy to activate hydrogen diffusion, but they do not supply sufficient energy to activate other diffusion processes that allow self-compensation mechanisms, like nitrogen vacancies, to play a significant role. During a thermal or an electron beam treatment, the hydrogen ions become hydrogen atoms and rapidly diffuse to the surface of the semiconductor. Once on the surface, the atoms react to form H_2 molecules, and the molecules are desorbed to the atmosphere. Despite these advances, high concentration p-doping is still difficult with III-nitride semiconductors compared to n-doping. [24]

2.3) Heterojunction Field Effect Transistor (HFET)

Heterojunction Field Effect Transistors were first conceived in the aluminum gallium arsenide (AlGaAs) material system in 1980 by Mimura et al at Bell Laboratories. Despite variations on the structure and materials system, the defining feature of an HFET is a 2 dimensional electron gas (2DEG) at the interface between a comparatively large band gap semiconductor and a smaller band gap semiconductor. A two dimensional electron gas has a higher sheet carrier concentration and higher carrier mobility than either of the surrounding bulk semiconductors. This region of high conductivity can be exploited to make transistors with excellent high frequency performance. The general structure of an AlGaN/GaN HFET is shown in Figure 8 below. A low temperature nucleation layer (not shown) is grown as described in section 2.2.3, followed by 1-3 µm of GaN buffer layer, and lastly a 10-30 nm layer of AlGaN. The source and drain are ohmic contacts, and the gate contact is a metal-semiconductor Schottky contact.[25]

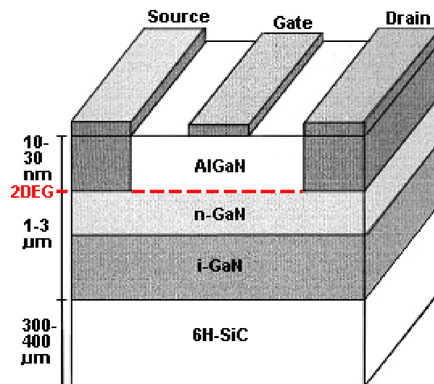

Figure 8: Basic HFET Design [26]

2.3.1) Band Diagrams and Carrier Transport

The two dimensional electron gas (2DEG) is located at the interface between the AlGaN and GaN layers. The band diagram in Figure 9 below shows an n-doped AlGaN/GaN HFET under a small negative bias (qV_g). The work function of the metal ($q\Phi_m$) is determined by the material used. The conduction band (E_C) has a discontinuity at the interface referred to as the conduction band offset (ΔE_C). The valence band has a discontinuity referred to as the valence band offset (ΔE_V). For an AlGaN/GaN interface the ΔE_C is approximately 1.02 eV, and the ΔE_V is equal to 0.4 eV.

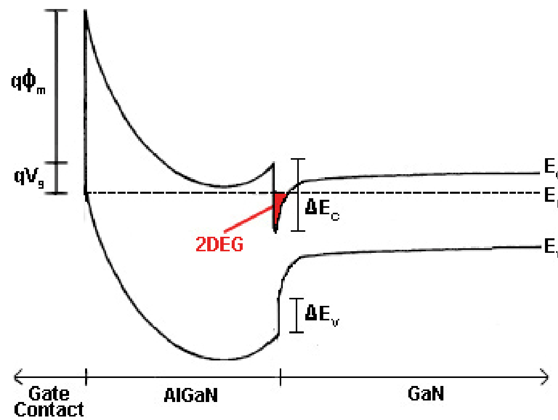

Figure 9: Band Diagram for the Gate Contact-AlGaN-GaN Heterojunction[7]

The 2DEG occurs at the heterojunction discontinuity in the conduction band below the Fermi energy (E_F). In the 2DEG layer, the electrons are confined to discrete quantum states and exhibit enhanced charge carrier properties, among them a higher mobility, as shown in Figure 10. Because the electrons are in confined quantum states, the interference from coulombic scattering is reduced, and the mobility is much higher in the 2DEG than in bulk material.[26,27] The effect is most pronounced at cryogenic temperatures, but phonon scattering reduces the benefits of 2DEG over bulk transport as the temperature increases. [28,29]

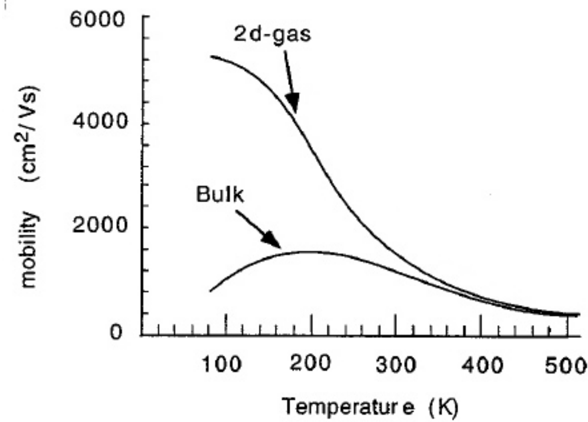

Figure 10: Electron Mobility vs. Temperature for AlGaN/GaN HFETs [4]

2.3.2) Spontaneous Polarization and 2DEG

The first HFETs made with the AlGas/GaAs system produced the free electrons to populate the 2DEG by n-doping the AlGaAs layer. However, the strong piezoelectric polarization and lattice mismatch between AlGaN and GaN interact to form an electron gas at the interface even in the absence of intentional doping. It is possible to estimate the sheet carrier concentration using the equations found in the earlier section on piezoelectric properties of the III-nitrides. Studies have shown that the non-linear effects in dilute AlGaN alloys are minute, so it is possible to linearly interpolate the physical constants for an $Al_xGa_{1-x}N$ alloy with high accuracy.[7]

$$a_o = (-0.077x + 3.189)10^{-10}\ m$$

Equation 4

$$C_{13} = (5x + 103)\ GPa$$

Equation 5

$$P_{SP} = (-0.052x - 0.029)\ Cm^{-2}$$

Equation 6

$$c_o = (-0.203x + 5.189)10^{-10}\ m$$

Equation 7

$$C_{33} = (-32x + 405)\ GPa$$

Equation 8

$$\varepsilon = (0.4x + 8.5)$$

Equation 9

Additionally, thick AlGaN layers or high aluminum content in the alloy can cause partial relaxation in the AlGaN layer, reducing the piezoelectric response. Figure 11 shows the critical thickness of the AlGaN layer as a function of aluminum concentration. Experimental data showing pseudomorphic and partially relaxed samples are plotted with several theoretical models. The inset shows a graph of the relaxation constant vs. the aluminum concentration.

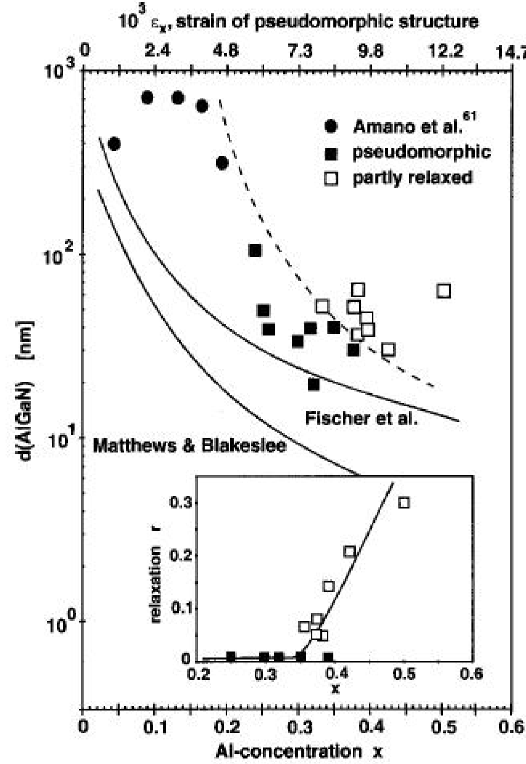

Figure 11: Critical Thickness and Relaxation Constants for $Al_xGa_{x-1}N$ [9]

Taking the relaxation constants from the graph in Figure 11 and applying the correction to Equation 3, it is possible to calculate the total polarization of the AlGaN layer as a function of aluminum concentration:

$$P_{tot} = 2(r(x)-1)\left[\frac{a(x)-a(GaN)}{a(x)}\right]\times\left[e_{31}(x)-e_{33}(x)\frac{E_{13}(x)}{E_{33}(x)}\right]+P_{sp}(x)$$

Equation 10 [7]

Where r(x) is the relaxation constant from the graph in Figure 11. The spontaneous polarization P_{sp} can either be positive if it is Ga-faced or negative if it is N-faced (See Figure 2). In addition to the total polarization, the sheet carrier concentration is also dependent on the relative dielectric constants (ε), the size of the conduction band discontinuity (ΔE_c), the Fermi level (E_F) and the work function between the two semiconductors (φ_b). Taking all of these into account, the final model developed by Ambacher et. al. predicts the sheet carrier concentration to be:

$$n_s = \frac{P_{tot}}{e} - \left(\frac{\varepsilon(GaN)\varepsilon(x)}{d(AlGaN)e^2} \right) \left[e\phi_b(x) + E_F(x) - \Delta E_C(x) \right]$$

Equation 11 [7]

Ambacher computed the sheet concentration for various compositions as a function of depth. Figure 12 is the theoretical CV profile showing the shape and location of the 2DEG based, in part, on the calculations shown above. The AlGaN alloy was 33% AlN and 67% GaN, and the thickness of the AlGaN layer was assumed to be 30 nm. The calculated sheet carrier concentration is 1.0×10^{13} cm^{-2}.

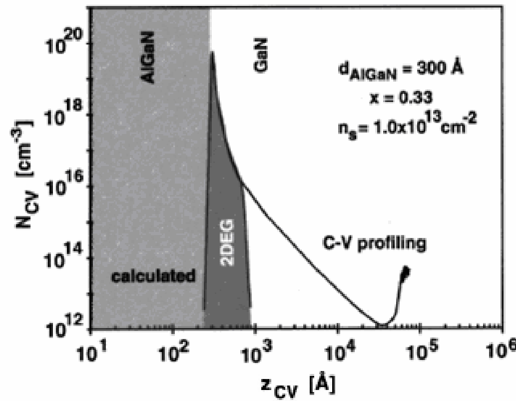

Figure 12: Calculation of Density of the 2DEG at a $Al_{0.33}Ga_{0.67}N$ Undoped Interface [9]

In the undoped case, the 2DEG is located exclusively on the GaN side of the interface. However, in order to increase the sheet carrier concentration of the 2DEG and increase the conductivity of the channel, the AlGaN layer is often n-doped with silicon (Si). Figure 14 is result of the same parameters in Figure 13, but with 1×10^{19} cm^{-3} Si doping. The doping causes a 20% increase in the sheet carrier concentration.

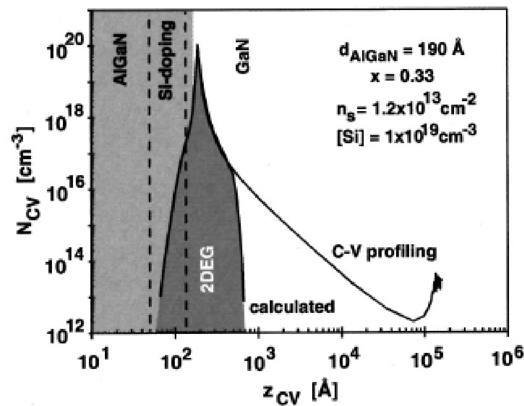

Figure 13: Density of the 2DEG with 1×10^{19} cm^{-3} Si Doping in the AlGaN Layer [9]

2.3.3) Piezoelectric Polarization and Surface Donor States

The spontaneous formation of the 2DEG at the AlGaN-GaN interface is an asset for the fabrication of HFETs, it is not without its consequences. The two dimensional electron gas is, by definition, a strong concentration of negative charges, and coulombic attraction causes charge segregation in the AlGaN layer. A positive charge forms on the AlGaN side of the interface as electrons, and a net negative charge forms at the free surface of the AlGaN. Figure 14 is a Ga-faced crystal illustrating the charge segregation and the location of the surface donor states. [4]

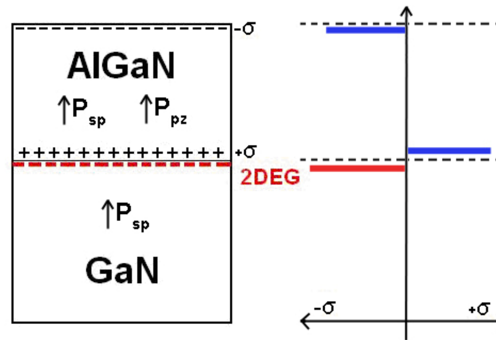

Figure 14: Formation of Surface Donor States in AlGaN [4]

The surface states partially shield the 2DEG from the gate and can trap carriers. Because both of these effects are detrimental to the performance of the device, several research groups have attempted to limit the concentration and mobility of surface states using different passivation materials. The most common employed passivation layer is a silicon dioxide layer. [30,31] Other groups have experimented with rare earth scandides or polymers. [32,33]

2.3.4) Field Effect Transistor Small Signal Model

The small signal model for field effect transistors is a standard 2-port model with a common source. In the simplest form, the steady state model, transient signals do not account for significant error and are neglected. Only the most fundamental aspects, the dependent current source, the source-drain transconductance, and an ideal open between gate and source, are retained. However, HFETs are used at high frequencies and additional elements must be incorporated to account for parasitic and non-ideal behavior. Figure 15 is a diagram of the small signal model which incorporates a gate leakage current, gate-source capacitance, gate-drain capacitance, and drain-source capacitance.

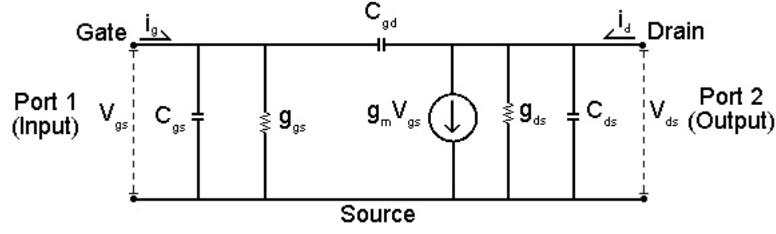

Figure 15: Small Signal Model for High Frequency Transistors[34]

Fundamental performance characteristics, such as transconductance, cut-off frequency, and maximum oscillating frequency, are obtainable by manipulating the characteristics of this circuit. Transconductance (g_m) describes the amplification of the transistor. It is derived in from Ohm's Law:

$$g_m = \left.\frac{i_{d1}}{v_{gs}}\right|_{Vds=0} = \left.\frac{\Delta I_{d1}}{\Delta V_{gs}}\right|_{Vds=const} \approx \left.\frac{\Delta I_d}{\Delta V_{gs}}\right|_{Vds=const}$$

Equation 12 [34]

Where I_{d1} is the current entering the dependent current source and V_{gs} is gate-source voltage. In the final expression, I_{d1} can be simplified to the drain current when g_{ds} is negligible and the frequency is low.

The cutoff frequency (f_T) is defined as the frequency at which the current gain is equal to one when the output port (drain-source) is shorted, and it can be derived from the 2-port model and Kirchoff's Laws:

$$i_g = \dot{i}\omega\left(C_{gs} + C_{gd}\right)v_{gs} - \dot{i}\omega C_{gd} v_{ds}$$
$$i_d = \left[g_m - \dot{i}\omega C_{gd}\right]v_{gs} + \left[g_{ds} + \dot{i}\omega\left(C_{ds} + C_{gd}\right)\right]v_{ds}$$

The current gain evaluated when the source-drain path is shorted is expressed as:

$$G_i = \left.\frac{i_d}{i_g}\right|_{Vds=0} = \frac{g_m - \dot{i}\omega C_{gd}}{\dot{i}\omega\, C_{gs} - \dot{i}\omega C_{gd}}$$

Usually, C_{gd} is neglected because it has a relatively small influence in most cases. If the current gain is equal to one, and the simplified equation is solved for the cutoff frequency:

$$G_i = \frac{g_m}{2\pi f_T C_{gs}} = 1$$

$$f_T = \frac{g_m}{2\pi C_{gs}}$$

Equation 13 [34]

Given this result, a large transconductance and small gate-source capacitance will yield the highest cutoff frequency. In real transistors, the transconductance and gate-source capacitance are most strongly influenced by the gate geometry. A smaller gate length will simultaneously increase the transconductance and decrease the gate-source capacitance, consequently increasing the cutoff frequency.

The maximum oscillating frequency (f_{max}) is defined as the frequency at which the unilateral power gain is equal to one. The unilateral power gain is an idealized condition when the input and output ports are attached to lossless matched loads. As the name suggests, the maximum oscillating frequency is also the maximum frequency that a transistor can be operated. Above this frequency, the transistor ceases to amplify the signal. Simplifying the expression, setting the unilateral gain to one, and solving for f_{max} yields:

$$G_U = \frac{V_{ds} i_d}{V_{gs} i_g}$$

$$G_U = \frac{\left[g_m - \dot{i}\omega C_{gd}\right] v_{gs} v_{ds} + \left[g_{ds} + \dot{i}\omega\left(C_{ds} + C_{gd}\right)\right] v_{ds}^2}{\dot{i}\omega\left(C_{gs} + C_{gd}\right) v_{gs}^2 - \dot{i}\omega C_{gd} v_{ds} v_{gs}}$$

$$G_U = \frac{\left[g_m - 2\pi f_{\max} C_{gd}\right] v_{gs} v_{ds} + \left[g_{ds} + 2\pi f_{\max}\left(C_{ds} + C_{gd}\right)\right] v_{ds}^2}{2\pi f_{\max}\left(C_{gs} + C_{gd}\right) v_{gs}^2 - 2\pi f_{\max} C_{gd} v_{ds} v_{gs}} = 1$$

$$f_{\max} = \frac{f_T}{\sqrt{4 g_{ds} + 2\frac{C_{gd}}{C_{gs}}\left(\frac{C_{gd}}{C_{gs}} + \frac{g_m}{g_{gs}}\right)}}$$

Equation 14 [34]

Despite the multiple dependencies of maximum oscillating frequency, it is clear that parasitic capacitances strongly reduce the performance of the device and the transconductance has a weaker influence on the f_{max} compared to the cutoff frequency.

2.4) Multi-Finger HFETs and Air Bridges

Because of the potential of AlGaN/GaN HFETs to be used in high power applications, the transistors are usually not implemented as single gate devices. In order to increase power output, transconductance, and cutoff frequency, the HFETs are typically "multi-fingered." Multi-finger transistors have multiple sources, drains, and gates connected in parallel. While the design offers distinct advantages in operation, it also adds complexity to fabrication.

2.4.1) Multi-Finger HFET Design

Multi-finger AlGaN/GaN HFETs have the same basic elements as a standard transistor and multi-finger designs can be fabricated on the same substrate with standard devices. The fabrication paths diverge after the standard transistors are finished. The three types of transistors tested are compared after the final standard fabrication step in Figure 16.

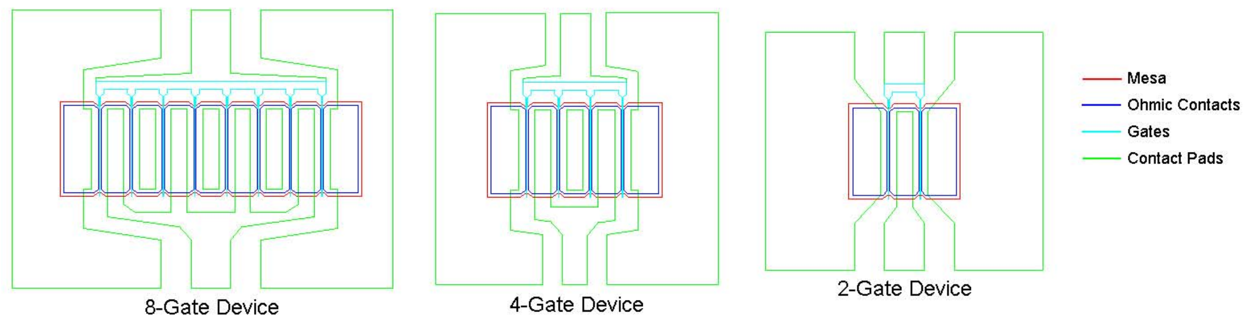

Figure 16: 2-, 4- and 8-Gate HFET Structures

The mesa is the first step, and it electrically isolates each transistor by removing the AlGaN layer except in the active areas. The mesa is followed by fabricating the ohmic source and drain contacts that provide a low resistance electrical path to the electron gas. The gates are deposited next as Schottky contacts to control the channel conductivity. The contact pads are deposited last to give a larger area to attach connections or probes for device operation and testing. The specifics of the fabrication process will be presented in Section 3.1 below. Additional steps can be added to improve device performance, such as a SiO_2 passivation layer on the exposed AlGaN surface between the source and drain. Such measures improve device properties, but are not critical to basic device operation.

After the basic 4-stage process, the standard 2-gate transistor is fully functional, but the 4- and 8-gate transistors are not. Only the two outer current paths are functional on the multi-finger devices because the source contacts in the center are not connected. None of the potential

benefits of multi-finger HFETs can be realize without all of the channels working simultaneously and symmetrically. In order to connect the sources, the typical solution for HFETs has been air bridges.

2.4.2) General Air Bridge Fabrication

The 4- and 8-gate devices in Figure 16 are configured for source-to-source air bridges, in contrast to the less common gate-to-gate air bridges. As the name suggests, a gate-to-gate configuration connects the sources and the drains in the plane of the device, and each gate is contacted to the gate contact pad by air bridges over the source contact. Only the former type, source-to-source air bridge will be discussed in detail because it is the most similar to the polymer bridges designed in the experiment. A scanning electron microscope image (SEM) of a completed transistor with air bridges is shown in Figure 17.

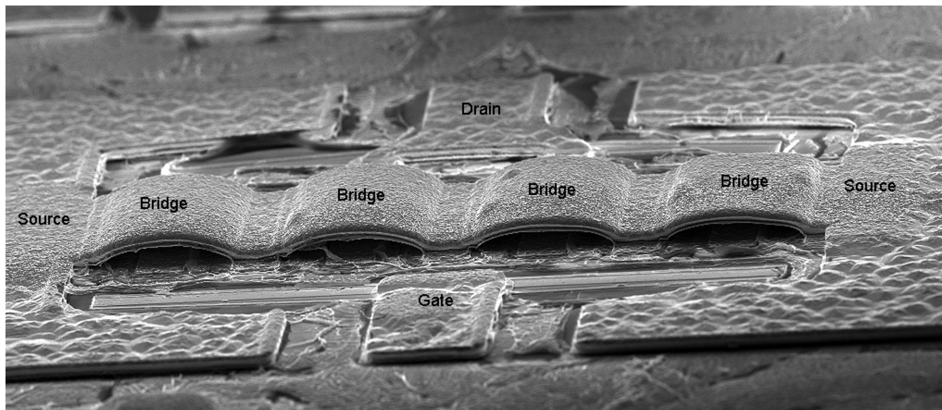

Figure 17: Completed 8-Gate Transistor with Air Bridges

The first step in air bridge fabrication is use a photolithography step to define which areas will be exposed for galvanic metal plating. Once the pattern is developed in photoresist, the photoresist is hardened, and a thin metal layer is deposited on the surface. A second photolithography step protects the bridge pattern from being etched away in the subsequent acid dip. The acid dip removes the metal from the areas that will not be deposited on by the galvanic cell. The galvanic cell thickens the bridge metal and the contacts so the bridge metal can support itself as it arcs over the gates and the drains. The final step is a lift-off that removes the two resist layers, leaving the bridges free-standing with an air gap of approximately 1-3 μm between the bridge and the drain below it. The dielectric constant of air is 1, so the theoretical high frequency performance is quite good because it minimizes the parastic capacitances between the source and drain and the source and gate.

While air bridges are inherently useful because they allow multi-finger HFETs to be built and operated, there are several inherent drawbacks. During the final lift-off, it is necessary to remove all of the photoresist underneath the bridge. If photoresist remains beneath the bridge, the resist will decompose or burn when the device is operated with a high current or high frequency because of resistive heating. Because of the geometry, removing the resist and confirming the resist is completely stripped is difficult. Furthermore, the bridges are fragile. The lift-off or subsequent operation can loosen or weaken the bridge, making the devices relatively unreliable over time. The fragility of the air bridges also prevents direct topside cooling of the devices. Typical cooling schemes only cool from the bottom side of the wafer and might use a forced convection fan on the top. This is inefficient, particularly when a sapphire substrate is used. For power devices, direct topside cooling could offer a second and shorter thermal path. This would allow the same device to operate at lower temperature and handle more power or handle the same amount of power more efficiently.

2.5) Electronic Polymers and Photoactive Resists

2.5.1) Design Considerations for Electronic Polymers

A large amount of research has been conducted on low-k dielectrics for passivation layers between interconnects in VLSI silicon technology. In this case, the primary technology drivers, dielectric constant, thermal stability, and chemical resistance are also critical to incorporation into AlGaN/GaN HFETs.

A low dielectric constant is critical to AlGaN/GaN power HFETs because many potential applications would operate above 10 GHz. In general, a parasitic reactance has a linear dependence with frequency:

$$|X| = \frac{\varepsilon \cdot l \cdot w}{t}\omega$$

Equation 15 [34]

The magnitude of the reactance (X) is dependent of the dielectric constant (ε), the area of the electrodes (length multiplied by width), the thickness (t) of the interceding layer and the frequency (ω). Reducing the length and the width of the electrodes would reduce the capacitance but also increases the resistance and the resistive heating of the device. It is possible to reduce layer thickness, but layers that are too thin will fail in dielectric breakdown because of the large

electric field across the thickness. In order to minimize parasitic capacitances, the dielectric constant must be as low as possible. [35]

AlGaN/GaN HFETs are able to operate at far higher temperatures than Si or GaAs devices. They also function in much higher electric fields and high current densities, meaning they usually run at high temperatures due to resistive heating. To introduce a polymer that changes shape or decomposes at relatively low temperatures is to reduce the capability of the transistor and remove many of the advantages of using AlGaN/GaN HFETs. Therefore, the polymer should be thermosetting with a high decomposition temperature and a relatively low coefficient of thermal expansion. It is also important that thermal cycling will not significantly degrade the polymer over time.[35]

Because further lithography steps are necessary on top of the polyimide film, the cured film must be unaffected by organic solventsb, hydrochloric acid, or hydroxide based photoresist developers. All of these chemicals are used in a subsequent photolithography step, and the polymer must be neither chemically or dimensionally altered by prolonged immersion in the chemicals listed above.[35]

Among the less critical, yet still desirable, features are low moisture absorption, high tensile strength, good adhesion to GaN and different metals, high thermal conductivity, and high dielectric breakdown. Low moisture absorption prevents the polymer from swelling and keeps the dielectric constant low. The adhesion to the materials above and below the polymer is important because the polymer layer could delaminate and device would cease to function. High thermal conductivity allows more efficient cooling of the device. High dielectric breakdown allows the polymer film to be thinner, and reduces the parasitic capacitances. [35]

2.5.2) Polyimide Photoresist Chemistry, Preparation, and Properties

The polyimide photoresist HD-4000 was the best fit for the properties listed in the previous section. It is intended as a thick stress buffer and as a bonding layer for flip chip structures. The exact formulation of the photoresist is proprietary, but the general chemistry and polymerization of polyimides are discussed in Figure 18. The polyimide usually comes from two precursor monomers: a dianhydride and a diamine. Typical examples of the dianhydride are PMDA, BPDA, and BTDA; the diamine could be ODA, Bz, SDA, MDA, or others. A photoactive catalyst, when activated by I-line light exposure, allows a polymerization reaction

between the two monomers to form a polyamic acid at room temperature. The polyamic acid is resistant to dissolution in the developer, formulation PA-400D, but the monomers are removed in the unexposed area by development. After the pattern is rendered in the resist, the resist must be cured at 375°C under a non-oxidizing atmosphere to disconnect the -COOH acid group and form a polyimide.

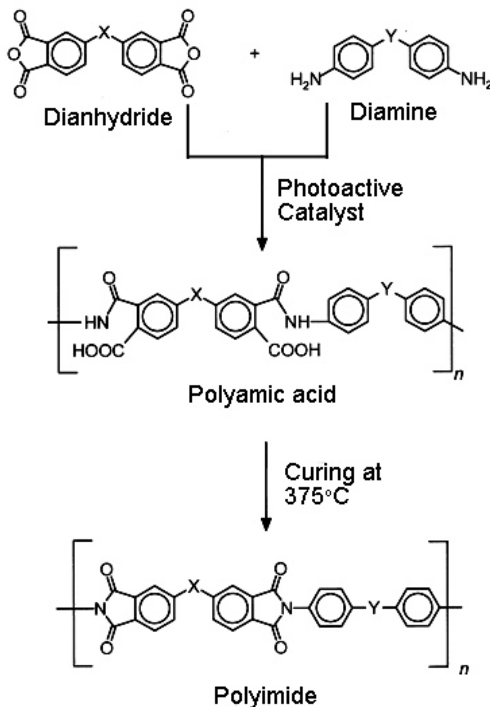

Figure 18: General Polymerization of Polyimide Resists [35]

Another aspect of the fabrication procedure has bearing on the final thickness of the film is the dimensional shrinkage as the sample is processed. The polyimide as spun is nominally 25% solids with a rather high viscosity of 33 m^2s^{-1} at room temperature. The soft bake immediately after spinning removes the solvents, leaving only the solids. The soft bake step is typical of all resists, but after the high temperature curing step, the film thickness is approximately 50% of the soft baked thickness. Because it is a factor that controls capacitances in the operational device, controlling the thickness of the final film is critical to this investigation. Figure 19, provided by the manufacturer of HD-4000, illustrates the thickness loss from the soft bake to the curing step. The resist was spun for 10 seconds at 1000 RPM and then 60 seconds at the desired speed. The samples were all cured at 375°C. [36]

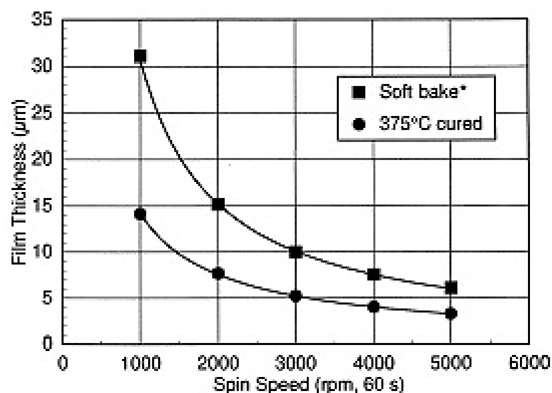

Figure 19: HD-4000 Thickness Data from Manufacturer [36]

The properties of the cured film are excellent for the application. Some of the physical properties are listed in Table 5 below. Additionally, the cured resist is resistant to all organic solvents, bases, and most acids. The only wet etchant that effectively removes cured HD-4000 is a concentrated HF solution. The moisture uptake for polyimides is approximately one percent. Adhesion tests on silicon reported by HD Microsystems conformed to ASTM standards, but polyimides as a class have had adhesion challenges. Low thermal conductivity is a problem with this resist, but it is a necessary accommodation for the material's other excellent properties.

Table 5: Properties of Cured HD-4000 Polyimide Photoresist [36]

Property	**Value**	**Units**
Dielectric Constant (@ 1 MHz)	3.3	-
Glass Transition Temperature	350	^{o}C
1% Weight Loss	420	^{o}C
Decomposition Temperature	530	^{o}C
Coefficient of Thermal Expansion	$35x10^{-6}$	$^{o}C^{-1}$
Tensile Strength	200	MPa
Thermal Conductivity	0.02	$Wcm^{-1}s^{-1}$

3) Experimental Procedure

The goal of the following study was to examine an alternate implementation of multi-finger AlGaN/GaN HFETs. The alternative, polymer supported bridges, attempted to maintain the functionality and performance of air bridges while correcting some of the disadvantages in reliability and fabrication. The polymer supported bridge offered a more robust design fabricated with standard semiconductor processes. Additionally, the polymer supported bridge allowed for topside cooling and packaging. The polymer also provided a passivation layer on the free AlGaN surface that could reduce the effect of the charged surface states and improve device performance. The fabrication and evaluation methods for multi-finger AlGaN/GaN HFETs with polymer supported bridges are presented below.

3.1) AlGaN/GaN HFET Fabrication Process

The sections below introduce the fabrication process of AlGaN/GaN HFETs. The process consists of fabricating four sub-structures: isolation mesas, ohmic contacts, Schottky gate contacts, and contact pads. The full process and the specific parameters used for each step are explained in the appendices.

3.1.1) Epitaxial Layers

The epitaxial layers were grown by Cree on semi-insulating 2-inch 6H-SiC wafers. They were grown with a AlN nucleation layer, a 3 μm buffer layer, followed by a $Al_{0.3}Ga_{0.7}N$ cap layer. In two cases the AlGaN cap layer was nominally undoped, with a n-carrier density of less than $1x10^{16}$ cm^{-3} and a AlGaN layer thickness of 30 nm. The third sample had a 10 nm layer of $2.0x10^{18}$ cm^{-3} doping in the 25 nm AlGaN layer. The epitaxial layers used in this study are summarized in Table 6 below.

Table 6: Properties of Expitaxial Layers Used in the Study

Sample	$Al_xGa_{1-x}N$ alloy	AlGaN Thickness (nm)	GaN Buffer Thickness (nm)	AlGaN Doping (cm^{-3})
F1738	x = 0.3	30	3000	Undoped
F1749	x = 0.3	25	3000	$2.0x10^{18}$
M0566	x = 0.3	30	3000	Undoped

3.1.2) Cutting and Mesa Etching

The wafers were cut into 1 cm squares with a diamond saw. Subsequent to organic and acid cleaning, the first lithography step masked the mesa patterns to isolate individual devices. AlGaN and GaN are particularly resistant to chemical etching, so -the patterned samples were etched to a depth of 300 nm using Ar^+ ion beam etching. The AlGaN layer was, at most, 30 nm deep; therefore, etching 300 nm ensured the high conductivity 2DEG was etched away and the resistance of the underlying GaN layer increased between devices. After ion beam etching, the AlGaN/GaN interface and the 2DEG was located exclusively in the active regions of the transistors.

3.1.3) Ohmic Contacts

After organic and acid cleaning, the second positive lithography step patterned the ohmic contacts for the sources and drains on top of the mesas fabricated in the first step. The ohmic contact metals were applied with e-beam metal evaporation. The ohmic contact metal stack has been used in the literature with good success: 35 nm of titanium (Ti), 200 nm of aluminum (Al), 40 nm of nickel (Ni), and capped with 100 nm gold (Au). In order to be effective as ohmic contacts, the metal stack must be annealed at 900°C for 30 seconds in a nitrogen atmosphere with a rapid thermal annealing (RTA) furnace. This allows the Ti and Al to diffuse through the thin AlGaN layer and make good electrical contact with the 2DEG at the interface with the GaN buffer layer underneath.

3.1.4) Gate Schottky Contacts

The gate length for the transistors in question is 700 nm, with a source-drain gap of 3 μm. This resolution and alignment is achievable with conventional I-line contact photolithography, but it is at the lower limit of the technology. In order to ensure dimensional repeatability and alignment, the lithography for the gate contacts was completed with electron beam lithography. Polymethyl-methacrylate (PMMA) replaced the typical I-line resists because the exposure energies in electron beam lithography are higher. Through proximity correction modeling and experimentation, the nominal electron dosage was 320 $\mu C/cm^2$ with a 120 second development time to achieve acceptable resolution. The gate metal stack was 25 nm of Ni followed by 100 nm of Au, and this metal stack is not annealed. The result was a Schottky barrier with a

sufficiently small leakage current to function as field effect gate to control conductivity in the 2DEG.

3.1.5) Contact Pads

The final step of the basic process was to create larger, low resistance contact pads to allow testing with standard three-prong probes or preparation for wire bonding and packaging. Contact pads were completed with a positive I-line photolithography step and an electron beam evaporator that deposited 25 nm of Ti followed by 300 nm of Au.

3.2) Polymer Supported Bridge Fabrication Process

After the conventional four-step process was complete, a novel process was employed to connect the sources of the multi-finger HFETs. In contrast to traditional air bridges, the process described below did not require a galvanic cell or a difficult lift-off step. As with the previous section, this text only summarizes the fabrication steps. The full description appears in the appendix.

3.2.1) Polyimide Lithography and Annealing

The HD-4000 photoresist was first spun onto samples at various speeds to achieve different thicknesses. Using the data provided by the manufacturer as a guide, different spinning speeds were tested in-house to see the effect on final cured thickness. The results are presented in Figure 20. Similar to the Figure 19, there was a spin-up at 500 rpm for 10 seconds followed by the spin speed and time described, and the samples were cured at 375°C for one hour.

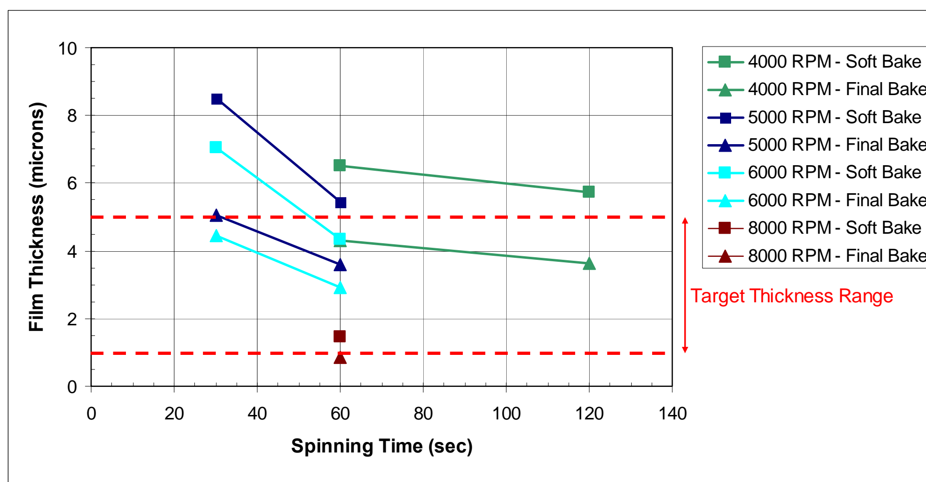

Figure 20: HD-4000 Soft and Cured Film Thicknesses vs. Spinning Time

Less thickness reduction was observed than in the manufacturer's tests. The average thickness reduction was 36.3% for the in-house tests, in contrast to the nearly 50% for the manufacturer's.

After the soft bake, the sample was exposed using a negative mask and developed using the PA-400D formulation provided by the manufacturer. Because it was a negative resist, the required exposure dosage was much higher, 7.0 mW/cm^2 for 45 seconds. Development time varied from 50 to 60 seconds, depending of the thickness of the film. The curing bake profile, shown in Figure 21, was also recommended by the manufacturer. It was done in a sealed Heraus Instruments drying oven with a dry nitrogen flow because the polymer is sensitive to a high oxygen partial pressure at the curing temperature.

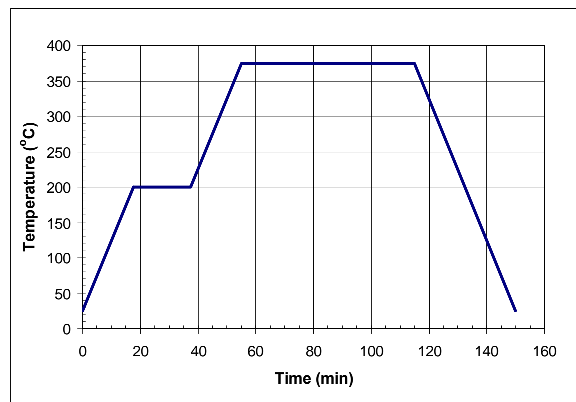

Figure 21: HD-4000 Curing Bake Profile [36]

Ultimately, three cured polyimide thicknesses based on spinning speed were prepared and confirmed with Dektak microprobe measurements. A summary of the samples and their respective polyimide thicknesses appear in Table 7 below.

Table 7: Sample Preparation with Polyimide Thickness

Sample	AlGaN Thickness (nm)	Doping (cm^{-3})	Polyimide Thickness (μm)
F1738	30	Undoped	0.8
F1749	25	$2.0x10^{18}$	3.6
M0566	30	Undoped	4.8

3.2.2) Bridge Metal Contact

The bridge metal contact was applied on top of the polyimide support structure to electrically connect all of the sources. Because of the chemical resistance of the polyimide film, the standard lithography process employed for the ohmic contacts and the contact pads could be

used. The metal stack was 25 nm of Ti followed by 200 nm Au by electron beam evaporation. Lift-off in acetone removed the excess metal. For 4.8 μm thick polyimide films, a second bridge metal pattern and metal evaporation became necessary because of the thinning of the metal on the side walls.

3.3) Evaluation

3.3.1) Hall Effect Measurements

Hall Effect measurements are four point probe measurements made with and without a strong magnetic field passing through it. Through manipulations of Maxwell's equation originally advanced by Van der Pauw, the differences in electric field and current flow can yield important electronic information like the resistivity, carrier mobility, and carrier density of the film.[39]

Resistivity is determined by a single four point probe measurement with the magnetic field off. Four probes are used instead of a two probe measurement because the contact resistance, which may be orders of magnitude larger than the sample resistance, is automatically subtracted out. The voltage drop across the sample (V) is measured when a given current (I) is passed through the sample. The voltage divided by the current equals the sheet resistance. In bulk samples, the thickness of the film must be determined by other means to obtain the resistivity; however, in HFETs, the 2DEG is only a few angstroms thick and has a much higher conductivity than the bulk material. Therefore, it is typical only to report a sheet resistance for HFETs. [39]

Sheet carrier mobility is a critical property to the performance of HFETs. It is derived from the resistivity by comparing the respective voltage drops when the magnetic field is off and on. The carrier mobility is calculated from the measured Hall parameters:

Equation 16 [39]

$$\mu_H = \frac{\vec{E} - R_s \vec{j}}{R_s \left(\vec{j} \times \vec{B} \right)}$$

Where μ_H is the mobility, E is the electric field, R_s is the sheet resistance, j is the current flux, and B is the magnetic field. The sheet carrier concentration also strongly influences the

conductivity of the channel, and it can be isolated using Hall Effect measurements. The carrier concentration is obtained from the data through the definition of resistivity:

Equation 17 [39]

$$n_s = \frac{1}{q\mu_H R_s}$$

Equation 17 neglects the minority carrier, but the intrinsic carrier concentration for GaN is so low at room temperature that the minority carrier has no appreciable contribution to the conductivity, no matter how low the doping concentration.

3.3.2) DC Measurements

The direct current (DC) measurement apparatus, pictured in Figure 22, consists of the device under test (DUT), 2 multiple prong probe tips, a splitter box, an Agilent 8-slot Electrical Measurement Mainframe, and a computer running Agilent's version of Visual Basic (not pictured).

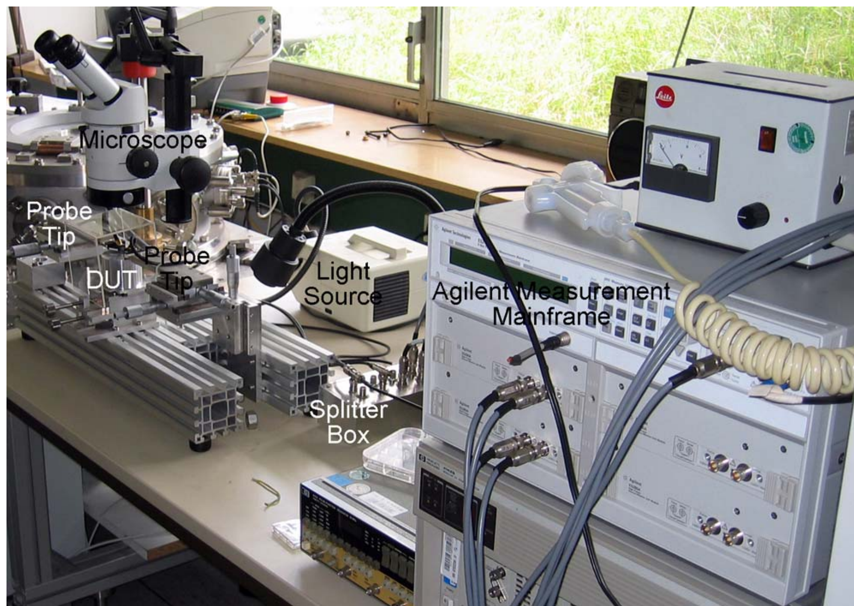

Figure 22: DC Measurement Apparatus, Forschungszentrum Jülich

The mainframe can source up to 1.0 A up to 20 V or up to 0.5 A above 20 V. Therefore, the transistors were measured from 0 to 15 V source-drain bias for gate voltages ranging from +1 V to -6 V. The information extracted from the DC measurements was used to calculate the normalized current response, the threshold voltage, and transconductance (see Equation 12). [40]

3.4.3) S-Parameter Measurements

The S-parameter measurement system, pictured in Figure 23 below, was used to determine the high frequency characteristics of the transistors. For a set source-drain bias in the range of 0 V to 15 V and a gate voltage in the range from +1 V to -5 V, the frequency was varied from 1 GHz to 50 GHz with a 100 mV oscillation by the frequency generator, and the four S-parameters were measured. The loads and the reflection canceling were located as close to the probe tips as possible to minimize external parasitic capacitances and impedances.

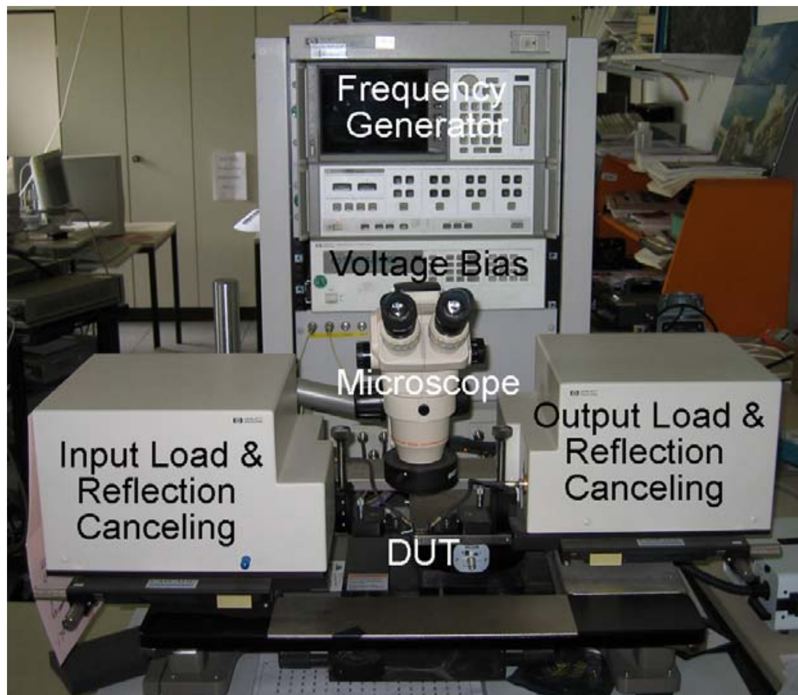

Figure 23: S-Parameter Measurement System, Forschungszentrum Jülich

The S-parameter system works off the 2-port small signal model described in Figure 15. However, it is not straightforward to measure the open and short conditions for such high frequencies because the physical dimensions of the measurement system required would be prohibitively small. Therefore, the measurement system puts a 50 Ω complex load on the input and output ports and measures the complex amplitude of the signal and the reflection from both the input and output. The S-parameters are defined as:

$$S_{11} = \left. \frac{input\ signal}{output\ signal} \right|_{input\ reflection=0} \qquad S_{12} = \left. \frac{output\ signal}{input\ reflection} \right|_{input\ signal=0}$$

$$S_{21} = \left. \frac{output\ reflection}{input\ signal} \right|_{input\ reflection=0} \qquad S_{22} = \left. \frac{output\ reflection}{input\ reflection} \right|_{input\ signal=0}$$

The first measurement extracted from the S-parameters was the stability correction factor, K:

$$K = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}S_{21}|}$$

Equation 18 [41]

From the S-parameter measurements, it is possible to also extract the current gain and the unilateral power gain as a function of frequency for each working point:

$$G_i = |h_{21}|^2 = \frac{-2S_{12}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}$$

Equation 19 [41]

$$G_u = \frac{\left| \frac{S_{21}}{S_{12}} - 1 \right|^2}{2\left(K\left| \frac{S_{21}}{S_{12}} \right| - \mathrm{Re}\left(\frac{S_{21}}{S_{12}} \right) \right)}$$

Equation 20 [41]

From the plots of the current gain and the unilateral power gain, it is possible to draw best-fit regression lines and extrapolate the cutoff frequency and the maximum oscillating frequency for each working point, respectively. The frequencies are compared at each working point, and the largest values are reported, along with their respective working points.

3.3.4) Load-Pull Power Measurements

Because the devices in question were primarily intended as RF power devices, several important performance characteristics could not be addressed by either DC measurements or S-parameter measurements. The load-pull system was designed to modify the power input and output signal in amplitude and phase to maximize the power output, gain, and power added efficiency as functions of the input power. Figure 24 shows the major components of the load pull system to elucidate the operation of the actual device shown in Figure 25 a and b. First, an RF signal at 7.5 GHz modulates a power input signal, and the reflection of the input signal is canceled out using additional hardware. The gate-source and drain-source biases are added right before the tuners to minimize large-signal losses. Rather than being tested over a range of biases,

the typical procedure fixes the gate-source and drain-source biases and optimizes the tuning at one working point. The input tuner and the output tuner modifies the input and output load according to an iterative algorithm to maximize power output.

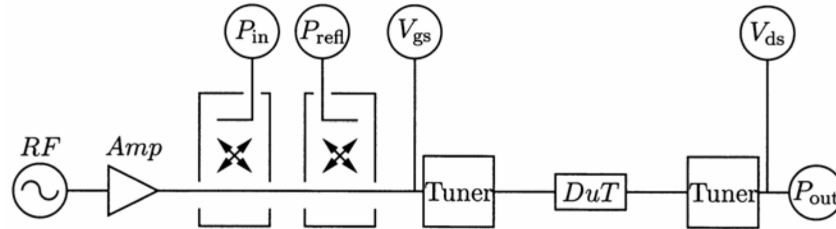

Figure 24: Schematic of Load-Pull Measurement System [42]

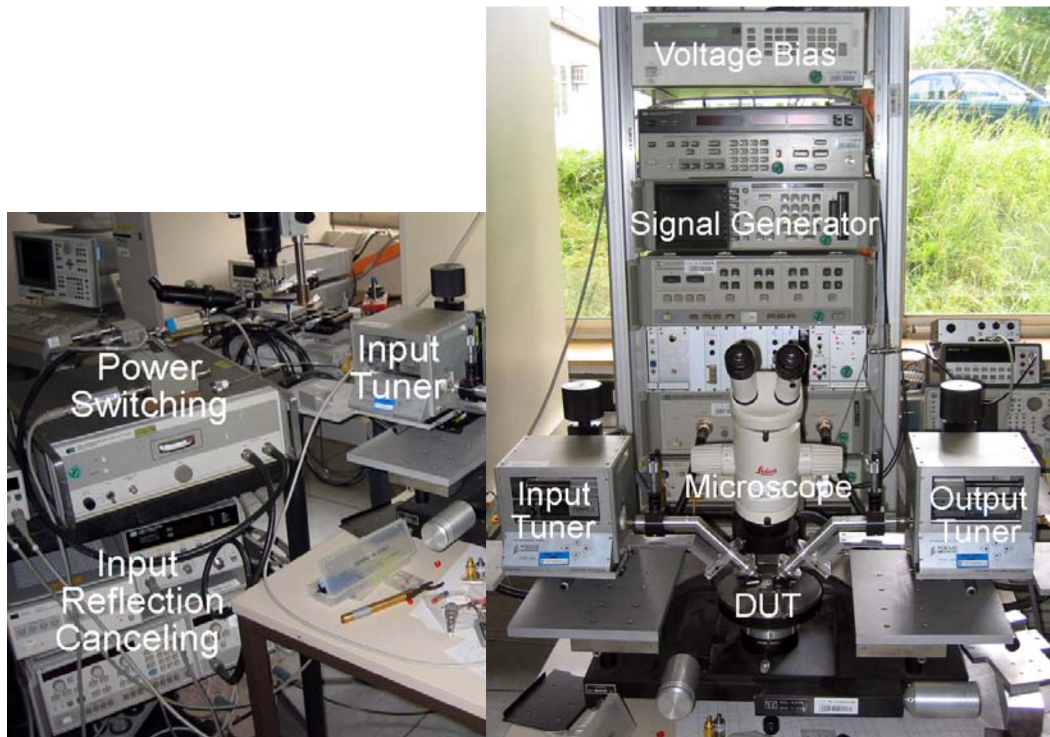

Figure 25: Load-Pull System, Forschungszentrum Julich

Once optimized for the 20 V drain-source voltage and -2.0 V gate-source voltage, the power input was scanned from approximately 5 dB to 30 dB, and the power output response followed as a direct measurement. The gain, more formally called the maximum available gain (MAG), reported is different than the current gain and the unilateral power gain reported for S-parameter measurements, but it is related. It is derived from the S-parameters:

$$MAG = \left|\frac{S_{21}}{S_{12}}\right|$$

Equation 21 [42]

The power added efficiency (PAE) is a standard measure of the efficiency of the transistor to amplify the power signal:

$$PAE = \frac{\left(P_{out} - P_{in}\right)}{V_{ds} I_{ds}} \times 100\%$$

Equation 22 [42]

The drain-source voltage and current in Equation 22 are DC working values, not RMS values.

4) Results and Discussion

Transistors with two, four, and eight gates were fabricated and evaluated according to the processes and procedures described in Section 3 and Appendices C and D. The evaluation is presented and discussed below.

4.1) Optical and SEM Observations

Optical and scanning electron microscope (SEM) observations were helpful throughout the processing for in checking the quality of a process step and diagnosing problems. A basic 2-gate transistor shown in Figure 26 did not require a polymer bridge, so it is shown in its completed form after the lift-off of the contact pad mask. The bright, mottled appearance of the ohmic contacts was a result of the rapid thermal annealing at 900°C. Because the contact pads were added after the annealing step and not exposed to high temperature, they have a more uniform surface. The optical and electron beam lithography resolution and alignment was excellent. These features do not guarantee a high performance transistor, but it is a necessary condition.

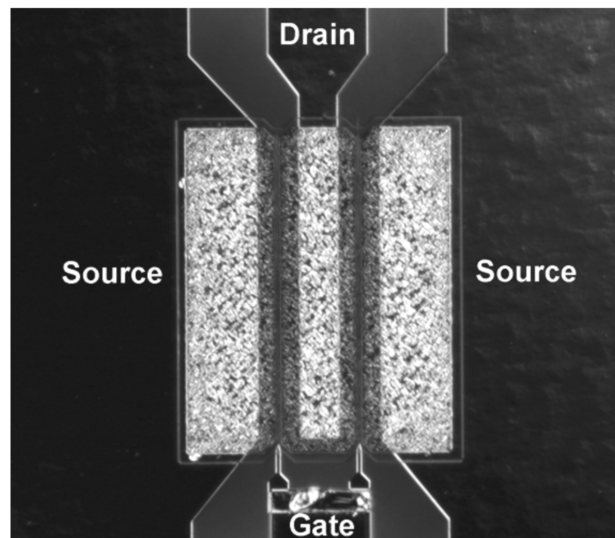

Figure 26: Completed 2-gate Transistor

In contrast, the optical image of a 4-gate transistor in Figure 27 after the completion of the standard process had visible alignment flaws in the electron beam lithography and process flaws in the gate development. It was unclear at this point in the process whether this device would function properly because the central source is not connected.

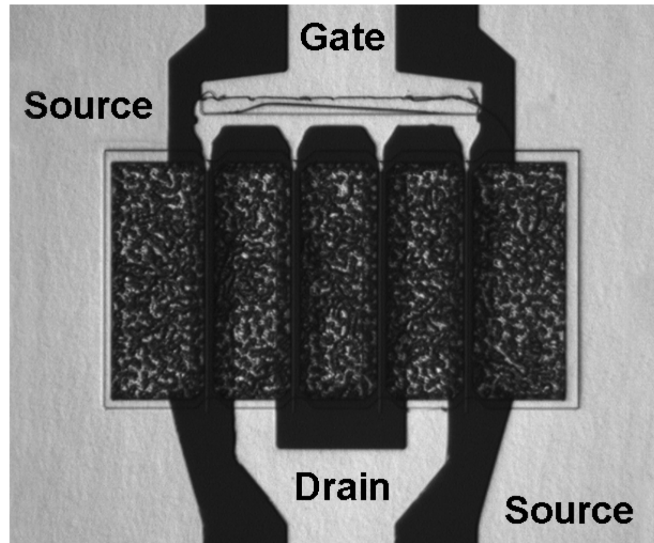

Figure 27: 4-Gate Transistor without Polymer Supported Bridge

Because of the height and shape of the bridges, the depth of field and magnification in optical microscopy was insufficient to explore the structure and processing of the polymer bridges. However, scanning electron microscopy had its own challenges. The exposed polymer was susceptible to charging, and sputtering a thin conductive gold or carbon layer was not feasible because it would have rendered the transistors shorted and inoperative. Ultimately, an environmental SEM with an in-lens secondary electron detector at a low accelerating voltage provided the best images. An additional disadvantage to using electron microscopy is the gate and drain structures are no longer visible because the polymer is too thick. The following SEM images were take at a sixty degree tilt from normal to better observe the height of the bridges and the quality of the bridge metal. Figure 28 shows an entire 8-gate transistor with the polymer bridges complete. The dark areas are insulating polyimide, and the light areas are gold metallization for the different electrical components that are labeled. In this case, the polyimide had excellent dimensional control and bridge metallization bonded well to the ohmic contacts and the polymer bridges.

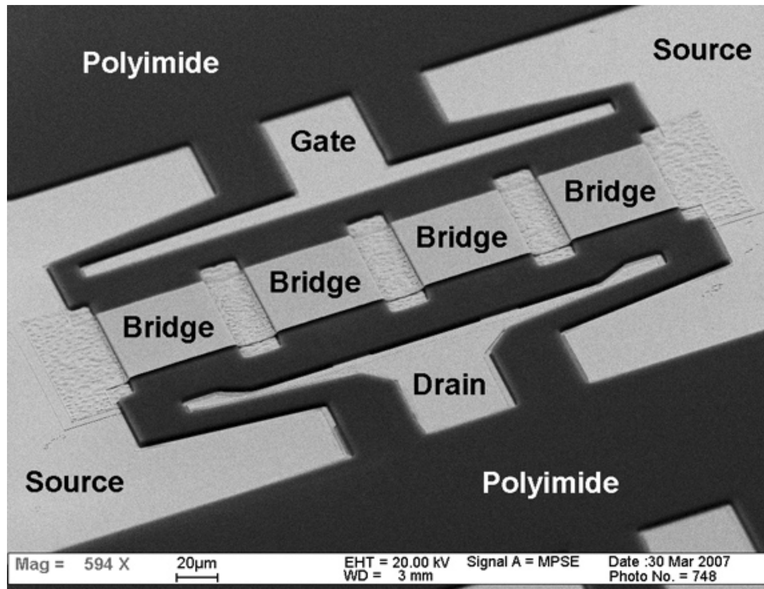

Figure 28: 8-Gate Multi-Finger Transistor with Polymer Supported Bridges

The advantages of SEM became clear in examining the bridge metallization at higher magnification. In Figure 29, the polymer bridge step is viewed at a higher magnification. The nearly vertical sidewalls were typical of the polyimide resist. The step height in this case was 3.6 μm, small enough that the metallization conformed well to the step and did not thin significantly on the sidewall. The apparent curling at the edges of the bridge metallization was due to the lift-off process and did not appear to be an initiation of delamination.

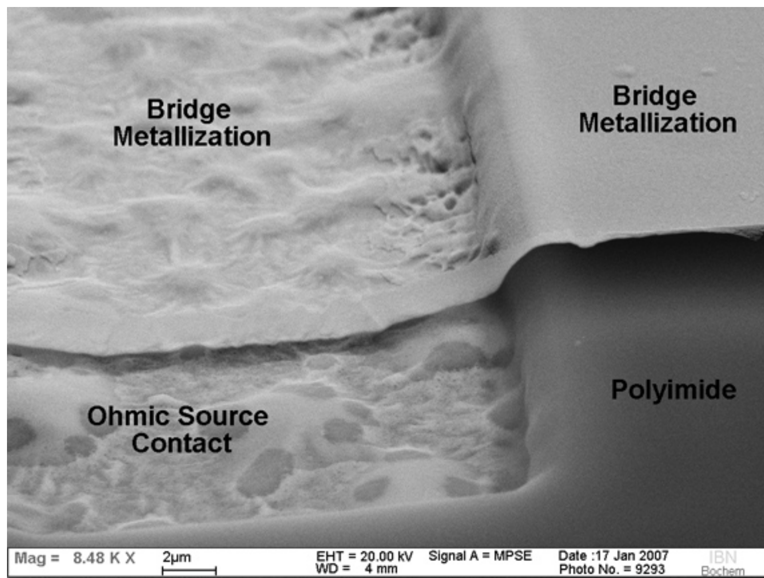

Figure 29: 3.6 μm Bridge Step on a Multi-Finger Transistor

More processing difficulties appeared as higher step heights were fabricated. In Figure 30, the two primary processing issues with higher step heights are evident in this 4.8 μm sample.

In area 1, the bridge metallization does not conform to the step. The source of this problem was in the development of the resist pattern for the bridge metallization. Because of the high aspect ratio of the step, the exposed resist at the bottom of the step was not fully developed, and during the final lift-off the resist dissolved, leaving the metal at the bottom of the step unsupported. In addition to the obvious reliability issue, there could have been remaining resist in the gap that could decompose at the operating temperature and damage the metallization. The first problem was solved in subsequent samples by increasing the development time by 10 seconds. In area 2, the thinning of the bridge metallization was quite severe. At this step height, the metal bridge failed consistently at typical current densities for multi-finger devices. Despite several iterations with different metallization thicknesses, multiple metallization steps, and sample rotation during metal evaporation, the second problem area was not satisfactorily solved in the course of the study. Metal sputtering, rather than electron beam evaporation, might be better suited to this step height because sputtering conforms better to difficult geometries; however, gold sputtering was not available to be tested.

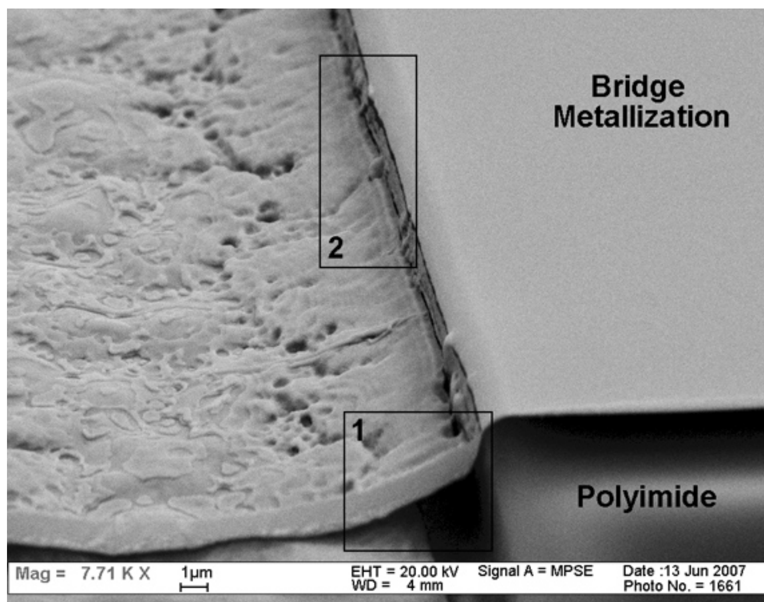

Figure 30: 4.8 μm Bridge Step Processing Issues

Devices that failed during test or did not function correctly were also examined with SEM. Figure 31 shows a typical breakdown due high electric fields. The source and the drain shorted where the drain contact and the source contact are closest together and the electrical field is highest. The ohmic contact pads were removed and the underlying layers exposed, indicating the failure initiated in the epitaxial layers. The breakdown had a dramatic effect on the rest of

the device. The metal of the nearest source contact and the bridge contact delaminated. The breakdown damaged the gate too. The failure is unrelated to the polymer supported bridge; furthermore, the polymer in the area immediately around the affected area remained intact despite the high electrical, thermal, and mechanical stress before and during the failure.

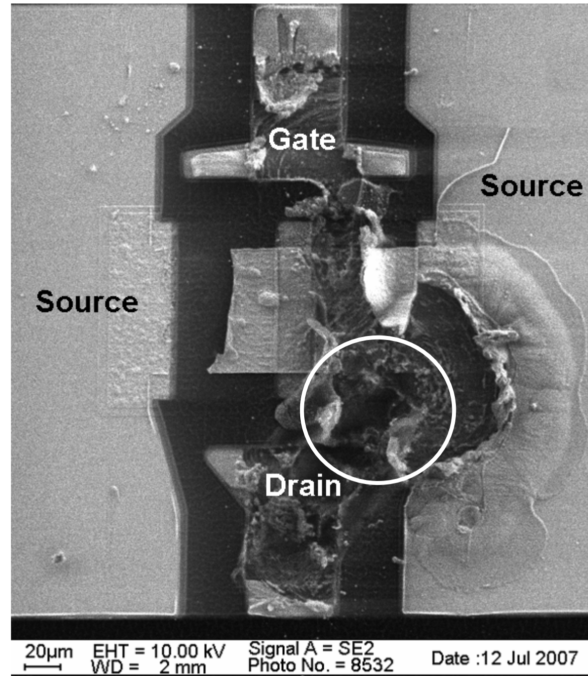

Figure 31: Breakdown on a 4-gate device

A more common and more problematic failure was the failure of the bridge metal at the polymer step. Figure 32 shows a SEM image of the bridge metallization on an 8-gate transistor with 4.8 microns of polyimide and an inset of the DC measurements from that transistor. The metallization in the image was 500 nm thick, double the amount used for the lower gate heights. Regardless of this accommodation for the larger step height, the current density was too high and the thinner metal at the polymer step failed. The inset supports this conclusion because the device initially outputted similar absolute currents to 8-gate transistors, but the device failed, and the absolute current quickly drops to levels similar to 2-gate transistors. Only the outer two gates were functioning after the failure because all of the sources were no longer in electrical contact.

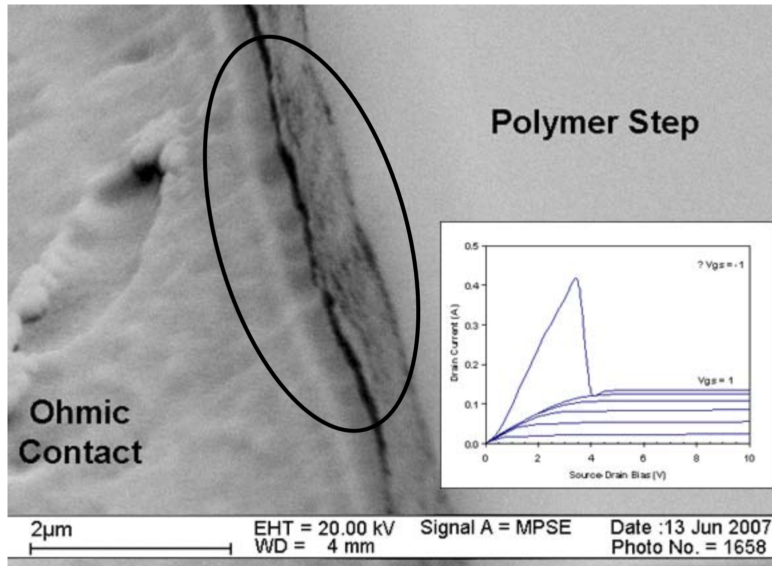

Figure 32: Bridge Metallization Failure at the Polymer Bridge Step

4.2) Hall Effect Measurements

The results of the Hall Effect measurements at 300 K are summarized in Table 8 below. The two F-series samples were consistent with expectations. Because F1749 is moderately doped, the mobility decreases, the carrier concentration increases, and the sheet resistance decreases compared to the undoped F1738 sample. The last sample, M0566, was part of a later series, so impurity levels could have varied or the AlGaN-GaN interface could have been more abrupt. Despite the higher than expected sheet carrier concentration and the relatively low mobility, the sheet resistance is comparable to the other samples.

Table 8: Hall Effect Measurements

Sample	AlGaN Thickness (nm)	Doping (cm^{-3})	Sheet Resistance (Ω/□)	Mobility (cm^2/Vs)	Sheet Carrier Concentration(cm^{-2})
F1738	30	Undoped	448	1855	7.53×10^{12}
F1749	25	2.0×10^{18}	407	1618	9.52×10^{12}
M0566	30	Undoped	462	1465	9.22×10^{12}

4.3) DC Measurements

Figures 33-36 introduce the DC measurements for each polyimide thickness. The current response was normalized to gate length so the performance as a function of the number of gates could be compared directly. The complete range of gate voltages, from +1 V to -6 V, is shown only for the 2-gate devices in all blue. In order to summarize the differences in the most effective way, only the +1 V gate voltage line is shown for the 4-gate (in red) and the 8-gate (in green) transistors. The thickest dielectric layer does not have an 8-gate line because the current density was too high, and the metal source contact failed for all 8-gate transistors. It is also important to note that the sample with a 3.6 μm polyimide has a doped AlGaN layer, so the absolute drain-source current is higher than in the other samples. For the thinnest dielectric layer (Figure 33), the normalized DC characteristics were similar for the 2-, 4-, and 8- gate transistors. The current outputs of the 4- and 8-gate transistors diverged because of heating effects and relatively small parasitic resistances. The peak normalized drain-source current of the 4-gate device is 5.8% less and the 8-gate device is 8.3% less than the peak normalized drain-source current of the 2-gate device lacking a polymer supported bridge.

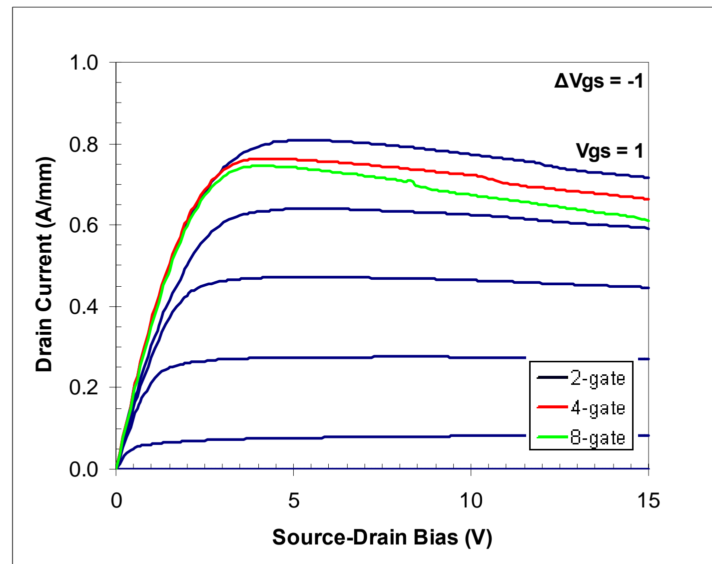

Figure 33: Normalized I-V Curves for 2-gate, 4-gate, and 8-gate Transistors with 0.8 μm Polyimide

The thicker layers (Figure 34 and 35) showed progressively worse results. The absolute amplification decreased with increasing number of gates. The 4-gate device shows a 13.2% decrease in the peak normalized drain-source current over the source. The 8-gate device shows a

similar, albeit slightly smaller 10.5% drop. The drop can be attributed to the increase in the source resistance. Thinning of the bridge metal at higher polymer step heights reduced the cross-sectional area of the conductor and increased the resistance of the source. The cause of the bridge metal thinning is discussed in Section 4.1, and Figures 30 and 32 are examples of metal thinning.

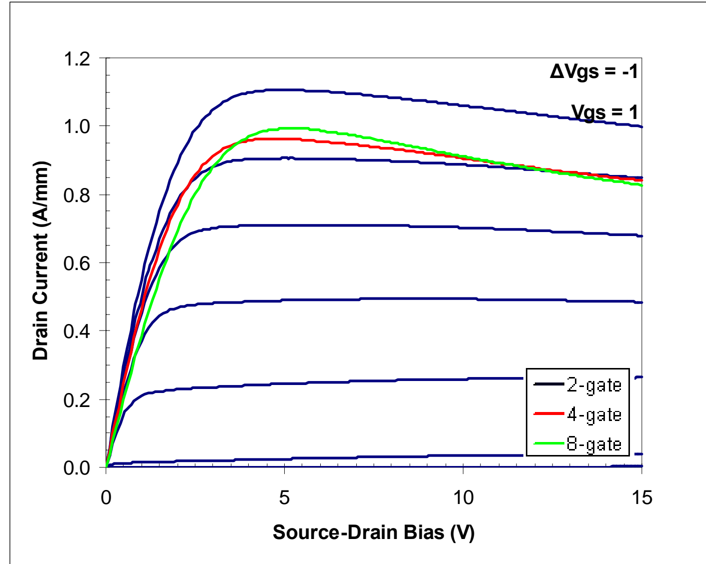

Figure 34: Normalized I-V Curves for 2-gate, 4-gate, and 8-gate Transistors with 3.6 µm Polyimide

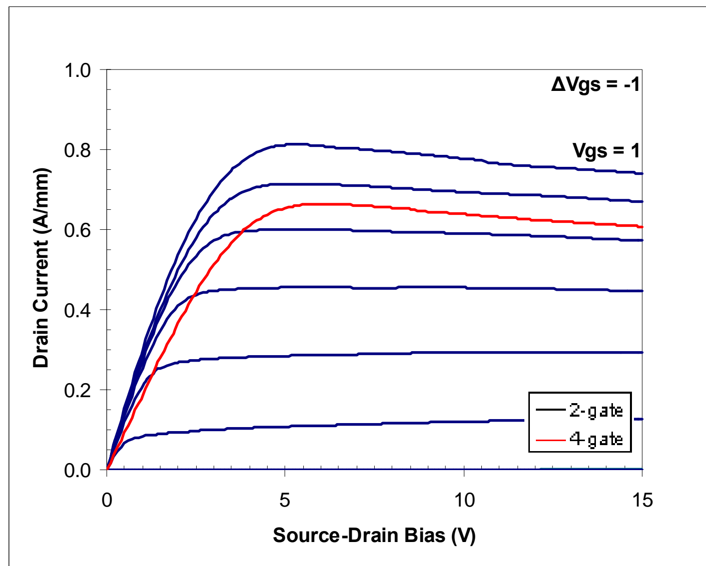

Figure 35: Normalized I-V Curves for 2-gate and 4-gate Transistors with 4.8 µm Polyimide

Pictured in Figure 36, the plot of the transconductance versus the gate voltage for each polymer step height also shows how a higher source resistance undermines key DC performance

characteristics. Allowing that doping in the 3.6 µm polyimide sample increased the transconductance due to lower resistance in the channel, the profiles for the 2-gate transistors looked comparable. The performance debit is most evident in the sample with the highest step. Ideally, an 8-gate transistor should have a 4-fold higher transconductance than the 2-gate device, and a 4-gate transistor should have a 2-fold increase in the transconductance over the 2-gate device. The peak values of the two samples with smaller polymer steps showed strong, albeit less than ideal, conformance to the expected result. However, the high step showed significant deviation from the ideal. The 4-gate transistor in this case had only a 1.64-fold improvement in transconductance over the 2-gate transistor at the peak transconductance.

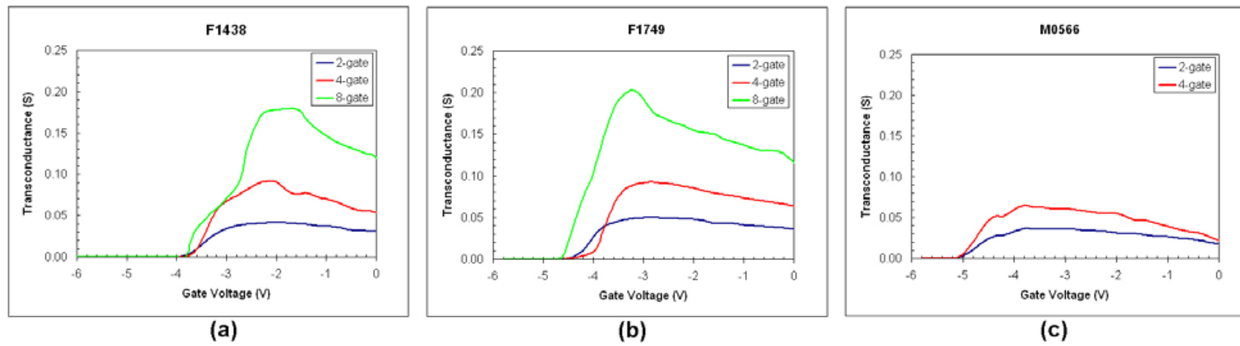

Figure 36: Transconductance vs. V_{gs} for 0.8 µm (a), 3.6 µm (b), and 4.8 µm (c) Polyimide

Another performance consideration was the threshold voltage, which is also most easily demonstrated in Figure 36. When the transconductance approached zero, the channel was pinched-off because the electric field from the gate had completely depleted the channel. Transconductance peaked just before the pinch-off because the channel was partially depleted, the carrier concentration decreased, and the carrier mobility increased. The devices with the 0.8 µm polyimide had the lowest threshold voltage at approximately -3.8 V, and the threshold voltage tended to increase with increasing polyimide thickness, up to approximately -5.0 V for the 4.8 µm. The most likely explanation for this effect is that the polyimide passivated the surface donor states that previously trapped carriers, so the carrier density in the channel was effectively higher and required a stronger electric field to pinch-off.

4.4) S-Parameter Measurements

Figures 37 and 38 summarize the salient results of S-parameter measurements. Generally, there is a trend of increasing cutoff frequency with number of gates. The cutoff frequency trends tracked well with the theoretical framework set down in Section 2.3.4. The cutoff frequency was primarily dependent on the transconductance and inversely dependent on the gate-source capacitance (Equation 13), and the transconductance increased dramatically due to increased gate length. However, the gate-source capacitance also increased due to the increased area of the gate and source. The transconductance seemed to dominate for the 4-gate transistors, but the gate-source capacitances reduced the high-frequency performance of the 8-gate devices.

Additionally, there appeared to be a correlation of decreasing cutoff frequency with increase height of the polyimide step, which was not immediately clear from the equations derived in the small signal model. However, the small signal model assumes the intrinsic resistances of the sources, drains, and gates are negligible compared to the resistance of the channel. In this case, the source resistance for the larger polyimide step heights made a significant contribution to the parasitics. For the reasons already described above, the thinning metallization of the bridge metal also decreased high-frequency performance of the devices.

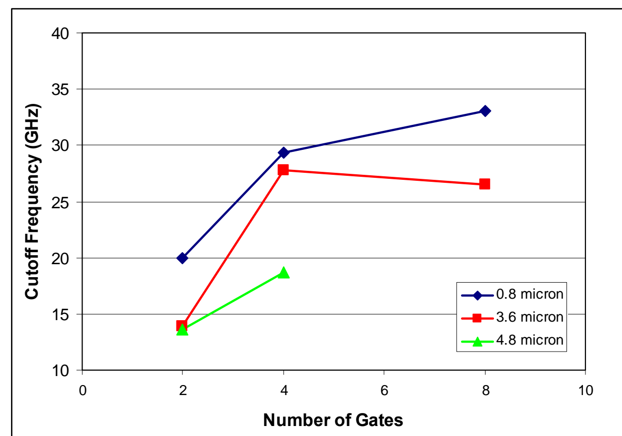

Figure 37: Cutoff Frequency vs. Number of Gates

The maximum oscillating frequency, while also a measure of high-frequency performance, is more strongly affected by parasitic capacitances and the conductivity of the channel (Equation 14). The dependence on the transconductance is also reduced. Figure 38 shows that there was virtually no difference in the maximum oscillating frequency with increasing number of gates or increasing height of the polyimide step. The conclusion follows

that the additional parasitic capacitances due to the polymer-supported did not play a significant role in the limiting the high-frequency performance of the device. The intrinsic capacitances of the geometry of the source, drain, and gates were far more determinative than external connections, likely due to the relatively large dielectric constants of AlGaN and GaN.

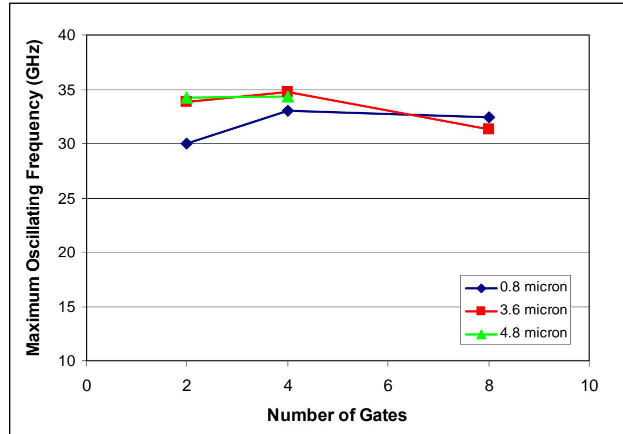

Figure 38: Maximum Oscillating Frequency vs. Number of Gates

4.5) Power Measurements

Data for power output, maximum available gain, and power added efficiency was gathered as a function of power input for each polymer step height and number of gates. The composite graphs in Figures 39-41 have three measurements plotted on the same scale: power output (in blue), maximum available gain (in green), and power added efficiency (in red). The scale for the power output and gain are in decibels (dB), a logarithmic base 10 scale, so an approximate increase of 3 dB indicates a doubling of the absolute value. The PAE is measured in percent. The power performance for all of the devices was measured at 7.5 GHz with a drain-source bias of 20 V and a gate-source bias of -2 V. The lower half of the graphs for the 8-gate samples were omitted because the current load necessary to maintain the working point exceeded the capability of the measurement system at low power inputs, so the data in this regime was not directly comparable to the rest of the data.

In the ideal case, power output should have increased approximately 3 dB each time the number of gates doubled. For all three polymer step heights, the power output doubled when the number of gates was increased from two to four gates. However, the power output for the 8-gate transistors was significantly less than a 3 dB increase over the 4-gate transistors. The gain also

stagnated for the 8-gate transistors on the 0.8 μm polyimide sample. This translated into generally lower power added efficiency for the 8-gate transistors.

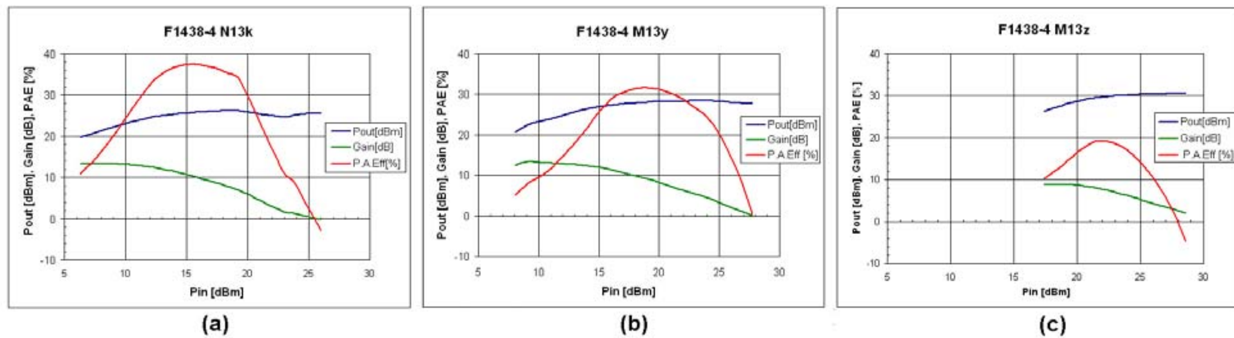

Figure 39: Output, Gain, and PAE for 2-Gate (a), 4-Gate (b), and 8-Gate (c) Devices with 0.8 μm Polyimide

The gain tracked better with the power output of the 3.6 μm polyimide sample, so the maximum power added efficiency was relatively stable as the number of gates increased.

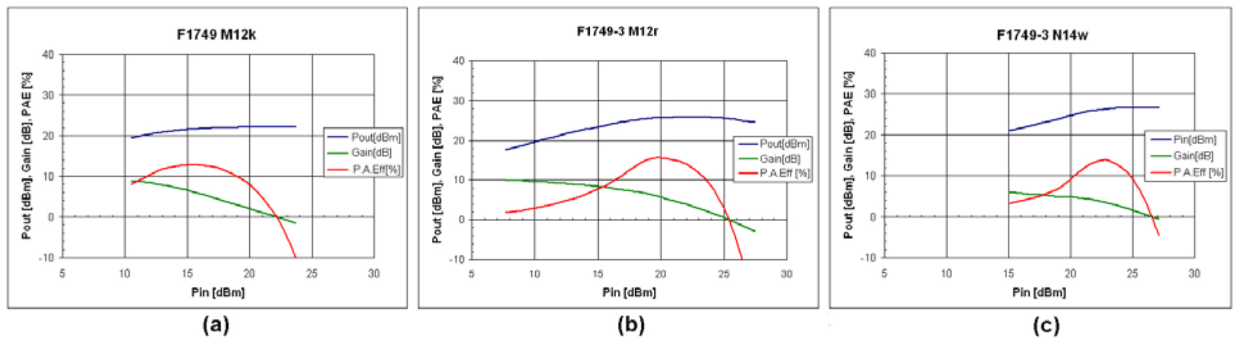

Figure 40: Output, Gain, and PAE for 2-Gate (a), 4-Gate (b), and 8-Gate (c) Devices with 3.6 μm Polyimide

Power performance of the devices with 4.8 μm polyimide was unexpectedly good, considering sub-optimal DC and high frequency performance. Most likely, this is because of the original quality of the epitaxial material, which came from a different growth series than the other two samples. The Hall measurements of the layers indicated that the carrier concentration in the electron gas was high, despite being nominally undoped. The higher conductivity of the channel could have been better suited to this intermediate regime.

Additionally, the peak power added efficiency shifted to higher power inputs with increasing number of gates. This effect is inherent to the device because it requires more power to turn off each gate.

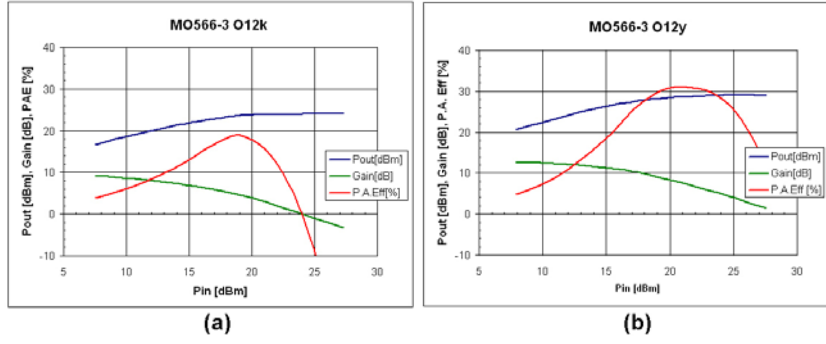

Figure 41: Output, Gain, and PAE for 2-Gate (a) and 4-Gate (b) Devices with 4.8 µm Polyimide

5) Conclusions and Future Work

A simplified technique was developed to connect the sources in a multi-finger AlGaN/GaN HFET using polyimide-supported bridge in contrast to the traditional air bridge design. First, lithographic steps were employed to construct the device isolation, ohmic source and drain contacts, Schottky gate contacts, and contact pads. A polyimide resist was patterned and cured over the gates and drains to construct mechanical support and electrical isolation for the source contact metallization above. Varying polymer thicknesses were prepared to evaluate the effect of polymer step height on the transistor characteristics. The completed devices with two, four, and eight gates were characterized using Hall Effect, DC, high frequency s-parameter measurements, and AC power measurements.

5.1) Efficacy and Impact

The polymer supported bridges performed well in initial qualitative tests. Scanning electron microscopy images showed the polyimide layer had good dimensional control and repeatability. The Ti-Au metallization adhered well to the polyimide layer and did not show any significant delamination. Because the metal was deposited with an electron beam evaporation system, the metal thinned at the higher steps of the thicker polyimide layers.

The metal thinning and the accompanying increase in source resistance cause significant reductions in the device performance. For DC measurements, higher step heights were associated with lower drain-source current responses. For a given number of gates, the higher step heights generally decreased the cut-off frequency during s-parameter measurements, but did not strongly affect the maximum oscillating frequency, which is less dependent on the transconductance. For power measurements, the best gain and power output performance was also attributed to the sample with the thinnest polyimide layer.

Additionally, the results showed the dielectric constant of the polyimide was sufficiently low as to contribute relatively small parasitic capacitances, even with relatively thin dielectric layers. Coupled with a more conformal metallization process, such as sputtering, samples with a dielectric layer of approximately a micron could approach theoretical performance characteristics of multi-finger HFETs. The thin dielectric layer would also have a relatively low thermal

resistance despite the lower thermal conductivity of the polyimide, allowing for efficient top side cooling.

5.2) HFET Oscillator for Terahertz Generation (HOTGaN)

The Institute for Bio- and Nanosystems (IBN-1) at Forschungszentrum Jülich has recently started a major research initiative into ultra-high frequency electronics based on the AlGaN-GaN HFET. In the frequency continuum, a technology gap exists in the terahertz range. Below 300 GHz, various semiconductor electronics have been very successful in producing the broad range of necessary frequencies for applications in wireless communication, radar, radio. Above 10 THz, semiconductor optoelectronics, black body radiators, or high energy sources can generate a large spectrum of frequencies for numerous infrared, visible, ultraviolet, and x-ray applications. However, possible applications for compact, intense, low noise tertahertz frequency sources make this gap important to close. In telecommunications, higher frequencies enable greater bandwidth. In radar technology, higher frequencies improve accuracy and resolution. In medical imagining, the absorption of terahertz frequencies is low in soft tissue, so bone scans could potentially be done without harmful ionizing X-rays.

The research described above is primarily focused on optimization for lower frequency, but higher power devices. However, the results show the cutoff frequency was improved by increasing the gate length using multi-finger devices. Furthermore, the polyimide supported-bridges did not reduce the maximum oscillating frequency of the devices because of the low dielectric constant of the polyimide. In order to fabricate oscillators that operate near 1 THz, low dielectric constant materials will be necessary for passivation layers and possibly interconnect layers. Improvement of the metal deposition could improve the cutoff and maximum oscillating frequency of multi-finger devices. The research above is also a proof-of-concept that polyimide resists can be generally compatible with AlGaN/GaN HFETs in a relatively high frequency and at normal operational temperatures.

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C) AlGaN/GaN HFET Fabrication Process Flow

Step	Process Step	Sub-Process Step	Activity	Workplace	Supplies	Reference Times	Other Parameters
0	Pre-Processing	Sample Preparation	Cleaning in acetone and propanol	Wet Bench 6	Acetone, Propanol	-	-
0	Pre-Processing	Sample Preparation	Dehydration bake on hotplate	Wet Bench 2	Hotplate	10 min	180 C
0	Pre-Processing	Applying Photoresist	Apply Photoresist	Wet Bench 2	AZ 5214, Spinning Machine	-	Program 04
0	Pre-Processing	Applying Photoresist	Pre-bake (Soft bake) on hotplate	Wet Bench 2	Hotplate	5 min	90 C
0	Pre-Processing	Cutting Wafer	Cutting Wafer	Wafer Cutting Lab		-	-
1	Mesa	Sample Preparation	Cleaning in acetone and propanol	Wet Bench 6	Acetone, Propanol	-	-
1	Mesa	Sample Preparation	Dehydration bake on hotplate	Wet Bench 2	Hotplate	10 min	180 C
1	Mesa	Applying Photoresist	Apply Photoresist	Wet Bench 2	AZ 5214, SpinningMachine	-	Program 04
1	Mesa	Applying Photoresist	Pre-bake (Soft bake) on hotplate	Wet Bench 2	Hotplate	5 min	90 C
1	Mesa	Removing Side Resist	Expose to UV-Light	Mask Aligner	Side Resist Mask	25 sec	-
1	Mesa	Removing Side Resist	Develop	Wet Bench 3	AZ 400K, H2O	25 sec	AZ 400K:H2O (1:4)
1	Mesa	Creating Mesa Structures	Expose to UV-Light	Mask Aligner	Power-2-Mask	4.0 sec	-
1	Mesa	Creating Mesa Structures	Develop	Wet Bench 3	AZ 400K, H2O	50 sec	AZ 400K :H2O (1:4)
1	Mesa	Creating Mesa Structures	Rinse in running D.I. water	Wet Bench 3	D.I. water	-	-
1	Mesa	Creating Mesa Structures	Postbake on hotplate to harden photoresist	Wet Bench 2	Hotplate	10 min	110 C
2	Mesa	Etching Mesa-Structure	Ar+ sputtering	IBE Lab	Ar+ sputtering machine	10 min	500 V, 88 mA, 30 deg, rotation on

3	Mesa	Removing Resist	Cleaning in acetone and propanol	Wet Bench 6	Acetone, Propanol	-	-
3	Mesa	Removing Resist	Oxygen plasma	Clean Room	Plasma Processor	20 min	Program 07
3	Mesa	Removing Resist	HF:H2O dip, rinse in DI water	Wet Bench 4	HF, H20	2 min	HF:H2O (1:2)
3	Mesa	Removing Resist	HCl:H2O dip; rinse in DI water	Wet Bench 5	HCl, H20	2 min	HCl:H2O (1:2)
3	Mesa	Removing Resist	NH4OH:H2O2 dip, rinse in DI water	Wet Bench 6	NH4OH, H2O2	10 min	NH4OH:H2O 2 (2:1)
3	Mesa	Removing Resist	Dehydration bake on hotplate	Wet Bench 2	Hotplate	10 min	180 C
2	Ohmic Contacts	Applying Photoresist	Apply Photoresist	Wet Bench 2	AZ 5214, Spinning-Machine		Program 04
2	Ohmic Contacts	Applying Photoresist	Pre-bake (Soft bake) on hotplate	Wet Bench 2	Hotplate	5 min	90 C
2	Ohmic Contacts	Removing Side-Resist	Expose to UV-Light	Mask Aligner	Side Resist Mask	25 sec	-
2	Ohmic Contacts	Removing Side Resist	Develop	Wet Bench 3	AZ 400K, H2O	25 sec	AZ 400K :H2O (1:4)
3	Ohmic Contacts	Creating Ohmic Contacts	Expose to UV-Light	Mask Aligner	Ohmic-Contact-Mask	4.0 sec	-
3	Ohmic Contacts	Creating Ohmic Contacts	Chloro-Benzol dip	Wet Bench 4	Chloro-Benzol	3 min	-
3	Ohmic Contacts	Creating Ohmic Contacts	Develop	Wet Bench 3	AZ 400K, H2O	50 sec	AZ 400K :H2O (1:4)
3	Ohmic Contacts	Creating Ohmic Contacts	DI Water Rinse	Wet Bench 6	D.I. water	-	-
3	Ohmic Contacts	Creating Ohmic Contacts	Oxygen Plasma	Plasma Processor	Plasma Processor	2 min	Program 01
4	Ohmic Contacts	Sample Preparation	HCL:H2O dip	Wet Bench 4	HCl, H20	10 sec	HCl:H2O (1:2)
4	Ohmic Contacts	Creating Ohmic-Contact	Deposit metal	E-beam Evaporator	E-beam Evaporator	Ti/Al/Ni/Au of 35/200/40/100nm, Ar-Sputtering (10 sec), No Heating	

5	Ohmic Contacts	Creating Ohmic Contact	Deposite probe into acetone	Wet Bench 6	Acetone	> 2 hr	-
6	Ohmic Contacts	Creating Ohmic Contact	Lift off in acetone	Wet Bench 6	Acetone	-	-
6	Ohmic Contacts	Creating Ohmic Contact	Rinse with propanol, blow with N2	Wet Bench 6	Propanol, N2	-	-
6	Ohmic Contacts	Creating Ohmic Contact	Anneal (Immediately after Lift off)	Clean Room	Rapid Annealing Furnance	30 sec	900 C, N2-Atmosphere, Program bj gan1
7	Gate Contacts	Sample Preparation	Cleaning in Acetone and Propanol, blow with dry N2	Wet Bench 6	Acetone, Propanol	-	-
7	Gate Contacts	Sample Preparation	Dehydration bake on hotplate	Wet Bench 2	Hotplate	10 min	180 C
7	Gate Contacts	Applying Photoresist	Apply Photoresist	Wet Bench 2	PMMA 600K	-	6000rpm
7	Gate Contacts	Applying Photoresist	Hardening Photoresist on hotplate	Wet Bench 2	Hotplate	2 min	180 C
7	Gate Contacts	Applying Photoresist	Apply Photoresist	Wet Bench 2	PMMA 200K	-	6000rpm
7	Gate Contacts	Applying Photoresist	Hardening Photoresist on hotplate	Wet Bench 2	Hotplate	2 min	180 C
7	Gate Contacts	Applying Photoresist	Apply Photoresist	Wet Bench 2	PMMA 600K	-	6000rpm
7	Gate Contacts	Applying Photoresist	Hardening Photoresist on hotplate	Wet Bench 2	Hotplate	2 min	180 C
8	Gate Contacts	Creating Gate Structure	Complete work order with AutoCAD layout for E-beam exposure	Office	AutoCAD	-	-
8	Gate Contacts	Creating Gate Structure	Expose to E-Beam	E-Beam	E-Beam-Mask	-	320µC per cm2
9	Gate Contacts	Creating Gate Structure	Develop	Wet Bench 3	AR600-55	120 sec	
9	Gate Contacts	Creating Gate Structure	Rinse in propanol	Wet Bench 6	Propanol	-	-
9	Gate Contacts	Creating Gate Structure	Oxygen Plasma	Clean Room	Plasma processor	2 min	Program 01
10	Gate Contacts	Sample Preparation	HCL:H2O dip prior to metal-deposition, rinse in DI water	Wet Bench 4	HCl, H20	10 sec	HCl:H2O (1:2)

10	Gate Contacts	Creating Gate	Deposit metal	E-beam Evaporator	E-beam Evaporator	Ni/Au of 25/100nm, No Ti/Cr Atmosphere, No Ar-Sputtering, No Heating	
11	Gate Contacts	Creating Gate	Deposit in acetone	Wet Bench 6	Acetone	> 2 h	-
11	Gate Contacts	Creating Gate	Lift off in acetone	Wet Bench 6	Acetone	-	-
11	Gate Contacts	Creating Gate	Rinse with propanol, blow with N_2	Wet Bench 6	Propanol, N_2	-	-
12	Pads	Sample Preparation	Dehydration bake on hotplate	Wet Bench 2	Hotplate	10 min	180 C
12	Pads	Applying Photoresist	Apply Photoresist	Wet Bench 2	AZ 5214, Spinning-Machine	-	Program 04
12	Pads	Applying Photoresist	Pre-bake (Soft bake) on hotplate	Wet Bench 2	Hotplate	5 min	90 C
12	Pads	Removing Side Resist	Expose to UV-Light	Mask Aligner	Side Resist Mask	25 sec	-
12	Pads	Removing Side Resist	Develop	Wet Bench 3	AZ 400K, H_2O	35 sec	AZ 400K:H_2O (1:4)
12	Pads	Creating Pads	Expose to UV-Light	Mask Aligner	Pad-Mask	4.0 sec	-
12	Pads	Creating Pads	Chloro- Benzol dip	Wet Bench 4	Chloro-Benzol	3 min	-
12	Pads	Creating Pads	Develop	Wet Bench 3	AZ 400K, H_2O	50 sec	AZ 400K:H_2O (1:4)
12	Pads	Creating Pads	Rinse in running D.I. water	Wet Bench 6	D.I. water	-	-
12	Pads	Creating Pads	Oxygen Plasma	Clean Room	Plasma Processor	2 min	Program 01
12	Pads	Creating Pad	Deposit metal	E-beam Evaporator	E-beam Evaporator	Ti/Au of 25/300nm, Ti/Cr Atmosphere, No Ar-Sputtering, No Heating	
13	Pads	Creating Pad	Deposit probe into acetone	Wet Bench 6	Acetone	> 2 h	-
13	Pads	Creating Pad	Lift off in acetone	Wet Bench 6	Acetone	-	-
13	Pads	Creating Pad	Rinse with propanol, blow with N_2	Wet Bench 6	Propanol, N_2	-	-

D) Polymer Supported Bridge Fabrication Process Flow

Step	Process Step	Sub-Process Step	Activity	Workplace	Supplies	Reference Times	Other Parameters
1	Bridges	Applying Photo-Resist	Apply Photo-Resist	Wet Bench 2	HD 4000, Spinning Macine	60 s	5000-8000 rpm **(1)**
1	Bridges	Applying Photo-Resist	Pre-bake (Soft bake) on hotplate	Wet Bench 2	Hotplate	120 s	110 C
2	Bridges	Creating polymer supports	Expose to UV-Light	Mask Aligner	Air Bridge 1 Mask	45 sec	-
2	Bridges	Creating polymer supports	Develop	Wet Bench 6	PA-400D	50-60 sec **(1)**	PA-400D
2	Bridges	Creating polymer supports	Rinse, dry	Wet Bench 6	Propanol, N2	-	-
2	Bridges	Creating polymer supports	Cure Bake	Oven	Oven	Under N2: 10 C/min ramp to 200 C, hold at 200 C for 20 min, 10 C/min ramp to 375 C, hold at 375 C for 60 min, 10 C/min ramp to RT	
3	Bridges	Applying Photo-Resist	Apply Photo-Resist	Wet Bench 2	AZ 5214, Spinning-Machine	-	Program 04
3	Bridges	Applying Photo-Resist	Pre-bake (Soft bake) on hotplate	Wet Bench 2	Hotplate	5 min	90 C
3	Bridges	Removing Side-Resist	Expose to UV-Light	Mask Aligner	Side Resist Mask	25 sec	-
3	Bridges	Removing Side-Resist	Develop	Wet Bench 3	AZ 400K, H2O	35 sec	AZ 400K:H2O (1:4)
4	Bridges	Isolating Bridge structures	Expose to UV-Light	Mask Aligner	Air Bridge 2 Mask	4.0 sec	-
4	Bridges	Isolating Bridge structures	Develop	Wet Bench 3	AZ 400K, H2O	50-60 sec **(1)**	AZ 400K:H2O (1:4)
4	Bridges	Isolating Bridge structures	Rinse in D.I. water	Wet Bench 6	D.I. water	-	-
4	Bridges	Isolating Bridge structures	Oxygen Plasma	Plasma Processor	Plasma Processor	2 min	Program 01
4	Bridges	Isolating Bridge structures	Photo-resist hardening bake	Wet Bench 2	Hotplate	10 min	120 C

<table>
<tr><td>5</td><td>Bridges</td><td>Preparing Sample</td><td>HCL:H_2O dip</td><td>Wet Bench 4</td><td>HCl, H20</td><td>10 sec</td><td>HCl:H_2O (1:2)</td></tr>
<tr><td>5</td><td>Bridges</td><td>Metallization</td><td>Deposit metal</td><td>E-beam Evaporator</td><td>E-beam Evaporator</td><td colspan="2">Ti (20 nm), Au (100 nm), No Ti/Cr Atmosphere, No Ar-Sputtering, No Heating</td></tr>
<tr><td>5</td><td>Bridges</td><td>Lift-off</td><td>Lift off in acetone</td><td>Wet Bench 6</td><td>Acetone</td><td>-</td><td>-</td></tr>
<tr><td>5</td><td>Bridges</td><td>Final Clean</td><td>Rinse with propanol, blow with N_2</td><td>Wet Bench 6</td><td>Propanol, N_2</td><td>-</td><td>-</td></tr>
</table>

(1) The spinning speed and the development time depend on the thickness of the polyimide resist

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