Design of a Low Power Delta Sigma Modulator for Analog to Digital Conversion

by

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ABSTRACT

The growing demand of “System on a Chip” applications nececitates integration of multiple devices on the same chip. Analog to Digital conversion is essential to interfacing digital systems to external devices such as sensors. This presents a difficulty since high precision analog devices do not mix well with high speed digital circuits. The digital environment constraints put demand on the analog portion to be resource efficient and noise tolerant at the same time. Even more demanding, Analog to Digital converters must consume a small amount of power since “System on a Chip” circuits often target portable applications. Analog to digital conversion based on Delta Sigma modulation offers an optimal solution to the above problems. It is based on digital signal processing theory and offers benefits such as small footprint, high precision, noise de-sensitivity, and low power consumption.

This thesis presents a methodology for designing low power Delta Sigma modulators using a combination of modern circuit design techniques. The developed techniques have resulted in several modulators that satisfy the initial design parameters. We applied this method to design three different modulators in the 0.35um digital CMOS technology with a 3.3V supply voltage. A first order Self-Referenced modulator has a resolution of 8 bits and the lowest power consumption at 75 uW. The most successful design is the second order Self Referenced modulator that produces 12 bits of resolution with a power consumption of 87 uW. A second order Floating Gate modulator posesses features for high noise rejection, and produces 10 bits of resolution while consuming 276 uW. It is concluded that self-referenced modulators dissipate less power and offer higher performance as compared more complicated circuits such as the floating gate modulator.

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Table of Contents:

Design of a Low Power Delta Sigma Modulator for Analog to Digital Conversion

List of Figures:

CHAPTER 1: Introduction

Modern day industry has a growing demand for digital integrated circuits. While high performance applications still drive the industry and the development efforts, it is the Application Specific Integrated Circuits (ASIC) that enable many new technologies. ASIC developments have brought on the minimization of modern applications such as cellular phones by integrating complex digital functions within small packages. ASICs serve to improve performance and lower power consumption for portable devices. Perhaps the most important reason for the success of ASICs is that they serve to minimize cost by using one custom chip where several generic components would have been necessary.

These capabilities and importance of ASICs have grown with the advent of the System on a Chip (SOC) technologies. The ability to integrate distant technologies such as digital MOS logic, RAM, ROM, and analog and bipolar circuits on a single chip has the potential to put SOCs at the frontier of the integrated circuit technology. For this reason, the smooth integration of analog and digital technologies is a priority.

Similarly, we have started this project while working with custom underlayer and gate-array circuits. A demand has appeared for a low profile analog to digital conversion (ADC) system capable of high precision measurements. While low precision converters have been available for some time, creating an accurate analog circuit within a digital environment posed a significant challenge. To increase complications, this circuit intended for portable applications, making power consumption a significant factor.

The expected requirements for our analog-to-digital converter is to operate on low to mid frequency analog signals, at a resolution of 10bit or higher, and to have power consumption on the order of microWatts in CMOS 0.35um technology. This thesis describes the process of designing such an ADC.

1.1 Traditional Designs

Before searching for a new design method it is important to understand why the traditional analog-to-digital conversion systems may be inadequate for the required application.

Flash converters are known for high precision and high speed operation. This circuit operates by defining every possible signal level with a reference and using comparators to associate each input sample with the corresponding digital code. For a 10 bit converter, this architecture would require 1024 accurate reference levels and comparators, which incurs large area and consumes a significant amount of power.

Scaling circuits help to minimize design complexity by reusing analog components for successive scaling of the input signal. These converters use current or charge scaling to narrow down the input level over several clock cycles. Scaling converters can produce high accuracy using relatively small layout areas, at the cost to the sampling rate. Switching noise and component mismatch limit the accuracy of such devices, particularly so for digital SOCs.

Similar techniques can be used to create an ADC that can be used to sweep the possible voltage levels until one matches the input. The digital code that results in the correct voltage level is the ADC output. The sweeping pattern can be adjusted to improve precision or bandwidth limitations. Once again, this technique is only as accurate as the precision of the components and level of noise allow.

While all of the above architectures can provide the necessary accuracy, they are not necessarily power conscious. Oversampling converters are effective where the signal bandwidth is much smaller than the effective sampling rate. For a sucsessive approximation converter, this means that the signal change is small from sample to sample, and the converter needs to track a much smaller input range. A smaller tracking range requires fewer scaling operations per sample, and therefore lower power consumption per sample. Although the successive approximation converter still requires accurate component matching, the fast sampling rate can help offset device limitations.

1.2 Delta Sigma Modulator

Under certain conditions, an oversampling converter can use a combination of multiple samples to offset its imprecision. This means that a high speed low precision converter can emulate a low speed high precision converter providing a direct tradeoff between the sampling rate and the digital precision. A large number of one bit samples can be combined to represent one sample at high resolution. This has a distinct requirement that the samples be interrelated through some error function.

A train of one bit samples is nothing more than a train of digital pulses at a fixed rate. A digital word can be obtained by integrating several samples. The signal information is carried in the cummulative magnitude of the samples and not in the pulse rate; the pulse rate is just the carrier signal. This is similar to communication devices that use high frequency signals to transport low frequency data; it is called modulation.

An analog input signal is modulated onto a digital clock, so that it can be transported through the digital medium. The modulated signal has analog properties, yet it is completely digital. An analog filter can recover the input signal, a digital filter will accumulate the samples into a digital word.

A circuit capable of creating the above described bit stream is called Delta Sigma (or Sigma Delta) modulator, where Delta indicates a negative feedback system and Sigma implies integration. Modulated bit streams have been used for a long time for Digital-to-Analog conversion. More recently, the Delta Sigma modulators have emerged as the means for Analog-to-Digital conversion.

The high operational frequency qualifies the Delta Sigma as an oversampling converter. In reality it offers much more functionality that what is described in this thesis.

A Delta Sigma system provides several benefits over conventional methods. The use of negative feedback makes this system self-correcting; the error of one sample is factored into calculating the next sample. The output of the modulator can thus be made more precise than what the internal components allow. This is called component de-sensitivity.

Integrating function in the Delta Sigma can be used to correlate individual samples in order to enhance overall accuracy and error correction. The performance of the entire system can be adjusted through the integrator, which is easier than dealing with multiple reference schemes.

Delta Sigma modulator does not require a large number of components. It can be made compact, and with fewer analog requirements than other types of ADCs, it is easier to fit into a digital environment. With fewer devices drawing current it also has a good potential for low power applications.

The one bit operation is an interesting concept for Analog-to-Digital conversion. The requirements are different than for converters with multi-bit samples. The data rate can be made very high, however, it is processed one bit at a time. Simple boolean operations can replace the bulky multi-bit processors to achieve much of the same effects, and that is a benefit on its own. Furthermore, the serial bit stream is versatile, it can be processed, filtered, stored, and de-modulated to an analog signal, it can be accumulated into multibit words, and it can also be transmitted through a single digital wire.

The Delta Sigma architecture has the best fit for the initial requirements of our project: It is suitable for low power operation. It is capable of achieving a 10 bit resolution. Although this architecture is not optimal for high frequency signals, our target application rarely requires high frequency signals to be measured. Finally, it is a compact system, and it has the best potential to be integrated into a digital environment.

For the reasons above, we have chosen the Delta Sigma modulator architecture for our project.

CHAPTER 2: Background Information

This chapter reviews the fundamentals of Analog-to-Digital conversion. Several architectures are discussed and evaluated for performance and power consumption. The final section addesses the concept of one-bit conversion and its application to low power.

2.1 Fundamentals of Analog-to-Digital Conversion

The function of an analog-to-digital converter is to measure the level of a specific signal and represent that level in a binary digital format. This digital representation can be processed and propagated through a digital system without any degradation.

An analog voltage V_O is normalized as a fraction of some reference voltage Vref defined by system parameters. The digital word that represents this fraction is expressed as:

$$D = \frac{V_O}{Vref} = b_1 \cdot 2^{-1} + b_2 \cdot 2^{-2} + \ldots + b_N \cdot 2^{-N} \qquad 2.1$$

Here, N is the number of bits in the digital word, and *b* is a binary bit. [23] When an analog signal is converted into this binary representation, it is effectively quantized into 2^N discrete levels. The separation between two adjacent levels is represented by the least significant bit (LSB) of the digital word, and is illustrated in Figure 2.1 for a three bit converter. For a voltage $V_O <$ Vref, LSB is defined by:

$$\text{LSB} = \text{Vref} / 2^N \qquad 2.2$$

Since a digital word is limited to N bits, this quantization has a finite resolution that results in a quantization error:

$$\text{Error} = 1/2\ \text{LSB} = \text{Vref} / 2^{N+1} \qquad 2.3$$

The quantization error is imposed by the finite length of the digital word, and thus it is inherent to all analog-to-digital converters.

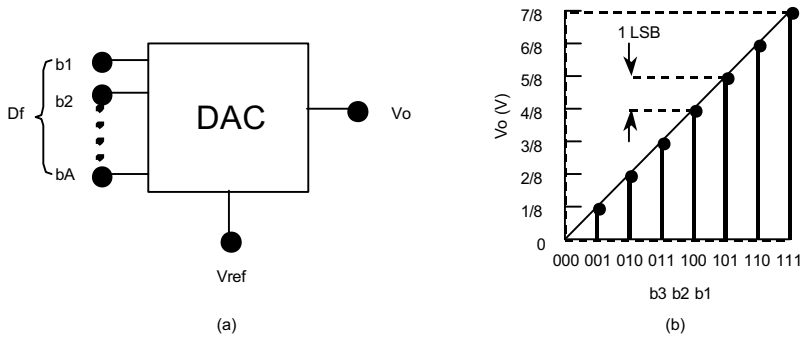

Figure 2.1 Quantization Error

The quantization error described above is imposed by the word size, and not necessarily by the precision of the converter itself. The actual performance of an ADC depends on the noise and distortion properties of the circuit itself. A signal-to-noise ratio (SNR) indicates the quality of the analog components in the system.

$$SNR = \frac{Vref}{NoiseAmplitude} \qquad 2.4$$

Distortion in an ADC output is the error caused by the circuit operation. Patterned distortion is a linearity and gain mismatch that can be observed over the entire ADC range. The maximum error resulting from the patterned distortion is called the *integral nonlinearity*, INL and it is illustrated in Figure 2.2.

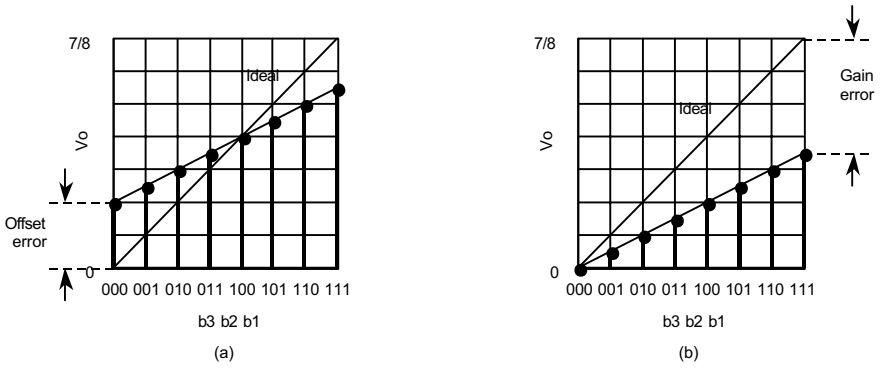

Figure 2.2 Integral Nonlinearity (INL)

Similarly there are repeatable deviations from the ideal output that do not follow a linear pattern, or deviations that are unique to each quantization level. These effects are illustrated in Figure 2.3, where each state has a constant deviation from the ideal output but has no correleation to the error of any other state. The maximum output deviation from the expected output is called *differential nonlinearity*, DNL, as illustrated in Figure 2.3.

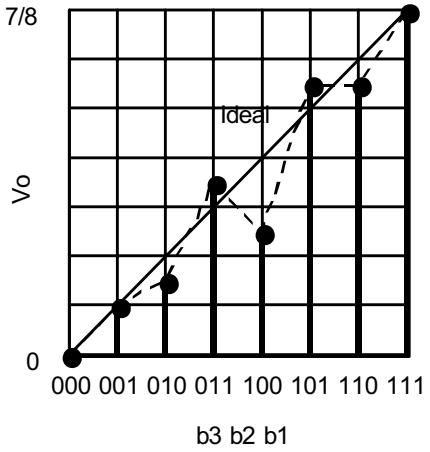

Figure 2.3 Differential nonlinearity (DNL)

The effective resolution of an ADC is determined from the maximum combined error from noise and distortion; the signal to noise and distortion ratio (SNDR) is a direct measure of the converter accuracy:

$$SNDR = \frac{Vref}{\text{Noise Amplitude + Distortion Ampliutude}} \geq 2^N \qquad 2.5$$

Here, the Distortion Amplitude is the maximum distortion due to INL and DNL effects, and N is the effective output resolution of the ADC circuit in the number of bits. [1] For a converter with an SNDR of 61dB, the reference voltage is 1,122 times larger than the distortion, leaving 1,122 voltage levels that can be uniquely distinguished, which is sufficient for an 10 bit converter with 1024 distinct levels.

There are other critical properties that must be considered such as sampling rate, power consumption, circuit area and in some cases signal bandwidth. It is important to keep all of the above measures in mind when evaluating a specific ADC architecture, because each architecture enhances certain properties at the expense of others.

2.2 Analog-to-Digital Converter Architectures

There is a multitude of ADC architectures that have evolved over the years. Each architecture offers specific benefits which are useful for particular applications and not others. This section describes several ADC designs with their benefits and drawbacks.

Nyquist rate ADCs are those whose sampling rates are sligtly above the Nyquist frequency, while oversampling ADCs sample at a much higher frequency than the Nyquist rate. Since such a converter produces more samples than required to recover the original signal, the output can be enhanced through digital signal processing.

2.2.1 Nyquist Rate ADCs

Flash or parallel converters, such as the one shown in Figure 2.4, take the most straight forward approach by providing a reference voltage for every quantization level and performing 2^N comparisons for each sample. This allows a very fast ADC conversion with an output every clock cycle. On the flip side, this architecture requires 2^N comparators and references, so the circuit complexity grows exponentially with the number of resolution bits. In addition to the growing complexity, it becomes increasingly difficult to generate accurate reference signals for higher resolutions, therefore flash converters are limited to small word sizes [17],[19].

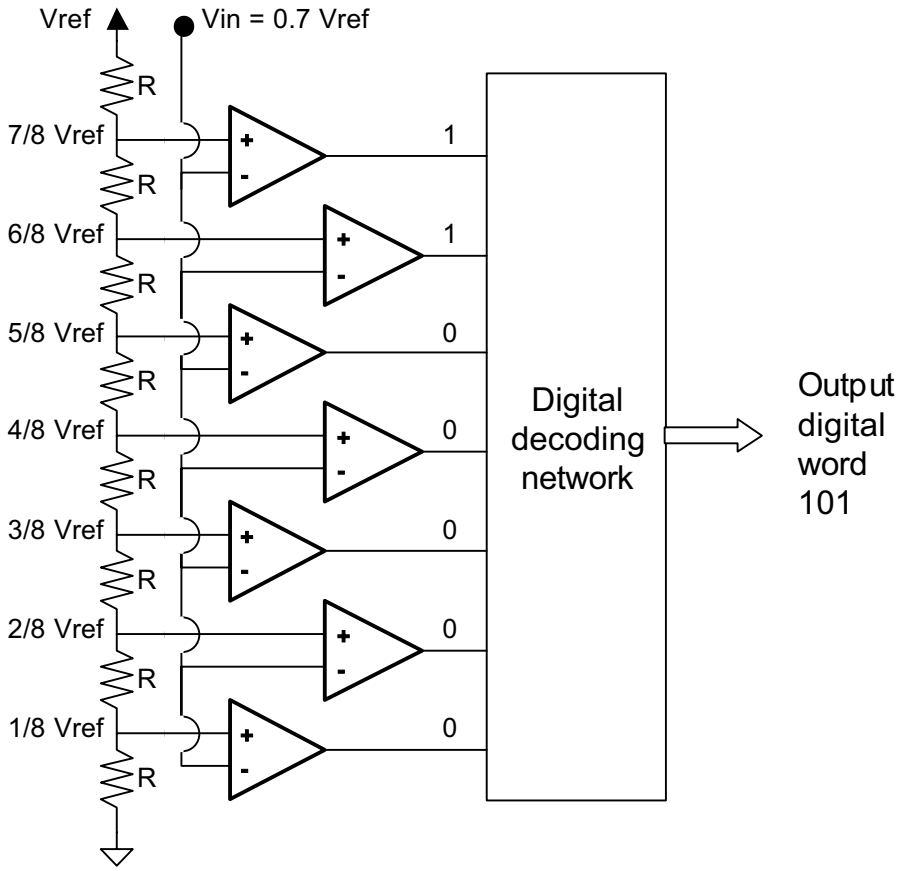

Figure 2.4 Flash ADC

Successive approximation ADC uses iterative techniques to narrow down to the correct output level. These techniques include voltage, current and charge scaling. The iterations allow the same hardware to be reused by determining the word over several clock cycles. Successive approximation ADC are much smaller than comparable flash converters at the price of a lower sampling rate [17],[19]. Figure 2.5 illustrates the successive approximation algorithm.

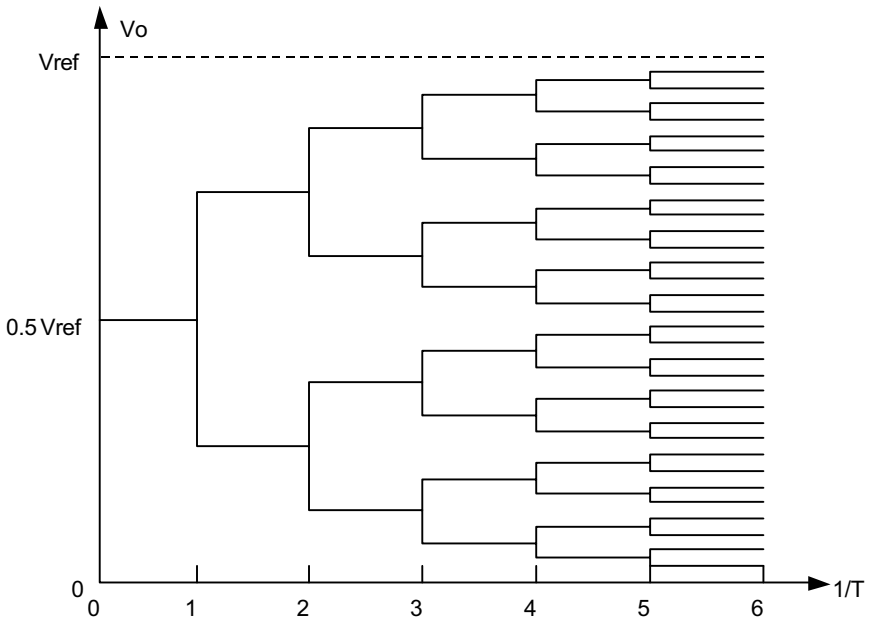

Figure 2.5 Successive Approximation Algorithm

The trade off between area and sampling rate is taken even further with a serial ADC architecture illustrated in Figure 2.6. A ramp generator or a digital-to-analog converter (DAC) is used to sweep a reference voltage over the entire quantization range until the level closes to the input voltage is found. The entire voltage range is swept over 2^N clock cycles, and a digital counter is used in determining the exact point on the voltage ramp that corresponds to the input. This architecture requires only one comparator, and can be implemented using simple hardware. The price for compactness is the 2^N cycles required to quantize a single sample, which is extremely slow [17],[19].

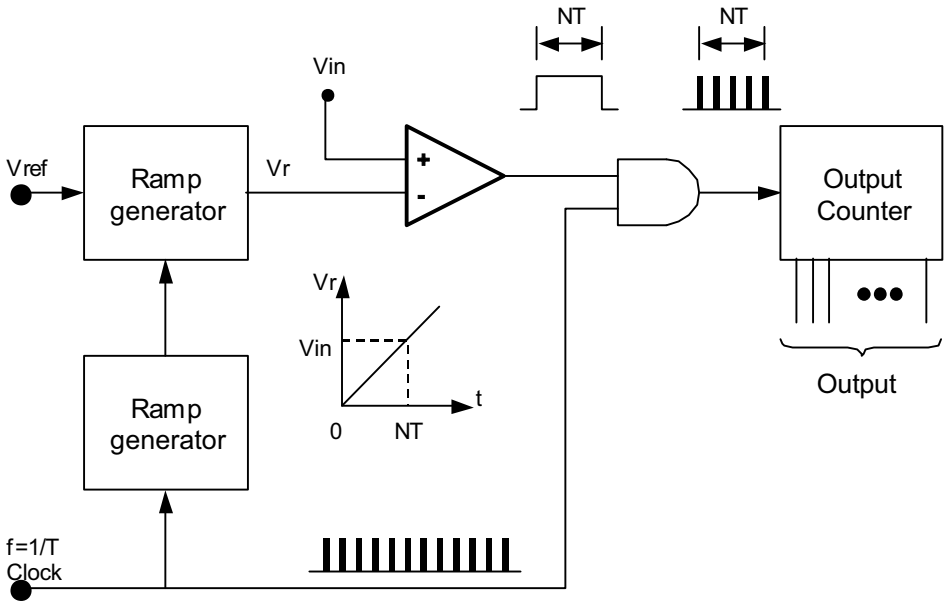

Figure 2.6 Serial ADC

2.2.2 Oversampling ADCs

An oversampling ADC based on a Delta Sigma modulator is shown in Figure 2.7. Delta sigma modulation is a technique for encoding a measurable quantity into a one bit digital pulse string. Contrary to the previous architectures, the signal is not only quantized in voltage but also in time. Delta Sigma converters are also called single bit ADCs, since the digital output has only two levels. The details of delta sigma ADC architecture are explained in Chapter 3.

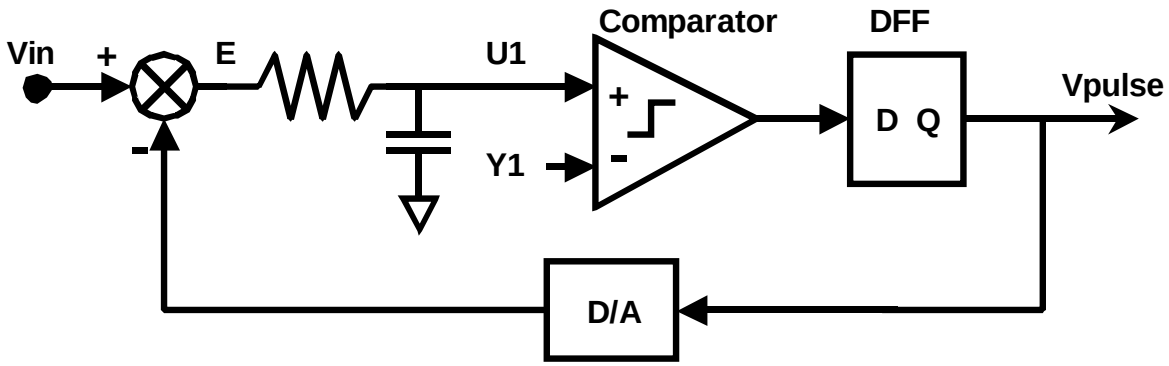

Figure 2.7 Delta Sigma Modulator

The benefit of a delta sigma modulator system is due to only two quantization levels, so that the analog circuitry is simple and the power consumption is low. This architecture also ensures perfect linearity since the gain line is defined by only the two points. The drawback of this architecture is the additional digital processing required to produce multibit output words from the single bit stream. This extra step is an explicit trade-off between effective bandwidth and effective quantization level [1],[2],[3].

2.3 Analog-to-Digital Converters for Low Power Operation

The main objective of this research is to find an architecture suitable for low power operation of ADCs. This section describes several categories in selecting such an architecture.

The first category is the required circuit complexity; fewer devices draw less power. The flash architecture is bulky and for that reason it is rarely considered for low power applications. Combined architectures are also rarely used for low power application due to the implied complexity and accumulation of supporting circuits.

The second category is the static current draw. Since the major source of power consumption in the analog circuits is due to static current, this is an important area to minimize. This means that the circuit must not rely heavily on resistive voltage dividers and current mirrors, which can draw significant quantities of static current. Circuits that rely on scaling voltage or operate on

multiple currents are power hungry by nature. This also puts limits on high gain circuits, since a good gain requires large static current.

A category which is often overlooked is the energy efficiency, or how much power is consumed to produce one output word. For instance, successive approximation converters consume less power than flash ADCs, however they take N times longer to produce an output word. It is worth noting that a particular flash ADC may have a higher energy efficiency than the successive approximation converter. In cases where both energy and performance are critical, energy efficiency must be considered.

The final consideration goes to power consumption by the supporting circuitry. Circuits such as voltage references, voltage regulators, sample and hold, voltage-to-current and current-to-voltage converters are often necessary in ADCs. Although they are not explicitly considered in block diagrams of ADCs, they are a significant source of power consumption. Systems that require minimal supporting circuitry tend to be more power efficient.

2.4 Review of Contemporary Analog-to-Digital Converters

Low power ADCs receive more attention in industry, and the following reviews include several ADCs targeting industrial applications.

This thesis targets low power ADC design with low-megahertz sampling rates with output resolutions larger that 10 bits. Since performance and power consumption are the most critical factors in these designs, the following criterion was used to compare ADCs across different architectures.

$$PerformanceFactor = \frac{SamplingRate \times EffectiveResolution}{CurrentDraw} \qquad 2.6$$

Where Sampling Rate is measured in megasamples per second (MS/s), Effective Resolution is in bits, and Current Draw is in mA. Higher Performance Factor indicates better performance.

Bourgette, Cavalari and Luo proposed a successive approximation ADC in 0.25um CMOS technology. [27] Their ADC uses switched current to achieve a 12 bit resolution with an effective

sampling rate of 1.7 MS/sec while drawing up to 4mA of current. This yields a performance factor of 5.1

A low power ADC based on a redundant signed-digit cyclic algorithm was design by Aust at Virginia Tech. [26] This design was created in a 0.35um CMOS technology, and claims to achieve a 12 bit resolution at 1.7 MS/s while drawing 1.8mA. This ADC achieves identical performance as the successive approximation converter proposed by Bourgette et al [27] but comsumes only half the power. The performance factor for this ADC is 11.3.

Delta Sigma architectures also have a great potential for low power applications. Norsworthy, Schreier and Temes used a second order Delta Sigma modulator to achieve 16 bits of resolution at a sampling rate of 12.8 MS/s and a current draw of 2.76 mA. [28] This has a performance factor of 74.2, much greater than the previous designs due to the high output resolution.

A low power approach to Delta Sigma design was proposed by Peluso, Steyaert and Sansen. [10] A third order Delta Sigma modulator was implemented in 0.7 um CMOS technology, and yielded a 10 bit resolution at a sampling rate of 500 kS/s and a current draw of only 67 uA. The performance factor for this ADC is 75. This is a good example for the trade-off between performance and power consumption. A more recent design by the same researchers in 0.5um technology uses a differential switched Op-Amp technique to minimize power. They achieved a 10 bit resolution for a 1.5 MS/s rate with a current draw of only 45 uA. The performance factor for this ADC is 333.

The above examples show that the Delta Sigma modulator has a tremendous potential in low power ADC design. The design by Bourgette, Cavalari and Luo is considered a low power ADC, but it is outperformed by the Delta Sigma designs by factors of 15 to 65 times. While this may not be true in all areas of consideration, a Delta Sigma converter is a good candidate architecture for low power design.

2.5 Feasibility of a Low Power Delta Sigma ADC

ADCs described in the previous section illustrate the potential of Delta Sigma modulation for low power consumption. Peluso, Steyaert and Sansen claimed that Delta Sigma architecture is superior in low frequency operation and low power consumption.

A potential problem for the ADCs described in previous section, is that they were tested as stand-alone devices with dedicated external components and low noise test boards. Integrating such ADCs into a digital environment where I/O is scarce and noise is abundant is not a trivial task. The main focus of our research is to design a Delta Sigma ADC in an all-digital environment, hence our ADC is useful for ASIC and SOC applications. The delta sigma functionality of the devices above has to be mapped into a digital CMOS technology with limited internal capacitances, resistances and device matching.

CHAPTER 3: Delta Sigma Modulator Overview

This chapter is an overeview of Delta Sigma modulation and its applications to Analog-to-Digital conversion. Key topics cover the modulation theory, modulator structure, noise shaping and implementation techniques. The final section describes application of the theory to a practical component design.

3.1 Modulation

Analog-to-Digital conversion is a process of taking an analog data signal and transforming it into a form that can be propagated through a digital system. Although similarities between traditional ADC and modulation systems are superficial, this concept can be pursued further drawing on the knowledge base in both fields.

First, let us define the transmission medium suitable for a digital system. Drawing from a single channel concept, a signal is transmitted through a single wire. A single wire binary digital signal can only assume two states: one or zero, it is a single bit system. Furthermore, the transmission frequency is limited by the system clock; only one bit can propagate in one clock cycle.

Pulse Code Modulation (PCM) uses the system clock as a carrier signal. The amplitude of the analog signal is represented in terms of pulse density. Figure 3.1 illustrates how an analog function u(t) is sampled and quantized using a 3-bit binary code to form a discrete time function u(k). The values of u(k) are illustrated along the x-axis. The 3-bit quantized values are converted into a 1-bit waveform v(k), by representing the sample amplitude with an average of several pulses. The pulse rate of v(k) must be at least 2^3 times larger than the sample rate of u(k) to accomodate the same resolution. [29]

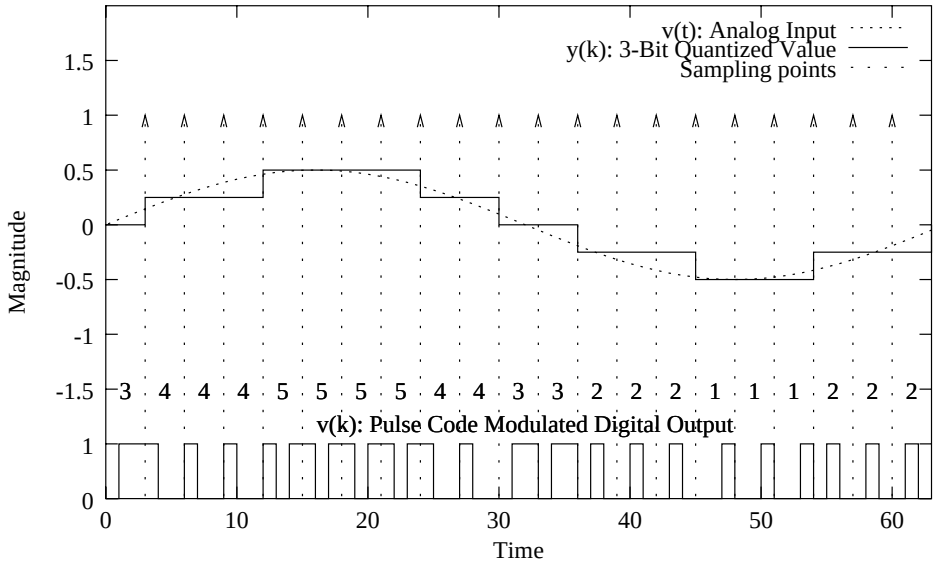

Figure 3.1 Pulse Code Modulation

PCM encodes an analog signal onto a 1-bit waveform. It is not an optimal solution because it does not lend itself to a simple algorithm. Furthermore, the pulse order and location is arbitrary making signal recovery difficult. A good modulation system must define a pattern in addition to the parameters.

Delta modulation (DM) has been used for several decades to convert analog signals into digital pulse streams for improved noise immunity during transmission. It offers the benefits of structure based conversion, which is simple to implement and provides a pattern that can be used for signal recovery. A delta modulator system is illustrated in Figure 3.2.

Delta modulation is an iterative algorithm, it calculates every successive pulse in y(k) based on the accumulated error s(k). Figure 3.3 illustrates the function of the Delta Modulator. Unlike the PCM procedure where sampling is performed every 2^N clock cycles, the input waveform is sampled every clock cycle in a DM. This means that the input signal can be tracked more accurately and an error correcting pattern can be established.

Delta Modulator is a differentiator. Each pulse in v(k) is a quantized difference between the input signal and the accumulated output f(k). This effect is illustrated in Figure 3.3, the output is high when the input signal u(k) is larger than the feedback f(k). In order to recover the signal, the pulse stream must be filtered to remove the clock frequency and integrated to counteract the differentiation effect of the modulator.

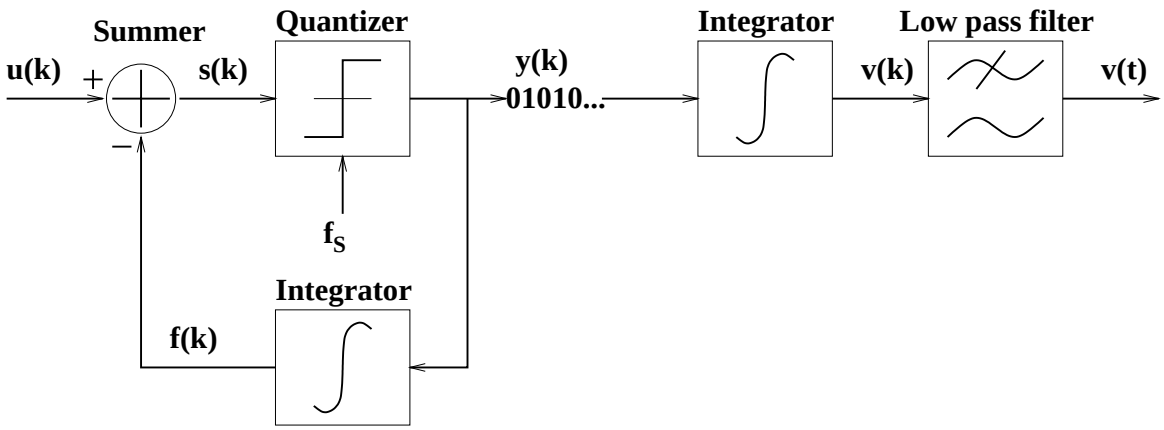

Figure 3.2 Delta Modulator [29]

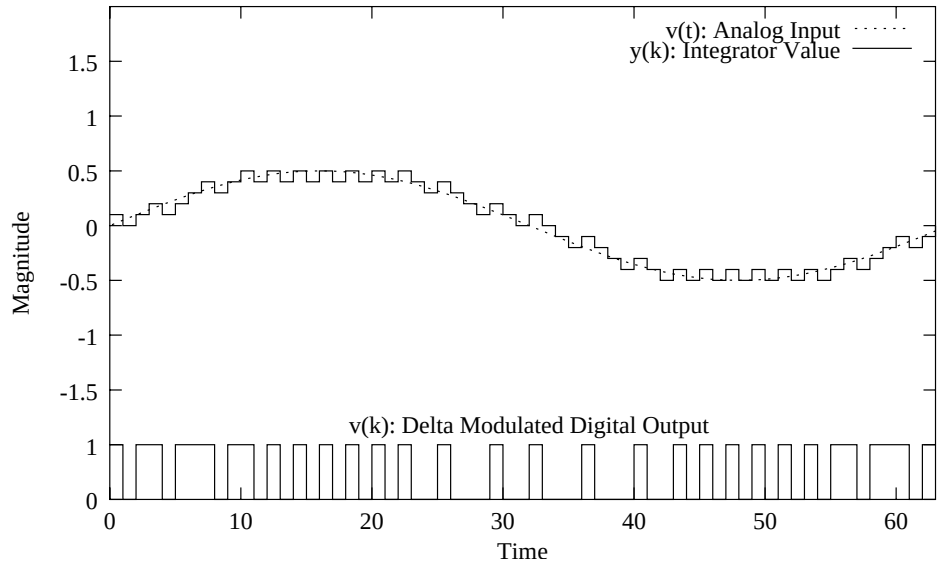

Figure 3.3 Delta Modulation Signals

Delta modulator encodes a differential of the input into a single bit stream. If the input signal is DC, it does not change, and the delta modulator will fail to track it. Figure 3.4 illustrates the inability of a delta modulator to track a DC input.

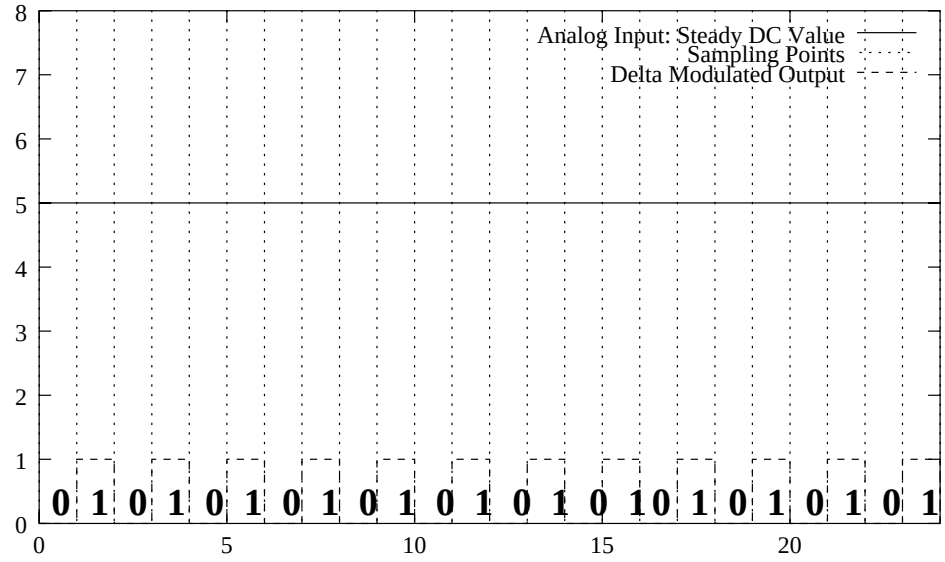

Figure 3.4 Delta Modulation of a DC signal

By extension, problems that affect DC signals may affect other signal frequencies. When the frequency is too slow for a delta modulator, the output suffers from granularity problems shown in Figure 3.5. When the output changes too fast, the delta modulator can not track it either, and the modulator output suffers from a slope overload shown in Figure 3.6. For these reasons delta modulator is useful only for bandlimited high frequency AC signals, which is inadequate for most ADC systems. [2],[28],[29]

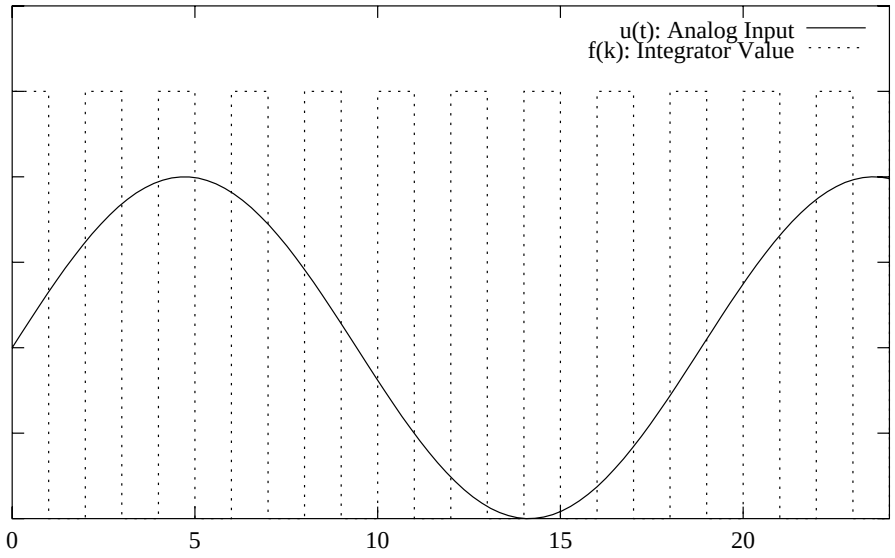

Figure 3.5 Delta Modulator with Granularity Problems

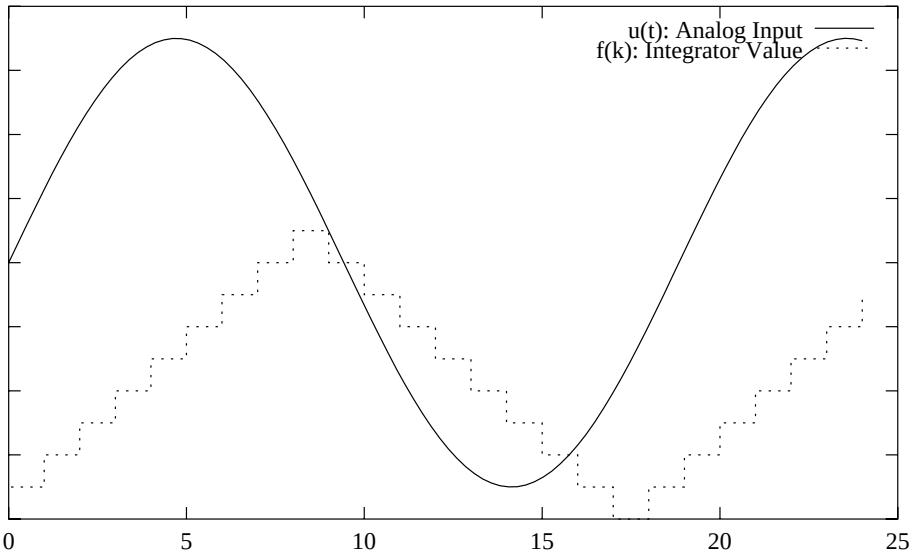

Figure 3.6 Delta Modulator Suffering from Slope Overload

Another problem for using a delta modulator for an ADC system is the integration required to recover the signal. By design this operation accumulates quantization error and noise, which makes it difficult to transmit high quality signals.

The drawback of the delta modulator can be rectified by integrating the input signal as illustrated in Figure 3.7. [2],[28],[29] The ouput of the new structure, y(k), is a pulse representation of the input signal. Furthermore, since the demodulation process no longer requires integration, the error is not accumulated when v(k) is recovered. This change is still dependent on matching of the two integrators, but makes high precision design more feasible.

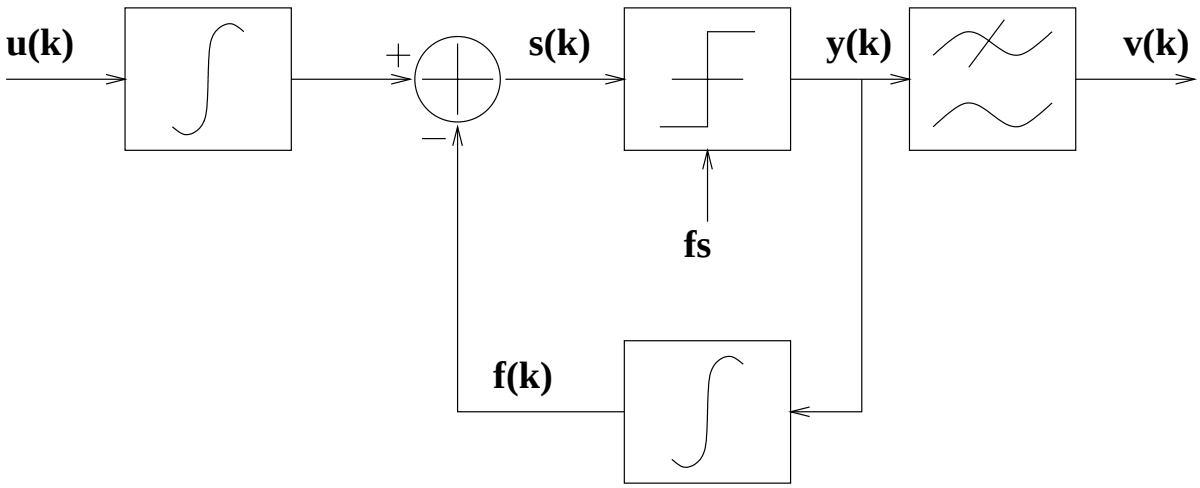

Figure 3.7 Improved Delta Modulator

3.2 Delta Sigma Modulation and ADC

Delta Sigma modulator is a feedback system based on the delta modulator. Figure 3.8 shows the structure of a Delta Sigma modulator using a single integrator, quantizer, DAC and a delay element. Because there is one integrator in the forward loop, the structure in Figure 3.8 is called the First Order Delta Sigma modulator.

For an input signal u(k), Delta Sigma modulator generates a corresponding bit pattern v(k). The feedback signal f(k) is the DAC equivalent of quantized input, which is extracted from v(k). The quantization error, s(k) is the difference between the input and the output. The integrator accummulates the errors of several bits into y(k), and this indicates whether the output representation is higher or lower than required. The quantizer processes the error on y(k) and generates a 1

to pull up the output or a zero to pull it down to correct the error. The resulting pulse becomes a part of the output pattern v(k), which, in its turn, goes through the feedback loop.

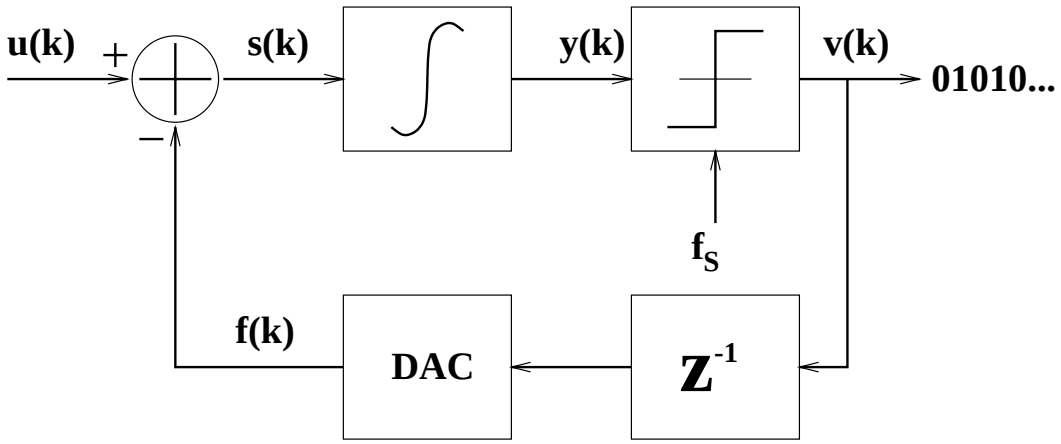

Figure 3.8 Delta Sigma Modulator

For a one-bit Delta Sigma modulator, the quantizer is a comparator with a digital output, and a DAC is a circuit that converts the high and low digital pulses into high and low analog voltages. Since Delta Sigma converts an input from one domain to another, amplification is undesirable, and the feedback loop and the DAC must have a gain of 1.

As a result of a unity feedback, Delta Sigma modulator converts the amplitude of the input signal into a corresponding pattern of binary pulses as seen in Figure 3.9. Each ampitude level on the input corresponds to a specific pulse density on the output; the higher the input the greater the number of ones on the output. [28][29] Note, that since Delta Sigma tracks the amplitude of the input signal, it is possible to encode DC signals as well as AC.

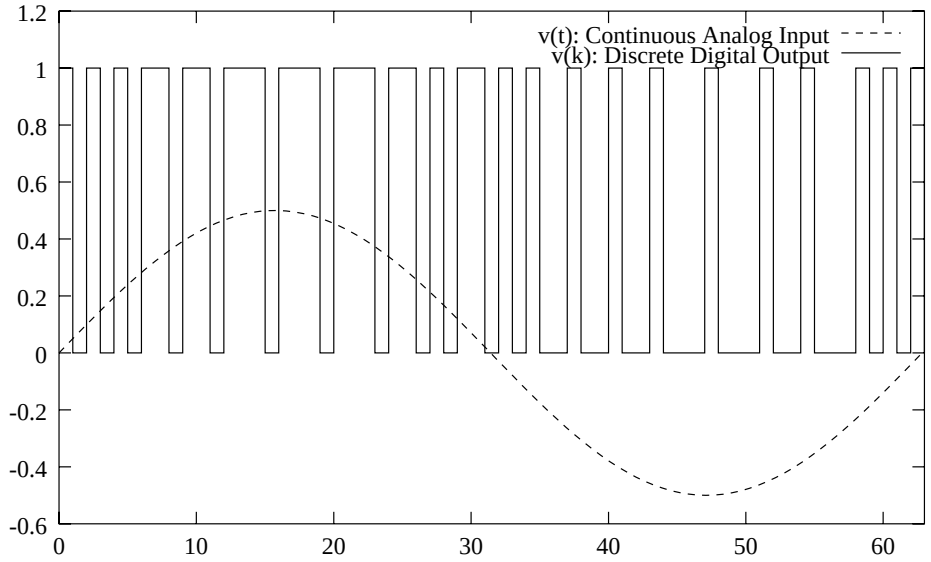

Figure 3.9 Delta Sigma Modulation of a Sample Waveform

The Delta Sigma operation can also be viewed as encoding the amplitude of the input into the duty cycle of the output waveform, where a quantized input amplitude is proportional to an average amplitude of several output pulses. Every quantization level has a unique corresponding pulse pattern.

For the purposes of illustration, the integrator in the Delta Sigma loop can be modeled by a forward Euler integrator shown in Figure 3.10.

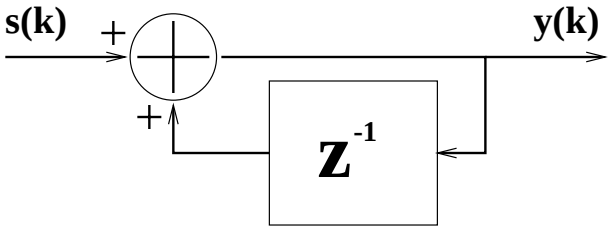

Figure 3.10 Forward Euler Integration

The z-transform of the forward Euler integrator looks like this:

$$\frac{Y(Z)}{S(Z)} = \frac{1 + Z^{-1}}{1 - Z^{-1}} \qquad (3.1)$$

The quantization error for the above system is a function of the Signal to Noise and Distortion Ratio (SNDR) of the Delta Sigma Modulator and the number of pulses available for each sample. The error due to Noise and Displacement is modeled in Figure 3.11. Here the output is represented as:

$$v(k) = y(k) + e(k) \qquad (3.2)$$

where e(k) is the modeled error. The z-transform of the Equation 3.2 is:

$$V(z) = Y(z) + E(z) \qquad (3.3)$$

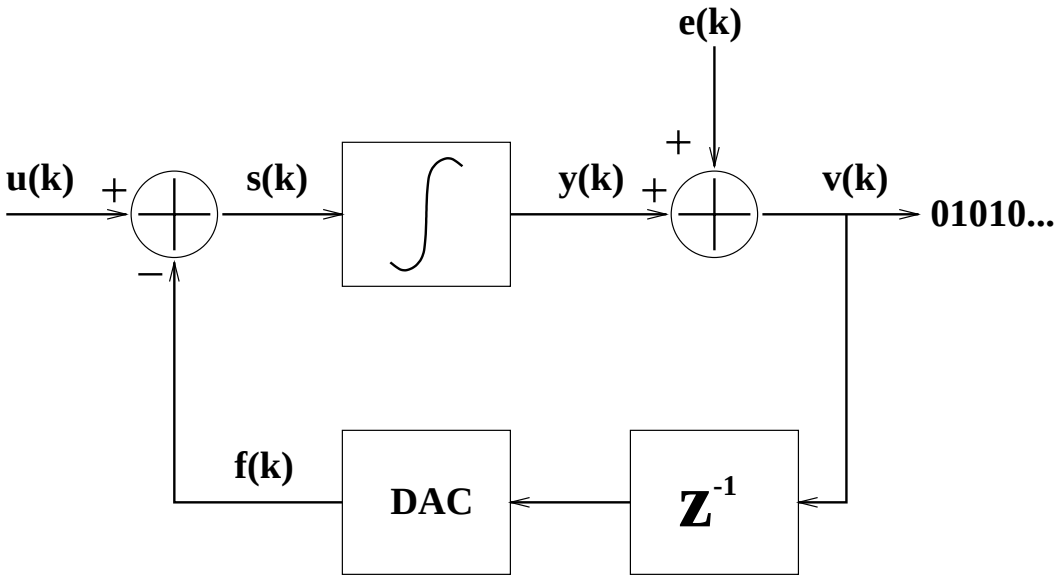

Figure 3.11 Delta Sigma Modulator with a Modeled Noise Source

The integrator output Y(z) can be defined as:

$$Y(z) = V(z) - E(z) = z^{-1}Y(z) + U(z) - z^{-1}V(z) \qquad (3.4)$$

The loop equation is derived by subsituting Equation 3.3 into Equation 3.4:

$$V(z) - E(z) = z^{-1}Y(z) + U(z) - z^{-1}(Y(z) + E(z)) \quad (3.5)$$

$$V(z) - E(z) = U(z) - z^{-1}E(z) \quad (3.6)$$

$$V(z) = U(z) + (1 - z^{-1}) E(z) \quad (3.7)$$

More generially the First order tranfer equation can be written as:

$$V(z) = U(z) + H(z) E(z) \quad (3.8)$$

The error E(z) in Equation 3.8 is attenuated by the component H(z), in this case acting as a highpass filter for noise. This effect is illustrated in Figure 3.12 for a sine wave input on u(k) and random noise on e(k). The plot's x-axis is the normalized frequency with respect to the clock frequency, and the sine wave frequency is 128 times smaller. It can be seen that the noise on e(k) is attenuated at lower frequencies and allowed to pass at the higher end of the spectrum. The noise energy is effectively moved from the signal band to higher frequencies where it is less significant. This process is called "noise shaping," because the noise spectrum is shaped to be away from the signal band. As a result of this manipulation, the Delta Sigma modulator has a high SNR in the signal band even though it only uses a single bit of resolution. [32]

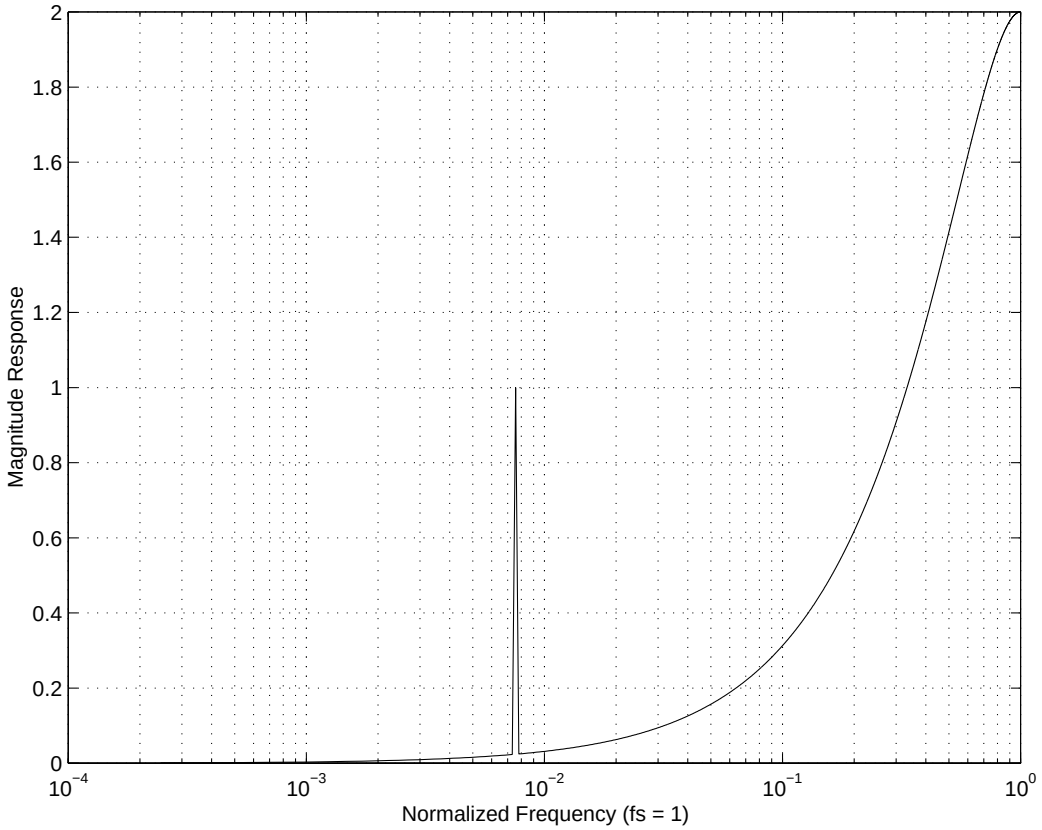

Figure 3.12 Noise Shaping in a First Order Delta Sigma Modulator

The generallization used above assumes that the quantization noise is uncorrelated white noise. This assumption fails for DC inputs where the quantization noise forms a pattern dependent on the input level and the natural frequency of the Delta Sigma modulator. [33] This patterned noise is difficult to suppress by itself, and must be reduced by dithering the input signal to reduce the correlation.

3.3 High Order Delta Sigma Modulation

As first order filters are limited in suppressing unwanted frequencies, first order Delta Sigma modulators are also limited in their ability to shape quantization noise. A second order Delta Sigma modulator is illustrated in Figure 3.13.

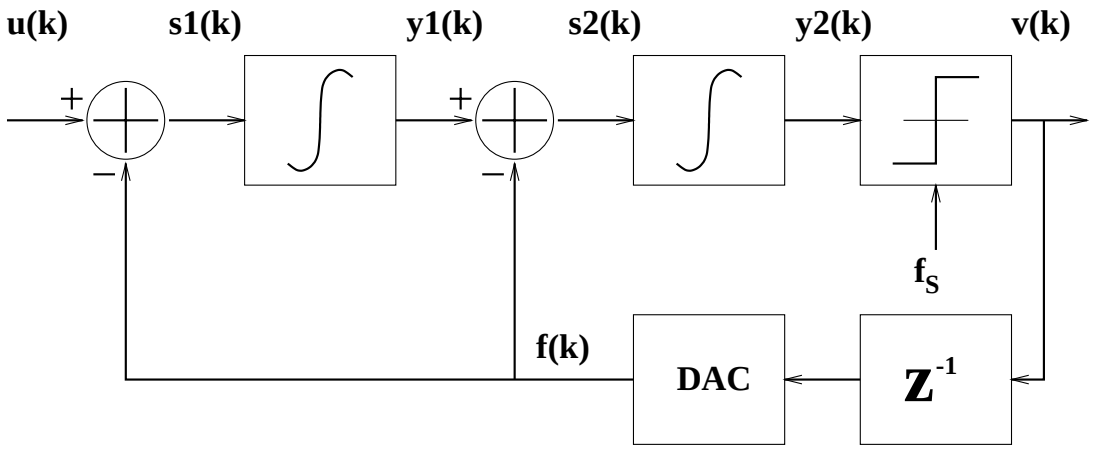

Figure 3.13 Second Order Delta Sigma Modulator.

A transfer function for the second order modulator can be derived as follows:

$$V(z) = Y_2(z) + E(z) \tag{3.9}$$

$$Y_1(z) = z^{-1}Y_1(z) - z^{-1}V(z) + U(z) \tag{3.10}$$

$$Y_1(z) - z^{-1}Y_1(z) = U(z) - z^{-1}V(z) \tag{3.11}$$

$$Y_1(z) = \frac{U(z) - z^{-1}V(z)}{1 - z^{-1}} \tag{3.12}$$

$$Y_2(z) = z^{-1}Y_2(z) - z^{-1}V(z) + Y_1(z) \tag{3.13}$$

Substituting Equation 3.9 into Equation 3.13:

$$V(z) - E(z) = z^{-1}Y_2(z) - z^{-1}V(z) + Y_1(z) \tag{3.14}$$

$$V(z) - E(z) = z^{-1}Y_2(z) - z^{-1}(Y_2(z) + E(z)) + Y_1(z) \tag{3.15}$$

$$V(z) - E(z) = Y_1(z) - z^{-1}E(z) \tag{3.16}$$

Substituting Equation 3.12 into Equation 3.16:

$$V(z) - E(z) = \frac{U(z) - z^{-1}V(z)}{1 - z^{-1}} - z^{-1}E(z) \tag{3.17}$$

$$(1 - z^{-1})(V(z) - E(z)) = U(z) - z^{-1}V(z) - z^{-1}(1 - z^{-1})E(z) \tag{3.18}$$

$$V(z) - z^{-1}V(z) - E(z) + z^{-1}E(z) = z^{-2}E(z) - z^{-1}E(z) + U(z) - z^{-1}V(z) \tag{3.19}$$

The second order Delta Sigma modulator equation is:

$$V(z) = U(z) + (z^{-2} - 2z^{-1} + 1)E(z) \tag{3.20}$$

This corresponds to the general transfer function:

$$V(z) = U(z) + H_1(z)H_2(z)E(z) \tag{3.21}$$

where $H_1(z) = H_2(z) = 1 - z^{-1}$.

The second order Delta Sigma modulator has a steeper noise cutoff rate than the first order modulator, which allows better noise shaping. The noise in the signal band can be suppressed more effectively, and as a result, improve the SNR of the modulator. [1] Similarly by choosing appropriate H_1 and H_2 a band-pass system can be created. [1] The pulse patterns generated by a second order system exhibit more complicated behavior than the first order, which reduces correlation in the error signal. [33] Thus a higher order system reduces noise-related error on the output, and improves the output resolution and oversampling ratio.

The effect of higher order noise shaping can be best illustrated in Figure 3.14. Higher order modulators suppress noise more effectively at the target frequency. The additional precision can be used to improve the output resolution or to reduce the oversampling ratio and allow higher input bandwidth.

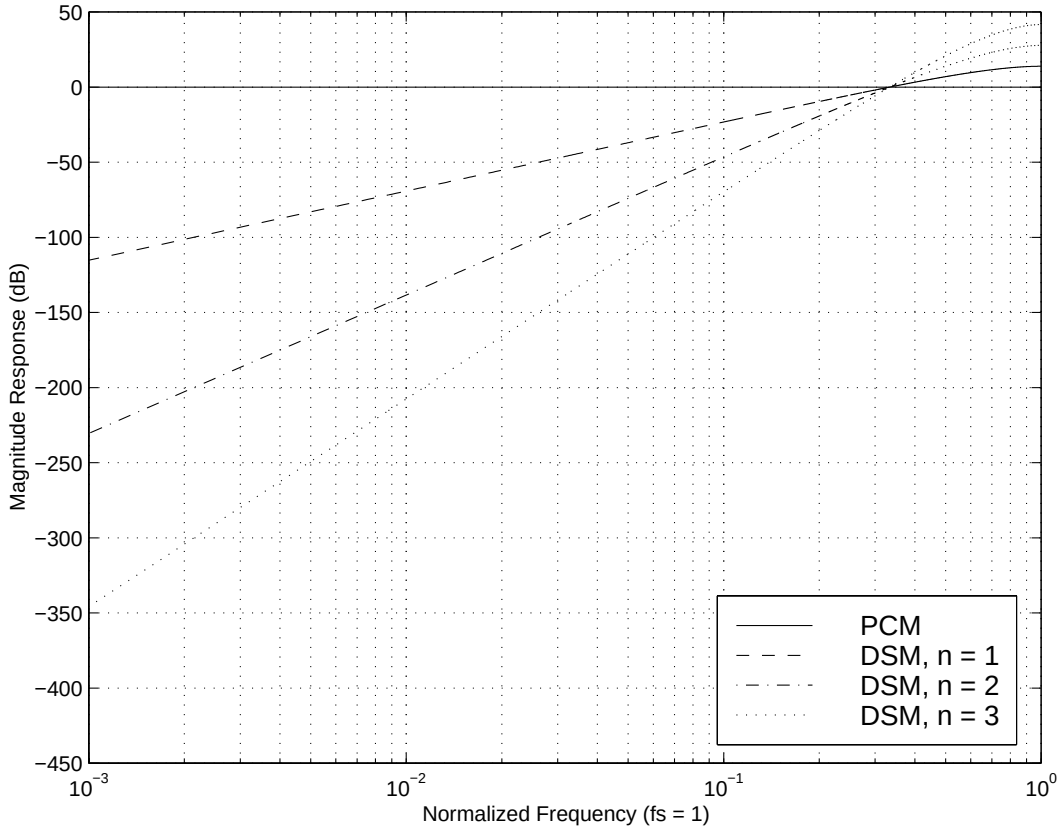

Figure 3.14 Attenuating Quantization Noise wich Pulse Code and Delta Sigma Modulators

The biggest deterrent to designing higher order systems is that system stability becomes a critical design factor as the order increases. Stability concerns and resulting design complexity make high order systems large and expensive to a point where they become unfavorable for many applications. Although there are many approaches to high order filter design and tradeoffs to be evaluated, they are beyond the scope of this work.

3.4 De-Modulation and Pulse Code Quantization

In order to assign a digital value to a sample, the duty cycle must be measured for a specific number of pulses. The easiest way to do this is to count the number of high pulses for a fixed number of periods and use that ratio as the digital word output. In order to use this method, the following condition must be met:

$$Word\ Length = N,\ and:\ \ T / Tclk = 2^N \qquad (3.22)$$

Where T is the duration of one sample and Tclk is the period of a system clock.

The condition in Equation 3.22 is necessary to convert a pulse count into an N-bit word without additional hardware. This is accomplished by selecting a window that relates to the clock by some power of 2. For an 8-bit word, this window will be 256 pulses wide. This digitizer architecture is illustrated in Figure 3.15.

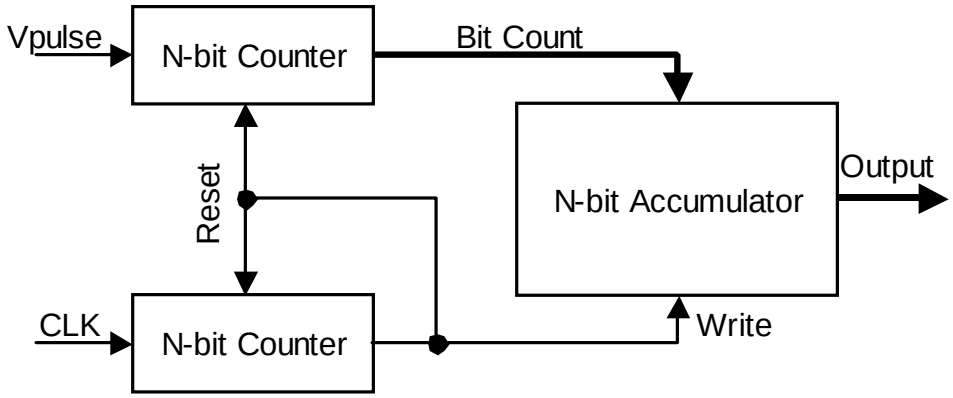

Figure 3.15 Basic Digitizer Architecture

The upper N-bit Counter counter accumulates the number of pulses in the signal Vpulse. The lower N-bit counter provides the Reset signal at every 2^N clock cycles, and the Bit Count is stored in the Output Accumulator. Since Equation 3.22 provides that N is also the word length, the ratio of the Vpulse bit count to 2^N is equivalent to Vin/Vdd.

The precision of the digitizer in Figure 3.15 can be increased by increasing N. It is a compact and effective quantization system that requires minimal storage and logic elements. The only drawback is it requires a long time to process one word and a large decimation ratio. For an 8-bit word, one sample is produced for every 256 cycles, which reduces the effective sampling rate by 256. The decimation ratio can be reduced by using several digitizers in parallel or adding a 2N memory element to store the entire sample window. Improving the input bandwidth is a more difficult task.

The circuit in Figure 3.15 is essentially an FIR integrator with a square window designed for a one bit input stream. By the same principles the FIR window can be reshaped to provide additional filtering features such as a wide signal band, and a lower noise floor. Several window schemes are illustrated in Figure 3.16.

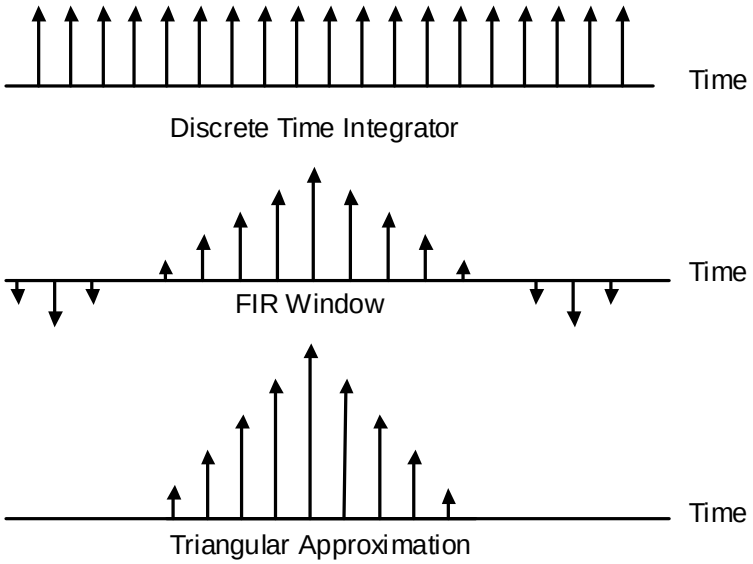

Figure 3.16 Sample FIR Windowing Schemes

A sinc pattern FIR window is frequently used for generating a sharp frequency cutoff. This pattern is complicated to generate, and requires high overhead if it is stored in memory. A compromise can be reached by using a triangular window which can be generated dynamically and

requires fewer cycles than the equivalent square window. Note that for any chosen window, the sum of the pulses must be the same in order to achieve a resolution of N.

A particular question is how can accurate results be obtained using fewer samples. Figure 3.17 shows the resolution ranges for a triangular window with 98 impulses. Such a window can be generated using a modified 7-bit up-down counter, with the highest pulse reaching $2^7 = 128$. The maximum output resolution of this system is $(2^7)^2 = 2^{14}$ steps, which makes the maximum word size 14 bits. Note that a square wave of the same length would only generate 6 bits.

Figure 3.17 shows that a 14 bit resolution is practical only for a small range of signals around 50% duty cycle. The triangular window uses high pulse density to enhanse the effective resolution of the signal as illustraged by the Worst Case curves.

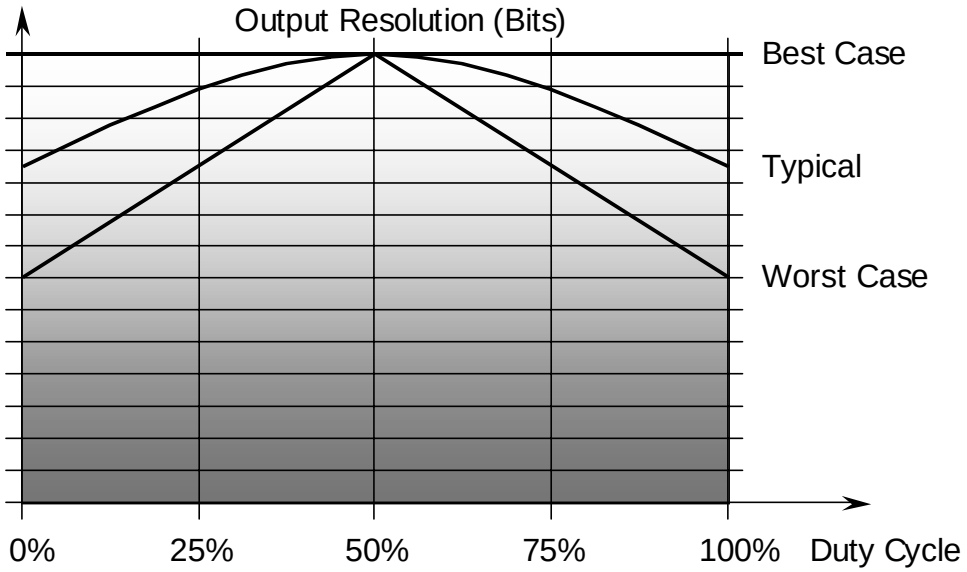

Figure 3.17 Expected Resolution for a 98-Impulse Triangular Window

The worst possible resolution occurs at the extremes of the input range and is equivalent to 7 bits. This case assumes the worst of pulse distribution and high levels of correlation wich are highly unlikely. The typical case curve takes into account the pulse density and the low levels of pulse correlation charactesistic of Delta Sigma modulators. It is reasonable to attain 13 bits of

resolution for a waveform between 25% and 75% of the input range. A critical point here is that the signal information is not only stored in the pulse quantity, it is stored in pulse order and the pattern of the bit stream.

A triangular window FIR has advantages for systems that can tolerate moderate decimation, in order to achieve higher precision. However, this system is much more demanding on physical resources, and it is costly to create a non-decimating version of this filter. It shows that Delta Sigma systems offer many possibilites, where the output precision can be enhansed and formatted using digital signal processing.

3.5 Design of Delta Sigma Modulator

In creating a low power Delta Sigma modulator, it is impoortant to understand not only the structure and function of the device, but the underlying principles and limitations behind it. For this reason, it is adventageous to consider higher level design and lower level practicalities at the same time. It is necessary to evaluate several architectures and to choose the most suitable approach for both high and low levels of abstraction.

When looking at the Delta Sigma design on block diagrams or high level transfer functions, it is difficult to estimate the power performance because the supporting circuitry is not accounted for. When considering the design in terms of subcomponents, it is difficult to keep track of system performance, because extra circuits required for intefacing often hinder system accuracy. The selective approach avoids many such pitfalls. The most relevant architecture can be selected by defining criteria for the Delta Sigma circuit.

3.5.1 Design Constraints

The target criteria for this design are circuit performance and power consumption. The performance requirement for this ADC is an accuracy of ten bits or higher at the output. In a Delta Sigma circuit this translates into SNDR of 60dB or higher. The power dissipation is evaluated as the total power consumed by the circuit components, the power required by supporting ciruicts such as references, and the power required by interface circuitry.

Delta Sigma is an architecture for digital systems where, high precision analog circuitry is technologically challenging. Whether the limitations are due to the available technology or the cost, significant limits must be assumed in a practical design.

The final design must operate on a single power supply, CMOS technology and internal capacitances of 10 pF or less. Using multiple supply voltages is constly because of additional power supplies and internal routing. The final limitation is area, particularly when it comes to passive components. Resistors and capacitors can be created accurately, however, their values are limited by available silicon area.

Aside for physical constraints there are practical design guidelines to be considered. Even though the accuracy of the Delta Sigma system is due to the feedback loop, evey stage that operates on the signal is a potential source of injected noise. It is a good practice to minimize the intermediate circuitry, particularly circuits that operate on the input signal.

Delta Sigma architecture should offer a degree of flexibility, so that it can be tuned or augmented to a higher order or turned into a multiple stage system. A modulator that is too rigid in design defeats the purpose behind a dynamic system. If a system is very demanding on its environment, it will not peroform well in the real world.

A modular system provides design flexibility by its nature. The ability to tune or swap individual components allows greater control of performance and power consumption. Modular designs are more predictable, easier to optimize and they can be rused later in similar applications. Although modularity is not critical, it is a highly desirable feature in any design.

A Delta Sigma modulator can be broken down into five functional blocks: Subtractor, Integrator, Comparator, A/D converter, feedback D/A converter, and the output register. This breakdown is illustrated in Figure 3.18. For a single bit architecture, the most critical sub-components are the Subtractor and Comparator, because they determine the system precision and the final ADC resolution. The integrator is the most resource hungry component, because it requires large passive components for noise attenuation. Since area is the most limiting factor, the integrator design must be considered first.

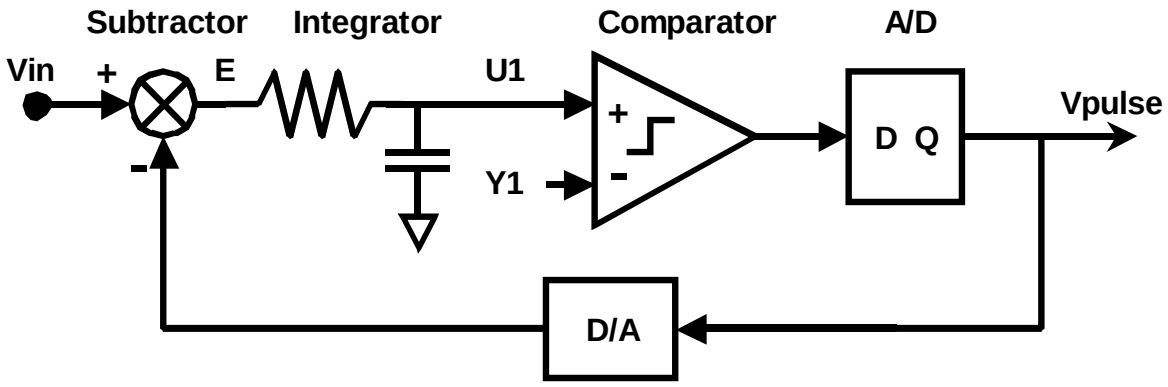

Figure 3.18 Delta Sigma Modulator Breakdown

The most basic integrator design in an RC filter as seen in Figure 3.18. This filter has a unity gain and can operate rail-to-rail. The problem for the rail-to-rail operation is that it requires a negative feedback to have a negative voltage. In addition, voltage mode operation is very sensitive to noise which puts great strain on the Subtractor circuit operating directly on the input signal.

3.5.2 Active Integration

Active integrators are popular because they provide an active gain and supply noise de-sensitivity by feedback. In addition since the amplification is performed differentially in current mode, the circuit can be designed to accomodate negative feedback without negative voltage. By performing feedback subtraction in current mode rail-to-rail input can be accommodated. An example of such an integrator is shown in Figure 3.19.

The combination of Vref and input signal Vin provides a bias for the BJT transistors. Without Q2 and Q4, this circuit is a comparator of Vref and Vin. Q4 serves as a fixed current offset to the system. Node X on Q2 can be connected to node A if the output is high, and in doing so, the current due to feedback is subtrcated from the current due to the input causing the voltage on node A to drop a fixed amount. If the output is low, node X is connected to node B. Then there is no subtraction performed, and nodes A and B are pulled down evenly. The output is differential across

A and B, therefore the comparator has no need for a separate reference voltage. The only external requirement for this circuit is Vref which serves to bias the integrator for optimum operation range. The capacitor C1 integrates the ouptut across nodes A and B, and the resistor R1 provides the means for crosstalk necessary for system stability.

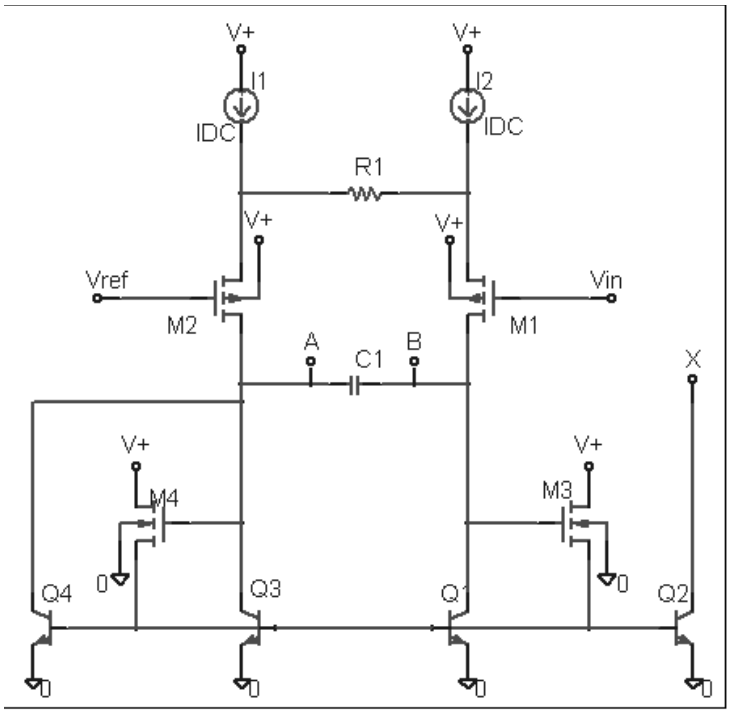

Figure 3.19 Differential Integrator for Delta Sigma Modulation

3.5.3 Switched Current Integration

Both active and passive integrators rely on the properties of the passive components to provide the necessary functionality. This presents a problem because on-chip resistors and capacitors are limited in size and tolerance, which makes integration costly. An alternative approach is to integrate the signal in discrete time.

The output of the Delta Sigma modulator is digital, so it is natural if the integration circuit operates at the same clock. If the modulation and integration are performed at the same rate, then the discrete circuits will not add any additional error. Furthermore, by sampling the input at regu-

lar intervals, the integrator can prevent the feedthrough of transient noise that bothers the continuous time integrators.

Figure 3.20 shows a discrete time integrator based on the trapezoidal rule. The circuit samples its input at a discrete time period T, and those samples can be used to approximate the curve and to approximate its integral by forming a trapezoid illustrated in Figure 3.20a. Equation 3.23 illustrates the integral approximation, and Equation 3.24 is the resulting transfer function.

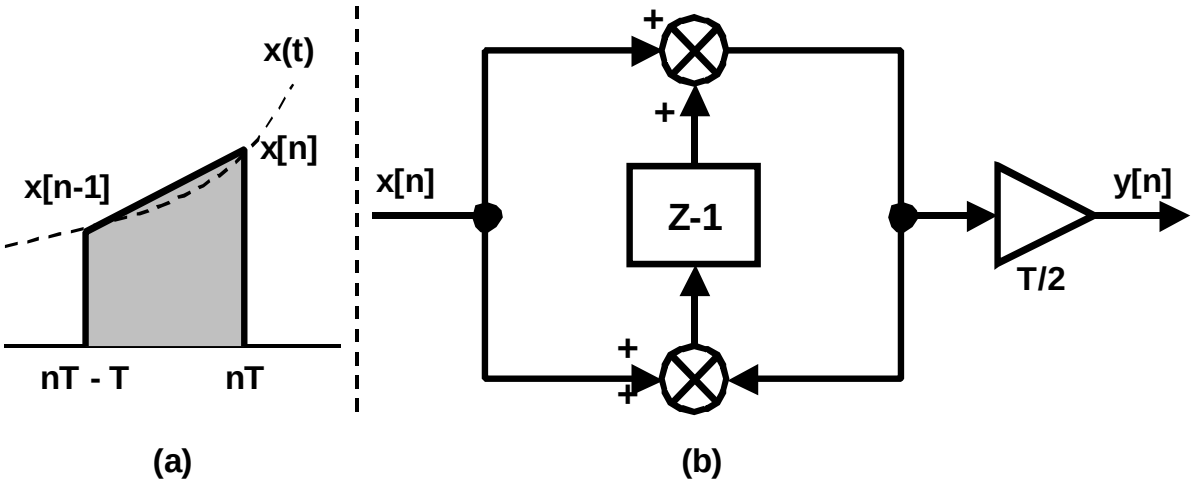

Figure 3.20 Discrete Time Integration

$$y[n] = y[n-1] + (x[n-1] + x[n]) \times \frac{T}{2} \qquad (3.23)$$

$$H(z) = \frac{T}{2} \times \frac{1 + z^{-1}}{1 - z^{-1}} \qquad (3.24)$$

An example of a discrete time integrator is illustrated in Figure 3.21. This is a current mode integrator that operates off a single power supply voltage. The subtraction in current mode is performed when S1 is on and S2 is off, and the final state is stored on C1.

$$Iout = Io - I(M2)\, z^{-1} \qquad (3.25)$$

$$I(M1) = Iout + Iin + Io \qquad (3.26)$$

When S2 is on, S1 is off, the integrated current value is stored in M2.

$$I(M2) = 2\,Io - I(M1)\,z^{-1} \qquad (3.27)$$

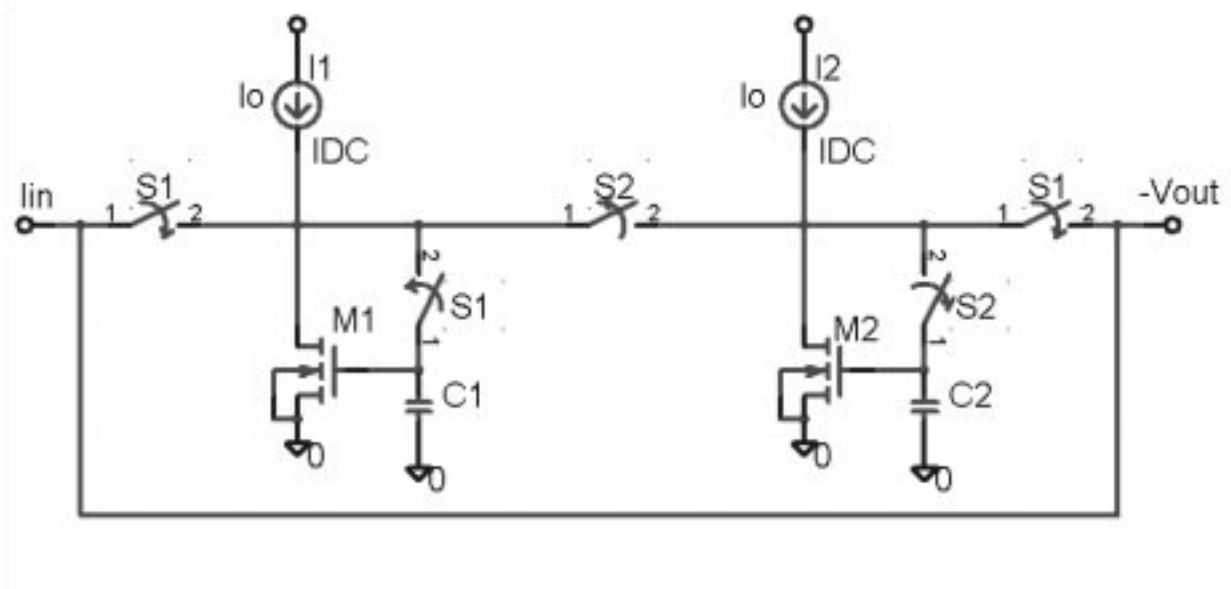

Figure 3.21 Current Mode Discrete Time Integrator

The capacitors and MOS gates provide the memory elements that store the current settings. the stage following this integrator must not draw any current from the feedback. Since the output is represented by the direction of the current, a simple CMOS inverter would perform the function of a comparator without drawing any current from its input.

Both the active and the current mode integrators draw static current. In addition current references are required, and this overhead consumes significant power. Circuits that operate in charge mode provide a low power alternative to circuits relying on current. Switched capacitor circuits operate in discrete time, and use charge as the medium for storing and processing information. [17][,[19],[23]. Figure 3.22 illustrates the principles behind switched capacitors.

For the RC circuit in Figure 3.22b, the current supplied to (C1) is:

$$Ieq = (Vin - Vout) / Req \qquad (3.28)$$

For the switched capacitor circuit in Figure 3.22b, the current into (C1) is equivalent to the transfer of charge during one clock cycle multiplied by the clock frequency:

$$Ieq = Fclk \times \Delta Q = Fclk \times C2 \times (Vin - Vout) \qquad (3.29)$$

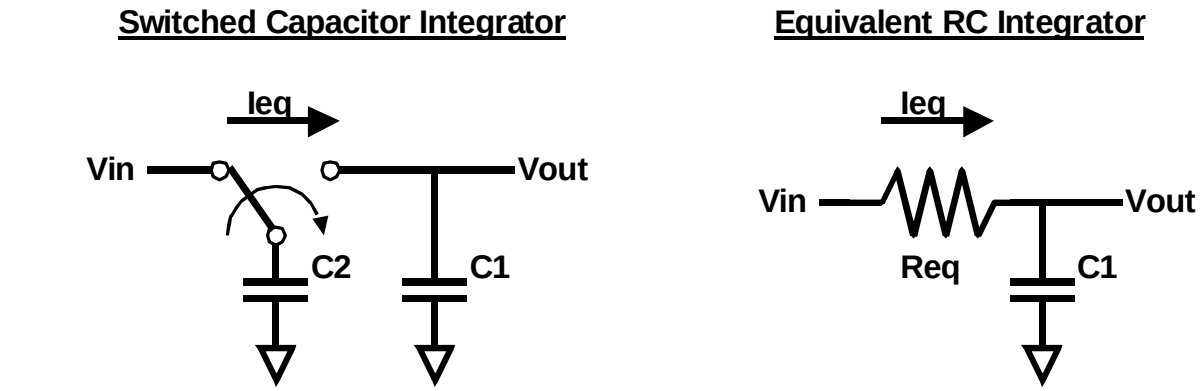

Figure 3.22 Switched Capacitor Technique

Equation 3.29 makes sense since the definition of current is charge transferred over time. Ieq can be made very small by using smaller capacitors at low frequencies. An added benefit is that on-chip capacitors can be matched much better than resistors, because they are less susceptible to process and temperature variations.

The switched technique can be expanded further to perform basic operations such as scaling and subtraction, it is called “flying capacitor” technique. If left undisturbed, a charged capacitor

retains its charge and its potential for prolonged periods of time. If the the voltage on one plate of the capacitor changes, the other plate changes by the same amount. By using different reference voltages for charge and discharge cycles, the signal can be linearly scaled. Figure 3.23 illustrates this phenomenon.

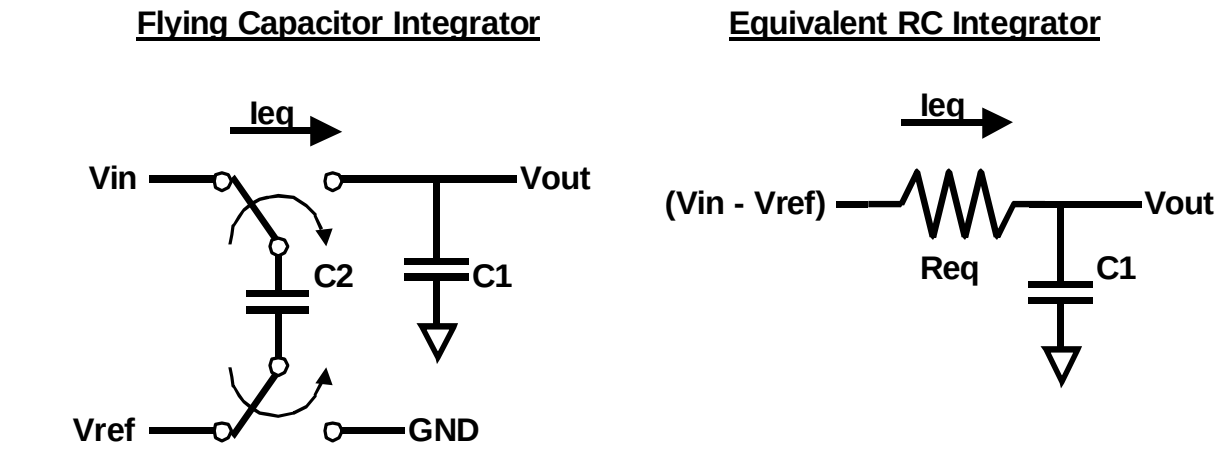

Figure 3.23 Flying Capacitor Technique

The principle behind the flying capacitor is the same as the switched capacitor in Figure 3.22 except that C2 is charged up to a deliberately smaller voltage. The flying capacitor circuit in Figure 3.23 is scaled with respect to Vref; the resulting current is derived below:

$$Qin = (Vin - Vref) \times C2 \;\; ; \;\; Qout = Vout \times C2 \qquad (3.30)$$

$$Ieq = \frac{\Delta Q}{\Delta T} = Fclk \times (Qout - Qin) = Fclk \times (Vout - Vin + Vref) \times C2 \qquad (3.31)$$

The circuit in Figure 3.23 can be used to perform several functions in addition to integration such as voltage scaling and subtraction. Figure 3.24 shows an adaptation of the flying capacitor technique to perform three functions in one circuit: subtraction, scaling and integration.

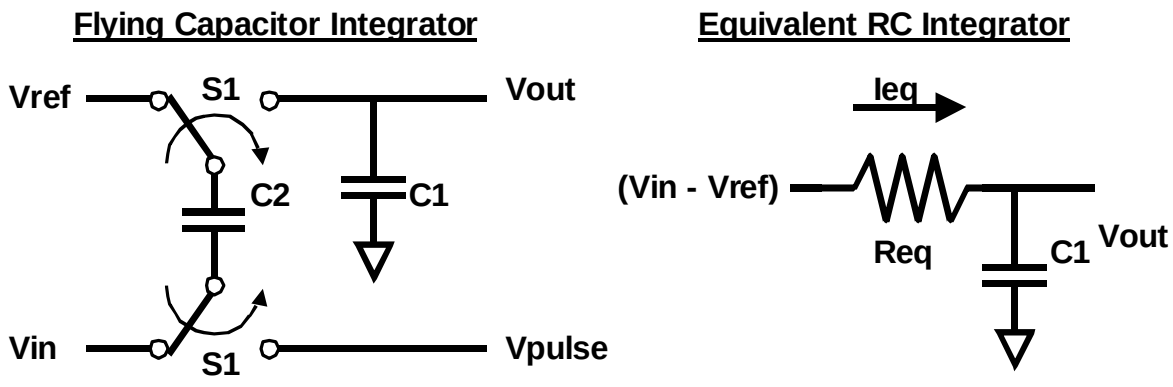

Figure 3.24 Flying Capacitor Subtractor - Integrator

The feedback signal, Vpulse is a digital waveform that runs at the clock frequency, the same frequency as S1. The resulting current that flows into C1 is:

$$Qin = (Vref - Vin) \times C2 \;\; ; \;\; Qout = (Vout - Vpulse) \times C2 \qquad (3.32)$$

$$Ieq = Fclk \times (Qout - Qin) = Fclk \times (Vout - Vref + Vin - Vpulse) \times C2 \qquad (3.33)$$

Equation 3.33 shows that the final current into C1 is defined by four voltages. For normal operation, the average of the output would be: $|Vout| = Vref$. In this case, the instantaneous voltage of the integrator and at the input of the comparator is:

$$Vout - Vin = \int (Vin - Vpulse)dt \qquad (3.34)$$

The reference voltage Vref is selected arbitrarily for the integrator implementation. It is a constant signal used to offset the output and has no bearing on the integration functionality. For these reasons, the reference voltage is not constrained by physical requirements, nor is capacitor matching an issue. Essentially, Vref can be selected such that it improves the operation of the comparator that follows this circuit.

3.6 Comparator Design

The flying capacitor technique is a good design choice, because it takes care of three out of five Delta Sigma functions, the feedback scaling, the subtractor, and the integrator. The remaining task is finding a fitting comparator architecture.

The most popular choice for a comparator architecture is a differential comparator. Figure 3.25 shows a schematic of a basic differential comparator. [19],[21]

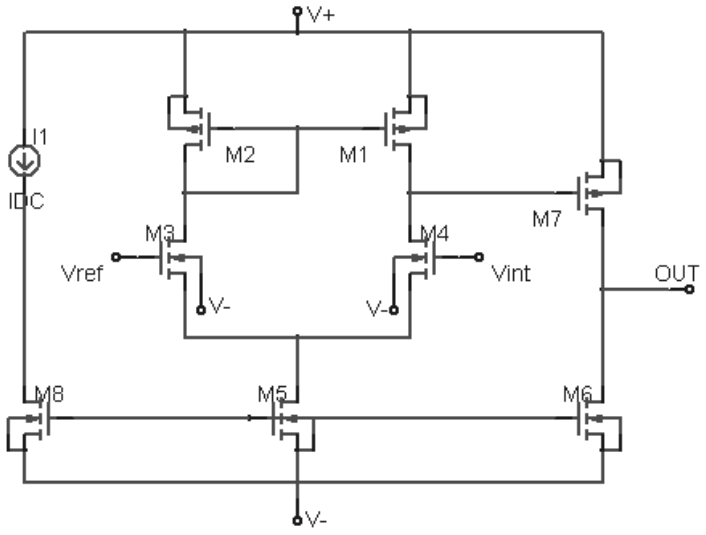

Figure 3.25 Differential Comparator

The reference voltage, Vref, and the integrated signal, Vint, are applied to their respective branches on the differential stage. When the two voltages are unequal, the impedance of the differential branches is mismatched, and the output voltage reflects that mismatch. The output of the differential stage is applied to the gate of M7, the voltage gain stage that serves to amplify the detected difference. The accuracy of this comparator is determined by how well the transistors M1, M2 and M3, M4 are matched.

The basic differential comparator is sufficient for certain applications, but several drawbacks become apparent for high performance devices. The comparator requires a static current draw, especially to achieve large gains. PMOS transistors saturate at inputs close to V-, and the compar-

ator saturates at low voltages. Accurate current references are required to drive the comparator biases and to provide sufficient power supply rejection, which is in addition to the comparator circuitry. Lastly, the comparator accuracy is highly dependent on transistor matching, which adds a sensitivity to process variations.

The differential architecture is a proven implementation, and over time many methods have been developed to improve its performance. Improved circuits, however, tend to become bulky and power hungry. Non-differential comparators seem to offer a better alternative.

A non-differential inverter can be composed of a single gain stage with a pull up and a pull down network. At the very simplest level, this stage has the same structure as a digital inverter, where the PMOS stores the pull up current and the NMOS stores the pull down current.

An inverter has a fixed voltage at which the output state changes, a switching point that is determined by the NMOS and the PMOS ratios. The output of an inverter depends on whether the input is above or below the swithing point, thus it acts as a voltage comparator. This is not immediately useful, however, if Vref is made equal to the switching point of an inverter, that inverter can be used as comparator. This implementation is illustrated in Figure 3.26.

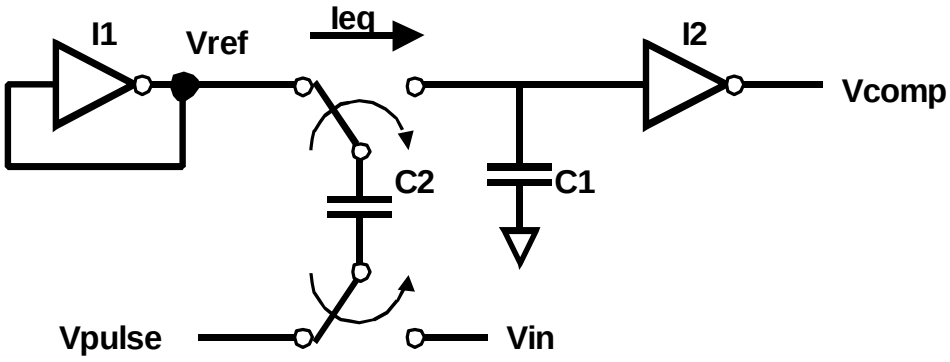

Figure 3.26 Setup for a Non-Differential Self-Referenced Comparator

The inverter, I1 is biased at its equilibrium point, which is also its switching point. Using this equilibrium point as a reference voltage, centers the output of the integrator at the switching point

of I2, such that even a small deviation in Vint will force the ouput to a discrete state. The accuracy of the comparator is thus dependent on matching I1 and I2.

This method has several merits. The transistors in the inverter stage I2 do not require to be matched for current, although it is assumed that I1 and I2 are well matched. The transistor count for this implementation is as few as 4 transistors within the two inverters, the remaining hardware is already provided by the integrator circuitry. This offers efficiency and symplicity, two imprortant components for low power systems.

The immediate drawbacks are the static current draw in the I1 inverter, and the fact that single stage circuits are more sensitive to power supply noise. Both of these problems can be addressed by creating starved-current inverters and selecting the integrator bandwidth to filter the noise.

Still, an inverter is not a comparator in its own right, and a voltage divider may not be an optimal voltage reference. An inverter would perform better as a comparator if the inverter switching level was set independently of the reference voltage. Floating gate techniques can be used to accomplish that. In floating gate devices, a capacitive memory element is used to store critical information such as a bias voltage, an offset or a reference. A system with critical requirements can be tuned without altering device properties. [7],[8]

The principle behind this technique is that an isolated MOS gate can store a charge for a long period of time, particulary if it is completely isolated by the insulating layers. Digital circuits such as PROM and Flash are based on this property, as well as some neural and adaptive architectures. With shrinking technology it becomes necessary to use it in analog design as well. Figure 3.27 shows a basic floating gate inverter.

Capacitors C1 and C2 are preset with specific voltages such that the gate voltages are offset. This can be done out of power considerations; with a higher Vd’ and lower Vd, the inverter will draw much less current, particularly in analog applications. If the switching threshold of Vin is different from the inverter switching point, the capacitors can provide the offset between the input and the gate voltages to compensate.

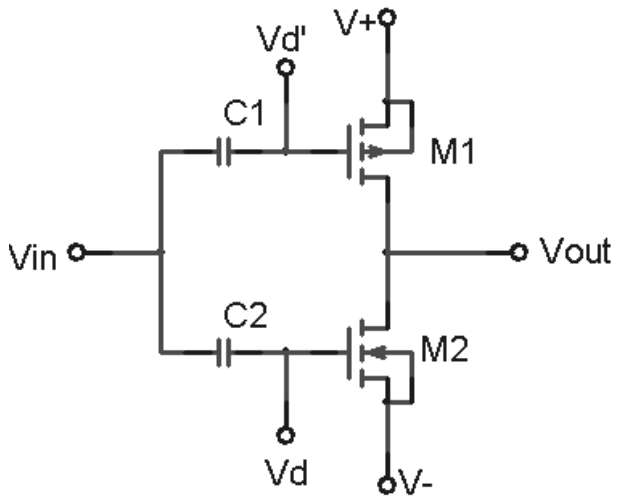

Figure 3.27 Floating Gate Inverter

The tricky part in using floating gate circuits is presetting the correct charge on the gates, particularly when the offset is not known prior to application. Charge shifting techniques and UV trimming are impractical for small circuits. For the purposes of Delta Sigma modulator, the gate charge can be preset through and ohmic network. Although gate charge can deteriorate over time, it can be refreshed and dynamically altered to adapt to changes in the environement. Figure 3.28 shows a CMOS implementation of a pseudo-floating gate comparator.

In Figure 3.28, S1 is the system clock, and S2 is the refresh signal. Just like the reference circuit in Figure 3.26, the switching threshold, Vsw of I2 is determined by shorting its input and output. This operation is performed during the refresh cycle, and the potential difference between the reference and the inverter thershold is stored in C3. This operation is called autozeroing. During normal operation, S2 switches are in the illustrated position, and the gates in I2 are floating. The circuit equations break down like this:

$$V(C3) = Vsw - Vref \qquad (3.35)$$

$$|V(C1)| = Vsw - V(C3) = Vref + |Vin - Vpulse| \qquad (3.36)$$

One must note that matching is no longer a problem since the switching voltage is measured directly from I2.

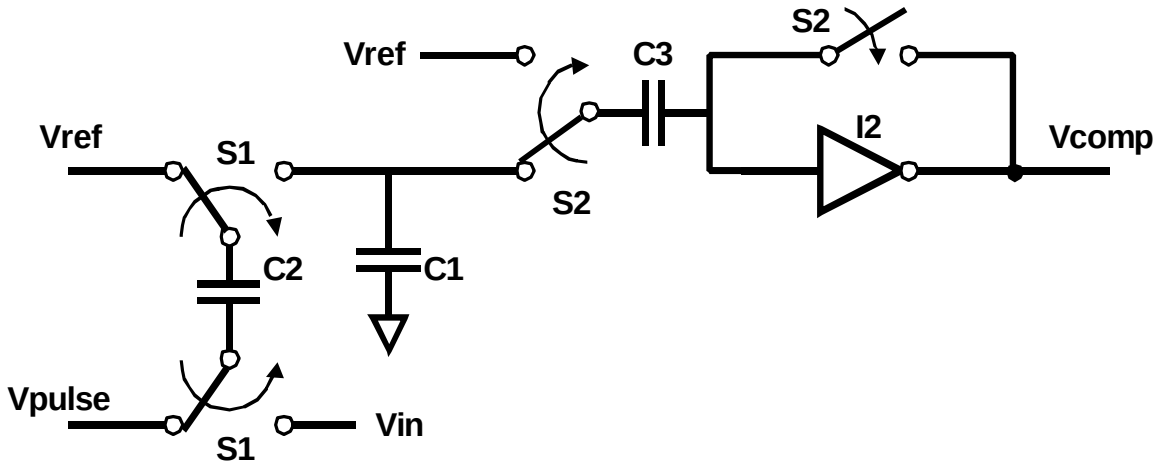

Figure 3.28 Pseudo-Floating Gate Comparator

The floating gate circuit provides an adaptive alternative to component matching. It is not as simple as the previous circuit, but it can provide accurate results even under poor design cndi-tions. Since it is a discrete time circuit, it can also be turned off when not required.

3.7 Voltage Reference

When circuit conditions are poor, an accurate voltage reference becomes critical to circuit performance. The same conditions make the creation of a stable voltage reference circuit much harder. A band-gap reference circuit can be designed with a high degree of rejection for power supply and temperature related variations.

The circuit in Figure 3.29 is a CMOS implementation of a band-gap circuit for technologies where BJT transistors are poorly characterized. It is particularly suitable for compact and low power designs.

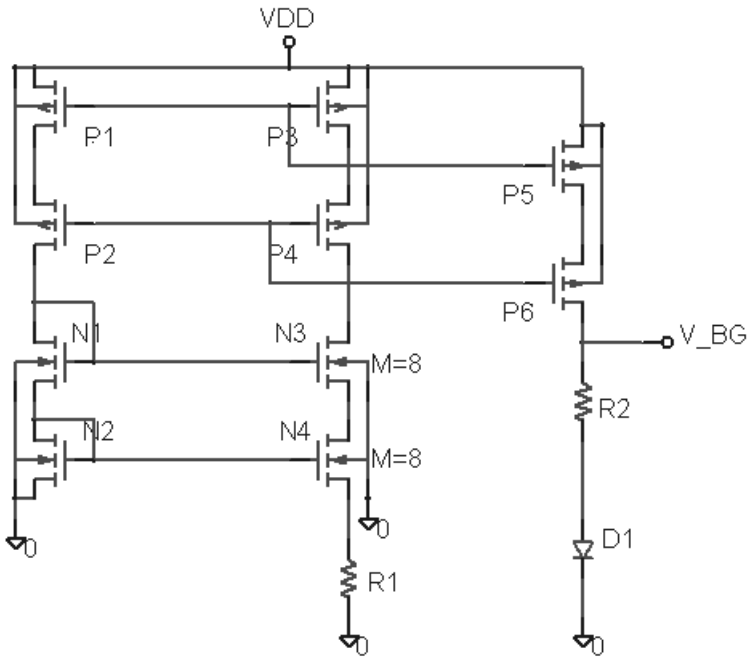

Figure 3.29 Band-Gap Reference Circuit

This circuit has several distinguishing characteristics. The first stage, represented by the MOS transistors, is a modified Beta Multiplier circuit with dual feedback for higher impedance and power supply rejection. The output of this stage has a positive temperature coefficient. The second stage is the diode D1, where the voltage across the diode results from the current through it with relative independence from the power supply. The temperature coefficient of the second stage is negative, and the resistor, R2 is selected such that the temperature coefficients of the two stages cancel out. When the stages are matched, the output V_BG is virtually immune to temperature effects.

3.8 Low Power Latch

Although the largest portion of the power consumption for the switched capacitor modulation is due to the static referencing and switched current, the digital circuits involved are still significant. It is in the principle of Delta Sigma modulation that the output is switched regularly and frequently, which translates into dynamic power consumption.

The circuit in Figure 3.30 is suitable for high frequency switching. It is a dynamic latch that minimizes the switching power consumption by using only one clock signal and using only two switches to accomplish its function. [9]

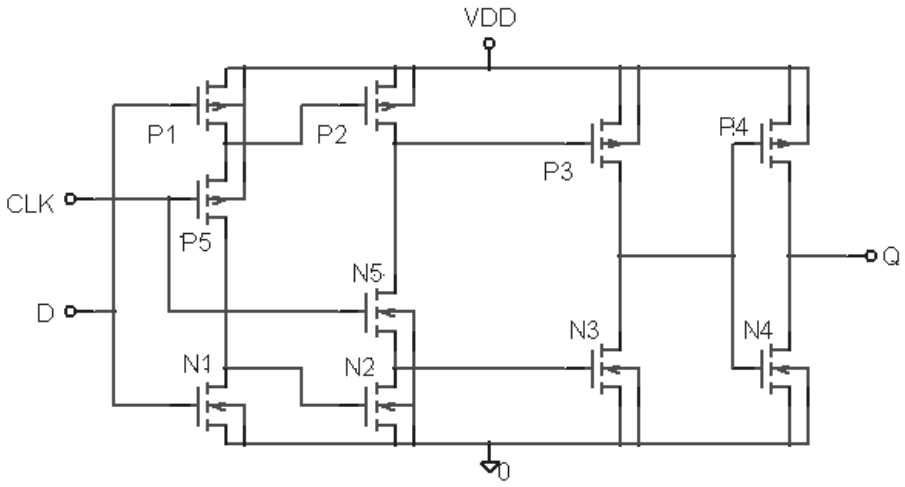

Figure 3.30 Low Power Latch

Aside for the memory function, the above latch provides additional gain to the output of the comparator, as seen in Figure 3.30, there are four additional stages in the latch, each forcing the output to its digital form. Once the output is defined as either a high or a low, further gain is no longer necessary, but having the additional gain helps to improve the system resolution and ensures that the digital state is always defined at the output.

3.9 Summary

The hybrid of switched and floating capacitance systems is the most compact and power efficient system proposed so far. It is attractive to low power design for two reasons: The minimal number of components, and the use of charge recycling. Due attention is given to the device precision by using the input signal in its original voltage form, and by optimizing the comparator for accuracy.

After such efforts to achieve comparator accuracy, it may be tempting to ask why it is necessary since the feedback loop desensitizes the system to component deficiencies. The ojective of

this design is to achive high precision output with minimal resources. The precision of Delta Sigma is dependent on the high gain of the forward loop, and that in turn is limited by the precision of the comparator. A good comparator design can improve system performance at the smallest cost.

We covered the basic components of a Delta Sigma modulator in this chapter. Several attractive designs have been derived based on available references and integration of new techniques. The following step is to realize this design through complete transistor-level implementation. In chapter 4 we present the implementation of circuits described in this chapter.

CHAPTER 4: Delta Sigma ADC Implementation

This chapter describes implementation of a delta sigma modulator described in the previous chapter. Key topics cover the overview of the proposed architectures, implementation of major components, implementation of closed loop systems and the layout considerations.

4.1 Project Overview

The goal of this research was to develop a low power architecture for precise analog-to-digital conversion targeting an environment with limited resources for analog design. Such a system targets the large maket of digital integrated circuits that has a renewed pressure to provide precision analog interfacing. A low power Delta Sigma modulator implemented inside a digital silicon is a low cost low profile solution that is easily portable between technologies.

All designs presented in this thesis are impelementated in a fixed silicon underlayer whose primary use is for digital gate-array circuits. This means that the transistor sizes are fixed and not necessarily optimized. The only analog resources avalable are for use in Electro-Static Discharge (ESD) devices and I/O buffering, and those are limited to scarse poly-silicon resistors, diodes and some large MOSFETs.

As a result of strict constraints many devices evolved out of improvization, such as interleaved capacitors, use of gate polysilicon for resistance, use of ESD diodes for band-gap reference, and use of floating reference schemes and feedback schemes to offset device mismatch. The ability to make such use of available resources has been critical in all stages of the design process, and it is the cornerstone to designing analog devices on a digital silicon underlayer.

4.2 Proposed Delta Sigma Architecture

The proposed delta sigma architecture is illustrated in Figure 4.1. It is important to note, that a single loop model does not imply that the Delta Sigma modulator is a first order system. The order of the closed loop system is determined by the order of the open loop components; in this

case it is determined by the filter implementation. A first order filter corresponds to a first order system. Increasing the order of the filter will increase the system order accordingly.

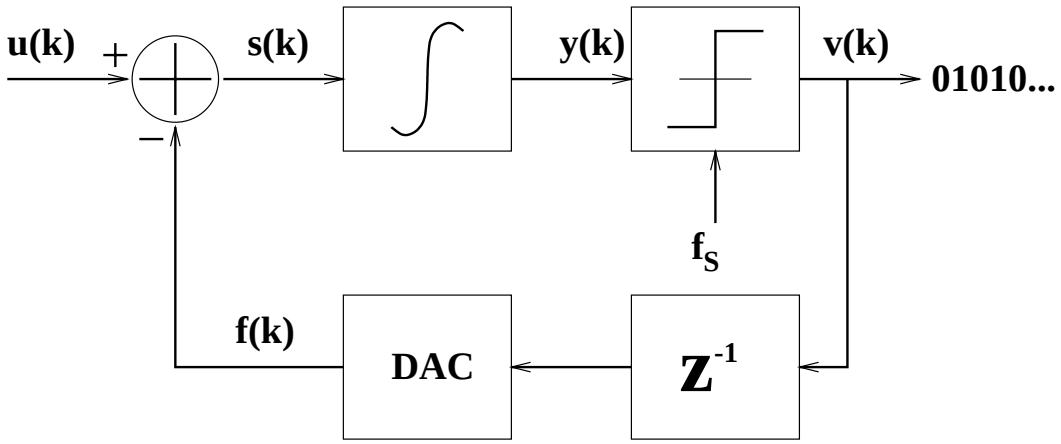

Figure 4.1 Proposed Delta Sigma Modulator

4.3 Implementation of Major Components

This section addresses the implementation of the delta sigma modulator components in Atmel 0.35 um technology. The design was verified primarily through simulation.

4.3.1 Band Gap Implementation

The band gap reference circuit is designed to provide an accurate voltage reference with minimal variations due to changes in Vdd and Temperature. The design in Figure 4.2 shows a schematic designed specifically for a CMOS process. Two current reference stages with opposite temperature sensitivities are used to create a single temperature tolerant voltage reference. The first reference stage is an all MOS circuit; it uses a cascode current mirror to provide resistance to power supply variations. The second stage is a forward biased diode. The R12 resistor sets the relative gain of each stage to a point where their temperature sensitivities cancel out, and the output voltage becomes resistant to temperature effects.

The temperature sensitivity has been optimized such that for a temperature sweep from -25^{o}C to 125^{o}C, the reference voltage only varies by 6mV. The temperature sensitivity curve at 3.3V on the power supply is shown in Figure 4.3. The sensitivity to power supply voltage, Vdd is illustrated in Figure 4.4, with measurement taken with Vdd = 3.0V, 3.33V, 3.67V and 4.0V. The curvature in the voltage vs. temperature plot is a recognizable trait of the band-gap reference circuits caused by the non-linear effects of temperature on each of the band-gap stages. The flat portion of the curve is optimally set at the typical operation temperature, 27^{o}C.

Figure 4.5 shows the frequency response of the band gap circuit to the noise on the power supply. It is critical to have a stable reference voltage even if the power supply is noisy. High frequencies get damped by the capacitance of the power net and the bypass capacitors, but the band-gap has to suppress the lower frequency noise. Figure 4.5 shows that the band-gap circuit suppresses the power supply noise by 53dB for frequencies up to 1MHz. At 10MHz noise on the power supply the suppression falls to 40 dB. This means that the bypass network on the power supply must minimize the noise above 10MHz in order to keep a steady reference.

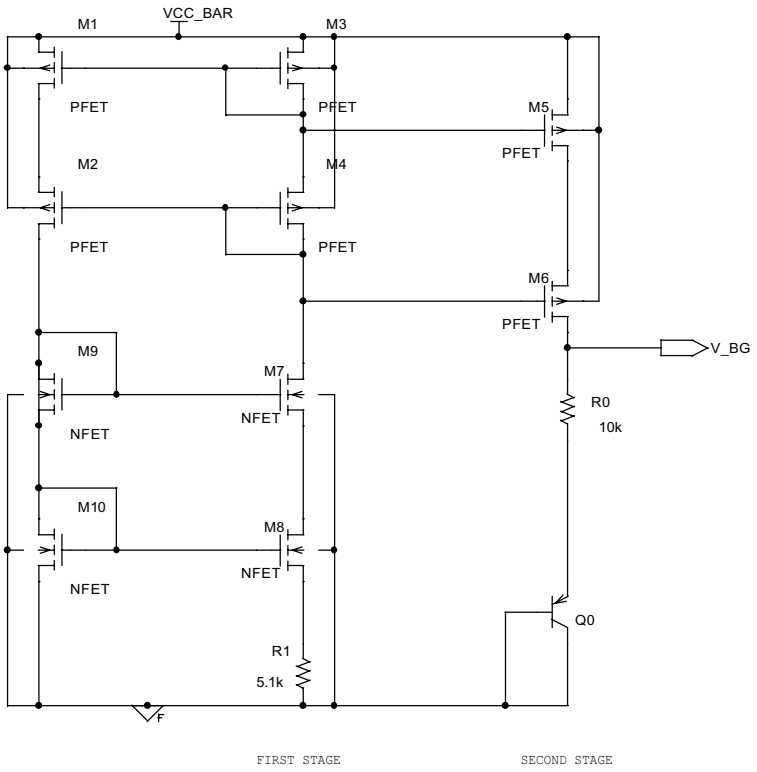

Figure 4.2 Band Gap Voltage Reference Schematic

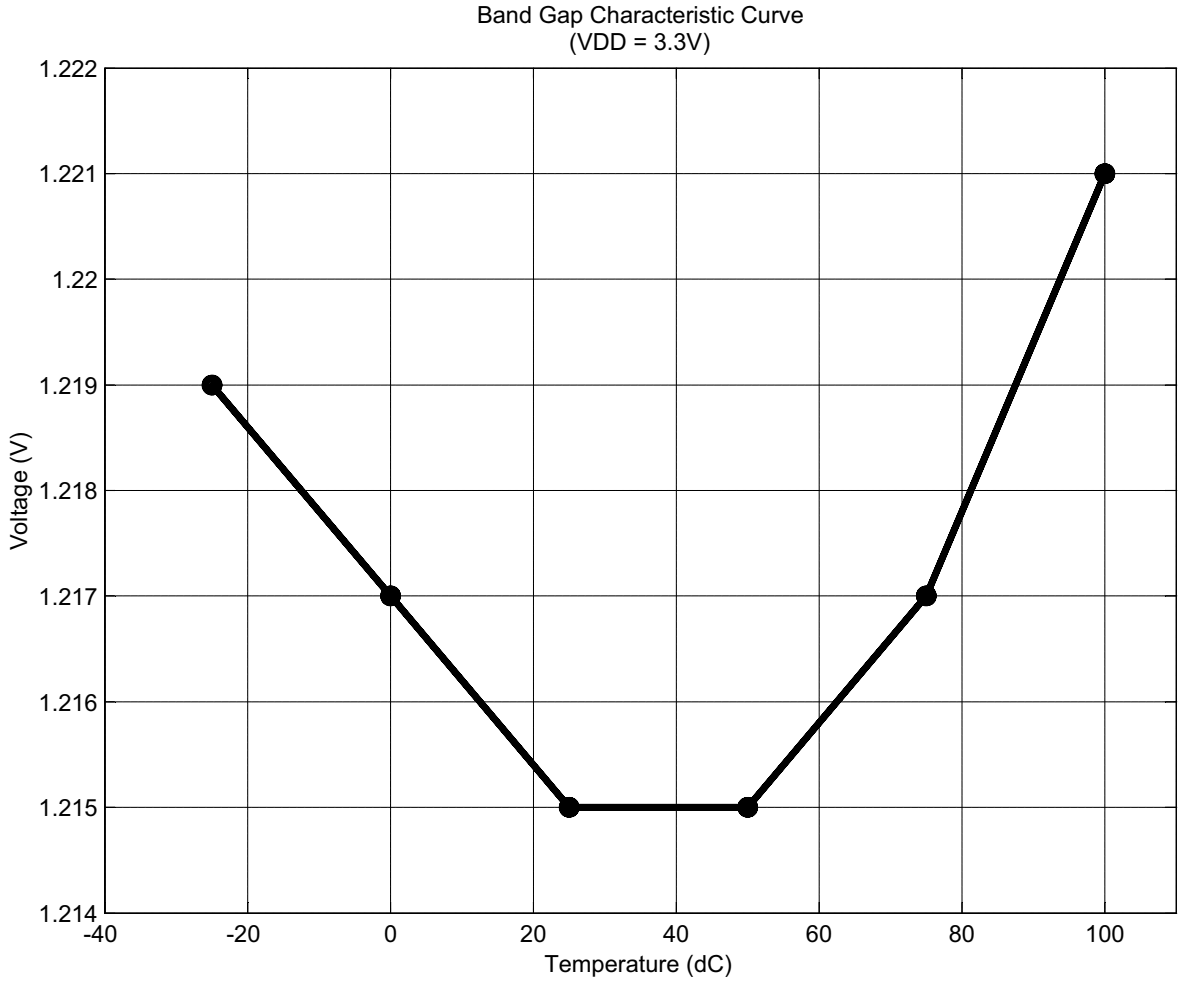

Figure 4.3 Temperature Sensitivity Curve for the Band Gap Voltage Reference

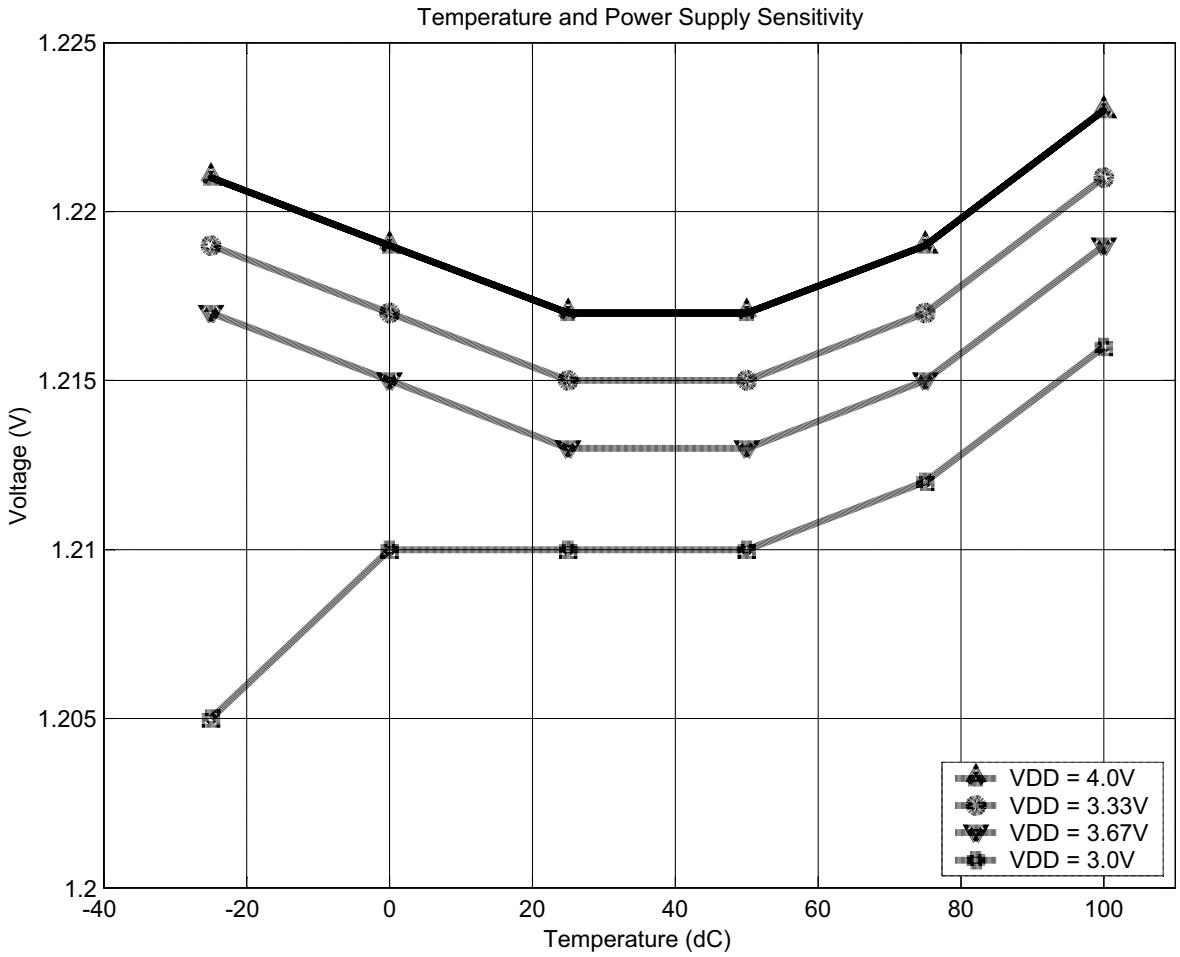

Figure 4.4 Band Gap Reference Sensitivity to Supply Voltage

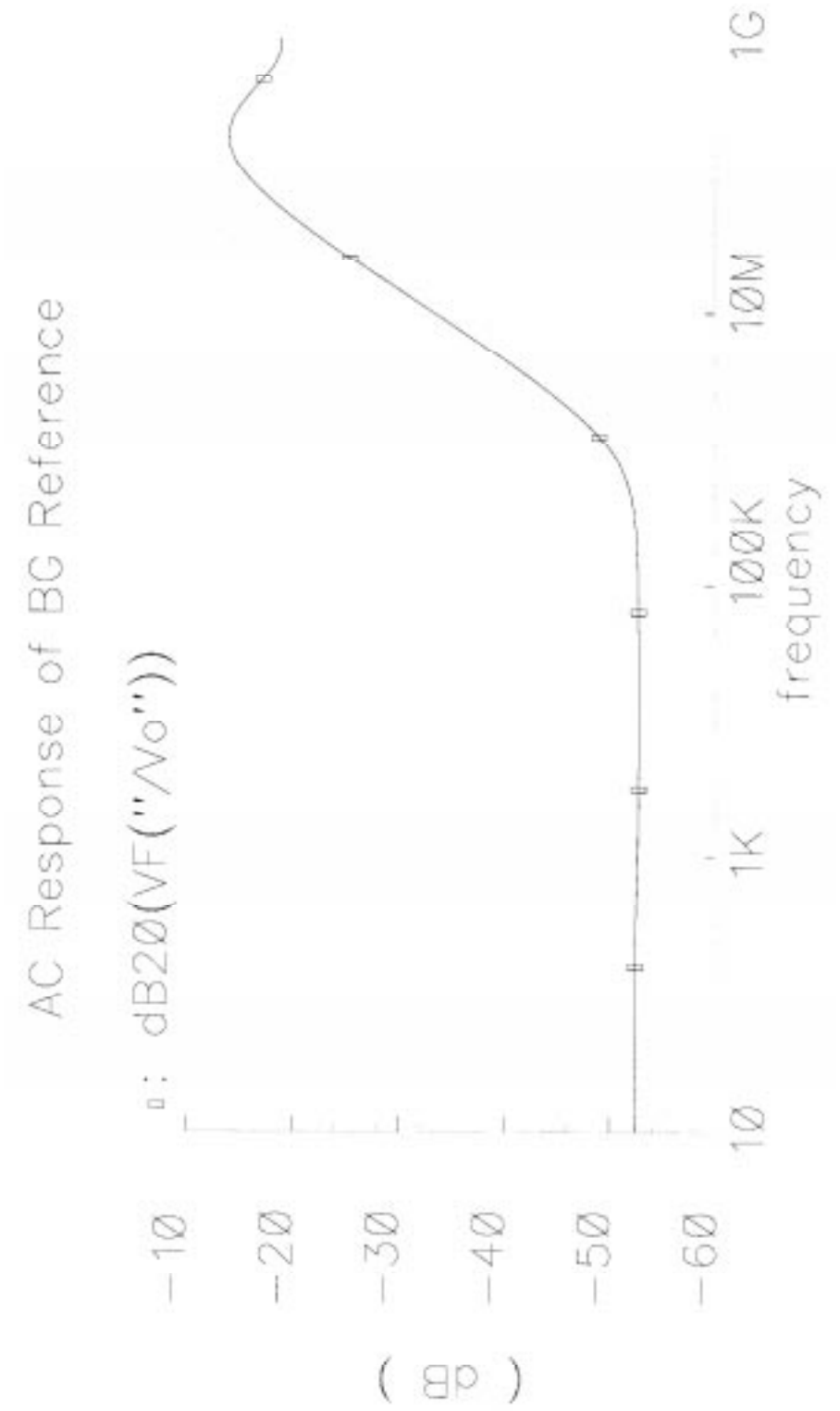

Figure 4.5 Band Gap Suppression of Power Supply Noise

4.3.2 Low Power Latch

The low power latch in Figure 4.6 is implemented as a dynamic memory circuit with a single phase clock. This device switches fewer devices per clock period than a traditional static latch, hence the power savings.

Further power savings are possible by resizing the ouput transistors, however the target process uses a fixed underlayer, so arbitrary transistor sizing is not an option. The transistors in Figure 4.6 have a gate length of 0.35 um, and matched gains between PMOS and NMOS devices to allow sharp edges and a mid-voltage transition point.

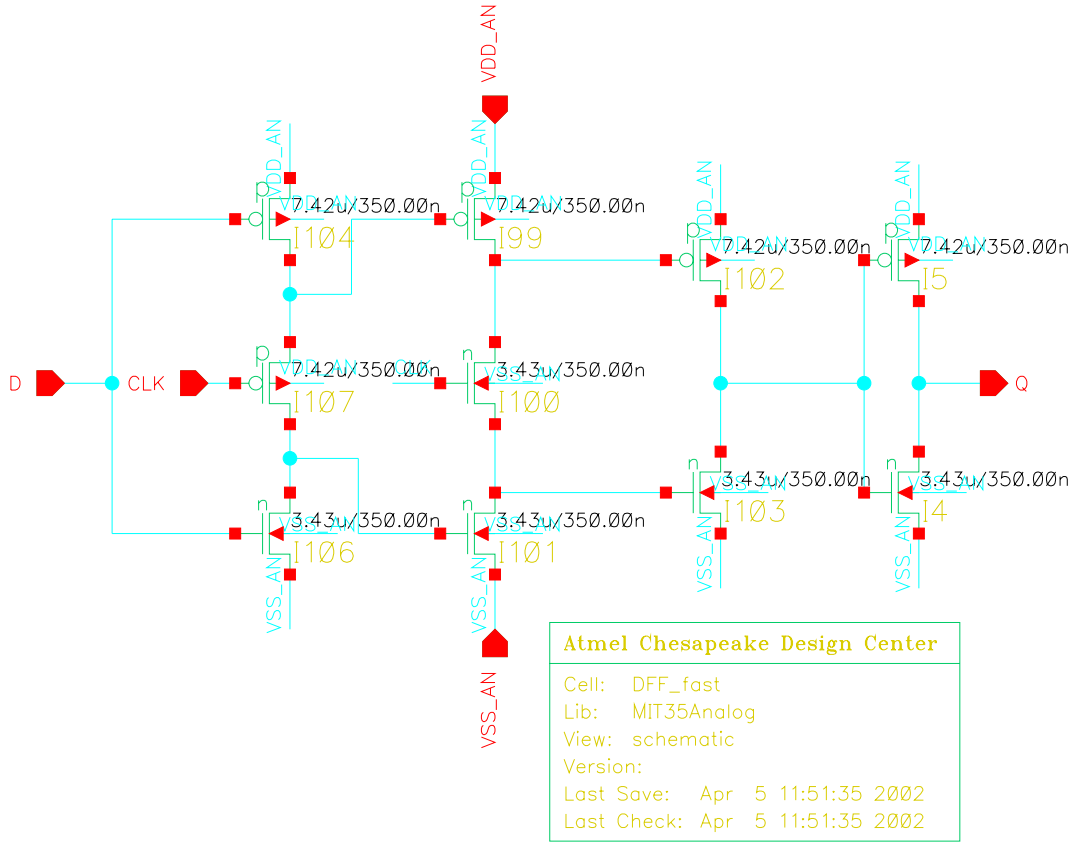

Figure 4.6 Low Power Latch

4.3.3 Comparator Implementation

The comparator is an enhanced digital buffer which features starved-current inverter stages for low power operation and a plain inverter stage for gain. The comparator schematic is shown in Figure 4.7. Although fewer stages would suffice, starved current stages are added for better matching between stages and to prevent large dc currents during operation.

The comparator characteristic curve is shown in Figure 4.8. The reference voltage of the comparator is fixed at 1.3 V; when the input is below the reference, the output is pulled to 0V, alternately the output is pulled to 3.3 V. The gain of the comparator is 285,000, determined using points A and B on the curve. This means that the difference between the input and the reference must be 4 uV or larger in order for the output to reach a known state. This is sufficient since even a 12-bit ADC has a resolution of only 4096, with a step of 900 uV.

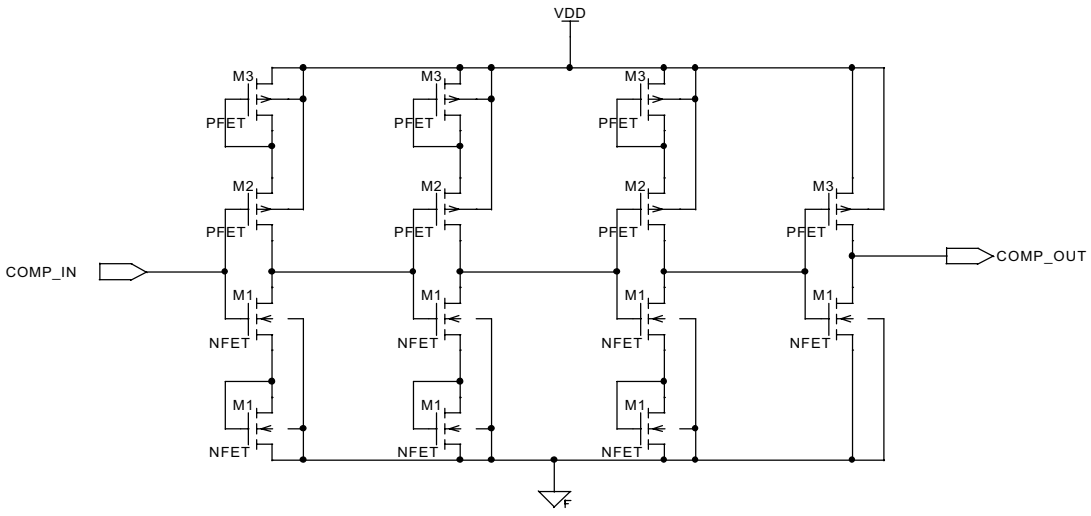

Figure 4.7 Comparator Schematic

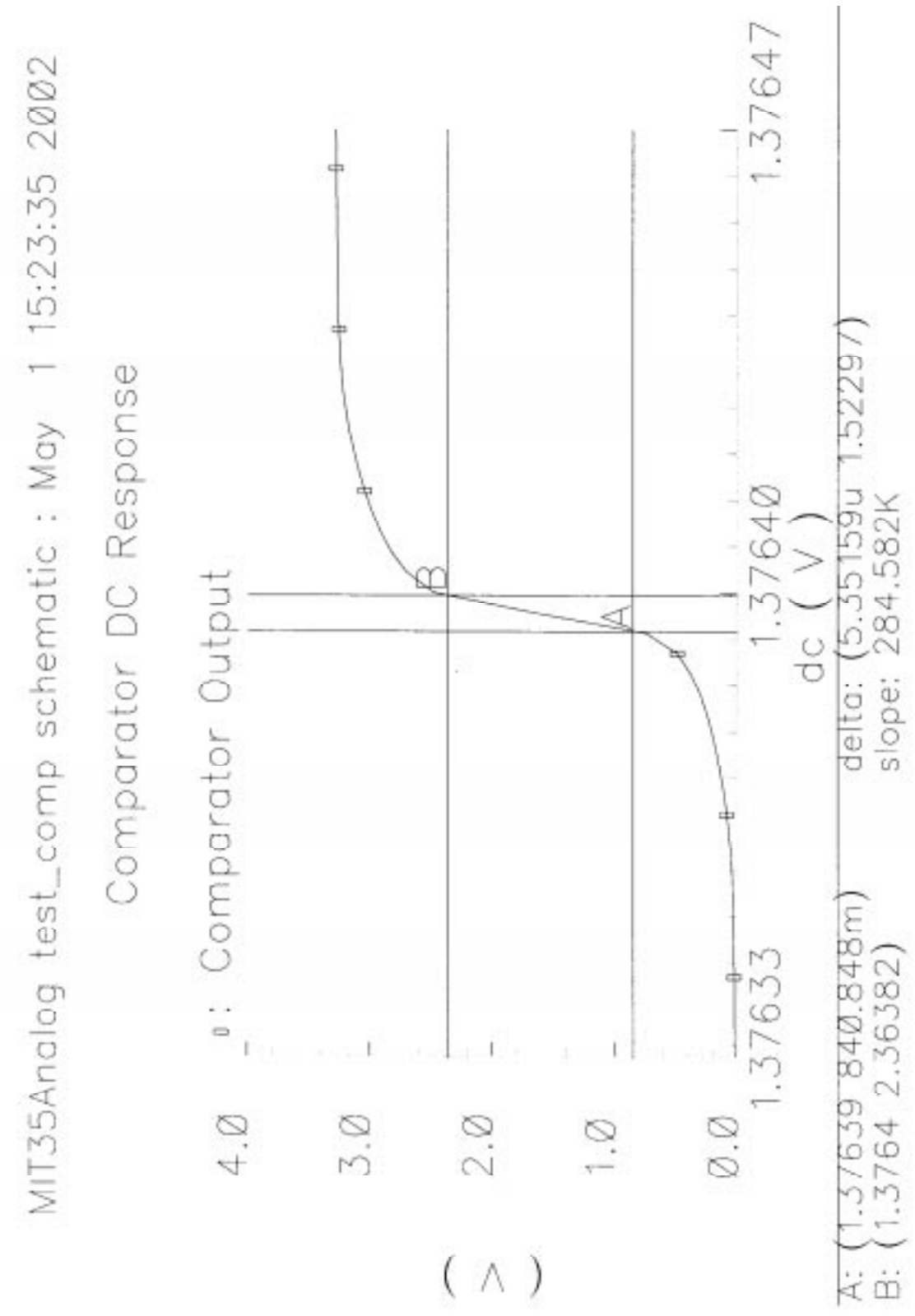

Figure 4.8 Comparator Characteristic Curve

The starved current inverters require an external bias. Figure 4.9 shows a setup that provides a low current bias to the comparator stages, and at the same time pulls the switching point toward VDD/2 by forcing equivalent current on pull-up and pull-down stages. This improves integration within the Delta Sigma modulator and minimizes the comparator offset. The mirrored current in Figure 4.9 isprovided by the diode biasing of M6 and M10 or by connecting the MED signal in the left figure to a Band Gap reference signal which provides additional noise suppression.

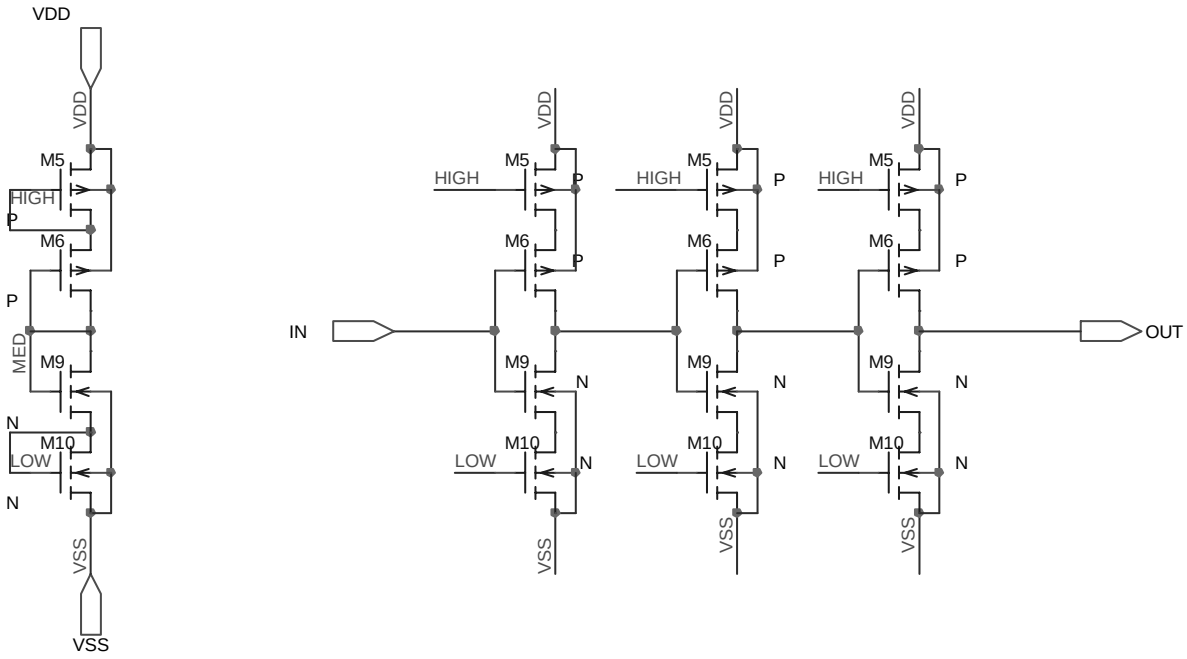

Figure 4.9 Biasing Setup for the Comparator Stages

4.3.4 Sizing of Switched Capacitors for Subtractor and Comparator.

The main constraint for the switched capacitors is the charge injection. Details of charge injection are discussed in the Appendix. Large capacitors are less affected by charge injection, but require a much larger silicon area. It is important to determine the minimum capacitor size that sufficiently suppresses the effects of charge injection. The capacitor size determinations for the 0.35 um technology are shown below.

For a channel length of 0.35 um, the gate capacitance has the following distribution:

$$STI \approx 0.05 \frac{fF}{\mu m} \tag{4.1}$$

The total combined width, W, of a CMOS switch is taken for a worst case value:

$$W \approx 7\mu m + 3\mu m = 10\mu m \tag{4.2}$$

The resulting channel capacitance is:

$$C_{channel} = 10\mu m \cdot 0.05 \frac{fF}{\mu m} = 0.5fF \tag{4.3}$$

Assuming that channel charge escapes evenly through source and drain:

$$C_{injection} = 0.5 \cdot C_{channel} = 0.25fF \tag{4.4}$$

The target voltage sensitivity to chare injection is determined with respect to the voltage range:

$$\Delta V \leq 0.001 \cdot \frac{V}{V_{VDD}} \tag{4.5}$$

Given the above requirements, the switched capacitance, Csw is defined:

$$Csw \geq \frac{0.25fF}{0.001} = 250fF \tag{4.6}$$

The above method is not intended for precision, but it ensures that sufficient suppression is applied to switching noise. The capacitance of 250 fF provides sufficient absorption of the injected charge. The final effects of the switching noise are small and can be compensated in the feedback loop.

It should be noted that the provided capacitance distribution data is conservatively rounded in order not to disclose information which may be proprietary or confidential.

4.3.5 Sizing of Filter Capacitance

Having determined the switched capacitance, the remaining filter properties can be calculated. For calculation purposes, the switched capacitor is approximated by the equivalent resistance as shown in Figure 4.10. The filter capacitance calculations are shown below.

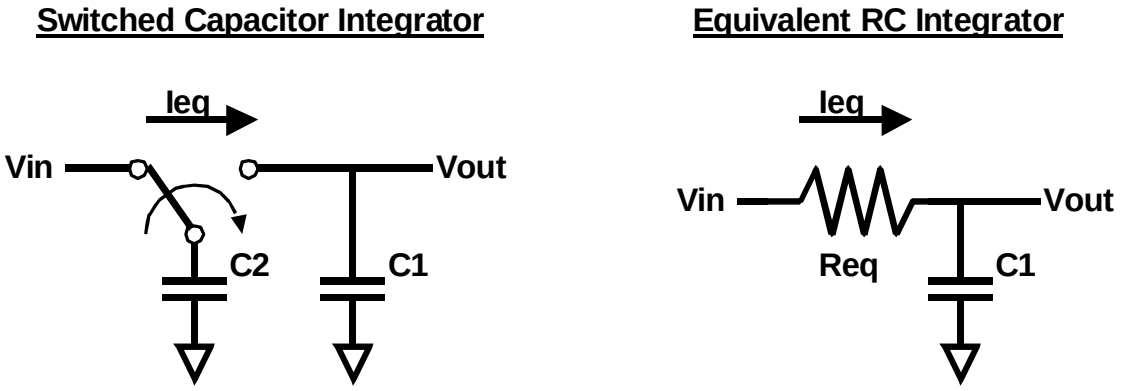

Figure 4.10 Switched Capacitor Equivalence

The initial variables are defined by the nature of the Delta Sigma system. The clock frequency is picked conservatively as the one that can decimate to 5 kHz at a 10 bit accuracy.

$$Fclk \geq 5kHz \cdot 2^{10} = 5.12MHz \qquad (4.7)$$

$$Fclk = 6MHz \text{ (standard crystal value)} \qquad (4.8)$$

The minimum required signal bandwidth is selected at 100 kHz, and this specifies the corner frequency for the filter, Fc.

$$Fc \geq 100KHz \tag{4.9}$$

The equivalent resistance can be determined from the clock frequency and switched capacitance, as shown in Figure 4.10.

$$Req = (Fclk \cdot Csw)^{-1} = 670k\Omega \tag{4.10}$$

The filter capacitor, C1 is a function of the corner frequency and the filter resistance.

$$C1 = (Fc \cdot Req)^{-1} = 15pF \tag{4.11}$$

A capacitor larger than 10 pF is not practical. Several values are calculated for different corner frequencies:

$$C1 = 15pF \text{ at } Fc = 100kHz \tag{4.12}$$

$$C1 = 8pF \text{ at } Fc = 187kHz \tag{4.13}$$

$$C1 = 4pF \text{ at } Fc = 373kHz \tag{4.14}$$

$$C1 = 2pF \text{ at } Fc = 746kHz \tag{4.15}$$

In order to stay within the 10 pF limit, an 8 pF capacitor is used for a first order filter. Two siwtched capacitor filters in series are combined to make a second order filter. In that case, two 4 pF capacitors must be used. A 2pF capacitor saves space, but larger loop filters offer better noise suppression.

4.4 Closed Loop Delta Sigma Modulators

We ahve implemented three different modulators described below. The simulation results are reported in Chapter 5. The target resolution of the three modulators is 10 bits, and some architectures fall short of the goal as reported in Chapter 5.

4.4.1 First Order System

Having defined the basic building blocks, a first order system can be built. Figure 4.11 illustrates a first order self-referenced Delta Sigma modulator. The principle behind this system is that the reference signal, MED is also the switching pont of the first stage of the comparator, thus the ouput of the ingegrator needs no further scaling.

This system offers the lowest possible power consumption because it uses the minimum number of components to make it functional, and minimizes the total switching power. The comparator stages are starved current inverters matched to the current in the reference circuit. The switches on the subtractor are complimentary in order to pass the analog signals that are close to both power rails. These precautions are not necessary for the integrating capacitor because the loop will correct for any linear offsets.

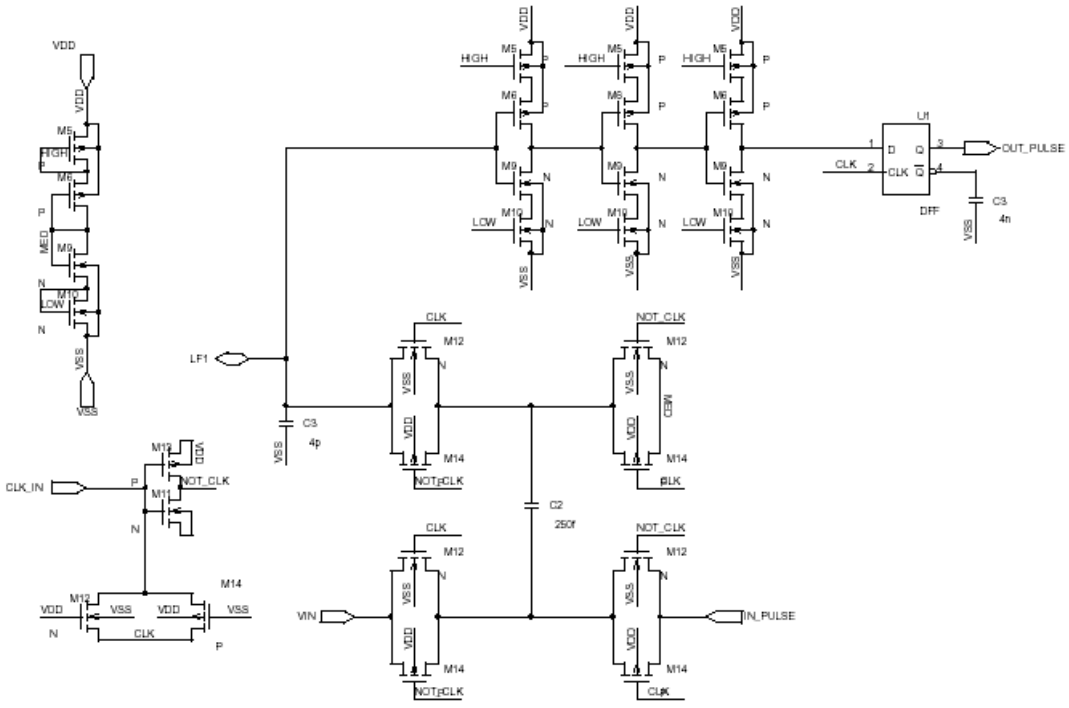

Figure 4.11 First Order Self-Referenced Delta Sigma Modulator

4.4.2 Second Order System

A first order system may be the most power efficient, however it does not take full advantage of the modulator architecture. A second order system is more suited for removal of the clock frequency from the control signal without limiting the bandwidth of the error signal.

Figure 4.12 shows a second order self-referenced system. The second order effect is created by a ladder filter, which adds a switched capacitor stage in series with the flying capacitor subtractor. Two first order filters with the same bandwidth make up a second order Butterworth filter with minimum distortion of the pass band.

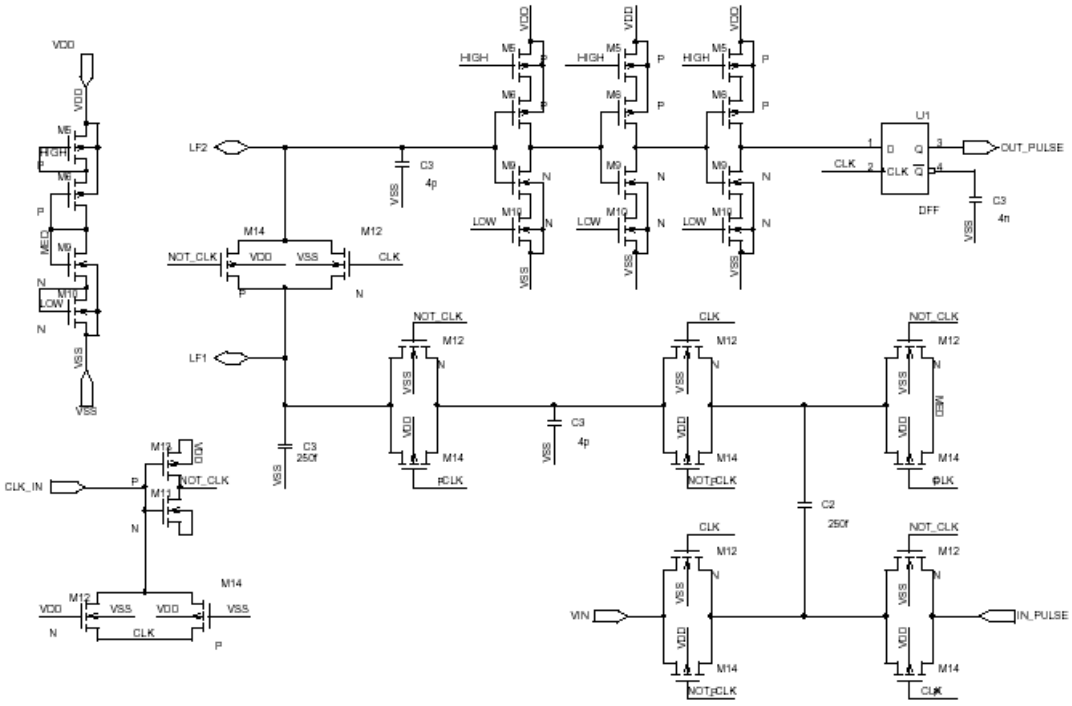

Figure 4.12 Second Order Self-Referenced Delta Sigma Modulator

In this implementation, the voltages on both stages of the filter are centered at the reference signal, MED. The input of the comparator is thus centered at the natural switching point of the inverter stage, and the signal has the benefit of second order sweeping properties. Like the first

order system, the switches on the substracting and integrating capacitors are matched for charge injection.

The use of low-pass filters instead of the conventional inegrators is not coincidental. Although the traditional Delta Sigma architectures use integrators in their loop, there are compelling reasons for using alternate attenuation.

Primary reason for a second order system is stability. A second order system utilizing only integrators is unstable by its nature. A second order system that uses low-pass filters is always stable, because the phase curve never crosses the -180^{o}. The margin plots of the two alternatives are illustrated in Figure 4.13.

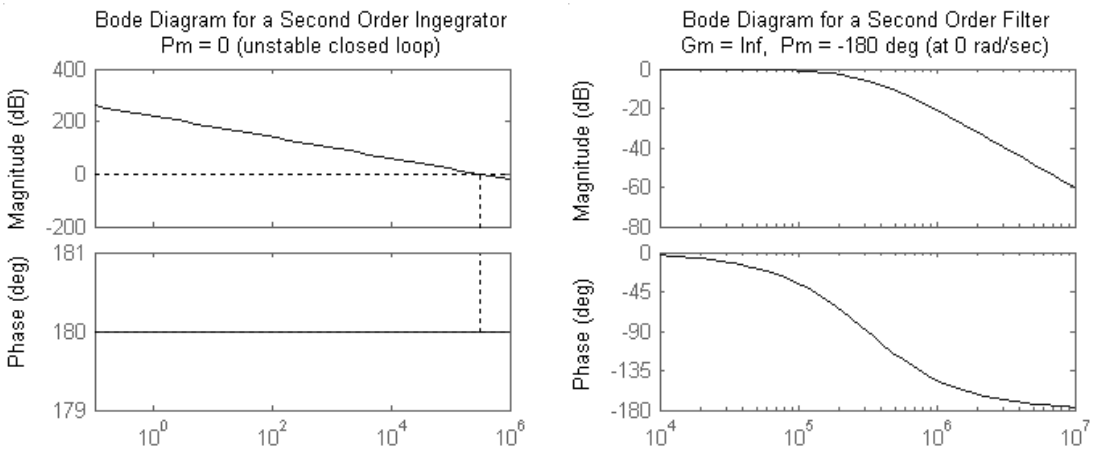

Figure 4.13 Margin Plots for Systems with Integrators and Filters

4.4.3 Pseudo-Floating Gate System

The self-referenced circuit is a minimal system made from carefully selected components. That system expects a certain degree of device matching and supply stability, which is reasonable for an analog system of its caliber, but may not alwyas be practical in a digital technology. A floating gate system in Figure 4.14 addresses the matching issues.

The Band Gap circuit provides a stable reference voltage, however this voltage is no longer the same as the comparator switching point. A static voltage offset is required, so the capacitor, C1 is preloaded with the offset voltage during a Reset cycle. During normal operation, the input of the comparator is left floating, so C1conserves its charge at that node, and thus maintain the offset voltage. At the same time, the other node of C1 integreates the charge from the switched capacitor. Any change on the node of C1 reflects directly on the other node so that the charge is conserved. Thus the Delta Sigma modulator can use the Band Gap reference without sacrificing the self-referenced comparator.

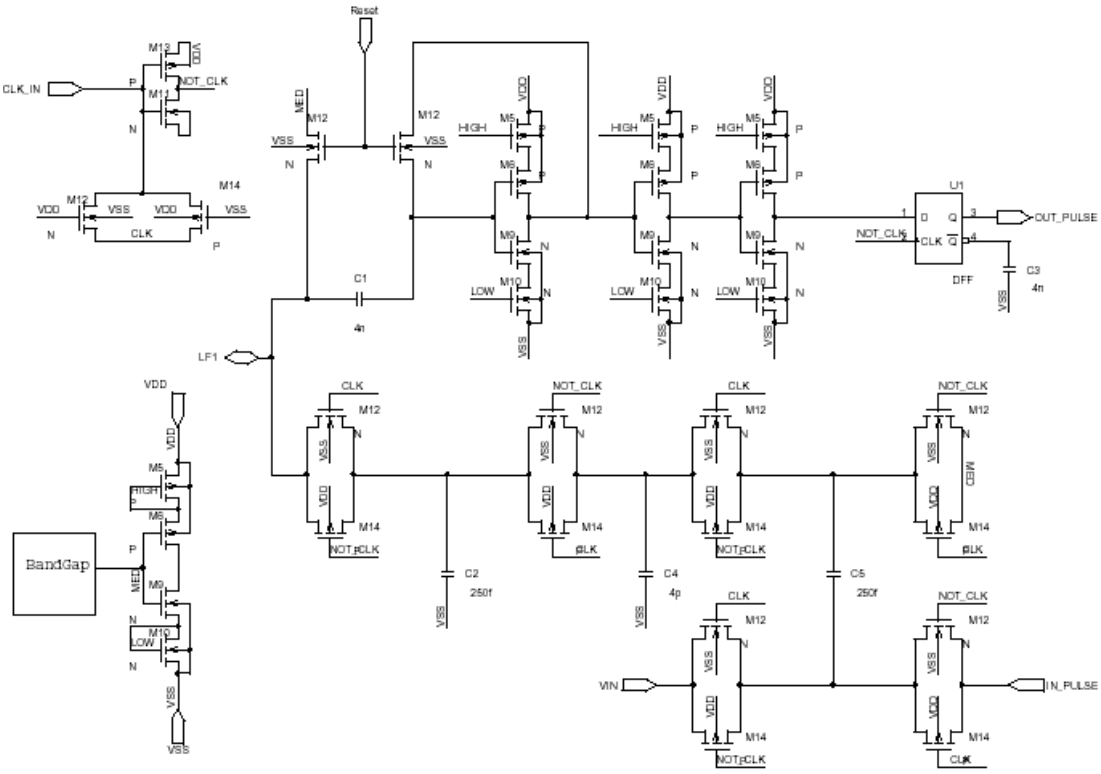

Figure 4.14 Pseudo-Floating Gate modulator with Band-Gap

By following the voltage transformations of each subcomponent in Figure 4.14, an open loop transfer function can be compiled in Laplace domain. Even while assuming ideal conditions and circuit operation, a simple transfer function provides a good insight into circuit operation and performance.

Beginning with the reference circuit, where the output of the bandgap is V(BG):

$$V(BG) = MED \tag{4.16}$$

A subtractor circuit begins the open loop by operating on the reference and the output signals:

$$V(C5+) = MED - V(IN\_PULSE) + V_{in} \tag{4.17}$$

The switched capacitor has an impedance R5eq:

$$R5_{eq} = \frac{1}{C5 \cdot F_{clk}} \tag{4.18}$$

The output of the first filter on C4 is V(C4):

$$V(C4) = V(C5+)\frac{1}{1 + s \cdot R5_{eq} \cdot C2} \tag{4.19}$$

The output of the second filter on C1- is V(C1-):

$$R2_{eq} = \frac{1}{C2 \cdot F_{clk}} \tag{4.20}$$

$$V(C1-) = V(C2+)\frac{1}{1 + s \cdot R2_{eq} \cdot C1} \tag{4.21}$$

Capacitor C1 as a filter yileds an output V(C2). The offset voltage stored in C1 is Voffset:

$$V_{offset} = V_{switching\_point} - MED \tag{4.22}$$

The input voltage of the comparator is V(C1+):

$$V(C1+) = V(C1-) + V_{offset} \tag{4.23}$$

Finally, the output of the comparator is a digital voltage Vcomp.

$$V_{comp} = 0V \quad if\ V(C1+) < V_{switching\_point} \tag{4.24}$$

$$V_{comp} = VDD \quad if\ V(C1+) > V_{switching\_point} \tag{4.25}$$

The digital ouptut is stored in the D flip-flop, and in turn, feeds to the subtractor. Ignoring the clock component, the output voltage Vout can be approximated by a linear signal. To achieve that, the comparator and the flip-flop are modeled by a linear gain Kcomp:

$$V_{out} = K_{comp}\, V(C1+) \tag{4.26}$$

The linear effect of the comparator and the flip-flop can be approximated by a gain Kcomp. Similarly, the voltage shifts (Voffset and MED) have no meaning in frequency domain. The resulting Laplace transfer function for Figure 4.14 is:

$$G(s) = \frac{Vout}{Vin} = \frac{K_{comp}}{(1 + s \cdot R5_{eq} \cdot C4)(1 + s \cdot R2_{eq} \cdot C1)} \tag{4.27}$$

$$G(s) = \frac{K_{comp}}{\left(1 + \frac{s \cdot C4}{C5 \cdot F_{clk}}\right)\left(1 + \frac{s \cdot C1}{C2 \cdot F_{clk}}\right)} \tag{4.28}$$

4.5 Layout Considerations

4.5.1 Capacitance Considerations

When considering capacitor layout, there are two factors that have particular importance: required area and capacitor linearity. An all-metal capacitor does not change value with voltage and can be made accurately. A parallel plate capacitor is the most direct approach, however it is not the most area efficient. The dialectric spacing between two metal layers is not controlled as well as the intra-metal spacing and metals themselves will not be distributed evenly over the plate areas.

Figure 4.15 shows an interleaved all-metal capacitor implementation which has the benefit of process control and additional surface area. An interleaved capacitor uses the more precise inter-metal capacitance to complement the capacitance between metal layers. With smaller features, the metal thickness is under control, and the increased surface area allows for larger capacitance. The structure in Figure 4.15 can have as much as 50% more capacitance than the parallel plate

implemented in the same area. The interleaved structure can be continued through all available metal layers in order to effectively use the silicon area.

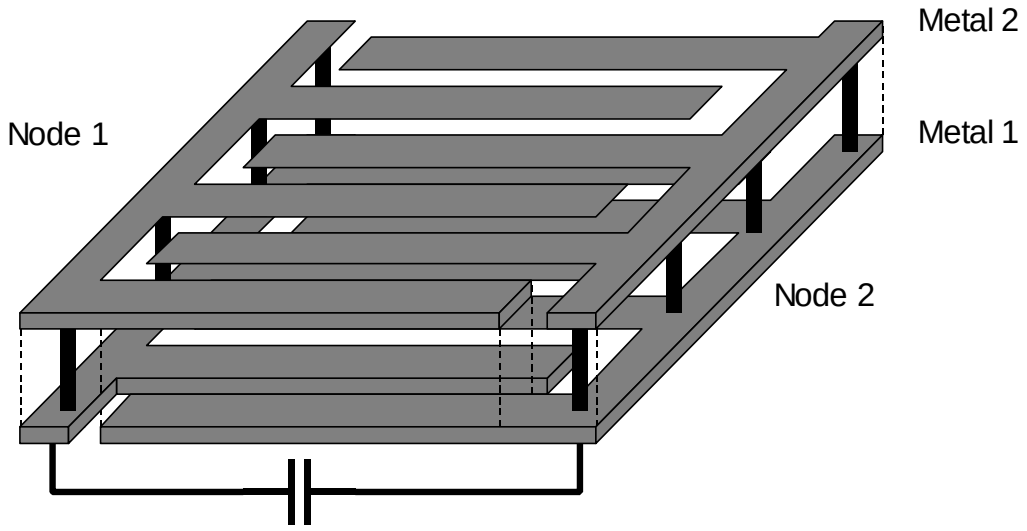

Figure 4.15 Interleaved Capacitor Layout

4.5.2 Layout Technology

All layout in this project was performed for an Atmel 0.35 um CMOS technology with single poly and four metal layers. Process specifics are confidential.

4.5.3 Final Layout

The First Order modulator is implemented using a standard I/O underlayer and interleaved capacitors, as illustrated in Figure 4.16. This four pad structure contains its own power and ground pads for supply isolation, a pad for an input voltage, and a pad for additional loop filter capacitance. The metal capacitors for the modulator, and power-ground metalization consumes most of the area in this device.

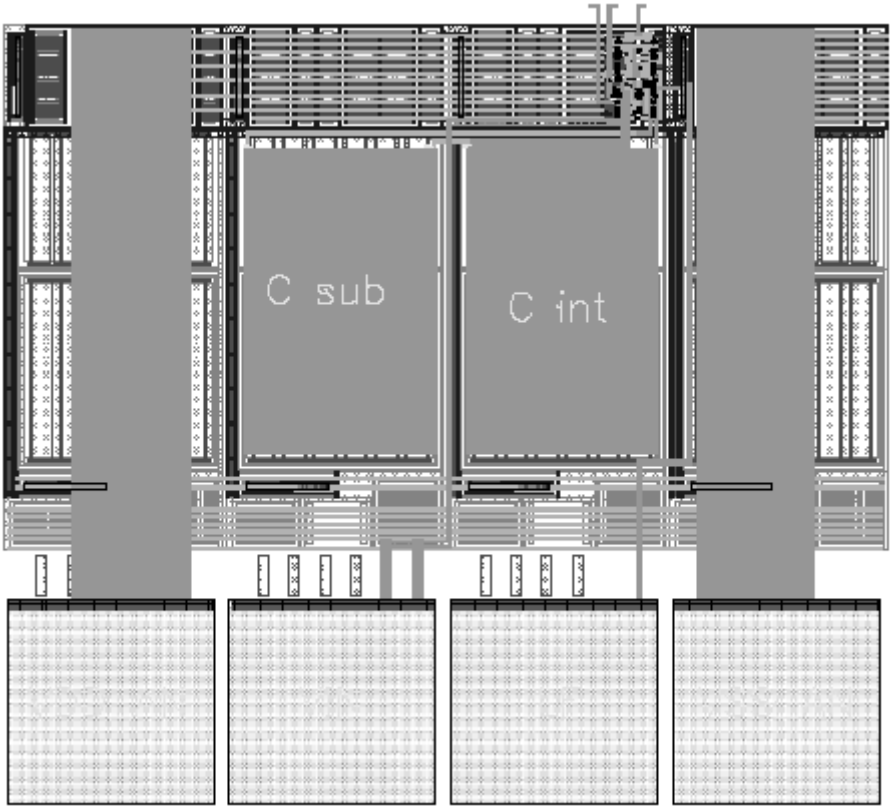

Figure 4.16 Layout of the First Order Delta Sigma Modulator

A band gap reference is illustrated in Figure 4.17. It has been combined with an optional 20 mA 3.3V voltage regulator to make better use of the standard underlayer area. The band gap does not require external circuitry, and the single pad is used to power the regulator.

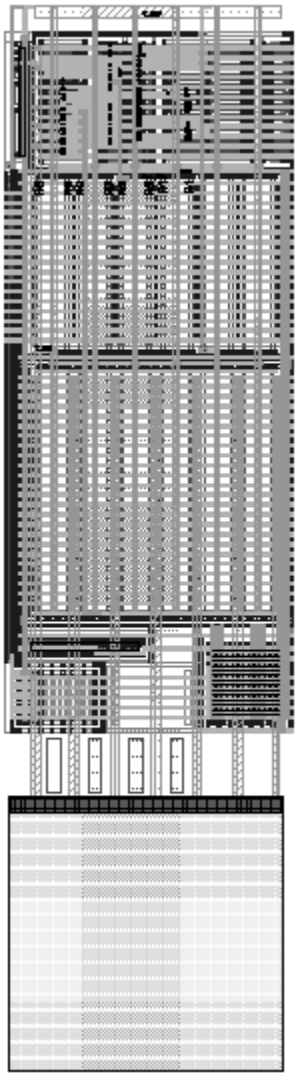

Figure 4.17 Band Gap Voltage Reference Layout

Circuits in the examples above are combined on a 1.7 mm^2 68 pad test chip shown in Figure 4.18. This chip contains four Delta Sigma modulators, one on each side, and relating test infra-structure to allow access to internal nodes for test purposes.

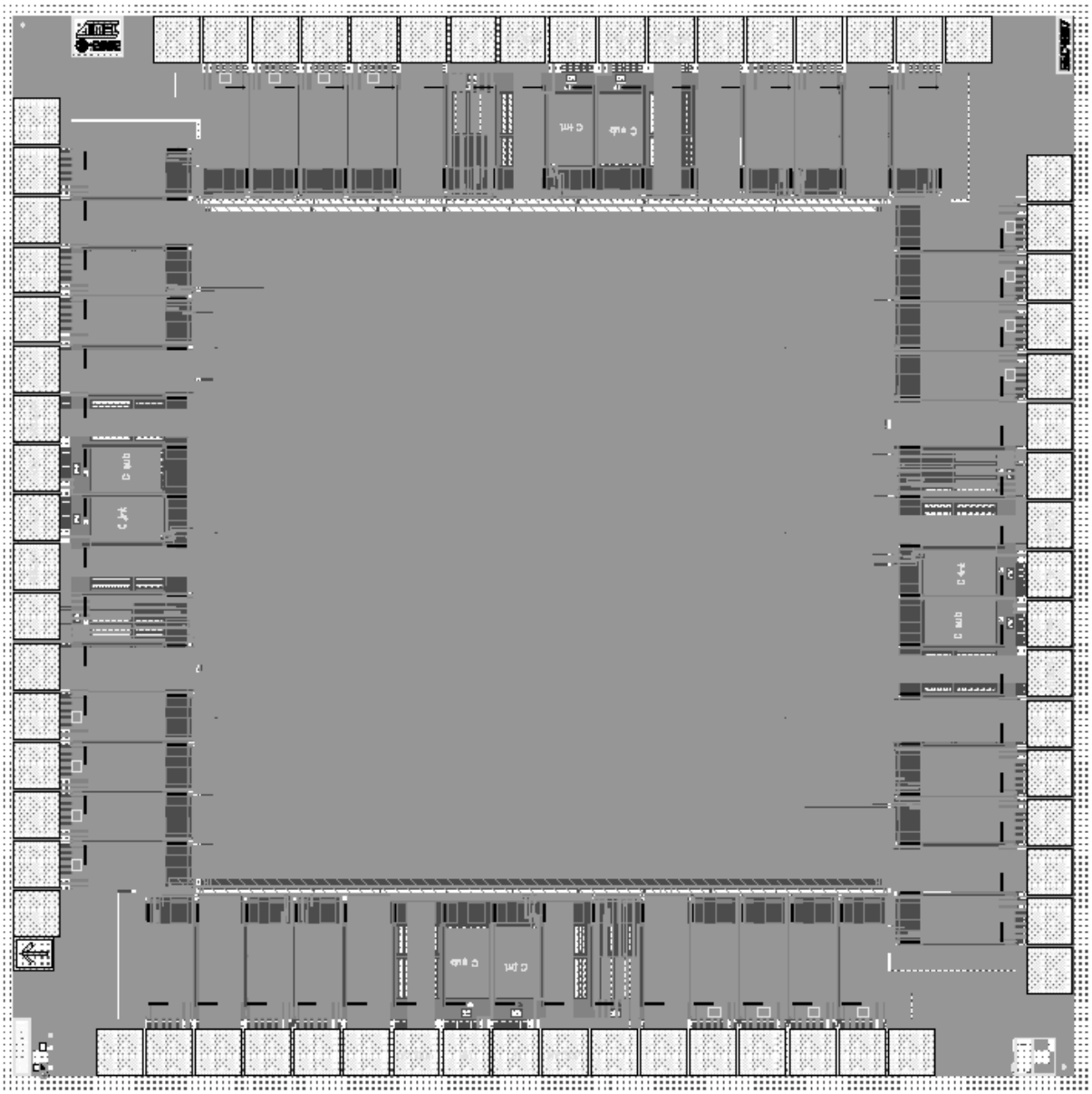

Figure 4.18 Test Chip Layout in 0.35u technology

4.6 Summary

This chapter applies the theory and derivations of previous chapters to create a compact Delta Sigma modulator suitable for low power. It shows how modular components are designed and integrated into a complete feedback system. It also shows how to create a first order Delta Sigma modulator, and how to upgrade it to a second order system. The pseudo-floating gate design is

shown as the final result of this design effort; it offers the same low power architecture with enhansed noise rejection.

We described a second order Delta Sigma modulator as an improvement on the first order, however the second order modulator was not implemented in layout because the target technology, Atmel 35 um, was no longer available for a test chip.

CHAPTER 5: Simulation Results

5.1 Introduction

This chapter summarizes the simulation results for the Delta Sigma architectures described in Chapter 4. Since it is impractical to include all the collected data, the graphs are to illustrate critical observations in system behavior.

All simulation results in this chapter are obtained using the Cadence simulation environment and the Spectre simulator. The input voltage of the modulators is swept from rail to rail using multiple points, and a transient analysis is performed on each point for several thousand clock cycles. Due to the long simulation times and the large amounts of data involved, the presented data is a sub-sample of all possible simulation points, but it can be used as a representative of circuit performance.

5.2 First Order Modulator

Tranisent simulations of the First Order self-referenced modulator were performed in Cadence, Spectre simulator for 10 input voltage points. Samples of the output waveforms have been displayed in Figure 5.1 to illustrate system behavior.

Since a sweep of all input points for an 8-bit system was unfeasible, a sweep across ten input voltages is taken to represent the performance of the system.

Each of ten simulations ran for 640 cycles (= 128*5) to give an accurate representation of the modulator performance. The goal of each simulation was to determine the system behavior at various input voltages and to measure the pulse rate of the modulator output. As was shown in the previous sections that the delta sigma pulse rate is equivalent to the duty cycle of the output waveform. Rather than counting individual pulses, the modulator output was fed into an ideal gate model which removed transient properties of the waveform and forced rise and fall times to be equivalent. The duty cycle of the processed waveform was then calculated using the Cadence

Analog Environment tools. This process was easier to automate particularly for the longer runs and parametric analyses.

Figure 5.1 shows snapshots of the transient ouput of the First Order modulator. An important observation is that all changes in the output are performed in a predictable linear manner, characteristic of a first order system.

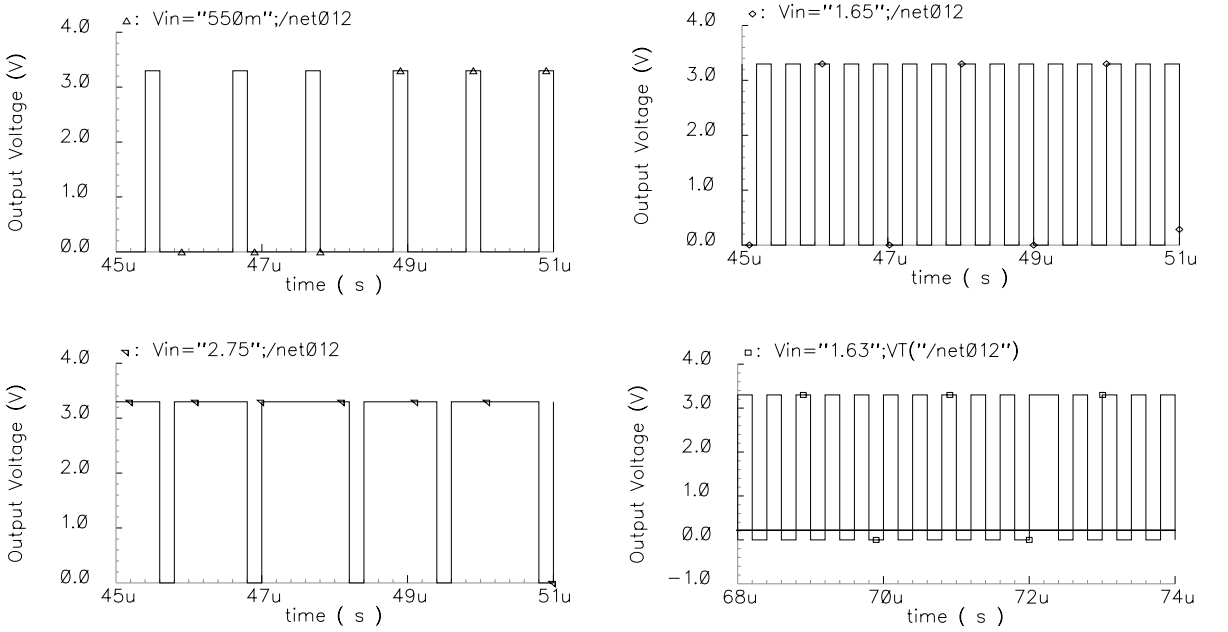

Figure 5.1 Sample transient outputs for the First Order modulator

Figure 5.2 shows the output error pattern for the First Order modulator. The modulator is highly accurate when looking at mid-voltage ranges, but the performance degrades quickly when approaching the power rails. While in the range from 0.8 V to 2.5 V the output qualifies for the 8-bit resolution. For the rail-to-rail operation the output quality degrades to 6 bits.

The SNDR (Signal to Noise and Distortion Ratio) plot in Figure 26 shows that this modulator delivers a signal to noise ratio up to 51.7 dB which qualifies for 8 bits of resolution. The dynamic range of the system is measured to be 62 dB, which means that the smallest voltage variation detectable by this modulator is 2.6 mV, or equivalent to a 10-bit resolution. Table 5.1 sum-

marises the modulator specifications for the first order system. Note that the circuit draws less than 25 uA of current.

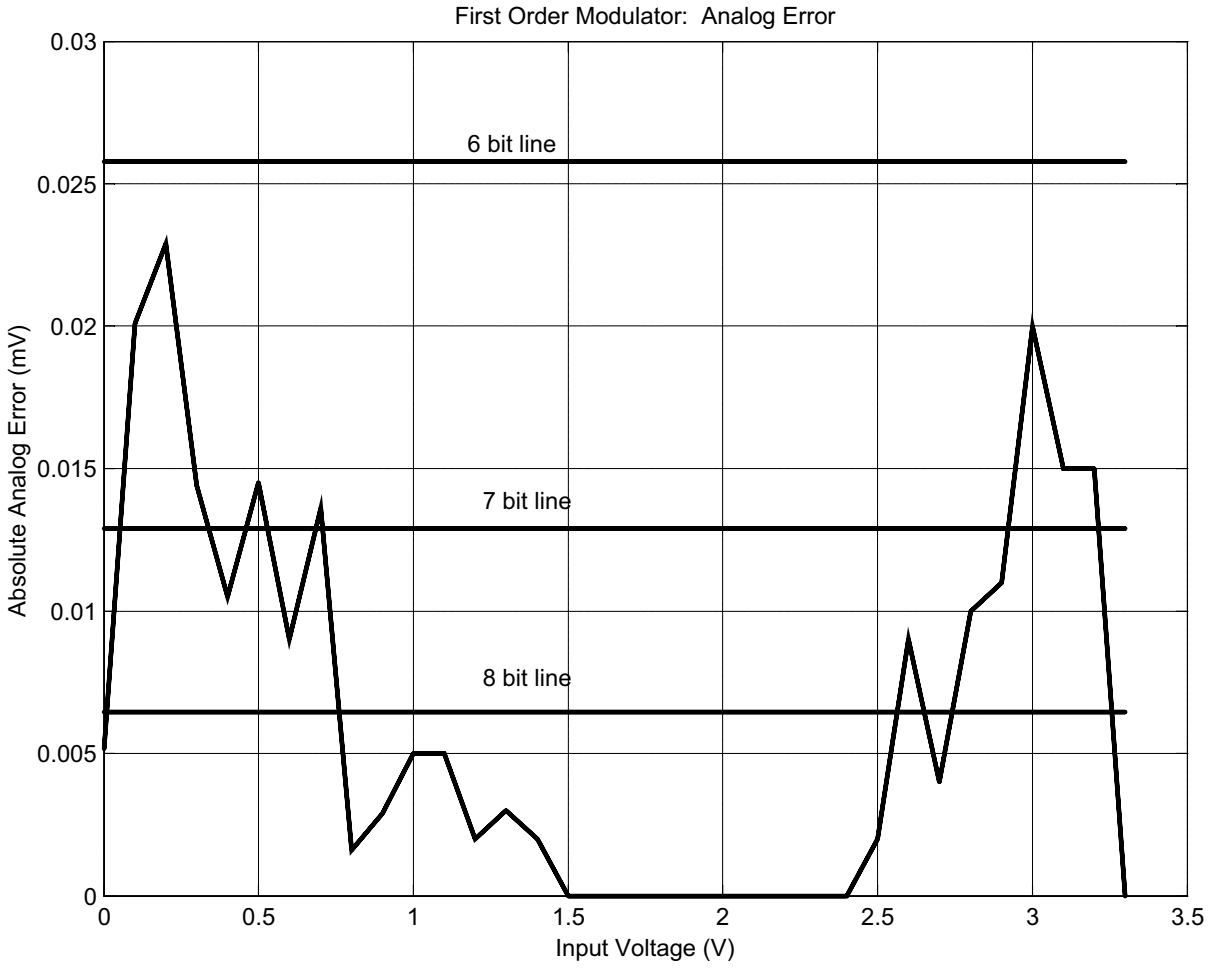

Figure 5.2 First Order modulator, error dependence on the input voltage

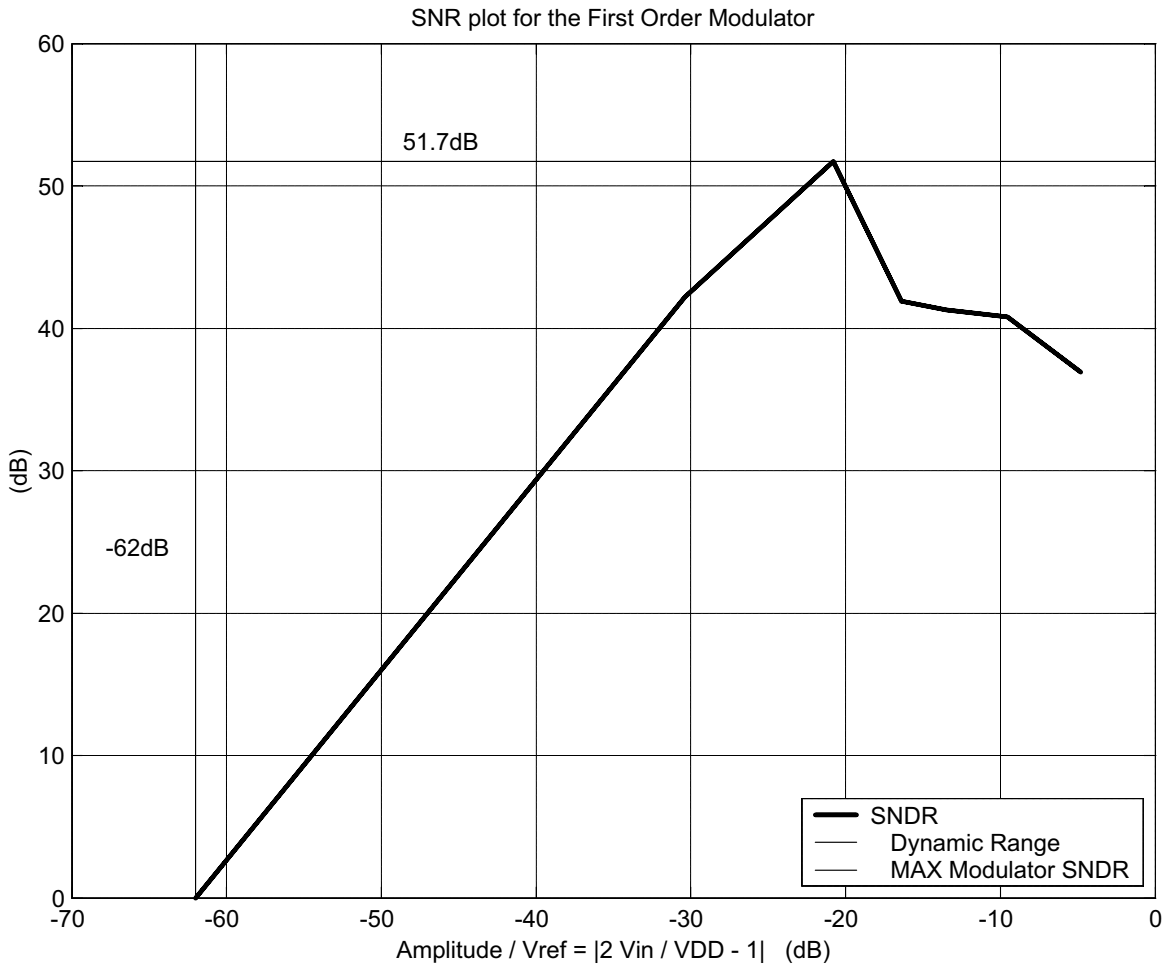

Figure 5.3 SNR properties of the First Order modulator

Table 5.1: First Order Modulator Specifications

Category	Symbol	Value
Technology		0.35um
Clock Frequency	Fclk	5 MHz
Power Supply Voltage	VDD	3.3V
Input Voltage Range	Vin	0V - 3.3V
Simulated Modulator Resolution		6 bit - 8 bit
Minimum Allowed Input Step		3.9 mV
Average Offset Voltage	Voff	0 V
Signal Bandwidth at Modulator Resolution	BW	19.5 kHz - 78.1 kHz
Signal to Noise Ratio (for Fin < BW)	SNR	~ 51.7 dB
Simulated Signal to Noise and Distortion Ratio (for Fin < BW)	SNDR	51.7 dB
Simulated Dynamic Range	DR	62 dB
Output Rate	Fout	5M samples/sec.
Current Drawn	I_Q	19.8 uA - 24.5 uA
Average Power Consumption	Pout	75.2 uW

5.3 Second Order Self Referenced Modulator

Transient simulations of the Self-Referenced Delta Sigma modulator were performed in Spectre simulator for 69 different input voltages. Example output waveforms are displayed in Figure 5.4.

A sweep of all 4,096 input voltages for a complete 12 bit characterization was unfeasible due to extremely long simulation times required for each point and the enormous data size. Ten out of 69 points were simulated for a 10,000 bit window to give accurate error estimates. These ten values were used to determine the static peformance of the system and for the error plots. The remaining 59 simulations were performed for 500 bit windows to give a thorough representation

of system performance and linearity, however the data was not used for any other purpose, since at least 4,096 points are required to represent a 12 bit system.

Snapshots of select transient outputs are shown in Figure 5.4. Unlike the first order modulator, these waveforms have a non-linear sweeping quality. A second order system has a better memory element, it tracks the signal and its rate of change. It is this quality that makes a second order system more accurate.

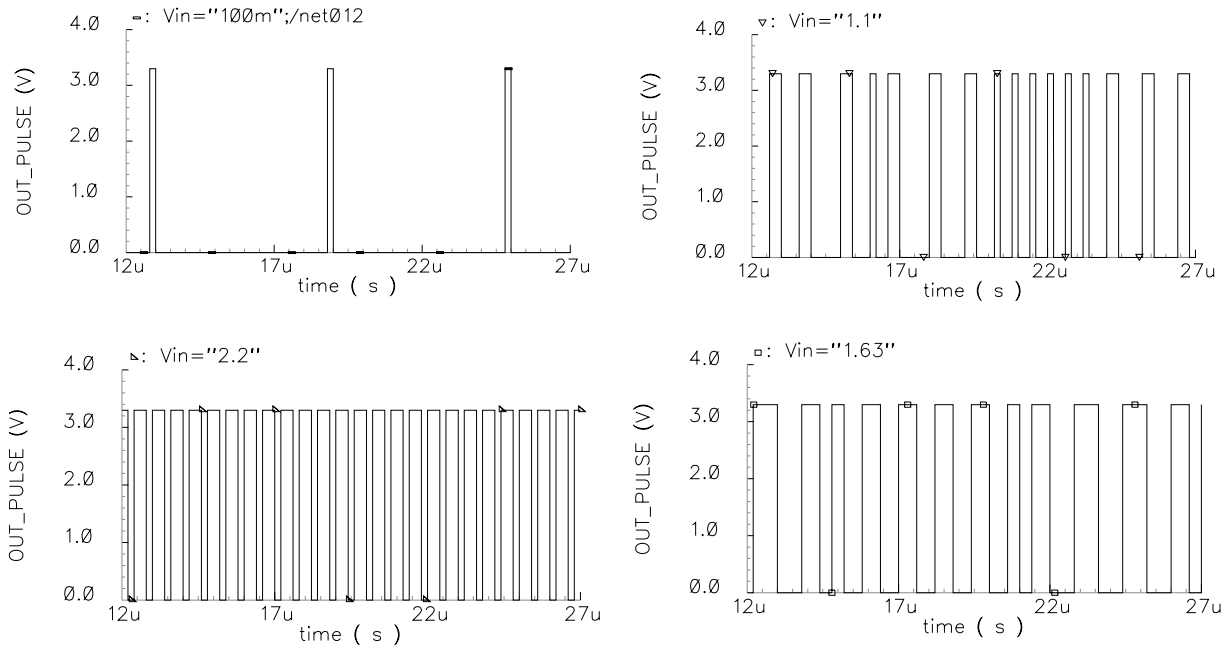

Figure 5.4 Sample transient outputs for the Self Referenced modulator

Figure 5.5 illustrates the output error as it relates to quantization error. The DC signal that can be recovered from the output window of 10,000 samples contains a combination of patterned and random errors. The patterned error is due to the discrete nature of the output, where the de-modulated signal occupies one of 10,000 discrete voltage levels. The smallest distinguishable voltage step for the data points is 3.3 V/10,000 = 0.33 mV. The smallest distinguishable voltage step for a 12 bit system is 3.3 V / 4,096 = 0.806 mV. For these reasons, the output of the modulator follows the input signal in quantization steps rather than being linear as illustrated in Figure 5.5a. The analog error due to the modulator noise is much smaller, and well below 403 mV decision level of a 12 bit system, which can be seen in Figure 5.5b.

It is interesting to note that the modulator error is not completely random, and it still contains the quantization error pattern although to a lesser extent. There are several reasons for this, the major reason is that the number of samples is 10,000, which is differet from the number of steps in a 12 bit system whcih is 4096.

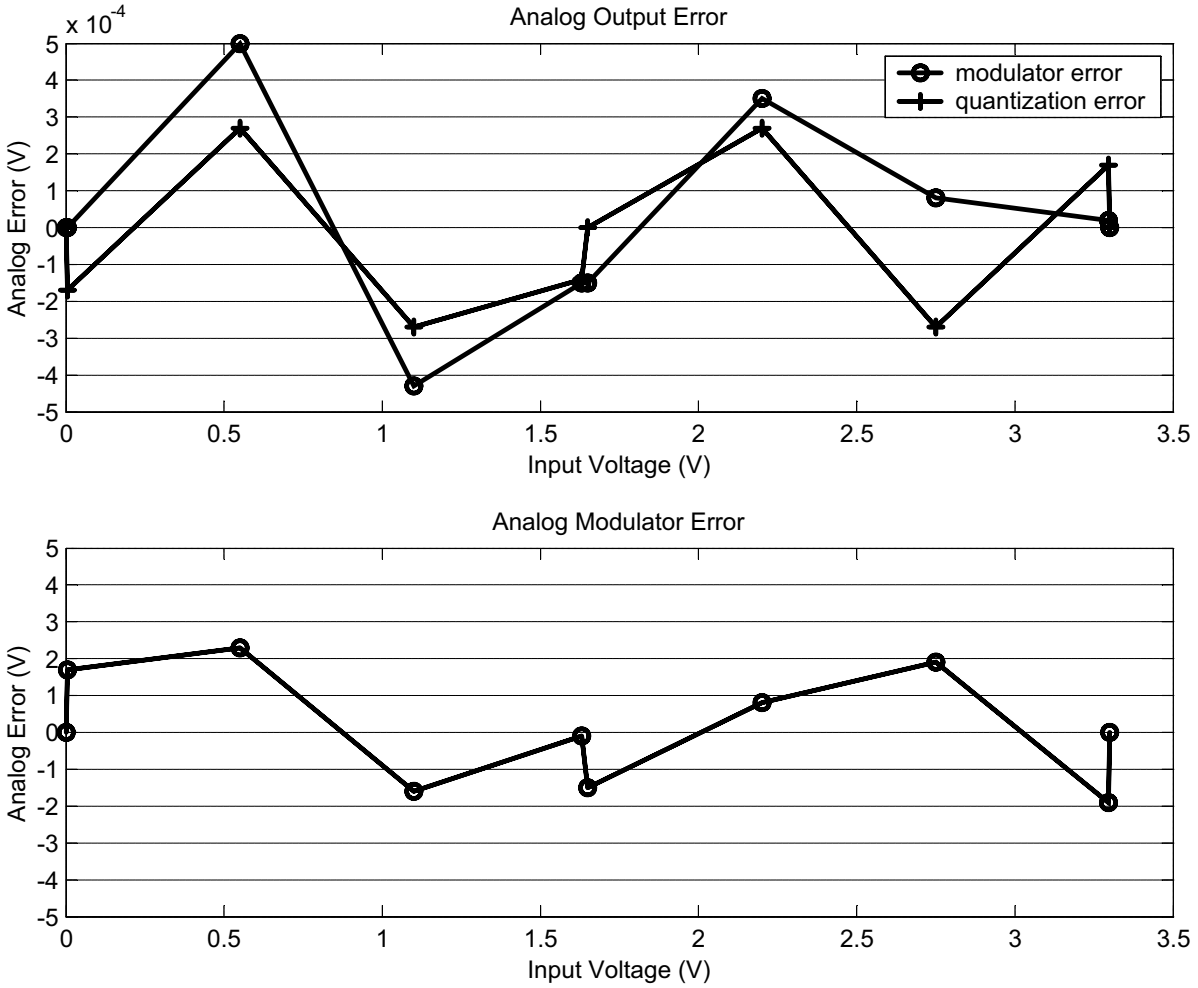

Figure 5.5 Select analog output errors for the Self Referenced modulator

Figure 5.6 shows the SNR plots estimated from the simulations. Although the simulations look ideal, this device reaches its limit at rail-to-rail inputs. A feedback system must operate on non-zero error, and for rail inputs it must be at least 1 bit. For this reason, the SNR of this system rolls off just before 75.6 dB point. The Self Referenced modulator performance is summarized in Table 5.2.

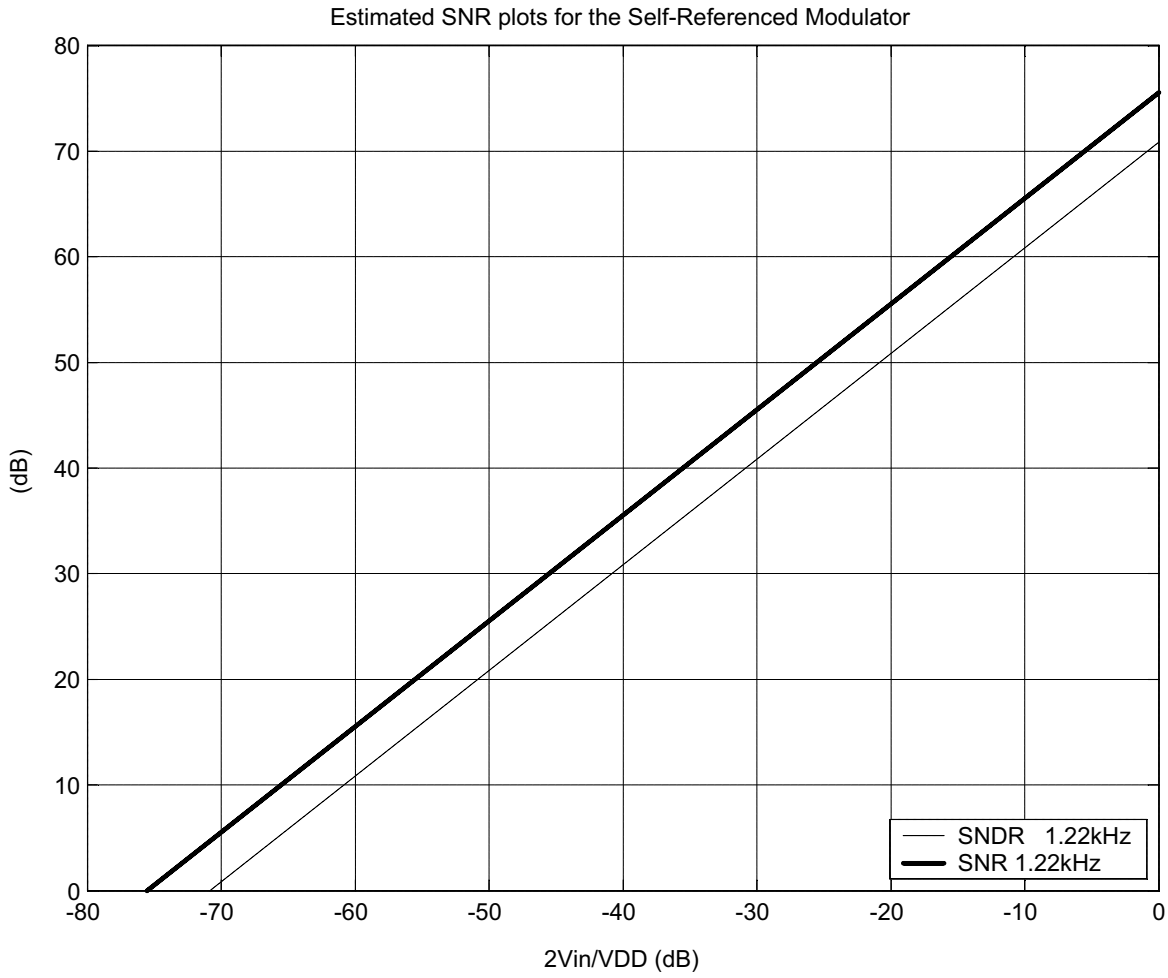

Figure 5.6 SNR plots for the Self-Referenced modulator (estimated from DC simulations)

Table 5.2: Second Order Self-Referenced Modulator Specifications

Category	Symbol	Value
Technology		0.35um
Clock Frequency	Fclk	5 MHz
Power Supply Voltage	VDD	3.3V
Input Voltage Range	Vin	0V - 3.3V
Simulated Modulator Resolution		12 bit
Minimum Allowed Input Step		0.805 mV
Average Offset Voltage	Voff	0 V
Signal Bandwidth at Modulator Resolution	BW	1.22 kHz - 39 kHz
Signal to Noise Ratio (for Fin < BW)	SNR	< 75.6 dB
Simulated Signal to Noise and Distortion Ratio (for Fin < BW)	SNDR	70.9 dB
Simulated Dynamic Range	DR	75.6 dB
Output Rate	Fout	5M samples/sec.
Current Drawn	I_Q	18.3 uA - 34.1 uA
Average Power Consumption	Pout	86.46 uW

5.4 Second Order Floating Gate Modulator

Transient simulations of the Floating Gate modulator were performed in Spectre simulator for 10 different input voltages chosen at critical points of modulator operation. As with the previous modulators it was not feasible to sweep more data points due to simulator limitations, however the chosen points are sufficient to describe the behavior and performance of the Floating Gate modulator as it compares to other implementations.

Figure 5.7 shows snapshots of select tranisient output waveforms. The second order sweeping patterns are apparent. The output and quantization error plots are shown in Figure 5.8a, and the analog error describing the inaccuracies of the modulator is shown in Figure 5.8b. The output

error is sufficient for a 10-bit system, and the error pattern follows the 10-bit quantization pattern fairly closely. The modulator error is significant by itself, even without the distortion effects the system is limited to 10 bits.

An interesting observation is that the error for the Floating Gate modulator has a much larger random component than the second order Self Referenced modulator, so the error due to noise is almost as large as the error due to distortion. This is apparent when comparing the output waveform in Figure 5.8a to the analog modulator error in Figure 5.8b.

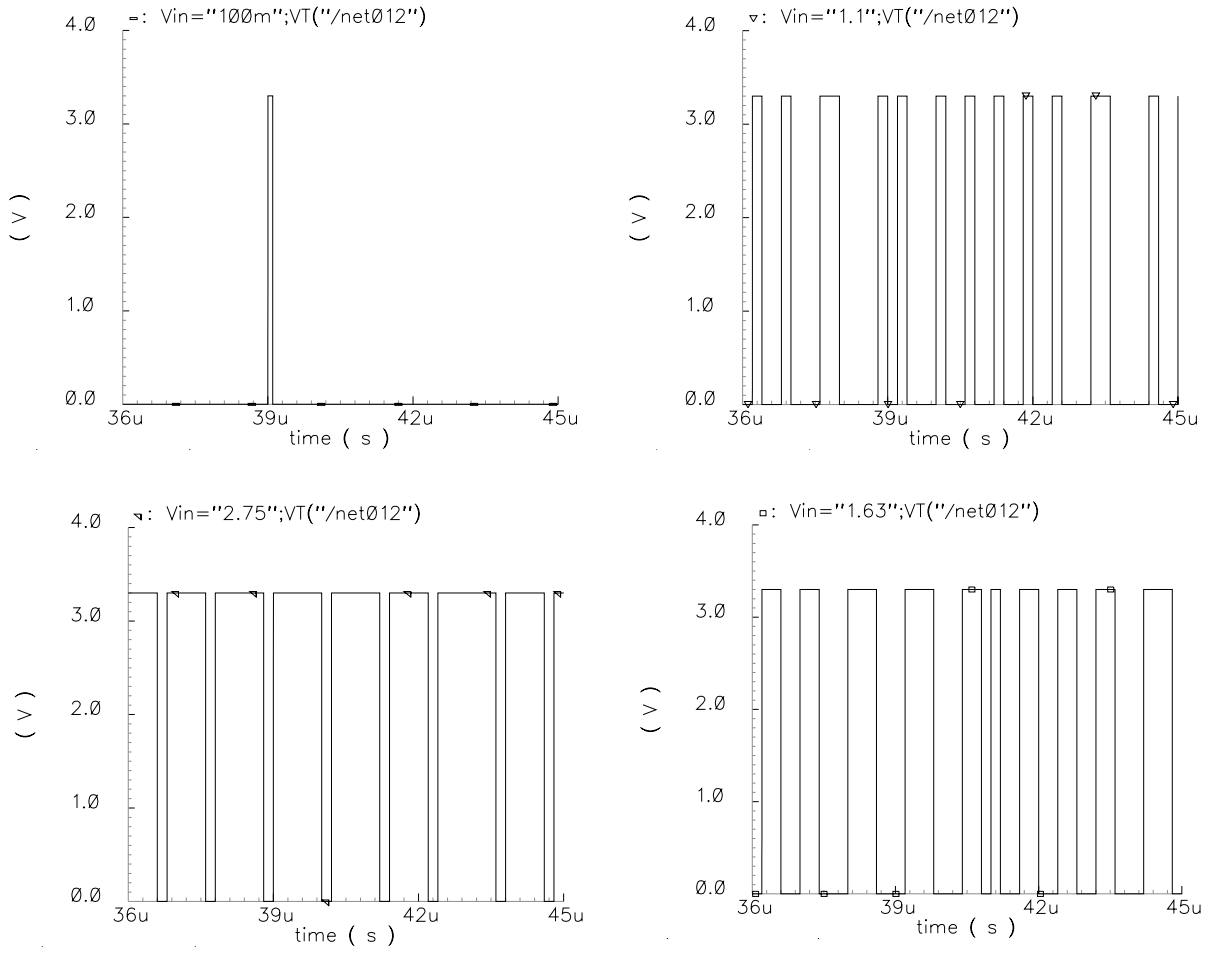

Figure 5.7 Sample transient outputs for the Floating Gate modulator

It is too difficult to simulate the dynamic properties of the Floating Gate modulator system, particularly at an expected precision level. Figure 5.9 shows the SNDR curve estimated from the

DC simulations. At the highest precision of this modulator, 10 bits, and signals within 4.88 kHz can be evaluated as a DC signal. As in the case of the Self-Referenced modulator, it is expected that the accuracy declines when the inpu signal reaches either of the power rails, so while the Dynamic Range of the system is expected to be at 61.4 dB, the Signal to Noise ratio is expected to be a step smaller.

Table 5.3 shows the simulated specifications for the Floating Gate Delta Sigma modulator. The value that differs most from the previous modulator implementations is the large current draw. Roughtly two thirds of the total power consumed is attributed to the static current drawn by the added Band Gap reference, which accounts for most of the additional power consumption. The remaining power difference would be due to the refresh cycles of the autozeroed comparator.

Even though the power specifications for the Floating Gate modulator are much larger than the other designs considered, the additional fucntionality may be worth it in a noisy system. At 276 uW this modulator is more than competitive, and does provide the the target resolution of 10 bit.

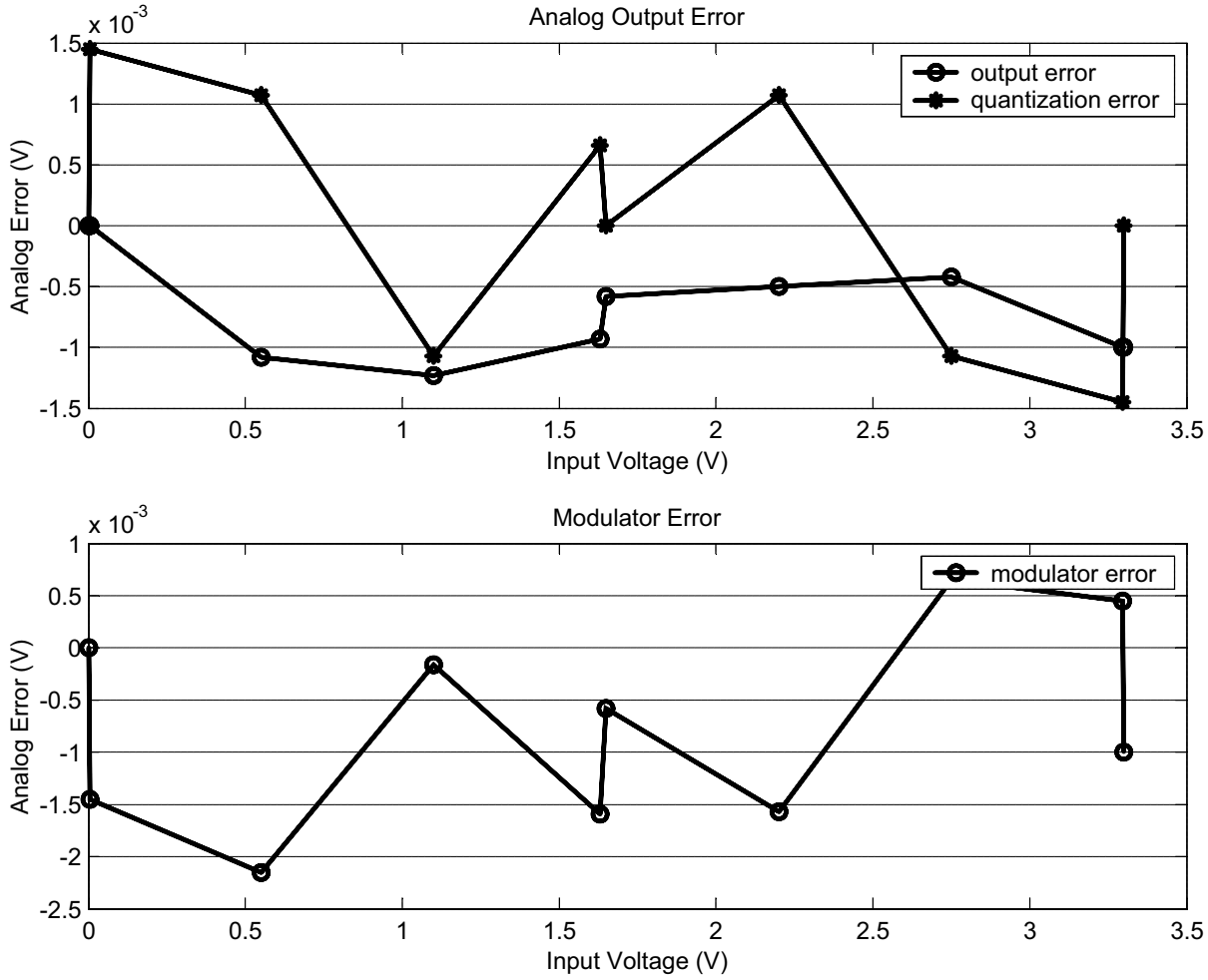

Figure 5.8 Select analog output errors for the Floating Gate modulator

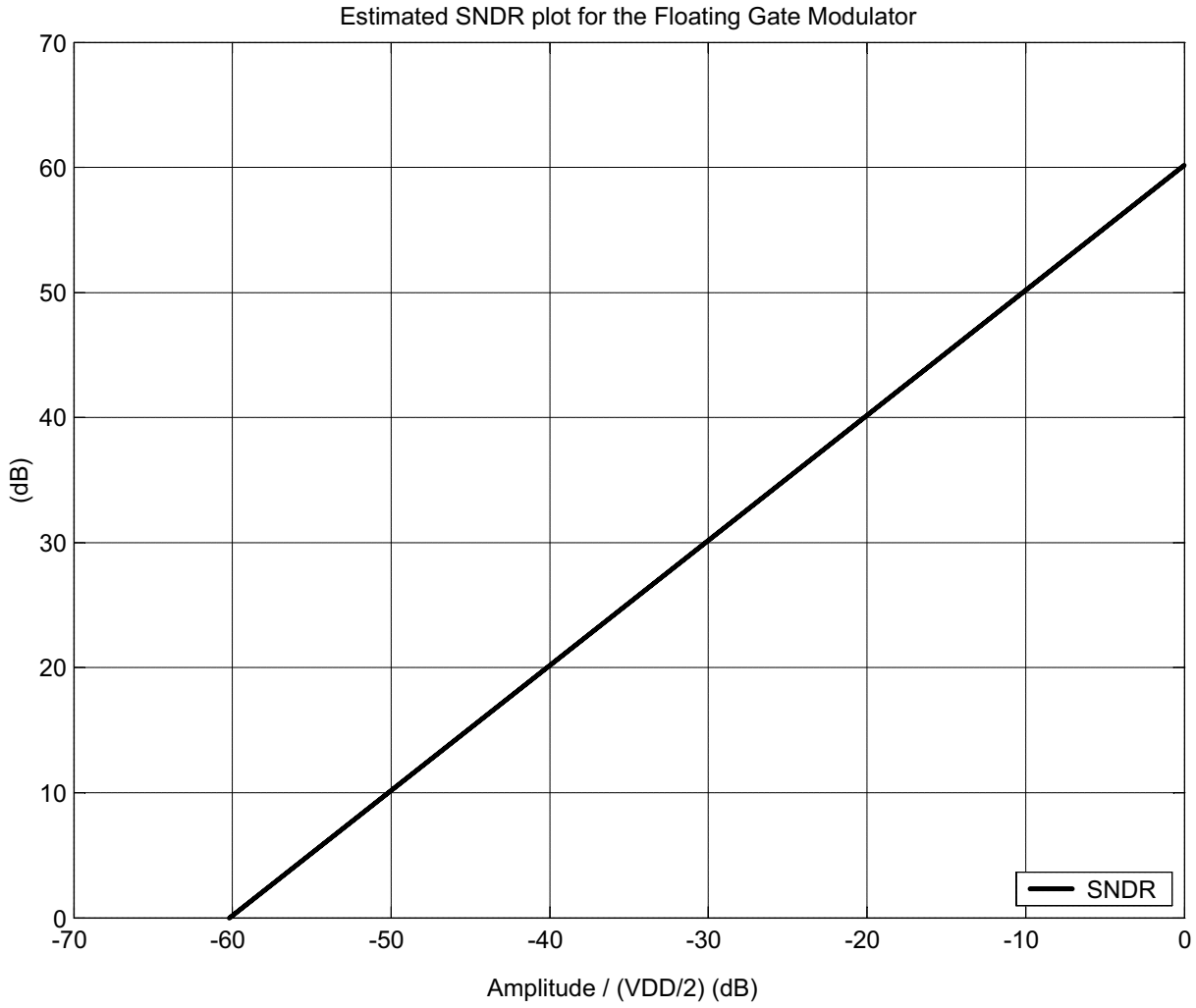

Figure 5.9 SNDR plot for the Floating Gate modulator (estimated from DC simulations)

Table 5.3: Second Order Floating Gate Modulator Specifications

Category	Symbol	Value
Technology		0.35um
Clock Frequency	Fclk	5 MHz
Power Supply Voltage	VDD	3.3V
Input Voltage Range	Vin	0V - 3.3V
Simulated Modulator Resolution		10 bit
Minimum Allowed Input Step		3.22 mV
Average Offset Voltage	Voff	0 V
Signal Bandwidth at Modulator Resolution	BW	4.88 kHz
Signal to Noise Ratio (for Fin < BW)	SNR	< 61.4 dB
Simulated Signal to Noise and Distortion Ratio (for Fin < BW)	SNDR	~ 60.8 dB
Simulated Dynamic Range	DR	61.4 dB
Output Rate	Fout	5M samples/sec.
Current Drawn	I_Q	77.5 uA - 89.6 uA
Average Power Consumption	Pout	276 uW

5.5 Summary

Perhaps the most important contribution is the alternative design methodology for mixed signal components that targets low power digital systems. Partitioning a system into independent modules allows each subcircuit be designed independently. The sub-components are selected by cycling through available technologies for a circuit with the best fit. Using prioritized system constraints in selecting individual sub-components creates an “annealing” process where a system improves one step at a time and one component at a time. As a result the system design systematically evolves until it meets the design constraints.

Such forethought in the design stage makes implementation trivial. The 'annealing" technique produces the device level implementation at the same time as the system level specification, and when the circuit is defined, the design process becomes very simple. Using simulation tools such as "HSPICE" and "Spectre" in the final stages of the process serves to verify the design as well. Once the system is defined using the above methods, the layout and verification is only a matter of days.

The final design decision settled on a Delta Sigma modulator architecture using switched capacitors. This architecture was selected for its low power consumption and perfect modularity. Furthermore, reference and comparator circuits were designed to take account of transistor mismatching and arbitrary switcing points.

By the end of the design process, several implementations of the switched Delta-Sigma modulator have evolved that conformed to the initial design criteria. While sharing many similar characteristics, each design offered something unique, therefore three implementations were selected for final presentation. The three final circuits embody the tradeoff between area, power consumption and process tolerance, where each circuit is specialized. A first order modulator occupies the smallest area, and offers the smallest power consumption. A self-referenced design offers the highest accuracy under normal running conditions. The modulator using the floating gate technique with a band-gap reference offers the most process and environment independent operation.

5.6 Comparison of the Three Architectures

In order to give the reader a good perspective on Delta Sigma modulators, the modulators in this thesis were characterized using commonly accepted methods, to be compared and evaluated next to implementations documented in other respectable publications.

Comparing the performance of Delta Sigma architectures is not a straight forward task. This is particularly the case when comparing designs of different researchers. All data from performance measurements to silicon area is subject to the specific methods, available tools and assumptions of the researcher. Although this project has made use of commonly accepted meth-

ods of characterization of Delta Sigma modulators, the goals and methodology of this project differ from other publications, as they should.

All the data in the comparison tables was displayed the way it was recorded and presented in the publications. It is important for the reader to keep in mind the scarecely mentioned features that may effect compatibilities of certain designs with certain design environment. For example, area is an important consideration, but it is difficult to compare area measurements for a gate-array, standard cell, standard underlayer and custom underlayer designs, because ther may not be interchangeable. Modulator precision is another important measurement, however precision can be defined as the smallest step size, the signal-to-noise ratio or as the dynamic range depending on the target requirements. For a chip designer, the ultimate decision will rest on technology compatibility of a particular implementation, which may as well be a design with the poorest performance.

The results of this project were compared to the designs documented in the “Design of Low-Voltage Low-Power CMOS Delta-Sigma A/D Converters” by V. Peluso, M. Steyaert and W. Sansen. The above publication has similar goals to this project, and has well documented methodology, implementation and results. It is believed that their techniques are sound and worthy of comparison, even though their results are extremely competitive. The Delta Sigma modulator data is summarized in Table 5.4.

Table 5.4: Delta Sigma Modulator Summary

Category	First Order Modulator	Self-Referenced Modulator	Floating Gate Modulator	Modulator 1 (V. Peluso, M. Steyaert, W. Sansen)	Modulator 2 (V. Peluso, M. Steyaert, W. Sansen)
Technology	0.35um	0.35um	0.35um	0.7um	0.5um
Description	First Order	Second Order	Second Order with Band-Gap	Third Order Architecture	Third Order Differential Architecture
Integration Method	Switched Capacitor	Switched Capacitor	Switched Capacitor	Switched Op-Amp	Switched Op-Amp
Passive Components	On-Chip	On-Chip	On-Chip	Off-Chip	Off-Chip
Clock Frequency	5MHz	5MHz	5MHz	500kHz	1.538MHz
Frequency Technology Factor	1.75 Hz*m	1.75 Hz*m	1.75 Hz*m	0.35 Hz*m	0.769 Hz*m
Power Supply	3.3V	3.3V	3.3V	1.5V	900mV
Input Voltage Range	0.83V - 2.5V	0V - 3.3V	0V - 3.3V	120 Vrms	500 Vp-p
Absolute Modulator Resolution*	8 bit	12 bit	10 bit	9 bit	12 bit
Effective Modulator Resolution **	7 bit	12 bit	10 bit	6 bit	11 bit
Quantization Step	12.9 mV	0.805 mV	3.22 mV	2.9 mV	0.22 mV
Bandwidth at Maximum Resolution	> 19.5 kHz	> 1.22 kHz	> 4.88 kHz	3.4kHz	16kHz

Table 5.4: Delta Sigma Modulator Summary

Category	First Order Modulator	Self-Referenced Modulator	Floating Gate Modulator	Modulator 1 (V. Peluso, M. Steyaert, W. Sansen)	Modulator 2 (V. Peluso, M. Steyaert, W. Sansen)
Signal to Noise Ratio	~ 51.7 dB	~ 75.6dB	~ 61.4 dB	66 dB	76 dB
Signal to Noise and Distortion Ratio	51.7 dB	70.9 dB	60.8 dB	-	62 dB
Dynamic Range	62 dB	75.6 dB	61.4 dB	74 dB	77 dB
Output Rate	5M samples/s	5M samples/s	5M samples/s	500k samples/s	1.538M samples/s
Silicon Area	0.1 mm^2	0.128 mm^2	0.154 mm^2	0.5 mm^2 ***	0.85 mm^2 ***
Layout Type	Standard Underlayer	Standard Underlayer	Standard Underlayer	Custom Underlayer	Custom Underlayer
Average Current Drawn	22.15 uA	26.2 uA	83.5 uA	66.7 uA	44.4uA
Current Draw -Sample Rate Ratio	4.43 uA/Msample	5.24 uA/Msample	16.7 uA/Msample	133.4 uA/Msample	28.9 uA/Msample
Average Power Consumption	75.2 uW	86.5uW	276 uW	100 uW	40 uW
Power to Sample Rate Ratio	15.0 uW/Msample	17.3 uW/Msample	55.2 uW/Msample	200 uW/Msample	26.0 uW/Msample

* The Absolute Modulator Resolution is calculated from the Signal to Noise Ratio, with repect to the supply voltage: $\log_2(10^{SNR/20}))$

** The Effective Modulator Resolution is calculated from the Signal to Noise Ratio, with repect to the measurable voltage range: $\log_2(10^{SNR/20} * V_{swing} / VDD))$.

*** Represents the area of the entire test chip.

5.7 Conclusions

The Delta Sigma modulators presented in this thesis perform competitively when compared to similar endeavors by other researchers. Table 5.4 summarizes the important statistics from the three modulators described in this thesis and two comparable implementations taken from "Design of Low-Voltage Low-Power CMOS Delta-Sigma A/D Converters" by V. Peluso, M. Steyaert, and W. Sansen.

Before comparing the performance of the listed modulators it is important to note the design differences between them. The first notable difference is in the technologies used. The technology used in this paper is 0.35 um process, as compared to the 0.5 and 0.7 processes in the other modulators. Although analog devices rarely use minimal features, technology minimization helps to lower gate capacitance and the total amount of charge being swithed at each event.

Smaller charge transfers allow a switched circuit to run at faster rate without hurting the power consumption or accuracy. In this case the circuits created in 0.35 um technology run at 5MHz as opposed to 1.538MHz at 0.5um and 500kHz at 0.7um. The Frequency-Technology factor quantizes the scaling as it pertains to both frequency and technology, where a larger number denotes a more agressive approach. At 1.75 Hz*m the modulators in this paper were designed much more agressively than the implementations from Peluso, Steyaert and Sansen that rate at 0.35 Hz*m and 0.769 Hz*m.

Power supply voltage is a very important factor in circuit operation. Lowering the supply voltage is the most effective technique in reducing power consumption where dividing the supply voltage by a factor of 2 will reduce the power consumption up to 4 times. Lowering the supply voltage also effects the circuit speed and more importantly transistor gain, which will hinder comparator performance where gain is extremely important. Furthermore, each technology targets a specific operating voltage for digital circuits, and it is unreasonable to assume operation at lower levels. Even if operating analog circuits at lower voltages saves power for those circuits, the additional circuits for power supply scaling and level-shifting required for the digital interface will consume more power than saved. For these reasons, the current draw becomes another important measure of power efficiency.

The final important difference is the allowed input voltage range. Most single loop modulator circuits saturate when the input is close to the rail voltages and many can only follow a voltage within a small range. This is particularly true of low power circuits and differential circuits where low gain and device limitations prevent operation at certain voltages or make operation too inaccurate. Although modulators with small input ranges can be created to detect very small voltage steps, the Effective Modulator resolution may be small if there are fewer detectable steps within the allowed voltage range. Comparably, modulators that operate rail-to-rail may have a high Effective Resolution, but will not be able to distinguish fine voltage steps over the entire range. This is an important difference to remember since the modulators presented in this paper target rail-to-rail operation and the designs from Peluso, Steyaert and Sansen are content with the limited voltage range.

Two more categories were added to facilitate comparison. Power consumption is directly proportional to sampling rate, and the higher frequency devices generally draw more current. Since the power consumption is compared for devices with different sampling rates, the ratio of power consumption to sampling rate is considered the most objective measure. Similarly the ratio of current drawn to the sampling rate gives the most objective measure of circuit efficiency. These two categories have been added to Table 5.4 for reader's reference.

CHAPTER 6: Conclusions

We investigated three different types of delta sigma modulators for low power analog-to-digital conversion: a First Order Self-Referenced modulator, a Second Order Self-Referenced modulator and a Band-Gap referenced Second Order Floating Gate modulator. Among the three modulators, the First-Order modulator has the smallest current and power ratios. It is the smallest circuit, and switches the smallest amount of charge. The drawback is that it can only produce a SNDR of 51.7dB, which can produce 8 bits of resolution at best, and even that is for a limited input range. This is much lower than the initial targe of a 10-bit resolution, leaving a tough task for the digital filter design.

The Self-Referenced modulator offers much better accuracy at 12 bits of resolution while consuming very little power at 17.3 uW/MSample. Another advantage of the second order Self-Referenced modulator is its consistent operation for rail-to-rail input voltages, from 0 to 3.3V while being able to distinguish steps of 0.8 mV. The main performance advantage of the Self-Referenced modulator is the low current requirement which is 4.43 uA/Msample. This achievement is owing to the circuit minimization efforts described in Chapter 3.

Another advantage lies in low system cost. The Self-Referenced modulator was designed in a standard digital silicon underlayer, and used exclusively internal components. This offers large cost and area savings as compared to traditional designs with cusom underlayer and predominantly external capacitors. In addition, systems with external components are extremely vulnerable to coupling noise combined with the effects of paracitic inductance on the external capacitors, solder connections, socket inductance and chip packaging. When considering a large mixed signal system, the Self-Referenced modulator is more fitting.

The Floating Gate modulator has a power rating at 55.2 uW/Msample as well as a 10 bit effective resolution. This, however, falls short of the expectations for this circuit. The addition of a Band-Gap reference and the Floating Gate comparator was a measure to increase system accuracy and noise immunity. The fact is that while the Floating Gate modulator may be more resistant to external noises, the floating gate itself becomes a source of non-linearities that limit the modulator

precision. The Floating Gate modulator is a practical solution for systems operating in very poor or noisy conditions, but when noise levels are moderate, the Self-Referenced design offers the best performance. This does not dismiss floating gate methodology for signal processing, but it does leave room for improvement in the area of noise suppression. If nothing else, the Floating Gate modulator was an innovative circuit that may open the door to new design possibilities.

It is a little surprising that the Self-Referenced modulator has shown to be the best architecture for a low power Delta Sigma modulator. Drawing a mere 26.2 uA of current, this modulator is capable of producing digital bit streams with 70.9 dB of SNDR, and offering digital resolution up to 12 bits.

This is a second order modulator carefully minimized to its bear essentials, and through this simlicity arises a great level of accuracy. In the process of systematic elimination of supporting circuitry, the number of stages that affect the input signal has been reduced, and that has served to minimize the system noise.

As a result of the design process, the Self-Referenced modulator architecture is compatible with any digital CMOS process including gate-array implementations. It offers a small footprint of $0.1mm^2$ which includes the filter capacitors and requires no further support circuitry.

The circuit was designed and verified using pre-defined digital underlayer with mediocre transistor sizing and switching parameters. It was unexpected to see this circuit perform so well compared to designs with more noise suppressing features.

6.1 Suggestions for Improvement

Finally, we suggest a few areas to improve the performance. This project was a search for low power low complexity analog to digital converter architecture. As a result, this research has concentrated on discrete time charge mode analog circuits. Several other techniques have been mensioned, but could not be explored within the scope of this thesis. Several of the mensioned techniques stand out, and deserve further exploration.

An important complement to a low power delta sigma modulator is a low power digital filter and signal processor. Several filter concepts were mensioned in this thesis, and they hint on some interesting possibilities. Thus there is a concept for a follow up paper to cover the digital aspect of delta sigma modulation.

Several concepts were presented from the analog point of view that deserve further investigation. Floating Gate circuits in particular deserve a closer look. Floating Gate technique is a gateway to low-voltage circuits, charge re-distribution and neural devices, all of which have favorable characteriscitcs for low power research.

A comprehensive study on noise shaping methods and effects would provide future mixed signal designers with a valuble reference. Presently there is a multitude of papers on Delta Sigma modulation that attempt to shape noise through increasing device orders and complexity, and most of them loose track of the undelying theories. Thus a good reference on this topic would be invaluble to the growing research interest in this field.

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VITAE

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