Power Line Communications in Microprocessors - System Level Study and Circuit Design

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(ABSTRACT)

Power line communications (PLC) as applied to electrical power grid is known since long; however, PLC in microprocessors was recently introduced by VTVT Lab. Since power distribution network (PDN) inside a microprocessor is ubiquitous, therefore, any node inside a microprocessor can be accessed by attaching a simple communication circuit to it. The scheme is extremely attractive as it avoids the routing overhead of the data-path between an internal node and an I/O pin. A number of applications are possible for PLC in microprocessors such as on-line testing, monitoring/control of internal nodes, fault diagnosis etc.

Feasibility of the PLC approach has been extensively studied by earlier researchers at VTVT. The feasibility studies investigated the frequency response of a microprocessor's PDN and looked for existence of passbands – frequency bands where signal attenuation through the PDN is small. Two different approaches were followed – the first approach employed analytical modeling of the high frequency characteristics of the PDN, while the second approach conducted measurements on Intel® microprocessors' PDN. Although, differences were observed in the results of the two approaches; both the approaches demonstrated existence of passbands, thus affirming the feasibility of the PLC scheme.

This thesis presents a system level study conducted to estimate performance of the PLC scheme. Measurement results were used to model the PDN channel. The study provides useful insights for the design of microprocessor level PLC system. Specifically, the study estimates optimal pulse width required to maximize the system performance and the range of achievable data-rates. The study demonstrates that it is feasible to communicate data through a microprocessor's PDN without inducing large disturbances on the power line.

The other work presented in this thesis is the design of low power receiver for microprocessor

level PLC, also called data recovery block. The proposed design of data recovery block employs Correlation Detection (CD) receiver architecture. The design has been implemented in IBM 0.13 μm CMOS process and has been verified to operate reliably across Process, Voltage and Temperature variations. The design has a small foot-print of 300 μm x 160 μm and consumes 3.58 mW while operating from 1.2 V power supply.

To my parents
for their patience in seeing me work through my graduate studies
for their unquestioned support and trust.

"Mom and Dad with this I am finally going to graduate"

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Chapter 1

Introduction

1.1 Motivation

Silicon process technology scaling is pushing the limits of integration in today's state of the art microprocessors. For example, Dual Core Intel® Itanium 2 processor chip carries as many as 1.72 billion transistors [1]. An important constraint on the level of integration comes from the microprocessor package, due to limiting factors like provision of stable power supply at high current consumption, I/O pin count, thermal heat removal etc. Restricted number of I/O pins in a microprocessor package poses a major challenge to microprocessor system designers, who aim to integrate increasingly larger number of functions in a chip. The challenge is exacerbated by the associated routing overhead in the chip.

A need is being felt to incorporate mechanisms into state-of-the-art microprocessors to predict/detect occurring system failure, recover system state and possibly repair the system [2]. This need is accentuated by two main factors, firstly, increasing system complexity and secondly, decreasing reliability of CMOS in deep sub-micron silicon technology. Thus, future microprocessors are going to integrate more and more sensors and controls to ensure reliable operation. Routing data from these sensor and control units is going to pose a major design overhead.

Power distribution network (PDN) is ubiquitous inside a chip; therefore, PDN can be used to reach any node in a chip. Thus, the idea of communicating data through PDN, while simultaneously delivering power, is highly attractive. Data communication over a microprocessors PDN can avoid the routing overhead of integrating sensing/control nodes, thus,

providing flexibility in their placement in the chip. The ability to communicate with internal nodes without routing data paths opens up a possibility for fault diagnosis, monitoring transient logic values during built-in self test and for on-line/off-line testing.

1.2 Power Line Communications in Microprocessors

The use of power lines in an IC environment for data communication was introduced by VTVT Lab in [3], [4]. Specifically, Impulse Ultra wideband (I-UWB) modulation scheme has been proposed as the modulation scheme of choice because of its associated merits for the proposed Power Line Communication (PLC) scheme [5], [6]. The proposed scheme achieves communication between multiple nodes integrated inside a microprocessor chip and an external monitor/control module through the microprocessor PDN. Each node inside the chip has pre-assigned IDs, which can be used by the external module to address and send data to a particular node. Communication between the internal nodes and the external module can be either unidirectional (from off-chip to on-chip) or bidirectional, depending upon the application requirement. In case of uni-directional communication, only receivers (also called data recovery blocks) are integrated on-chip, whereas in case of bi-directional communication both data recovery blocks and I-UWB transmitters are integrated on-chip. The proposed microprocessor level PLC scheme is illustrated in Figure 1.1. The figure shows the communication path between the external module going through the system board, socket pins, through the package power planes and finally entering the chip through power/ground bumps. The inset in the picture shows multiple transceivers (node ID # 1, 2) or receiver only (node ID # 3) nodes connected to the on-chip PDN, which is depicted as a mesh.

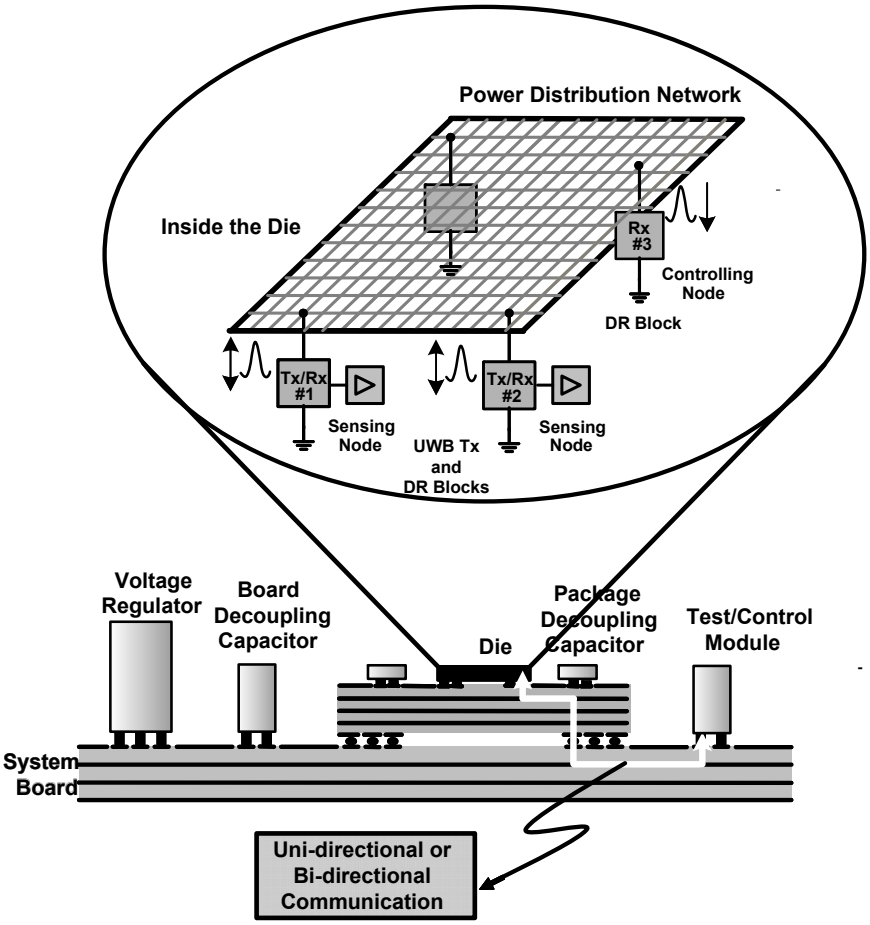

Figure 1.1: Power line communication in microprocessor environment.

1.3 Contributions of this thesis

VTVT lab has been engaged in investigating the feasibility of the proposed power line communication scheme. The research work was supported and funded by Intel Corporation and Semiconductor Research Corporation (SRC). Main goals of the research work were:

- Feasibility study through modeling of a microprocessor's PDN.
- Validation of modeling results and feasibility study through actual measurements on Intel microprocessors' PDNs.
- Measurement of noise in Intel microprocessor's power line.
- Modeling of PDN as a communication channel.

- ✓ Study of I-UWB pulse propagation through PDN channel.
- ✓ Design of a low power and reliable data recovery block circuit for power line communications at chip level.
- ✓ Integration of data recovery block circuit in an Intel microprocessor test run.

The research goals listed with bulleted dots were pursued by two earlier PhD students, who have graduated from VTVT Lab. In this thesis, the results of prior investigations were followed up and the remainder of the research goals listed with bulleted ticks were accomplished.

A system level modeling was conducted in MATLAB to study the propagation of UWB impulses through Intel microprocessor's PDN. The study was conducted using PDN channel models developed from measurements conducted on two generations of Intel microprocessors, namely, 65 nm Intel® Pentium 4 and 45 nm Intel® Core 2 Duo. The study demonstrated feasibility of UWB communication over a microprocessor's power line without disturbing its integrity. The study is discussed in detail in Chapter 4.

Other contribution of this work is the design of a data recovery block circuit for power line communications in microprocessor. The data recovery block is essentially an Impulse-UWB receiver which can detect UWB impulses from its power line. Implementation of data recovery block is challenging because of small area and low power constraints. The design was done in TSMC 0.18 μm CMOS process and the results were published in [36]. The project aimed to finally integrate data recovery block in Intel microprocessor test run, however, because of limited availability of on-site work opportunities at Intel, test run integration was deemed infeasible. Therefore, a stand-alone test-chip was fabricated through MOSIS in IBM 0.13 μm CMOS process. The design and the test chip results are discussed in Chapter 5.

Results of the work done in this thesis have also been reported in various project deliverable reports submitted to SRC. Subsequently, the project has been successfully completed, earlier this year.

1.4 Thesis Organization

The organization of this thesis is as follows; chapter 2 discusses the necessary preliminaries in

regards to the thesis research work. Some theoretical background of UWB communication and its advantages for the proposed scheme are discussed, which is followed by a brief overview of modulation schemes applicable to Impulse-UWB. Next, Direct Sequence Spread Spectrum (DSSS) coding scheme, as applied to Impulse-UWB communication is discussed. Finally, the structure of PDN of a microprocessor is overviewed.

Chapter 3 briefly covers the investigations on PLC in microprocessors, conducted by earlier graduate of VTVT Lab. Feasibility studies conducted through PDN modeling and measurements are presented in this chapter. The focus of these studies was to characterize frequency transfer characteristics of a microprocessor's PDN and to investigate existence of passbands at high frequencies. Both the feasibility studies, the one based on PDN models and the other based on actual measurements, demonstrated existence of passbands in the frequency response of a microprocessor's PDN. However, it was shown that PDN frequency response derived from PDN model developed at VTVT lab differed widely from measurements. These differences are reasoned towards the end of Chapter 3. Subsequently, the results from measurements are used in the following work to model PDN channel in the system level study, covered in chapter 4.

Chapter 5 presents circuit design for data recovery block. Challenges in implementation of data recovery block are discussed. Simulation results from implementation of the proposed design in TSMC 0.18 μm CMOS process are presented. The design is also ported to IBM 0.13 μm CMOS process, for fabrication through MOSIS. The test-chip micrograph is provided and the fabrication results are covered in the later part in the chapter.

Lastly, chapter 6 concludes the work presented in this thesis. A set of possible application of the proposed PLC scheme are discussed. The proposed communication scheme is extremely attractive for distributed sensing and control, which is going to become an integral part of the future microprocessors. The chapter ends by highlighting the directions for future research in this field.

Chapter 2

Preliminaries

Power line communications in microprocessors brings together a variety of electrical engineering topics, namely, digital communications, Ultra Wideband (UWB) modulation, spread-spectrum communications, PDN of microprocessors and RF/analog circuit design. This chapter briefly covers relevant background information on UWB modulation, providing overview of UWB signaling and discussing advantages of UWB scheme for the PLC application. The chapter also briefly covers DSSS modulation scheme, as applied to Impulse-UWB. Lastly, the chapter overviews structure of a microprocessor's PDN. Hierarchy of the PDN is described, providing information about various components at each level. Placement of decoupling capacitors, used for PDN impedance control and for reducing supply voltage fluctuations, is also discussed.

2.1 UWB

2.1.1 Definition

In general, a modulation scheme is called UWB modulation if the information bandwidth is 20% of carrier frequency or the absolute bandwidth is at least 500 MHz [8], [9]. A qualitative comparison of the power spectral density of narrowband, wideband and ultra wideband modulation schemes is shown in Figure 2.1.

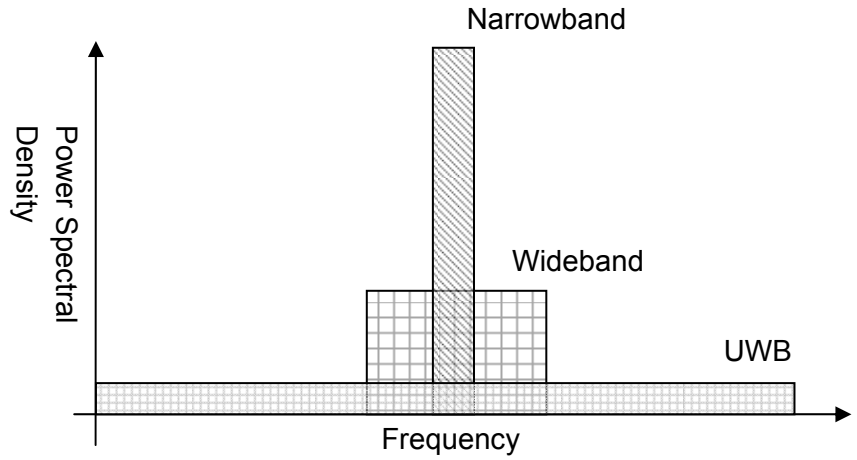

Figure 2.1: Power spectral density of UWB, wideband and narrowband modulation.

Federal Communications Commission (FCC) limits the operating bands and spectral emission of a UWB device according to its application. Licensed UWB band operations include applications such as health monitoring, ground penetrating radar and through-walls sensing. Unlicensed operations are allowed for certified UWB communications devices, which operate in the band from 3100 MHz to 10600 MHz. UWB spectral emission mask for unlicensed operation is shown in Figure 2.2.

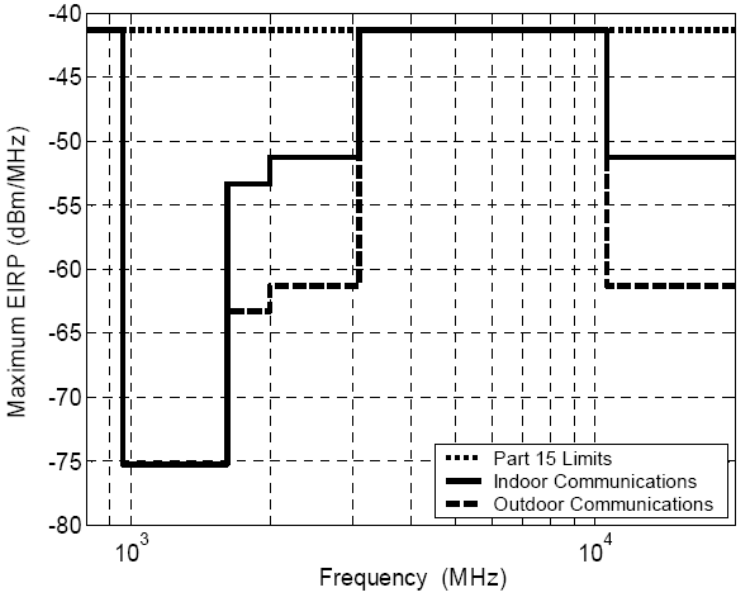

Figure 2.2: UWB Spectral Emission Mask.

2.1.2 UWB Signaling

UWB signaling can be either carrier-based or impulse-based. Impulse-UWB is based on a train of narrow pulses (which are typically a few hundreds of picoseconds to a few nanoseconds wide). Direct Sequence UWB (DS-UWB) is an example of Impulse-UWB modulation scheme, which has been standardized as an optional PHY for Wireless Personal Area Network (IEEE 802.15.4a) [10]. Carrier based UWB modulation involves divison of UWB frequency band into multiple narrow-bands and transmitting separate narrowband modulated signals in each band. An example of such a multi-carrier UWB modulation is Multi-Band Orthogonal Frequency Division Multiplexing (MB-OFDM).

Impulse based UWB is more suitable for the proposed application due to the advantages discussed later in this chapter. The most popular pulse shapes used for impulse UWB are Gaussian pulses and their derivatives [11]. Various modulation schemes such as On-Off Keying (OOK), Pulse Amplitude Modulation (PAM), Pulse Position Modulation (PPM) and Binary Phase Shift Keying (BPSK) are available for Impulse-UWB. Order of a modulation scheme adds another degree of freedom in the system design. For example, 2-PPM and 4-PPM are shown in Figure 2.3. The choice of modulation scheme is governed by application requirements such as required data rate, channel noise characteristics, regulatory requirements, hardware complexity and Bit Error Rate (BER).

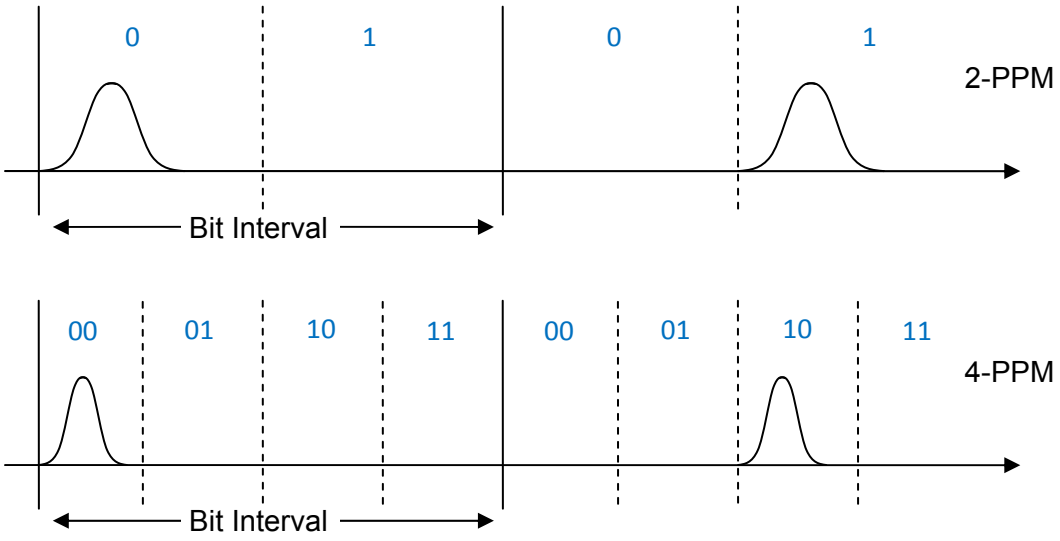

Figure 2.3: Example of order of a modulation scheme – 2-PPM and 4-PPM.

2.1.3 Advantages of UWB

Compared to narrowband communication, UWB has several advantages such as high data rate, low average power and simple RF circuitry. Shannon's theorem states that the channel capacity C is given as B*log2(1+SNR) [12], where B is the bandwidth and SNR is the signal-to-noise ratio. Since the bandwidth of a UWB signal is much larger (on the order of several GHz) than a narrowband signal, the SNR required to achieve the same data rate can be much smaller for UWB. Therefore, with UWB communications one can often recover data, even if the signal power is close to the noise level. In other words, the power level of UWB signals can be at the noise level of power lines to have little impact on the power line integrity. This is especially important for microprocessor level PLC system because of the extremely low (0.8 - 2.5 V) power supply voltage.

Specifically, Impulse-UWB has several advantages for the proposed applications. Impulse-UWB is relatively immune to multipath fading because different multipath can be resolved and combined together by employing a RAKE receiver [11]. This property is useful in microprocessor level PLC because of existense of strong multipath components due to signal reflections from a large number of discontinuities in a PDN. Lastly, the carrierless nature of Impulse-UWB favors simpler and lower power consuming hardware implmentation of receivers and transmitters. Further, Impulse-UWB transmitters can have nearly all-digital implmentation using CMOS process technology [13], [14]; this is important for integration in microprocessors ICs.

2.2 Direct Sequence Spread Spectrum

In DSSS modulation 'n' bits are transmitted for each data bit, where 'n' is called the Spreading Factor. The transmitted bits, also called Chips, are determined by the input data bit and a code sequence. The code sequence is a pseudo random sequence of bits of length $L \geq n$. For example, for a spreading factor of n = 4 and a code of the same length L = 4, given by {-1, 1 ,1, -1}, the output chips corresponding to an input data bit of '1' is given by {-1, 1, 1, -1}, while for data bit '0' the output chip sequence is {1, -1, -1, 1}, where each chip in the sequence has been inverted. Such a scheme when applied to Impulse-UWB with BPSK modulation implies sending a

positive-going impulse for a chip value of '1' and a negative-going impulse for a chip value of '-1'. This spreading operation is further illustrated in Figure 2.4.

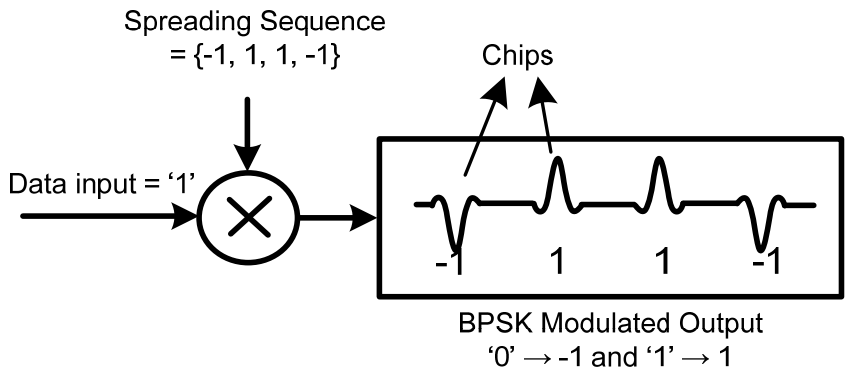

Figure 2.4: BPSK modulation with Direct Sequence Spread Spectrum, as applied to UWB.

Benefit of DSSS for the proposed application is processing gain, which is given by *10*log(Spreading Factor)*. Thus, for a spreading factor of 4, processing gain = 6 dB. Ideally, this implies that the transmitted signal power can be reduced by 6 dB, while maintaining the same SNR at the receiver; however, the actual gain is generally lower. Another advantage of DSSS is that it suppresses narrow-band interferers by the same factor as processing gain. This property is useful for PLC in microprocessor because of the presence of narrow-band noise in microprocessor's noise spectrum [29].

2.3 Structure of a Microprocessor's PDN

PDN of a microprocessor consists of three levels of hierarchy. At the first level of hierarchy is a mesh type chip level PDN; the second level is the package level power distribution planes and power/ground pins and finally, the system board level power distribution network, which connects to external power supply through a Voltage Regulator Module (VRM) forms the third level. The structure of a microprocessor's PDN is depicted in Figure 2.5.

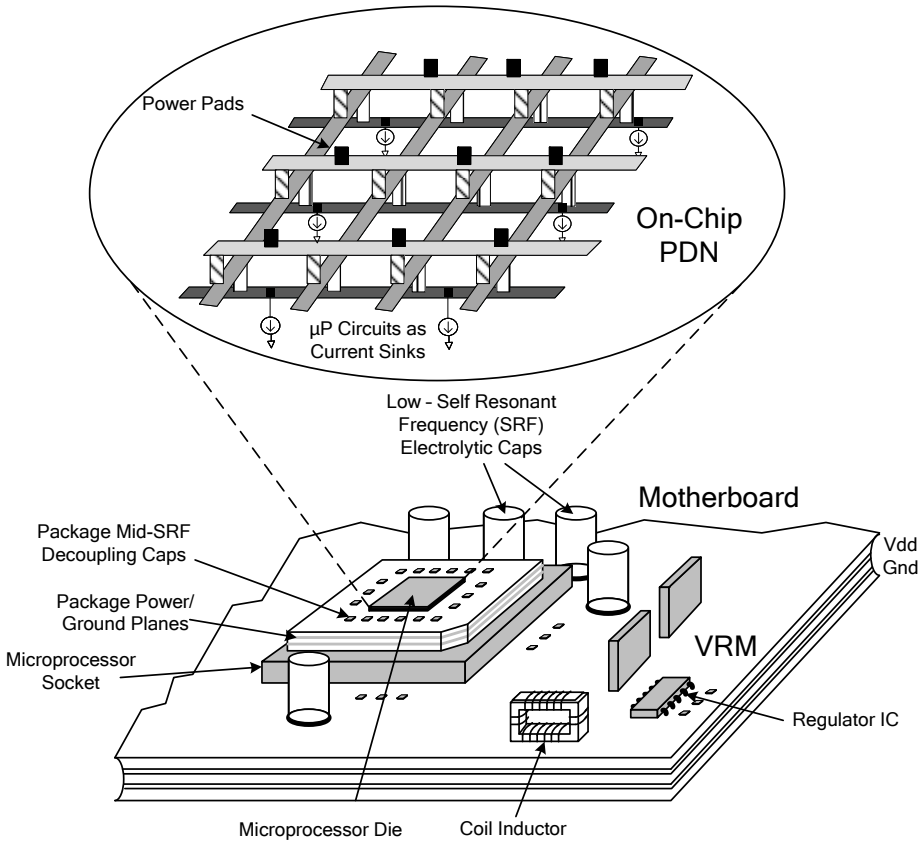

Figure 2.5: Structure of a microprocessor's power distribution network.

The PDN is responsible for providing a stable power supply to the microprocessor. However, in today's fast switching and power hungry microprocessors, it is a challenge to meet the design goal of providing a stable power supply. The switching activity of microprocessor circuits causes both fast, as well as slow fluctuations in the current consumption. These fluctuations in current consumption result in power supply voltage to droop and shoot above the desired voltage, leading to what is called as simultaneous switching noise (SSN) as shown in Figure 2.6. These voltage fluctuations occur due to three main electrical effects, namely, IR voltage drop, inductive Ldi/dt fluctuations and capacitive and inductive coupling with signal traces. These effects come into play due to parasitics of the components in the PDN and the distributed effects of the PDN at high frequencies. A careful design of the PDN is required to minimize power supply voltage overshoot and droop. It is pertinent to take a brief look at the structure of a microprocessor's PDN, both for understanding the causes of voltage fluctuations and for studying the feasibility of

PLC in microprocessors.

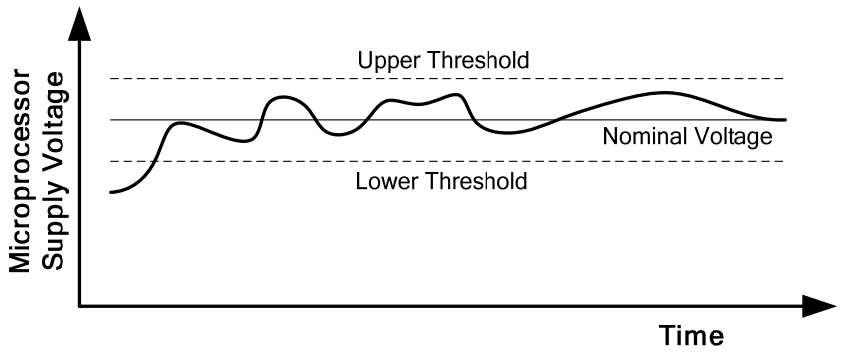

Figure 2.6: Microprocessor supply voltage variation – simultaneous switching noise.

2.3.1 System-Board Level PDN

Components of board level PDN of a microprocessor are voltage regulators, decoupling capacitors and power/ground planes. Voltage regulators are designed to supply high currents (as high as 100 A or more) at a low output voltage in the range of 0.8 - 2.5 V [15]. Moreover, the power supply voltage needs to be regulated within a very strict voltage margin of ±5%. Due to the high supply current requirement and low output voltage fluctuation margin, the voltage regulator needs to have very low output impedance, in the range of a few mΩ. This is achieved by using feedback. However, the output impedance cannot be maintained low as frequency increases because the feedback gain decreases as the frequency increases. Therefore, decoupling capacitors are added to supply currents during the response time interval of the voltage regulator. However, parasitics of decoupling capacitors, namely, Effective Series Resistance (ESR) and Effective Series Inductance (ESL), as shown in Figure 2.7 (a), render them ineffective at higher frequencies. As shown in Fig. 2.7 (b), impedance of decoupling capacitor becomes inductive after a frequency called Self Resonance Frequency (SRF). In a computer system, multiple groups of parallel decoupling capacitors are added. These groups of parallel capacitors are arranged such that the group with higher SRF and lower total capacitance is placed closer to the microprocessor. Lastly, there are multiple power and ground planes in the computer system board which interconnect VRM, decoupling capacitors and package power pin.

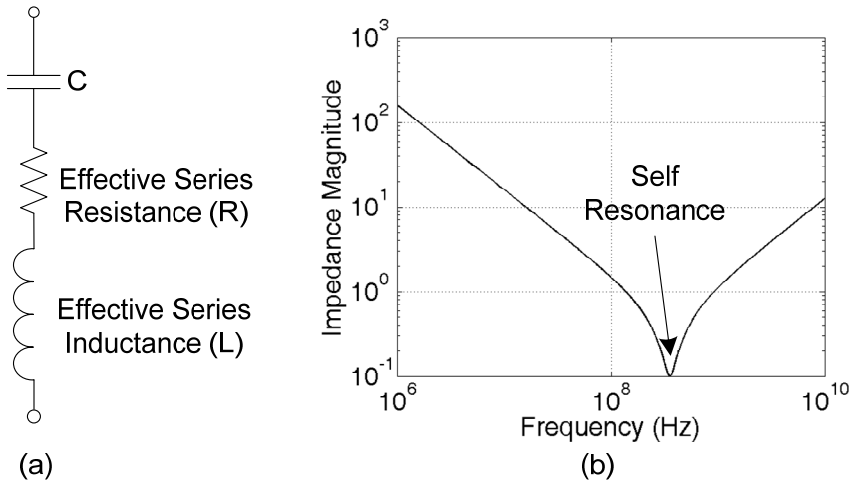

Figure 2.7: (a) Decoupling capacitor model. (b) Self resonance in decoupling capacitor.

2.3.2 Package Level PDN

PDN at package level consists of package power planes and package level decoupling capacitors. Ceramic capacitors are used as package decoupling capacitors because of their high SRF. Embedded decoupling capacitors are also being investigated for decoupling at even higher frequencies [16]. The package level power/ground planes provide interconnection between power/ground pads of the microprocessor IC and power/ground planes of the system board. Connections to power/ground pads of microprocessor IC is either through C4 bumps, as in a flip-chip package, or through bondwires, as in a wire-bond package. Similarly, connections to the system board level power planes are made through either pins or balls or lands, depending upon the type of I/Os used in a package. For example, in state-of-the-art Intel® Core2 Duo microprocessor, Flip-Chip Land Grid Array package with 775 I/O lands is used. Out of these 775 lands, 226 lands are dedicated for power connects and 274 lands are dedicated for ground connects.

2.3.3 On-chip PDN

On-chip PDN consists of a grid of supply and ground routings and on-chip decoupling capacitors. The power/gound routings are arranged in a multilayer mesh type structure forming

the power distribution grid. A diagrammatic representation of the power grid is shown in the inset in Figure 2.5. In the figure on-chip active circuits have been shown as current sources sinking current from the power grid. Technology scaling is making design of on-chip power grid more and more difficult. Higher integration densities, faster devices and reducing supply voltage are leading to circuits requiring higher and faster switching currents and reduced noise margins. Also, leakage currents are becoming comparable or greater than active switching current for 90 nm silicon technologies and beyond [17], making IR voltage drop a major concern in the design of on-chip power grid. To counter these design challenges, new approaches for power grid design are being adopted. One of them is the division of on-chip power grid into voltage domain, called voltage islands [18]. In this scheme, the circuits with lower performance requirements are powered from lower supply voltage, in order to limit their leakage power.

For on-chip decoupling, capacitance is formed between the n-well and polysilicon gate of a MOSFET. This capacitance is also called MOScap. These decoupling capacitors are placed in-between the on-chip circuit blocks. This space between the circuit blocks is often referred to as "white" space. These days, use of more than 10% of overall die area for on-chip decoupling capacitors is quite common in high-performance integrated circuits [19]. Besides, this intentionally added decoupling caps; power supply decoupling is further enhanced by the parasitic capacitance of the on-chip CMOS circuits.

Overall, the PDN of a microprocessor system forms a complicated structure. The function of this structure is to supply large currents to a microprocessor IC at a low voltage and with very small voltage fluctuation margin.

2.4 Chapter summary

This chapter covered theoretical background information on three different topics, relevant to the presented research work in this thesis.

In section 2.1, definition of UWB was discussed, followed by an overview of FCC regulations on UWB spectral emissions. The section also covered modulation schemes applicable to UWB and lastly, advantages of UWB communication for the proposed application were discussed.

In section 2.2, a brief overview of DSSS communication, as applied to Impulse UWB, was given. Impact of DSSS on effective SNR of the received signal and narrowband interference suppression was also discussed.

Lastly, section 2.3 described the complicated structure of a microprocessor's PDN. The three tier hierarchy of the PDN was discussed, which consists of System board level PDN, package level PDN and on-chip PDN. The requirement of decoupling to control the impedance of PDN at high frequency and to reduce SSN in a microprocessor power line was highlighted. Also, the placement of these decoupling capacitors at each of the PDN levels was covered.

Chapter 3

Feasibility Study

A bi-pronged approach for determining the feasibility of the microprocessor level PLC scheme was adopted. The first approach was to develop high-frequency models of the PDN of a microprocessor and study the frequency response of the PDN thus obtained. This approach has been presented in the first part of the chapter. The other approach was to measure frequency characteristics of an actual microprocessor's PDN. Undertaking these measurements was not straight-forward due to practical issues involved, as explained later in this chapter. The second approach, supposed to verify the results of analytical approach, showed complete divergence from the analytical models. However, the measurements still supported feasibility of the PLC scheme, which has also been verified through system level modeling, presented in the next chapter.

3.1 Feasibility Study Using PDN Models

This section elaborates the approach followed for modeling the PDN. Specifically, models for each individual components of PDN are described. Finally, these models are combined together to study the frequency response of a generic microprocessor's PDN. Based upon the microprocessor level PLC scheme, illustrated in Figure 1.1, the communication path goes through microprocessor socket pins, package power and ground pin, package planes, chip I/O (C4 bumps and solder balls) and finally to IC level power grid. The following sub-sections discuss models employed for each of these PDN components.

3.1.1 Model for Power/Ground Pins of a Socket or a Package

The socket and package power and ground pins can be modeled with good accuracy using a series lumped resistor and inductor model [20]. Due to the presence of a large number of power and ground pins, supplying and sinking currents in parallel, the effective resistance and inductance of package pins is quite low. The effective inductance is less than a few pH and the effective resistance is less than a mΩ. This small inductance is inconsequential, considering the inductance of package power and ground planes and hence is neglected in order to simplify the analysis of the PDN [21]. Moreover, the resistance of socket/package pins is an important concern only while considering IR voltage drop. However, it can also be neglected in our analysis, where the signal power involved is small.

3.1.2 Package Plane Model

It has been indicated that the use of lumped element models for modeling PDN components, especially for package power planes, is unable to capture PDN frequency characteristics accurately at frequencies above 1 GHz [22]. At GHz frequencies wave propagation and edge effects from power distribution planes becomes a dominant factor impacting frequency characteristics of PDNs. Numerical methods can be applied to analyze such structures [23], however, using such techniques to construct broadband models valid up to GHz of frequency range becomes computationally very intensive. In [22], physics based model called Cavity Resonator Model has been proposed for modeling power planes. Power planes are considered as a resonant cavity connected to electrical ports located arbitrarily on the planes and are characterized by a modal N-port impedance (Z) matrix. Figure 3.1 illustrates the CRM model. The figure shows two power planes with 2 ports i and j being modeled with a 2-port impedance (Z) matrix. The model has been shown to be computationally efficient and accurate for high frequency modeling of power planes [21].

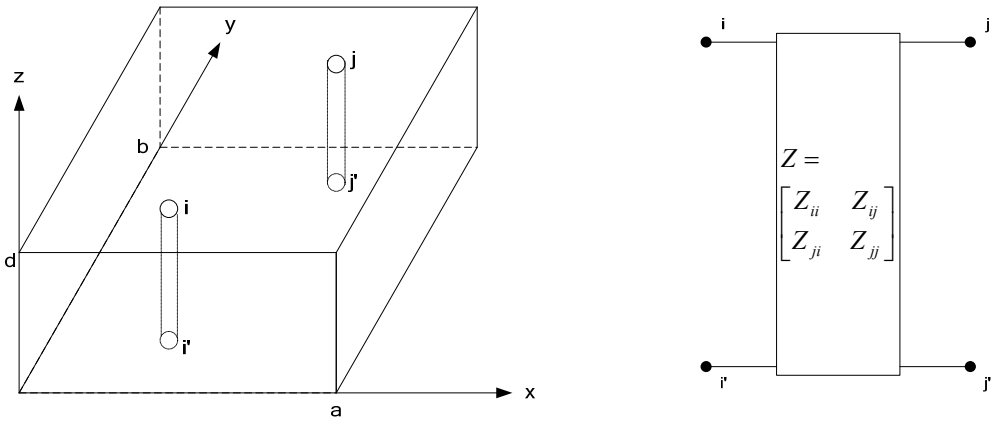

Figure 3.1: Two parallel planes with ports i and j, modeled by Z-impedance matrix using Cavity Resonator Model.

Impedance characteristics for a single plain pair, with ports i,j defined as shown in Figure 3.2, is given as below;

$$Z_{ij}(\omega) = \sum_{n=0}^{\infty}\sum_{m=0}^{\infty} \frac{N_{mni} N_{mnj}}{1/\, j\omega L_{mn} + j\omega C_{mn} + G_{mn}} \qquad \ldots(1)$$

where,

$$L_{mn} = d/\left(\omega_{mn}^2 ab\varepsilon\right),\ C_{mn} = ab\varepsilon/d,$$

$$G_{mn} = \left(ab\varepsilon/d\right)\omega_{mn}\left(\tan\delta + \left(\sqrt{2/\omega_{mn}\mu\sigma}\right)/d\right)$$

$$N_{mni} = \varepsilon_m \varepsilon_n \cos\left(\frac{m\pi x_i}{a}\right)\sin c\left(\frac{m\pi t_{xi}}{2a}\right)\cos\left(\frac{n\pi y_i}{b}\right)\sin c\left(\frac{n\pi t_{yi}}{2b}\right)$$

The impedance equation is based upon the assumptions that a, b >> d and d << λ (wavelength), where a x b are the dimensions of the power planes and d is the distance between them. m and n are the propagating modes. δ is the dielectric loss angle, and ε_m and ε_n = 1 for m, n = 0 and $\sqrt{2}$ otherwise. (x_i, y_i) and (x_j, y_j) are the coordinates of the port locations and (t_{xi}, t_{yi}) and (t_{xj}, t_{yj}) are the dimensions of port i and j. $\omega_{mn} = 2\pi f_{mn}$, where f_{mn} is the resonant frequency of each mode.

The spice equivalent circuit based upon CRM model of two power planes with N arbitrarily located ports is shown in Figure 3.2.

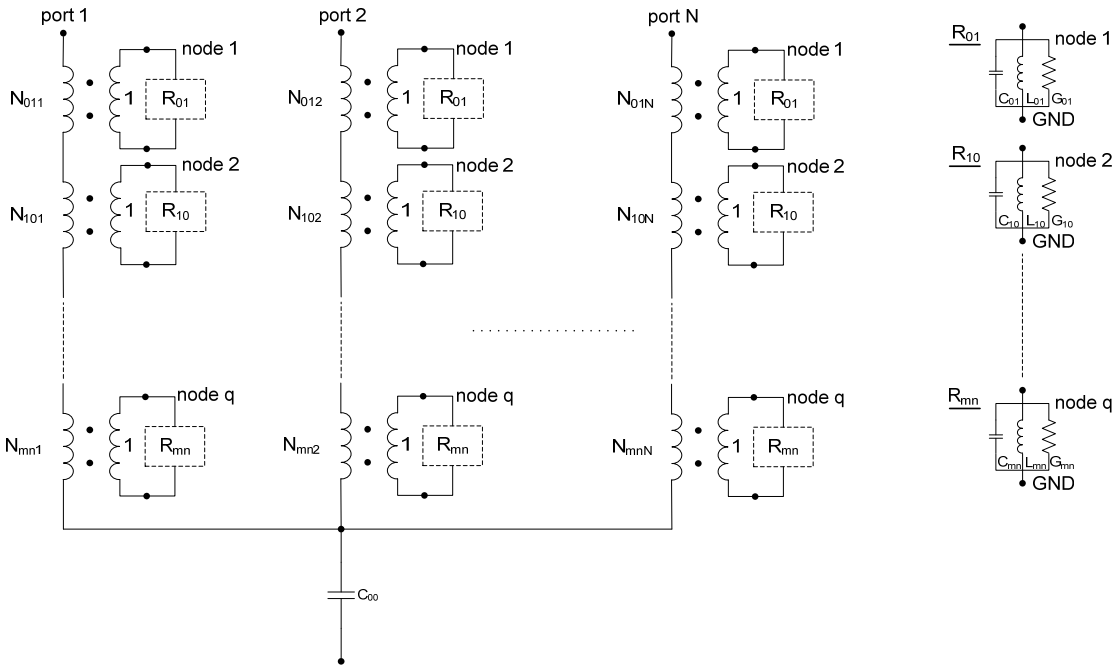

Figure 3.2: N-port SPICE circuit of two parallel planes based on Cavity Resonator Model.

3.1.3 Solder Ball and C4 Bump Models

Solder balls and C4 bumps can be accurately modeled using lumped elements because of their small sizes. A series resistor with an inductor models solder balls or C4 bumps accurately [20]. Due to small size of solder balls and C4 bumps, their parasitic inductance and resistance is quite small, even smaller than those of package/socket pins. Moreover, effective parasitic impedance of power and ground bumps is further reduced due to the use of a large number of power and ground bumps in a microprocessor die. Based upon the reasoning given in section 3.1.1, the parasitic of solder balls and C4 bumps are neglected in our analysis.

3.1.4 IC Level Power Grid Model

In order to estimate the delay and attenuation at various locations in a microprocessor chip, a distributed model of the on-chip power grid is required. A simple and widely used distributed RLC model is employed in our analysis. In the distributed RLC model, the die area is divided

into a grid of cells. Each cell is then reduced to a simplified RLC macromodel. These macromodels combine together to form a RLC grid model of the on-chip power grid, as shown in Figure 3.3. RLC extraction for each macrocell is carried out using the procedure explained in the following paragraphs.

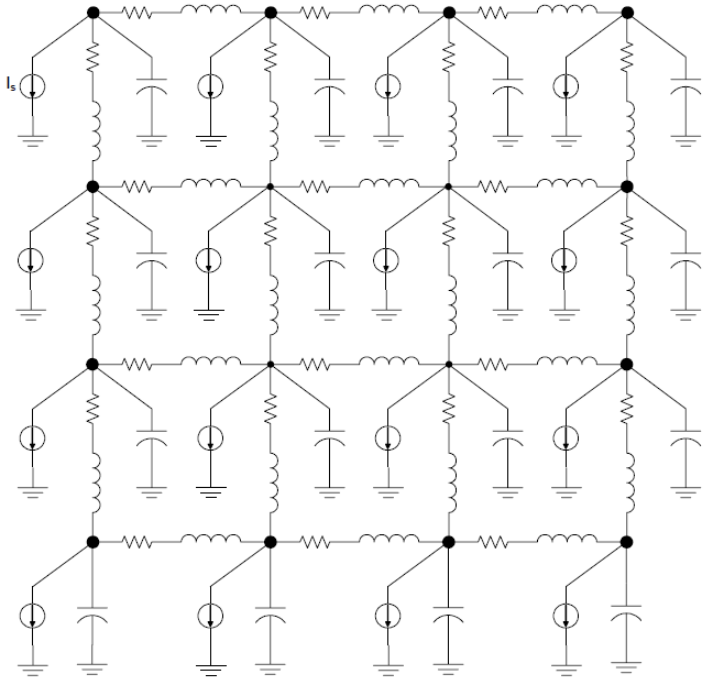

Figure 3.3: A 3-stage π-type distributed RLC model for on-chip power distribution network.

Resistive component of a metal wire can be calculated using the formula given in equation (2), where the metal trace length depends upon the macrocell size. Metal trace width calculation involves an iterative procedure [24], [25]. The goal of this iterative procedure is to estimate the minimum number of power pads, their placement and the minimum width for power trace routings, in order to reduce the IR voltage drop at any location in the die. Final IR voltage drop at any location in the die should lie within the design specifications.

$$R = R_s\left(l/w\right) \qquad \ldots(2)$$

where,

l = conductor length,

w = conductor width and

R_s = sheet resistance.

Estimation of parasitic inductance of a macrocell is difficult because of its dependence on the return current flow path, which can vary depending upon neighboring conductors. A simplified formula used in our analysis, which calculates the inductance of a conductor on the silicon substrate under the assumption of negligible thickness of the conductor and w < h, is given in equation (3).

$$L = \frac{\mu}{2\pi} \ln\left(\frac{8\mathrm{h}}{\mathrm{w}} + \frac{w}{4h}\right) \qquad \ldots(3)$$

where,

μ = permeability,

h = thickness of the substrate and

w = width of the conductor [26].

Calculation of capacitive parasitic of a metal trace is complicated because of its dependence upon neighboring conductors and fringing effect. An empirical formula that is computationally efficient with reasonable accuracy [27] is given in equation (4) and has been used in our analysis.

$$C = \varepsilon\left[\left(\frac{w}{h}\right) + 0.77 + 1.06\left(\frac{w}{h}\right)^{0.25} + 1.06\left(\frac{t}{h}\right)^{0.5}\right] \qquad \ldots(4)$$

where,

ε = permittivity,

w = conductor width,

h = conductor height, and

t = conductor thickness.

3.1.5 Case-Study: Modeling PDN of a Microprocessor Die Packaged in a FC-PGA Package

Models of various PDN components, described in previous sub-sections, were combined together and used to model the PDN of a microprocessor die packed in Flip Chip Pin Grid Array Package (FC-PGA) package. The design parameters, such as chip dimension, number of power pins (or balls), package were selected for constructing a generic integrated circuit whose specifications are comparable to a high performance microprocessor. The selection was carefully done in order to avoid landing-up with an extremely huge netlist which will be hard to simulate using the university compute resources. The design parameters are enlisted below:

Package model parameters:

- Package dimension: 20 mm × 20 mm.
- Number of pins: 400.
- Number of power pins: 100.
- Number of ground pins: 100.
- Number of signal pins: 200.

PDN model parameters:

- Chip dimension: 10 mm × 10 mm (More accurately, 9999.96 μm × 9999.96 μm).
- Number of power cross points: 100 (10 and 10 wires in M4 and M5, respectively).
- Metals for power bus: M4 and M5.
- Sheet resistance for M5: R = 0.04 Ω/sq.
- Sheet resistance for M4: R = 0.07 Ω/sq.
- Via resistance (Rvia) for the interconnection between M4 and M5 = 8.68 Ω.

The necessary parameters for RLC parasitic computation were extracted from TSMC 0.25 um process technology. Also, FR4 was assumed as the material used in the package substrate. Note that we have modeled only power mesh of the on-chip power grid because we are interested in analyzing signal propagation through the power line. Figure 3.4 illustrates the simulation setup.

The point of application of UWB impulse through the package pin (P1) is highlighted in the figure. Also, the point of reception of the impulse inside the chip (P2) is indicated. It is assumed that the receivers of microprocessor level PLC can be placed close to the chip power pads, therefore P2 is placed at location n1v1 marked on the distributed RLC model of on-chip PDN.

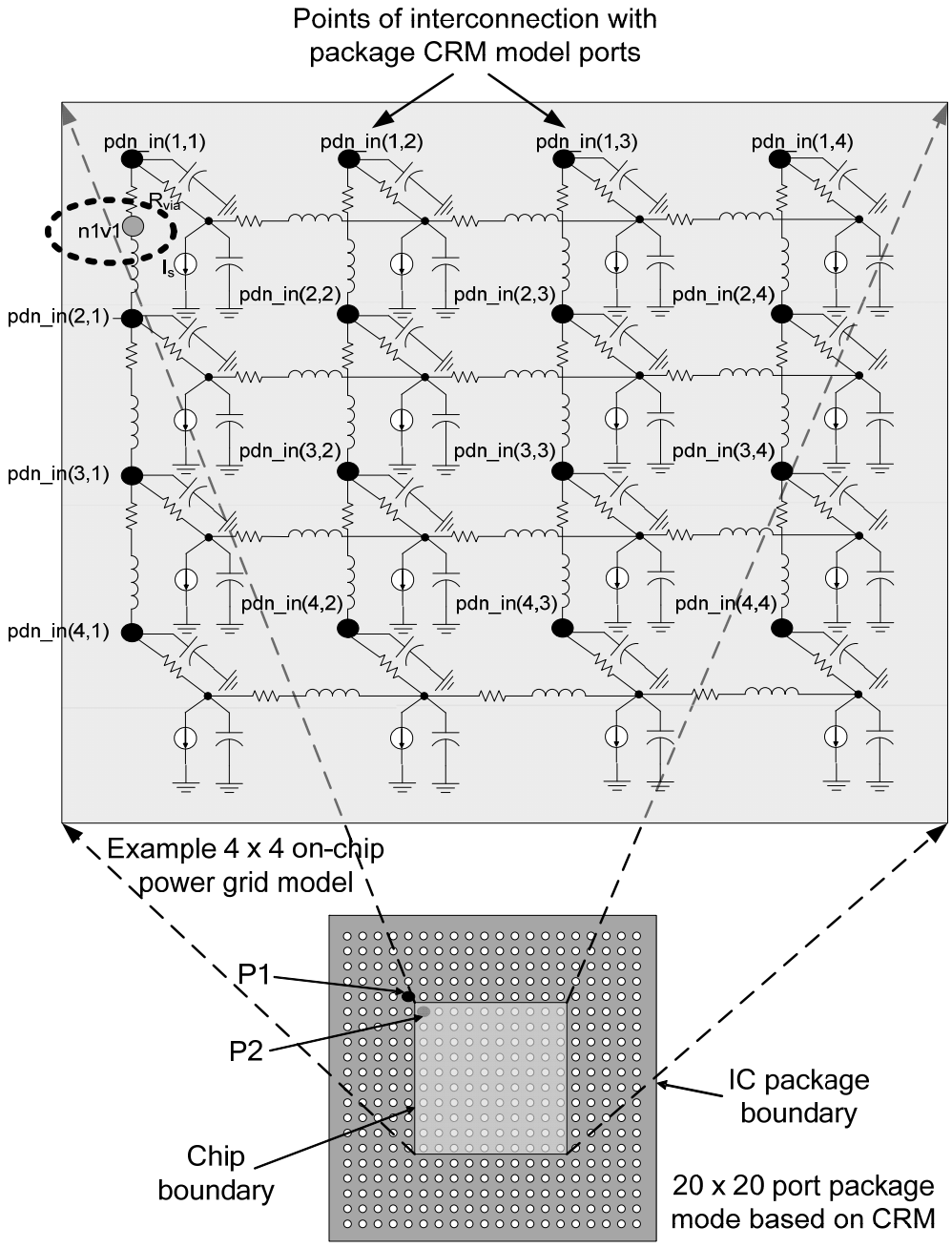

Figure 3.4: Simulation setup for PDN considered in the case study.

The simulation results showing frequency response of the signal path from P1 to P2 is shown in Figure 3.5. From the transfer characteristics, it is evident that passbands exist where signal attenuation is quite low. Specifically, there are passbands in the 1.6 GHz to 1.8 GHz, 4 GHz to 4.5 GHz and 5.2 GHz to 5.8 GHz frequency band. Existence of these passbands is a promising result for feasibility of PLC through a microprocessor's PDN.

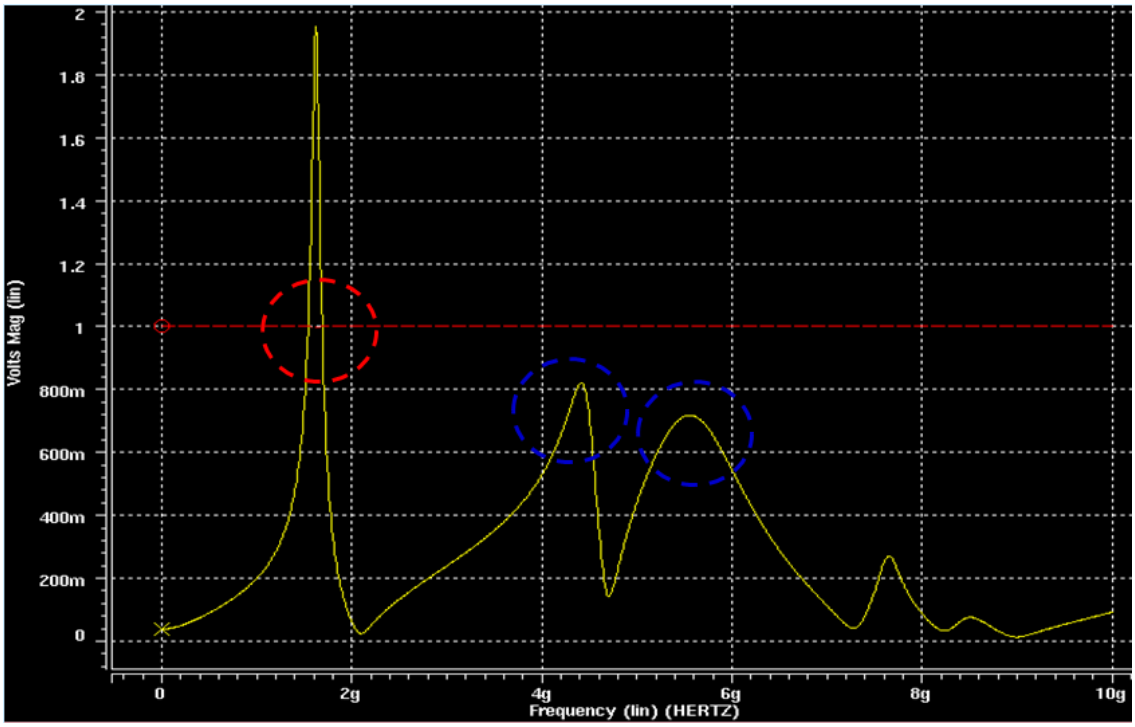

Figure 3.5: Simulation results – PDN frequency response.

3.2 Feasibility Study through Measurements on PDN

PDN modeling provides an initial idea about the feasibility of PLC in microprocessors. However, measurements are required to firmly confirm the feasibility of proposed PLC scheme. Measurements are of significance because a number of simplifying assumptions are made in order to keep the model complexity within manageable limits. Also, a number of PDN design parameters are unknown due to proprietary nature of the information. These factors limit the accuracy of PDN model. This section discusses the high frequency measurements conducted on state-of-the-art Intel® microprocessors' PDNs. The measurements were conducted at Intel's facilities. Initial results on measurements of 65nm Intel® Pentium 4 processor's PDN were

reported in [5]. More extensive measurements were accomplished later on 45nm Intel® Core2 Duo processor. The following sub-sections report the measurement procedure and the results obtained for measurements on 45 nm Intel® Core 2 Duo microprocessor's PDN.

3.2.1 Measurement Setup

A broadband Vector Network Analyzer (VNA) was used for measuring S-parameters of a microprocessor's PDN. Use of vector network analyzer for measurement of high frequency response of microprocessor's PDN has also been mentioned in [15]. Due to the unique nature of our research, putting together a measurement setup was not trivial. A setup typically used for power supply noise measurements at Intel was modified to suit our needs. The setup used for characterizing PDN is shown in Figure 3.6.

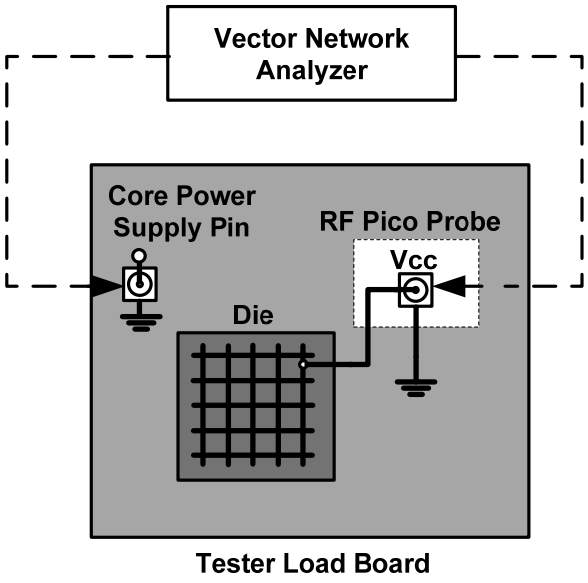

Figure 3.6: Measurement setup for high-frequency measurements on microprocessor's PDN.

The microprocessor die under test was mounted on a tester load board. One port of VNA was connected to power supply pin on the load board. A launcher needle, used in Time Domain Reflectometer (TDR) measurement of tester board power planes, was used to connect the VNA port to power supply pin of the load board. The second port of VNA was connected to a node in

the on-chip power grid of the microprocessor. Contact to the node in the on-chip power grid was made through the substrate side of the microprocessor die using electropolishing, chemical etching and metal deposition using Focused Ion Beam (FIB). Since the current generation of Intel microprocessors employ flip-chip packaging technology, therefore, internal nodes in the chip are available only through the back of the die through the substrate. Eletropolishing, is typically used to thin the substrate and chemical etching is applied to create a stepped ladder like cavity to expose an internal node in the die. Focused Ion Beam is used to deposit metal into the cavity to make a contact, which can be probed using picoprobes [28]. Since the contact to on-chip power grid was made through the back of the chip, therefore, metal layers were approached in the increasing order of layer hierarchy, i.e. M1, followed by M2 and so on. The node in the on-chip power grid was chosen at M2 layer, which can be conveniently exposed without destroying much of the other on-chip routing. In fact, this is suitable for our measurements as PLC transmitters/receivers will eventually be connected to V_{cc} (power) lines at M2.

3.2.2 Measurement Results

Measurements were carried out on three different samples of 45nm Intel(R) Core2 Duo microprocessor. Two nodes were etched on each microprocessor die sampled for measurements, in order to characterize spatial variations in the high-frequency transfer characteristics of the PDN. Locations of these nodes were randomly chosen on each sample. The five individual measurements and the superimposed average measurement are shown in Figure 3.7. The plot shows measured frequency dependent S21 parameters, where Y axis is magnitude of S21 in percentage and X-axis is frequency in GHz. The measurements were carried out over a frequency range of 45 MHz to 6 GHz.

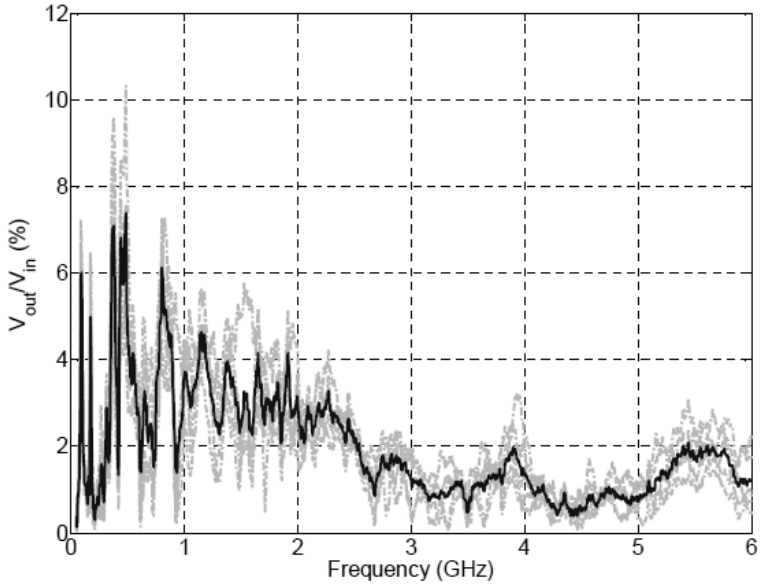

Figure 3.7: Spatial and intra-die variation of the transfer characteristics of 45 nm Intel ® Core2 Duo power distribution network (Individual transfer characteristics are shown in lighter shade and the average is shown in dark color.

Another set of measurements were done with the load board mounted on a production-level tester. Two measurements were performed, one with the microprocessor powered down and another with the microprocessor running a test loop. Due to limitation of the setup, simultaneous picoprobing and thermal cooling of the microprocessor was not feasible. Therefore, the microprocessor was run at the lowest core V_{cc} and clock frequency, at which the processor was functional. Consequently, temperature effects were minimal. The current drawn under these conditions is less than 7A. The frequency response in terms of measured S21 parameters is plotted in Figure 3.8. The two curves correspond to the microprocessor being active (powered-up) and inactive (powered-down).

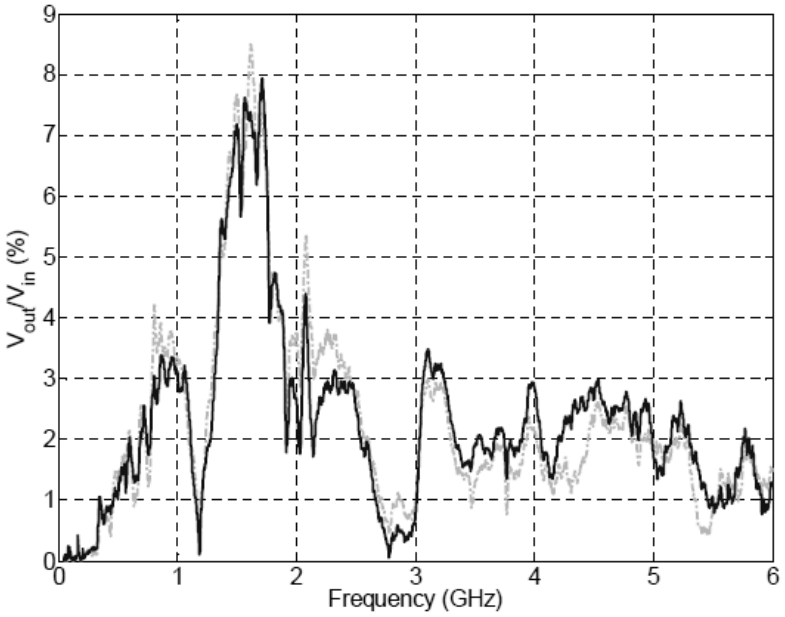

Figure 3.8: Transfer characteristics of power-up vs powered-down Core2 Duo PDN (dark shade corresponds to power-up processor and light shade corresponds to powered-down processor.

3.2.3 Significant Findings

From the measurements on tester load board, shown in Figure 3.7, it can be observed that pass-bands do exist in high frequency transfer characteristics of the PDN. The passbands observed are narrow and sporadic. Specifically, passbands are observed at 500 MHz and at 850 MHz. Also, it can be observed that the signal attenuation is lower for frequencies below 2.5 GHz.

The second set of measurement conducted with the load board mounted on a production-level tester, shows significant change in passbands characteristics. It can be observed from Figure 3.8 that the passbands are now smoother and wider. One large passband, where about 5-7 % of the signal passes through, is observed at 1.4 GHz with a bandwidth of about 500 MHz. Note that these differences in transfer characteristics is attributed to the extra capacitance and inductance associated with the tester power supply. Therefore, passbands tend to move based upon the system design. Also, variations are observed from one silicon technology process to another [5]. So, instead of identifying individual passbands, a more viable method would be to cover the

entire range of frequency spectrum with lower attenuation, say from 300 MHz to 2.5 GHz. This further supports the suitability of UWB modulation for PLC in microprocessors.

Measurements results, reported above are considerably different from the modeling based results. The reason for this difference is attributed to the fact that PDN design information is generally unknown and is kept proprietary by companies. However, the overarching aim of establishing the existence of passbands is met through measurements, as the measurements confirm the existence of passbands in the frequency transfer characteristics of a microprocessor's PDN. This ascertains the feasiblity of the proposed PLC scheme in microprocessors.

3.3 Chapter Summary

This chapter covered the earlier work done to study the feasiblity of the PLC scheme. Two approaches to feasibility study, namely, analytical modeling based and measurement based were followed at VTVT lab. In section 3.1, the analytical approach for modeling a microprocessor's PDN was discussed. A case study was presented, where the described PDN modeling approach is used to model the frequency response of a microprocessor's PDN.

In section 3.2, measurement based appraoch for characterizing the frequency response of a microprocessor's PDN was described. Results from measurements conducted on state-of-the-art Intel® microprocessors' PDNs were discussed. Considerable differences observed in the results of PDN modeling and measurements were qualified. Lastly, implications of the fndings from measurement results were given.

Chapter 4

System Level Study

Prior investigations on the feasibility of the PLC scheme mainly involved characterization of the frequency response of the PDN of microprocessors. As a next step, system level performance of PLC in microprocessors was estimated through a simulation based study. MATLAB has been used to model the PLC system. This chapter elaborates the MATLAB simulation model, explaining the PDN channel model employed in the simulations and the PLC architecture. Laslty, the results obtained from the simulations are discussed.

4.1 Simulated System Model

Measured frequency characteristics of the PDN channel are used to model the microprocessor level PLC system. The system consists of an off-chip Impulse-UWB transmitter (test/control module), which communicates with an integrated Impulse-UWB receiver (data recovery block) in the microprocessor chip through the PDN, as illustrated in Figure 1.1. A block diagram of the simulated system considered for our analysis is shown in Figure 4.1. The communication system consists of three blocks: a transmitter, a PDN channel, and a data recovery block. These sub-blocks are discussed in details in the following sub-sections.

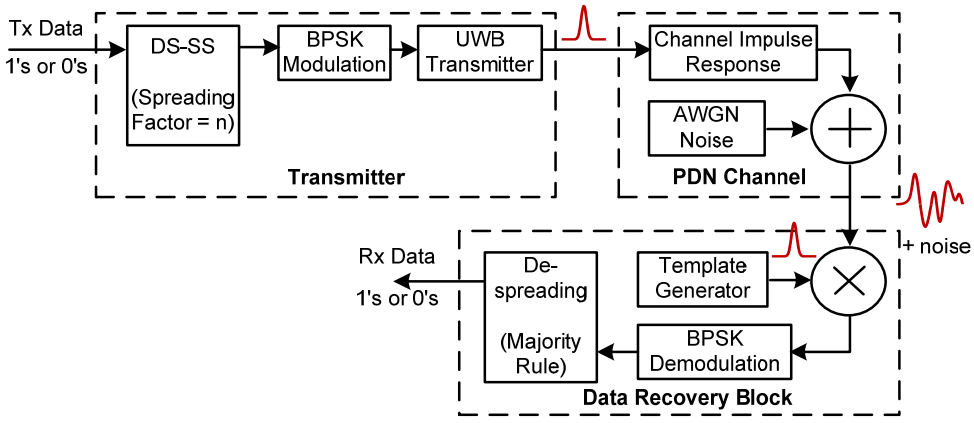

Figure 4.1: Simulation Block Diagram

4.1.1 Transmitter Model

The transmitter takes as input a random bit sequence and outputs a sequence of UWB impulses. DSSS is employed in the transmitter with a variable spreading factor of n. Thus each input data bit is converted into a sequence of n bits, depending upon the employed pseudo random code. The spread bit sequence, also called chips, is BPSK modulated and transmitted as a sequence of postive-going or negative-going Gaussian shaped UWB pulses. The pulse characterisitics, namely, pulse width (Δ) and amplitude (A), are varied during the simulation for studying their impact on system performance.

4.1.2 PDN Channel Model

PDN of a microprocessor with its multilayered branched-grid structure behaves as a multipath channel. Impulse response of a simple L-tap multipath channel model is given by (1).

$$h(t) = \sum_{l=0}^{L-1} \alpha_l \delta(t - \tau_l) \qquad \ldots (1)$$

where, α_l is the attenuation and τ_l is the delay in the arrival of l^{th} multipath component. A typical communication channel model is shown in Figure 4.2. The received signal *r(t)* in this case can be expressed as in (2).

$$r(t) = x(t) * h(t) + n(t) \qquad \ldots(2)$$

where * represents the convolution operation.

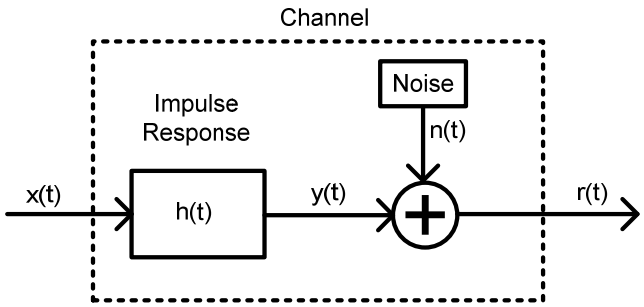

Figure 4.2: Typical communication channel model.

For an accurate multipath channel model, several measurements are required to capture the statistical variations in the impulse response as well as the delay spread of different multipath components. A number of measurements were conducted on different Intel microprocessors, where s-parameters were measured using the setup explained in section 3.2.1. Measurements conducted for 45 nm Intel Core 2 Duo and 65 nm Intel Pentium 4 processors have shown existence of passbands (peaks in the frequency response) for both the processors; however, these passbands are quite different for 65 nm Pentium 4 processors and 45 nm Core 2 Duo processors. An example measurement result for 45 nm Intel® Core 2 Duo processor is shown in Figure 4.3 (a). The corresponding impulse response computed by taking an IFFT of the frequency response is shown in Figure 4.3 (b).

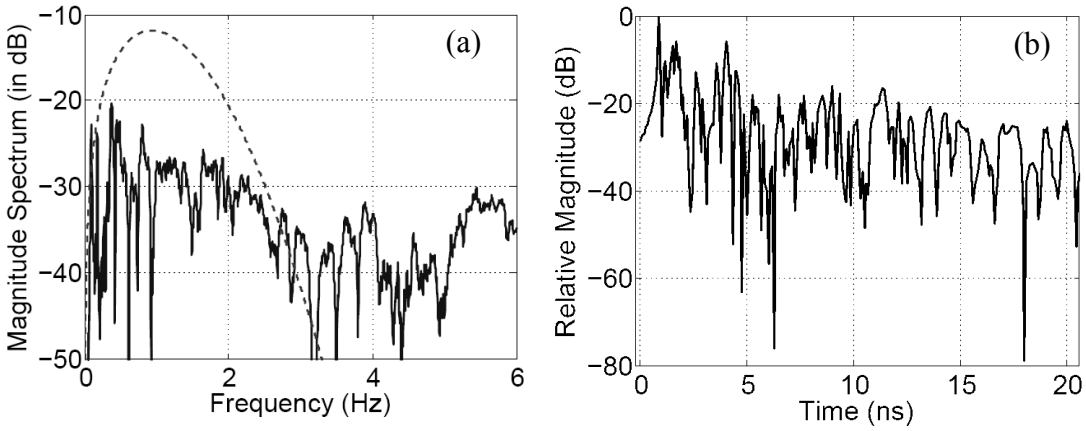

Figure 4.3: (a) Frequency response of 45nm Intel® Core2 Duo processor and with an impulse UWB spectrum superimposed. (b) Normalized impulse response of 45 nm Intel® Core2 Duo processor, computed by performing an IFFT operation on the measured frequency response.

The measurements show that spatial and inter-die variations of the frequency response for the same process technology is minimal (refer Figure 3.7). An interesting observation is that the overall attenuation is lower for frequencies below 2.5 GHz in all the measurements for both the processors. Therefore, UWB impulse with a spectrum which covers this frequency band can be used to effectively communciation data over a microprocessor's PDN, as shown by a dotted line in Figure 4.3.

A PDN channel model, based on the general channel model shown in Figure 4.2, is generated from the measurements. Channel impulse response is computed from the frequency domain measurements of the PDN channel by performing an IFFT operation, as shown in Figure 4.3 (b). The received waveform can then be computed by convolving transmitted impulse with the channel impulse response and adding noise, as given in (2). An example received waveform for Gaussain transmitted impulse, sans the channel noise, is shown in figure 4.4. It can be seen that the received waveform has a lot of multipath components, which last for a duration much longer than the pulse duration. These multipath components eventually die off, however, they limit the data-rate. Also, the receiver needs to synchronize with the received impulse giving maximum correlation output.

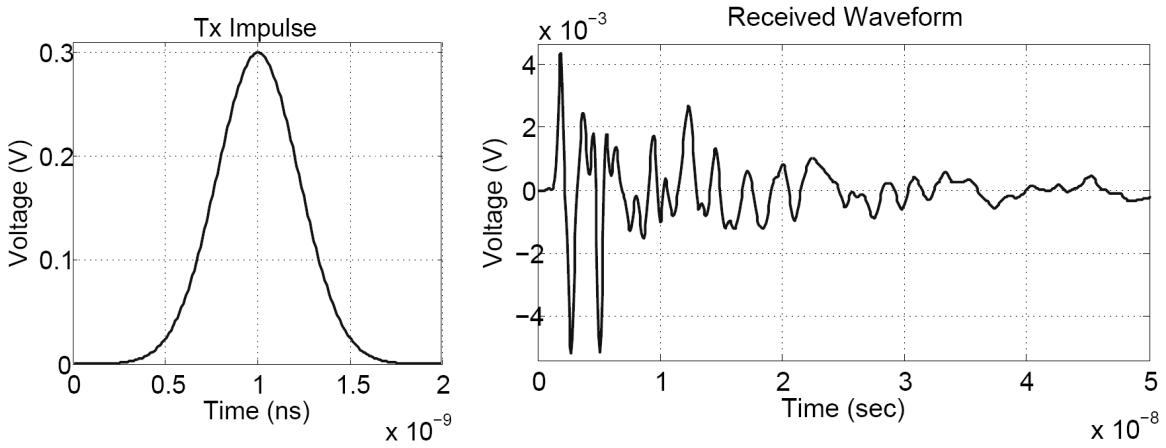

Figure 4.4: Transmitted Gaussian impulse (left) and the corresponding received waveform (right) after convolution with the PDN impulse response.

4.1.3 Noise in the PDN Channel

Measurement of noise on the power line of microprocessors has shown following properties [29], [30]:

a. Gaussian cyclostationary background noise which appears due to large number of circuits switching synchronously with the main clock.

b. Strong deterministic components at clock frequency and at higher frequencies because of flip-flop and logic-gate toggling at or near the clock edge, which generates a current profile with reptitive pulses.

c. Low frequency (20 – 100 MHz) noise resulting from resonances in the impedance characteristics of the PDN.

From the perspective of implementing a PLC system, certain components of noise can be rejected. Firstly, the impact of low frequency noise components can be minmized using circuit design techniques. Similarly, high frequency noise can be suppressed by limiting the circuit bandwidth. Secondly, DSSS helps in reducing the narrowband interference due to clock and related switching activity. Therefore, in our study we will assume that the processing gain of DSSS is high enough to supress narrow-band interference.

Gaussian cyclostationary noise present in a microprocessor's PDN can be modeled as shown in Figure 4.5, where a white Gaussian noise source is sampled periodically [30]. The sampling clock in the model need not be the same as the main clock. PLC system analysis can be further simplified by assuming that the data communication and noise generation processes are asynchronous. Under such an assumption, the noise can be resonably modeled as additive white Gaussian noise (AWGN) [31]. This has been verified through both numerical analysis and Monte Carlo simulations using MATLAB and will be discussed in the following sections.

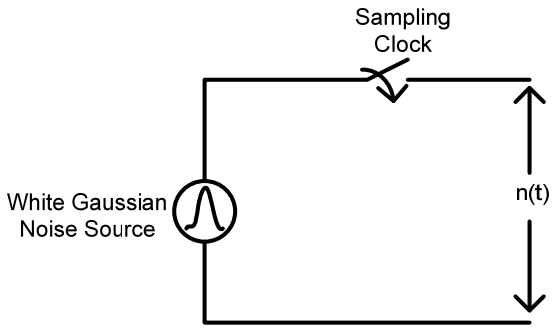

Figure 4.5: Simple Gaussian cyclostationary noise model.

4.1.4 Receiver or Data Recovery Block Model

Receivers for I-UWB are broadly categorized as threshold or leading edge detector (LED), correlation detectors (CD) and RAKE receivers. Although, RAKE receivers are more popular for their robustness but LED and CD receiver are preferable options for the considered application because of their simpler implementation. A CD receiver structure has been selected because it is sensitive to total received power rather than peak power, which is important in a noisy microprocessor environment. Another important reason for the choice of CD circuit receiver is its simpler circuit implementation, which is an important factor in data recovery block design.

As discussed in section 4.1.2, the received waveform is given by equation (2), which can be written as:

$$r(t) = b\sum_{l=0}^{l=L-1} \alpha_i p(t-\tau_l) + n(t) \qquad \ldots(3)$$

where, $b = \pm 1$ is the transmitted data bit and *p(t)* is Gaussian pulse. The decision statistic or the output of the correlator for a CD receiver, using a template matched with the transmitted impulse

is given by:

$$Z = \int_{\tau_o}^{T+\tau_o} \left(b \sum_{l=0}^{l=L-1} \alpha_i p(t-\tau_l) + n(t) \right) p(t-\tau_o) dt \qquad \ldots (4)$$

Perfect synchronization between transmitter and receiver is assumed, therefore, the delay $\boldsymbol{\tau_o}$ corresponds to the delay giving the peak correlation output. Assuming that this correlation output is not dominated by the multipath interference, the synchronization delay $\boldsymbol{\tau_o}$ will correspond to the delay of the multipath component with lowest attenuation, say $\boldsymbol{\tau_K}$.

For the case of Additive White Gaussian Noise (AWGN), mean and variance of z conditioned on the transmitted bit $b = \pm 1$, is given by (5) and (6) respectively:

$$\begin{aligned} u_1 = u_{-1} &= \sum_{l=0}^{l=L-1} \alpha_l \int_{\tau_o}^{T+\tau_o} p(t-\tau_l) p(t-\tau_o) dt \\ &\approx \sum_{l=0}^{l=L-1} \alpha_1 \rho(\tau_1 - \tau_o) \qquad \ldots (5) \end{aligned}$$

$$\sigma_1^2 = \sigma_{-1}^2 = \frac{N_o}{2} \int_{\tau_o}^{T+\tau_o} p^2(t-\tau_o) dt \approx \frac{\mathrm{N_o}}{2} \rho(0) \qquad \ldots (6)$$

where, ρ is the auto-correlation function of the Gaussian pulse *p(t)*.

Therefore, Bit Error Rate (BER) or Probability of bit error (P_e) for AWGN case is given by:

$$P_e = Q\left(\frac{u_1}{\sigma_1} \right) = \mathrm{Q}\left(\sqrt{\frac{2}{\mathrm{N_o}} \left[\alpha_K + \frac{1}{\rho(0)} \sum_{\substack{l=0 \\ l \neq K}}^{l=L-1} \alpha_i \rho(\tau_o - \tau_i) \right]} \right) \qquad \ldots (7)$$

where, $\boldsymbol{\alpha_K}$ is the attenuation of the multipath component corresponding to maximum correlation.

The case when noise *n(t)* is Gaussian cyclostationary, as modeled in Figure 4.5, is considered next. Assuming that the pulses are transmitted asynchronously with respect to the gating clock, the probability of bit error depends upon the pulse duration. First consider the case when pulse duration is much smaller than half of the clock period. The probability of bit error in this case will depend upon the position of the pulse with respect to the clock. The pulse may lie completely within the interval when clock is zero or when clock is high or it may lie in the

region of clock transition. When the pulse lies in the clock '0' interval, the probability of error is zero; however, when the pulse lies in clock = '1' interval, the pulse sees twice as much noise as the equivalent time averaged noise of the cyclostationary noise process. The reason for double noise is the fact that cyclostationary noise power is zero for half of the time interval, thus it's time averaged Power Spectral Density (PSD) is 1/2 the PSD of the internal Gaussian process. Assuming that the pulse duration is much smaller than the clock period, such that the probability of pulse overlaps with clock transitions is negligible. Then the average P_e or BER is given by:

$$P_{e,\,\text{cyclostationary}} = \frac{1}{2}\left(P_{e,\,\text{AWGN with 2xPSD}}\right) \qquad \ldots(8)$$

Where, the expression in parenthesis on the right-hand side is the probability of bit error in the presence of Gaussian noise with PSD equal to twice the average PSD of the cyclostationary noise process.

The other case is when the impulse duration is much larger than the period of the gating clock of the cyclostationary noise process and the impulses are transmitted asynchronously with respect to the gating clock. The equivalent noise in the received bits in this case will average out to the equivalent time averaged AWGN case and hence probability of bit error will be equal to the AWGN bit error probability.

4.2 MATLAB Simulation Results

Performance of the PLC system was evaluated in MATLAB using two different simulation techniques. In the first technique, MATLAB was used to numerically evaluate receiver decision statistics, as given by equations (4) to (7) for the AWGN case. In the second type of simulations, MATLAB was used to perform Monte Carlo simulations [12]. In Monte Carlo simulations, received waveform is computed by convolving transmitted waveform with the channel impulse response and adding noise. The received waveform is then correlated with a template waveform for CD reception. The correlation output is then used as decision metric. This process is repeated for long sequence of random data bits and in the end total reception errors are computed. Total number of reception errors divided by the number of transmitted bits gives an estimate of BER.

Monte Carlo simulations were performed for both AWGN and cyclostationary noise cases. Two different studies were conducted; the first study compared BER performance of the PLC system for the two different noise cases – AWGN and cyclostationary noise. The second study was conducted to estimate the impact of various system parameters, e.g. spreading factor, pulse width etc, on PLC system performance i.e. BER and data-rate.

In the first study, Monte Carlo simulations were conducted for different transmitted impulse widths. The resulting BER performance was compared with the performance in the presence of AWG noise with ½ the PSD of the internal Gaussian process of cyclostationary noise. The plots are shown in Figure 4.6. BER trends exhibited in the plots are as expected; BER for cyclostationary process is smaller than AGWN case when the pulse width is much smaller than the gating clock period and it tends to match the BER in AWGN case, as pulse width increases.

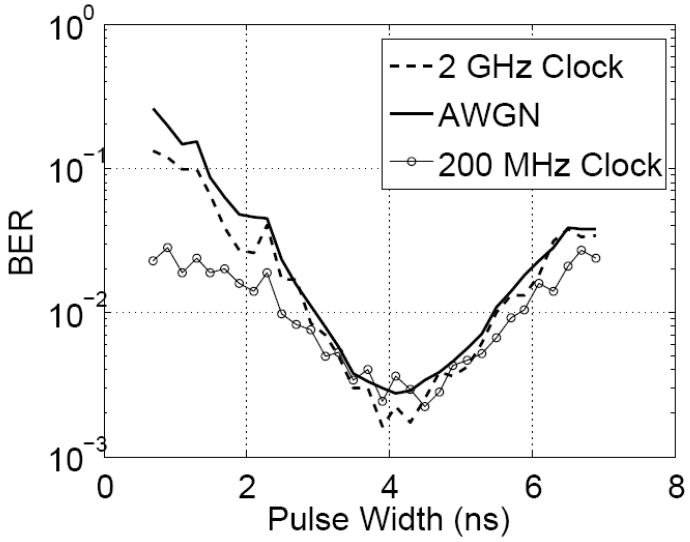

Figure 4.6: PLC system performance in cyclostationary noise.

In the second study, both Monte Carlo and numerical simulations were performed for AWGN noise case, where the system performance was evaluated for various spreading factors (n) and pulse width (Δ), for a fixed transmitted pulse amplitude (A). The motivation is to estimate the minimum required received pulse amplitude or fluctuations on the power line to achieve a desired BER. As expected, the results of both types of simulations (numerical and Monte Carlo) were found to match, therefore, in the following discussions results from the two simulations are

not mentioned separately. The plots in Figure 4.7 (a) show BER versus transmitted impulse width Δ for a spreading factor of 21 for two channel models of 65 nm Intel Pentium 4 and 45 nm Intel Core 2 Duo. It is interesting to note that there exists an optimal pulse width which minimizes the BER. The optimal pulse width is in the range of 1 to 1.5 ns for both the processors. Figure 4.7 (b) shows BER versus spreading factor for two different received pulse amplitudes of 5 mV and 10 mV observed at the on-chip power grid, while the transmitted impulse width is fixed to 1.5 ns. As expected, the BER decreases proportionally with increase in the spreading factor. For example, a BER of 10^{-10} can be achieved with the spreading factor of 111 for peak amplitude of 5 mV and the spreading factor of 51 for peak amplitude of 10 mV. The corresponding data rates are 112 kbps for peak amplitude of 5 mV and 245 kbps for the 10 mV case.

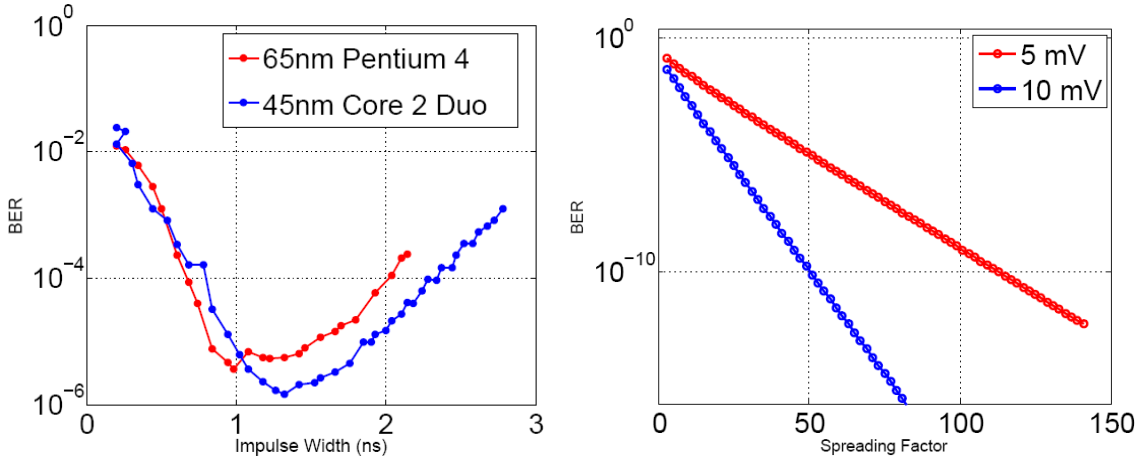

Figure 4.7: (a): BER versus transmitted impulse width. (b): BER versus spreading factor.

4.3 Significant Findings

The simulation results showing comparison of PLC system performance in the presence of cyclostationary noise and in the presence of AWGN are shown in Figure 4.6. As predicted analytically in section 4.1.4, it can be seen from the figure that when gating clock is 200 MHz, reduction in BER is observed for pulse widths much smaller than the clock period, i.e. 5 ns. For 2 GHz gating clock, the time period is very small and hence the reduction in BER is not appreciable for the simulated impulse widths. For both the clock frequencies, BER tends to the

AWGN case when transmitted impulse width increases. Based upon this observation, the remainder of the study was done only for AWGN case. It is assumed that the microprocessor clock frequency is in GHz range; therefore, the pulse width used for PLC is comparable to or larger than the clock period.

The second study demonstrated that with the use of DSSS, small received pulse amplitude of 5 mV to 10 mV is sufficient to achieve a BER as low as 10^{-10}. However, to incur 5 mV at the on-chip power grid, the simulations indicate that the transmitted amplitude at an input pin of a tester load-board should be about 150 mV, and the input pin voltage increases to 300 mV for 10 mV at the on-chip power grid. The voltage required at an input pin of a load-board may be a concern, although the voltage at the on-chip power grid is much lower than acceptable fluctuation limit of ± 5% of Vdd [32]. The required transmitted pulse amplitude can be reduced by employing following techniques:

a. Use of pulse shaping at the transmitter to reduce multipath interference at the receiver. It has been shown that pulse shaping can bring significant improvement in performance [33].
b. Routing one or a few power-pins of a microprocessor through signal paths of the package.
c. Utilizing the existing VCC_SENSE pins, which are connected directly to the on-chip power grid.

Both cases (b) and (c) avoid the attenuation through on-package decoupling capacitors and are subject to future investigations.

The achievable communication data rate, observed in the second study, is in the range of few hundred KHz to a few MHz. Although, currently feasible data rate is low, still, the use of a microprocessor's PDN for low data communication opens up the potential for a broad spectrum of applications. These applications are discussed in details in Chapter 6.

4.4 Chapter Summary

A system level study of the PLC scheme was presented in this chapter. In section 4.1, simulation model of the system was discussed. Each of three blocks in the simulation model, namely, transmitter, PDN channel and data recovery block, were described in details.

In section 4.2, results from MATLAB simulation were given. Both numerical analysis and Monte Carlo simulations were carried out using MATLAB. The results of both types of MATLAB simulations were found to match.

In section 4.3, inferences obtained from the simulation results were discussed. A simple CD receiver was shown to be capable of performing PLC in microprocessors. However, the achievable data rate was found to be considerably low. Such low data communication still has a lot of potential applications in future microprocessors.

Chapter 5

Data Recovery Block Design

A key circuit element of microprocessor level PLC system is data recovery block. Implementation of data recovery block is quite challenging because of the small area and low power constraints. This is required because the intended applications need to integrate tens or more of these on a single chip without encompassing significant area and power overhead. The design is also required to be digital process friendly. Lastly, the receiver needs to recover UWB impulses from a noisy power line; therefore, it should have high-sensitivity with low-offset errors. This chapter presents architecture of the proposed data recovery block design. Next, the chapter covers circuit designs of its sub-blocks. Simulation results from the implementation of data recovery block design in TSMC 0.18 μm CMOS process and IBM 0.13 μm CMOS process are provided. Lastly, the chapter covers the results from the test chip fabricated through MOSIS.

5.1 Architecture

As discussed previously a CD receiver is most suitable for data recovery block because of its low complexity and simple hardware implementation. Further, a CD receiver is sensitive to total received power rather than peak power – an important factor in a noisy microprocessor environment. A block-level diagram of CD receiver based data recovery block circuit is shown in Figure 5.1.

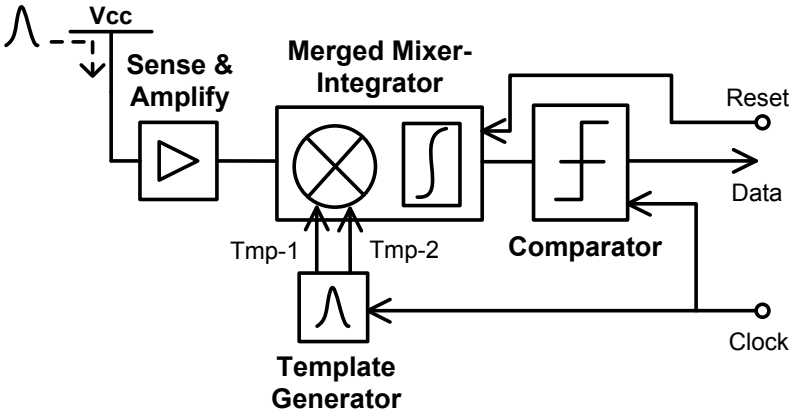

Figure 5.1: Data recovery block architecture.

Data recovery block mainly consists of four different sub-blocks. The first sub-block, namely - Sense and Amplify, senses UWB impulse from its power line and converts it to a differential signal. It also provides amplification and translation of common mode voltage of the impulse from supply voltage (V_{dd}) to an intermediate voltage. The differential output of Sense and Amplify sub-block is fed to a Mixer-Integrator sub-block. This sub-block correlates the received impulse with a template impulse generated by the Template Generator sub-block. The clock signal, input to Data Recovery Block, triggers Template Generator to generate two template signals. Template-1 signal is used to correct offset error, as will be explained later, while Template-2 signal is generated in synchronization and correlated with the incoming impulse. An optimal template for an I-UWB receiver is the one that matches the received pulse waveform; however, template generation of such waveform is complex and power hungry [34]. Therefore, a digitally generated impulse has been adopted as the template waveform. Lastly, Comparator sub-block converts the differential output of Mixer-Integrator to a digital signal, depending upon its polarity.

After each data recovery cycle the Mixer-Integrator sub-block is reset to initialize data recovery block for receiving next impulse. Following section covers circuit designs for each sub-block in details.

5.2 Circuit design

5.2.1 Sense and Amplify

The goal of Sense and Amplify sub-block is to reliably detect short duration UWB impulse from a noisy power line of a microprocessor. Power line noise characteristics of some of the state-of-the-art microprocessors has been measured and reported in [29], [35]. Measurements conducted by Saint-Laurent et al [35] over duration of around 40 µs showed that power supply noise has large low frequency swings superimposed with small high-frequency noise, illustrated in Figure 5.2. These low frequency variations are due to change in processing load of the microprocessor. The measurements reported by Naffziger et al in [29] showed similar trend for low frequency noise and further established the presence of peaks at high-frequencies in the noise frequency spectrum due to switching of microprocessor circuits with the clock. The sense and amplify circuit sub-block has been designed to cancel out the large low-frequency variations in power supply noise, thus minimizing their impact on data recovery block operation. Further, DSSS spreading scheme minimizes the impact of narrow-band noise (noise corresponding to the peaks in noise spectrum) [11].

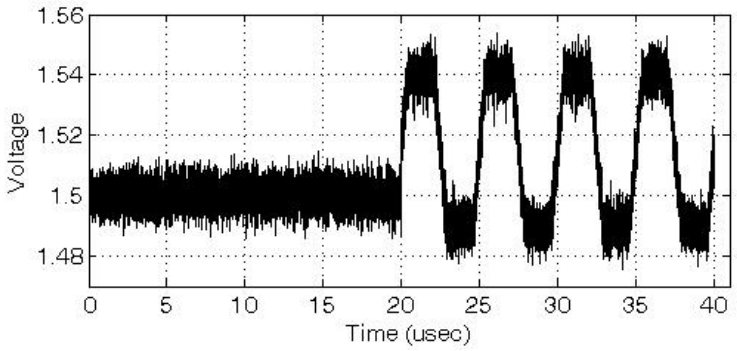

Figure 5.2: Illustration of fluctuations and noise on a microprocessor's power line. Note that the shown plot is only a figurative representation and not actual measurements.

The circuit diagram for Sense and Amplify sub-block is shown in Figure 5.3. It is a cascaded two stage differential amplifier design. Care has been taken to minimize the number of required bias voltages. The design requires one single bias voltage of 700mV, for biasing the current source FETs of differential pairs.

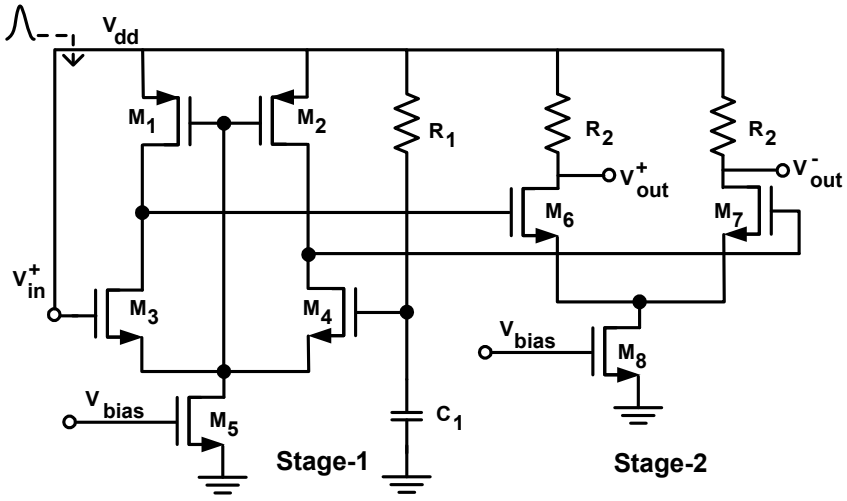

Figure 5.3: Sense and Amplify circuit diagram.

One of the differential inputs of the first differential pair is connected directly to power supply line, whereas, it's other input is connected to power supply line through a R-C low pass filter formed by R_1 and C_1. This type of connection causes low frequency fluctuations in V_{dd} to appear as a common mode voltage at the differential pair input, whereas high-frequency fluctuations appear differentially at the differential pair inputs. Therefore, UWB impulse will appear at the directly connected input of the differential pair, whereas, the capacitor at the other input will suppress the impulse. The first stage provides mainly the sensing operation. The second stage is a simple differential pair with resistive loads and acts as a gain stage. The simulated AC and transient characteristics of the design are shown in Figure 5.4 and 5.5, respectively. The results are shown for three different power supply voltages 1.23 V, 1.2 V and 1.17 V. These voltage levels were chosen corresponding to the specification of 5% peak-to-peak fluctuations in power supply voltage [32]. The input impulse on the power-line is a small 10 mV impulse with duration of 1.2 ns. Transient response shows that the amplified impulse at the output of Sense and Amplify sub-block has a peak to peak voltage of about 130 mV.

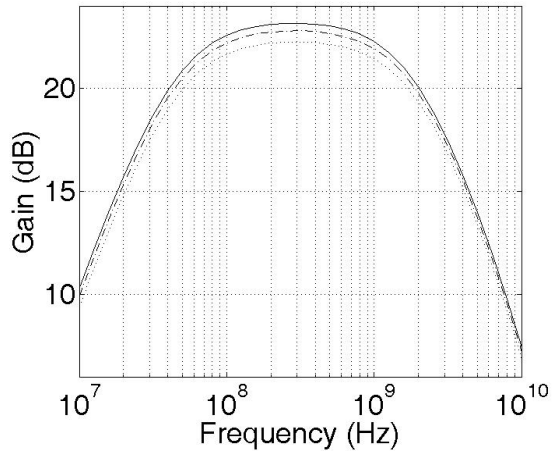

Figure 5.4: Gain vs frequency plot for Sense and Amplify.

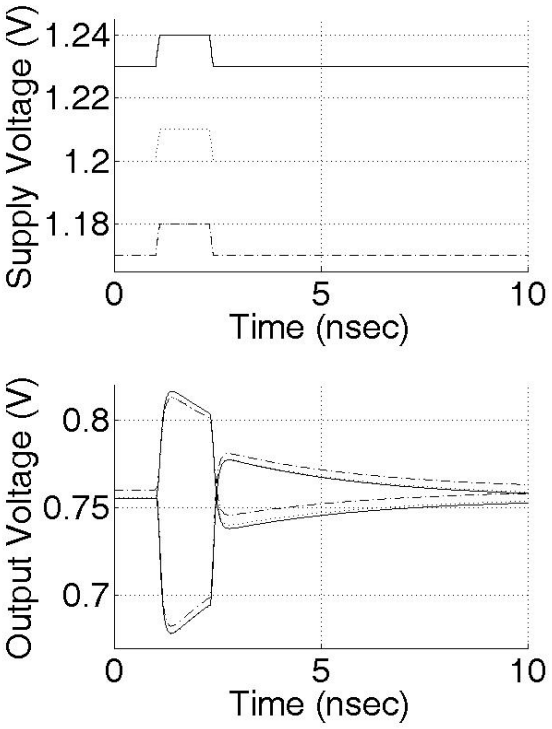

Figure 5.5: Simulated transient response of Sense and Amplify.

5.2.2 Merged Mixer-Integrator

CD receiver requires mixing and integration operations. In the proposed design, both operations have been combined into a low power merged mixer-integrator. The circuit design is

illustrated in Figure 5.6. Lower portion of the design consists of two single-balanced mixers with cross-coupled outputs. Mixer outputs are loaded with capacitors C1 and C2. Transconductors (M_{15} and M_{16}) at the bottom of the two single-balanced mixers are driven by two similar but time separated template signals. The template signals are digital impulses generated by Template Generator. The detected UWB impulse is fed differentially to the mixer-integrator at the RF inputs - V_i^+ and V_i^-. Operation of the mixer is explained as follows.

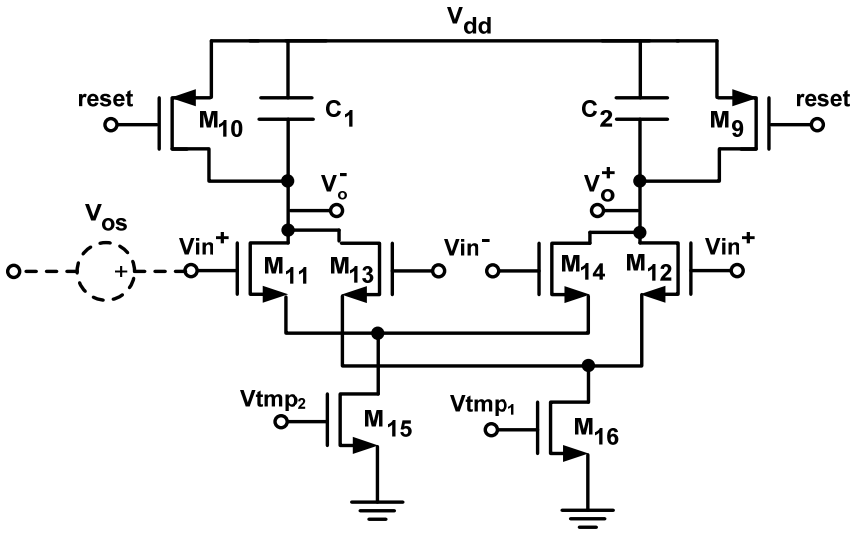

Figure 5.6: Merged Mixer-Integrator circuit diagram.

The mixer is reset by charging the output nodes (V_o^+, V_o^-) to V_{dd} by turning on M_9 and M_{10}. Once completely charged, M_9 and M_{10} are turned off. The mixer-integrator operates by discharging output nodes through FETs $M_{11} - M_{14}$ when a template signal is applied to either M_{15} or M_{16}. However, the rate of discharge differs for the two outputs. The difference is dependent upon the differential voltage at the RF input of the mixer. $Vtmp_1$ template signal is applied prior to receiving UWB impulse from power line. In this template cycle, the mixer integrates a voltage corresponding to any offset in Sense and Amplify sub-block and the mixer itself (offset voltage is shown as a voltage source (V_{os}) at Mixer-Integrator input). Next, the second template signal ($Vtmp_2$) is applied in synchronization with the received UWB impulse on power line. In the second template cycle, the merged mixer-integrator integrates the offsets in the system in reverse polarity with respect to the first template cycle, thus cancelling their effect. Also, in the second template cycle the received UWB impulse is correlated with the template

impulse, thus creating an output voltage proportional to the signal correlation. Employing two template cycles with integration in reverse polarity not just cancels out system offset voltages but also helps in low-frequency noise cancellation. This can be shown mathematically as follows.

Assume that for a differential input signal to the mixer-integrator, given by *x(n)*, the correlated output corresponding to the first template cycle is given by *-f[x(n)] = -t(n)*. Therefore the correlated output for the second template cycle, corresponding to an input of *x(n+1)* is will be *f[x(n+1)] = t(n)*. The overall output of the mixer-integrator can be written as:

$$y(n+1) = F[x(n+1)] - F[x(n)]$$
$$\Rightarrow y(n+1) = t(n+1) - t(n) \quad \ldots(1)$$
In z domain (1) becomes:
$$zY(z) = zT(z) - T(z)$$
$$\Rightarrow Y(z) = \left[\frac{(z-1)}{z}\right] T(z)$$

The above formulation is true only for noise and offset-voltage, present during both template cycles. Thus, for noise and offset the merged mixer-integrator acts as a high-pass filter. Apparently, offsets can be completely canceled using the proposed mixing technique; however, due to mismatch between transconductors M_{13} and M_{16}, the cancellation is not perfect.

5.2.3 Template Generator and Comparator

The differential output of mixer is sensed and converted to digital level using a comparator. The comparator circuit is shown in Figure 5.7 (a). It has an input gain stage and a regenerative latch stage. The input stage consists of $M_{17} - M_{21}$, where M_{17} and M_{18} are input transistors and M_{19} and M_{20} are included to minimize static current of the input stage. Regenerative latch is simply two inverters connected back-to-back forming a positive feedback loop. PMOS transistors M_{24} and M_{27} are used to pull-up the output nodes to V_{dd} (a valid digital signal level) when clock is low. When clock is high, M_{24} and M_{27} are disabled and one of the outputs of the latch stage is discharged faster than the other, depending upon the differential voltage applied to the input stage. This action is reinforced by the positive feedback of the latch stage, thus pushing the outputs to opposite rails.

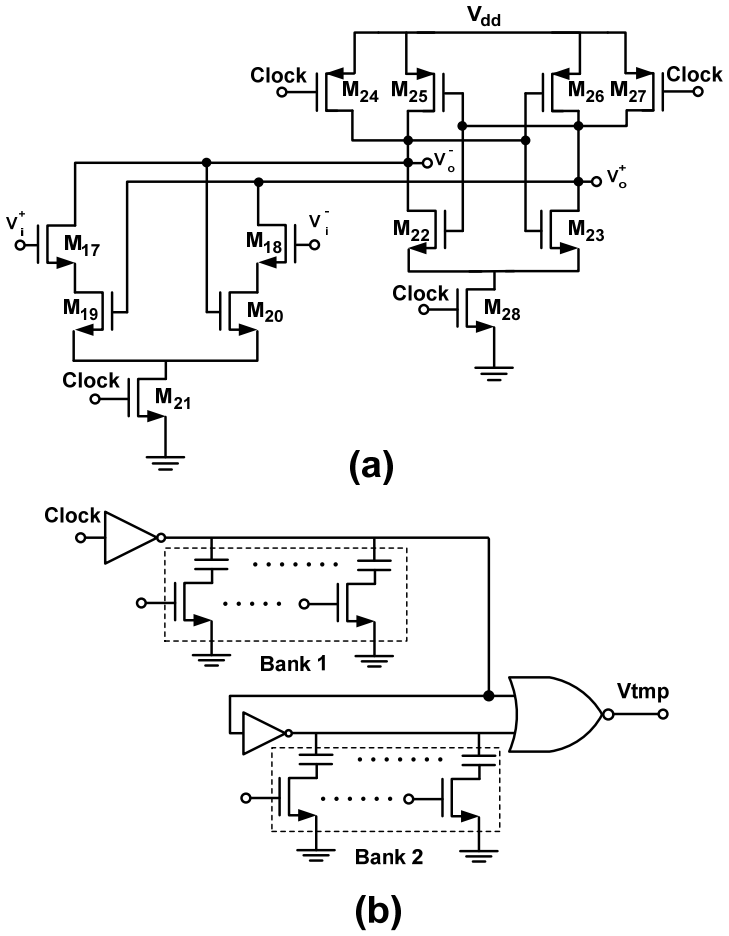

Figure 5.7: (a) Comparator circuit diagram. (b) Template Generator circuit diagram.

Template generator circuit diagram is illustrated in Figure 5.7 (b). One of the inputs to the NOR gate is inverted with respect to the other by introducing an inverter. Every time the input switches from V_{dd} to 0, a glitch is generated at the output (V_{tmp}). The generated glitch is used as the template waveform for correlation. The glitch duration can be adjusted by controlling the delay between the two inputs of NOR gate. A switched capacitor bank (bank 2) is used to tune the delay between the two inputs of NOR gate and hence control the width of the glitch. The template generator clock input is connected to the system clock through an inverter loaded with a switched capacitor bank (bank 1). Therefore, a template is generated at every clock transition from 0 to Vdd. The switched capacitor bank 1 is used to tune the clock delay in order to synchronize the template waveform with the received impulse.

5.3 Performance Evaluation

Data recovery block circuit was simulated using Cadence in IBM 0.13 μm process with a supply voltage of 1.2 V. Power supply variation in a microprocessor is typically set to ±5% to ensure data-integrity [32]. The received pulse amplitude was set to 10mV, which is much lower than the constraint, in order to add minimal noise to the existing power supply variation. The pulse-duration was set to 1 ns with a pulse repetition-rate of 100 MHz. Operation of data recovery block is shown in Figure 5.8. An offset voltage of -35 mV, corresponding to 3-sigma worst case mismatch, was intentionally added at the input of the mixer-integrator. The offset voltage source is depicted in Figure 5.6 and is used to demonstrate offset cancellation in simulations.

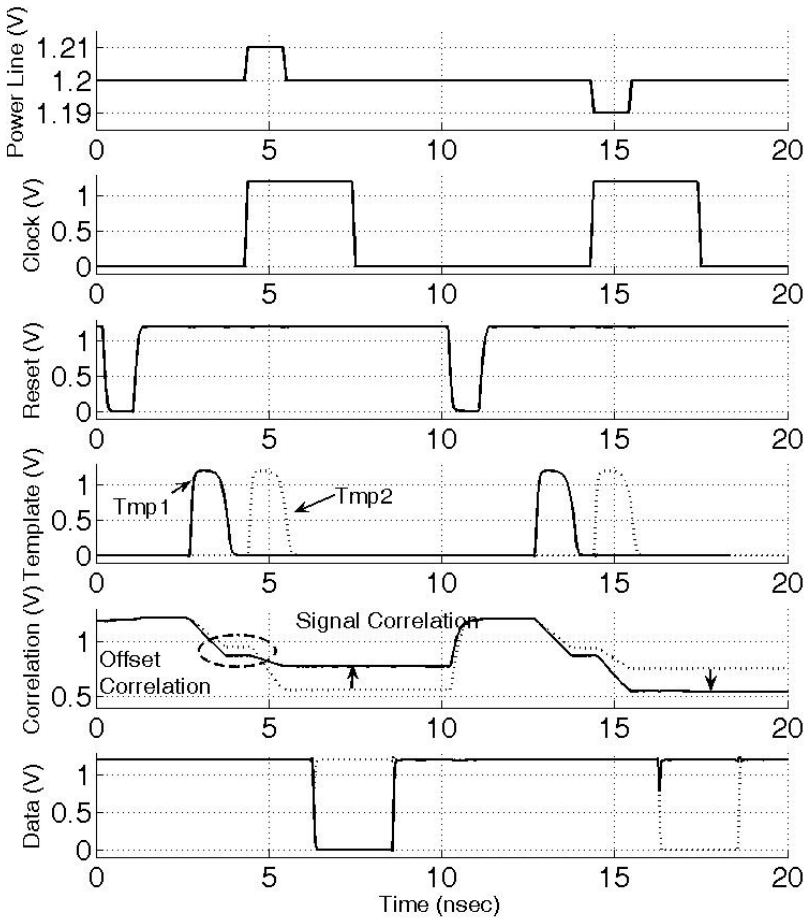

Figure 5.8: Transient simulation of Data Recovery Block.

The topmost plot in Figure 5.8 shows received impulses on the power line. Second and third plots are clock and reset signals respectively. The reset signal is 1 ns wide. Fourth plot shows template 1 and template 2 signals, separated in time by around 500 ps. Next plot shows differential outputs of Mixer-Integrator, with arrows indicating a positive difference for positive-going incoming pulse and vice-versa. Finally, the last plot shows the recovered digital data. It should be noted that the polarity of the recovered data is inverted and can be easily corrected using an inverter.

Circuit performance was evaluated across Process, Voltage and Temperature (PVT) variations using Monte-Carlo simulations. The process variation parameters were provided by the foundry. The results from Monte-Carlo simulations show successful operation across 3-sigma worst case process variations. Performance of data-recovery block is summarized in Table 5.1.

Table 5.1: Simulated Performance Summary in IBM 0.13 μm CMOS process

Parameter	Simulated Result
Supply Voltage	1.2 V
Pulse Amplitude	10 mV
Pulse Duration	1 ns
Pulse Repetition Rate	100 Mpps
Power Consumption (Sense & amplify)	3.03 mW
Power Consumption Total	3.58 mW

Data recovery block design was also implemented in TSMC 0.18 μm CMOS process. Results from this implementation were published in [36]. For the sake of completeness Table 5.2 summarizes the performance of data recovery block, implemented in TSMC 0.18 μm CMOS process.

Table 5.2: Simulated Performance Summary in TSMC 0.18 μm CMOS process

Parameter	Simulated Result
Supply Voltage	1.8 V
Pulse Amplitude	20 mV
Pulse Duration	200 ps
Pulse Repetition Rate	200 Mpps
Power Consumption (Sense & amplify)	3.78 mW
Power Consumption Total	4.42 mW

5.4 Test Chip Implementation

Due to limited number of opportunities available to work at Intel – only during summer internships, integration of data recovery block circuit in an Intel microprocessor test run was deemed infeasible. Therefore, an independent test chip fabrication was planned. The purpose of independent test chip fabrication was to demonstrate the concept of power line communication in a VLSI circuit and provide experimental results for the designed PLC circuit blocks. The test chip was fabricated through MOSIS using IBM 0.13 μm CMOS process. The process technology was selected as an optimal choice between cost and relevancy, in terms of being state-of-the-art. The overall die layout is shown in Figure 5.9. Figure 5.10 shows details of the layout of data recovery block; the individual sub-blocks of the circuit are marked in the figure. The size of the die was 2 mm x 1 mm, while data recovery block occupied much smaller space of 300 μm x 160 μm.

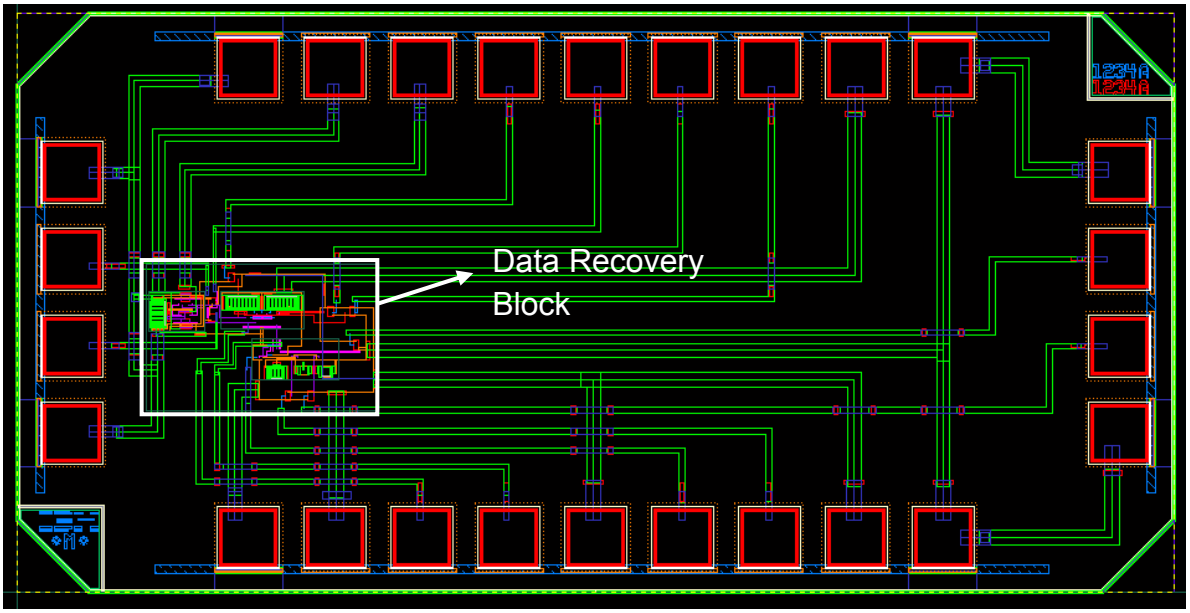

Figure 5.9: Layout of the test chip.

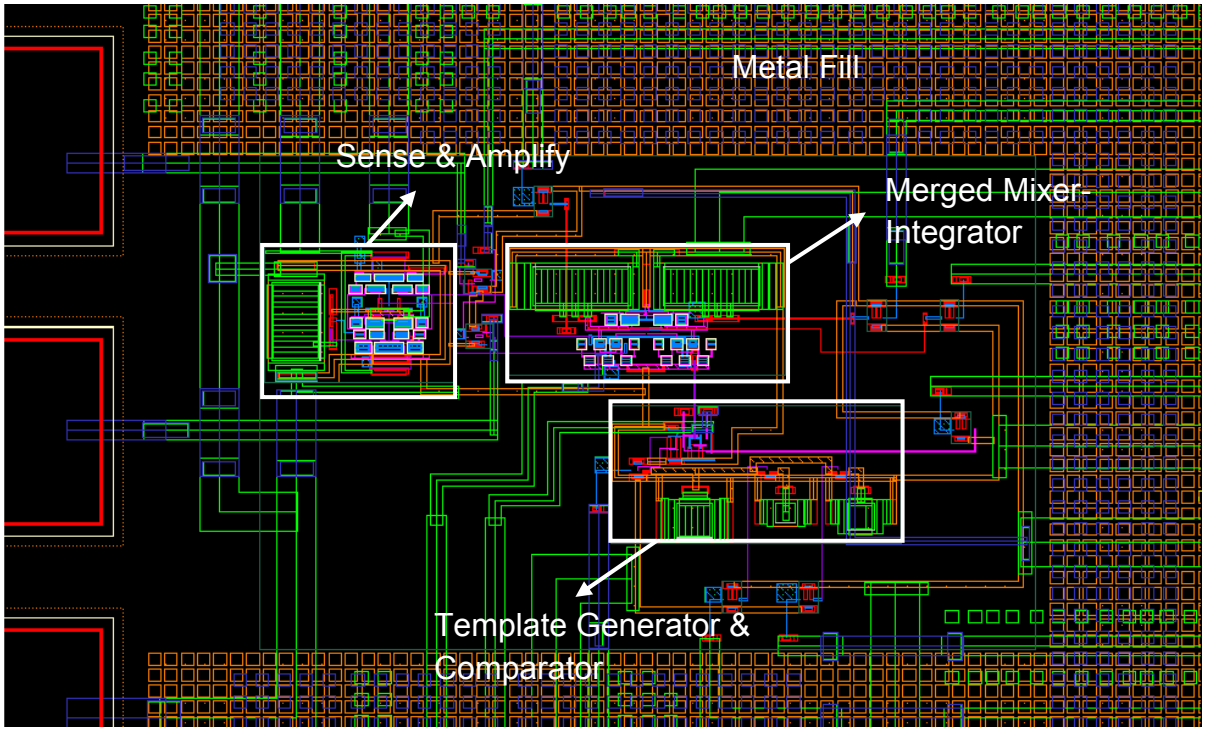

Figure 5.10: Layout of the test chip showing details of data recovery block placement.

5.5 Fabrication Results

A micrograph of the test chip die is shown in Figure 5.11.

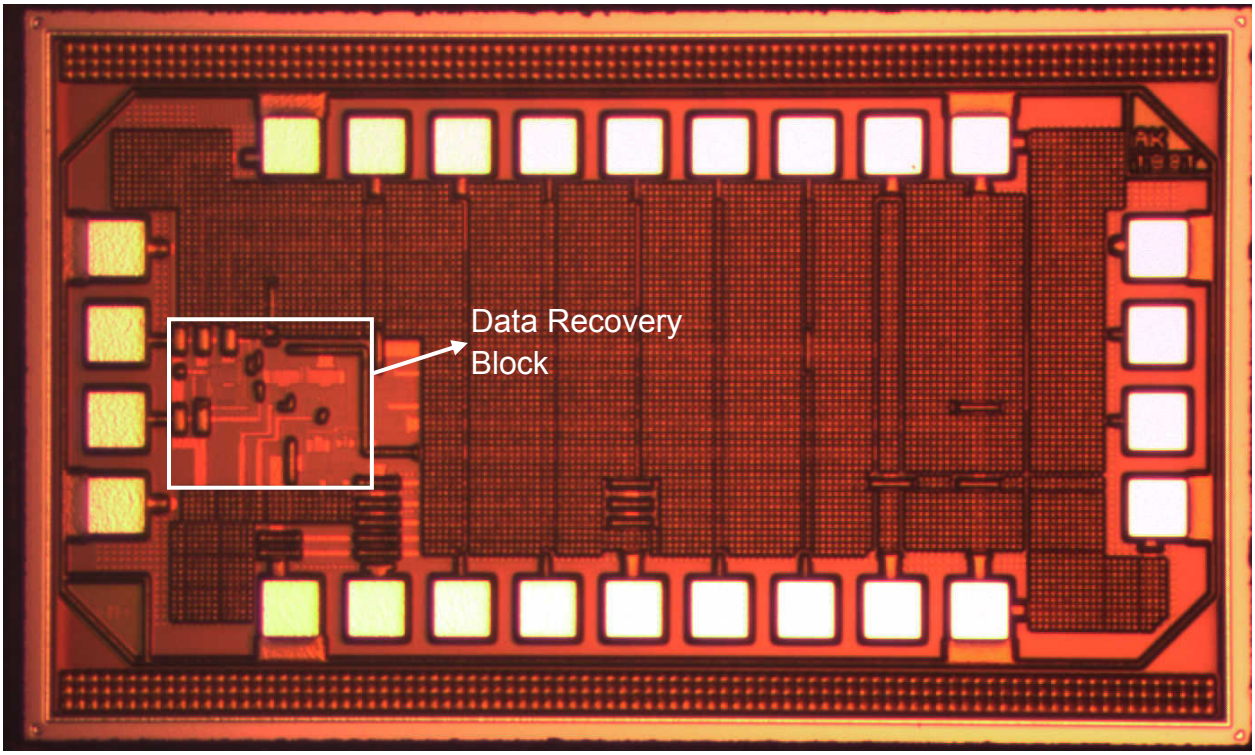

Figure 5.11: Die micrograph of the test chip.

A closer view of data recovery block in shown in Figure 5.12. However, the circuit is not clearly visible because of the metal fill in the top metal level.

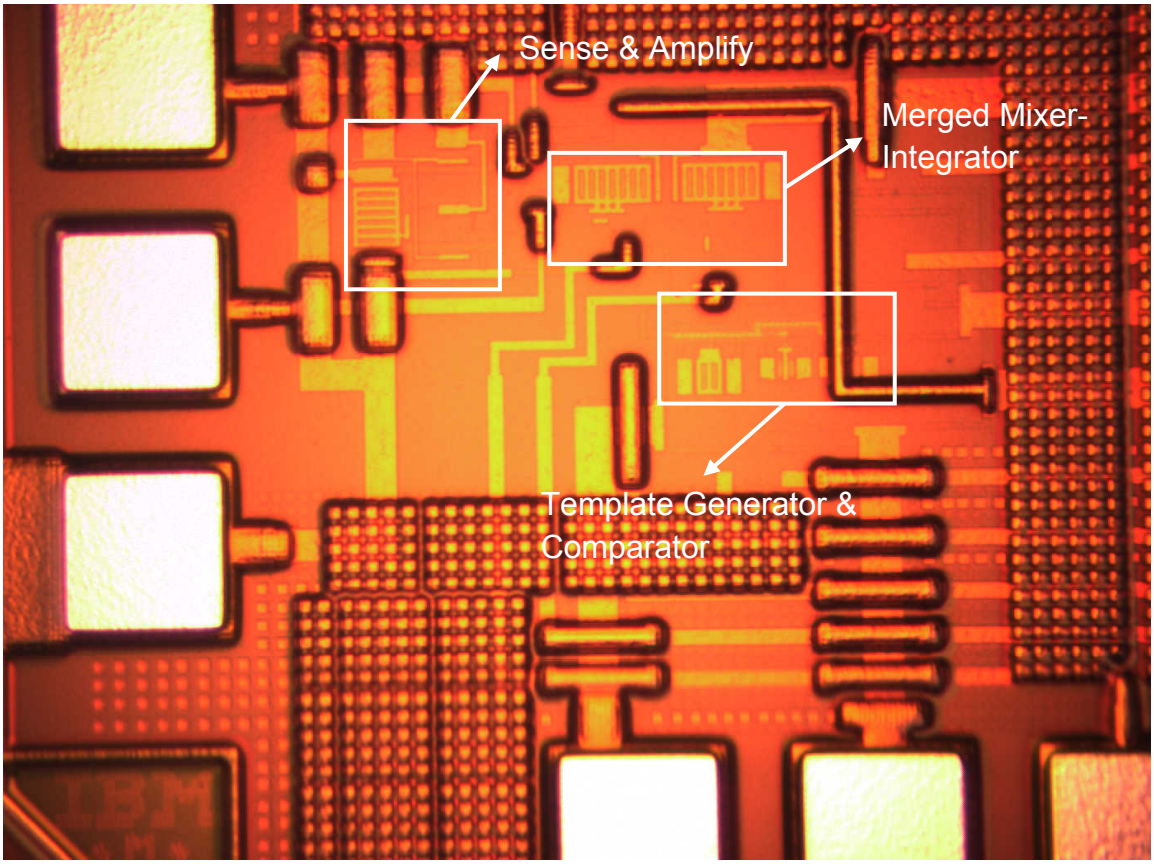

Figure 5.12: Die micrograph of the test chip showing data recovery block

Unfortunately, the test chip suffered a manufacturing defect due to the breakdown of a diode connected to V_{bias} input of Sense and Amplify sub-block. The purpose of diode is to discharge the charge which accumulates during fabrication on metal traces connected to V_{bias} input. Thus, the diode keeps the MOSFET gate voltage within the limits set for reliable operation. The point of faliure is illustrated in Figure 5.13. Although the diode doesn't come into picture under normal operation, however, due to breakdown of the diode the V_{bias} input now has a short to ground through the substrate. Note that the diode was sized according to the metal antenna design rules set by the technology library and also passed Design Rule Check (DRC). However, it was unfortunate to still have the device fail.

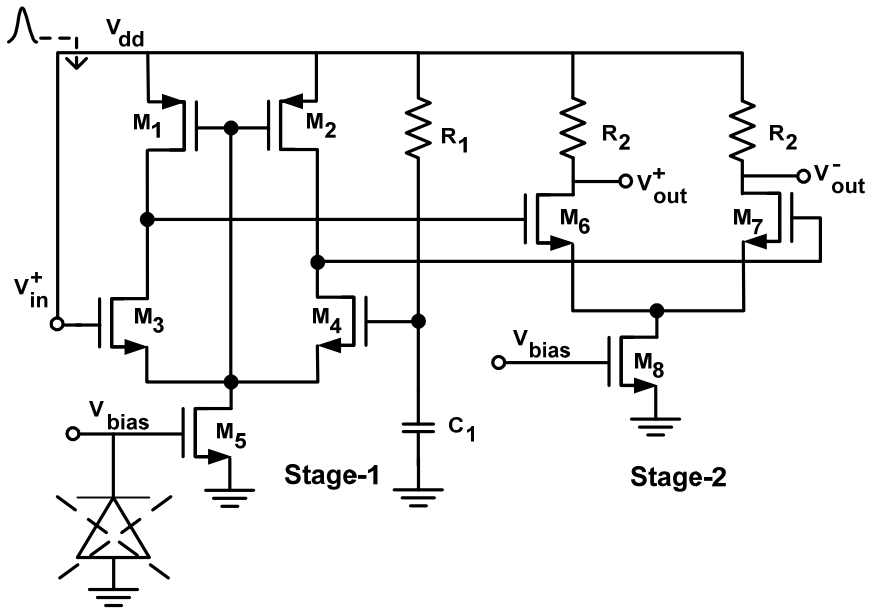

Figure 5.13: Point of test chip failure.

5.6 Chapter Summary

Proposed architecture and circuit design for data recovery block was presented in this chapter. Section 5.1 discussed the proposed CD receiver based architecture for data recovery block. The architecture has four main sub-blocks, namely, Sense and Amplify, Merged Mixer-Integrator, Template Generator and Comparator.

In section 5.2, circuit designs for each of the four sub-blocks of the architecture were discussed. Cadence simulations were used to verify the operation of data recovery block. Section 5.3, provided a summary of the simulation results obtained from Cadence. Simulation results indicated reliable operations of the proposed circuits across PVT variations. The power consumption of the proposed circuits is quite low – 3.58 mW.

In section 5.4, implementation of the test chip was discussed. Layout of the test-chip was described. Lastly, section 5.5 covered results of test chip fabrication.

Chapter 6

Conclusion and Future Work

A novel technique for the dual use of power line of a microprocessor for communicating data while simultaneously delivering power was previously proposed at VTVT [3], [4]. The technique proposed to use PDN to communicate data between an external Test/Control module and multiple transmitter/receiver nodes integrated inside a chip. Since PDN in a microprocessor is ubiquitous, therefore, the technique can be used to communicate data to any node located anywhere inside a chip.

The proposal opened a completely new area of research for PLC in VLSI systems. However, feasibility of the proposed scheme was a major concern and was extensively investigated through both modeling and measurement in the earlier work [7]. This thesis followed up from the previous work and used the measurement data to perform a study to evaluate PLC system performance in microprocessors. Further, a design for data recovery block was proposed. The design was done by taking into considerations, important factors like low power consumption, small area and ability to operate in noisy power line conditions in microprocessors.

6.1 Conclusion

The system level study modeled the microprocessor level PLC system using MATLAB. PDN channel was modeled using measurement data. Impulse-UWB with Gaussian pulse shapes was employed for communication. The system utilized BPSK modulation scheme and employed coding to reduce the required received pulse amplitude in order to achieve a desired BER.

Numerical analysis, based on theoretical analysis, and Monte Carlo simulations were done using MATLAB. The results of both types of simulations were found to match.

The simulation results establish that at a given received pulse amplitude there is an optimal pulse width, in the range of 1 ns to 1.5 ns, for which BER is minimized. The simulations also demonstrate that by employing DSSS small received pulse amplitude of just 5 mV to 10 mV can achieve a desired BER of 10^{-10}, while communicating data over a noisy power line. Received pulse amplitude of just 10 mV on a microprocessor's power line is smaller than the power line voltage (V_{dd}) fluctuation budget of ±5 % (where V_{dd} is 0.8 V or higher). This indicates that the PLC scheme can be implemented without disturbing the integrity of power line. However, achievable data rate is quite low, of the order of few 100 KHz to a few MHz. Therefore, implementation of parallel scan chains, initially proposed as an application of microprocessor level PLC, is currently not feasible and requires further research. However, possibility of communicating data through PDN even at a low data rate opens up a broad range of applications for implementing distributed sensing and control in microprocessors. Some of the possible applications of this technique are discussed in section 6.2.

Second aspect of this thesis involved design of data recovery block. The design constraints were to minimize circuit complexity, area and power consumption, while ensuring reliable operation in a noisy power line condition. CD receiver architecture was chosen for data recovery block. Circuit designs of various sub-blocks of data recovery block were presented in Chapter 5. Data recovery block, implemented in IBM 0.13 µm CMOS process, is shown to operate reliably across process corners with a 1.2 V power supply voltage and consumes 3.58 mW power.

Overall, the thesis work has contributed to the field of PLC in microprocessors in two ways. Firstly, it has been shown that it is indeed feasible to do PLC in microprocessors without disturbing the power line integrity. Further, it has been shown that simple and low power consuming circuits can be used to detect short duration pulses from a noisy power line. Although, the currently achievable data rate is low, still the PLC scheme is extremely attractive for distributed sensing and control in microprocessors. These applications will be discussed next.

6.2 Applications

PLC in microprocessors has numerous applications for testing and monitoring. There are applications in post-manufacture testing and in on-line or off-line system monitoring and control. The need for such type of monitoring and control is increasing with silicon process technology scaling into deep-deep sub-micron. A few application scenarios are discussed below:

1. *Monitoring and repair of aging defects*

MOS transistors suffer from usage based aging which leads to chip failures over time. The current design techniques assume design margins, to ensure reliable operation over a microprocessor's life time. However, these aging effects are expected to worsen with silicon technology scaling such that it will become impossible to include their impact within design margins in future designs [37]. Therefore, future microprocessors will require monitoring of these aging effects and thereby, self or controlled adaptation of the microprocessor circuits to optimize the overall performance. This kind of adaption will require monitoring and hence multiple sensors will be required in the microprocessor, which can sense aging effects [38]. PLC can provide an effective means of communication of the sensor data to be aggregated on-chip or off-chip for prediction of anomalies.

2. *Temperature dependent clock delay compensation*

With growing complexity of microprocessor, temperature gradients across a microprocessor die are becoming more prominent [39]. Further, these temperature gradients vary with the operating ambient conditions of the die and also with the operating load of different blocks of a microprocessor. These temperature variations lead to both spatial as well as temporal variations of temperature in a microprocessor due. These temperature variations are transformed into corresponding spatial and temporal variations of delay in the clock distribution network. Thus, use of tuned delay elements in clock trees have been proposed in [40]. However, need of dynamically tuned clock tree has been stressed and proposed in [39]. Implementation of such dynamically tuned clock trees requires distributed temperature sensing across the chip, hence demanding multiple temperature sensors in a die. PLC can be used to avoid the routing overhead associated with such integrated temperature sensors, thus giving freedom to designers in choosing number and placement of such sensors.

3. Temperature aware power management

Inclusion of on-chip temperature sensors to guard against excessive heating in case of failure of heat removal mechanisms has been known for quite some time. However, need has been felt to actually monitor the chip temperature online. Such monitoring has been proposed to adaptively control clock frequency and power supply to reduce the design constraints on microprocessor thermal heat removal systems. Moreover, need for distributed on-chip temperature monitoring has been proposed for such kind of power management systems [41]. Again, PLC is very attractive for implementation of these distributed on-chip temperature sensing systems.

4. Critical path time monitoring

Large process variations in deep sub-micron CMOS causes large chip to chip variations in the delay of critical path. Accounting for these variations in design margins will lead to overly conservative performance. The deep sub-micron circuits also suffer from higher sensitivity to temperature and voltage variations. Therefore, it has been proposed to integrate critical path timing monitors in high performance microprocessors [42]. Such monitors can measure critical path delays in either on-line or off-line modes and can be used to properly choose chip operating frequency. PLC is highly suitable for aggregating critical path timing data from such sensors for both post-manufacture microprocessor die characterization and for on-line adaptive clock frequency management.

The application examples provided above form a small set of possible applications of PLC in microprocessors. The overall theme of these applications is that PLC can provide a communication medium for distributed sensing and control in microprocessors. Such sensing and control is going to be a crucial requirement for reliable operation of high complexity microprocessors in near future.

6.3 Future Work

PLC in microprocessors is a new concept. The research is still in nascent stages and a number of avenues for future research exist. The possible research directions are:

a. The PDN channel needs to be further characterized using more measurements. Such measurements can help in the development of probabilistic channel models, as used in any conventional communication system.

b. Improvements are required in analytical modeling of a microprocessor's PDN. The models need not be precisely accurate; however, they should broadly predict the trend in the frequency response of a microprocessor's PDN. The effect of system board needs to be included in the PDN channel model.

c. Work also needs to be done at the system level. Issues relating to integration of PLC transmitters and receiver in a microprocessor system needs to be investigated. An actual demonstration of a working prototype PLC in a microprocessor test run can go a long way in this direction.

d. MAC layer protocols from wireless communication and computer networking fields need to be studied and adopted for the PLC scheme.

e. The concept of PLC in VLSI system has a broad range of applications. At this early stage of research focus can be shifted to simpler VLSI systems, where new and novel applications of the PLC scheme can be thought of.

Considering the large number of possible applications of PLC in VLSI system, the above mentioned research avenues outline an exciting path for advancements in this field. The work presented in this thesis will serve as an important reference for future work.

Bibliography

[1] "Intel Microprocessor Quick Reference Guide", http://www.intel.com/pressroom/kits/quickreffam.htm, retrieved on Aug 16th, 2009.

[2] T. Austin, V. Bertacco, S. Mahlke, C. Yu, "Reliable Systems on Unreliable Fabrics", IEEE Design & Test of Computers, Vol. 25, Issue 4, pp. 0 - 10, July 2008.

[3] W. C. Chung, D. S. Ha, and H. J. Lee, "Dual use of power lines for data communications in a system-on-chip environment," Proceedings of IEEE International Symposium on Circuits and Systems, Vol. 4, pp. 3355-3358, May 2005.

[4] W. C. Chung, and D. S. Ha, "A new approach for massive parallel scan design," Proceedings of IEEE International Test Conference, pp. 497-506, November 2005.

[5] R. Thirugnanam, D.S. Ha, and T. M. Mak, "On Channel Modeling for Impulse-Based Communications over a Microprocessor's Power Distribution Network," International Symposium on Power Line Communications, pp. 355-359, March 2007.

[6] V. Chawla and D. S. Ha, "On feasibility study for power line communications in microprocessors", TBD journal, manuscript submitted on xxxx date.

[7] R. Thirugnanam, "The dual use of power distribution networks for data communications in high speed integrated circuits," Ph.D. dissertation, Department of Electrical and Computer Engineering, Virginia Tech, 2006.

[8] U.S. Federal Communications Commission, FCC Revision of part 15 of the commission's rules regarding ultra-wideband transmission systems: First report and order. Technical report, Feb. 2002.

[9] U.S. Federal Communications Commission, Part 15 – Radio frequency Devices, Dec. 8, 2003, Available: http://www.fcc.gov/oet/info/rules/part15/part15_12_8_03.pdf.

[10] IEEE Computer Society, (August 31, 2007). IEEE Standard 802.15.4a-2007. New York,

NY: IEEE.

[11] J. H. Reed (Editor), “An introduction to ultra wideband communication systems,” Prentice Hall, 2005.

[12] John G. Proakis, “Digital communications,” McGraw-Hill Higher Education, 4th Ed. 2000.

[13] I. D. O’Donnell, and R. W. Brodersen, “A 2.3 mW Baseband Impulse-UWB Transceiver Front-End in CMOS,” Symposium on VLSI Circuits, pp. 200-201, 2006.

[14] J, Ryckaert, M. Verhelst, M. Badaroglu, S. D'Amico, V. De Heyn, C. Desset, P. Nuzzo, B. Van Poucke, P. Wambacq, A. Baschirotto, W. Dehaene, and G. Van der Plas, "A CMOS Ultra-Wideband Receiver for Low Data-Rate Communication," IEEE Journal of Solid-State Circuits, vol. 42, No. 11, pp. 2515-2527, Nov. 2007.

[15] M. Swaminathan, A. E. Engin, "Power Integrity Modeling and Design for Semiconductors and Systems", Prentice Hall, November 2007.

[16] P. Muthana, M. Swaminathan, E. Engin, P. M. Raj, T. Rao, “Mid frequency decoupling using embedded decoupling capacitors”, IEEE Topical Meeting on Electrical Performance of Electronic Packaging Meeting, pp. 271-274, October 2005.

[17] M. Horowitz, E. Alon, D. Patil, S. Naffziger, R. Kumar, K. Bernstein, “Scaling, power, and the future of CMOS”, IEEE International Electron Devices Meeting, pp. 7-15, December 2005.

[18] D. E. Lackey, P. S. Zuchowski, T. R. Bednar, D. W. Stout, S. W. Gould, J. M. Cohn, “Managing power and performance for System-on-Chip designs using Voltage Islands”, IEEE International Conference on Computer-aided Design, pp. 195-202, November 2002.

[19] P. E. Gronowski, W. J. Bowhill, R. P. Preston, M. K. Gowan, R. L. Allmon, “High-performance microprocessor design”, IEEE Journal of Solid-State Circuits, pp. 676-678, May 1998.

[20] D. M. Hockanson, J. T. Dibene II, "Power Delivery for High Performance Packages, Part I", IEEE International Symposium on Electromagnetic Compatibility, pp. 1-6, July 2007.

[21] N. Na, J. Choi, M. Swaminathan, J. R. Libous, D. P. O'Connor, "Modeling and simulation of core switching noise for ASICs", IEEE Transactions on Advanced Packaging, pp. 4-11, February 2002.

[22] N. Na, J. Choi, S. Chun, M. Swaminathan, J. Srinivasan, "Modeling and Transient Simulation of Planes in Electronic Packages", IEEE Transactions On Advanced Packaging, VOL. 23, NO. 3, pp 340 – 352, August 2000.

[23] O. P. Mandhana, J. Zhao, "Comparisons study on effectiveness of on-chip, onpackage and PCB decoupling for core noise reduction by using broadband power delivery network models," IEEE Electronic Components and Technology Conference, pp. 732-739, 2005.

[24] R. Dutta and M. Marek-Sadowska, "Automatic sizing of power/ground (P/G) networks in VLSI," IEEE Design Automation Conference, pp. 783-786, 1989.

[25] S.-W. Wu and Y.-W. Chang, "Efficient power/ground network analysis for power integrity-driven design methodology," IEEE Design Automation Conference, pp. 177-180, 2004.

[26] H. B. Bakoglu, Circuits, interconnections, and packaging for VLSI, Addison-Wesley Publishing Co., 1990.

[27] N. V. D. Meijs and J.T. Fokkema, "VLSI circuit reconstruction from mask topology Integration", Vol. 2, No. 2, pp. 85-119, 1984.

[28] Picoprobes are available at http://www.ggb.com.

[29] S. Naffziger, B. Stackhouse, T. Grutkowski, D. Josephson, J. Desai, E. Alon and M. Horowitz, "The Implementation of a 2-Core, Multi-Threaded Itanium Family Processor," IEEE Journal of Solid-State Circuits, Vol. 41, pp. 197-209, January 2006.

[30] E. Alon, V. Stojanovic, and M. A. Horowitz, "Circuits and techniques for high-resolution measurement of on-chip power supply noise," IEEE Journal of Solid State Circuits, Vol. 40, No. 4, April 2005.

[31] M.T. Terrovitis, K.S. Kundert, R.G. Meyer, "Cyclostationary noise in radio-frequency communication systems", IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, Vol. 49, Issue 11, pp. 1666-1671, Novermber 2002.

[32] Q. K. Zhu, “Power distribution network design for VLSI”, N. J. Hoboken, Wiley-Interscience, 2004.

[33] H. Wang, Q. Zhang, N. Zhang and X. Sha, “Pulse Shaping for UWB Communications in Dense Multipath,” International Conference on Innovative Computing, Information and Control, Vol. 2, pp: 714-717, August 2006.

[34] P. Heydari, “A study of low-power ultra wideband radio transceiver architectures,” IEEE Wireless Communication and Networking Conference, pp. 758-763, Match 2005.

[35] M. Saint-Laurent and M. Swaminathan, "Impact of power-supply noise on timing in high-frequency microprocessors", IEEE Transactions on Advanced Packaging, Vol. 27, Issue 1, pp. 135 - 144, February 2004.

[36] V. Chawla, R. Thirugnanam, D.S. Ha, and T.M. Mak, "Design of a Data Recovery Block for Communications over Power Distribution Networks of Microprocessors,” International Conference on Circuits & Systems for Communications, pp. 708 – 712, May 2008.

[37] S. Borkar, “Designing Reliable Systems from Unreliable Components,” IEEE Micro, Vol. 25, Issue 6, pp. 10 – 16, Nov.-Dec., 2005.

[38] M. Agarwal, B.C. Paul, Z. Ming, S. Mitra, "Circuit Failure Prediction and Its Application to Transistor Aging", IEEE VLSI Test Symposium, pp. 277 - 286, May 2007.

[39] A. Chakraborty, K. Duraisami, A. Sathanur, P. Sithambaram, L. Benini, A. Macii, E. Macii and M. Poncino, "Dynamic Thermal Clock Skew Compensation Using Tunable Delay Buffers", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 16, Issue 6, pp. 639 - 649, June 2008.

[40] J.-L. Tsai, D. Baik, C. C.-P. Chen, and K. K. Saluja, “A yield improvement methodology using pre- and post-silicon statistical clock scheduling”, IEEE/ACM International Conference Computer-Aided Design, pp. 611–618, November 2004.

[41] D. Brooks and M. Martonosi, “Dynamic thermal management for high performance microprocessors”, IEEE International Symposium on High-Performance Computer Architecture, pp. 171–182, January 2001.

[42] A. Drake, R. Senger, H. Deogun, G. Carpenter, S. Ghiasi, T. Nguyen, N. James, M. Floyd and V. Pokala, "A Distributed Critical-Path Timing Monitor for a 65nm High-Performance Microprocessor", IEEE International Solid-State Circuits Conference, pp. 398 - 399, February 2007.