CHAPTER 2

MULTILEVEL VOLTAGE SOURCE INVERTER USING CASCADED-INVERTERS WITH SEPARATED DC SOURCES

The structure of the multilevel inverter using cascaded-inverters with separated dc sources will be introduced in this chapter, as well as switching pattern.

2.1 Full-bridge or "H-bridge" Voltage Source Inverter

2.1.1 Introduction

The smallest number of voltage levels for a multilevel inverter using cascaded-inverter with SDCSs is three. To achieve a three-level waveform, a single full-bridge inverter is employed. Basically, a full-bridge inverter is known as an H-bridge cell, which is illustrated in Fig. 2.1. The inverter circuit consists of four main switches and four freewheeling diodes.

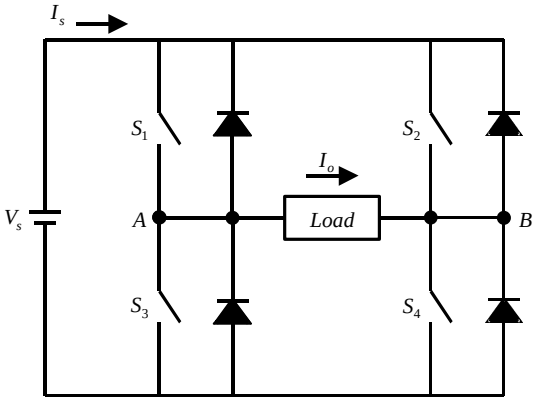


Figure 2.1 An H-bridge cell.

2.1.2 Gate Signal and Inverter Operation

According to four-switch combination, three output voltage levels, +V, -V, and 0, can be synthesized for the voltage across A and B. During inverter operation shown in Fig. 2.1, switch of S_1 and S_4 are closed at the same time to provide V_{AB} a positive value and a current path for I_o. Switch S_2 and S_4 are turned on to provide V_{AB} a negative value with a path for I_o. Depending on the load current angle, the current may flow through the main switch or the freewheeling diodes. When all switches are turned off, the current will flow through the freewheeling diodes.

In case of zero level, there are two possible switching patterns to synthesize zero level, for example, 1) S_1 and S_2 on, S_3 and S_4 off, and 2) S_1 and S_2 off and S_3 and S_4 on.

A simple gate signal, repeated zero-level patterns, is shown in Fig. 2.2. All zero levels are generated by turning on S_1 and S_2.

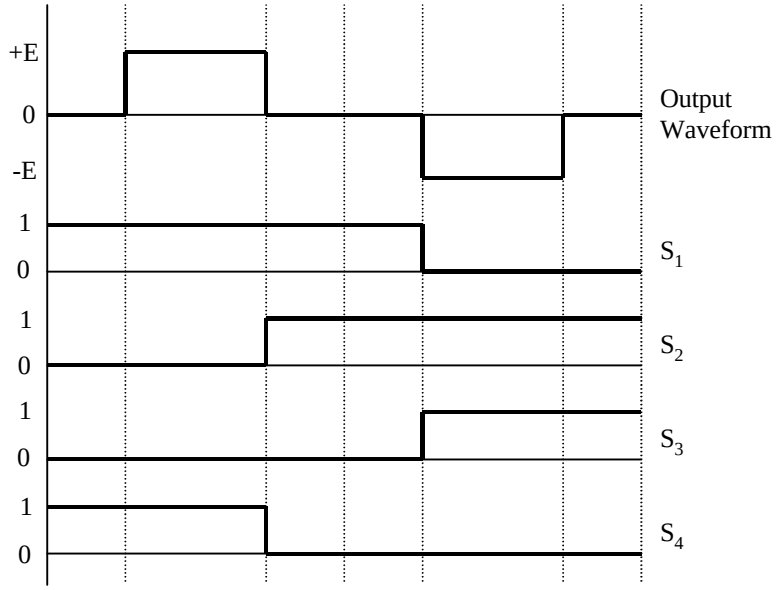


Figure 2.2 Repeated zero-level switching pattern.

Note that level 1 represents the state when the gate is turned on, and level 0 represents the state when the gate is turned off. In Fig. 2.1, S_1 and S_2 are turned on longer than S_3 and S_4 do in each cycle because the same zero level switching pattern is used. As a result, S_1 and S_2 are consuming more power and getting higher temperature than the other two switches. To avoid such a problem, a different switching pattern for zero level is applied. In the first zero stage, S_1 and S_2 are turned on; then, in the second zero stage, S_3 and S_4 are turned on in stead of S_1 and S_2. By applying this method, turn-on time for each switch turns out to be equal, a shown in Fig. 2.3. This switching pattern will be used for experimental verification in this thesis.

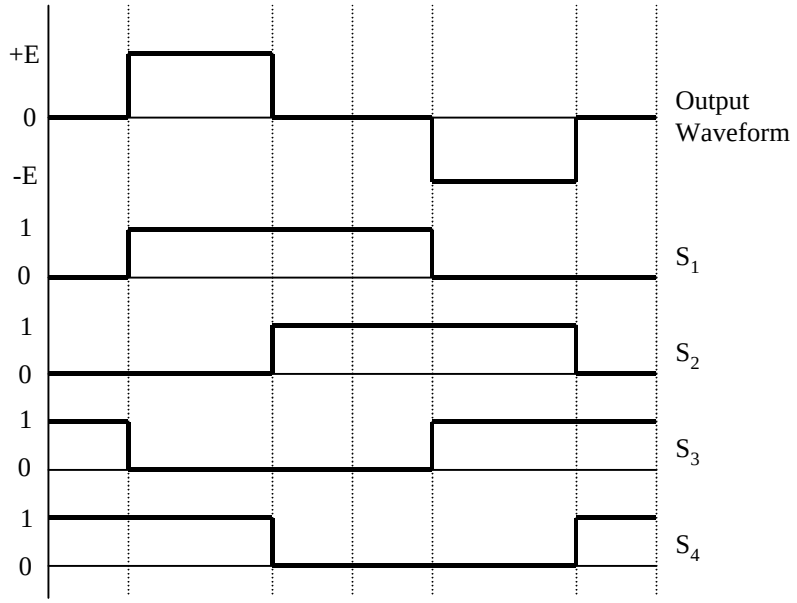


Figure 2.3 Swapped zero-level switching pattern.

2.1.3 Blanking Time

Another issue that has to be concerned is providing blanking time for gate signal. In 2.1.2, the switches were assumed to be ideal, which allowed the state of the two switches in an inverter leg to change simultaneously from on to off and vice versa. In practice, switching devices are not ideal. To completely turn-off the devices, a short period, which depends on the type of the device, is needed. Usually, because of the finite turn-off and turn-on times associated with any types of switch, a switch is turned off at the switching time instant. However, the turn-on of the other switching in that inverter leg is delayed by a blanking time, t_Δ, which is conservatively chosen to avoid cross-conduction current through the leg. A blanking time concept is illustrated in Fig 2.4. The leg of S_1 and S_3 are used as an example.

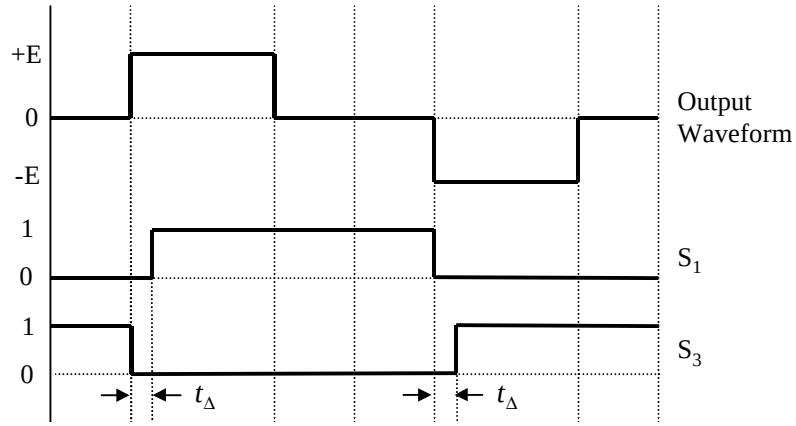


Figure 2.4 Apply blanking time to the gate signal.

2.2 Cascade Inverter Configuration

2.2.1 Single-Phase Structure

To synthesize a multilevel waveform, the ac output of each of the different level H-bridge cells is connected in series. The synthesized voltage waveform is, therefore, the sum of the inverter outputs. The number of output phase voltage levels in a cascaded-inverter is defined by

$$m = 2s + 1$$

where s is the number of dc sources. (2.1)

For example, a nine-level output phase voltage waveform can be obtained with four-separated dc sources and four H-bridge cells. Fig 2.5 shows a general single-phase m-level cascaded inverter.

From Fig. 2.5, the phase voltage is the sum of each H-bridge outputs and is given as

$$V_{AN} = V_{dc1} + V_{dc2} + ... + V_{dc(S-1)} + V_{dcS} \quad (2.2)$$

Because zero voltage is common for all inverter outputs, the total level of output voltage waveform becomes $2s+1$. An example phase voltage waveform for a nine-level cascaded inverter and all H-bridge cell output waveforms are shown in Fig. 2.6. In this thesis, all dc voltage are assumed to be equal, i.e., $V_{dc1} = V_{dc2} = ... = V_{dc(S-1)} = V_{dcS} = V_{dc}$.

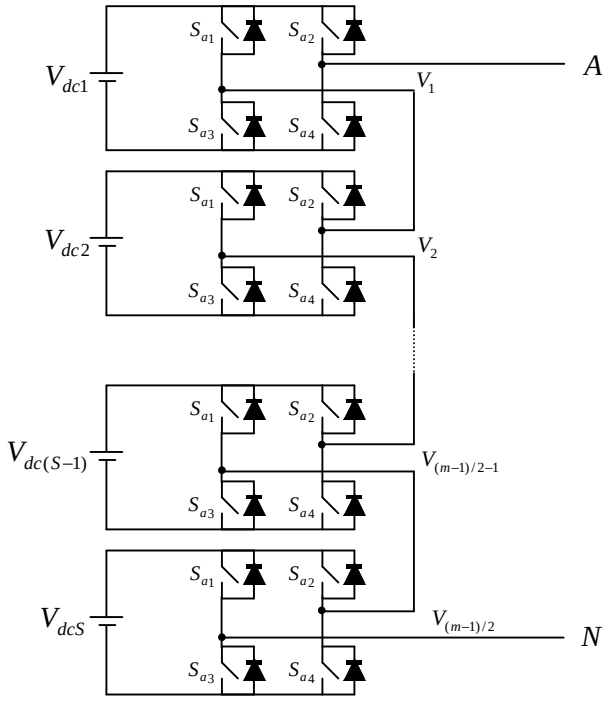


Figure 2.5 Single-phase configuration of an m-level cascaded inverter.

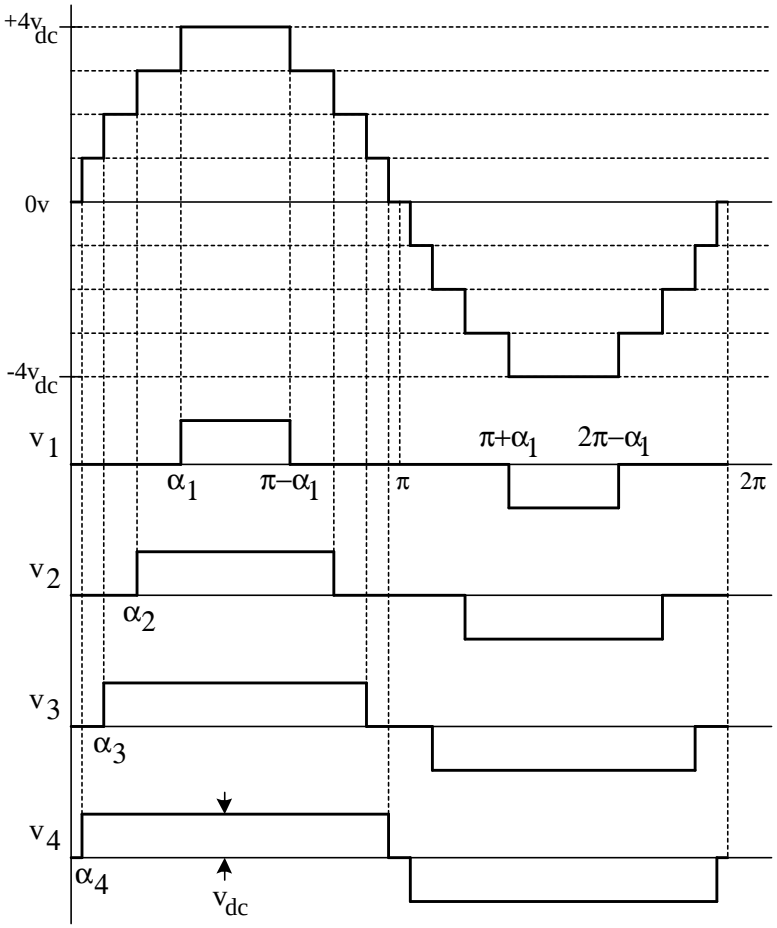


Figure 2.6 Waveform showing a nine-level output phase voltage and each H-bridge output voltage.

According to sinusoidal-liked waveform, each H-bridge output waveform must be quarter-symmetric as illustrated by V_1 waveform in Fig. 2.6. Obviously, no even harmonic components are available in such a waveform. To minimize THD, all switching angles will be numerically calculated, which will be proposed in chapter 4.

2.2.2 Three-Phase Structure

For a three-phase system, the output of three identical structure of single-phase cascaded inverter can be connected in either wye or delta configuration. Fig 2.7 illustrates the schematic diagram of wye-connected seven-level inverter using three H-bridge cells and three SDCSs per phase, which will be used to verify the concept of the optimized harmonic stepped-waveform technique in chapter 6.

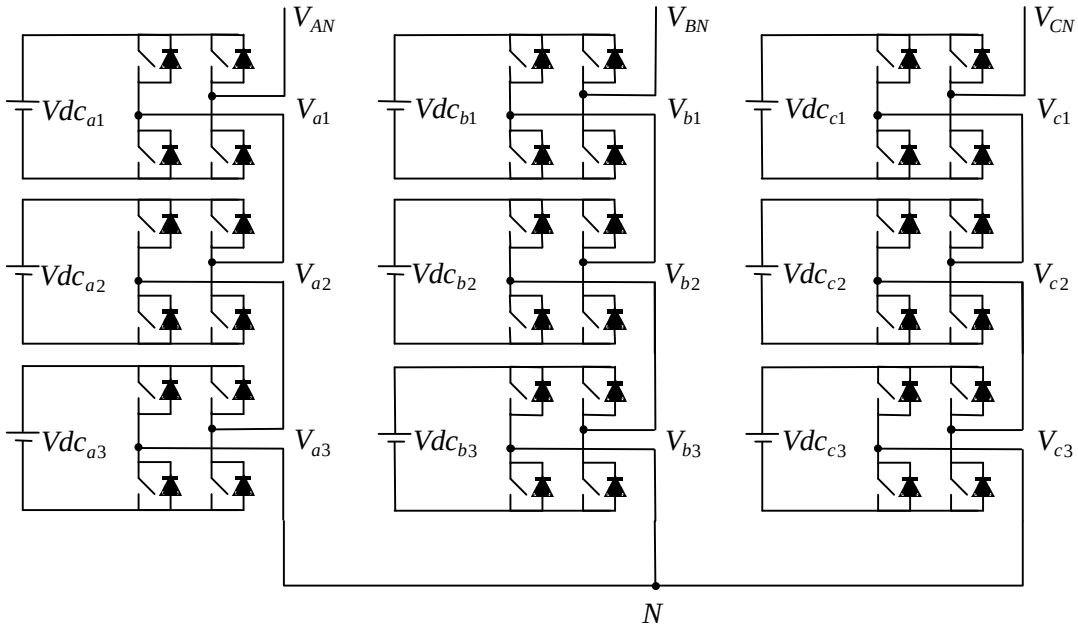


Figure 2.7 Three-phase seven-level inverter using cascaded-inverters with SDCSs.

From Fig 2.7, V_{AN} is voltage of phase A, which is the sum of V_{a1}, V_{a2}, and V_{a3}. The same idea is applied to phase B and phase C. To synthesize seven-level phase voltage, three firing angles are required. The same three switching angles can be used in all three phase with delaying 0, 120, and 240 electrical degree for phase A, B, and C, respectively.

According to three-phase theory, line voltage can be expressed in term of two-phase voltages. For example, the potential between phase A and B is so-called V_{AB}, which can be written as follows:

$$V_{AB} = V_{AN} - V_{BN} \tag{2.3}$$

where

V_{AB} is line voltage

V_{AN} is voltage of phase A with respect to point N

and V_{BN} is voltage of phase B with respect to point N

Theoretically, the maximum number of line voltage levels is 2m-1, where m is the number of phase voltage levels. The number of line voltage level depends on the modulation index and the given harmonics to be eliminated. The seven-level cascaded inverter, for example, can synthesize up to thirteen-level line voltage.

The advantage of three-phase system is that all triplen harmonic components in the line voltage will be eliminated by one-third cycle phase shift feature. Therefore, only non-triplen harmonic components need to be eliminated from phase voltage. In single-phase nine-level waveform, for example, the 3^{rd}, 5^{th}, and 7^{th} harmonics will be eliminated from output phase voltage. Compared to single-phase inverter, in three-phase nine-level inverter, the 5^{th}, 7^{th}, and 11^{th} harmonics will be eliminated from output phase voltage. Thus, the 9^{th} harmonic is the lowest harmonic component in phase voltage in single-phase system, while the 13^{th} harmonic is the lowest harmonic component appearing in line voltage of three-phase system.

Fig 2.8 shows output voltage of phase A, V_{AN}, and output voltage of phase B, $V_{BN,}$ line voltage waveform, V_{AB} of seven-level cascaded inverter in Fig 2.7.

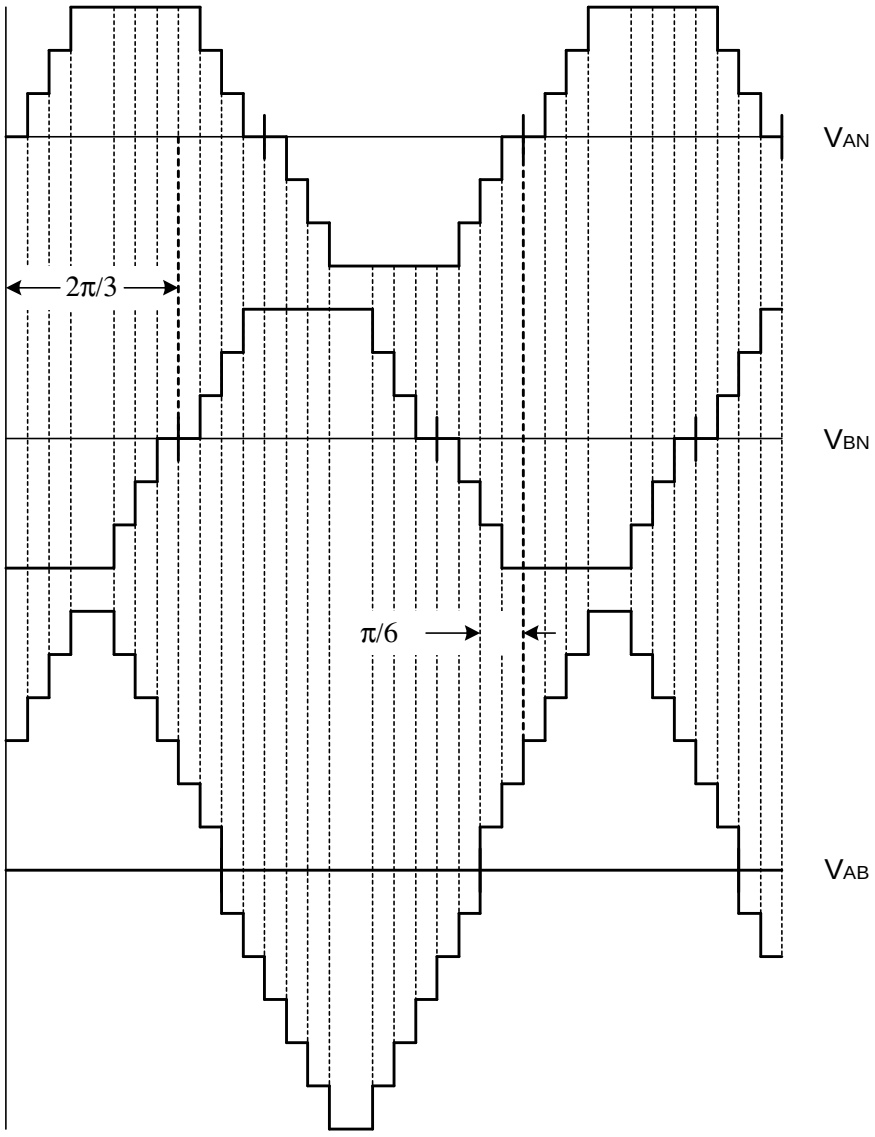
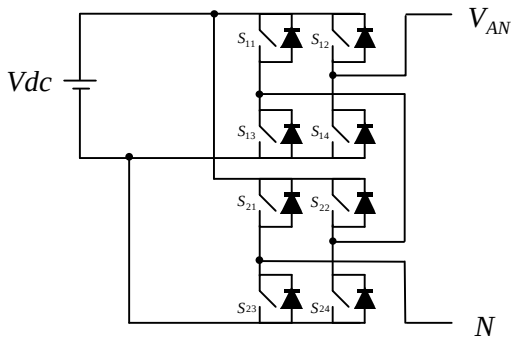


Figure 2.8 Two phase and line voltages of three-phase seven-level cascaded inverter in Fig. 2.7.

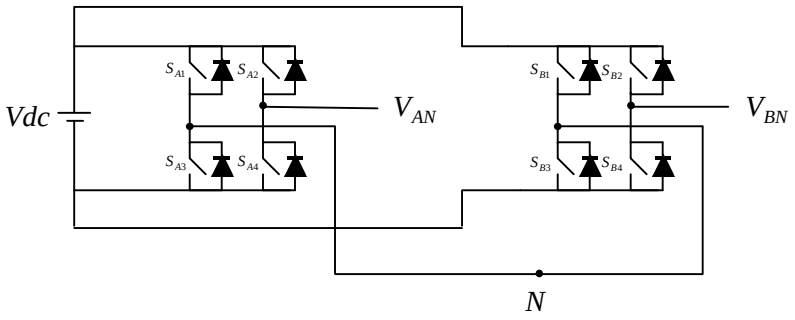
From Fig. 2.8, assuming the positive sequence three-phase system, output voltage of phase B lags output voltage of phase A by 120 electrical degree. The line voltage, V_{AB}, therefore, leads voltage of phase A by 30 electrical degree, which is according to the three-phase theory.

2.2.3 Separated DC Sources (SDCSs)

To avoid short circuit of dc sources, the separated dc source configuration is applied to the multilevel inverter using cascaded-inverter. This section will discuss about why cascaded inverter have to employ the separated dc sources (SDCSs). To explain this, two possible dc sources connections are assumed. In the first case, all H-bridge cells in the same leg share the same dc source. Another connection is that the same dc source is shared in the same level of each phase. Fig. 2.8(a) and 2.8(b) illustrate the first connection and the second connection of five-level cascaded inverter, respectively.



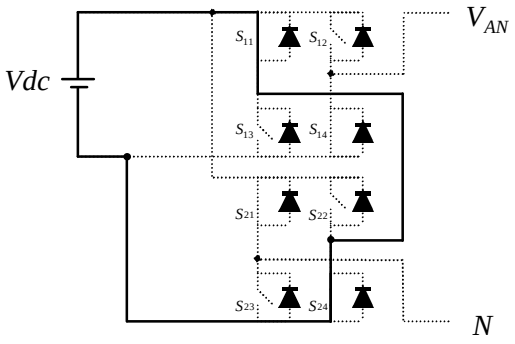
(a)



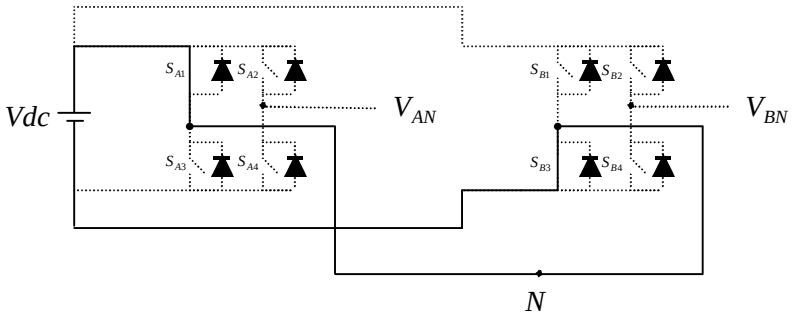
(b)

Figure 2.8 shows two possible dc source connections

To avoid confusing, both cases will be assumed that no self shoot-through described in 1.2 is possible. However, there are many combinations, which make short circuit happen. Therefore, one possibility of each case will be presented. In the first case, short circuit across the dc source exists when switches S_{11} and S_{24} are turned on simultaneously, which is illustrated in Fig. 2.9(a). Likewise, in the second connection, when switch S_{A1} and S_{B3} are on at the same time, which is shown in Fig. 2.9(b), short circuit will be happened.



(a)



(b)

Figure 2.9 shows a short circuit possibility of each case.

2.3 Conclusions

A full-bridge inverter or so-called H-bridge cell is introduced. Basically, an H-bridge cell can generate up to three output voltage levels. The appropriate gate control signal and blinking time are presented.

Multilevel inverter using cascaded-inverter with SDCSs are introduced in both single-phase and three-phase structure. The output voltage is the sum of the output voltage of each H-bridge cell. In three-phase system, the voltage THD can be improved in line voltage. Finally, the reason to use SDCSs is explained.

In the next chapter, the concept of the optimized harmonic stepped-waveform technique will be presented. Also, the procedure to find the switching angles for such a waveform will be proposed.