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APPENDICES

Appendix A.

A 7-level cascaded inverter circuit is implemented to verify the simulation results. In each phase leg, there are three H-bridge inverter circuits, which are connected in series as shown in Fig. A-1. The rated output of each power stage is 600V/6A.

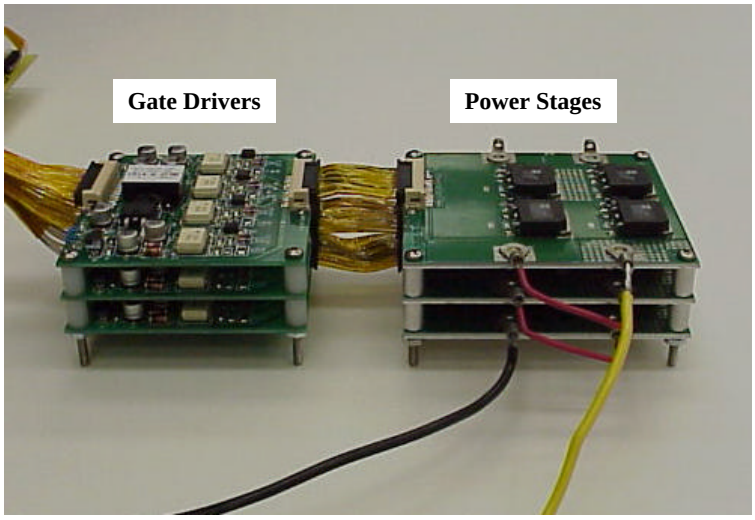

Figure A-1. Gate drivers and power stages of 7-level cascaded inverter.

The schematics of gate driver and H-bridge inverter are shown in Fig. A-2.

The control circuit board is shown in Fig. A-3. An 89AT51 is used as the main processor to generate gate signals.

All three-phase legs are shown in Fig. A-4. The system can synthesis up to 13 line voltage levels.

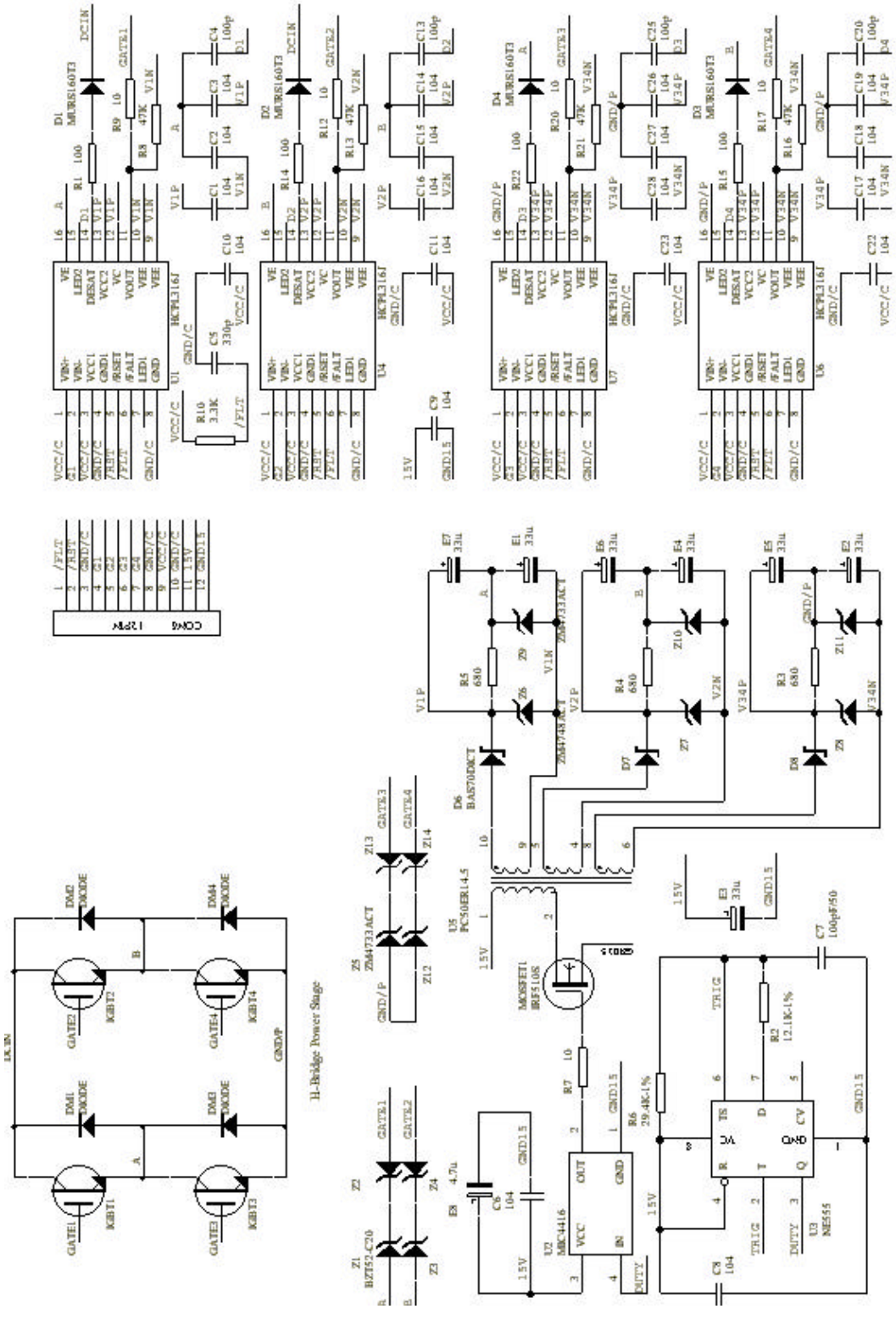

Figure A-2. Schematics of gate driver and H-bridge power stage.

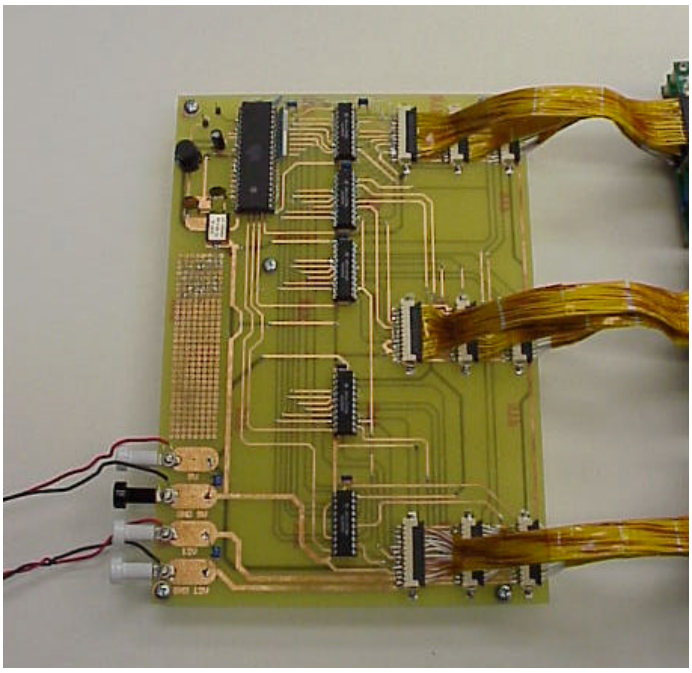

Figure A-3 Control circuit board.

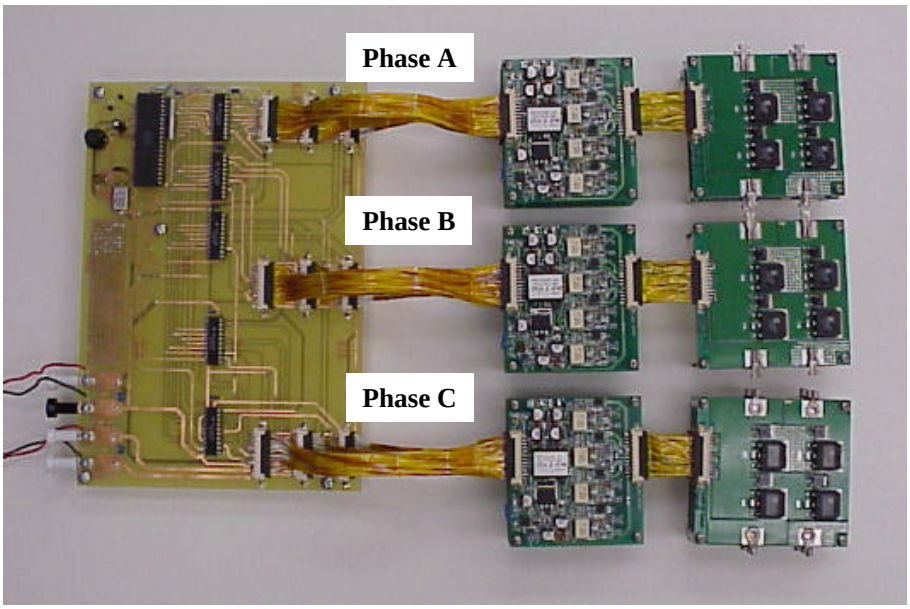

Figure A-4 Three phase of 7-level cascaded inverter.

Appendix B.

Used as an example, an m-file used to solve the switching angles of optimized harmonic stepped-waveform is presented as follows:

```
********************************************************************************
*   Solve switching angle of 11-level OHSW by using the Newton-Raphson method    *
********************************************************************************

clear all; close all;

E=5; %The number of dc sources
dM=0.001; %The modulation index step
Mstart=1.0; %The initial modulation index
M=Mstart*E;
Mrange=1000; %Range of calculation results

p1=34*pi/180; p2=44*pi/180; p3=54*pi/180; p4=65*pi/180; p5=77*pi/180;
% Guess initial value of switching angles

p=[p1 p2 p3 p4 p5]'; %The switching angle matrix

for j=1:Mrange
t=[M*pi/4 0 0 0 0]'; %The corresponding harmonic amplitude matrix
df=1; i=1;
while abs(df) > 1e-20 & i < 40 %i=40 %Degree of accuracy condition
   p1=p(1,:); p2=p(2,:); p3=p(3,:); p4=p(4,:); p5=p(5,:);
   f=[cos(p1)+cos(p2)+cos(p3)+cos(p4)+cos(p5);
      cos(5*p1)+cos(5*p2)+cos(5*p3)+cos(5*p4)+cos(5*p5);
      cos(7*p1)+cos(7*p2)+cos(7*p3)+cos(7*p4)+cos(7*p5);
      cos(11*p1)+cos(11*p2)+cos(11*p3)+cos(11*p4)+cos(11*p5); % The nonlinear system-
      cos(13*p1)+cos(13*p2)+cos(13*p3)+cos(13*p4)+cos(13*p5)]; % matrix
   delf=[-sin(p1) -sin(p2) -sin(p3) -sin(p4) -sin(p5);
         -5*sin(5*p1) -5*sin(5*p2) -5*sin(5*p3) -5*sin(5*p4) -5*sin(5*p5);
         -7*sin(7*p1) -7*sin(7*p2) -7*sin(7*p3) -7*sin(7*p4) -7*sin(7*p5);
         -11*sin(11*p1) -11*sin(11*p2) -11*sin(11*p3) -11*sin(11*p4) -11*sin(11*p5);
         -13*sin(13*p1) -13*sin(13*p2) -13*sin(13*p3) -13*sin(13*p4) -13*sin(13*p5)];
          % The differential matrix
   df=inv(delf)*(t-f); % Calculate solution error
   p=p+df; % Update the solutions.
   i=i+1;
end

mm(j)=M/E; % The modulation index
M=M-dM; %Update the modulation index
end

%--data for plotting--
figure(1);
pf1=abs(pf1); pf2=abs(pf2); pf3=abs(pf3); pf4=abs(pf4); pf5=abs(pf5); %Convert neg angle
to pos angle
plot(mm,pf1*180/pi,mm,pf2*180/pi,mm,pf3*180/pi,mm,pf4*180/pi,mm,pf5*180/pi);
axis([mm(Mrange) mm(1)  0 90]);

%--calculate phase THD--
for i=1:200 % Empty the harmonic matrix
   ha(i)=0;
   hindex(i)=i;
end

for j=1:length(pf1)
   sumh=0;
```

```
   sumhll=0;

   for i=1:100
      k=2*i-1; % k is odd number
      ha(k)=(cos(k*pf1)+cos(k*pf2)+cos(k*pf3)+cos(k*pf4)+cos(k*pf5))/k;
      % Calculate amplitude of harmonic amplitude
   end

   for i=2:200
      sumh=ha(i)^2+sumh;
   end
   THDph(j)=sqrt(sumh)/ha(1)*100; % Calculate phase voltage THD

   for i=2:100
      k=2*i-1;
      ck=round(sin(k*2*pi/3)); % Round towards nearest integer
      if ck ~= 0
         sumhll=sumhll+ha(k)^2;
      end
   end
   THDll(j)=sqrt(sumhll)/ha(1)*100; % Calculate line voltage THD

end

figure(2);
plot(M,THDph,'k:',M,THDll,'k');
title('The Voltage THD vs. The Modulation Index of 11-level OSHW');
xlabel('Modulation Index');
ylabel('THD (%)');
% End of File
```

VITA

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Siriroj Sirisukprasert was born in Nakhon Sawan, Thailand. He received his Bachelor degree in Electrical Engineering with first class honor from Kasetsart University, Thailand, in May 1996. Since then he has joined the department of Electrical Engineering at the same university as a lecturer member. In January 1997, he won the Thai Government Scholarship and pursued on his Masters degree in Electrical Engineering at the Bradley Department of Electrical and Computer Engineering at Virginia Tech. He has also joined an engineering research program at the Center for Power Electronics System (CPES) at Virginia Tech. His specific area is Power Electronics in high power applications. He is a member of IEEE.