IMPLEMENTATION OF A FIXED TIMING COUPLED INDUCTOR SOFT-SWITCHING INVERTER

By

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Abstract

In research environments, many soft switching inverters have been conceived, simulated, designed, implemented and proven to have advantages over hard switched inverters. To date however, no soft-switching inverters have reached commercial production for various reasons. The fixed timing coupled inductor soft-switching inverter is of interest because in simulation and previous implementation it exhibits load and source adaptability using simple RC timer circuitry and can be implemented with low cost active auxiliary devices. During the course of this implementation, it is noted that attempting to use excessively small/inexpensive active auxiliary devices has reliability ramifications related to device packaging. The issue of auxiliary active device reliability is conjectured upon by referencing available datasheet information, application specific requirements, device pulse testing and secondary research findings related to semiconductor failure characteristics. It is also noted that aspects of the simple fixed timing circuitry operation, in conjunction with coupled inductor and saturable inductor design, can lead to coupled inductor saturation if not properly addressed. Simulation is performed and validates various causes for this non-ideal behavior.

Acknowledgements

I would like to thank Dr. Jason Lai for his guidance; his technical expertise and ever present willingness to come in to the lab any day (even weekends or holidays) to improve his students' level of understanding of power electronics through hands-on experimentation assistance are duly noted and appreciated.

Special thanks are due to members of the FEEC particularly Mike Schenck who has been a true friend as well as a valued colleague and Dr. Huijie Yu whom developed many of the basic and advanced concepts of this soft switching inverter. Special thanks also goes to Dr. Jaime De La Ree as a friend and an excellent educator, who always keeps every one of his students actively engaged in a classroom setting – truly a difficult task (madly waving his hands describing Lenz's law and then pointing to students and demanding that they tell him what field is where and what currents are flowing in what direction). I would also like to thank Dr. Ramu for his review of this document and constructive suggestions.

I would like to thank the authors of all cited work for their contribution to the field. Without their tireless work and passion for advancing the field of power electronics through publication, this work would have never been possible.

Lastly, I would like to thank my wonderful, understanding and supportive wife Kym whom implicitly believes in my abilities and fosters my passion for advanced technology and entrepreneurship.

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Chapter 1 - Introduction

1.1 Motivation

Power electronics are an enabling technology and interface multiple systems with different requirements. As such, constraints are applied to power electronics systems by outside variables such as the load, source, environmental factors, life span requirements, packaging and cost; all of these must be weighed and balanced to create an optimal power electronics solution for an application. Soft-switching topologies offer the promise of increasing power density, reducing life cycle costs, and reducing the detrimental effects of electromagnetic interference (EMI) on any vulnerable electronics.

1.2 Application Specifications

This thesis is tailored to the implementation of one phase-leg of a three-phase inverter for a 150Hp magnetic bearing permanent magnet (PM) machine. In recent years, this type of machine has been developed for HVAC compressor applications such as air-conditioning, heating and refrigeration. In this application, the motor drive is mounted in close proximity to many other electronic components such as control circuitry, sensors, and magnetic bearings which when exposed to high levels of EMI can have harmful effects [1] [2]. The overall system is desired to have a high efficiency, high power density, and high reliability while maintaining comparable cost to the hard switched inverter. This application bodes well for implementing a soft-switching inverter technology. Additional design criterion imposed includes:

- The soft-switching has to utilize the pre-existing inverter control scheme.
- The soft-switching inverter must fit the form factor of the previous inverter.
- Modifications to the main buss bar construction and DC link capacitors undesired.

1.3 Soft-switching inverters

Soft-switching inverters are of keen interest to researchers and product designers alike for their many beneficial characteristics. Many papers have been written on soft switching inverters describing the characteristics of various different topologies. Though

various topologies excel in different areas, the general family of soft-switching inverters has several possible advantages over traditional hard-switching inverters.

- Higher efficiency – Soft-switching inverters significantly reduce the amount of switching loss in power semiconductor switches and make efficiency less dependent on switching frequency.
- Harmonics and audible noise reduction – If increases in switching frequency are made, the harmonic filtering becomes easier. Additionally, above 18 kHz there is no longer any audible noise from the power electronics [3].
- Increased power density – The use of smaller main switch die size is possible because lower switching losses will result in lower device junction temperatures for a given average load current. The efficiency improvements ideally lead to higher power density and smaller cooling system size, but the additional space required for auxiliary components may negate any such benefits.
- Increased switch utilization – Voltage overshoot is reduced and current spikes are minimized allowing the use of switches with lower peak voltage and current ratings.
- Decreased EMI – A normal hard switching application intrinsically has high EMI associated with the high di/dt and dv/dt of the switching process caused by the rapid turn-on and turn-off of the power semiconductors. The rate of these rapid changes can be reduced using soft-switching, reducing EMI.

These aforementioned points are highly desirable characteristics in some applications and considered unimportant in others. This is especially important to take into consideration when considering the drawbacks of soft-switching converters as well as their benefits. Some prominent production design holdups are:

- Increased component count – soft switching inverters require additional components which increase supply management issues, circuit layout complexity and the overall number of possible failure points in the inverter.
- Increased cost – The soft switching inverter will likely cost more in production than a hard switching inverter due to increased components.

- Design and control complexity – Many soft switching inverters have complex operations that differ from a traditional inverter. This extra complexity usually involves additional control circuitry. Additionally, the overall design process will take longer than the traditional inverter leading to higher engineering costs.
- Reliability questions - Soft switching inverters by nature are not inherently unreliable, but since there are no soft switching inverters in production there is not significant information available about the long term reliability of soft switching inverters in various applications.

1.3.1 Various Soft-Switching Inverter Topologies

Though there are many various soft switching inverter topologies, they can be classified into three major groups. The three major classifications of soft-switching inverters are load resonant, resonant transition and resonant link. They can be further classified based on the location and type of the additional components needed for soft switching (active/passive) and the soft switching waveform characteristics: ZVS (zero voltage switching) or ZCS (zero current switching).

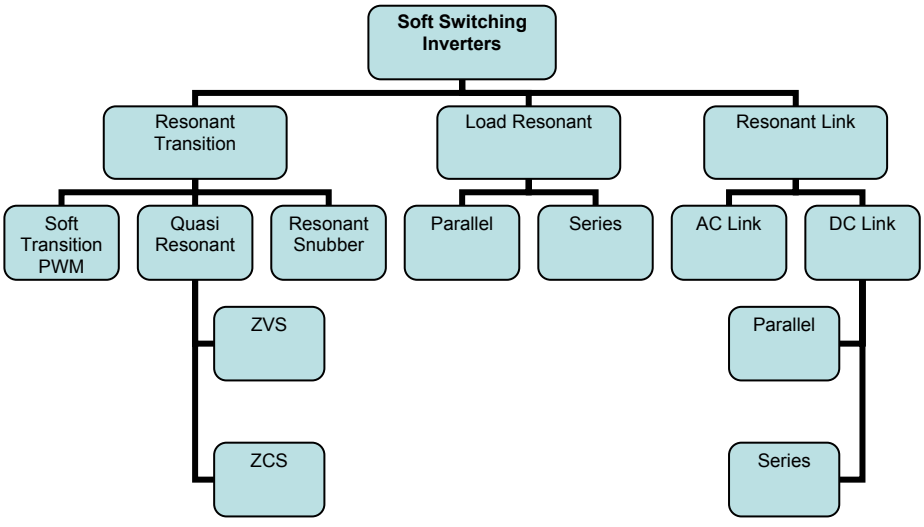


Figure 1 Soft Switching Classification

This classification system and many topologies are further described in detail in [3]. Typically, the topologies of interest for motor drive application are resonant dc link

inverters, and resonant transition ZVS and ZCS inverters. Load resonant inverters are not of interest mainly because they have poor load regulation associated with any change in load inductance; a common occurrence when driving a motor.

1.3.1.1 Resonant Link Inverters

Despite generally low auxiliary component count and compact size, some resonant link inverters such as the Resonant DC Link (RDCL) inverter [4] [5] and the Passive Clamped Quasi-Resonant Link (PCQRL) inverter [6] require a modified control schemes or use an inductor in the main power path and do not fit aforementioned application specific criteria. The resonant link construction is typically simpler than other types of soft-switching inverters, but also effectively requires modification to a higher switching frequency to obtain similar output resolution [7].

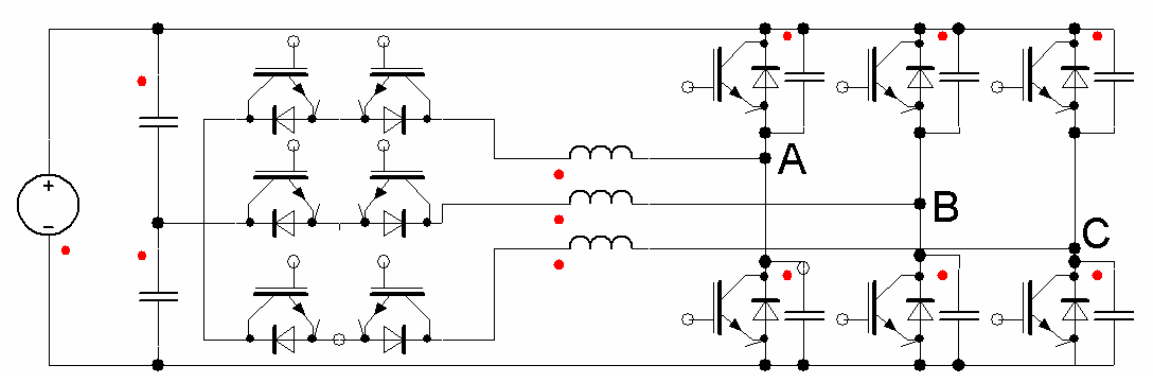
1.3.1.2 Resonant transition inverters

There are many different resonant transition inverters both of the ZVS and ZCS type. Like some DC link inverters, many resonant transition inverters require modified control schemes for proper operation and load adaptability. Some promising topologies for high efficiency that meet the application specific criterion are the ARCP [8 9], ZCS 6-switch [10], ZCS 3-switch [11] and ZVS 6-switch Coupled Inductor [18 23 24] inverters. There are many variations of these inverters as well that attempt to reduce the number and size of the auxiliary components and reduce circuit deficiencies [12] however, these also require modified switch modulation or add complexity. Included in this category is the bridge between the ARCP and ZVSCI topologies, the transformer assisted ARCP [13].

1.3.2 Topology selection discussion

A resonant transition inverter topology is chosen to best fit the application requirements. In references [14 15 16] and [17] comparative analysis is performed from a theoretical standpoint of the ARCP, ZCS 6-switch, ZCS 3-switch and ZVS 6-switch coupled inductor inverters for a 55kW adjustable speed drive (an application similar to the implementation in this thesis). Circuit schematics are shown in Figure 2 and Figure 3. The analysis legitimizes the selection of any one of these topologies for further

investigation. References [14,17] proceed to implement the ARCP and/or ZCS type inverters but do not provide strong argument against the implementation of the ZVS 6-switch coupled inductor inverter (ZVSCI).



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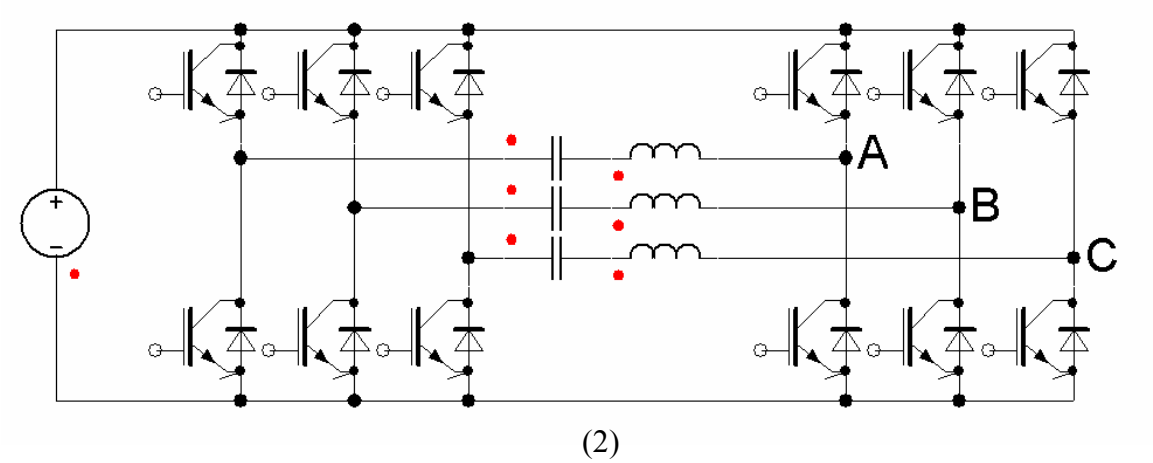

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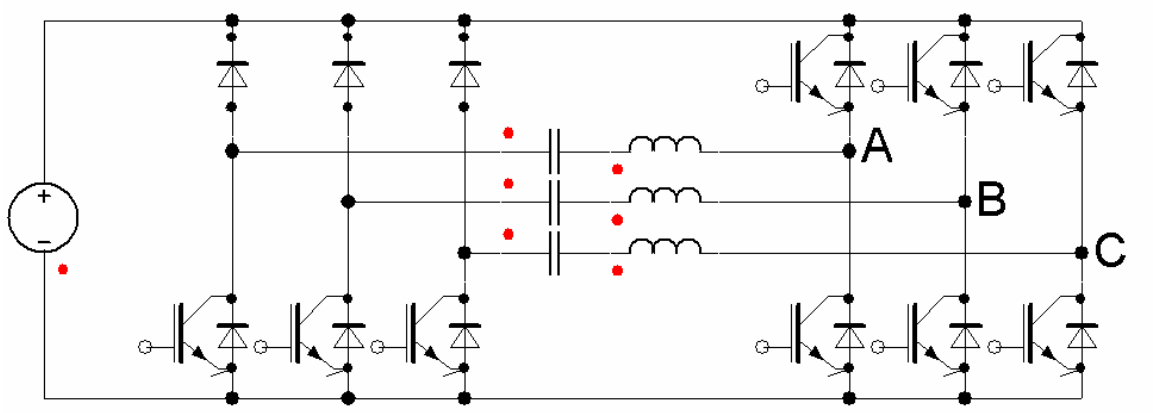

(3)

Figure 2 Some Resonant Transition Inverters (excluding the ZVSCI): (1) ARCP, (2) six switch ZCT, (3) three switch ZCT

Efficiency

Specifically, reference [14] provides theoretical computation showing the ZVSCI inverter efficiency to be lower than the ARCP inverter by .2 percent or less at 10-20kHz and on par with the other three inverter types; yet the ZVSCI is ruled out from implementation on the basis of the efficiency study. Reference [17] Gives evidence for the ZVSCI inverter efficiency to be higher than the ARCP inverter under all studied conditions and second in efficiency to the 6-switch ZCS inverter in two out of four tested switching frequency/load conditions. It is noted however, that the results of the implemented inverters do not show benefits in efficiency and in fact show that all of the soft switching inverters have lower efficiency than the hard switched counterpart (Note: the efficiency differences between topologies are all within the study margin of error). The study also emphasizes the importance of auxiliary device selection when designing for efficiency which will be a topic within this thesis.

Cost/Component Count

The ARCP has documented issues related to the usage of a DC mid-point that present significant design challenges and cost penalties. Capacitor balancing circuits, large capacitor banks and complex control adjustments [14,18,13] are required for good control of the mid-point related issues. The ZVSCI has the same component count as the ARCP, but without the midpoint balancing problem. Comparison of device stresses yields that the ARCP auxiliary switch and diode currents are twice that of the ZVSCI, but half the voltage [17]. In the voltage range of application semiconductor cost is more dependent on current carrying capability (i.e. die size and packaging) than voltage blocking capability making the ARCP is at a cost disadvantage to the ZVSCI. Individually noted, the transformer assisted ARCP topology addresses many problems with the ARCP topology [13] reducing the circuit deficiencies, but the ZVSCI achieves similar performance with reduced component count (2 less diodes per phase and simpler magnetic components). The ZVSCI has a higher auxiliary component count than the 6-switch ZCS inverter (6 and 3 additional diodes and resonant capacitors respectively), but the auxiliary diodes have to be rated at twice the current of the ZVSCI and the resonant capacitors must have an operating voltage that of twice the ZVSCI resonant capacitors.

The ZVSCI has a higher component count than the 3-switch ZCS topology requiring more auxiliary diodes, but the main switch, auxiliary diode and auxiliary switch currents are lower. The ZVSCI also requires more resonant capacitors, but are smaller capacitors and only require half the voltage rating of the ones required for use in the 3-switch ZCS. Though additional switches require additional driving circuitry, in general this device stress and cost analysis narrows the initially perceived high cost differential between the topologies to a smaller margin. Based on this analysis, a full commercial design needs to be performed to provide a definitive best solution; weighing the inherent circuit performance properties.

EMI

EMI reduction is a crucial performance aspect in general, but particularly in this application based on the proximity of the motor drive to EMI sensitive components even though the close proximity reduces the effect of cable di/dt. Soft switching can reduce EMI without the use of specialized PWM techniques [19]. Previous literature regarding the benefits of soft-switching on EMI performance is positive but inconclusive [15] [20] [21]. In general ZVS topologies are expected to give better EMI performance to ZCS topologies because EMI can not be directly controlled in ZCS topologies. The most benefit is expected in the high frequency EMI range, with little to no EMI decrease at low frequencies. The ARCP (a close relative of the ZVSCI) has been shown to have EMI advantages in experimental implementations. The ARCP benefits are limited by resonant branch diode reverse recovery ringing accentuated by high resonant currents (which can be controlled by good layout and control methodology). Thus, the ZVSCI is expected to achieve similar EMI performance benefits.

1.4 Thesis Objective and Overview

This thesis will demonstrate the viability of the fixed timing inductor coupled ZVS inverter by hardware construction, software implementation, testing and analysis. The simulation and design of this type of inverter has previously been described in detail in [18]. As such, special consideration and discussion is given to the auxiliary power device selection, gate driving, and testing. Further simulation is also presented to investigate the causes of non-ideal operation seen experimentally.

Chapter 2 - Describes the theory and principles of operation for the fixed timing inductor coupled ZVS inverter with discussion pertaining to prior art. Application specific design information is presented. Some known problematic issues with the topology are also discussed as well as possible solutions.

Chapter 3 - Explains the experimental hardware implementation of this drive system, including the power stage, gate-drivers, DSP coding, auxiliary device selection, pulse testing setup, pulse testing results and auxiliary switch "single shot" timing development. Based on the auxiliary device requirements, auxiliary device testing results and paper research, the issue of auxiliary device reliability is addressed.

Chapter 4 – Explains the open-loop phase leg test setup and illustrates preliminary testing performed with an inductor load and varied DC bus voltage. Soft-switching waveforms are compared to simulation. An efficiency comparison is made between the implemented soft switching inverter and the traditional and hard switching inverter. Some non ideal behavior is first noted related to distorted coupled inductor current.

Chapter 5 – Investigates the root causes of non-ideal circuit operation seen experimentally in the coupled inductor current. The characteristics are identified and a method is devised and carried out to further study the behavior through simulation; best practice recommendations are presented.

Chapter 6 - Presents the conclusions derived from the thesis, and describes ongoing work with the project and future research topics.

Chapter 2 - The Fixed Timing Coupled Inductor Inverter

2.1 Prior Art and Principles of Operation

The coupled inductor inverter achieves zero voltage switching through the addition of auxiliary switching devices, diodes, coupled inductors and resonant capacitors. The devices are arranged in a manner capable of being adapted to any standard six-switch, three phase inverter [Figure 3].

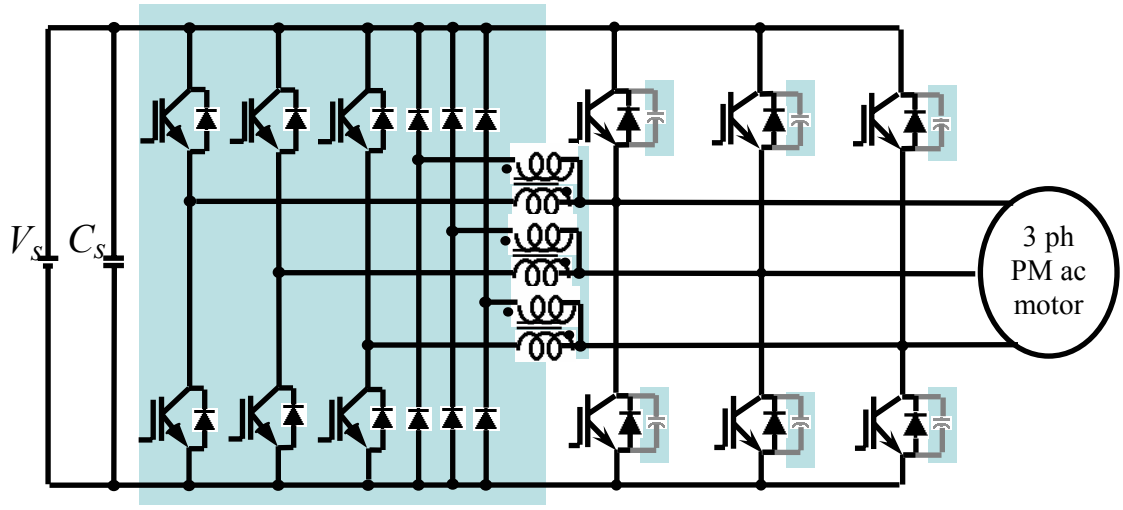

Figure 3 Three Phase Coupled Inductor Inverter Schematic

Generally speaking, reductions in EMI and improvements in efficiency over hard-switched inverters can be attributed to the zero voltage turn-on and capacitor snubber assisted turn-off of the main IGBTs. The initial concept for using coupled inductors in a soft-switching application was described for a boost converter in reference [22] and then further refined and adapted to inverter applications [23]. The first implementation was fixed timing based, but did not achieve full zero voltage turn on of the main switch and excessive currents are apparent in the auxiliary components during low load conditions. Variable timing control methods achieved zero voltage turn-on of the main switch and load adaptation, but added complex controls and sensors [24].

This implementation utilizes a non-unity turns ratio for the coupled inductor eliminating a period known as the "boost period" [18]. This enables a simple fixed timing control scheme to be implemented for both the commutation from switch to diode and diode to switch. Benefits of this implementation include reduced control complexity,

elimination of required current sensing and increased efficiency. Specifically, the increases in efficiency are due to a load adaptive behavior that reduces excessive currents in the auxiliary circuit (lowers conduction losses) and the operation of main and auxiliary switches under soft-switching conditions. Since the operation of each phase is independent, the simplified principles of operation can be described referring to the single phase leg circuit as shown in Figure 4.

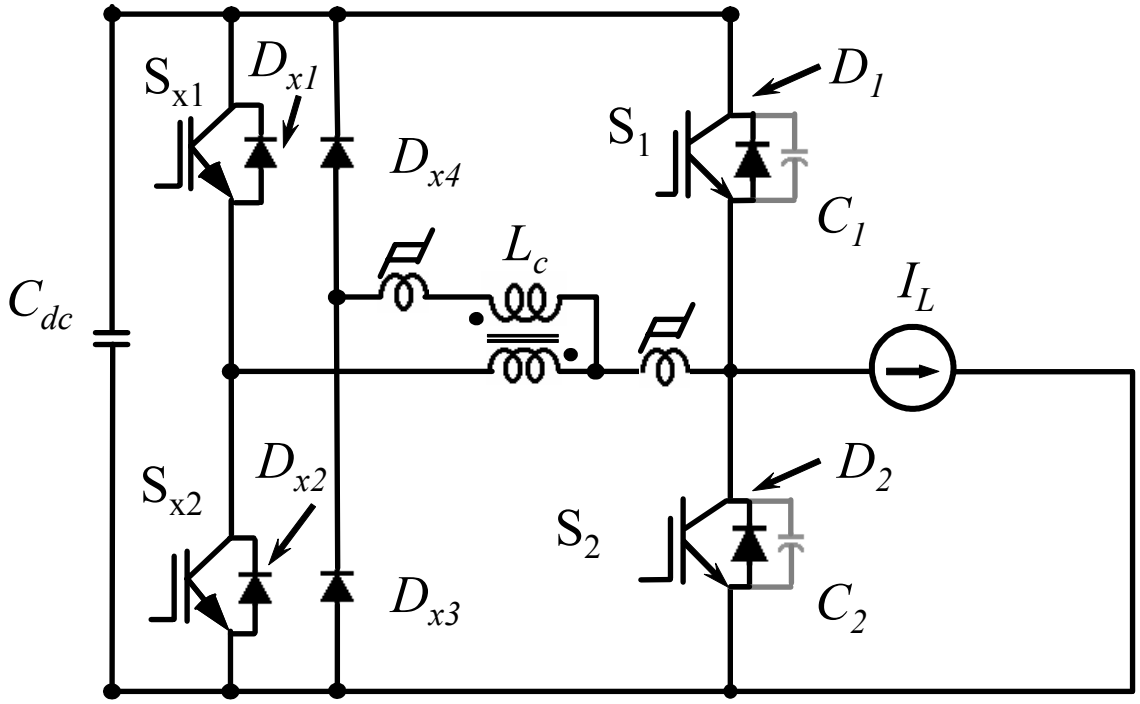

Figure 4 Single phase circuit of the coupled inductor inverter

Each phase leg consists of two main IGBTs, two auxiliary IGBTs, two auxiliary diodes, two resonant capacitors, one coupled inductor and two saturable inductors. The saturable inductors are added to each phase to reduce known freewheeling and residual magnetizing current issues that reduce efficiency and can cause EMI issues [20]. An alternative method for reducing freewheeling and residual magnetizing current uses two blocking diodes in series with the auxiliary switches to produce a similar result, but would undesirably restrict the auxiliary components to discrete packages. The use of blocking diodes also does not reset the residual magnetizing current [25]. Though both solutions undesirably add cost to the design, the saturable inductor implementation is chosen as less cost intensive and more effective. Simplified principles of operation for the

fixed timing inductor coupled inverter are described here for the commutation from D_2 to S_1 and the key waveforms are shown in Figure 5.

Operational steps for commutation from D2 to S1.

1. With the load current (I_L) flowing in the direction shown in Figure 4 (positive), D_2 is conducting the entire load current.
2. In preparation to turn on the main switch S_1, the auxiliary switch S_{x1}, is turned on. During this period, load current is flowing through a combination of D_2, and through the coupled inductor paths via D_{x3} and S_{x1}. The current through the coupled inductor windings increases linearly and the current through D_2 decreases at the same rate.
3. The coupled inductor windings now carry the entire load current. Due to a resonance between the leakage inductance (not shown) of the coupled inductor and the added resonant capacitors C_1 and C_2 the voltage across C_2 increases to the bus voltage and the voltage across C_1 decreases to zero. This zero voltage condition remains until the coupled inductor current decreases below the load current. D_1 is now conducting.
4. The voltage across the secondary winding is now V_{DC} and the coupled inductor current is decreasing. The voltage across S_1 is clamped to zero and S_1can be turned on under the zero voltage condition. Turn on of the main switch (S_1) allows an alternate source for the load current.
5. When the coupled inductor current decreases to the load current, the current through the main switch increases linearly to full load current and the coupled inductor current discharges at the same rate to zero.
6. The auxiliary switch S_{x1} now only caries the magnetizing current of the coupled inductor and is turned off under a near zero current condition when the main switch S_1 current equals the load current. The main switch S_1 continues to carry the load current until the end of the switching period.

The same process is used in the commutation from S_1 back to D_2.

The three key timing parameters are:

T_d: Dead time required for capacitor snubbed turn-off of complimentary switch

T_c: Delay time for main switch (after turn-on of auxiliary switch)

T_{aux}: Duration of auxiliary switch on-time

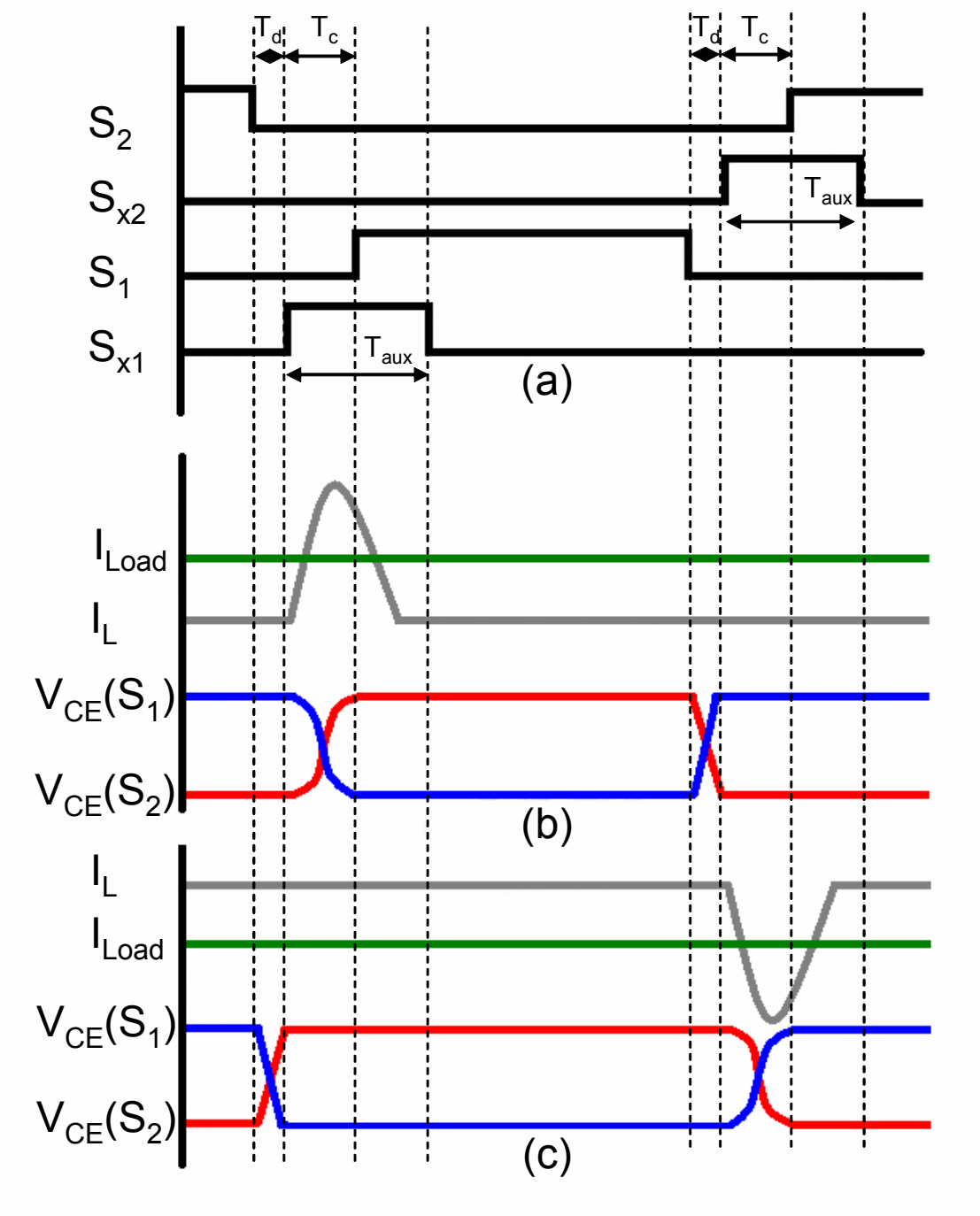

Figure 5 Key commutation waveforms for the implemented fixed timing control method (a) Gate Signals (b) Positive Load Current (c) Negative Load Current

2.2 Timing Parameter Calculations

The initial design is completed by following the fixed timing parameter selection procedure outlined in [18]:

1. Snubber capacitor is chosen at 0.14uF to significantly reduce turn off loss:
2. Resonant inductance Le selected to be .864uH to limit peak resonant current to around 300A: Lr1 is defined as the nominal resonant inductance.

$$Vdc = 640V; Ires\_p = 300A; C = 0.14uF$$
$$Zr = \sqrt{Lr1/2C}$$
$$Zr = Vdc / Ires\_p = 1.76$$
$$Lr1 = Zr^2 \times 2C = 1.27uH(selected\_1.2uH)$$
$$Le = Lr1 \times 2 \times (n \div (n+1))^2 = .864uH$$

3. Turns ratio is selected as 1.5:

$$Ip = 300A$$
$$\sqrt{n^2 - 1} \geq Ip \div Ires\_p$$
$$n = 1.5$$

4. Tc (main switch delay time) determined to be approximately 1.2us:

$$Tr = 2\pi\sqrt{Le \times 2C}$$
$$\omega_{rn} = (1+n)/n \times 2\pi / Tr = 3.389$$
$$Tres = \arccos in(-1/n)/\omega_{rn} = .679us$$
$$T1,0Max = (2 \times n/(1+n))(Le \times Ip / Vdc) = .468us$$
$$Tc = T1,0Max + Tres = 1.165us$$

5. Taux (auxiliary switch on time gating) determined to be greater than 1.9us:

$$T_{5,2\_max} = (n^2/(1+n)) \times Le \times (Ip + Ires\_p \times \sqrt{(n^2-1)}/n)/Vdc = .7us$$
$$Taux \geq T_{5,2\_max} + Tc = 1.9us$$

6. Td (dead time) to allow snubbered turn off of complementary switch and low load adaptability determined to be approximately 1.8us (Ispec chosen to be 100A):

$$Td = 2 \times C \times Vdc \div Ispec = 1.8\text{us}$$

Chapter 3 - Hardware & Software Design and Implementation

3.1 Various Implemented Hardware

This section describes various hardware implemented not discussed in other parts of this chapter. These particular components characteristics and circuit functions are described with relevance to simulation results. Though they are significant in their contributions to the project, the amount of new work done in these areas for this project is limited.

3.1.1 Gate Drives & Optical Interface Board

The gate drive board has integrated isolated power supplies for driving the IGBTs. The gate signals were controlled using the MC33153 gate drive chip with integrated de-saturation protection which drives the IGBT off if a de-saturation condition is sensed. De-saturation detection and device auto turn off is a common form of IGBT short-circuit protection, with more advance versions being developed [26]. The de-saturation trip point on the MC33153 is tunable to a particular IGBT and current level by varying a resistor in series with a high voltage clamp diode that feeds back to the de-saturation pin of the MC33153. During pulse testing, the gate drive for the auxiliary switch is modified by bypassing the resistor to maximize the allowable V_{CE} de-saturation protection set point. This is necessary for the proper characterization and selection of the auxiliary IGBT and described further in section 3.2.

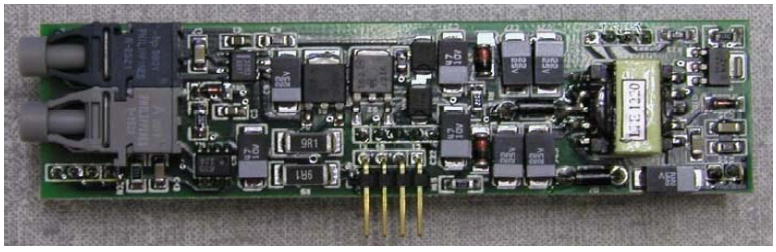

Figure 6 Optical Gate Driver

The gate driver boards are sent gate signals via an optical interface board. Gate drive generated fault signals are also sent back to the DSP through the optical interface board. The optical board Figure 7 Optical Interface Board [Figure 7] receives gate signals from the DSP generated at the 5V level.

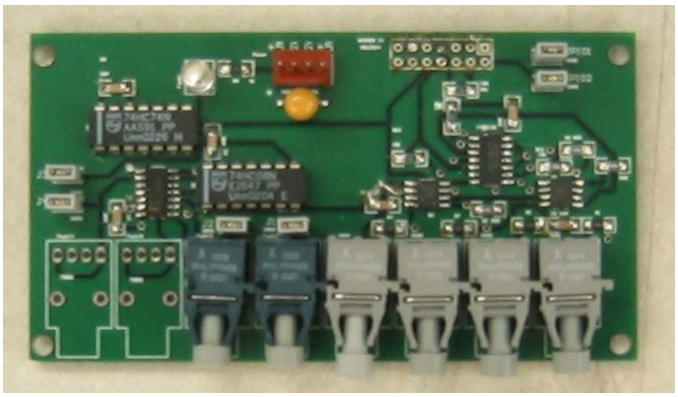

Figure 7 Optical Interface Board

In the final version, the gate driver is modified to operate on 15V CMOS logic using Agilent opto-couplers of the HCPL-0630 type. This is required for integration with the final application's existing controller to meet the design drop in criterion.

3.1.2 Auxiliary Diodes

The auxiliary diodes have few design requirements. They need to have larger voltage drop than the main diode to reduce circulation currents and they also need to be very fast with good reverse recovery characteristics. To minimize space and component count the IXYS VUE 130-12N07 6-pack diode module rated at 130A continuous with a 40ns reverse recovery time is selected. They work properly without incident in the implementation. A high peak current rating of a diode is very typical because of widespread use in 50 and 60 Hz applications. The particular selected diode has a forward current rating of 500A for a duration of 10ms which is adequate for the implemented ICZVT inverter. Since the diode is not a major cost item, no detailed analysis is performed to attempt to reduce the diode ratings. From simulations, the auxiliary diode peak and rms current ratings need to be at least 250A and 23A respectively.

3.1.3 Main IGBT

The main IGBT used is the Eupec FF400R12KE3, rated at 1200V and an I_C of 580A @ 25C. This device exhibits low conduction and switching losses and is capable of 5 kHz+ operation. The device is designed for traditional hard switching applications. Since the ICZVT almost completely eliminates switching losses, the packaging of the selected device is more substantial and costly than necessary. In a design for complete cost reduction, a device with packaging capable of dissipating the RMS conduction losses only is necessary. From simulations, the main switch peak and rms current ratings need to be at least 320A and 108A respectively.

3.1.4 DC Bus Capacitors

The main DC bus capacitors used are a parallel series combination of 8000uF capacitors. There are two 8000uF capacitors in parallel and two in series with the neutral point in the middle. These capacitors are connected to the main power stage via a low inductance/high current bus bar. Additionally, some 1uF, 1200V, Electronic Concepts "Lo Henry 88 Series" capacitors are used across the DC bus as snubber capacitors. Their low equivalent series inductance and equivalent series resistance design makes them suitable for this application.

3.1.5 Resonant Capacitor

The resonant capacitors are 1000V, 0.14uF, SBE 716P series polypropylene capacitors. This type of capacitor is needed due to the high current, low equivalent series resistance requirements of the ICZVT inverter. The resonant capacitor size is determined based on previous project work and device switching test results to give an optimal soft device turn off with minimal voltage overshoot.

3.1.6 Coupled Inductor and Saturable Inductor

The coupled inductor value is optimized to match the load to give the optimal inductor wave shape and soft-switching performance. The original coupled inductor value has an inductance of 1.2uH. After some testing, the inductance is changed to 1.6uH

to help mitigate the direction of the negative current pulses. Additionally, the saturable inductor used to prevent circulation current is designed with two cores and various turns ratios. Three turns is the most common saturable inductor design tested. After several iterations and performance tests, the final design uses four saturable cores with two turns each.

3.2 Auxiliary IGBT Selection Methodology

3.2.1 Auxiliary IGBT Selection Foreword

For reasons of overall system cost it makes sense to attempt to find auxiliary IGBTs that will yield the lowest appreciable cost to the system but still match system goals for performance, cost and reliability. As switching characteristics, the device must have fast enough turn on and turn off characteristics to quickly turn on and off as to conduct the required auxiliary current through the coupled inductor for a short amount of time. Modern IGBTs are capable of turning on and off in this short period of time and have no problem operating at the 5 kHz inverter frequency. Since the auxiliary IGBT turns on under zero current and turns off under zero voltage conditions, the switching energy calculations are not of great importance either. Hence, for IGBT selection the switching characteristics are largely neglected.

The current carrying capabilities are the area of primary concern. IGBT cost is directly proportional to die area/current carrying capability and also highly dependent on packaging. In the ICZVT inverter, the auxiliary IGBTs conduct current for only a few microseconds resulting in a low RMS current carrying requirement, but have a high repetitive peak current requirement. From simulations, the auxiliary switch peak and rms current requirements are 280A and 43A respectively. Most IGBT datasheets describe device current carrying capabilities in terms of continuous collector current (I_C), and some define a peak repetitive collector current (I_{CM} or I_{RCM}) at a duration on the level of milliseconds at a given junction temperature. However, the auxiliary switching device in the ICZVT is not being operated anywhere near continuously, and conduction time is three orders of magnitude shorter than the typical datasheet I_{CM} rating. The datasheet current ratings are therefore inadequate for determining which IGBT will be right for the

application. More information must be extrapolated from datasheet curves, and/or the IGBT must be tested to determine a suitable device.

3.2.2 Design for Reliability

To correctly select the auxiliary IGBTs for the system, the IGBT must be understood on a more fundamental level. There are two failure mechanisms of IGBT dies, over-voltage (avalanche energy breakdown) and over-current. There are additionally primary and secondary combinations of the two failures such as avalanche induced second breakdown limit (AISBL) and circuit oscillations [27] that can lead to device failure. In this application the 640V DC bus is very stiff and a device rating of 1200V prevents any voltage spikes from exceeding the device SOA. The device is operated within the SOA even under short circuit conditions so the avalanche characteristics/over voltage failure mechanisms of the IGBT are not considered. Of more importance is the high temperature behavior and over-current failure.

An over-current failure is actually an over-temperature failure caused by excessive conduction or de-saturation region power losses that the device packaging and external thermal system are unable to remove resulting in excessive increased heating of the device silicon. Once an IGBT's junction temperature exceeds a limit defined by the manufacturer (a property of the die) the silicon may fail. This failure may not be immediate evident to the end user if the over-temperature condition is only seen for a short period of time and does not cause thermal runaway. Only measuring the case temperature to determine junction temperature is not a totally adequate technique to determine reliability. Additionally, though not failures seen early in the IGBT life, failures due to IGBT packaging such as, coefficients of thermal expansion and solder fatigue will limit lifetime and must be considered to ensure long IGBT life. Further analysis is required for robust design.

3.2.3 Transient Thermal Impedance and V_{CE}

One IGBT characteristic investigated is the transient thermal impedance (Z_{thJC}). This is the ability of the packaging material to absorb and transfer energy away from the die to the case in a short period of time. Z_{thJC} is defined in terms of degrees K temperature rise seen per watt of power loss at the junction (K/W) and is defined on some datasheets

for a given duty cycle (D) (square wave pulse) and pulse duration down to the microsecond level. This time duration is much closer to the conduction time of the auxiliary IGBT in the ICZVT inverter than the I_C or I_{CM} datasheet ratings enabling a better look into how to utilize the die size more effectively and optimize cost without sacrificing reliability by exceeding device peak junction temperature. An example transient thermal impedance chart is shown in Figure 8.

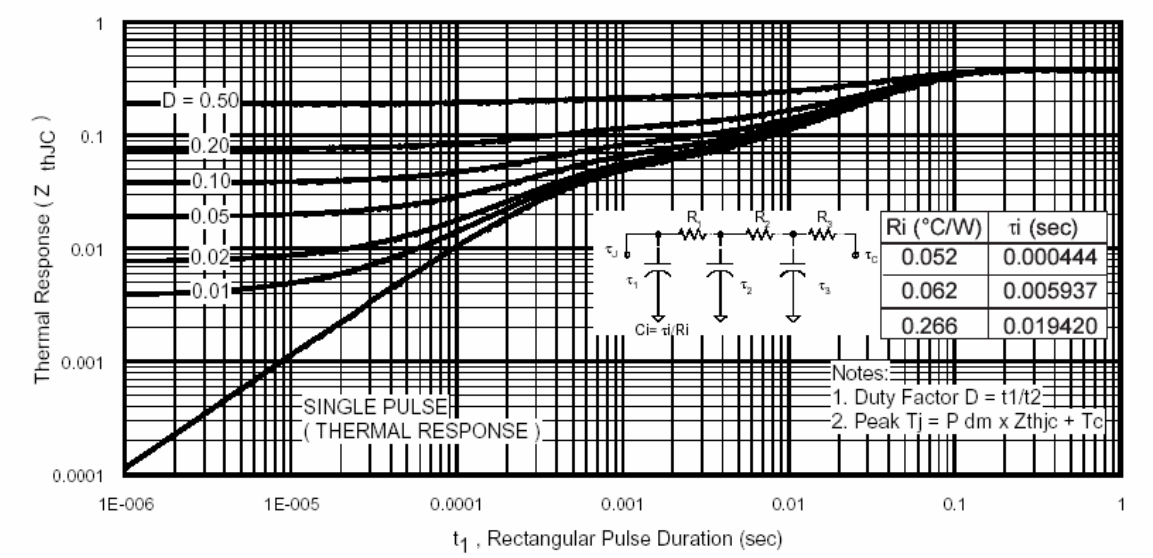

Figure 8 IRF GB50XF150K IGBT Datasheet Transient Thermal Impedance (Normalized)

For simplicity, the current waveform through the auxiliary device is viewed as a rectangular pulse, even though it is actually parabolic in nature. Additionally, all the devices prospective IGBTs have a peak recommended junction temperature of 150C. The governing equation defining peak junction temperature is a function of the transient thermal impedance (junction to case), the initial case temperature, and power dissipated at the junction (P_{DM}). For inverter operation P_{DM} is equal to IGBT V_{CE} multiplied by I_C; the governing equation is:

$$IGBT\_Peak\_Tj = I_C \times V_{CE} \times Zth_{JC} + T_C$$

Equation 1 IGBT Junction Temperature

In the turbo-compressor application, the inverter heat sink is cooled using a liquid refrigerant and maintained very cold (sub zero C). In the lab, this cooling equipment is not available for use in testing the inverter, so the auxiliary devices selection calculations

are performed with higher heat sink/IGBT case temperature of 50C to prevent failure of the inverter during the preliminary testing phases when the ICZVT inverter is operated on an air cooled heat sink at room temperature. Combined with the known operating condition of I_C = 300A, the undetermined IGBT characteristic is V_{CE}.

For most devices, the V_{CE} is not characterized on the datasheet for I_C values far in excess of the continuous current rating due to the fact that operation of this type is not a common procedure. It is therefore necessary to extrapolate the information from the datasheets. Information can be extrapolated graphically by drawing lines on the output characteristic plots assuming a linear change of V_{CE} with increasing I_C and that the device will not enter de-saturation.

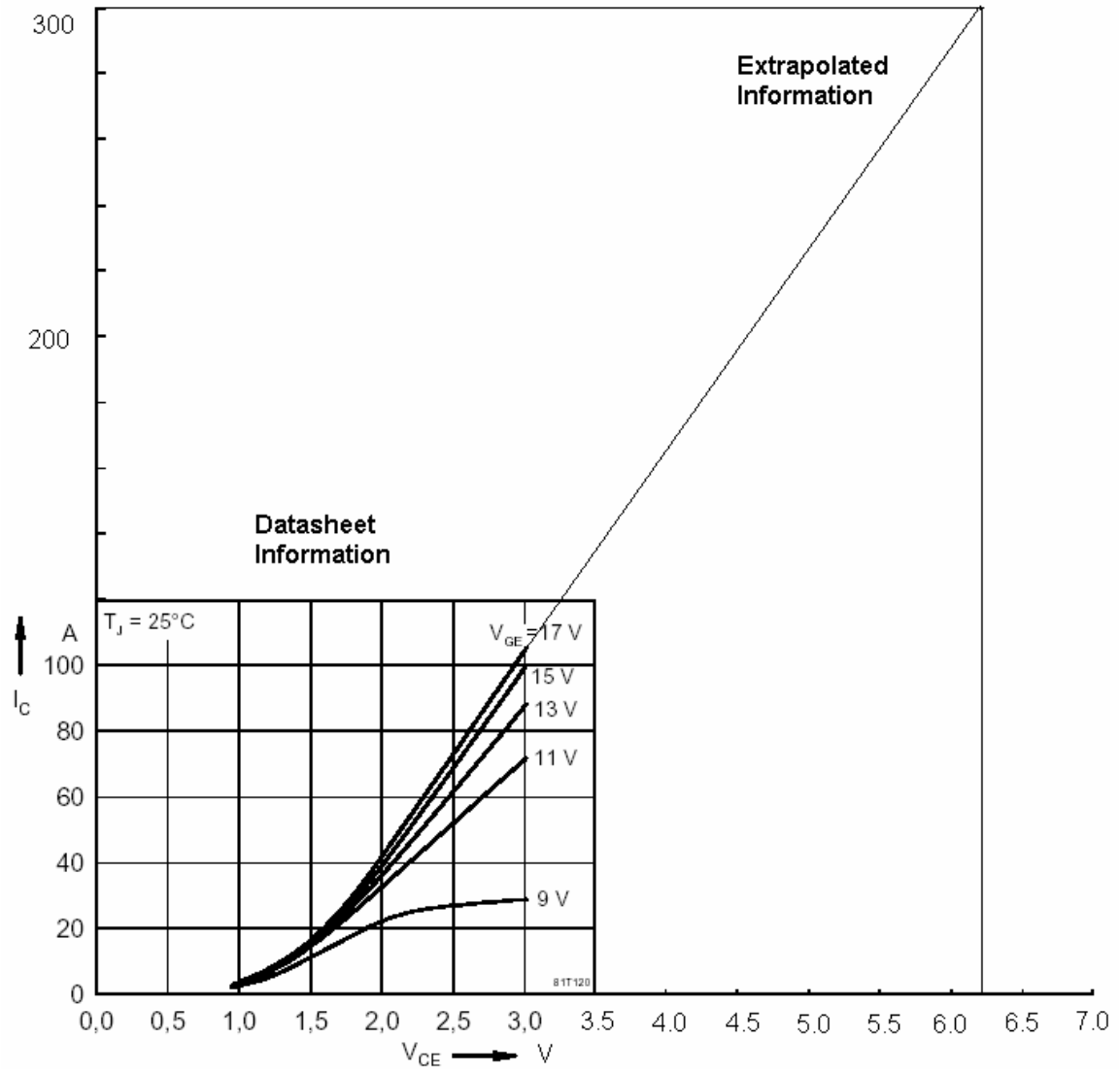

Figure 9 IXYS VII 75-12P1 300A V_{CE} Extrapolation (non de-saturation assumed)

This information can also be roughly calculated using device output characteristic equations if available. However, it is not common to find complete equations that vary with junction temperature, gate-emitter voltage, collector current, et cetera on datasheets. It requires a significant amount of work for semiconductor manufacturers to perform and verify this full equation based characterization on an ad-hoc basis. In lieu of full characterized equations, the extrapolation technique is used on the auxiliary device prospects with results shown in Table 1.

Table 1 Comparison of Auxiliary IGBT prospects at 300A current carrying condition

Manuf.	Device (1200V)	$I_{C\ rated}$	V_{CE}* 25C	V_{CE}* 125C	Package	Devices Packaged
IXYS	IXEN 60N120	100A	4V **	5.2V**	SOT 227-B	Discrete
IXYS	MWI 100-12 E8	165A	N/A ***	N/A ***	EcoPac	6-Pack
IXYS	VII 75-12P1	92A	6.2V **	7.3V **	EcoPac	Half Bridge
EUPEC	FS75R12KE3G	75A	3.8V **	5.2V **	EcoPac	6-Pack
EUPEC	FS100R12KE3	100A	3.1V **	4.1V **	EcoPac	6-Pack
EUPEC	FS150R12KE3	150A	2.4V	3.1V	EcoPac	6-Pack
IRF	IRGPS60B120KD	60A	6.6V **	7.9V **	Super TO-247	Discrete
IRF	GB50XF120K	50A	6.2V **	8.1V **	Econo2	6-pack

* V_{GE} applied for the characterization varies between manufacturer and datasheet 15-18V

** Information extrapolated from datasheet curves

*** Not enough information on datasheet to extrapolate

Unfortunately, there is a wide range of different test conditions between devices and manufacturers as well as an inconsistent breadth of information presented on various datasheets preventing accurate comparison. Further datasheet extrapolation can be done in an attempt to normalize the comparison with a V_{GE} of 17V (the gate driving voltage used in implementation), but is not deemed necessary given that the goal of the initial datasheet extrapolation is only for preliminary device selection.

3.2.4 Analysis of Theoretical and Extrapolated IGBT Information

The two IRF devices, rated at 50A and 60A exhibit the highest V_{CE}s and coincidentally, their datasheets are the only datasheets that provide Zth_{JC} for a range of duty cycles instead of only the single pulse thermal response characteristic. To allow greater flexibility for auxiliary device timing/control tuning and coupled inductor design, a pulse time of up to 4us is desired. This results in the duty cycles of interest being .02 for a 5 kHz operating frequency. From Figure 8, at the point of interest, the GB50XF120K has a Zth_{JC} of approximately .008 K/W. At the point of interest, the IRGPS60B120KD is extrapolated to have a Zth_{JC} of approximately .02 K/W. Using Equation 1, the maximum V_{CE} values that allow the junction temperatures to remain below 150C are 41.67V (GB50XF120K) and 16.67V (IRGPS60B120KD). These values are both above the highest extrapolated V_{CE} values that the IGBTs are expected to exhibit in inverter application 7.9V and 8.1V respectively. This means that either device is suitable for the application on a pure transient impedance calculation. Even though the IRGPS60B120KD is rated 10A higher than GB50XF120K with a lower max V_{CE} characteristic, the packaging of the GB50XF120K 6-pack is superior to the discrete Super TO-247 resulting in better thermal performance and lower effective device junction temperature. This shows that in general, the best device for the application will have the lowest (V_{CE} x Zth_{JC}) value for the lowest price that fits in the required physical footprint and satisfies the 150C peak junction temperature requirement.

Not all IGBT datasheets define Zth_{JC} for a range of duty cycles and instead only focus on the single pulse thermal response characteristic. From analysis of several datasheets with duty cycle and single pulse information, no conclusive trend can be drawn quantitatively relating single pulse Zth_{JC} to duty cycle based Zth_{JC} values. The one piece of useful information gathered is that most multiple IGBT dies packaged together exhibit a lower overall Zth_{JC} value. This becomes increasingly important if the inverter frequency is desired to be increased to above audible range (i.e. 20 kHz). With increased inverter frequency, the switching period decreases and increases the duty cycle of the auxiliary switch leading to an increased Zth_{JC} as can be seen in Figure 8.

As a secondary point of analysis, the average power dissipation capabilities of the IGBT packages are examined at the maximum extrapolated V_{CE} values for T_J <150 in [Table 2] Auxiliary IGBT current is represented as a 300A square wave pulse D = 0.02.

Table 2 Average Power Dissipation and Thermal Resistance Requirements

	GB50XF120K	IRGPS60B120KD
Pd instantaneous	2,370 W @ V_{CE} 7.9V	2,430 W @ V_{CE} 8.1V
Pd average	47.4W	48.6 W
Max T_j Rise above heat sink	150C – 50C = 100C	150C – 50C = 100C
Max R_{th} Junction to heat sink	2.11 deg C/W	2.06 deg C/W

The average power dissipation capabilities of the packaging are not exceeded with any reasonable case to heat sink thermal medium.

3.2.5 Pulse Testing

To obtain V_{CE} values in a previous section, two assumptions are made: a linear change of V_{CE} with increasing I_C and that the device will not enter de-saturation at high current levels. To verify that these assumptions are correct, pulse testing is performed. The prospective IGBTs are subjected to 300A current pulses and the device V_{CE} is observed. If the observed device V_{CE} is higher than expected for a given current, the device is no longer operating with a linear change of V_{CE} with increasing I_C and nearing de-saturation. The non-linear increase of V_{CE} is illustrative of the device nearing entering the de-saturation region. If an excessive increase in V_{CE} or the inability to carry 300A is seen, the device has entered de-saturation. Either of these conditions is non-ideal and represents an exponential increase V_{CE} with increasing current after reaching the divergence point on the output transfer characteristic curve. The exponential increase in V_{CE} leads to an exponential increase of conduction losses. This is illustrated in Figure 10 with an applied V_{GE} of 9V as an example case.

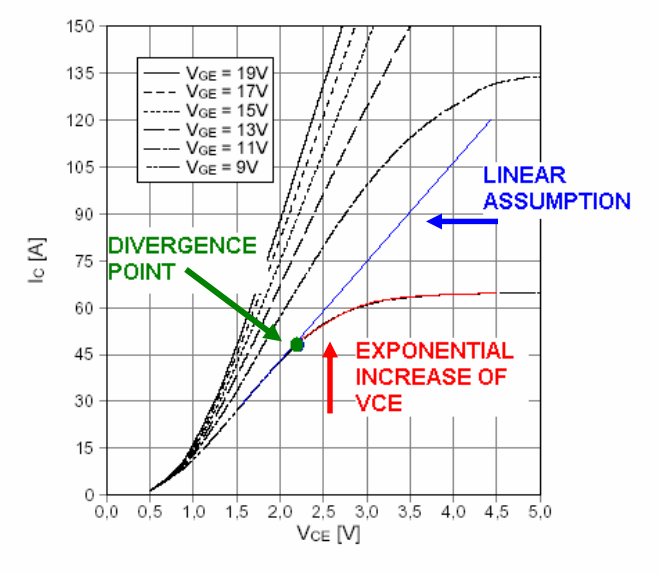

Figure 10 IGBT Non-Linear Point EUPEC FS75R12KE3G

The IGBT will exhibit similar characteristics at higher currents with a higher applied V_{GE}. If V_{CE} values are measured slightly in excess of the 125C predicted value, the device may not be entering de-saturation, but the actual junction temperature is likely above 125C. Thus, the extrapolated 125C junction temperature V_{CE} values are used as rough evaluation points to determine device de-saturation or an operating temperature greater than 125C. For the devices whose datasheet characteristics were extrapolated at a V_{GE} not equal to 17V, there will naturally be an acceptable difference in V_{CE} seen in the actual pulse testing from the estimated V_{CE}.

The pulse testing setup is designed only to determine the saturation voltage of the IGBT at a 300A condition. The current is ramped up using an external 275uH inductor as a load and the pulse rise time and duration is not representative of the actual duty cycle the IGBT will see in the inverter application. The timing is controlled by the use of an external pulse testing timing box that contains circuitry that will output fiber optic signals at a rate determined by front panel user inputs. The pulsing is repeated at long time intervals of a second or greater to allow the device packaging to transfer some of the heat out to the mounted heat sink, but still allow repeatable V_{CE} observation. Optimally, this procedure would be performed on the final heat sink and cooling assembly under-soft switching conditions and at the application switching frequency.

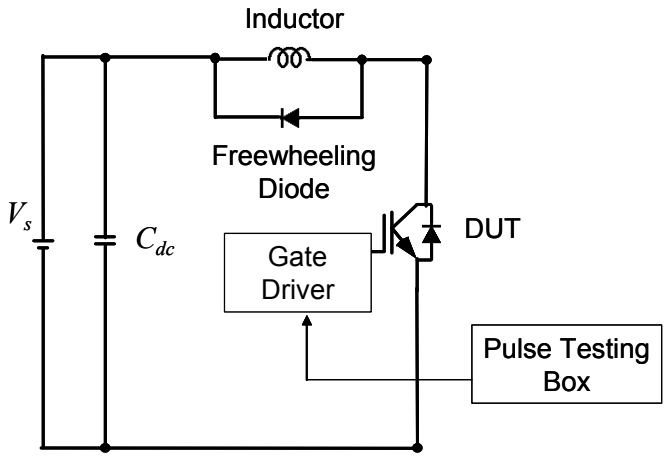

Figure 11 Pulse Testing Setup

Extending the pulse duration beyond the 1-4us inverter application time to slowly ramp up the IGBT current through the external inductor allows the gate drive voltage to stabilize and avoids noise interference caused by high parasitic inductance related di/dt that would be result in Vce monitoring inaccuracy if the IGBT was switched on for only a few microseconds [14]. Thus, it can be accurately observed as to whether or not the device is entering de-saturation. This procedure was performed on all of the candidate devices available at the time of testing.

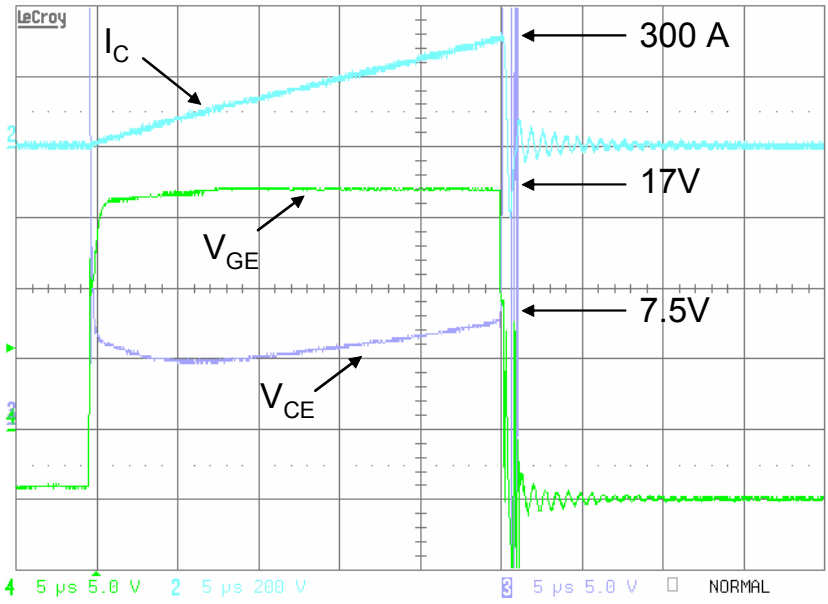

Figure 12 Pulse Testing of the IXYS VII 75-12P1 (92A device)

In the case of the 92A IXYS VII 75-12P1 device, the device is pulsed on for 25us allowing the current to increase through the device from zero to 300A. The maximum V_{CE} seen is 7.5V which is very close to the linearly extrapolated 125C result of 7.3V with an applied V_{GE} of 17V and linear behavior of the collector current (I_c). Thus, the 92A device does not enter de-saturation, even at the 300A condition. Nor has the device seem to have even reached the divergence point, so there are no associated exponential losses and best device efficiency is maintained. Even the IRF 60A IRGPS60B120KD does not stray more than .2V from the linearly extrapolated predictions. It is suspected that the actual junction temperatures are in the range of 120-130C because of the close correlation of pulse tested V_{CE} values to the datasheet interpreted 125C junction temperature V_{CE} values. Note that these junction temperatures may be artificially inflated because the overall conduction power loss is greater than will be experienced in the inverter application due to the extended pulse time of 25us. As a result, they should all have adequate die characteristics.

Based on these promising results, an attempt was made to stress the smaller devices until they entered de-saturation to determine the actual maximum current carrying capability. The attempts led to the gate drive circuitry pre-maturely indicating de-saturation faults. The de-saturation voltage threshold was already modified for a maximum of approximately 9V V_{CE} (I_C limitation) for the 300A pulse testing. Re-design of the gate drive circuitry for the express purpose of determining device failure limits is forgone.

3.2.6 Remarks on Final IGBT selection and Reliability

It has been shown that any of the candidate IGBTs in Table 1 should be adequate for functional implementation in the ICZVTI. Further testing is proposed for devices that were unavailable at the time of testing (IRF IRGPS60B120KD, Eupec FS75R12KE3G and FS100R12KE3) though it is hypothesized based on the results of tested IGBTs that they will all be sufficient for the application. Additionally, it is proposed to test devices with current ratings below the 50A level and it is suspected that suitable devices will still be found at these low current levels. Though the packaging is shown to be important for transient thermal reasons (more so at high switching frequencies), high power dissipation

capability of the packaging is not an important characteristic since the average power dissipated by the auxiliary IGBTs is low. Notwithstanding functional testing, there are several key issues related to using an off the shelf low current IGBT which are related to device packaging. Though it is shown from pulse testing that the silicon die can handle this type of high current operation for some time, the long term reliability is in question. Even if average case temperatures are within limits, repetitive local overheating can lead to premature device failure [28] [29] [30] [31] [32].

- Wire bond lift off – This is a primary and well known failure mechanism in IGBTs due to inconsistencies in wire bonding pressure and temperature during manufacturing as well as mechanical tension stresses during power cycling.
- Die attach & solder fatigue – Variances between device component coefficients of thermal expansion cause expansion and contraction in applications with high peak temperatures and low minimum temperatures.
- Electromigration induced wire failure – The mean time to failure for an IGBT related to electromigration effects is directly proportional to the current density in the wire bonds as defined by Black's equation. In this inverter, the currents carried by the wires are far in excess of the manufacturer designed values.
- Local overheating inducted burnout – The temperature distribution on an IGBT die is highly non uniform. Even if the average case temperature is within specifications, very high localized temperatures may still exist that can cause premature failure.
- Overall power cycling limitations – combining the above failure modes, the number of times the device can be power cycled is limited and can cause the device to fail earlier than the rest of the inverter.

If small auxiliary devices are used in the ZVSCI implementation, any manufacturing defects in the IGBT devices will be more quickly apparent due to the high degree which the devices are stressed compared to traditional applications. It is also noted that although all the tested devices are capable of conducting the required current, the devices with higher V_{CE} values will adversely affect overall efficiency. The goal of high efficiency combined with physical area packaging constraints [Figure 13] and reliability questions leads to the final selection of the 150A Eupec FS150R12KE3 or the 165A IXYS MWI

100-12 E8 (no datasheet comparison available) 6-pack modules. This Eupec six pack module will fit in the prescribed area, give high efficiency and perform reliably due it's 150A rating (and associated packaging) and single direct copper bond (DCB) to aid in heat spreading .The IXYS MWI 100-12 E8 is a special case; although tested, there are no output characteristic curves on the datasheet and no conclusion can be drawn about whether or not the device is in de-saturation or over-temperature. If the primary design drivers for implementing a soft switching inverter are EMI reduction and low cost, any device that meets the aforementioned selection methodology is suitable. Smaller devices can be used and run in deep de-saturation if desired, but will suffer in efficiency due to excessive power loss and reliability due to a large internal temperature gradient and high local temperatures of operating in the de-saturation region (short circuit like response is seen). The FS150R12KE3 auxiliary IGBT 6-pack used in the final implementation is shown in the final layout in [Figure 14].

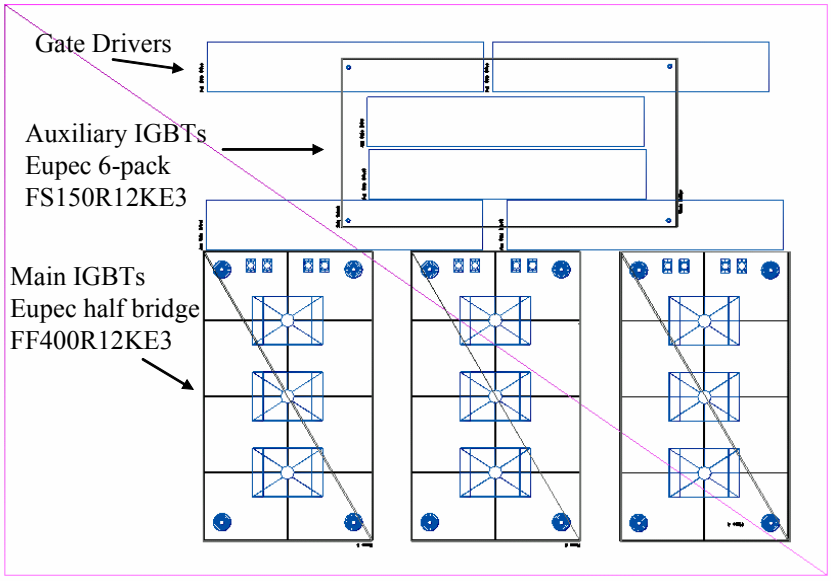

Figure 13 Proposed three-phase power device and driver layout

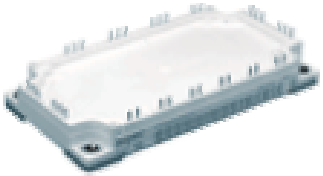

Figure 14 Eupec 6-pack module

3.3 Auxiliary IGBT "Single Shot" Testing

"Single Shot" timing development involves the testing of the auxiliary and main power device together along with the resonant tank components observing only one switching period. Though the end inverter is a fixed timing inverter, during development the ability to modify the timing quickly is needed to select the final fixed timing value as different system parameters are changed. This enables the development of a robust design capable of maintaining soft-switching under all load conditions and a wide range of bus voltage variations. The Analog Devices ADMC401 motor controller DSP is used as the foundation of the timing development. The DSP is coded using internal counters and digital outputs to send signals via a fiber-optic transmitter board to fiber optic gate drivers that drive one main power device and complimentary auxiliary power device with a software variable delay between the two pulses.

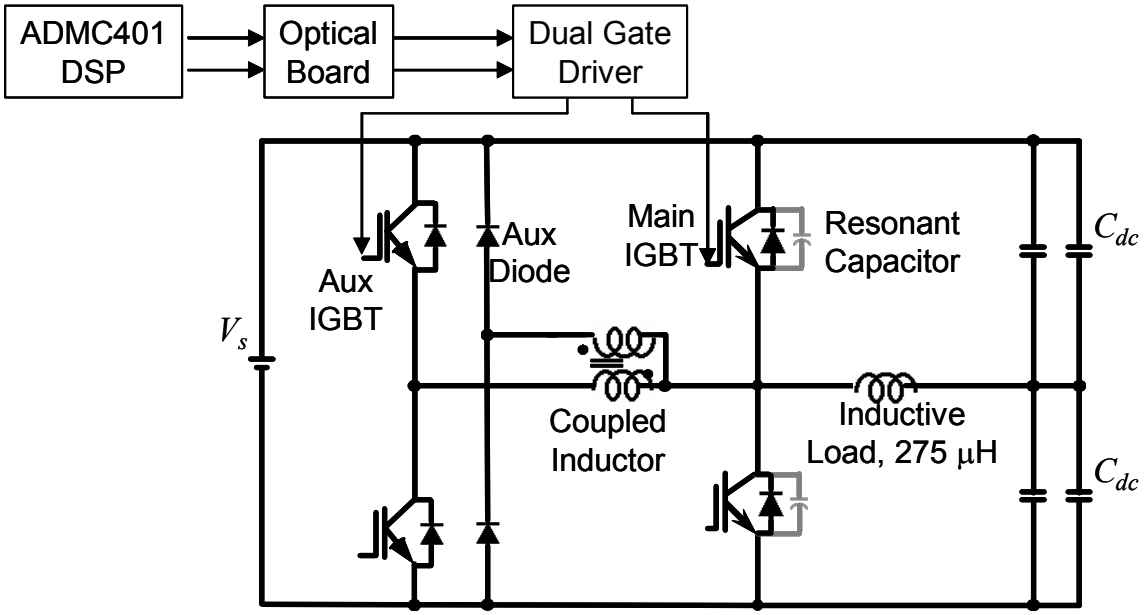

Figure 15 "Single Shot" Test Setup

This phase of testing involved using two oscilloscopes observing DSP timing signals, load current, device/bus voltages and the main power device gate drive voltages simultaneously. Using all these together soft-switching/non-soft switching conditions can be observed and the timing modified concurrently. There are two distinct sets of pulses. The first set of pulses is intended to ramp up the load current to a pre-determined condition and the second set of pulses ramps up the load current to the desired operating

condition of observation. Using this test setup, a variety of turn on and turn off conditions can be observed for soft switching by varying the device on times (and bus voltage if desired).

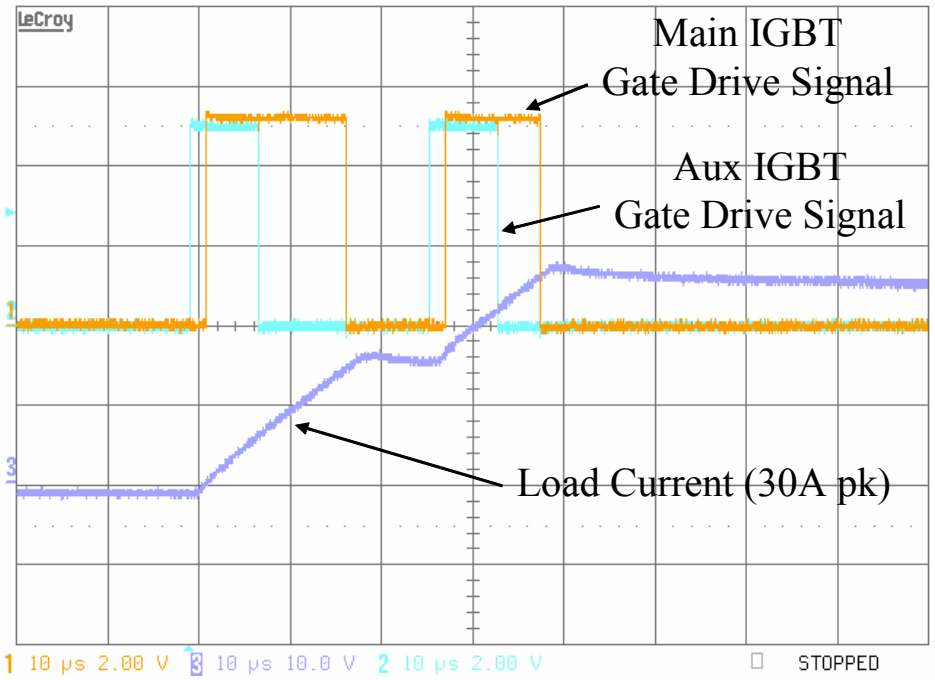

Figure 16 "Single Shot" Testing Signals (scope 1)

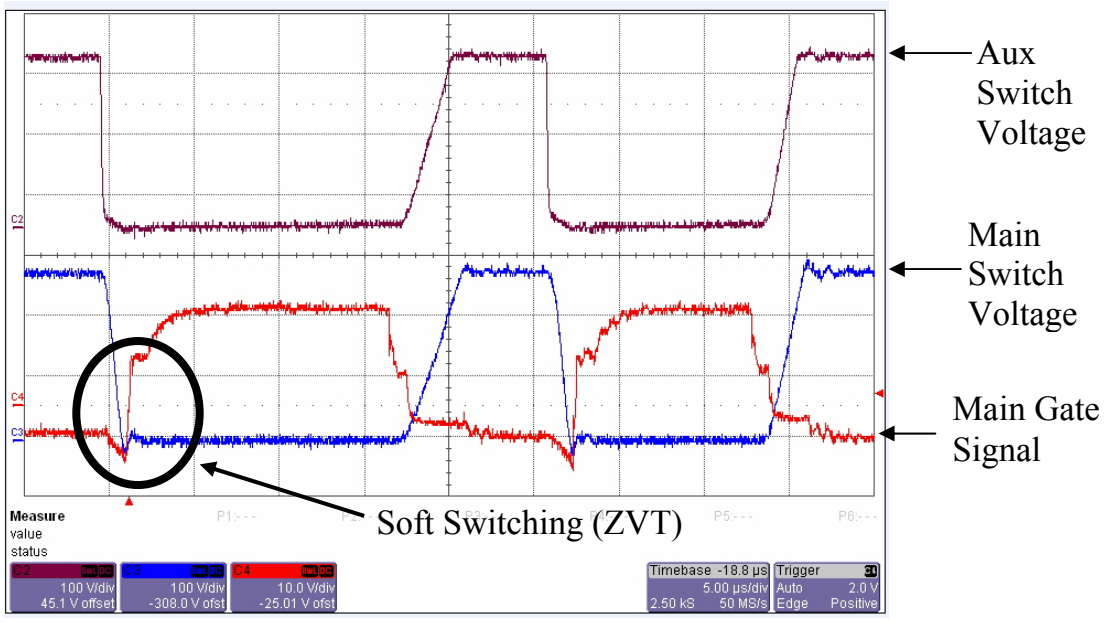

Figure 17 "Single Shot" Testing Signals (scope 2)

From a number of trial and error tests with two different coupled inductor designs, it is determined that a decent starting place for load/bus adaptation a 1-2 us main switch delay. The auxiliary switch duration is not a crucial parameter since after the main switch turns on, the auxiliary current will be conducting zero current. However it must be given enough on-time to account for the longest inductor discharge period. It then needs to be turned off at least a few microseconds before the main device turn off. Auxiliary switch duration of 6us is used in the initial implementation. These timing parameters are consistent with the theoretical timing calculations described in section 2.2 Timing Parameter Calculations.

Chapter 4 - Single Phase Test Setup and Results

4.1 Single Phase Test Setup

The single phase test setup is similar to the "Single Shot" test setup described in Figure 15 of section 3.3. A suitable high voltage power supply is not available in the lab capable of more than pulse and single shot testing, so a rudimentary high voltage DC power supply is designed. A three phase AC power supply was used as the main power source and a voltage trippler was designed and coupled to the three phase output to achieve the needed 600V bus voltage. A large DC bus cap bank is also incorporated to create a very stiff DC bus. The only other notable differences are: the two main devices and two auxiliary devices are driven, two saturable inductors are included, and fixed timing circuitry is implemented. A photo of the power stage of the test setup is shown in Figure 18. The ADMC401 is coded [APPENDIX A – ADMC401 Code and Configuration (20kHz, 1.9us dead time)] to produce a two gate drive signals for single phase operation utilizing phase A of the built in three-phase sine-wave 16-bit PWM generation unit with parameters shown in [Table 3].

Table 3 ADMC401 parameters for single phase testing

ADMC401 Parameter	Fundamental Frequency	PWM Dead Time	PWM Min Pulse Time	Clock Frequency	PWM Frequency
Value	400 Hz	1.9 us	1.9 us	12960 kHz	5/20 kHz

Since the auxiliary device is turned on before the main device, the ADMC401 5V PWM signals are sent directly to the optical board and then to the auxiliary IGBT gate drivers. The main IGBT signals are delayed by a selected value using a simple RC timer circuit before being sent to the optical transmitter board.

Figure 18 Phase leg experimental test setup (power stage)

All tests performed use a two core saturable inductor ranging from 0-3 turns and a 275uH load inductor.

4.2 Single Phase Test Results

For the first tests, the bus voltage is varied between 150-200V and modulation index varied between .2-.4 using a two turn saturable inductor. A two microsecond timing delay demonstrates good bus voltage variation adaptation and soft switching is achieved even at a low bus voltage [Figure 19] throughout an entire line cycle [Figure 20].

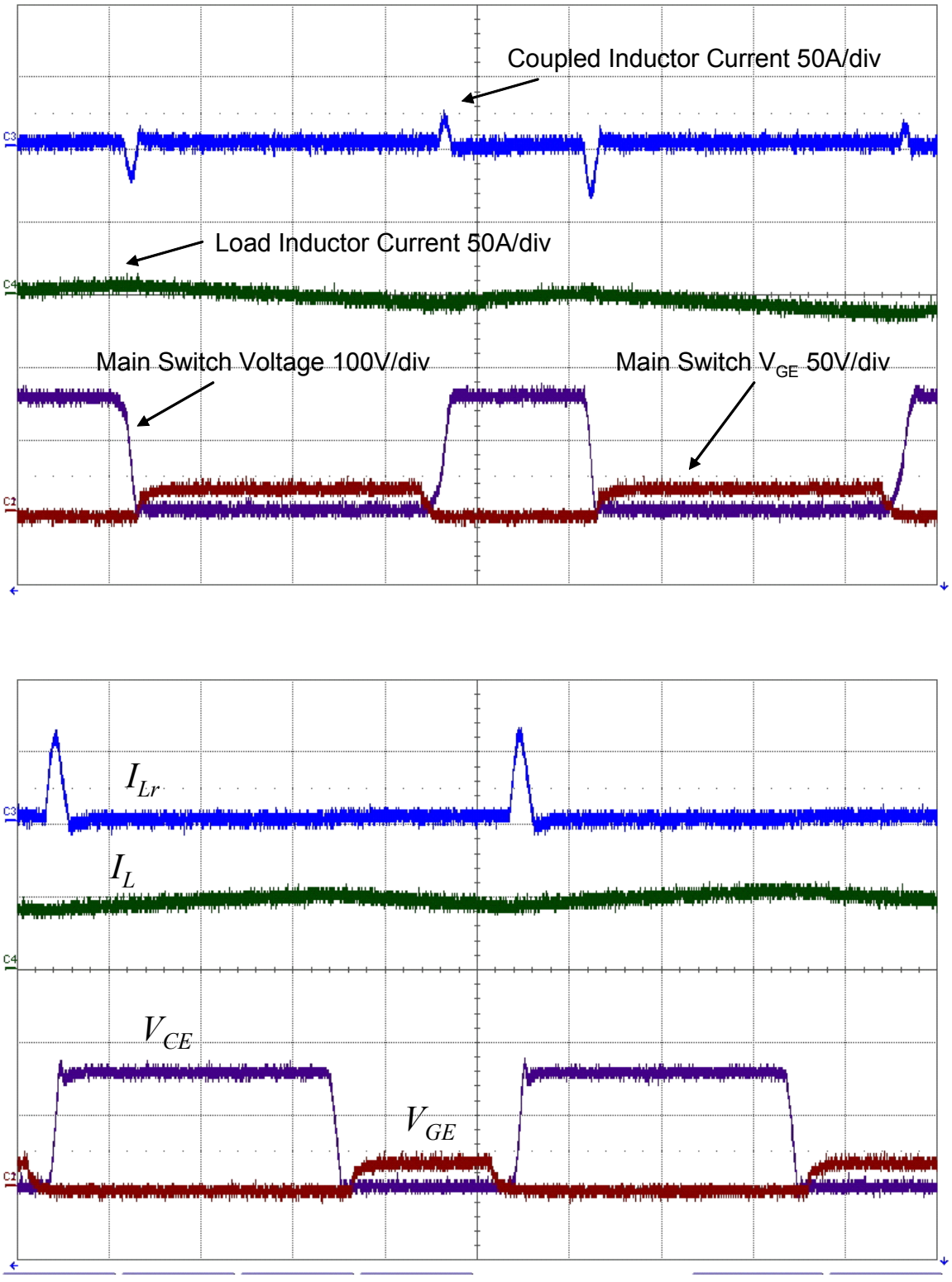

Figure 19 Single phase with V_{bus} = 150V, 10 us/div (Top) Light Load (Bottom) Heavier Load

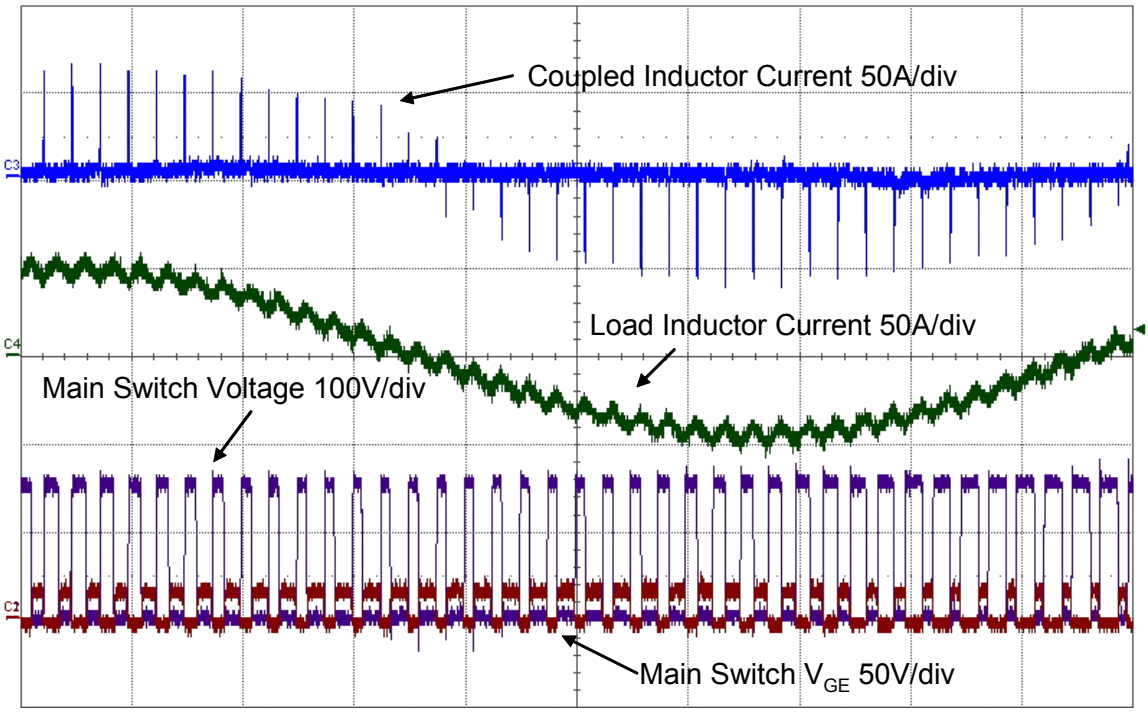

Figure 20 Single Phase Line Cycle at V_{BUS} = 150V

At bus voltages higher than 150V, coupled inductor current distortion is observed.

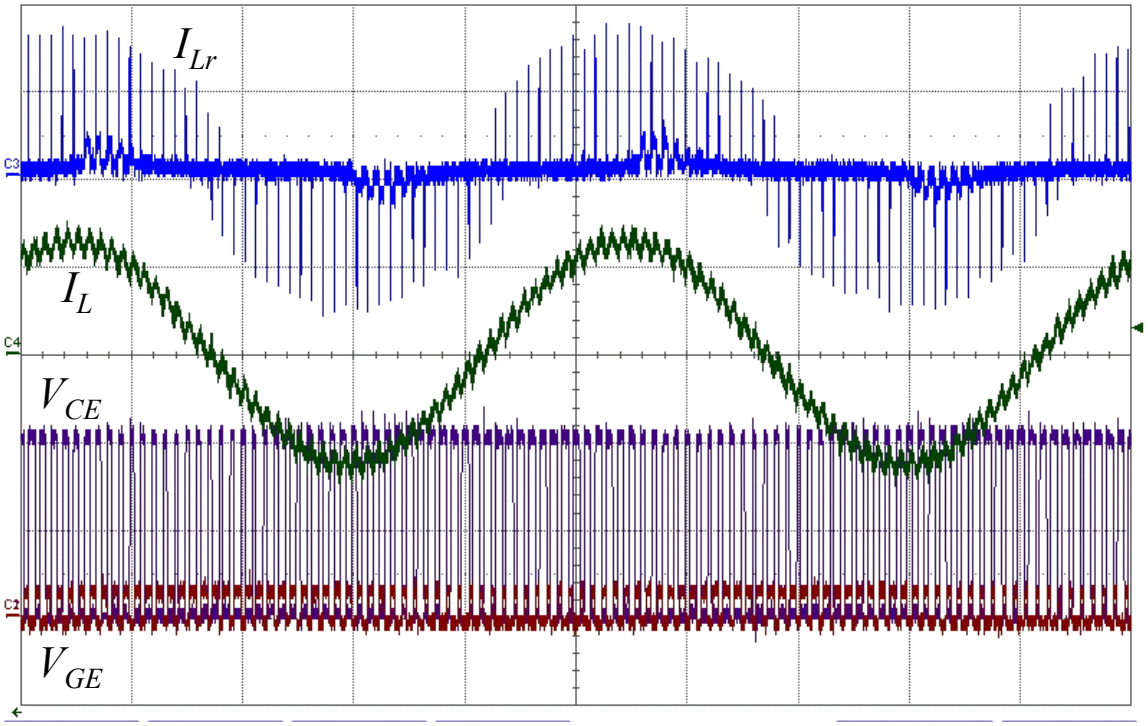

Figure 21 Coupled inductor current distortion at V_{BUS} = 200V

The distortion does not appear to have a negative effect on the output waveform, but this is not recognized as proper behavior. Residual current is apparent in the coupled inductor windings. The auxiliary switch appears to be turning off before the coupled inductor current discharges to zero. Under this condition, the residual coupled inductor current discharges through the auxiliary switch diode and auxiliary diodes into the load for the remainder of the switching cycle. The timing parameter that controls the auxiliary switch duration is T_{aux}. However, this parameter is already timed to stay on for an extended time longer than the calculated requirement to ensure that the coupled inductor discharges. Simulation is performed to determine the source of the inductor current distortion and summarized in

Chapter 5 – Inductor Current Distortion.

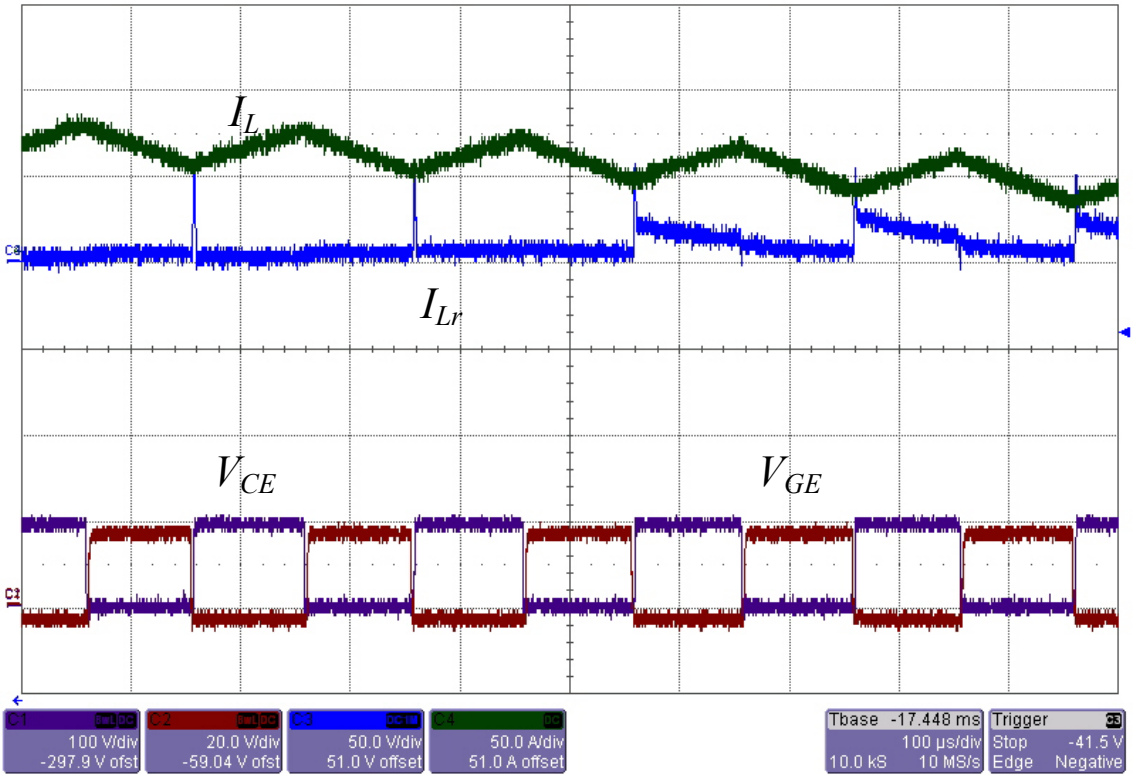

Figure 22 Zoom in of coupled inductor current distortion

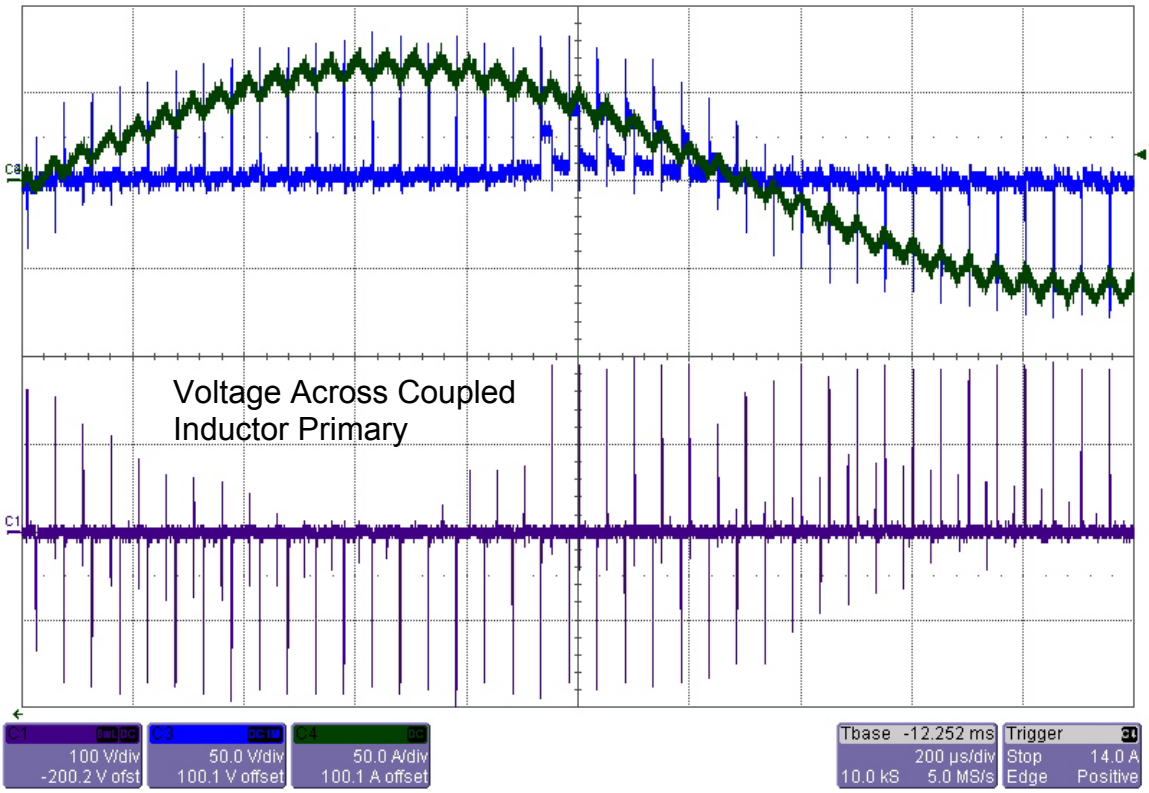

Figure 23 Coupled Inductor Voltage under distortion condition

The following tests at increased voltage show insufficient dead time between turn off of the main switch and turn on of the auxiliary switch resulting in excessive current pulses in the negative direction [Figure 24]. As an example case, assume positive load current is being carried through S_1. In accordance with the normal fixed timing protocol, S_1 is turned off and capacitor snubbed, slowing down turn off time. However, without sufficient dead-time, S_{x2} is turned on while S_1 is still in the process of turning off causing S_1 current to flow through the coupled inductor in the negative direction. S_1 then fully turns off and the coupled inductor current discharges. Note that S_{x2} and the negative direction current pulses do not provide any beneficial soft-switching function.

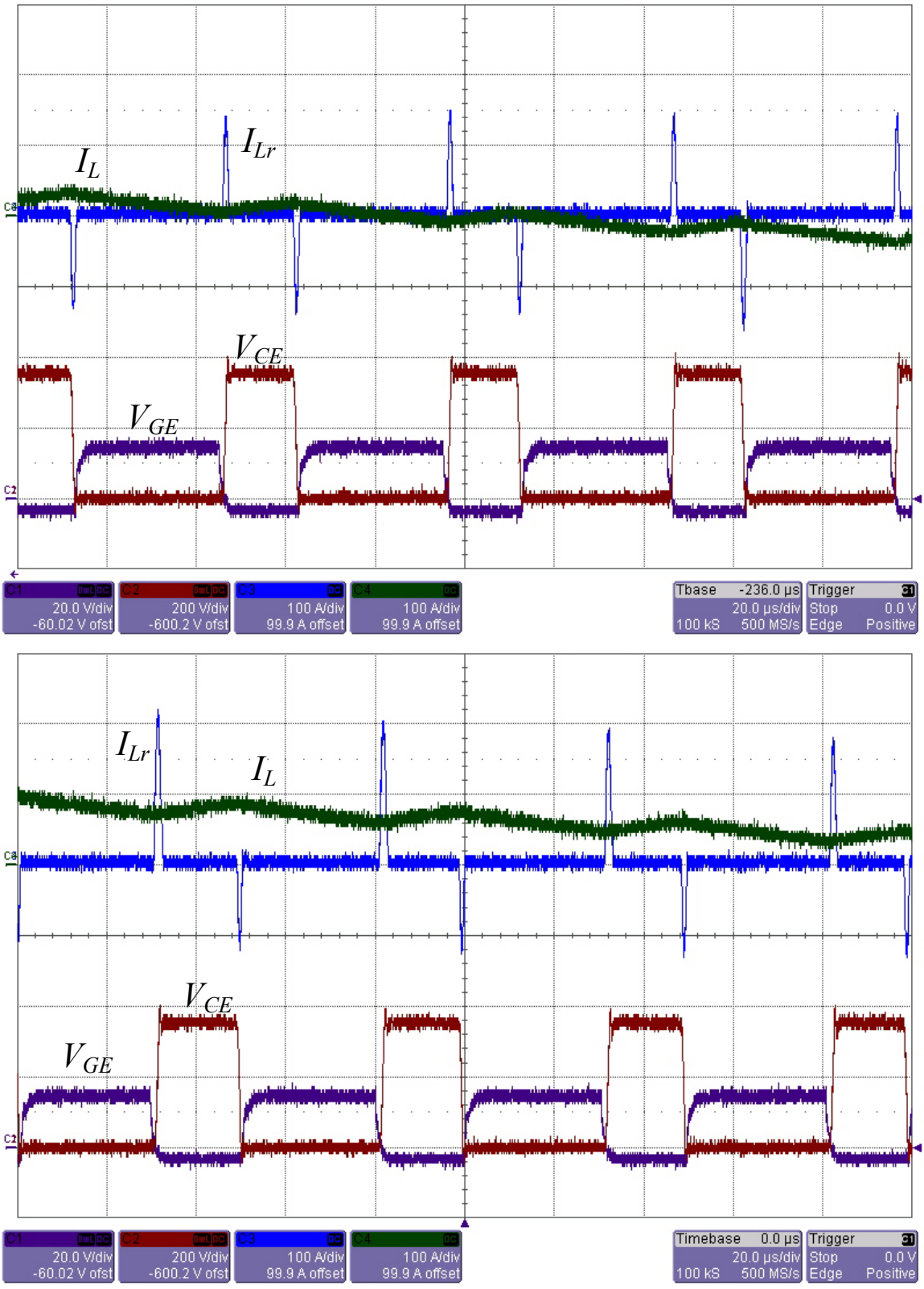

Figure 24 Single phase with Vbus = 380V, 20 us/div (Top) Light Load (Bottom) Heavier Load

4.3 Loss Comparison of Hard-Switched v. Soft-Switched Inverter

Comparative low power efficiency testing is performed with a modulation index of .375 and a load inductor of 275uH. Different load currents were tested by increasing the DC bus voltage. Measured DC bus voltage and current determine the input power and according output voltage and current determine the output power. Figure 25 illustrates the reduction in power loss for various load currents corresponding to a DC bus voltage variation from 100-400V to illustrate source adaptive capability.

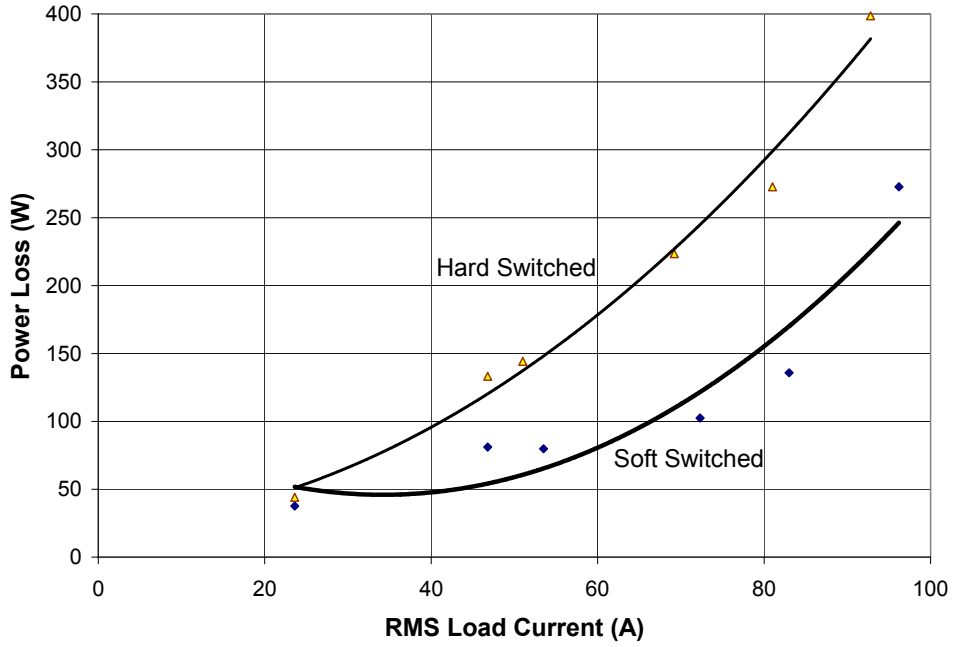

Figure 25 Loss Comparison between Hard and Soft-Switching Inverters (100-400V source variation)

Through the power range tested, the ZVSCI inverter shows a loss reduction ranging from 15-50% over the traditional hard switched inverter. Soft switching is achieved even at low source voltages and provides notable loss reduction. From these initial test results high overall efficiency is expected at higher loading conditions. Though soft-switching is achieved for the main device, switching power loss still exists and is attributed to the auxiliary switching components. Regardless, given the 125kW power level of this inverter the relative improvement in overall efficiency is very low.

4.4 Simulation Waveform Comparison

The waveforms from a single phase-leg fixed timing coupled inductor soft-switching inverter previously modeled in PSpice [Figure 26, Figure 27] are referenced to show agreements and discrepancies with experimental results.

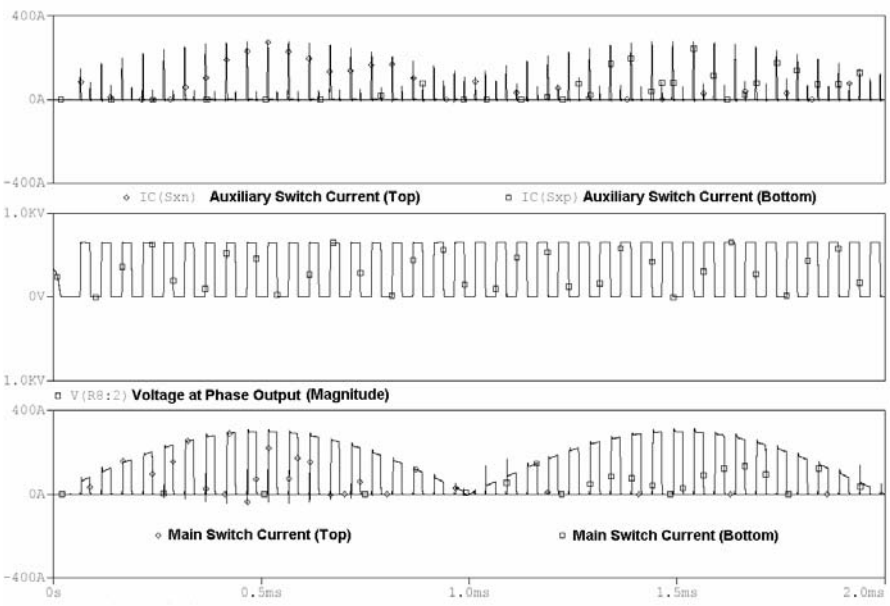

Figure 26 Line Cycle Simulations

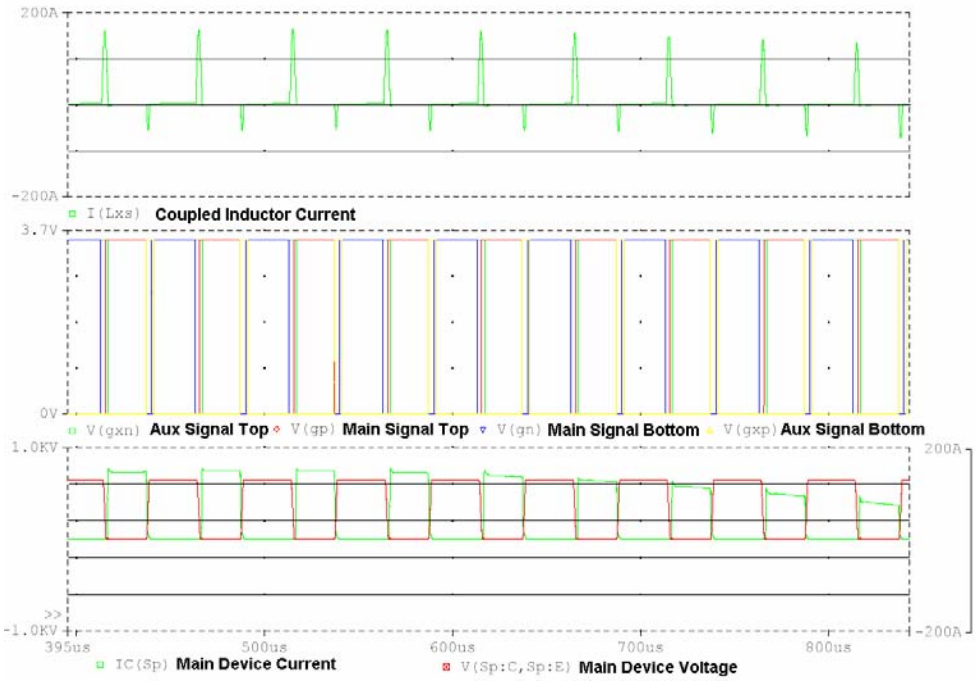

Figure 27 Simulation Timing Waveforms

Several observations are made from comparison of the simulated line cycle and timing waveforms to results in section 4.2 Single Phase Test Results. The simulated timing waveforms agree with experimental results showing that the delay timing and on timing of the main and auxiliary switches are correct for providing zero voltage turn-on of the main device and allowing sufficient coupled inductor discharge current time. Comparison also shows there is agreement of minimal overshoot voltage spike being produced on main switch turn off; verifying the main device turn-off snubber capacitor is sized correctly. Peak auxiliary switch and coupled inductor currents are also in agreement at approximately 300A. The existence of negative pulse current through the coupled inductor was predicted by simulation, but the magnitude was not accurately predicted. One potential source for this discrepancy is that the IGBT gating of the simulation does not include non-ideal characteristics of the gate-drive circuitry including power supply stability, rise/fall time and regulation. Additionally due to availability the simulation did not use spice models for the same main and auxiliary devices as used in the implementation. Differences in gate charge, capacitance and other turn on/off characteristics between the simulated and implemented devices can be a source of additional divergence in this matter. From the standpoint of general waveform fidelity and characteristics necessary for driving the load properly under soft-switching conditions, the simulation agrees well with the experimental results. The experimentally observed inductor current distortion is further investigated through simulation in Chapter 5.

Chapter 5 – Inductor Current Distortion

Characteristics of "distorted waveform"

1. Resonant branch current does not decrease to zero according to normal resonant behavior.
2. Resonant branch current remains high until auxiliary switch is gated off.
3. Turn off of auxiliary switch under non-zero current condition.
4. Increase of circulation current through auxiliary anti-parallel diode.

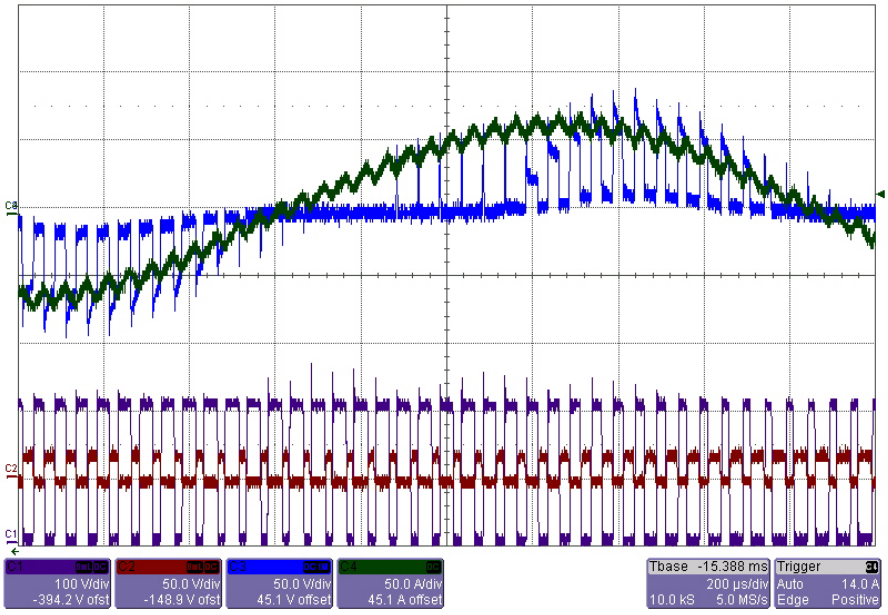

Figure 28 Distorted Waveform over a Line Cycle

Simulations are performed using Simplorer [APPENDIX B – Simplorer Schematic].

5.1 Recreation of Distortion

To investigate the cause of the distortion further, the system is modeled in Simplorer. The system is modeled using device level semiconductors and a linear transformer. Through parametric sweep analysis (1uH to 1000uH), it is discovered that the magnetizing inductance of the coupled inductor (primary) is directly linked to the distorted waveforms. Figure 29 shows a single resonant period for a system with a high

magnetizing inductance and a low magnetizing inductance. It is observed that the resonant current does not linearly decrease to zero in the system with a low magnetizing inductance. The current level at which the resonant current diverges from nominal operation is dependent on the value of the magnetizing inductance.

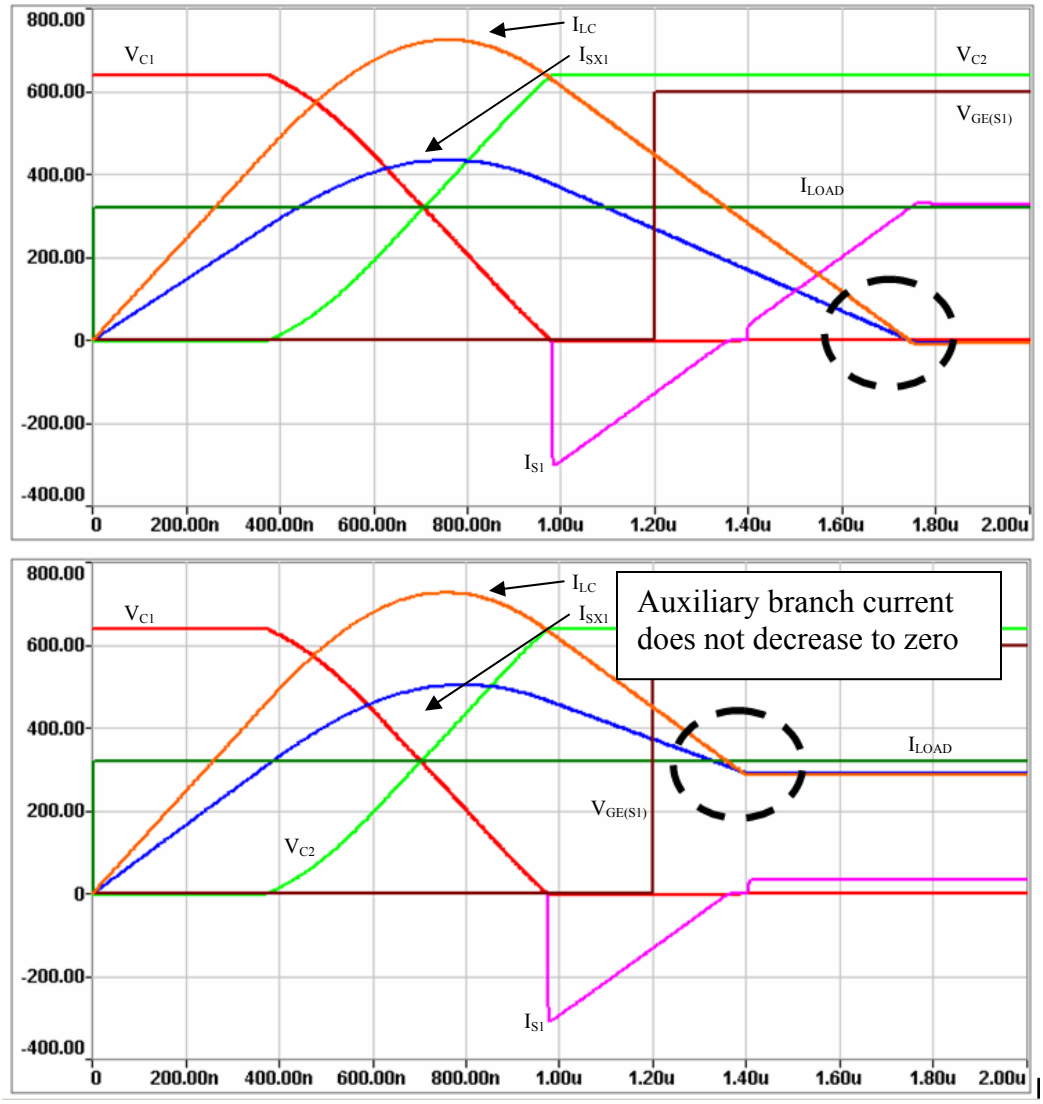

Figure 29 Simulated Resonant Period (320A Load)

Nominal Operation, L_m = 1000uH (Top), "Distorted" Condition, L_m = 10uH (Bottom), C1 Voltage (Red), C2 Voltage (Light Green), Sx1 Current (Blue), L_C Current (Orange), V_{GE} S1 (Brown & scaled), S1 & D1 Current (Magenta), Load Current (Dark Green)

The main switch and auxiliary switch are both on under this condition and it is noted that when the coupled inductor magnetizing inductance is low, a low impedance path exists through the auxiliary circuit branch [Figure 30]. The effect is current sharing between the main switch and the auxiliary switch. This is consistent with the observations of the experimentally encountered distorted waveform. Further, it is noted that the differences in the realized V_{CE} values of S_{x1} and S_1 (due to semiconductor characteristics and current level) will affect the magnitude of the undesired resonant path current.

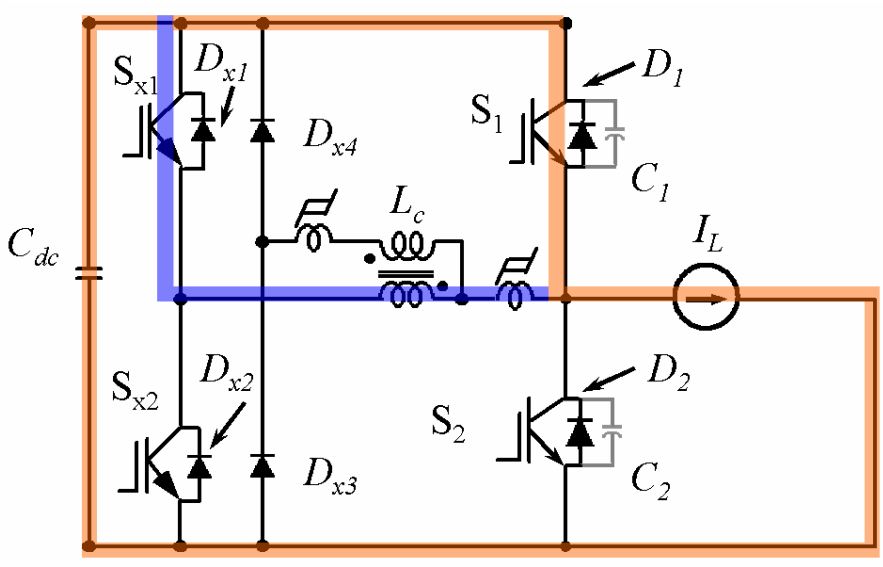

Figure 30 Low impedance paths during coupled inductor saturation

The behavior noted is consistent with transformer saturation, characterized by a significant reduction in main inductance due to excessive flux density build up. The flux density build up is caused by excessive accumulation of flux linkages - the integral of voltage applied across the primary winding:

Equation 2 Flux Linkage

$$\lambda = \int_{t1}^{t2} v(t)dt$$, where v(t) is the voltage across the primary winding, t1 is the start time and t2 is the end if the time interval.

In the experimental results [Figure 28] the circuit performs sufficiently until such a time when the accumulated flux saturates the core before the positive half cycle is complete,

causing the waveform to become distorted. When the positive half line cycle ends and the waveform changes to the other half line cycle, the coupled inductor core is reset and performs normally until the core gets saturated again part way through the negative half line cycle.

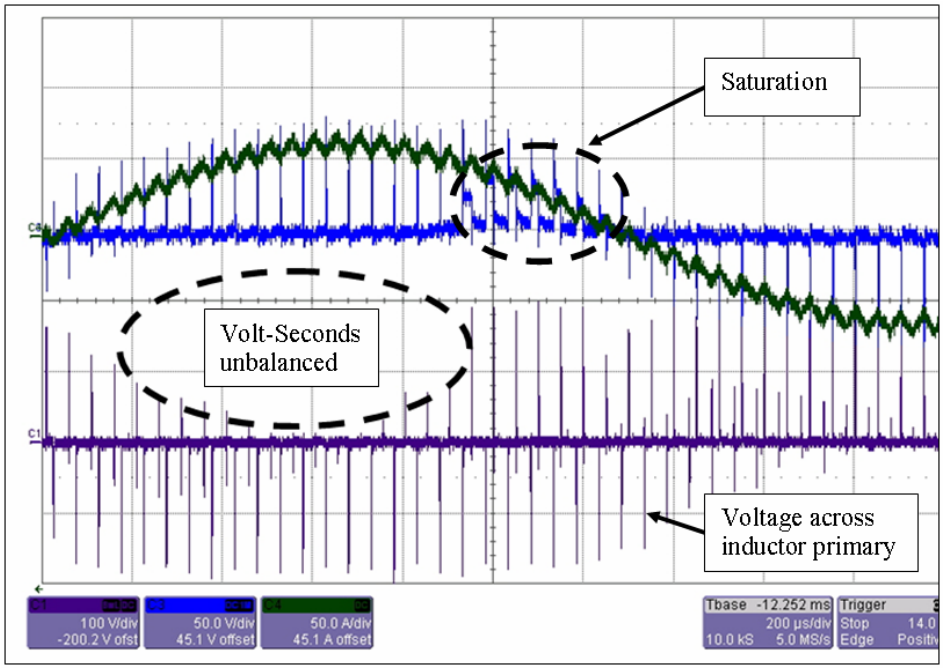

Figure 31 Volt-Seconds unbalance and saturation effect

Line cycle simulation with dynamic saturation as a function of the operating point on the B-H curve is performed [Figure 32]. The simulation is characterized by a non-static value for the magnetizing inductance that represents actual B-H curve characteristics observed in the experiment [Figure 33] with the magnetizing inductance (L_m) is proportional to the slope of the B-H curve. Correlation with experimental results is achieved, further verifying coupled inductor saturation as the cause of the current distortion.

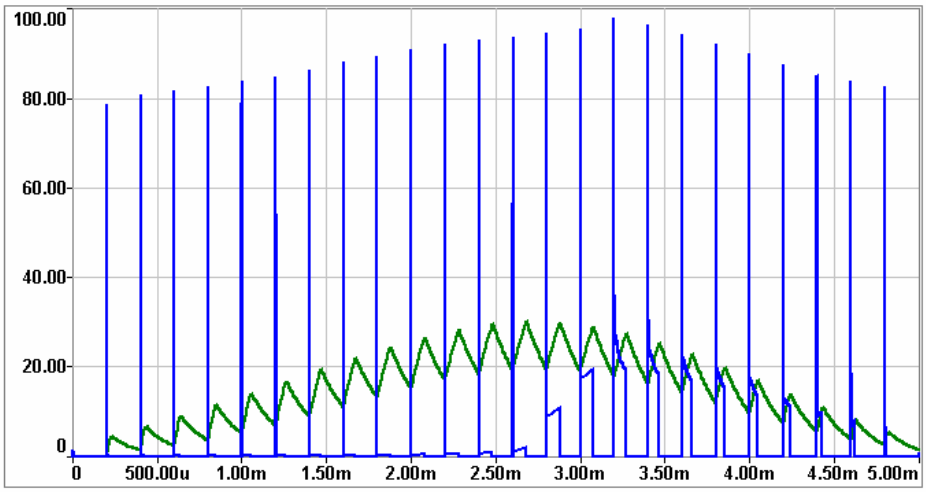

Figure 32 Line cycle simulation at 250Vdc with dynamic coupled inductor saturation

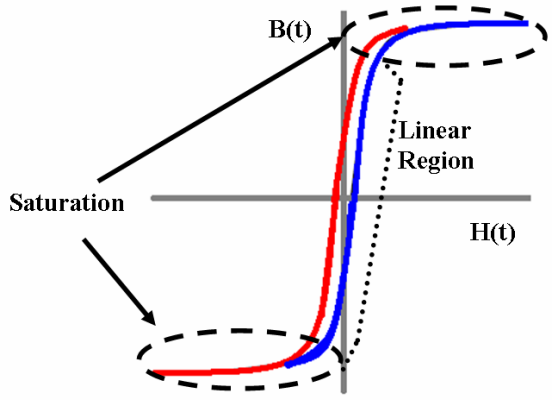

Figure 33 Coupled Inductor B-H Characteristics

5.2 Volt-Second Imbalance Root Cause Analysis

Ideally, the integral of the coupled inductor applied volt-seconds should be zero after every switching cycle [Figure 34].

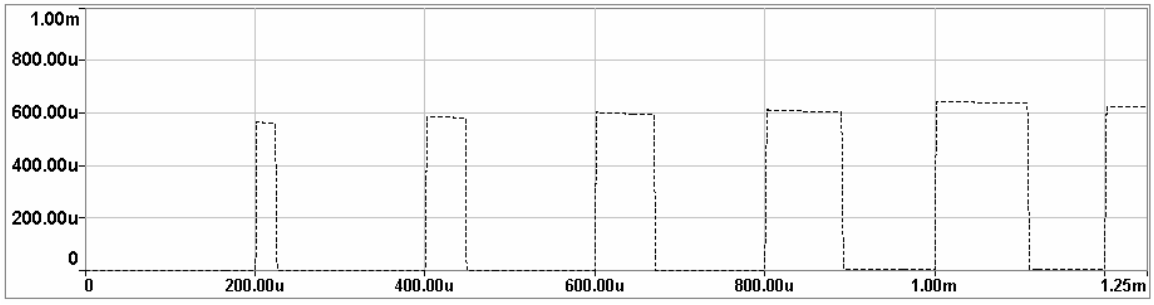

Figure 34 Flux linkage of coupled inductor primary, 320A peak current, 640VDC bus (0-45°)

5.2.1 Comparison of Selected Simulations

Simulation is performed investigating the impact of various circuit parameters and timings on coupled inductor saturation. Comparison and analysis of selected simulated waveforms is presented:

A. Current allowed to flow between main and auxiliary circuits unimpeded (no saturable inductor): Freewheeling and magnetizing currents not mitigated.
B. Ideal saturable inductor - current only allowed in direction of previous current: Freewheeling currents not affected, magnetizing current path through main IGBT is eliminated.
C. Current only allowed to flow between main and auxiliary circuit when auxiliary switch is ON
D. Current only allowed to flow between main and auxiliary circuit when either auxiliary or main switch are ON
E. Ideal saturable inductor with increased coupled inductor winding resistance (100x)

For the following simulations, the top waveform is the integral of the applied voltage across the coupled inductor primary (black dashed line) according to [Equation 2]. The lower waveform illustrates the period of the waveform when the primary of the coupled inductor has a negative voltage applied to reset the volt-seconds. Voltage applied to primary (red), Voltage applied to secondary (dark blue), Primary current (magenta), Secondary current (light blue), Auxiliary IGBT applied gate voltage (thick dashed black), Main IGBT applied gate voltage (thin dashed black). Currents are in Amps and scaled 500x. Transformer voltages are in Volts and scaled 1x. IGBT gate voltages are in Volts and scaled 25x.

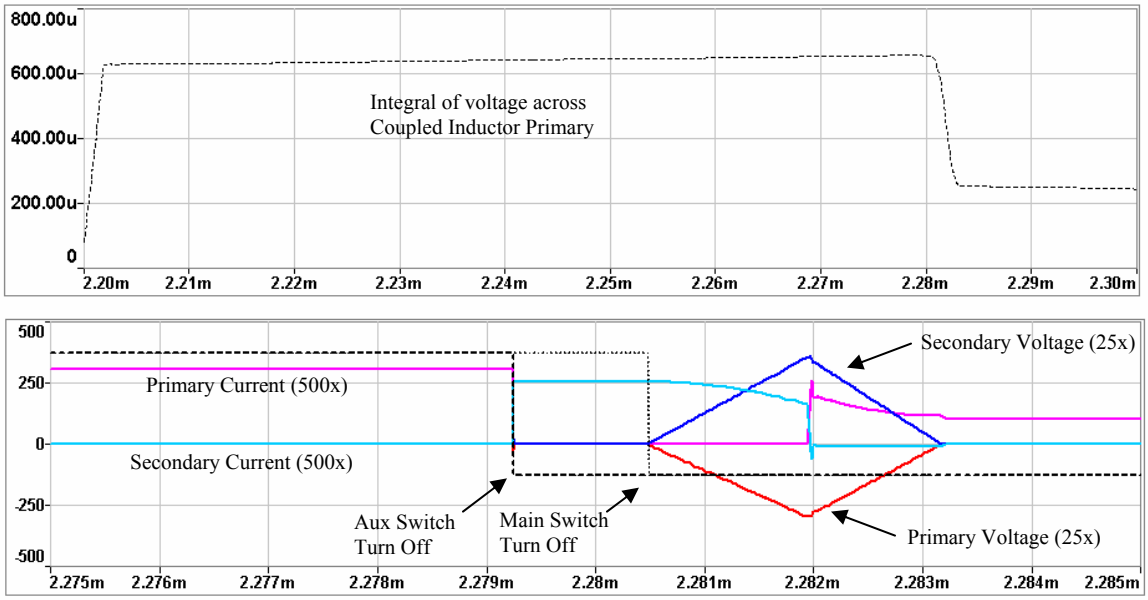

Figure 35 Condition A, unimpeded current flow

Condition A Notes: Volt second balance reset does not start until both main and auxiliary switches are turned off. Volt second balance is not reset, nor is magnetizing current. This imbalance increases every switching cycle over the duration of the ½ line cycle. Reverse bias applied is due to the voltage of resonant capacitor C2. However, C2 is discharging during this period and does not provide sufficient reverse bias to balance out the applied volt-seconds.

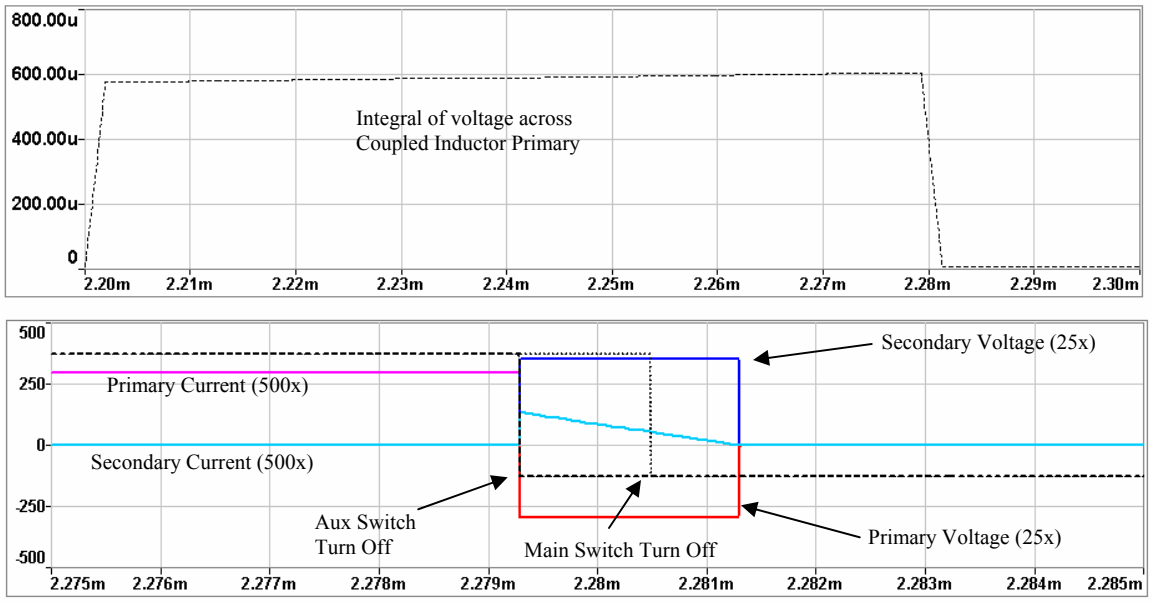

Figure 36 Condition B, ideal saturable inductor

Condition B Notes: Volt seconds accumulation slowly increases (positive integral slope) during time when main and auxiliary switches are on. Volt second balance reset begins when auxiliary switch is turned off. Complete volt second balance reset is achieved in the switching cycle.

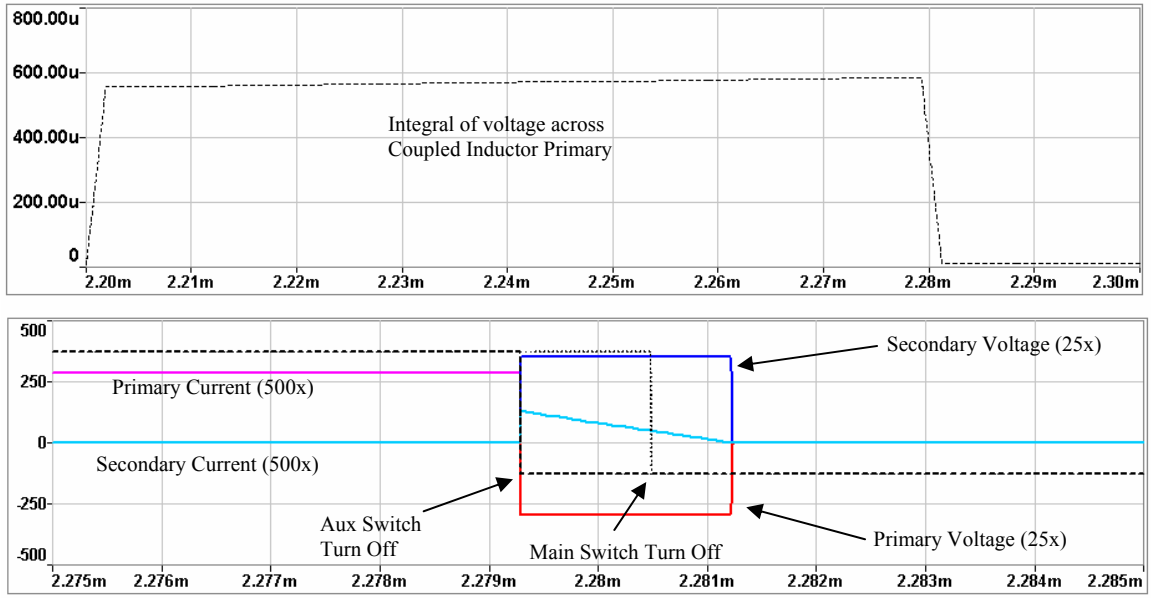

Figure 37 Condition C, current flow only allowed when auxiliary switch is on

Condition C Notes: Similar results to condition B with slow increase in volt second imbalance (positive integral slope) during the time when main and auxiliary switches are on.

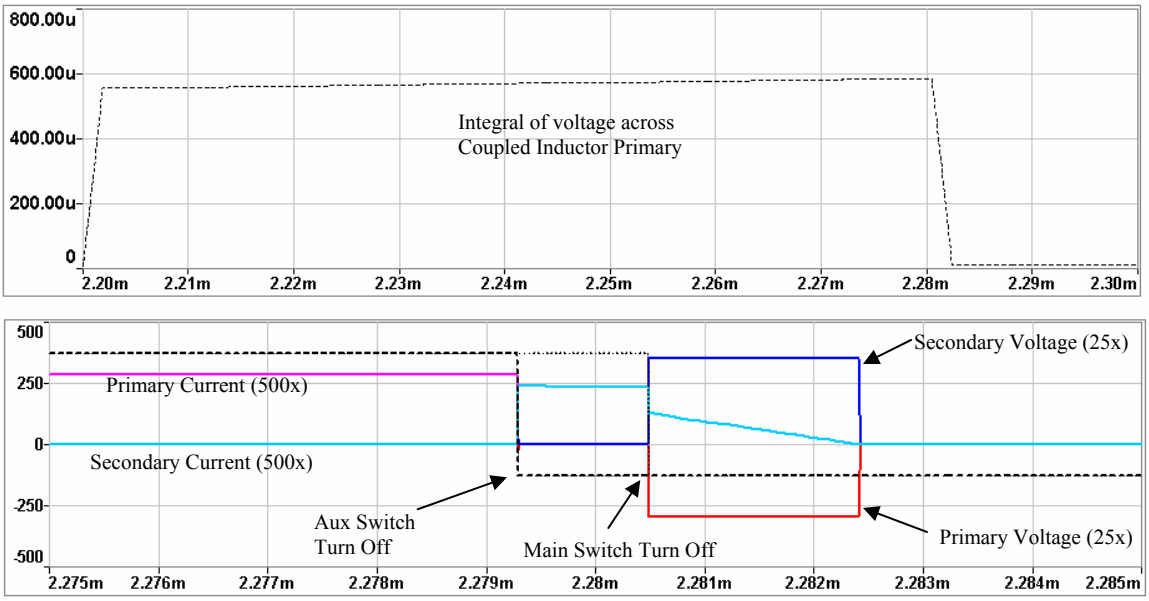

Figure 38 Condition D, current flow only allowed when either main or auxiliary switch is on

Condition D Notes: Same result as C, but volt second balance reset does not begin until main switch is turned off.

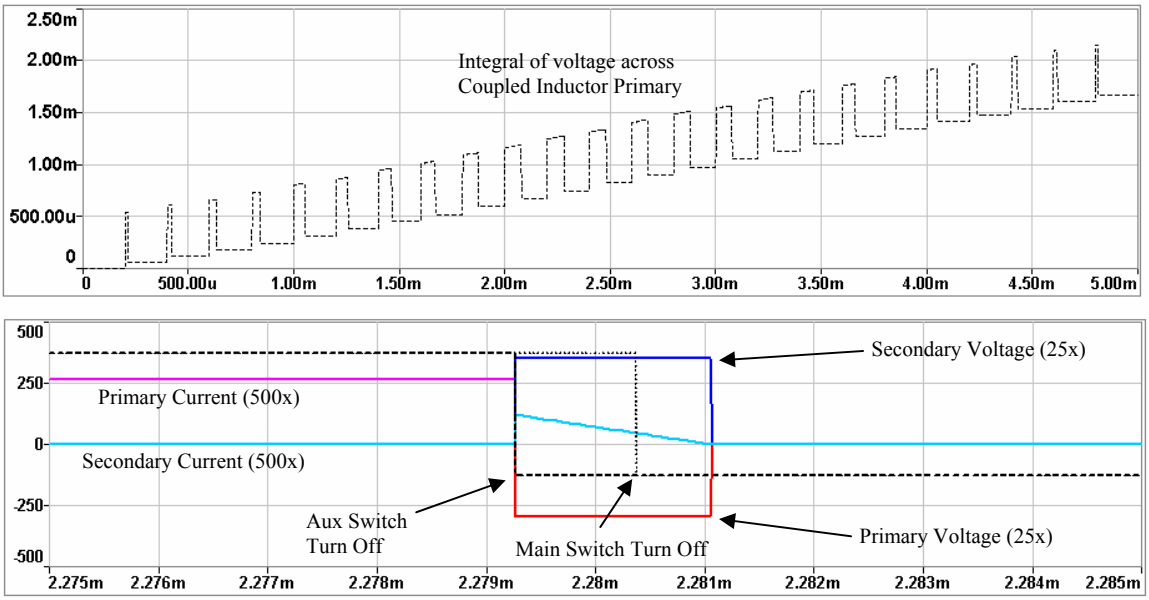

Figure 39 Condition E, Ideal saturable inductor with increased coupled inductor winding resistance

Condition E Notes: Cycle waveforms are similar to C except that current in the coupled inductor windings decreases to zero faster in condition E. The fast current decay results in volt second imbalance observed over ½ line cycle. Peak volt-second integral is about 4x that of the converter with lower winding resistance. This same effect is noticed when increasing the auxiliary circuit diode voltage drop (but is not observed with practical numbers for diode voltage drop and bulk resistance).

5.2.2 Quantification of Volt-Second Imbalance

The energy stored in the coupled inductor after the auxiliary switch is gated off is due to the residual magnetizing current and as such it is needed for resetting the volt seconds balance:

Equation 3 Coupled Inductor Energy and Inductor Discharge Time (dt)

$$E_{Lc} = 1/2 \times L_m \times I_m^2$$
$$dt = L_m \times I_m \div V_{RESET}$$
$$V_{RESET} = V_{DCBUS} - 2 \times V_{diode} - R_{winding} \times I_m$$

In the case of high coupled inductor winding losses a higher portion of the residual coupled inductor energy is dissipated as heat since the resulting V_{RESET} is lowered by the voltage drops in the auxiliary branch. So for complete volt-seconds balance reset of the applied volt-seconds during linear charge, resonant period and linear discharge:

Equation 4 Volt-second reset time requirement

$$dt \times V_{RESET} \approx Duty \times F_{sw} \times V_{DCBUS}$$

In all conditions simulated, a positive slope in accumulated volt seconds from the end of the resonant period to the turn off of the auxiliary switch is observed. This is attributed to the difference in V_{CE} drop across the main and auxiliary IGBTs [Figure 40]. Since a small current is flowing through the auxiliary IGBT compared to a larger current flowing through the main IGBT, the voltage drops are different. This creates a small forward bias of the coupled inductor after the resonant period is complete as long as the auxiliary switch is gated on. The consequence of extended auxiliary gate on time is a slow increase

in the applied volt-seconds integral [Figure 35, Figure 36, Figure 37, Figure 38]. Higher load and higher duty cycle result in a faster volt seconds increase [Figure 41].

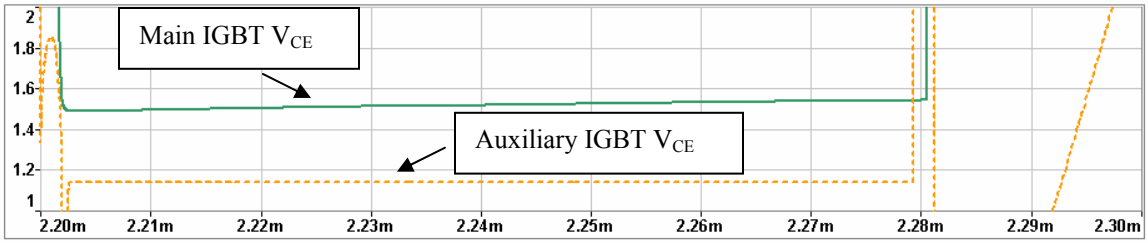

Figure 40 V_{CE} comparison of main and auxiliary IGBTs @ 50-70A load current

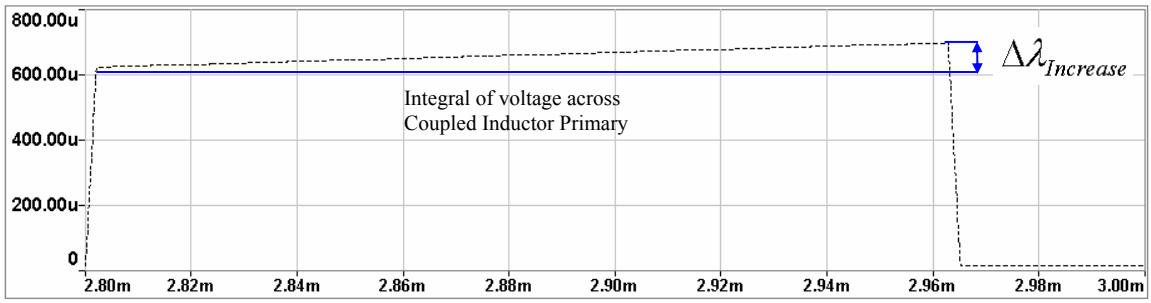

Figure 41 Volt Seconds integral at high load (130A) and high duty (85%)

The following equation is derived for quantifying this effect on overall coupled inductor design as a function of duty cycle, load current and switch timing - V_A and V_{AX} are defined as the node voltages at the center point of the main switches and auxiliary switches respectively:

Equation 5 Increase in Flux Linkage Due to Coupled Inductor Forward Bias

$$\Delta\lambda_{Increase} = \int_{tchg+tres+tdischg}^{taux} (V_{AX} - V_A)dt$$

Where:

$$V_{AX} = V_{DCBUS} - V_{CE,Sx1}(i), i \approx 0$$

$$V_A = V_{DCBUS} - V_{CE,S1}(i)$$

In the experimental condition, the auxiliary switch on time is a function of duty cycle: $taux = fsw \times D$, yielding the aforementioned dependence. The RC timer realizes fixed timing by directly passing the normal PWM signal to the auxiliary device. The signal is

delayed by the RC timer and sends that delayed turn on signal to the main device; the turn-off signal is likewise delayed. The increased flux linkage effect can be minimized with modification to the timing strategy to limit the auxiliary switch on time to that more closely with the longest resonant period calculated in Chapter 3. However, addressing this issue requires adding complexity to the fixed timing circuitry.

5.3 Summary of Simulation Results

From simulation and experimental observation the integral of the applied voltage to the coupled inductor primary is observed to be non-zero. The original simulations did not take into account the maximum core flux density or saturation related effects such as inductance decrease. In the simulation, it is noted that increasing DC bus voltage, increasing duty cycle and high current exacerbate the problem: more volt-seconds accumulated over the same time interval increases the likelihood of saturation. This explains why significant distortion was not observed until testing at a DC bus voltage in excess of 200V.

In the condition where the saturable inductor is not used or is not designed properly, increased load current causes the resonant capacitor to be more quickly discharged providing less reverse bias time. This is illustrated by the lack of a reduced reverse bias period (increase in volt second imbalance) as the load current increases throughout the first half of the line cycle. Though a saturable inductor is used in the experimental line cycle test setup, the collective design is shown to be ineffective.

5.3.1 Primary Simulation Findings

Through simulation, and comparison to experimental waveforms several circuit parameters are noted to have a significant effect on coupled inductor saturation and related current distortion.

1. The coupled inductor is shown to enter saturation due to volt-second imbalance even when the magnetizing current is reset. Previous literature has noted that the saturable inductor resets the coupled inductor magnetizing current. However, this simulation shows that the introduction of a properly designed saturable inductor enables the volt-second balance reset period to begin. The design of the coupled

inductor to mitigate both magnetizing current and maintain volt-second imbalance is important.

2. Long gate timing of the auxiliary switch is shown to have a significant effect on the coupled inductor saturation. When the auxiliary switch and main switch are both on a small forward bias exists across the coupled inductor due to the difference in V_{CE} drops of the main and auxiliary switches. The problem increases proportional to load current increase. The auxiliary switch should be turned off at the completion of the resonant period to prevent an undesirable increase in accumulated volt seconds. Proper timing of the auxiliary switch can reduce required coupled inductor B_{MAX} and prevent saturation. Under conditions simulated, a >15% increase in flux linkages is noted. If this is not corrected in the timing circuitry, the coupled inductor design needs to account for this effect in the coupled inductor design using Equation 5.
3. Magnetizing current is necessary for achieving volt-second balance. Increasing the winding resistance of the primary and secondary sides of the transformer will increase the reset speed of the magnetizing current through dissipation, but exacerbate the volt-second imbalance problem. If the magnetizing current is reset too quickly, the coupled inductor will stop being reversed biased before the volt-second reset is complete. The losses in the path of the magnetizing current must be kept to a minimum. Even with the utilization of a saturable inductor, the volt seconds can become unbalanced over a line cycle if the coupled inductor winding resistance and auxiliary diode voltage drop is too high.

5.3.2 Best Practices for Circuit Operation Considering Saturation

Further conclusions and discussion on best practices for coupled inductor saturation prevention are presented below based on additional simulation and design principles:

1. Increase B_{MAX} handling capability of the coupled inductor through use of a larger core: The coupled inductor can be designed to withstand a higher B_{MAX} before saturation by increasing the cross sectional area. Since volt-second imbalance is accumulated through an entire half cycle rather than one switching cycle.

However, the inductor size and cost are adversely increased and this type fix is not optimal.

2. Increase magnetizing inductance [Equation 6]: This makes the inductor behave more ideally and achieve higher flux densities before exhibiting inductance reducing saturation behavior (increase B-H slope Figure 33). Reducing the air gap or using a higher permeability core both can achieve this, but the contributions may not be enough to prevent saturation. These techniques should be viewed only as optimization techniques to achieve the most advantageous coupled inductor size or to prevent partial saturation.
3. Increase B_{MAX} handling capability of the coupled inductor by increasing the number of turns on primary: This has an adverse effect on the efficiency because of increased copper losses. As shown by simulation, increased resistance can further lead to worse coupled inductor saturation – as such, using a higher permeability core may be preferred.
4. Optimize saturable inductor for minimal current circulation: Two coupled inductors are used to prevent multiple paths for saturation current.
5. Decrease turns ratio: Choosing a high coupled inductor turns ratio reduces the reverse bias voltage applied to the coupled inductor during the reset period. The cumulative impact of this does not increase the needed Bmax because the reverse bias time is increased. However, a small flux offset is observed by the end of the ½ line cycle. It is recommended, that coupled inductor turns ratio be selected at the minimum value determined by normal design parameters, but this was not shown to significantly impact saturation.
6. Auxiliary gate timing: The auxiliary switch needs to be gated off several microseconds before the main switch is turned off to allow as much reverse biased time as possible before main switch shut off.
7. Change the ratio of primary leakage inductance to secondary leakage: In an attempt to keep the primary path impedance high even during saturation, the ratio of primary to secondary leakage inductance is increased (conserving equivalent resonant inductance). This has little effect since the ratio of the magnetizing inductance to the leakage inductance is several orders of magnitude.

8. Reduce diode freewheeling current: The existence of freewheeling current in the auxiliary circuit introduces a DC current bias over a half line cycle which increases the required coupled inductor B_{MAX} handling capability. From simulation this has little appreciable effect compared to other causes, but should be addressed for optimal design.
9. Increase resonant capacitance: In the case where no coupled inductor is used (or poorly designed), increasing resonant capacitance will increase the amount of time that the coupled inductor is reverse biased after the main switch is turned off. However, this will have the subsequent effect of increasing the resonant time where positive bias is applied to the coupled inductor – negating any net benefit.
10. Design for minimum coupled inductor winding resistance.

Equation 6 Magnetizing Inductance

$$Lm = \mu \times n1 \times Ac \div lm$$

Chapter 6 – Closing Remarks and Future Work

Much research continues in the realm of soft switching inverters to achieve their promised benefits over traditional hard switched inverters. Reduction in complexity and added cost along with robust design and small space requirements are some crucial parameters in the adaptation of soft switching three phase inverters into the mainstream power electronics marketplace. A single phase leg of a three phase fixed timing coupled inductor inverter is implemented in this thesis. Through theoretical analysis, discussion and test results the reality of the fixed timing coupled inductor inverter as an advanced power electronics solution is furthered.

6.1 Accomplishments

In order to select the appropriate inverter, Chapter 1 reviews previous research on soft-switching topologies and associated systems integration issues. Through discussion, merits and drawbacks of various inverter classifications and specific inverter types are investigated. Comparison of various inverters and rational is given for the selection of the inductor coupled zero voltage transition inverter fitting the application specific requirements; no modification to the main control scheme, occupies same space, no bus bar or DC link modificatiosn. Chapter 2 proceeds to explain the fundamental operations and design procedures specific to the fixed timing version of the inductor coupled inverter. Dialogue is given with regards to the evolution of previous versions of the coupled inductor inverter. The inherent simplicity of the fixed timing control methodology is illustrated and the timing parameter selection provides the basis for prototype control parameters and hardware design.

Description of various components used in implementing the single phase inverter is presented in Chapter 3 along with varied levels of design explanation. Particular attention is given to discussion and study of the auxiliary power device selection. Theoretical analysis and much testing are performed as a basis for the auxiliary device selection. Though many different devices are suitable auxiliary device candidates, the best device for a robust and efficient design is a device with excellent thermal transient response characteristics but not an excessively small die size. Coupled with a desire for

low cost and small available space, a six-pack module with low average power dissipation characteristics is selected to be operated at two times the continuous collector current rating.

Single phase test setup and results are presented in Chapter 4. Some problems come across during the testing process are remedied. Care must be taken to reduce circulation current and minimize negative current pulses in the coupled inductor. Circuit layout must minimize space and stray inductance. Waveform capture analysis shows that soft switching is achieved through a range of loads and bus voltage conditions. In section 4.3 efficiency gains over the traditional hard-switched inverter are evident at the power levels tested (Figure 25), but do not represent a significant impact on overall efficiency.

Chapter 5 investigates the causes of non-ideal waveform characteristics encountered in experimentation. Careful consideration must be paid to coupled inductor winding resistance, gate timing, saturable inductor design and volt-second balance to achieve optimal coupled inductor design and prevent saturation.

6.2 Future Work

Since the completion of the single phase testing, functional testing of the three-phase fixed timing coupled inductor inverter has been successfully completed in an air cooled environment. This thesis represents another step towards fully understanding the full potential and complexity of soft-switching inverter topologies. Though historically highly touted, many issues still exist with implementing soft-switching topologies in the transition to becoming a viable industry solution. The two key topics delved into in this implementation in which future work is requisite are:

- Cost vs. Reliability - Attempting to reduce inverter cost by auxiliary device size reduction will have a noteworthy impact on overall inverter reliability. Full reliability testing and subsequent failed auxiliary devices should be analyzed. Design and testing of custom six pack modules with low cost/small IGBT dies and beefed up wire bonds with comparison to off the shelf modules is recommended.
- Design Complexity – The design of the final coupled inductor and saturable inductor included several designs that were trial and error in nature. The

simulation work performed deepens the understanding of the circuit operation to enable better designs that prevent saturation, but a succinct design process needs to be fully developed and proven. Additionally, the simple RC timer circuitry is proven not optimal for coupled inductor sizing; a new design for this circuitry is a potential subject for future work.

It was also shown that some perceived benefits such as efficiency improvements are not significant enough alone to warrant implementation. The commercial motivating factors need to be revisited and the EMI benefits fully quantified. There is consistently debate about which topology is superior for any particular application based on component count, performance, control complexity, size, cost, and without full design for production analysis. This gap makes it difficult for companies to adopt soft switching technologies without a track record or clear necessary path. Furthermore, advances are continually made in power switching device technology; reducing switching and conduction losses. EMI sources and mitigation techniques are becoming better understood through advanced modeling and circuit analysis and key parasitic circuit elements are able to be corrected within components and layout. Advances are also being made in the way power devices are driven by modified hard switched inverter switching schemes and controlled gate voltage and current (device turn on/off speed) to reduce EMI [33] [34] [35]. Combined, all of these developments will impact the future of soft-switching inverter technology and need to be researched thoroughly and applied.

The known problematic issues of existing soft-switching inverter topologies need to continually be addressed using the most recent advances in all related areas to advance the practicality/commercialization of soft-switching inverters. More importantly, full understanding of the benefits and limitations of these topologies will lead to new topologies and new ways of thinking as well as incrementally improving existing topologies. Regardless of whether or not soft-switching inverters become main stream, the associated research is valuable. Better power electronics solutions are an inevitable impact due to the high level of fundamental understanding of power electronics components and systems that is necessary to create an optimal soft-switching inverter.

APPENDIX A – ADMC401 Code and Configuration (20kHz, 1.9us dead time)

START main.h HEADER FILE

```
{*************************************************************************
***************
*                                                                       *
* Application: Three-phase Sine-wave Pulse Width Modulation with the ADMC401
*
*                                                                       *
* Embedded Control Systems                                              *
* Analog Devices Inc.                                                   *
*************************************************************************
**************}

#ifndef MAIN_INCLUDED
#define MAIN_INCLUDED

{*************************************************************************
***************
* General System Parameters and Constants                               *
*************************************************************************
**************}

.CONST  Cry_clock     = 12960;      {Crystal clock frequency [kHz]          }

#include <admc401.h>;
#include <macro.h>;

{*************************************************************************
********************}
{ Library: PWM block
}
{ file   : PWM401.dsp                                                     }
{ Application Note: Usage of the ADMC401 Pulse Width Modulation Block
            }

.CONST  PWM_fout=400;             {Desired maximum fundermental output freq}
.CONST  PWM_deadtime    = 1900;         {Desired deadtime [nsec]              }
.CONST  PWM_minpulse    = 1900;         {Desired minimal pulse time [nsec]      }
.CONST  PWM_syncpulse   = 1900;         {Desired sync pulse time [nsec]       }

{*************************************************************************
********************}
```

```
{*************************************************************************
**********************}
{ Library: Trigonometric functions                                        }
{ file   : TRIGONO.dsp
}
{ Application Note: Basic trigonometric functions on the ADMC401
}

{ None                                                                    }
{*************************************************************************
**********************}

{*************************************************************************
**********************}
{ Application specific constants and header files                         }
{ file   : none                                                           }
{*************************************************************************
**********************}


#endif
```

START ADMC401.h HEADER FILE

```
{*************************************************************************
***************
*                                                *
* Library: Configuration Constants for the ADMC401                        *
*                                                *
* File: ADMC401.h                                        *
*                                                *
* Analog Devices Inc.                                    *
*************************************************************************
***************}

#ifndef ADMC401_INCLUDE
#define ADMC401_INCLUDE

{
 This include file defines important ADMC401 addresses.  The names
 defined below can be used in user programs by "including" this file.
 This file defines:
   - names for the peripheral registers of the ADMC401
   - names for the memory mapped core registers of the ADMC401
   - interrupt vector table addresses
}
```

```
{ peripheral registers of the ADMC401 }

.CONST  PWMTM     =   0x2008;     {PWM timer register}
.CONST  PWMDT     =   0x2009;     {PWM dead time register}
.CONST  PWMPD     =   0x200A;     {PWM pulse deletion}
.CONST  PWMGATE   =   0x200B;  {PWM gate register}
.CONST  PWMCHA    =   0x200C;   {PWM channel A register}
.CONST  PWMCHB    =   0x200D;   {PWM channel B register}
.CONST  PWMCHC    =   0x200E;   {PWM channel C register}
.CONST  PWMSEG    =   0x200F;    {PWM segment selection}
.CONST  AUXCH0    =   0x2010;   {Auxiliary PWM channel 0 duty cycle}
.CONST  AUXCH1    =   0x2011;   {Auxiliary PWM channel 1 duty cycle}
.CONST  AUXTM0    =   0x2012;   {Auxiliary PWM channel 0 period}
.CONST  AUXTM1    =   0x2013;   {Auxiliary PWM channel 1 period}
.CONST  MODECTRL  =   0x2015;  {MODE control register}
.CONST  SYSSTAT   =   0x2016;     {System status register}
.CONST  WDTIMER   =   0x2018;   {Watchdog timer register}
.CONST  PICVECTOR =   0x201C;   {ISR address           }
.CONST  PICMASK   =   0x201D;   {IRD mask regsiter      }
.CONST  EIUCNT    =   0x2020;   {Encoder count register }
.CONST  EIUMAXCNT =   0x2021;   {Encoder max count register }
.CONST  EIUSTAT   =   0x2022;   {Encoder status register    }
.CONST  EIUCTRL   =   0x2023;   {Encoder control register   }
.CONST  EIUPERIOD =   0x2024;   {Encoder loop timer period register}
.CONST  EIUSCALE  =   0x2025;   {Encoder loop timer scale register}
.CONST  EIUTIMER  =   0x2026;   {Encoder loop timer}
.CONST  EETCNT    =   0x2027;   {Latched value of EIUCNT register}
.CONST  EIUFILTER =   0x2028;   {EIU filter control register}
.CONST  EIZLATCH  =   0x2029;   {EIZ latch register}
.CONST  EISLATCH  =   0x202A;   {EIS latch register}
.CONST  ADC0      =   0x2030;   {ADC0 register          }
.CONST  ADC1      =   0x2031;   {ADC1 register          }
.CONST  ADC2      =   0x2032;   {ADC2 register          }
.CONST  ADC3      =   0x2033;   {ADC3 register          }
.CONST  ADC4      =   0x2034;   {ADC4 register          }
.CONST  ADC5      =   0x2035;   {ADC5 register          }
.CONST  ADC6      =   0x2036;   {ADC6 register          }
.CONST  ADC7      =   0x2037;   {ADC7 register          }
.CONST  ADCCTRL   =   0x2038;   {ADC control register     }
.CONST  ADCSTAT   =   0x2039;   {ADC status register }
.CONST  ADCXTRA   =   0x203B;   {extra ADC data register }
.CONST  ADCOTR    =   0x203C;   {ADC out of range register  }
.CONST  PIOLEVEL  =   0x2040;   {PIO level control register }
.CONST  PIOMODE   =   0x2041;   {PIO mode control register  }
.CONST  PIOPWM    =   0x2042;   {PIO PWMTRIP control register }
```

```
.CONST  PIODIR    =   0x2044;   {PIO direction register     }
.CONST  PIODATA   =   0x2045;   {PIO data register}
.CONST  PIOINTEN  =   0x2046;   {PIO interrupt enable register }
.CONST  PIOFLAG   =   0x2047;   {PIO interupt flag register  }
.CONST  ETUA0     =   0x2050;   {ETU0 Event A capture register }
.CONST  ETUB0     =   0x2051;   {ETU0 Event B capture register }
.CONST  ETUAA0    =   0x2052;   {ETU0 Event AA capture register }
.CONST  ETUA1     =   0x2053;   {ETU1 Event A capture regsiter}
.CONST  ETUB1     =   0x2054;   {ETU1 Event B capture register}
.CONST  ETUAA1    =   0x2055;   {ETU1 Event AA capture register}
.CONST  ETUTIME   =   0x2056;   {ETU timer value}
.CONST  ETUCONFIG =   0x205C;   {ETU configuration register }
.CONST  ETUDIVIDE =   0x205D;   {ETU clock divide register }
.CONST  ETUSTAT   =   0x205E;   {ETU status register }
.CONST  ETUCTRL   =   0x205F;   {ETU control register }
.CONST  PWMSYNCWT =   0x2060;   {PWMSYNC width register}
.CONST  PWMSWT    =   0x2061;   {PWM software trip register}
.CONST  EETN      =   0x2070;   {EET pulse decimator register }
.CONST  EETDIV    =   0x2071;   {EET timer decimator register }
.CONST  EETDELTAT =   0x2072;   {EET delta timer register     }
.CONST  EETT      =   0x2073;   {EET timer period register    }
.CONST  EETSTAT   =   0x2074;   {EET overflow status register }

{ memory mapped core registers of the ADMC401 }

.CONST  SYSCNTL                 =   0x3fff;
.CONST  MEMWAIT                     =   0x3ffe;
.CONST  TPERIOD                 =   0x3ffd;
.CONST  TCOUNT                  =   0x3ffc;
.CONST  TSCALE                  =   0x3ffb;
.CONST  Sport0_Rx_Words1        =   0x3ffa;
.CONST  Sport0_Rx_Words0        =   0x3ff9;
.CONST  Sport0_Tx_Words1=   0x3ff8;
.CONST  Sport0_Tx_Words0=   0x3ff7;
.CONST  Sport0_Ctrl_Reg   =   0x3ff6;
.CONST  Sport0_Sclkdiv    =   0x3ff5;
.CONST  Sport0_Rfsdiv     =   0x3ff4;
.CONST  Sport0_Autobuf_Ctrl =   0x3ff3;
.CONST  Sport1_Ctrl_Reg   =   0x3ff2;
.CONST  Sport1_Sclkdiv    =   0x3ff1;
.CONST  Sport1_Rfsdiv     =   0x3ff0;
.CONST  Sport1_Autobuf_Ctrl       =   0x3fef;

{ interrupt vector table addresses for ADMC401 }

.CONST ADC_INT_ADDR       = 0x30+1;     {ADC INTERRUPT }
```

```
.CONST PWMSYNC_INT_ADDR    = 0x34+1;      {PWMSYNC interrupt   }
.CONST EIUTIMER_INT_ADDR   = 0x38+1;      {EIU timer interrupt }
.CONST PIO_INT_ADDR        = 0x3C+1;      {PIO4 - PIO11 interrupt }
.CONST EIUERROR_INT_ADDR   = 0x40+1;      {EIU error interrupt }
.CONST ETU_INT_ADDR        = 0x44+1;      {ETU interrupt }
.CONST PIO0_INT_ADDR       = 0x48+1;      {PIO0 interrupt }
.CONST PIO1_INT_ADDR       = 0x4C+1;      {PIO1 interrupt }
.CONST PIO2_INT_ADDR       = 0x50+1;      {PIO2 interrupt }
.CONST PIO3_INT_ADDR       = 0x54+1;      {PIO3 interrupt }
.CONST PWMTRIP_INT_ADDR    = 0x58+1;      {PWMTRIP interrupt}
.CONST  TX0_INT_ADDR       = 0x10;        {SPORT0 transmit interrupt}
.CONST  RX0_INT_ADDR       = 0x14;        {SPORT0 receive interrupt}
.CONST  SW1_INT_ADDR       = 0x18;        {software interrupt 1}
.CONST  SW0_INT_ADDR       = 0x1C;        {software interrupt 0}
.CONST  TX1_INT_ADDR       = 0x20;        {SPORT1 transmit interrupt}
.CONST  RX1_INT_ADDR       = 0x24;        {SPORT1 receive interrupt}
.CONST  TIMER_INT_ADDR     = 0x28;    {Timer interrupt}

{ ROM addresses }
.CONST PUT_VECTOR                = 0x0D8E;   {PUT_VECTOR routine in ROM}
.CONST HALT_FLAG                 = 0x3B68;   {used by exit library function}
.CONST IDE_SP                  = 0x0C9E;         {used by exit library function}

#endif
```

START pwm401.h HEADER FILE

```
{*************************************************************************
***************
*                                                                       *
* Library: Configuration of PWM block in single update mode             *
*                                                                       *
* File: pwm401.h                                                        *
*                                                                       *
* Description: pwm401 include file                                      *
* Purpose    : Declare library routines and macros for PWM block operation *
*                                                                       *
*************************************************************************
**************}

{*************************************************************************
***************
*                                                                       *
* Constants that need to be defined in main.h:                          *
*                                                                       *
* .CONST  Cry_clock       = xxxx;             Crystal clock frequency [kHz]     *
```

```
* .CONST  PWM_freq       = xxxx;          Desired PWM switching frequency [Hz]   *
* .CONST  PWM_deadtime    = xxxx;               Desired deadtime [nsec]           *
* .CONST  PWM_minpulse    = xxxx;               Desired minimal pulse time [nsec]
*
* .CONST  PWM_syncpulse   = xxxx;               Desired sync pulse time [nsec]
*
*************************************************************************
**************}

{*************************************************************************
***************
*                                                 *
* Other Libraries Required by this Module:                          *
*                                                 *
* None                                              *
*************************************************************************
**************}

#ifndef PWM_INCLUDED
#define PWM_INCLUDED

{*************************************************************************
***************
* Routines Defined in this Module                                   *
*************************************************************************
**************}
.EXTERNAL PWM_Init_;

{*************************************************************************
***************
* Global Variables Defined in this Module                           *
*************************************************************************
**************}

{ None }

{*************************************************************************
***************
*                                                 *
* Type: Macro                                           *
*                                                 *
* Call: PWM_Init(PWMSYNC_ISR, PWMTRIP_ISR);                         *
*                                                 *
* Initialises the PWM block of the ADMC401 with the parameters set in main.h        *
* All outputs are enabled, no crossover and no chopping. Also setup PWM interrupts.   *
*                                                 *
```

```
* Inputs  :      %0: Label of PWM_SYNC interrupt service routine                  *
*                %1: Label of PWM_TRIP interrupt service routine                 *
*                                                                                *
* Ouputs  :      None                                                            *
*                                                                                *
* Modified:      I4, AR, AX1, AY0, MR0, SR, PX                                   *
*                                                                                *
**********************************************************************
**************}

        .MACRO PWM_Init(%0, %1);
                call PWM_Init_;

                Set_InterruptVector(PWMSYNC_INT_ADDR, %0); { Vector for
PWM_SYNC int   }
                Set_InterruptVector(PWMTRIP_INT_ADDR, %1); { Vector for
PWM_SYNC int   }

            AY0 = 0x0402;     {Enable PWMSYNC,PWMTRIP             }
                AR = DM(PICMASK); {interrupts in PIC. Preserve        }
                AR = AR OR AY0;   {other bits of PICMASK by ORing     }
                DM(PICMASK) = AR; {PWM Interrupt is fully enabled here!!}

        .ENDMACRO;


{**********************************************************************
***************
*                                                                                *
* Type: Macro                                                                    *
*                                                                                *
* Call: PWM_update_dutycycles(ChannelA, ChannelB, ChannelC);                     *
*                                                                                *
* Updates the PWM channels with the normalised dutycycles                        *
*                                                                                *
* Inputs  :      %0: register containing desired dutycycle (0-1) for channel A   *
*                %1: register containing desired dutycycle (0-1) for channel B   *
*                %2: register containing desired dutycycle (0-1) for channel C   *
*                                                                                *
* Ouputs  :      None                                                            *
*                                                                                *
* Modified:      SR0, MY0, MR                                                    *
*                                                                                *
**********************************************************************
**************}
        .MACRO PWM_update_dutycycles(%0, %1, %2);
```

```
                sr0= DM(PWMTM);
                my0 = %0; mr= sr0 * my0 (SS); dm(PWMCHA) = mr1;
                my0 = %1; mr= sr0 * my0 (SS); dm(PWMCHB) = mr1;
                my0 = %2; mr= sr0 * my0 (SS); dm(PWMCHC) = mr1;
        .ENDMACRO;

{*********************************************************************
***************
*                                                       *
* Type: Macro                                                   *
*                                                       *
* Call: PWM_update_demanded_Voltage(ChannelA, ChannelB, ChannelC);
*
*                                                       *
* Updates the PWM channels with the normalised average Voltage                  *
*                                                       *
* Inputs  :     %0: register containing desired Voltage (-1 to 1) for channel A     *
*               %1: register containing desired Voltage (-1 to 1) for channel B     *
*               %2: register containing desired Voltage (-1 to 1) for channel C     *
*                                                       *
* Ouputs  :     none                                            *
*                                                       *
* Modified:     sr, my0, mr                                             *
*                                                       *
*********************************************************************
***************}
        .MACRO PWM_update_demanded_Voltage(%0, %1, %2);
                sr0= DM(PWMTM);
                sr = LSHIFT sr0 by -1 (LO);
                mr =0; mr1= sr0; my0 = %0; mr= mr + sr0 * my0 (SS); dm(PWMCHA) =
mr1;
                mr =0; mr1= sr0; my0 = %1; mr= mr + sr0 * my0 (SS); dm(PWMCHB) =
mr1;
                mr =0; mr1= sr0; my0 = %2; mr= mr + sr0 * my0 (SS); dm(PWMCHC) =
mr1;
        .ENDMACRO;

#endif
```

APPENDIX B – Simplorer Schematic

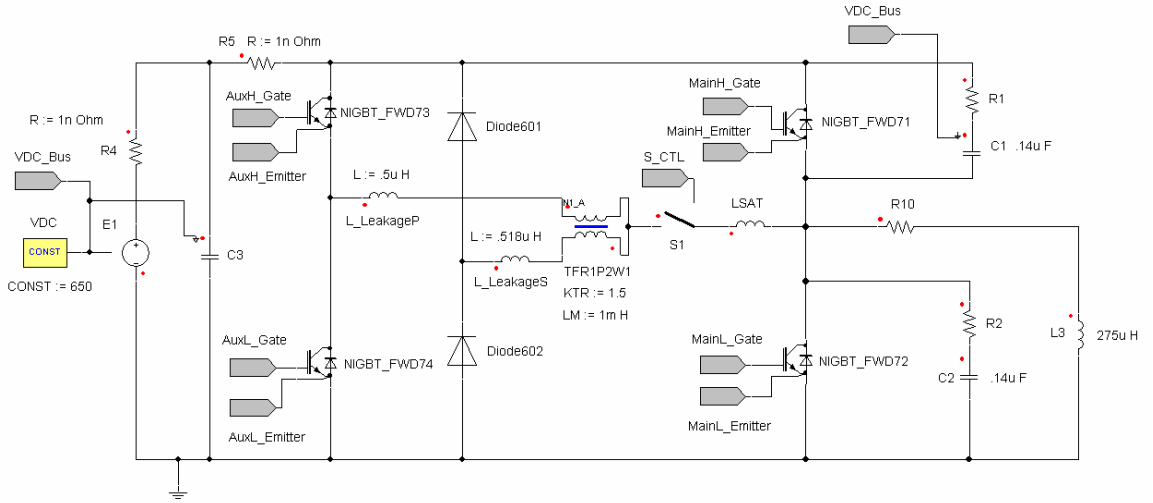

Figure 42 Main Schematic

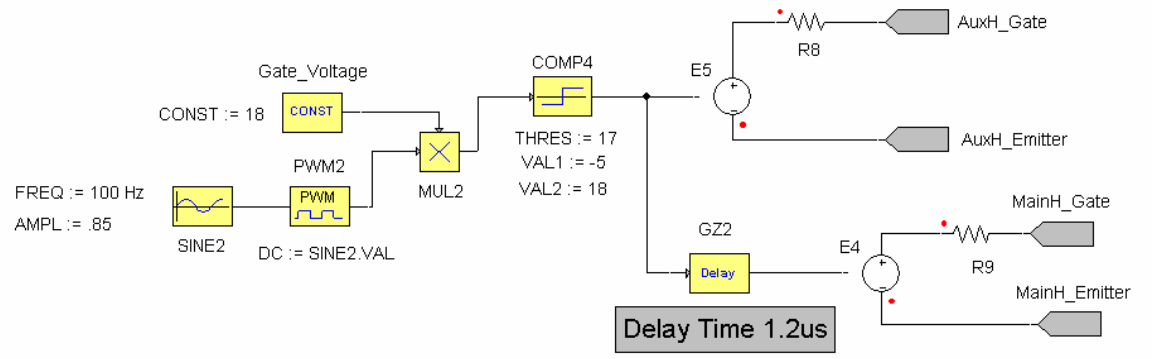

Figure 43 Gate Timing Schematic ("simple" fixed timing delay)

APPENDIX C – References

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