High Frequency, High Current Integrated Magnetics Design and Analysis

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(Abstract)

The use of computers in the modern world has become prevalent in all aspects of life. The size of these machines has decreased dramatically while the capability has increased exponentially. A special DC-DC converter called a VRM (Voltage Regulator Module) is used to power these machines. The VRM faces the task of supplying high current and high di/dt to the microprocessor while maintaining a tight load regulation. As computers have advanced, so have the VRM's used to power them. Increasing the current and di/dt of the VRM to keep up with the increasing demands of the microprocessor does not come without a cost. To provide the increased di/dt, the VRM must use a higher number of capacitors to supply the transient energy. This is an undesirable solution because of the increased cost and real estate demands this would lead to in the future. Another solution to this problem is to increase the switching frequency and control bandwidth of the VRM. As the switching frequency increases the VRM is faced with efficiency and thermal problems. The current buck topologies suffer large drops in efficiency as the frequency increases from high switching losses.

Resonant or soft switching topologies can provide a relief from the high switching loss for high frequency power conversion. One disadvantage of the resonant schemes is the increased conduction losses produced by the circulating energy required to produce soft switching. As the frequency rises, the additional conduction loss in the resonant schemes can be smaller than the switching loss encountered in the hard switched buck. The topology studied in this work is the 12V non-isolated ZVS self-driven presented in [1]. This scheme offered an increased efficiency over the state of the art industry design and also increased the switching frequency for capacitor reduction. The goal of this

research was to study this topology and improve the magnetic design to decrease the cost while maintaining the superior performance.

The magnetics used in resonant converters are very important to the success of the design. Often, the leakage inductance of the magnetics is used to control the ZVS or ZCS switching operation. This work presents a new improved magnetic solution for use in the 12V non-isolated ZVS self-driven scheme which increases circuit operation, flexibility, and production feasibility. The improved magnetic structure is simulated using 3D FEA verification and verified in hardware design.

To my parents,

George and Janet Reusch

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My colleagues in the VRM group have been instrumental in this research as well. The VRM team is a very motivated group in which all members contribute to help each others research progress. Without the support and knowledge of the VRM group this work would not have been possible. The leader of the VRM group is Dr. Ming Xu, and the members of the group are: Dr. Y. Qiu, J.L. Sun, J.J. Sun, C. Wang, Y. Dong, J. Li, D. Reusch, D. Sterk, C. Person, A. Ball, B. Lu, M. Lim, K. Lee, Y. Meng, Y. Yang, Y. Ying, and Y. Sun. I would also like to thank my first mentor Dr. Jingahi Zhou, he mentored me during my first year in the VRM group and without his teaching and advice I would have never been able to improve upon his great work.

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Chapter 1

Introduction

1.1 Background and Research Objectives

As technology advances, so does the demand on the power supplies. The computer has seen exponential growth in performance and the power requirements have increased in a linear manner. Shown below is a plot of power requirements of Intel processors from [1.1]. The power demands of the CPU have grown for the last 6 years and these demands are expected to continue to increase in the future.

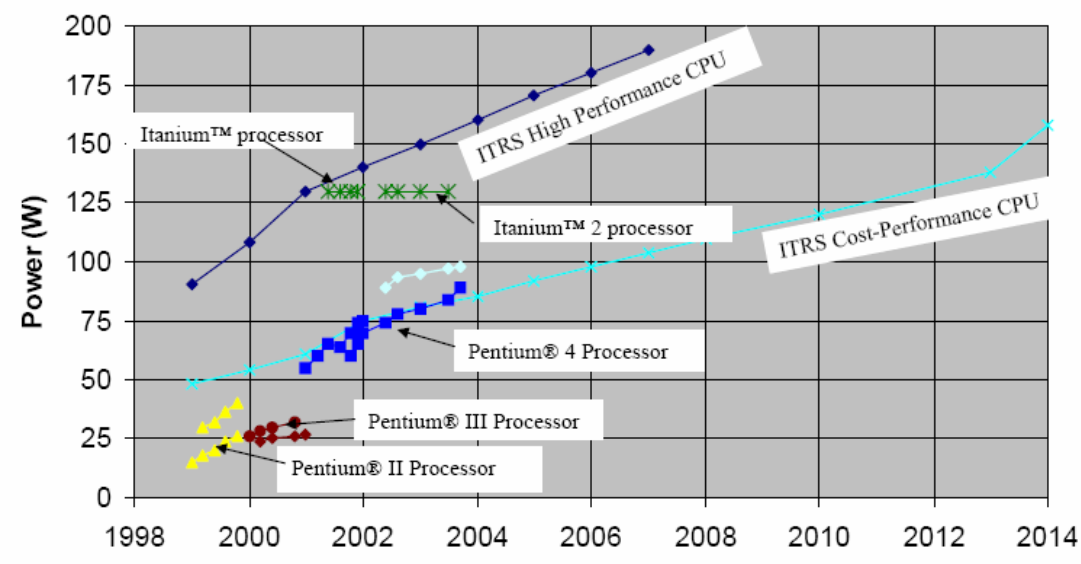

Fig 1.1 Power consumption history of various Intel CPU's

Improved versions of traditional multiphase buck converters have improved the efficiency of the power supplies, also known as voltage regulator modules (VRM). One issue with the traditional buck converter has to do with real estate in the CPU. To maintain an operable efficiency, multiple phases must be used in parallel resulting in a larger VRM. According to [1.2] the size of the VRM can not only not increase, but it

must get smaller. The plot below shows Intel's desire for higher power density and smaller size for the future VRM's.

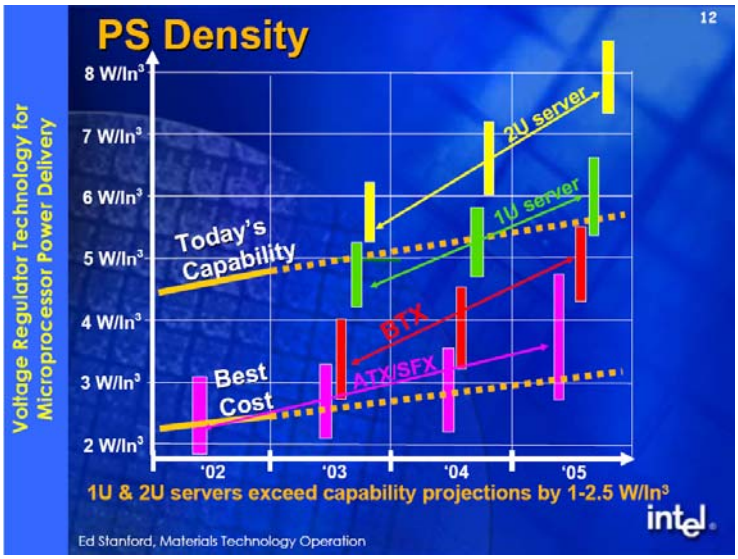

Fig 1.2 Power density demands of future Intel products

The current, voltage, and slew rate demands have changed for future microprocessors. Shown below are the demands as given by [1.3]. The increased current and slew rate present many issues for the current buck converters. Increased current means increased losses in a hard switched converter and increased slew rate means increased number of output capacitors required to maintain a high slew rate.

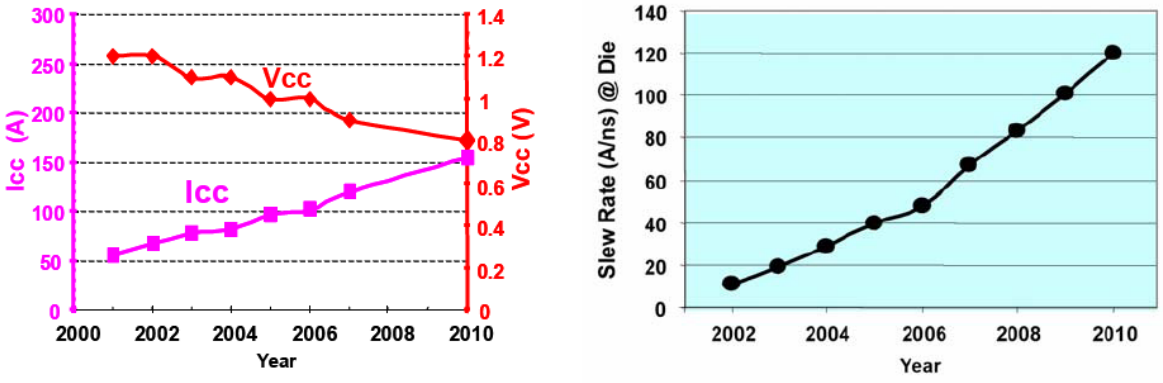

Fig 1.3 Future current, voltage, and slew rate requirements according to Intel

In [1.4], it is proposed that increasing the switching frequency will reduce the number of capacitors to needed to increase the slew rate. An issue with increasing the switching frequency is increased losses. The future of the VRM must be at higher frequency solutions to help reduce the output capacitance required, the size of magnetic components, and to increase power density but must also maintain high efficiency.

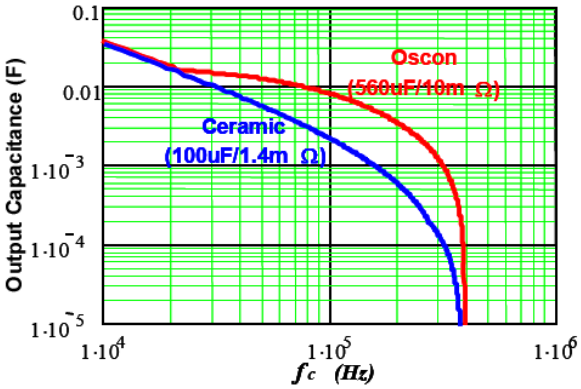

Fig 1.4 Capacitor reduction offered by increased bandwidth

Soft switching topologies like the one proposed in [1.5] offer improved efficiency at high switching frequencies as a result of the reduced loss from zero voltage switching. One drawback of this soft switching topology is the complexity of the magnetics design. The buck converters used in current VRM designs have single chip output inductors, the topology proposed by Dr. Zhou uses two transformers which utilize the magnetizing inductance for the output filter inductor and use the transformer leakage inductance to achieve zero voltage switching.

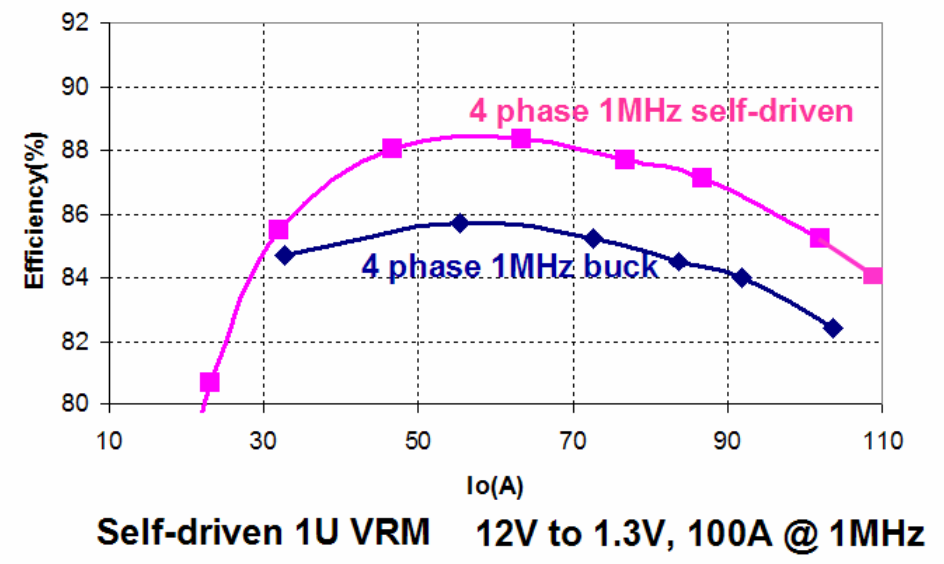

Fig 1.5 Efficiency comparison between 12V non-isolated self driven topology and conventional buck converter

The purpose of this work is to study this complex magnetic structure and explain the leakage inductance issues faced in the 12V non-isolated ZVS self-driven scheme clearly. Another purpose of this work is to propose an improved magnetic design to further improve upon the topology proposed by Dr. Zhou. This work is also applicable to any magnetic inductor or transformer to help estimate the leakage inductance and offers methods to control the leakage inductance.

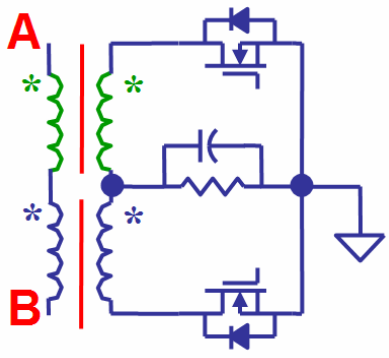

Fig 1.6 Integrated magnetics design proposed by Dr. Zhou

1.2 Thesis Outline

This thesis contains four chapters.

Chapter one gives an introduction to the trends of VRM's in the past and projected for the future. Also contained in chapter one is the problems facing the current VRM designs. The benefits and weaknesses of the 12V non-isolated ZVS self-driven scheme proposed by Dr. Zhou are discussed.

Chapter two introduces the 12V non-isolated ZVS self-driven scheme and discusses its modes of operation. Then chapter two discusses the effect of the leakage inductance of the transformer on circuit performance. The leakage inductance affects the duty cycle loss, body diode conduction loss, and the ZVS conditions of the converter. The tradeoffs between low and high leakage inductance are discussed.

Chapter three gets into the issue of leakage inductance. The method used to derive the leakage inductance is explained. The two magnetic designs produced by Dr. Zhou are studied and the losses related to each are given. The leakage inductance of the integrated magnetic structure is then studied and a method to reduce the leakage inductance is studied. Next, the leakage inductance improvements are utilized in a new design and tested. Lastly, the winding losses of all the magnetic designs are determined.

Chapter four summarizes the future work related to this topic. It discusses the future design options for a surface mounted magnetic structure. A coupled solution is studied and the benefits of coupling are discussed. Finally, an improved magnetic design is discussed for the embedded magnetics version.

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Chapter 2

12V Non-Isolated Zero Voltage Switched Complimentary-Controlled Full Bridge with Self-Driven Synchronous Rectification for High Frequency, High Current VRM Applications

The topology used in this work is 12V Non-Isolated Zero Voltage Switched Complimentary-Controlled Full Bridge with Self-Driven Synchronous Rectification. This topology was presented by Dr. Jinghai Zhou in [2.1]. The topology proposed by Dr. Zhou is a "buck-derived soft switching topology with duty cycle extension and SR device self-driven capabilities". Shown below is a circuit diagram of the 12V non-isolated zero voltage switched complimentary-controlled full bridge with self-driven synchronous rectification from [2.2].

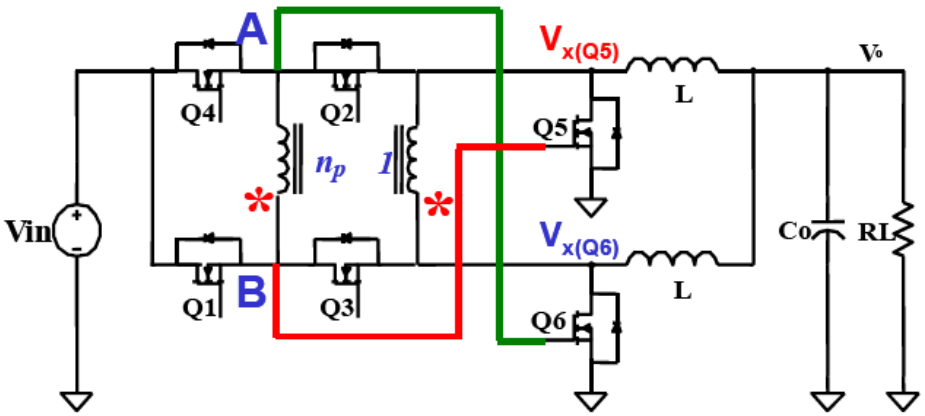

Fig 2.1 Schematic of 12V non-isolated zero voltage switched complimentary-controlled full bridge with self-driven synchronous rectification

This topology uses complementary controlled bridge (CCB) self driven design to allow for soft switching. The overall benefit from this topology is its ability to allow for

reduction of switching losses allowing for higher switching frequencies to be used. This will reduce the size of the converter and reduce the number of output capacitors needed.

2.1 Principles of Operation

The detailed circuit operation of this design is thoroughly discussed in [2.2]. For the purposes of this work, a small overview from [2.2] of circuit operation is given with expanded analysis given to the areas related to the effect of leakage inductance on the circuit performance. Shown below is the control strategy of the 12V non-isolated ZVS self-driven scheme.

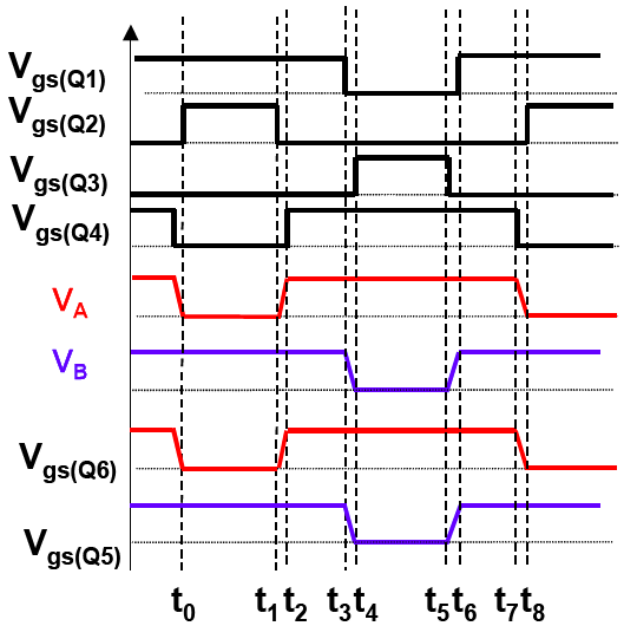

Fig 2.2 Voltage and timing diagram for full bridge and SR switches

Mode 1: to-t1: Switches Q1 and Q2 are on during this period. This means that the gate of Q5 is connected to the input voltage and is on during this period. With Q2 and Q5 on, the gate signal of Q6 is connected to ground and off during this period. This period is an energy transfer period; the energy is transferred to the output from the transformer.

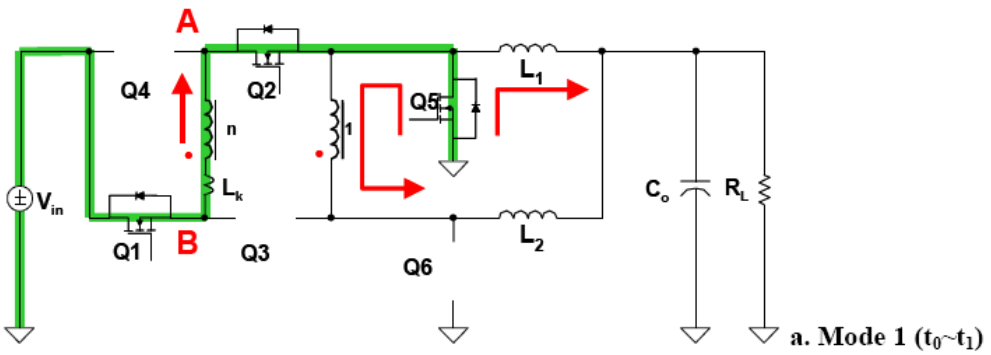

Fig 2.3 Circuit operation in mode 1

Mode 2: t1-t2: At t1, Q2 is driven off by the external driver. The output current is reflected to the primary side to charge the output capacitor of Q2 and discharge the capacitor of Q4. The input capacitor of Q6 is also charged during this period because of its connection to point A.

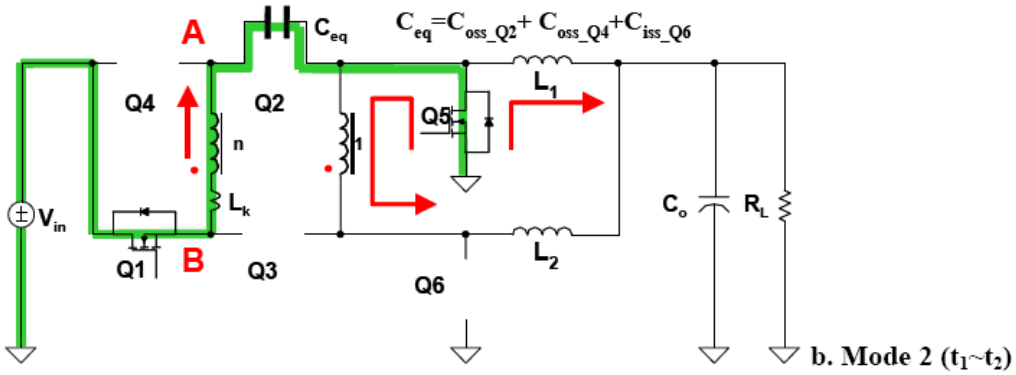

Fig 2.4 Circuit operation in mode 2

A dead time is required to allow for the voltage of point A to reach the input voltage to allow for ZVS switching of Q4 in the next period. The required dead time is given below

$$t_{d1} = \frac{2 \cdot n_p \cdot C_{eq} \cdot V_{in}}{I_{o\min}} \qquad (2.1)$$

This dead time will insure ZVS of Q4 which saves switching loss and helps this topology push the switching frequency. The number of turns in the transformer is represented by n_p, the equivalent capacitive network C_{eq} is equal to $C_{eq} = C_{oss\_Q2} + C_{oss\_Q4} + C_{iss\_Q6}$, V_{in} is equal to the input voltage, and $I_{o\min}$ is equal to the minimum load current required to achieve ZVS in this scheme.

Mode 3: t2-t3: During this mode of operation Q4 is turned on with zero voltage and the energy stored in the leakage inductance of the transformer freewheels through Q1 and Q4. Q5 and Q6 are also on during this period and a freewheeling current path is seen in the current doubler loop.

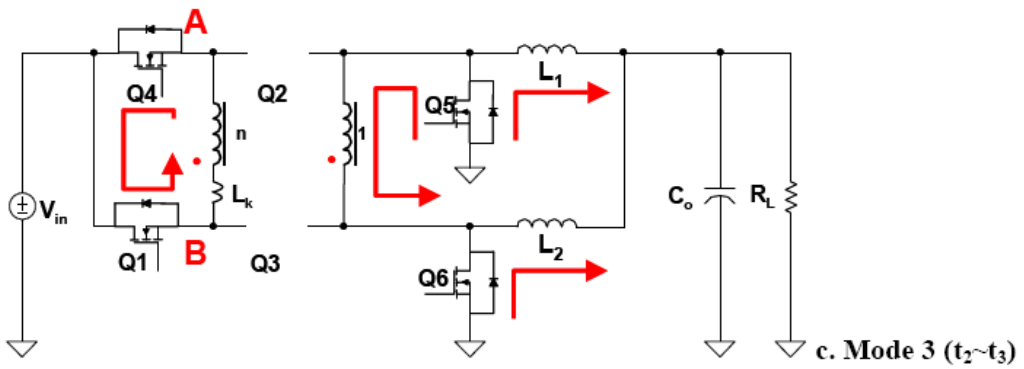

Fig 2.5 Circuit operation in mode 3

Mode 4: t3-t4: Q1 is driven off at t3. The reflected loop inductance of the current doubler and leakage inductance resonate with the output capacitors of Q1, Q3 and the input capacitor of Q5. To achieve ZVS for Q3, two criteria must be met. The leakage inductance must produce enough energy to charge and discharge the equivalent capacitive network created by Q1, Q3, and Q5. The minimum output current to achieve ZVS is derived by using

$$E = \frac{1}{2} C_{eq} \cdot V_{in}^{\ 2} \le \frac{1}{2} L_k \cdot I_p^{\ 2} \qquad (2.2)$$

where $C_{eq} = C_{oss\_FB} + C_{oss\_FB} + C_{iss\_SR}$, this simplifies to

$$\frac{1}{2} C_{eq} \cdot V_{in}^{\ 2} \le \frac{1}{2} L_k \cdot \left(\frac{I_o}{n} \right)^2 \tag{2.3}$$

which gives the minimum required load current to achieve ZVS

$$I_{o\_\min} \ge n \cdot \sqrt{\frac{C_{eq} \cdot V_{in}^{\ 2}}{L_k}} \tag{2.4}$$

The second requirement to achieve ZVS is to use a dead time between Q1 and Q3 of one fourth the resonant period to allow for Q3 to be turned on while achieving ZVS. This dead time is given as

$$t_{d2} = \frac{\pi \sqrt{L_k \cdot C_{eq}}}{2} \tag{2.5}$$

where L_k is the leakage inductance of the transformer and the current doubler loop.

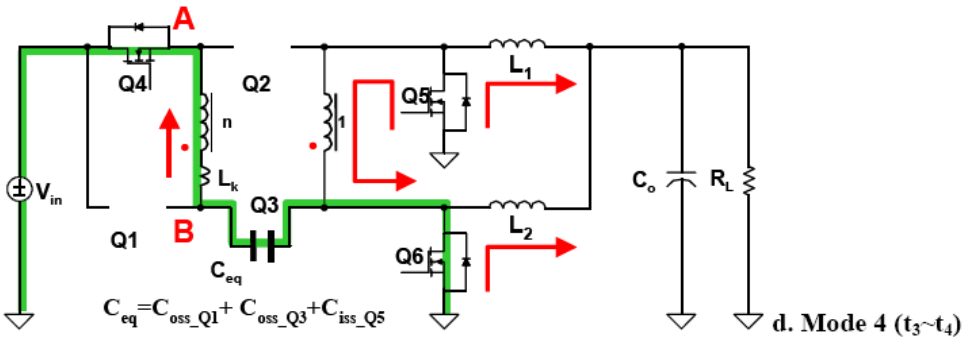

Fig 2.6 Circuit operation in mode 4

Modes 5-8: t4-t8: The second half period occurs during this period and follows the same operation but with reversed polarity.

2.2 Effects of Leakage Inductance on Circuit Performance

The leakage inductance of the transformer and current doubler affect the performance of the 12V Non-Isolated Zero Voltage Switched Complimentary-Controlled Full Bridge with Self-Driven Synchronous Rectification significantly. The leakage inductance results in duty cycle loss, affects ZVS operation points, and affects the body diode conduction loss of the current doubler switches. In this section, the effects of the leakage inductance will be studied the benefits of reduced leakage will be explored.

2.3 Duty Cycle Loss

The first affect of leakage inductance is duty cycle loss. Shown below is the schematic and waveforms of the transformer windings and voltages in the 12V Non-Isolated Zero Voltage Switched Complimentary-Controlled Full Bridge with Self-Driven Synchronous Rectification topology.

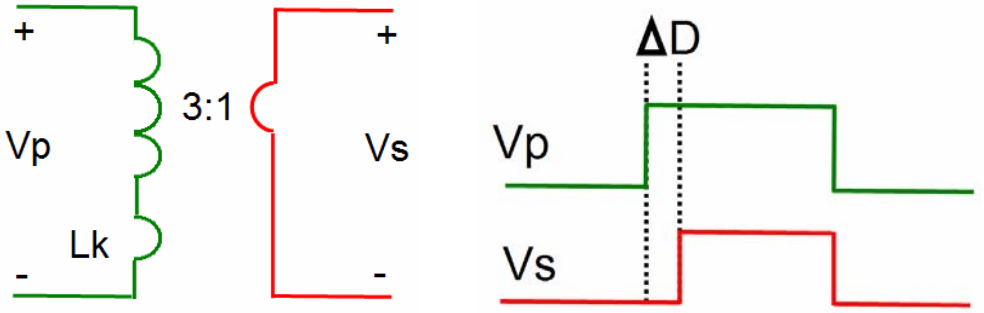

Fig 2.7 Voltage waveforms of primary and secondary as resulting duty cycle loss

The secondary voltage of the transformer loses duty cycle as a result of the leakage inductance of the transformer. The time it takes the primary current to switch polarities is

responsible for this duty cycle loss. Looking at the primary current waveform during the duty cycle loss period a formula for duty cycle loss can be obtained.

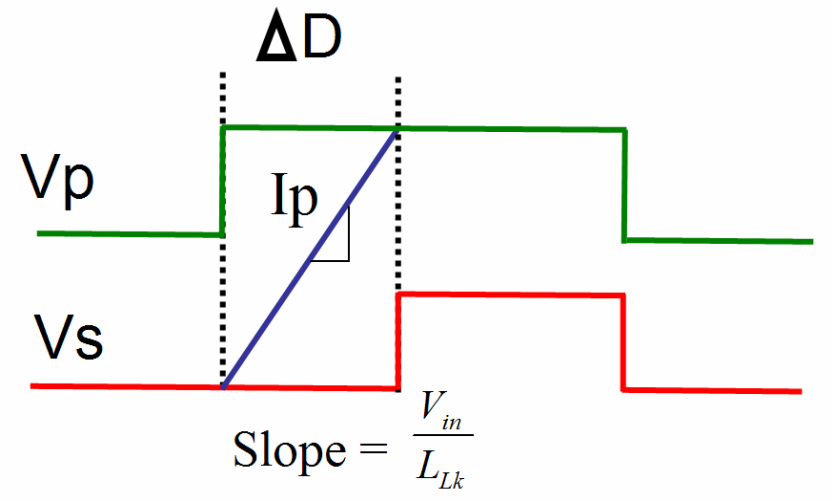

Fig 2.8 Voltage waveforms and effect of primary current on duty cycle loss

The duty cycle loss for this scheme can be approximated using the formula from [2.3]

$$\Delta D = \frac{2 \cdot L_{Lk} \cdot f_s \cdot I_o}{n_p \cdot V_{in}} \tag{2.6}$$

where f represents the switching frequency and I_o represents the output current.

As the switching frequency and load current are increased the duty cycle loss also increases. To minimize the duty cycle loss, the leakage inductance should be improved. This will allow for a larger range of operation. Shown below are plots showing the duty cycle loss related to various load currents and switching frequencies. Another factor in the loss of duty cycle is the winding resistance of the transformer and loop inductance. The transformer and loop resistance drop a small portion of resistance, but for this case only the duty cycle loss resulting from leakage inductance is studied.

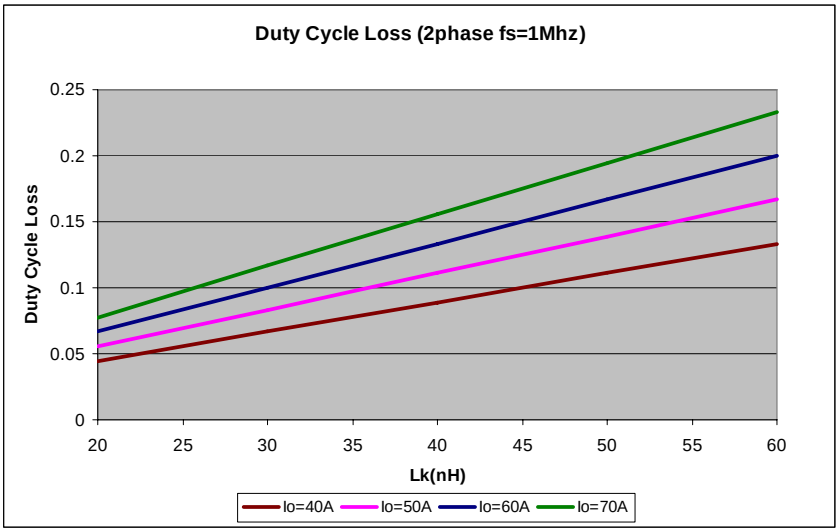

Fig 2.9 Duty cycle loss resulting from various leakage inductances and output loads

The duty cycle loss plot above shows how as the load current increases, so does the duty cycle loss. As was discussed in chapter 1, it is expected that the current demands of the future microprocessors will increase. This means that something will have to be done to reduce the duty cycle loss for this topology; one means of doing this is by reducing the leakage. The plot below tells a similar story, if the switching frequency of this topology is to be increased in the future, the duty cycle loss must be decreased, lower leakage again is a logical solution.

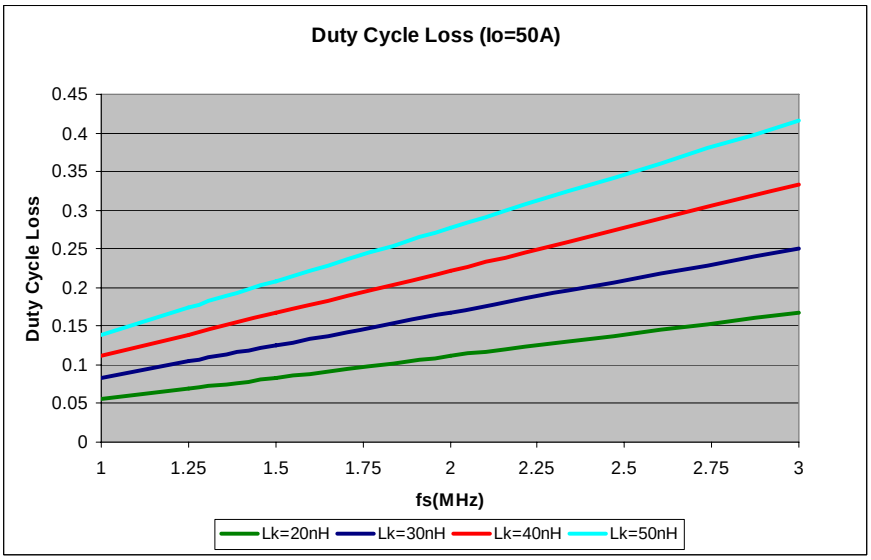

Fig 2.10 Duty cycle loss from various leakage inductances and switching frequencies

This section discussed the duty cycle loss related to leakage inductance for the chosen topology; there are alternate solutions to reduce the duty cycle loss other than reducing the leakage. The next section will explain why reduced leakage would be a beneficial solution not only for duty cycle loss but for body diode conduction loss. By reducing the leakage inductance, the duty cycle loss problem and body diode conduction loss problems can be solved.

2.4 Body Diode Conduction Loss

A major source of loss in the 12V non-isolated zero voltage switched complimentary-controlled full bridge with self-driven synchronous rectification is related to the body diode conduction losses in the current doubler switches. The body diode conduction period and loss was explained in [2.4] and [2.2]. The switching diagram below from [2.1] shows the body diode conduction period. When Q1 is driven to be off and the equivalent capacitive network resonates with the leakage inductance until the voltage reaches zero. Q5 continues to conduct current until the transformer completely switches polarity, during this period, the body diode of Q5 conducts current. The same process occurs for Q6 in the opposite interval.

The body diode conduction loss is given in [2.1] as:

$$P_D = 0.5 \cdot I_D \cdot \Delta t \cdot V_f \cdot f_s \tag{2.7}$$

where I_D is the diode current, Δt is the diode conduction period, V_f is the body diode forward drop voltage which is assumed to be 0.7, and f_s is the switching frequency. Also given in [2.1][2.4] is the diode current and diode conduction period:

$$I_D = \frac{I_o}{2} \cdot \left(1 + \sqrt{1 - \left(\frac{2 \cdot n_p \cdot V_{in}}{I_o \cdot Z_K} \right)^2} \right) \tag{2.8}$$

$$\Delta t = \frac{L_K I_o}{2 \cdot n_p \cdot V_{in}} \cdot \left(1 + \sqrt{1 - \left(\frac{2 \cdot n_p \cdot V_{in}}{I_o \cdot Z_K} \right)^2} \right) \tag{2.9}$$

$$Z_K = \sqrt{\frac{L_k}{C_{eff}}} \tag{2.10}$$

where Z_K is the characteristic impedance of the LC network created by the leakage inductance and mosfet capacitors.

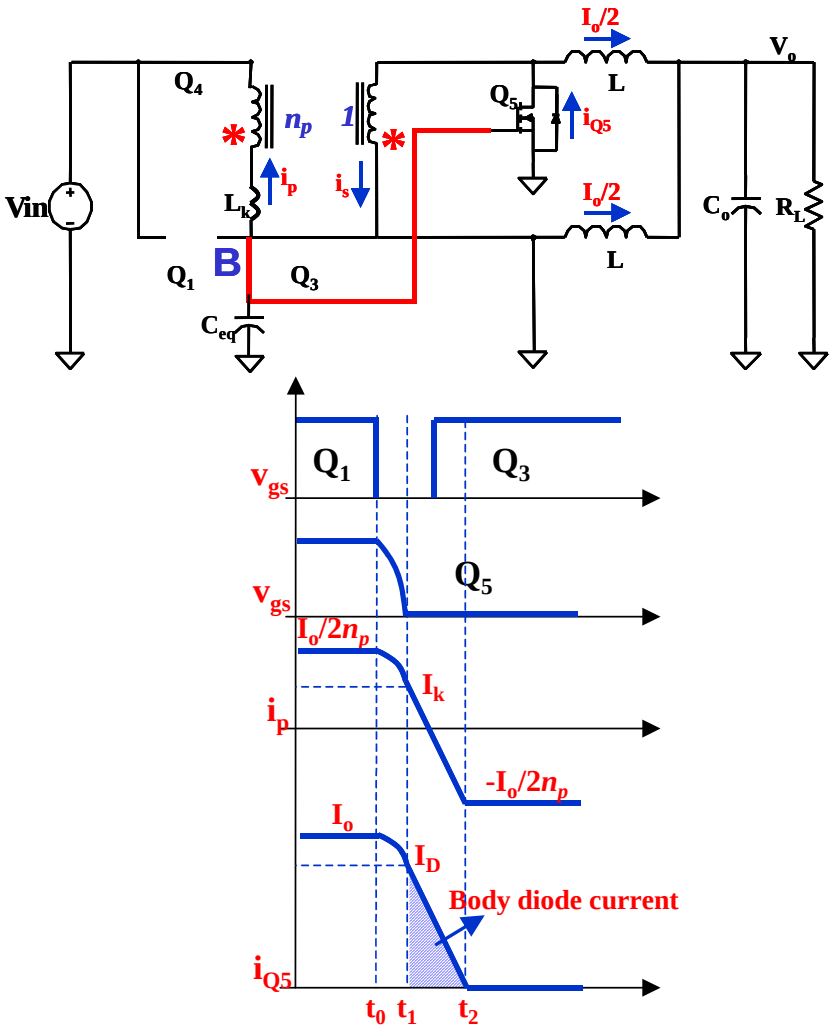

Fig 2.11 Mode of operation in which body diode conduction occurs and the related voltage and current waveforms during this period

Holding the devices, input voltage, and turns constant the body diode conduction is dependant upon the leakage inductance and output current. Since the load current demands are decided by the CPU, the one independent variable to improve performance becomes leakage inductance. In the previous section, lower leakage reduced duty cycle loss which was a desirable case. In this section it can be seen that reducing the leakage also reduces the body diode conduction loss, which improves overall efficiency.

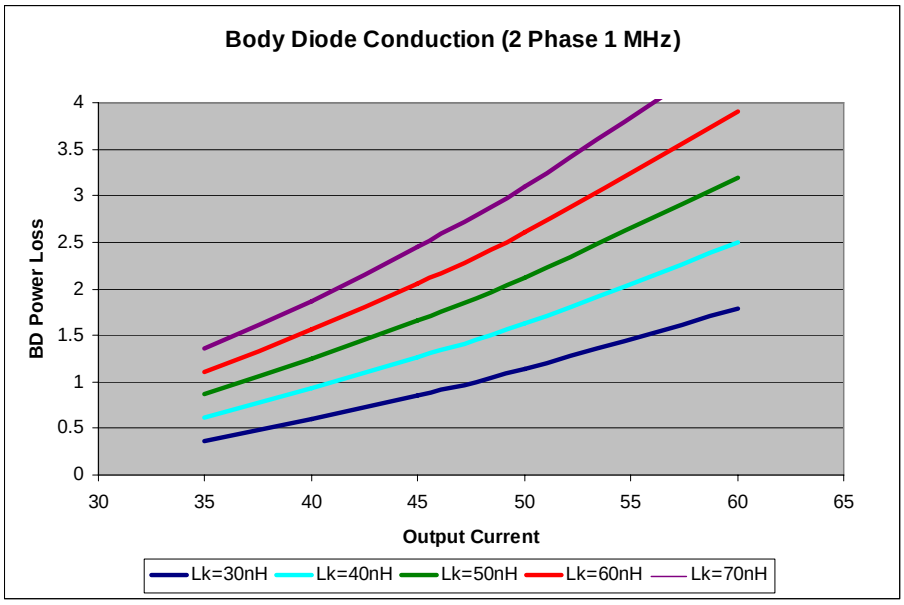

Fig 2.12 Body diode conduction loss for various leakage inductances and output loads

Just as was the case with duty cycle loss, at higher load currents, lower leakage is required to keep the duty cycle from saturating and reducing body diode conduction losses. This shows that without a low leakage inductance the benefits of this topology are negated. Low leakage is beneficial, but having some leakage is necessary to achieve ZVS. This will be discussed in the following section.

2.5 Affect of Leakage Inductance on ZVS

The previous two sections discussed the benefits of lower leakage inductance in the 12V non-isolated zero voltage switched complimentary-controlled full bridge with

self-driven synchronous rectification scheme. But, there is a disadvantage of having lower leakage in the design. The disadvantage comes in the form of reduced ZVS operation. The minimum load current to achieve ZVS is:

$$E = C_{eq} \cdot V_{in}^{\ 2} \le \frac{1}{2} L_k \cdot I_p^{\ 2} \tag{2.11}$$

where $C_{eq} = C_{oss\_FB} + C_{oss\_FB} + C_{iss\_SR}$, this simplifies to

$$C_{eq} \cdot V_{in}^{\ 2} \le \frac{1}{2} L_k \cdot \left(\frac{I_o}{n} \right)^2 \tag{2.12}$$

which gives the minimum required load current to achieve ZVS

$$I_{o\_\min} \ge n \cdot \sqrt{\frac{2 \cdot C_{eq} \cdot V_{in}^{\ 2}}{L_k}} \tag{2.13}$$

With the input voltage set by the specifications of the computer manufacturer and the turns ratio chosen to optimize efficiency the only two independent variables are the equivalent capacitance and the leakage inductance. Shown below is a plot comparing minimum output current required to achieve ZVS and leakage inductance. The plot shows that as the leakage inductance decreases, a higher load current is required to achieve ZVS. The result of decreasing the leakage inductance is increased high current efficiency and decreased low current efficiency. The following chapter will show examples of the trade off between the low leakage and high leakage cases. With the emphasis in the industry to achieve high full load efficiency a low leakage is desirable. As devices improve the input and output capacitances decrease the light load efficiency will become less of an issue. Another future solution to improve light load efficiency will be by using a single full bridge design.

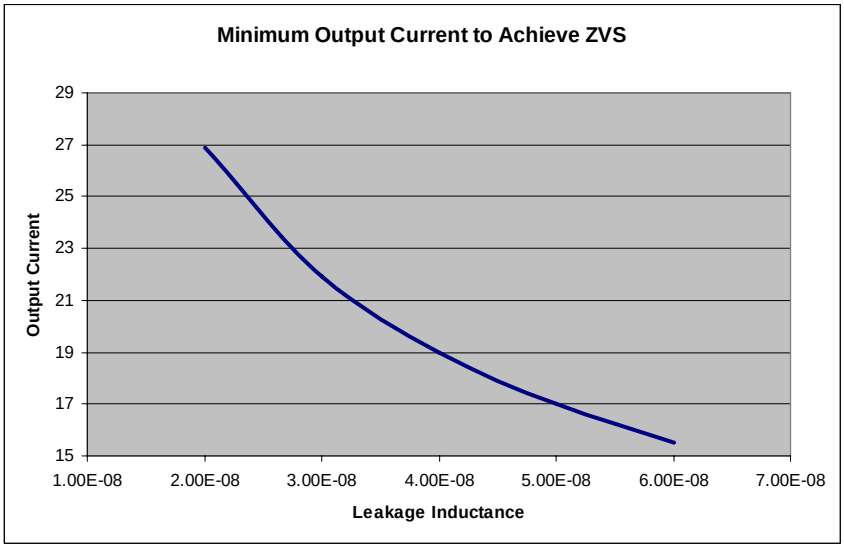

Fig 2.13 Minimum output current required to achieve ZVS on full bridge switches

Looking at the ZVS conditions with a smaller equivalent capacitance shows that the ZVS conditions can and will be reduced in the future with better devices. The current design uses two synchronous rectifiers in parallel for each of the current doubler switches to reduce conduction losses. Having better devices will allow for the use of a single synchronous rectifier which will result in achieving ZVS at smaller loads.

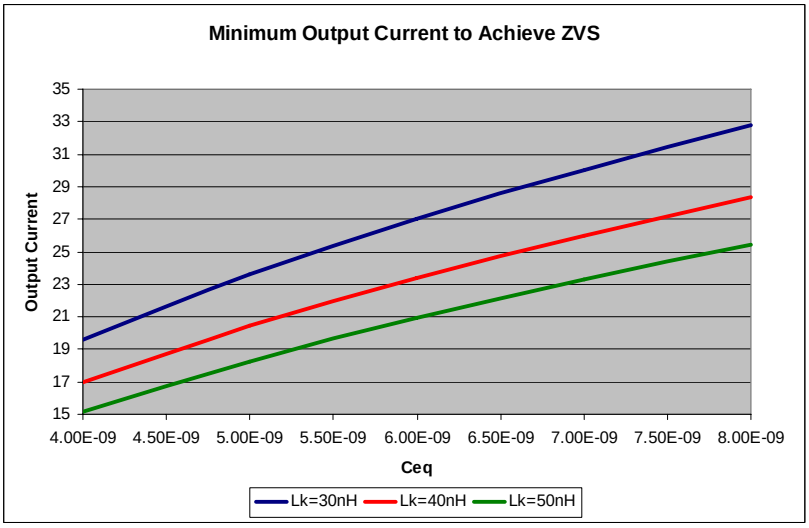

Fig 2.14 Minimum output current required to achieve ZVS on full bridge switches with various leakage inductances and equivalent capacitances

The effect of the lower capacitances will also affect the body diode conduction losses, shown below is a plot describing body diode loss with varied leakage inductance and capacitances. This plot shows that the effect of the equivalent capacitance is relatively small on the body diode conduction loss.

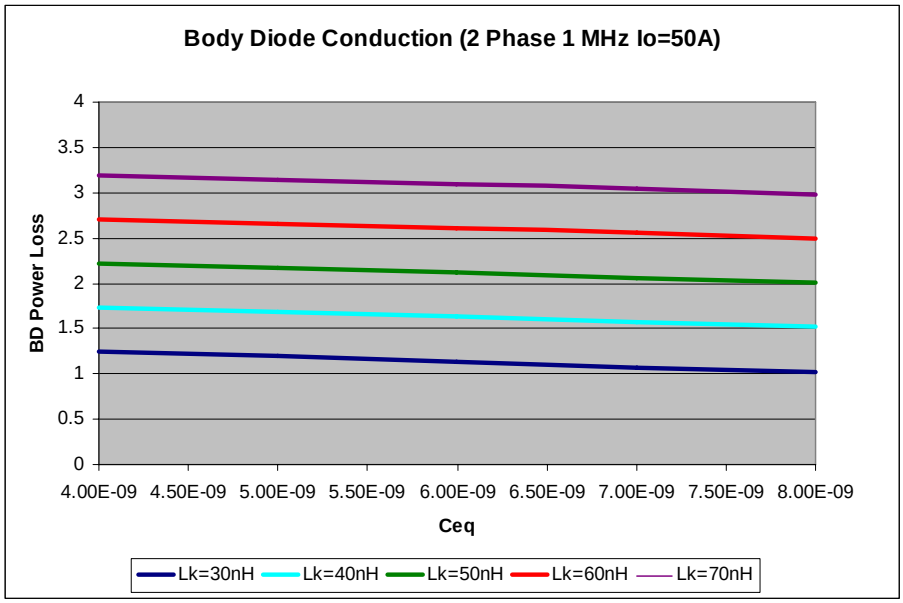

Fig 2.15 Body diode conduction for various leakage inductances and equivalent capacitances

This section shows that as devices improve, the benefit of this topology will also improve. The switching losses will remain small and the range of ZVS operation will be improved significantly.

2.6 Summary

This chapter gave an overview of the circuit operation and emphasized the circuit operation related to the leakage inductance. The leakage inductance had an affect on ZVS conditions, duty cycle loss, and body diode conduction loss. A smaller leakage inductance reduced duty cycle loss and body diode conduction loss but made it harder to achieve ZVS operation. As switches in the industry improve, so will the parasitic

capacitance in the devices, this will allow for the 12V non-isolated self driven zero voltage switched complimentary-controlled full bridge to achieve ZVS at lighter loads without degrading the full load performance significantly.

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Chapter 3

Improvements of 12V Non-Isolated Zero Voltage Switched Self-Driven Scheme VRM with Low Leakage Magnetics Design

The previous chapter discussed the importance of the magnetics design on the converter operation. A large leakage inductance provides more energy which allows the converter to achieve ZVS at a smaller load current but results in a much higher body diode conduction loss and duty cycle loss at higher loads. For our application we are concerned with having a leakage value that is too large. Larger leakage inductance results in increased losses and decreases the benefit of the 12V non-isolated ZVS self-driven scheme. This chapter explores the leakage inductance of the 12V non-isolated ZVS self-driven scheme and offers a new integrated magnetics design that offer reduced leakage inductance.

3.1 Leakage Inductance and Winding Resistance Calculations

The leakage inductance and winding resistance of the magnetics in the non-isolated ZVS self-driven scheme is key to its improved performance. If the magnetics have an excessively high leakage and winding loss then the soft switching benefits of the design will be outweighed by the losses generated as a result of the magnetics.

To accurately measure the leakage inductance and winding resistance Maxwell 3D FEA simulation software is used. The FEA software package takes into account the eddy current effect, skin depth effect, cornering effect, and proximity effect encountered in high frequency low profile magnetics [3.1]. As described in [3.2], the eddy current solver uses an AC current input and computes the magnetic field in the system (and stores them in magnitude and phase vectors) by using the following equation

$$\nabla \times \left(\frac{1}{\sigma + j\omega\varepsilon} \nabla \times H \right) = j\omega\mu H \tag{3.1}$$

where σ represents conductivity , ω represents radian frequency, and H represents magnetic field intensity.

The energy stored in a magnetic field is given by [3.3]:

$$W_H = \frac{1}{2} \int_{Vol} B \bullet H dv = \frac{1}{2} L_k I^2 \tag{3.2}$$

This energy is equal to the energy stored in the leakage inductance produced by an external AC current source. Using the eddy current solver the energy is only considered from AC current source without a DC bias, therefore we find the value of the leakage inductance and AC winding resistance without any of the DC inductance or DC winding resistance. Solving the energy equation yields the value of the leakage inductance:

$$L_k = \frac{1}{I^2} \int_{Vol} B \bullet H dv \tag{3.3}$$

The final equation needed to begin FEA analysis is the AC resistance equation which is derived from the power dissipation perspective.

$$I = \int_S J \bullet dS \tag{3.4}$$

$$V = \int_L \frac{J}{\sigma} \bullet dL \tag{3.5}$$

$$P = I_{RMS} \cdot V_{RMS} = {I_{RMS}}^2 R_{AC} = \frac{1}{2} \cdot I_{Peak}^2 \cdot R_{AC} \tag{3.6}$$

which yields the value for AC resistance:

$$R_{AC} = \frac{1}{I^2} \iiint_V \frac{J \bullet J^*}{\sigma} dV \tag{3.7}$$

Having the tools in place to analyze leakage inductance and AC resistance allows for the magnetics in the original 12V non-isolated ZVS self-driven scheme shown in [3.4] to be studied and improved.

3.2 Discrete Magnetics Components

The original design of the 12V non-isolated ZVS self-driven scheme presented in [3.4] used a discrete transformer to step down the voltage and two discrete output inductors. The use of a transformer makes this design have one more magnetic component than a standard two phase buck converter. The transformer results in an additional circuit loss and decreases the advantage of this scheme. The transformer used in [3.5] was a TDK EIR14 (PQ50 material) core. Shown below is an FEA model of the discrete transformer used in the original 12V non-isolated ZVS self-driven circuit. This model is used to determine the leakage inductance and AC resistance of the original layout and find the loss breakdown as a result of the magnetics in the original design. The transformer used in the original design had a 3:1 turns ratio, used 12 layer PCB with two ounce copper in each of the inner layers, contained two sets of primary windings in parallel shown in blue, and contained six sets of secondary windings in parallel shown in red.

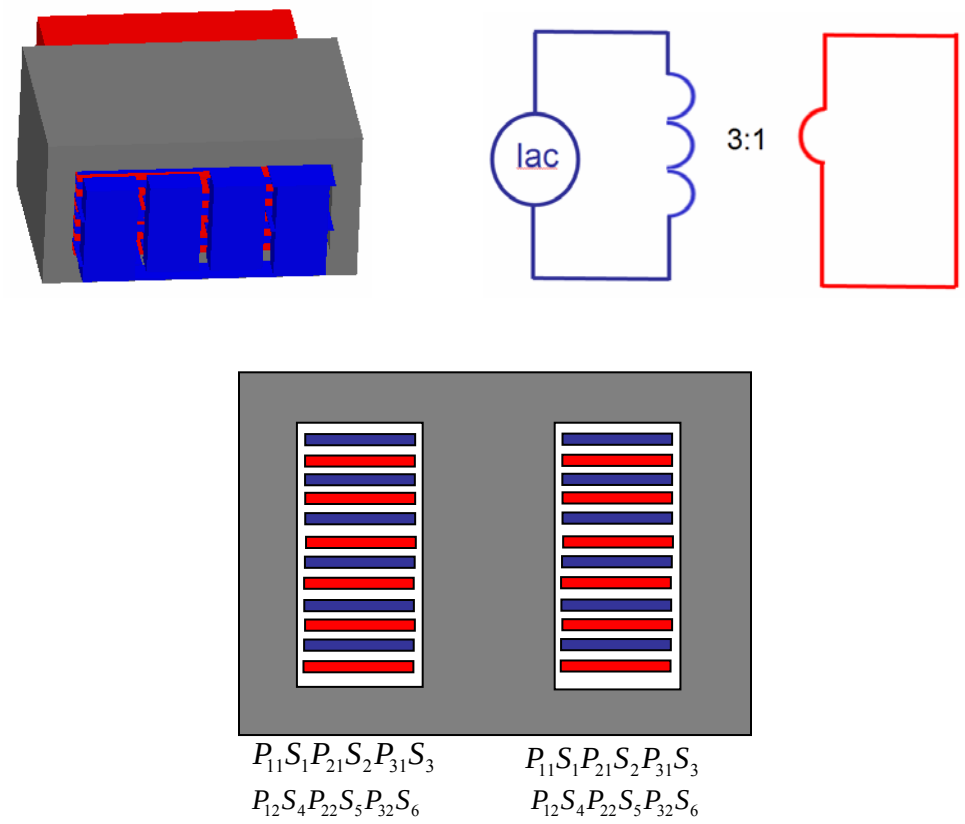


Fig 3.1 Discrete transformer modeled (a) Maxwell 3D Model (b) Electrical Model (c) Cross Section Core View

The values obtained for the leakage inductance and AC resistance from the FEA simulation run at 1Mhz and the experimental values found by Dr. Jinghai Zhou in [3.5] are described in the table below. The FEA value corresponds very well to the measured values from the impedance analyzer by Dr. Zhou.

	Leakage Inductance (nH)	AC Resistance (mΩ)
Maxwell FEA Simulation	24.68	12.73
Measured Value	25	12

Table 3.1 Comparison between Maxwell theoretical and experimental results for discrete transformer

The leakage inductance of the transformer is not the only source of leakage in the system. The secondary loop inductance of the current doubler is equally important.

Modifying the FEA simulation to take into account the transformer and secondary loop the leakage inductance and AC resistance were measured and compared to the measurements performed in [3.5]. This leakage value is the effective leakage inductance in the system.

	Leakage Inductance (nH)	AC Resistance (mΩ)
Maxwell FEA Simulation	59.03	21.54
Measured Value	60	20

Table 3.2 Comparison between Maxwell theoretical and experimental results for discrete transformer and secondary loop inductance

Having the leakage inductance and AC resistance values we can estimate the losses resulting from body diode conduction loss, winding loss, and core loss from the discrete transformer and two output inductor scheme. The core loss of the transformer is given by [3.6] as 0.16W at a switching frequency of 1Mhz and a load current of 50A. The output inductors used are four high frequency inductors, two in parallel for each phase to reduce DCR loss of the output inductors. The resistance of each output inductor is around 0.1mΩ. Shown below is a bar graph showing the loss breakdown as a result of the magnetic design. This loss breakdown is for two phases operating at a switching frequency of 1Mhz and a load current of 50A.

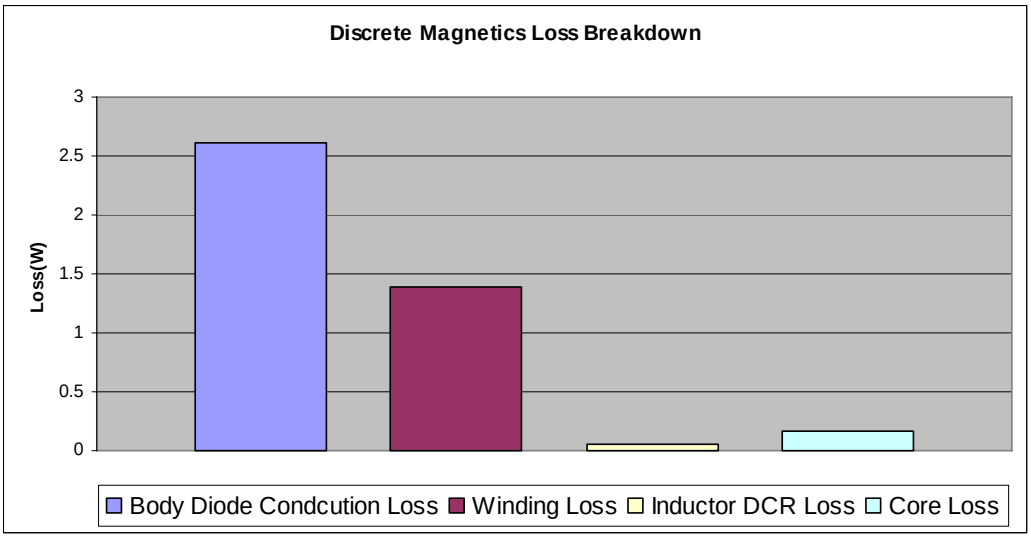


Fig 3.2 Loss breakdown of discrete magnetics case

Comparing the discrete magnetics version of the 12V non-isolated ZVS self-driven circuit to the state of the art 4 phase buck converter the benefit of this topology can be seen. The self driven running at a switching frequency of 1MHz is much more efficient than the state of the art buck converter run at the same frequency.

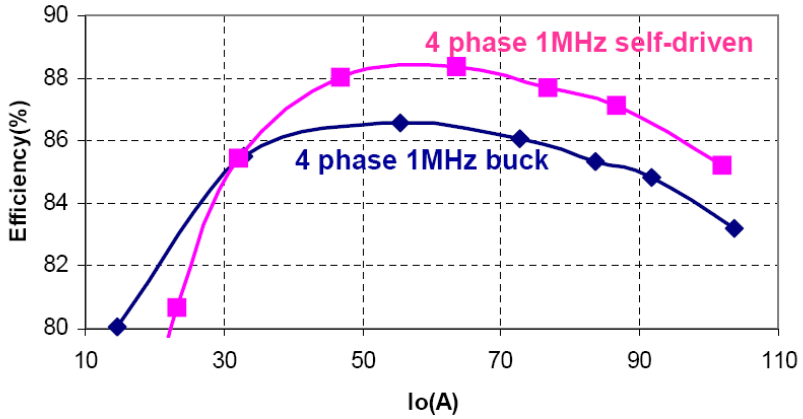


Fig 3.3 Efficiency comparison between self driven design and simple buck [3.5]

From the analysis of the discrete magnetics design we notice some areas for improvement. The body diode conduction loss is very high. Dr. Zhou proposed in [3.5] an improved magnetics structure which could remove the need for discrete output inductors which would reduce the number of magnetic components required and the leakage inductance. Lowering the leakage inductance will reduce the body diode conduction loss.

3.3 Original Integrated Magnetics Concept and Design

The original magnetics design that used a discrete transformer and two discrete output inductors was later changed by Dr. Zhou to the integrated magnetics version which consists of two UI cores which act as transformers and utilize the magnetizing inductance of the transformer to produce the output inductors. This design eliminates one magnetic component and also reduces the overall size of the magnetic components significantly. As noted in [3.5] having a smaller magnetic footprint allows for the use of wider winding traces which will reduce the transformer loss. The affect on circuit

operation was discussed in the previous chapter and the magnetic layout and loss breakdown will be discussed now.

Using a Maxwell FEA model to duplicate the original magnetics design performed by Dr. Zhou we can find why the integrated magnetics improved the efficiency of non-isolated ZVS self-driven circuit. The design of the integrated magnetics used three layers connected in series by vias (shown in black with grey through hole) to create each primary and used three layers in between the primary windings connected in parallel to create the secondary winding. The secondary windings have the three layers connected in parallel to reduce the winding loss in the high current output. Two sets of this design are placed in parallel to reduce winding loss and leakage inductance creating a twelve layer design. Shown below is the FEA model used for simulation.

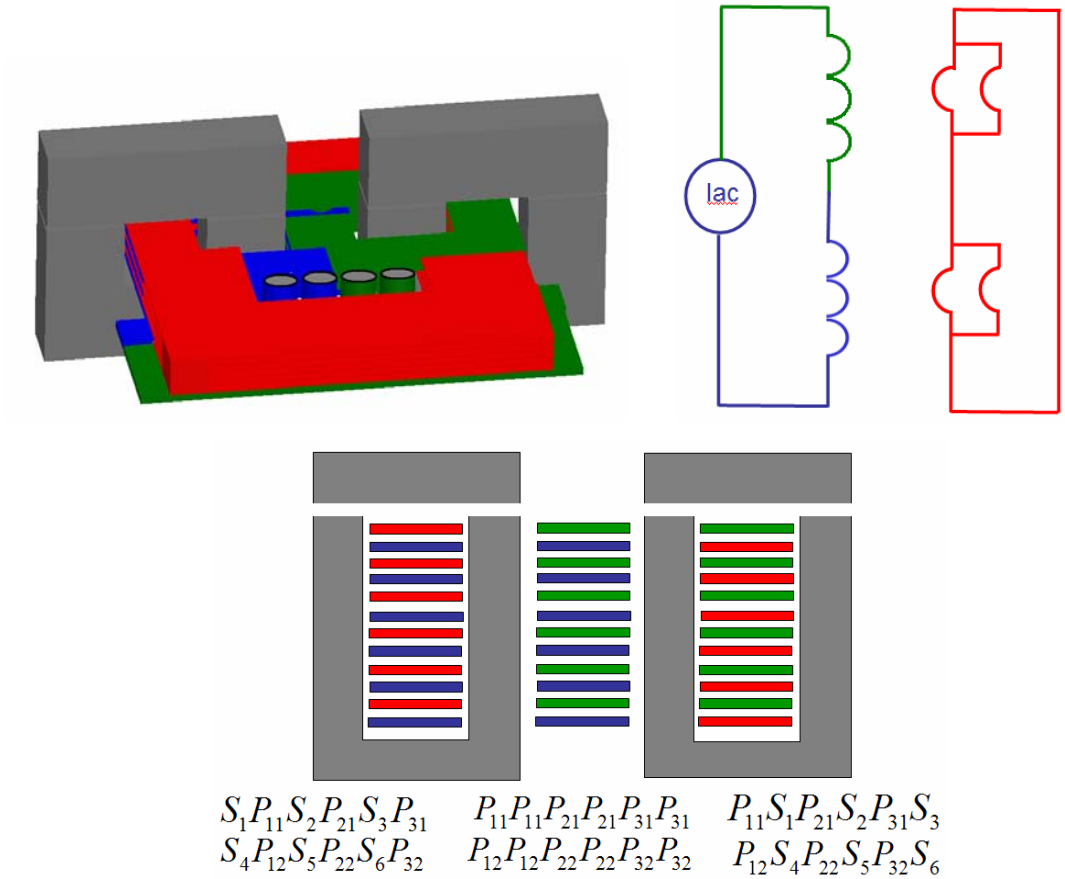


Fig 3.4 12 layer integrated magnetics modeled (a) Maxwell 3D Model (b) Electrical Model (c) Cross Section Core View

The integrated magnetics version used a 12 layer PCB design with two ounce copper used on each layer. The integrated magnetics structure uses two transformers that contained air gaps so that the magnetizing inductance can be set to the desired level for the output inductor. The primary windings in the integrated magnetics are interleaved in the center to reduce the leakage inductance and stray magnetic fields [3.7]. Shown below are two six layer cases to illustrate the benefit of interleaving, one with the primary windings not interleaved and the other with the primary windings interleaved. For simplicity, the skin effect is not considered in these cases. The benefit of interleaving the windings is that the opposing fluxes will partially or completely cancel and greatly reduce the MMF in the dielectric layers between windings which reduces winding loss and leakage inductance.

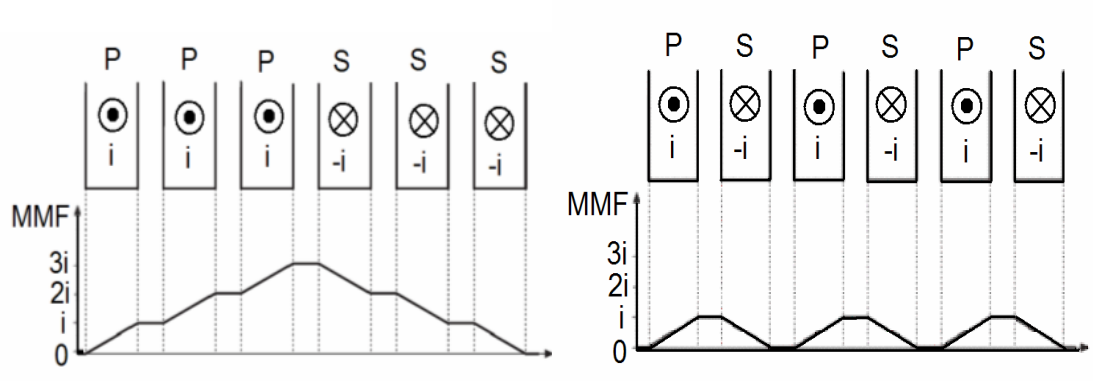


Fig 3.5 Interleaved and non-interleaved transformer designs

The primary windings are interleaved with the secondary windings inside the window to utilize the proximity effect to reduce the leakage inductance during the period of interest. The key period for leakage inductance occurs when both of the current doubler switches are turned on. During this period the secondary loop becomes a short for the purpose of leakage inductance. Lenz's law states that the induced voltage on a wire acts to produce an opposing flux [3.8]. Applying Lenz's law to our case we see that the primary winding will induce an opposing field in the secondary winding which will help reduce the leakage flux therefore reducing leakage inductance. The primary winding shown in blue has a current flowing out of the page which produces a field in a counter clockwise direction. According to Lenz's law a clockwise field will be generated

in the secondary winding which is depicted in red. This clockwise field in turn creates a current flowing into the page which will circulate in the secondary during this period. The current generated in the secondary winding will also produce additional winding loss but do to the brevity of this period it is considered negligible compared to the loss savings from reduced leakage inductance.

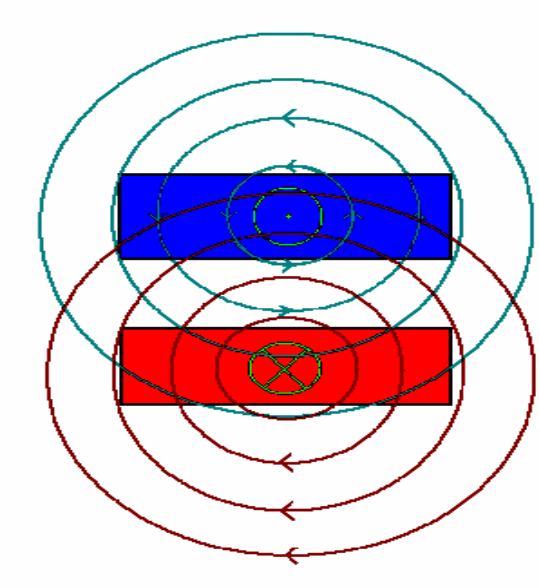


Fig 3.6 Illustration of fields induced on conductor according to Lenz's law

Using the FEA model for the original integrated magnetics version we can find the leakage inductance and AC resistance and quantify the benefit of the integrated magnetics over the use of discrete magnetics. The measurements performed were considered at 1MHz switching frequency and a 50A Load current.

	Leakage Inductance (nH)	AC Resistance (mΩ)
Maxwell FEA Simulation	43.07	28.73
Measured Value	38.77	28.14

Table 3.3 Comparison between Maxwell theoretical and experimental results for 12 layer integrated magnetics and secondary loop inductance

Having the leakage inductance and AC resistance values we can estimate the losses resulting from body diode conduction loss, winding loss, and core loss from the integrated magnetics scheme. The core loss of the transformer is estimated based on formulas from the manufacturer [3.6] as:

$$P_{Core} = C_m \cdot f_s^{\,x} \cdot B_{peak}^{\,y} \cdot (ct_0 - ct_1 \cdot T + ct_2 \cdot T^2)[mW/cm^3] \tag{3.8}$$

and

$$B_{peak} = \frac{\left(\frac{V_{in}}{N} - V_o\right) \cdot D}{2 \cdot f_s \cdot N \cdot A_C} \tag{3.9}$$

For the selected 3F4 core material we obtain the values from to datasheet for $C_m = 12 \cdot 10^{-4}$, x=1.75, y=2.9, $ct_0 = 1.15$, $ct_1 = 0.011$, and $ct_2 = 0.95 \cdot 10^{-4}$ From our circuit design we know the values for $V_{in} = 12$, N=3, $V_o = 1.3$, D=0.325, and $f_s = 1MHz$. A_C is the cross sectional area of our core and is equal to $12\,mm^2$. Using these formulas and the circuit parameters the core loss is estimated at 0.133W at a temperature, T, of 80 degrees Celsius.

Shown below is a bar graph showing the loss breakdown as a result of the magnetic design. This loss breakdown is for two phases operating at a switching frequency of 1Mhz and a load current of 50A. The winding loss of the magnetics is increased over the discrete case but is compensated for by decreasing the body diode conduction loss, core loss, and removing the output inductors completely. The key loss improvement is in the body diode conduction loss which is greatly improved.

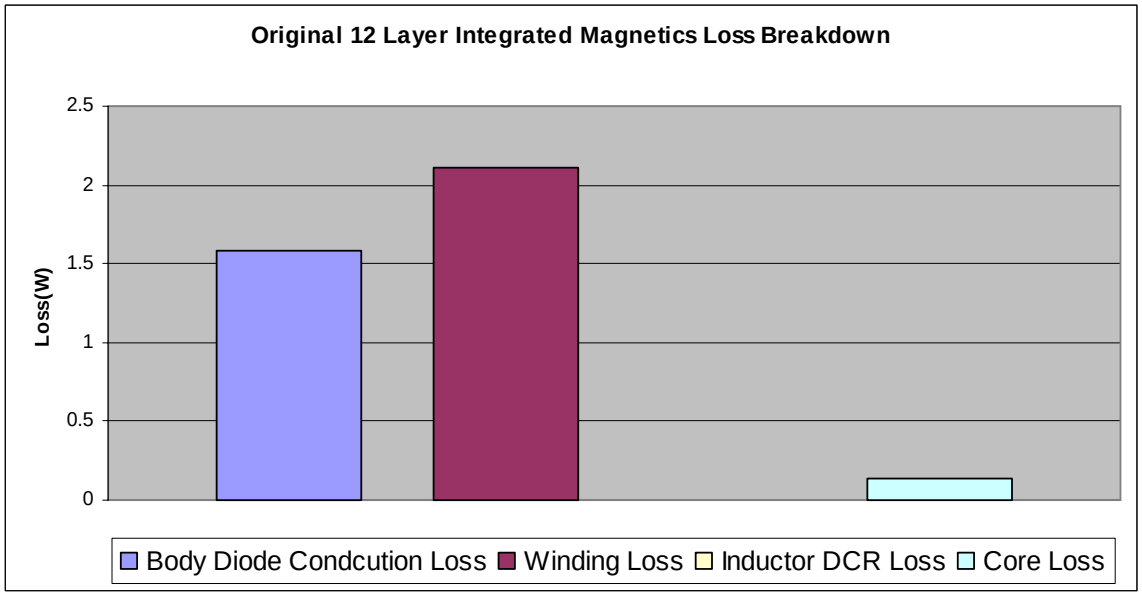


Fig 3.7 Loss breakdown for 12 layer integrated magnetics case

Comparing the integrated magnetics version of the 12V non-isolated ZVS self-driven circuit to its discrete magnetic component version we can see the efficiency improvements offered by the use of integrated magnetics. The integrated magnetics version of the self driven running at a switching frequency of 1MHz is about 2.5% more efficient than the discrete version run at the same frequency at a load of 50A. The hardware results shown below were performed by Dr. Zhou [3.5].

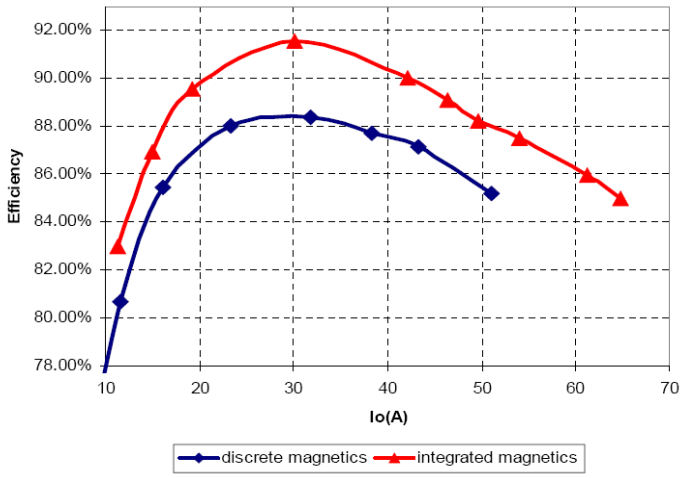


Fig 3.8 Efficiency comparison between discrete magnetics and integrated magnetics self driven designs

3.4 Cost Effective Integrated Magnetics Design

The original magnetic design in the non-isolated ZVS self-driven circuit used a twelve layer PCB board with two ounce copper on each layer. The industry's standard practice uses PCB boards with four to six layers because of the higher cost of boards with a great number of layers. To make this design more viable for industry adoption a six layer version was desired. To keep the winding loss similar between the six and twelve layer versions the copper thickness was doubled to four ounces for the six layer version. The first step was to recreate the twelve layer board while using only six layers. The winding pattern was left unchanged and the copper thickness made two times larger. The results from this design resulted in a much lower efficiency. Solving, explaining, and resolving theses issues is the work of this thesis.

Running at a very high switching frequency we encounter a significant amount of the skin depth effect in our windings. At high frequency the majority of current flows along the outside of windings. The current density decreases in at an exponential rate as you move towards the center of the conductor [power electronics book]. At the skin depth, δ, the current density is reduced to $e^{-1} = 0.368$. Since we doubled the copper thickness to four ounces it had to be made sure that the skin effect would not make such a move worthless because of skin effect. The calculation of skin depth at 1MHz is given as:

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \tag{3.10}$$

where ρ is the resistivity of copper (at 100 degrees C) and μ is the permeability and is considered equal to μ_o. This yields:

$$\delta = \frac{7.5}{\sqrt{f}} cm \tag{3.11}$$

At a switching frequency, f, of 1MHz the skin depth is calculated to be 0.075mm which is equivalent to 2.95 mils (1mil=1/1000inch=0.0254mm). The thickness of two ounce copper is given by [3.9] as 2.8 mils per layer and the thickness of four ounce copper is 5.6 mils thick. Shown below are the cases of two ounce and four copper at a switching frequency of 1MHz. The two ounce copper distributes current without any problem because its width is smaller than the skin depth. For the four ounce case there is also very good conduction because the skin depth is more than half the width so the current is well distributed in all of the winding. The two ounce copper never has a current density below 62% of the surface density while the four ounce copper has current density as low as 39% at the center. The higher current density is desirable but as the temperature rise, so will the skin depth and the four ounce copper's current distribution will be more uniform.

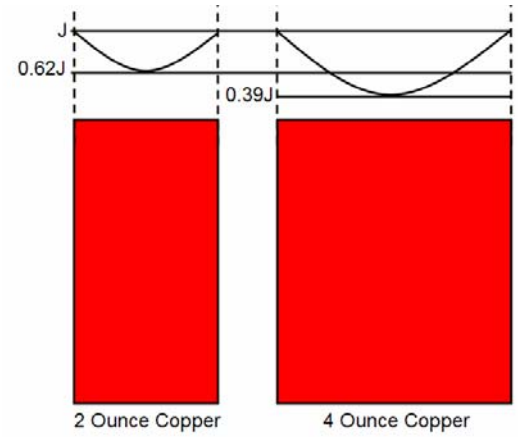


Fig 3.9 Current distribution in 2 and 4 ounce copper based on skin depth

The other major change by going from twelve layers to six layers is the leakage inductance. This is the significant problem faced for this case. The twelve layer version essentially used two parallel six layer boards so that the copper loss would be minimized and the leakage inductances would be essentially in parallel and theoretically be reduced to half of the value of the six layer version. As was discussed earlier the copper loss was combated by doubling the copper thickness. There is no solution that is an easy cost effective solution to reduce the leakage inductance. To reduce the leakage inductance the

magnetic design must be changed and improved. Before studying magnetic design alterations the current structure with six layers and four ounce copper is studied.

Shown below is the FEA simulation used to obtain the leakage inductance and AC resistance of the six layer four ounce copper design which will be the benchmark for this thesis work.

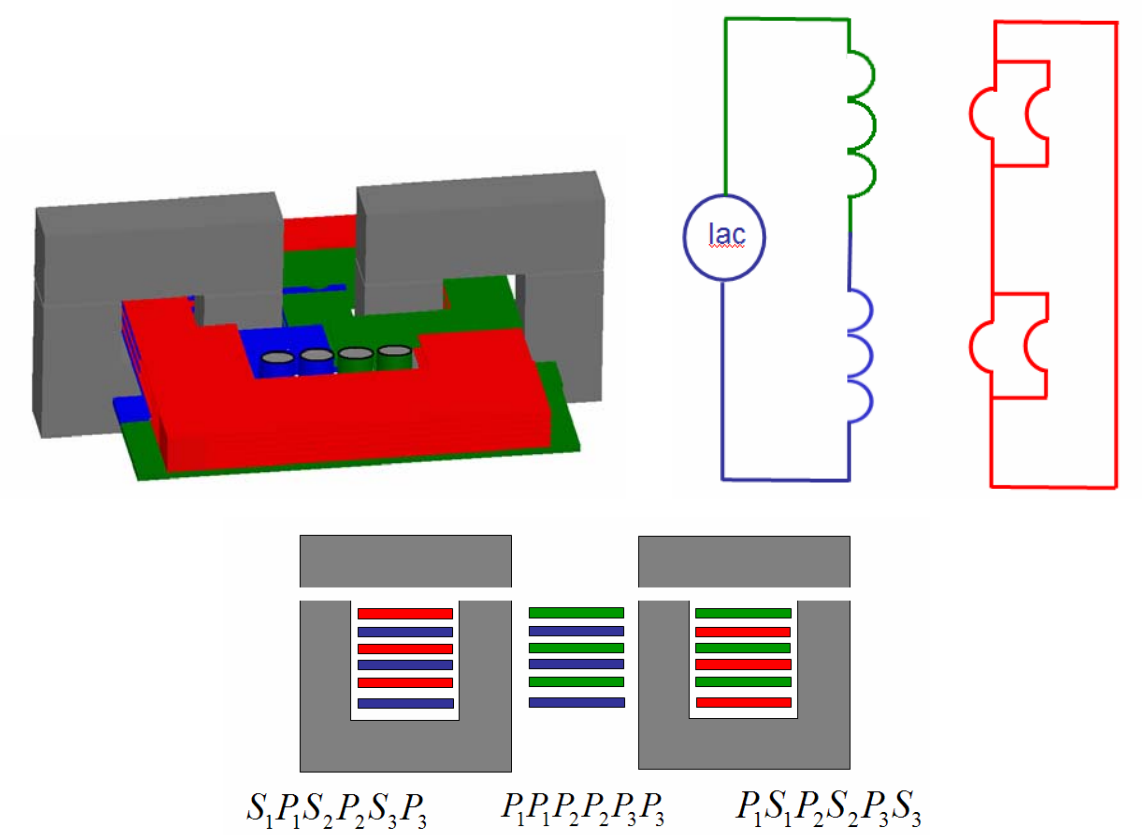


Fig 3.10 6 layer integrated magnetics modeled (a) Maxwell 3D Model (b) Electrical Model (c) Cross Section Core View

Using the FEA model the leakage inductance and AC resistance can be found and the areas that need to be improved in the magnetics can be identified. The measurements performed were considered at 1MHz switching frequency and a 50A load current. The difference between the measurement and simulation is a result of simplifications of the design that were implemented in the FEA to allow for faster simulation.

	Leakage Inductance (nH)
Maxwell FEA Simulation	49.84
Measured Value	52.49

Table 3.4 Comparison between Maxwell theoretical and experimental results for benchmark 6 layer integrated magnetics and secondary loop inductance

Looking at the loss breakdown and experimental results it becomes clear that the leakage inductance must be improved significantly if a six layer version is to approach the high efficiency of the more costly twelve layer design. The leakage inductance was found to be 38.77nH in the original twelve layer board, but was found to be 52.49nH in the six layer version using the same winding layout. The body diode conduction loss for the benchmark six layer case is significantly higher than the twelve layer case.

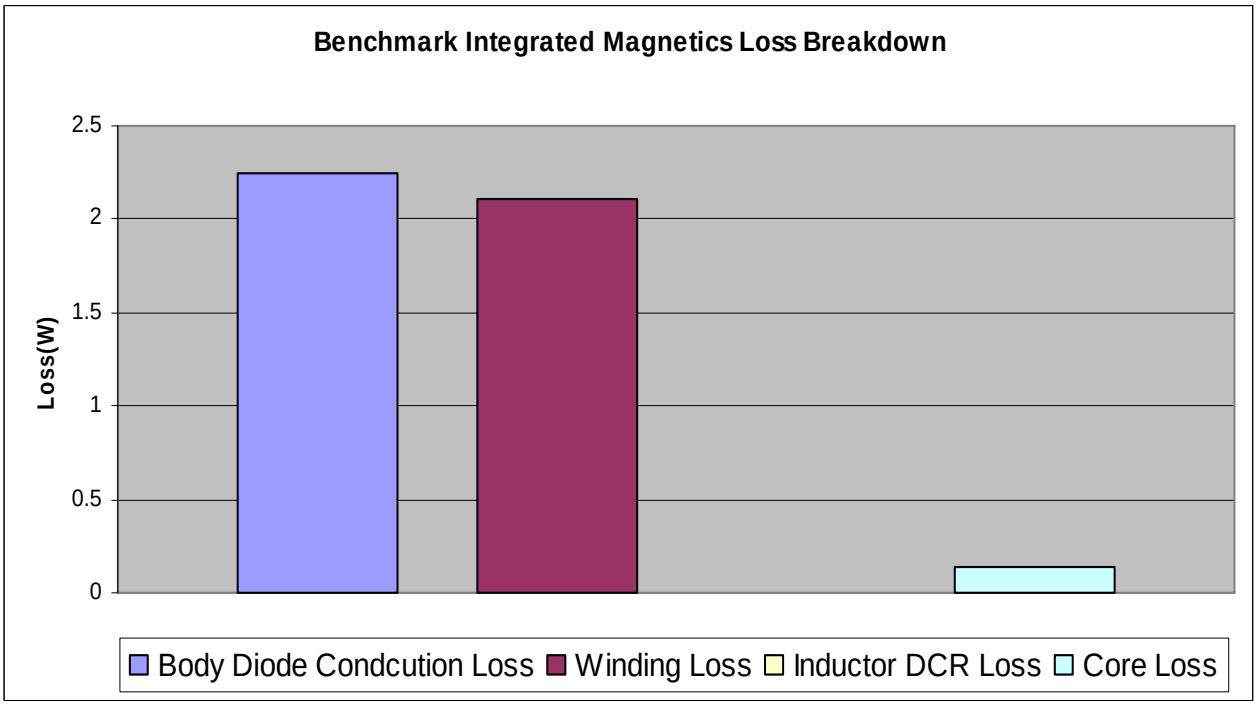


Fig 3.11 Loss breakdown of benchmark 6 layer integrated magnetics

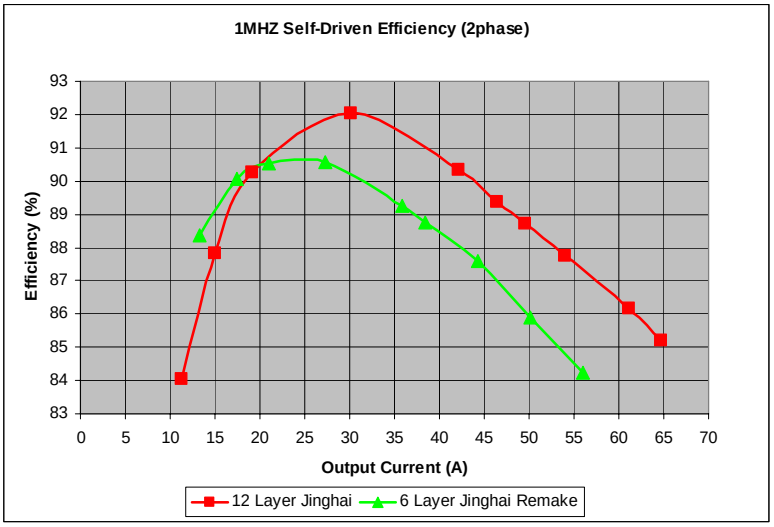


Fig 3.12 Efficiency comparison between 12 layer and 6 layer PCB integrated magnetics

Having a benchmark version with six layer PCB and four ounce copper allows for improvements in the magnetics to be quantified and prove that the improvements were a result of the magnetic design itself and not the board specifications and material changes. The goal is to achieve a similar overall efficiency of the twelve layer integrated magnetics design while using only six layers.

3.5 Improved Leakage Inductance Design

Knowing the areas of improvement for the cost effective 12V non-isolated ZVS self-driven circuit the study can begin. Having solved the major winding loss issues we know that the excess leakage inductance in the cost effective version degraded the performance significantly. To minimize the leakage inductance and improve overall circuit performance the magnetic design is analyzed from a simple single UI core case with one primary winding and one secondary winding and evolved from there into a new magnetic design with minimal leakage inductance for two three to one turn transformers.

The first test case used in the analysis of leakage inductance is a simple UI core with a single primary and single secondary winding. The dielectric thickness or distance between windings is varied and the effect on leakage inductance is studied. The effect of copper thickness on AC winding resistance was also looked at. Shown below is the FEA

simulation which was run at 15A (1/3 of load current) and at a switching frequency of 1MHz.

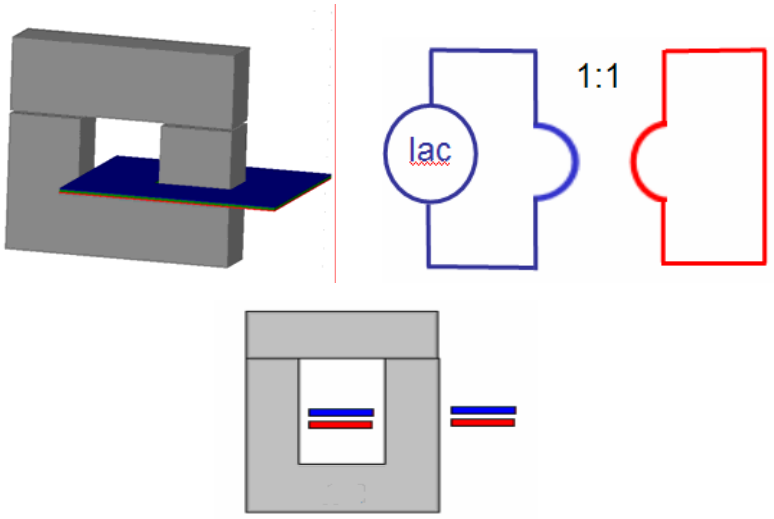


Fig 3.13 Simple 2 winding case modeled (a) Maxwell 3D Model (b) Electrical Model (c) Cross Section Core View

The simulation results showed that the leakage inductance is greatly dependent upon the dielectric thickness for the case where the primary and secondary windings are perfectly interleaved. From this simulation it can also be seen that at 1MHz switching frequency going to four ounce copper is justified. While the resistance may not be exactly half when you double the copper thickness it is a very acceptable improvement. The dielectric thickness was determined by the PCB manufacturer. The standard 6 layer board has a dielectric thickness of 12 mils between each layer but upon request at no additional cost a dielectric thickness of 5 mils can be used for our low voltage design.

Leakage Inductance

Dielectric Thickness \ Copper Weight	2oz	4oz
5mil	1.27nH	1.53nH
12mil	2.46nH	2.70nH

AC Resistance

Dielectric Thickness \ Copper Weight	2oz	4oz
5mil	3.05mΩ	1.80mΩ
12mil	3.06mΩ	1.74mΩ

Table 3.5 Effects of dielectric thickness and copper weight on leakage inductance and AC resistance for perfectly overlapped case

From the first test case which had perfectly interleaved windings it can be seen that keeping the windings in close proximity is directly related to lowering the leakage inductance. The next step was to create a case more like the one encountered in the 12V non-isolated ZVS self-driven circuit. In this case, two layers of the current design and varied the dielectric thickness between the layers.

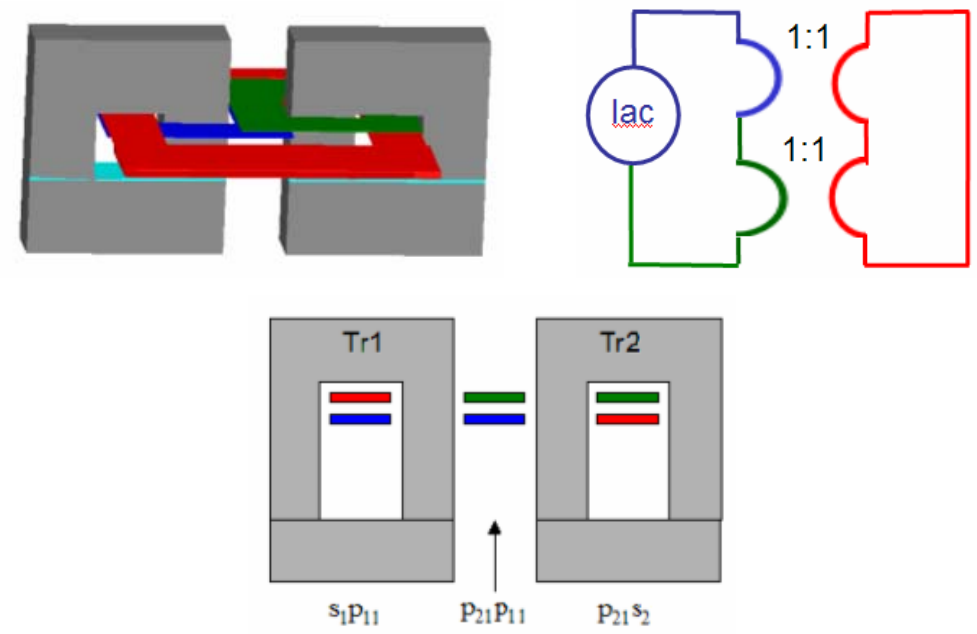


Fig 3.14 Non-overlapped 4 winding case modeled (a) Maxwell 3D Model (b) Electrical Model (c) Cross Section Core View

Looking at the leakage inductance in this case we see that varying the dielectric thickness has a minimal affect on the leakage inductance of the system. The AC resistance of the system was also not greatly affected by the dielectric thickness. The difference between this case and the perfectly interleaved winding case showed in the effect of the dielectric thickness on the leakage inductance. For this test case, the secondary winding path (red color) which contains the two current doubler switches was placed away from the primary windings. With the secondary windings moved away from the primary windings we see that effect of non-perfectly interleaving between windings.

Dielectric Thickness	Leakage Inductance Copper Weight	
	2oz	4oz
5mil	17.01nH	16.83nH
12mil	18.47nH	18.31nH

Dielectric Thickness	AC Resistance Copper Weight	
	2oz	4oz
5mil	10.80mΩ	6.33mΩ
12mil	10.60mΩ	6.12mΩ

Table 3.6 Effects of dielectric thickness and copper weight on leakage inductance and AC resistance for poorly overlapped case

To gain better theoretical insight into the reason why the non-interleaved secondary and primary windings result in a much higher leakage a simple test case is again used. For this test case a single primary winding and single secondary winding are used in a simple UI core arrangement. The alteration is in the interleaving of the primary and secondary windings. This case followed the actual design by having the secondary winding lie further off the core on one side, while the primary is tightly wound to the core. So, only partial interleaving of primary and secondary winding is achieved.

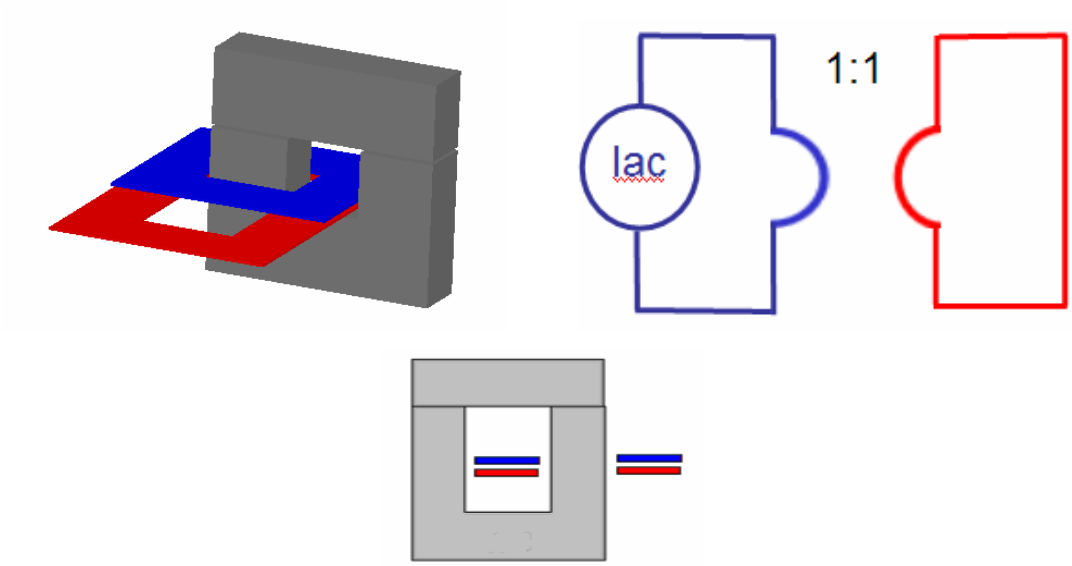


Fig 3.15 Simple 2 non-overlapped winding case modeled (a) Maxwell 3D Model (b) Electrical Model (c) Cross Section Core View

The leakage inductance for this case was found to be 8.06nH which is over four times larger than the perfectly interleaved case where the leakage was found to be

1.53nH. This increase in leakage inductance can be explained by looking at the definition of leakage inductance derived earlier:

$$L_k = \frac{1}{I^2}\int_{Vol} B \bullet H dv \tag{3.12}$$

which is equivalent to

$$L_k = \frac{\mu_o}{I^2}\int_{Vol} H^2 dv \tag{3.13}$$

The leakage inductance for our case has one independent variable, the magnetic field intensity, H. The permeability of air, μ_o, is set and the current I^2 is determined by the circuit operation. So, to minimize the leakage inductance in the system the magnetic field intensity must be minimized. Taking a look at the case where the primary and secondary windings are perfectly interleaved shown below we can see an issue related to leakage inductance.

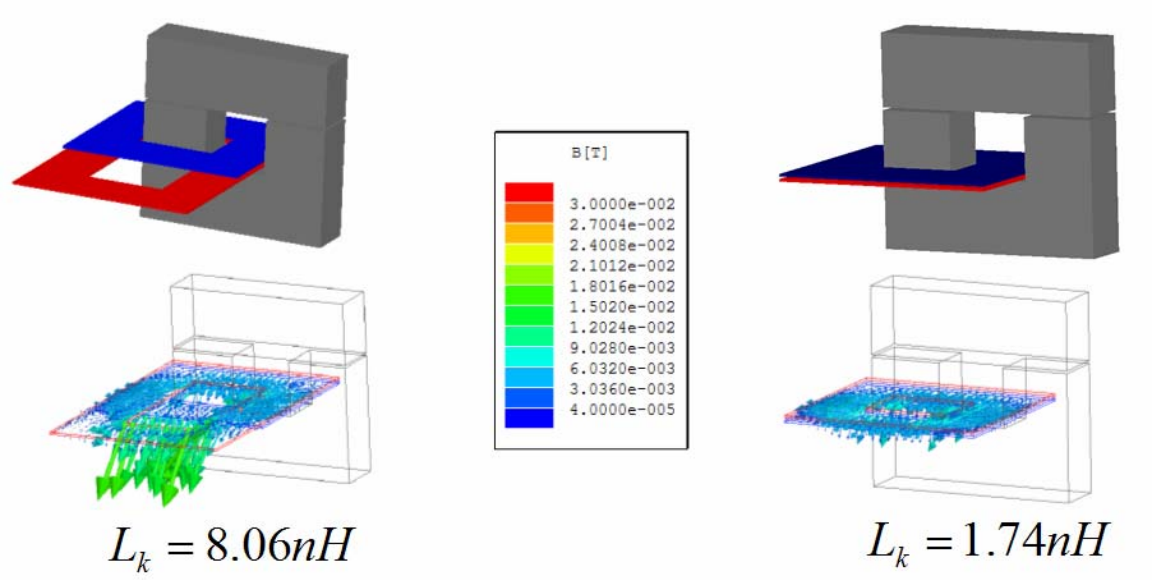


Fig 3.16 Magnetic field and leakage inductance comparison for overlapped and non-overlapped primary and secondary windings

The perfectly overlapped case encountered low leakage because the fields generated in the primary and secondary windings cancelled each other out significantly because of the close proximity of the wires. Also, as the wires were moved closer together there was a smaller gap for leakage inductance to be stored. For the case we are faced with we do not have the option to perfectly interleave the primary and secondary windings. This leads to little or no cancellation of magnetic field intensity for all windings that are not interleaved.

As can be seen in the FEA simulations, the magnetic field intensity is very high in the areas in which the primary and secondary windings are not perfectly interleaved. These areas lead to a significant amount of leakage inductance in the system. This explains why for the 12V non-isolated ZVS self-driven circuit changing the dielectric thickness or distance between windings has little affect on the leakage inductance. Having the conductors closer together improves the leakage inductance of the system, but not to the degree necessary to match the performance of the twelve layer original PCB design.

To better explain how the field cancellation occurs in the perfectly interleaved case and poorly interleaved case refer to the diagrams below. If the windings are not interleaved or aligned then the magnetic fields induced by the wires are also unaligned and unable to cancel and reduce the stray fields in the system. This situation is bad not only for our case but for basic transformer design where leakage inductance is undesired. Shown below are the cross sections of conductors that are perfectly overlapped and poorly overlapped. The primary winding is shown in blue and the secondary conductor is shown in red. The primary current flows out of the page and produces a counter clockwise magnetic field. The field from the primary current induces a current flowing into the page on the secondary winding. The current in the secondary produces a magnetic field in the clockwise direction which will cancel out with the primary very well if the overlapping is very good.

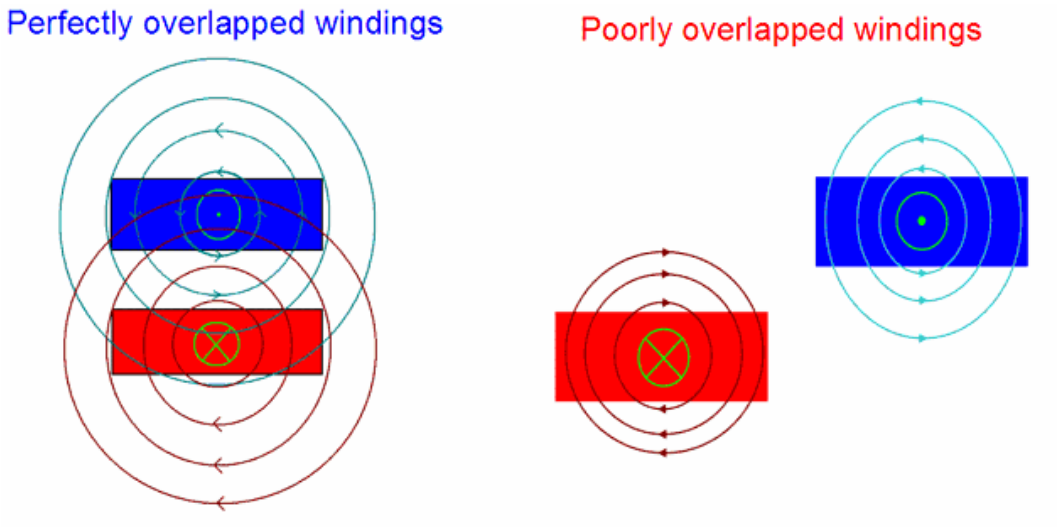


Fig 3.17 Effects of overlapping windings on field cancellation

Having identified the area of high leakage in the 12V non-isolated ZVS self-driven circuit an alternate magnetics design can studied to reduce the leakage in the system. Taking a look at the current layout it can be seen that the two switches in the current doubler are offset from the primary windings by 4 vias. These are the vias used to connect the primary windings in series.

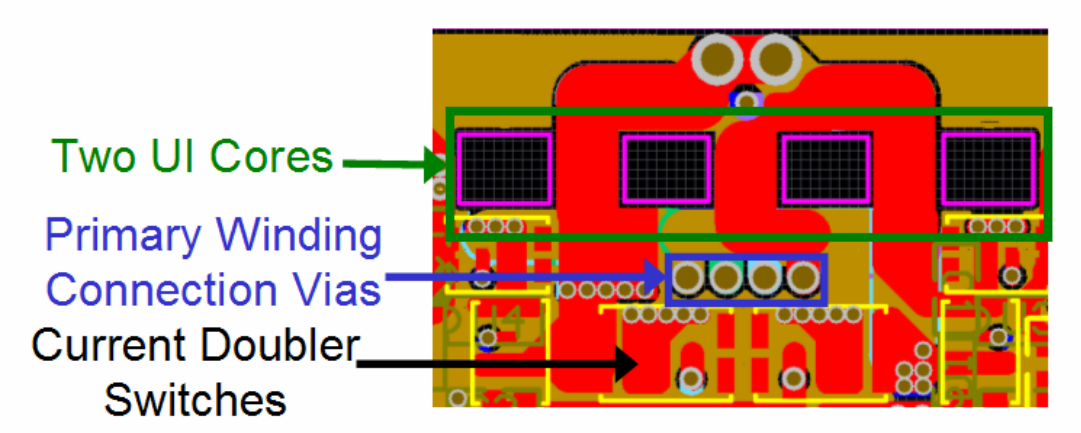


Fig 3.18 Problem resulting from connection vias decreasing winding overlapping

The primary winding connection vias push the current doubler switches further away from the windings and prevent the secondary winding from extending wider and interleaving with the primary windings better. The next test simulation was to remove

the primary winding connection vias and push the current doubler switches closer to the primary windings.

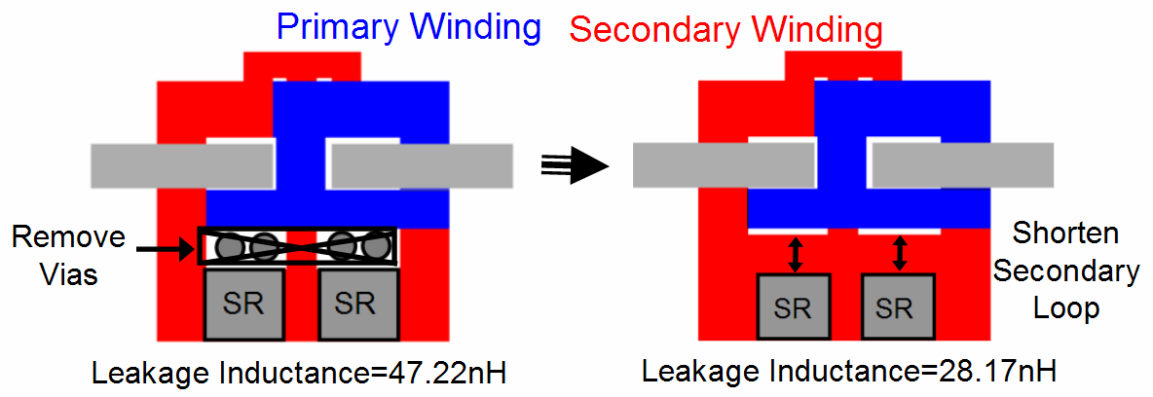


Fig 3.19 Reduction of leakage inductance resulting from removing connections vias

The leakage inductance is reduced by over 40% by removing the primary winding vias. Shown below are the FEA models for the two cases and plots with the energy fields. As can be seen from the legend, there is a lot of lost energy in the gaps. The place where the most energy is lost is at the connector for the secondary windings at the top of the magnetic structure and in the gap between the current doubler switch path and the primary windings. Changing the secondary winding connection point to reduce leakage would be difficult without causing large electrical losses. But, changing the area between the current doubler switch path and primary windings is something that can be done that will not hurt the electrical performance.

The four primary winding connection vias for the original design create a large gap between the current doubler switch path and primary windings, in this area a great amount of leakage energy occurs. When those primary winding connection vias are removed a much smaller amount of lost energy is encountered which leads to a 40% reduction in leakage inductance.

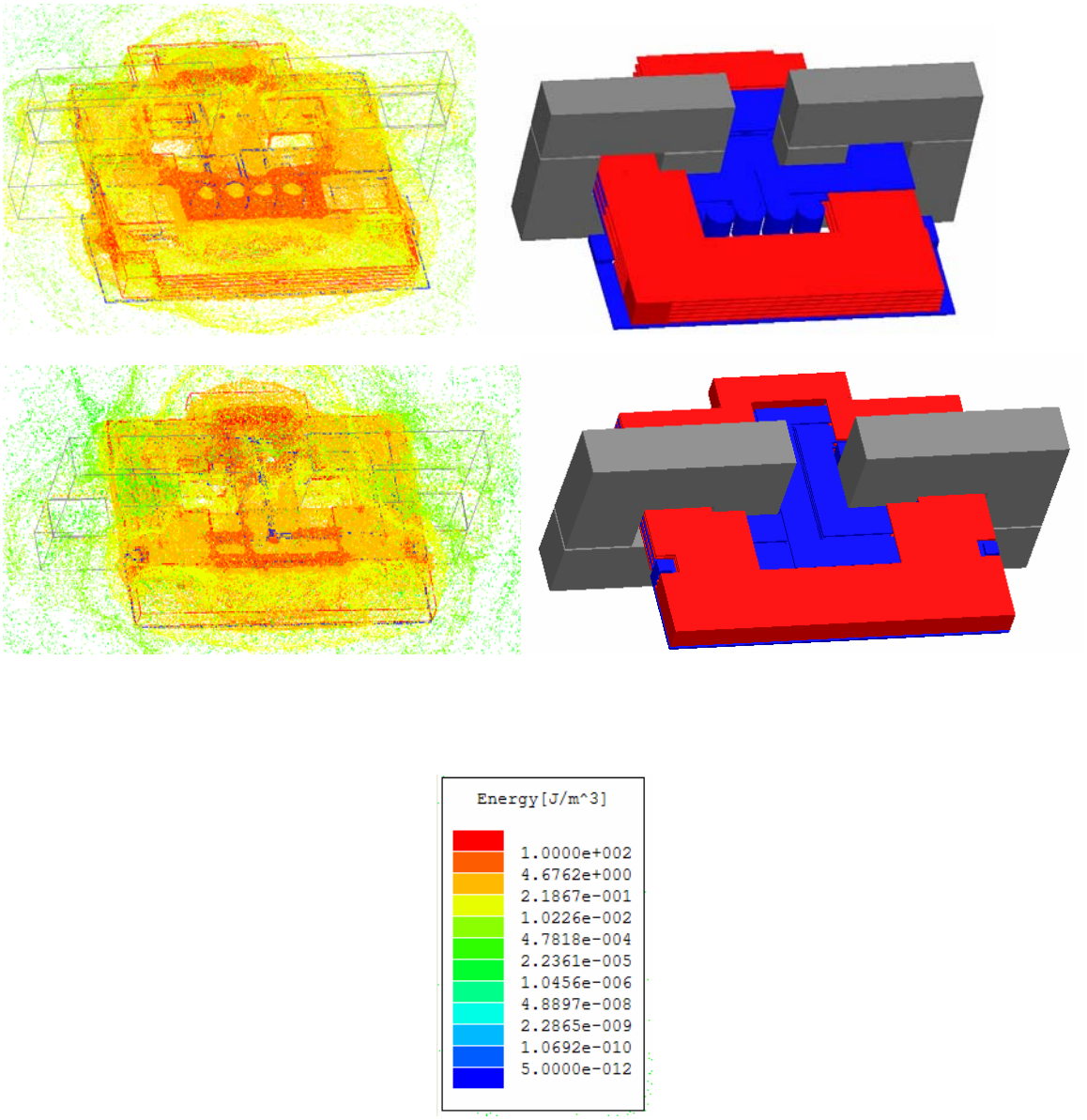


Fig 3.20 Reduced amounts of energy lost to the air as a result of removing the connection vias to allow for better overlapped windings

Removing the primary connection vias also allows for an improvement in the secondary windings. The secondary windings can now become wider and interleave with the primary windings better. This leads to additional leakage inductance saving of over 30%. The reduction of leakage resulting in this case can be once again be explained by looking at the energy plot of the system.

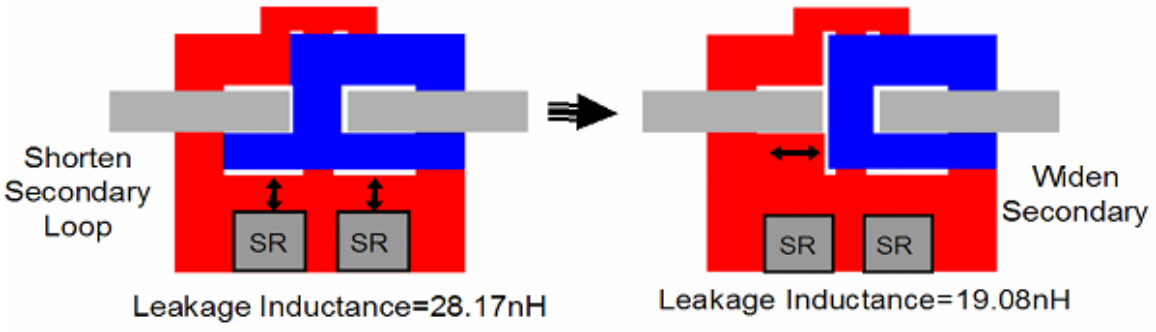


Fig 3.21 Effects of overlapping windings on reducing leakage inductance

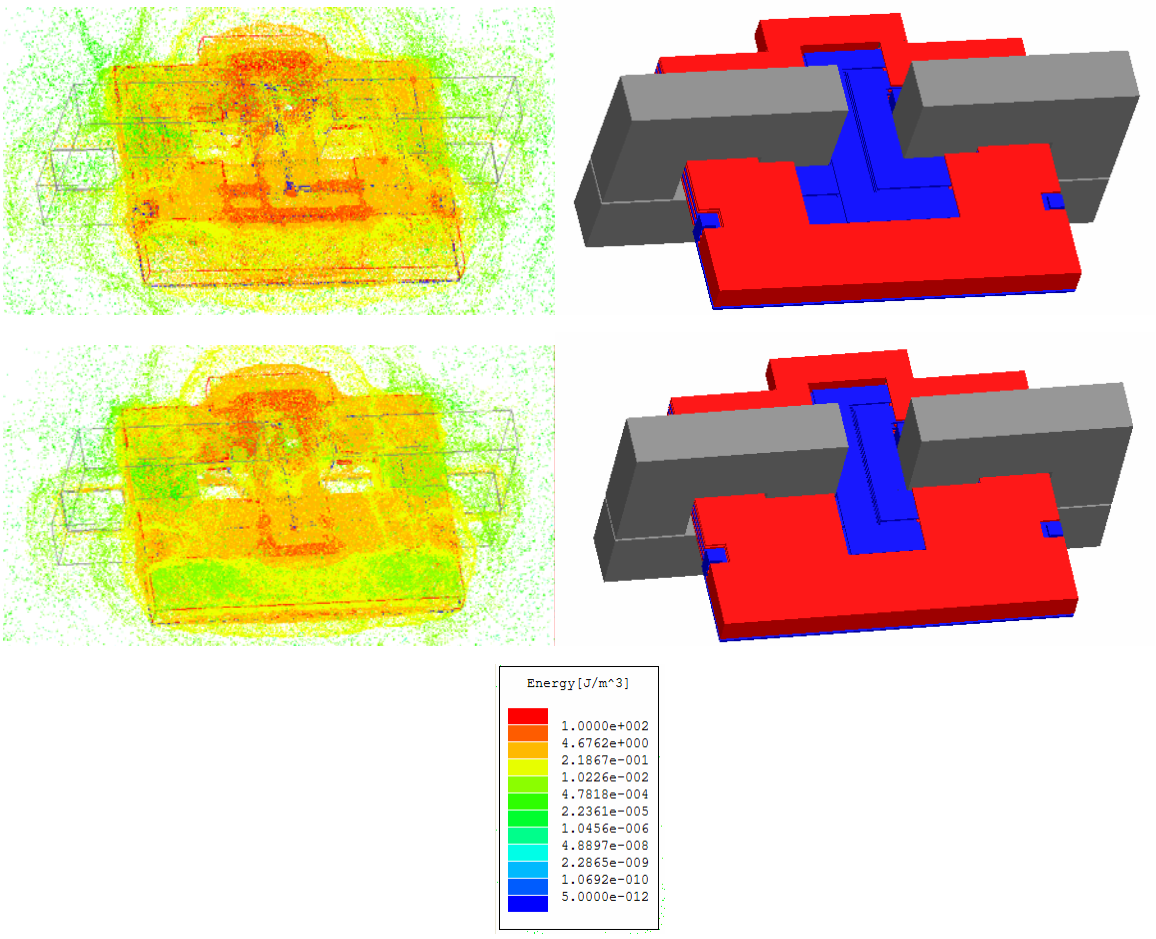


Fig 3.22 Reduced amounts of energy lost to the air as a result of overlapping the secondary windings better with the primary windings

The energy plot for this case shows a similar result as when the primary winding connection vias were removed. When the secondary winding interleaves with the primary winding better, the fields generated cancel out more completely and there is less energy lost in the system. As the overlapping in this case increases, the area where interleaving does not occur is reduced and the energy hotspot is reduced.

In this section a method to reduce the leakage inductance of the original 12V non-isolated ZVS self-driven magnetics design was proposed. By reducing the leakage inductance to a lower value than the twelve layer board achieved it is hoped that a similar performance can be achieved with a greatly reduced overall cost. The next step is to implement these magnetic improvements and verify the benefit of the improved magnetic structure.

3.6 Improved Magnetics Design Implementation

As was discussed in the previous section there is a great benefit related to leakage inductance that can be achieved by removing the primary winding connection vias and interleaving the primary and secondary windings as much as possible. But, to remove these windings another way must be found to connect the primary windings or create three turns. The obvious choice is a spiral configuration like the one shown below.

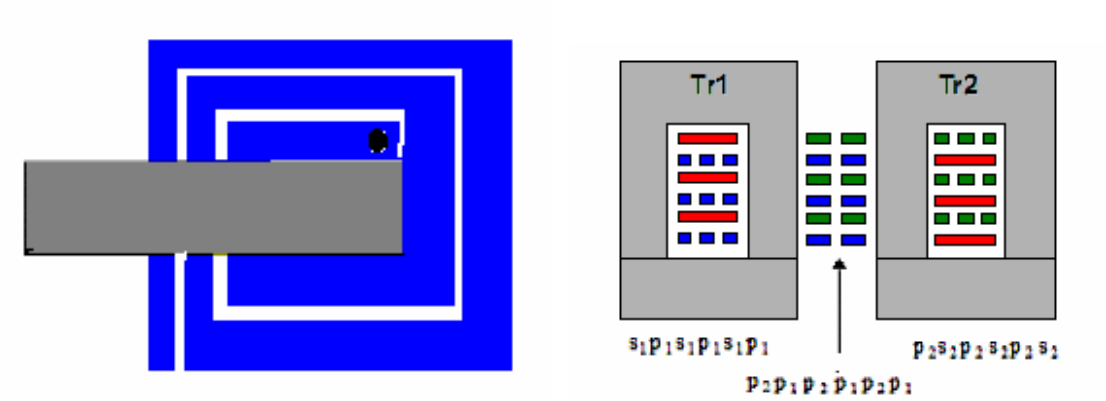


Fig 3.23 Spiral winding configuration and cross section view

The spiral configuration makes all three primary turns in one layer. The thinner windings will have a higher resistance but since all three turns are in one layer the other three layers can be used for parallel winding sets to minimize the resistance. The secondary winding design does not change other than that they are interleaved better with the primary windings because the connection vias have been removed from the primary windings. The spiral winding configuration provides a sense of freedom in the choice of layers used for the primary and secondary windings. As was discussed in chapter 2, the secondary current carries the sum of the transformer current and inductor current. Having additional current in the secondary may make it beneficial to reduce the number of primary layers and increase the number of secondary layers to minimize winding loss.

The two configurations considered in this study are two primary layers, four secondary layers and three primary layers, three secondary layers designs. The four secondary layers design offers a lower secondary resistance which would be beneficial for the higher secondary current. The four secondary layers design also offers a simpler layout for the current doubler switches in this topology. The three primary and secondary layers design offers a lower standard leakage and minimal primary losses.

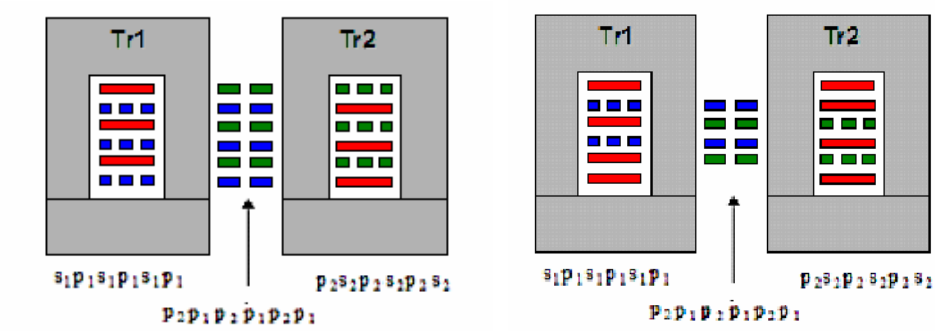


Fig 3.24 Two different winding arrangement options: 3 primary and 3 secondary windings or 2 primary and 4 secondary windings

Analyzing the leakage inductance in the two cases begins by looking at the field generated in between the windings for each case. Looking at the MMF diagram for the two cases it can be seen that the three primary three secondary case with perfect interleaving has much smaller energy in the dielectric area than the two primary four secondary winding case. This will result in a lower leakage in the better interleaved case if all else is held constant.

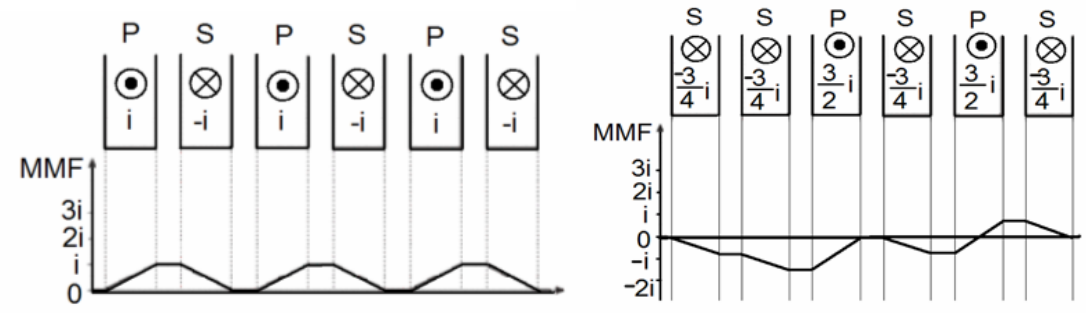


Fig 3.25 MMF diagrams of 3 primary and 3 secondary windings and 2 primary and 4 secondary windings

With the lower leakage in between layers we find that the three primary three secondary design has a lower leakage than the two primary four secondary design. The problem with this assumption is the affect on layout.

	Leakage Inductance (nH)
3 Primary 3 Secondary	25.17
2 Primary 4 Secondary	27.53

Table 3.7 Leakage inductance comparison between different winding arrangements without considering layout

Even though the theoretical leakage of the two primary four secondary designs is higher, it is not ruled out as a possible best case because it could offer lower conduction losses and because it allows for easier layout. The layout for the two primary winding and four secondary winding design allows the current doubler switches to be placed in a different orientation which will minimize allow for the secondary loop to be much smaller than the three primary design. The leakage current must flow through the switches so the two primary designs offers a route for the current that allows for much better interleaving with the primary winding a smaller secondary loop. But, it must overcome the extra energy that will be stored in between the winding layers.

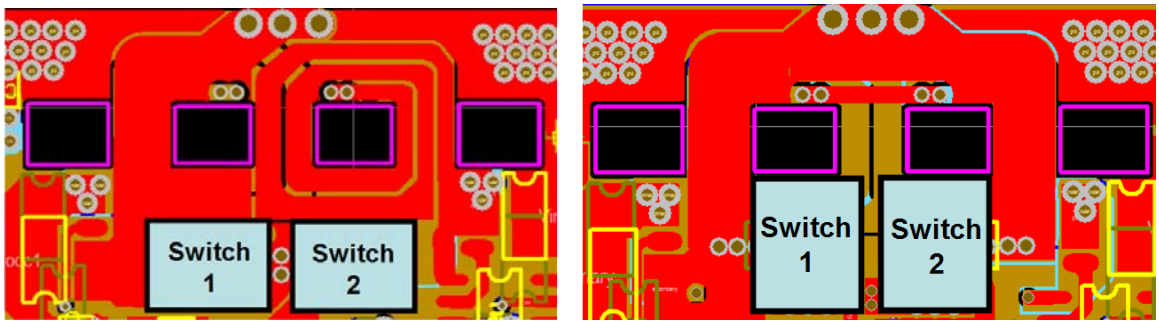


Fig 3.26 PCB layout differences for 3 primary and 3 secondary windings and 2 primary and 4 secondary windings

The final way to determine which leakage design was optimal was through hardware testing. The hardware results showed that the improved chip layout in the two primary case did indeed overcome the excess leakage in between the layers and prove to have improved leakage inductance. Although, in both cases the leakage inductance was improved significantly and for cases where switch layout is not an issue the 3 primary 3 secondary design is recommended to achieve low leakage inductance.

	Leakage Inductance (nH)
3 Primary 3 Secondary	30.09
2 Primary 4 Secondary	28.64

Table 3.8 Leakage inductance comparison between different winding arrangements considering layout

The experimental results shown below reflect the difference in leakage inductance values. The lower leakage case having higher full load efficiency and the higher leakage case having better light load efficiency.

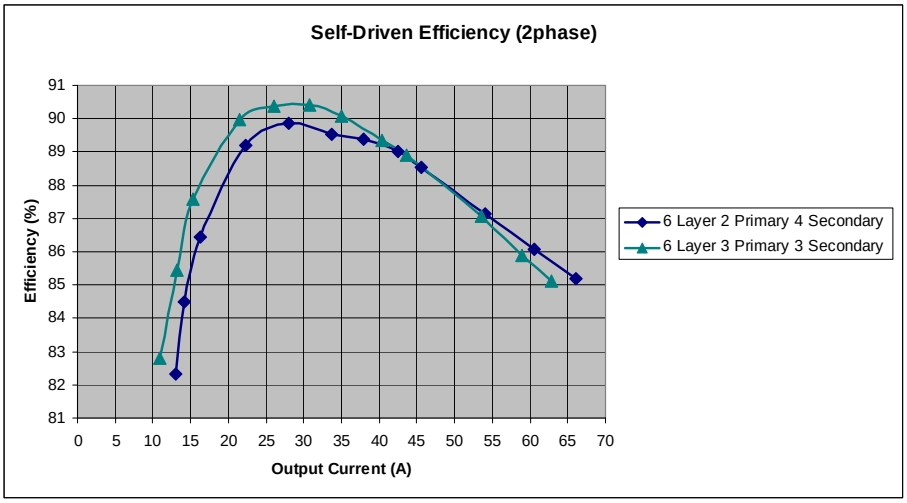


Fig 3.27 Efficiency comparison between 3 primary and 3 secondary windings and 2 primary and 4 secondary windings designs

The theoretical value of the two primary and four secondary case closely matched the value obtained from FEA simulation because of the very similar layout. For the three primary three secondary design the FEA simulation file had to be modified to accommodate the changes that had to be made to the hardware design. Shown below is the modified FEA simulation for the three primary winding three secondary winding design and the simulated leakage inductance which matches very well with the measured value.

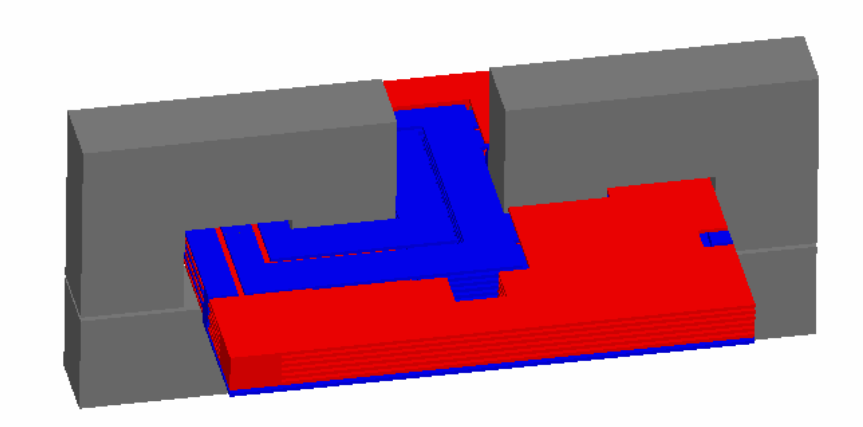


Fig 3.28 Maxwell 3D model of 3 primary 3 secondary winding design

	Leakage Inductance (nH)
Maxwell FEA Simulation	29.53
Measured Value	30.09

Table 3.9 Leakage inductance comparison between theoretical and experimental results for 3 primary 3 secondary case

The final magnetics design used the two primary layer four secondary layer layout and placed the two current doubler switches onto the primary windings for minimal leakage inductance. This design made it difficult to route the gate signals for the parallel set of current doubler switches, so only one was used for phase. This design allows for the lowest leakage possible do to the almost perfect interleaving of the primary and secondary windings. The measured leakage inductance for this design was found to be 22.29nH which is significantly lower than the four current doubler device designs discussed earlier. The main drawback is the use of only one switch changes the circuit operation greatly and the leakage gain is offset by conduction loss and thermal limitations of the current doubler switch.

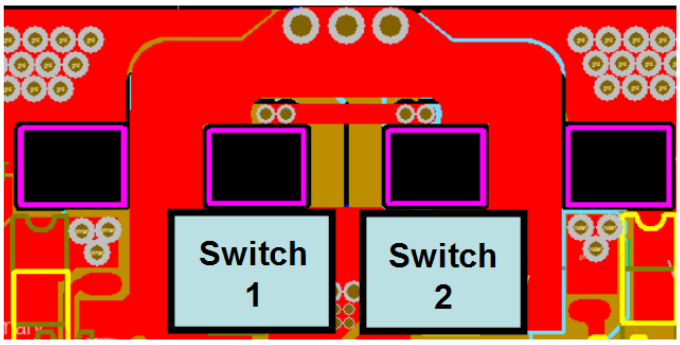


Fig 3.29 Layout for single current doubler switch design

	Leakage Inductance (nH)
Maxwell FEA Simulation	23.76
Measured Value	22.29

Table 3.10 Leakage inductance comparison between theoretical and experimental results for 2 primary 4 secondary case with a single current doubler switch

Shown below is a summary of the leakage inductance found for the six cases analyzed in this chapter. As can be seen for the table, the improved magnetic designs proposed in this work all have much lower leakage inductances than the first version of the six layer version of the integrated magnetics version and even have a substantial improvement over the twelve layer design.

	Measured Leakage Inductance (nH)	Maxwell FEA Leakage Inductance (nH)
3 Primary 3 Secondary	30.09	29.53
2 Primary 4 Secondary	28.64	27.53
Original 12 Layer Design	38.77	43.07
Original 6 Layer Design	52.49	49.84
Discrete Transformer Design	60	59.03
Single Switch Design	22.29	23.76

Table 3.11 Leakage inductance comparison between theoretical and experimental results for all cases studied in chapter 3

The leakage inductance for this topology was greatly improved while using the same real estate as the original version while decreasing cost. But, in the 12V non-isolated ZVS self-driven circuit the winding loss in the magnetics is also very important to the efficiency.

3.7 Winding Loss for Integrated Magnetics

In the previous sections the winding loss was assumed to be very similar in each case so leakage inductance could be focused on. Having improved the leakage inductance improvements an accurate winding loss analysis of the different winding structures must be performed so that the best magnetics structure can be identified.

Earlier in this chapter the formula for AC resistance was derived to be:

$$R_{AC} = \frac{1}{I^2} \iiint_V \frac{J \bullet J^*}{\sigma} dV \tag{3.14}$$

Using the FEA models created earlier the AC resistance of the primary and secondary windings could be obtained separately by looking at the current and current density in the primary and secondary windings and the corresponding current density. To break down the winding loss for the simple transformer design is relatively simple and discussed in [3.5] as:

$$P_{primary} = I_{Rms}^2 \cdot R_{ac(\,first\_harmonic)} \tag{3.15}$$

The primary winding current for the 12V non-isolated ZVS self-driven circuit is treated as a sinusoidal current for our analysis.

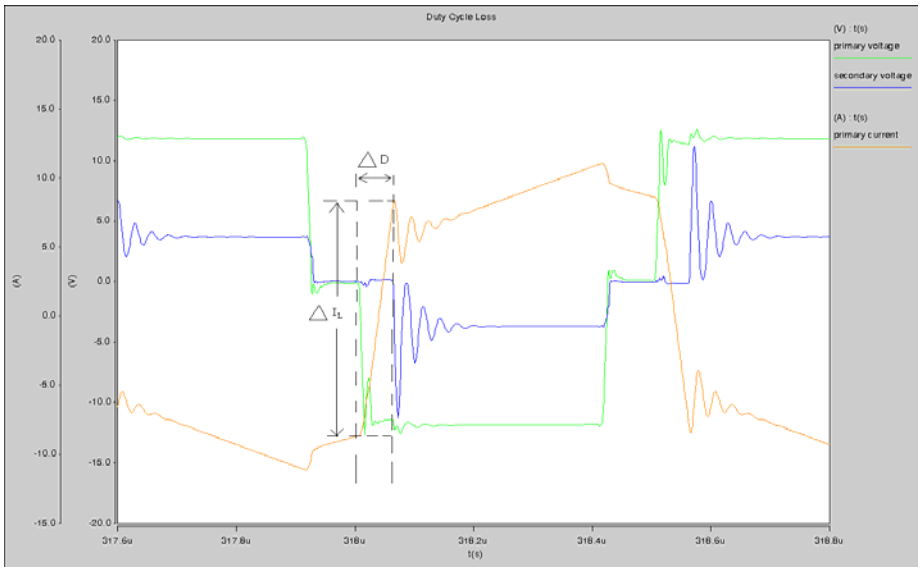


Fig 3.30 Primary current in the transformer windings

The secondary windings current in the original design using a discrete transformer is the same as the primary, raised by the turns ratio. But, for the integrated magnetics version, the secondary is a combination of the transformer current and the output inductor current. This current does not follow a sinusoidal pattern and this will have an effect on the winding loss calculation[3.5].

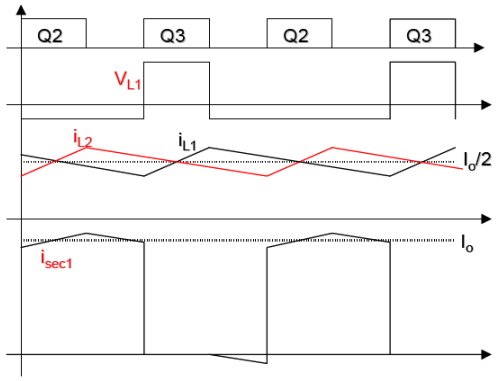


Fig 3.31 Secondary winding waveforms and currents

Since the current in the secondary winding does not follow the sinusoidal shape it would be inaccurate to treat the loss the same as with the primary case. A method

proposed in [3.10][3.11] proposes breaking down the waveform into DC and AC harmonic components and then using computing the winding loss from:

$$P_{Secondary} = I_{AV}^2 \cdot R_{DC} + I_{Rms}^2 \cdot R_{ac(\,first\_harmonic)} \tag{3.16}$$

To find the harmonic currents [3.11] uses Fourier series to break down some waveforms common in switched power supplies. The secondary current in the integrated magnetics version of the 12V non-isolated ZVS self-driven circuit is treated as a rectangular wave pulse for easier Fourier analysis.

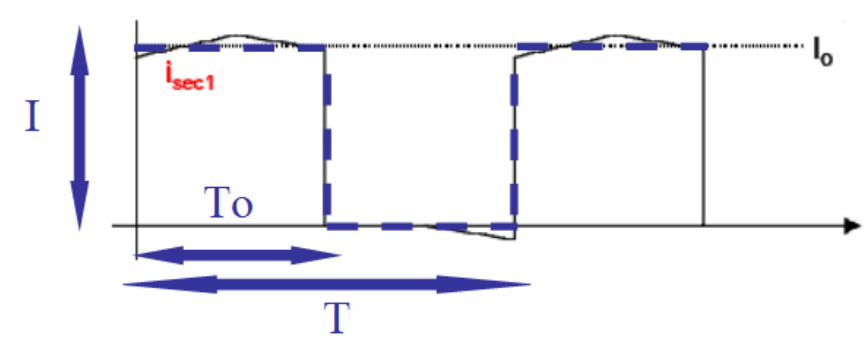


Fig 3.32 Approximation of secondary current as a square wave

The Fourier series for the simplified current in the secondary windings is given by:

$$I(t) = \frac{I * T_o}{T} + \sum_{n=1}^{\infty} \frac{2I}{\pi n} \cdot \sin\left(\frac{nwT_o}{2}\right)\cos(nwt) \tag{3.17}$$

The harmonic current and DC bias current sum together to build the waveform encountered in the secondary windings.

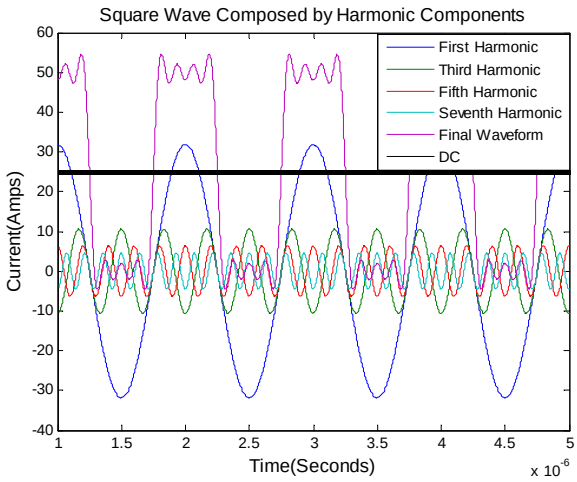


Fig 3.33 Final secondary current composed by harmonic components

To find the power loss in the secondary windings the AC resistance of the secondary at the harmonic frequencies must be found. The higher the frequency, the greater the impact of skin depth is encountered in the system. According to [3.7] the AC resistance of a conductor can be estimated from the DC resistance of a conductor which is given as:

$$R_{DC} = \rho \frac{\ell_b}{A_W} \tag{3.18}$$

where ρ is the resistivity of copper which is estimated to be $2.3 \cdot 10^{-6} \Omega - cm$ for copper at 100° C, ℓ_b is the mean length of the winding, and A_W is the cross sectional area of the winding.

$$R_{AC} = \frac{h}{\delta} R_{DC} \tag{3.19}$$

where h is the height or depth of the conductor and δ is the skin depth which was defined earlier as:

$$\delta = \frac{7.5}{\sqrt{f}} cm \tag{3.20}$$

Using this approximation the AC resistance of the windings for each harmonic is found to be (layer four ounce copper case):

	Normalized Resistance
First Harmonic (1Mhz)	1
Third Harmonic (3Mhz)	1.73
Fifth Harmonic (5Mhz)	2.24
Seventh Harmonic (7Mhz)	2.65

Table 3.12 Effect of skin depth effect in conductors assuming depth of conductor much larger than the skin depth

One drawback of this approximation is that the height or depth of the conductor is much larger than the skin depth, which is not the case for the 12V non-isolated ZVS self-driven circuit with four ounce copper where the conductor height is about twice as large as the skin depth. For this case the proximity effect does not have as dramatic affect when inducing currents in the other windings. In this complex case, FEA simulation is the best chance to give an accurate look at the AC resistances. The values obtained from FEA simulation show how the simplified calculation has error in the case where the conductor depth is not much larger than the skin depth.

	Normalized Resistance
First Harmonic (1Mhz)	1
Third Harmonic (3Mhz)	1.53
Fifth Harmonic (5Mhz)	1.79
Seventh Harmonic (7Mhz)	1.89

Table 3.13 Effect of skin depth effect in conductors when skin depth is similar to copper thickness

Obtaining the AC resistances up to the 7^{th} harmonic is a very long and time consuming process and to simplify the loss breakdown the power loss for each harmonic

is broken down. As can be seen below, the losses from the DC bias, first and third harmonic give a very accurate look at the losses encountered in the system and speed the analysis up greatly.

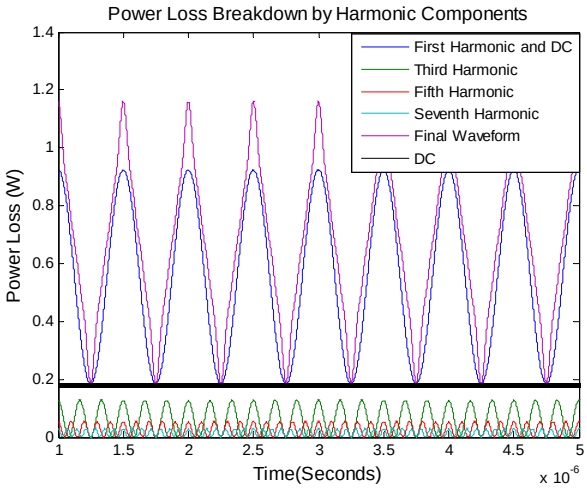


Fig 3.34 Total power loss comprised of harmonic loss components

	DC	DC,1	DC,1,3	DC,1,3,5
PLoss(W)	0.37	1.11	1.24	1.29

Table 3.14 Power loss resulting from harmonic losses

	Original Layout (4oz copper)	Spiral configuration 3 primary 3 secondary (4oz copper)	Spiral configuration 2primary-4secondary (4oz copper)
Rsec(mΩ)	13.56	13.30	13.16
Psec(W)	1.34	1.29	1.18
Rprim(mΩ)	16.43	15.44	17.65
Pprim(W)	1.14	1.07	1.23
Ptotal(W)	2.48	2.36	2.41

Table 3.15 Power loss for all cases studied

Having accurate estimates of the AC resistances up to the third harmonic of the different designs the winding loss can be determined. The values of the secondary and primary winding resistances were obtained separately to give a more accurate loss breakdown. Shown below are the measurements obtained for the winding resistance and the resulting losses. The losses are all reflected to the primary side of the transformer.

The winding loss analysis shows that the winding structures have a very similar loss breakdown because they have very similar AC resistances. The case with the additional secondary winding has a lower secondary loss, but it is offset by the additional loss in the primary winding. One thing to note about these losses is that the winding structures proposed in this work use parallel layers and that this FEA simulation does not take into account the thermal balance of the windings. Thermal balance is the changing resistance of the windings based on temperature. As one of the layers closer to the current source draws additional current because of its lower relative resistance, its temperature raises and so does the resistance of the winding. This will cause the winding layers at equilibrium to carry equal or very similar current current. Shown below is the current breakdown for the winding structures studied in this work. The current is normalized to the lowest primary and secondary current.

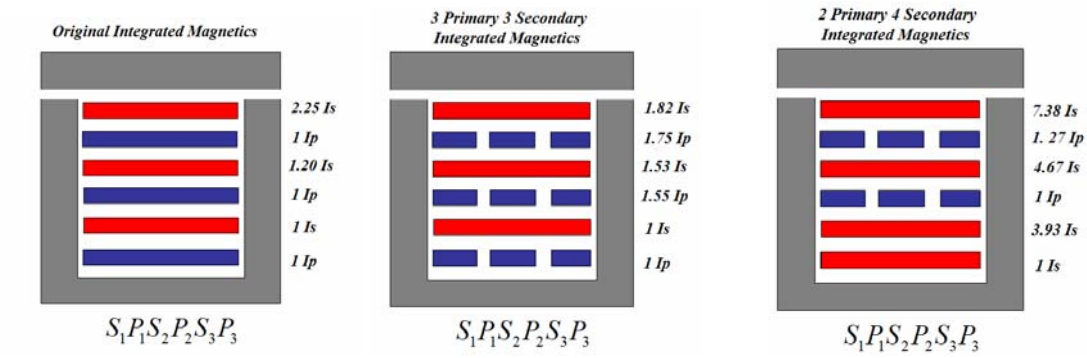


Fig 3.35 Current distribution in the different cases studied

The original design and the three primary three secondary design show similar current distributions in the secondary windings due to similar structure layouts. The two primary four secondary winding case is the outlier in this case. The extra secondary winding that is mapped to no primary winding sees almost no current in this analysis. In

steady state operation this wire would eventually carry more current do to the temperature rise in other windings.

In this section, improved winding layouts were created based on the findings of the previous section. Different designs were created and the benefits of each design were discussed. The leakage inductances were measured and compared to the results obtained from FEA simulation. Also in this section a winding loss breakdown was discussed to take in account for the secondary current which differs in the integrated magnetics design. The final stage of analysis in this work is the experimental results obtained from the hardware to verify the work performed in this thesis.

3.8 Experimental Results and Summary

Having completed all of the theoretical analysis of leakage inductance and winding loss, hardware verification is performed. All of the PCB boards used in this work were 6 layers with 4ounce copper on all layers. The dielectric thickness in between layers was estimated by the manufacturer to be between 5-8 mils between each layer. The devices used in this analysis were 4 Renessas 2168 switches for the full bridge devices, 4 Renessas 2165 switches for the current doubler switches, and National LM2726 drivers for the full bridge MOSFETS.

	Measured Leakage Inductance (nH)	Body Diode Conduction Loss (Io=50, fs=1MHz) (W)
3 Primary 3 Secondary	30.09	1.14
2 Primary 4 Secondary	28.64	1.08
Original 12 Layer Design	38.77	1.58
Original 6 Layer Design	52.49	2.25
Discrete Transformer Design	60	2.61
Single Switch Design	22.29	0.76

Table 3.16 Body diode conduction losses for all cases studied

The analysis from the previous section showed that the main difference between the magnetic designs were the leakage inductance. The winding losses were similar in all cases, but the body diode conduction losses were significantly different. Shown below are the leakage inductances for each setup, the body diode conduction loss, and resulting efficiency drop as a result of body diode conduction. The two designs proposed in this thesis work saved almost 2% of efficiency compared to the original integrated magnetics by reducing the leakage inductance.

Measured Leakage Inductance (nH)	Efficiency Drop From Body Diode Conduction Loss (Io=50, fs=1MHz)
30.09	1.75
28.64	1.66
38.77	2.43
52.49	3.46
60	4.01
22.29	1.17

Table 3.17 Efficiency drop resulting form body diode loss

Shown below is a plot of the efficiency curves obtained for this thesis work. Looking at the 50A operation it can be seen that the efficiency is improved by around 2%, which is what was predicted from analytical analysis. The efficiency of the new magnetic structures are increased even more as the load current is increased above 50A. This increased higher load efficiency is a result of body diode conduction losses and is discussed in chapter 2. The lower light load efficiency is a result of reduced ZVS operation that is caused by reduced leakage. The light load efficiency drop can be corrected by using better and fewer devices. Since devices will improve in the future allowing for the use of fewer devices the light load efficiency is not foreseen to be a significant problem.

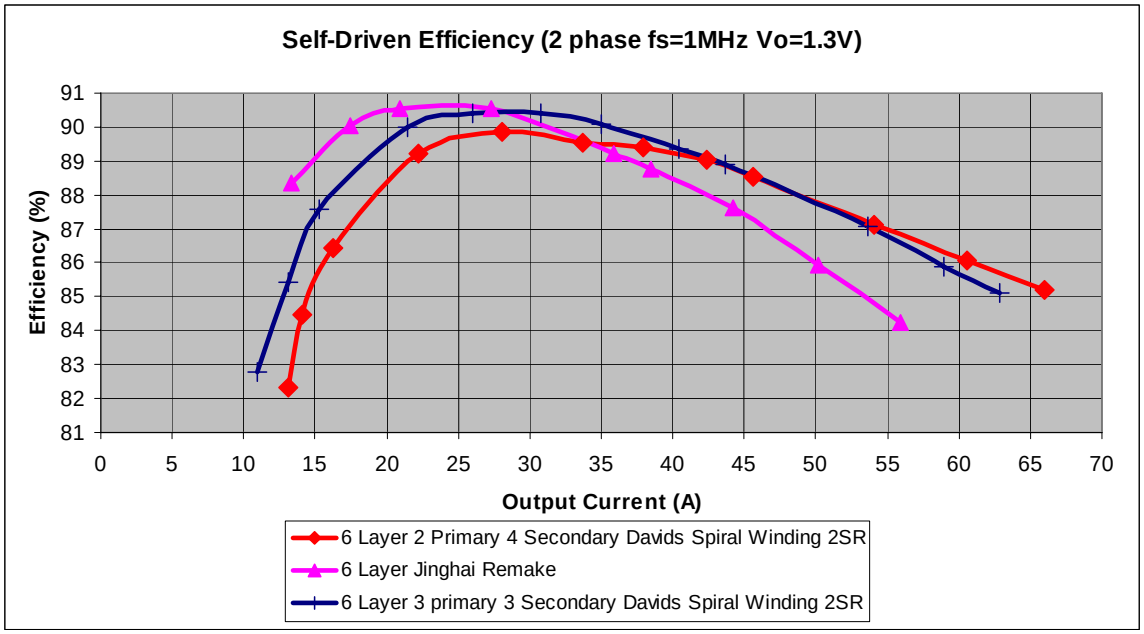


Fig 3.36 Efficiency curves comparing benchmark and new designs presented in this work

This chapter has offered a methodology to analyze the leakage inductance and winding loss in a magnetics structure accurately. Also, improvements are made to the original magnetic design as presented by Dr. Zhou in [3.5]. The end result is a better understanding of leakage inductance, how to control leakage, and how to measure winding resistance. Finally, all of this work is verified with hardware demonstration that results in an improved version of the 12V non-isolated ZVS self-driven scheme.

Chapter 4

Future Work

4.1 Alternate Winding Configurations

The work in this thesis focused on improving the magnetics in the 12V non-isolated ZVS self-driven scheme using the same magnetic footprint size as the original. Limiting the study to the same core area and winding area allowed for a solid foundation of this work which can now be expanded using different cores shapes, core sizes, and winding arrangements. Expanding this work can lead to the best magnetic solution possible for the 12V non-isolated ZVS self-driven scheme.

The first alternate core structure explored was a rounded core. The rounded core shown below was proposed in an attempt to minimize the crowding effect that the corners in the square winding patterns. Reducing the crowding effect using the rounding core is hoped to reduce the overall winding loss. Shown below are the simple single primary and secondary turn cases for the circle core and square core windings.

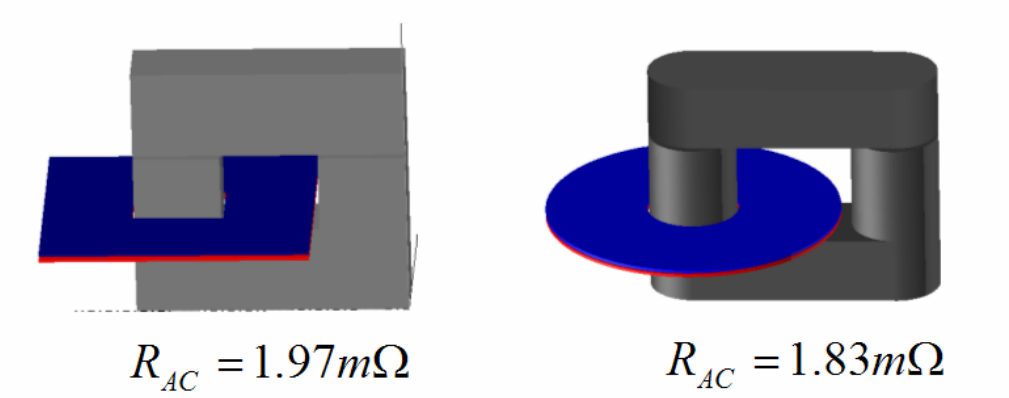


Fig 4.1 AC resistance comparison between square winding and rounded winding

The core volume and window area were maintained to be the same and the result was a lower resistance in the rounded core case than the square case. The current density breakdown for the two cases is shown below. The square windings have more current in the square corners near the inside of the winding and very low current density in the outer corners. The circular core offers a much better current distribution and does not have the same crowding effect that was encountered in the square core design.

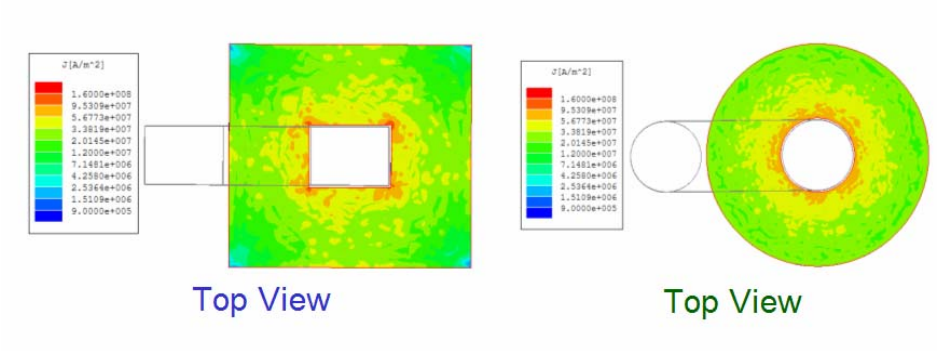
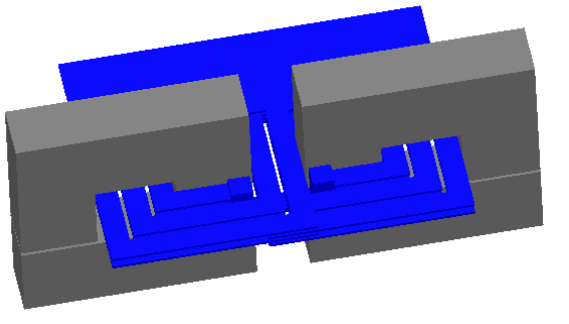


Fig 4.2 Current distribution comparison between square winding and rounded winding

One improvement explored for the spiral winding configuration studied in this work was to use a uniform winding width for all of the conductors. Using this method, the cores could be placed in closer proximity and the secondary loop could be decreased. The result of this winding arrangement is lower leakage inductance and very similar winding resistance. Shown below are the simulation models and the altered primary windings and how it compares to the original design.

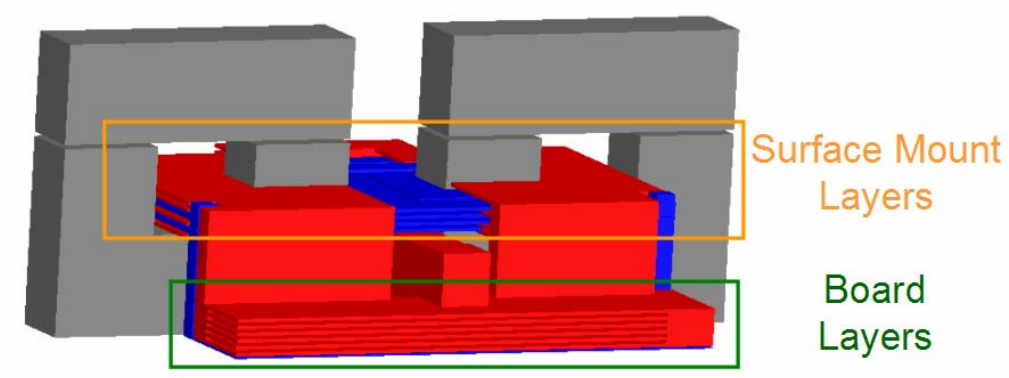


$$L_{k\_original} = 27.53 \qquad L_{k\_future} = 22.46nH$$

Fig 4.3 Leakage inductance comparison between current magnetics and future design

4.2 Surface Mount Magnetic Components

The main future objective is to create a surface mount magnetic structure for the 12V non-isolated ZVS self-driven scheme. Many applications in the VR industry use the VRD design which is embedded into the actual motherboard and has components on one side of the board only. Creating a VRD version would require that the magnetic structure not be embedded into the board like in the VRM case. Moving the magnetics out of the board can offer many benefits to the cost and ease of manufacturing. One major drawback is the leakage inductance resulting from having the winding paths elevated above the board. Preliminary results show that the leakage is increased dramatically.

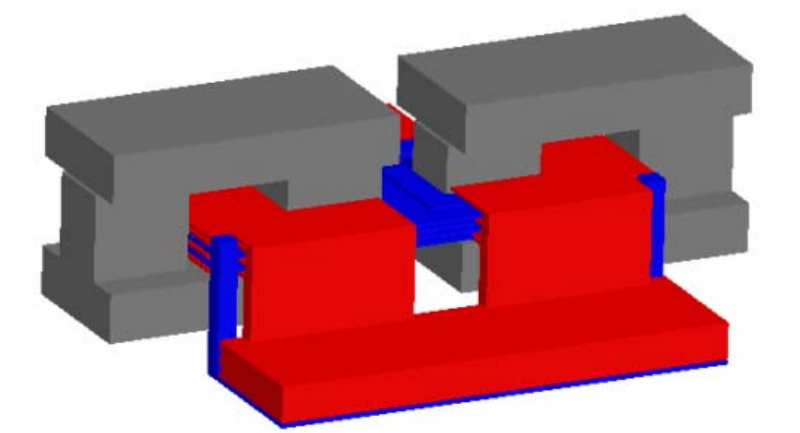


$$L_{k\_Surface\_Mount} = 59.18nH$$

Fig 4.4 Surface mount magnetics using current core design

The first idea to reduce this excess leakage inductance is to use lower profile magnetics so that the windings would be closer to the board. This would also make the core shorter which would give a smaller volume on the board. Shown below is one of the first efforts using lower profile planar magnetics. As can be seen from the simulation results below there is a significant improvement in the leakage inductance of lower profile magnetics. This work is in its beginning stages and careful consideration must be made in regards to the winding layout style and core shape to ensure that the end result

could be packaged as a surface mount component without much complication and cost to the supplier.



$$L_{k\_Low\_profile} = 38.39nH$$

Fig 4.5 Surface mount magnetics using low profile core design

4.3 Coupled Magnetic Solutions

The benefits of coupled inductors have been explored and explained in works like [4.2]. Adapting a coupled magnetic structure in the 12V non-isolated ZVS self-driven scheme would allow for capacitor reduction because of the reduced transient inductance offered by a coupled inductor. One concern facing the use of coupled inductors in this topology is the sensitive leakage inductance conditions. There are different forms of coupling being explored and considered for use. One possible solution [4.3] is a single core solution that achieves coupling through the magnetic structure like the one shown below.

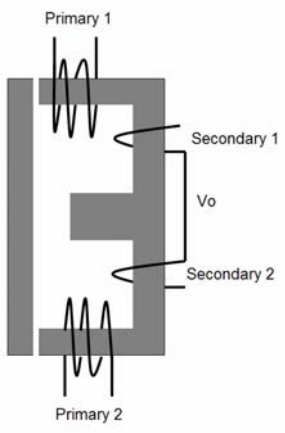


Fig 4.6 Coupled inductor design by Dr. Peng Xu

Another potential way to couple the magnetics would be by using winding based coupling. This idea was presented by Dr. Ming Xu in [4.4] and also in [4.5]. This solution would allow for very low leakage but is a more complex solution. The operation of the coupled inductor used in this topology must be given greater attention before the magnetic solution is chosen.

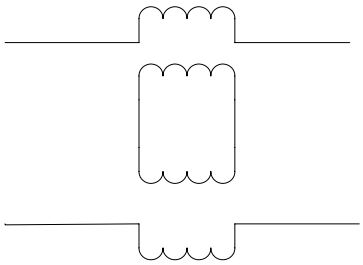


Fig 4.7 Alternate Coupled inductor design

4.4 Alternate Topology Solutions

The analysis in this thesis work used the same circuit design structure throughout. Future versions will explore other options to allow for different winding structures to offer more benefits to the topology performance. One concept being explored is increasing the turns ratio of the transformer. This will reduce the conduction losses in the full bridge and greatly improve efficiency. The drawback of increasing the turns is the

increased effect of leakage inductance. The loop inductance of the secondary is increased by a factor of a squared which makes the leakage inductance design very important. This will lead to more study of the spiral configurations for higher turns and also into matrix transformers. The ultimate goal of the future work is to explore many magnetic options that will allow for optimization not only in the 12V non-isolated ZVS self-driven scheme but in many other applications.

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