A 60 GHz Uniplanar MMIC 4X Subharmonic Mixer

by

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(ABSTRACT)

In this modern age of information, the demands on data transmission networks for greater capacity, and mobile accessibility are increasing drastically. The increasing demand for mobile access is evidenced by the proliferation of wireless systems such as mobile phone networks and wireless local area networks (WLANs). The frequency range over which an oxygen resonance occurs in the atmosphere (~58-62 GHz) has received recent attention as a possible candidate for secure high-speed wireless data networks with a potentially high degree of frequency reuse. A significant challenge in implementing data networks at 60 GHz is the manufacture of low-cost RF transceivers capable of satisfying the system requirements. In order to produce transceivers that meet the additional demands of high-volume, mobility, and compactness, monolithic millimeter wave integrated circuits (MMICs) offer the most practical solution.

In the design of radio tranceivers with a high degree of integration, the receiver front-end is typically the most critical component to overall system performance. High-performance low-noise amplifiers (LNAs) are now realizable at frequencies in excess of 100 GHz, and a wide variety of mixer topologies are available that are capable of downconversion from 60 GHz. However, local oscillators (LOs) capable of providing adequate output power at mm-wave frequencies remain bulky and expensive. There are several techniques that allow the use of a lower frequency microwave LO to achieve the same RF downconversion. One of these is to employ a subharmonic mixer. In this case, a lower frequency LO is applied and the RF mixes

with a harmonic multiple of the LO signal to produce the desired intermediate frequency (IF).

The work presented in this thesis will focus on the development of a GaAs MMIC 4-X subharmonic mixer in Finite Ground Coplanar (FGC) technology for operation at 60 GHz. The mixer topology is based on an antiparallel Schottky diode pair. A discussion of the mechanisms behind the operation of this circuit and the methods of practical implementation is presented. The FGC transmission lines and passive tuning structures used in mixer implementation are characterized with full-wave electromagnetic simulation software and 2-port vector network analyzer measurements. A characterization of mixer performance is obtained through simulations and measurement. The viability of this circuit as an alternative to other high-frequency downconversion schemes is discussed. The performance of the actual fabricated MMIC is presented and compared to currently available 60 GHz mixers. One particular MMIC design exhibits an 11.3 dB conversion loss at an RF of 58.5 GHz, an LO frequency of 14.0 GHz, and an IF of 2.5 GHz. This represents excellent performance for a 4X Schottky diode mixer at these frequencies. Finally, recommendations toward future research directions in this area are made.

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CHAPTER 1
INTRODUCTION

In the past decade, society has become increasingly dependent on the electronic exchange of data for business, personal, and educational purposes. This dependence demands the existence of high-speed data networks capable of supporting a large number of users. Because fiber optic networks offer extremely high data capacities, their existence as last-mile end user connections will undoubtedly increase. Although this will clearly meet the needs of fixed-terminal applications, it will not address society's demands for *mobile* data connectivity. Wireless communication systems offer a convenient and versatile compromise between data capacity and mobility. As a result, we have witnessed the deployment of networks such as Wireless Local Area Networks (WLANs) and Personal Communication Networks (PCNs) [1]-[2]. These systems have typically been operated at frequencies below 20 GHz due to favorable atmospheric propagation characteristics in that frequency range. As the market penetration of wireless data networks increases, demands for greater user capacity may cause frequency bands under 20 GHz to become saturated.

In addition to supporting a greater number of users, the WLANs of the future will demand greater data bandwidth per user. Currently, a typical use for a wireless local area network would be to link Ethernet systems at 10 Mbps. However, the reduction in manufacturing costs of fiber optic network equipment has brought about faster protocols such as 1-Gb Ethernet and it is anticipated that the IEEE will soon approve a 10 Gb Ethernet protocol [3]. In order to provide a large number of users with such high data rates, WLANs will have to utilize a large spectral bandwidth, which will be increasingly difficult to realize at the currently available microwave frequencies (~3-30 GHz). These demands will force system designers and governing agencies such as the FCC to consider the use of high-frequency mm-wave bands for these applications. One band that has received recent attention is the frequency range between 58 and 63 GHz, commonly referred to as the 60 GHz band [4]-[7]. Not only are several GHz of bandwidth available in this band, but there are certain physical properties of mm-

wave terrestrial links in this band which can be used to further improve bandwidth efficiency.

The 60 GHz band is unusual in that it has an atmospheric attenuation peak between 58 and 63 GHz. This is caused by the resonance of oxygen molecules in the atmosphere. For most wireless communication applications, this characteristic causes unacceptable path losses in excess of 13 dB/km [4]. However, short-range terrestrial links may take advantage of this characteristic if the path length is short enough to avoid prohibitively high loss. This offers the advantage that the mm-wave signals do not travel much farther than is necessary to achieve the link. This allows communications systems to operate at the same frequency in relatively close proximity with a greatly reduced risk of mutual interference. An additional benefit of high attenuation is that some measure of security is provided since any transmissions in this frequency band will reach a relatively small coverage area.

For any wireless communication system operating over a large area, *frequency reuse* is a ubiquitous method of maximizing bandwidth efficiency [8]. Cellular telephony systems offer an illustrative example of the design issues involved in frequency reuse. These systems involve the division of the service area into *cells*. The available spectrum is divided into many frequency ranges, with each cell assigned a particular range. The cells using the same frequency range must be spaced far enough apart so that mutual interference does not occur. The more cells which can operate in the same frequency range, however, the greater the overall number of users that can occupy the same spectral bandwidth. Therein lies the advantage of using an air channel with a high path loss. For a cell diameter of 1 km operating at 60 GHz with no oxygen resonance, studies have suggested that a cell separation of 32 km is required in order to achieve a 30 dB carrier-to-interferer rejection ratio [4]. With the additional attenuation due to oxygen resonance, the necessary separation reduces to 2.5 km. The potential system user capacity is therefore increased drastically. In addition to such cellular-type systems, the 60 GHz band also has potential uses in indoor LAN systems. Studies have been conducted which investigate the use of wall

coatings that have high attenuation at 60 GHz. This would introduce the possibility of using the same frequency at several locations simultaneously within a single building.

Other potential applications have been proposed for the 60 GHz band. One interesting possibility lies in roadside assistance links for the Intelligent Vehicle Highway System (IVHS) [5]. This application would benefit from the unique propagation characteristics since roadside beacons could provide localized data about a particular section of highway. It is desirable to limit the coverage area since the information is relevant to only a relatively small area of highway. Finally, the FCC allocation currently specifies that this band is to be used for inter-satellite communications [5]. Since satellites do not operate in the atmosphere, no oxygen attenuation is experienced on cross-links between satellites. Satellite communication system manufacturers as well as wireless LAN and IVHS developers would therefore benefit from the development of highly integrated, relatively inexpensive communications hardware for operation at 60 GHz.

Deployment of such systems at 60 GHz is not a trivial issue. In order for such systems to be competitive with existing approaches, transceiver hardware must achieve a level of integration and cost-effectiveness which is comparable to that found at lower frequencies. Once this has been secured, the road will be paved for the implementation of a low-cost, highly integrated 60 GHz communications system. Such a system could offer a viable solution to the impending demand for greater data bandwidth while maintaining the advantage of mobility.

1.1 Mixers at 60 GHz

One of the greatest difficulties in designing integrated transceiver hardware at 60 GHz band lies in the design of the receiver front end. Recent advances in the design of integrated low noise amplifiers at 60 GHz have made integrated receiver design more feasible [9], [10]. A very difficult task remains, however, in the design of a

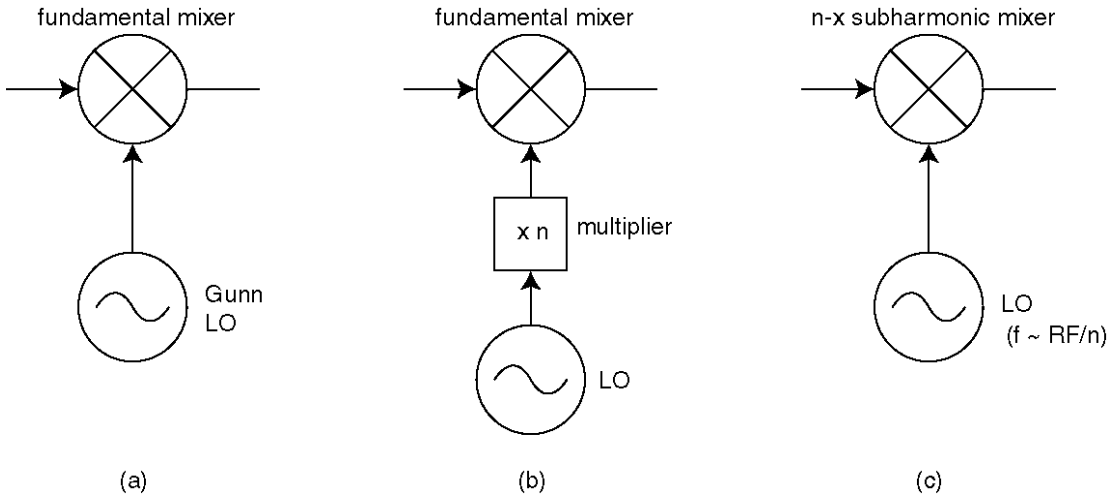


Figure 1.1: Several common methods of mm-wave LO generation, (a) Gunn oscillator, (b) low-frequency LO with *n*-X multiplier, (c) *n*-X subharmonic mixer

high-performance local oscillator to drive the downconversion mixer. The typical method of LO generation has usually been by the use of negative resistance devices such as Gunn or IMPATT diodes [Figure 1.1 (a)]. These devices can provide a superior LO drive level to existing integrated solutions, but require the use of a resonant waveguide cavity with stringent mechanical tolerances. These structures are also bulky and cannot be integrated onto the circuit substrate. Another alternative is to generate a lower frequency oscillator at some integral fraction of the desired LO frequency and using a multiplier chain to achieve the correct frequency at the mixer LO port [Figure 1.1 (b)].

The aforementioned methods of LO generation assume that the mixer is to be operated as a fundamental mixer. This means that the RF signal mixes with the fundamental frequency component of the signal incident at the LO port (Figure 1.2). For example, in order to convert a 60 GHz RF signal to a 2 GHz IF frequency, the appropriate LO frequency for low-side injection would be 58 GHz. At these frequencies, the required LO for fundamental mixing is close enough to the RF frequency to present isolation problems between the RF and LO ports. This can lead to undesired LO radiation and receiver front-end desensitization.

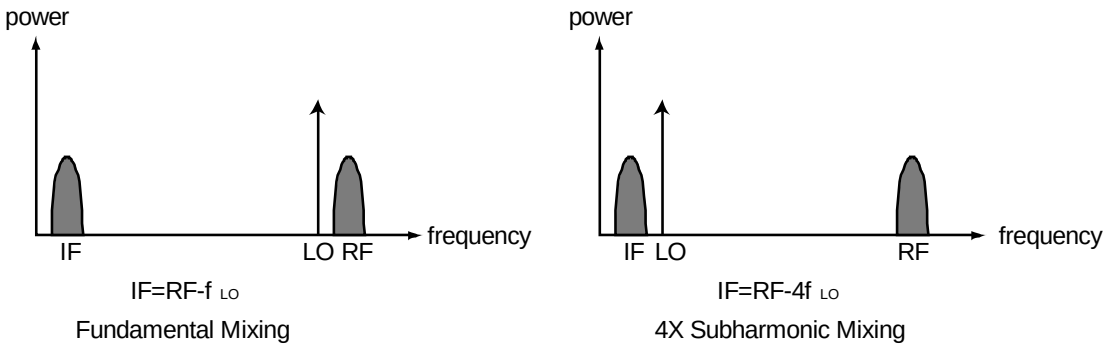


Figure 1.2: Fundamental Mixing vs. Subharmonic Mixing

A practical solution to these problems has been found in the use of subharmonic mixers (Figure 1.1 (c)) [11]. The difference in the operation of a subharmonic mixer and a fundamental mixer is in the frequency applied to the LO port. A subharmonic mixer operates at an LO frequency which is equal to the analogous fundamental LO frequency divided by some integer *n*. For example, in a 4X subharmonic mixer, the IF component is the result of mixing between the RF frequency and the 4^{th} harmonic of the LO (shown in Figure 1.2). In the previous example, for an RF frequency of 60 GHz and an IF frequency of 2 GHz, a 4X subharmonic mixer would operate at 14.5 GHz using low-side injection. This scheme provides adequate frequency separation between the RF, LO, and IF signals, facilitating isolation of those frequencies from one another. This is essentially equivalent to placing a 4X multiplier on the LO input port of a fundamental mixer. Subharmonic mixers, however, have an improved ability over this analogous method to suppress even-order intermodulation distortion and dc offsets. This is of particular interest for application in direct conversion receivers, where dc offsets in mixers due to LO self-mixing are of particular concern [12]. The most prominent disadvantage to using subharmonic mixers is greater conversion loss than that which is found in fundamental mixers. Typical passive 4X subharmonic mixers have losses in excess of 10 dB [11]. Generally, a 3-dB degradation in conversion loss is expected for each increase in the even LO harmonic multiple used in subharmonic mixing. However, the advent of low-noise, high-gain LNAs at 60 GHz allows the use of a relatively lossy mixer for conversion from that

frequency. The advantages gained by the ability to use a lower frequency oscillator offset the disadvantage of higher conversion loss.

In addition, of particular importance to 60 GHz systems is the need to achieve high-performance mixer circuits in an integrated solution. In the past, radio receivers at this frequency have required the use of waveguide sections to connect the individual circuit blocks (mixer, LNA, etc.). Unfortunately, waveguide components are bulky and expensive. In order to meet the demands of practicality for such high-volume applications as indoor WLANs and IVHS, these circuits must become relatively cheap and miniaturized. The answer to this need is found in the use of monolithic microwave integrated circuits (MMICs). Subharmonic mixing facilitates the use of a MMIC front end by enabling the use of a lower frequency integrated oscillator. In designing these MMICs, careful consideration must be given to the transmission line and distributed element topologies to be used. The next section introduces a planar transmission line technology that has received much recent attention – Finite Ground Coplanar Waveguide (FGC).

1.2 Finite Ground Coplanar (FGC) Waveguide

Coplanar waveguide (CPW) technology has found wide acceptance for use in high-frequency transmission lines. Although microstrip is another popular choice for mm-wave MMICs, CPW offers several advantages over microstrip for high-frequency circuit implementation [13]. Many of these advantages are inherent in the physical structure of the lines, i.e. the position of the ground plane (see Figure 1.3 (a)). Some of these advantages are:

- Microstrip technology requires the use of via holes to make connections to the backside ground plane, whereas the coplanar ground conductors in CPW technology obviate this need. The elimination of vias from the fabrication process offers the advantage of potentially lower cost and higher yield.

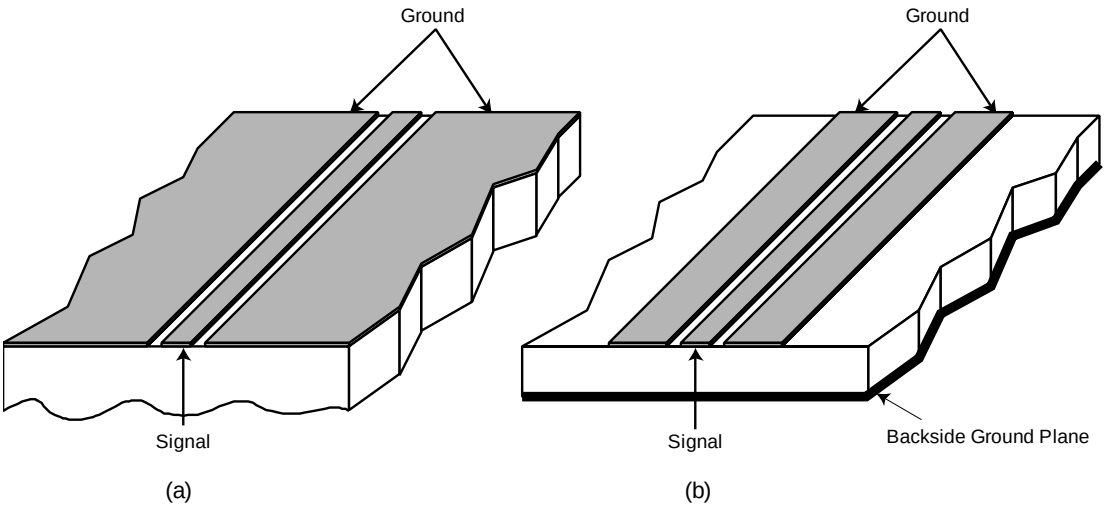


Figure 1.3: (a) Canonical coplanar waveguide (CPW) and (b) finite ground coplanar waveguide (FGC)

- The coplanar ground planes facilitate circuit testing in that the transmission lines are directly compatible with standard ground-signal-ground (GSG) type wafer probes.
- CPW displays less dispersion than microstrip on a given dielectric substrate, enabling quasi-static operation up to very high frequencies.
- In the desired mode of CPW operation (the so-called odd mode), the electric fields between either ground plane and the center conductor effectively cancel in the far field, thereby reducing radiation loss and cross-coupling with other circuits on the wafer.

There are, however, drawbacks to using CPW in many practical applications due to necessary deviations from the canonical topology. As mentioned above, coplanar waveguide in its canonical form consists of a center conductor that is flanked by ground planes on either side (Figure 1.3 (a)) [13]. The coplanar ground planes are infinite in extent and printed on a substrate that has no bottom ground layer. In reality, this is never the case. The ground planes used in coplanar waveguide are truncated at the edge of the IC, or where an adjacent circuit component interrupts the ground plane. If backside metallization is present, or if the circuit is mounted in a

metallized package, the CPW structure may then support a parasitic parallel plate waveguide mode between the upper ground plane and the bottom metal. This can lead to unwanted box-type resonances in the parallel plate mode and cause power leakage from the desired CPW mode [13], [14].

A solution to this problem lies in the use of Finite Ground Coplanar (FGC) Waveguide [15]. In this geometry, the ground plane is truncated to a uniform width for each length of transmission line (see Figure 1.3 (b)). This transmission line type has been shown to be successful in suppressing the parallel plate waveguide mode, while having only slightly greater attenuation than conventional coplanar waveguide. The suppression of the parallel plate mode is extremely important to the proper operation of CPW and its variants. It is therefore desirable to use a transmission line type that will suppress the parallel plate waveguide mode while preserving the inherent advantages of CPW. The FGC structure will be explored further in Chapter 2.

1.3 Objective

The objective of the work presented in this thesis is the development of a 4X subharmonic downconverter for the 60 GHz band. This circuit is intended for future integration with an on-chip LO and LNA in an integrated receiver front-end MMIC. The IF of the circuit is between 2 and 3 GHz to allow the use of current RFIC technology for IF processing. The performance objective of this design is to offer conversion loss competitive with currently available 60 GHz passive mixers. A comparative analysis of the advantages and disadvantages of subharmonic mixing vs. fundamental mixing is made.

Implementation of this mixer design includes the use of finite ground coplanar waveguide transmission lines on a gallium arsenide substrate. These lines are thoroughly characterized through electromagnetic simulations and measurements.

Shunt and series tuning elements available in this transmission line structure and their performance are investigated.

1.4 Overview of Thesis

This thesis consists of six chapters. Chapter 2 develops the theory and design considerations necessary for the finite ground coplanar waveguide technology to be used in the mixer implementation. Simulation results based on these are presented and explained for a wide range of possible transmission line dimensions. A particular FGC configuration is defined as the standard transmission line for the mixer application based on its simulated performance in the MMIC technology available for circuit fabrication.

Chapter 3 explains the theoretical operation of subharmonic mixers, focusing on antiparallel diode mixers. A specific mixer circuit topology is proposed and simulated using ideal distributed circuit elements. These ideal elements provide target performance specifications for the various FGC stubs to be fabricated for MMIC implementation. In Chapter 4, the design of these FGC stubs is completed and simulated based on the available fabrication technology. The simulated performance is evaluated and compared to the performance of actual fabricated stubs.

Chapter 5 combines the concepts developed in each of the previous chapters in the implementation of an integrated mixer based on a conventional GaAs MMIC process. Test results are presented and circuit performance compared with simulated results. The relevance of these results in the context of modern 60 GHz mixers is summarized in Chapter 6. Future research directions stemming from this work are suggested in this chapter as well.

CHAPTER 2
FINITE GROUND COPLANAR WAVEGUIDE

The performance of coplanar waveguide transmission lines with truncated ground planes has recently been the subject of extensive research [15]-[17]. This transmission line type, referred to as finite ground coplanar waveguide (FGC), has exhibited promising performance for application in mm-wave integrated circuits. The low loss, low dispersion, and inherent parasitic mode rejection found in FGC lines make them particularly well suited for use in the proposed 60 GHz subharmonic mixer. For these reasons, a thorough study and characterization of these lines is made. This chapter focuses on the theory of operation for FGC lines, as well the design and simulation of the lines for operation on the mixer integrated circuit substrate.

In order to illustrate the advantages or disadvantages of any particular transmission line structure, it is beneficial to first consider the IC process in which it is to be fabricated. Semiconductor substrates are generally populated on the upper side by transmission lines and other circuit elements. The bottom side of the substrate is often directly adjacent to a metal layer. This metal layer is either metal in the IC package to which the die is fastened, or plated metal on the bottom side of the die, sometimes called backside metallization. This metal helps conduct heat from the substrate and provides structural strength, or may serve as the ground plane for microstrip transmission lines. In circuits that include coplanar waveguide, however, backside metallization is not necessary for signal propagation and may actually cause the transmission line to support additional parasitic modes [17].

In its canonical form, the CPW ground plane is unbounded in extent in either direction tangent to the center conductor [Figure 1.3 (a), 2.1 (a)] [15]. This is obviously not physically realizable. In most CPW circuit layouts, it is adequate to cover the areas of the substrate surface not occupied by transmission lines or circuit elements with ground conductor. This is usually a reasonable approximation of an

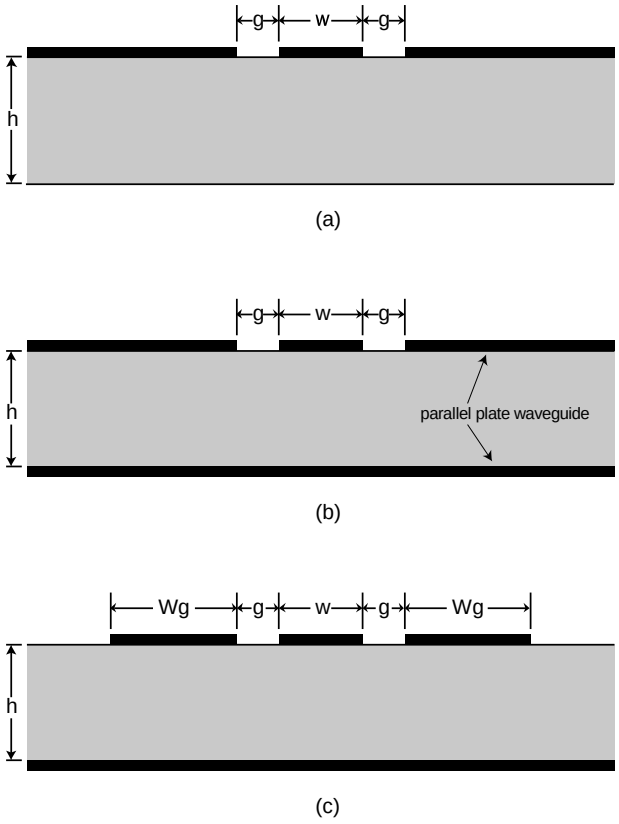


Figure 2.1: Canonical coplanar waveguide (a), coplanar waveguide with lower ground plane (b), and finite ground coplanar waveguide (c).

unbounded ground plane in terms of circuit performance. The majority of high-frequency current conduction in the ground conductors takes place at their inner edges, parallel to the center conductor. Therefore, the outermost extents of the ground conductors do not contribute significantly to the line characteristics. This does introduce a problem, however, in that the upper ground plane and lower ground plane constitute a parallel plate waveguide structure, as shown in Figure 2.1(b) [17]. Since the geometry of the ground plane is designed around the surface circuit components, its boundaries are somewhat arbitrary. This makes its electrical characteristics at high frequencies difficult to characterize at best. It is therefore a complex task to predict if any box-type parallel plate resonances could be excited under these conditions. If such resonances occur, power is drawn from the CPW mode, resulting in a degradation in the transmission coefficient of the line at the resonant frequency. A common method of suppressing the parasitic mode is to use

vias to connect the CPW upper ground plane and the bottom metal plane [15]. These vias short the metal planes together, eliminating the parallel plate waveguide mode. This method, however, obviates one inherent advantage of coplanar waveguide, i.e. the elimination of grounding vias between the upper and lower metal planes. Therefore, an alternative method of suppressing the parallel plate mode would be highly preferred.

An answer to this problem lies in the use of a uniformly truncated ground plane for all CPW transmission lines [Figure 1.3 (b), 2.1 (c)]. Truncating the ground planes to an overall structure width ($w+2g+2Wg$) less than one quarter of a dielectric wavelength ($\lambda_d/4$, where $\lambda_d = \lambda_o/\varepsilon_r^{1/2}$) at the highest frequency of interest guarantees that no parallel plate resonance will be excited below that frequency [15]. While narrower ground planes offer this advantage, they also significantly affect the characteristic impedance and attenuation of the line [17]. For example, the characteristic impedance of a conventional CPW transmission line is determined solely by the ratio of center conductor width to overall slot width [13]. In FGC lines, line attenuation and characteristic impedance are changed slightly by altering the width of the ground conductors. Therefore, the available models for CPW lines in circuit simulation tools such as EEsof LineCalc [18] have limited use for the design of FGC lines. However, a very accurate simulation of transmission line characteristics may be obtained from currently available full-wave electromagnetic simulation software using the method-of-moments, finite element method, or other suitable technique.

2.1 Design of FGC Lines

When designing FGC lines, the physical dimensions must be carefully chosen so that properties such as characteristic impedance (Z_o) and line attenuation (α) are suitable to the application. The dimensions of lines with these characteristics will vary with the type of substrate to be used. The substrate thickness (h) must be taken into account during CPW/FGC line so that coupling to the lower ground plane (microstrip mode) can be avoided. For this reason, substrate properties such as thickness (h) and

relative dielectric constant (ε_r) directly affect all important transmission line parameters. The MMIC fabrication process must therefore be established before any FGC lines are designed. For the proposed 60 GHz mixer, a 125 μm thick gallium arsenide substrate is used. The process associated with this substrate features 4.5 μm thick gold conductors atop a 0.8 μm passivation layer of SiN that covers the GaAs substrate. This process was chosen based on its availability for this research and its support of a standard schottky mixer diode.

The FGC line dimensions were designed to provide the desired value of characteristic impedance while providing a reasonably low value of line attenuation. For this application, a characteristic impedance (Z_o) of 50 Ω was chosen for compatibility with standard RF systems and test equipment. For FGC lines, Z_o is largely determined by the ratio of the center conductor width (w) to the overall slot width ($w+2g$), but is affected to a lesser degree by the ground conductor width (W_g). For the sake of design simplicity, W_g for the lines used in this experiment was fixed to equal to the overall slot width, $w+2g$. This design has been shown to provide line attenuation comparable to that found in CPW lines [15]. Using these guidelines, specific characteristic impedance values were achieved for a given center conductor width (w) by varying the overall slot width ($w+2g$) and the corresponding ground plane width (W_g). The dimensions for a 50 Ω line can then be determined through simulations for a wide range of center conductor widths.

The range of practically feasible center conductor widths is bounded at the low end by line attenuation [17]. Center conductor width has an inverse relationship with the line attenuation. The maximum acceptable level of attenuation depends on the particular circuit design requirements. The upper bound on practical center conductor widths may be due to one of two factors [14]. The first is that a larger center conductor width would result in a value of $w+2g$ that could violate the rule of thumb regarding overall line width and the excitation of the parallel plate mode (overall structure width $< \lambda_d/4$ at the highest frequency of interest). The second issue has to

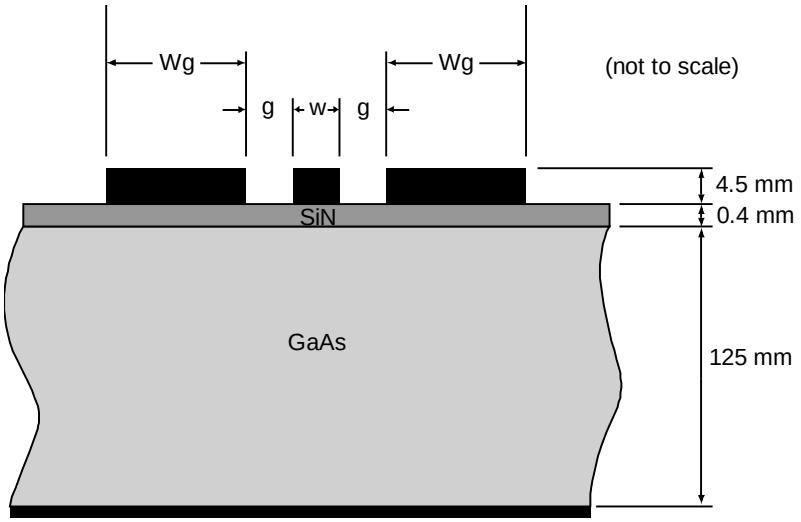


Figure 2.2: Simulated FGC substrate dimensions

do with the excitation of a parasitic microstrip mode. This mode becomes excited due to coupling between the center conductor and the lower metal plane. If the center conductor is too wide relative to the substrate thickness, coupling to the bottom ground plane can become more dominant than coupling to the coplanar ground planes. The transmission line no longer operates in a pure CPW mode, but rather in what is called a coplanar microstrip, or CPM mode. Which upper bound dominates depends on the particular substrate thickness and material and must be determined experimentally or by simulations.

2.2 Simulated Results

The FGC transmission lines were characterized using Zeland IE3D electromagnetic simulation software [19]. The substrate dimensions used for simulations are shown in Figure 2.2. Simulations were carried out for FGC lines on this 125-μm thick gallium arsenide substrate with a relative permittivity of 12.9 and a loss tangent of 0.006. Atop the substrate is a layer a 0.4 μm thick SiN layer with a relative dielectric constant of 7 and a loss tangent of 0.002. The transmission line structures were simulated as 4.5 μm-thick gold conductors atop the SiN layer. A range of center conductor widths were simulated. The design process began with the choice of a

w (μm)	g (μm)	W_g(μm)
10	4.5	19
20	11	42
30	15	60
40	23	86
50	29	107
60	38	136
80	58	195

Table 2.1: Simulated FGC line dimensions for 50 Ω characteristic impedance.

particular center conductor width *(w).* Slot widths *(g)* were then chosen for a 50-Ω characteristic impedance and

the ground plane widths (W_g) were set equal to the overall slot and center conductor width ($w+2g$). For each set of dimensions, the characteristic impedance (Z_o), line attenuation (α), and effective permittivity (ε_{eff}) were determined. Table 2.1 shows the dimensions of 50 Ω lines for various center conductor widths. Figure 2.3 is a plot of the characteristic impedance and line attenuation for various ratios of w to W_g for FGC lines on the defined substrate. Figure 2.4 shows a plot of α vs. frequency for various center conductor widths for 50 Ω FGC lines. The simulated effective permittivity of FGC lines with various center conductor widths is shown in Figure 2.5. Each of these plots is useful in determining the optimum dimensions for 50 Ω FGC transmission lines for the given substrate.

The rule of thumb for parallel plate mode suppression suggests that the overall line width should be less than a quarter dielectric wavelength at the highest frequency of interest. For a maximum operating frequency of 70 GHz, the overall line width should be less than 300 μm. This corresponds to a maximum center conductor width of 40 μm, according to the dimensions determined in Table 2.1. In order to verify that the choice of W_g results in line attenuation comparable to that of CPW, a study into the effects of the ratio of ground conductor width to center conductor width (W_g/w) on line characteristics was made. According to simulations, the effective

dielectric constant remains approximately constant over nearly all ground plane widths, but the characteristic impedance and line attenuation change rather dramatically as W_g/w is varied. The results of these simulations are shown in Figure 2.3. These results show a similar trend in line attenuation as observed by Ponchak and Katehi in [15]. From these results, the decision to set the ground plane width W_g equal to $w+2g$ may be evaluated. For a 40 μm center conductor, the ground plane width for a 50 Ω line was determined to be 86 μm, resulting in a W_g/w ratio of 2.15. Figure 2.3 shows that this ratio is near the asymptotic minimum attenuation as W_g/w approaches infinity. From this, it can be inferred that the line attenuation of this line is approximately equal to that of a canonical CPW line, suggesting that this choice of W_g is acceptable.

The optimum center conductor width was found to be 40 μm. This choice is based on several factors. Figure 2.4 indicates that this width provides relatively low line attenuation compared to narrower center conductors. In addition, any 50 Ω FGC line with a larger center conductor is in danger of exciting a parallel plate mode. A 40 μm line width is well suited for the intended application in terms of spatial compactness, low line attenuation, and low dispersion. Dispersion, a deviation in phase velocity over frequency, is evidenced by similar variation in ε_{eff} over frequency. The flatness of the simulated effective permittivity (ε_{eff}), shown for each center conductor width (w) in Figure 2.5, verifies low dispersion for the 40 μm FGC lines. This simplifies the calculation of electrical length (EL) of a given physical length of transmission line simpler since guided wavelength is related to frequency by the formula:

$$\lambda_g = \frac{c}{f\sqrt{\varepsilon_{eff}}}, \tag{2.1}$$

where c represents the speed of light and f represents frequency; $EL=L/\lambda_g \bullet 360°$.

The standard dimensions for a 50 Ω transmission line in this thesis shall henceforth be defined as a center conductor width (w) of 40 μm, a slot width (g) of 23 μm, and a ground plane width (W_g) of 86 μm. These lines will be employed in Chapter 4 for

various distributed stub and filter structures for applications in a MMIC 4X subharmonic mixer.

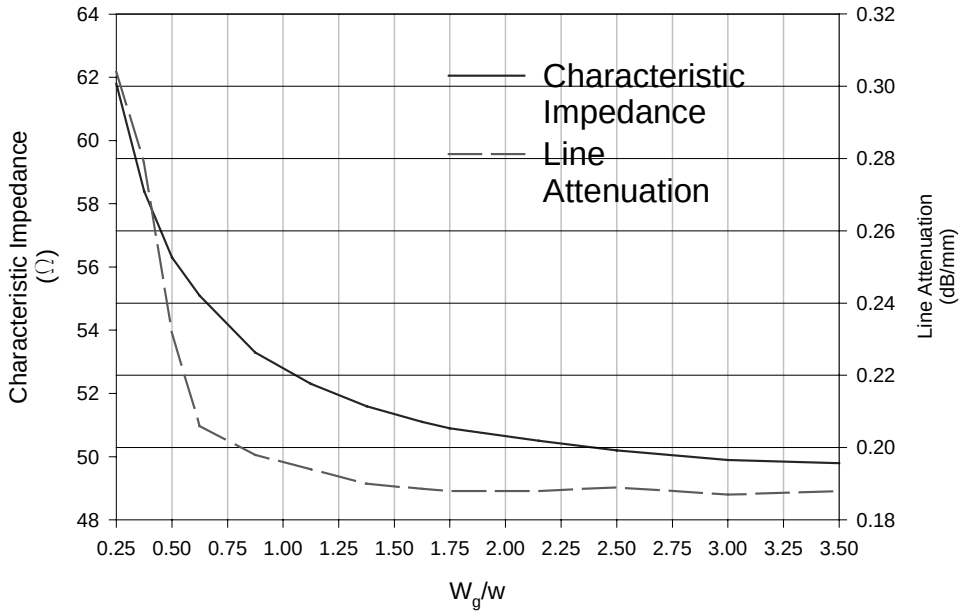


Figure 2.3: Simulated line attenuation and characteristic impedance vs. ratio of ground plane width (W_g) to center conductor width (w) for w=40 μm, g=23 μm

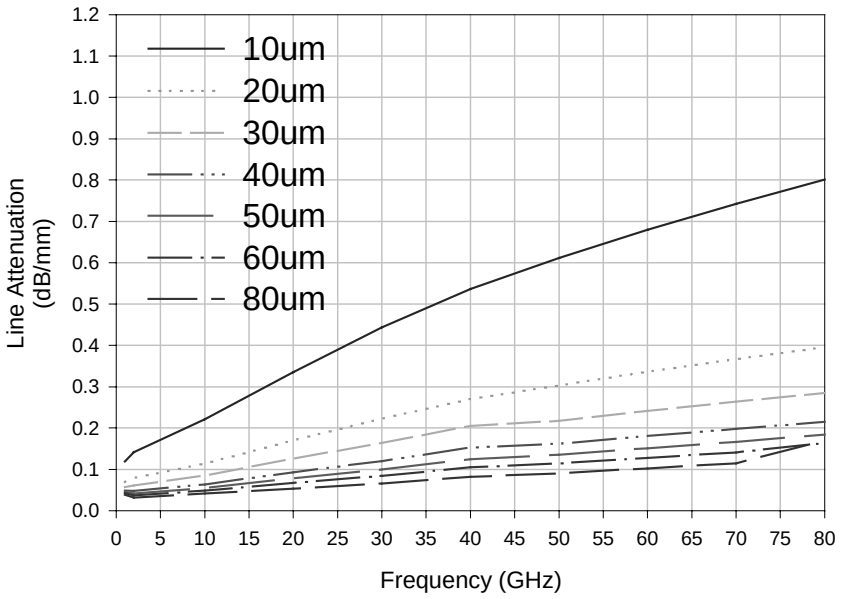


Figure 2.4: Simulated line attenuation vs. frequency for various center conductor widths

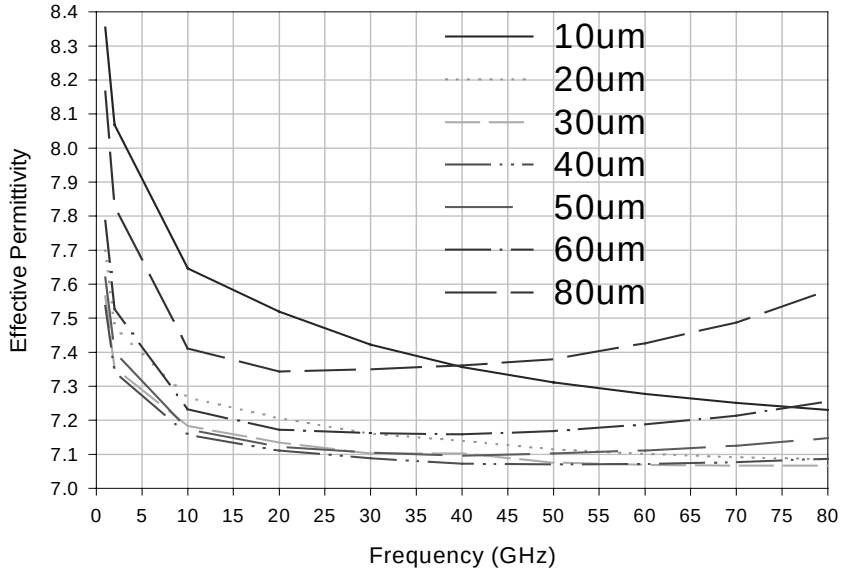


Figure 2.5: Simulated effective permittivity vs. frequency of FGC lines for various center conductor widths

CHAPTER 3
4X SUBHARMONIC MIXER DESIGN AT 60 GHZ

A high-performance receiver is a vital component of a high-speed wireless communication system. The quality of the received signal has a direct impact on the achievable data rate, the most important standard by which modern communication systems are evaluated. The receiver *front-end* plays a dominant role in determining the received signal quality. The term front-end typically refers to the low-noise amplifier (LNA) and the first downconversion mixer, as well as any interstage filtering components. Achieving the necessary performance from the low-noise amplifier and the first conversion mixer is often the most challenging task facing the designer. These components operate at the highest frequencies in the receiver chain, and the performance of nearly all active devices is known to degrade as frequency increases. Since high-frequency device technology is continues to improve, the methods used to achieve the necessary front-end performance must adapt to take full advantage of the latest technology. In this manner, improvements in the performance of individual front-end components will result in better overall receiver performance.

The most important performance metrics for low-noise amplifiers are largely self-evident. The purpose of this block is to amplify the signal without significantly degrading the signal-to-noise ratio. Therefore, high gain and low noise figure are the most desirable qualities in an LNA. In addition, front-end components must usually be highly linear to minimize intermodulation distortion (IMD) from high-power interfering signals at the receiver input. These performance concerns are important in mixers as well. Basic receiver theory dictates that for a given overall noise figure, higher gain in the first stage relaxes the required noise figure of the subsequent stages. Passive mixers have a noise figure roughly equivalent to their conversion loss, so a high-gain LNA may then allow a higher conversion loss in the mixer stage without significantly degrading receiver noise performance. In the past, LNA performance at mm-wave frequencies has been so poor in some cases as to lead

designers to eliminate it from the receiver chain altogether. However, recent advances in MMIC technology have made high-gain LNAs feasible at 60 GHz and above [9], [10]. This offers greater freedom in the choice of mixer, since mixers may be implemented in a wide variety of circuit topologies with attendant advantages and disadvantages. Typical mixer conversion gain may range from roughly –10 to 10 dB, depending on the circuit topology chosen.

Low mixer conversion loss is heavily dependent on the power of the LO signal. For all mixers, optimum conversion gain will occur within a particular range of LO power levels (typically somewhere between 0 and 15 dBm). Outside this range, mixer conversion gain degrades drastically. The output power available from an oscillator circuit depends on the available gain of the active device. As noted before, active device gain typically decreases with increased frequency. This effect causes a significant impediment to the development of high-power oscillator sources at mm-wave frequencies, necessitating the use of very high-performance active devices. In the past, Gunn diode oscillators have been the favored method of LO generation for 60 GHz applications. Oscillator topologies based on these devices display excellent output power, phase noise, and $1/f$ noise properties [20], [21]. Unfortunately, their optimum configuration requires a resonant waveguide cavity. These cavities are both bulky and relatively expensive and cannot be integrated onto a monolithic substrate. It is possible to implement Gunn diode oscillators using integrated planar resonant circuits [20]. This approach is limited, however, by the poor DC-to-RF efficiency of Gunn diodes, which results in a significant amount of power dissipated as heat [22]. This may cause excessive temperatures that prohibit the use of the device toward a feasible integrated solution by introducing temperature stability issues. As a result, much recent research has been devoted to the development of high quality integrated oscillators at mm-wave frequencies using more efficient active devices. The most successful results have been seen in heterojunction bipolar transistor (HBT) oscillators and high electron mobility transistors (HEMTs) [22]-[29]. These circuits have displayed output power and phase noise characteristics that may be feasible for use with high-performance 60 GHz receivers.

An alternative to the above methods is to employ an LO signal at some integer fraction 1/*n* of the required fundamental LO frequency [Figure 1.1 (b)]. The LO signal may then be fed through an *n*·X frequency multiplier chain which raises the frequency to the equivalent fundamental LO frequency. Since this scheme calls for a relatively low frequency oscillator, it is easier to obtain higher output power and lower phase noise than oscillators at the fundamental frequency. If the increase in available oscillator power at the lower frequency is large enough to offset the overall loss in the frequency multiplier chain, this solution works well. Although the phase noise of oscillators at lower frequencies is typically better, frequency multiplication has the effect of increasing the phase noise of the output signal at a given frequency offset by a factor of *20·log(n)*, where *n* is the multiplication factor [30]. This effect must be considered in receiver design since the phase noise in the LO signal may contribute to mixer noise figure.

3.1 Subharmonic Mixers

As discussed above, the recent improvements reported in the performance of mm-wave LNAs permit the use of mixers with relatively high conversion loss in 60 GHz receivers. One type of lossy mixer that could be useful in this application is the subharmonic mixer. Subharmonic mixers (SHMs), like other mixers used in receivers, are used to convert an RF carrier to a lower intermediate frequency (IF) at which demodulation or further downconversion may occur. The difference between a subharmonic mixer and a fundamental mixer is in the frequency required at the LO input port to achieve frequency conversion from RF to the desired IF. A fundamental mixer is used to produce an IF frequency that is equal to the difference between the RF and local oscillator (LO) signal frequencies. This is described by the equation:

$$f_{IF} = \left| f_{RF} - f_{LO_{fundamental}} \right|. \tag{3.1}$$

Subharmonic mixers may be used to achieve the same frequency conversion as a fundamental mixer, but the frequency of the signal applied to the LO port is at a

fraction 1/*n* of that supplied to a fundamental mixer's LO port. The analogous description to Equation 3.1 for an *n*·X subharmonic mixer is given by:

$$f_{IF} = \left| f_{RF} - n \cdot f_{LO_{subharmonic}} \right|. \tag{3.2}$$

It is the reduction in the applied LO frequency by a factor of *n* which gives SHMs their principal advantage. The operation of these mixers is equivalent in the above formula to using a lower frequency LO source with an *n*·X multiplier on the LO line, as described in the previous section. Subharmonic mixing, however, offers several additional performance advantages over the LO multiplication technique.

Another benefit of reduced LO frequency is greater frequency separation between the RF and LO frequencies. For example, a fundamental mixer with an RF of 60 GHz and an IF of 2 GHz would require an LO frequency of 58 GHz (low-side injection). It is difficult to distinguish these signals with practical bandpass filters since they are very close in frequency and require filters with very narrow bandwidths in order to achieve adequate isolation between the RF and LO paths. This isolation is very important since excessive LO leakage to the RF port could degrade receiver performance. Since the LO signal level is so much larger than the received RF signal level, any leakage can cause problems such as receiver desensitization and undesired LO radiation. A 60 GHz 4X subharmonic mixer with a 2 GHz IF requires an LO frequency of 14.5 GHz. With this frequency scheme, each signal can be filtered at its respective port where additional isolation is necessary.

In addition to poorer conversion loss, subharmonic mixers have two notable inherent performance disadvantages in comparison to fundamental mixers. The linearity of subharmonic mixers is known to be lower than that achievable with fundamental mixers [11]. This could cause problems in a high-interference environment. Signals outside of the desired channel may cause intermodulation distortion products that fall inside the desired channel bandwidth. This may degrade sensitivity and the receiver's resilience to interfering signals at the receiver input. Fortunately, the high

atmospheric attenuation at 60 GHz may relax the upper dynamic range requirements of the receiver due to lower power levels at the receiver antenna. The linearity requirements of individual receiver blocks are almost always governed by the system upper dynamic range requirements. Therefore, the linearity required from individual receiver components is likely to be lower than would normally be expected. A second disadvantage is the increase of effective phase noise in the mixer for a particular offset due to effective LO multiplication [30]. This factor of phase noise degradation ($20 \cdot log(n)$) is identical to that described for the LO multiplication technique, where n is the LO multiple used in subharmonic mixing. However, in a comparison of effective phase noise due to subharmonic mixing with a modern 15 GHz integrated oscillator vs. phase noise of a modern integrated 60 GHz oscillator (required for fundamental mixing), the subharmonic mixer will generally provide an overall lower noise contribution to the receiver than in the fundamental case due to poor phase noise in 60 GHz oscillators.

3.2 Mixer Implementation

Subharmonic mixing, like fundamental mixing, is achieved by applying an RF signal to a non-linear device that is "pumped" into its nonlinear region by a large LO signal. The nonlinear behavior of the device causes many multiples (harmonics) of the two signals (RF and LO) to be generated. Intermodulation products appear at the sum and difference frequencies of these various harmonics of the RF and LO signals (e.g., $|2\omega_{LO} \pm \omega_{RF}|$, $|4\omega_{LO} \pm \omega_{RF}|$, etc.). The desired product, the IF signal, is then extracted at the appropriate frequency. The difference between subharmonic mixing and fundamental mixing is in the choice of which IM product serves as the IF signal. A suitable subharmonic mixer circuit is any one in which the amplitude of the product of the n^{th} LO harmonic and the RF signal is large enough to result in an acceptably low conversion loss. SHMs have been realized using a variety of active and passive topologies. The nonlinear device configuration most commonly used for subharmonic mixing has been the antiparallel diode pair, shown in Figure 3.1(a) [11]. Successful results in this topology are well documented [31]-[38]. The diode pair

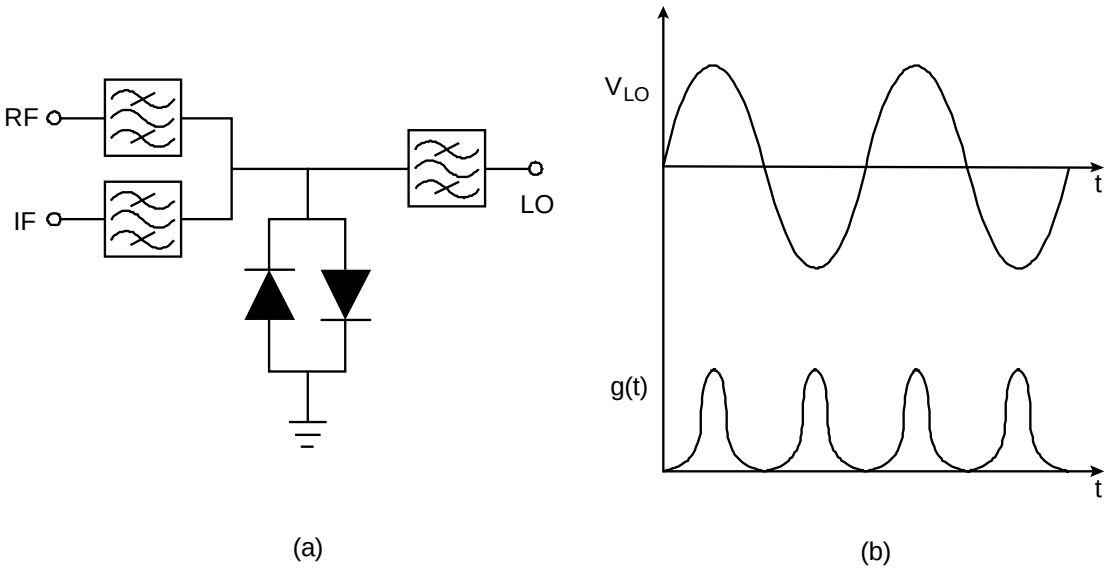


Figure 3.1: (a) Generic antiparallel diode subharmonic mixer (b) Local oscillator voltage waveform and diode pair conduction waveform vs. time.

shown here is connected in a shunt configuration with each signal path (RF, LO, and IF) connected to the same node.

This configuration is particularly amenable to subharmonic mixer applications due to inherent rejection of the fundamental mixing mode. In general, a subharmonically pumped mixer still generates a fundamental IF mixing component as described by Equation 3.1. For a single-ended diode mixer, this component comprises most of the converted RF power, which represents a loss mechanism to the subharmonically converted products [11]. The antiparallel diode mixer alleviates this problem by providing rejection of the fundamental mixing product. This can be seen by an analysis of the diode pair conduction waveform resulting from a symmetrical LO voltage waveform (Figure 3.1(b)). Conduction occurs on both the positive and negative portions of the LO voltage cycle, resulting in two identical conduction pulses for each cycle. Thus, the lowest frequency component present in the conduction waveform is exactly twice the LO frequency. The resulting large signal voltage over the diode pair now only contains the second LO harmonic and its multiples. Therefore, all fundamental and subharmonic mixing products due to odd multiples of the LO frequency are suppressed. This results in the conversion of more

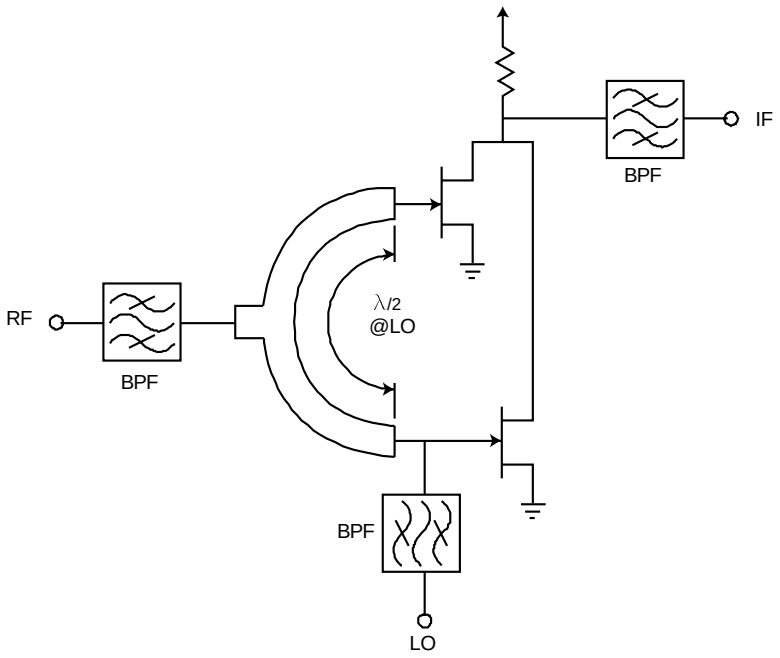


Figure 3.2: Resistive FET Subharmonic Mixer

RF power to subharmonic mixing products resulting from even LO multiples [11]. Consequently, a reduction in subharmonic conversion loss is achieved by eliminating the unwanted fundamental and odd LO multiple subharmonic conversion products. From this argument, it follows that the diodes must have nearly identical I-V curves for symmetric conduction of the diode pair. Any asymmetry in diode conduction results in a first LO harmonic frequency component in the conduction waveform. This represents the dominant mechanism in degrading the rejection of the fundamental response.

It is possible to achieve fundamental response rejection from transistor based subharmonic mixer circuits, as well. Any mixer topology that has a symmetric conduction waveform for an applied LO source will provide the same benefit. This has been implemented in the past using two parallel common-drain configured field-effect transistors (FETs) as a resistive mixer [38], as shown in Figure 3.2. The LO signal is applied to one gate and fed to the other gate via a transmission line with a 180 degree phase delay at the LO frequency. This ensures that the overall conduction

I_s (pA)	$R_s(\Omega)$	η	τ(ps)	C_{jo}(fF)	φ_{bi}(V)	E_g (eV)	BV (V)	I_{bv}
0.2	17.6	1.25	1.0	13.5	0.73	1.43	-7	200

Table 3.1: M/A-COM MSAG 5 Schottky mixer diode model parameters

waveform created by the LO is symmetric- that is, the circuit conducts on both the positive and negative portions of the LO cycle. A potential problem with this design is that the 180 degree delay line introduces loss to the LO signal, introducing asymmetry into the diode conductance waveform. The fundamental mode rejection for this subharmonic mixer topology will then be theoretically worse than with an antiparallel diode pair.

3.3 Mixer Design

Based on circuit simplicity and demonstrated success, an antiparallel diode configuration was chosen for implementation of the proposed 4X subharmonic mixer. Figure 3.3 shows the mixer schematic. The circuit is intended to operate at RF frequencies of 58-62 GHz with an IF frequency of 2.5 GHz and LO frequencies of 14-15 GHz (low-side injection). The circuit design is based on the Schottky mixer diodes in the M/A-COM MSAG 5 mixer diode implant (MDI) process. The diode model parameters for these devices were obtained from the foundry and are shown in Table 3.1.

The mixer schematic shown in Figure 3.3 includes the antiparallel diode pair, as well as various coupling networks. Each of these coupling networks serves several important purposes. At the RF port, a series bandpass filter connects the RF input port to the diode pair. This filter must present an open-circuit at IF so that no downconverted power leaks back through the RF port instead of to the mixer IF port. Conversely, it is important that all incident RF power be directed to the diodes from

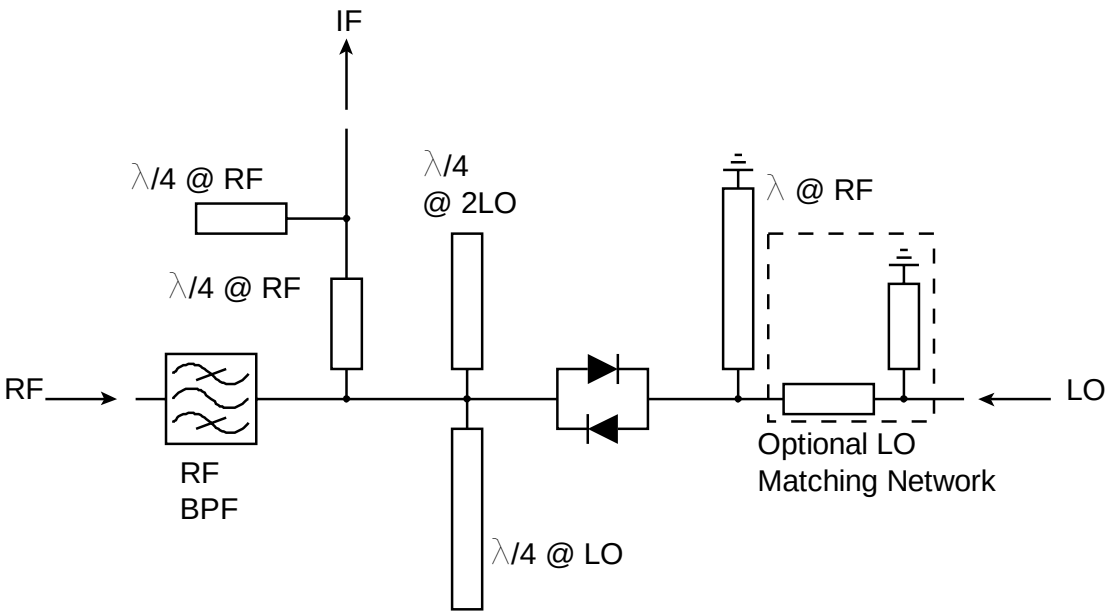


Figure 3.3: 60 GHz 4X subharmonic antiparallel diode mixer

the RF port and not allowed to leak through the IF port. This is accomplished by adding an open-circuited shunt stub of length $\lambda_g/4$ at RF to the IF line. This presents an RF short circuit at the junction with the IF line, but the stub is electrically short enough at the IF such that it presents a shunt open-circuit at this frequency, allowing the IF signal to pass with no loss of power. This shunt stub is connected to the RF feed point by a $\lambda_g/4$ at RF transmission line, which transforms the short-circuit to an open-circuit at RF. The IF coupling network therefore appears transparent at the IF frequency without loading the RF signal at its input to the diode pair. At the point where the IF coupling network and the RF bandpass filter connects to the diode pair, additional shunt stubs are present in order to present the proper termination to the diodes at the LO frequencies. This end of the diode pair should be grounded at the LO frequency so that the full LO voltage is dropped across the diode pair. This is accomplished by the use of a $\lambda_g/4$ @ LO open-circuited shunt stub, which presents a short circuit to the diodes at the LO frequencies. Since the RF frequency is approximately four times the LO frequency, the stub has a length of roughly one wavelength at RF, presenting an open circuit to this node at RF. This stub serves the additional purpose of suppressing LO leakage to the RF and IF ports. Finally, a $\lambda_g/4$

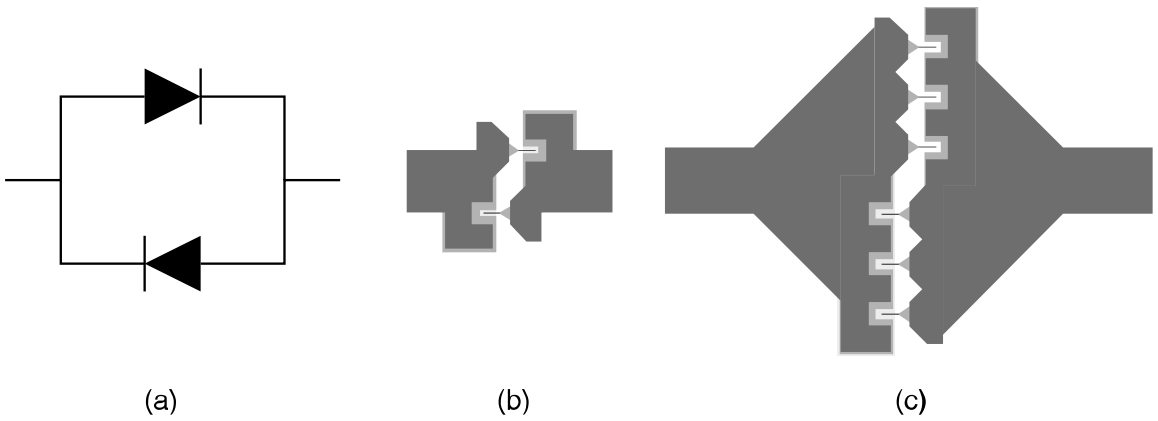


Figure 3.4: (a) Schematic antiparallel diode representation (b) Single antiparallel schottky diode implementation (c) Triple antiparallel schottky diode pair implementation

at $2 \cdot LO$ open-circuited stub is added at this node to suppress the 2X subharmonic conversion product as well as higher order (6X, 10X, etc.) products. Suppression of these products is important because they result in a degradation of conversion loss due to the conversion of RF power to unwanted spurious frequencies. This will be discussed further in section 3.4.

The side of the diode pair where the LO port is connected requires a specialized coupling network, as well. It is important that this side of the diode pair be grounded at RF and IF so that the full voltage of each respective signal appears at the side of the diode pair from which they are to be coupled. This is accomplished by placing a shunt short-circuited stub of length λ_g at RF at the LO input port. Since this stub length corresponds to a full RF wavelength, the short circuit at RF is presented at the LO feed line as well. One wavelength at RF is approximately a quarter wavelength at the LO frequency, which so the stub presents an open-circuit at the LO frequency, allowing the undisturbed LO signal to pass. This stub also serves the purpose of grounding the LO input line at the IF frequency. At the relatively low IF frequency and DC, the line is electrically short, so it appears to be a short circuit. It has also been shown that a DC ground is important for suppression of imbalanced DC currents circulating in the diode pair [37].

The LO matching network shown in the schematic is an optional addition to the circuit. While it may not improve the conversion loss significantly, it may help to lower the optimum LO drive level, potentially relaxing the power requirements of the oscillator. This benefit comes at the expense of spatial compactness of the circuit, since electrical delay lines for matching networks at the LO frequency are relatively large compared to the overall circuit size.

3.4 Simulated Results

The circuit shown in Figure 3.2 was simulated with a harmonic balance analysis using HP EESof Series IV[1] [18] using the schottky diode parameters of Table 3.1 (see Appendix B for detailed simulation schematics). Since the EESof Series IV simulation package does not include accurate models for FGC transmission lines, the FGC tuning stubs were simulated as ideal transmission line elements. The design of the actual FGC lines for mixer implementation will be presented in Chapter 4. The RF bandpass filter was simulated as a lumped equivalent circuit of the filter used in actual MMIC implementation. This filter is implemented as a series open-circuit FGC stub and its design and equivalent circuit are described in detail in Appendix A. The diode pair was implemented as both a single antiparallel pair (Figure 3.4(a)) and a triple antiparallel pair (Figure 3.4 (b)). In diode mixers, the use of two or more parallel diodes in place of each diode in the schematic is a common method of reducing the effective series resistance of the diodes. Since the diodes are in parallel, the effective series resistance is approximately equal to the series resistance of a single diode divided by the number of diodes. Since diode series resistance is a dominant factor in mixer conversion loss, its reduction can translate to an improvement in loss performance.

Initially, simulations were conducted with no matching networks present on the LO side. Figure 3.5(a) shows the conversion loss vs. LO power for each mixer, simulated at RF, LO, and IF frequencies of 60 GHz, 14.375 GHz, and 2.5 GHz, respectively.

[1] Now Agilent EEsof EDA

As expected, the conversion loss of the triple diode pair mixer is superior to that of the single diode pair mixer by approximately 2 dB, justifying the use of the triple diode pair. The optimum LO drive level is between 5 and 7 dBm for the single antiparallel pair and between 7 and 9 dBm for the triple antiparallel pair. Frequency sweeps are shown for both mixers using LO drive levels of 6 dBm and 8 dBm for the single diode pair and triple diode pair mixers, respectively. The results of these simulations are shown in Figure 3.5(b). Minimum conversion loss in either diode configuration occurs between 59 and 61 GHz. The simulated minimum conversion loss of these mixers is 12.3 dB at 60.1 GHz for the single diode pair and 10.8 dB at 60.1 GHz for the triple diode pair.

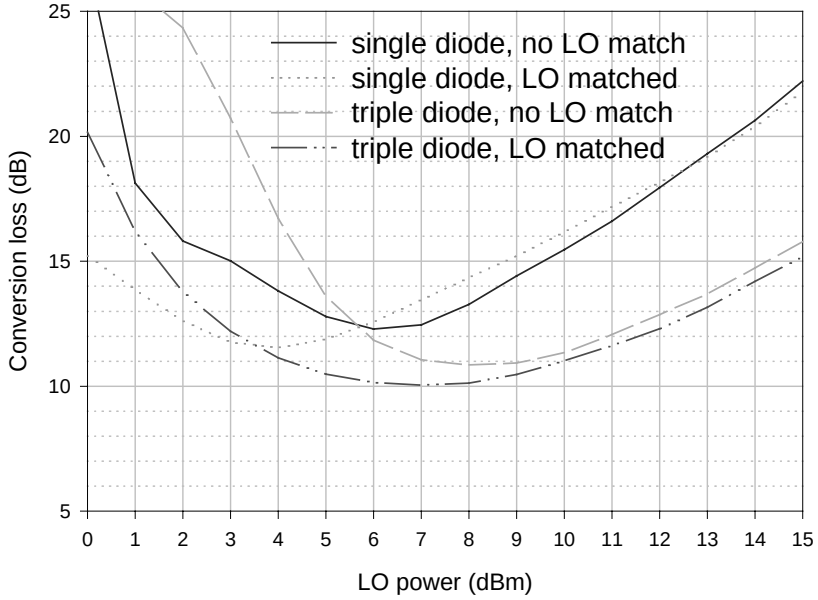
The circuits were then simulated with appropriate single-stub matching network at the LO input. The matching networks were designed to optimize conversion loss at an LO power lower than that for the unmatched case. This was accomplished by attempting a match for the optimum LO drive as determined for the unmatched mixers. It was observed that the minimum conversion loss does not necessarily coincide with a 50 Ω match. Therefore, the implemented matching network dimensions represent an iterative approach that results in a compromise between a 50 Ω impedance match and optimal conversion loss at a relatively low LO power. Figure 3.6 shows the simulated S_{11} of the LO input ports at the optimum LO drive level. Inspection of these data reveals that the impedance is closer to 50 Ω at lower power levels for the mixers with LO matching networks. The result is that the LO drive level at which the best conversion gain occurs is lower for the mixers with matching networks. The match is accomplished for both the single and triple diode cases by the addition of a delay line followed by a short-circuited shunt stub to the LO port. The single diode mixer require a delay line of 24 degrees and a shunt stub of 57 degrees at 14.5 GHz. For the triple diode pair mixer, the electrical lengths were chosen as 28 degrees and 50 degrees at 14.5 GHz for the delay line and shunt stub, respectively. The impact of these networks on the return loss of the LO port is shown in Figure 3.7. As shown in Figure 3.5, the effect of the matching network for the single diode case is to shift the optimum LO drive level from 6-7 dBm to 3-4 dBm.

The optimum drive level for the triple diode case shifts from 7-9 dBm to 6-8 dBm with the addition of the LO matching network. A slight improvement in conversion loss is noted, as well. The frequency sweep shown in Figure 3.5 (b) was simulated at the optimum LO drive level for each case. The optimum levels are 4 dBm for the case of the matched single diode mixers and 7 dBm for the matched triple diode mixers. The addition of matching networks results in an improvement in optimum conversion loss to 11.4 dB at 60.5 GHz for the single diode pair and 10.0 at 59.7 GHz for the triple diode pair.

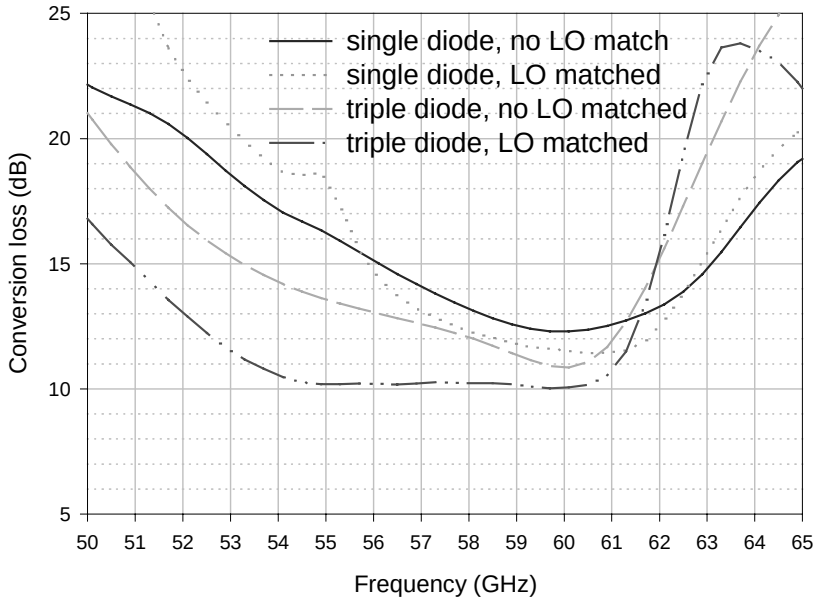
An investigation into the utility of the $2f_{LO}$ suppression was conducted, as well. Preliminary simulations showed that the most prominent spurs are the RF–$2f_{LO}$ and the $6f_{LO}$-RF products. The conversion loss from RF to each of these products was simulated and plotted for the LO matched triple diode mixer in Figure 3.8. Figure 3.8 (a) indicates that the conversion loss from RF to the *undesired* RF-$2f_{LO}$ product is *lower* than the *desired* RF-$4f_{LO}$ product. The $6f_{LO}$-RF product is about 20 dB lower than the desired product at the optimum LO drive level, so its contribution to the conversion loss of the desired IF is negligible. Figure 3.8(b) shows that the addition of the $2f_{LO}$ suppression stub increases conversion loss of the RF-$2f_{LO}$ product by about 15 dB. The RF power converted to this product is then negligible, as is evidenced by the approximately 3 dB of improvement in the conversion loss of the desired RF-$4f_{LO}$ product. There is little or no improvement in the RF-$6f_{LO}$ rejection due to the addition of the $2f_{LO}$ stub. This is of little concern since the rejection of this product is greater than 15 dB with or without the additional stub. Figure 3.9 shows mixer conversion loss vs. frequency for the triple diode mixer with LO matching both with and without the $2f_{LO}$ suppression stub. Clearly, it is critical to include the $2f_{LO}$ suppression stub to achieve the optimum conversion loss.

Figure 3.10 shows the simulated 1 dB compression point for the mixer. This point occurs at an RF input power of about 1 dBm, which suggests an approximate input third-order intercept point (IP3) of 11 dBm. This is based on the assumption that the input IP3 is roughly 10 dB higher than the input 1 dB compression point. The IP3 is

a useful metric in predicting the amplitude of in-channel spurs caused by out-of-channel interferers. Whether or not this linearity will satisfy the system linearity requirements is dependant on the LNA gain and any loss prior to the mixer. A mixer with considerable conversion loss as in this case (10 dB), would likely be preceded by an LNA with a gain in the vicinity of 20 dB. If the IP3 of the mixer is then referred to the input of the LNA, it has an equivalent value of –9 dBm [mixer IP3 (11 dBm) – LNA gain (20 dB)]. This approximation suggests poor mixer linearity which could possibly be a more significant contributor to receiver intermodulation distortion than the LNA. The linearity of subharmonic mixers is known to be worse than fundamental mixers, so this effect would have to be carefully considered during the receiver system design phase.

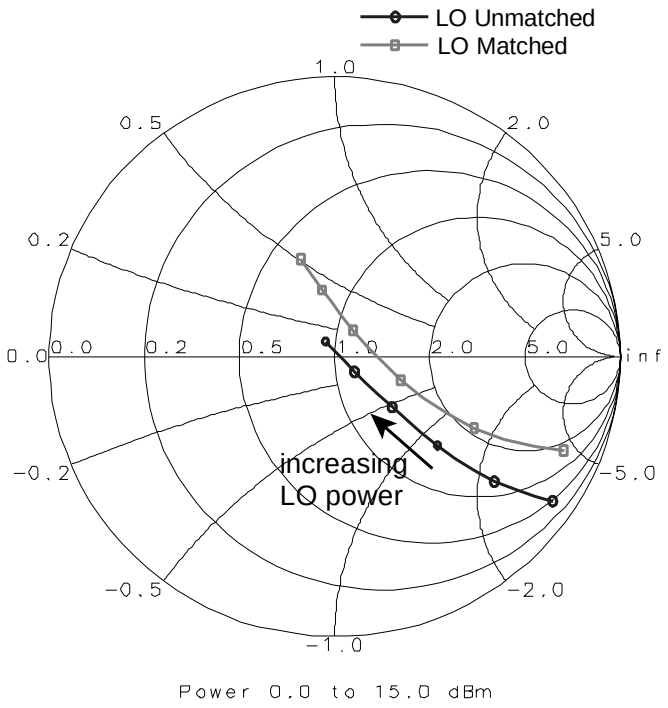


(a)

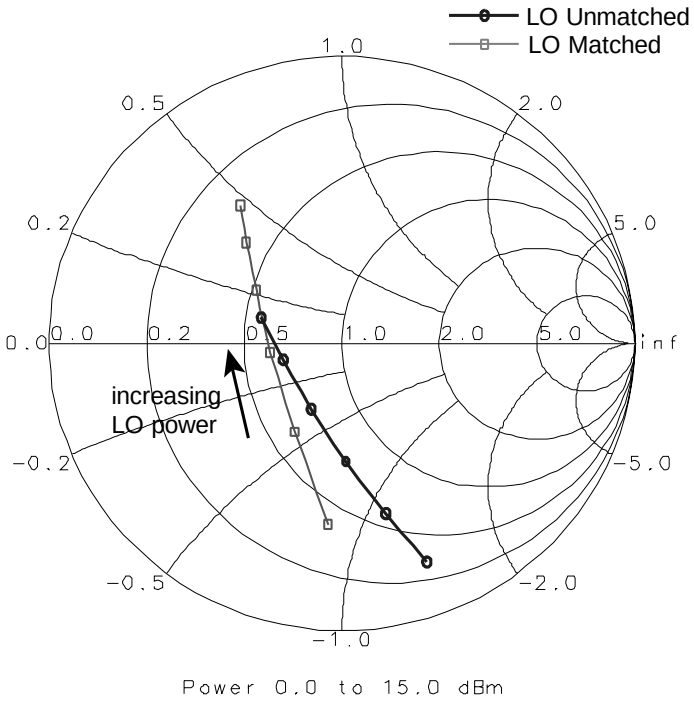


(b)

Figure 3.5: (a) Simulated mixer conversion loss vs. LO drive level, RF=60 GHz, f_{LO}=14.375 GHz, IF=2.5 GHz, (b) simulated USB conversion loss vs. RF frequency, IF=2.5 GHz, optimum LO drive level

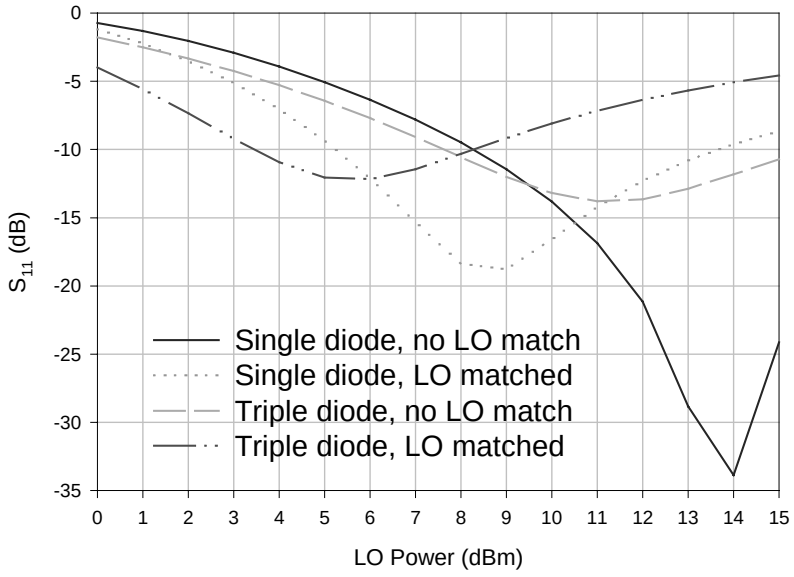


(a)

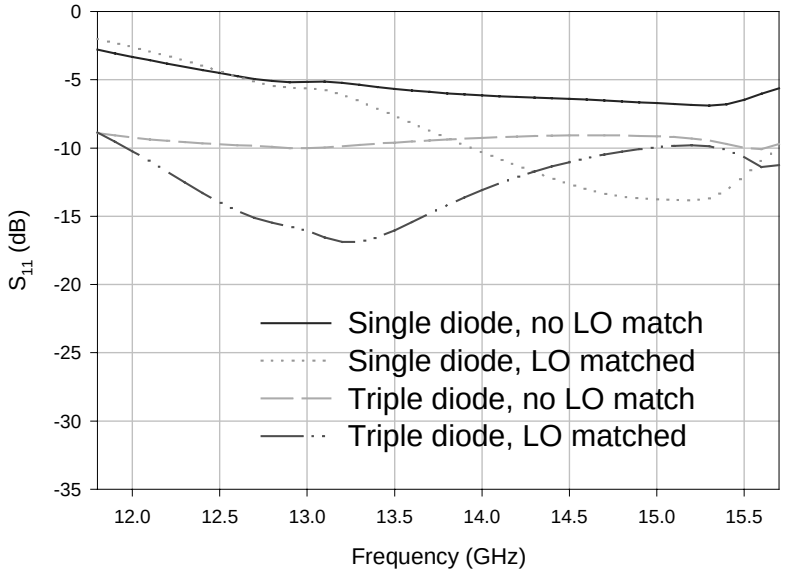


(b)

Figure 3.6: Simulated S_{11} of LO input port for RF=60 GHz, f_{LO}=14.375 GHz, IF=2.5 GHz for (a) single diode mixer, (b) triple diode mixer

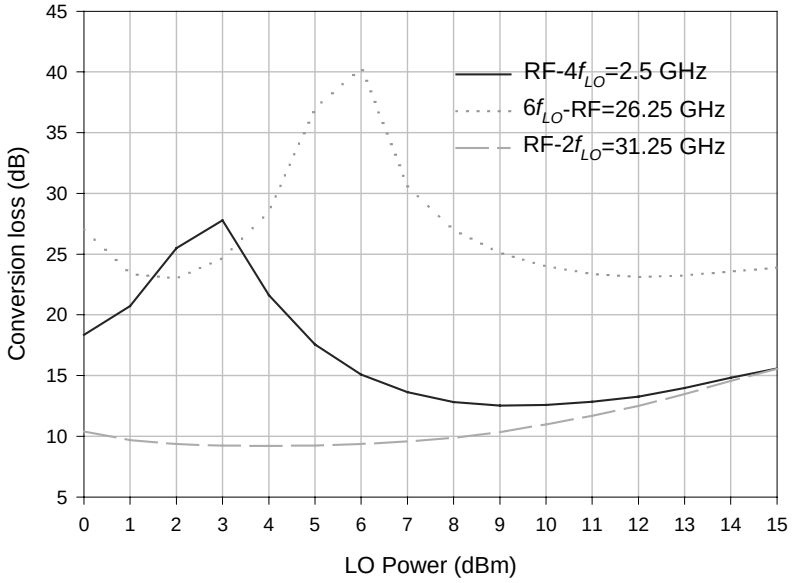


(a)

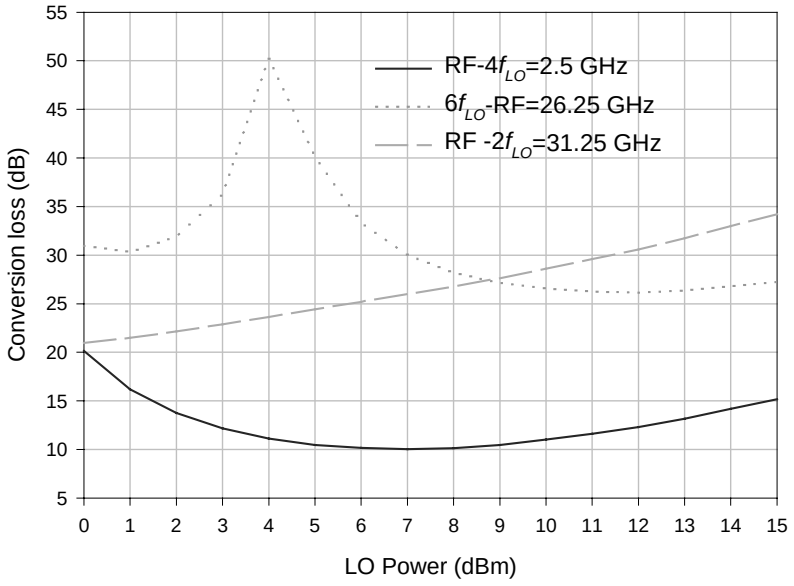


(b)

Figure 3.7: Simulated LO port return loss (a) vs. LO power, RF=60 GHz, f_{LO}=14.375 GHz, IF=2.5 GHz, (b) vs. LO frequency, optimum LO drive level



(a)



(b)

Figure 3.8: Simulated conversion loss of various mixing products, RF=60 GHz, f_{LO}=14.375 GHz, (a) no $2f_{LO}$ suppression stub, (b) with $2f_{LO}$ suppression stub

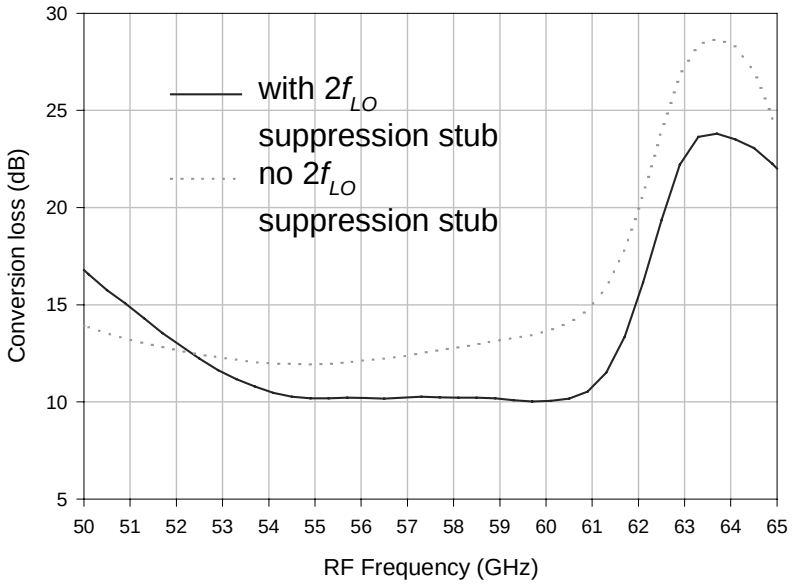


Figure 3.9: Simulated USB conversion loss vs. frequency, f_{LO} = 14.375 GHz

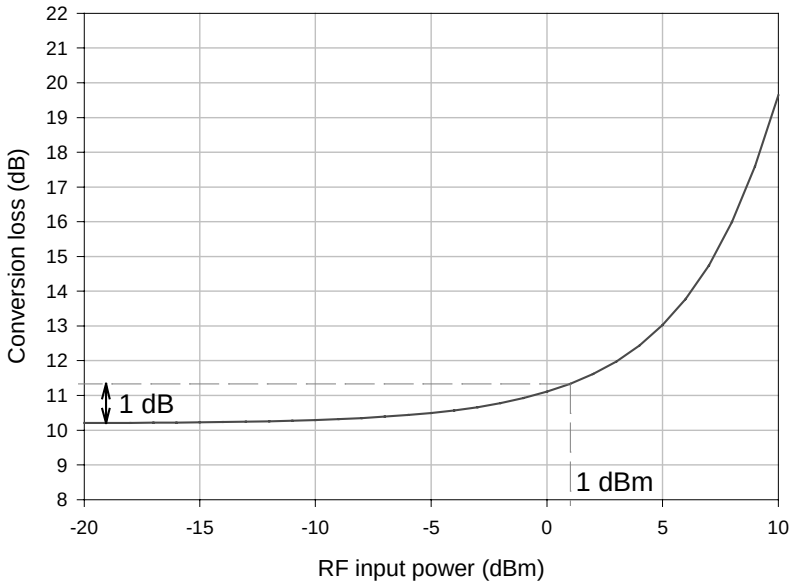


Figure 3.10: Simulated 1 dB compression point for triple diode mixer with LO matching, USB, RF = 60 GHz, IF = 2.5 GHz, LO power = 7 dBm

CHAPTER 4
DESIGN AND IMPLEMENTATION OF FINITE GROUND COPLANAR WAVEGUIDE STUBS

The proper design of tuning stubs is crucial to performance of the proposed 60 GHz 4-X subharmonic mixer. In Chapter 2, FGC transmission lines were designed to provide good return loss and low insertion loss in a 50-Ω system. Chapter 3 included mixer design and simulation using ideal tuning stubs. In this chapter, the design results and requirements of Chapters 2 and 3 will be combined to allow implementation of tuning stubs in FGC technology that approximate the electrical performance of the ideal stubs used for mixer simulations. The goal of these efforts will be to design and fabricate a MMIC mixer using FGC lines that will match the performance simulated in Chapter 3.

The stubs used in the simulations of Chapter 3 are ideal models in that they allow an electrical length and characteristic impedance to be specified at a particular frequency, since these are the parameters of most interest to the designer. In practice, the electrical length of shunt circuit elements may not hold a simple correspondence to the physical length of the fabricated element. In the case of CPW and its variants, transmission line discontinuities such as t-junctions and bends make electrical length difficult to predict from the physical line length alone. Therefore, full-wave electromagnetic simulations are necessary in order to account for these effects on the electrical characteristics of the tuning elements. It will further be explained that these discontinuities may also promote the excitation of parasitic propagation modes that must be given careful consideration. Methods of suppressing these parasitic modes will be investigated and implemented.

4.1 Slotline Mode Suppression

In the implementation of transmission lines in FGC technology, several potentially problematic issues must be addressed. One of these is a parasitic mode supported by the FGC structure called the slotline, or *even* propagation mode [39], [40]. The voltage potential of an EM wave propagated in the slotline mode is illustrated in comparison with that of the desired CPW, or odd propagation mode in Figure 4.1. This mode is caused by a potential difference between the two ground planes in the FGC structure. This potential difference can be excited by asymmetries in the slot lengths flanking the center conductor resulting from discontinuities such as T-junctions and bends. In order to suppress the slotline mode in the presence of these discontinuities, it is necessary to prevent the voltage potential difference that arises near the discontinuity. This can be accomplished by connecting the two ground planes together near any discontinuity that may excite the even mode. Since it is necessary to do this without shorting out the center conductor, additional structures such as bond wires, airbridges, or dielectric crossovers must be used [40]. These structures are illustrated in Figure 4.2 (a), (b), and (c), respectively.

Bond wires are suitable for connecting the ground planes together at relatively low frequencies, but require additional post-processing steps and are unacceptable for mm-wave frequencies. This is due to an inductive component that represents a significant series impedance at higher frequencies such as 60 GHz. Airbridges may provide acceptable electrical performance by offering sufficiently low series impedance to suppress the slotline mode, but are not available in all MMIC processes. Since part of the structure is suspended above the center conductor, airbridges are potentially prone to damage. This may negatively affect fabrication yield. This drawback leads some chip vendors to avoid their use. Therefore, a different method of electrically connecting the two ground planes using a structure called a dielectric crossover is often used. In the MSAG-5 process used in this thesis, the particular dielectric crossover technology is referred to as a *PLC crossover*.

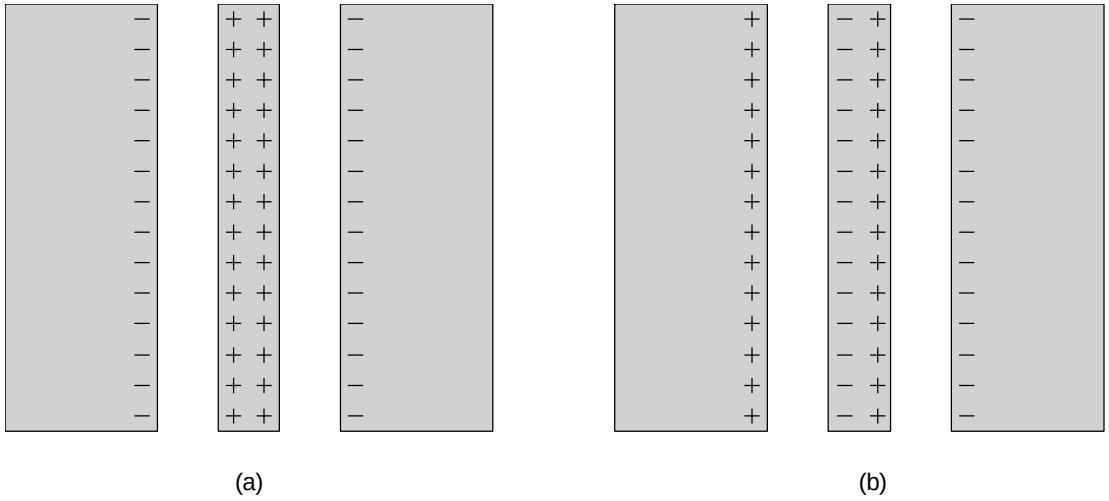


Figure 4.1: EM wave voltage potentials for the (a) CPW (odd) propagation mode, (b) slotline (even) propagation mode

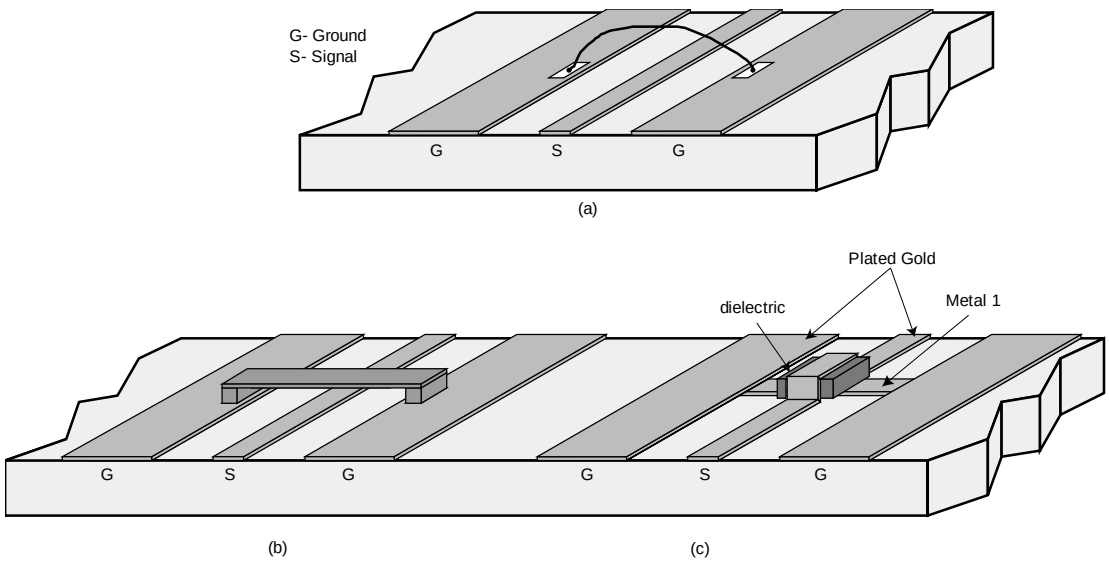


Figure 4.2: Methods of slotline mode suppression: (a) bond wire, (b) airbridge, (c) dielectric crossover

4.2 PLC Crossover Design

A description of the PLC crossover structure requires an explanation of the layer composition in the available fabrication process, shown in Figure 4.3. The top layer on this diagram is the plated gold layer. This layer is used for transmission lines and spiral inductors because the gold has good conductivity and low loss due to a relatively thick metallization (4.5 μm). Directly beneath this layer is an optional layer, the PLC dielectric. The dielectric is optional because it is only used where additional spacing is needed between the Plated Gold and Metal 1 layers to reduce the capacitive coupling between the two. The silicon nitride layers (SiN) are called the passivation layers and are used to prevent unwanted electrical contact between Metal 1 and the plated gold and GaAs layers. Metal 1 is an additional conductor layer used for lower capacitor plates. As shown in Figure 4.2, this is the layer used for connecting the two ground planes of the FGC lines in a PLC crossover. The FGC lines are fabricated on the plated gold layer. The Metal 1 strip crosses underneath the center conductor and is connected to the ground planes at either end by vias (openings in the SiN). A rectangular section of PLC is defined above the Metal 1 conductor to reduce its mutual capacitance with the FGC center conductor. A cross section of the PLC crossover topology is shown in Figure 4.4. Although the PLC dielectric reduces the shunt capacitance to ground caused by the proximity of the Metal 1 conductor underneath the center conductor, a significant capacitance still exists between the two. The effect of this capacitance is to reduce the characteristic impedance of the line at that point, which degrades the return loss of the transmission line unless some compensation method is employed.

In order to address this problem, several approaches have been proposed to compensate for the change in characteristic impedance caused by the PLC crossover [41]. The most obvious technique would be to reduce the width of the center conductor until the desired characteristic impedance is attained for the section of center conductor suspended over the Metal 1 conductor. Figure 4.4 shows that the cross section of the PLC crossover can be viewed as a short microstrip transmission

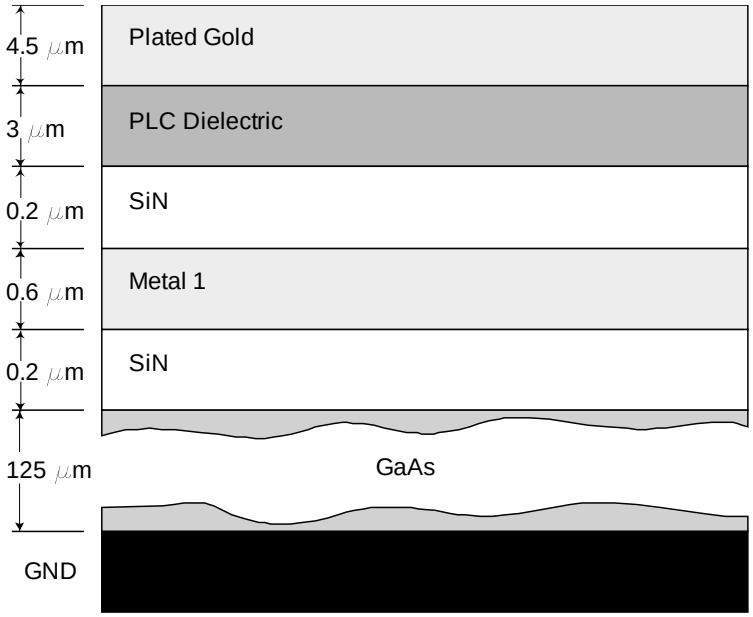


Figure 4.3: M/A-COM MSAG 5 process layer stackup

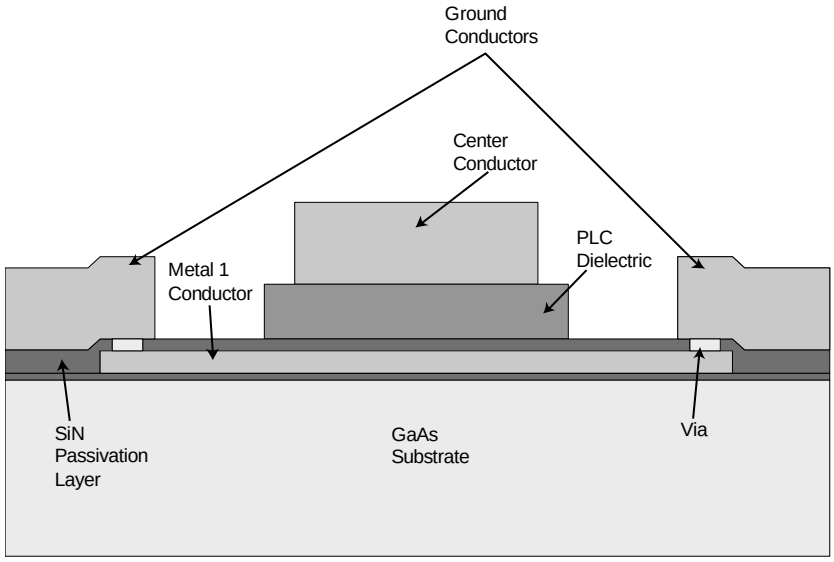


Figure 4.4: Cross section of PLC crossover for slotline mode suppression in FGC

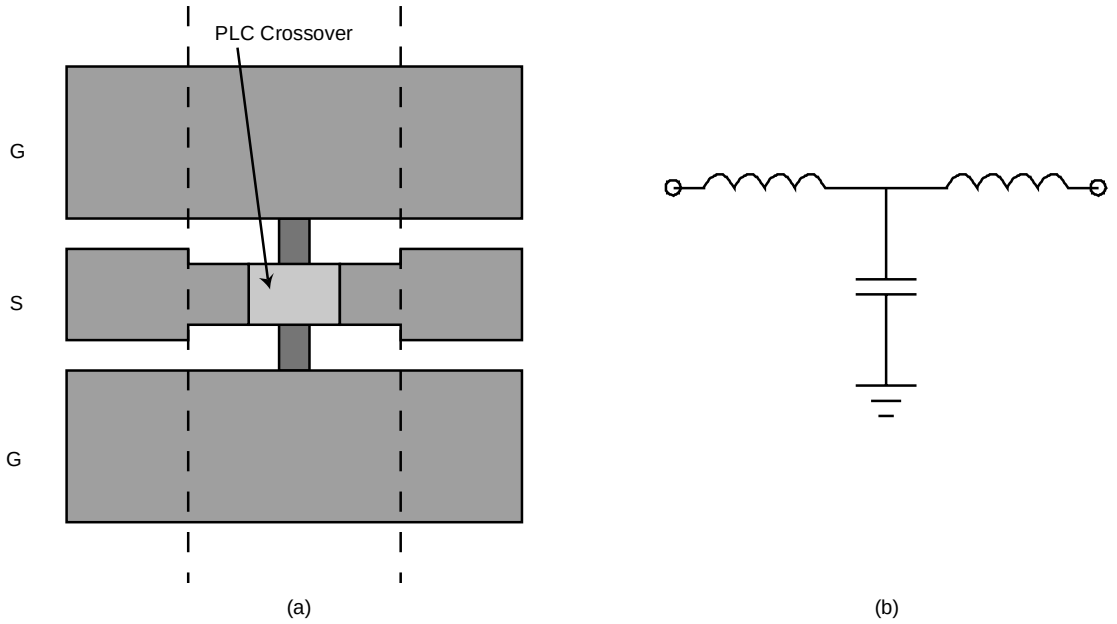


Figure 4.5: PLC crossover compensation, (a) physical representation (b) equivalent circuit

line with the Metal 1 conductor as the ground plane. Therefore, the center conductor could theoretically be reduced in width until the characteristic impedance matches that of the standard FGC line, in this case 50 Ω. However, further investigation into this technique revealed that this would require a line width that is drastically less than that of the standard FGC line. This results in large reflections due to the step discontinuity in line width. These reflections would be significant enough as to negate the advantage offered by correcting the characteristic impedance at the crossover. Therefore, another method of impedance compensation at the crossover was investigated. As mentioned before, the PLC crossover may be electrically modeled as a shunt capacitor on the transmission line. It is possible to create a compensation structure that is equivalent to a tee lowpass filter with a 50-Ω impedance by narrowing the center conductors for a certain length on either side of the crossover [41]. The physical implementation and equivalent circuit are shown in Figure 4.5. For this approach to be successful, the cutoff frequency of the equivalent lowpass filter must be in excess of all frequencies of interest for the transmission lines.

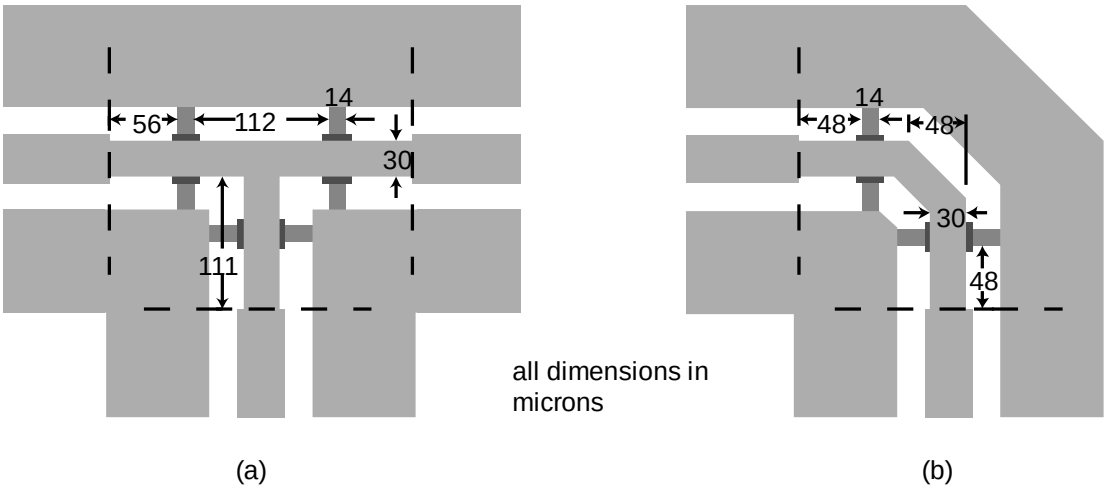


Figure 4.6: FGC discontinuities with PLC crossovers and characteristic impedance compensation, (a) T-junction, (b) 90º bend

A specific PLC crossover design was implemented for the standard transmission lines defined in Chapter 2. The Metal 1 conductor strip width was chosen to be 14 μm. This width was based on recent research indicating that slotline mode suppression is related to the width of airbridges [40]. Wider airbridges have been shown to provide greater even mode rejection, so the same relationship was assumed to hold true for the PLC crossover structure. Once the Metal 1 strip width has been fixed, simulations may then be carried out as to the effects of the additional shunt capacitance and the compensation required to mitigate those effects. Based on layout considerations for items such as T-junctions and bends, the length of the narrowed transmission line section (enclosed by the dotted lines in Figure 4.5) was chosen to be 56 μm. IE3D simulations indicate that for this length, a line width of 30 μm results in a 50-Ω characteristic impedance for the overall crossover structure. The cutoff frequency simulated was in excess of 75 GHz, suggesting that this crossover configuration will work well with the standard FGC lines designed in Chapter 2 for all frequencies of interest. These dimensions for PLC crossovers will be applied in mixer fabrication at all FGC T-junctions and bends. The standard T-junction and bend are shown in Figure 4.6. The chamfer of the bend was chosen for a less abrupt 90º transition than a right-angle bend.

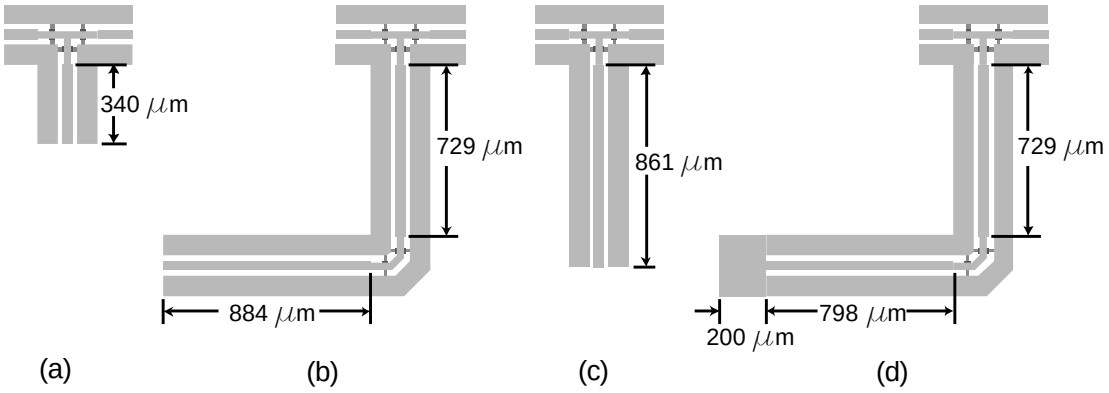


Figure 4.7: Shunt tuning stub layouts: (a) open circuited $\lambda_g/4$ @ RF, (b) Open-circuited $\lambda_g/4$ @ LO, (c) Open-circuited $\lambda_g/4$ @ 2*LO, (d) Short circuited λ_g @ RF

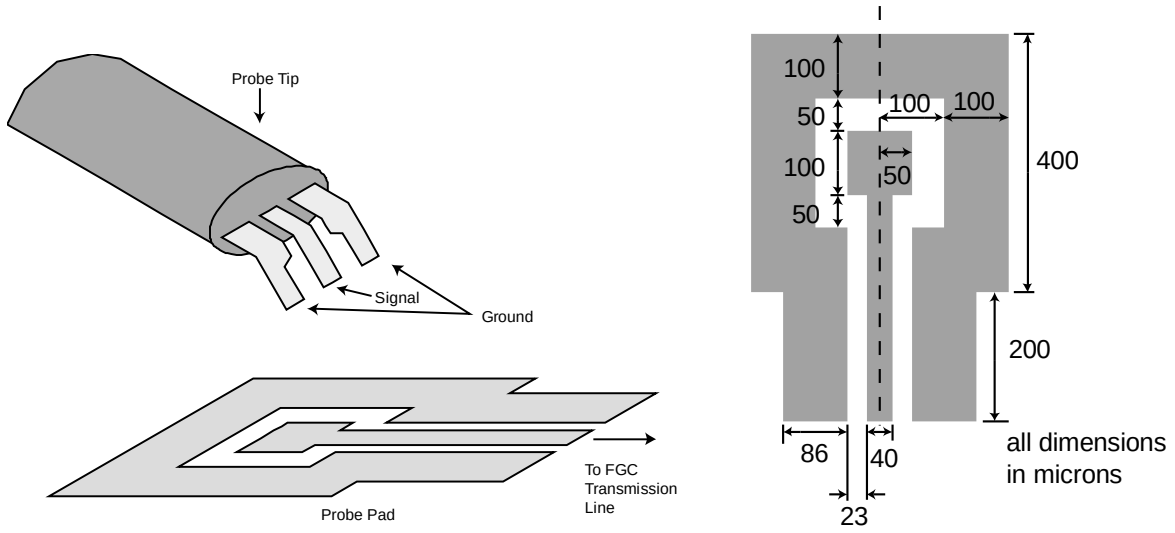
4.3 Design and Simulation of Tuning Stubs

The standard transmission lines designed in Chapter 2 and the T-junction and bend shown in Figure 4.6 comprise the essential building blocks necessary for construction of the proposed mixer. Although the compensation of PLC crossovers corrects the change caused in characteristic impedance, it also causes a change in effective dielectric constant for the length of the compensation. This change, along with the T-junction and bend discontinuities, makes the electrical length corresponding to a physical shunt stub length difficult to predict. Therefore, the line lengths of the tuning stubs required for resonance at the necessary frequencies must be determined through full-wave simulation. The approximate FGC implementations of the four ideal stubs used for mixer simulation in Chapter 3 were determined based on simulation data from IE3D. The lengths of the simulated FGC stubs were iteratively tuned until the resonant frequencies were equal to those of their ideal counterparts in Chapter 3. The layouts of the simulated structures are shown in Figure 4.7. The T-junctions are incorporated so that the shunt stubs may be added to any standard FGC transmission line. Ninety-degree bends are used on stubs with particularly large physical lengths. This is to preserve the spatial compactness of the overall mixer circuit, and can be seen in Figure 4.7 (b) and (d). The line lengths indicated here

denote the lengths of the simulated lines referenced from the end of the standard T-junction or bend to which they are connected. The lengths indicated are the result of iterative tuning to achieve the same resonant frequency as the ideal stubs used for mixer simulation in Chapter 3. The performance data for these simulated stubs will be presented in the following section and compared to the measured data for the actual fabricated stubs.

4.4 Measurement of FGC Tuning Stubs

Circuit fabrication was completed in three different process variations. The basic substrate composition for each of these variants is the same as described in Chapter 4. In the standard process, the gallium arsenide wafers are initially about 650 μm thick. After the circuits are formed on the front side of the wafer, the wafers are thinned to the standard 125-μm thickness and backside metallization is added. The wafer is then diced into individual chips. In the first of the three process variations, the wafer thinning process step is omitted and the substrate thickness remains 650 μm with no backside metallization. This is to provide a benchmark for comparison with thinned substrates with backside metallization which could support undesired modes. Vendor manufacturing rules dictate that since the wafers in this process variation are unthinned, individual circuits cannot be diced and must be tested on whole 4-inch wafers. The wafers fabricated in the second process variation are of the standard thickness of 125 μm with backside metallization. This process composition is roughly equivalent to that used for transmission line and stub simulations in Chapters 2 and 4. Finally, the third process variation is the same as the second with the addition of a polyimide buffer layer on the top side of the wafer. This layer provides mechanical strength during dicing and protects the top of the wafer. Windows in this buffer layer must be included where there are GSG probe pads so that the circuits may be accessed for testing. The covering of the FGC lines with this polyimide layer (ε_r=2.9) will cause different transmission line characteristics than the FGC lines in the other process variations, which are covered by air (ε_r=1). The effect of the buffer layer will be to increase the effective permittivity of the FGC lines with polyimide



(a) (b)

Figure 4.8: (a) Wafer probe tip and probe pad, (b) standard probe pad dimensions

covering. The implications this may have on transmission line performance will be analyzed and discussed with the measured data.

4.4.1 Testing Issues

At mm-wave frequencies such as 60 GHz, a packaged circuit with external leads is typically not feasible due to the parasitics associated with bond wires and package leads. Therefore, any testing must be accomplished by the use of probes specifically designed for on-wafer testing. This is a more relevant measurement in this work since the mixer is intended to be part of an integrated receiver including an on-chip antenna and LNA. The wafer probes used are of the ground-signal-ground (GSG) type, shown in Figure 4.8 (a), which are compatible with the signal paths used in CPW and FGC transmission lines. The probe dimensions indicated in Figure 4.8 (b) match the pitch of the wafer probes, which measure 150 μm between the centers of each probe tip. The probes make direct contact with probe pads that are connected to the standard FGC transmission lines. The probes interface to 1.85 mm or 2.4 mm coaxial cable for connection to standard microwave/mm-wave test equipment.

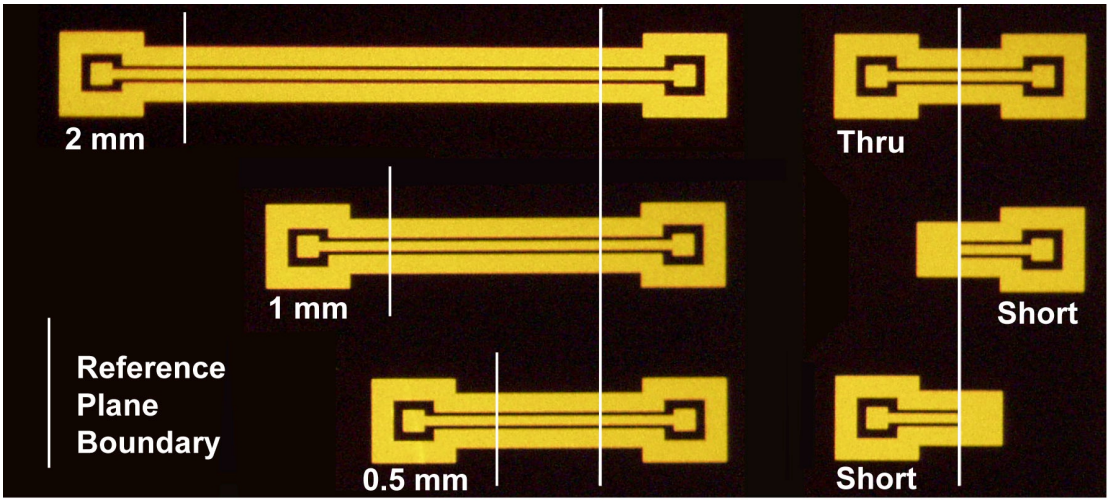
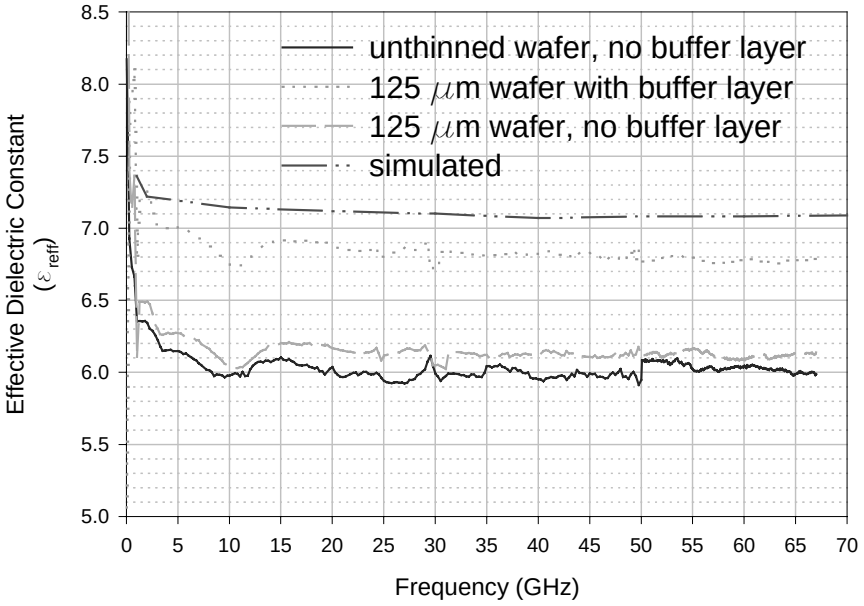
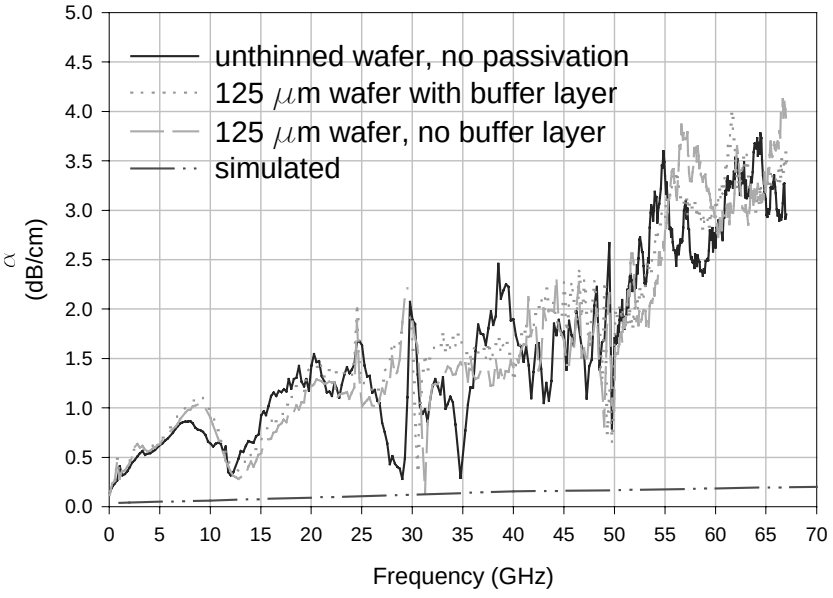


Figure 4.9: Photograph of on-wafer TRL calibration standards

Full 2-port S-parameters of the passive tuning structures were measured using a Cascade wafer probe station and an HP 8510C vector network analyzer. In order to de-embed the effects of the analyzer test set, cables, probe tips and probe pads, a TRL (thru, reflect, line) two-port calibration was conducted using the NIST Multical program [42]. The standards needed for a TRL calibration are easily fabricated on-wafer in FGC technology. A photograph of the 2-port calibration standards and probe pads is shown in Figure 4.9. The calibration reference plane is located at the center of the thru standard. The reflect standard required for the TRL calibration is provided by the short-circuit standards shown in the photograph. The line standards are three FGC lines of L=500 μm, 1000 μm, and 2000 μm. The Multical calibration program records the measured S-parameters of these standards and creates a set of calibration coefficients based on these data. The calibration coefficients are then loaded into the network analyzer, which uses them to correct the effects of the test cable, probes, and probe pads up to the calibration reference plane. The program also calculates useful transmission line parameters such as effective permittivity (ε_{eff}) and line attenuation (α) based on the measured S-parameters of the delay lines.



(a)



(b)

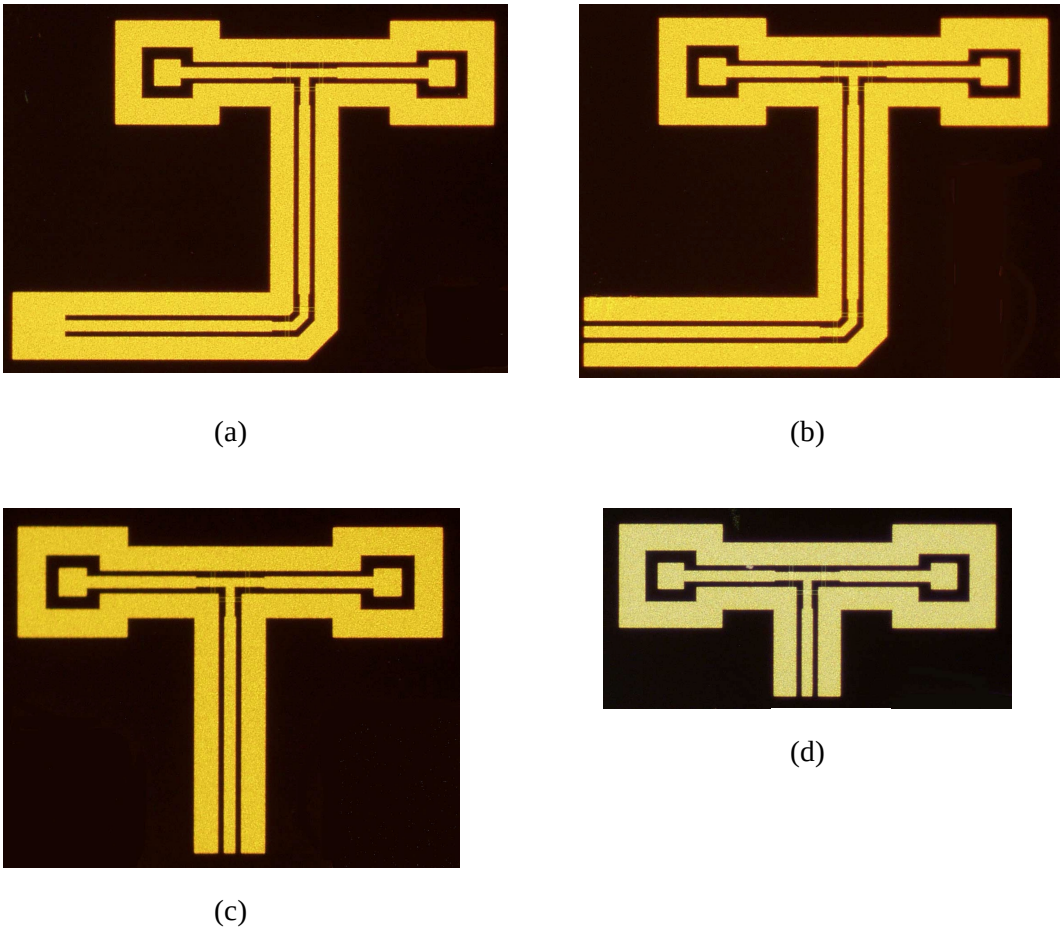
Figure 4.10: Transmission line properties of standard 50-Ω FGC lines for various wafer processes: (a) effective dielectric constant, (b) line attenuation

4.4.2 Transmission Line Parameter Measurements

The transmission line parameters of effective permittivity and line attenuation are plotted for each process variation in Figure 5.3. Figure 5.3 (a) shows that on each of the measured wafers, ε_{eff} is lower than in the simulated data. This is most likely due to simulating the FGC conductors as two-dimensional, without considering the thickness of the gold. The effective permittivity is based on a weighted combination of the permittivities of the two media in which the electric fields of the CPW mode reside, in this case gallium arsenide (ε_r=12.9) and air (ε_r=1). The weighting is based on the fraction of the electric field that lies in each medium. Simulations with two-dimensional conductors do not account for the coupling in air between the side walls of the FGC conductors, which is the likely cause of error in the simulated ε_{eff}.

It must also be noted that the effective permittivity of the FGC lines on the wafer coated with a polyimide buffer layer is much closer to the simulated value than in the other process variations. The increase in effective permittivity caused by the presence of the polyimide (explained in section 4.3) offsets the erroneously low effective permittivity due to two-dimensional simulation errors, resulting in a closer value to the simulated result. Since the dielectric constant of the buffer layer is higher than that of air, the effective dielectric constant of the FGC lines is higher. Inspection of Equation 2.1 shows that a lower value of ε_{eff} will result in a larger guided wavelength in a given FGC line. Therefore, a stub of a given length will appear *electrically shorter* for a lower value of ε_{eff}.

The line attenuation of the FGC lines in each process variation is plotted in Figure 4.10 (b). The measured line attenuations are significantly higher than the simulated data. Although the high line attenuation is not desirable, this should not critically degrade mixer performance. The transmission line lengths in mixer implementation will be on the order of 1-2 mm, which should result in a worst-case line attenuation of less than 0.5 dB (60 GHz).



(a) (b)

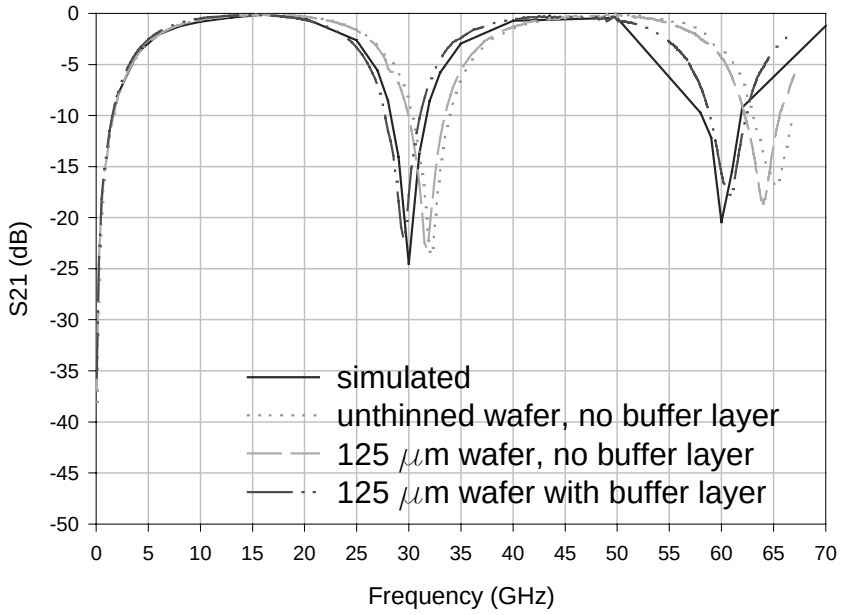
(c) (d)

Figure 4.11: Photographs of fabricated tuning stubs: (a) short-circuited λ_g at RF, (b) open-circuited $\lambda_g/4$ at LO, (c) open-circuited $\lambda_g/4$ at 2LO, (d) open-circuited $\lambda_g/4$ at RF

4.4.3 Tuning Stub Measurements

The differences in the transmission line characteristics are evident in the measured S-parameters of the tuning stubs. Photographs of the fabricated tuning stubs with probe pads are shown in Figure 4.11. The dimensions and construction of these stubs are identical to the designs in section 4.2. Transmission coefficient (S_{21}) measurements for these stubs are shown in Figures 4.12 and 4.13. These figures indicate that the measured resonant frequencies of stubs on the thinned substrate with no buffer layer are roughly 10% higher than the simulated values; this verifies the prediction of mistuned stub resonant frequencies due to the lower ε_{eff}. The resonant frequencies of the stubs covered in polyimide buffer are closer to the designed values of 60 GHz, 14.5 GHz, and 29 GHz for the RF, LO ,and $2f_{LO}$ stubs, respectively. This agrees with

the measured ε_{eff} values which indicate that the circuits covered by the polyimide buffer have closer characteristics to the simulated circuits than those fabricated in the other process variations. Based on these observations of the measured data, the wafer with a buffer layer should show similar mixer performance to simulated results. The wafers from the other two process variations should be tuned to a higher reception frequency than the standard process, but should otherwise show similar performance as well. Aside from the resonant frequency deviations, the measured tuning stubs exhibit similar performance to the simulated data. Chapter 5 will include the mixer measurements for each process variation and will analyze the effects of resonant frequency differences in the fabricated tuning stubs.



(a)

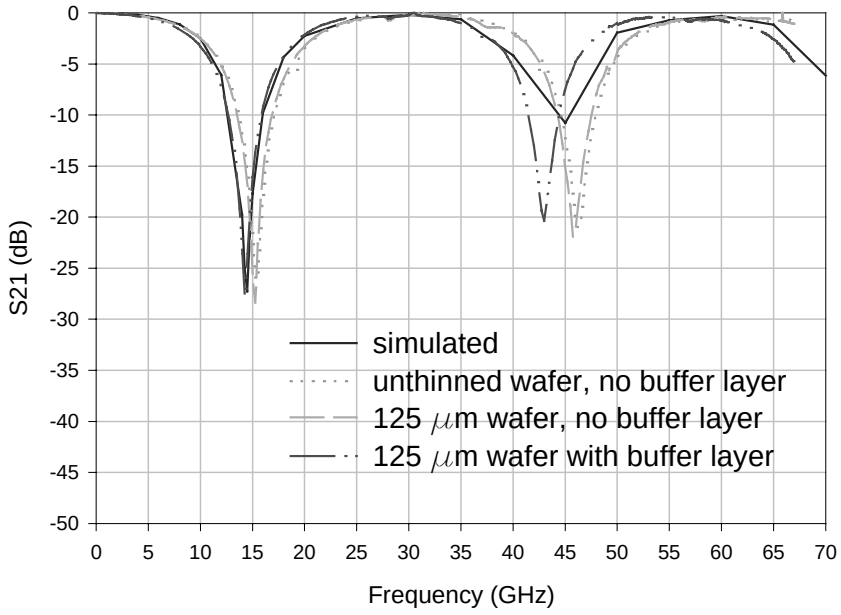


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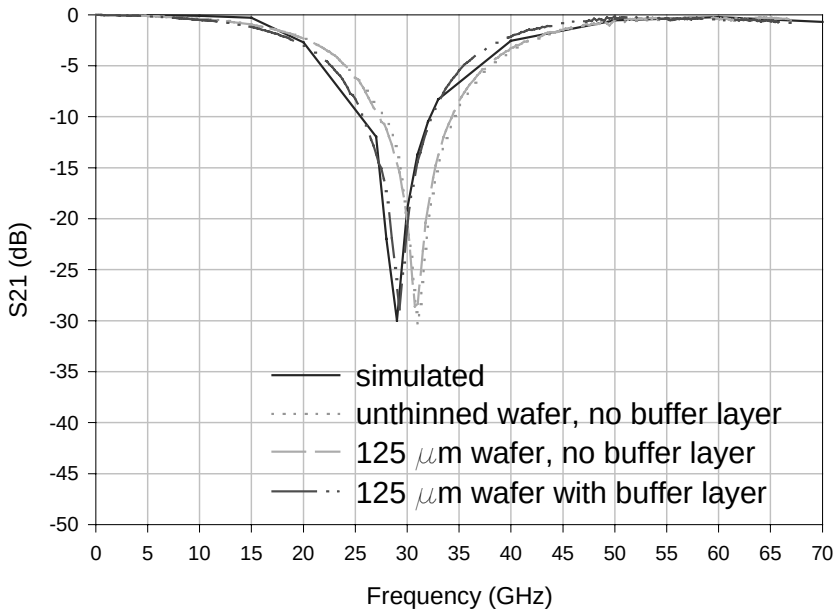
Figure 4.12: S_{21} of tuning stubs: (a) short-circuited λ_g @ RF, (b) open-circuited $\lambda_g/4$ @ LO



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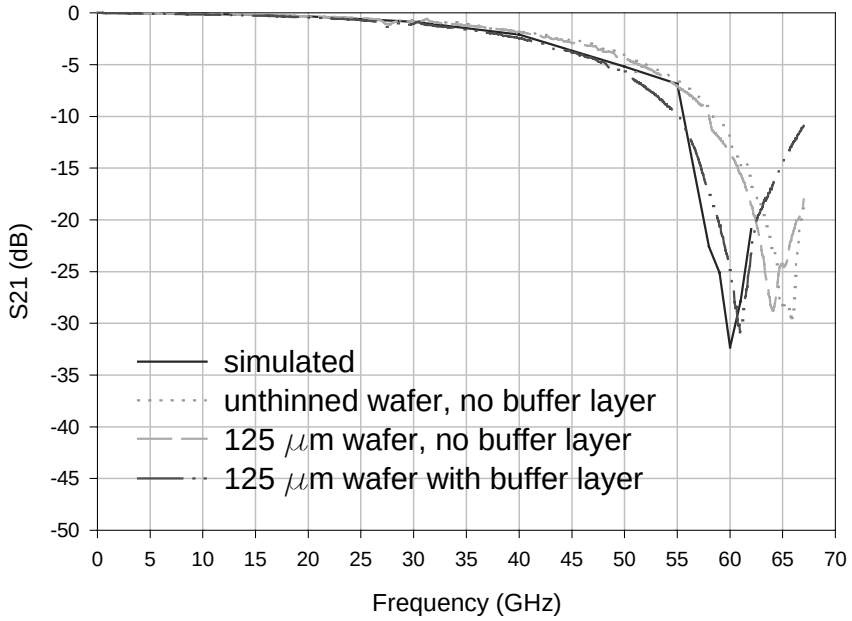


(b)

Figure 4.13: S21 of tuning stubs: (a) open-circuited $\lambda_g/4$ @ 2LO, (b) open-circuited $\lambda_g/4$ @ RF

CHAPTER 5
MMIC MIXER FABRICATION AND MEASUREMENT RESULTS

The design and implementation work in Chapters 2-4 culminates in the fabrication and testing of a 60 GHz GaAs MMIC 4X subharmonic mixer. The mixer designs simulated in Chapter 3 are implemented using the FGC transmission lines and tuning elements designed in Chapters 2 and 4, respectively. The mixer's 60 GHz bandpass filter is realized with a series open-circuit resonant stub in FGC (see Appendix A). These circuits are fabricated in the M/A-COM MSAG Process 5. Each mixer has been thoroughly characterized for conversion loss, LO-RF isolation, and LO-IF isolation at various operating frequencies and LO drive levels. An estimate of the fabricated Schottky diode series resistance (R_s) is also obtained from measured diode I-V curves in order to assess the impact on mixer performance.

5.1 Diode I-V Measurements

Good mixer conversion loss is largely dependent on parameters of the Schottky diode, particularly the series resistance (R_s). A simple Schottky diode model is shown in Figure 5.1 (a). By measuring the I-V curves of the diode, several important diode parameters may be extracted including R_s, ideality factor (η), and current parameter (I_s). These values may then be compared with the values of the Schottky diode model parameters used in mixer simulations. Any discrepancy between the simulated and measured diode parameters may be useful in explaining differences between simulated and measured mixer performance. Ideal diode current is given by the familiar Shockley Equation:

$$I(V) = I_s \exp\left(\frac{qV}{\eta KT} - 1\right) \tag{5.1}$$

where q is electron charge, K is Boltzmann's constant, and T is temperature. When plotted on a logarithmic scale, this equation forms a straight line, as shown in Figure 5.1 (b). In practical Schottky diodes, the voltage drop across R_s becomes significant enough to cause the diode to deviate from this straight line. This phenomenon is

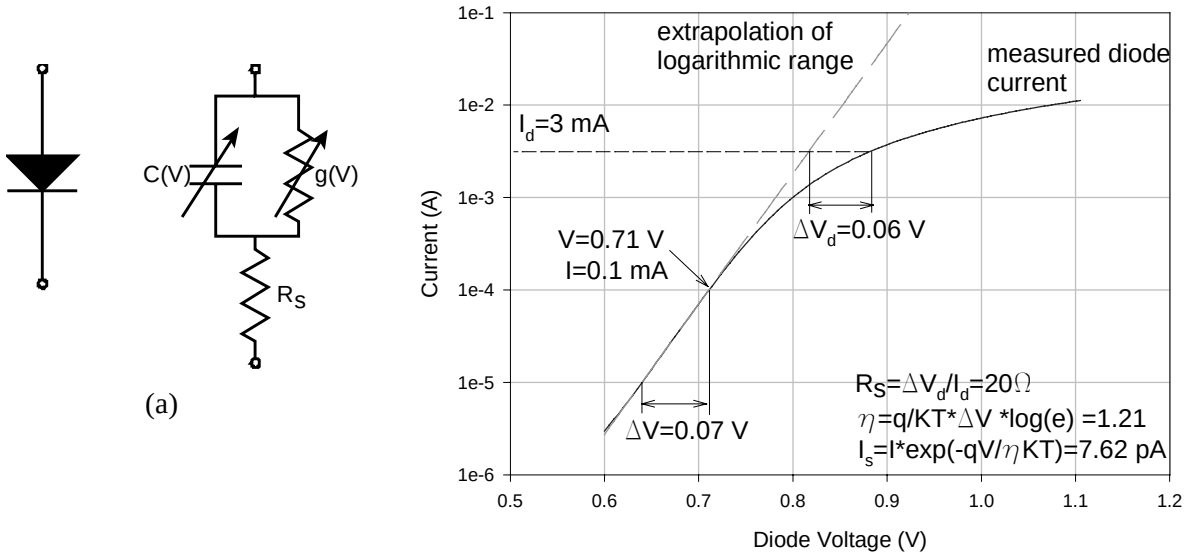


Figure 5.1: (a) Schottky diode equivalent circuit, (b) measured I-V curve for fabricated diode with diode parameters calculated from curve data for T=290 K

evident in the measured data from a Schottky diode fabricated in the M/A-COM mixer diode implant (MDI) process, shown in Figure 5.1 (b). It is then possible to estimate R_s by the equation $\Delta V_d/I_d$, where ΔV_d is the voltage difference between the extrapolated logarithmic current and the measured diode current [11]. The ideality factor (η), and current parameter (I_s) may also be estimated by fitting the logarithmic portion of the I-V curve to the Shockley equation as follows:

$$\eta = \frac{q}{KT}\Delta V \log(e) \tag{5.2}$$

$$I_s = I(V)\exp\left(\frac{-qV}{\eta KT}\right) \tag{5.3}$$

where ΔV is voltage change per decade of diode current. I-V measurements were conducted on a single Schottky diode and three parallel Schottky diodes. The parameters extracted from measurements of for each configuration are shown in Table 5.1. Note that for the three parallel diodes, the extracted R_s is approximately one-third of the single diode R_s. In addition, the I_s is approximately tripled for the case of three parallel diodes due to the fact that three parallel diodes will draw three

	R_s (Ω)	η	I_s(pA)
Manufacturer's data	17.6	1.25	0.2
Measured single diode	20.0	1.21	7.62
Measured 3 parallel diodes	7.2	1.21	25.3

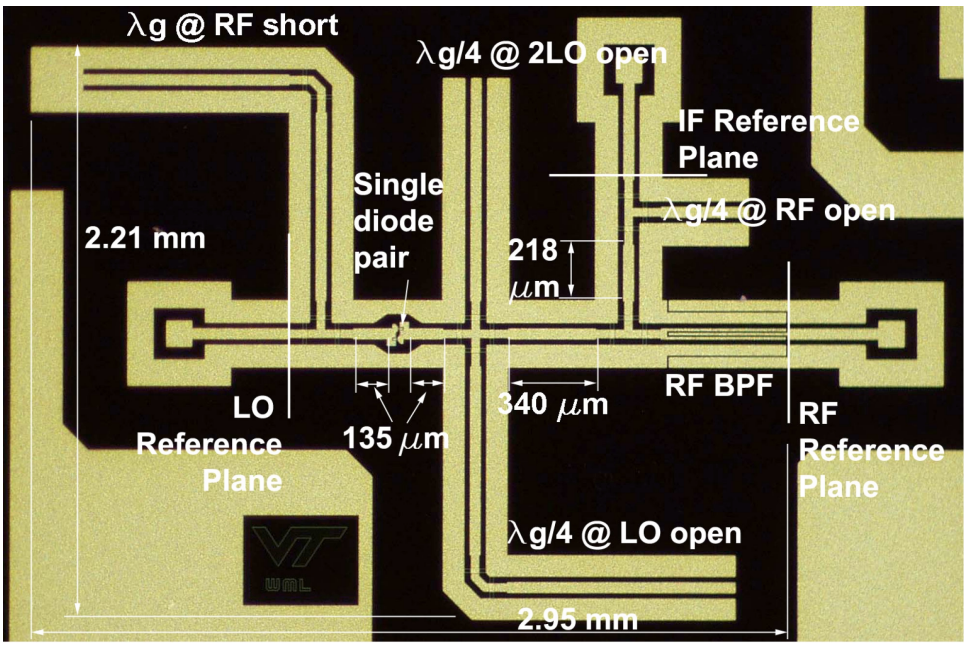
Table 5.1: Schottky diode parameters extracted from measurement compared to manufacturer's data

times the current for a given voltage. The use of three parallel diodes to achieve lower R_s is thus confirmed, although the ultimate validation of this approach will lie in the demonstration of reduced conversion loss as a result of this topology. It must also be noted that the R_s value extracted from the I-V curves is 2.4 Ω higher than what was used for simulations. The measured conversion loss would therefore be expected to be slightly worse than the simulated value for all mixers.

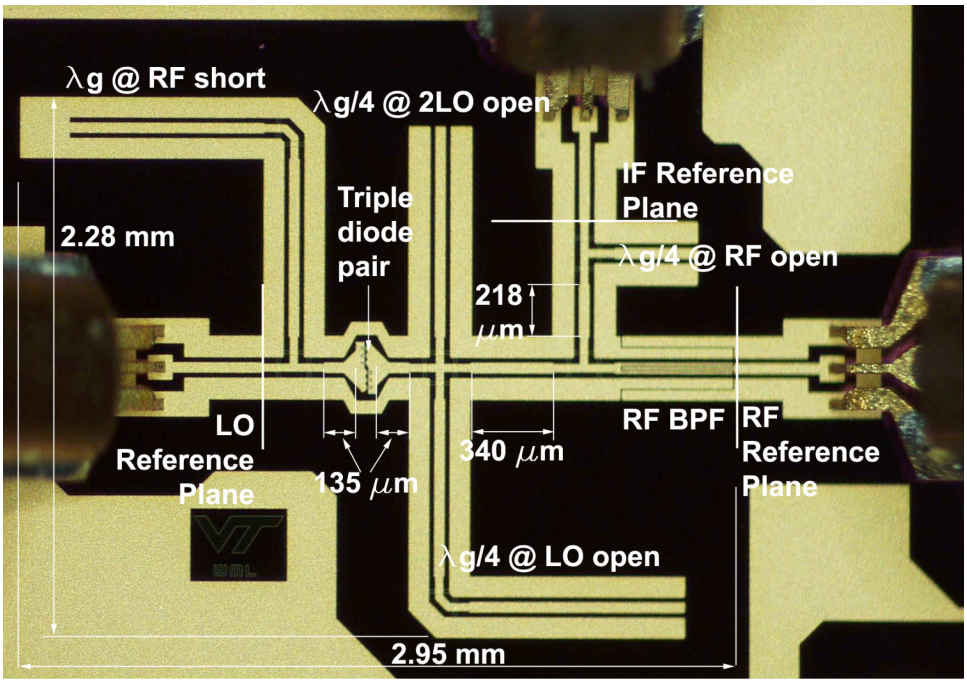
5.2 Conversion Loss Measurements

Photographs of the fabricated mixers are shown in Figures 5.2 and 5.3. The layouts shown in these figures are the MMIC implementation of the mixer designs of Chapter 3 using the FGC stub designs of Chapter 4. The FGC stubs, probe pads, and diodes are connected as specified in Chapter 3 with minimal additional transmission line lengths for spatial separation between circuit components. Unless otherwise noted, all FGC component and probe pad dimensions are as specified in Chapter 4. Any transmission lines added to provide spatial separation between circuit components are indicated and dimensioned.

The conversion loss measurement setup is shown in Figure 5.4. The RF signal is generated by an HPV85104 V-band source module, which provides mm-wave output at a WR-15 waveguide connection over a frequency range of 50-75 GHz. The desired continuous-wave RF frequency and power level is selected using the HP8510C system controller. The source module is connected to a WR-15 directional

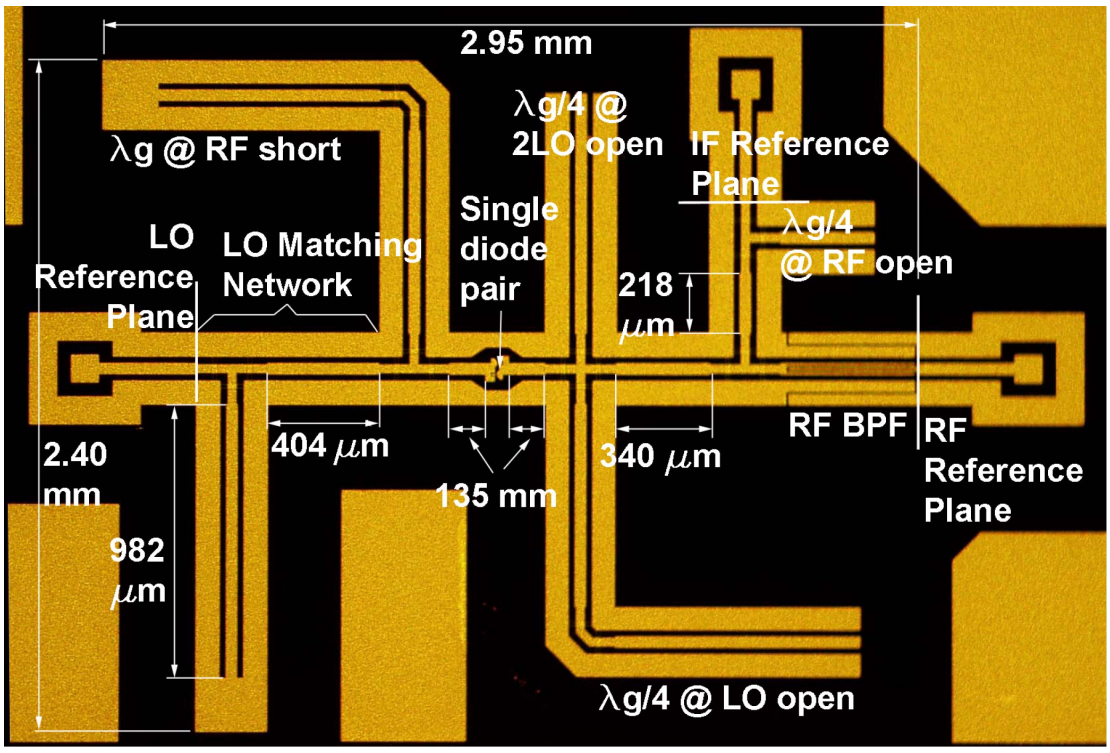


(a)

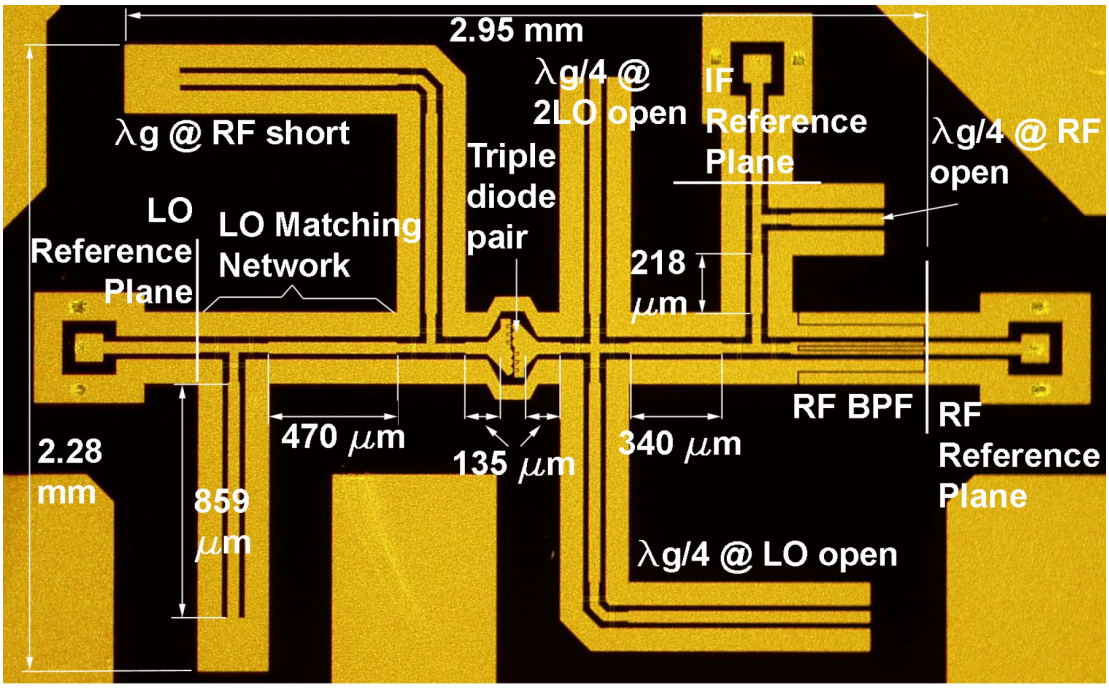


(b)

Figure 5.2: Photographs of fabricated mixers without LO matching networks, (a) single diode mixer, (b) triple diode mixer (with wafer probes on probe pads).



(a)



(b)

Figure 5.3: Photographs of fabricated mixers with LO matching networks, (a) single diode mixer, (b) triple diode mixer.

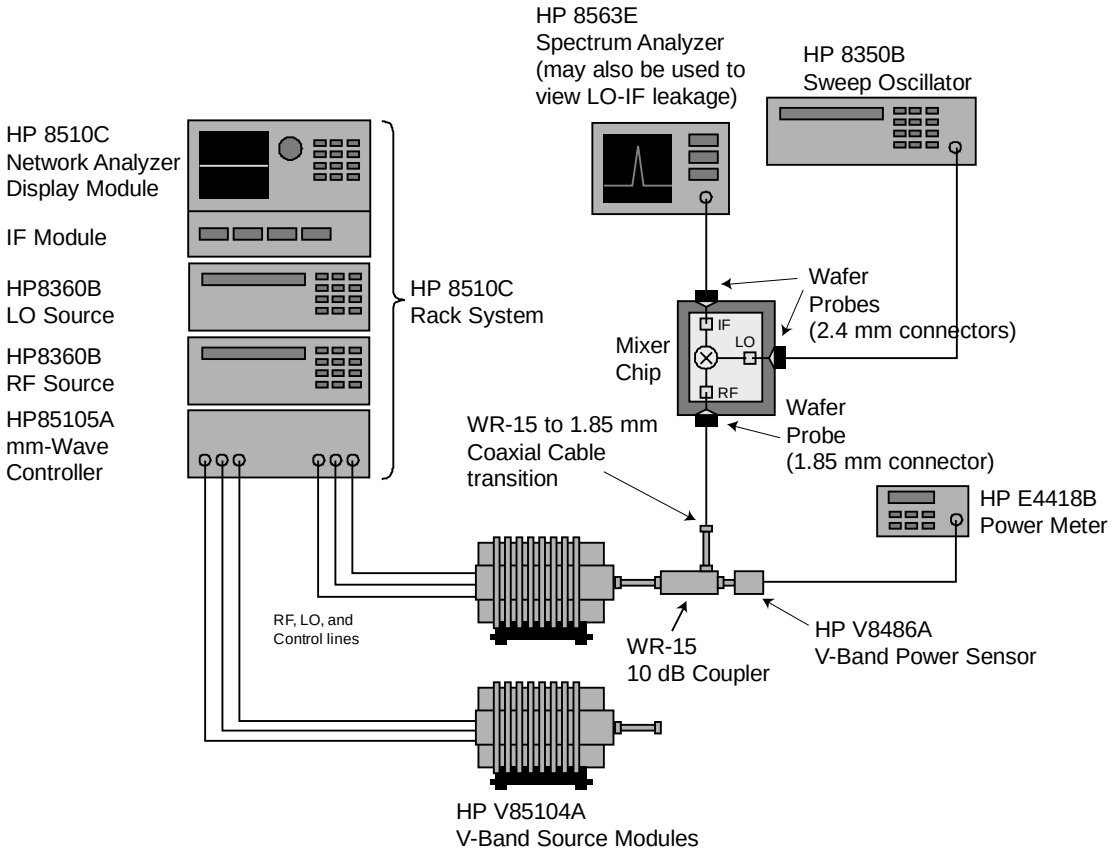


Figure 5.4: Conversion loss test setup for 60 GHz 4X subharmonic mixer

coupler so the signal may be fed to the mixer while RF input power is monitored. The thru port of the coupler (0.7 dB insertion loss) is fed to the waveguide power sensor and the coupled port (10 dB coupling factor) is connected to a WR-15 to V-connector (1.85 mm) transition for connection to the RF wafer probe (1.85 mm connector). The LO signal is generated by an HP 8350B sweep oscillator and connected to a wafer probe (2.4 mm connector) via 2.4 mm cable. The IF output is monitored with an HP 8563E spectrum analyzer connected to the mixer via 2.4 mm cable and wafer probe (2.4 mm connector). Conversion loss measurements are made by comparing the IF power measured at the spectrum analyzer to the RF power measured at the waveguide coupler and subtracting cable losses according to the following equation:

$$L_C(dB) = P_{RF}(dBm) - P_{IF}(dBm) - L_{cables},$$

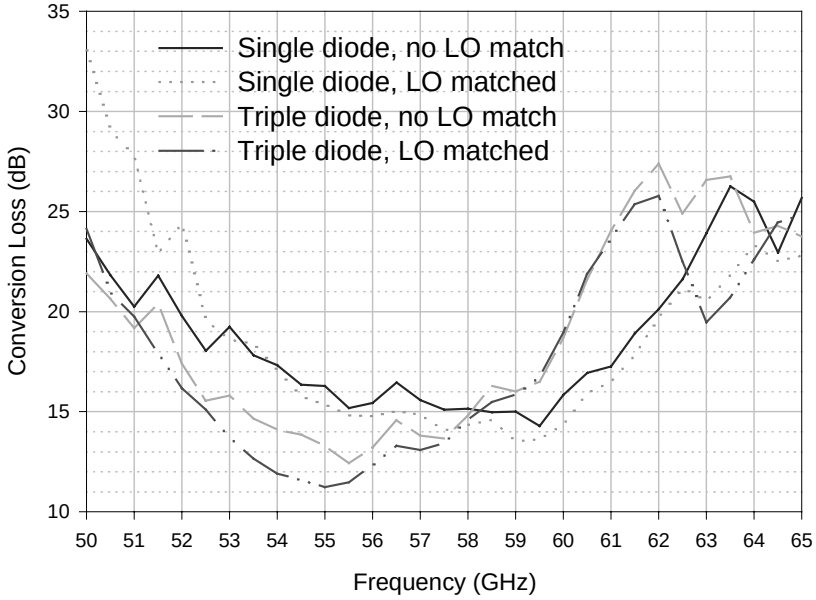
where L_C represents conversion loss and P_{RF} and P_{IF} represent the measured signal power of the RF and IF signals, respectively. The losses of these cables were

	Standard process				No buffer layer			
Diode configuration	Single		Triple		Single		Triple	
LO Matching (Y/N)	N	Y	N	Y	N	Y	N	Y
Optimum LO power (dBm)	6	5	7	7	6	5	6	7
Optimal conversion loss (dB)	14.3	13.5	12.4	11.2	13.8	12.8	12.6	11.3
Optimum loss frequency (GHz)	59.5	59.0	55.5	55.0	60.5	60.5	59.5	58.5
RF Center Frequency (GHz)	57.5	57.5	55.3	55.5	60.3	60.5	59.3	58.5
3-dB conversion loss bandwidth (GHz)	7	7	5.5	5	5.5	5	4.5	5

Table 5.2: Summary of mixer conversion loss performance of Figure 5.5, USB, IF=2.5 GHz.

calibrated out by making a measurement of the loss of each cable type (1.85 mm and 2.4 mm) and wafer probes at their respective frequencies of operation. This measurement was conducted by measuring the S_{21} of the cables and the thru calibration standard (see section 4.4.1) and dividing the measured S_{21} in half. Thus, the losses of each cable were measured from the reference plane of the wafer probe pad to the WR-15 to V-band transition (for the 1.85 mm cable) or to the end of the cable (for the 2.4 mm cable).

Measured conversion loss is plotted for each mixer variant in Figure 5.5 and summarized in Table 5.2. Measured data for the unthinned wafer with no buffer layer has been omitted since this process variation was found to exhibit nearly identical performance to the 125 μm wafer with no buffer layer. As expected from the FGC stubs measured in Chapter 4, the mixer fabricated in the standard process (125 μm wafer with polyimide buffer layer) is tuned approximately 3-4 GHz lower than the mixer with no buffer layer. Both wafer process variations provide comparably low



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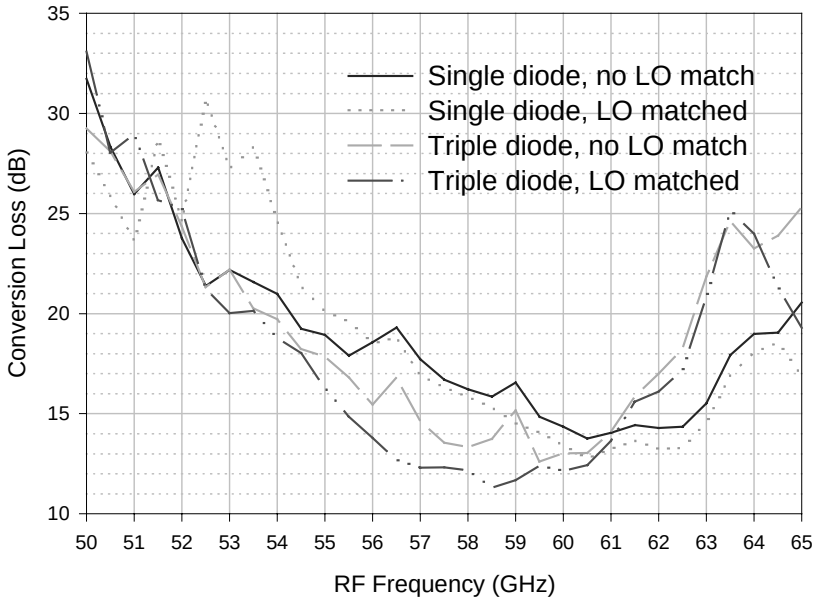


(b)

Figure 5.5: Measured conversion loss of mixers at respective optimum LO drive levels, USB, IF=2.5 GHz: (a) standard process (125 μm wafer with polyimide buffer), (b) process variation with no polyimide buffer

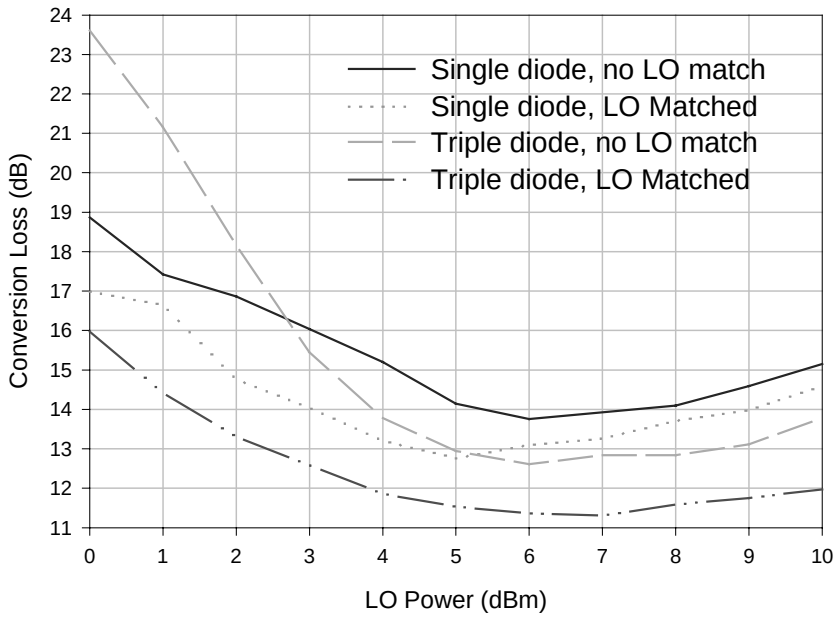
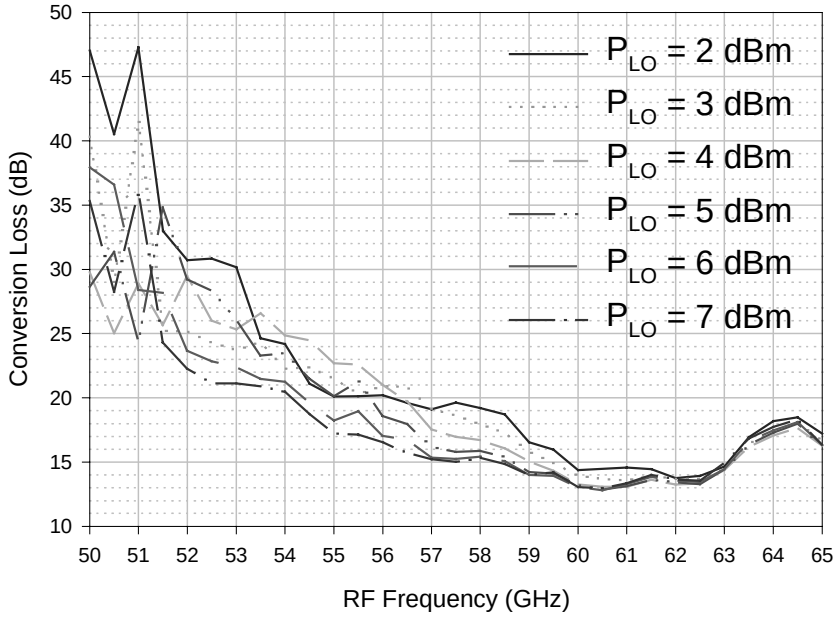


Figure 5.6: USB conversion loss vs. LO power at optimum respective RF frequency for mixers with no buffer layer, IF = 2.5 GHz

minimum conversion loss at their respective frequencies. The mixers in both process variations are tuned lower in frequency than their respective stub resonant frequencies from section 4.4.3. This observation is particularly notable for the case of the triple diode mixers. The likely cause of this effect is parasitic capacitance in the physical diode layout. The fact that the triple diode pair layout covers a broader width (see Figures 5.2 and 5.3), the potential for parasitic capacitive coupling across the diode pair is increased. This explains the more significant degradation in gain as frequency increases for the mixers with the triple diode pair. Based on the fact that the process variation with no buffer layer provides good performance at the target frequency of 60 GHz, all mixer results henceforth will focus on this process variation. Figure 5.6 shows a plot of measured conversion loss vs. LO drive level at the respective optimum conversion loss frequency of each mixer variant (given in Table 5.2). The values shown here are 1-2 dB worse than the simulated values for each case. The difference is most likely primarily due to the higher series resistance of the measured Schottky diodes than that used in simulation. Other lesser contributors to the difference between simulated and measured loss are the losses in non-ideal



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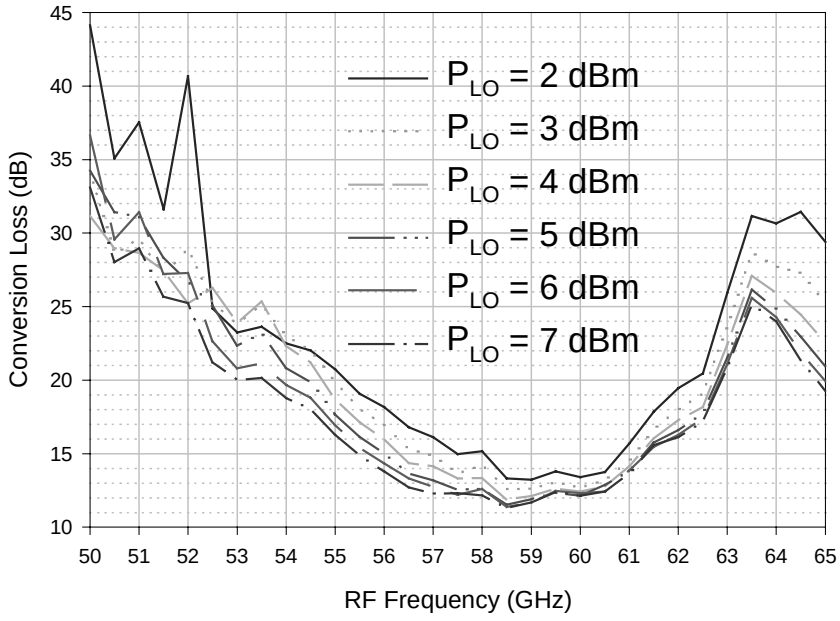


(b)

Figure 5.7: USB conversion loss vs. RF frequency for 125 μm wafer with no buffer layer, IF = 2.5 GHz, (a) single diode mixer, (b) triple diode mixer

transmission lines and T-junctions.

The utility of the LO matching networks may be assessed by comparing the conversion loss with and without LO matching networks. In the case of the single diode mixer, the benefit of the LO matching network is evidenced by a 1-dB improvement in conversion loss and a shift in optimum LO power from 6 to 5 dBm. A similar effect is seen in the conversion loss of the triple diode mixers, which show a conversion loss improvement of more than 1 dB resulting from the addition of the LO matching network. An additional benefit is offered in that the conversion loss the mixer can operate with fairly low conversion loss over a wider range of LO powers due to the addition of an LO matching network. Figure 5.6 shows that although the optimum LO drive level occurs at 7 dBm for the LO matched triple diode mixer, the conversion loss is better than 13 dB for drive levels as low as 2.5 dBm. On the other hand, in the unmatched case, the conversion loss degrades drastically below 4 dBm. It is evident from the presented conversion loss data that the triple diode mixer with LO matching provides the best conversion loss, and that its performance is competitive with that of the other mixer variants at LO drive levels as low as 2 dBm.

Figure 5.7 shows the effects of various LO drive levels on the frequency response of the LO-matched mixers with no buffer layer. This graph shows that the effect of sub-optimum LO drive level on conversion loss is uneven across the 3-dB bandwidth of both mixers. Over a smaller bandwidth, however, both mixers with LO matching are capable of a fairly constant conversion loss (± 1 dB) over a relatively wide range of LO drive levels. For an LO power range of 3 to 7 dBm, the LO matched single diode mixer is capable of lower than 14 dB conversion loss over the RF range of 60-62.5 GHz (Figure 5.7 (a)). Over the same LO power range, the LO matched triple diode mixer is capable of lower than 13 dB conversion loss over the RF range of 58.5-60.25 GHz (Figure 5.7 (b)). In this research, mixers are measured at a discrete continuous-wave (CW) frequency. In application, however, these receivers would most likely operate over a wide RF band (1-2 GHz). Therefore, the power converted to IF will not lie at a single frequency, but rather distributed over the receiver bandwidth. It is

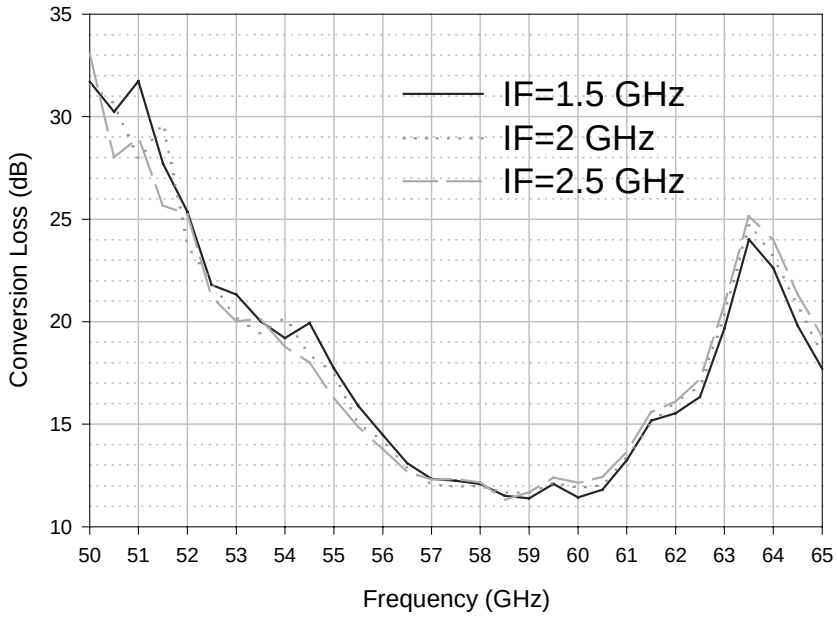
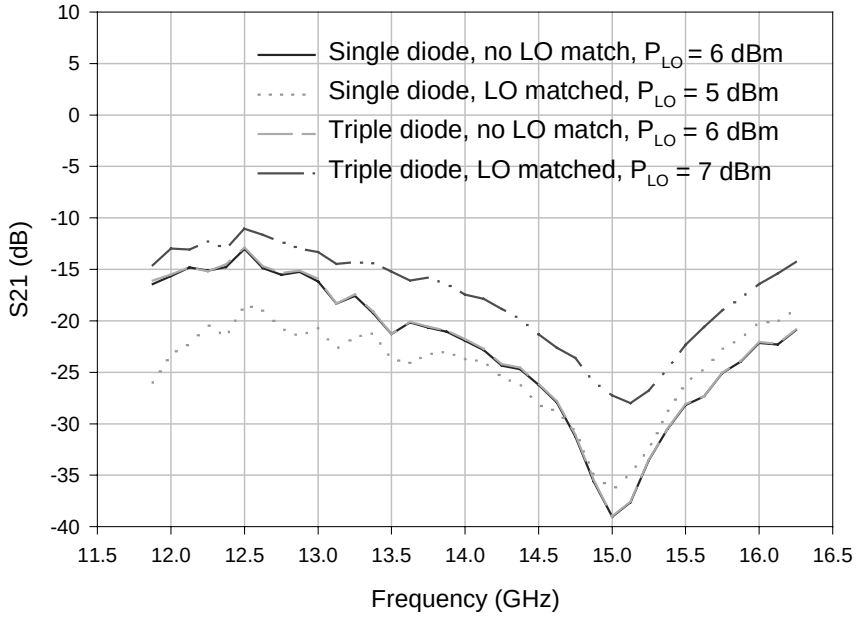


Figure 5.8: USB Conversion loss vs. RF frequency for various IFs, triple diode mixer with no buffer layer, LO power = 7 dBm

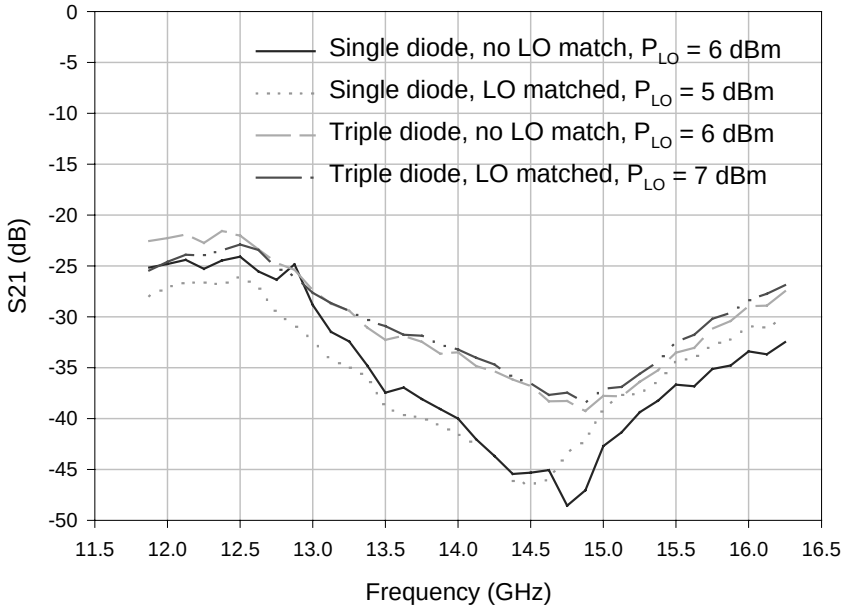
therefore also desirable to verify that the conversion gain response is reasonably flat over IF frequency so that the spectrum of the received band is not distorted. To confirm this, the conversion loss measurements have been performed at optimal LO drive levels for IF frequencies of 1.5 GHz, 2 GHz, and 2.5 GHz. The results indicate that conversion loss remains approximately the same for every IF in this range. The conversion loss of the LO-matched triple diode mixer is plotted for each of these IF values in Figure 5.8. The other mixer variants show similar insensitivity to the choice of IF frequency within this range.

5.3 Isolation Measurements

Isolation measurements have been performed with a similar test setup as the conversion loss setup. The LO-IF measurement setup is identical to the conversion loss setup, but the spectrum analyzer is used to measure the power of the LO signal leaking to the IF port instead of the IF signal. For LO-RF isolation measurement, the



(a)



(b)

Figure 5.9: Isolation vs. frequency at optimum LO drive levels for wafers with no polyimide buffer (a) LO-IF, (b) LO-RF

spectrum analyzer is connected to the RF input port and the IF port is terminated with a wideband 50Ω load. In each case, the LO port is fed with the optimum LO drive level (indicated in the legend) for the particular mixer variant measured. All measured mixers are on 125 μm wafers with no polyimide buffer layer.

Figure 5.9 (a) shows the measured LO-IF isolation for the mixer vs. frequency. The greatest isolation coincides with the resonant frequency of the LO $\lambda_g/4$ open-circuit stub. This stub is mistuned to about 15 GHz instead of 14.375 GHz (f_{LO} for RF=60 GHz and IF=2.5 GHz, USB). Therefore, the greatest isolation occurs outside of the desired band of operation. While both the single and triple diode mixers display identical isolation over frequency, the two mixers with LO matching networks show significant variation in isolation values. Over the LO frequencies required to access the full 3-dB RF bandwidth of each mixer (14-14.5 GHz), the LO-IF isolation has a worst-case value of about 17 dB for the LO-matched triple diode mixer. All other mixer variants have isolation of better than 22 dB over the frequencies of operation.

The LO-RF isolation is shown in Figure 5.9 (b). This isolation shows the same dependence on the frequency response of the LO $\lambda_g/4$ stub, but the isolation is much higher than the LO-IF isolation. This is expected because the LO-RF path includes 10-15 dB of additional attenuation due to the RF filter rejection at the LO frequency. The triple diode mixers have about 5-dB worse isolation than the single diode mixers. The LO-RF isolation for all mixer variants, however, is better than 33 dB for all frequencies of operation.

	Min	Max
Operating Frequency (GHz)	58.5	60.5
LO Power (dBm)	3.0	10.0
Conversion Loss (dB)	11.3	13.2
LO-IF Isolation (dB)	17.5	23.6
LO-RF Isolation (dB)	33.2	37.5

Table 5.3: Operating conditions and performance for triple antiparallel diode 4X subharmonic mixer with LO matching network on 125 μm GaAs substrate with no polyimide buffer layer

5.4 Summary of Test Results

The measured results in this chapter represent a thorough characterization of the designed 4X 60 GHz subharmonic mixer. Based on the presented data, it is apparent that the mixers fabricated on a 125 μm substrate with no buffer layer offer the best conversion loss for 60 GHz operation. Simulated data in section 3.4 shows that for the triple diode mixer with LO matching, conversion loss is flat from about 55 to 60 GHz for tuning stubs tuned to an RF of 60 GHz. Therefore, the simulations indicate that the mixer will function well as low as 5 GHz below the RF stub resonant frequency. This implies that the mixer with no buffer layer (stubs optimized for 64 GHz) should operate well as low as 59 GHz. However, measurements have indicated a degradation across that band due to some presumed parasitic capacitance near the diodes. Therefore, the excellent mixer operation displayed by the triple diode mixers at 60 GHz would follow the simulated data. The parasitic capacitance, however, prevents the measured mixers from displaying low conversion loss at the RF frequencies at which the stubs are optimized (60 and 64 GHz for the wafers with and without buffer layers, respectively).

Among the mixer variants on this process variation, the triple diode mixer with LO matching clearly offers the best conversion loss and most flexibility in choice of LO

power. A summary of performance at the optimum operating conditions is provided in Table 5.3. Although the optimal LO drive level agrees well with simulated data, the conversion loss is 1-3 dB worse than predicted in simulation, depending on RF frequency. The difference between the simulated and measured values may be attributed to several factors:

- Measured series resistance (R_s) of the diodes (20 Ω) is higher than the values used in simulation (17.6 Ω). Diode series resistance is a key attribute affecting the conversion loss of Schottky diode mixers.
- Mistuning of LO and RF tuning stubs to incorrect frequencies as described in Chapter 4, resulting in less than optimal terminations at the desired frequencies of operation.
- The ideal transmission lines used in simulation have zero line attenuation. The implemented FGC lines have nonzero attenuation that is most significant at RF (0.3 dB/mm). Nonideal losses such as junction and discontinuity effects and radiation losses in the FGC lines could contribute additional loss, as well.

The dominant mechanism contributing to worse conversion loss than was simulated is the Schottky diode series resistance. Improved Schottky diode processes are capable of yielding R_s values below 10 Ω, which would improve conversion loss. In addition to this improvement, the mistuning of the RF and LO stubs could be corrected in subsequent revisions by a simple adjustment of stub length. The remaining loss mechanisms listed are unavoidable realities of mm-wave design. Fortunately, their contributions to conversion loss are probably the least significant of all.

CHAPTER 6
CONCLUSIONS AND FUTURE WORK

This chapter concludes the research work presented in this thesis. The objective of this work was to realize a uniplanar 60 GHz 4X subharmonic mixer for future integration in a monolithic receiver front-end. The subharmonic mixer topology is intended to offer comparable system performance to other common methods of 60 GHz downconversion with the advantage of reduced local oscillator (LO) frequency. The motivation behind this work is to present a viable solution to one of many challenges facing the prospective designer of an integrated 60 GHz receiver.

6.1 Conclusions

Of the mixer designs presented in this thesis, the triple diode mixer with LO matching offers the best performance toward fulfillment of the objectives of this research. This design variant achieved a minimum conversion loss of 11.3 dB, with a maximum conversion loss of 13.2 dB over the frequency range 58.5-60.5 GHz. The mixer was shown to operate with a fairly constant conversion loss over a wide range of LO powers, from 3 dBm to 10 dBm. Integrated oscillators at 15 GHz that can provide this power are well within the realm of possibility, especially since an LO buffer is almost certain to be used in any practical implementation. Furthermore, phase-locked loops (PLLs) are more practical at 15 GHz than at 60 GHz.

Table 6.1 shows several recently published results on 60 GHz downconversion mixers. The performance achieved in this work is quite competitive with other subharmonic mixers at this frequency. In fact, the measured conversion loss is lower than some passive 2X subharmonic mixers. Although fundamental mixer topologies display better conversion gain than the mixer in this work, this is to be expected. Use of a subharmonic mixer constitutes a straightforward tradeoff between conversion loss and the convenience of a relatively low-frequency local oscillator.

Mixer Topology	Active or Passive	LO mixing harmonic	Maximum Conversion Gain (dB)	LO Power (dBm)	Reference
Image reject MESFET	Active	Fundamental	1	5	[43]
Source injected FET	Active	Fundamental	0	7	[44]
Gate injected HEMT	Active	Fundamental	5	4.5	[45]
Drain-injected HEMT	Passive	Fundamental	3.7	10	[46]
Resistive HEMT	Passive	Fundamental	-7.7	5	[46]
Dual-gate HFET	Active	Fundamental	-5	5	[47]
Antiparallel diode	Passive	2^{nd}	-14	-3	[48]
Antiparallel diode	Passive	2^{nd}	-12	8	[32]
Antiparallel diode	Passive	4^{th}	-11.3	7	This work

Table 6.1: Summary of recently reported 60 GHz downconversion mixer performance

The conversion loss performance of this mixer is on par with other passive mixers topologies currently used for downconversion at 60 GHz. Subsequent design iterations of this mixer, however, would certainly provide better conversion loss performance than this initial attempt. This circuit, coupled with an integrated high-gain LNA and a relatively low-frequency integrated oscillator (14-15 GHz), offers the possibility of achieving excellent performance in a 60 GHz integrated receiver.

Several system considerations are necessary in the implementation of a full receiver chain with the LO-matched triple diode mixer. The LO-IF isolation, for example, is 15-25 dB, which is likely to be inadequate for most applications. With an LO power on the order of 0 dBm, the LO signal leaking through to the IF output will almost always be much greater in amplitude than the IF signal. In order to avoid saturating the IF amplifier, additional filter will almost certainly be necessary if this isolation is not improved in subsequent revisions. The LO-RF isolation is greater than 33 dB for all frequencies, including the LO rejection provided by the implemented RF filter. In practice, however, this filter may be rendered unnecessary by an image reject filter between the LNA and mixer. This RF image-reject filter is likely to provide

significant rejection at the LO frequency, which will provide additional isolation between the LO and LNA output. This will reduce the risk of degrading LNA performance due to excessive LO signal amplitude at its output.

6.2 Future Work

Several modifications may improve the performance of the 60 GHz 4X subharmonic mixer in subsequent revisions. It is evident from the isolation data shown in Chapter 5 that the frequencies at which maximum LO-IF and LO-RF isolation values occur do not coincide with the frequencies at which the best conversion loss occurs. The maximum rejection provided by the open-circuited $\lambda_g/4$ LO stubs should coincide with the optimum operating frequency of the mixer. This can be accomplished by modifying the FGC transmission line simulations in Chapter 4 to more closely approximate the measured results (often called a "backfit" in the MMIC industry). This will result in a more accurate prediction of stub resonant frequency and LO matching network performance in subsequent chip revisions. This also ensures that the resonance presented by the stubs to the diodes occurs at the correct frequency, possibly improving conversion loss. Using an improved Schottky diode process could also provide significant performance improvements. The series resistance (R_s) of the diode is relatively high compared to state-of-the-art devices, which offer R_s values below 10 Ω.

In addition, several experiments using different subharmonic mixer topologies are recommended. The addition of a DC bias network to the passive antiparallel diode structure could allow even lower LO drive levels than achievable with the unbiased antiparallel pair. The difficulty in this would be to break the antiparallel connection between the two diodes at DC so that they could be individually forward-biased while maintaining the equivalent AC circuit of the diodes at the LO, RF, and IF frequencies in an antiparallel configuration. An example of a possible scheme for an antiparallel diode pair DC bias is shown in Figure 6.1.

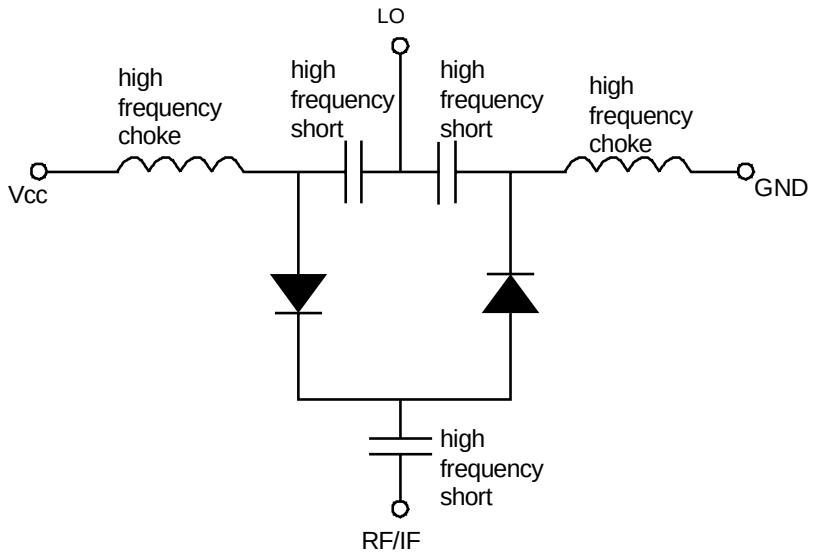


Figure 6.1: Possible DC bias scheme for antiparallel diode pair

An investigation into active 4X subharmonic mixing topologies could provide a solution to the disadvantage of relatively high conversion loss shown by passive subharmonic mixers. Further investigations into topologies such as balanced mixers and image rejection mixers could prove useful, as well. Any of these ideas implemented in an active topology could significantly improve conversion loss, making the use of subharmonic mixers at high frequencies even more attractive.

APPENDIX A
A COMPACT, SECOND ORDER 60 GHZ BANDPASS FILTER IN FINITE GROUND COPLANAR WAVEGUIDE

The 60 GHz 4X subharmonic mixer design in Chapter 3 requires an FGC bandpass filter in order to facilitate the required conversion loss measurements. This filter serves the purpose of coupling the RF port to the diode pair without loading the IF output port. Therefore, the filter must have low insertion loss at 60 GHz and present an open-circuit at the IF frequency of 2.5 GHz. Significant rejection of the LO frequency of 14.5 GHz is also a secondary design goal. Since the bandpass frequency and the unwanted frequencies (IF and LO) are widely separated, good rejection of the unwanted frequencies is fairly easy to attain using low order filters. The center frequency of the filter is to be 60 GHz, which allows filter implementation with resonant tuning stubs that are small enough to fit on a reasonably sized die. An FGC tuning stub configuration that is particularly useful in this application is the open-circuit series stub. These stubs are known to have a bandpass response centered where the stub length is equal to one-quarter of a guided electrical wavelength. Below this center frequency, the stub appears as a series capacitance. The filter may then be designed such that the RF frequency falls in the passband and the capacitive impedance presented at the IF and LO frequencies is large enough to provide significant rejection to those signals.

When implemented in conventional CPW, series open-circuit stubs are fabricated in the center conductor. An interesting feature of FGC lines is that series elements may be fabricated not only in the center conductor, but also in the ground conductors, as well. An investigation into performance differences between series open-circuit stubs in the center and ground conductors of FGC lines is made in this appendix. The design, simulation, fabrication, and measurement of a series open-circuit stub filter suitable for the above mixer implementation are presented.

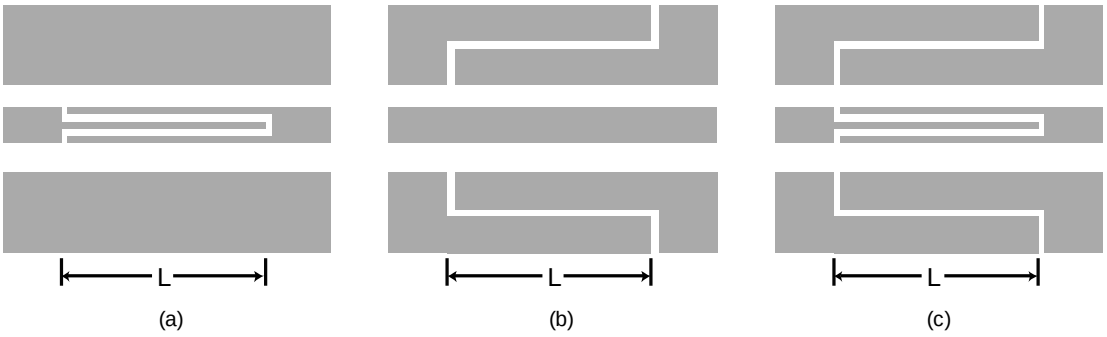


Figure A.1: Series FGC Open-circuit Stubs (a) in center conductor, (b) in ground conductors, (c) in both center and ground conductors.

A.1 Design of Series Open-Circuit Stubs in FGC

Series open-circuit stubs in CPW have been characterized theoretically and experimentally in several publications, [49], [50], [16]. A typical layout for a series open-circuit stub in the center conductor is shown in Figure A.1 (a). In FGC lines, the stubs may be fabricated in the center conductor, the ground conductors (Figure A.1 (b)), or both (Figure A.1 (c)). Previous studies indicate that the *impedance* of stubs is approximately the same regardless of whether they are fabricated in the center conductor or ground conductor [16]. However, since implementation in the ground conductor requires one stub in each ground plane, they must be viewed as two parallel stubs. The implications of this will be discussed with the simulated results. For both center conductor and ground conductor stubs, the resonant frequency is given by the formula:

$$f_r = \frac{c}{4L\sqrt{\varepsilon_{eff}}}, \tag{A.1}$$

where c is the speed of light, ε_{eff} is the effective dielectric constant of the transmission line, and L is the physical length of the stub. This formula indicates that the resonant frequency occurs where the physical length of the stub is equal to one-quarter of a guided electrical wavelength ($\lambda_g/4$). The filters were designed using the standard 50-Ω FGC transmission line dimensions as described in section 2.2. The physical stub length was chosen to equal $\lambda_g/4$ at 60 GHz. Figure 2.4 indicates that at 60 GHz, the

simulated effective permittivity of a standard FGC line is about 7.05. Using this value of permittivity, Equation 2.1 indicates that $\lambda_g/4$ is approximately equal to 470 μm at 60 GHz. The dimension L as indicated in Figure A.1 was therefore set to equal 470 μm. The width of the center stubs and slots dividing the center stubs were arbitrarily chosen as 5 μm. The slots separating the ground conductor stubs were chosen to be 5 μm to equal the dimension of the center stubs. This resulted in a ground plane stub width of 40.5 μm.

A.2 Simulation and Measurement

The three different filter variations were simulated using Zeland IE3D for the dimensions designed in the previous sections. The simulated filter S-parameters are shown in Figures A.2 and A.3. Figure A.2 (a) indicates that each filter produces the desired response, i.e. rejection at low frequencies and low insertion loss at the 60 GHz center frequency. The rejection of the filter with the stubs in the ground plane is the worst of all three. This is due to the fact that at low frequencies, the series stubs present a large negative (capacitive) reactance, causing rejection of signals at these frequencies. For the case of the ground plane stubs, the reactances presented by each ground stub are in parallel, effectively halving the reactance presented outside the filter passband. Thus, out-of-band filter rejection is worse for the filter with only ground plane stubs. The filter with stubs in both the center and ground conductors represent an effective cascade of a filter in the center conductor (forward signal path) and a filter in the ground conductor (return signal path). Therefore, the filter combines the rejection of both the center and ground conductor stubs at low frequencies. An additional disadvantage exists, however, of cascading the passband insertion loss. The S_{11} and S_{22} at various frequencies are shown in Figure A.2 (b). This verifies that below about 10 GHz, the filter presents an approximate open-circuit at either port. This plot also indicates that the filter presents a capacitive impedance below resonance and an inductive impedance above resonance. These data were modeled with an equivalent circuit as shown in Figure A.3 for mixer simulations in section 3.4. The parameters for each of these components were tuned iteratively until

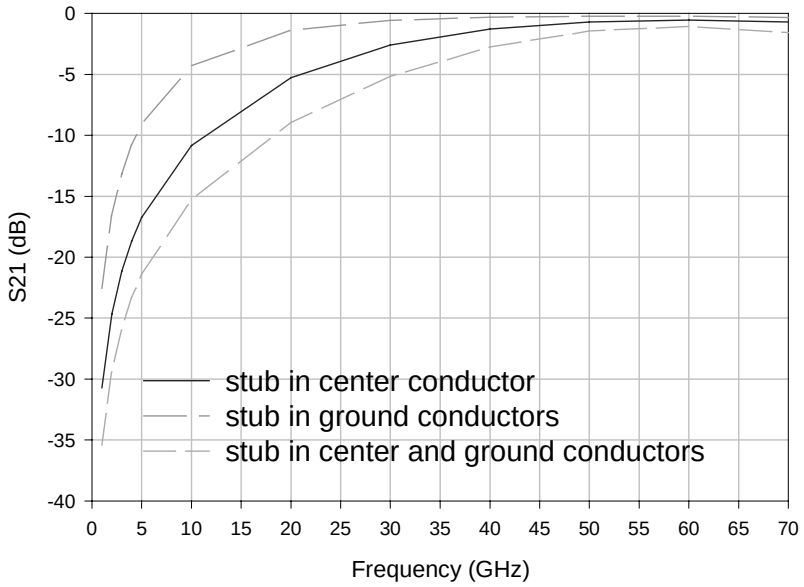


Figure A.2: Simulated transmission coefficient of series open-circuit RF stubs for various stub configurations

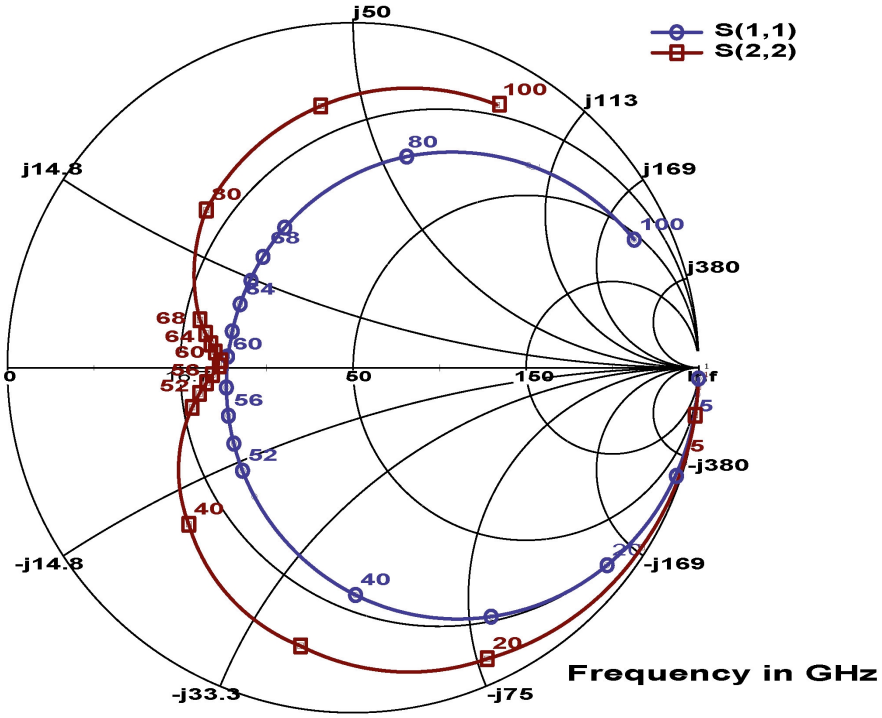


Figure A.3: Simulated S_{11} and S_{22} of series open-circuit RF stubs for various stub configurations

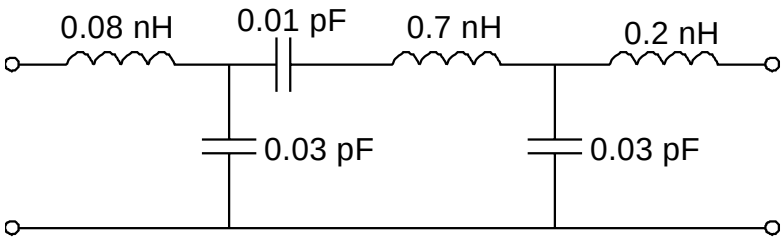
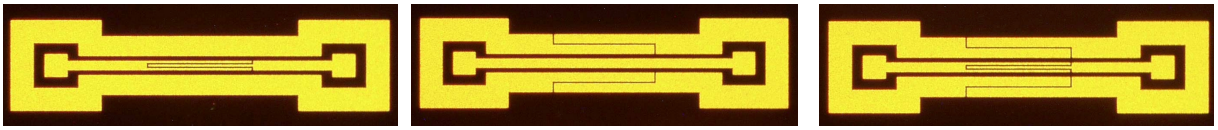


Figure A.4: Equivalent L-C model of series open-circuit FGC stub with stubs in both center and ground conductors with center frequency at 60 GHz



(a) (b) (c)

Figure A.5: Photographs of fabricated stubs with probe pads, (a) stub in center conductor, (b) stubs in ground conductor, (c) stubs in center and ground conductors

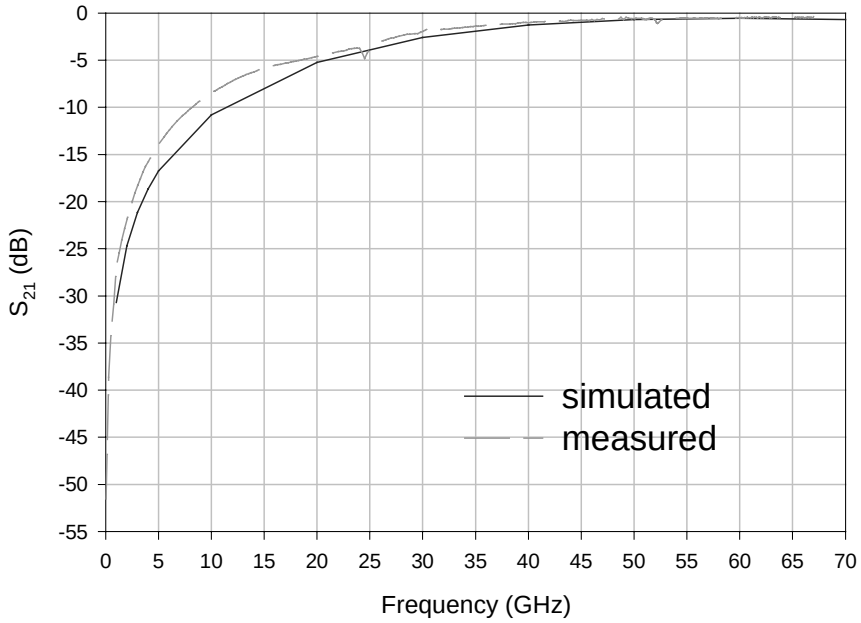
the circuit was found to reasonably approximate the simulated performance of the series stub in both the center and ground conductors.

The dimensions designed in section A.1 were used to fabricate stubs in the M/A-COM MSAG 5 process as described in Chapter 2. Photographs of the actual fabricated filters are shown in Figure A.4. Filter variations include a version with a stub in the center conductor (a), stubs in the ground conductors (b), and stubs in both the center conductor and ground conductors (c). Each of these structures was characterized with full 2-port S-parameter measurements using an HP 8510C network analyzer. The effects of the probe pads shown in Figure A.4 were calibrated out using NIST's Multical TRL calibration software [42]. The measured and simulated transmission coefficients of each variant are shown in Figure A.5.

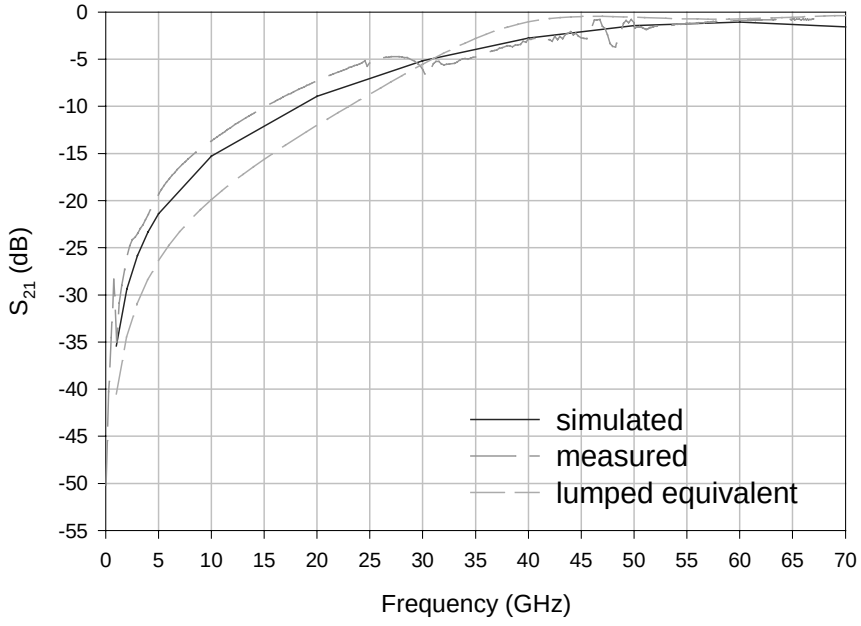
The measured rejection at the LO and IF frequencies is slightly worse than predicted by simulation in each case, but both the simulated and measured insertion losses at 60 GHz are all in good agreement. It is apparent from the test data that the filter with

stubs in the center and ground conductors offers slightly better rejection below resonance than the other filter variations. The simulated and measured 60 GHz insertion loss of the filter with center and ground conductor stubs were 1.1 and 0.9 dB, respectively. The lumped element approximation displays a 60 GHz insertion loss of 0.7 dB (plotted in Figure A.5 (b)). Based on these observations, this filter variation is chosen for mixer implementation in Chapter 5.

An additional comment must be made regarding the measurement setup used to test these filters. It can be noted in the measured transmission coefficient of circuits with stubs in the ground plane that at low frequencies (< 5 GHz), several spikes are present in the plotted data. This is because the principle of operation of these filters dictates that at low frequencies, the return signal path in the ground plane is interrupted by the capacitive reactance presented by the stub, thereby rejecting signal transmission at those frequencies. In a single-ended measurement system such as a network analyzer, the common (signal ground) terminal of each port is connected to a system ground bus (earth ground). This represents an alternate signal return path, undermining the rejection provided by the capacitive reactance in the ground plane of the FGC line. At low frequencies, this system ground connection provides a path for ground currents that undermines the ground path rejection in the FGC stub structure. At higher frequencies, the measurement error due to this phenomenon is not as important since the ground stubs present a low impedance at those frequencies, thereby providing a dominant ground path within the FGC line itself. In order to accurately measure the characteristics of these stubs at low frequencies, a multiport network analyzer must be used which can isolate the device-under-test (DUT) ground return path from the test system ground return path. This phenomenon must also be considered in any system implementation of this filter, since the system ground bus present in most radio receivers would offer a similar alternate ground path to the series open circuit stub in the FGC ground plane.



(a)



(b)

Figure A.6: Transmission coefficient of series open-circuit $\lambda_g/4$ @ RF stub on 125 μm wafer with no buffer layer (a) in center conductor, (b) in center conductor and ground conductors

APPENDIX B
MIXER SIMULATIONS IN LIBRA

This appendix provides detail on the simulations used to predict mixer performance during the design phase in Chapter 3. These simulations were performed with HP EESof Libra v.6.6 [18] simulation software. The simulated mixer schematics and the test conditions for the harmonic balance analysis are described herein.

The schottky diode was simulated as the standard nonlinear diode element with the M/A-COM diode parameters in Table 3.1. All stub elements are modeled as ideal elements as described in Chapter 3 and the RF bandpass filter was modeled as a lumped element equivalent circuit, as described in Appendix A.

An ideal directional power sampler (DPWRSMP) is used to sample frequency-selective forward and reverse voltage amplitudes at each port. From these measurements, port s-parameters and conversion loss at any frequency can be tested.

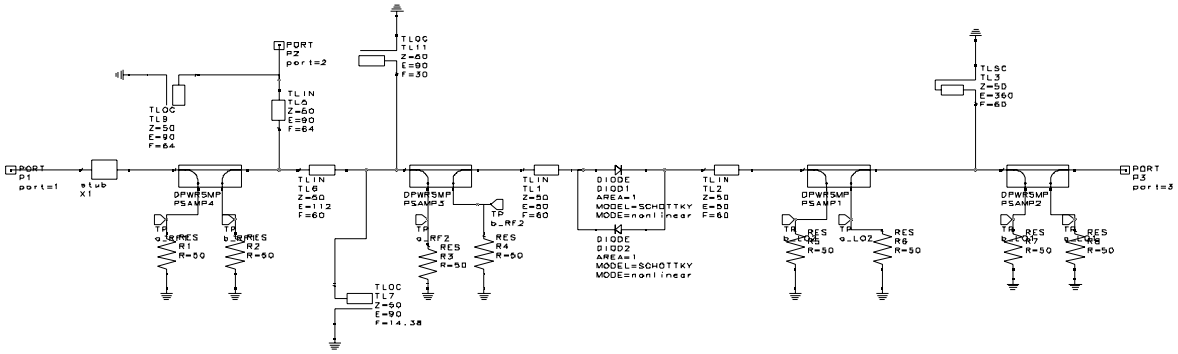


Figure B.1: Libra schematic of single antiparallel diode pair mixer

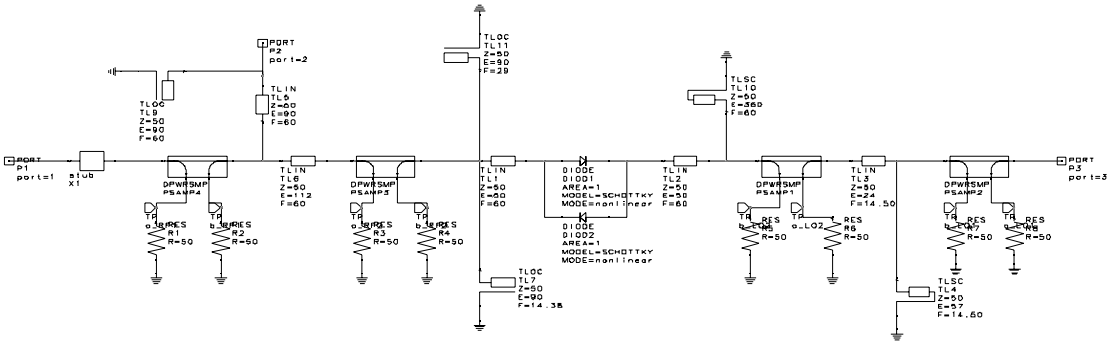


Figure B.2: Libra schematic of single antiparallel diode pair mixer with LO matching network

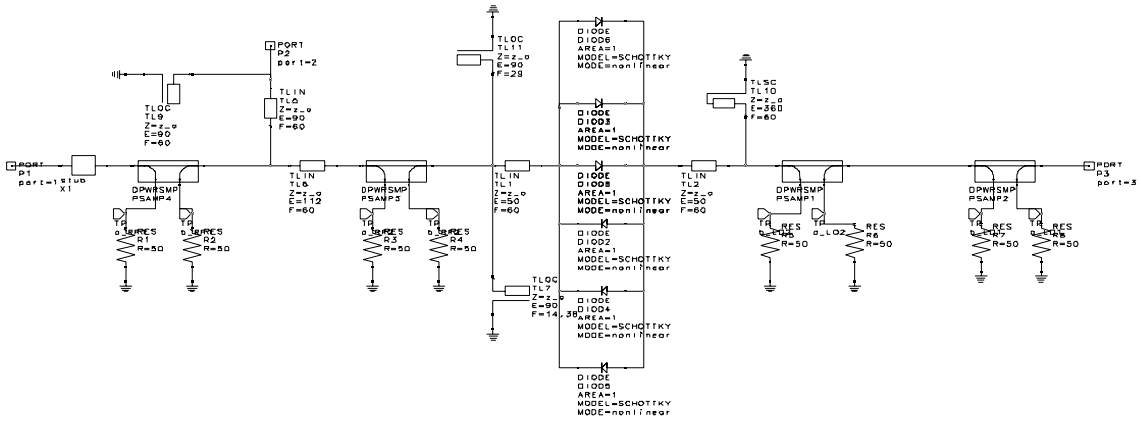


Figure B.3: Libra schematic of triple antiparallel diode pair mixer

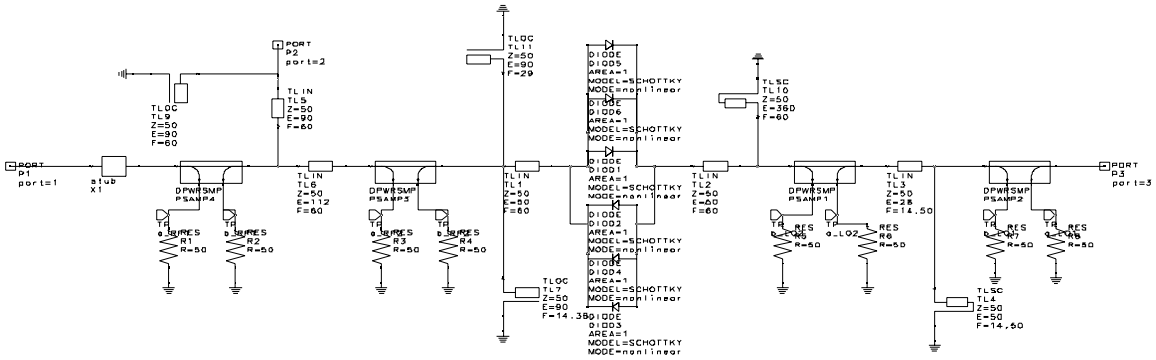


Figure B.4: Libra schematic of triple antiparallel diode pair mixer with LO matching network

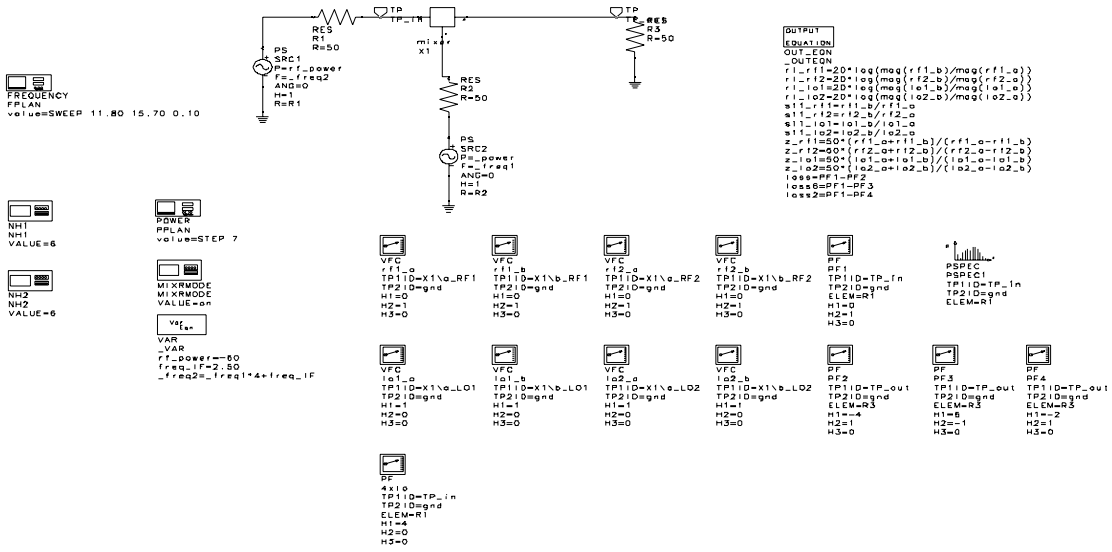


Figure B.5: Libra harmonic balance test bench for 4X subharmonic mixer

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