# SINGLE PHASE POWER FACTOR CORRECTION CIRCUIT WITH WIDE OUTPUT VOLTAGE RANGE

by

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(ABSTRACT)

The conventional power factor correction circuit has a fixed output voltage. However, in some applications, a PFC circuit with a wide output voltage range is needed. A single phase power factor correction circuit with wide output voltage range is developed in this work.

After a comparison of two main power stage candidates (Buck+Boost and Sepic) in terms of efficiency, complexity, cost and device rating, the buck+boost converter is employed as the variable output PFC power stage. From the loss analysis, this topology has a high efficiency from light load to heavy load.

The control system of the variable output PFC circuit is analyzed and designed. Charge average current sensing scheme has been adopted to sense the input current. The problem of high input harmonic currents at low output voltage is discussed. It is found that the current loop gain and cross over frequency will change greatly when the output voltage changes. To solve this problem, an automatic gain control scheme is proposed and a detailed circuit is designed and added to the current loop.

A modified input current sensing scheme is presented to overcome the problem of an insufficient phase margin of the PFC circuit near the maximum output voltage. The charge average current sensing circuit will be bypassed automatically by a logical circuit when the output voltage is higher than the peak line voltage. Instead, a resistor is used to

sense the input current at that condition. Therefore, the phase delay caused by the charge average current sensing circuit is avoided.

The design and analysis are based on a novel air conditioner motor system application. Some detailed design issues are discussed. The experimental results show that the variable output PFC circuit has good performance in the wide output voltage range, under both the Boost mode when the output voltage is high and the Buck+Boost mode when the output voltage is low.

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# 1. INTRODUCTION

With the increasing demand for power from the ac line and more stringent limits for power quality, power factor correction has gained great attention in recent years. A variety of circuit topologies and control methods have been developed for the PFC application [1-22]. While the discontinuous conduction mode (DCM) converters such as boost and flyback converters are well suited for low power applications, continuous conduction mode (CCM) boost converters with average current mode, peak current mode or hysteresis control are commonly chosen for many medium and high power applications. The output voltage of the boost PFC converter should be always higher than the peak line voltage. For universal line application (85 V-265 V), the output voltage is ususally set around 400 VDC. Recently, a Buck+Boost PFC converter has been adopted for wide input voltage range application [21]. The output voltage of the Buck+Boost converter can be lower than the peak line voltage.

Conventionally, the output voltage of the PFC circuit is fixed. However, in some applications, a PFC circuit with a wide output voltage range is needed. Figure 1.1 shows a conventional residential air conditioner motor system. The motor of the compressor is a permanent magnet motor. Before the motor is a PWM inverter. The switching frequency of the inverter is about 3 kHz. Before the inverter is the rectifier.

It is clear that this kind of system has large input harmonic currents. To meet the IEC requirements, a PFC circuit should be added in the system. A commonly used boost PFC circuit can be inserted into the system, shown in Figure 1.2. However, after adding the PFC function, the cost of the system will increase and the efficiency of the system will decrease.

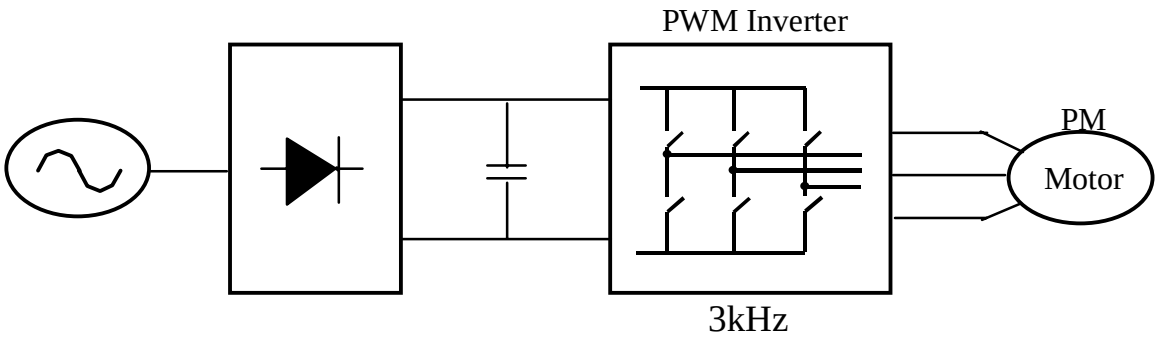



Fig. 1.1 Conventional system with large harmonic distortion

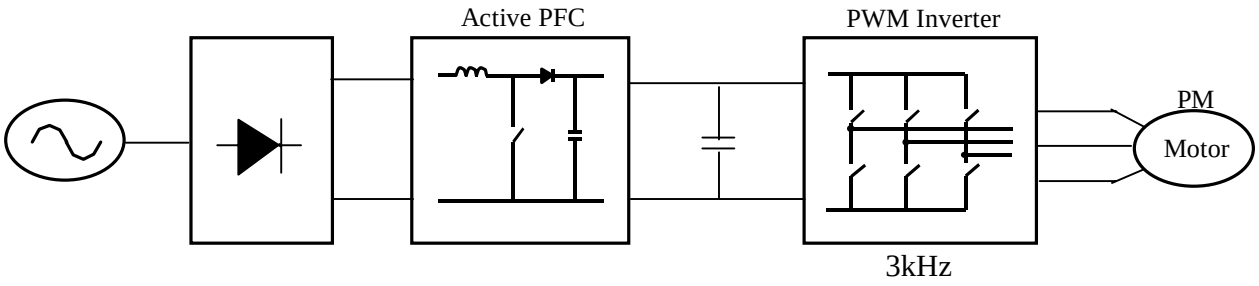



Fig. 1.2 Active PFC circuit + PWM inverter

To get a better solution, a new system is proposed, shown in Figure 1.3. The idea is that after adding the PFC circuit, if some functions of other system parts can be shifted to the PFC circuit, these parts perhaps can be simplified and the total cost of the system can be reduced.

In the new system, the function of changing the input voltage of the motor is shifted from the PWM inverter to the PFC circuit. The output voltage of the PFC circuit should be variable, and therefore, a simple PAM (pulse amplitude modulation) inverter can replace

the PWM inverter. The PAM inverter is operated in a low frequency range. The switching frequency of the PAM inverter is much lower than 3 kHz. (The frequency is variable according to the load condition.). The duty cycle of the PAM inverter does not need to be adjusted. Therefore, the inverter is much simpler than before. The switching loss and noise of the inverter are reduced and the cost of the new system is lower than the PFC + PWM inverter system.

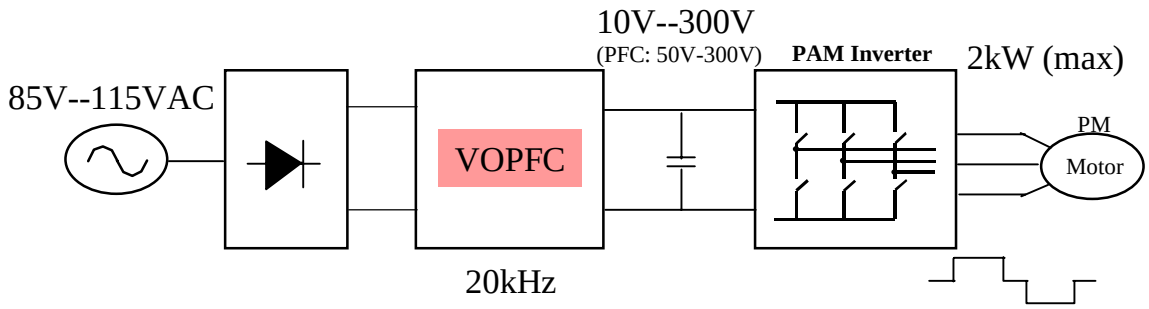



Fig. 1.3 Novel system block diagram:
Variable output PFC + PAM inverter

In this application, the output voltage of the variable output PFC (VOPFC) circuit should range from 10 VDC to 300 VDC. From 50 V to 300 V, which is the normal working condition, it should meet the IEC 1000-3-2 requirements. The input voltage range is from 85 V to 115 V. The maximum output power of the PFC circuit is 2 kW. Figure 1.4 shows the load characteristic of the PFC circuit. The maximum output power accurs at the highest output voltage 300 V. When the output voltage of the PFC is 50 V, the output power is less than 500 W.

It is clear that this variable output PFC is a quite unique PFC circuit. To design this kind of PFC circuit is a real challenge.

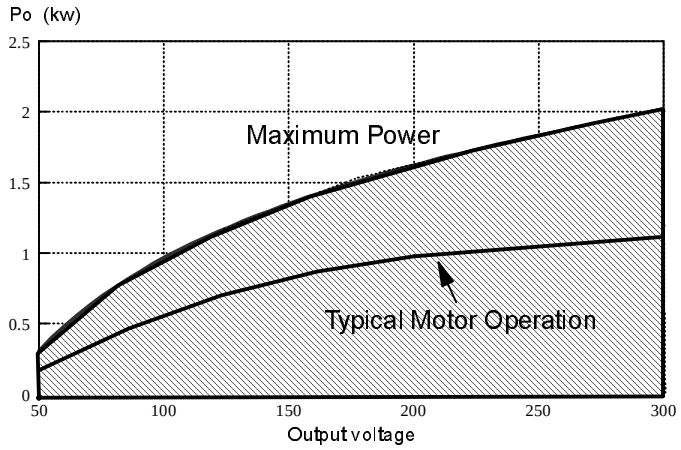



Fig. 1.4 Load characteristic of the PFC circuit

In this thesis, a single-stage power factor correction circuit with wide output voltage range is designed and analyzed. The design is based on the novel air conditioner motor system application, shown in Figure 1.3. The thesis consists of five chapters:

In Chapter 2, two main power stage candidates (Buck+Boost and Sepic) for the variable output PFC circuit have been discussed. A comparison of these two circuits is given in terms of efficiency, complexity, cost and device rating. The Buck+Boost PFC circuit is chosen in the application.

In Chapter 3, the control system of the variable output PFC circuit is analyzed and designed. Charge average current sensing scheme has been adopted to sense the input current. The problem of high input harmonic currents at low output voltage is found and discussed. Automatic current loop gain control scheme is proposed to solve the problem. A modified input current sensing scheme is presented to overcome the problem of insufficient phase margin of the PFC circuit near maximum output voltage.

In Chapter 4, some detail design issues are discussed and the experimental results are provided.

Conclusions are given in Chapter 5.

# 2. POWER STAGE OF THE VARIABLE OUTPUT PFC CIRCUIT

## 2.1 Introduction

The objective of this chapter is to perform a trade-off study in terms of efficiency, complexity, and cost, and to choose a PFC converter topology which meets the design specifications for a variable output PFC circuit designed to interface with a PAM (Pulse Amplitude Modulation) inverter. The system diagram was shown in Fig. 1.3. The design specifications for the PFC circuit are:

- PFC input voltage: single phase 85 - 115 VAC
- Power factor: > 0.95
- Meet IEC 1000 harmonic distortion specification
- Output voltage: Variable from 50 to 300 VDC
  (at starting: from 10 to 300 VDC)
- Peak to peak output ripple: < 10 %
- Output power: 2 kW maximum
- Switching frequency $f_s$: 20 kHz
- Efficiency $\eta$: around 94 %
- Isolation: not required

Since the converter outputs a very wide range voltage, it should operate in the Buck mode when the input voltage is higher than the output voltage, and in the Boost mode while the input voltage is below the output voltage. After careful study, two topologies which are Buck+Boost converter and Sepic converter are investigated for this application. Section 2 deals with the Buck+Boost converter including the principle operation and loss analysis. Section 3 explores the Sepic converter, and also includes loss analysis and design issues. Finally, comparisons between these two converters will be given and one of the converters is chosen for implementation.

## 2.2 Buck+Boost PFC Circuit

In this section, Buck+Boost PFC converter is analyzed in terms of loss analysis and component selection. It will be shown that this converter has several advantages and disadvantages for the variable output voltage application. These advantages and limitations have been carefully assessed and summarized.

### 2.2.1 Principle Operation

Boost converter is a conventional PFC circuit since its input current can be programmed to follow the input voltage. It has several advantages, such as a small EMI filter due to its continuous input current, and a simple circuit. The basic requirement is that the output voltage must be higher than the input voltage. For a wide range output voltage, as in this application, the converter outputs lower voltage, below the input voltage, when the system operates at low power level. A Boost converter can't accomplish this function. In order to achieve high power factor for this operation condition, a Buck converter or the converter which has Buck function has to be used. Fig. 2.1 shows the proposed Buck+Boost converter. Actually, this converter combines a buck converter with a boost converter. The basic operation can be described as follows:

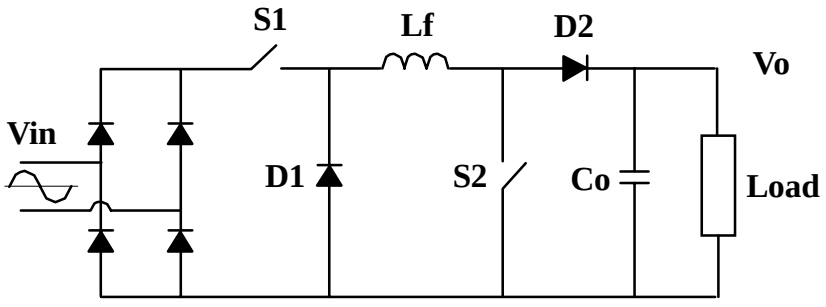



Fig. 2.1 The Buck+Boost PFC circuit

- **$V_0 > \sqrt{2}$ Vrms**

In this operation condition, shown in Fig. 2.2, the output voltage is always higher than the instantaneous line voltage. The circuit needs to run under Boost mode. Switch S1 is kept for conduction and diode D1 is always in the off-state. So the converter becomes the conventional boost converter**.**

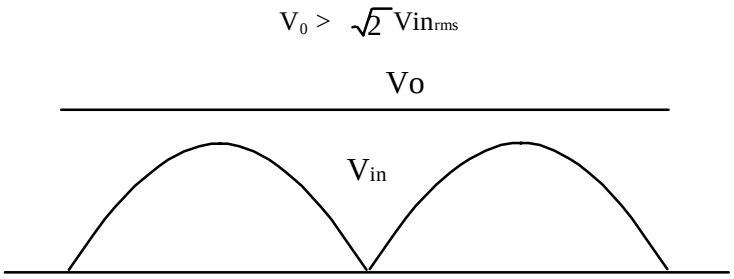



Fig. 2.2 Boost operation

- **$V_0 < \sqrt{2}$ Vrms**

From Fig. 2.3, obviously, the converter will operate both buck mode and boost mode depending on the instantaneous line voltage. During the time period from $\pi$-$\alpha$ to $\pi$+$\alpha$, where the line voltage is lower than the output voltage, switch $S_2$ is off while diode $D_2$ remains on. Therefore, the converter runs under boost mode. When the line voltage is above the output voltage, corresponding to the time interval from $\alpha$ to $\pi$-$\alpha$, Switch S1 remains on and diode D1 is off. So the circuit is a buck converter. High power factor can be obtained by using average current mode control. The control scheme will be discussed in the next chapter.

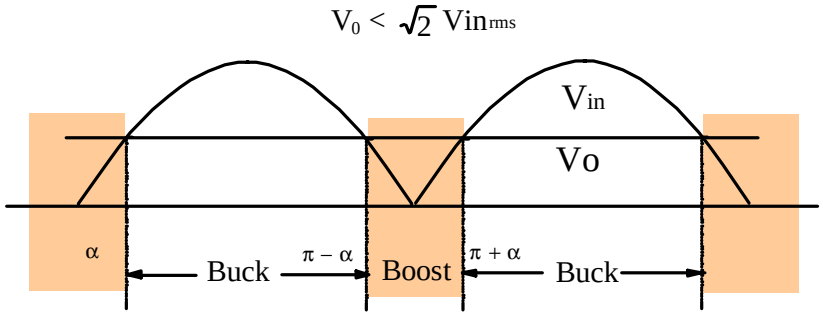



Fig. 2.3 Buck+Boost operation

### 2.2.2 Loss Analysis of Buck+Boost PFC Circuit

The simplified schematic of the Buck+Boost PFC circuit is shown in Fig. 2.4. The principal power stage components are:

- S1, S2: IRGPC40U 600 V / 27 A
- D1, D2: 25CPF40 25 A/400 V
- DB: 25CPF30 25 A/300 V
- $C_0$: 3300 µF / 450 V
- $f_s$: 20 kHz

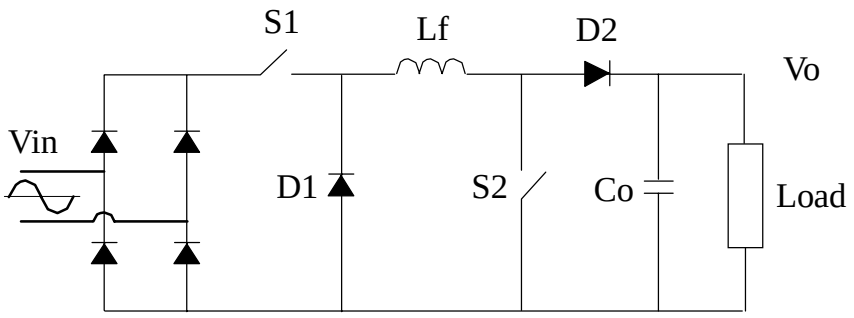



Fig. 2.4 Schematic of the Buck+Boost PFC Circuit

The load characteristic of this variable output PFC converter is shown in Fig. 2.5. It can be seen that the operation area is very wide from no load to heavy load at every output voltage. In this section, the loss will be analyzed only at the maximum power operation and typical motor operation conditions. The losses are calculated at two operating conditions depending upon the output voltage. One case is boost mode operation when the output voltage is higher than the input peak voltage; The other is the Buck+Boost operation while PFC output voltage is below the input voltage. The semiconductor losses, including switching losses and conduction losses, were calculated as follows:

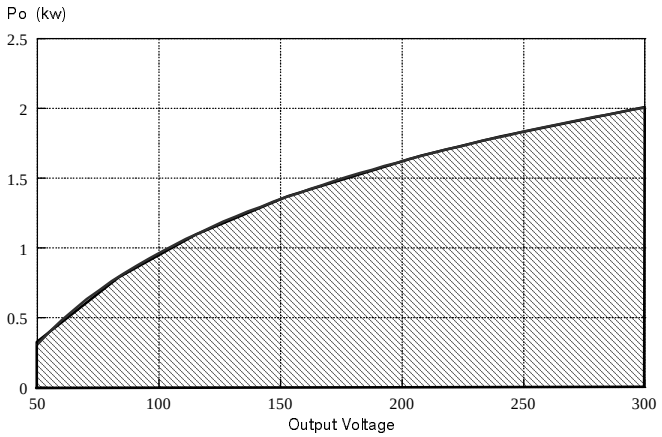



Fig. 2.5 The load characteristic of PFC circuit

**CASE A: BOOST OPERATION MODE**

Input Rectifier bridge: The input current is continuous when the circuit operates in boost mode. Therefore, the input rectifier loss consists of only conduction loss and reverse recovery switching losses can be neglected. The conduction losses are given by

$$P_{c,DB} = \frac{4\sqrt{2}P_0 V_F}{\pi\eta V_{rms}} \tag{2.1}$$

where $\eta$ is the efficiency of the circuit and $V_F$ is the forward drop of an individual diode at the average current through the diode, which is the half of the average input current.

Buck Switch S1: The buck switch S1 is always on when the circuit runs in boost mode. So there is no switching loss and only conduction loss exists. The conduction loss is actually the average conduction loss over a line cycle, which is given by:

$$P_{c,S1} = \frac{1}{\pi}\int_0^{\pi} I_{c,S1}(\psi)\, V_{ce}(sat)\, d\psi \tag{2.2}$$

where $I_{c,S1}$ is the instantaneous current through S1. This current is actually the line current

$$I_{c,S1} = \frac{\sqrt{2}P_0}{\eta\, V_{rms}}\ \sin\psi \tag{2.3}$$

The value of $V_{ce}$(sat) is a function of the collector current, but in order to simplify the calculation, $V_{ce}$(sat) is assumed to be constant and determined by the average collector

current over a line cycle. By integrating Eq. (2.2), the conduction loss of S1 is expressed as follows:

$$P_{c,S1} = \frac{2\sqrt{2}P_0}{\pi\,\eta\,V_{rms}}\ V_{ce}(sat) \tag{2.4}$$

Boost Switch S2: Losses of S2 consist of conduction loss and switching losses.

(A) The conduction loss:

$$P_{c,S2} = \frac{1}{\pi}\ \int_0^{\pi} I_{c,S2}(\psi)\ V_{ce}(sat)\ D(\psi)\ d\psi \tag{2.5}$$

where $I_{c,S2}$ is the same as Eq. (2.3) and $D(\psi)$ is the instantaneous duty cycle of $S_2$, which is given by

$$D(\psi) = 1 - \frac{\sqrt{2}\ V_{rms}}{V_0}\ \sin(\psi) \tag{2.6}$$

So the conduction loss of S2 is

$$P_{c,S2} = \frac{\sqrt{2}P_0 V_{ce}(sat)}{\pi\,\eta\,V_{rms}}\left(2 - \frac{\pi\sqrt{2}\ V_{rms}}{2V_0}\right) \tag{2.7}$$

(B) Switching losses: The switching losses consist of turn-on loss and turn-off loss. The instantaneous turn-off current of the switch S2 is

$$I_{S2,off} = \frac{\sqrt{2}P_0}{\eta V_{rms}} \sin\psi + \frac{\Delta i_L}{2} \tag{2.8}$$

If assume that the inductor current ripple is about 30% of the input line current, the above Eq. (2.8) then becomes:

$$I_{S2,off} = 1.15 \frac{\sqrt{2}P_0}{\eta V_{rms}} \sin\psi \tag{2.9}$$

The voltage across S2 is $V_0$ when it is turned off. Therefore, the turn-off switching loss:

$$P_{s,S2,off} = f_s E_{off,baseline} \frac{V_0}{V_{ce,baseline}} \frac{I_{s2,off}}{I_{ce,baseline}} \tag{2.10}$$

where $E_{off,baseline}$ is the turn-off energy per cycle including the loss due to the tail current under the test conditions. $V_{ce,baseline}$ and $I_{ce,baseline}$ are the test voltage and current used for device turn-off measurements. Since the turn-off current $I_{S2,off}$ varies over a line cycle, the average turn-off loss can be obtained by averaging Eq. (2.10), which is given by:

$$P_{s,S2,off} = f_s E_{off,baseline} \frac{2.3\sqrt{2}P_0 V_0}{\pi \eta V_{rms} V_{ce,baseline} I_{ce,baseline}} \tag{2.11}$$

Similarly, the turn-on switching loss is as follows:

$$P_{s,S2,on} = f_s E_{on,baseline} \frac{1.7\sqrt{2} P_0 V_0}{\pi \eta V_{rms} V_{ce,baseline} I_{ce,baseline}} \qquad (2.12)$$

So, the total switching loss of S2 is the summation of the above two equations.

Boost Diode D2: The loss of $D_2$ is comprised of conduction loss and reverse recovery switching loss.

(A) The conduction loss of $D_2$ is given by:

$$P_{c,d2} = \frac{P_0 V_F}{V_0} \qquad (2.13)$$

where $V_F$ and $P_0$ are the forward voltage drop at the average conduction current of $D_2$ and output power.

(B) Fig. 2.6 shows the switching waveforms when the diode is turned off. The reverse recovery switching loss is

$$P_{s,D2} = f_s \int_{t1}^{t2} i_d V_0 \, dt = f_s V_0 Q_{rr} \qquad (2.14)$$

where $Q_{rr}$ is the reverse recovery charge of the diode. Therefore, the total loss of $D_2$ is

$$P_{D2} = \frac{P_0 V_F}{V_0} + f_s V_0 Q_{rr} \qquad (2.15)$$

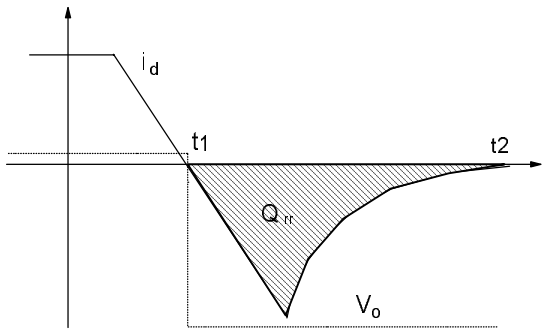



Fig. 2.6 The switching waveforms of diode

**CASE B: BUCK+BOOST OPERATION MODE**

Input rectifier bridge: The input current is discontinuous when the converter operates in the buck mode. The reverse recovery switching loss of the input rectifier should be considered besides their conduction losses, which are given by Eq. (2.1). The reverse recovery switching losses can be determined by:

$$P_{s,DB} = 4 f_s Q_{rr} \frac{2\sqrt{2}V_{rms}}{\pi} \frac{\pi - \alpha}{\pi} \tag{2.16}$$

where $\alpha = sin^{-1}\left(\frac{V_0}{\sqrt{2}\, V_{rms}}\right)$

Buck switch S1: The conduction loss of S1 is the same as that in the boost mode since it is determined by the average current. The switching loss exists when the output voltage

is less than the instantaneous input voltage. Using the same calculation method as shown in the last section, the switching loss is given by:

$$P_{s,S1} = f_s E_s \frac{\sqrt{2} P_0 V_{rms}}{I_{ce} V_{ce} V_0} \frac{\pi - 2\alpha + \sin 2\alpha}{\pi \eta} \tag{2.17}$$

where $E_s$ is the total switching energy.

Boost Switch S2: The conduction loss should be averaged over a line cycle since the current through $S_2$ varies from time to time. The conduction loss over a switching period is given by:

$$p_{c,S2}(t) = \frac{\sqrt{2} P_0 \sin \omega t}{\eta V_{rms}} D(t) V_{ce}(sat) \tag{2.18}$$

where the D(t) is the duty cycle of $S_2$. Thus, the conduction loss can be obtained by averaging Eq. (2.18), which is as follows:

$$P_{c,S2} = \frac{\sqrt{2} P_0 V_{ce}(sat)}{\pi \eta V_{rms}} \left[ 1 - \cos\alpha - \frac{V_{rms}}{\sqrt{2} V_0} \left( \alpha - \tfrac{1}{2} \sin 2\alpha \right) \right] \tag{2.19}$$

The switching loss also can be calculated using the same approach above.

$$P_{s,S2} = 2 f_s E_s \frac{\sqrt{2} P_0 V_0}{I_{ce} V_{ce} V_{rms} \eta} (1 - \cos\alpha) \tag{2.20}$$

Diode D1: $D_1$ has both conduction loss and switching loss only when the converter operates in the buck mode ($\alpha$, $\pi$-$\alpha$). The instantaneous current through D1 is given by

$$I_{d1} = \frac{\sqrt{2}P_0}{\eta\, V_{rms} D(t)} \sin \omega t \tag{2.21}$$

where D(t) is the duty cycle of S1. So the conduction can be calculated as:

$$\begin{aligned} P_{c,D1} &= \frac{1}{\pi}\int_{\alpha}^{\pi-\alpha} I_{d1}(t)\, V_{ce}(sat)\, d\omega t \\ &= \frac{\sqrt{2}P_0 V_{ce}(sat)}{\pi\eta V_{rms}}\left[\frac{V_{rms}}{\sqrt{2}V_0}(\pi - 2\alpha + 2\sin 2\alpha) - 2\cos 2\alpha\right] \end{aligned} \tag{2.22}$$

For the switching loss of D1, it is given by

$$P_{s,D1} = \frac{\pi - 2\alpha}{\pi}\frac{2\sqrt{2}V_{rms}}{\pi} Q_{rr} f_s \tag{2.23}$$

Diode D2: Its conduction loss and switching loss are

$$P_{c,D2} = \frac{P_0 V_F}{V_0} \tag{2.24}$$

$$P_{s,D2} = \frac{2\alpha}{\pi} V_0 Q_{rr} f_s \tag{2.25}$$

Inductor: The inductor loss actually includes the copper loss and core loss. In this loss analysis, to simplify our calculation, the total inductor loss is estimated at approximately 0.5% of the output power.

Output (bulk) capacitor: The bulk capacitor has some loss associated with the 120 Hz component of the ripple current flowing through the capacitor ESR. This is given by:

$$P_{ESR} = \frac{1}{\pi} \int_0^{\pi} I_c^2(\psi) R_{esr} d\psi, \tag{2.26}$$

where

$$I_c(\psi) = \frac{2P_0}{V_0} sin^2 \psi - \frac{P_0}{V_0} \tag{2.27}$$

Integrating Eq. 2.27 yields

$$P_{ESR} = \frac{P_0^2 R_{esr}}{2V_0^2} \tag{2.28}$$

A Mathcad program was developed to calculate the losses. The efficiency is then determined as

$$\eta = \frac{P_0}{P_0 + P_{Loss}} \tag{2.29}$$

Table 2.1 Buck+Boost efficiency at Maximum output power operation P=2 kw, Vo=300 V (high line)

| **Loss Source** | **Loss (W)** | **% of Total Loss** |
|---|---|---|
| IGBT conduction ( Buck S1) | 26.37 | 23.8% |
| IGBT switching (Buck S1) | 0 | 0 |
| IGBT conduction ( Boost S2) | 11.36 | 10.3% |
| IGBT switching (Boost S2) | 19.1 | 17.3% |
| Output rectifier D2 conduction | 6.3 | 5.7% |
| Output rectifier D2 switching | 0.7 | 0.6% |
| Input rectifier conduction | 36.3 | 32.8% |
| Boost inductor | 10 | 9.1% |
| Output capacitor Esr loss | 0.44 | 0.4% |
| Total loss | 110.57 | |
| **Efficiency** | **94.8 %** | |

Table 2.2 Buck+Boost efficiency at Maximum output power operation P=0.85 kw, Vo=100 V (Low line)

| **Loss Source** | **Loss (W)** | **% of Total Loss** |
|---|---|---|
| IGBT conduction ( Buck S1) | 11.85 | 21.9% |
| IGBT switching (Buck S1) | 2.8 | 5.2% |
| IGBT conduction ( Boost S2) | 0.63 | 1.2% |
| IGBT switching (Boost S2) | 5.1 | 9.5% |
| Output rectifier D2 conduction | 5.84 | 10.8% |
| Output rectifier D2 switching | 0.22 | 0.4% |
| Input rectifier conduction &switching | 19.21 | 35.6% |
| Boost inductor | 4.25 | 7.9% |
| Output capacitor Esr loss | 0.72 | 1.3% |
| Buck freewheeling diode D1 | 3.3 | 6.1% |
| Total loss | 53.92 | |
| **Efficiency** | **94.0%** | |

Table 2.1 and Table 2.2 show the loss analysis of the converter under maximum output power operation, V0=300 V (Boost operation) and $V_0$=100V (Buck+Boost operation). Figures 2.7, 2.8 and 2.9 show the converter operation area and efficiency versus the output voltage for maximum output power operation and typical motor operation

conditions, respectively. It is shown that about 95% efficiency can be achieved at high line, and approximately 94% efficiency can be achieved at low line.

### 2.2.3 Conclusions

This topology is very attractive for this typical application since boost operation mode runs at high power while buck operation mode operates at low power (P < 1.3 kW) from its load characteristics. From the loss analysis, this topology has a high efficiency from light load to heavy load. In addition, a low voltage rating power device can be used. However, this topology suffers from a disadvantage, that is, a larger EMI filter is needed due to its discontinuous input current in the buck mode. In Section 4, a comparison between Buck+Boost topology and Sepic converter will be given to show that this topology has better performance.

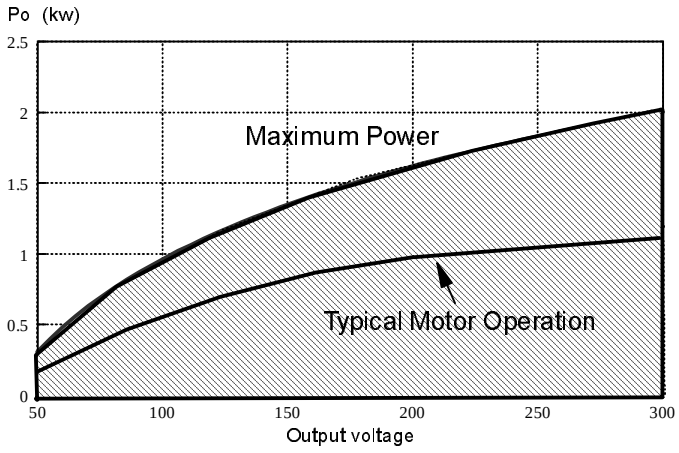



Fig. 2.7 Operation area of the converter

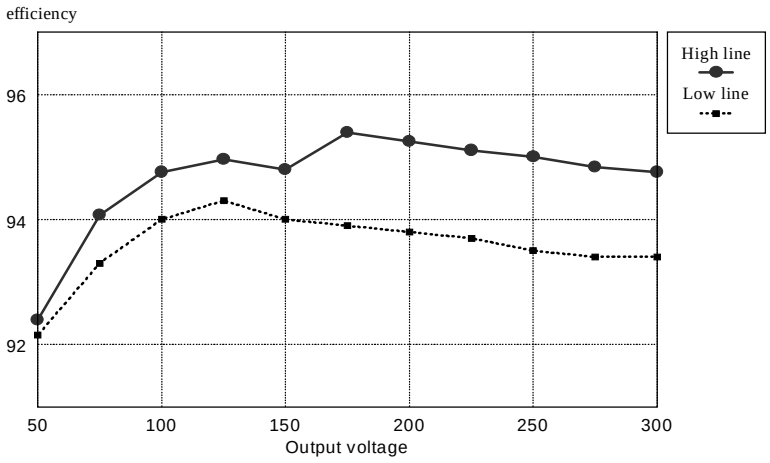



Fig. 2.8 Efficiency at the maximum power operation

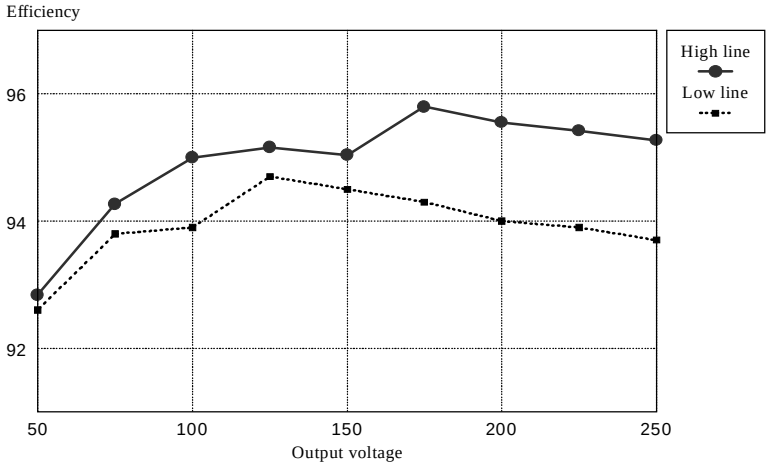



Fig. 2.9 Efficiency at the typical motor operation

## 2.3 Sepic PFC Circuit

In this section, the Sepic PFC circuit is analyzed and designed. The advantages and limitations have been carefully assessed and summarized.

### 2.3.1 Principle operation

The output voltage of Sepic converter can be either higher or lower than the input voltage. This makes it suitable in the wide output range PFC circuit. The topology of the basic Sepic converter is simple, and is shown in Fig. 2.10. It contains one active switch S and one passive switch (diode) D, operating in PWM mode. Not only does it have an input inductor and an output capacitor, but it also has a bulk capacitor and an inductor in the middle of the converter.

When the active switch S is on, the bulk capacitor $C_f$ is discharged, and the energy will be transferred from the capacitor $C_f$ to inductor $L_f$ . When the switch S is off, the capacitor $C_f$ is charged by the input line current, and the energy stored in the inductor $L_f$ will be transferred to the output.

The input current is continuous in Sepic converter. This also makes it suitable in PFC application and a small input filter can be used.

The control of this circuit is simple to achieve high power factor. A commonly used power factor correction chip, such as UC3854, can be chosen as the IC controller in this case.

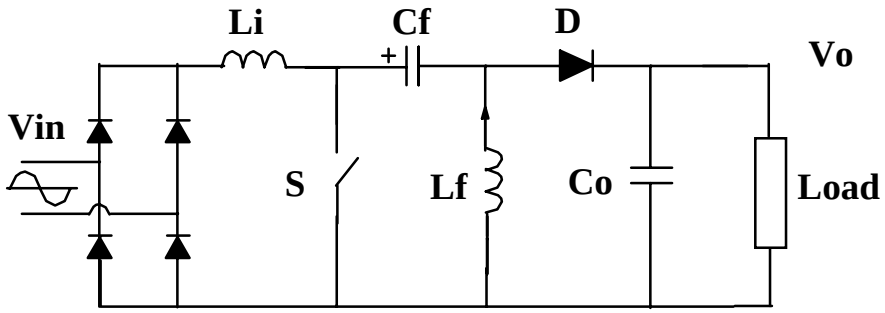



Fig. 2.10 Sepic PFC converter

### 2.3.2 Loss Analysis of Sepic PFC Circuit

The device selection is based on its voltage stress and average current in the worst case.

Switch S:

IRGPC50U (ultrafast IGBT)

$V_r$=600 V, $I_c$=27 A (Tc=100°C), $V_{ce}$(on)=2.0 V (typical)

Diode D:

HFA25PB60 (ultrafast, soft recovery)

$V_r$=600 V, $I_f$(av)=25 A, $V_{fm}$=1.3 V (typical)

Rectifier Bridge:

26MB20A (IR) to calculate rectifier bridge loss.

$I_o$=25 A, $V_{rrm}$=200 V, $V_{fm}$=1.1 V

The switching frequency $F_s$ is 20 kHz.

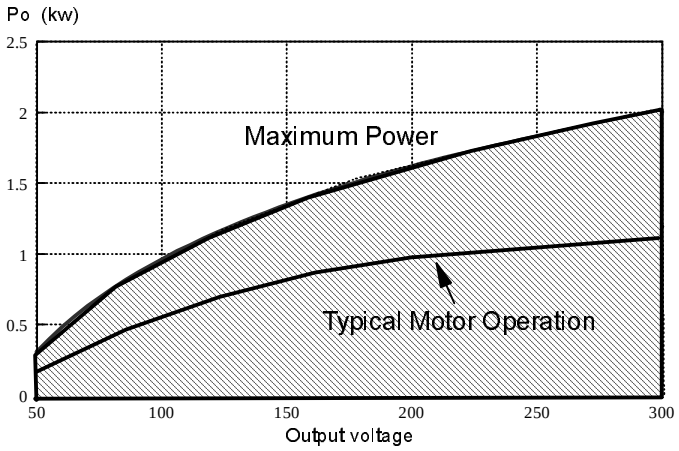



Fig. 2.11 Load characteristics of the Sepic PFC converter

The loss analysis has been carried out according to the different operation conditions. Because the output voltage Vo changes from 50 V to 300 V (normal working conditions), we calculate all the losses at every 25 V , i.e., at $V_o$=50 V,75 V,100 V,...300 V (along solid load line, Vo from 50 V to 250 V)

Define: $V_o(i)=25+25\times i$ (V) , i=1,2,3,...11 (Max. Po)

i=1,2,3,...9 (solid load line) (2.30)

**Switch duty cycle:**

Using the volt-second balance of the input inductor, we have

$$V_p \sin\omega t \;\; T_{\text{on}} = \left(V_0 + V_{cf} - V_p \sin\omega t\right) T_{off} \tag{2.31}$$

Then

$$\text{d'(t)}=\frac{T_{off}}{T_{on}+T_{off}} = \frac{V_p \sin\omega t}{V_0 + V_{cf}} \tag{2.32}$$

$$\text{d(t)}=1 - \text{d'(t)}$$

$$=1 - \frac{V_p \sin\omega t}{V_0 + V_{cf}} \tag{2.33}$$

where $\omega = 2\pi f$ rad/s, $f$ is line frequency and $V_p$ is rectified AC line peak voltage,

$V_p = V_{plow} = 120.19$ V, when $V_{in} = 85$ V

$V_p = V_{phigh} = 162.61$ V, when $V_{in} = 115$ V

$V_{cf}$ is the voltage across capacitor $C_f$ ,

$$V_{cf} = V_p \tag{2.34}$$

$T_{on}$ is the switch on-time, while $T_{off}$ is the switch off-time.

The average value of duty cycle d(t) over a line cycle is given by:

$$D = \frac{2}{T} \times \int_0^{T/2} d(t)\, dt \tag{2.35}$$

Switch S (IGBT)

(1) Conduction Loss: Pscond is the average conduction loss over a line period since the current through the switch varies in one line cycle, which is given by:

$$P_{\text{scond}}=\frac{2}{T}\times\int_{0}^{0.5\times T} I_s(t)\times V_{ce}\times d(t)dt \qquad (2.36)$$

Where, switch current $I_s(t)$ is the sum of the line input current and discharging current through $C_f$:

$$I_s(t)=\frac{\sqrt{2}P_0}{\eta V_{in}}\ \sin\omega t+\frac{P_0}{V_0} \qquad (2.37)$$

$V_{ce}$ is collector-to-emitter saturation voltage of the switch S (IRGPC50U). Po is output power of the converter. $\eta$ is the efficiency of the converter.

(2) Switching Loss: $P_{ssw}$

$$P_{ssw}=\frac{2}{T}\times\int_{0}^{0.5\times T} E_{ts}\times F_s\times\frac{V_p\times\sin\omega t+Vo}{480}\times\frac{I_s(t)}{27}dt \qquad (2.38)$$

where, $E_{ts}$ is the total switching loss including the loss due to the tail current at one switching cycle:

$E_{ts}$=2.5mJ (Tj=150°C , $I_c$=27 A , $V_{cc}$=480 V )

When the switch is turned off, the voltage stress across S is ($V_p \times \sin\omega t + V_o$)

Diode D

(1) Conduction Loss: $P_{dcond}$

$$P_{dcond} = I_0 \, V_{fm} \tag{2.39}$$

where $I_0 = \frac{P_0}{V_0}$ and $V_{fm}$ is the forward voltage drop of the diode.

(2) Switching Loss: $P_{dsw}$

$$Pdsw = Fs \, (V_{cf} + V_o) \, Q_{rr} \tag{2.40}$$

where $Q_{rr}$ is the reverse recovered charge. ($Q_{rr} = 250 \times 10^{-9}$ (C) (Tj=125°C)).

($V_{cf} + V_o$) is the voltage stress on the diode D when it is off.

Input Rectifier Bridge Loss: $P_{rec}$

The input current is continuous so only conduction loss has been considered.

$$P_{rec} = \frac{4\sqrt{2}\, P_0}{\eta \times \pi \times V_{in}} \times V_{fm} \tag{2.41}$$

where, $V_{fm}$ is the forward voltage drop.

Inductor Loss: $P_L$

The inductor losses include the copper loss and the core loss. For simplicity in loss calculation, it is assumed that the inductor loss has 0.5% of output power

$$P_{L1} = 0.5\%\ P_0 \tag{2.42}$$

There are two inductors in the circuit. So the total inductor loss $P_L$ is two times of $P_{L1.}$

Capacitor Loss: $P_c$

$$P_c = P_{cf} + P_{co} \tag{2.43}$$

where $P_{cf} = I_0^2 R_{esr} D + I_0^2 \frac{D^2}{1-D} R_{esr}$ and $P_{co} = \frac{I_0^2 R_{esr}}{2}$

### 2.3.3 Results of the Loss Analysis

Total Loss $P_{loss}$ is the sum of all the losses analyzed above. So the total losses are given by

$$P_{Loss} = P_{scond} + P_{ssw} + P_{dcond} + P_{dsw} + P_{rec} + P_L + P_c \tag{2.44}$$

Total efficiency can be calculated as follows:

$$\eta = \frac{P_0}{P_0 + P_{Loss}} \tag{2.45}$$

Table 2.3 Sepic efficiency at $P_o$=2 kW, $V_o$=300 V and $V_{in}$=115 V

| **Loss Source** | **Loss (W)** | **% of Total Loss** |
|---|---|---|
| IGBT conduction | 27.4 | 20.4% |
| IGBT switching | 37.6 | 27.9% |
| Diode D conduction | 7.5 | 5.5% |
| Diode D switching | 2.3 | 1.7% |
| Input rectifier | 36.2 | 27% |
| Inductors | 20 | 14.9% |
| Capacitors | 3.5 | 2.6% |
| Total loss | 134.5 | 6.7% of $P_0$ |
| **Efficiency** | **93.7 %** | |

Table 2.3 summarizes the results of the loss calculations (based on loss source) under maximum output power operation, output voltage 300 V and line voltage 115 V. Table 2.4 gives another example of the loss calculations under maximum output power operation, output voltage 100 V and line voltage 85 V.

Figures 2.12 and Fig.2.13 compare and summarize the efficiency at high line ($V_{in}$=115 V) and low line ($V_{in}$=85 V), for maximum output power operation and typical motor operation conditions, respectively.

Table 2.4 Sepic efficiency at $P_o$=0.85 kW, $V_o$=100 V and $V_{in}$=85 V

| **Loss Source** | **Loss (W)** | **% of Total Loss** |
|---|---|---|
| IGBT conduction | 14.3 | 20.1% |
| IGBT switching | 12.9 | 18.2% |
| Diode D conduction | 10.0 | 14.1% |
| Diode D switching | 1.1 | 1.5% |
| Input rectifier | 20.8 | 29.3% |
| Inductors | 8.5 | 12% |
| Capacitors | 3.4 | 4.8% |
| Total loss | 71.0 | 8.4% of $P_0$ |
| **Efficiency** | **92.3 %** | |

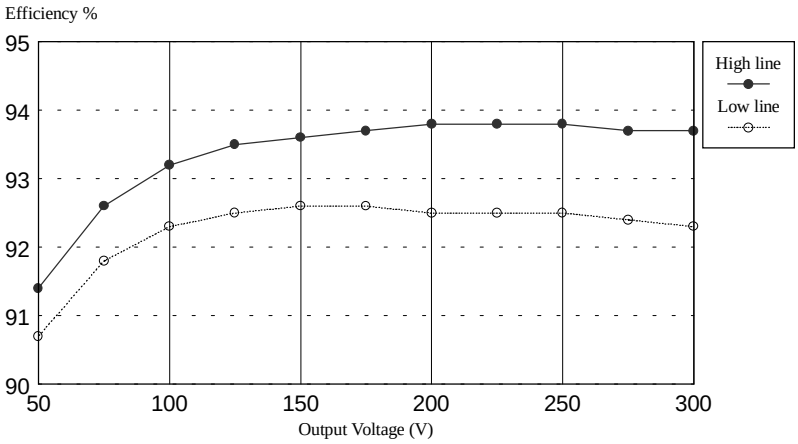



Fig. 2.12 Efficiency at maximum operation

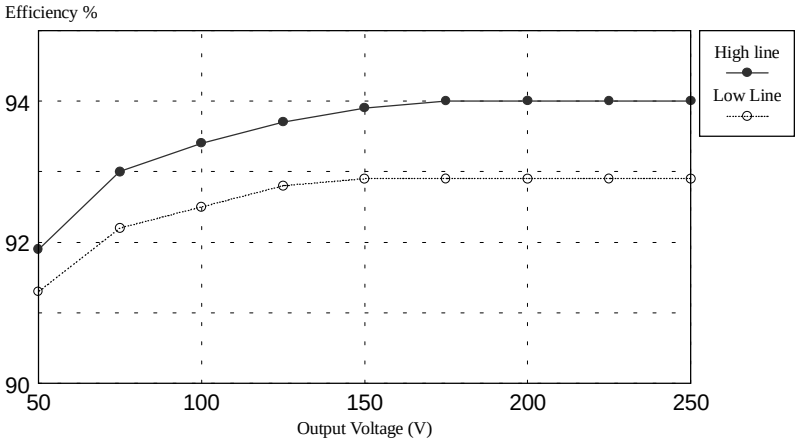



Fig. 2.13 Efficiency at typical Motor operation

### 2.3.4 Conclusions

The Sepic PFC converter is an attractive alternative for the Variable Output PFC Circuit topology. The major advantages of this converter are:

- The topology is simple and only need one active switch.
- The control is simple to achieve high power factor. A conventional PFC controller can be used as IC control chip.
- The input current is continuous and a small input filter can be used.

The principal disadvantages of this converter are:

- Two inductors and two capacitors are needed.
- There are two energy storage and transferring stages in the converter, which will cause extra conduction loss in the IGBT and copper loss of the reactive components.
- The current stress on the active switch is relatively high.

## 2.4 Comparison and Conclusions

Two topologies (Buck+Boost and Sepic) for the variable output PFC circuit have been discussed. A comparison of these two circuits will be given in terms of efficiency, complexity, cost and device rating.

Efficiency: From Fig. 2.14 and 2.15, it is shown that the Buck+Boost PFC topology has higher efficiency than that of the Sepic PFC circuit although Buck+Boost converter has an extra conduction loss of the buck switch. However, the conduction and switching current of the switch for Sepic circuit is much higher since it has to carries both input rectified line current and discharged current from the bulky capacitor. Consequently, it causes higher conduction loss and switching losses. Furthermore, the Sepic circuit actually has two energy conversion stages which leads to higher conduction loss in the circuit.

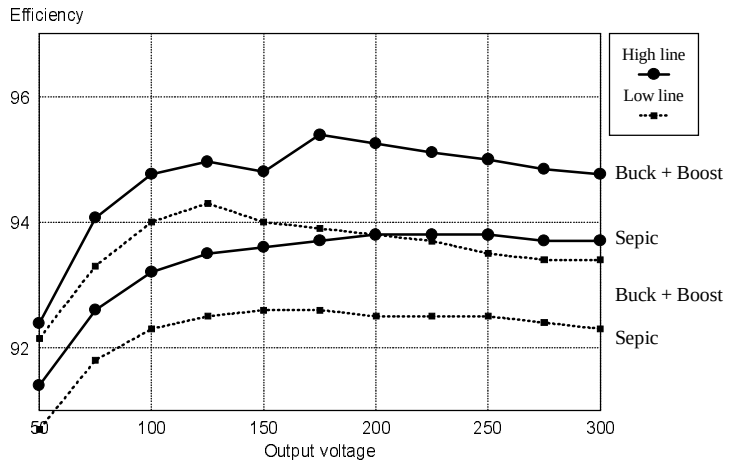



Fig. 2.14 Efficiency at Maximum output power operation

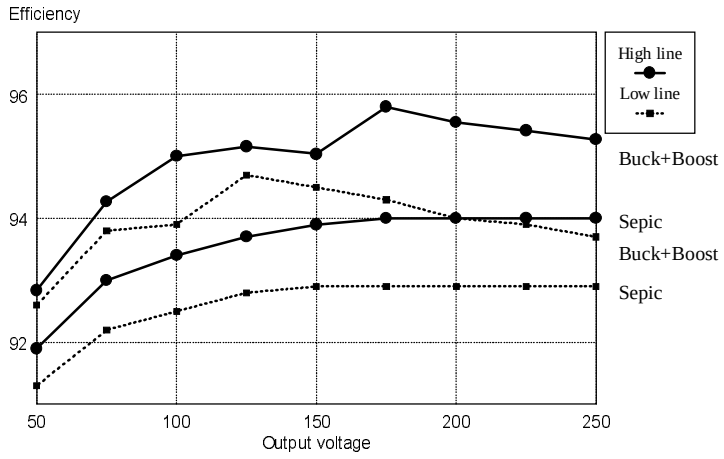



Fig. 2.15 Efficiency at Typical Motor operation

Complexity: Basically, complexity is proportional to the parts count. From this point of view, these two circuits are almost the same. The Buck+Boost converter has an extra buck switch which is required only at a low voltage rating while the Sepic topology has an extra inductor and a bulky capacitor. So the price of the Sepic circuit may be higher than that of the Buck+Boost converter.

Device Stress: The voltage stress of the switches for the Buck+Boost circuit is less than that of Sepic converter. 250 V buck switch, 400 V Boost switch and 400 V fast reverse recovery diode are required for Buck+Boost circuit while 600 V IGBT and 600 V fast reverse recovery diode have to be used for Sepic converter. The low voltage rating device will translate into a lower cost. For the current stress, the Sepic switch suffers from higher current stress since it has to take the current from both the input rectified line current and discharged current from the bulky capacitor while it only carries the input rectified line current for the Buck+Boost converter. Although the buck switch takes

higher switching current than the line current in buck mode, it operates only at low power.

Based upon the above analysis, the Buck+Boost converter has better performances and is recommended to be the candidate for this type of application.

# 3. CONTROL OF THE VARIABLE OUTPUT PFC CIRCUIT

## 3.1 Buck+Boost PFC Basic Control System

The basic system block diagram of the Buck+Boost PFC circuit is shown in Figure 3.1. Average current mode control is adopted. A multiplier/divider is used to generate the current reference signal $I_{ref}$. Signal C is the output signal of the feed-forward circuit. Signal B is the voltage error amplifier output of the feed-back loop. Signal A is a signal

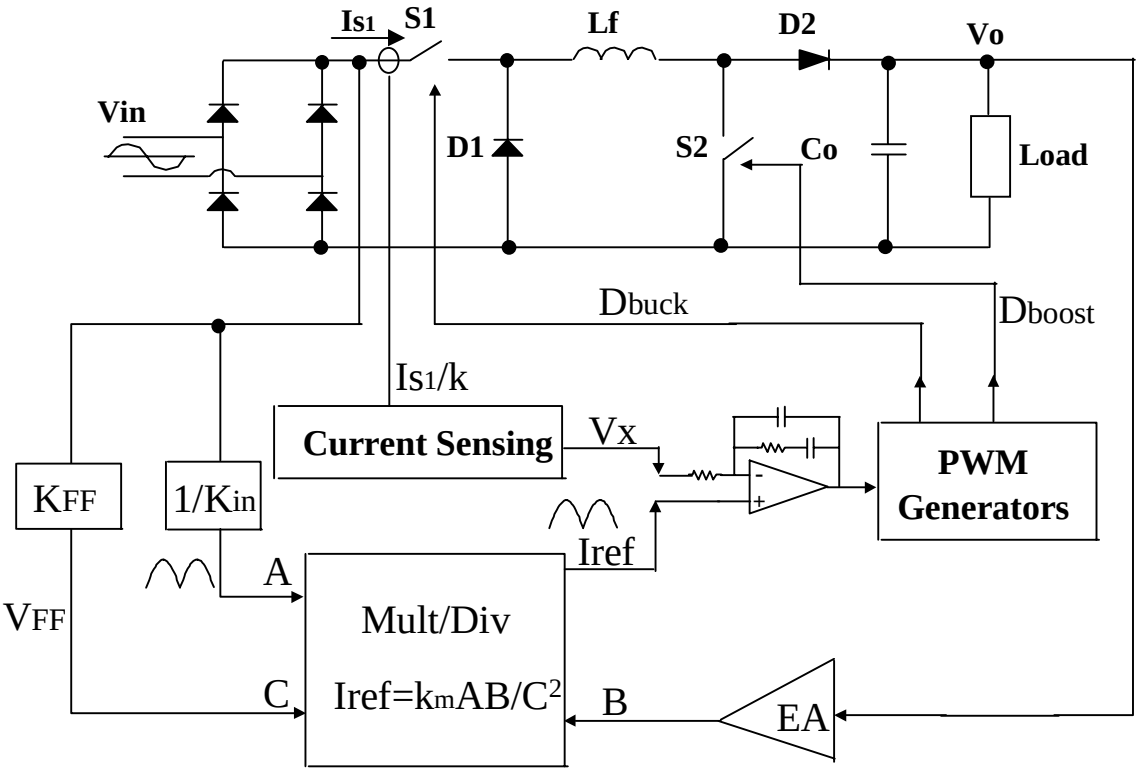



Fig. 3.1 Buck+Boost PFC circuit basic system block diagram

representing the waveform of the rectified input voltage. The input current sensing signal Vx compares with the current reference signal $I_{ref}$. After the current loop compensator, two driving signals are generated for the two main active switches.

The control of the Buck+Boost converter PFC circuit has to be different from that of the conventional boost PFC circuit since there are two different operation modes: the boost mode and the buck mode within half line cycle when output voltage is lower than the peak line voltage. An interesting question is how to properly sense and control the average input current under both modes. This will be discussed below.

## 3.2 Input Current Sensing Scheme

In a conventional boost PFC circuit, the input current is the inductor current, which is continuous in most cases. The inductor current passes through the sensing resistor and provides a voltage signal proportional to the inductor current. This voltage signal is fed to the current compensator as the average current feedback signal. However, in this Buck+Boost PFC converter, under the buck mode operation, the input current is pulsating. The input current waveforms in boost mode and buck mode are shown in Figure 3.2. If using the same input current sensing method, the created voltage signal is pulsating which requires a low-pass filter before being fed into the compensator. In this case, if the low-pass filter is designed to remove most of the switching frequency pulsating component, the current loop speed can't be fast enough to meet the PFC requirement. Therefore, the input current sensing scheme of the Buck+Boost PFC converter has to be different from that of the conventional boost PFC converter. The suitable input current sensing scheme will be introduced below.

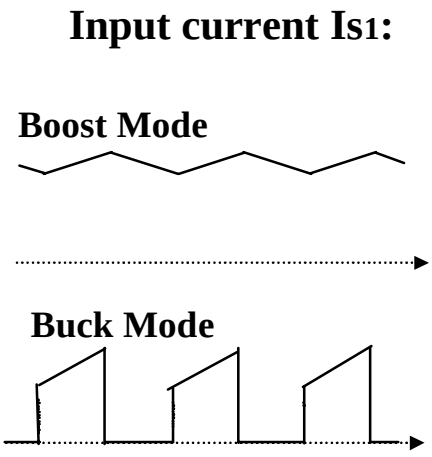



Fig. 3.2 Input current waveforms in boost mode and buck mode

### 3.2.1 Charge Control Concept

In the buck+boost PFC converter, during buck mode operation, the input current is pulsating. We may consider using charge control scheme. Charge control was proposed in the late 1970s. It is one form of average current mode control [23], [24], [27]. Charge control uses a resettable integrator to control the average value of a pulsating circuit variable. This control scheme has been successfully applied in many cases, such as single-phase CCM flyback PFC converters [26], multi-resonant DC/DC converter [27], and three-phase buck PWM rectifiers [29]. The small-signal models and design guidelines of charge control for DC/DC converters can be found in [25], [27], [28].

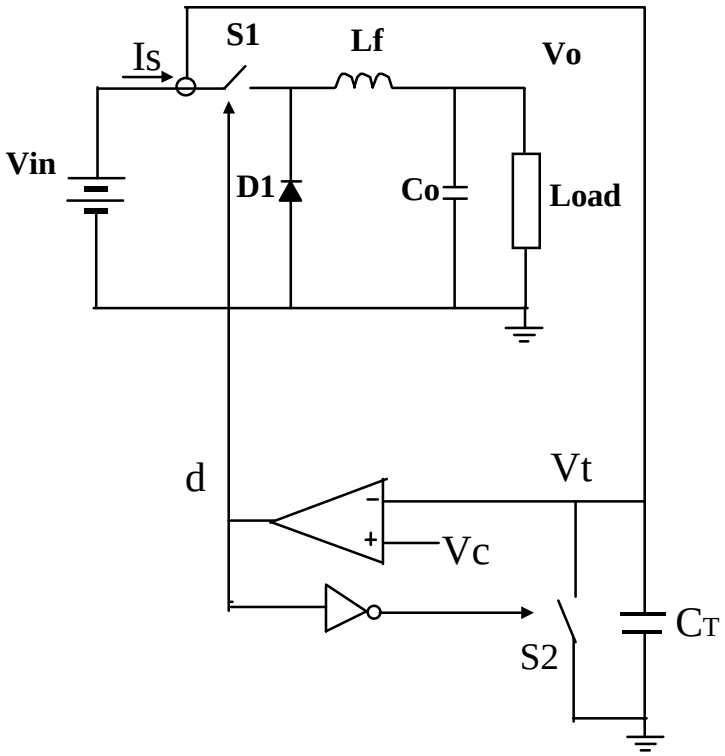



Fig. 3.3 Buck converter using charge control

The basic concept of charge control is illustrated in Figure 3.3. This is a simple example of a buck DC/DC converter using charge control. The active switch S1 in the power stage turns on at the beginning of each switching cycle. The switch current is integrated with a capacitor $C_T$. When the capacitor voltage Vt reaches the control voltage Vc, switch S1 turns off, and the switch S2, which is across the capacitor $C_T$, turns on to discharge the capacitor. The capacitor will be completely discharged before the next switching cycle. Switch S2 turns off when S1 is on. The steady state waveforms of a buck converter using charge control are shown in Fig. 3.4. From Eq. 3.1-3.3, it is clear that the capacitor voltage Vt is proportional to the average switch current $Is_{(av)}$.

$$Is_{(av)} = \frac{1}{Ts}\int_0^{DTs} Isdt \tag{3.1}$$

$$Vt = \frac{1}{C_T}\int_0^{DTs} Isdt \tag{3.2}$$

$$Vt = \frac{Ts}{C_T} Is_{(av)} \tag{3.3}$$

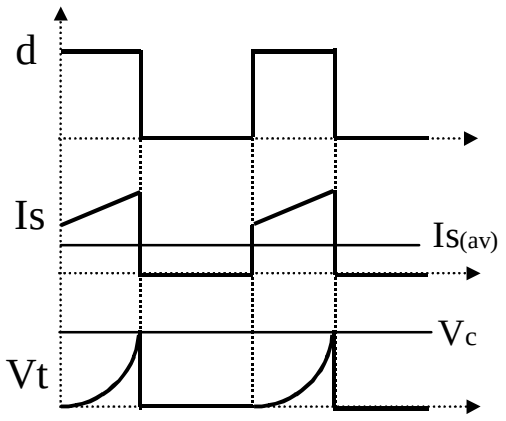



Fig. 3.4 Charge control waveforms of the buck converter

Charge control can control the switch current. It can be used in a flyback or buck type converter to control the input average current. However, it cannot control the average input current of a boost converter, because the boost switch current is not equal to the input current. Therefore, charge control cannot be employed directly in the buck+boost converter.

### 3.2.2 Charge Average Current Sensing Scheme

For constant frequency operation, which is the case in our circuit, it is easy to see that the average input current can be obtained by integrating the real input current over one switching cycle as in Eq. 3.4.

$$I_{ave} = \frac{1}{T_s}\int_0^{Ts} i_{in}\,dt \qquad (3.4)$$

Fig. 3.5 shows the average input current sensing circuit [21]. Since this scheme is based on the charge information as in charge control, it is called *the charge average current sensing scheme.*

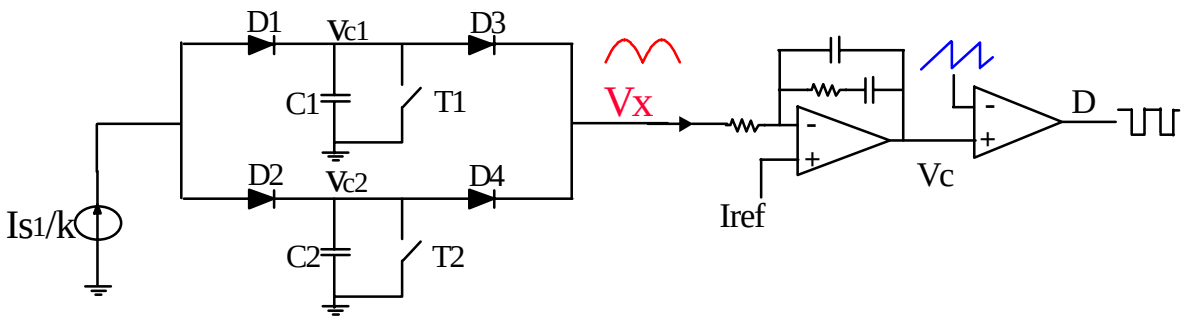



Fig. 3.5 Charge average current sensing circuit

$Is_1/k$ is the hall current sensor or current transformer output current which is proportional to the instantaneous input current. Two capacitors, $C_1$ and $C_2$, are used for integrating the input current alternatively. Transistors $T_1$ and $T_2$ are employed to quickly discharge the capacitors. The four diode bridge $D_1$ - $D_4$ allows $Is_1/k$ to charge the capacitor with lower voltage, and allows $V_x$ to pick up the higher capacitor voltage, which represents the average input current.

For the boost mode, the operation waveforms are shown in Fig. 3.6. $T_s$ is the switching period of the boost switch. $T_1$ and $T_2$ are transistor drive signals for discharging the capacitor voltages. $V_{c1}$ and $V_{c2}$ are the voltages on the capacitors. $V_x$ is the sensor output voltage which gives the average current information.

Starting from a switching cycle at time $t_0$, transistor $T_1$ conducts for a very narrow period to discharge the capacitor $C_1$, and thus $V_{c1}$ drops down to zero immediately. After $T_1$ is turned off, the capacitor $C_2$ is holding a voltage, $Is_1/k$ flows through diode $D_1$, and charges up the capacitor $C_1$. Since it is in boost mode, the input current is continuous and the charging action lasts until time $t_1$. The value of $V_{c1}$ is proportional to the average input current because it is the integration of the input current over a whole switching period. At time $t_1$, transistor $T_2$ is turned on for a very short time interval and $C_2$ is fully discharged. $V_{c1}$ will hold the value at time $t_1$ since the input current begins to charge $C_2$.

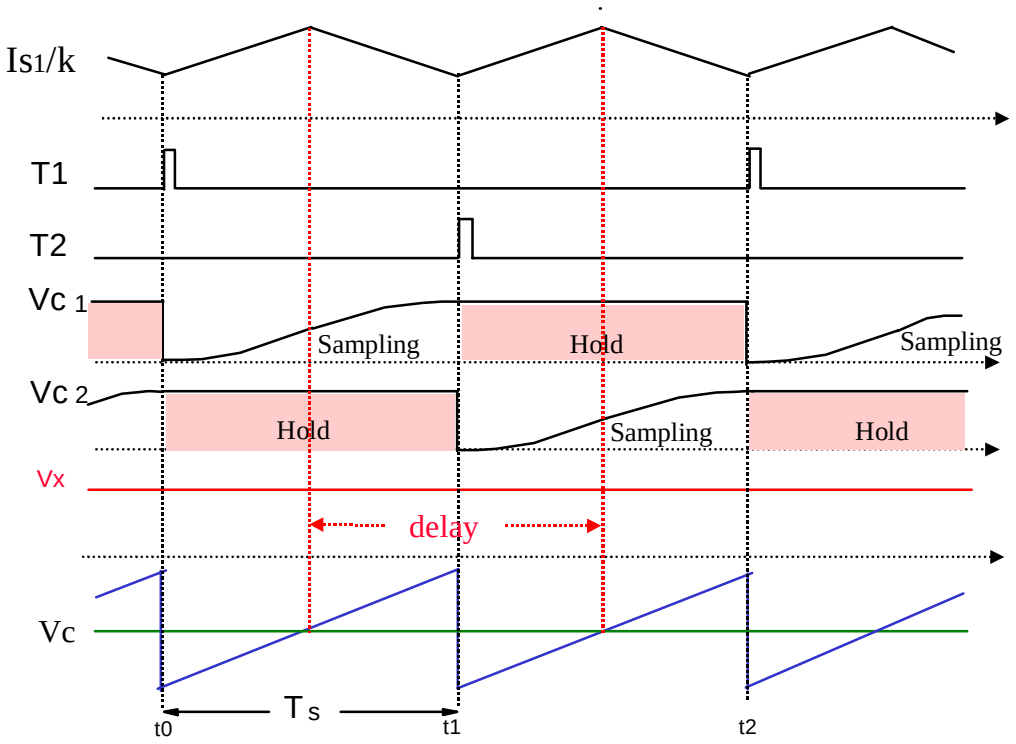



Fig. 3.6 Boost mode operation waveforms

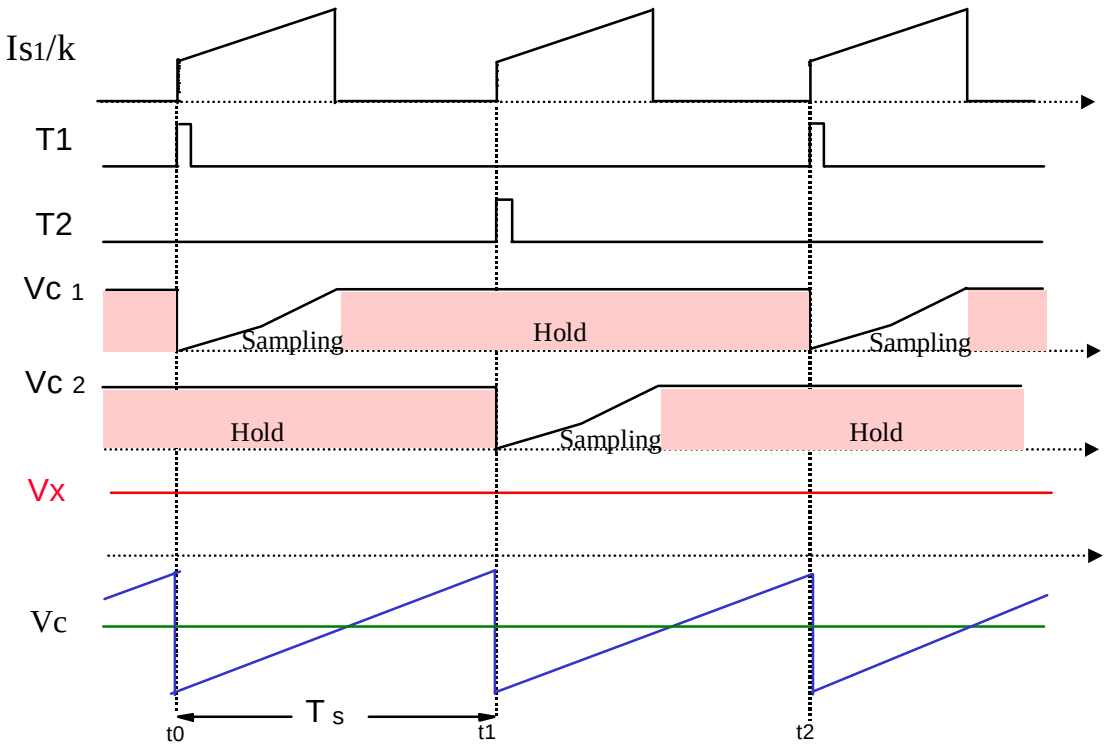



Fig. 3.7 Buck operation mode waveforms

Such charge-hold-charge of $C_1$ and $C_2$ happens consecutively to provide a voltage signal $V_x$ which is proportional to the average input current.

For the buck mode, the operation waveforms are shown in Fig. 3.7. Its basic operation is the same as that in the boost mode except the charge action stops when the buck switch is turned off and capacitor voltage will be held at that value because there is no input current after that point.

Theoretically, for a DC/DC converter under steady state, $V_x$ is a ripple-free DC signal for both buck mode and boost mode operations. Thus the fastest possible average current sensor is obtained.

Due to the sampling and hold effect, there is one switching cycle delay by using this kind of current sensing scheme. This circuit is approximately a zero-order-holder (ZOH), and the mathematical model is shown in Fig. 3.8.

Compared with the three-loop control scheme [22] which needs two current sensors and two current loops, the control with the charge average current sensing scheme is simpler. It needs just one current sensor and one current loop. Therefore, the charge average current sensing scheme is adopted in the variable output PFC circuit.

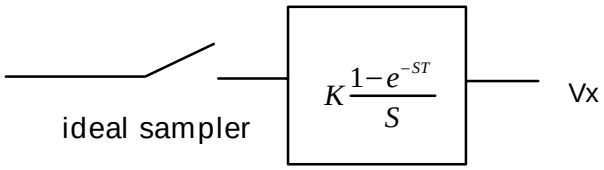



Fig. 3.8 Mathematical model of a ZOH

## 3.3 Buck+Boost PFC PWM Generators

There are two main active switches in a Buck+Boost PFC converter. How to generate the driving signals of the two switches? One method can be found in [21], [22]. Figure 3.9 shows the schematic of the current compensator and the PWM generators. Figures 3.10 and 3.11 show the waveforms of the PWM generators in buck mode and boost mode, respectively. $V_x$ is the output of the average current sensing circuit. The compensator output $V_c$ is compared with two ramps to create the buck duty cycle and the boost duty cycle. The two ramps have the same shape but different DC bias so that the buck duty cycle is one while the boost switch is switching, and the boost duty cycle is zero when the buck switch is running.

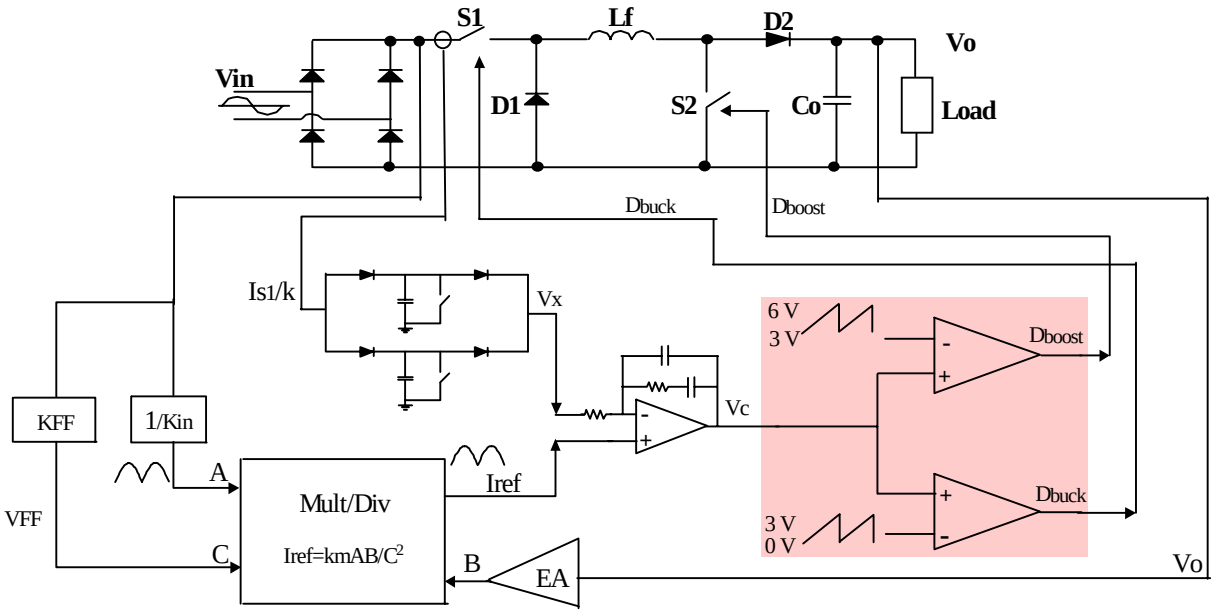



Fig. 3.9 Buck+Boost PFC PWM generator circuit

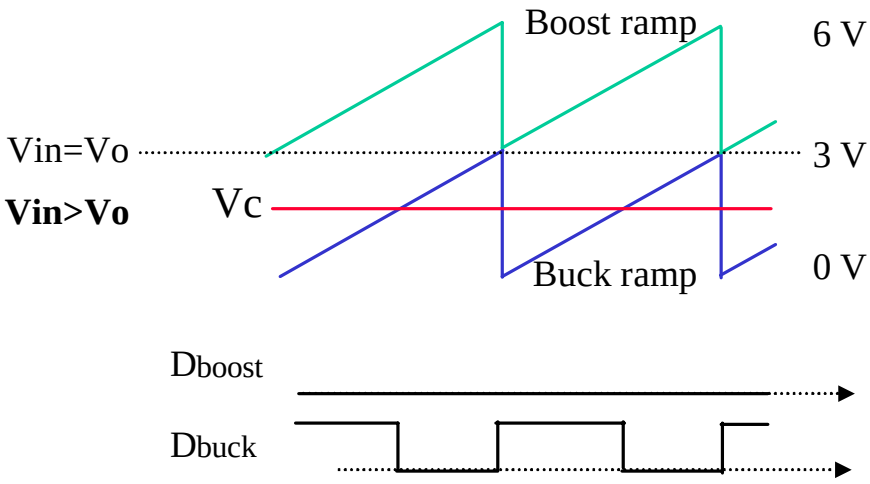



Fig. 3.10 Waveforms of the PWM generators in buck mode

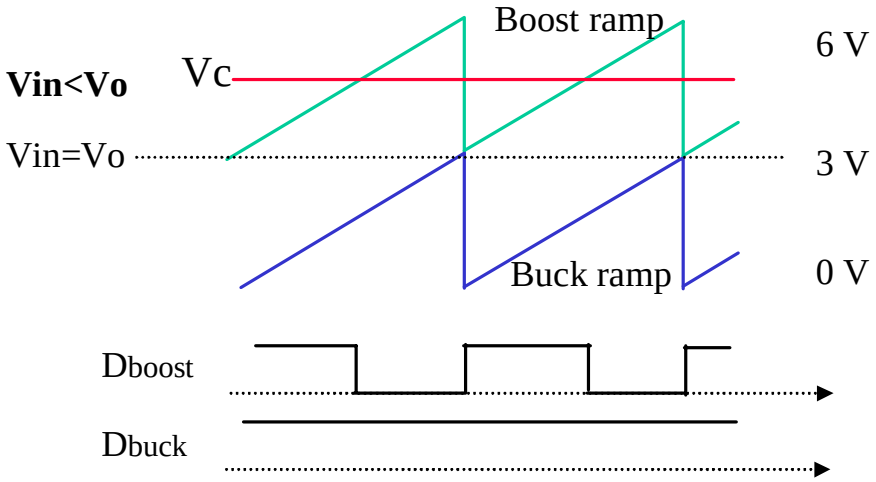



Fig. 3.11 Waveforms of the PWM generators in boost mode

## 3.4 Problem 1: High Input Harmonic Currents at Low Output Voltage

The VOPFC's output voltage is not fixed, but has a very wide range (from 50 V to 300 V for PFC requirement). This causes problems in the current loop design. One problem is that at low output voltage the input current waveform becomes very bad and the input harmonic currents are much higher than the PFC specification. Figure 3.12 shows the measured input harmonic currents when the output voltage of the PFC converter is 100 V. It is clear that these harmonic currents (from $5^{th}$ to $11^{th}$ harmonic) are much higher than IEC1000-3-2 specification.

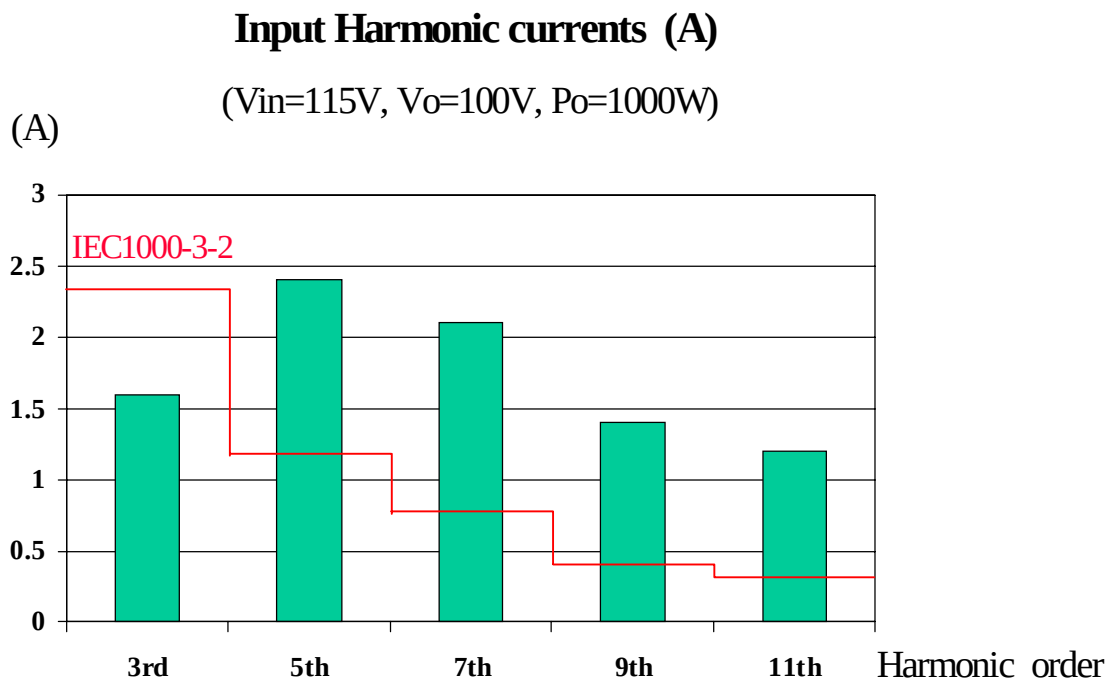



Fig. 3.12 Measurements of input harmonic currents

Because the current loop gain and cross over frequency are closely related to the output voltage (current loop gain is proportional to the output voltage in boost mode), they will change significantly when the output voltage changes. The lower the output voltage is, the narrower the current loop bandwidth will be. Figure 3.13 shows the current loop of the PFC circuit. If we design the circuit according to the low output voltage condition, then the circuit will be unstable at high output voltage. If we design the circuit according to the high output voltage condition, then the circuit will have low power factor and high input harmonic currents at low output voltage, because of the low current loop gain and cross over frequency. (Some current loop gain measurements will be given in the following. The circuit parameters can be found in chapter 4 and appendix A.)

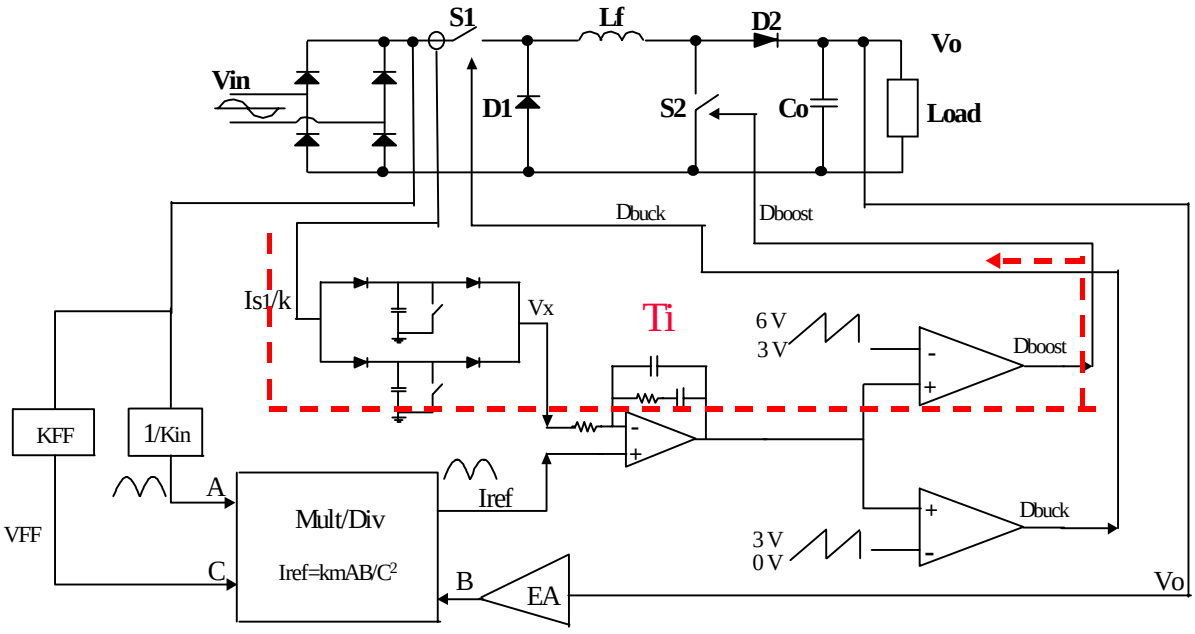
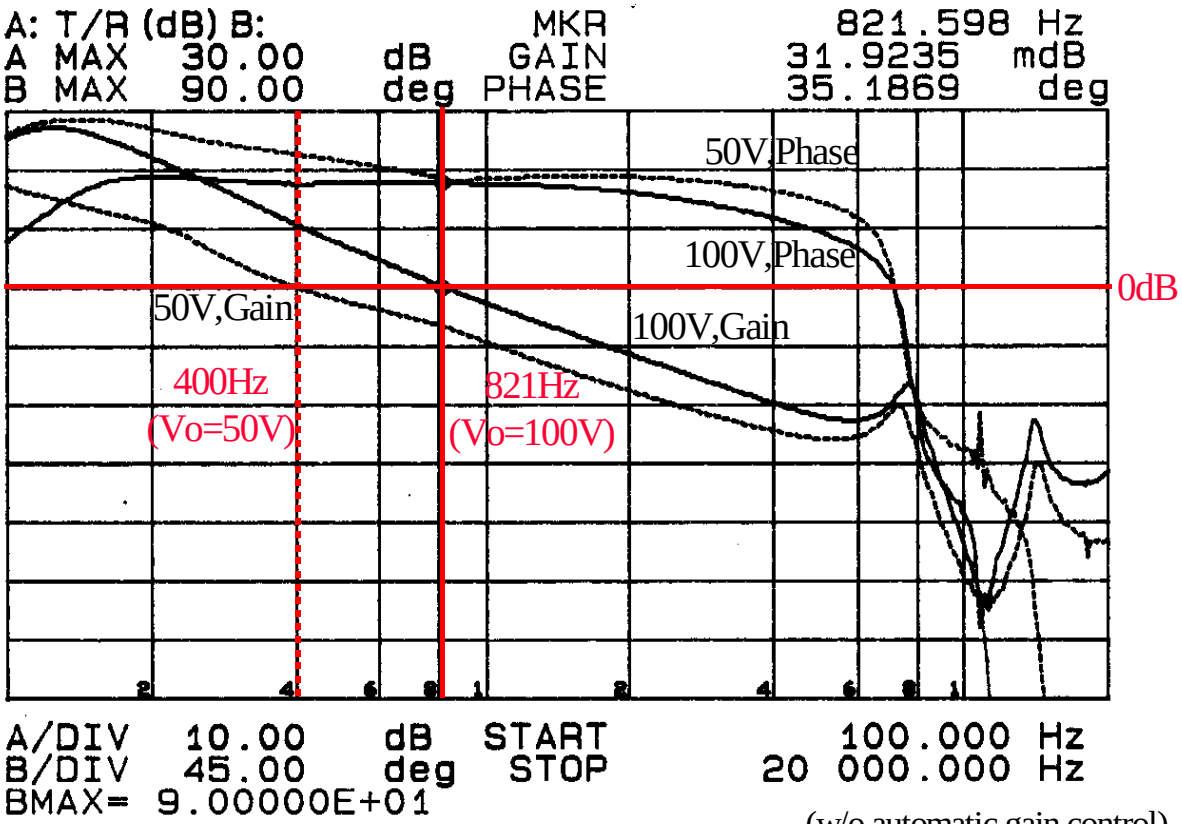



Fig. 3.13 Current loop of the PFC circuit

( Solid line: Vo=100V, Io=4A, Vin=115VDC
Doted line: Vo=50V, Io=4A, Vin=115VDC)




(w/o automatic gain control)

Fig. 3.14 Current loop gain measurement (Vo=100 V & Vo=50 V)

( Vo=300V, Io=3A, Vin=115VDC )

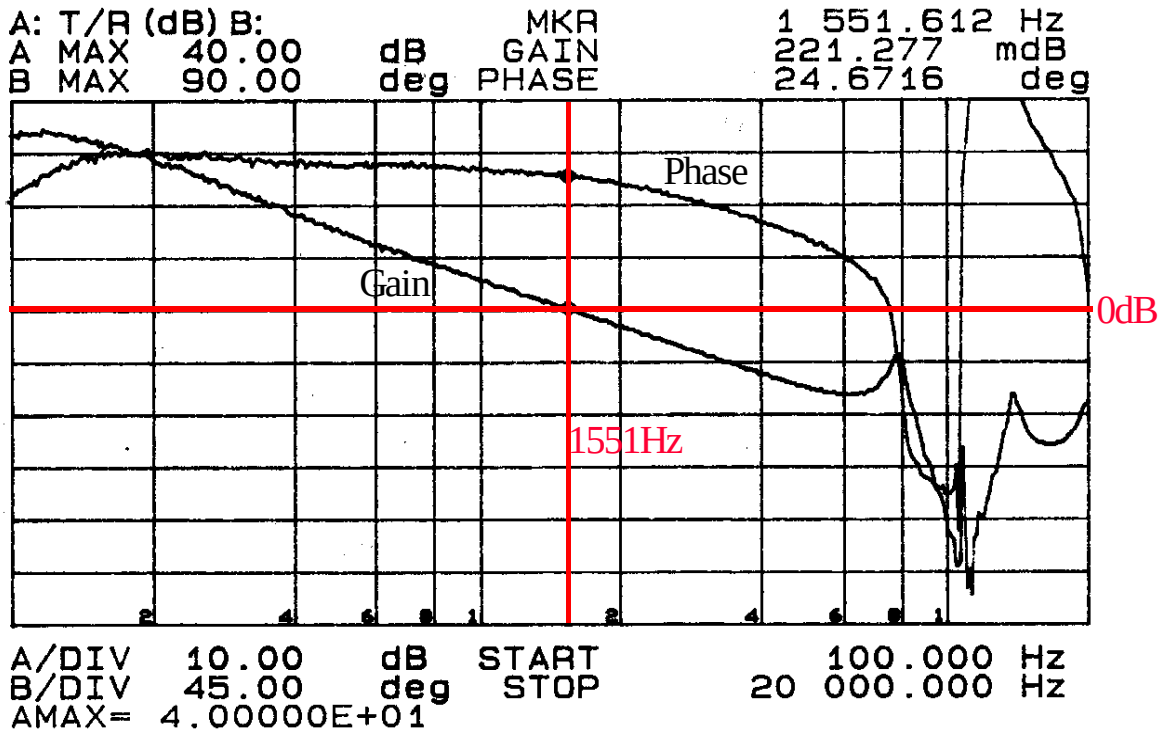



Fig. 3.15 Current loop gain measurement (Vo=300 V)

With a wide output voltage range, the VOPFC circuit will have a very narrow current loop bandwidth at low output voltage. Figure 3.14 shows how dramatically the current loop bandwidth decreases with the output voltage. When the output voltage is 100 V, the bandwidth drops to about 800 Hz. With such a low current loop bandwidth, the input harmonic currents will be very high and the circuit cannot meet the IEC requirements. This is already shown in Figure 3.12. When the output voltage is 50 V, the current loop bandwidth further decreases to about 400 Hz! Figure 3.15 shows the current loop gain measurement when the output voltage is 300 V. It is clear that the current loop bandwidth will be much higher at high output voltage condition than that at the low output voltage condition.

## 3.5 Automatic Gain Control of the Current Loop

To solve this problem, an automatic gain control circuit is proposed and added to the current loop. Figure 3.16 shows the circuit diagram after adding the gain control function. This circuit is quite simple, as shown in Fig. 3.17.

This gain control circuit is actually a voltage divider which can be automatically adjusted with the output voltage signal. Here, Sa and Sb can be either tiny switches or IC chips. When the output voltage is low, both Sa and Sb are open. When the output voltage is raised to a preset level, Sa is closed, while Sb is still open. When the output voltage exceeds a higher level, both Sa and Sb are closed. So the gain of the voltage divider will be reduced when the output voltage is higher. Therefore, the current loop gain and cross over frequency can be adjusted automatically to remain approximately unchanged when the output voltage varies across a wide range. It is clear that the current loop gain is regulated by step changes. If needed, more switches and resistors can be added to generate more step changes. The adjusting of the current loop gain will be smoother with more step changes, and the input current shape will be more ideal in the entire range of the output voltage.

Figure 3.19 shows the current loop gain measurement after the automatic gain control circuit is added. Now the current loop bandwidth increases from about 800 Hz to about 3200 Hz!

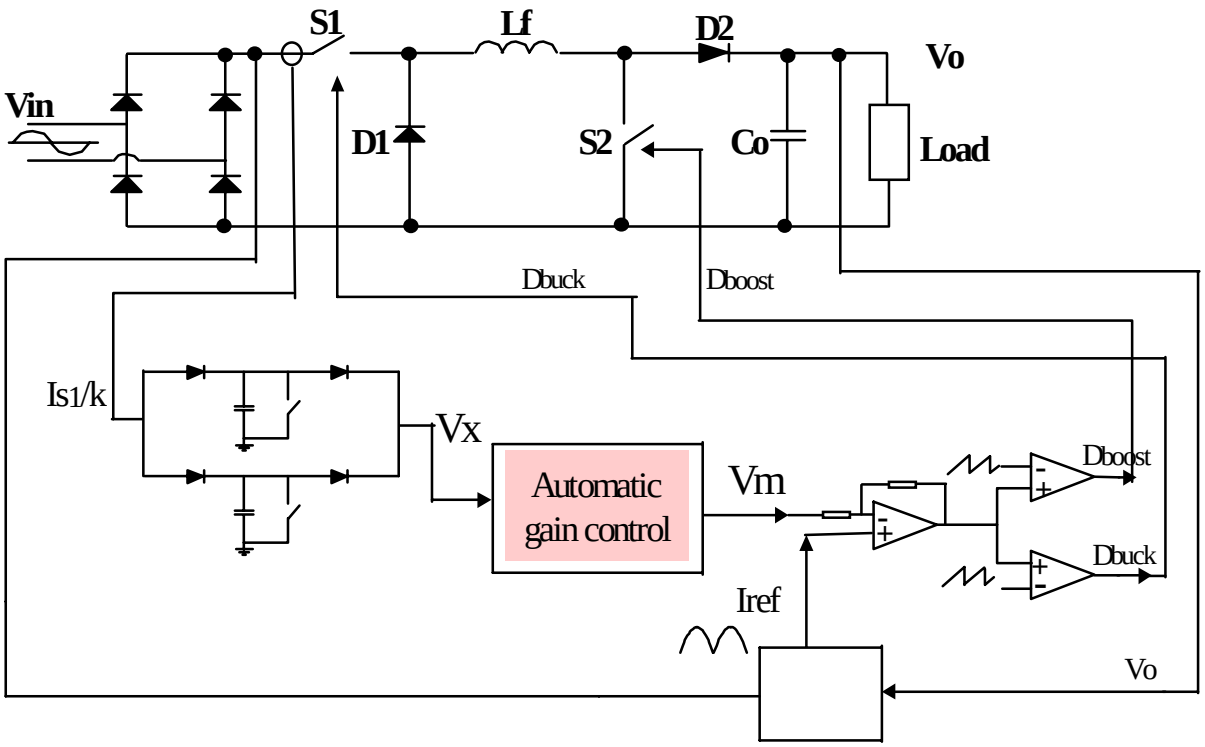



Fig. 3.16 Circuit diagram after adding gain control function

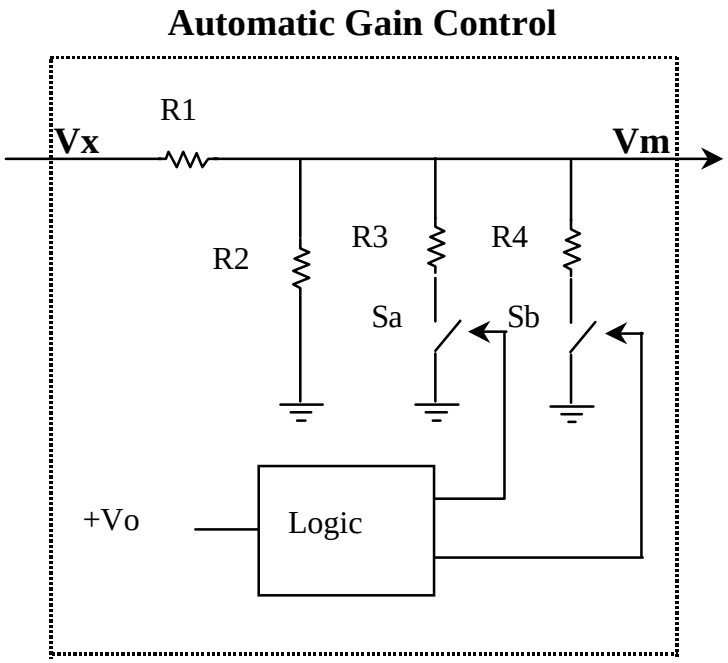



Fig. 3.17 Automatic gain control circuit

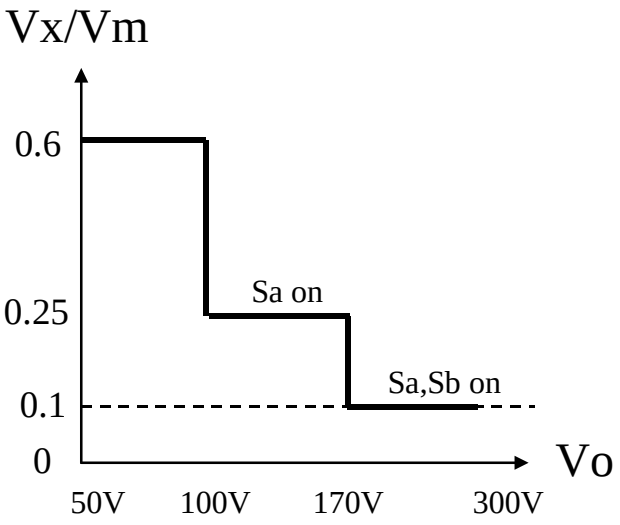



Fig. 3.18 Step changes of the automatic gain control

## Current loop Gain Measurement
### (with Automatic gain Control)

( Vo=100V, Io=4A, Vin=115VDC )

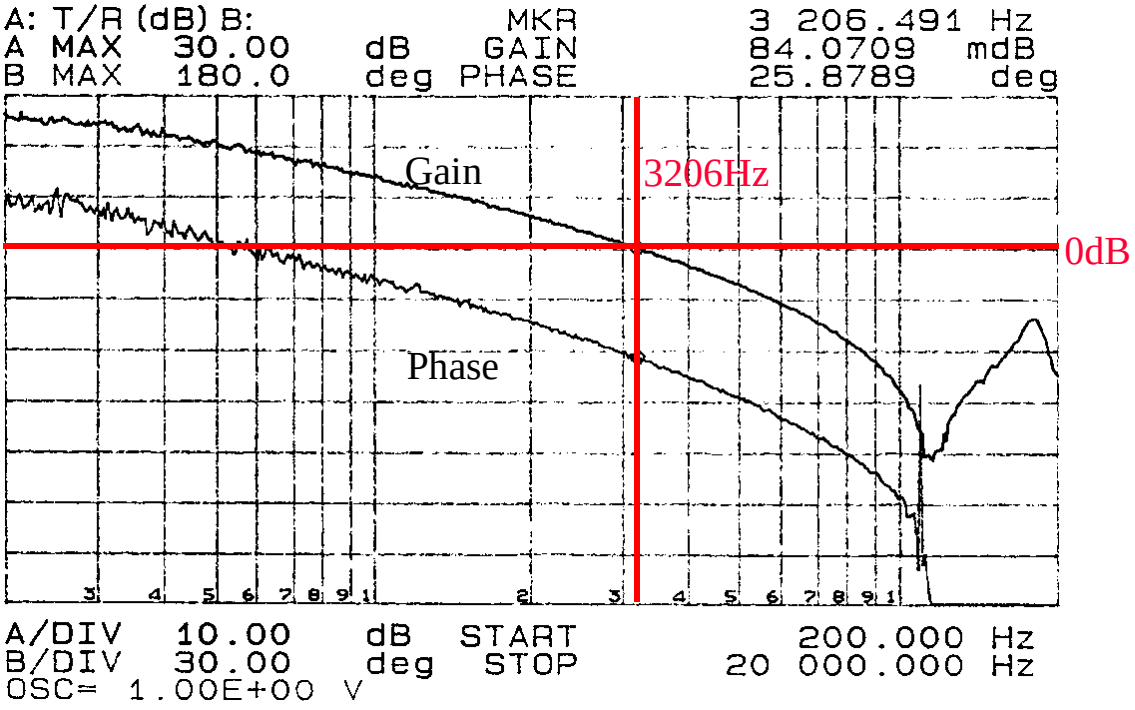



Fig. 3.19 Current loop gain measurement

(Vo=100 V, with automatic gain control)

## 3.6 Problem 2: Insufficient Phase Margin at Full Load

To get a better power factor and further reduce the input current harmonics, the current loop cross over frequency should be as high as possible. However, the phase margin will be smaller. In the VOPFC, the switching frequency is only 20 kHz, to ensure high efficiency. So the current loop cross over frequency can only be about 2 kHz. At the

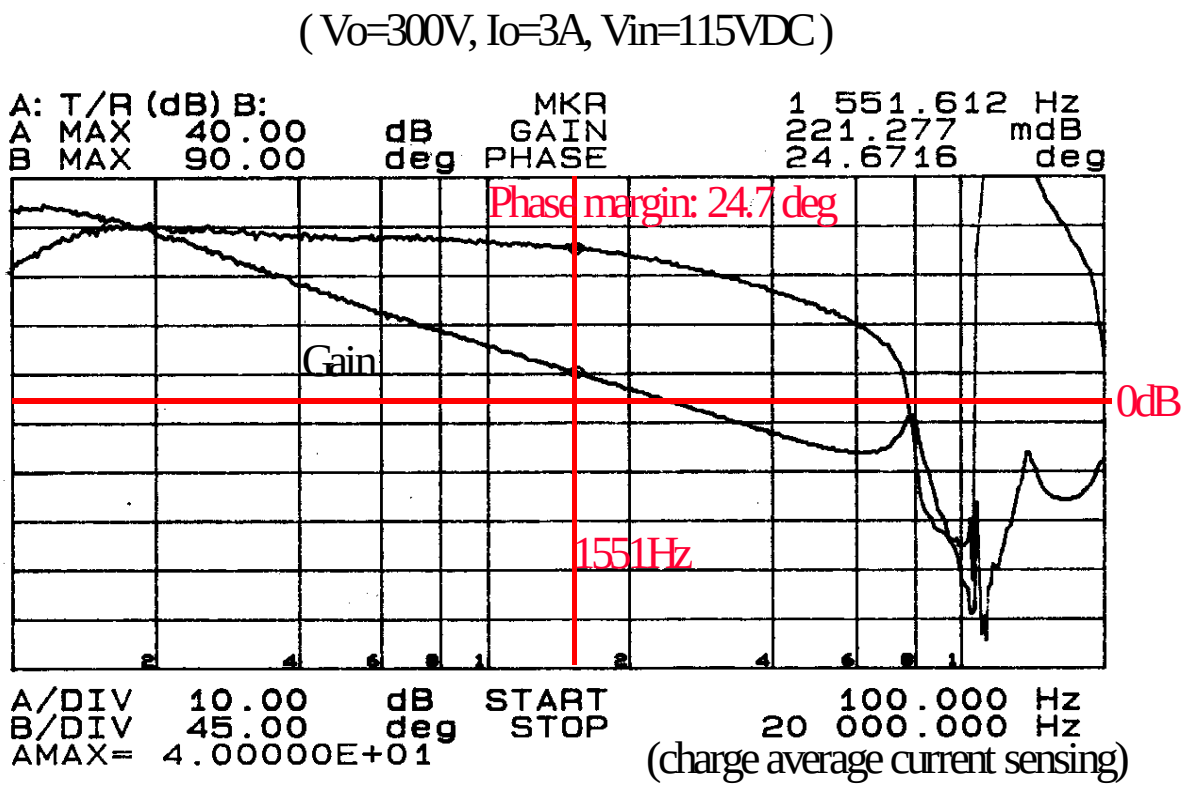



Fig. 3.20 Current loop gain measurement

(Vo=300 V, charge average current sensing)

maximum output power test condition (Vo=300 V, Po=2 kW), it is found that the current loop cross over frequency is not high enough to let the circuit meet the IEC 1000-3-2 requirements. However, the cross over frequency can hardly be increased because of insufficient phase margin.

Figure 3.20 shows this problem. When the output voltage is 300 V, the current loop cross over frequency is about 1550 Hz. At this time, the phase margin is less than 25 degrees. If the current loop bandwidth is pushed to higher frequency, the phase margin will be even smaller and the circuit will become unstable.

## 3.7 Modified Input Current Sensing Scheme

To solve this problem, a modified input current sensing scheme is proposed here, shown in Fig. 3.21. As has been mentioned before, the charge average current sensing circuit will always cause some phase delay. The idea of the modified current sensing scheme is to bypass the charge average current sensing circuit with a resistor when the output voltage is always higher than the peak line voltage, because in this condition the converter is totally in boost operation and the input current is continuous. Therefore, the phase delay caused by the charge average current sensing circuit is avoided.

The charge average current sensing circuit will be bypassed automatically by a logical circuit when the output voltage is higher than the peak line voltage. In that case, the converter is just a typical boost PFC circuit. Switch SW1 will be off and switch SW2 will be on. So a resistor is used to sense the input current. The hall sensor output signal ($Is_1/k$) will go through this resistor instead of the charge average current sensing circuit. While the circuit is in Buck+Boost operation, switch SW1 is on and switch SW2 is off, and the charge average current sensing circuit is still employed.

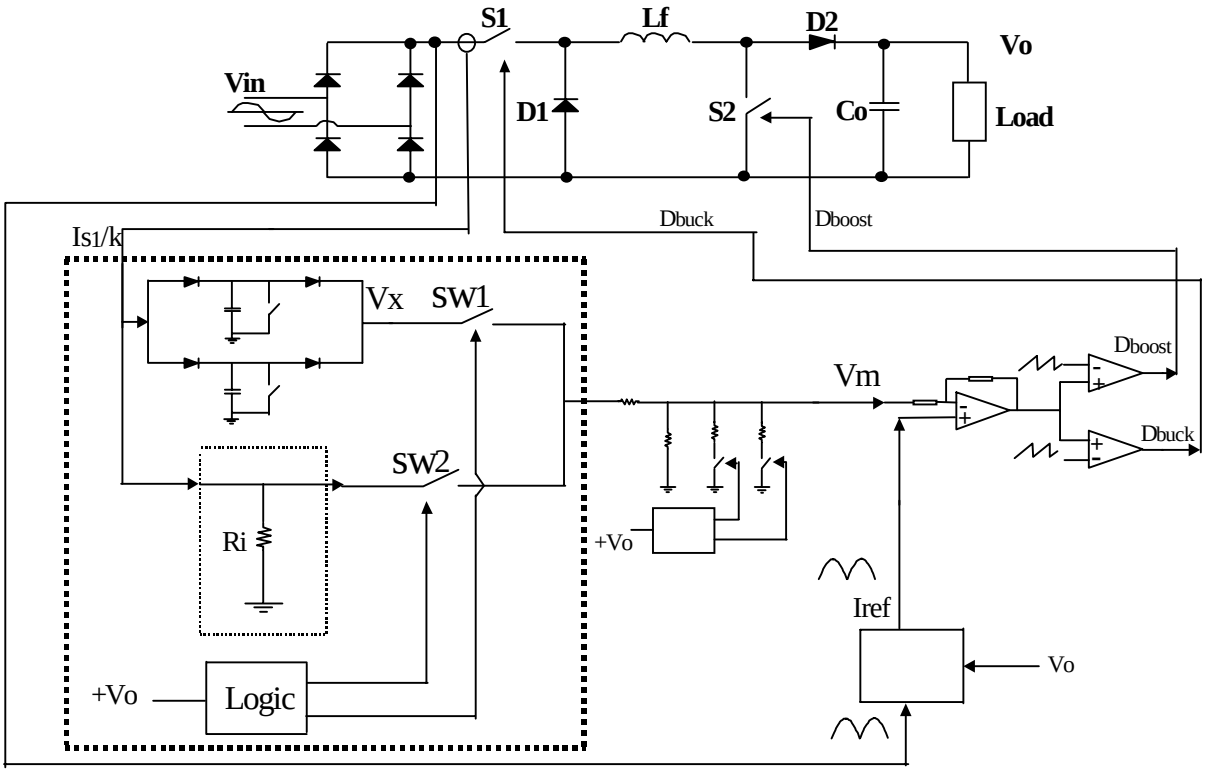



Fig. 3.21 Modified input current sensing scheme

Figure 3.22 shows the current loop gain measurement using the modified input current sensing scheme when the output voltage is 300 V. It is clear that the current loop cross over frequency has been pushed from about 1550 Hz to about 2120 Hz. At the same time, the phase margin is also increased to about 37 degrees.

**Current loop Gain Measurement**

**(Resistor current sensing)**

( Vo=300V, Io=3A, Vin=115VDC )

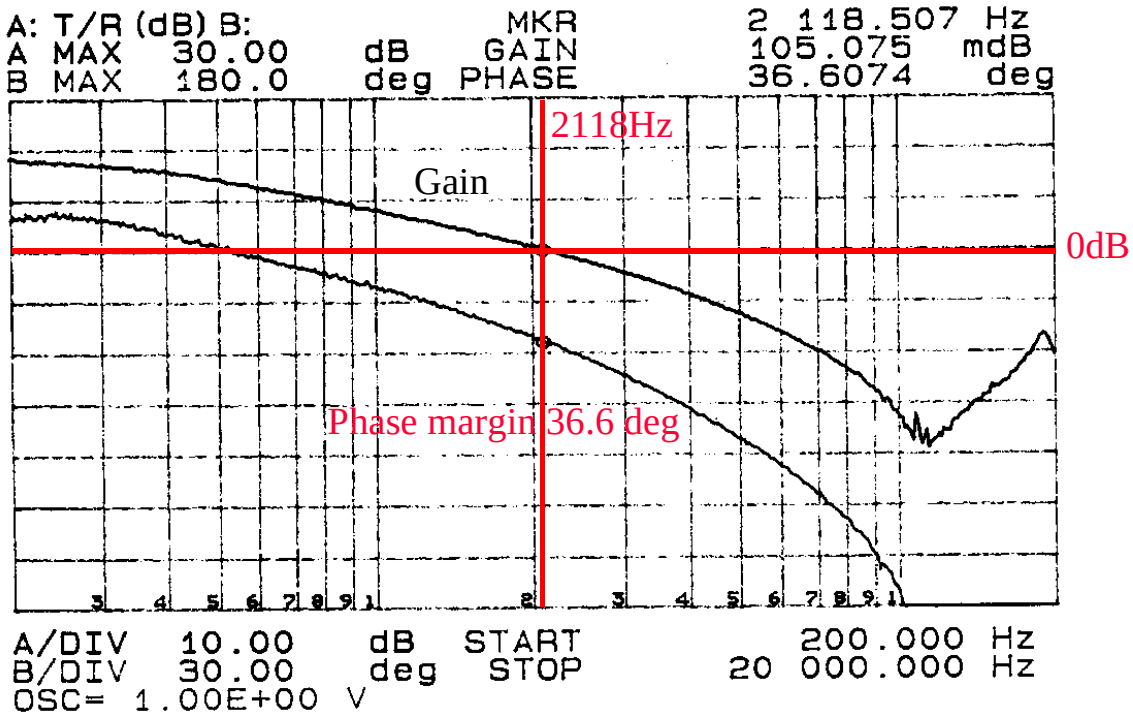



Fig. 3.22 Current loop gain measurement

(Vo=300 V, modified current sensing)

# 4. SOME DESIGN ISSUES AND EXPERIMENTAL RESULTS

## 4.1 Some Design Issues of the VOPFC Circuit

### 4.1.1 Inductance Value Selection

The selection of the inductance value for the Buck+Boost PFC circuit is based on the following criteria:

- current ripple and maximum current in the inductor
- discontinuous conduction at the line voltage cross overs
- volume and weight

The selection involves a trade-off decision, because reduction of inductor current ripple and discontinuous operation mode always result in a larger inductor. However, a reduction of the inductance value does not imply a proportional size reduction of the inductor. Large current ripple corresponding to smaller inductance increases ac core losses, offsetting the volume reduction expected.

The inductor current ripple for the boost converter is:

$$\Delta i(t) = \frac{Vin(t)}{L} \cdot [1 - \frac{Vin(t)}{Vout}] \cdot \frac{1}{fs} \qquad (4.1)$$

The inductor current ripple for the buck converter is:

$$\Delta i(t) = \frac{Vout}{L} \cdot [1 - \frac{Vout}{Vin(t)}] \cdot \frac{1}{fs} \quad (4.2)$$

Where Vin(t) is the input voltage, Vout is the output voltage, L is the inductance value, and fs is the switching freqnency.

For the Buck+Boost converter the worst case ripple at the input corresponds to the discontinuous input current characteristic of buck converter operation.
After considering all the factors, a 400 uH inductor is used in the circuit. The core used here is a TDK PC30, EIC 90 ferrite core. (Vol=90.8 $cm^3$, le=14.6 cm, Ae=6.32 $cm^2$). The size is about 90 mm×60 mm×30 mm. The air gap is 10 mm, and the inductor has 40 turns of winding (AWG #14, two wires parallel).

### 4.1.2 Output Capacitance Value Selection

To select the output capacitance value in this circuit, the main factor is the output ripple voltage which is caused by the second harmonic. The equation to define the capacitance value can be expressed as:

$$C_o = \frac{P_{in}}{2\pi f_r \cdot V_{opk} \cdot V_0} \quad (4.3)$$

Where Vopk is the peak value of the output ripple voltage (the peak to peak value will be twice this), and fr is the second harmonic line frequency.
The worst case will happen when Vo is 50 V and Vopk is 2.5 V (for peak to peak output ripple <10% ). In this case, Co will have the largest value,

$$Co \approx \frac{450}{2\pi \times 120 \times 2.5 \times 50} = 4777 \text{ uF}$$

If it is possible, the capacitor value should be as small as possible. After many experiments, 3300 uF/450 V (total) output capacitors are used. Under the maximum load (300 V, 2 kW), the output ripple is about 5 V, which is well under the specification (10%, i.e. 30 V). When Vo=50 V, the output ripple is about 10%. The output capacitance can be further reduced. However, at low output voltage (Vo=50 V), the output ripple will exceed 10%.

### 4.1.3 Current Error Amplifier Compensation

Shown in Fig. 4.1, the current amplifier with a two pole, one zero compensation network is adopted in the control circuit.

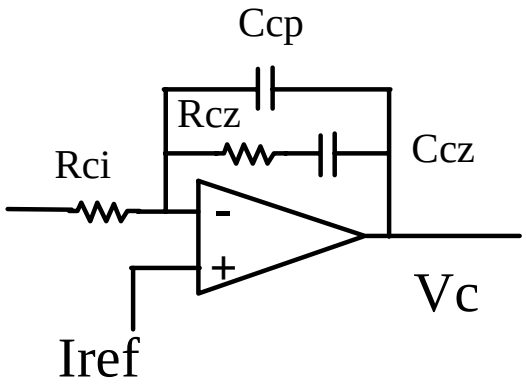



Fig. 4.1 Current error amplifier

The small signal transfer function of the amplifier is:

$$Gc(s) = \frac{\omega i}{s} \cdot \frac{1 + s/\omega z}{1 + s/\omega p} \tag{4.4}$$

where

$$\omega i = \frac{1}{Rci \cdot (Ccp + Ccz)} \tag{4.5}$$

$$\omega z = \frac{1}{Rcz \cdot Ccz} \tag{4.6}$$

$$\omega p = \frac{Ccp + Ccz}{Rcz \cdot Ccp \cdot Ccz} \tag{4.7}$$

If Ccp<< Ccz, then

$$\omega i \approx \frac{1}{Rci \cdot Ccz} \tag{4.8}$$

$$\omega p \approx \frac{1}{Rcz \cdot Ccp} \tag{4.9}$$

The high frequency pole $\omega p$ is placed near the switching frequency to filter out the switching noise. And the pole will not affect the frequency response of the current loop when the pole is above half the switching frequency. The zero $\omega z$ is placed at about 500 Hz to obtain enough phase margin. The integrator gain $\omega i$ can be placed between $\omega z$ and $\omega p$.

The measured current loop gain and phase characteristics of both boost mode and Buck+Boost mode are shown in Fig. 3.22 and Fig. 3.19, respectively.

### 4.1.4 Voltage Error Amplifier Compensation

Compared to the switching frequency, the bandwidth of the voltage loop is so small that the principal requirement for the voltage control loop is to keep the input distortion to a minimum. The loop bandwidth must be low enough to attenuate the second harmonic of the line frequency on the output capacitor to keep the modulation of the input current

small. As shown in Fig. 4.2, the voltage loop compensator has the following small signal transfer function:

$$Gv(s) = \frac{\omega v}{1 + s / \omega pv} \tag{4.10}$$

where

$$\omega v = \frac{1}{Rvi \cdot Cvf} \tag{4.11}$$

$$\omega pv = \frac{1}{Rvf \cdot Cvf} \tag{4.12}$$

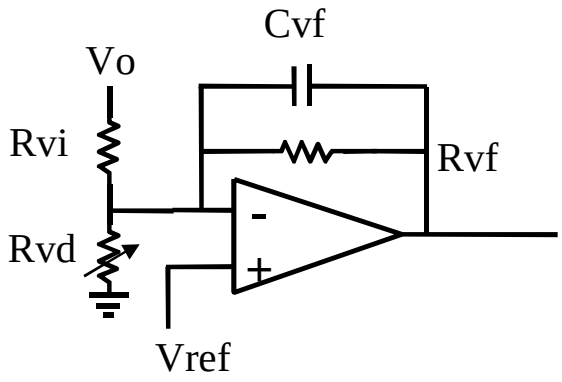



Fig. 4.2 Voltage error amplifier

The bandwidth of the voltage loop is designed to be less than one fourth of the line ripple frequency to minimize the distortion. The pole $\omega pv$ is placed after the cross over frequency of the voltage loop. The pole should provide enough attenuation for the line frequency ripple and provide a reasonable phase margin.

### 4.1.5 Feed-forward Voltage Divider

The low pass filter provides a voltage proportional to the RMS value of the line voltage. The feed-forward ripple voltage must be kept small to achieve a low distortion input current. A two-pole filter has been chosen because it has a faster transient response than a single pole filter. The low pass filter is designed to have a double real pole at a frequency about one fourth of the line frequency. The capacitor and resister values can be given by the following equations:

$$Vff = \frac{Vin(av) \cdot Rf3}{Rf1 + Rf2 + Rf3} \tag{4.13}$$

$$Vnode = \frac{Vin(av) \cdot (Rf2 + Rf3)}{Rf1 + Rf2 + Rf3} \tag{4.14}$$

$$Cf1 = \frac{1}{2\pi \cdot fp \cdot Rf2} \tag{4.15}$$

$$Cf2 = \frac{1}{2\pi \cdot fp \cdot Rf3} \tag{4.16}$$

where Vff=1.414 V, Vnode≈7.5 V, Vin(av) is the average value of Vin, and fp is the pole frequency.

### 4.1.6 PFC Controller

An enhanced high power factor preregulator, UC3854B, is used as the main PFC control chip in the circuit.

The UC3854B contains a voltage amplifier, an analog multiplier/divider, and a current amplifier. Pin 11 is the voltage amplifier inverting input pin. It is connected to the output of the PFC converter through a feedback network. The output of the voltage error

amplifier is available on pin 7 and it is also an input to the multiplier. The other input to the multiplier is pin 6, and it is used for sensing instantaneous line voltage.

Pin 8 is the feedforword input pin, and the input value is squared before being fed into the divider input of the multiplier. The output of the multiplier and the non-inverting input of the current amplifier are connected together at pin 5. The inverting input to the current amplifier is on pin 4, and pin 3 is the current amplifier output.

In our application, the inner PWM circuit of UC3854B has not been used. Instead, two external comparators (LM393) are adopted to generate the buck and the boost PWM signal. Figure 3.9 shows the schematic of the current compensator and the PWM generators.

The PWM oscillator frequency is set by a resistor Rset and a capacitor Ct which are connected to pin 12 and pin 14, respectively. The PWM frequency is given by:

$$F_s = \frac{1.25}{R_{set} \cdot C_t} \tag{4.17}$$

### 4.1.7 Discharging Signal Generating of Charge Average Current Sensing Circuit

In Fig. 4.3, the narrow driving signals of transistor T1 and T2 in the charge average current sensing circuit are generated by a Retriggerable Monostable Multivibrators (74HCT123). The multivibrators feature pulse width control by selection of external resistance and capacitance values. The output pulse Tw is a function of the external components Cext and Rext, which is given by

$$Tw = K \cdot \mathrm{Re}xt \cdot Cext \tag{4.18}$$

where K is nominally 0.45

The multivibrators are triggered by the output signal of a D-type Flip-Flop (74LS74A). This signal is a square wave at half switching frequency of the converter. The clock pulse input of the D-type Flip-Flop is given by the output PWM signal of UC3854B, an enhanced high power factor prereguIator.

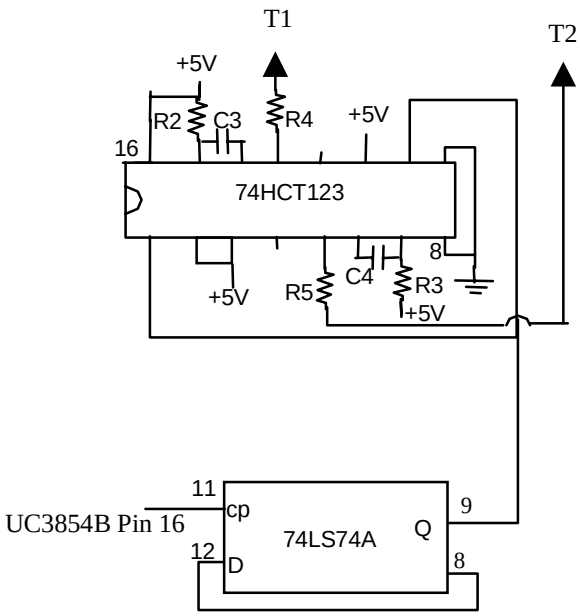



Fig. 4.3 Discharging signal generating of charge average current sensing circuit

### 4.1.8 Automatic Gain Control Circuit

As discussed in the previous chapter, an automatic gain control circuit is proposed and added to the current loop, and a general form of the circuit is shown in Figure 3.17. A

quite simple and detailed automatic gain control circuit is also developed here, as shown in Fig. 4.4.

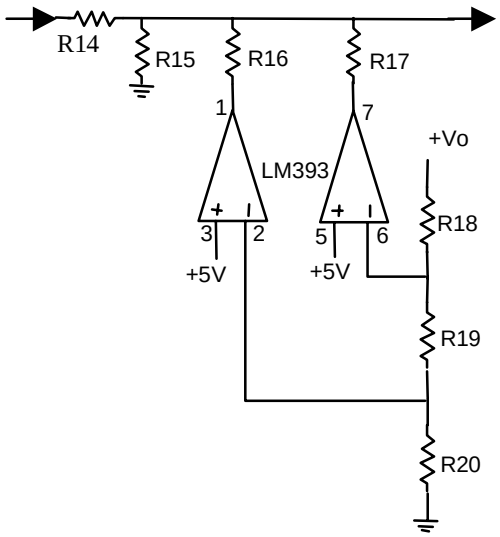



Fig. 4.4 A proposed automatic gain control circuit

This circuit consists of two comparators and some resistors ( R14-R20 ). The two preset output voltages are about 100 V and 170 V here. When the output voltage is below 100 V, the output terminals of the two comparators are open, so there is no effect on the current loop. When the output voltage reaches 100 V, one output terminal of the comparators (Pin 7 of LM393) will be pulled to ground, and R17 is connected to the circuit. Hence the current loop gain can be reduced to the value that you desire, by choosing the resistor. Similarly, when the output voltage reaches about 170 V, both R17 and R16 are connected to the circuit, and the current loop gain will be reduced further.

It is clear that there are two step changes here to adjust the current loop gain. If it is needed, more comparators can be added to generate more step changes. The more steps, the smoother the gain change will be, and the more ideal the input current shape will be. However, the circuit will be more complex.

### 4.1.9 Modified Input Current Sensing Circuit

The detailed modified input current sensing circuit is shown in Fig. 4.5, To bypass the charge average current sensing circuit in the boost mode (i.e., when output voltage is higher than the peak input voltage), three tiny switches (T3, T4, T5) are used. When the VOPFC operates in the Buck+Boost mode, T3 is always on and T4, T5 are always off, so the charge average current sensing circuit is in effect. When the output voltage is high and the VOPFC operates in the boost mode, T3 is always off and T4, T5 are always on. So the charge average current sensing circuit does not work, and a resistor (R21) is used to sense the input current signal.

Two diodes, D8 and D9, are also used in this circuit. D9 is used to block the body diode of the MOSFET T4. D8 is used to prevent the output current of the hall sensor to flow through D3 and /or D4 while T4, T5 are on.

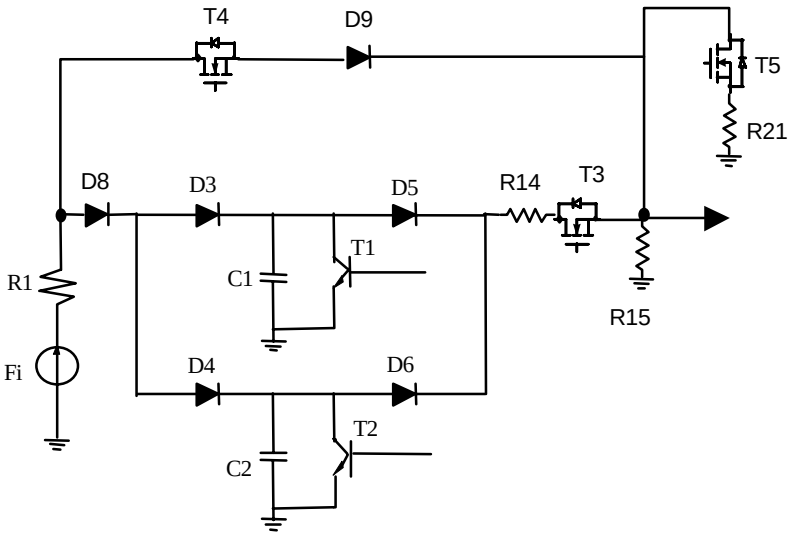



Fig. 4.5 Modified input current sensing circuit

### 4.1.10 Control of the Modified Current Sensing Circuit

The gate driving signals of the modified input current sensing circuit switches T3, T4, T5 are provided by a feedback circuit which is mainly a comparator (LM393), (and also contents R22-R27), as shown in Fig. 4.6. Hysteresis is put in this feedback loop of the comparator to suppress possible oscillation. It can function as a Schmitt trigger with presettable trigger points.

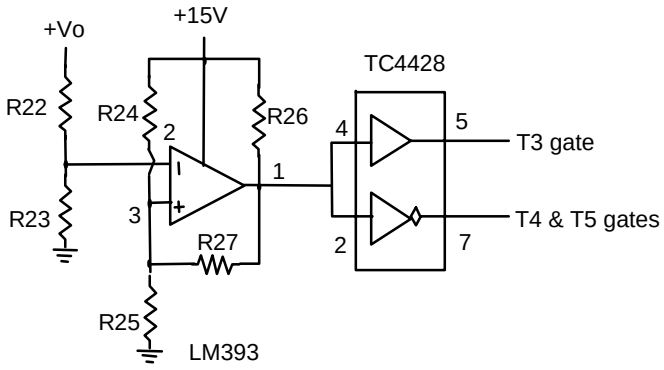



Fig. 4.6 Control of the modified current sensing circuit

The upper trip output voltage, Vu, is set by:

$$Vu = \frac{Vcc \cdot R25}{(R24 || R27) + R25} \cdot \frac{R22 + R23}{R23} \tag{4.19}$$

The lower trip output voltage, Vl, is set by:

$$Vl = \frac{Vcc \cdot (R25 || R27)}{R24 + (R25 || R27)} \cdot \frac{R22 + R23}{R23} \tag{4.20}$$

Where, Vcc is 15 V here. Vu, Vl are set at about 190 V and 180 V, respectively. Hence, when output voltage rises above 190V, T4 and T5 will turn on. When output voltage drops below 180 V, T3 will turn on.

### 4.1.11 Protection circuits

Over current protection circuit is shown in Fig. 4.7. The input current signal is from the output of hall sensor, and the output (LM393 pin 7) is connected to the PWM control signal (UC3854B pin 3). When the current through the buck switch reaches about 40 A, this circuit will pull the PWM control signal (UC3854B pin 3) to ground, so both buck and boost switches will be turned off. In this circuit, AMP-02 is a high accuracy 8-pin instrumentation amplifier.

Output over voltage protection circuit is a similar circuit, shown in Fig. 4.8. When the output voltage reaches about 320 V, the PWM control signal will be pulled to zero, and both buck and boost switches will be turned off.

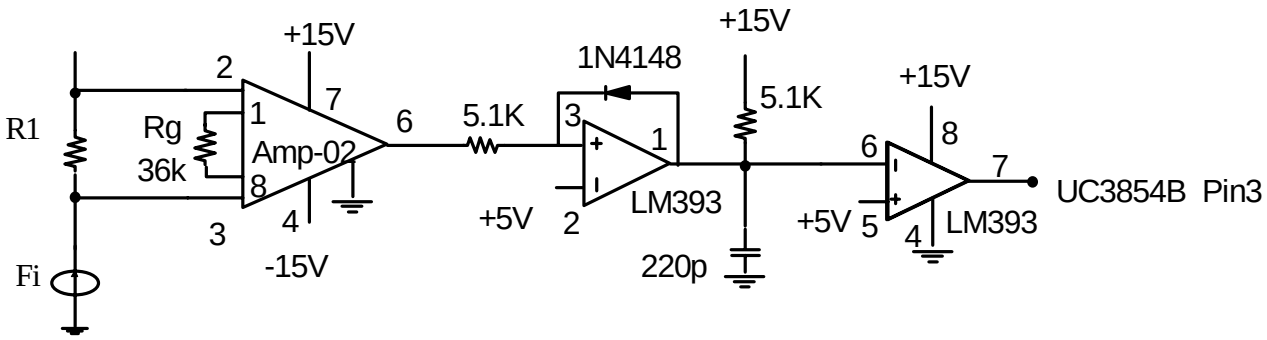



Fig. 4.7 Over current protection circuit

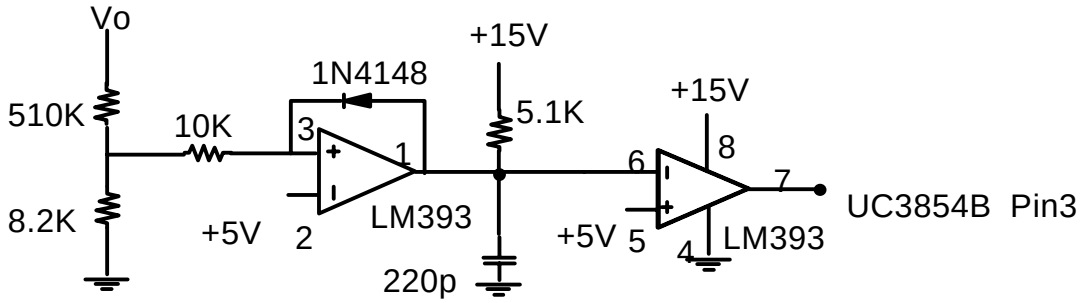



Fig.4.8 Output over voltage protection circuit

### 4.1.12 Variable output PFC system schematic

Figure 4.9 shows the variable output PFC circuit system schematic. A list of components can be found in appendix A.

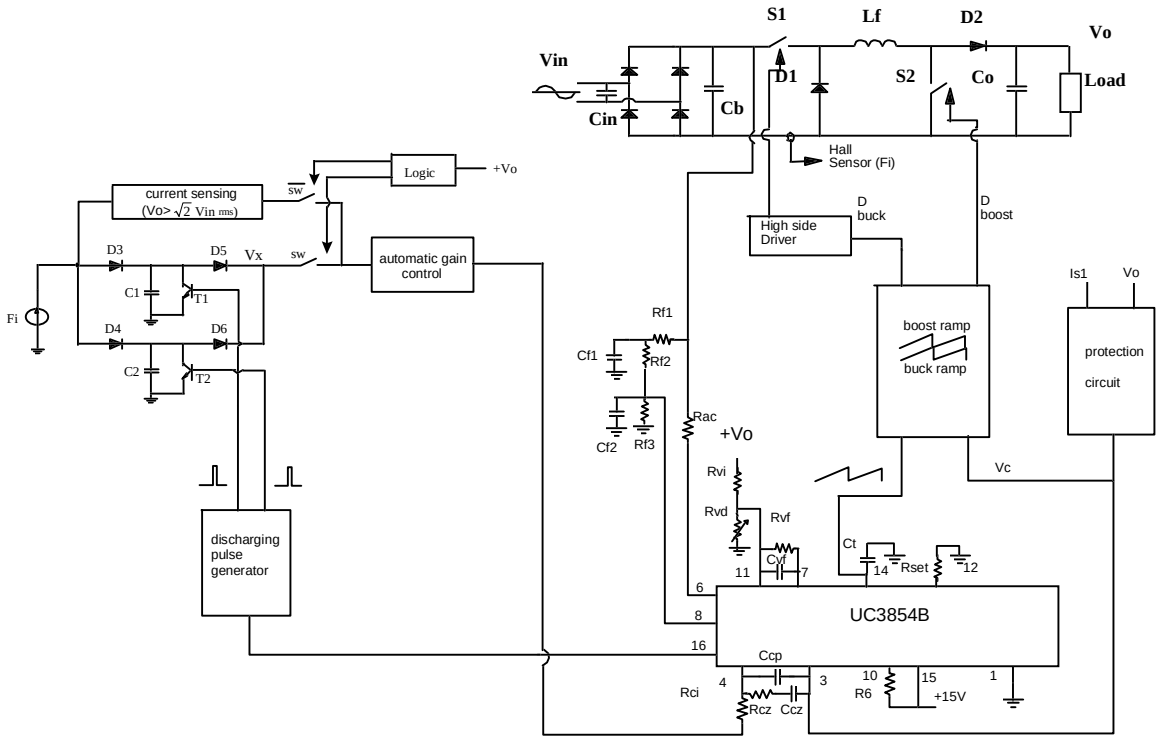



Fig. 4.9 Variable output PFC system schematic

## 4.2 Experimental Results

A prototype of a 2 kW, 20 kHz VOPFC circuit was implemented. The major components used are listed below:

S1: IRGP450U (IR IGBT)

S2: IXGH30N60 (IXYS IGBT)

D1,D2: DSEI30-06A (IXYS)

Lf: 400 uH

Co: 3300 uF

### 4.2.1 Experimental Waveforms

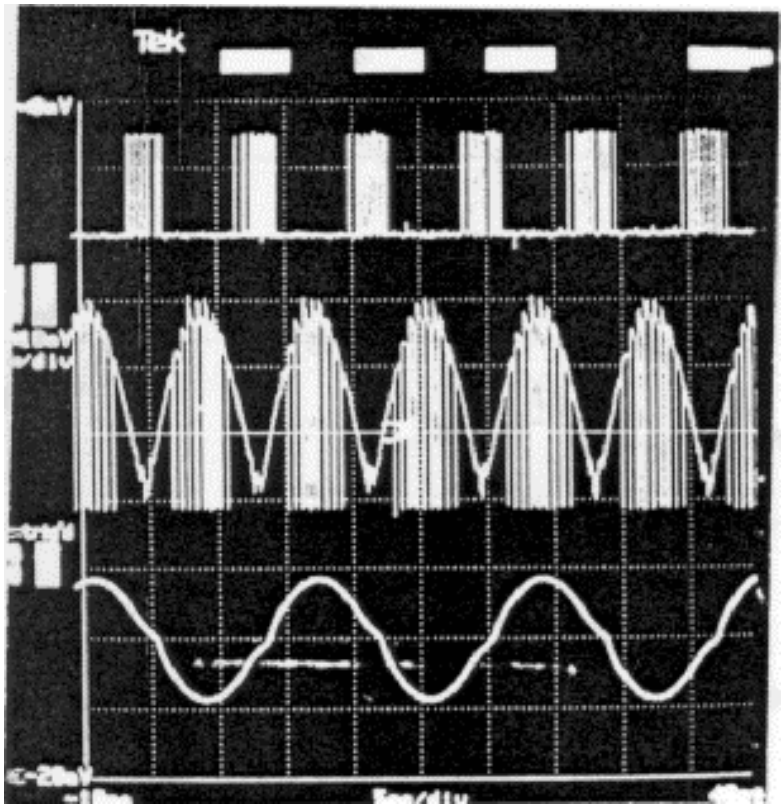



Fig. 4.10 Buck+Boost operation (Vo=80 V, Io=8 A)

Figures 4.10 and 4.11 show the experimental waveforms of the VOPFC circuit. The top waveform Dboost is the gate signal of the boost switch S2. The middle waveform VD1 is the voltage on the buck diode D1 with the envelope representing the rectified line voltage. The bottom waveform Iin is the input current.

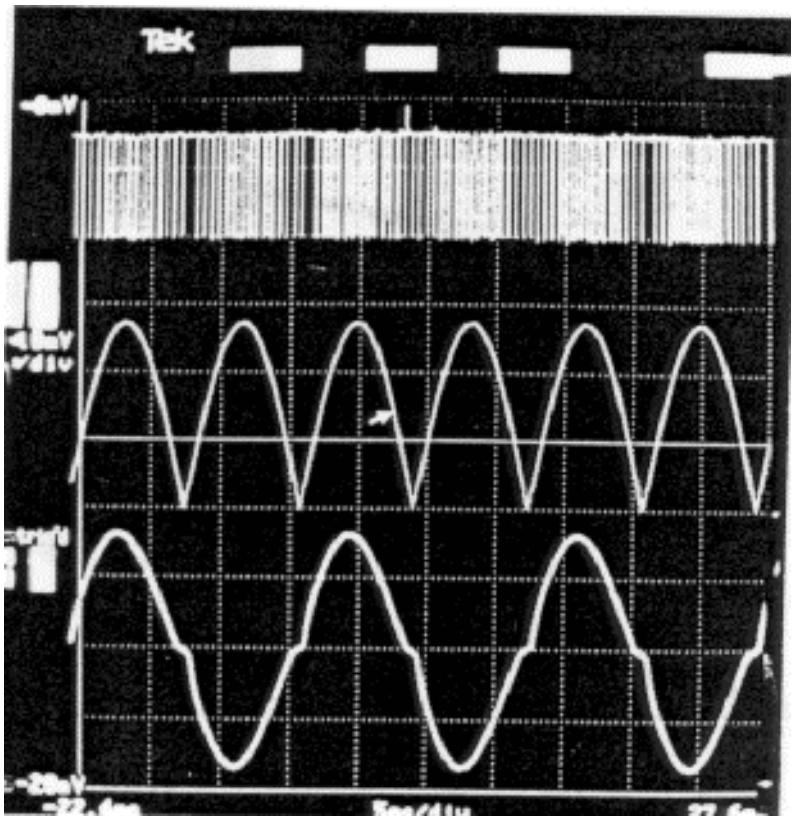



Fig. 4.11 Boost operation (Vo=300 V, Io=6.7 A)

### 4.2.2 Measured Efficiency

Figures 4.12 and 4.13 show the measured efficiencies. It is clear that the efficiency is higher at high line than that at low line.

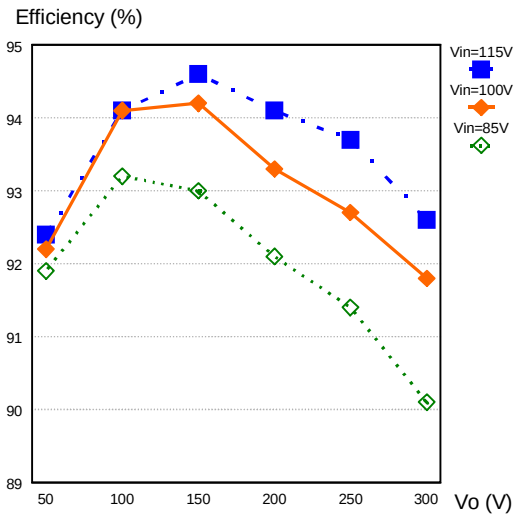



Fig. 4.12 Efficiency: typical operating condition of the motor

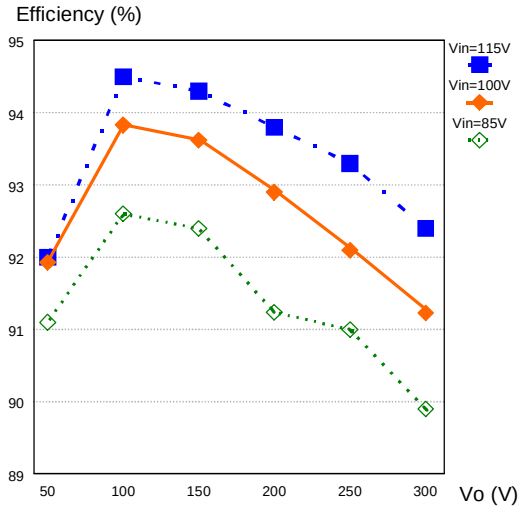



Fig. 4.13 Efficiency: maximum output power condition

### 4.2.3 Measured Power Factor

Figures 4.14 and 4.15 show the measured power factor. It is found that the power factor is higher at low line than at high line.

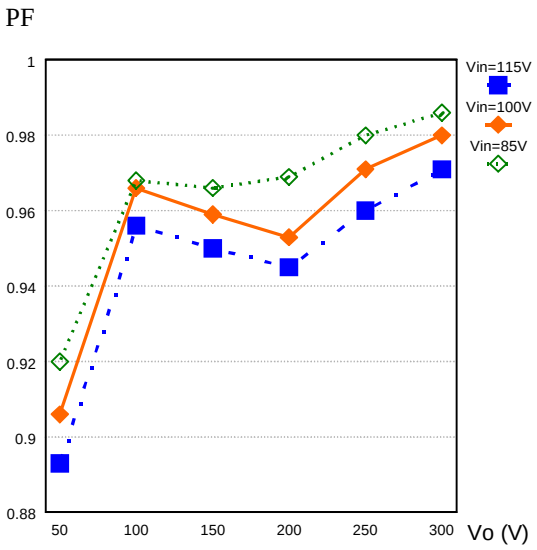



Fig. 4.14 PF: typical operating condition of the motor

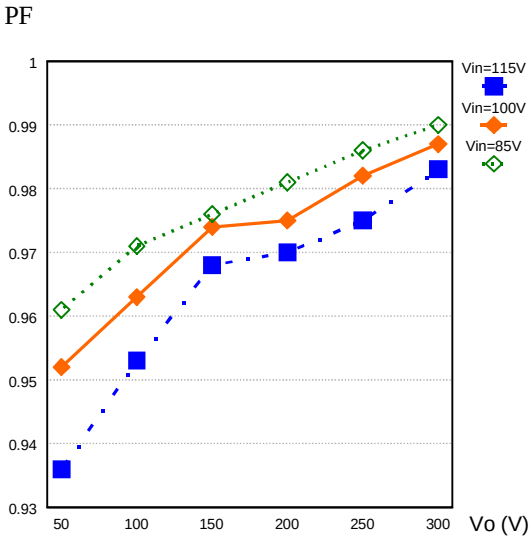



Fig. 4.15 PF: maximum output power condition

### 4.2.4 Measured Input Harmonic Currents

Figures 4.16, 4.17 and 4.18 show the measured input harmonic currents under the maximum output power condition. The VOPFC meets IEC1000-3-2 (class A) harmonic distortion specification under all of the typical motor operating condition. Under maximum output power test condition, $15^{th}$ harmonic current is a bit higher at some points, as shown in Fig. 4.17 and 4.18. These tests are done without an input LC input filter. After adding an input filter, the $15^{th}$ harmonic current can be reduced easily.

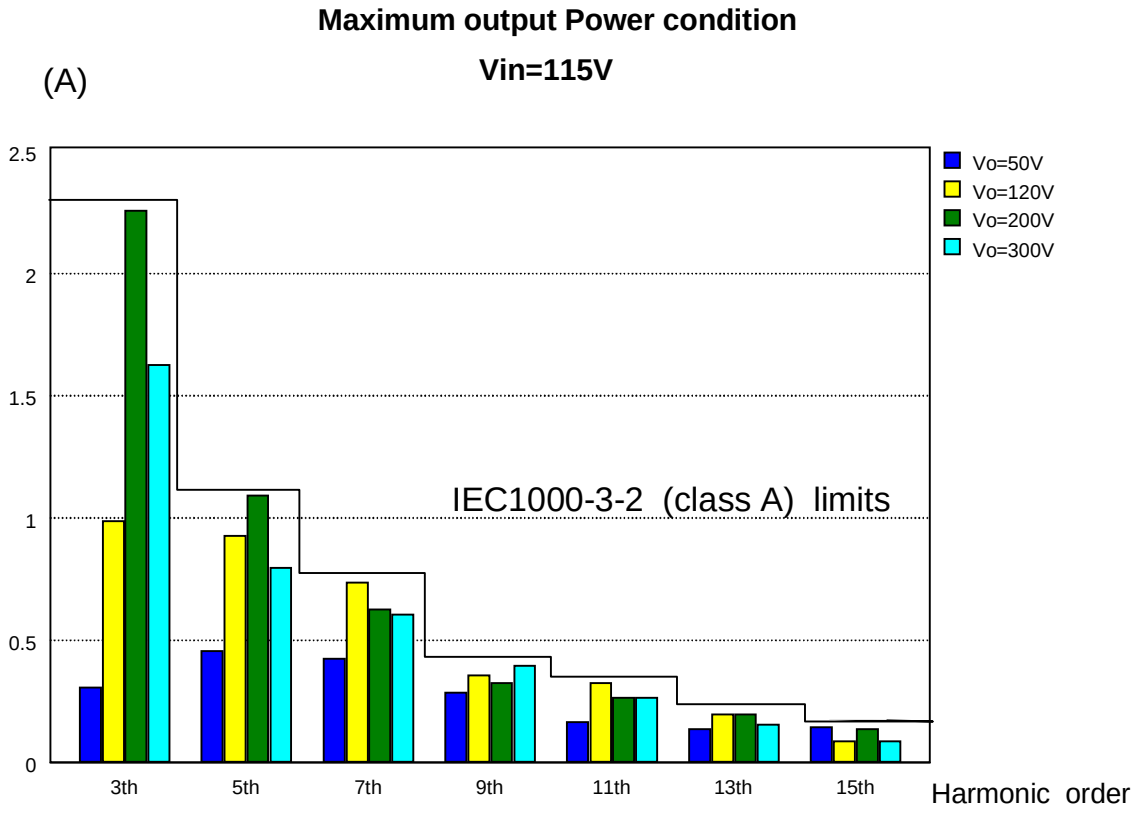



Fig. 4.16 Input harmonic currents (Vo=115 V)

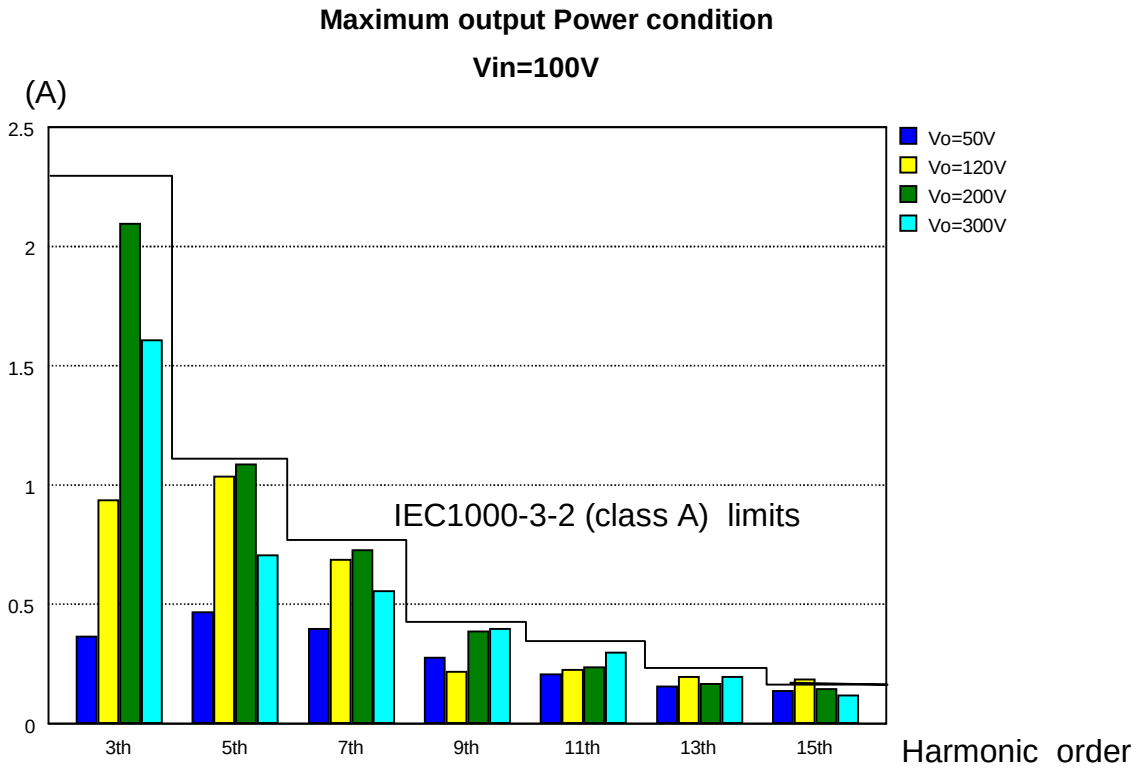



Fig. 4.17 Input harmonic currents (Vo=100 V)

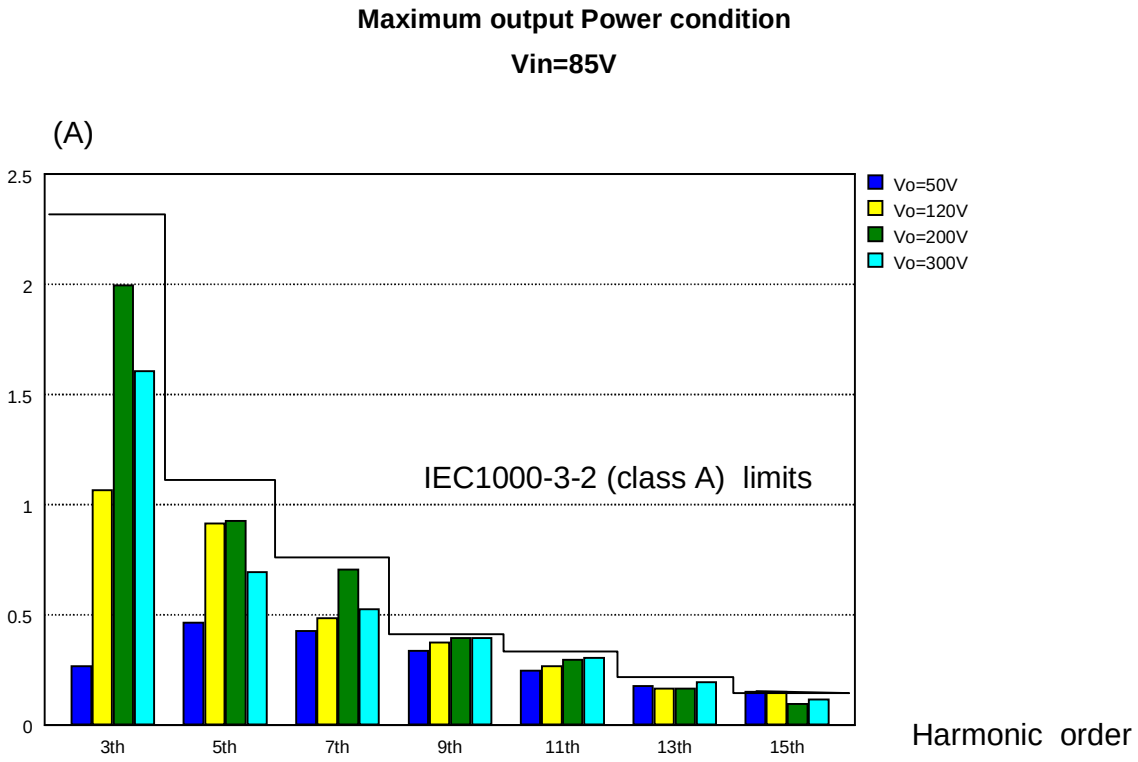



Fig. 4.18 Input harmonic currents (Vo=85 V)

# 5. Conclusions

The conventional power factor correction circuit has a fixed output voltage. However, in some applications, a PFC circuit with a wide output voltage range is needed. In this thesis, a single phase power factor correction circuit with wide output voltage range is developed. The design is based on a novel air conditioner motor system application.

A Buck+Boost converter is employed as the VOPFC power stage. This topology is very attractive for the application since boost operation mode runs at high power while buck operation mode operates at low power from its load characteristics. From the loss analysis, this topology has a high efficiency from light load to heavy load, besides, low voltage rating power devices can be used. Unlike the conventional boost PFC converter, the Buck+Boost converter is easy to start up softly and easy to have short-circuit protection. One limitation is that the input current of the converter is discontinuous in the buck mode.

The charge average current sensing scheme [21] is adopted in the Buck+Boost PFC circuit. This current sensing scheme is based on the charge information as in the charge control. Compared with the three-loop control scheme [22], which needs two current sensors and two current loops, this control scheme is simpler and has a wider bandwidth of the current loop. The limitation of this current sensing circuit is that it causes some phase delay.

The VOPFC's output voltage is not fixed, but has a very wide range. This causes problems in the current loop design. One problem is that at low output voltage the input current waveform deteriorates and the input harmonic currents are much higher than the PFC specification. This is because the current loop gain and cross over frequency are closely related to the output voltage, and they will change greatly when the output voltage changes. To solve this problem, an automatic gain control scheme is proposed and a detailed circuit is designed and added to the current loop.

To meet power factor requirements, the current loop cross over frequency should be as high as possible. However, the phase margin will be smaller. At the maximum output power test condition, it is found that the circuit easily becomes unstable. In order to

increase the phase margin while not sacrificing the cross over frequency of the current loop, a modified input current sensing scheme is proposed. The charge average current sensing circuit will be bypassed automatically by a logical circuit when the output voltage is higher than the peak line voltage. In that case, a resistor is used to sense the input current. Therefore, the phase delay caused by the charge average current sensing circuit is avoided.

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# APPENDIX A

## List of Components

Table A List of Components

| Component | Index | Description | Component | Index | Description |
|---|---|---|---|---|---|
| Resister | R1 | 47Ω | | R23 | 20K |
| | R2,R3 | 5.1K | | R24 | 20k |
| | R4,R5 | 150Ω | | R25 | 18K |
| | R6 | 22K | | R26 | 3K |
| | R7 | 2K | | R27 | 360K |
| | R8,R9 | 10K | Capacitor | C1,C2 | 220n |
| | R10 | 15K | | C3,C4 | 1.2n |
| | R11,R12 | 20K | | C5 | 68u |
| | R13 | 1K | | C6 | 220n |
| | Rf1 | 1M | | Cf1 | 100n |
| | Rf2 | 91K | | Cf2 | 6.8u |
| | Rf3 | 20K | | Cvf | 68n |
| | Rac | 680K | | Ccp | 1.5n |
| | Rvi | 510K | | Ccz | 56n |
| | Rvd | 50K | | Ct | 1.8n |
| | Rvf | 180K | | Co | 3300uF |
| | Rci | 2.2K | | Cin | 3u |
| | Rcz | 5.6K | | Cb | 2u |
| | Rmo | 2.2K | Diode | D1,D2 | IXYS DSEI30-06A, 600V/37A |
| | Rset | 36K | | D3,D4,D5,D6 | 1N5817 |
| | R14 | 20K | | D7,D8 | 1N4148 |
| | R15 | 20K | | D9 | 1N5817 |
| | R16 | 2.4K | Switch | S1 | IRGP450U,500V/33A |
| | R17 | 6.8K | | S2 | IXYS IXGH30N60,600V/30A×2 |
| | R18 | 510K | | T1,T2 | 2N2222A |
| | R19 | 10K | | T3,T4,T5 | IRFD020 50V,0.1Ω |
| | R20 | 16K | Inductor | Lf | 400uH |
| | R21 | 18Ω | Hall Sensor | (Fi) | F.W.Bell Model CL-50 |
| | R22 | 510K | | | |

# APPENDIX B

## MATHCAD Program for UC3854B Control System Design

# Design for UC3854B control system

Engineering exponential identifier:

$Meg := 1 \cdot 10^{6}$ $k := 1 \cdot 10^{3}$ $m := 1 \cdot 10^{-3}$ $\mu := 1 \cdot 10^{-6}$ $n := 1 \cdot 10^{-9}$ $pico := 1 \cdot 10^{-12}$

Define useful functions:

$round(x) := if((mod(x,1) \geq 0.5) + (x < 0) \cdot (mod(x,1) > -0.5), ceil(x), floor(x))$ sign-correct rounding

$parallel(x,y) := \frac{x \cdot y}{x + y}$

Local standard E6/E12/E24 vectors not for general use:

$E6 := (1 \ \ 1.5 \ \ 2.2 \ \ 3.3 \ \ 4.7 \ \ 6.8 \ \ 10)$

$E6c := (0 \ \ 1 \ \ 2 \ \ 3 \ \ 4 \ \ 5 \ \ 6)$

$E12 := (1 \ \ 1.2 \ \ 1.5 \ \ 1.8 \ \ 2.2 \ \ 2.7 \ \ 3.3 \ \ 3.9 \ \ 4.7 \ \ 5.6 \ \ 6.8 \ \ 8.2 \ \ 10)$

$E12c := (0 \ \ 1 \ \ 2 \ \ 3 \ \ 4 \ \ 5 \ \ 6 \ \ 7 \ \ 8 \ \ 9 \ \ 10 \ \ 11 \ \ 12)$

$E24 := (1 \ \ 1.1 \ \ 1.2 \ \ 1.3 \ \ 1.5 \ \ 1.6 \ \ 1.8 \ \ 2 \ \ 2.2 \ \ 2.4 \ \ 2.7 \ \ 3 \ \ 3.3 \ \ 3.6 \ \ 3.9 \ \ 4.3 \ \ 4.7 \ \ 5.1 \ \ 5.6 \ \ 6.2 \ \ 6.8 \ \ 7.5 \ \ 8.2 \ \ 9.1 \ \ 10)$

$E24c := (0 \ \ 1 \ \ 2 \ \ 3 \ \ 4 \ \ 5 \ \ 6 \ \ 7 \ \ 8 \ \ 9 \ \ 10 \ \ 11 \ \ 12 \ \ 13 \ \ 14 \ \ 15 \ \ 16 \ \ 17 \ \ 18 \ \ 19 \ \ 20 \ \ 21 \ \ 22 \ \ 23 \ \ 24)$

Use one of the following functions for finding a standard E6/E12/E24 resistor value:

$E6find(oddvalue) := E6findfactor(findfactor(oddvalue)) \cdot 10^{floor(log(oddvalue))}$

$E12find(oddvalue) := E12findfactor(findfactor(oddvalue)) \cdot 10^{floor(log(oddvalue))}$

$E24find(oddvalue) := E24findfactor(findfactor(oddvalue)) \cdot 10^{floor(log(oddvalue))}$

$ppd := 20$ Points per decade to be plotted

$fstart := 300 \cdot Hz$ Start frequency for impedance plot

$fstop := 30 \cdot k \cdot Hz$ Stop frequency for impedance plot

$f(n) := fstart \cdot 10^{\frac{n}{ppd}}$ Calculate n-th frequency of a exponential row

$p(n) := i \cdot 2 \cdot \pi \cdot f(n)$ Calculate n-th s

Run over all demanded frequencies:

$$fi := 0 .. ceil\left(log\left(\left\langle \frac{fstop}{fstart} \right\rangle\right)\right) \cdot ppd$$

Define functions for plots:

$gain(x) := 20 \cdot log(|x|)$ Gain in dB

$phase(x) := arg(x) \cdot \frac{180}{\pi}$ Phase in degree

## SPECIFICATIONS OF PFC CIRCUIT

vinmin := 85·V  vomin := 50·V

vinmax := 115·V  vomax := 300·V

pomax := 2·k·W

## DESIGN PARAMETERS FOR UC385

fs := 20·k  $Ts := \frac{1}{fs}$

vCt := 5.2·V

vramp := 5·V

## DESIGN PARAMETERS FOR POWER STAGE

L := 400·µ

$ilp := \frac{pomax}{vinmin} \cdot \sqrt{2}$  peak inductor current in low line  ilp = 33.276

Cch := 0.1·µ

Co := 3480µ

## MULTIPLIER SECTION

deisgn requirements : Imo = Km Iac (vvea - 1.5) / vff / vff

vinav := vinmin·0.9

vff := 1.6  ensure vff >= 1.414  vnode := 7.5

vrspk := 0.7  maximum voltage of current sensing

Rff1 := 910·k  Rff2 := 91·k  Rff3 := 20·k

Given $\frac{vinav \cdot Rff3}{Rff1 + Rff2 + Rff3} = vff$  $\frac{vinav \cdot (Rff2 + Rff3)}{Rff1 + Rff2 + Rff3} = vnode$  Rff1 + Rff2 = 1000000

$\begin{bmatrix} Rff1 \\ Rff2 \\ Rff3 \end{bmatrix} := Find(Rff1, Rff2, Rff3)$  feedforward voltage divider

Rff1 := E12find(Rff1)  Rff1 = 1·Meg

Rff2 := E12find(Rff2)  Rff2 = 82·k

Rff3 := E12find(Rff3)  Rff3 = 22·k

$Rvac := \frac{vinmax \cdot \sqrt{2}}{250 \cdot \mu}$

$Rvac = 680 \cdot k$

maximum multiplier input

$Rvac := E12find(Rvac)$

$Rb1 := 0.25 \cdot Rvac$

bias resistor

$Rb1 := E12find(Rb1)$

$Rb1 = 180 \cdot k$

$iacmin := \frac{vinmin \cdot \sqrt{2}}{Rvac}$

$iacmin = 176.777 \cdot \mu$

$Rset := \frac{3.75}{2 \cdot iacmin}$

reset resistor

$Rset := E12find(Rset)$

$Rset = 10 \cdot k$

multiplier resistor

$Rmo := \frac{vrspk \cdot 1.12}{2 \cdot iacmin}$

$Rmo := E12find(Rmo)$

$Rmo = 2.2 \cdot k$

oscillator frequency

$Ct := \frac{1.25}{(Rset \cdot fs)}$

$Ct := E12find(Ct)$

$Ct = 6.8 \cdot n$

CURRENT ERROR AMP. COMPENSATIOI

find the required gain of the error amplifier

* assume the voltage across the output of the hall effect is 5 Vpk = vhall and
* later on this voltage will be divided to the maximum sense voltage vrspk 1.5V

$Ghall := 1000$

$vhall := 7.5 \cdot V$

check the experimental setup right now

currenrt loop crossover frequency
use the charge control modulation gain and
approxomate high-frequency boost model

Ti(s) = Fm Ri He(s) Gid(s) Gic(s

$Gid(p) := \frac{vomax}{p \cdot L}$ $\omega n := \pi \cdot fs$ $qn := -\frac{2}{\pi}$

$He(p) := 1 + \frac{p}{\omega n \cdot qn} + \frac{p^2}{\omega n \cdot \omega n}$

$Cch := \frac{ilp \cdot Ts}{vhall \cdot Ghall}$ $Cch := E12find(Cch)$ $Cch = 0.22\mu$

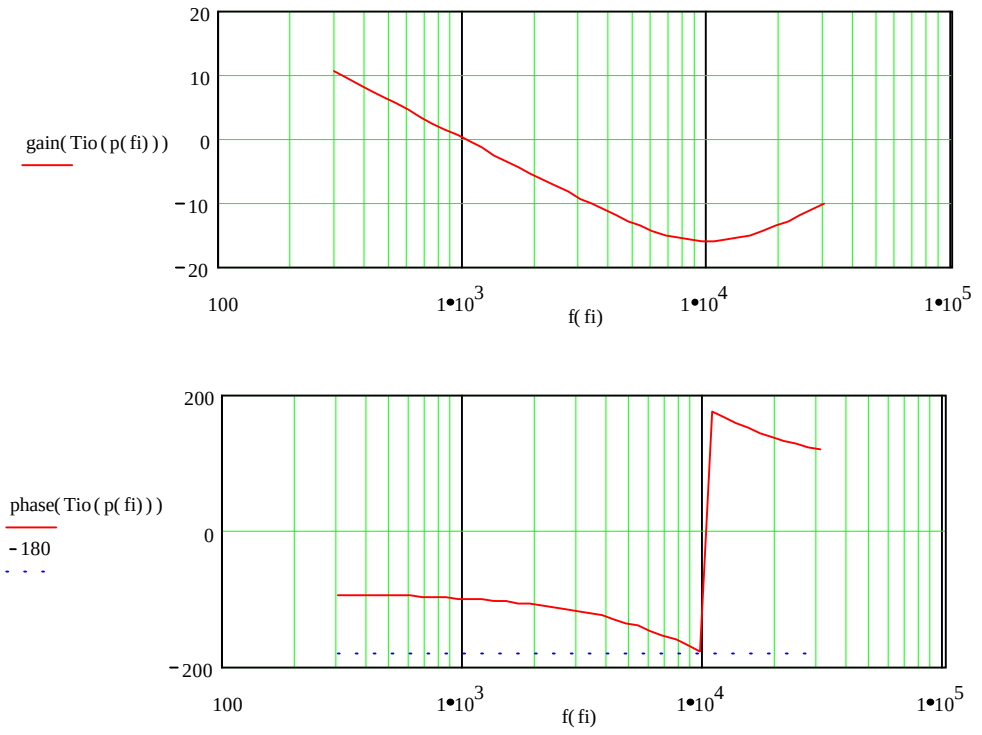
$Fm := (0.5 \cdot vramp)^{-1}$ $Fm = 0.4$

$Ghldiv := \frac{vrspk}{vhall}$ add a divider after the average charge control $Ghldiv = 0.093$

$Ri := \frac{Ts}{Cch \cdot Ghall} \cdot Ghldiv$ $Ri = 0.021$

$D := \frac{vomax - vinmin \cdot \sqrt{2}}{vomax}$ $D = 0.599$

$Tio(p) := Ri \cdot He(p) \cdot Gid(p) \cdot Fm$



OBJECTIVES FOR CURRENT CONTROL LOOP

$i := \sqrt{-1}$

Define the crossover frequency of the current loop

$fc := 2.5 \cdot k \cdot Hz$

$fz := 0.5 \cdot k$ $\omega z := 2 \cdot \pi \cdot fz$

$fp := 20 \cdot k$ $\omega p := 2 \cdot \pi \cdot fp$

$\omega i := 150$ will include the voltage divider gain

$$Gis(p) := \frac{\left(1 + \frac{p}{\omega z}\right)}{p \cdot \left(1 + \frac{p}{\omega p}\right)}$$ feedback compensator of current loop

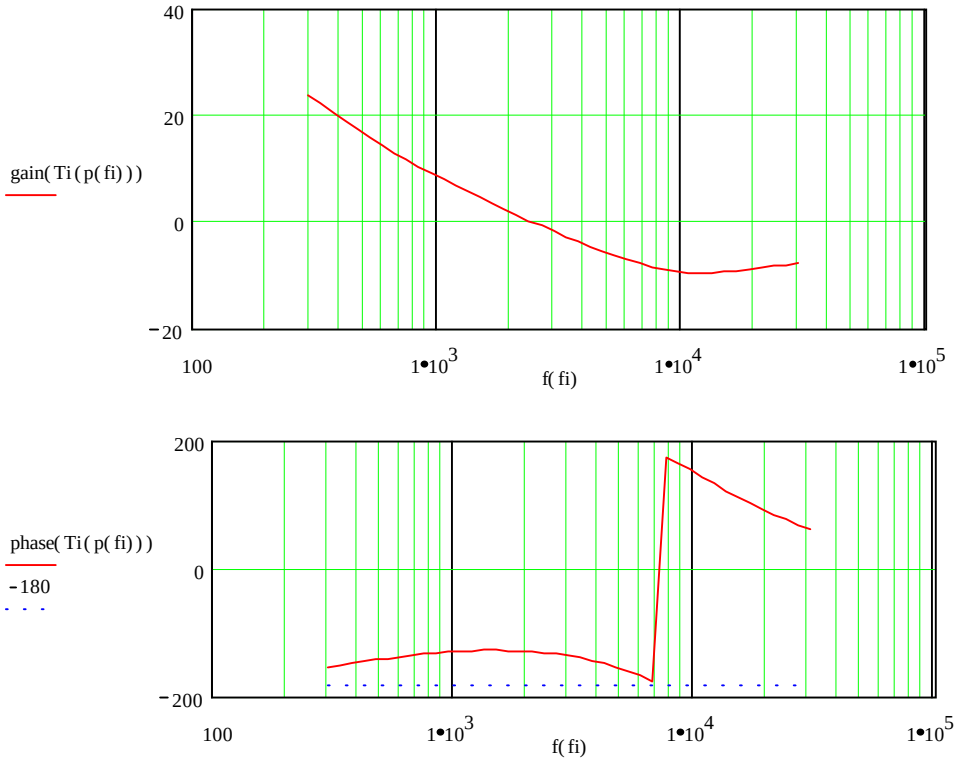
$Ti(p) := Tio(p) \cdot Gis(p)$

Given $gain(\omega i \cdot Ti(i \cdot 2 \cdot \pi \cdot fc)) = 0 \cdot dB$ $\omega i := Find(\omega i)$ $\omega i = 7.539 \cdot 10^{3}$

$$Gis(p) := \frac{\omega i \cdot \left(1 + \frac{p}{\omega z}\right)}{p \cdot \left(1 + \frac{p}{\omega p}\right)}$$

$Ti(p) := Tio(p) \cdot Gis(p)$

$phasemargin := phase(Ti(i \cdot 2 \cdot \pi \cdot fc)) + 180$ $phasemargin = 48.837$




## DESIGN THE COMPENSATOR OF THE CURRENT ERROR AMPLIFI

$Rl := Rmo$

$Rf := 1 \cdot k$ $\quad Cfp := 1 \cdot n$ $\quad ns := \frac{\omega p}{\omega z}$

Given

$$\frac{1}{Rl \cdot (1 + ns) \cdot Cfp} = \omega i$$

$$\frac{1}{Rf \cdot Cfp \cdot ns} = \omega z$$

$$\begin{bmatrix} Rf \\ Cfp \end{bmatrix} := Find(Rf, Cfp)$$

$Cfz := ns \cdot Cfp$

Theoretical value:

$Rl = 2.2 \cdot k$

$Rf = 5.412 \cdot 10^{3} \cdot \Omega$

$Cfp = 1.47 \cdot n$

$Cfz = 0.059 \cdot \mu$

$Rl := E12find(Rl)$

$Rf := E12find(Rf)$

$Cfp := E12find(Cfp)$

$Cfz := E12find(Cfz)$

Off-the-shelf value

$Rl = 2.2 \cdot k$

$Rf = 5.6 \cdot 10^{3} \cdot \Omega$

$Cfp = 1.5 \cdot n$

$Cfz = 0.056 \cdot \mu$

VERIFICATION

$$\omega i := \frac{1}{Rl \cdot (1 + ns) \cdot Cfp} \qquad \omega i = 7.391 \cdot 10^{3}$$

$$fz := \frac{1}{2 \cdot \pi \cdot Rf \cdot Cfp \cdot ns} \qquad fz = 0.474 \cdot k$$

$$fp := \frac{1}{2 \cdot \pi \cdot Rf \cdot Cfp} \qquad fp = 20 \cdot k$$

$$Gis(p) := \frac{\omega i \cdot \left(1 + \frac{p}{2 \cdot \pi \cdot fz}\right)}{p \cdot \left(1 + \frac{p}{2 \cdot \pi \cdot fp}\right)}$$

$Ti(p) := Tio(p) \cdot Gis(p)$

Given $gain(Ti(i \cdot 2 \cdot \pi \cdot fc)) = 0 \cdot dB$ $fc := Find(fc)$ $fc = 2.578 \cdot k \cdot Hz$

$phasemargin := phase(Ti(i \cdot 2 \cdot \pi \cdot fc)) + 180$ $phasemargin = 48.386$

## FEEDFORWARD VOLTAGE DIVIDER CAPACITOR

$THD := 1.5$

$Gff := \frac{THD}{66.2}$ $Gff = 0.023$

$fvp := \sqrt{Gff \cdot fr}$ $fvp = 18.063 \cdot Hz$

$Cff1 := \frac{1}{2 \cdot \pi \cdot fvp \cdot Rff2}$ $Cff1 := E12find(Cff1)$ $Cff1 = 0.1 \cdot \mu$

$Cff2 := \frac{1}{2 \cdot \pi \cdot fvp \cdot Rff3}$ $Cff2 := E12find(Cff2)$ $Cff2 = 0.39 \cdot \mu$

## VOLTAGE ERROR AMPLIFIER COMPENSATION

$fr := 120$ $ripple := 0.05$ $Vref := 7.5 \cdot V$

$vopk := \frac{pomax}{2 \cdot \pi \cdot fr \cdot Co \cdot vomax}$ $vopk = 2.541 \cdot V$

$vvao := 4$ p-p value of o/p voltage of voltage amp.

$Gva := \frac{vvao \cdot ripple}{vopk}$ $Gva = 0.079$

$Rvi := 510 \cdot k$

$Cvf := \frac{1}{2 \cdot \pi \cdot fr \cdot Rvi \cdot Gva}$ $Cvf := E12find(Cvf)$ $Cvf = 33 \cdot n$

set dc output voltage

$Rvd := \frac{Rvi \cdot Vref}{vomax - Vref}$ $Rvd := E12find(Rvd)$ $Rvd = 12 \cdot k$

$fvi := \sqrt{\frac{pomax}{vvao \cdot vomax \cdot Rvi \cdot Co \cdot Cvf \cdot (2 \cdot \pi)^2}}$ $fvi = 26.848$

$Rvf := \frac{1}{2 \cdot \pi \cdot fvi \cdot Cvf}$ $Rvf := E12find(Rvf)$ $Rvf = 180 \cdot k$

## VOLTAGE ERROR AMPLIFIER COMPENSATION

$Rvi := 510 \cdot k$

$Cvf := 0.068 \mu$

$Rvf := 180 \cdot k$

$\omega v := \frac{1}{Rvi \cdot Cvf}$ $\omega v = 28.835$

$\omega pv := \frac{1}{Rvf \cdot Cvf}$ $\omega pv = 81.699$

$$Gvc(p) := \frac{\omega v}{1 + \frac{p}{\omega pv}}$$

$Io := 6$ $Vc := 3$ $Co := 3300 \mu$ $Vo := 300$

$$Gvd(p) := \frac{Io}{Vc} \cdot \frac{1}{p \cdot Co}$$

$$Kv := \frac{3}{Vo}$$

$$Tv(p) := Kv \cdot Gvc(p) \cdot Gvd(p)$$

$fstart := 0.1 \cdot Hz$ Start frequency for impedance plot

$fstop := 100 \cdot Hz$ Stop frequency for impedance plot

Calculate n-th frequency of a exponential row

Calculate n-th s

$f(n) := fstart \cdot 10^{\frac{n}{ppd}}$

$p(n) := i \cdot 2 \cdot \pi \cdot f(n)$

Run over all demanded frequencies:

$$fi := 0 .. \text{ceil}\left(\log\left(\frac{fstop}{fstart}\right)\right) \cdot ppd$$

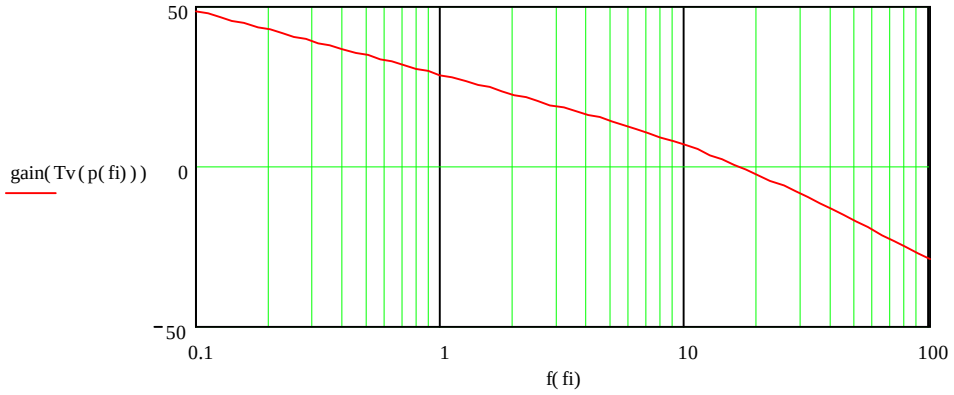
Gain in dB

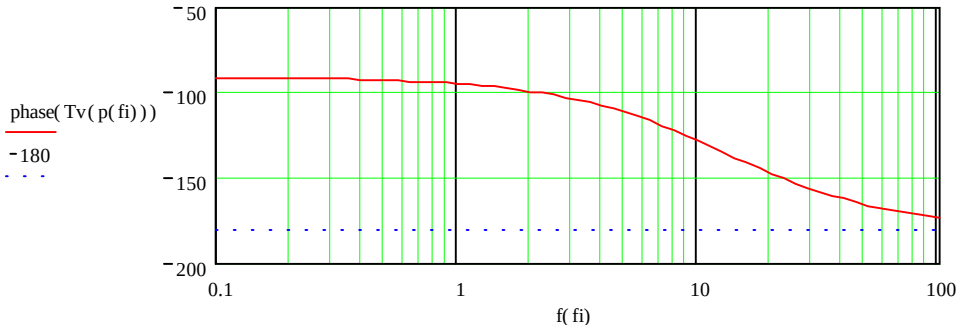
Phase in degree

Define functions for plots:

$$gain(x) := 20 \cdot \log(|x|)$$

$$phase(x) := \arg(x) \cdot \frac{180}{\pi}$$



# Vita

Yiqing Zhao was born in Hangzhou, Zhejiang Province, China on June 20, 1967. He received his B.S. and M.S. degrees from Zhejiang University, China in 1989 and 1992, respectively, both in electrical engineering. From 1992 to 1995, he worked as a lecturer at the Department of Electrical Engineering, Zhejiang University.

He joined the Virginia Power Electronics Center (VPEC), Virginia Tech in 1995 as a graduate research assistant. His main research interests include power factor correction circuits, high frequency dc-dc converters and dc-ac inverters, and soft-switching techniques.