Fabrication of Three-Dimensionally Independent Microchannels Using a Single Mask Aimed at On-Chip Microprocessor Cooling

Kevin F. Gantz

Thesis submitted to the Faculty of Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

Master of Science

In

Mechanical Engineering

Masoud Agah, Chair
Leyla Nazhandali
Scott Huxtable
Sanjay Raman

November 28, 2007
Blacksburg, Virginia

Keywords: Microfluidics, RIE lag, Nonlinear Regression, Isotropic Etching, Chip Cooling, CMOS Compatible

Fabrication of Three-Dimensionally Independent Microchannels Using a Single Mask Aimed at On-Chip Microprocessor Cooling

Kevin F. Gantz

(Abstract)

A novel fabrication process is presented which allows for three-dimensionally independent features to be etched in silicon using SF_6 gas in a deep reactive ion etcher (DRIE) after a single etch step. The mechanism allowing for different feature depths and widths to be produced over a wafer is reactive ion etch lag, where etch rate scales with the exposed feature size in the mask. A modified Langmuir model has been developed relating the geometry of the exposed areas in a specific mask pattern as well as the etch duration to the final depth and width of a channel that is produced after isotropic silicon etching. This fabrication process is tailored for microfluidic network design, but the capabilities of the process can be applied elsewhere. A characterization of an Alcatel DRIE tool is also presented in order to enhance RIE lag by varying etch process parameters, increasing the variety of channel sizes that can be fabricated. High values of flow rate, coil power, and pressure were found to produce this effect. The capability of the modeled process for creating a microchip cooling device for high-heat flux applications was also investigated. Using meander channels, heat flux in excess of $100W/cm^2$ were cooled using $750\mu L/s$ flow rate of water through the chip. This single-mask process reduces risk of damage to the chip and provides the capability to cool high-heat-flux microprocessors for the next 10 years, and for an even longer time once the geometry of the channels is optimized.

Table of Contents

List of Figures and Tables

Figures

Tables

Acknowledgements

I would first like to thank my parents and my entire family for supporting me through this process. You always let me know how proud you were of me and you gave me the motivation to keep trying my best and to give as much effort as I could. Thank you for instilling in me pride in myself and my achievements. I could never have made it this far without all of you. I would also like to thank my father, Dr. Donald T. Gantz, and my sister, Dr. Marie Gantz, as well as Dr. John Miller for their assistance in statistical data analysis and nonlinear regression.

I would also like to extend many thanks to Dr. Masoud Agah, my advisor. With his help I have improved so much academically and I know that I have truly earned my degree. Thank you for encouraging me all along the way. With your guidance I was able to attend the Transducers '07 conference in Lyón, France, a trip I will never forget, and have my work accepted for publication. Thank you for dedicating your time and resources to my achievements and I am sorry that I could not have been a part of the VT MEMS Lab for a longer time. I would also like to thank the rest of my committee, Dr. Leyla Nazhandali, Dr. Sanjay Raman, and Dr. Scott Huxtable.

Mehdi, Bassam, Syed, Amin, and Liam, you all were great graduate students to work with and I am thankful I got to spend my graduate years in your company. Thank you for your assistance, listening, and always having the time to answer my questions. The atmosphere in the lab was great and you all are the reason for it. I would like to thank Liam Renaghan especially for his assistance with my project. He took a large amount of data for me and also assisted me during my chip cooling experiments. Thank you for your great ideas and creativity, I look forward to seeing the progress you make.

I would like to thank all of the other staff at Virginia Tech that helped me through my graduate degree, especially the lab technicians, Don Leber, Dan Huff, and Steve McCartney. Don, thank you for keeping the clean room in working order and always having the time to answer the questions I had. Steve, thank you for always working with a smile and for teaching me how to use the SEM. Dan, thank you for putting time aside in your schedule to wire bond my chips, you were a great help. And Cathy Hill, thank you for all your emails and reminders of due dates and opportunities, you are a valuable asset to the mechanical engineering graduate program.

I would also like to thank all my friends who helped me reach a healthy balance between work and leisure. H.P., Travis, Chris, Steven, and so many others, I will always remember the great memories and times we shared together. Nikki, thank you for staying patient through all of the "one-more" months and keeping me motivated when my frustrations were at their highest.

Lastly, I would like to thank Virginia Tech and everyone who helped make it the perfect environment to spend six years living and learning.

Nomenclature

Mask Variables

w	Rectangular opening dimension transverse to the channel length
l	Rectangular opening dimension parallel to the channel length
s	Spacing between rectangular openings
c	Number of rectangular openings transverse to the channel length
L	Length of the channel mask pattern
W_P	Total width of the mask pattern

Modeling Variables

α, β, γ	Terms in the modified Langmuir model
F	Ratio of the open area in the pattern to the total area times c
t	Duration of the etch step

Characterization Variables

L	Under-etched length beyond the surface pattern of the channel
D	Etched depth of the channel

Heat Transfer Variables

T_{bulk}	Average temperature of the fluid at a given point along the channel
T_h	Average temperature of the heated surface
T_{in}	Bulk inlet temperature of the fluid to the chip
T_{out}	Bulk outlet temperature of the fluid from the chip
T_s	Temperature of the surface being touched by the cooling fluid
T_{max}	Maximum chip temperature
q	Heat input to the system
R_{th}	Thermal resistance of the chip
C_p	Specific heat
μ	Dynamic viscosity (fluid property)
k	Thermal conductivity (fluid property)
Pr	Prandtl number (fluid property)
Nu	Nusselt number
Re	Reynolds number
h	Convection coefficient
D_h	Hydraulic diameter
A	Cross sectional area
P	Perimeter
$x_{fd,h}$	Hydraulic development length
f	Darcy friction factor
u	Mean fluid velocity
ρ	Density
$\Delta P/\Delta x$	Pressure gradient
V	Voltage
I	Current
R	Resistance
Q	Liquid flow rate

Chapter 1

Introduction and Objectives of Modeling RIE Lag for a Single-Mask Fabrication Process

In recent years of microelectromechanical system (MEMS) design, fabrication simplicity has become of higher importance even for MEMS devices of complex functionality [1-3]. One possible way to address this issue is to use a single mask for the fabrication of three-dimensional (3-D) microdevices, where all feature dimensions are independent of those elsewhere on a single wafer. This approach is important in particular for two reasons: reduction in resources and shortened processing time. The reduction of the number of photolithographic masks reduces the fabrication cost, the number of processing steps, and the use of associated resources. In addition, shorter fabrication time allows for faster optimization through multiple design cycles and leads into rapid device implementation.

Generally, in order for structures to be created with 3-D control, multiple steps of lithography and etching are required. Complexity of this method, especially when dealing with surfaces with multiple topographical variations, illustrates the need for the development of simpler, single-mask processes [4, 5]. Currently, there are two methods that are compatible with conventional semiconductor process technologies, use common processes such as deep reactive

ion etching (DRIE), and require only a single mask. One method relies on gray-scale lithography, which uses a special photolithographic mask with several gray levels ranging from fully opaque to fully translucent. When exposed and developed, the opacity defines different surface height profiles in photoresist which are then transferred into the substrate using DRIE [6-8]. However, this technique requires delicate control of exposure, development, and etching conditions.

The second method utilizes reactive ion etch (RIE) lag, in which etching of small features lags behind that of large features , to create complex 3-D surface profiles using a single mask. A few different methods have been presented in [4, 5, 9] with similar results. These methods use a mask design with different sized openings closely spaced apart to modify the local etch rate of silicon through RIE lag effects. They then use a primary etch step through the mask, and a secondary etch step without the mask to achieve a smooth surface. The minimum feature size of the previous studies utilizing RIE lag for single-mask fabrication of out-of-plane structures has been about 50μm [4].

This thesis reports the utilization of RIE lag for the first time to create a single-mask process for the fabrication of complex 3-D microfluidic structures. Newly developed models are presented that relate the width and depth of isotropically etched microchannels to the geometry of the exposed surface and to the etch duration. These models are based on an exposed surface structure with five independent geometric variables and a single DRIE process using SF_6 plasma to isotropically etch silicon substrate. The result is a powerful simulation tool to accurately predict, design, and fabricate a network of channels and cavities etched in silicon with different depths and widths using only a single etch step. This process allows for today's microfluidic devices, composed of microfluidic junctions, cavities, and nozzles, to be fabricated in a single-mask process, and also for new devices to be implemented that take advantage of the precise control of channel dimensions. This thesis demonstrates the usefulness of the RIE-lag based technique for fabricating microfluidic networks by presenting an on-chip microprocessor cooler capable of cooling above $100W/cm^2$ power density.

The following sections detail the relevant research that has been performed in the field prior to this investigation. Next, the wafer surface pattern and the process parameters of the deep reactive ion etcher that were chosen to increase RIE lag in the formation of microfluidic channels are presented. The complex models relating the depth and width of etched channels to the geometric variables of the masking layer are then developed and are proved to be accurate. Lastly, the models are used to design and fabricate an on-chip microprocessor cooling device capable of keeping future microprocessors below their critical temperature during high power operation.

Chapter 2

Review of DRIE and Three-Dimensional Etching Literature

2.1 Introduction to DRIE Technology

The causes and results of reactive ion etch lag have been presented in many papers in recent history. As research into miniaturizing circuits and mechanical systems has progressed, the feature size of lithographic processes has gotten progressively smaller. Below a certain point, dependent on etching conditions, the etch rate will begin to diminish as feature size decreases. The reason for this relationship between feature size and etch rate is due to transport limiting factors of the active etch species [10].

The deep reactive ion etching process, which is used in this study, works to etch a substrate by a combination of both highly directional ions and reactive radicals. The ionic component works to physically etch the surface of the substrate by high energy bombardment while the radicals react with the substrate material, vaporizing and forming byproducts. These two factors work in tandem to create an "ion assisted chemical reaction" that can etch at a very high rate [11].

The structure of a DRIE machine is displayed in Figure 1 thanks to Surface Technology Systems plc. The figure shows a diagram of a Surface Technology Systems (STS) brand tool

with its major components. The etcher features a large plasma chamber where the gas that enters

through the gas inlet nozzle dissociates into plasma due to high-powered radio-frequency

excitation. The excited plasma then reaches the substrate, which is held by metal fingers to a

helium cooled substrate holder, where it removes exposed substrate material by the

aforementioned ion assisted chemical reaction. The gas then exits the chamber and passes

through an automatic pressure control (APC) valve which limits the rate of gas that can exit,

thereby controlling the chamber pressure. The substrate holder also has a power source attached

to it which helps to direct ionic species to the substrate.
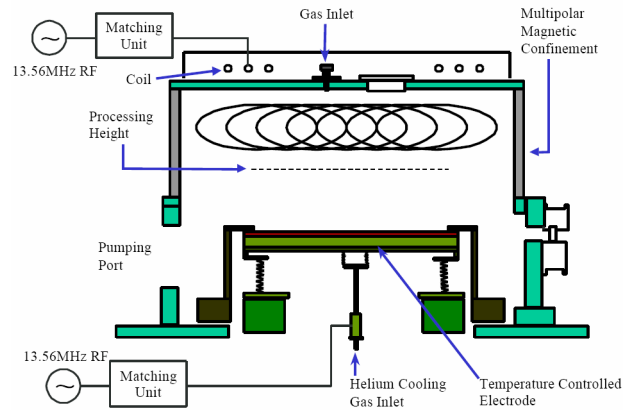
Figure 1: Schematic of an STS DRIE system. Reproduced with permission from
[12]. *Copyright 1999, Surface Technology Systems plc*.

When structures are etched using DRIE, not all of the reactive gas in the chamber goes to

etching the substrate. The probability that a reactive molecule will reach the etch front and react

relates to the geometry that the gas can flow through [11]. As feature size approaches the order

of 10μm there is less room for all the species to flow freely in and out of the trench. This

inhibition of mass flow allows less etch species to enter the feature, and the etch rate decreases as

a result. This transportation limited reduction of etch rate is deemed RIE lag [10]. The term RIE

lag is sometimes used to refer to aspect ratio dependent etching (ARDE) which is when etch rate

decreases as the depth to width aspect ratio of a trench increases [13], but this thesis will only use RIE lag to refer to the relationship between etch rate and feature size.

2.2 DRIE Characterization

As MEMS features have increasingly reached sizes on the order of tens of micrometers, significant research has been performed on methods to control the presence of RIE lag and to find out what aspects of the etch process affect the magnitude of the scaling effect [11, 14-19]. The majority of work done to control RIE lag has focused on the parameters of plasma etch processes and their relationship to the transport of reactive and ionic species to the substrate. In a typical reactive ion etcher under isotropic etch conditions, the parameters that can be changed are substrate temperature, coil power, platen power, pressure, and flow rate of reactive gasses. For anisotropic etches using the Bosch process, additional parameters such as passivation time and the overlap between passivation and etching gas flow can also be adjusted.

Ayón et al. have performed significant research in the relationship between reactive ion etch lag and feature size in both isotropic and anisotropic etching in DRIE using SF_6 as the etch gas [14, 15]. In his investigation of isotropic RIE lag, Ayón changed the SF_6 flow rate, platen power, coil power, and the APC valve position. The flow rate and the APC valve position are used to control the pressure within the chamber. Table 1 shows the values of flow rate and APC position along with the corresponding chamber pressure. They tested the effects of each parameter using a photolithographic mask composed of line arrays ranging 2 to 64µm in width progressing in powers of two. After measuring the channels, the group found that coil power and SF_6 flow rate were the most important factors affecting etch rate. Their explanation for this relationship is that coil power increases the ion flux to the substrate and high flow rate helps to remove etch products as well as replenish the chamber with fresh etch species, which is

evidenced by a low residence time of the species in the etch chamber. A smaller degree of influence was observed with coil power and chamber pressure.

Table 1: Pressure and residence time vs. flow rate and APC position. Reproduced with permission from [15]. Copyright 1999, *The Electrochemical Society*.

APC (°)	SF_6 flow rate (sccm)	Pressure (mT)	Residence time (s)
50	70	6.6	0.27
50	140	11.4	0.23
65	70	13.8	0.56
65	140	24	0.49
80	70	60.8	2.47
78	140	85	1.73

Coil power and flow rate were also found to have a high influence on RIE lag, measured by a relative difference between the trenches at 16μm and 4μm width. Coil power was cited to contribute to RIE lag effects by increasing the amount of ion shadowing for small trench widths, preventing the ionic species from reaching the bottom of the channel with as great of a frequency as wider trenches. Low pressure was also found to decrease RIE lag, resulting from the greater mean free path of reactive molecules, lowering the probability that etch species will be obstructed in their path to the substrate. The etched width to depth ratio was also investigated and it was determined that high power and low SF_6 flow rate decrease the ratio of the width to the depth, and high pressure decreases the ratio despite there being a greater amount of atomic fluorine at high pressures. A second publication by Ayón affirms these trends in the anisotropic Bosch process using the same STS etcher with some added time dependent variables using the process. These results were also confirmed in a nearly identical experiment performed by Ji et al. [19].

Rickard and McNie also investigated a DRIE system by STS in order to determine the response of RIE lag and the microloading effect to different etch parameters [18]. The macroloading effect describes how etch rate decreases over the entire wafer due to a global

depletion of etch species. This effect increases when more surface area is exposed to the etch plasma [20]. Rickard and McNie investigated these effects with different sized lines and holes with different amounts of exposed substrate surrounding the portions of the wafer to be tested. They found that to decrease the presence of RIE lag, a short etch duration, low pressure, low platen power, and a high passivation time using the Bosch process are required. Also, the etch rate over the wafer decreases linearly when more than 2% of the wafer surface is exposed to the plasma. However, the observation was made that the process parameters that decrease lag effects over the wafer also decrease the etch rate.

Richter et al. examined the influence of process parameters on etch rate for the purpose of making microfluidic nozzles/diffusers that started/ended with a very wide channel and ended/started with a thin channel [21]. Based on the relationship of etch rate to RIE lag observed by Rickard's group, this information is useful for improving depth uniformity over a multi-width feature. Richter et al. found the same trends as Ayón et al.; however, they investigated a range of parameters large enough to determine what happens at very high values of flow rate, pressure, coil power, and platen power, when limiting regimes are observed. Although flow rate increases etch rate, after a point etch rate begins to decrease because the time that the gas spends in the chamber, the residence time, becomes long enough that fresh etch species do not reach the substrate often enough. Pressure and platen power level off in their influence on etch rate, and at very high pressures using anisotropic etching, "grass" forms due to increased polymer deposition and decreased ion energy.

Zhu and Lindquist investigated a different material, tetraethyl orthosilicate, or TEOS, during isotropic etching in a plasma etcher [22]. The key measurement that was made was the channel width to depth ratio after etching. They varied the pressure, coil power, flow of helium, and the substrate holder temperature. The two main effects that were observed are that the vertical etch rate increases at low pressure and the lateral-to-vertical etch rate ratio decreases with decreasing temperature. Zhu and Lindquist also observed strong interaction effects between

pressure and temperature. One method outside of process parameters to decrease the lateral to vertical feature ratio is to bake the TEOS film at 110°C for 30 minutes before etching.

A similar finding to the Zhu and Lindquist study was observed from Tachi et al. using a microwave plasma etcher and a reactive ion etcher. They etched silicon at various substrate holder temperatures in order to examine the effects influencing the anisotropy of the etch profile [23]. They found that no sidewall reaction occurs below -110°C and a perfectly anisotropic profile results as seen in Figure 2. The sidewall etching is inhibited because of the reduced reaction energy at lower temperatures for the reflected radicals, but the ion assisted chemical reaction still occurs on the bottom of the trenches. Tachi was able to obtain a 1µm/min etch rate in a microwave plasma etcher without any sidewall etching.
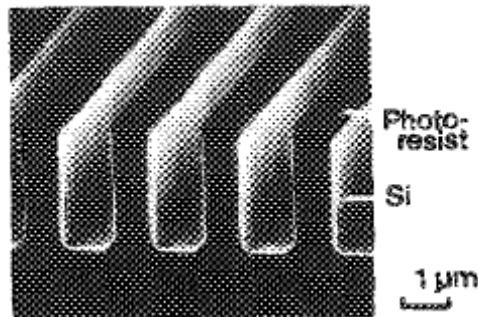
Figure 2: Anisotropic channels etched in silicon using SF_6. Etched with SF_6 gas at -120°C in a microwave plasma etcher. Reproduced with permission from [23]. Copyright 1988, *The American Institute of Physics*.

An electron cyclotron resonance, ECR, system was used in Doh et al.'s investigation of the effect of pressure, bias voltage, bias frequency, and microwave power on RIE lag. Doh's group experimentally examined these parameters on open holes with diameters ranging from 0.3 to 1.2µm, and to gain some insight into the effect of frequency on ion distribution over the wafer a Monte Carlo particle-in-cell method was used [16]. They determined that RIE lag decreases with increasing bias frequency due to a lower power bimodal distribution of ion energy existing at low frequencies that shifts toward the high energy component with increasing frequency. Lag

9

was also found to decrease with decreasing pressure, resulting in a higher ion current density, and a higher bias voltage, with lag being completely removed at -300V.

ARDE, a similar effect mentioned earlier, was examined by Lill et al. in order to determine its relationship to DRIE process parameters [11]. This effect is exhibited by decreasing etch rate as the trench becomes deeper, and was measured by Lill et al. *in situ* using interferometry and dividing the etch rate at a given time by the initial etch rate. The results are strikingly different from investigations of RIE lag. ARDE is found to be reduced at pressures around 20mTorr and temperatures at 20°C but there is no effect from coil power or gas flow rate. This is a definite contrast from the relationship of RIE lag to the process parameters as coil power and flow rate had the highest influence.

Another factor that influences etch uniformity is the microloading effect. The microloading effect is similar to the macroloading effect, except the former occurs in a local area of the wafer rather than over the whole substrate [24]. Local variations in the exposed substrate density affect the concentration of reactive molecules and ions and, thus, the local etch rate. Microloading was found by Hedlund et al. to increase at pressures above 5mTorr, with diffusion cited as being able to mask reactant concentration differences at low pressures [24]. The effect was also found to be more pronounced at low flow rates, as there is less reactant species available. These trends are also the opposite of RIE lag trends.

Similar trends of process parameter variation on RIE lag have been observed by several groups using various types of etchers and a wide range of parameters. A main summary of the observed trends are that RIE lag effects decrease at low coil power, flow rate, and pressure, all of which decrease the etch rate of the substrate. The effect of substrate holder temperature has been found to decrease the lateral to vertical etch rate ratio during isotropic etch scenarios, but the effect of temperature on RIE lag has not been investigated. The major trends for RIE lag do not share similarity to other loading effects, such as microloading and ARDE, and the resulting etched features may be affected by all of the loading scenarios at once.

10

These trends are important to determine for this investigation because three-dimensionally independent features are to be produced by utilizing the RIE lag effect. As such, lag must be increased to as high a degree as possible so that greater spans of channel dimensions can be created after a single etch duration. A deep reactive ion etcher is used in this study, similar to the STS tools used in some of the RIE lag investigations, but because of key differences in the STS systems to the system used in this study our tool will have to be characterized as well. The trends are expected to remain the same, but the degree to which parameters must be tuned to be "high" or "low" will be quite different. Also, an additional parameter, substrate holder temperature, will be investigated in relation to RIE lag.

2.3 Three-Dimensional Fabrication Using RIE Lag

The idea of three-dimensionally independent microstructures fabricated using RIE lag is not unique to this thesis, but the method and depth of investigation into the relationship of the mask geometry and the resulting feature dimensions is. Three-dimensional fabrication using a single mask and RIE lag was first demonstrated by Chou and Najafi in 2002 [9]. First, the degree of RIE lag achievable for different opening sizes from 2 to 50μm was calibrated using a test array of trenches. Their idea was then to design a mask that will produce a customizable three-dimensional surface profile with feature depths from 45 to 65μm depending on the local opening size in the mask. First, an anisotropic etch was performed using DRIE to form a rough surface profile. The remaining pillars between openings were then removed by either wet or dry isotropic etching, followed by thermal oxidation and oxide removal to further smooth out the features. The etch technique was demonstrated by the design and fabrication of a high frequency electrostatic actuator for use in micromachined acoustic ejectors.

Following Chou and Najafi's work, Bourouina et al. created a similar process using two isotropic etch steps and one mask which they called the Microloading Effect for Micromachining

11

3-D Structures of Nearly All Shapes, or the MEMSNAS process [4, 25]. The mask structure used in the MEMSNAS process is composed of an array of circular openings at a constant pitch but each opening has a different diameter depending on the desired depth under the feature. In order to determine the corresponding depth to opening size relationship, an analysis was performed and it was determined that the diameter related to the depth beneath the feature by

$$Z = aLn(b\Phi + 1) \qquad\qquad (1)$$

where Z is the depth underneath the opening and Φ is the diameter of the opening. A microlens in silicon, shown in Figure 3, was fabricated to demonstrate the accuracy of the model in predicting the depth and to illustrate the usefulness of the technique. The minimum feature size achievable using this method is 50μm and the smoothness of the features was found to depend strongly on the pitch of the mask openings.
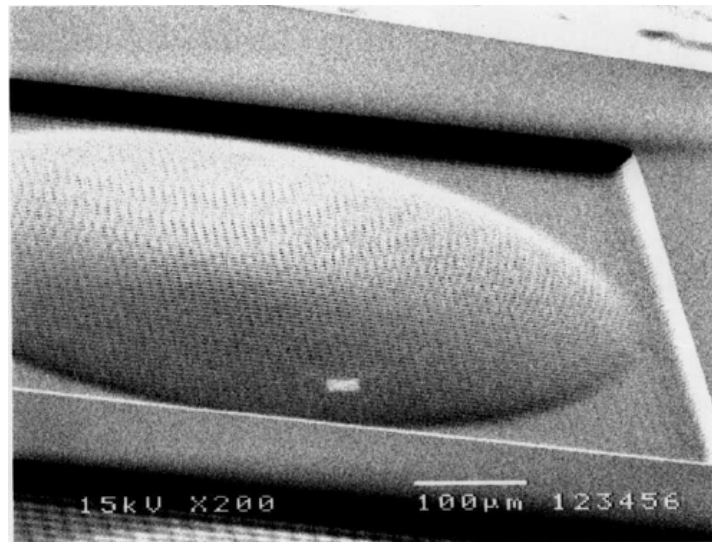

Figure 3: Microlens fabricated using the MEMSNAS process. Reproduced with permission from [4]. Copyright 2004, *IEEE/ASME*.

Wang et al. showed a simple method of multilevel etching using a single isotropic wet etch step in silicon [26]. Just as in dry etching, wet etching reaches a diffusion limitation when small features are etched and lag results. The features that were etched consisted of 100μm and 8μm trenches that were 1500μm long. The resulting structure was a bi-level planar structure with the shallower plane etched to 80μm and the deeper section to 120μm. A useful device was not fabricated with the method and a predictive model was not created for the process.

The three aforementioned RIE-lag based three-dimensional fabrication methods have relatively large feature sizes due to the necessary smoothing of the profile. Rao et al. avoided this limitation by using an anisotropic etch followed by thermal oxidation and oxide removal to smooth out the structure [5]. During thermal oxide, 46% of the oxide thickness takes the place of the original silicon, allowing the pillars to be removed after they are fully oxidized [27]. The rectangular openings ranged from 1.5μm to 4.5μm and there was a constant spacing between openings. The resolution of this method was much better than the MEMSNAS process, but the tradeoff is that the roughness of the profile is significant. However, the rough structure boundaries can be used as self patterning electrode boundaries during metallization. The usefulness of this technique was demonstrated in the fabrication of a sloping electrode for a micromirror device and is shown in Figure 4. The difference between the feature size between the methods shown in Figures 3 and 4 are obvious.

All of the aforementioned methods of three-dimensionally independent fabrication are compatible with integrated circuit (IC) fabrication processes and are all achieved using a single mask. The results of these papers show the benefit of incorporating microstructures with electronic components while saving money by simple fabrication techniques. However, most of these techniques do not have predictive models of the final geometry and the one that does, the MEMSNAS process, is limited in its dependence on a single geometric variable. The process demonstrated here overcomes these limitations by presenting a model combining 4 geometric

13

variables in addition to time and their relationship to the resulting structure depth and width after isotropic etching of silicon.
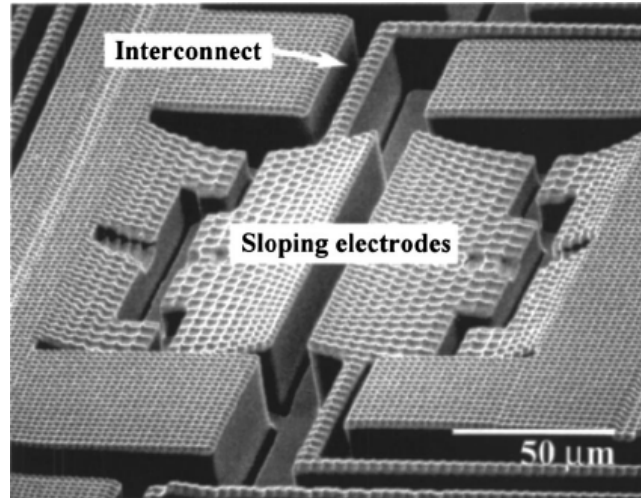

Figure 4: Sloping electrode fabricated by Rao et al.   It is part of a micromirror device fabricated using anisotropic DRIE and sacrificial oxidation. Reproduced with permission from [5]. Copyright 2004, *The American Institute of Physics*.

Chapter 3

DRIE Characterization and Modeling

3.1 Experimental Procedure

Developing a comprehensive model describing the progression of etched microfluidic channels fabricated using RIE-lag involved three experimental stages. The first stage required an in-depth analysis of etched channel dimensions in relation to the geometry of the mask pattern. After taking data, a model was made that related the geometric variables of the surface pattern to the depth and width of the resulting microchannels. The developed model then had to be verified on a separate etcher to ensure that the model captured the qualities of the process rather than just the qualities of the individual etcher. Before this could be done, the second etcher had to be characterized so that RIE lag could be made as high as possible. After the ideal parameters were found that increased RIE lag, wafers had to be etched on the second etcher so that the relationship of channel dimensions to surface pattern dimensions could be found and compared to the results from the first DRIE tool. Once the consistency of the model was verified, an additional variable, etch duration, was incorporated into the previously developed equations, resulting in a new comprehensive etch model. The following sections provide the detailed experimental procedure

that was followed to obtain a comprehensive model for three-dimensionally independent fabrication.

3.1.1 Model Formulation Using an STS DRIE System

In order to relate channel dimensions to the exposed surface geometry dimensions, a consistent surface pattern must be chosen with specific geometric variables. The photolithographic pattern used in this study is composed of five independent geometric dimensions as illustrated in Figure 5. The pattern consists of a grid of exposed rectangular areas with width and length dimensions w and l, respectively, spaced equally apart a distance, s, in the two grid dimensions. The pattern continues for a specific length, L, in one direction, and for a variable number of repetitions in the other direction. This latter value is referred to as the number of columns in the pattern, or c. All of the pattern variables will affect the surface profile of the channel that is created by changing the local density of exposed substrate over a channel. The main mechanism affecting the development of the channels is RIE lag, but microloading also influences the results. The microloading effect is a decrease in etch rate as the local density of the exposed substrate increases due to local etch species depletion [24]. Once a channel is formed, the microloading effect will work counter to the effects of RIE lag.
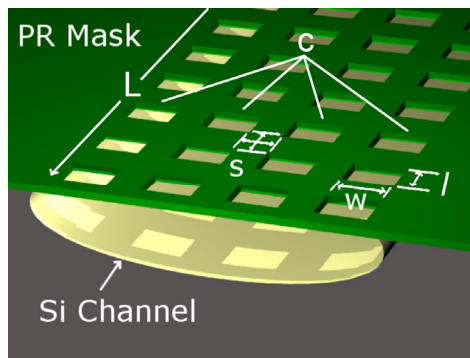

Figure 5: Schematic of the surface pattern with geometric variables. The five independent geometric variables are labeled.

16

The five variables, *s*, *w*, *l*, *c*, and *L* are the quantitative geometric terms that can be related to the resulting etched channel dimensions. A wafer mask composed of three repetitions of a factorial design of the five geometric parameters was designed to make channels out of every combination of *s*, *w*, *l*, and *c*, and most combinations of *L*. The five geometric variables took values detailed by Table 2. These sets of channels were organized into a rectangular section grouped by individual sets of *s*, *w*, and *l* with each channel separated by at least 40 μm laterally. The areas of unique *s-w-l* combinations were then set in an array over the surface of the wafer.

Table 2: Surface pattern variable values.

	s	*w*	*l*	*c*	*L*
Values	2μm	2μm	2μm	1	0.5mm
	3μm	4μm	3μm	3	1mm
	4μm	6μm	4μm	6	2mm
		10μm		50μm/(s+w)	4mm
				100μm/(s+w)	
				200μm/(s+w)	
				400μm/(s+w)	

Each wafer was prepared for etching by growing 3000Å dry-wet-dry thermal oxide to increase mask selectivity followed by spinning 2 μm-thick S1827 photoresist. After soft baking, the mask was transferred to the photoresist and then developed, followed by a hard baking step and then plasma etching of the oxide layer. Wafers were then individually etched in a Surface Technology Systems (STS) DRIE etcher with etching conditions of Table 3 chosen for the purpose of increasing RIE lag so that greater etch rate differences are present over the wafer. Each wafer was etched for 5, 15, or 30 minutes and maximum channel depth and width measurements were collected from each channel on the wafer. Regression was then performed to match the measured channel dimensions to the surface parameters. Once a suitable model was found, the process had to be repeated on an Alcatel AMS-100 etcher to verify the universality of the model's structure.

Table 3: High RIE lag parameters for the STS DRIE tool.

Parameter	STS Setting
Pressure (mbar)	0.13
Platen Power (W)	100
Coil Power (W)	800
Flow Rate SF6 (sccm)	260
Temperature (°C)	5

3.1.2 Characterization of the Alcatel AMS-100 DRIE Tool

Before the same experiment could be carried out on the Alcatel system, the tool had to be characterized. In an effort to increase the magnitude of RIE lag that is present so that a wide variety of microfluidic trenches can be fabricated, previous investigations into the relationship of RIE lag to DRIE process parameters were expanded upon. Our investigations add to previous DRIE characterizations by investigating the effect of coil power, pressure, and SF_6 flow rate, in addition to temperature, on the magnitude of RIE lag and the ratio of the lateral to vertical etch rates. Platen power was not included in this investigation because previous studies confirmed that it only played a major role in selectivity between silicon and photoresist etching [15, 19]. We also performed our investigation using the same mask as our investigation into the relationship between mask and channel geometry, which is designed to induce large RIE lag effects. In addition, the characterization reported herein took place on an Alcatel AMS-100 etcher. This etcher has four main design differences that enable it to perform differently than the STS etchers used in the previous studies. The first difference is that the Alcatel etcher has a source chamber that is less than half the size of that on the STS etcher. This quality, in addition to having a more powerful source, increases the probability of gas dissociation, which in turn increases the amount of etch species that reach the wafer. This quality is especially important at high gas flow rates. The remaining two differences affect the etch uniformity over the wafer. The plasma source is placed farther away from the target wafer in the AMS-100 to allow the gas to diffuse to a greater degree over the wafer. Also, the structure of the diffusion chamber has

been designed to allow uniform gas flow at high pressures, thereby increasing etch uniformity. This information has been provided by M. Puech of Alcatel Micro Machining Systems.

For each parameter combination, to be detailed later, RIE lag and the ratio of the lateral to in-plane etch rate was measured. To measure RIE lag, the difference in depth achieved with zero RIE lag effects, $c \rightarrow \infty$ and the depth with maximum RIE lag, $c = 1$, was measured. A graphic of the measurement is shown in Figure 6. The difference between the two measured values represents the maximum possible depth difference due to RIE lag effects. The second measured value, the lateral to in-plane etch rate ratio, L/D, is defined as the etched distance beyond the boundary of the surface pattern divided by the maximum depth in the isotropic profile. This concept is illustrated in the SEM image in Figure 7. This value was taken for the channel with the largest value of c of the set, where lag effects diminish.
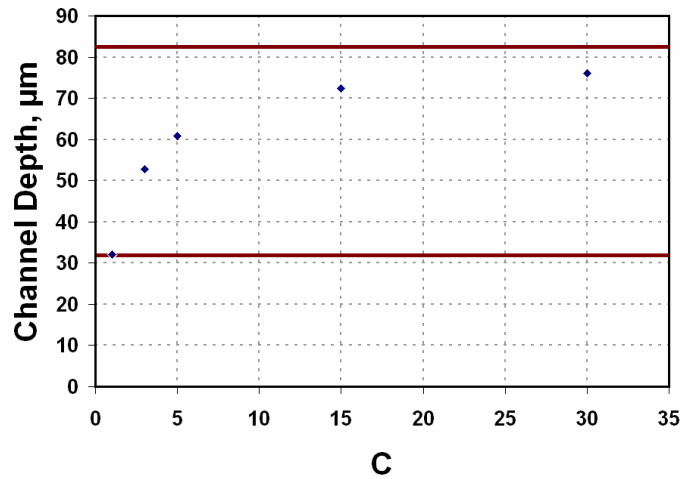

Figure 6: Channel depth vs. c. The depth at $c \rightarrow \infty$ and $c = 1$ are indicated by lines. The difference in these two values is a measure of RIE lag.
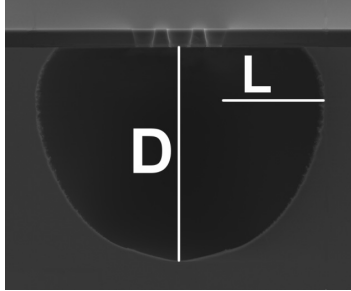
19

Figure 7: SEM image of L and D. A channel with $c = 3$ is used for visualization purposes.

Before a factorial investigation was carried out with the four etch parameters, each parameter was individually modified to determine the sensitivity of the output values in relation to the input parameters. These preliminary tests also allowed a "high" and a "low" value for each parameter to be determined for the full factorial experiment. 20 wafers etched for 10 minutes were used in the preliminary investigation. Etching for 10 minutes allows sufficient time for a continuous channel to form. At lower etch times, a complete channel does not have time to form, as illustrated in Figure 8. Each parameter was modified through 5 separate values in a random order, while all other parameters were held at their middle (3rd) value. Table 4 contains the settings of the values for each parameter. After each wafer was processed, all channels with different c values were measured for a single s-w-l pattern exhibiting high RIE lag identified by the preliminary model developed from the STS etcher. Minitab main effects and interaction plots created from the data were then used as the basis for analyzing the results.
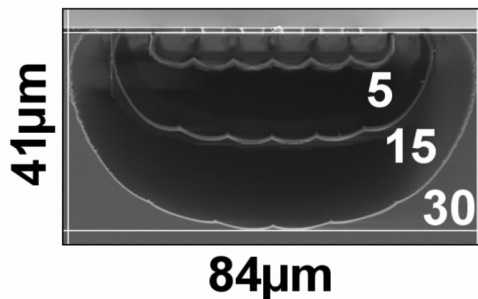

Figure 8: Development of a channel from 5 to 30 minutes. At 5 minutes, not enough time has passed to create a relatively smooth, continuous channel.

20

Table 4: Etch parameters in the Alcatel DRIE tool characterization study. The values in bold were chosen as "high" and "low" values for the full factorial experiment.

	1	2	3	4	5
Temperature (°C)	**-10**	0	10	**20**	30
Pressure (mbar)	**.02**	.05	.08	**.11**	.14
Coil Power (W)	**1300**	1600	1900	**2200**	2500
Flow Rate (sccm)	**100**	200	300	**400**	500

3.1.3 Development of a Comprehensive Model

In order to verify the model developed on the STS DRIE system, the same procedure had to be carried out on the Alcatel AMS-100 tool. The etch conditions determined to increase RIE lag in the AMS-100 from the characterization process are given in Table 5. The same fabrication process was followed as in the procedure for the STS etcher, except the wafers in the Alcatel machine were etched for 10, 15, 20, or 25 minutes. The data from each wafer was fit to the previous model and the models developed at each one of these different etch durations, t, were then used to create a single universal model applicable for any etch time.

Table 5: High RIE lag parameters for the Alcatel DRIE tool.

Parameter	Alcatel Settings
Pressure (mbar)	0.11
Platen Power (W)	50
Coil Power (W)	2200
Flow Rate SF6 (sccm)	400
Temperature (°C)	20

3.2 Results and Analysis

This section presents the results of the investigation into the relationship of geometric mask parameters to the depth and width of channels that result after isotropic silicon etching. First, the initial model developed on an STS deep reactive ion etcher is presented, followed by the

results of the characterization of the Alcatel etcher. Finally, the comprehensive model that applies to any etch duration is presented based on data from wafers etched in the Alcatel system.

3.2.1 Initial Etch Model

3.2.1.1 Etch Quality

After a wafer was etched for etch model development, one of the three repetitions of the factorial design was chosen at random to be observed. A dicing saw was used to cut the wafer perpendicular to the channel length so that a perfect cross section of each channel was exposed. A scanning electron microscope, SEM, was then aligned to the view the cross section of the channels perpendicular to the channel length to measure the maximum depth and width of each channel.

A quick examination of the cross sectional profiles made several differences evident between separate channels. Some of the profiles were more rectangular shaped and others were almost perfectly circular (Figures 9a and 9b). Also, some of the channels exhibited scalloped edges and others had smooth profiles (Figures 9c and 9d). These differences are evident between different combinations of *s*, *w*, and *l* as well as for different values of *c* within the same *s-w-l* combination. The only pattern parameter that did not affect the etch profiles was the length of the channel pattern, *L*. For this reason, it can be noted that the RIE lag effects are constant in the pattern length direction at channel lengths greater than 500 μm, the smallest value of *L* for the examined etch times.
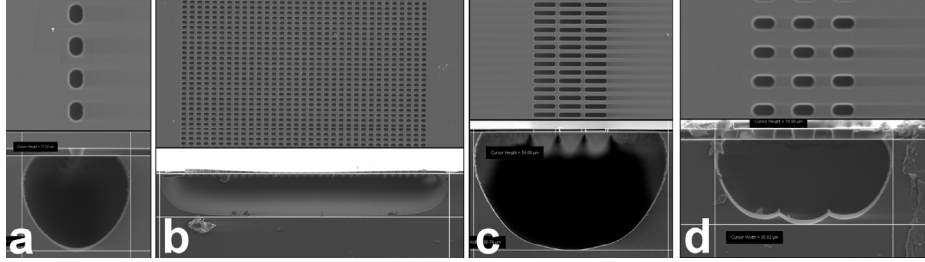
Figure 9: Shape and surface quality variation of channel cross sections. (a) a circular channel formed by $<s, w, l, c, t> = <3\mu m, 2\mu m, 3\mu m, 1, 30min>$, (b) a rectangular channel formed by $<s, w, l, c, t> = <2\mu m, 4\mu m, 2\mu m, 33, 15min>$, (c) a smooth channel formed by $<s, w, l, c, t> = <2\mu m, 10\mu m, 2\mu m, 3, 30min>$, and (d) a scalloped profile formed by $<s, w, l, c, t> = <4\mu m, 4\mu m, 2\mu m, 3, 15min>$.

When the width and depth of the channels are plotted versus each other as in Figure 10, only a specific portion of the plot is covered. In the instances where width is at its smallest values, it is possible to have a nearly circular 1:1 aspect ratio channel. As the channel width increases, the maximum channel aspect ratio decreases until the maximum depth becomes nearly constant for any large width. The lowest instances of channel aspect ratio occur for $s > w$, resulting in a nearly rectangular profile. It is in these cases as well that the most scalloping occurs over the profile. Figures 9c and 9d display a smooth and a scalloped channel profile, respectively, along with an SEM image of the surface pattern that produced it. The density of exposed surface area is notably lower for the pattern that produced the scalloped profile. The scalloping occurs from the slow merging of spherical etch pockets that form under each exposed area on the mask.
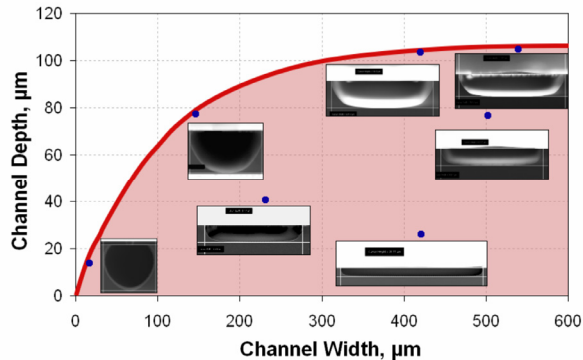

Figure 10: Achievable channel dimensions using the STS DRIE tool. The range is for a maximum 30 minute etch duration. SEM photos show typical results for each section on the plot.

23

As etch duration increases, the channels increase in depth and width and scalloping effects are reduced as summarized in Figure 11 and Figure 12. Figure 11 plots the channel progression over time for a single *s-w-l* combination and Figure 12 displays the SEM pictures of typical channels as etch duration increases. From the initial STS etcher investigation, only the channels fabricated from etch times of 15 and 30 minutes were adequate for modeling since they had fairly smooth profiles. For the wafer etched for 5 minutes, there is not enough time to develop a smooth, continuous channel.
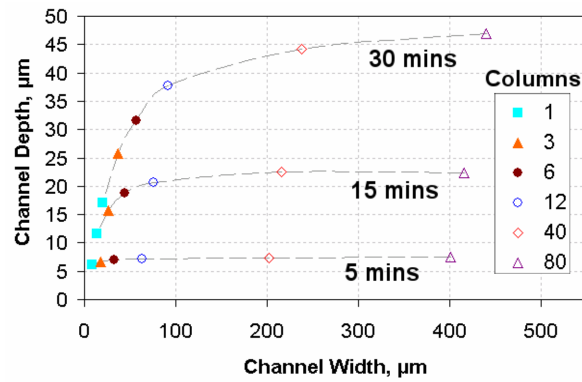
Figure 11: Plot of etch progress from 5 to 30 minutes. $l = 3\mu m$; $w = 2\mu m$; $s = 3\mu m$. A longer width is necessary in order to approach the maximum depth as time increases.
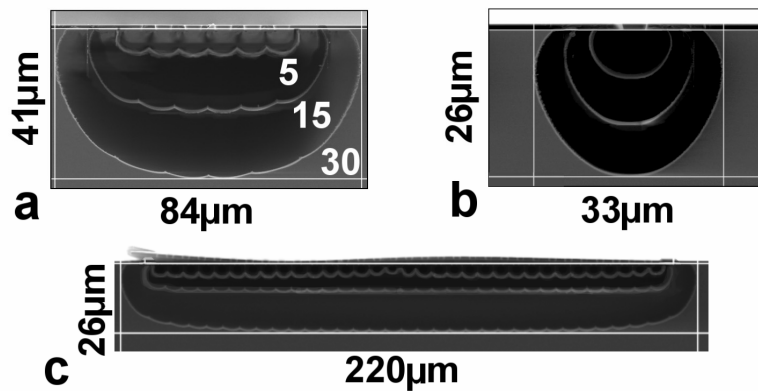
Figure 12: Cross-section geometry progress from 5 to 30 minutes for three channels. Etch progress is accompanied by a decrease in scalloping over bottom of the channel profile.(a) $s = 4\mu m$, $w = 4\mu m$, $l = 3\mu m$, $c = 6$; (b) $s = 2\mu m$, $w = 6\mu m$, $l = 2\mu m$, $c = 1$; (c) $s = 4\mu m$, $w = 2\mu m$, $l = 2\mu m$, $c = 33$.

3.2.1.2 Geometry-Based Model

In order to derive a model, a relationship needs to be identified between the quantitative pattern parameters and the depth and width of the etch profile. Increasing the span of the channels, quantized by the number of columns in the pattern, c, increased the channel depth. The relationship between the loading change produced by c and etch rate arises because of isotropic RIE lag. When the span of the pattern was small, less surface area is exposed to the etch species than the same channel pattern with a larger value of c. As c increases, the channel depth increases asymptotically to a maximum achievable depth. These results agree with the aforementioned observation that channel dimensions did not change with pattern lengths greater than 500 μm. The largest pattern span laterally was 400 μm, at which point the microloading and RIE lag effects had nearly reached a constant value. These two findings verify that for the wide variety of patterns studied in this work, effects influencing etch rate become constant in a single direction when the pattern spans at least 500 μm in that same direction.

The width of the channels also varies with the lateral span of the pattern on the surface of the wafer. As the span of the pattern increases, the width of the channel increases to approximately the same degree. This is expected, as a wider portion of the surface is exposed to the etch species. The width of the channel and the width of the pattern are not equal, however, because silicon is etched isotropically. Thus, there is some expansion of the etch boundary beyond the edges of the pattern.

When compared to the total width of the pattern, the channel width displays a relatively linear trend. Deviation from linearity is present at small pattern widths, where the channel width is slightly less than the rest of the trend as seen in Figure 13a. The deviation from linearity at small pattern widths can by explained by RIE lag effects. The isotropic nature of these effects during etch progression is verified by noting that the distance that silicon is etched underneath the

25

pattern in the lateral direction is comparable to the depth etched, illustrated in Figure 14. Our thorough data analysis showed that this relationship can be simply described by

$$Width = Depth + W_P \qquad (2)$$

where W_P is the total width of the pattern described numerically by

$$W_P = c(s + w) - s \qquad (3)$$

with variables c, s, and w defined in Figure 5. The validity of this trend is evident from the direct correlation seen in Figure 13b, a plot of channel width versus the width of the pattern plus the channel depth.

The trend of depth approaching an asymptotic value as c increases is observed over all combinations of s, w, and l. However, there are certain properties of the depth trend that differs between unique s-w-l combinations. These are the value of the maximum depth achievable without RIE lag effects, how quickly the channel depth converges to the maximum depth with increasing span, and the difference between the minimum depth and the maximum depth for a set of pattern parameters.
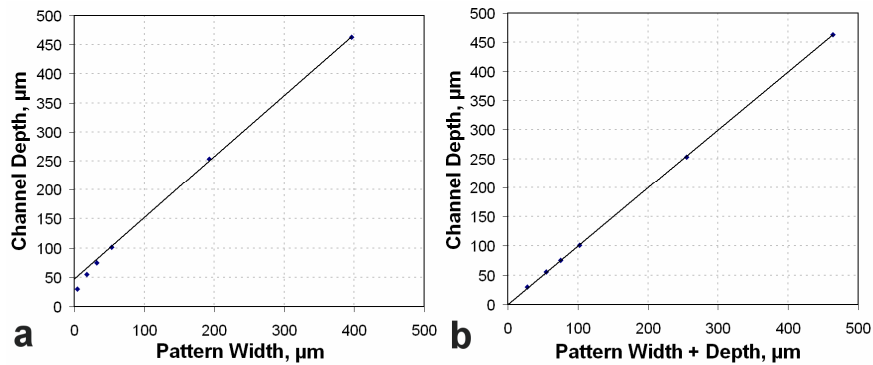

Figure 13: (a) Channel depth vs. pattern width. A linear trend develops after a pattern width ≈ 50μm. (b): Channel depth vs. pattern width + channel depth. A perfectly linear relationship results, proving the isotropic nature of RIE lag effects. The pattern used is $s = 2$μm, $w = 4$μm, $l = 4$μm, time = 30min.

26
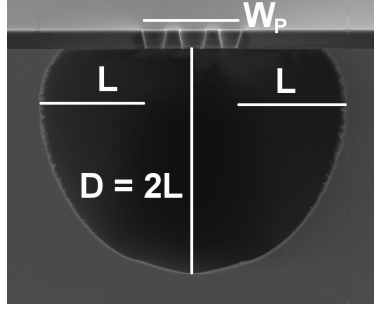
Figure 14: SEM of L = *0.5*D. $s = 2\mu m$, $w = 2\mu m$, $l = 2\mu m$, $c = 3$, time = 30min.

Using the nonlinear regression tool in MATLAB, it was found that the depth trend follows a modified Langmuir equation as

$$Depth = \exp\left(\frac{\alpha\beta F^{\gamma}}{1 + \beta F^{\gamma}}\right) \qquad (4)$$

where α, β, and γ are parameters of the equation and F is the modified fill factor defined by

$$F = c\left(\frac{wl}{(w+s)(l+s)}\right) \qquad (5)$$

In the model presented in equation 4, α is representative of the maximum depth achievable by the pattern as c increases to an infinite value, illustrated previously in Figure 6. The value of α is the depth that will be used in the characterization of the Alcatel etcher to quantify RIE lag. β and γ are parameters that describe the convergence of the depth with increasing W_P. A set of pattern parameters with a high β value indicates that there is a smaller RIE lag effect at small pattern widths as compared to a lower β value. A set of parameters with a high γ value will converge to the maximum depth faster than a set with a low γ value.

The equation parameters α, β, and γ were found to follow mathematical trends between combinations of s, w, and l. The equations for α, β, and γ are functions of s, w, and l, measured in
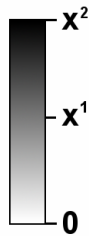
micrometers, and are presented in Table 6. Examining the structure of the equations presented in Table 6 provides useful information about the influence of s, w, and l on the channel dimensions. α and β are exponential equations and γ is a constant term. Table 7 illustrates the qualitative influence of each pattern variable on the three model parameters. When looking at the maximum depth achievable, α in Table 6, the results are intuitive. The maximum depth increases as the density of exposed surface area as well as time increase. The relationships of the variables to the β term are much different. When s and w are increased, the lag at small values of c decreases; however, increasing l increases β. Also, the spacing, s, of the pattern is by far the most influential factor in the value of β. The γ term, on the other hand, is only influenced by time. As etch time increases, the difference in etch rate at high values of c attributable to RIE lag becomes more pronounced, and a wider pattern span is required to achieve the maximum depth possible for a given set of s, w, and l.

Table 6: Model parameters for 15 and 30 minute etch durations.

Parameter	15 mins	30 mins
α	$4.15\exp\left(-0.45\dfrac{s}{lw^{2/3}}\right)$	$5\exp\left(-0.35\dfrac{s}{lw^{2/3}}\right)$
β	$(0.2w+4.25)\exp\left(0.4\dfrac{s^2}{lw^{1/2}}\right)$	$(0.2w+2.3)\exp\left(0.3\dfrac{s^2}{lw^{1/2}}\right)$
γ	$3/4$	$1/2$

Table 7: Qualitative of influence of pattern variables on model parameters. The + sign indicates a positive proportionality, and the − sign indicates a negative proportionality.

28

The model achieves prediction quality averaging less than 5% error when fit to a single wafer. When the model is fit to data from several different wafers, the error can increase to 15% due to process differences between wafers. These wafer-to-wafer differences can be accounted for by the addition of a multiplicative error term preceding the modified Langmuir equation for depth (equation 4). Figures 15a and 15b contain plots illustrating the predictive quality of the model. It is evident from Figure 15a that the structure of the model accurately describes the trends in wafers etched for 15 and 30 minutes, even with wafer-to-wafer process differences. Accuracy is shown in Figure 15b to increase further if the error term is known for each wafer. However, the value of the error term can be diminished with increased consistency of fabrication processes. Specifically, the key areas include photoresist thickness, baking conditions, development times, and consistency of the etch conditions.
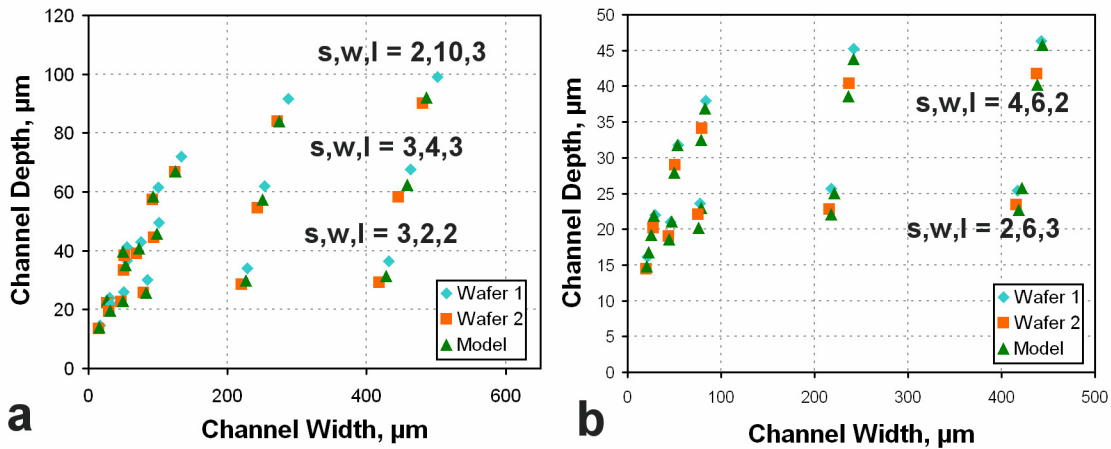
Figure 15: (a) Model accuracy for two wafers without an error term. Despite wafer-to-wafer differences, the model predicts with < 15% error. (b) Model accuracy for two wafers with an error term. The model is fit directly to the data in wafer 1, and with an incorporated error term for wafer 2. Equivalent accuracy results for both wafers.

3.2.2 Characterization of the AMS-100

In order for the same experiment to be carried out on a different etcher, the etcher has to be characterized so that RIE lag is at a maximum. The experimental results from the characterization of the Alcatel AMS-100 system showed that there was a significant relationship

between the etch process parameters and the magnitude of RIE lag. Figures 16 and 17 contain

digital images of the cross section of a small and a large channel from two different wafers. The

wafer in Figure 16 experienced less RIE lag than the wafer in Figure 17. In order to have an idea

of the degree of correlation between the process parameters and the measured variables, statistical

software (Minitab) was used. The RIE lag and L/D data is contained in Table 8. The main

effects and interactions plots produced by Minitab from the data are presented in Figures 19-22.

The dataset included 14 wafers rather than 16 because the two runs with high pressure and flow

rate and low coil power were unable to maintain stable plasma. The plots are constructed by

averaging the magnitude of the output at each setting of the independent variable(s).   The

resulting plot is a visual reference of the output sensitivity to each variable or group of variables.
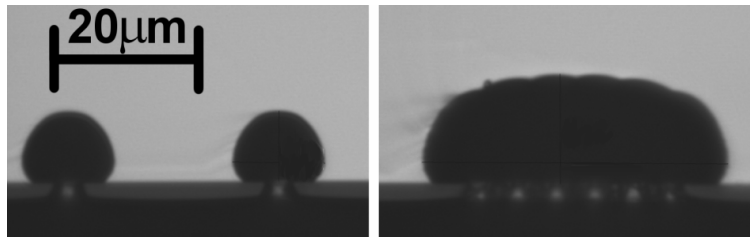
Figure 16: Channels etched from a low-RIE-lag process. Two channels with c = 1 and one with c = 6 from the set $<s,w,l>$ = $<2,6,4>$ and coil power = 1300 W, pressure = 0.11 mbar, flow rate = 100 sccm, and substrate temperature = -10 °C. Very low RIE lag is demonstrated as c increases.

Figure 17: Channels etched from a high-RIE-lag process. Two channels with c = 1 and one with c = 6 from the set $<s,w,l>$ = $<2,6,4>$ and coil power = 2200 W, pressure = 0.11 mbar, flow rate = 400 sccm, and substrate temperature = 20 °C. High RIE lag is demonstrated as c increases.
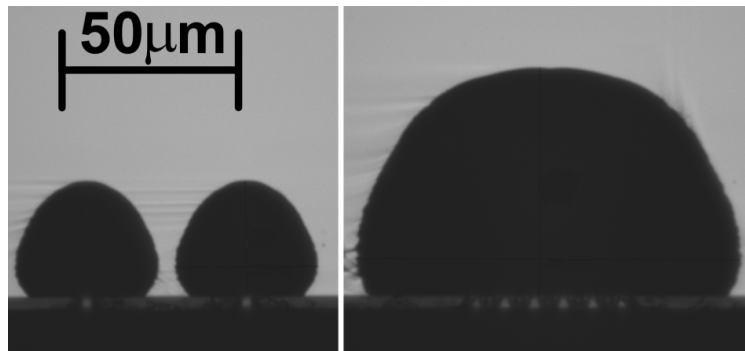
Table 8: RIE lag and L/D vs. process parameters. Two of the sixteen sets were unable to produce stable plasma and are therefore not shown here.

Temp (°C)	Coil Power (W)	Pressure (mbar)	Flow Rate (sccm)	RIE lag (μm)	L/D
-10	1300	.02	100	14	0.35
-10	1300	.02	400	18	0.43
-10	1300	.11	100	9	0.23
-10	2200	.02	100	20	0.32
-10	2200	.02	400	31	0.43
-10	2200	.11	100	21	0.29
-10	2200	.11	400	50	0.44
20	1300	.02	100	13	0.33
20	1300	.02	400	19	0.45
20	1300	.11	100	11	0.33
20	2200	.02	100	20	0.36
20	2200	.02	400	29	0.48
20	2200	.11	100	19	0.30
20	2200	.11	400	51	0.51

3.2.2.1 RIE Lag

The main effects plot in Figure 19 indicates that the coil power and the flow rate are the main contributors to RIE lag. Both parameters created an average increase of approximately 20μm from their low to their high values. In order to gain physical insight into the reason that this relationship exists, it should be pointed out that the measured RIE lag increases with overall etch rate. In accordance with previous analysis, etch rate increases when species transport is high, such as increasing w and l and decreasing s [20, 28]. Since RIE lag arises from transport limitation, any reaction limiting factor will eventually overshadow the possible presence of lag. Factors that increase the substrate etch rate reduce reaction limiting effects and, hence, make RIE lag more prominent. Using this insight, physical reasoning can be used to explain the trends observed.

The main effects plots indicate that flow rate has a strong positive influence on RIE lag. The reason for this trend can be tied to residence time of gas in the chamber. Low residence time introduces more gas to the plasma and it also helps to remove volatile etch products [13]. Figure 18 contains a plot of residence time versus pressure for different values of SF_6 flow rate.

Residence time decreases as pressure decreases and flow rate increases; however, the effect from flow rate is more pronounced. The low residence time and the increased amount of reactive gas resulting from high flow rate increases etch rate and, thus, RIE lag.

Increased coil power works to increase etch rate as well by increasing the maximum ion energy. Since the main mechanism of in-plane etching is from ion-assisted chemical reaction [11], increasing the energy that these ions have will increase the etch rate of silicon in that direction. Since RIE lag is only measured by the in-plane etch rate in this experiment, it increases as well. Increasing pressure also increases RIE lag to a lesser extent than coil power and flow rate.
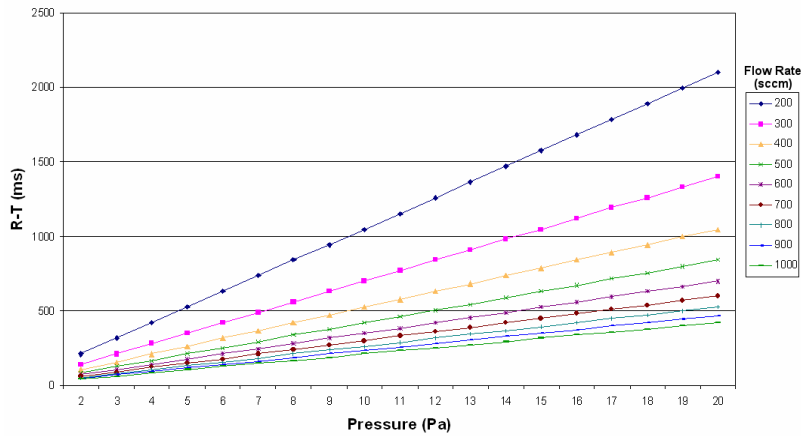

Figure 18: Residence time vs. pressure and SF_6 flow rate. Residence time decreases as pressure decreases and flow rate increases.
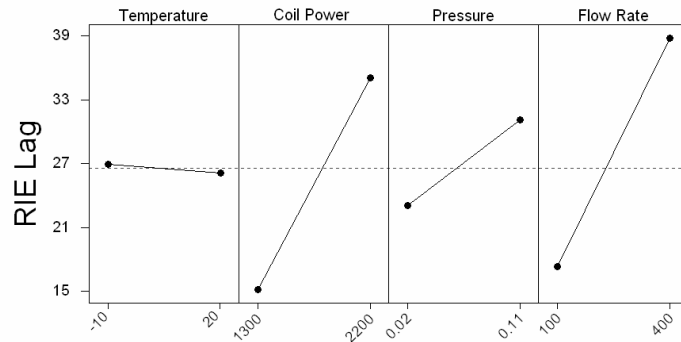

Figure 19: Main effects plot for RIE lag. SF_6 flow rate and coil power have the greatest positive effect on RIE lag.

The interactions plot for RIE lag, Figure 20, indicates that strong interactions exist between coil power and pressure as well as SF_6 flow rate and pressure. Pressure works to increase the amount of gas that is in the chamber available to be energized by the plasma. However, high pressure also increases the residence time of the species in the chamber. The increase in the density of the plasma that comes with high pressure increases RIE lag only as long as the introduction of new species is high and the energy of the plasma is high enough to excite the gas molecules. The interactions plot shows that when flow rate is low, increasing the pressure has no positive effect on the magnitude of RIE lag. When coil power is low, there is actually a decrease in etch rate as pressure increases. A possible explanation for this relationship is that as pressure increases, the mean free path decreases which results in a higher frequency of collisions between gas molecules. At low power, these collisions begin to affect the path of reactive species. The decrease of etch rate with increasing pressure at low coil power has been confirmed by Ayon et al. [14]. There is also a small positive interaction between coil power and flow rate.

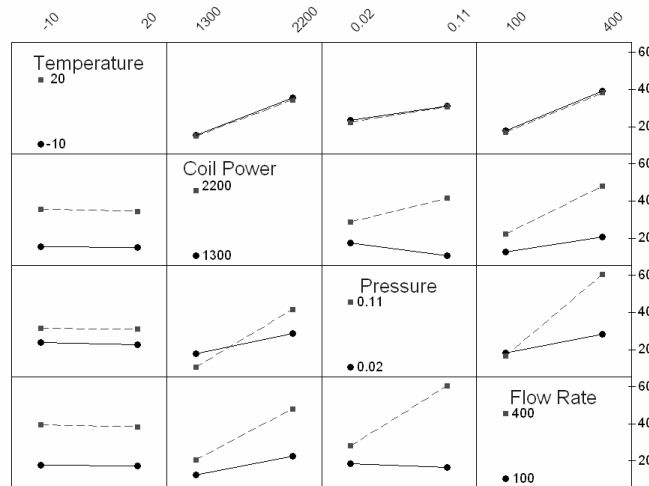
Figure 20: Interactions plot for RIE lag. The significant interactions result from pressure and coil power as well as pressure and flow rate.

3.2.2.2 Lateral/In-Plane Etch Rate

Highly directional ions and reactive radicals work together to etch in the in-plane direction, but lateral etching occurs only by the reflection and spontaneous reaction of radicals off

of the bottom of the channel. Therefore, the parameters that will increase the lateral to in-plane etch rate will be those that increase the probability of reflection. The main effects plot in Figure 21 indicates that SF_6 flow rate is the most influential factor in the value of L/D. As flow rate increases, more reactive species enter the chamber and increase the amount of radicals available to etch the sidewalls. The rest of the parameters had smaller effects on L/D. Figure 21 shows a non-intuitive negative response from pressure. As pressure increases, it promotes the formation of atomic fluorine, which should increase the lateral etch rate. However, the value of L/D decreased with pressure. One explanation for this behavior could be that the mean free path decreases at such high pressure, limiting the chances that reflected species will contact the adjacent wall.
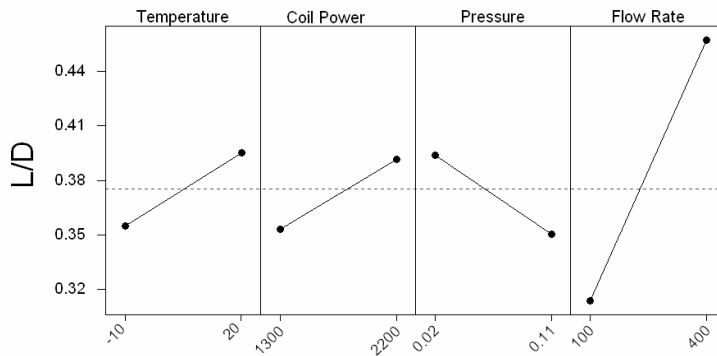

Figure 21: Main effects plot for L/D. Flow rate is the major factor in the value of L/D. Pressure has the only negative relationship to L/D.

The other two parameters, substrate temperature and coil power, had a positive effect on L/D, with approximately the same magnitude change as the effect from pressure. Coil power increases the lateral to in-plane etch ratio because it adds to the energy of the plasma by increasing the amount of species that travel to the substrate and by increasing their energy. Both of these factors contribute to the higher probability of reactive reflection from the bottom surface of the channel. Temperature increases the value of L/D because it increases the reaction energy of the radicals. Temperature did not affect the in-plane etch rate because temperature has no

effect on the energy of the highly directional ions, the main mechanism of in-plane etching. This is the only parameter that increases the lateral etch rate without changing the in-plane etch rate significantly. This result has been confirmed in a microwave plasma etcher by Tachi et al. [23].

The interactions plots for L/D in Figure 22 indicate that the two major interactions are between pressure and coil power and pressure and flow rate. In general, the effect of adding pressure decreases the value of L/D. However, when flow rate is high there is a very slight increase. It should be mentioned that this trend is suspect because this portion of the plot is only based on two wafers instead of four due to the aforementioned inability to maintain stable plasma when pressure and flow rate are high and coil power is low. The interaction between coil power and pressure indicates two limiting cases. When pressure is at a low value, the residence time is low and increasing the coil power does not affect the value of L/D. The other limiting case is when coil power is high and pressure increases. In this case, there is also no change in L/D. Even though the overall etch rate changes, the ratio between the etch rate in each direction stays the same.

From these results it can be concluded that in order to increase RIE lag the etch parameters should be chosen so that etch rate is increased as much as possible. This allows the transport limiting effects of the surface geometry to be used to their fullest extent. Parameter values that increase RIE lag are 2200W coil power, 400sccm SF_6 flow rate, and 0.11mbar chamber pressure. The substrate temperature was found to have negligible effect on the in-plane etch rate, but showed a slight positive relationship with lateral etch rate. Thus, the substrate temperature can be adjusted to fit the needs of the desired device without affecting the magnitude of RIE lag. These characterization results have been submitted to the Journal of Vacuum Science and Technology A for publication [29].
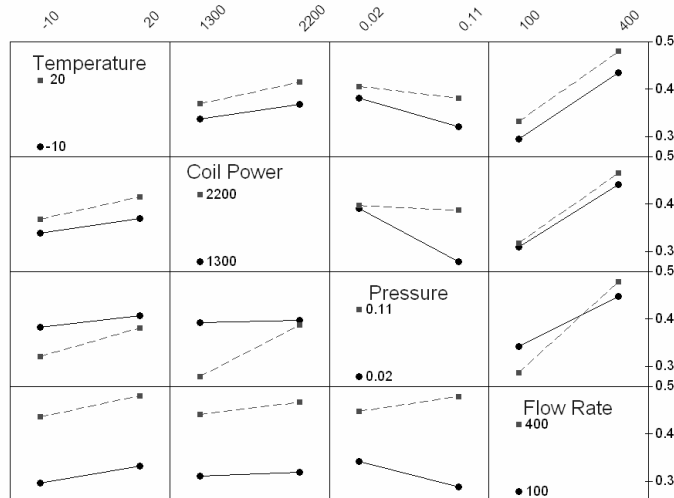
Figure 22: Interactions plot for L/D. The only significant interactions result from pressure and coil power as well as pressure and SF_6 flow rate.

3.2.3 Development of a Comprehensive Etch Model

3.2.3.1 Comprehensive Model

After the initial model had been found for specific etch times using the STS etcher, the universality of the model had to be tested using another etcher. We used an Alcatel AMS-100 etcher for this. Not only were the wafers used to test the previously developed model, but more wafers were also etched for different durations so that etch time could be incorporated into the model.

After all of the depth and width data had been collected from the structures fabricated using the AMS-100 for each etch duration, the data was successfully fit to equations 2 and 4. Due to the fact that this portion of the experiment was carried out on an Alcatel AMS-100 etcher and the previous portion was performed on an STS etcher, the respective model coefficients are very different despite having the same equation form. The reason for this difference is linked to the AMS-100 having almost two times the etch rate of the STS system. This difference in etch rate is evident from the plot of all the possible depth and width combinations from the Alcatel

etcher, Figure 23, being much larger than that from the STS etcher for a longer etch duration, Figure 10. The reasons for this etch rate difference have previously been stated.
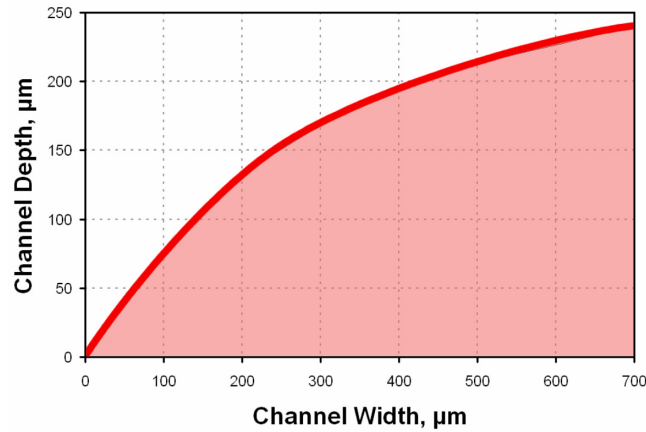

Figure 23: Achievable channel dimensions using the Alcatel DRIE tool. The maximum etch time is 25 minutes in an Alcatel AMS-100 etcher.

The fact that the equations applied to the STS etcher as well as to the Alcatel etcher, even with different etch parameters, leaves the possibility that the equations reveal something about the nature of the process and are not unique to each etcher. However, based on the previous characterization of the etcher, it is known that the amount of lateral etch in relation to the depth changes depending on the process parameters. Even though the model might change under certain etch conditions, there could be a common regime in all deep reactive ion etchers that the model applies to.

In order to determine how etch duration affects the depth and width of the channels, the coefficients of the model for each wafer fabricated by the AMS-100 need to be examined in their relationship to time. The first term, α, was found to increase exponentially over time for the same value of s, w, and l. In the case of these wafers, the α term for all times is

$$\alpha = \left[\frac{4.51\left(5.92\left(\dfrac{l}{s^2} \right)^{0.77} \right)w}{1 + \left(5.92\left(\dfrac{l}{s^2} \right)^{0.77} \right)w} \right] \exp(.02(t - 10)) \qquad (6)$$

where the term preceding the exponential term is the α equation for all examined wafers calculated at 10 minutes.

The β and γ terms behaved differently over time compared to α. For these terms, the coefficients of equations 2 and 4 were plotted over time and regression was fit to their behavior. The final equations for β and γ modeled from the four examined wafers are

$$\beta = \left(2.75\frac{w}{t} - 0.09\,t + 4 \right) \exp\left(0.3\frac{s^2}{l\sqrt{w}} \right) \qquad (7)$$

$$\gamma = -0.023t + 0.97 \qquad (8)$$

β is a function of the geometric variables and time while γ is only a function of time. Equation 4, the original equation for width, applies to the new model as well.

3.2.3.2 Accuracy

When the accuracy of the comprehensive model is compared to the data that the model was constructed from, an average of 10% error for depth and width result. The variation in accuracy is present due to inconsistencies in the photolithography and etching steps as was observed from the STS etched wafers. An average of 5% error arises in the model from photolithography pattern variation of just $\pm 0.5\mu$m. Despite these wafer-to-wafer differences, the

excellent accuracy of the model can be seen in Figure 24a for a typical set of channels over the four tested etch durations. When the overall fit of the model to the data is examined there are two sets of surface geometry where large error was observed. The first is when $w = l = 2$ μm. In this set, a combination of underexposure and the reduced etch rate of small features in the oxide masking layer contributed to a much lower etch rate than what was expected. The second set was when $l = 4$ μm, $t = 25$ min, $w > 4$ μm, and $c > 6$. In this regime a reverse lag effect was observed and the etch rate decreased as more surface area was exposed. The reverse lag effect is visible in Figure 25. A reasonable explanation for this observation is microloading. The presence of significant microloading effects at 25 minutes indicates that there is likely a maximum applicable time for the model. If the model is to be applied past 25 minutes, the exposed area should be relatively small to prevent etch rate limiting by microloading.
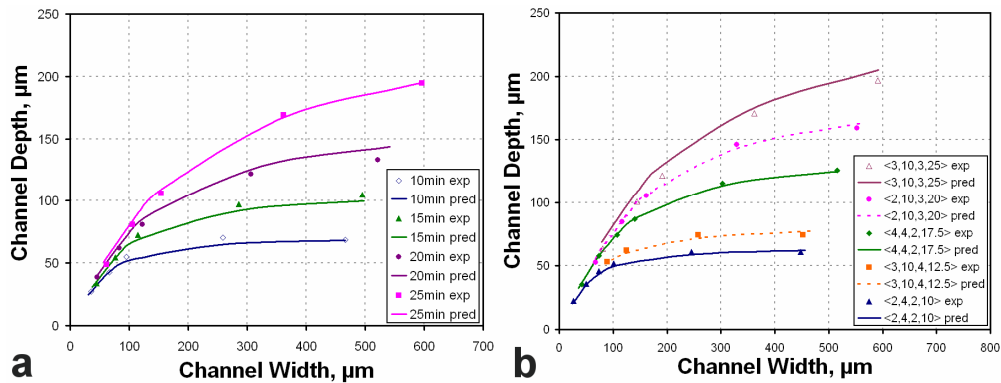

Figure 24: (a) Comprehensive model fit to $\langle s,w,l \rangle = \langle 2$μm, 6μm, 2μm $\rangle$ from 10 to 25 minutes. (b) Comprehensive model fit for several channels and etch durations. The wafers etched for 12.5 and 17.5 minutes were not used in constructing the model.
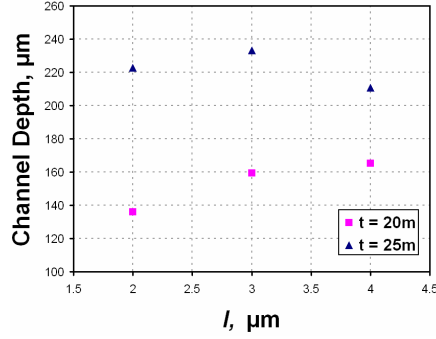
Figure 25: Channel depth vs. *l* showing reverse RIE lag. *s* = 2μm, *w* = 10μm, and *t* = 25. When *t* = 20 for the same pattern, reverse RIE lag is not evident.

The accuracy of the model was also tested by two different wafers that were not used in developing the model. The examined wafers were etched for 12.5 and 17.5 minutes by the same process as the previous four wafers. Three sets of *s*, *w*, and *l* were measured at random on each wafer and were compared with the calculated values from the model. The 12.5 minute wafer had the worst prediction quality of the two and returned an average of 7% prediction error in depth and 6% in width. Even greater accuracy in predicting these wafers when compared to the wafers that were used to construct the model demonstrate the consistency of the model in describing the etch process. The accuracy of the model in predicting both sets of wafers is visually evident in Figure 24b, a plot of the calculated and experimental channel dimensions for both sets of wafers.

Despite the suitable accuracy that results from the developed comprehensive model, the exact values of the model coefficients should be used with care during microfluidic design. When using the technique to fabricate channels from an entirely different mask, the etch rate will change due to macroloading. When the amount of exposed area exceeds a certain value, a reaction limited regime is reached and etch rate is decreased over the entire wafer. A brief experiment was performed with 25% (5.9×10^7 μm^2) and 50% (1.18×10^8 μm^2) of the mask pattern exposed, and for a single pattern exhibiting moderate RIE lag (*s* = 3μm, *l* = 3μm, *w* = 6μm) etch depth was found to increase by a maximum of 20% for the widest channel span. The equation form will still hold for any mask, but the magnitude of the results will change with a change in

40

etch rate due to macroloading. The relationship between total exposed area and etch rate is under investigation to be incorporated into the model. Nevertheless, the degree of macroloading should be factored in when designing microfluidic structures using the equations presented here.

3.2.4 Three-Dimensional Microfluidic Device Fabrication

The newly developed comprehensive model was used to design a mask for microfluidic structures. With a computer program written in MATLAB, the desired depth and width of a device's microfluidic channels can be input and the geometric surface structure as well as the etch duration is output. Given that there are many different combinations of parameters that can create identical channels, the structures can be designed so that the least etch time is necessary for fabrication. Alternatively, the whole mask could be designed with similar pattern sizes so that exposure and development can yield consistent results over the entire wafer. The end result is an etch process with a large amount of options for the designer to control quality and efficiency of a microfluidic device without sacrificing the integrity of the design.

The widest range of channel dimensions can be achieved when the RIE lag is maximized. In this respect, the fabrication technique would benefit from high pressure, coil power, and SF_6 flow rate. All of these parameters also serve to increase the etch rate of channels. Figure 26 contains SEM images of a large microchannel intersecting with several microcapillary channels under low (Figure 26a) and high (Figure 26b) RIE lag conditions induced by different fabrication parameters. The conditions which produce maximum RIE lag result in a depth difference of 81μm between the large and small channels as opposed to the difference of 23μm that results when RIE lag is minimized. Greater design versatility results when RIE lag effects are high because a wider range of channel sizes can be fabricated on the same wafer. When very small channels are required, such as 5μm in diameter, high RIE lag (and high etch rate) parameters

would not have to be changed to lower the etch rate. Rather, the etch duration would be modified to account for this change.
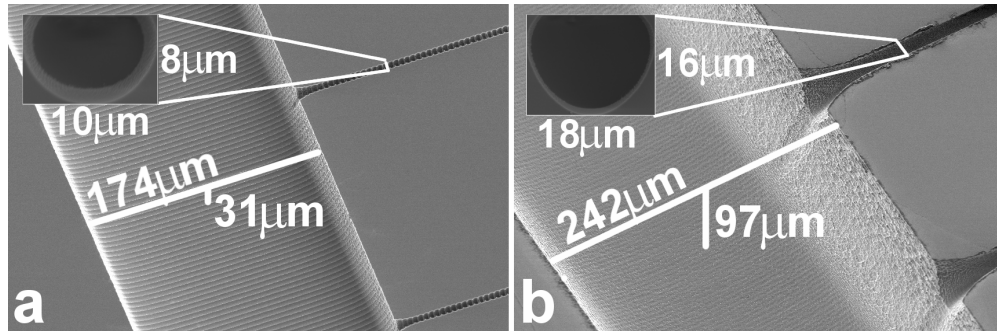

Figure 26: RIE lag effects on microfluidic structure fabrication. Structures were fabricated by a) coil power = 1300W, pressure = 0.11mbar, temperature = -10°C, flow rate = 100sccm, and b) coil power = 2200W, pressure = 0.11mbar, temperature = 20°C, flow rate = 400sccm, resulting in vastly different RIE lag effects.

Structures that were used in this study to prove the viability of design using the developed comprehensive model included a 3-D capillary network, an H-filter, a micro mixer, a cell migration channel, and several microfluidic junctions. Figure 27 shows pictures of some of the microfluidic structures that were fabricated. The results demonstrate the ability to join channels of similar and dissimilar dimensions as well as to vary the cross sectional dimensions of a single channels along the channel's length. The devices that were fabricated take advantage of the ability to accurately design channels with specific cross sectional depths and widths.
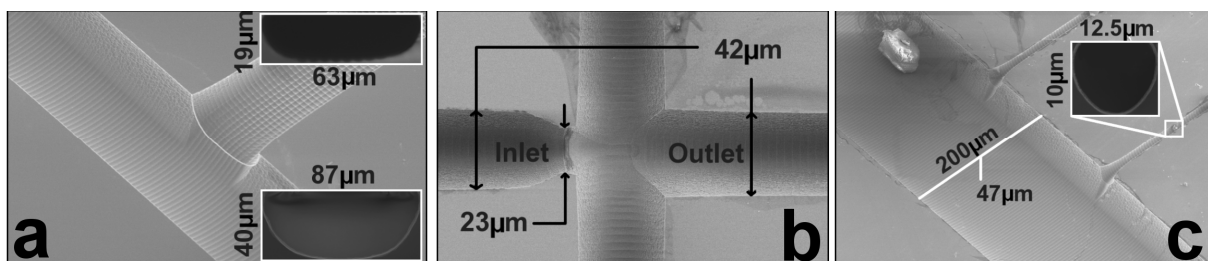

Figure 27: Microfluidic devices designed with the comprehensive model (a) an H-filter junction, (b) a micro nozzle, and (c) micro capillary passages for cell migration study.

The H-filter in Figure 27a, is designed to diffusively mix two solutions by parallel flow of the two fluids with a common surface boundary. If mixing results are to be easily simulated, a high width to depth aspect ratio is desired so that residence time of particles that diffuse in the transverse direction does not change drastically with a particle's distance from the centerline [30]. Aspect ratio control of the mixing channel is possible with the model presented in this study. The difference in aspect ratio between the main channels and the mixing channel is evident in Figure 27a. Figure 27b shows an overhead view of a micro mixer that was fabricated based on the design in [31] with three input channels and a single output channel. The input channel that is inline with the output channel is narrowed down into a nozzle to focus the fluid for mixing with another fluid that enters from either side. Another device was fabricated with small channels joined to a large channel to study cell migration (Figure 27c) following the design in [32]. The device in Figure 27c was designed so that the small channels are comparable to the diameter of a cell. A number of microfluidic junctions were also fabricated, demonstrating the wide range of microfluidic structures that are possible using this predictive single-mask process.

These devices demonstrate the high degree of flexibility in the single-mask development of 3-D microfluidic structures offered by the geometry-dependent behavior of isotropic RIE lag and the accuracy of the model in the design of such microstructures. The predicted cross sectional dimensions were accurate to an average of 6% of the measured values. This test verifies the reliability of our models for accurate design and fabrication of microfluidic channels in silicon using only one mask. These results have been presented at the Transducers '07 conference [33] and the work has been suggested for publication after minor revision by the Journal of Micromechanics and Microengineering [34].