CHAPTER 4
DECODER BOARD HARDWARE

This chapter describes the hardware components on the decoder board, and the hardware modifications needed to correct timing problems.

4.1 Overview
The decoder board is a custom designed circuit board comprised of surface mounted components. One side of the decoder board connects to the ICB backplane of the WMI via a 20-pin I/O connector, and the other side connects to the radio receiver via an IF connector. In simple terms, the function of the decoder board is to receive spread spectrum messages from the radio receiver and then forward these messages to the WMI.

Excluding the voltage regulator and oscillator circuit chips, the decoder board has the following circuit chips: Analog-to-Digital (A/D) Converter, Spread Spectrum Decoder (SSD), Microcontroller, Programmable Read-Only Memory (PROM), Random Access Memory (RAM), D Latch, Programmable Array Logic (PAL), and Serial-to-Parallel Shift Register (SPSR). Figure 4.1 shows the decoder board block diagram (for clarity, the D Latch is not shown), and its input/output (I/O) connections to the WMI and receiver.

As shown in Figure 4.1, the A/D Converter digitizes the analog messages for input to the SSD. The SSD then downconverts, despreads, and demodulates the digitized message for input to the SPSR. After the microcontroller retrieves the message from the SPSR, it packetizes the message and then transfers the message to the WMI. The PAL generates the necessary control and timing signals to coordinate the interactions of the components.

Figure 4.2 shows a simplified circuit diagram with the signal lines only. The support components such as pull-up resistors and by-pass capacitors are not shown. A complete schematic is available from Grayson Electronics Company.[4]
Figure 4.1 Decoder Board Block Diagram
Figure 4.2 Simplified Decoder Board Schematic (1 of 4)
Figure 4.2  Simplified Decoder Board Schematic (2 of 4)
Figure 4.2 Simplified Decoder Board Schematic (3 of 4)
Figure 4.2  Simplified Decoder Board Schematic (4 of 4)
4.2 Hardware Components
This section describes the function, the operating characteristics, and the I/O signals for each decoder board component.

4.2.1 Analog-To-Digital Converter
The receiver converts an RF message that has a frequency in the 900 MHz range to an Intermediate Frequency (IF) message that has a frequency of 20 MHz for input to the A/D converter. The A/D converter then digitizes the IF message into 8-bit values for input to the SSD. One must be careful not to drive the A/D analog input with excessive voltage. The receiver output voltage must satisfy the A/D converter’s nominal input voltage range of 2.788 volts (V) to 3.182 V.[1]

4.2.2 Programmable Read-Only Memory
Designated as “BOOT PROM” in Figure 4.2, this PROM contains the program code that the microcontroller executes upon decoder board power-up. The PROM contains the boot and application programs.

Grayson Electronics selected a PROM with 32 KB of memory. Consequently, the PROM has a 15-bit address bus, an 8-bit data bus, and two input control signals, CE (Chip Enable) and OE (Output Enable). The CE is an active-low signal that enables the PROM, and the OE is an active-low signal that enables the PROM output.

4.2.3 Random Access Memory
For IVDS, the RAM serves as buffer for messages to be sent to the WMI. During periods of heavy message traffic, the RAM will store backlogged messages until the WMI allows the microcontroller to send more messages.

Grayson Electronics selected a RAM with 32 KB of memory. Since a packetized message is 25 bytes long, RAM can store 1310 backlogged messages. RAM also has a 15-bit address bus, an 8-bit data bus, and two control signals, OE (Output Enable) and R/W (Read/Write). OE is an active-low signal that enables the RAM output. R/W is the signal that distinguishes between read and write operations. R/W is low for write operations and is high for read operations.

4.2.4 D Latch
To reduce the number of connections between the microcontroller and a peripheral, the D latch is used to multiplex the low address byte with the data byte on the same bus. The latch provides a constant address signal to the peripheral during the entire instruction cycle, so that the bus can be used for data during the read/write portion of the instruction cycle.
4.2.5 Serial-To-Parallel Shift Register
The SPSR converts the SSD serial data into byte quantities. SRCLK (Serial Clock) is the clock signal for shifting bits into the SPSR. After a byte is shifted into the SPSR, the most significant bit (MSB) and the least significant bit (LSB) are located in the QH and QA registers, respectively. RCLK (Read Clock) is an active-high signal that enables the SPSR output, and G (Gate Enable) is an active-low signal that enables the SPSR.

4.2.6 Programmable Array Logic
The PAL generates additional control signals for the decoder board. As shown in Figure 4.2, the PROM, RAM, SSD, and SPSR are all connected to the microcontroller on the same address and/or data bus. The PAL output control signals are used primarily to prevent bus contention when the microcontroller accesses a peripheral. Additionally, the PAL inverts two signals, generates a clock signal, and pulse width stretches another.

As shown in Figure 4.3, the PAL contains combinational logic circuits and one sequential logic circuit. The combinational logic circuits provide the additional control signals needed to prevent bus contention, and the sequential logic circuit transforms a clock signal to meet the input timing requirements of the microcontroller. Grayson Electronics originally programmed the PAL with the combinational circuits, while Virginia Tech requested Grayson Electronics to later program the sequential logic circuit.

As mentioned before, the microcontroller fetches its instructions from the PROM at power-up. The signal ROMCEn (ROM Chip Enable - not) ensures that this is accomplished. At power-up, the microcontroller ROMCE signal is initially in the high state. The PAL inverts ROMCE so that ROMCEn is in the low state, which enables the PROM and at the same time disables the RAM output.

RXACTIVEEn is an interrupt signal to the microcontroller but is not currently used. Therefore, this signal is not discussed further.

Before discussing the RAMWRn, RAMOEn, and DECODER WRn signals, MA15 is discussed since it affects these signals. MA15 is the highest order bit of the microcontroller address bus. Since the RAM and PROM have a 15-bit address bus, MA15 would not normally be unused. MA15 is used to select which peripheral is enabled during a read or write operation. If MA15 is low during read operations, the RAM output is enabled, otherwise the SPSR output will be enabled. If MA15 is low during write operations, the RAM is enabled, otherwise the SSD will be enabled. In other words, the programmer must set MA15 high when accessing the SSD or SPSR, and then immediately clear it so that RAM will be enabled.
Figure 4.3  Programmable Array Logic Gate Schematic (1 of 2)
The RAM is the only peripheral enabled during write operations when the RAMWRn (RAM Write - not) signal is low. RAMWRn is low only if MPWRn (Microcontroller Write - not) and MA15 are both low.

The RAM is the only peripheral enabled during read operations when the RAMOEn (RAM Output Enable - not) signal is low. If RAM is used to store program code, both PSENn (Program Store Enable - not) and ROMCE must be low so that the microcontroller will fetch instructions from RAM. For data reads, MPRDn (Microcontroller Read - not) and MA15 must be low so that the microcontroller will read data from RAM. Lastly, the RAMOEn signal also disables the RAM output when the microcontroller is fetching instructions from ROM.

When low, the DECODER WRn signal ensures that the SSD is the only peripheral enabled during write operations. DECODER WRn is low only if MA15 is high and MPWRn is low.

SRCLK is a clock input signal to the SPSR. The RXDRDYn (Receiver Data Ready - not) and the RXACTIVE (Receiver Active) signals from the SSD are used to generate the SRCLK signal. Figure 4.4 shows a timing diagram for these signals. Each time SRCLK transitions from low to high, a bit is clocked into the QA register while the other bits are shifted to the next registers in sequence.
The RCLK and G signals ensure that the SPSR is the only peripheral enabled during read operations. To enable the SPSR, MA15 must be high and MPRDn must be low.

RXC is an interrupt signal that indicates when valid data from the SSD is available at the SPSR output. Originally, RXDRDYn was the interrupt signal, but this signal did not meet the microcontroller timing and phase requirements. Thus, the pulse stretcher circuit shown in Figure 4.3 was developed to convert RXDRDYn into the appropriate RXC signal. Without stating the numerical details here, this circuit stretches the RXDRDYn pulse width to three times its original width and also inverts it. The RXSPLPLS (Receiver Sample Pulse) signal from the SSD is used to clock the circuit. Figures 4.5 - 4.6 show the state diagram, state table, truth table, and Karnaugh maps used to design the circuit. Figure 4.7 shows the pulse stretcher timing diagram.

As shown in Figure 4.7, RXDRDYn has a pulse width equal to one RXSPLPLS clock cycle, and RXC has a pulse width equal to three RXSPLPLS clock cycles and has opposite phase to RXDRDYn. Since the pulse stretcher is a Moore-type sequential circuit, the rising edge of RXC is delayed one clock cycle, but this does not cause adverse effects.
Figure 4.5  Pulse Stretcher State Diagram
**STATE TABLE**

<table>
<thead>
<tr>
<th>STATE</th>
<th>INPUT</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>RXDRDYn</td>
<td>RXC</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>A</td>
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<td>D</td>
<td>B</td>
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</table>

**TRUTH TABLE**

<table>
<thead>
<tr>
<th>STATE</th>
<th>INPUT</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>RXDRDYn</td>
<td>RXC</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<tr>
<td>0 0</td>
<td>0 1</td>
<td>0 0</td>
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<tr>
<td>1 1</td>
<td>1 1</td>
<td>1 1</td>
</tr>
<tr>
<td>1 0</td>
<td>0 1</td>
<td>1 1</td>
</tr>
</tbody>
</table>

**KARNAUGH MAPS**

- **RXDRDYn**
  - $Q0^* = RXDRDYn + Q1Q0$

- **Q1 Q0**
  - $Q1^* = Q0$

- **RXC**
  - $RXC = Q1 + Q0$

**Figure 4.6**  Pulse Stretcher State Table, Truth Table, and Karnaugh Maps
4.2.7 Spread Spectrum Decoder

The Z2000 Spread Spectrum Transceiver is a programmable single-chip, direct-sequence, spread spectrum transceiver manufactured by Zilog Company. The Z2000 is identical to the Stanford Telecom’s STEL-2000A. The Z2000 supports the implementation of a wide range of burst data communication applications because it supports a wide range of data rates and spread-spectrum parameters. For IVDS, the 20 MHz version of the Z2000 is used.

Since the Z2000 is a very complex component, its theory of operation is not discussed, but is provided in the product specification.[14] The discussion of the Z2000 will use a “black box” approach to describe its operation in terms of its I/O signals and will still be referenced as the Spread Spectrum Decoder (SSD). For IVDS, the Z2000 transmitter functions are not used and so are not discussed.

As shown in Figure 4.2, the SSD receives data at the Receiver In-Phase Input (RXIIN) port. RXIIN is an 8-bit input port for in-phase data from external A/D converters. The SSD is programmed to receive data in offset binary format. Following downconversion, despreading, and demodulation, the SSD output appears at its Receiver Output (RXOUT) port as a serial data stream.

The SSD provides the Receiver Data Ready Bar (/RXDRDY) as an output timing signal. /RXDRDY is normally high and pulses low during the baseband sampling clock cycle when a new RXOUT signal is generated. RXOUT data bits are valid on the rising edges of /RXDRDY. /RXDRDY has a 25 microsecond period with a low level pulse width of 0.25 microseconds. It should be noted that RXDRDYn is equivalent to /RXDRDY.

The SSD also provides Receiver Sample Pulse (RXSPLPLS) as an output timing signal that provides internal timing information to the user. RXSPLPLS is the internally generated baseband sampling clock. Excluding downconverter functions, all receiver
functions trigger internally on the rising edges of RXSPLPLS. This signal is a square wave with a period of 0.25 microseconds.

Lastly, the SSD provides Receiver Active (RXACTIVE) as an output timing signal. A high level on RXACTIVE indicates that the receiver has detected an Acquisition/Preamble Symbol and is currently receiving data symbols. RXACTIVE will be high one bit period before the first rising edge of /RXDRDY, indicating that the first data bit is about to appear at the RXOUT pin. RXACTIVE will go low immediately following the last rising edge of /RXDRDY, indicating that the last data bit has appeared at the RXOUT pin.

Figure 4.8 shows a timing diagram of the output timing signals for a 2-bit sample data burst. RXSPLPLS is not drawn to scale since there would be 100 cycles in between the two low pulses of RXDRDYn. Figure 4.8 also shows the RXC timing signal. The high pulse width of RXC is 0.75 microseconds which, as stated before, is three times longer than the low pulse width of RXDRDYn.

To program the SSD, the SSD has a 7-bit address bus and an 8-bit data bus. There are 87 data registers that are configured for a specific application. The contents and purpose of these registers are discussed in Chapter 5. The register contents are write-only and so there is no direct method for verifying their contents.

For troubleshooting purposes, the SSD has a Receiver Test (RXTEST) port that provides access to sixteen points within the receiver. The RXTEST output is selected according to the value set in its control register. All signals available at this port, with one exception, are expressed as two’s complement values, ranging from -128 to +127. The PN Matched Filter power output value is an unsigned binary number, ranging from 0 to 255.

The decoder board provides easy access to the data values on the RXTEST port and so an attempt was made to use this test port to evaluate the operation of the SSD during its initial development. However, this test port was not very useful due to the vagueness of the documentation on how to interpret the output values. As an example, the Dot Product of the Differential Demodulator and Carrier Discriminator test point was viewed on the RXTEST port. The documentation only states that this signal changes once per symbol during the data acquisition process. Although the signal was changing, it could not be determined from the data values if the SSD was configured and/or operating correctly. Since the RXTEST port was not very useful, it is not discussed further.
The microcontroller on the decoder board is a high speed Dallas Semiconductor microcontroller (DS80C320). The DS80C320 is a fast Intel 80C31/80C32 compatible microcontroller. The Intel 80C31/80C32 are members of the MCS-51 microcontroller family which is a collection of functional and pin compatible ROM, ROMless, and EPROM single component 8-bit microcontrollers.

The DS80C320 has a redesigned processor core so it executes instructions 1.5 to 3 times faster than the original Intel 80C32 for the same crystal rate. The Intel 80C32 uses 12 clock cycles per machine cycle, whereas the DS80C320 uses only 4 clock cycles per machine cycle. The DS80C320 offers a maximum crystal rate of 25 MHz, but has a crystal rate of 11.059 MHz on the decoder board.
The DS80C320 has four 8-bit I/O ports, three 16-bit timer/counters, and 256 bytes of scratchpad RAM. It has a multiplexed address/data bus, and the capability to address 64 KB ROM and 64 KB RAM. It also has a power-fail reset, a programmable watchdog timer, an early warning power fail interrupt, two full duplex hardware serial ports, and thirteen total interrupt sources with six external. Many of the these features are used for the decoder board and are described next. Only the more important details are given, but detailed descriptions are provided in the DS80C320 data sheet.[2]

The AD0 - AD7 address/data bits on Port 0 form the multiplexed address/data bus. When the Address Latch Enable (ALE) signal is high, the least significant byte of the memory address is clocked into the latch. When ALE goes low, Port 0 transitions to a bi-directional data bus for peripheral read/write operations. Also, A8 - A15 address bits on Port 2 form the most significant byte for external addressing.

Port 1 functions as both an 8-bit bi-directional I/O port and as an alternate functional interface for external interrupts, Serial Port 1, and Timer 2 I/O. Port 1 is used as a bi-directional I/O port on the decoder board. The reset condition of Port 1 has all bits in the high state. P1.3 - P1.0 pins are connected to light emitting diodes (LEDs) which illuminate when the signal is low. P1.4 is the ROMCE signal that forces the microcontroller to fetch instructions from ROM upon a reset condition. P1.5 - P1.7 pins are connected to the synthesizer of the radio receiver and are the following signals, respectively: Synthesizer Enable (SYN#ENAN), Synthesizer Clock (SYN#CLK), and Synthesizer Data (SYN#DATA).

Port 3 functions as both an 8-bit bi-directional I/O port and as an alternate functional interface for external interrupts, Serial Port 0, Timer 0/1 inputs, RD and WR strobes. For the decoder board, Port 3 functions as the alternate functional interface (except P3.5) with the alternate modes outlined below.

<table>
<thead>
<tr>
<th>Port</th>
<th>Alternate Mode</th>
</tr>
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<tbody>
<tr>
<td>P3.0</td>
<td>RXD0   Serial Port 0 Input</td>
</tr>
<tr>
<td>P3.1</td>
<td>TXD0   Serial Port 0 Output</td>
</tr>
<tr>
<td>P3.2</td>
<td>INT0   External Interrupt 0 Input</td>
</tr>
<tr>
<td>P3.3</td>
<td>INT1   External Interrupt 1 Input</td>
</tr>
<tr>
<td>P3.4</td>
<td>T0     Timer 0 External Input</td>
</tr>
<tr>
<td>P3.5</td>
<td>T1     Timer 1 External Input</td>
</tr>
<tr>
<td>P3.6</td>
<td>WR     External Data Memory Write Strobe</td>
</tr>
<tr>
<td>P3.7</td>
<td>RD     External Data Memory Read Strobe</td>
</tr>
</tbody>
</table>
RXD0 and TXD0 are the receive and transmit serial lines between the DS80C320 and the WMI. The baud rate and protocol for serial communications is discussed in Chapter 5. External Interrupts 0 and 1 inputs are connected to RXACTIVE and RXACTIVEn, respectively. Timer 0 External input is connected to RXC. The External Data Memory Read and Write strobes are used to differentiate the read and write operations when the DS80C320 accesses peripherals. Lastly, P3.5 is maintained as a bi-directional pin that is connected to the Synthesizer Lock (SYN#LOCK) output.

4.2.9 Synthesizer
Although the synthesizer is located in the radio receiver, it is discussed here since the microcontroller initializes it. The radio receiver uses a Philips Semiconductors low voltage, dual frequency synthesizer (UMA1018M) to tune the receiver to a desired carrier frequency. The UMA1018M is a BICMOS device that integrates prescalers, programmable dividers, and phase comparators to implement two phase-locked loops. The principal synthesizer operates at Voltage Controlled Oscillator (VCO) input frequencies up to 1.2 gigahertz (GHz), while the auxiliary synthesizer operates to 300 MHz. Each synthesizer has a fully programmable reference divider. All divider ratios are supplied via a three-wire serial programming bus. A complete description of the synthesizer is provided in the product specification.[10]

Similar to the SSD, the synthesizer is viewed as a blackbox. The synthesizer is programmed using a three-line unidirectional serial bus. The three lines are DATA, CLK, and E (Enable) and correspond to the microcontroller signals SYN#DATA, SYN#CLK, and SYN#ENAN, respectively. The data sent to the synthesizer is loaded in bursts framed by E. Programming clock edges and the data bits are ignored until E goes low. The programmed information is loaded into the addressed latch when E returns high. Only the last 21 bits serially clocked into the synthesizer are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. Lastly, the LOCK signal, which corresponds to the microcontroller signal SYN#LOCK, signals the microcontroller when the synthesizer is locked or tuned to the desired carrier frequency.

4.3 Summary
The decoder board is a custom designed circuit board that decodes IF spread spectrum messages from the receiver and then sends the messages to the WMI. To perform this function, the decoder board uses the following circuit chips: A/D converter, Spread Spectrum Decoder, Microcontroller, ROM, RAM, Programmable Array Logic, and Serial-to-Parallel Shift Register.

The A/D converter digitizes IF spread spectrum messages for input to the SSD. The SSD downsamples, despreads, and demodulates the IF messages. The microcontroller initializes the synthesizer and SSD, and packetizes the messages for transfer to the WMI. The ROM contains the software instructions for the microcontroller, and the RAM is used
as a storage buffer for messages that are to be sent to the WMI. The PAL contains combinational logic circuits that provide necessary control signals to prevent bus contention between peripherals connected to the microcontroller. The SPSR receives the serial data stream from the SSD and converts these bits into byte quantities for the microcontroller.

The PAL also contains one sequential logic circuit. This circuit stretches the pulse width of the RXDRDYn signal to three times its normal width and inverts it. This was done so that the RXC signal would satisfy the hold time requirements for an interrupt signal to the microcontroller.