LIST OF FIGURES

1.1	Interactive Video Data Service System Block Diagram	1
3.1	Laboratory Configuration for IVDS System	4
3.2	Interface Control Board Block Diagram	5
3.3	WMI Kernel Program Flow Chart	8
3.4	WMI Kernel Memory Map	9
3.5	Simplified Flow Chart for WMI Application Program	10
4.1	Decoder Board Block Diagram	13
4.2	Simplified Decoder Board Schematic	14
4.3	Programmable Array Logic Gate Schematic	20
4.4	SRCLK Timing Diagram	22
4.5	Pulse Stretcher State Diagram	23
4.6	Pulse Stretcher State Table, Truth Table, and Karnaugh Maps	24
4.7	Pulse Stretcher Timing Diagram	25
4.8	Sample SSD Data Burst Timing Diagram	27
5.1	DS80C320 Memory Map	32
5.2	Flow Chart for Receive ISR in Decoder Board Boot Program	36
5.3	Flow Chart for “Send STX/EOT” Subroutine in Decoder Board Boot Program	37
5.4	Flow Chart for “Send Serial” Subroutine in Decoder Board Boot Program	38
5.5	Flow Chart for Transmit ISR in Decoder Board Boot Program	39
5.6	Flow Chart for Main Routine in Decoder Board Application Program	40
5.7	Interactive Video Data Service Message Format	41
5.8	Synthesizer Control and Data Registers	43
5.9	Receiver Block Diagram	44
5.10	Principal/Auxiliary Synthesizer Block Diagram	44
5.11	Main Divider Coefficient Calculations for Synthesizer	45
5.12	Flow Chart for Synthesizer Initialization Subroutine	46
5.13	Subroutine Flow Charts for Sending Synthesizer One/Four/Eight Data Bits	48
5.14	Subroutine Flow Chart for Setting Principal Main/Reference Divider Coefficient	49
5.15	Flow Chart for Spread Spectrum Decoder Initialization Subroutine	51
5.16	Spread Spectrum Decoder Register Summary	53
5.17	Spread Spectrum Decoder Register Contents	54
5.18	Example Bit Stuffed IVDS Message	55
5.19	Flow Chart for Timer 0 ISR in Decoder Board Application Program	57
5.20	Flow Chart for Timer 2 ISR in Decoder Board Application Program	62
5.21	Flow Chart for Transmit ISR in Decoder Board Application Program	64
5.22	Flow Chart for “Send STX/EOT” Subroutine in Decoder Board Application Program	65
5.23	Flow Chart for “Send Serial” Subroutine in Decoder Board Application Program	66

LIST OF FIGURES

6.1	Motorola 68HC11 and Decoder Board Interface Block Diagram	71
6.2	Logic Analyzer Setup Menu Settings for Capturing Bits	73
6.3	Logic Analyzer Threshold Menu Settings	73
6.4	Logic Analyzer Trigger Menu Settings for Capturing Bits	74
6.5	Logic Analyzer Trigger Menu Settings for Capturing Bits After Start Bit	75
6.6	Logic Analyzer Setup Menu Settings for Capturing Bytes	76
6.7	Logic Analyzer Trigger Menu Settings for Capturing Bytes	77
6.8	Analog Pulse Stretcher Circuit	78