Self-Oscillating Unified Linearizing Modulator

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(Abstract)

The continuous conduction mode (CCM) boost, buck-boost and buck-boost derived pulse-width modulation dc-dc converters suffer from the large-signal control-to-output nonlinearity. Without feedback control, the large-signal control-to-output nonlinearity would lead to output overregulation and even damage the components.

The control gain is defined as the ratio of output voltage to control signal. The small-signal control gain is defined as differentiating output voltage with respect to control signal.

Feedback control helps to make the output trace the reference signal. A large-signal control-to-output linearity is established. Compared with open loop control, the feedback loop design is complex; and the feedback control might suffer from the instability caused by the negative small-signal control gain, which is due to the loss and parasitic in practice.

Except feedback control, open loop linearization methods can also realize the large-signal control-to-output linearity.

A modulated–ramp pulse-width modulation generator is introduced in [6]. A current source works as the control signal. A capacitor is charged by the current source, whose voltage works as the carrier and compared with a constant dc bias voltage to determine the duty cycle. When applying this method to boost, buck-boost and buck-boost derived PWM dc-dc converters, a

large-signal control-to-output linearity is established. However, the control gain is dependent on the input voltage; it cannot maintain constant when input voltage varies.

A feedforward pulse width modulator is introduced in [39] to realize a large-signal control-to-output linearity. The static conversion ratio is divided into numerator and denominator as the functions of duty cycle. An integrator with reset clock signal helps to determine the right timing. The control gain is ideally constant and independent of input voltage. However, the mismatch between the integrator time constant and the switching period would result in a nonlinear control gain, which is dependent on the input voltage.

In the thesis work, a self-oscillating unified linearizing modulator is introduced. It first provides a unified procedure to establish a large-signal control-to-output linearity for different pulse-width modulation dc-dc converters. Feedforward is employed to mitigate the impact from line voltage. Self-oscillation is adopted to provide the internal clock signal and to determine the switching frequency. A constant control gain is obtained, independent on the input voltage or the mismatch between clock signals. The modulator is constructed by three simple and standard building blocks. With the considerations of parasitic components and loss, how to design the constant gain, which excludes the negative small-signal control gain within the entire control signal range, is analyzed and discussed.

The performance of this self-oscillating unified linearizing modulator is verified by experiments. The impacts from propagation delay in practical components are taken into considerations, which improves the quality of generated signals. Combined with a boost converter, a good large-signal control-to-output linearization is demonstrated.

In the future work, the small-signal control-to-output transfer function is first deduced based on the SOUL modulator. Bode plots show the unique characteristic based on the SOUL modulator compared with the conventional modulator. Next, the impacts from this unique characteristic to feedback loop design and dynamic performance are discussed.

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Chapter 1. Introduction

1.1 Introduction and Motivation

The field of power electronics is concerned with the processing of electrical power using electronics devices. The key element is the switched-mode power conversion.

In general, a power conversion consists of a power stage and a control stage, as shown in Figure 1.1. The power stage can be divided into a dc-dc converter, an ac-dc rectifier, a dc-ac inversion and an ac-ac cycloconversion. A well-regulated output voltage is produced by a control stage, regardless of the variations in the input voltage and load current [1].

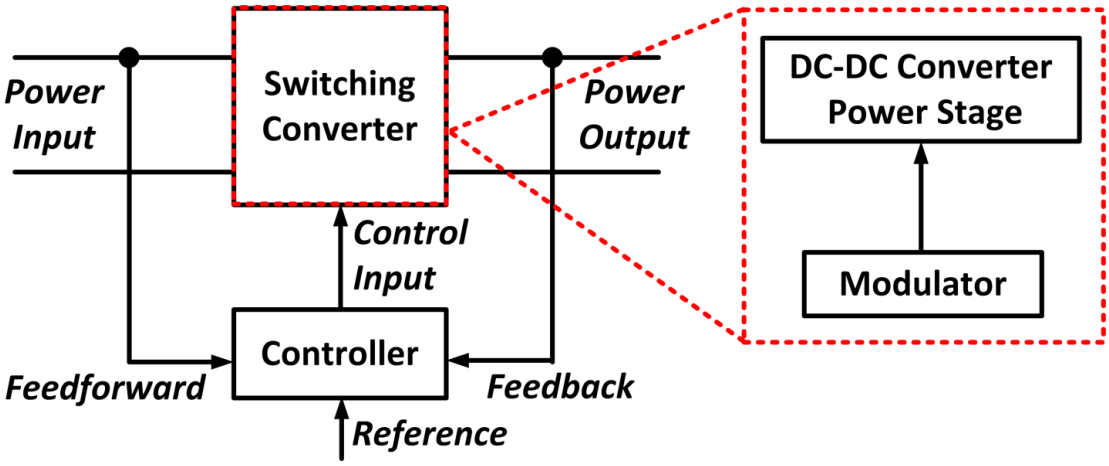


Figure 1.1 Structure of Power Stage and Control

Pulse-width modulation (PWM) dc-dc converters are widely used in many applications, including power supplies for personal computers, telecommunication equipment, aerospace power systems, etc. The PWM technique is effective in controlling the actual power flow by the

duty cycle. The static conversion ratio M (D) is defined as the ratio of output voltage Vo to input voltage Vin as the function of duty cycle D:

$$M(D) = \frac{Vo}{Vin} \tag{1.1}$$

According to the inductor current, there are three types of conduction mode, continuous conduction mode (CCM), discontinuous conduction mode (DCM) and boundary conduction mode (BCM).

In continuous conduction mode, the current in the energy transfer inductor never goes to zero between switching cycles. In discontinuous conduction mode, the current goes to zero during part of the switching cycle. Boundary conduction mode is the boundary mode between continuous conduction mode and discontinuous conduction mode. When the current goes to zero, it immediately increases and the next switching cycle begins.

Buck, boost and buck-boost converters are regarded as three commonly-used PWM dc-dc converters. Cuk, single-ended primary inductance (SEPIC) converter and flyback converters can be regarded as the buck-boost derived converters. The static conversion ratio of a cuk converter is the same as the one of a buck-boost converter. The static conversion ratio of a SEPIC converter has the same amplitude as the one of a buck-boost converter, but with an inverted polarity. The static conversion ratio of a flyback converter should be modified with the turns ratio [3]-[5].

The static conversion ratios of buck, boost and buck-boost converters in continuous conduction mode are listed in Table 1.1. The simplified circuits of these three converters as well as the plots of their static conversion ratio versus duty cycle are shown in Figure 1.2.

Table 1.1 Summary of the static conversion ratios of CCM buck, boost and buck-boost PWM dc-dc converters

Converter	M (D)
Buck	D
Boost	$\frac{1}{1-D}$
Buck-Boost	$\frac{-D}{1-D}$

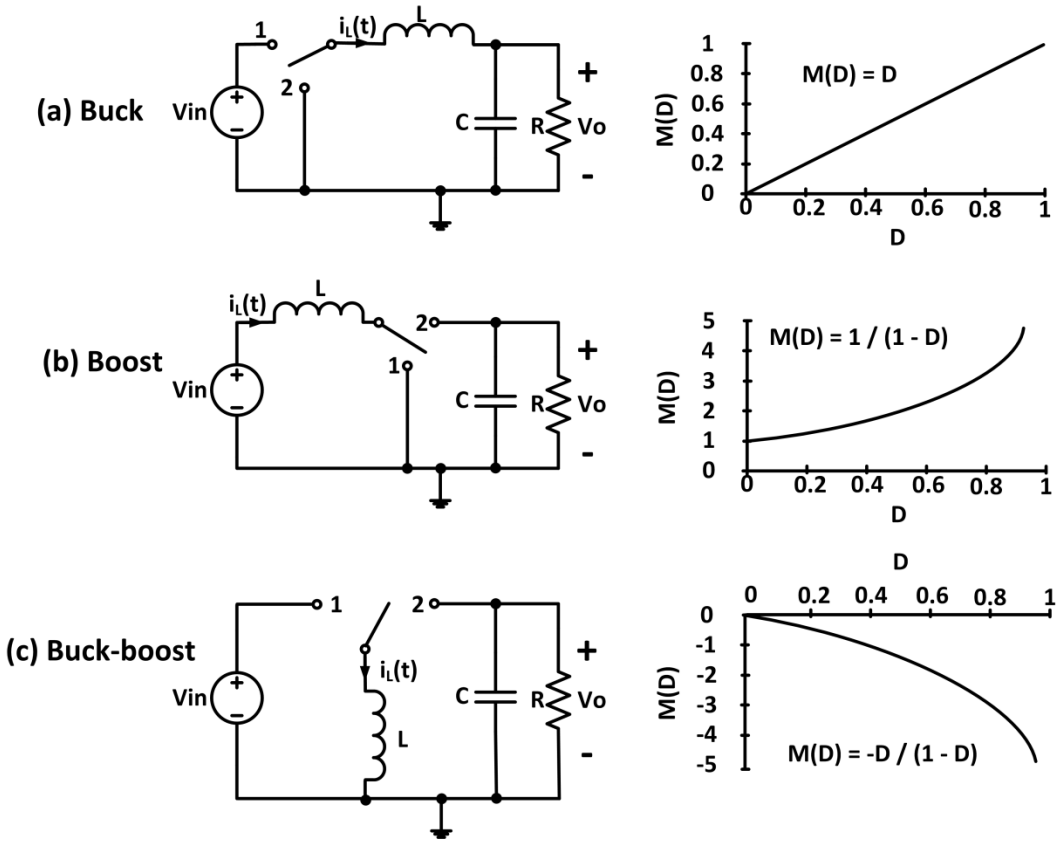


Figure 1.2 The simplified circuits and the plots of static conversion ratio versus duty cycle in continuous conduction mode: (a) buck (b) boost (c) buck-boost

For the conventional modulator used in Figure 1.1, a control signal Vc is compared with a saw-tooth ramp with constant frequency and constant amplitude. The schematic of the conventional modulator is shown in Figure 1.3.

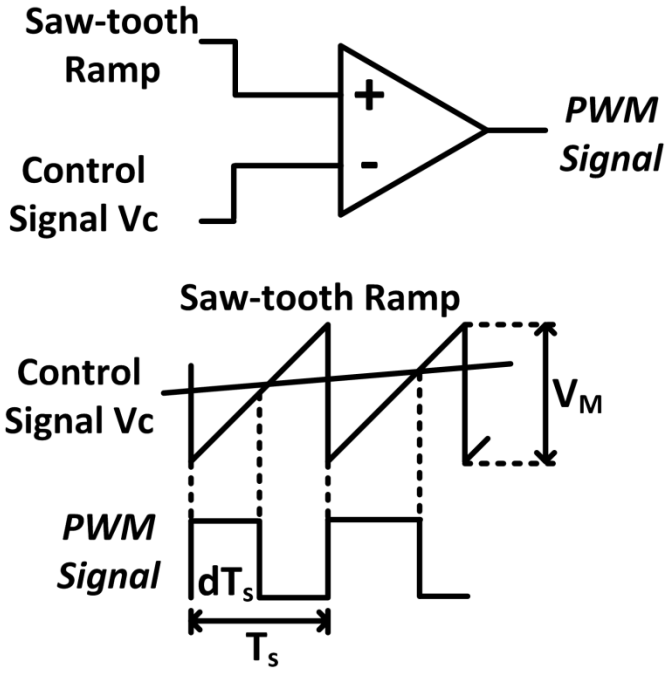


Figure 1.3 Schematic of a conventional modulator

V_M represents the constant amplitude of the saw-tooth ramp. The duty cycle D is determined by Vc as:

$$D = \frac{Vc}{V_M}, \quad 0 \le Vc \le V_M \tag{1.2}$$

Vo(Vc) represents the expression for output voltage Vo as the function of control signal Vc. Once (1.2) is substituted into Table 1.1, the Vo (Vc) expressions for CCM buck, boost and buck-boost PWM dc-dc converters are summarized in Table 1.2.

Table 1.2 Summary of Vo (Vc) expressions for CCM buck, boost and buck-boost PWM dc-dc converters

Converter	Vo(Vc)
Buck	$Vc \cdot \frac{Vin}{V_M}$
Boost	$\frac{Vin}{1-\frac{Vc}{V_M}}$
Buck-Boost	$\frac{-Vin \cdot \frac{Vc}{V_M}}{1-\frac{Vc}{V_M}}$

Based on Table 1.2, there is a high large-signal control-to-output nonlinearity in CCM boost and buck-boost converters when Vin and Vm are fixed.

With feedback control, the output follows the reference signal. In other words, the feedback control helps to realize a large-signal control-to-output linearity. One example would be the LEDs linear dimming as shown in Figure 1.4. A boost converter works as the power stage. The output current, which controls the dimming of LEDs, is proportional to the output voltage. A voltage mode control is used to make the output voltage tracing the reference signal.

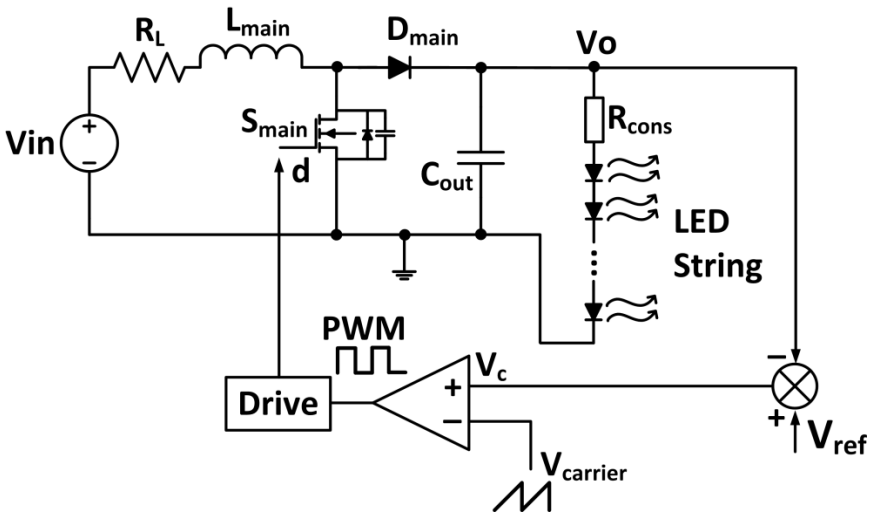


Figure 1.4 The diagram of LEDs linear dimming with a boost converter and feedback control

The control gain Gc is defined as the ratio of the output voltage Vo to the control signal Vc. The small-signal control gain Gc' is defined as differentiating the output voltage Vo with respect to the control signal Vc. In the plot of Vo versus Vc, Gc' represents the dVo / dVc slope. The reason that open loop control cannot replace feedback control is mainly due to the high nonlinearity of this small-signal control gain in the CCM boost converter. For example, if Vin = 20 V and Vm = 5 V, the ratio of winding resistor R_L to load resistor R is 0.005, the plot of Vo versus Vc is shown in Figure 1.5 as the red line. When Vc = 3.7 V, Vo = 71 V; when Vc = 4 V, Vo = 89 V. A small incremental change in control signal ΔVc = 0.3 V would lead to significant incremental change in the output voltage ΔVo = 18 V. Thus, the feedback control helps to prevent the over regulation and saves LEDs.

Another potential problem is due to the negative small-signal control gain. It is manifested as output decreasing when control signal increasing. The feedback control helps to form a negative feedback system. When the power stage enters the negative small-signal control gain

region, the whole control loop becomes positive. The noise and perturbation can no longer be mitigated but amplified. This would lead to instability for the whole system.

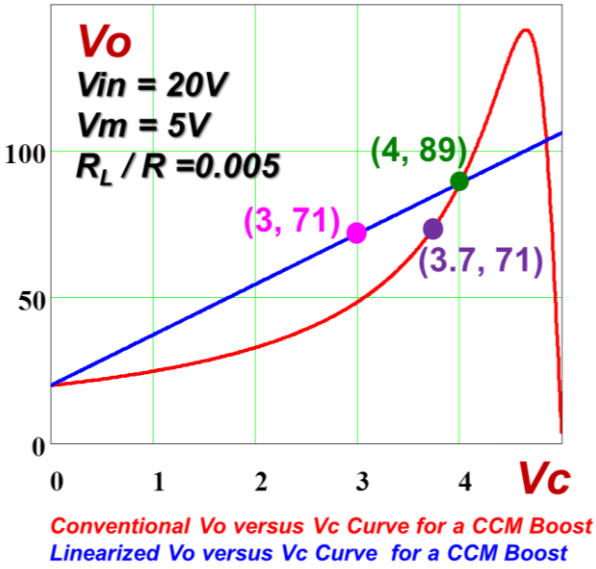


Figure 1.5 Conventional and Linearized Vo versus Vc curves for a CCM boost converter

If a large-signal control-to-output linearity can be established in a CCM boost converter, the open loop control would not suffer from the high nonlinearity of the small-signal control gain; and the output voltage can be predicted by control voltage. This brings a possibility to operate a CCM boost converter by open loop control. For example, if the linearized Vo versus Vc curve is as the blue line shown in Figure 1.5, the Vo = 71 V corresponds to Vc = 3 V. There is 1 V margin for Vc to adjust Vo from 71 V to 89 V. The reduced dVo / dVc slope also helps to mitigate the over regulation problem. Based on the linearization, the open loop control can achieve the LEDs linear dimming. The control strategy is simplified, as the output voltage can be predicted and directly controlled by the control signal. The design procedure is also simplified, which saves the small-signal analysis and compensator design for feedback control. With careful

design, the negative small-signal control gain would be excluded within the control signal range, which prevents the instability.

1.2 Review of Linearization Methods and Contributions by thesis work

Due to the drawbacks of the large-signal control-to-output nonlinearity mentioned above, various nonlinear control schemes have been proposed and discussed for linearization [7]-[25]. Typical linearizing methods can be divided into feedback control and open loop linearization. When designing the feedback control, it necessitates the linearization at an operation point to construct a small-signal model [8]-[27]. The state-space average approach [28]-[29] and the PWM switch model [30]-[31] are commonly used methods. The open loop linearization establishes an inverse nonlinearity in modulators to compensate for the nonlinearity in power stages [33]-[43].

A current-modulated-ramp PWM generator is introduced in [6]. The schematic is shown in Figure 1.6.

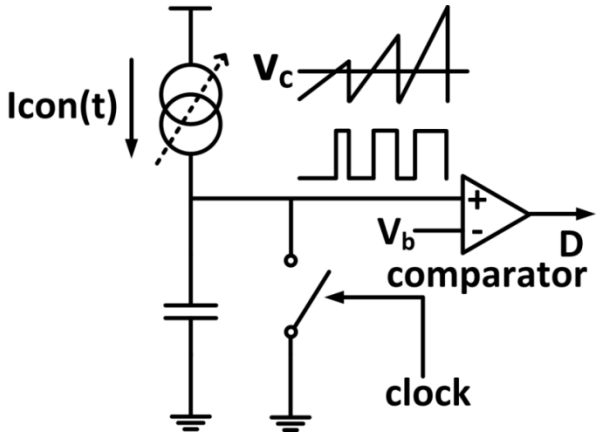


Figure 1.6 Current-modulated-ramp PWM generator

A variable current source Icon works as the control signal. A capacitor is charged by Icon and discharged with period Ts. The capacitor voltage Vc(t) can be expressed as:

$$Vc(t) = \frac{Icon}{C} \cdot t \tag{1.3}$$

Where C is the capacitor and t is time.

The capacitor's voltage becomes a constant-frequency variable-amplitude saw-tooth ramp controlled by Icon. The ramp is compared with a constant bias voltage Vb. The duty cycle is determined as:

$$D = 1 - \frac{Vb \cdot C}{Icon \cdot Ts} \tag{1.4}$$

A nonlinear relationship is established between Icon and D. When substituting (1.4) into Table 1.3, and define H as the control gain from Vo to Icon:

$$H = \frac{Vo}{Icon} \tag{1.5}$$

The expressions of H for CCM buck, boost and buck-boost PWM dc-dc converters are summarized in Table 1.3.

Table 1.3 The summary of control gain based on the modulated-ramp PWM generator

Converter	Control gain H
Boost	$\frac{V_{in}T}{V_b C}$
Buck-Boost	$-\frac{V_{in}T}{V_b C}$
Buck	$\frac{V_{in}V_b C}{I_{con}^2 T}$

The large-signal control-to-output linearity is established in the CCM boost and buck-boost converters. However, the control gain is dependent on the input voltage. If the input voltage varies, the control gain cannot maintain constant. Also, the large-signal control-to-output linearity originally existed in buck converter is changed into nonlinearity by applying this method.

Feedforward compensation is widely used in buck and buck-derived converters to reduce the impact from input to output. The amplitude of the saw-tooth ramp is proportional to the input voltage [34]-[37]. However, it reveals that varying the amplitude of the saw-tooth ramp cannot be directly applied to all converters, such as the boost converter [38].

A feedforward pulse width modulator is introduced in [39]. The static conversion ratio is divided into numerator P(D) and denominator Q(D) as functions of duty cycle D, as shown in (1.6):

$$\frac{Vo}{Vin} = M(D) = \frac{P(D)}{Q(D)} \tag{1.6}$$

(1.6) can be rewritten as:

$$Vc \cdot Q(D) - \frac{Vin}{A} \cdot P(D) = 0 \tag{1.7}$$

Where it's assumed that Vc = Vo / A and A is a constant.

Based on (1.7), P(D) and Q(D) can be implemented by integrator and clock:

$$Vc \cdot Q(t/Ts) - \frac{Vin}{A} \cdot P(t/Ts) = 0 \tag{1.8}$$

Where both Q(t / Ts) and P(t / Ts) are constructed by building blocks.

To better illustrate this method, a CCM boost converter is taken as an example.

Based on Table 1.1 and (1.8), there is:

$$Vc \cdot Q(1-t/Ts) - \frac{Vin}{A} \cdot 1 = 0 \tag{1.9}$$

The detailed implementation is shown in Figure 1.7. The building block of integrator with constant-frequency external clock is shown in red block.

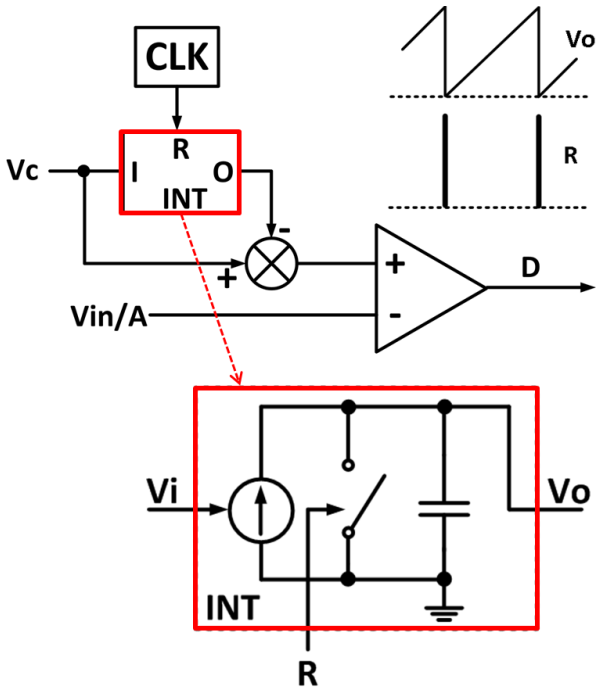


Figure 1.7 Implementation of the feedforward pulse width modulator for a CCM boost converter

If the integrator time constant Ti equals to the switching period Ts, there is:

$$Vc \cdot (1-D) - \frac{Vin}{A} \cdot 1 = 0 \tag{1.10}$$

If loss and parasitic components are negligible, (1.10) leads to:

$$Vo = A \cdot Vc \tag{1.11}$$

However, if the integrator time constant Ti cannot exactly match the switching period Ts, there would be:

$$Vo = AVc\frac{Ts}{Ti} \cdot \frac{Vin}{AVc(Ts/Ti - 1) + Vin} \tag{1.12}$$

In other words, this method relays on the match between the integrator time constant Ti and the switching period Ts. If Ti matches Ts, a constant control gain can be obtained. Otherwise the output voltage would be affected by both input voltage and the mismatch ratio between Ti and Ts.

In the thesis, a self-oscillating unified linearizing (SOUL) modulator is introduced to achieve a large-signal control-to-output linearizing method with a constant control gain. This method provides unified linearization format for various PWM dc-dc converters, such as buck, boost and buck-boost converters. The feedforward is employed to mitigate the impact from line voltage and help to maintain a constant control gain. Because of the self-oscillation mechanism, no external clock is needed. Aiming at the impact from parasitic components and loss, the optimization design of control gain is analyzed to exclude the negative small-signal control gain within the entire control signal range. Finally, experimental results verify the good large-signal control-to-output linearization.

1.3 Thesis Outline

The thesis is structured as follows:

In Chapter 1, the large-signal control-to-voltage nonlinearity in a CCM boost converter is first reviewed. The reasons why open loop control based on the conventional modulator cannot

replace feedback control are explained. Two open loop linearizing methods are reviewed and commented. The Self-oscillating unified linearizing modulator is introduced. The accomplishments and contributions in the thesis work are briefly summarized.

In Chapter 2, the principle of SOUL modulator is first introduced. Three basic building blocks and their detailed implementations are explained. How to design the optimized control gain to prevent the negative small-signal control gain within the entire control signal range is discussed. A prototype is built to verify the linearizing performance.

In Chapter 3, future work is discussed. The small-signal control-to-output transfer function is derived based on this SOUL modulator. It shows some unique characteristics compared with the small-signal control-to-output transfer function based on the conventional modulator. The feedback loop design and the benefits of dynamic performance based on the SOUL modulator are discussed.

Chapter 2. Self-Oscillating Unified Linearizing Modulator

2.1 Principle of Self-Oscillating Unified Linearizing (SOUL) Modulator

A diagram of SOUL modulator is shown in Figure 2.1. No feedback is employed. Feedforward is introduced and there is Vin* = Vin / K. K is a constant number and determined by the ratio of R1 and R2. The objective of SOUL modulator is to establish a large-signal control-to-output linearity with a constant control gain K in various PWM dc-dc converters operating in continuous conduction mode. Thus, there is:

$$K \cdot Vc = Vo \tag{2.1}$$

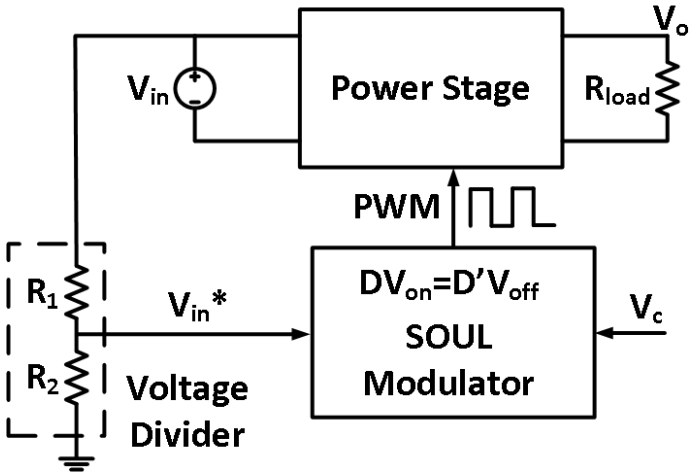


Figure 2.1 Diagram of SOUL Modulator

Take a CCM boost converter as an example.

The static conversion ratio of a CCM boost converter is:

$$\frac{Vo}{Vin} = \frac{1}{1-D} \tag{2.2}$$

It can be rewritten as:

$$Vin \cdot (D + D') = Vo \cdot D' \tag{2.3}$$

Since Vin* = Vin / K and it is expected to have Vc = Vo / K, (2.8) can be rearranged as:

$$Vin^* \cdot D = (Vc - Vin^*) \cdot D' \tag{2.4}$$

Define Von = Vin*, Voff = Vc – Vin*. A unified large-signal control-to-output linearizing format can be expressed as:

$$Von(Vin^*, Vc) \cdot D = Voff(Vin^*, Vc) \cdot D' \tag{2.5}$$

The duty cycle is determined by:

$$D = \frac{Voff}{Von + Voff} = \frac{Vc - Vin^*}{Vc} \tag{2.6}$$

Substitute (2.5) back into (2.2):

$$\begin{aligned} Vo &= \frac{1}{1-D} \cdot Vin = \frac{1}{1 - \dfrac{Vc - Vin^*}{Vc}} \cdot Vin \\ &= \frac{Vc}{Vin^*} \cdot Vin = Vc \cdot \frac{Vin}{Vin^*} \\ &= Vc \cdot K \end{aligned} \tag{2.7}$$

By this step, the large-signal control-to-output linearity with a constant control gain K is established by SOUL modulator, as shown in Figure 2.2.

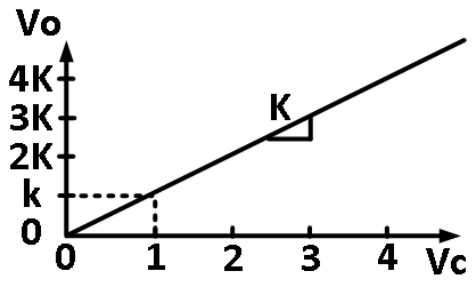


Figure 2.2 The large-signal control-to-output linearity with a constant control gain K

Based on the diagram and example above, a general procedure to design the SOUL modulator is proposed as:

1) *According to the static conversion ratios listed in Table 1.1, reorganize the M(D) into a unified linearization format.*

It can be expressed as:

$$Von(Vin^*, Vc) \cdot D = Voff(Vin^*, Vc) \cdot D' \tag{2.8}$$

Where Von and Voff are functions of Vc and Vin*.

Vin* is the sensed input signal by feedforward, which is proportional to Vin.

Vc is the control signal, which is expected to have the same proportion to Vo as the one from Vin* to Vin:

$$K = \frac{Vin}{Vin^*} = \frac{Vo}{Vc} \tag{2.9}$$

Where K is a constant control gain.

For a SEPIC converter, there is:

$$M = \frac{Vo}{Vin} = \frac{\frac{Vo}{K}}{\frac{Vin}{K}} = \frac{Vc}{Vin^*} = \frac{D}{1-D} = \frac{D'}{D'} \tag{2.10}$$

Rearrange (2.10) into the format of (2.8):

$$Vin^* \cdot D = Vc \cdot D' \tag{2.11}$$

Therefore, there are Von = Vin* and Voff = Vc for a SEPIC converter.

For buck-boost and Cuk converters, there is an inverting polarity in the conversion ratio but it can still use (2.10) and (2.11) if sensed Vin is inverted as (2.12), which can be implemented with an operational amplifier.

$$Vin^* = -\frac{Vin}{K} \tag{2.12}$$

Similarly, for a buck-boost derived isolated converter, such as a flyback converter, Vin* needs to be modified by the turns ratio as:

$$Vin^* = n \cdot \frac{Vin}{K} \tag{2.13}$$

Then it can be grouped into (2.10) and (2.11).

2) *Build a self-oscillating, constant-frequency, variable-amplitude carrier and determine the duty cycle.*

When Von and Voff are determined, they are used to generate the signal Vm:

$$Vm = Von + Voff \tag{2.14}$$

Vm plays two roles in the SOUL Modulator. Firstly, according to (2.8) and (2.14), there is always:

$$Vof\,f = D \cdot Vm \tag{2.15}$$

Thus, Vm is always compared with Voff to determine the duty cycle.

Secondly, a self-oscillating constant-frequency carrier with constant amplitude Vm is generated in the SOUL modulator. Vm and ground are used as two boundaries to determine the shape of carrier.

Either triangular or saw-tooth ramp can be applied to the carrier. When applying the saw-tooth ramp, either leading-edge modulation or trailing-edge modulation can be adopted.

Since the real switching frequency is the same as the self-oscillating frequency, the mismatch between integrator time constant and switching period is avoided.

An example of triangular carrier is shown in Figure 2.3.

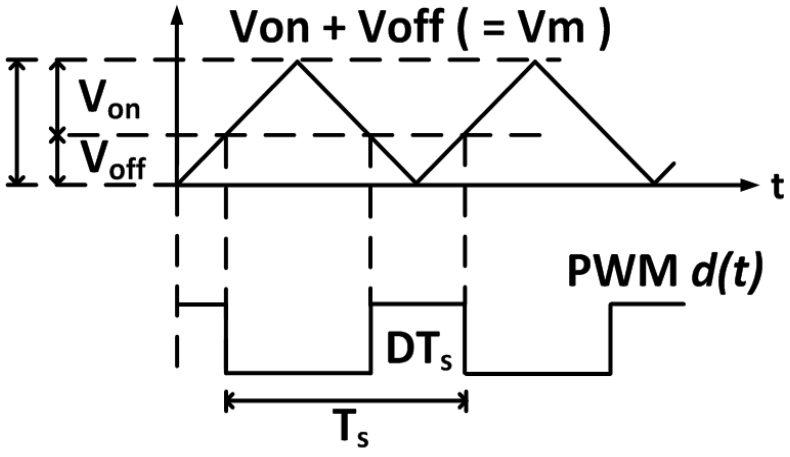


Figure 2.3 A triangular carrier and the determination of duty cycle

The expressions of Vin*, Vc, Von, Voff and Vm in the SOUL modulator for buck, boost, buck-boost and buck-boost derived PWM dc-dc converters are listed in Table 2.1.

Table 2.1 Summary of Vin*, Vc, Von, Voff and Vm in the SOUL modulator for buck, boost, buck-boost and buck-boost derived PWM dc-dc converters

Converter	Vin*	Vc	Von	Voff	Vm
Buck	$\frac{Vin}{K}$	$\frac{Vo}{K}$	$Vin^* - Vc$	Vc	Vin^*
Boost	$\frac{Vin}{K}$	$\frac{Vo}{K}$	Vin^*	$Vc - Vin^*$	Vc
Buck-Boost*	$n \cdot \frac{Vin}{K}$	$\frac{Vo}{K}$	Vin^*	Vc	$Vin^* + Vc$
Unified	$Von \cdot D = Voff \cdot D'$ $Voff = D \cdot Vm$				

* For buck-boost converter and Cuk converter, n = -1; for SEPIC converter, n = 1; for flyback, n = N which is the turns ratio.

2.2 Implementation of SOUL Modulator

There are three basic building blocks in the SOUL modulator, as shown in Figure 2.4.

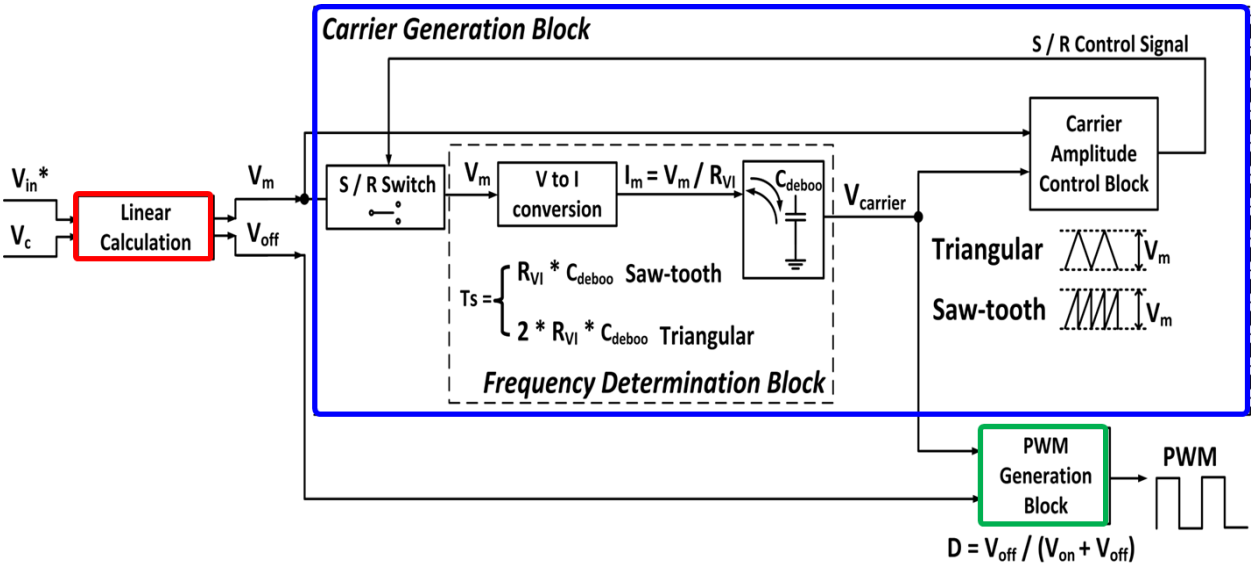


Figure 2.4 Schematic of the SOUL Modulator

First, the operational amplifier (op amp) based summing / subtraction circuits are used to construct Voff and ± Vm based on Vin* and Vc. It's called linear calculation block, as the red box in Figure 2.4.

The second block is called carrier generation block, as the blue box in Figure 2.4. A voltage-to-current conversion transfers the voltage into current to charge the capacitor. This forms the rising slope of carrier. According to the desired shape of carrier, either triangular or saw-tooth ramp, the falling edge of carrier is implemented by discharging the capacitor through either the same current or directly connecting to ground. The capacitor voltage is monitored. The carrier amplitude control block, constructed by comparators, is used to control the amplitude of carrier and control a set / reset (S/R) switch to implement either the rising or falling slopes of the carrier. The self-oscillating is achieved within this block and determines the switching frequency. If the voltage-to-current conversion ratio is defined as R_{VI}, and the capacitance is C_{deboo}, their time constant ($R_{VI} * C_{deboo}$) determines the switching period. The switching period is ($R_{VI} * C_{deboo}$) for the saw-tooth ramp and ($2 * R_{VI} * C_{deboo}$) for the triangular carrier.

The third green block is called PWM generation block. The Voff and capacitor voltage are compared in this block to determine the PWM signal with right duty cycle.

2.2.1 Summing / Subtraction Circuits

There are two basic varieties of summer circuits based on op amp: non-inverting and inverting.

The schematic of the inverting summer circuit is shown in Figure 2.5.

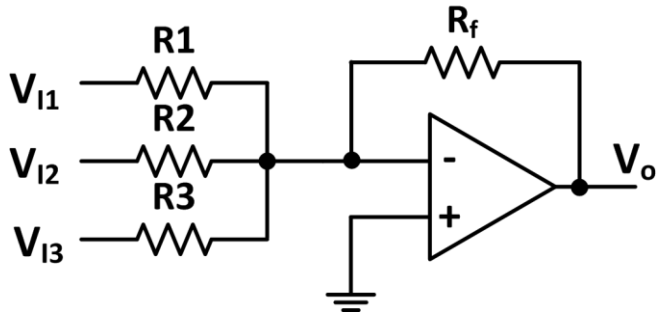


Figure 2.5 Schematic of a inverting summer circuit

For this circuit, there is:

$$Vo = -\frac{R_f}{R1} \cdot V_{I1} - \frac{R_f}{R2} \cdot V_{I2} - \frac{R_f}{R3} \cdot V_{I3} \tag{2.16}$$

The ratio is controlled by Rf and R1~R3. When there is:

$$R1 = R2 = R3 = R_f \tag{2.17}$$

The output can be simplified as:

$$Vo = -(V_{I1} + V_{I2} + V_{I3}) \tag{2.18}$$

The schematic of a non-inverting summer circuit is shown in Figure 2.6.

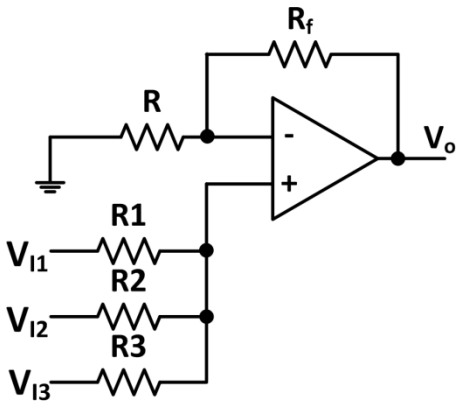


Figure 2.6 Schematic of a non-inverting summer circuit

For this circuit, there is:

$$Vo=(\frac{R2\|R3}{R1+R2\|R3}\cdot V_{I1}+\frac{R1\|R3}{R2+R1\|R3}\cdot V_{I2}+\frac{R1\|R2}{R3+R1\|R2}\cdot V_{I3})\cdot(1+\frac{Rf}{R}) \tag{2.19}$$

The ratio is controlled by Rf and R1~R3. When there is:

$$R1=R2=R3 \tag{2.20}$$

The output can be simplified as:

$$Vo=\frac{1}{3}\cdot(V_{I1}+V_{I2}+V_{I3})\cdot(1+\frac{Rf}{R}) \tag{2.21}$$

And if there is:

$$R_f=2R \tag{2.22}$$

The output can be further simplified as:

$$Vo=(V_{I1}+V_{I2}+V_{I3}) \tag{2.23}$$

The main consideration for the choice of them depends on the phase. It costs two inverting circuits to keep the output's phase the same as input's phase, while one non-inverting circuit is

enough. Therefore, the non-inverting summer circuit is cited. When converting Vm to –Vm, the inverting circuit can be used.

The schematic of a non-inverting summer circuit is shown in Figure 2.6.

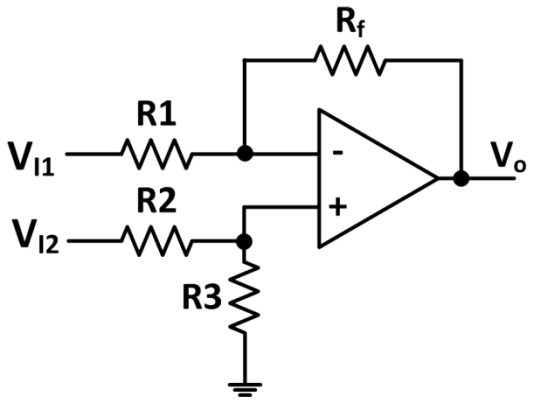


Figure 2.7 Schematic of a subtraction circuit

This circuit can be regarded as: when a signal is applied to one input, the differential amplifier operates as a non-inverting amplifier. When a signal is applied to the other input, it acts as an inverting amplifier.

For this circuit, there is:

$$Vo = -\frac{R_f}{R1} \cdot V_{I1} + \frac{R3}{R2+R3} \cdot (1+\frac{R_f}{R1}) \cdot V_{I2} \tag{2.24}$$

To eliminate the error caused by bias current, it is required:

$$R1 \,||\, R_f = R2 \,||\, R3 \tag{2.25}$$

When there is:

$$R1 = R2, \quad R_f = R3 \tag{2.26}$$

The output can be simplified as:

$$Vo = \frac{R_f}{R1} \cdot (V_{I2} - V_{I1}) \tag{2.27}$$

To further simplify the output, we make:

$$R1 = R_f \tag{2.28}$$

Then we can get:

$$Vo = V_{I2} - V_{I1} \tag{2.29}$$

For all the equations above, it can be concluded that a simple summing or subtraction relationship between input and output can be built if the values of resistors can be well designed.

2.2.2 Deboo Integrator

A Howland current source, which is also known as a deboo integrator, is used to work as the voltage-to-current conversion [44]. The schematic is shown in Figure 2.8. The part in the pink box can be regarded as a negative resistor connected to ground.

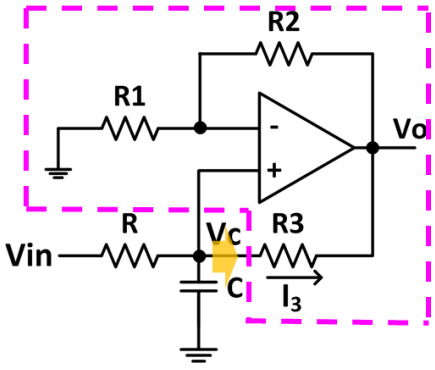


Figure 2.8 Schematic of a deboo integrator

To view the right side from input port and consider the virtual short, there are:

$$\begin{cases} Vo = Vc \cdot (\frac{R2}{R1} + 1) \\ I_3 = \frac{Vc - Vo}{R3} \end{cases} \tag{2.30}$$

Combining the two equations, we can get:

$$I_3 = \frac{Vc}{(-\frac{R1 \cdot R3}{R2})} \tag{2.31}$$

An equivalent negative resistor appears at the denominator. The circuit can be simplified as shown in Figure 2.9:

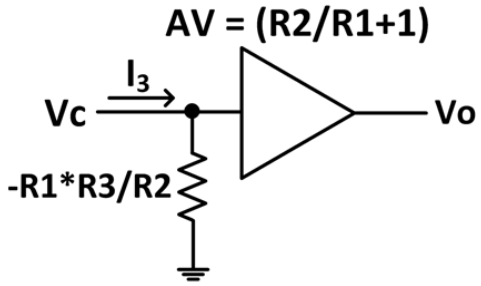


Figure 2.9 Simplified Circuits with a negative resistor

Substitute this simplified circuit back and the whole circuit can be simplified as:

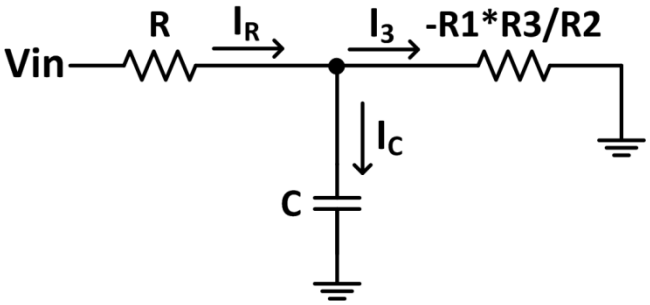


Figure 2.10 The simplified circuit for deboo integrator

According to Kirchhoff's Current Law (KCL), the current going into the capacitor is:

$$I_c = I_R + I_3 = I_3 = \frac{Vin - Vc}{R} + \frac{Vc}{(-\frac{R1 \cdot R3}{R2})} \tag{2.32}$$

If there is:

$$R = \frac{R1 \cdot R3}{R2} \tag{2.33}$$

Then the current can be expressed as:

$$I_c = \frac{Vin}{R} \tag{2.34}$$

According to (2.34), we can conclude that the current going into capacitor depends only on the input voltage Vin and input resistor R. The capacitor voltage can be calculated as:

$$Vc(t) = \frac{I_c}{C} \cdot t = \frac{1}{C} \cdot \frac{Vin}{R} \cdot t = \frac{Vin}{R \cdot C} \cdot t \tag{2.35}$$

According to (2.35), we can select resistor and capacitor to get the carrier waveform with desired frequency.

2.2.3 SR Latch and SPDT

Once the capacitor is charging, the capacitor voltage needs to be monitored. When it reaches the desired amplitude Vm, the carrier amplitude control block gives a control signal to the S/R switch which implements the discharge of capacitor until the capacitor voltage reaches to zero and begins charging again.

A single-pole-double-throw (SPDT) switch is used as the S/R switch. The SPDT switch is a three-port switch, as shown in Figure 2.11. One port (D1) is controlled by a control signal (IN1) and connected to one of the other two ports (S1A or S1B).

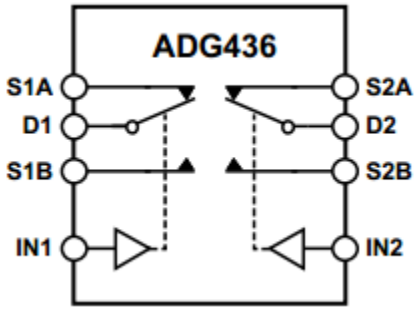
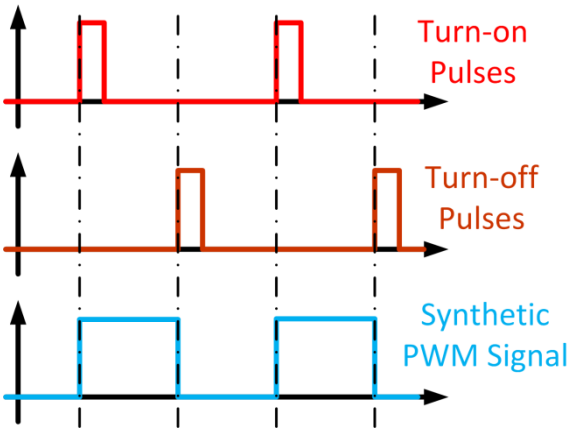


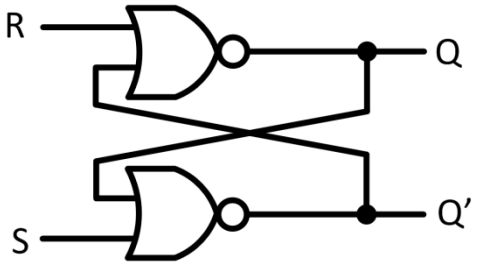
Figure 2.11 Schematic of a SPDT

The requirement for this SPDT switch contains: low off-leakage current to avoid capacitor voltage integration; low on-resistance to mitigate additional voltage drop and to reduce the impact on charging / discharging current; low power dissipation; short rising / falling time and propagation delay; and wide supply voltage range.

Once the capacitor voltage waveform is obtained, it's delivered to a comparator to finish two tasks: (1) compared with Vm and ground to determine the moment for charging or discharging. (2) compared with Voff to generate the PWM signal.

When the capacitor voltage reaches Vm and goes back, the comparator generates a short pulse to indicate it is discharging. However, the pulse is not enough to control the SPDT switch. A set-reset (SR) latch is used to convert these pulses into the control signal for the SPDT. To further shorten the propagation neither delay, two NOR gates are used to construct the SR latch to minimize the propagation delay, as illustrated in Figure 2.12.





SR Latch Operation		
S	R	Action
0	0	No change
0	1	Q = 0
1	0	Q = 1
1	1	Restricted Combination

Figure 2.12 Construction of a SR latch based on NOR gates

2.3 Optimization Design of Control Gain

In a real converter, the loss would not only reduce the efficiency but also affect the static conversion ratio. To simplify the analysis, we use R_L in series with the main inductor to represent the loss in a boost converter.

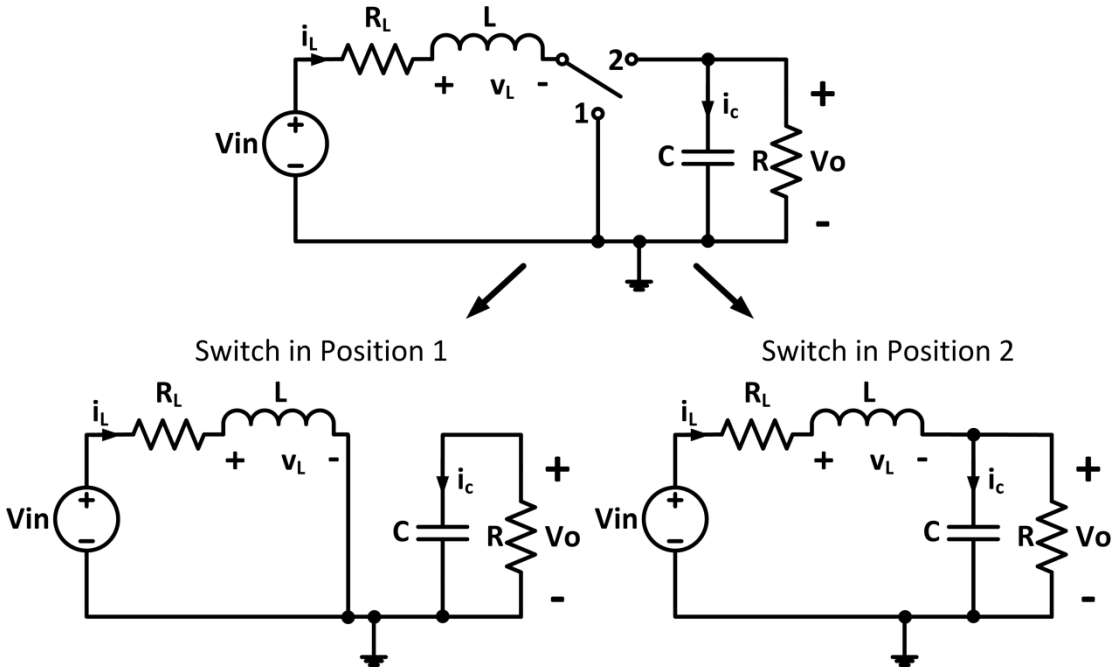


Figure 2.13 Equivalent Circuits during operations

The equivalent circuits for a boost converter during different operation stages are shown in Figure 2.13. When switch is in position 1 and with small ripple approximation, the expressions for inductor voltage V_L and capacitor current i_c are:

$$\begin{cases} v_L(t) = Vin - I_L \cdot R_L \\ i_C(t) = -Vo / R \end{cases} \tag{2.36}$$

When switch is in position 2 and with small ripple approximation, the expressions for inductor voltage V_L and capacitor current i_c are:

$$\begin{cases} v_L(t) = Vin - I_L \cdot R_L - Vo \\ i_C(t) = I_L - Vo / R \end{cases} \tag{2.37}$$

According to the inductor volt-second balance and the capacitor charge balance, there are:

$$\begin{cases} \langle v_L(t) \rangle = D \cdot (Vin - I_L \cdot R_L) + D' \cdot (Vin - I_L \cdot R_L - Vo) = 0 \\ \langle i_C(t) \rangle = D \cdot (-Vo / R) + D' \cdot (I_L - Vo / R) = 0 \end{cases} \tag{2.38}$$

Eliminate I_L and solve for V_O:

$$\frac{Vo}{Vin} = \frac{1}{D'} \cdot \frac{1}{(1 + R_L / D'^2 R)} \tag{2.39}$$

The equation can be rearranged as:

$$M(D, x) = \frac{Vo}{Vin} = \frac{1}{1 - D} \cdot \frac{1}{(1 + \frac{x}{(1-D)^2})} \tag{2.40}$$

Where $x = R_L / R$

According to this equation, the curves of static conversion ratio M(D) versus duty cycle D with different R_L / R can be plotted as shown in Figure 2.14.

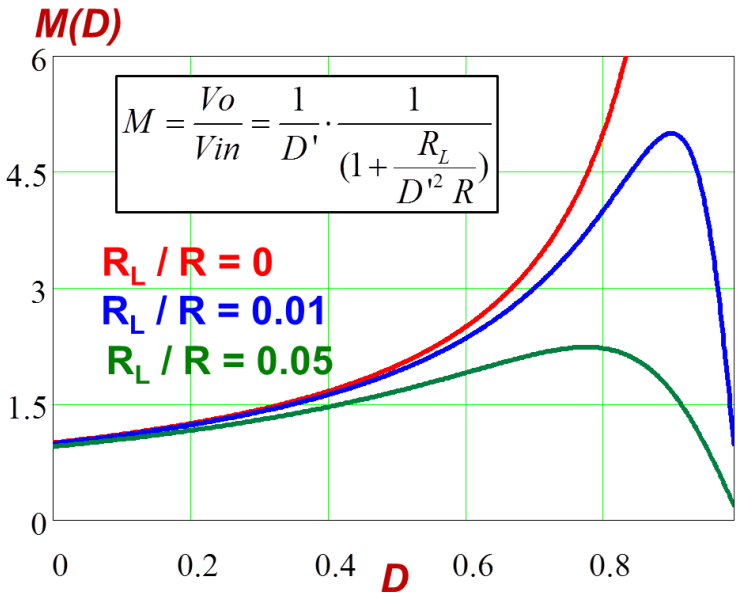


Figure 2.14 Static conversion ratio versus duty cycle with the consideratin of parasitic winding resistance for a CCM Boost converter

According to the three curves plotted above, we can get the conclusions that:

1) There is maximum M(D) when considering the parasitic components and loss.

2) Maximum M(D) is reduced when the ratio R_L / R increases.

3) The negative small-signal control gain appears earlier when the ratio R_L / R increases.

M_{con} stands for the static conversion ratio based on conventional modulator; and M_{SOUL} stands for the static conversion ratio based on SOUL modulator. When (1.2) and (2.6) are substituted into (2.40), there are:

$$M_{con}(Vc, x, Vm) = \frac{1}{[1+\frac{\frac{R_L}{R}}{(1-\frac{Vc}{Vm})^2}]\cdot(1-\frac{Vc}{Vm})} = \frac{1}{(1-\frac{Vc}{Vm})+x\cdot\frac{1}{(1-\frac{Vc}{Vm})}} \tag{2.41}$$

Where $x = R_L / R$

$$M_{SOUL}(Vc, x, K) = \frac{1}{[1+\frac{R_L / R}{(\frac{Vin / K}{Vc})^2}]\cdot(\frac{Vin / K}{Vc})} = \frac{1}{\frac{Vin / K}{Vc}+x\cdot\frac{Vc}{Vin / K}} \tag{2.42}$$

Where $x = R_L / R$ *and* $Vin^* = Vin / K$

To make a quantitative comparison, fix Vin = 50 V, Vm = 5 V and K= 100. Thus, the minimum value for Vc is determined as Vin / K = 0.5 V in SOUL modulator.

Vc is swept from 0 V to 5 V. The Vo versus Vc curves are plotted in Figure 2.15 based on (2.41) and (2.42).

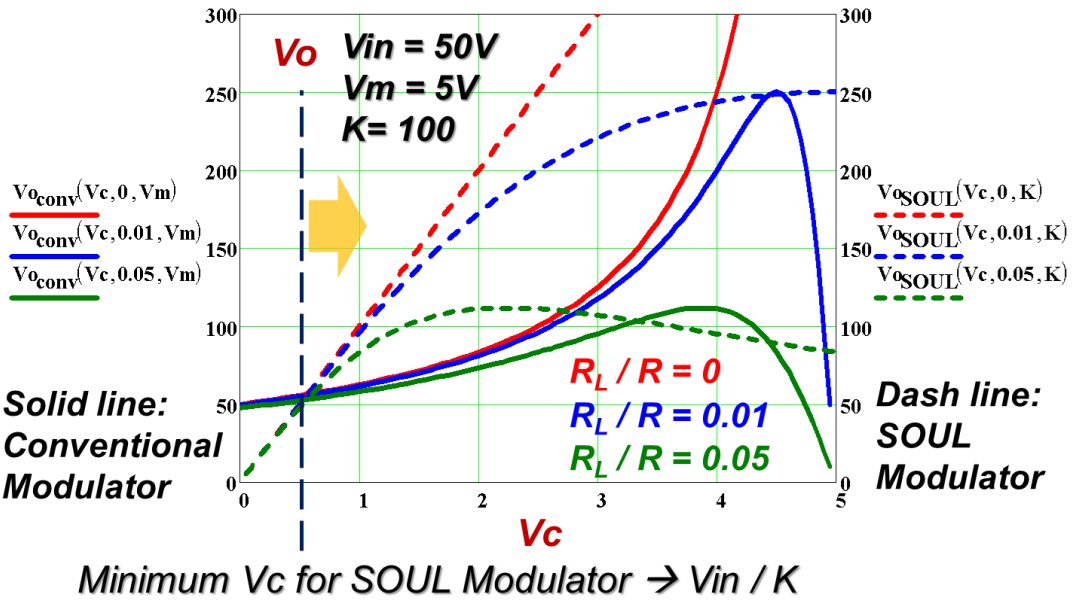


Figure 2.15 The Vo versus Vc curves for conventional and SOUL Modulators

The R_L / R ratio varies from 0 to 0.05. The solid lines stand for conventional modulator cases; and the dash lines stand for SOUL modulator cases.

Comparing the two teams of curves, we can conclude that:

1) The SOUL modulator can maintain the high output voltage in a wider control signal range compared with the conventional modulator.
2) The SOUL modulator can reach the high output voltage faster within a smaller Vc range.
3) The Vo versus Vc curves appear more gradual for SOUL modulator cases while they are sharper for conventional modulator cases.
4) The SOUL modulator brings the negative small-signal control gain earlier compared with the conventional modulator when the ratio R_L / R is high.

To illustrate these characteristics more clearly, the R_L / R = 0.01 case is used as an example. The conventional modulator cannot achieve Vo > 200 V until Vc is in the range from 4 V to 4.5 V; Vo drops significantly after Vc exceeds 4.5 V. The SOUL modulator can achieve Vo > 200 V with Vc ranging from 2 V to 5 V, and maintain more gradual dVo / dVc slope within that range.

However, when R_L / R = 0.05, the benefits mentioned above for SOUL modulator are not obvious and the negative small-signal control gain appears even much earlier.

To better understand these characteristics, the relationships from control signal Vc to duty cycle D are summarized in (2.43).

$$\begin{cases} D_c(v_c) = \dfrac{Vc}{Vm} & Conventional \quad Modulator \\ D_{soul}(v_c) = 1 - \dfrac{Vin^*}{Vc} = 1 - \dfrac{\dfrac{Vin}{K}}{Vc} & SOUL \quad Modulator \end{cases} \tag{2.43}$$

The curves of D versus Vc for Conventional (solid line) and SOUL (dash line) modulators are plotted in Figure 2.16:

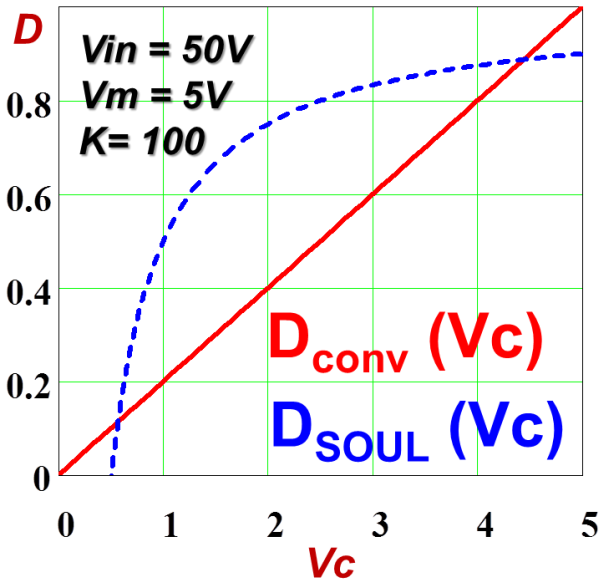


Figure 2.16 The D versus Vc curves for conventional and SOUL Modulators

Based on (2.43) and Figure 2.16, we can conclude that:

1) Compared with the conventional modulator, the control-to-duty nonlinearity in the SOUL modulator. It compensates the duty-to-output nonlinearity in the power stage, and provides a large-signal control-to-output linearity.
2) Except Vc and Vin* in the SOUL modulator, the control gain K also determines the duty cycle.

With a low loss and high efficiency power converter, the SOUL modulator brings benefits that are illustrated above. However, the small-signal control gain appears much earlier in a low efficiency power converter. To provide a clear illustration of small-signal control gain, the derivation from Vo to Vc based on the two modulators are plotted with fixed Vin, Vm and K, as shown in Figure 2.17.

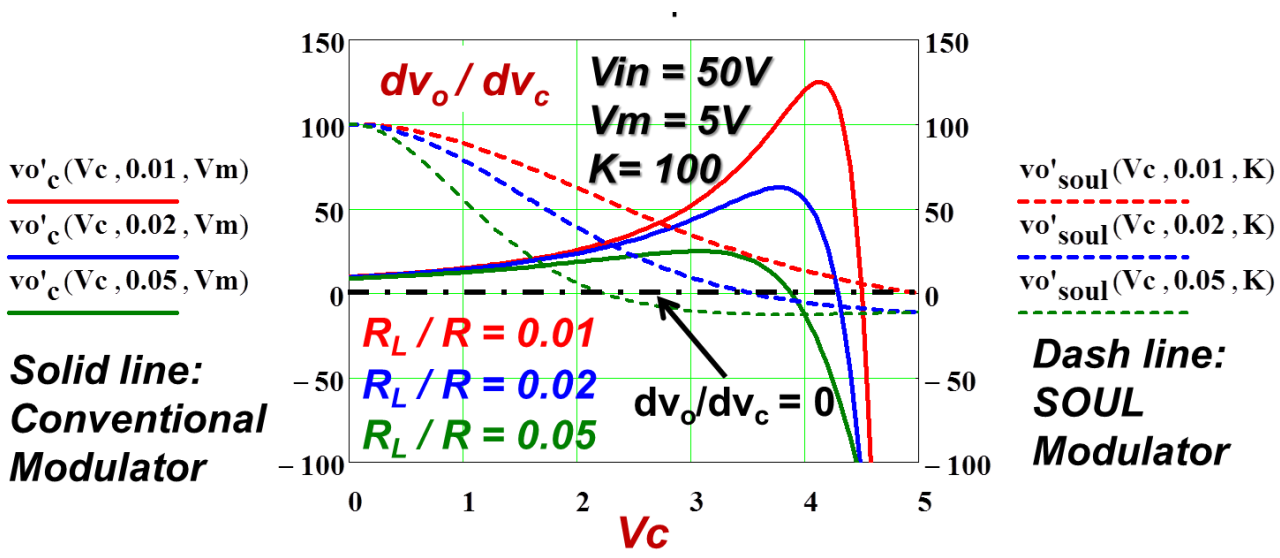


Figure 2.17 The small-signal control gain curves for conventional and SOUL Modulators

The cross point between the small-signal control gain curves and 0 dB indicates the points where small-signal control gain becomes negative. Comparing at the same R_L / R ratio, we can observe that except for the $R_L / R = 0.01$ case, the small-signal control gain curves based on the SOUL modulator touch 0 dB at smaller Vc value.

One way to prevent instability is to limit the maximum value of Vc. However, this method limits the Vc range. Another way is to maintain the Vc range by adjusting K.

Based on (2.42) and assuming that $R_L / R = 0.05$ and Vc ranges from 0V to 5V, K is swept from 30 to 200, as shown in Figure 2.18. One thing worth mentioning is that the minimum Vc is determined by Vin / K. The physical meaning is that the minimum Vin equals to Vo for a boost converter. Therefore, the initial point of Vc is different but all end by 5V.

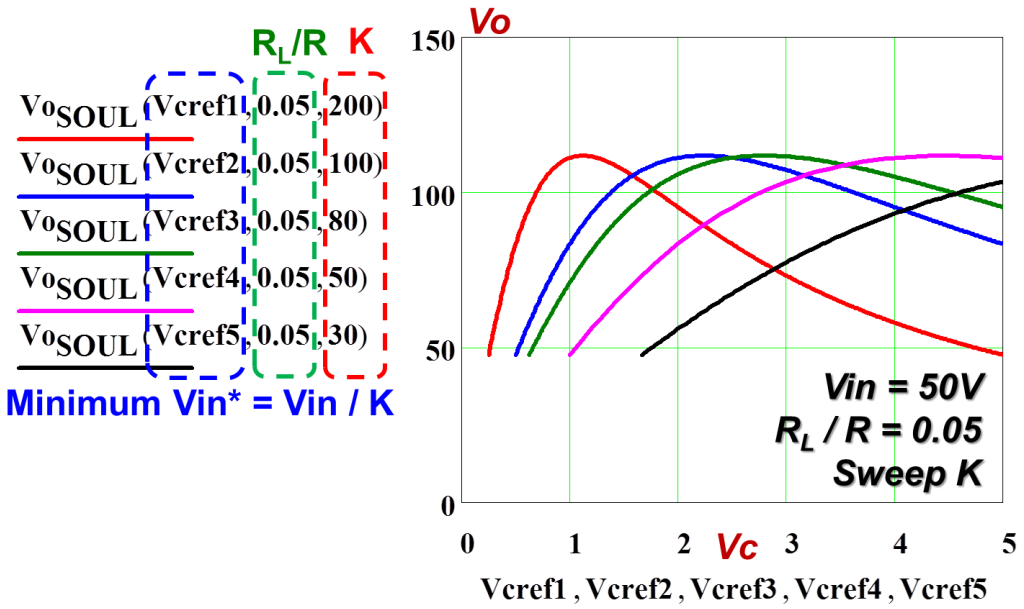


Figure 2.18 The Vc sersus Vo curves with K sweep and R_L / R = 0.05

From Figure 2.18, it can be observed that the small-signal control gain appears at small Vc for K=200 case. On the contrary, a good linearization performance can be obtained when K = 50 and K = 30; and these two curves almost eliminate the negative small-signal control gain within the entire Vc range.

To give a further comparison between these two curves, the small-signal control gain curves are plotted in Figure 2.19. Based on Figure 2.18 and Figure 2.19, it can tell that K = 50 leads to wider Vc and Vo range compared with K = 30. However, the negative small-signal control gain still appears when Vc is close to 5V.

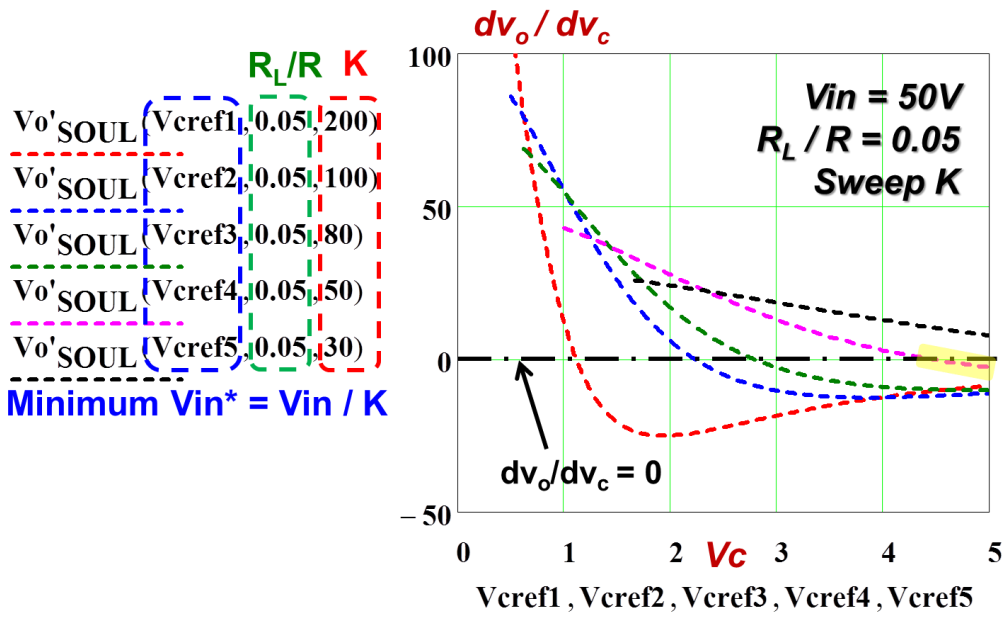


Figure 2.19 The small-signal control gain curves with K swept and R_L / R = 0.05

Is there a way to optimize the value K? To get a general solution, we can solve $V_{o\_soul}'(v_c) \geq 0$ or $V_{o\_soul}'(v_c) = 0$ where Vc reaches the maximum value in its range. Based on (2.42), the expression for V_{o_soul} is:

$$v_{o\_soul}(v_c) = \frac{K \cdot Vc}{\frac{K^2 \cdot Vc^2 \cdot R_L / R}{Vg^2} + 1} \tag{2.44}$$

Differentiating Vo with respect to Vc:

$$v_{o\_soul}'(v_c) = \frac{K}{\frac{K^2 \cdot Vc^2 \cdot R_L / R}{Vg^2} + 1} - \frac{2 \cdot K^3 \cdot Vc^2 \cdot R_L / R}{Vg^2 \cdot (\frac{K^2 \cdot Vc^2 \cdot R_L / R}{Vg^2} + 1)^2} \tag{2.45}$$

When Vg = 50 V, R_L / R = 0.05, Vc = 5 V are substituted to solve for $V_{o\_soul}'(v_c) = 0$, we can get that K = ± 44.72 or 0. Choose the positive integer solution K = 44 for R_L / R = 0.05 case.

For R_L / R = 0.01, 0.02, 0.05 and 1 cases, the optimized K values are solved and listed in Table 2.2. The Vo versus Vc curves with optimized positive integer solutions are plotted in Figure 2.20.

Table 2.2 Optimized K for different R_L / R cases

R_L / R	K
0.01	100
0.02	70.7
0.05	44.72
0.1	31.62

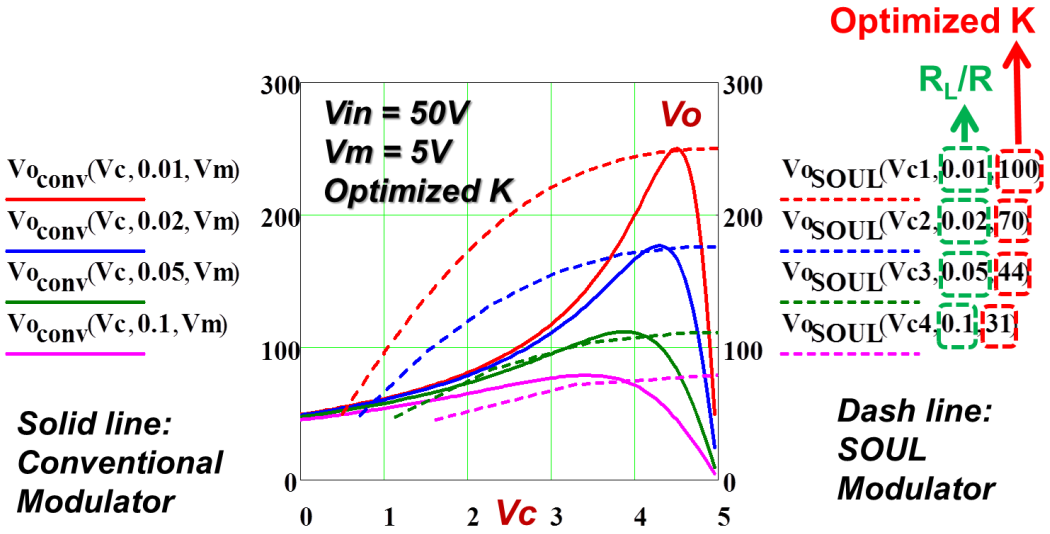


Figure 2.20 Plots of Vo versus Vc curves based on conventional and SOUL modulators with optimized K and different R_L / R ratios

The final question may come to how to use this K optimization method in practice, since the the core loss and copper loss of magnetic components, switching loss and conduction loss of switches, reverse recovery loss and conduction loss of diodes contribute to the total loss. Since the K optimization method is based on the R_L/R ratio, we can first measure and plot the converter's M (D) versus D curve based on a conventional modulator. Next, we can do the curve fitting, compare it with the plots of theoretical calculation, identify the approximate R_L / R value and design K with the estimation R_L / R value.

2.4 Experimental Results

With the theoretical analysis above, a prototypes SOUL modulator and a boost converter are built to verify the theory. The schematics and photos of prototypes are shown in Figure 2.21 and Figure 2.22. When building the boost converter, the high dv / dt loop is formed by switch – diode - output capacitor. Multiple ceramic capacitors should be paralleled with an aluminum electrolytic capacitor to minimize the dv / dt loop and provide a low-impedance path for high-frequency harmonics [45], which effectively reduces the voltage spike at the switching node, as shown in Figure 2.23.

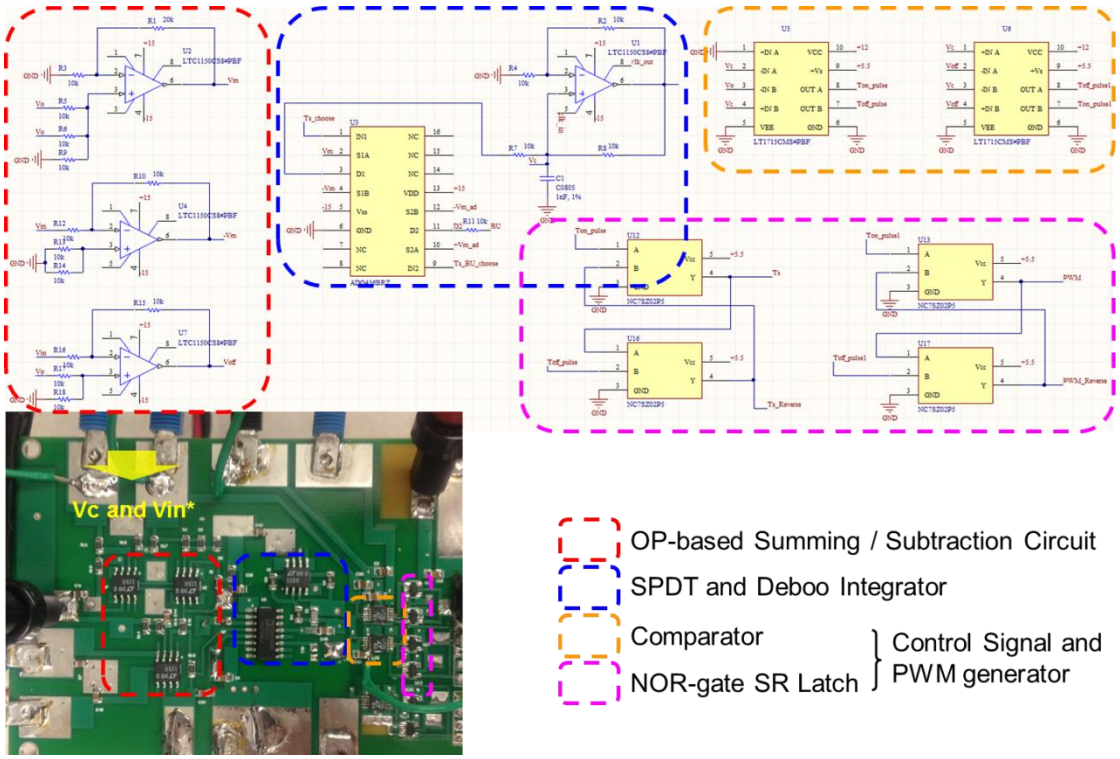
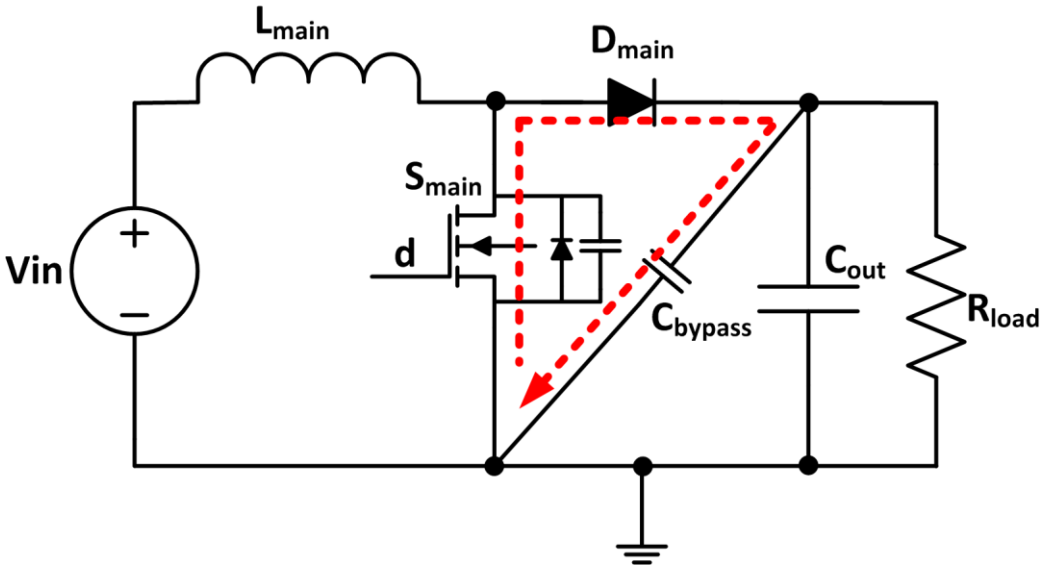
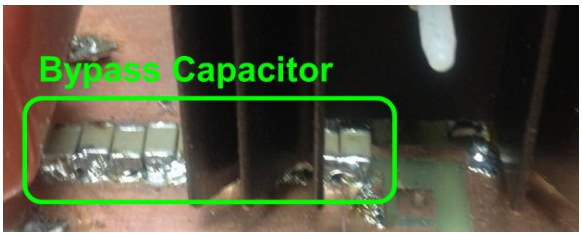
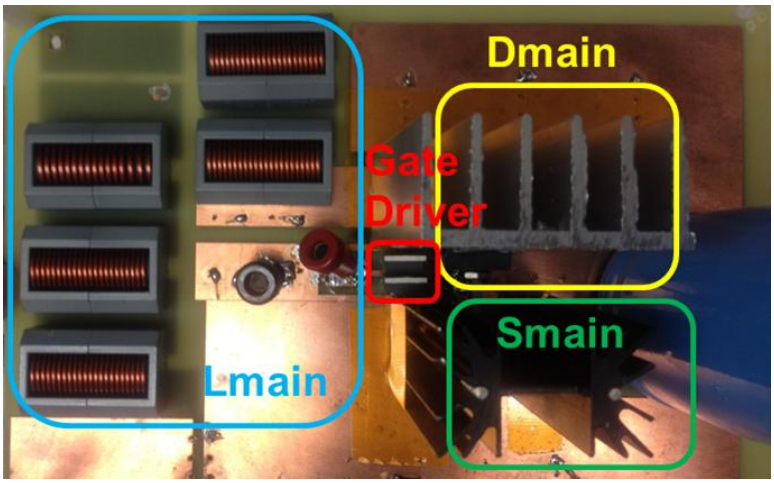


Figure 2.21 The schematic and prototype of SOUL Modulator



(a) High dv / dt loop in the boost converter





(b) The prototype of boost converter

Figure 2.22 The schematic and prototype of boost converter

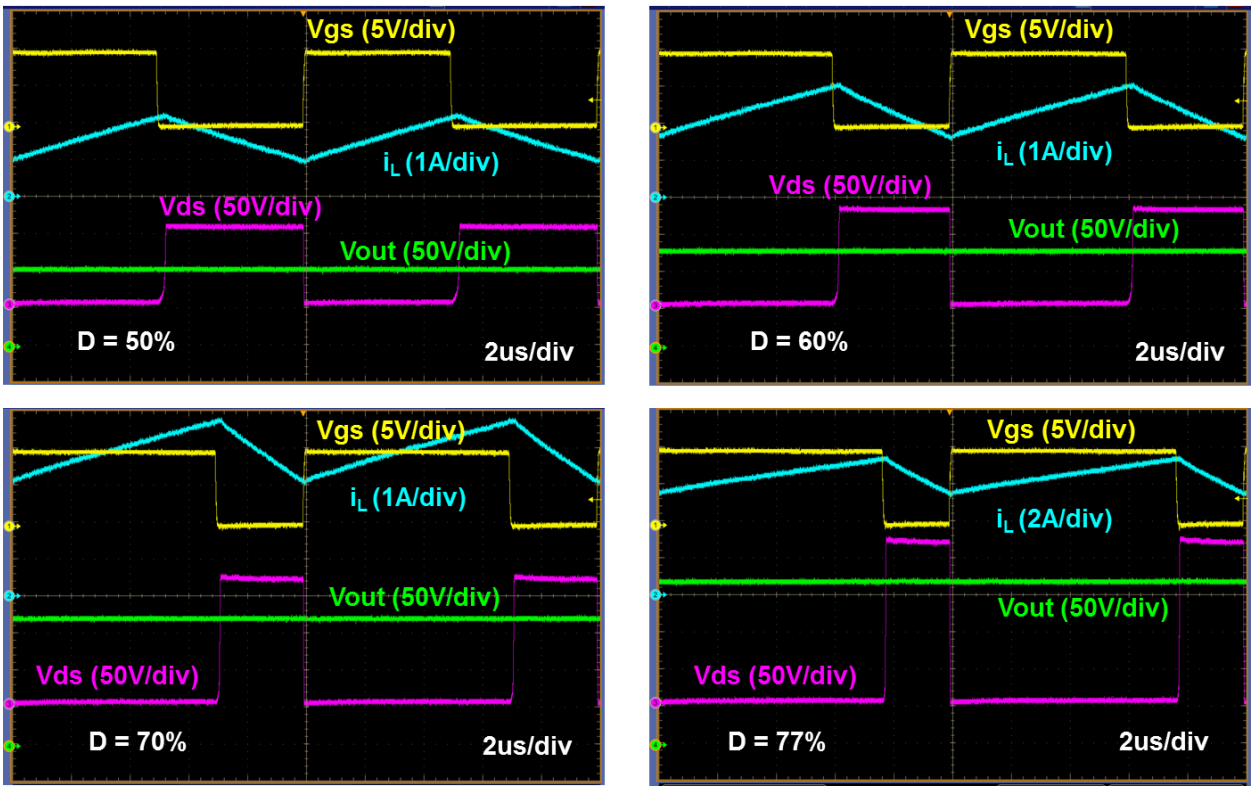


Figure 2.23 Switching waveforms of the prototype boost converter at different operation points when Vin = 50V

The Bill of Material (BOM) for the SOUL Modulator is listed in Table 2.3. The Bill of Material (BOM) for the Boost Converter is listed in Table 2.4.

Table 2.3 BOM for the SOUL Modulator

Component	Part No.	Comment
Op amp	LTC1150CS8#PBF	Used in summing / subtraction circuits
Comparator	LT1715CMS#PBF	Used in carrier generation block.
NOR Gate	NC7SZ02P5	Used to build the SR latch.
SPDT	ADG436BRZ	Used as the S / R switch.
Cap	1% Ceramic 0805	Used in deboo integrator.
Res	0.01% Res 0805	/

Table 2.4 BOM for the boost converter

Component	Part No.	Comment
Smain	STx35N65M5	CoolMos Si MOSFET N-CH 650V 27A TO-247
Diode	C3D10060A	DIODE SCHOT 600V 10A ZREC TO220
Inductor	INDUCTOR POWER 40 uH	
Cout	630 V 0805 ceramic capacitor + 630 V 1 uF film capacitor + 1.1 mF aluminum electrolytic capacitor	
Gate Driver	IXDD514D1	Totem-pole structure Gate Driver

2.4.1 Test of SOUL Modulator

The SOUL modulator is first tested with fixed Vin* and Vc. The switching frequency and duty cycle of the generated PWM signal are recorded in Table 2.5 and compared with the theoretical calculation results, as plotted in Figure 2.24.

Table 2.5 Test Result of SOUL Modulator

Volt Source (V)		MultiMeter Measured Results (V)			Oscilloscope Measured Results		Theoretical Calculation Results	
Vin*	Vc	Vm	-Vm	Von	fs (KHz)	PWM_D	fs (kHz)	PWM_D
1	4.5	9.030	8.990	3.501	93	78.08%	100	77.78%
1	4	8.000	-8.000	2.999	93.1	75.39%	100	75.00%
1	3.5	7.000	-7.000	2.499	93.3	72.12%	100	71.43%
1	3	5.990	-5.990	1.999	93	67.71%	100	66.67%
1	2.5	5.000	-5.000	1.499	93.36	61.27%	100	60.00%
1	2	4.000	-4.000	0.999	93.58	52.06%	100	50.00%
1	1.5	2.995	-2.995	0.499	93.33	36.12%	100	33.33%

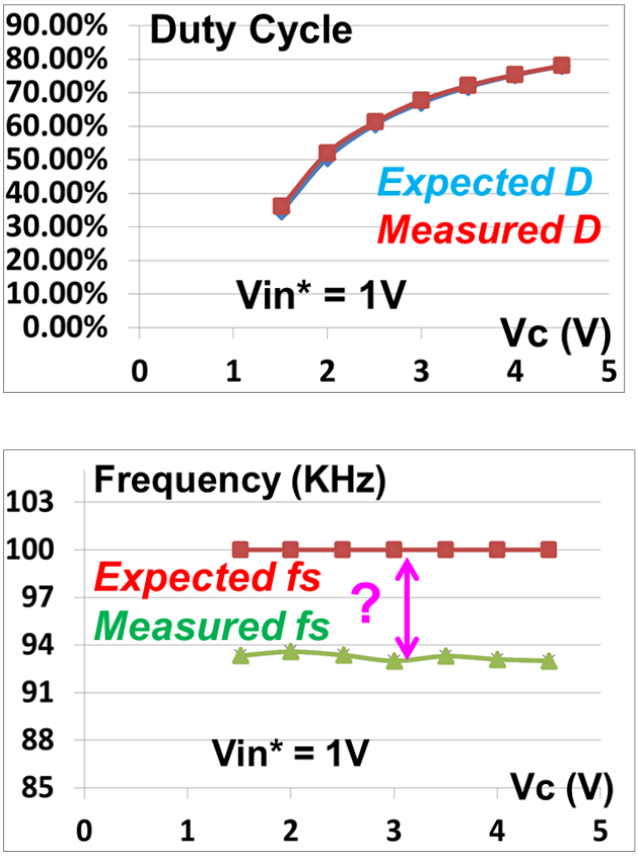


Figure 2.24 Comparison of switching frequency and duty cycle between generated PWM signals and theoretical calculation results

The duty cycle of the generated PWM signal nearly matches the theoretical calculation results. The error is maintained within 1% - 2%, which is acceptable. However there is a nearly 7 kHz frequency difference between experimental and theoretical results. This difference is mainly due to the propagation delay in the components used in the SOUL modulator.

The components introducing delay are marked in Figure 2.25. The function blocks in Figure 2.4 are replaced by detailed implementations. When the triangular carrier reaches Vm, which indicates that the SPDT should be switched to –Vm and discharge the capacitor, the SPDT actually does not execute the command immediately. Instead, the action is done after the delay

time which comes from the propagation delay of comparators, SR latch and SPDT. The equivalent delay chain is shown in Figure 2.26.

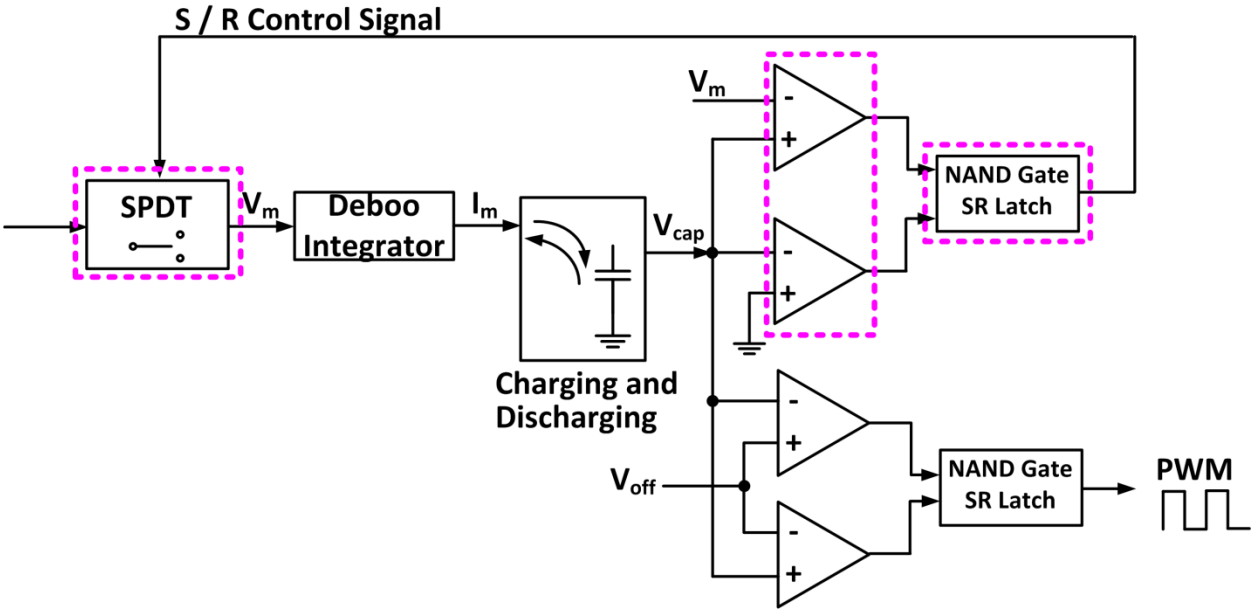


Figure 2.25 Components introducing delay in the SOUL Modulator

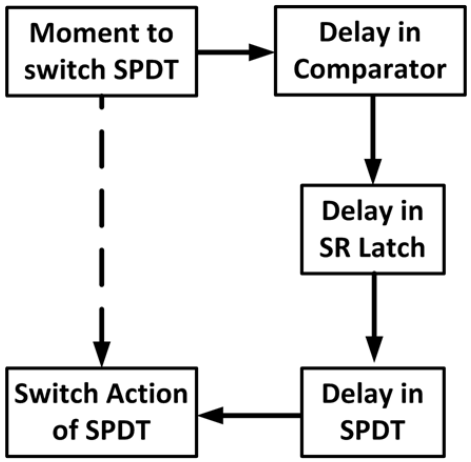


Figure 2.26 Equivalent Delay Chain

The actual waveform is plotted in Figure 2.27. The delay time Δt causes both the triangular carrier's amplitude and switching cycle to be extended. Thus, the switching frequency is reduced.

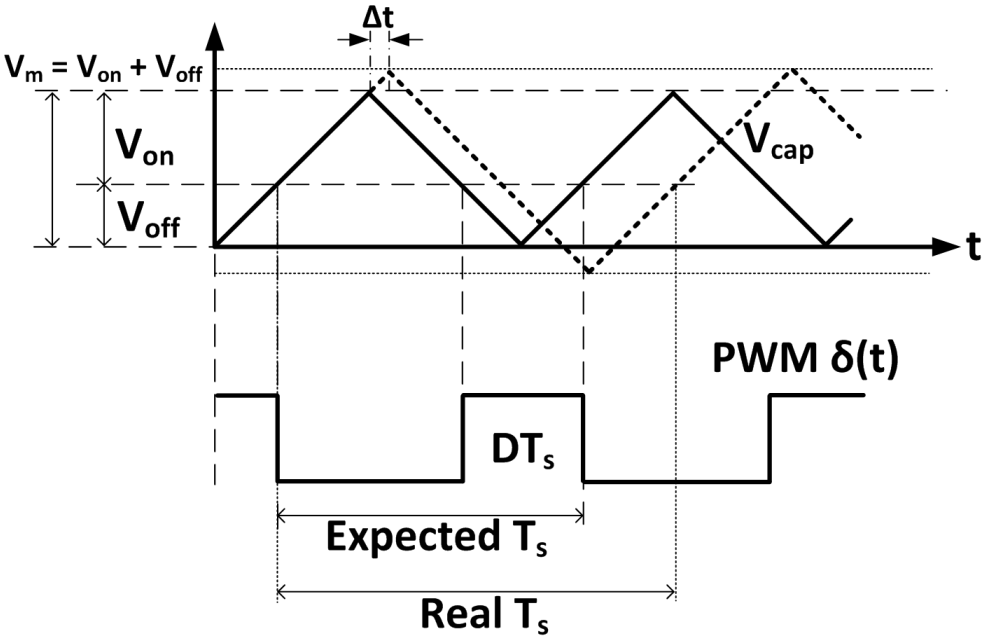


Figure 2.27 Illustration for switching frequency error

One way to correct the switching frequency is to modify the hysteresis boundaries, either reducing the top boundary below Vm or increasing the bottom boundary above zero. However, this method would increase the implementation complexity and is hard to debug. Another way is to change the capacitor value. According to:

$$\frac{Vm}{(t_s / 2)} = \frac{Im}{C} \tag{2.46}$$

Vm and Im should be maintained. Since the measured switching frequency is lower than expected, t_s should decrease which means C should also decrease.

According to the constant Vm and Im, the ratio of C to t_s stays constant. Thus, an experimental estimation is given:

$$\frac{C_1}{t_{s1}} = \frac{C_2}{t_{s2}} \tag{2.47}$$

Now C_1 = 1nF and t_{s1} = 1 / 93 kHz = 10.7 us. If we want t_{s2} = 10 us, C_2 would be around 935 pF. The final debugging result is 910 pF. The switching frequency and duty cycle of the output PWM signal is recorded in Table 2.6 and plotted Figure 2.28.

Table 2.6 Test Result of SOUL Modulator with Modified Capacitance

Volt Source (V)		Oscilloscope Measured Results		Theoretical calculation Results	
Vin*	Vc	fs (KHz)	PWM_D	fs (kHz)	PWM_D
1	4.5	100.3	77.77%	100	77.78%
1	4	100.3	75.15%	100	75.00%
1	3.5	100.3	71.77%	100	71.43%
1	3	100.3	67.29%	100	66.67%
1	2.5	100.4	60.75%	100	60.00%
1	2	100.3	51.20%	100	50.00%
1	1.5	100.2	35.58%	100	33.33%

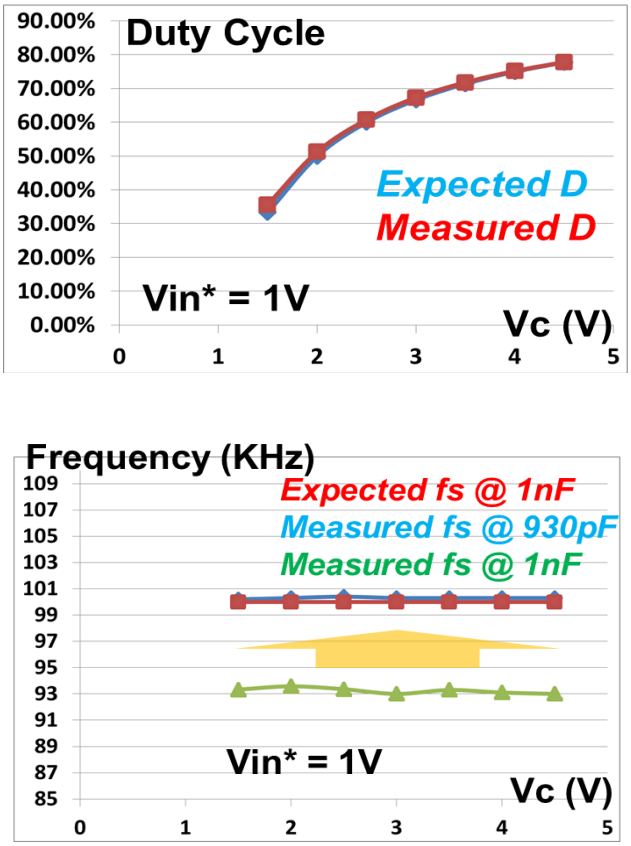


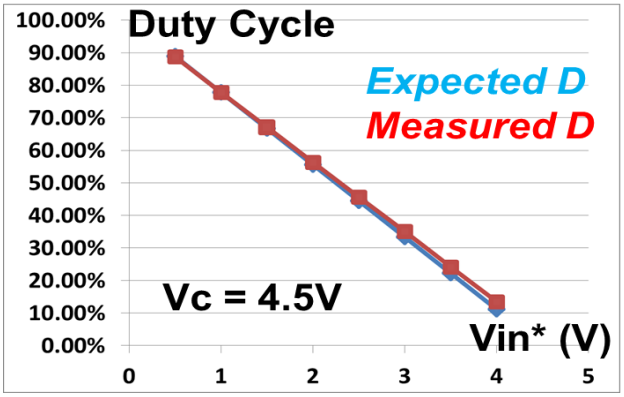
Figure 2.28 Comparison of switching frequency and duty cycle between generated PWM signals and theoretical calculation results with modified capacitance

It is clearly shown that with modified capacitance, both the switching frequency and duty cycle nearly match the expectation results.

With fixed Vc and sweeping Vin*, the switching frequency and duty cycle of the generated PWM signal is recorded in Table 2.7 and plotted in Figure 2.29. It's shown that there is a good match between experimental results and theoretical calculation results.

Table 2.7 Test Result of SOUL Modulator with fixed Vc

Volt Source (V)		Oscilloscope Measured Results		Theoretical calculation Results	
Vin*	Vc	fs (KHz)	PWM_D	fs (kHz)	PWM_D
4	4.5	100.3	13.51%	100	11.11%
3.5	4.5	100.3	24.18%	100	22.22%
3	4.5	100.3	35.06%	100	33.33%
2.5	4.5	100.3	45.62%	100	44.44%
2	4.5	100.3	56.34%	100	55.56%
1.5	4.5	100.2	67.13%	100	66.67%
1	4.5	100.2	77.78%	100	77.78%
0.5	4.5	100.3	88.73%	100	88.89%



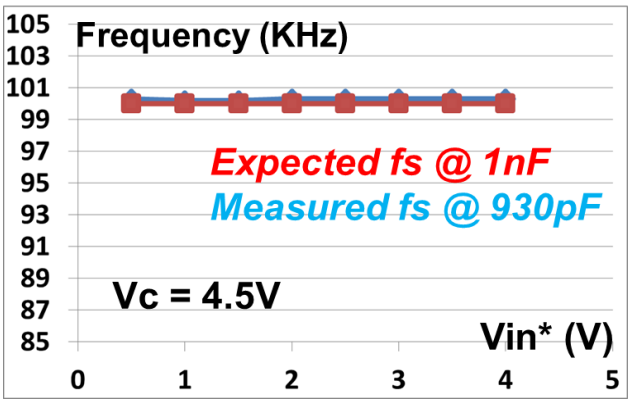


Figure 2.29 Comparison of switching frequency and duty cycle between generated PWM signals and theoretical calculation results with fixed Vc

2.4.2 Verification of Linearization Performance

The modified SOUL modulator is combined with a boost converter to test the linearization performance. The power stage's M(D) versus D curve is first plotted to predetermine the K's value.

The red diamond dots are measured results with Vin fixed at 50 V. The theoretical curves with different R_L / R ratios are also plotted and compared. The R_L / R ratio of this boot prototype is within 0 to 0.01. According to the analysis above, K is chosen 50 to achieve good linearization when Vc varies from 0 V to 5 V.

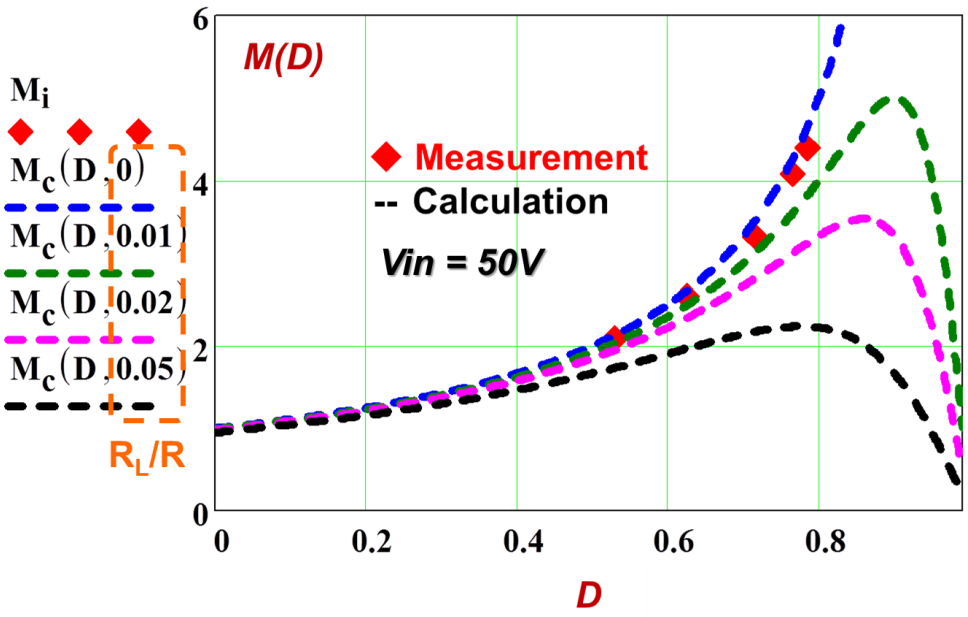


Figure 2.30 The comparison of M(D) versus D between the prototype boost converter and calculation results

Since the SOUL modulator is designed based on static conversion ratio, a triangular control signal Vc whose frequency is much lower than the switching frequency is used. The inductor current is monitored to make sure the converter works in CCM. The output voltage is observed and compared with the control signal to verify the large-signal control-to-output linearity, as shown in Figure 2.31.

Vc is set as a 0.5 Hz triangular waveform with peak of 4 V and valley of 2 V. The output of the boost converter is also a triangular waveform with peak of 197.4 V and valley of 103.65 V. The two triangular waveforms are in phase. Since the ratio of 197.4 to 4 is 49.35; and the ratio of 103.65 to 2 is 51.8, both ratios are almost 50 times. Thus, we can see that the linearization is achieved.

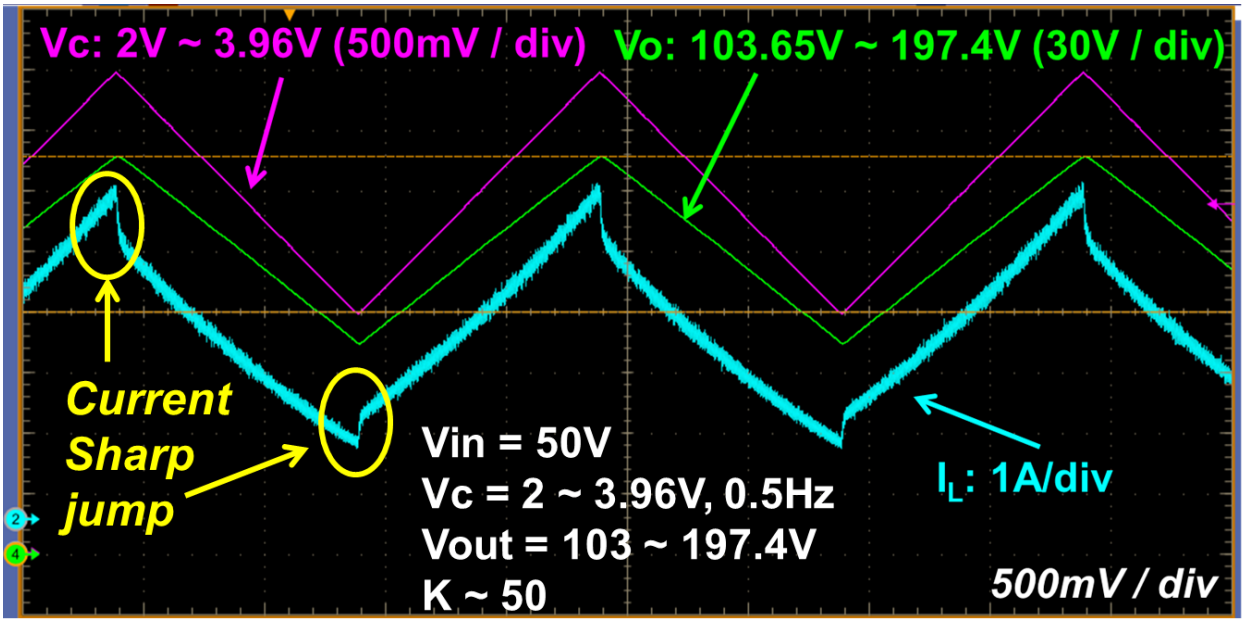


Figure 2.31 Verification of control signal-to-output voltage linearization

From this diagram, we can see that the current stays in CCM but there is a small current jump at the peak and valley points. This is due to the large 1.1 mF aluminum electrolytic capacitor used as the output capacitor. The detailed explanation is shown in Figure 2.32.

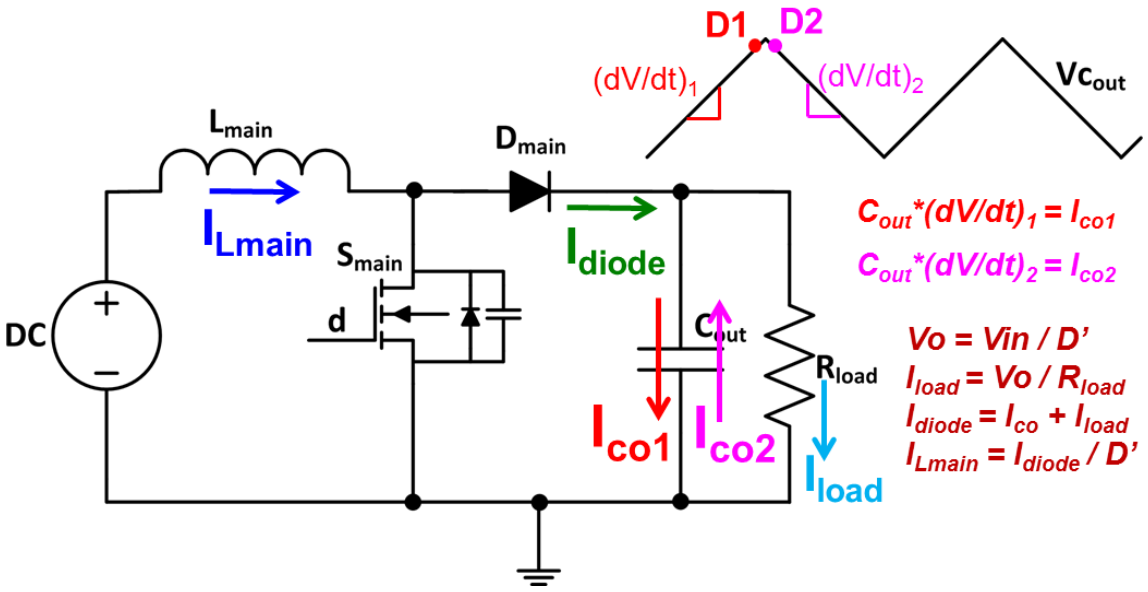


Figure 2.32 Explanation for the current jump

Since the output is a low frequency triangular waveform, we can pick up two operation points, namely D1 and D2, near the peak point. Assume D1 = D2. The dVo / dt slope is a positive constant before peak point, which means the output capacitor is charging with a constant current. The dVo / dt slope is a negative constant after the peak point. The output capacitor is discharging with a constant current. Because the frequency of triangular is much lower than the switching frequency, these two points can be regarded as static operation points. Since Vo = Vin / D', the output voltage Vo and current I_{load} are the same for these two points. If loss is negligible, there is $I_{Lmain} = I_{diode} / D'$. According to Kirchhoff's current law (KCL), there always exists $I_{diode} = I_{Co} + I_{load}$. The diode's current difference ΔI between these two points is due to the difference between the capacitor charging current and the capacitor discharging current. It can be expressed as $\Delta I = Cout * (dV / dt)_1 - Cout * (dV / dt)_2$, where $(dV / dt)_1$ and $(dV / dt)_2$ represent the dVo / dt slopes before and after the peak point. This current difference is transferred to I_{Lmain} by 1 / D', where D' corresponds to the complimentary duty cycle near peak or valley points.

Reduce the output capacitor's value can reduce this current jump. If the capacitance is significantly reduced, the current jump would be much smaller compared with I_{Lmain} and negligible. The simulation results are used to verify the explanation. The schematic is shown in Figure 2.34. The output capacitor Co is changed from 1.1 mF to 50 uF. The current jump is obvious when Co = 1.1 mF. The current jump is negligible when Co is reduced to 50 uF.

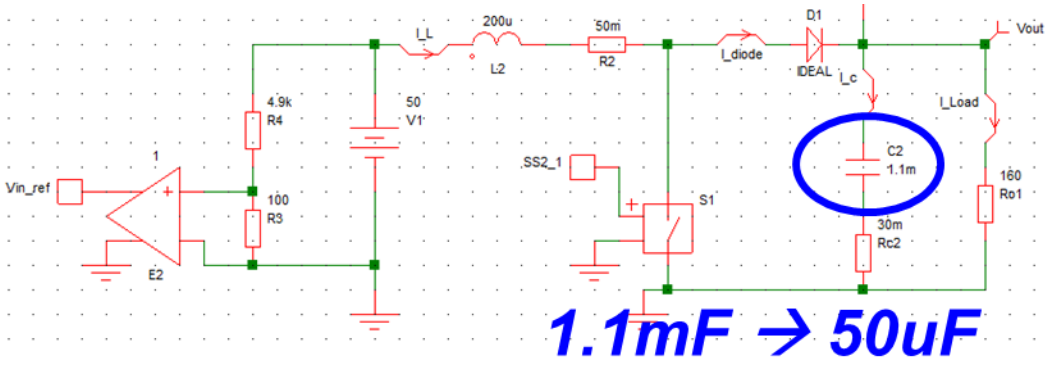
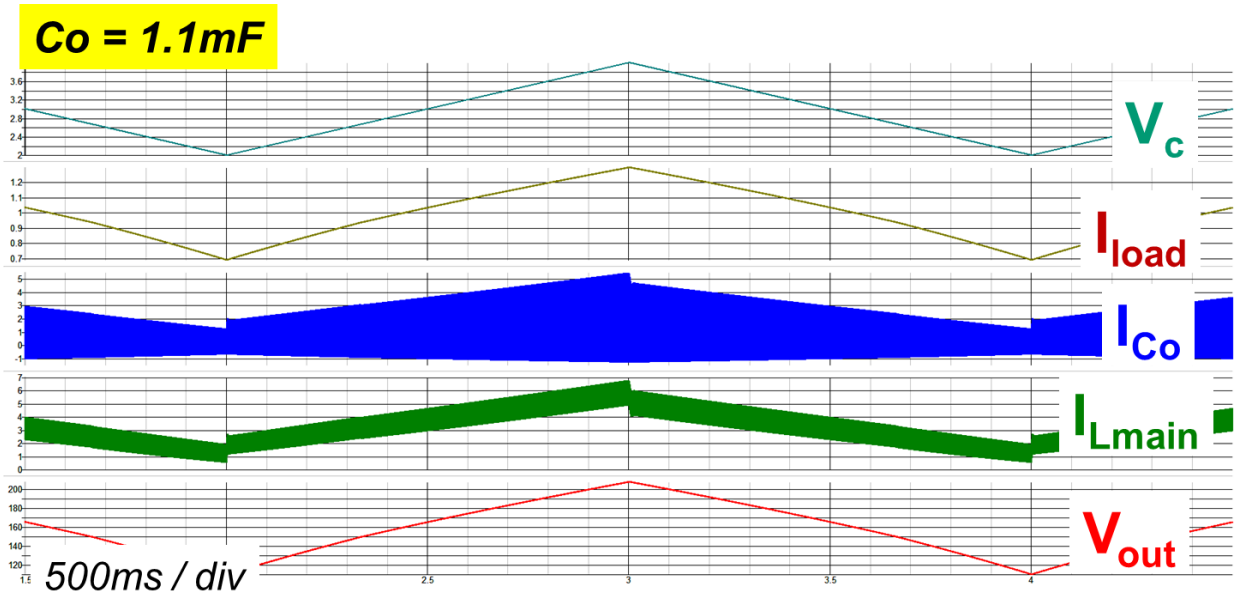


Figure 2.33 Schematic of simulation circuit to verify the elimination of current jump



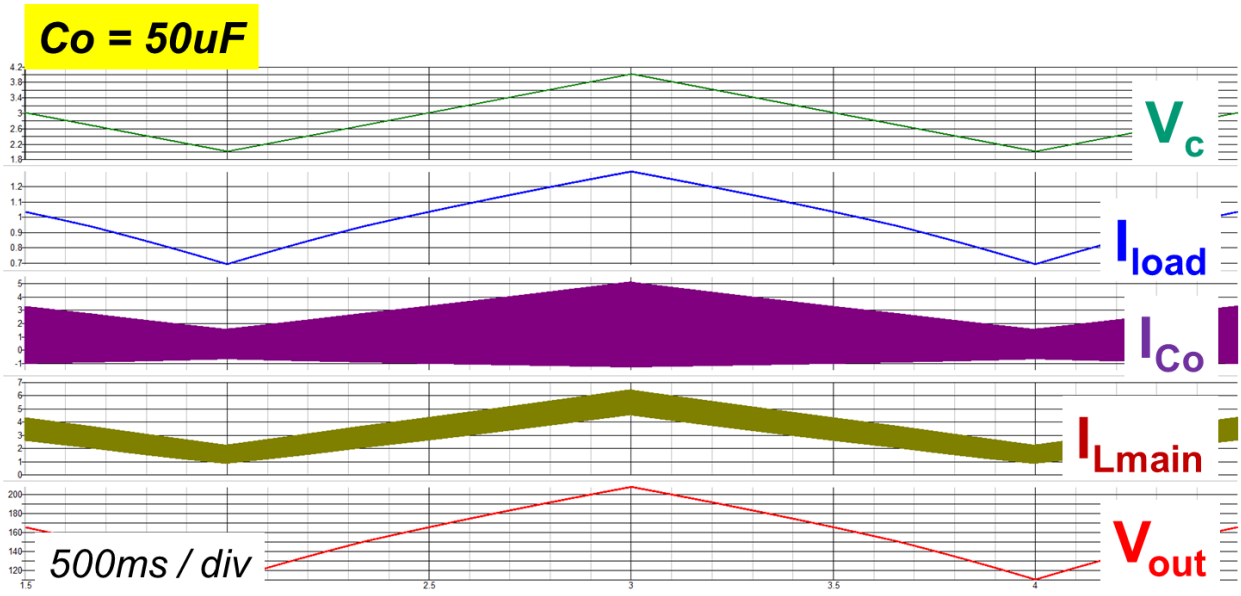


Figure 2.34 Simulation Results with different output capacitances

2.5 Summary

Compared with a conventional modulator, the SOUL modulator brings the following benefits:

1) A unified linearization method is achieved for various PWM dc-dc converters;
2) The large-signal control-to-output control gain is constant, independent on input voltage or external clock's switching period;
3) Feedforward is employed to mitigate the impact from line voltage;
4) Self-oscillation saves the external clock and avoids the mismatch problem between external clock and switching period;

5) The self-oscillation's switching period can be modified to reach the desired accuracy. The impact from propagation delay to switching period can be modified by careful selection of capacitance in the deboo integrator.

6) The negative small-signal control gain can be excluded within the entire control signal range by careful design of control gain;

7) Good linearization is verified by experiments.

Chapter 3. Future Work

Based on the SOUL modulator, a large-signal control-to-output linearity is achieved. However, the output accuracy is limited by parasitic and loss. In this chapter, the small-signal control-to-output transfer function is first deduced based on the SOUL modulator. Bode plots show the unique characteristic based on the SOUL modulator compared with the conventional modulator. Next, the impacts from this unique characteristic to feedback loop design and dynamic performance are discussed.

The small-signal control-to-output transfer function Gvd for a CCM boost converter is expressed in (3.1).

$$G_{vd} = \frac{\hat{v}_o}{\hat{d}} = G_{d0} \cdot \frac{(1+\frac{s}{\omega_{z1}}) \cdot (1-\frac{s}{\omega_{RHP-zero}})}{1+\frac{s}{\omega_0 \cdot Q}+\frac{s^2}{\omega_0^2}} \tag{3.1}$$

$$G_{d0} = \frac{Vin}{(1-D)^2} = \frac{Vo^2}{Vin}$$

$$\omega_{z1} = \frac{1}{r_c \cdot C_o}$$

$$\omega_{RHP-zero} = \frac{(1-D)^2 \cdot (R-r_L)}{L} \approx \frac{R}{L} \cdot (\frac{Vin}{Vo})^2$$

$$\omega_0 = \frac{1}{\sqrt{L \cdot C_o}} \cdot \sqrt{\frac{r_L + (1-D)^2 \cdot R}{R}} \approx \frac{1}{\sqrt{L \cdot C_o}} \cdot \frac{Vin}{Vo}$$

$$Q = \frac{1-D}{\omega_0} \cdot \frac{1}{\frac{L}{(1-D) \cdot R} + \frac{r_L \cdot C_o}{1-D} + r_c \cdot C_o} \approx (1-D) \cdot R \cdot \sqrt{\frac{C_o}{L}}$$

Where r_c is the ESR for the output capacitor; Co is the output capacitor's capacitance; R is the load resistor; r_L is the winding resistor in the inductor; L is the inductor's inductance.

For the conventional modulator, the modulation gain is 1 / Vm. Vm is the amplitude of the saw-tooth ramp, which is constant. As for the SOUL modulator, duty cycle is determined by Vin* and Vc. When there is a perturbation in Vc, there is:

$$D + \hat{d} = 1 - \frac{Vin^*}{Vc + \hat{v}_c} \tag{3.2}$$

Where $\hat{d}$ is the perturbation in duty cycle and $\hat{v}_c$ is the perturbation in control signal.

Rearrange (3.2), there is:

$$\begin{aligned} \Rightarrow \quad & (D + \hat{d}) \cdot (Vc + \hat{v}_c) = Vc + \hat{v}_c - Vin^* \\ \Rightarrow \quad & D \cdot Vc + \hat{d} \cdot Vc + D \cdot \hat{v}_c + \hat{d} \cdot \hat{v}_c = Vc + \hat{v}_c - Vin^* \\ \Rightarrow \quad & Vc \cdot \hat{d} = (1 - D) \cdot \hat{v}_c \\ \Rightarrow \quad & \frac{\hat{d}}{\hat{v}_c} = \frac{1 - D}{Vc} \end{aligned} \tag{3.3}$$

Substitute (3.3) into (3.1), the small-signal control-to-output transfer function for the SOUL modulator is:

$$G_{v_o-v_c}(s)=\frac{\hat{v}_o(s)}{\hat{d}(s)}\cdot\frac{\hat{d}(s)}{\hat{v}_c(s)}=G_{vd}\cdot\frac{1-D}{Vc}=G_{d0}\cdot\frac{1-D}{Vc}\cdot\frac{(1+\frac{s}{\omega_{z1}})\cdot(1-\frac{s}{\omega_{RHP-zero}})}{1+\frac{s}{\omega_0\cdot Q}+\frac{s^2}{\omega_0^{\,2}}}$$

$$=\frac{Vo^2}{Vin}\cdot\frac{1-D}{Vc}\cdot\frac{(1+\frac{s}{\omega_{z1}})\cdot(1-\frac{s}{\omega_{RHP-zero}})}{1+\frac{s}{\omega_0\cdot Q}+\frac{s^2}{\omega_0^{\,2}}}=\frac{Vo}{Vc}\cdot\frac{(1+\frac{s}{\omega_{z1}})\cdot(1-\frac{s}{\omega_{RHP-zero}})}{1+\frac{s}{\omega_0\cdot Q}+\frac{s^2}{\omega_0^{\,2}}} \tag{3.4}$$

$$=K\cdot\frac{(1+\frac{s}{\omega_{z1}})\cdot(1-\frac{s}{\omega_{RHP-zero}})}{1+\frac{s}{\omega_0\cdot Q}+\frac{s^2}{\omega_0^{\,2}}}$$

While the small-signal control-to-output transfer function for the conventional modulator is:

$$G_{v_o-v_c}(s)=\frac{\hat{v}_o(s)}{\hat{d}(s)}\cdot\frac{\hat{d}(s)}{\hat{v}_c(s)}$$

$$=G_{vd}\cdot\frac{1}{Vm}=G_{d0}\cdot\frac{1}{Vm}\cdot\frac{(1+\frac{s}{\omega_{z1}})\cdot(1-\frac{s}{\omega_{RHP-zero}})}{1+\frac{s}{\omega_0\cdot Q}+\frac{s^2}{\omega_0^{\,2}}} \tag{3.5}$$

$$=\frac{Vo^2}{Vin}\cdot\frac{1}{Vm}\cdot\frac{(1+\frac{s}{\omega_{z1}})\cdot(1-\frac{s}{\omega_{RHP-zero}})}{1+\frac{s}{\omega_0\cdot Q}+\frac{s^2}{\omega_0^{\,2}}}$$

Comparing (3.4) and (3.5), the zeros and poles are the same. The DC gain is variable for the conventional modulator; while the DC gain is constant for the SOUL modulator.

In practice, there are applications where the output voltage is constant while the input voltage varies in a wide range, such as the power factor correction (PFC). A boost converter is usually adopted as the power stage. Assuming that Vo = 80 V, Vin ranges from low line 20 V to high line 56 V; L = 50 uH with parasitic resistor r_L = 50 mΩ; Co = 50 uF with ESR r_c = 30 mΩ;

load resistor R = 25 Ω. Bode plots of the small-signal control-to-output transfer functions for conventional and SOUL modulators from low line to high line cases are shown in Figure 3.1 and Figure 3.2.

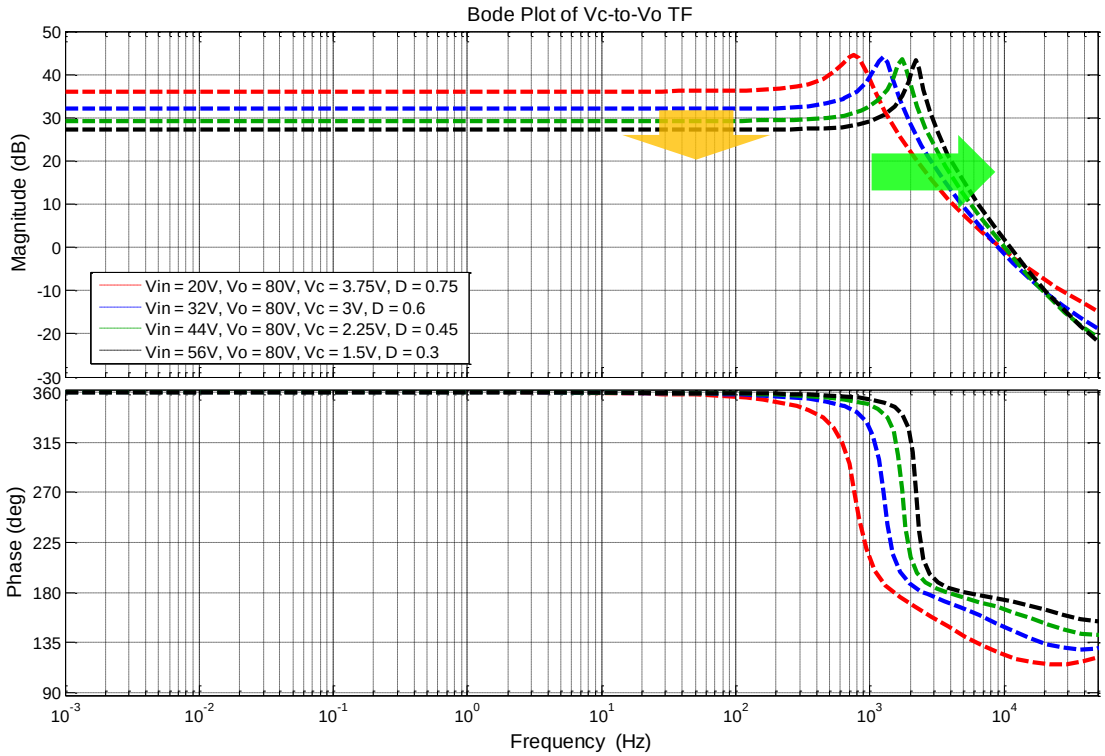


Figure 3.1 Bode plots of the small-signal control-to-output transfer functions for conventional modulator

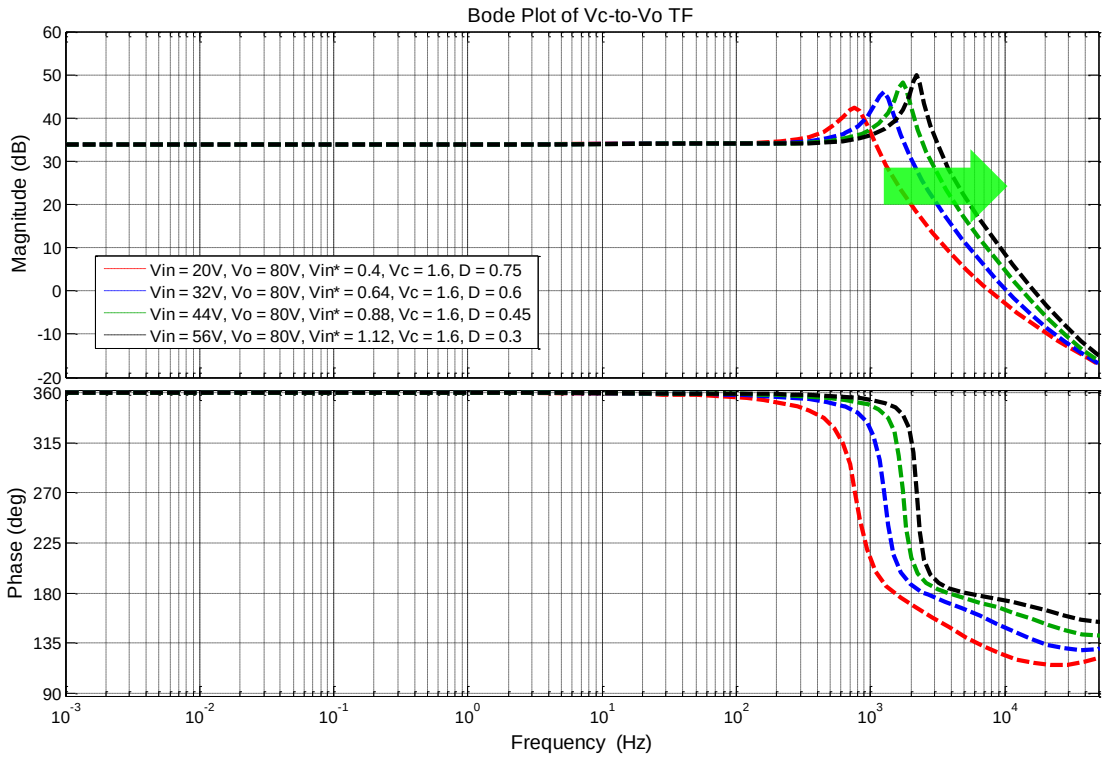


Figure 3.2 Bode plots of the small-signal control-to-output transfer functions for SOUL modulator

The plots verify (3.4) and (3.5). With the SOUL modulator, the DC gain of the small-signal control-to-output transfer function maintains constant even the operation point moves; with the conventional modulator, the DC gain moves lower when Vin varies from low line to high line. Zeros and poles are the same for the two modulators. Therefore there is no difference of the phase and of the corner frequency between the conventional and SOUL modulators.

When designing the compensator for the boost converter used in PFC, it is necessary to first identify the worst case with the poorest phase margin. Based on Figure 3.1 and Figure 3.2, it can be observed that the poorest phase margin always corresponds to the low line case. To make a fare comparison, it's assumed that the low line cases are the same for the two modulators. The compensator is designed based on the worst case. Thus, the loop gain's cross-over frequency is the same for the two modulators at the low line cases. When the operation point moves to the

high line case, we can predict that the SOUL modulator would bring faster transient response ability. This is due to the characteristics mentioned above.

When moving from low line to high line, the DC gain maintains constant and the corner frequency moves higher for the SOUL modulator; the loop gain moves towards right horizontally. The DC gain moves lower and the corner frequency moves higher for the conventional modulator; the loop gain moves towards right and lower. Thus, the loop gain's cross-over frequency would be pushed towards lower frequency based on the conventional modulator compared with the SOUL modulator at the high line case.In other words, due to the constant gain of the SOUL modulator, the loop gain's cross-over frequency would be extended to higher frequency which indicates a faster transient response.

With the same compensator, the low line and high line loop gains based on conventional and SOUL modulators are plotted in Figure 3.3, which verifies the conclusions above.

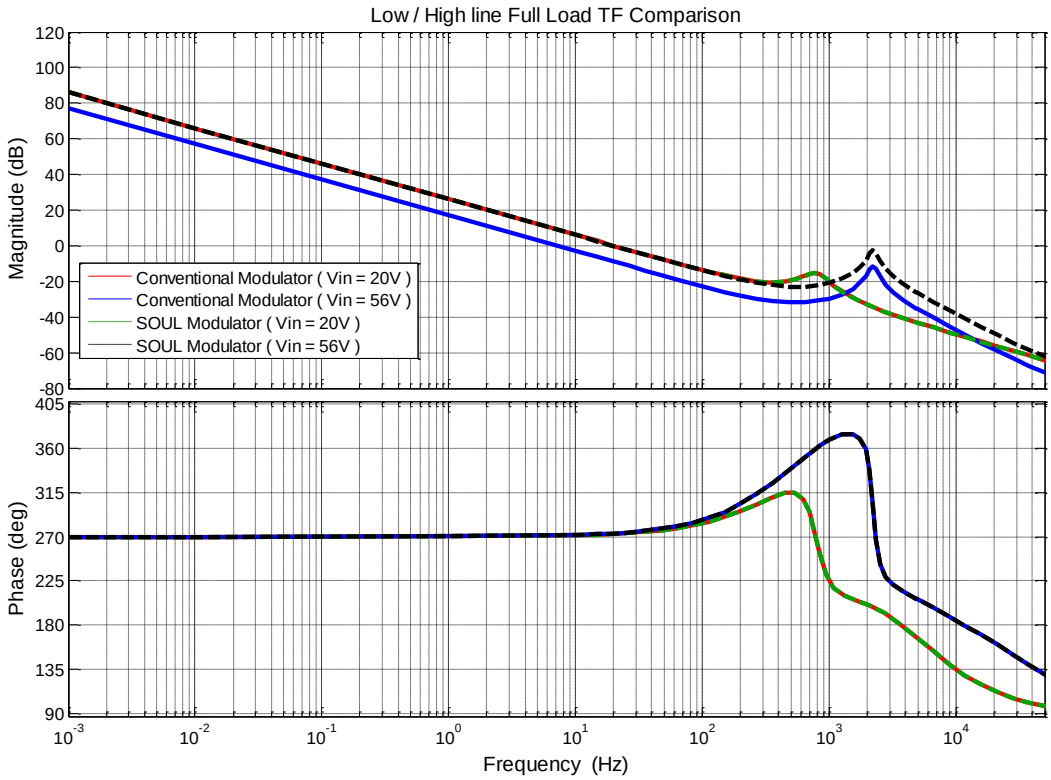


Figure 3.3 The comparison of low line and high line loop gains between conventional and SOUL modulators

In the future, the simulation and experiment for the transient response would be implemented to verify the analysis and conclusions above.

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