DIGITAL CONTROL OF A HIGH FREQUENCY PARALLEL RESONANT DC-DC CONVERTER

Marko Vulovic

Thesis submitted to the Faculty of

VIRGINIA POLYTECHNIC INSTITUTE AND STATE UNIVERSITY

in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

in

ELECTRICAL ENGINEERING

Dushan Boroyevich, Chairman

Fred C. Lee

Paolo Mattavelli

November 5, 2010

Blacksburg, Virginia

Keywords: parallel resonant converter, high frequency digital control, gain scheduling, non resonant coupled, DC-DC switching converter, inductorless output filter

DIGITAL CONTROL OF A HIGH FREQUENCY PARALLEL RESONANT DC-DC CONVERTER

Marko Vulovic

Abstract

A brief analysis of the nonresonant-coupled parallel resonant converter is performed. The converter is modeled and a reference classical analog controller is designed and simulated. Infrastructure required for digital control of the converter (including anti-aliasing filters and a modulator) is designed and a classical digital controller is designed and simulated, yielding a ~30% degradation in control bandwidth at the worst-case operating point as compared with the analog controller. Based on the strong relationship observed between low-frequency converter gain and operating point, a gain-scheduled digital controller is proposed, designed, and simulated, showing 4:1 improved worst-case control bandwidth as compared with the analog controller. A complete prototype is designed and built which experimentally validates the results of the gain-scheduled controller simulation with good correlation. The three approaches that were investigated are compared and conclusions are drawn. Suggestions for further research are presented.

Table of Contents

List of Figures

List of Tables

Acknowledgements

This thesis, and the research that went into creating it, would not have been possible were it not for the support of my advisor, Dr. Boroyevich, my employer, Agilent Technologies, my wife, Kelley, my family, and the Virginia Tech Department of Electrical and Computer Engineering.

Dr. Boroyevich was the single most influential professor I had during my undergraduate studies at Virginia Tech. His class initially sparked my interest in power electronics, which has been the focus of my career thus far. Were it not for his encouragement and recommendation, I would not have been able to return to Virginia Tech to pursue my MSEE. His support and flexibility during my Master's coursework and research have been critical to my success.

My employer, Agilent Technologies, was extremely supportive of my pursuit of a Master's degree. They not only paid for my tuition and books, but essentially granted me a year of paid time off in which to complete my coursework. My managers, including Dave Long, Dennis Gyma, and John Kenny, worked hard to make this happen and I am very appreciative. I hope that Agilent's investment in me will pay off for them. In addition, my collegues Jim McKim and Dan Schwartz generously contributed their time to proof-read this Thesis and review it for language and technical accuracy.

My wife, Kelley, sacrificed greatly by uprooting and moving down to Blacksburg, Virginia for nearly a year and she did so with a smile on her face. She always had a hug, a sandwich, or a back rub to offer me while I had my head buried in my books for twelve hours per day. What a wonderful woman!

My parents, Aleksandar and Linda, not only funded my undergraduate education, but my father's guidance and inspiration and my mother's encouragement are the main reasons that Electrical Engineering came to be my passion. My sister, Elena, preceded me as an undergraduate at Virginia Tech, setting an example and blazing the trail for me; if it hadn't been for the impressions I developed during visits with her at VT while I was still in high school, I likely would have never considered Virginia Tech for my undergraduate, and subsequently graduate studies.

I am grateful to Virginia Tech and more specifically, the Department of Electrical and Computer Engineering for being very flexible and understanding in granting me relief from some policies that would have otherwise made it impossible for me to achieve my educational objectives in the year my employer had granted me.

Finally, I would also like to thank Dr. Boroyevich, Dr. Lee, and Dr. Mattavelli for taking time out of their busy schedules to sit on my advisory committee, and Dr. Beex and Dr. Xu for each working with me on a separate independent study. I would not have been able to get the grounding I received in advanced DSP and resonant converters were it not for their help and attention.

Chapter 1: Introduction

1.1 Motivation for Research

Benefits of Digital Control of Power Converters

In [9], [11], [10], and [18], it is shown that digital controllers for power converters have many advantages over their analog counterparts, including being more flexible, integratable, cost-effective, reliable, and less susceptible to noise and parameter tolerance and drift [9], [11], [10]. They also have the potential to perform better by permitting the use of more complex techniques such as real-time optimization, parameter estimation, and adaptive, nonlinear, MIMO (multiple input/multiple output), and fuzzy control, which are impractical to implement in analog systems [11], [9], [18]. In addition, microprocessor- and FPGA-implemented digital controllers have the advantage of being reprogrammable thereby allowing rapid design iteration during development and field re-configurability without hardware modifications [9], [11], [10].

Because of these benefits, it is generally desirable to use digital controllers for all types of power converters. Consequently, digital control is now becoming more common in the context of high-frequency DC-DC converters. These converters have been slower to transition to widespread digital control than lower-frequency converters (such as motor drives and three-phase power converters for utility interfaces) [11] because their high switching frequencies require processing and digital modulator (e.g. DPWM) performance that often pushes the limits of what can be achieved at reasonable cost with present technology [2]. Additionally, the challenges specific to digital controllers such as quantization, limit cycling, and processing delays [4] are more difficult to overcome cost-effectively in high-frequency designs. However, as the following examples demonstrate, these obstacles are being surmounted as control design techniques and processing technology evolve.

In [4], the authors present a method for digital current mode control of high-frequency pulse width modulated (PWM) converters (i.e. buck, boost, flyback). Their method makes a cycle-by-cycle inference of the average inductor current from samples of the minimum and maximum inductor current (captured by analog to digital converters) by assuming a triangular inductor current wave shape. This signal is used as the feedback for an inner digital current loop, which is controlled by an outer digital voltage loop, similar to what is traditionally done in analog peak or average current mode control. The authors demonstrated their control technique using a step-down current-fed inverter that switches at 80 kHz and is controlled by a 16-bit digital signal processor (DSP). Their current loop is compensated using a proportional-integral controller and their results show a closed loop bandwidth of 7.5 kHz, which is slightly less than 10:1 below their switching frequency. The authors claim that approximately half of the phase shift at gain crossover is due to their two-cycle processing latency and they believe that faster processing would improve loop bandwidth at the expense of creating a minimum duty cycle constraint. Most importantly, however, they claim to see no need for slope compensation to avoid sub-harmonic oscillations (as required with analog peak current mode control), nor the need for gain restrictions at the switching frequency (as required with analog average current mode control).

In [2] the authors present a predictive digital current mode control technique for fixed-frequency PWM DC to DC converters. They analyze their control approach using various converter topologies (buck, boost, and buck-boost), controlled parameters (peak current, average current, and valley current), and modulation techniques (leading edge, trailing edge, and triangular modulation). For example, their approach to peak current control via leading edge modulation consists of sampling the inductor current, input voltage, and output voltage at the start of each cycle and then computing the change in duty cycle required to cause the predicted peak current of the subsequent cycle to track a reference. This method assumes a triangular inductor current wave shape, a known constant inductance, and input and output voltages that are sufficiently slow moving to be assumed static over the switching interval. Their analysis for a boost converter shows no instabilities and their findings were demonstrated using a 100 W PFC boost converter. The technique is essentially a practical method of digitally implementing traditional analog peak current mode control without requiring expensive high-frequency sampling of the inductor current waveform. It avoids the problems created by the processing delays inherent to digital systems by predicting the peak current instead of measuring it in real-time. The result is a system that performs similarly to its analog equivalent but has many of the aforementioned benefits of digitally controlled systems, including re-programmability, lower sensitivity to parametric variations, and more potential for integration.

Benefits of Resonant Converters

In the realm of DC-DC converters, resonant converters have many advantages over their more traditional PWM counterparts, such as higher efficiency, greater power density, higher switching frequencies, and lower component stresses [6], [17]. Amidst all of these benefits, however, is one significant disadvantage of resonant converters: they suffer from generally complex control relationships that are often sensitive to operating point and parameter tolerance and drift [1]. This complexity implies that resonant converters in particular could stand to benefit greatly from digital control, as the following two examples demonstrate.

In [1], the authors describe a digital fuzzy logic controller for a variable frequency series resonant converter. They created a fuzzy, nonlinear controller that accepts 9-step fuzzified inputs of v_o and dv_o / dt (where v_o is the converter's output voltage) and computes df_s / dt, which is integrated to create f_s, the converter's control frequency. The authors tested their design and found that, in contrast to linear control approaches they had tried, transient performance was consistently good over the converter's entire operating range. Additionally, the controller design process was much easier than that of other nonlinear control techniques and the resultant controller was low-cost due to the simplicity of the control algorithms.

In [3], a real-time digital technique for rapidly estimating the resonant frequency of a resonant converter is introduced. It involves sampling the resonant inductor current a few times per cycle and computing an estimate of the actual resonant frequency of the converter, despite potentially large variations of resonant capacitance and / or inductance. The technique enabled the author to maximize the efficiency of a series resonant converter by operating it precisely at resonance. This concept could also be more generally used to allow converters to be more precisely controlled in terms of f_n (normalized switching frequency) and to allow precise bounding of the converter in either the ZVS or ZCS region of operation. This technique could not be practically implemented in an analog controller.

For all of these reasons, the digital control of a resonant converter, specifically, a nonresonant-coupled parallel resonant converter (NC-PRC) was chosen as the subject of this research. Although similar to a conventional parallel resonant converter (PRC), this specific topology has the added benefits of being more compact [14], being easier to control [16], and having a well-bounded peak resonant capacitor voltage [8]. Additionally, although [8] introduces constant frequency current-programmed PWM control for the NC-PRC, no published work could be found on a generally applicable variable frequency NC-PRC control strategy, making it worthy of exploration.

In addition, CPES* at Virginia Tech was working in conjunction with the U.S. Army Research Lab (ARL) on an NC-PRC converter for use in a high-voltage capacitor charging application, as described in [14]. The controller used for the converter was an analog, voltage-mode controller. There was hope that the results of this research could eventually be applied to the ARL converter, improving performance. This application requires the converter to transition through a large range of voltage and current operating points during each charging cycle, making the control design problem more challenging.

1.2 Research Approach

To best achieve the previously stated benefits of digital controllers, the intent of this research was to explore entirely digital control of a NC-PRC with the goal of minimizing parts count and circuit complexity while maintaining stability and achieving as high performance as practical. This was accomplished by eliminating any non-essential analog subsystems, including peak current or voltage comparators, analog modulators, and any complex sensor systems.

In contrast to the traditional PRC where the output filter capacitor is decoupled from the rectifier by an inductor, control of the NC-PRC has not been extensively studied. In particular, no published work could be found that showed a linearized small-signal model of the NC-PRC. Since this is a critical first step in applying modern linear control techniques (such as linear-quadratic regulator, or LQR, and linear-quadratic Gaussian, or LQG), attempting to develop a small-signal model of the NC-PRC was an important first step in my research. To this end, I attempted to apply the extended describing function (EDF) method detailed in [20] to the NC-PRC. Although I have no reason to doubt the soundness of the extended describing function technique, I was unable to reach reasonable agreement between the results of the EDF method and simulation after substantial effort. I attribute this failure to a subtly incorrect implementation of the relatively complex EDF process. At that point, I decided to abandon development of a linearized small-signal model and instead focus my research on control methods that are not dependent on a known small-signal model.

In Chapter 2, I present the NC-PRC topology and summarize others' analysis of it. I also design and simulate a complete classical analog controller to use as a basis for comparison with the digital controllers I develop in later chapters.

* Center for Power Electronics Systems

In Chapter 3, I choose the average rectifier current as the controlled parameter instead of the output current or voltage because it removes the low-frequency pole created by the converter's substantial output impedance and the output filter capacitor from the plant's control-to-feedback transfer function. I then design the infrastructure necessary to measure and feed these signals into the digital controller, including simple sensing circuits, anti-aliasing filters, and analog-to-digital converters. I also design the period modulator, which allows the digital controller to actuate the converter by changing its switching period. Due to practical clock speed limitations of the FPGA used to build the controller, the raw frequency resolution of the modulator is too coarse which will result in limit-cycling. To address this, I also design a colored dithering system that modulates the switching period requested by the controller with the goal of increasing the modulator's effective resolution.

In Chapter 4, I design a simple linear digital controller empirically with the goal of maximizing control bandwidth while maintaining specified minimum stability margins at all operating points. I simulate the design and observe that the converter exhibits nearly 20 dB of small-signal gain variability with operating point resulting in a loop gain crossover frequency, and consequently transient response, that varies widely. Maintaining sufficient stability margins at the worst-case operating point forces the converter's performance to suffer over the rest of its operating range.

In Chapter 5, having taken note of the converter's gain variability observed earlier, I investigate adding a simple proportional gain-scheduling system to the controller. The goal is to reduce or eliminate the variation of the converter's gain with operating point, thereby yielding more consistent performance while still maintaining stability. I simulate the design and observe much improved results.

In Chapter 6, I build a prototype of my converter, implement the digital controller with proportional gain scheduling, and verify my simulation results. I show plots of the prototype converter's waveforms and their spectra. Unexpected sub-harmonic narrowband components observed in the spectra are evidence of aliasing occurring in the modulator.

In Chapter 7, I compare the performance of the three control approaches and the experimental results and draw conclusions. I also provide a list of possible further research topics that would build on my work.

In Chapter 8, I share a list of references I used throughout my research.

Chapter 2: NC-PRC Converter Behavior

2.1 NC-PRC and Comparison to PRC

The nonresonant-coupled parallel resonant converter (NC-PRC) is very similar to, and shares many characteristics with the more conventional parallel resonant converter (or PRC), which has an inductively- (or 'resonant-') coupled output filter. However, it has a few important advantages and significant behavioral differences that affect control design.

As described in [16], in a nonresonant-coupled converter the resonant tank is completely decoupled from the output (by the rectifier) when in resonant circuit modes. A traditional PRC can be made 'nonresonant-coupled' by eliminating the inductor in the output filter, coupling the output filter capacitor directly to the rectifier. When compared with a conventional PRC, the NC-PRC topology is more compact (due to the elimination of the output filter inductor) [14], is easier to control [16], and is more robust (due to the reduced component stress associated with a clamped peak resonant capacitor voltage [8]).

Figure 2.1 illustrates the NC-PRC topology and shows how similar it is to the PRC. This converter is controlled by varying the switching frequency of switches S1 and S2, which are switched 180° out-of-phase with each other at a 50% duty-cycle.

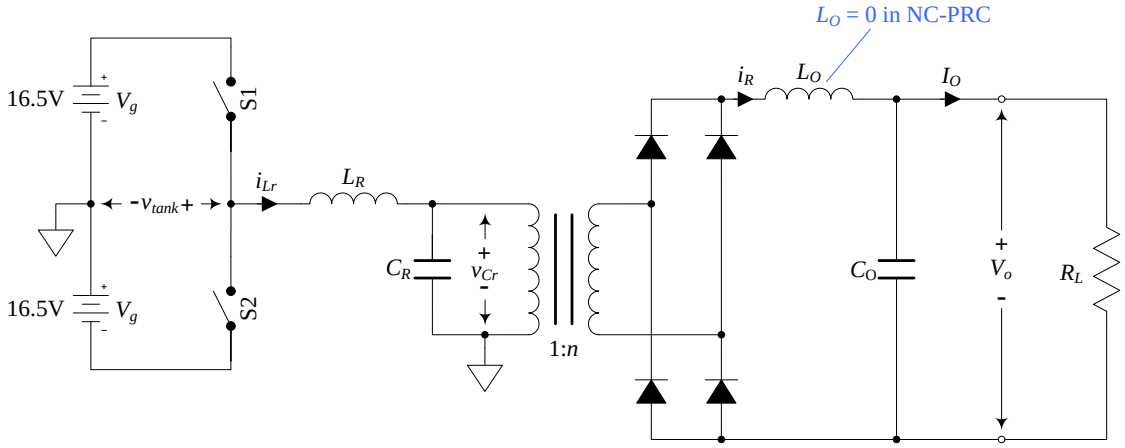


Figure 2.1 – Schematic of an ideal basic parallel resonant DC-DC converter (PRC) topology. A PRC becomes a nonresonant-coupled PRC (NC-PRC) when the output filter inductor is zero.

A detailed steady-state analysis of the NC-PRC topology shown in Figure 2.1 was presented in [5] and [6]. Following is a simplified and less comprehensive version of that analysis, including only information specifically relevant to this research.

2.2 Brief Nonresonant-Coupled PRC Analysis

As done in [5], the analysis of the converter is simplified by first normalizing all of its parameters using the factors shown in Table 2.1.

Units	Normalization Factor
Voltage (V)	$V_0 = V_g$
Resistance (Ω)	$R_0 = \sqrt{\frac{L_R}{C_R}}$
Current (A)	$I_0 = \frac{V_g}{R_0}$
Frequency (Hz)	$f_0 = \frac{1}{2\pi\sqrt{L_R C_R}}$
Angular Frequency (rad/s)	$\omega_0 = \frac{1}{\sqrt{L_R C_R}}$

Table 2.1 – PRC normalization factors.

Using these normalization factors, normalized circuit quantities of interest are defined in Table 2.2. Quantities on the secondary side of the transformer are reflected to the primary side for consistency.

Quantity	Normalized Quantity
Average Output Voltage	$M_O = \frac{V_O}{n\,V_0}$
Average Output Current	$J_O = \frac{n\,I_O}{I_0}$
Resonant Capacitor Voltage	$m_{Cr} = \frac{V_{Cr}}{V_0}$
Resonant Inductor Current	$j_{Lr} = \frac{i_{Lr}}{I_0}$
Rectifier Current	$j_R = \frac{n\,i_R}{I_0}$
Switching Frequency	$\omega_n = \frac{f_{sw}}{f_0}$

Table 2.2 – Normalized circuit quantities, reflected to the primary side of the transformer.

In [6] the author describes three mutually exclusive modes of steady-state operation of the NC-PRC, aptly named modes 1, 2, and 3. Figure 2.2, Figure 2.3, and Figure 2.4 illustrate typical normalized steady-state NC-PRC rectifier current (j_R), resonant capacitor voltage (m_{Cr}), and resonant inductor current waveforms (j_{Lr}) in each of these modes.

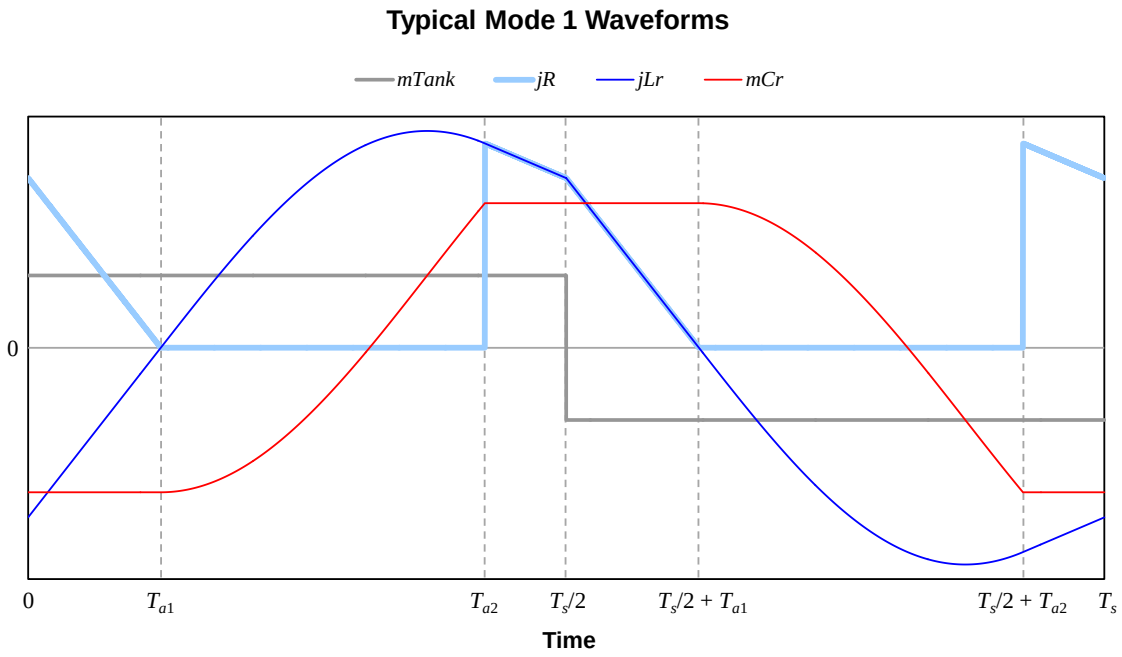


Figure 2.2 – One cycle of typical normalized resonant capacitor voltage (m_{Cr}), inductor current (j_{Lr}), and rectifier current (j_R) waveforms of the NC-PRC operating in mode 1 in steady-state.

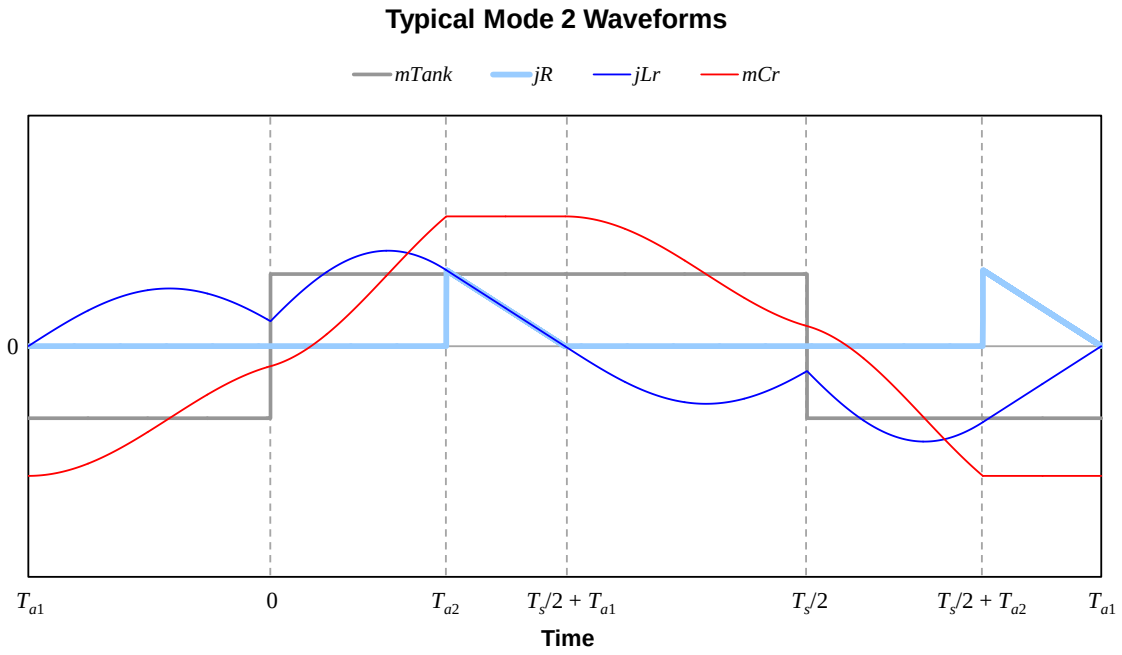


Figure 2.3 – One cycle of typical normalized resonant capacitor voltage (m_{Cr}), inductor current (j_{Lr}), and rectifier current (j_R) waveforms of the NC-PRC operating in mode 2 in steady-state.

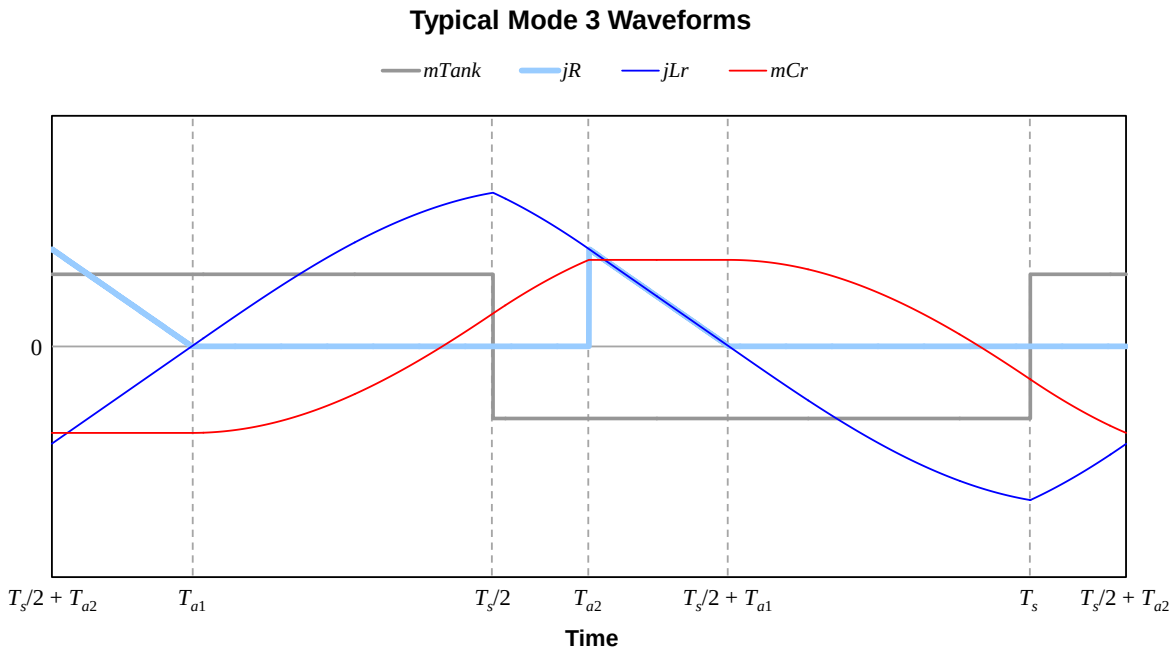


Figure 2.4 – One cycle of typical normalized resonant capacitor voltage (m_{Cr}), inductor current (j_{Lr}), and rectifier current (j_R) waveforms of the NC-PRC operating in mode 3 in steady-state.

Table 2.3 summarizes the circuit sub-interval boundaries shown in Figure 2.2, Figure 2.3, and Figure 2.4. Since the converter is operating in steady-state in all cases, time shifts by integer multiples of T_s have no effect.

Time	Event
0 (or T_s)	Start / end of cycle. S1 closes, inducing a positive voltage across the tank.
T_{a1}	Reverse diodes turn off. Occurs at positive zero-crossing of j_{Lr}.
T_{a2}	Forward diodes turn on. Occurs when resonant voltage m_{Cr} reaches M_O.
$T_s/2$	S2 closes, inducing a negative voltage across the tank.
$T_s/2 + T_{a1}$	Forward diodes turn off. Occurs at negative zero-crossing of j_{Lr}.
$T_s/2 + T_{a2}$	Reverse diodes turn on. Occurs when resonant voltage m_{Cr} reaches $-M_O$.

Table 2.3 – Summary of boundaries between the circuit sub-intervals of the NC-PRC.

Table 2.4 summarizes the steady-state conditions under which the converter operates in each mode.

Mode	Condition
Mode 1	$0 < T_{a1} < T_{a2} < \frac{T_s}{2}$
Mode 2	$T_{a1} < 0 < T_{a2} < \frac{T_s}{2}$
Mode 3	$0 < T_{a1} < \frac{T_s}{2} < T_{a2}$

Table 2.4 – Conditions for operation in each of the three modes of the NC-PRC.

Because it uses MOSFETs as switching devices (which are capacitive), the converter design used in this research is intended to operate using zero voltage switching (ZVS) to minimize switching losses. To operate in the ZVS region, the converter must switch above its resonant frequency. Since mode 2 occurs only when the converter is operated below resonance [6], it will not be discussed further here.

Using the converter topology shown in Figure 2.1, I applied the following process (derived from [6]) to derive a steady-state expression for the converter's average output current in mode 1.

1. Assuming zero voltage ripple on the output filter capacitor, C_O, develop equivalent linear circuits that model the behavior during each sub-interval of the switching period. All quantities on the secondary of the transformer should be referenced to the primary.
2. Using linear circuit analysis, develop expressions for the resonant inductor current, resonant capacitor voltage, and rectifier current waveforms in each sub-interval, based on the typical waveforms and boundary conditions shown in Figure 2.2.
3. Normalize these expressions as shown in Table 2.2.
4. Derive closed-form expressions for the steady-state waveforms by equating boundary conditions and solving the resultant set of simultaneous equations.
5. Integrate the steady-state waveforms over one switching period to obtain a closed-form expression for the average output current as a function of output voltage and switching frequency.

When simplified by assuming that all switches and diodes are ideal (no voltage drop, as shown in Appendix A), this yields an expression for normalized average output current in mode 1 of

$$J_{O,\mathrm{M1}}\left[\omega_n, M_O\right] = \frac{\left(1+M_O\right)\left(\pi - \omega_n \alpha\left[M_O\right]\right)\left(\left(1-M_O\right)\left(\pi - \omega_n \alpha\left[M_O\right]\right) + 4\omega_n\sqrt{M_O}\right)}{4\pi\,\omega_n} - \frac{\omega_n M_O}{\pi} \tag{2.1}$$

where

$$\alpha\left[M_O\right] = \arccos\left[\frac{1-M_O}{1+M_O}\right] \tag{2.2}$$

My attempt to follow the same solution process for mode 3 failed at step 4, which agrees with the findings in [5]: the resultant equations referenced the variable to be solved for in a mixture of linear and trigonometric terms, thus no closed-form solution could be found. Consequently, the steady-state solution in mode 3 can only be derived by numeric iteration. This precluded the use of static plant inversion as a general control strategy.

To derive an expression defining the boundary between modes 1 and 3, I used the process presented in [5]. I first derived an expression describing the normalized switching frequency along the boundary between modes 1 and 3, ω_{nb13}, from the mode 1 equations by setting $T_{a2} = T_s/2$ in step 4 (above) and computing ω_n. This resulted in

(2.3) $$\omega_{nb13}\left[M_O\right] = \omega_n\big|_{T_{a2}=T_s/2} = \frac{\pi}{\alpha\left[M_O\right] + \frac{2\sqrt{M_O}}{\left(1+M_O\right)}}$$

I next plugged this result into expression (2.1), yielding an expression for the normalized average output current along the boundary between modes 1 and 3 of

(2.4) $$J_{O,B13}\left[M_O\right] = \frac{2M_O}{2\sqrt{M_O} + \left(1+M_O\right)\alpha\left[M_O\right]}$$

As with expression (2.1), expressions (2.3) and (2.4) assume all switches and diodes to be ideal (no voltage drop).

A series of super-resonant normalized constant frequency curves for the NC-PRC is plotted in Figure 2.5 along with the boundary between modes 1 and 3 (from expression (2.4)). These curves were derived numerically using a Saber simulation of a normalized NC-PRC with an infinite output capacitor (implemented as an ideal voltage source set to the normalized output voltage). For each chosen value of normalized switching frequency, ω_n, the steady-state average normalized current, J_O, was measured* as the normalized output voltage, M_O, was swept through a series of 500 values. Since the converter needed to settle at each operating point, it took over 18 hours to capture this data using a state-of-the-art workstation.

* Derived from the instantaneous normalized output current, j_O, by averaging over an integer number of switching periods.

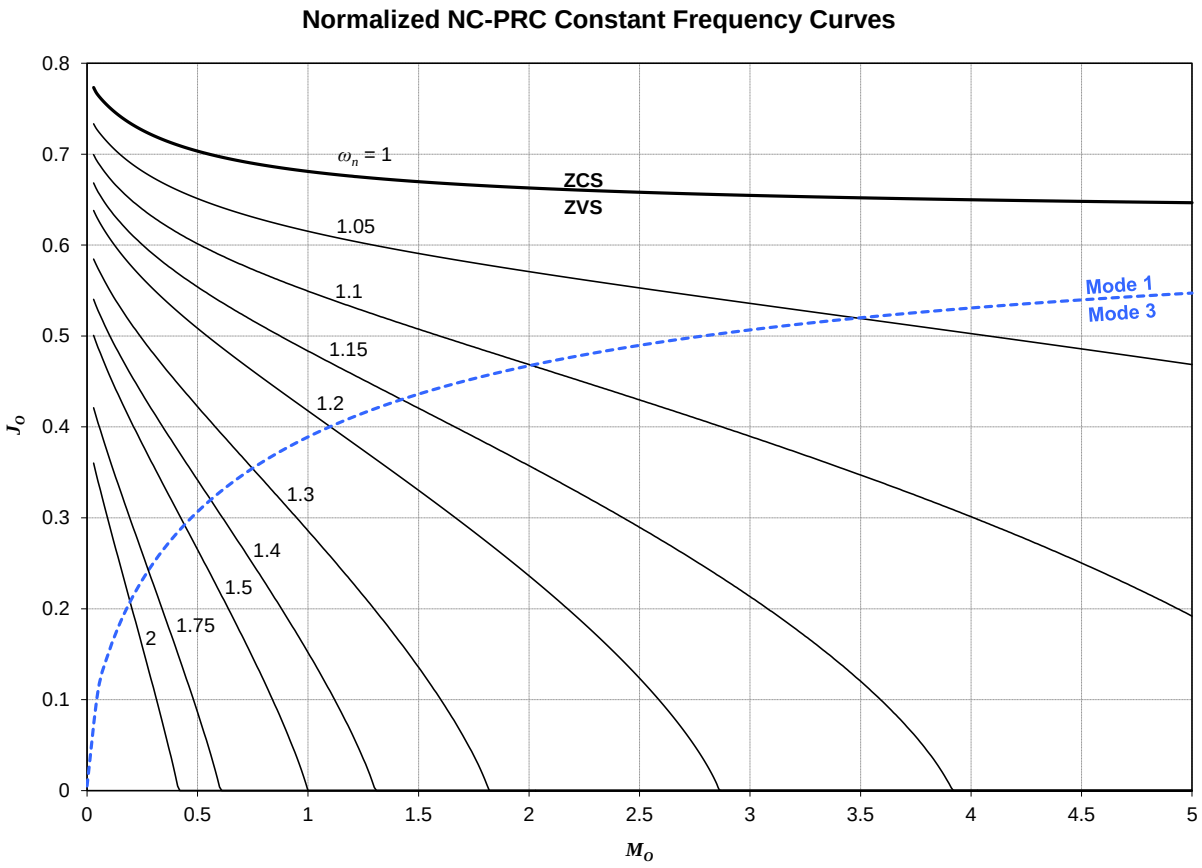


Figure 2.5 – Normalized super-resonant constant frequency curves of the NC-PRC, shown at selected normalized switching frequencies, ω_n, along with the ZVS / ZCS (in bold) and mode 1 / mode 3 (in dotted blue) boundaries.

2.3 Subject Converter Design

Figure 2.6 shows a simplified schematic of the NC-PRC converter design used as the basis for this research. The design is based on a three-level high-density 10 kV, 30 kW converter designed by a U.S. Army Research Lab-funded team of CPES* students and faculty at Virginia Tech for use in a high pulse power military application [14]. To facilitate prototyping, I simplified and scaled their converter design down to 50 V, 150 W using the process detailed in Appendix B, which preserves the converter's behavior and key control characteristics, including its resonant frequency and characteristic impedance. The resonant capacitor, resonant inductor, and output filter capacitor have been slightly modified from what is shown in Appendix B to account for transformer leakage inductance and part value availability while still preserving the converter's resonant frequency. A full schematic of the subject converter design in shown in Section C.1.

* Center for Power Electronics Systems

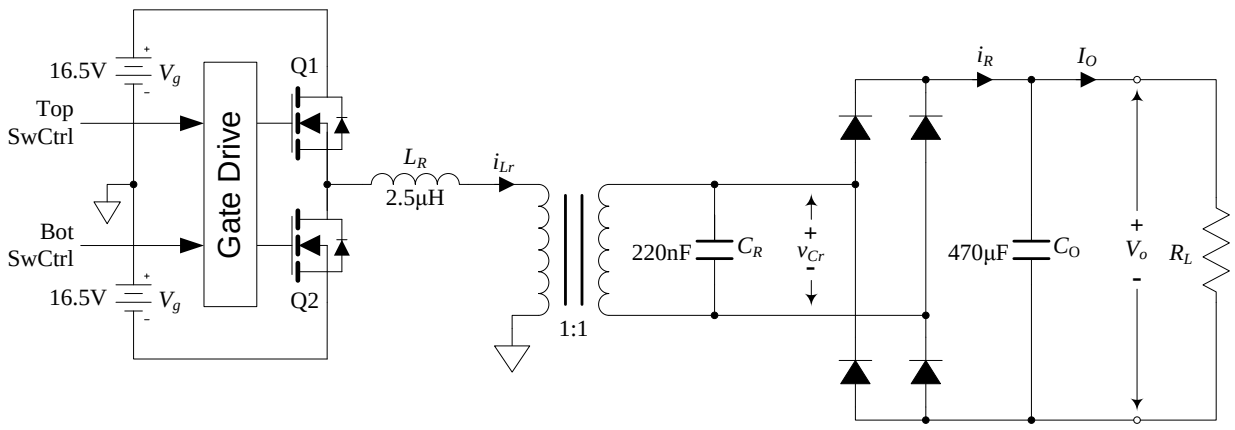


Figure 2.6 – Simplified schematic of the subject NC-PRC DC-DC converter used as the basis of this research.

As described in Section 2.1, switches Q1 and Q2 are driven using 50% duty cycle square waves of the same frequency that are 180º out of phase with respect to each other. The frequency of these square waves is varied to control the converter. The switching frequency must always be above the resonant frequency, f_0, to ensure ZVS (thereby minimizing switching losses).

Key parameters and characteristics of the converter are summarized in Table 2.5.

Parameter	Symbol	Expression	Value
Resonant Inductance	L_R		2.5 µH
Resonant Capacitance	C_R		220 nF
Transformer Turns Ratio	n	$\frac{n_s}{n_p}$	1
Resonant Frequency	f_0	$\frac{1}{2\pi n\sqrt{L_R C_R}}$	214.6 kHz
Characteristic Impedance	R_0	$\frac{1}{n}\sqrt{\frac{L_R}{C_R}}$	3.438 Ω
Input Voltage	V_g		16.5 V
Output Capacitor	C_o		470 µF
Maximum Output Voltage			50 V
Maximum Load Current			3 A
Maximum Output Power			150 W

Table 2.5 – Summary of key parameters of the NC-PRC DC-DC converter.

Figure 2.7 shows the constant frequency curves for the subject converter in modes 1 and 3, as well as the ZCS / ZVS and mode 1 / mode 3 boundaries. The rectifier diodes are assumed to have a forward drop of 0.7 V. This data was captured using the same technique described in Section 2.2.

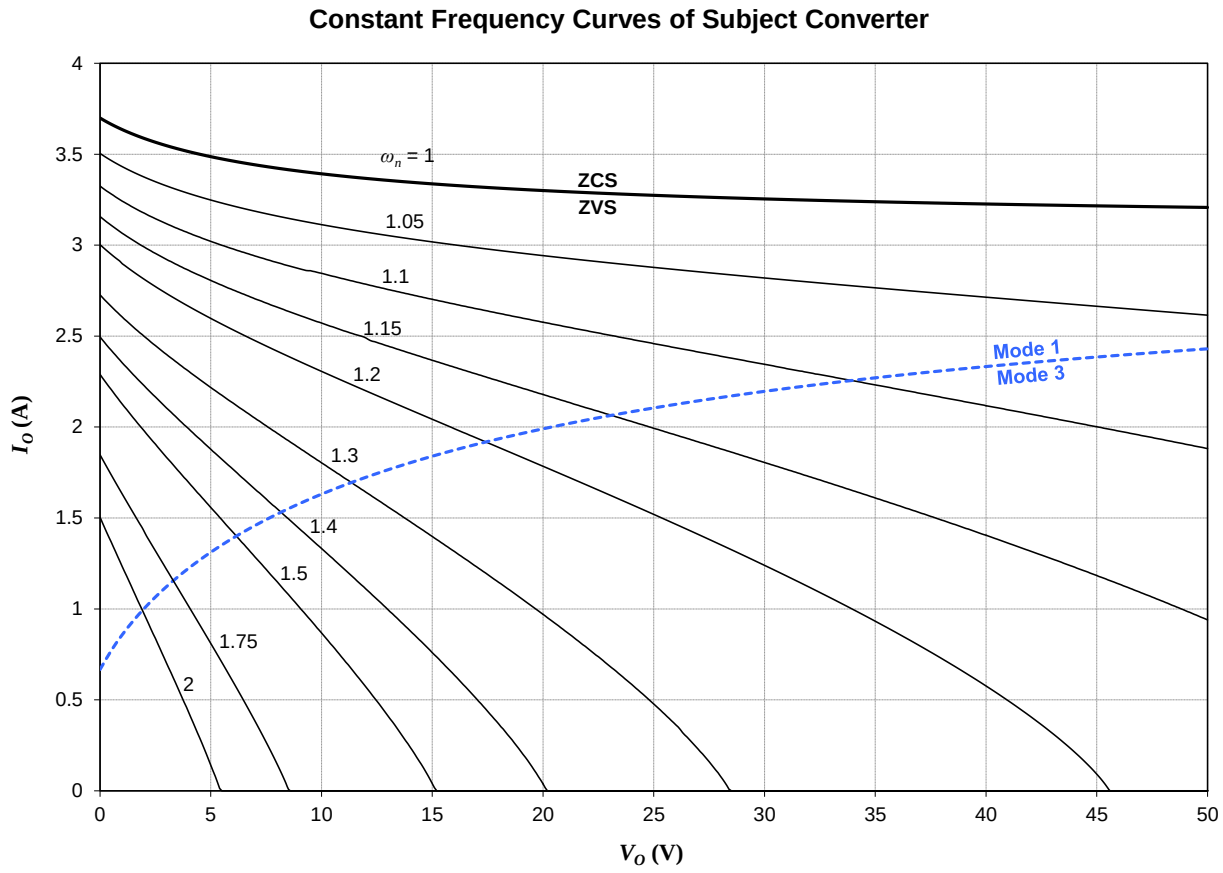


Figure 2.7 – Super-resonant constant frequency curves of the subject converter, shown at selected normalized switching frequencies, ω_n, along with the ZVS / ZCS (in bold) and mode 1 / mode 3 (in dotted blue) boundaries.

2.4 Classical Analog Control Design

Classical control design is the design of a linear time-invariant controller done in the frequency domain. To permit analysis in the frequency domain, the plant to be controlled must also be linear and time-invariant. Despite the nonlinear nature of the relationship between the subject converter's switching period (control input) and rectifier current (feedback signal), it can be approximated as linear for frequencies well below f_s by assuming sufficiently small perturbations as shown in Figure 2.8, where angled brackets denote small-signal quantities and τ_n represents the switching period, normalized to the resonant period, $1/f_0$.

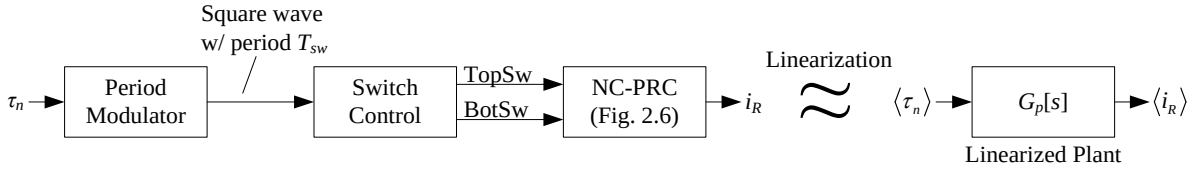


Figure 2.8 – Small-signal linear plant model obtained by linearizing the modulator and converter.

Although the intent of this research is to investigate digital control of the subject converter, I went through a classical analog control design as a reference for comparison. This was done using the rectifier output current, i_R, as the feedback source (via i_{Rsns}, explained in Section 3.2), and a τ_n-normalized version of the ideal continuous-time improved period modulator design from Figure 3.5 to actuate the converter. In addition, the anti-aliasing filter from Section 3.4 was included to prevent excessive aliasing in the modulator and to keep the ripple amplitude in the analog compensator reasonable.

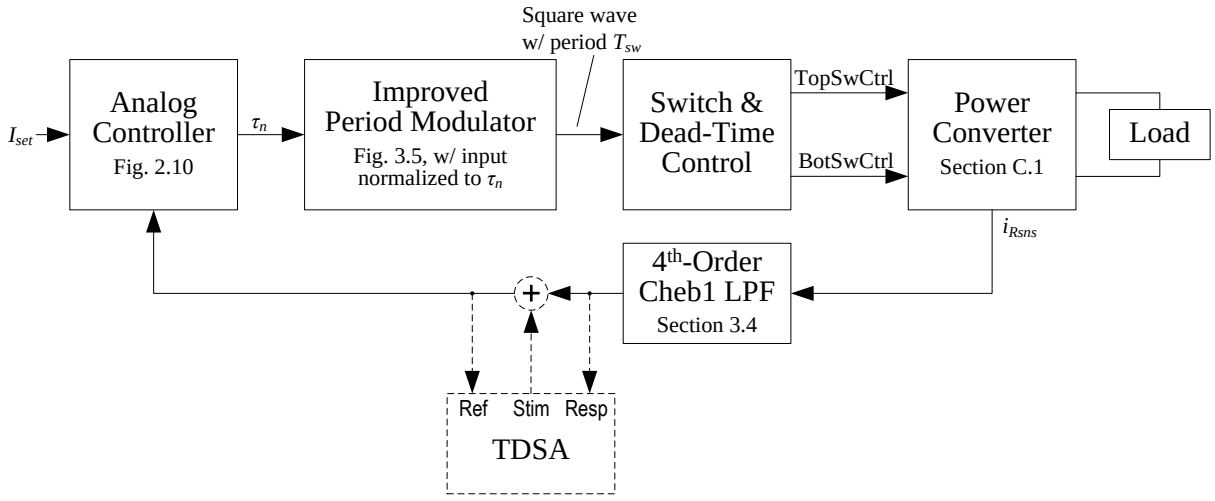


Figure 2.9 – Block diagram of the analog system.

Analog Controller Structure

For this design, a 2nd-order compensation filter was chosen in addition to the pole in the integrator, for a total control system order of three. Figure 2.10 shows a block diagram of the linear controller.

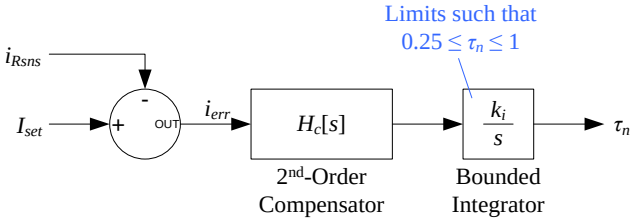


Figure 2.10 – Block diagram of the linear controller.

The compensator's 2nd-order transfer function, $H_c[s]$, can be represented as a second-order section (SOS), or

$$H_c[s] = H_{SOS}[s] \tag{2.5}$$

The transfer function of the SOS can be expressed as

$$H_{SOS}[s] = k_{dc} \frac{\left(s/s_{z1} - 1\right)\left(s/s_{z2} - 1\right)}{\left(s/s_{p1} - 1\right)\left(s/s_{p2} - 1\right)} \tag{2.6}$$

where $s_{z1,2}$ and $s_{p1,2}$ are zero and pole locations in the s-plane, respectively, and k_{dc} is the DC gain. For convenience, (2.6) can be equivalently expressed in terms of quality factor, Q, and corner frequency, ω_0, as

$$H_{SOS}[s] = k_{dc} \frac{1 + \frac{1}{\omega_z Q_z} s + \frac{1}{\omega_z^2} s^2}{1 + \frac{1}{\omega_p Q_p} s + \frac{1}{\omega_p^2} s^2} \tag{2.7}$$

where Q_z, Q_p are the quality factors and ω_z, ω_p are the corner frequencies of the zero and pole pairs, respectively. In general, Q can alternately be defined in terms of the damping ratio, ζ, as

$$Q = \frac{1}{2\zeta} \tag{2.8}$$

The s-domain poles and zeros of this transfer function can be computed in terms of their corresponding Q and ω from (2.7) to be

$$\begin{aligned} s_{p1,p2} &= -\frac{\omega_p}{2Q_p} \pm \omega_p \sqrt{\frac{1}{4Q_p^2} - 1} \\ s_{z1,z2} &= -\frac{\omega_z}{2Q_z} \pm \omega_z \sqrt{\frac{1}{4Q_z^2} - 1} \end{aligned} \tag{2.9}$$

Using the structure shown in Figure 2.10, the analog controller was designed following the process shown in Figure 2.11.

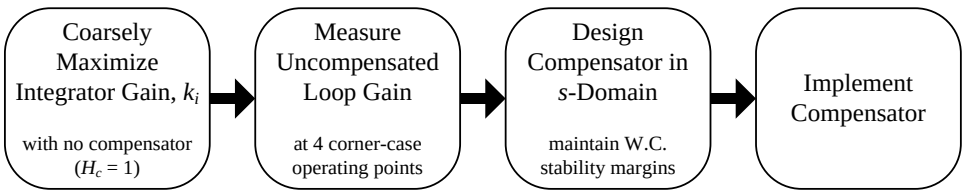


Figure 2.11 – Analog controller design process.

Integrator Gain Selection

Since no linear model of the subject converter was available (for reasons described in Section 1.2), the s-domain compensator's poles and zeros were chosen empirically based on the

uncompensated loop gain (as measured in simulation). This was done by closing the loop with flat compensation ($H_c[s] = 1$) in a Saber simulation of the analog system (shown in Figure 2.9) and then coarsely maximizing the integrator gain, k_i, such that the system settled quickly (to avoid unnecessarily long simulation times), but was still stable. Using this process, a value of 4 k (72 dB) was chosen for k_i.

Uncompensated Loop Gain Measurement

Loop gain measurements could not be made using traditional AC simulation techniques since they rely on static linearization of the system, which is not possible in the case of the subject converter (or any switching converter). To circumvent this problem, I used a time-domain signal analysis (TDSA) tool in Saber that emulates the behavior of a network analyzer. The TDSA tool stimulates the system with a sequence of discrete frequencies in time domain and then measures* the system's response to each stimulus frequency to derive frequency response. This yielded the four corner-case uncompensated loop gain measurements shown in Figure 2.12 and Figure 2.13.

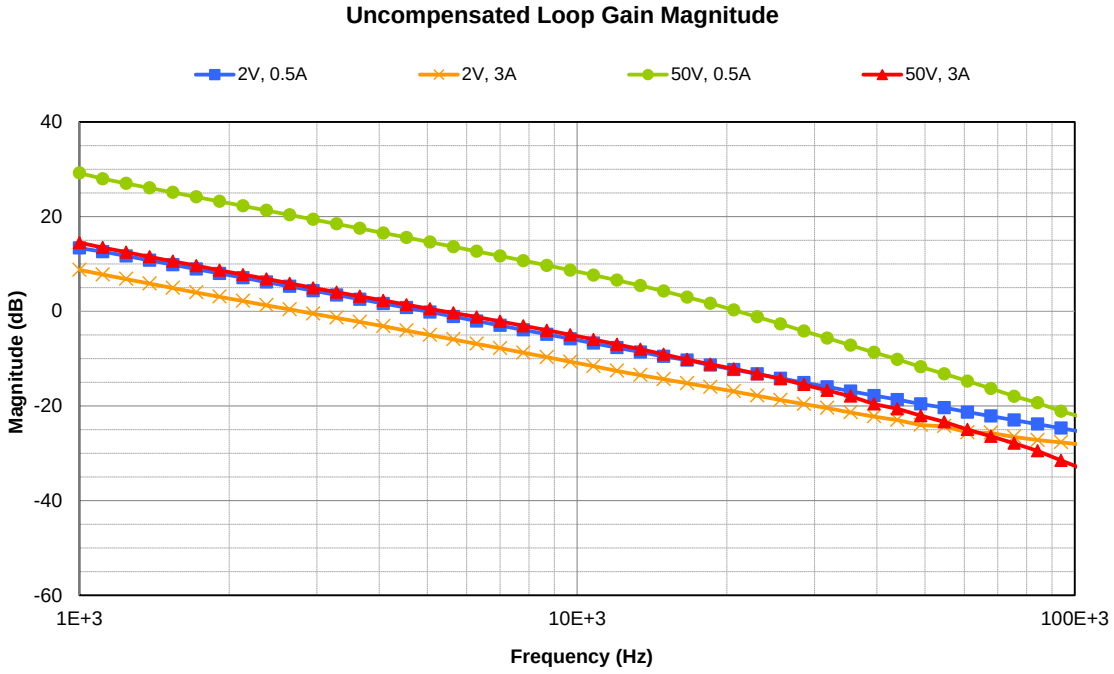


Figure 2.12 – Magnitude of the corner-case loop gain measurements of the uncompensated analog system, captured in simulation.

* Prior to measurement, Saber's TDSA tool filters the system's response to the stimulus with a high-Q band pass filter with the goal of rejecting all spectral content other than the stimulus frequency.

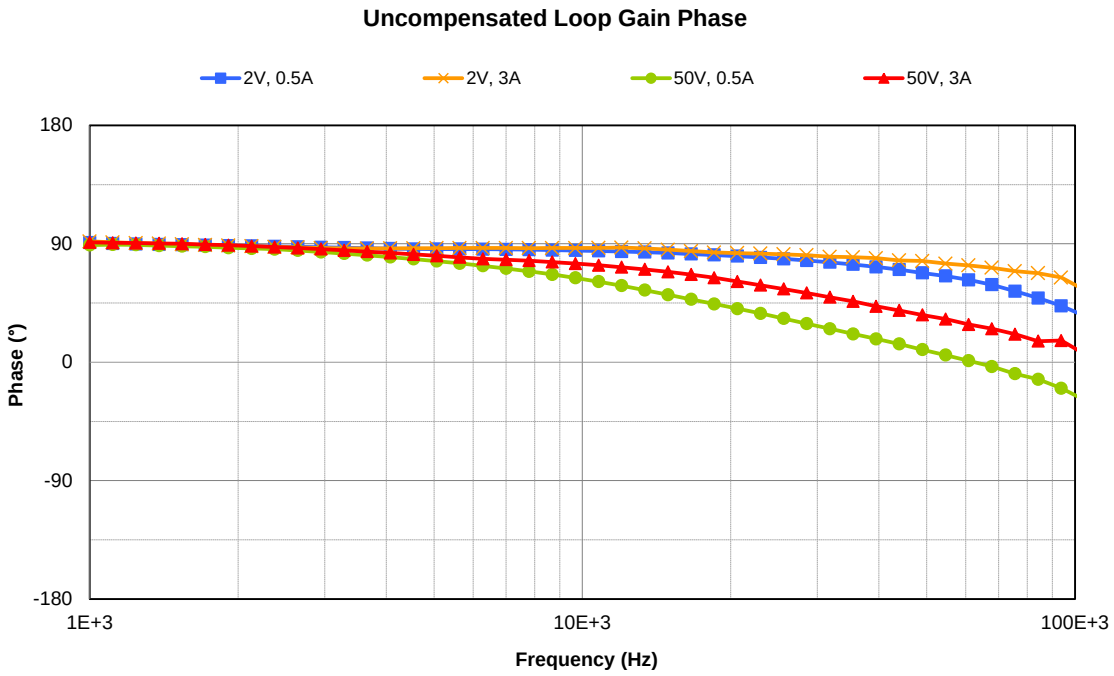


Figure 2.13 – Phase of the corner-case loop gain measurements of the uncompensated analog system, captured in simulation.

Compensator Design

Using this uncompensated loop gain data, I selected my compensator gain and pole / zero locations to maximize the worst-case control bandwidth while maintaining minimum gain and phase margins of 6 dB and 60° in the four corner cases. The *s*-domain integrator and compensator parameters that resulted from this process are shown in Table 2.6 and the implied transfer function's frequency response is plotted in Figure 2.14.

Parameter	Value
k_i	4 k
k_{dc}	1.67
s_{z1}	-128 + j160 krad/s
s_{z2}	-128 – j160 krad/s
s_{p1}	-217 + j271 krad/s
s_{p2}	-217 – j271 krad/s

Table 2.6 – Table of the analog compensator and integrator parameters resulting from the classical analog compensation exercise.

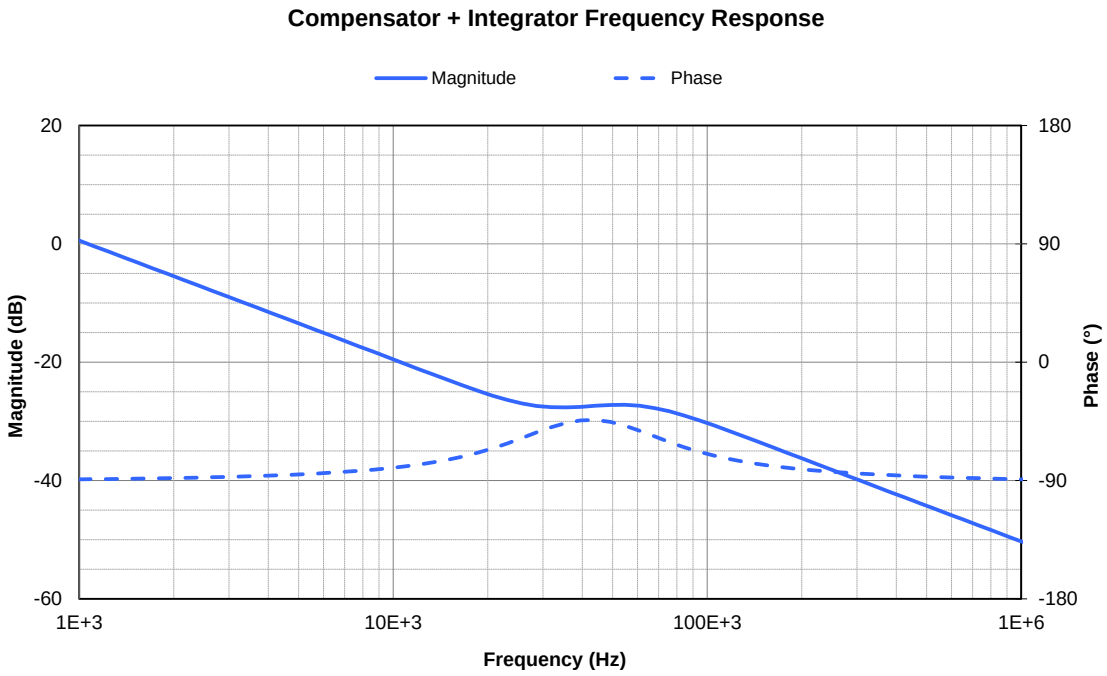


Figure 2.14 – Plot of the transfer function of the analog controller implied by the parameters in Table 2.6.

Results

The compensator implied by the parameters in Table 2.6 was implemented and the simulation was re-run. Plots of the resultant compensated corner-case loop gains are shown in Figure 2.15.

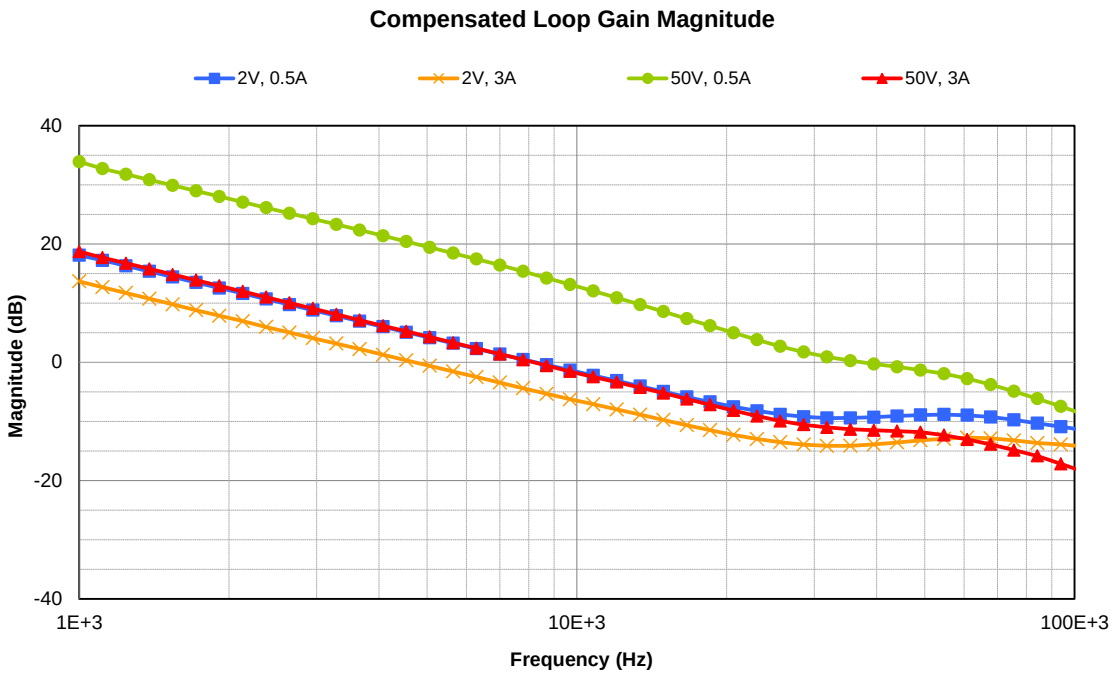


Figure 2.15 – Magnitude of the corner-case loop gain measurements of the compensated analog system, captured in simulation.

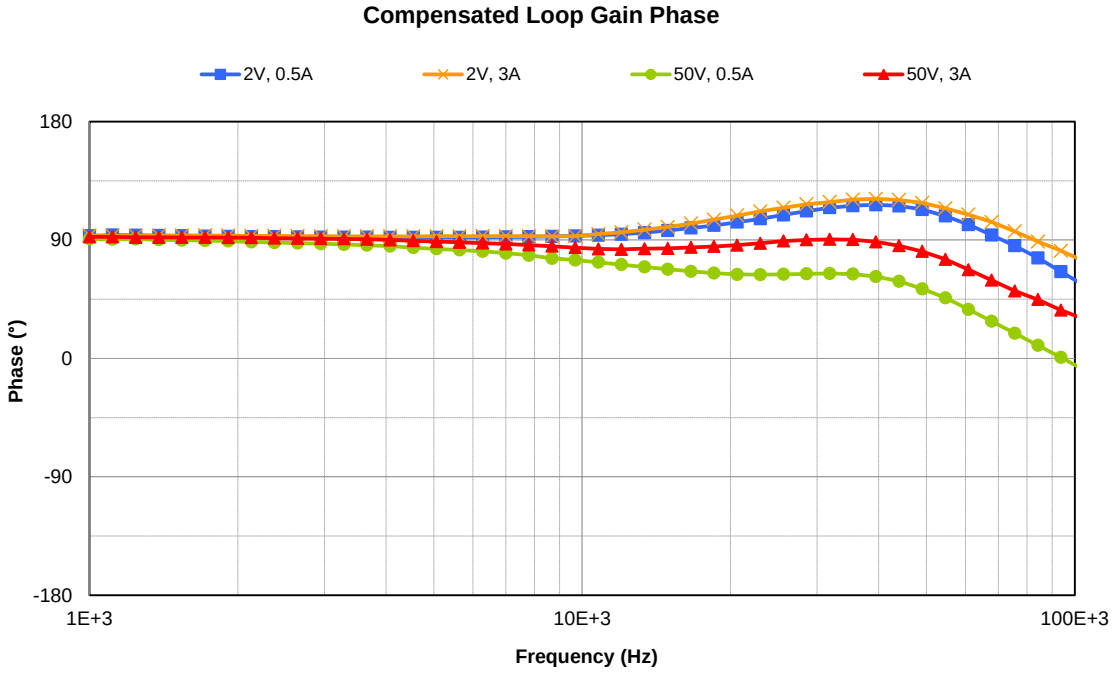


Figure 2.16 – Phase of the corner-case loop gain measurements of the compensated analog system, captured in simulation.

Take note of the large overall loop gain variation (~20 dB) with operating point in Figure 2.15. This translates into a similarly large variation in loop gain cross-over frequencies (~10:1) which results in inconsistent control-to-output frequency response characteristics (see Figure 2.17 and Figure 2.18) and transient behavior. The compensated system's response to a 10% input step and 1 V load transient are shown in Figure 2.19 and Figure 2.20, respectively. Results under all four corner-case conditions are summarized in Table 2.7.

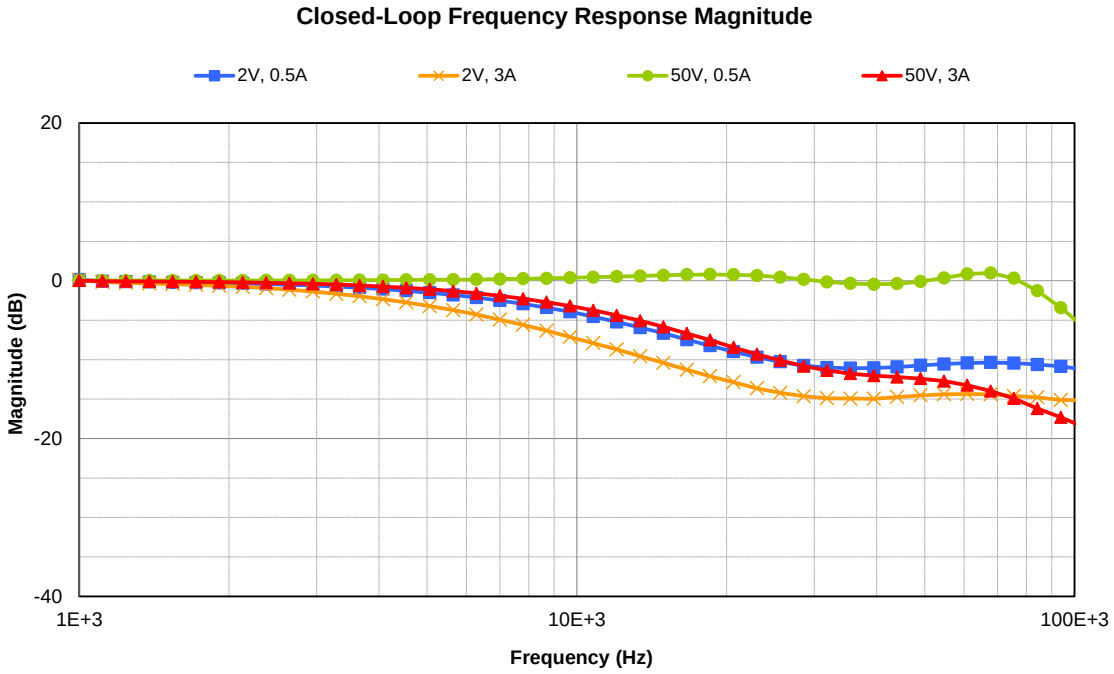


Figure 2.17 – Magnitude of the corner-case control-to-output frequency response measurements of the compensated analog system, captured in simulation.

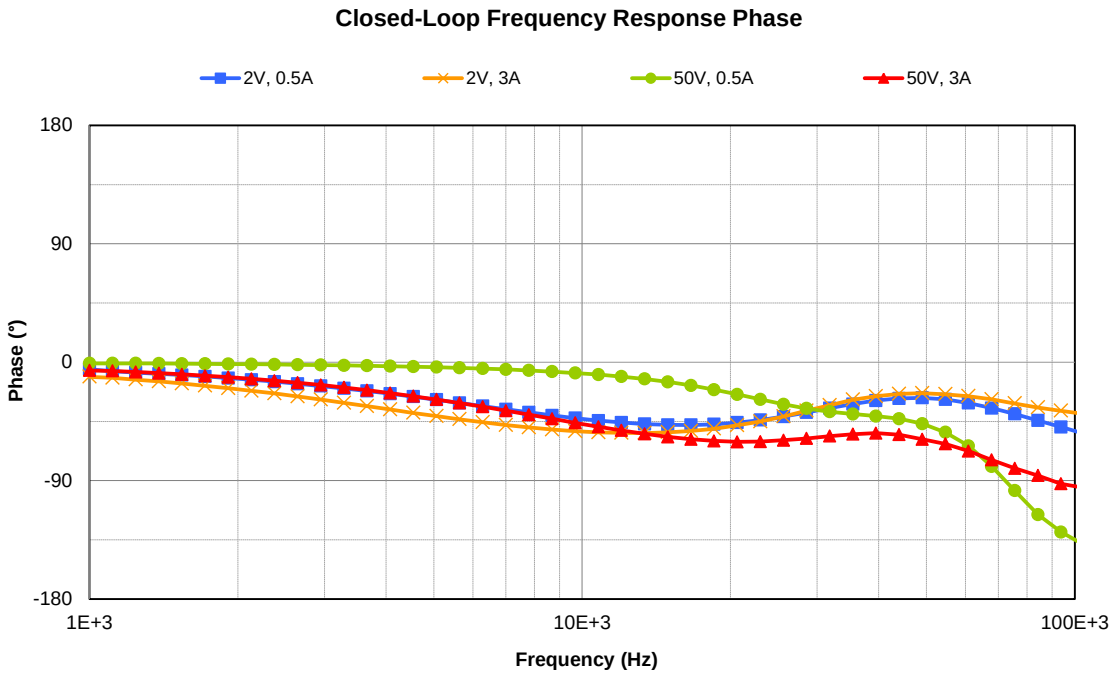


Figure 2.18 – Phase of the corner-case control-to-output frequency response measurements of the compensated analog system, captured in simulation.

Operating Point		Loop Gain Cross-over Frequency	Phase Margin	Gain Margin	Control-to-Output B.W. (-3 dB)
2 V	**0.5 A**	8.2 kHz	93°	15 dB	7.9 kHz
2 V	**3 A**	4.7 kHz	93°	14.5 dB	4.8 kHz
50 V	**0.5 A**	37 kHz	63°	7.5 dB	91 kHz
50 V	**3 A**	8.2 kHz	86°	23 dB	9.2 kHz

Table 2.7 – Summary of key simulated results of the compensated analog system at the four corner-case operating points.

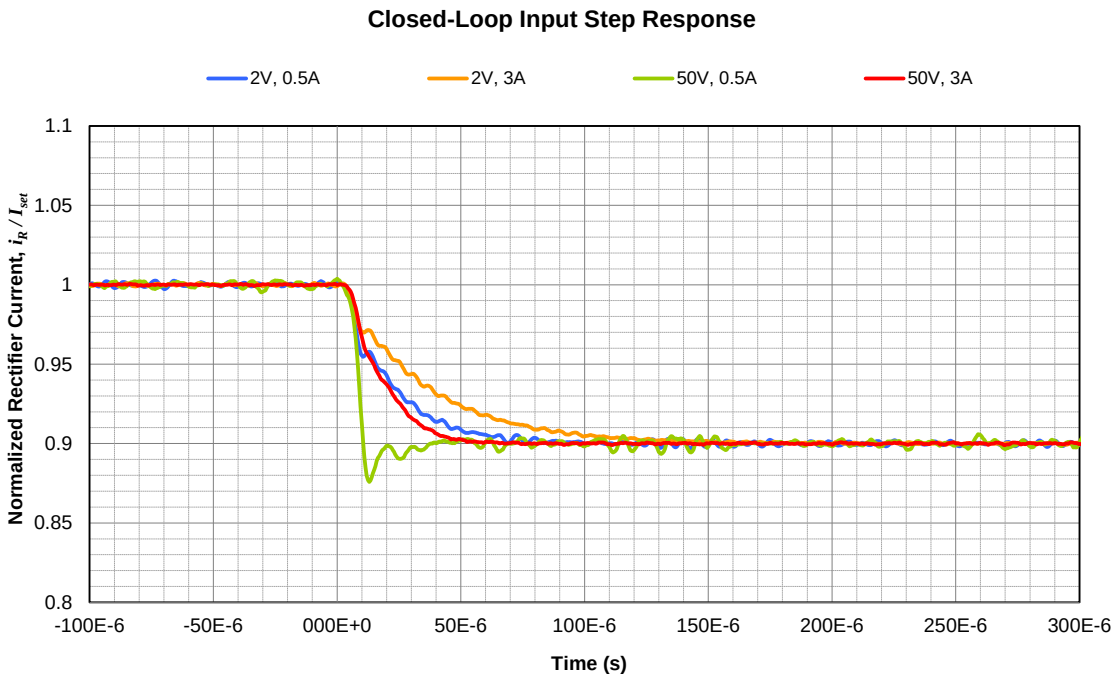


Figure 2.19 – Simulated corner-case closed-loop response of the analog system's average* rectifier current to a step in the current set point from 100% to 90%.

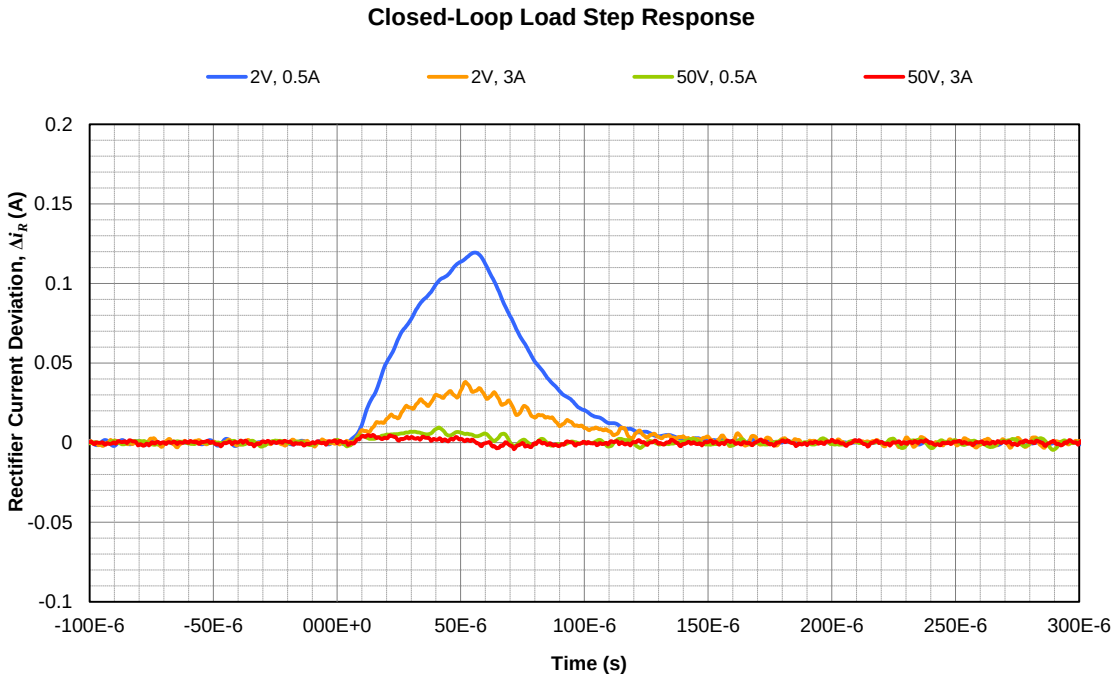


Figure 2.20 – Simulated corner-case closed-loop response of the analog system's average* rectifier current to a 1 V, 50 µs load step.

* Ripple was filtered using a 200 kHz 8th-order elliptic low-pass filter with 1 dB / 80 dB pass- / stop-band ripple.

Chapter 3: Digital Controller Infrastructure

3.1 Modulator Design and Modeling

Design and Modeling

The purpose of the modulator in this system is to provide the controller with a means of generating and actuating the switching frequency of the converter being controlled, in essence creating a variable frequency square wave oscillator. Since the system in which the controller will be implemented (either an FPGA or a microprocessor) is fundamentally time-based, it is easier to control the switching frequency by way of the switching period, avoiding the necessity to compute a reciprocal in real-time. This can be easily accomplished with the ideal simple period modulator shown in Figure 3.1.

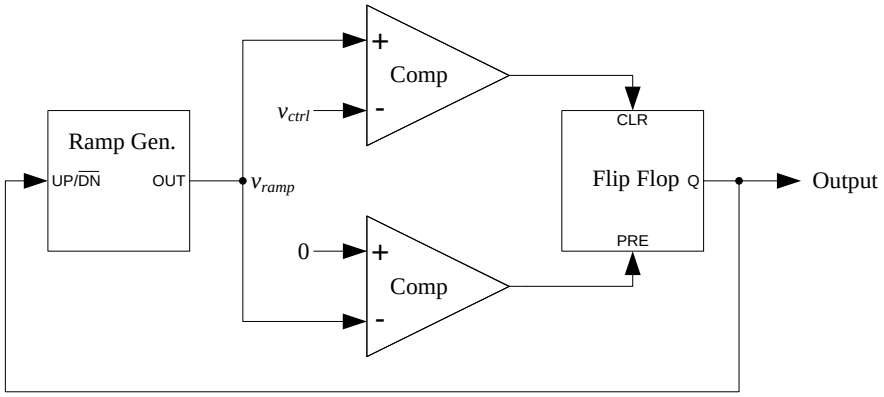


Figure 3.1 – Simple period modulator.

In the simple period modulator, a comparator monitors a ramp and reverses its direction once a threshold voltage of V_{ctrl} is crossed. When the ramp reaches zero again, another comparator reverses its direction again and the next cycle begins. The direction control signal for the ramp is the output signal, which has a steady-state period of

$$T_{sw} = \frac{2V_{ctrl}}{M_{ramp}} \tag{3.1}$$

where M_{ramp} is the slope of the ramp in V/s. Typical waveforms of this simple period modulator are shown in Figure 3.2.

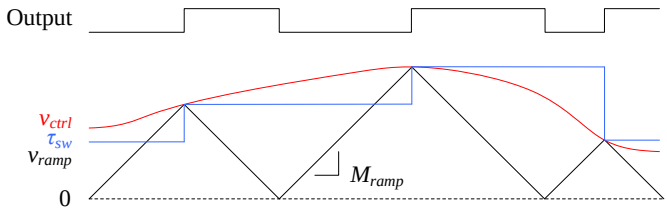


Figure 3.2 – Typical waveforms of the simple period modulator.

The simple period modulator modulates the rising edge of the square wave output, effectively sampling the input signal once per switching period. Based on the waveforms shown in Figure 3.2, a small-signal model of this modulator can be created using an ideal sampler and zero-order-hold, as shown in Figure 3.3.

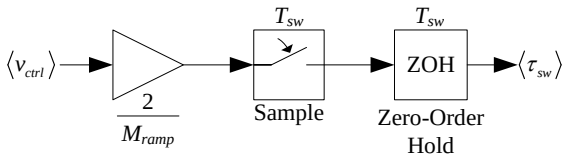


Figure 3.3 – Small-signal model of the simple period modulator. Angled brackets denote small-signal quantities.

Using Laplace transforms, the transfer function of the small-signal model shown in Figure 3.3 can easily be computed to be

(3.2)
$$H_{simple}[s] = \frac{2}{M_{ramp}} \frac{1 - e^{-sT_{sw}}}{sT_{sw}}$$

which yields the normalized frequency response shown in Figure 3.4.

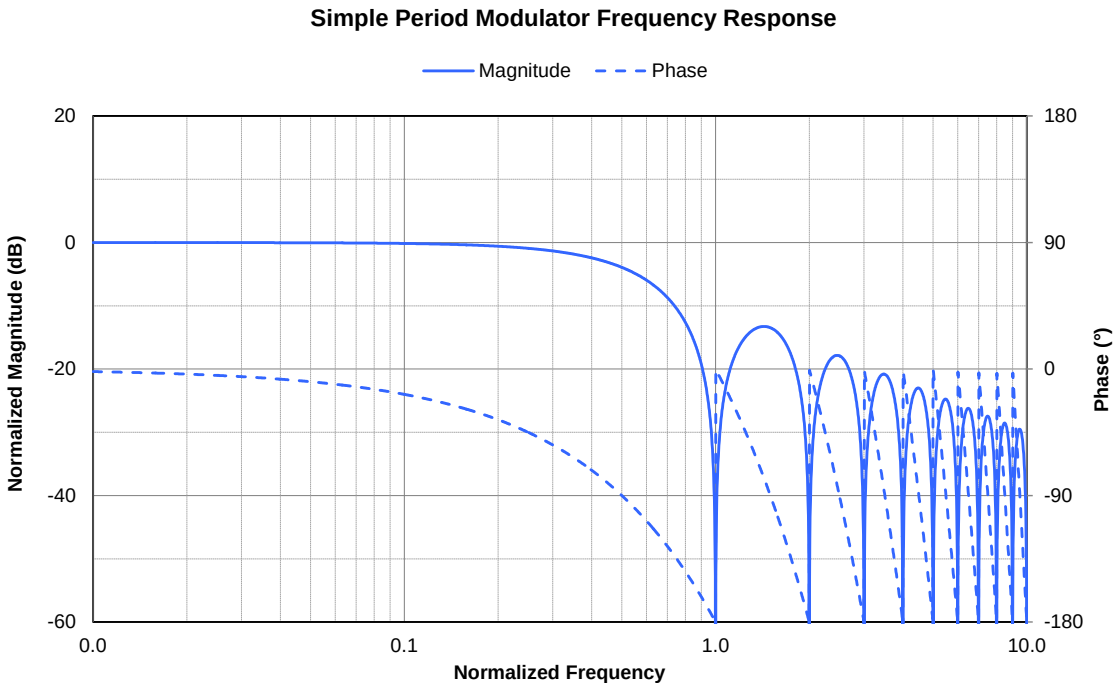


Figure 3.4 – Frequency response of the simple period modulator, normalized to the switching frequency.

The expression in equation (3.2) can be re-arranged and equivalently expressed as

(3.3) $$H_{simple}[s] = \frac{2}{T_{sw} M_{ramp}} \frac{1}{s} \mathrm{Sinh}\left[\frac{s T_{sw}}{2}\right] e^{-\frac{s T_{sw}}{2}}$$

the last term of which implies a delay of $T_{sw}/2$, which is the reason for the phase lag seen in Figure 3.4 at frequencies approaching the switching frequency. Seeking to reduce this phase lag, I created the improved modulator shown in Figure 3.5 that modulates both edges of the square wave thereby doubling the effective sample rate.

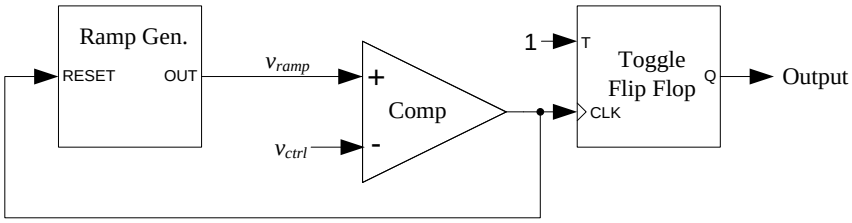


Figure 3.5 – Improved period modulator.

The typical waveforms and model of the improved modulator are shown in Figure 3.6 and Figure 3.7, respectively.

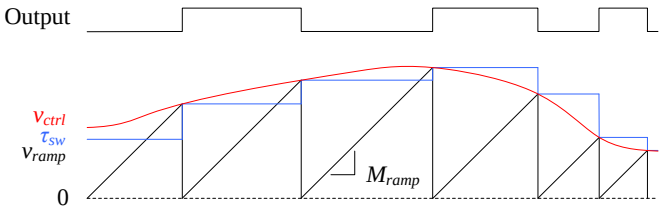


Figure 3.6 – Typical waveforms of the improved period modulator.

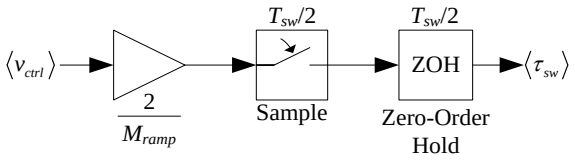


Figure 3.7 – Small-signal model of the improved period modulator. Angled brackets denote small-signal quantities.

As before, the transfer function of the small-signal model shown in Figure 3.7 can easily be computed to be

(3.4) $$H_{improved}[s] = \frac{4}{M_{ramp}} \frac{1 - e^{-\frac{s T_{sw}}{2}}}{s T_{sw}}$$

which yields the normalized frequency response shown in Figure 3.8 alongside that of the simple period modulator (for comparison).

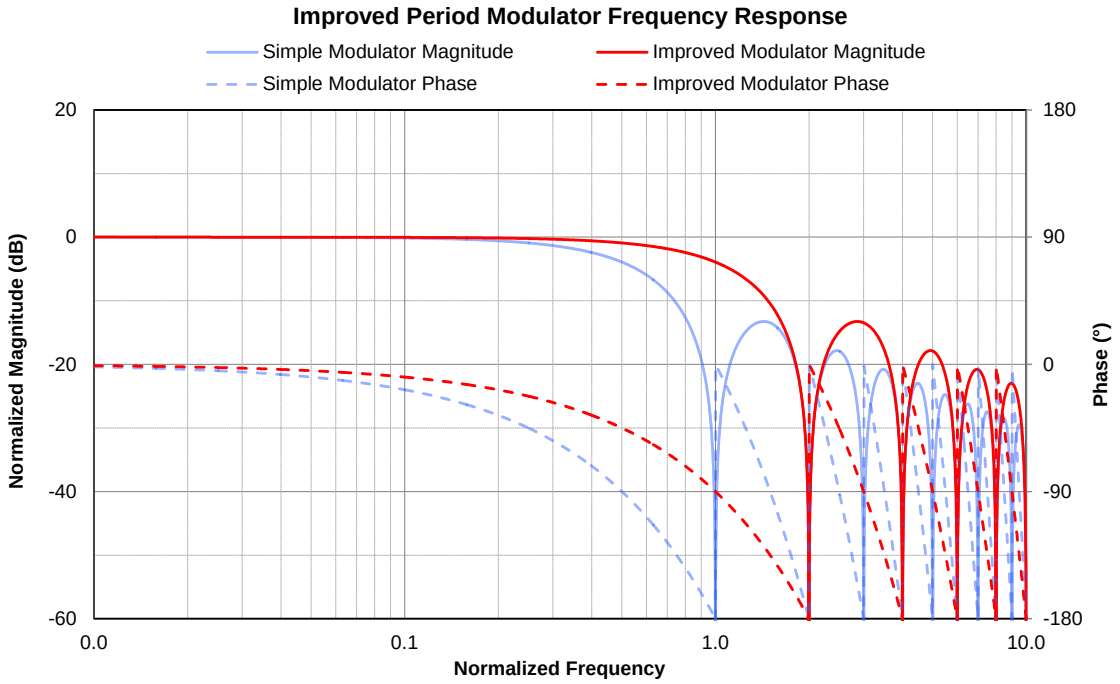


Figure 3.8 – Frequency response of the improved period modulator (in red), normalized to the switching frequency. The simple period modulator's response in also shown (in light blue) for reference.

As before, re-arranging the expression in equation (3.4) yields

$$H_1[s] = \frac{4}{T_{sw} M_{ramp}} \frac{1}{s} \mathrm{Sinh}\left[\frac{s T_{sw}}{4}\right] e^{-\frac{s T_{sw}}{4}} \tag{3.5}$$

the last term of which implies a delay of $T_{sw}/4$, resulting in a reduction in phase lag by a factor of two when compared with the simple period modulator. This is a significant improvement that enables higher control bandwidths.

Quantization and Its Effects

The improved modulator shown in Figure 3.5 is asynchronous and therefore operates in continuous time. Since the controller being designed will be digitally implemented, a synchronous (discrete-time) variant of this modulator was necessary. It is shown in Figure 3.9.

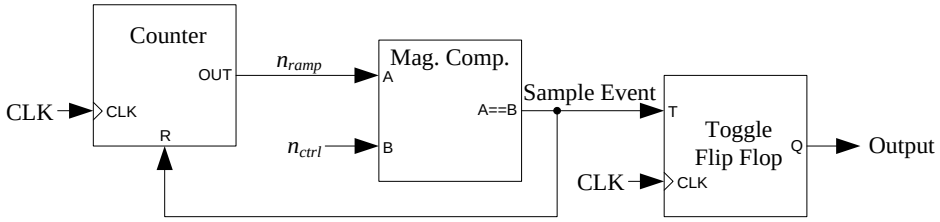


Figure 3.9 – Synchronous version of the improved period modulator of Figure 3.5.

Neglecting quantization effects, the relationship between the input of the synchronous modulator, n_{ctrl}, and period of its output signal, τ_{sw}, can be expressed as

(3.6) $$\tau_{sw} = 2T_{CLK}\left(n_{ctrl}+1\right)$$

Since this implementation is synchronous, the period of the modulated square wave it generates is quantized. Including quantization effects, (3.6) becomes

(3.7) $$Q\left[\tau_{sw}\right] = 2T_{CLK}\left(n_{ctrl}+1\right) \qquad \text{where } n_{ctrl} \in \{0,1,2,3,\ldots\}$$

which implies that the switching period is effectively quantized to integer multiples of twice the clock period, or

(3.8) $$\Delta\tau_{sw} = 2T_{CLK}$$

A model of the improved modulator including quantization is shown in Figure 3.10.

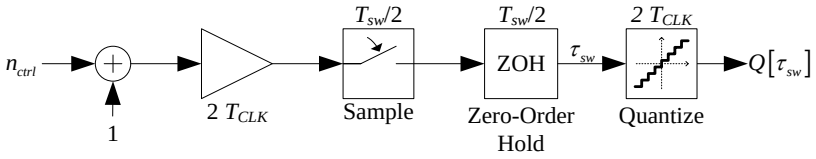


Figure 3.10 – Model of the synchronous improved modulator of Figure 3.9 including quantization effects.

The switching period quantization interval from (3.8) implies a switching frequency quantization interval that can be expressed as

(3.9) $$\left|\Delta f_{sw}[\tau_{sw}]\right| = \Delta\tau_{sw}\frac{\partial f_{sw}}{\partial \tau_{sw}} = \Delta\tau_{sw}\frac{\partial}{\partial \tau_{sw}}\left(\frac{1}{\tau_{sw}}\right) = -\frac{2T_{CLK}}{\tau_{sw}^{\,2}}$$

Expressing this in terms of normalized switching frequency yields

(3.10) $$\left|\Delta\omega_n[\omega_n]\right| = \frac{2f_0}{f_{CLK}}\omega_n^{\,2}$$

where f_{CLK} is the clock frequency (equivalent to $1/T_{CLK}$) and ω_n is the normalized switching frequency (equivalent to f_{sw}/f_0). Expression (3.10) is plotted in Figure 3.11.

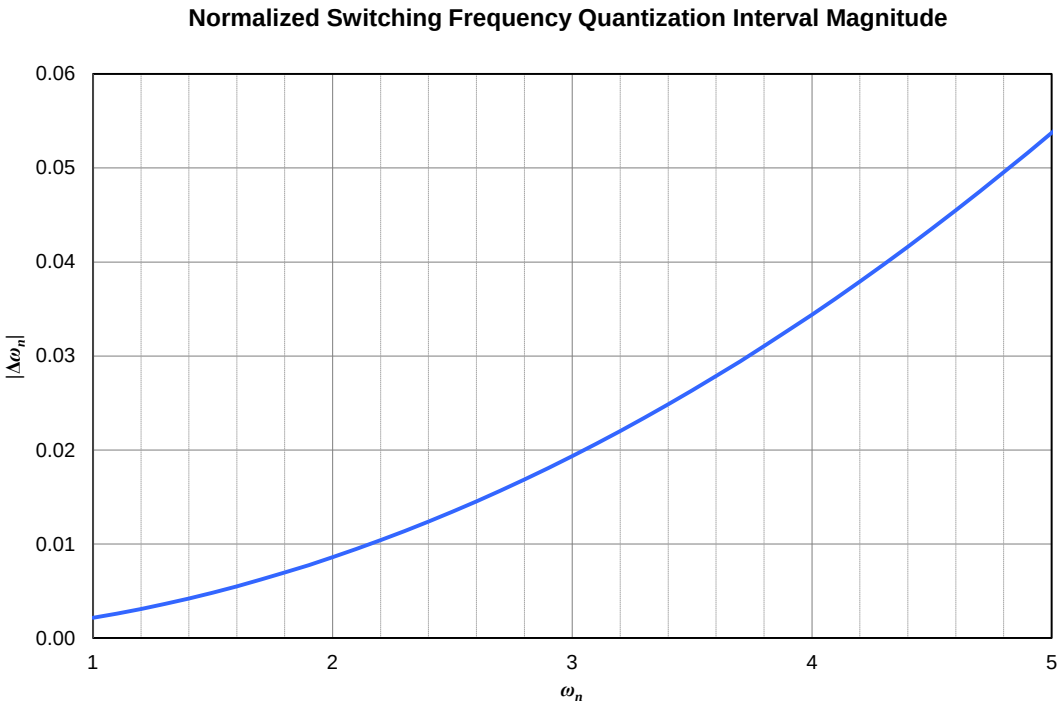


Figure 3.11 – Normalized plot of the magnitude of the normalized switching frequency's quantization interval resulting from the synchronous modulator implementation of Figure 3.9. Assumes a clock frequency of 200 MHz.

This switching frequency quantization implies a finite set of achievable steady-state operating curves. The density of those operating curves versus operating point is illustrated in Figure 3.12, assuming a τ_n quantization interval of 0.025 (for clarity). In the case of the subject converter, a 200 MHz clock frequency plugged into equation (3.7) yields an actual normalized switching period quantization interval of 0.00215. This implies an actual set of curves for the subject converter that is approximately 12 times denser than that shown in Figure 3.12.

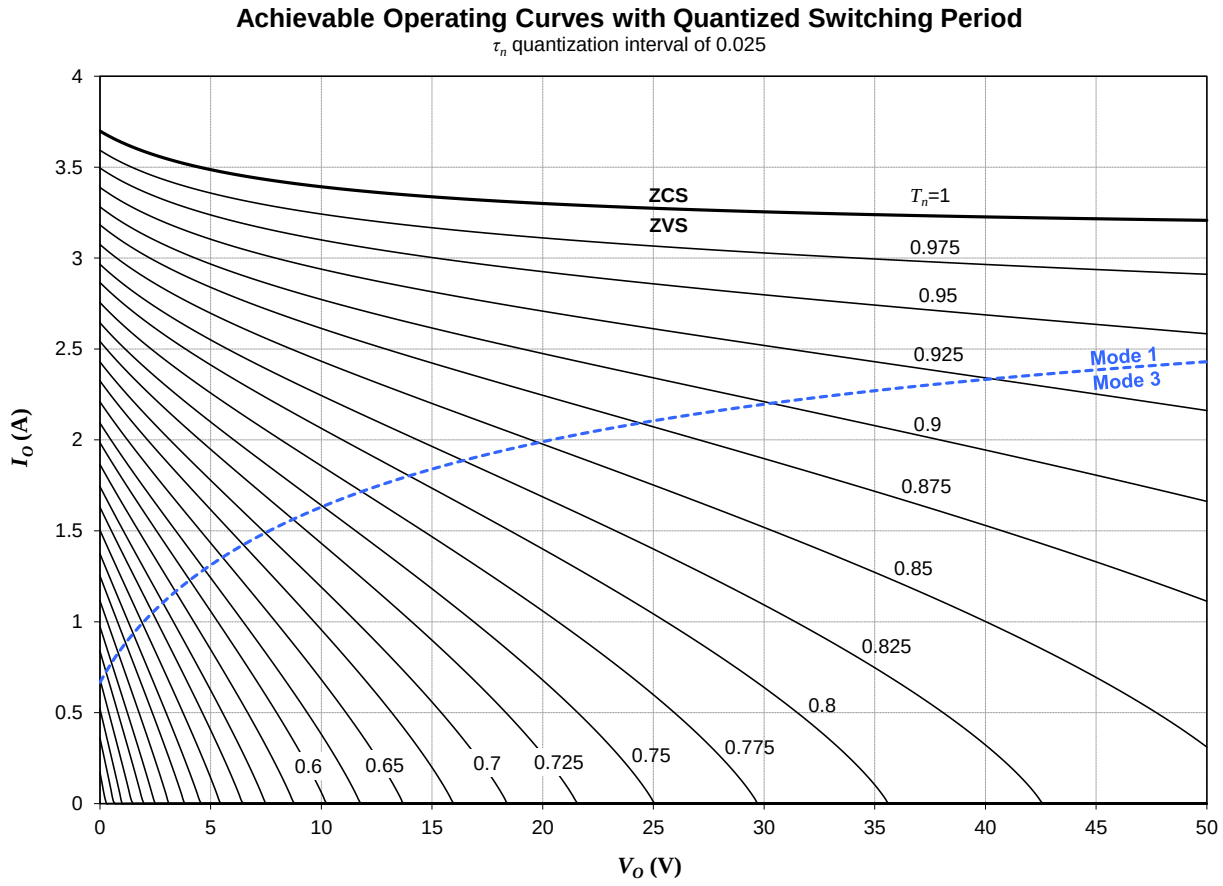


Figure 3.12 – Plot showing the density of achievable operating curves vs. operating point, assuming a τ_n quantization interval of 0.025 (for clarity). The subject converter has approximately 12 times the density shown.

For a given load line, this finite set of operating curves implies a finite set of achievable steady-state operating points where the load line and the curves intersect. The vertical distance between any two adjacent points along the load line implies the effective current quantization interval at that operating point. This implies that a steeper load line (lower impedance) necessarily results in a larger quantization interval. Because the large output filter capacitor acts like a voltage source at all but the lowest of frequencies, the AC load line is effectively vertical at all operating points.

This quantization is undesirable because its presence inside the proposed closed-loop control system will create steady-state limit cycling (or idle tones) in the output current. This occurs because the control loop's practically infinite DC gain will cause it to force the converter to 'bounce' between the two nearest achievable operating points at whatever duty cycle necessary to achieve the desired average current. This limit cycle will result in the average output current sub-harmonically 'oscillating' with a peak-to-peak amplitude equal to the current quantization interval and at a frequency that could vary anywhere between 0 and $f_{sw}/2$, depending on operating point. Since 200 MHz is the fastest that I could practically expect to operate my modulator in an FPGA or processor (without using special techniques or application-specific

silicon), this effect would result in a worst-case current quantization interval of ~75 mA, which is very significant and could not be neglected.

Normalization

For convenience, the period modulator can be controlled in terms of normalized switching period, τ_n, by computing n_{ctrl} in terms of τ_{sw} from (3.7), substituting τ_n/f_0 for τ_{sw}, yielding

$$n_{ctrl} = \frac{\tau_n}{2T_{CLK} f_0} - 1 \tag{3.11}$$

and adding a corresponding correction to the synchronous period modulator of Figure 3.9. The resultant gain-corrected synchronous improved period modulator design is shown in Figure 3.13, along with its corresponding model in Figure 3.14.

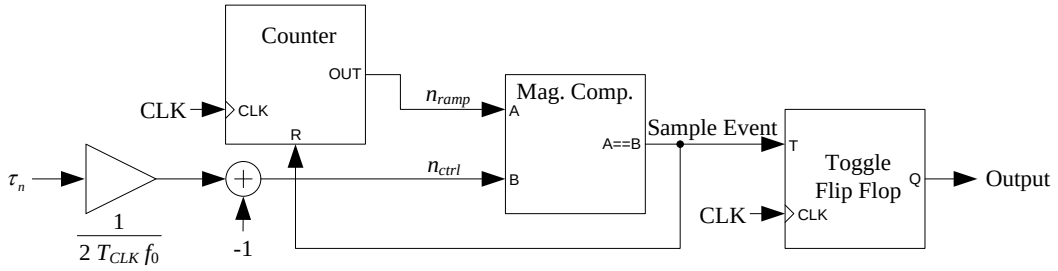


Figure 3.13 – Gain-corrected version of the synchronous improved period modulator of Figure 3.9, where τ_n represents the desired normalized switching period.

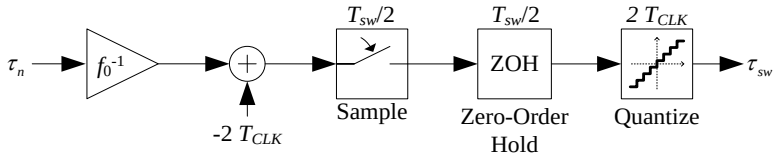


Figure 3.14 – Model of the gain-corrected synchronous improved period modulator of Figure 3.13, including quantization effects.

Dithering

To reduce the impact of modulator quantization, I investigated two alternatives: noise-shaping and dithering. Noise shaping is an approach which wraps a linear feedback loop around the quantizing element, effectively changing the spectrum of the resultant quantization noise to be more heavily weighted towards high frequencies [12]. This approach is commonly used in open-loop applications, such as delta-sigma data converters and down-sampling in digital audio processing. It seemed promising at first, but I soon became concerned with the lack of a lower bound on the resultant quantization noise spectrum, which implied that there would still be limit cycles at frequencies well below the output filter's cutoff frequency at certain operating points.

I next considered dithering, which is a process that injects (generally) uniformly-distributed noise prior to quantization. To be effective, the amplitude of the noise must be sufficient to practically de-correlate the quantization noise and the signal being quantized [19]. Dithering using white noise would also cause an increase in output noise below the output filter's cutoff frequency, but it would be distributed over a broad spectrum instead of a single frequency, which is an improvement over noise shaping. The addition of a filter to limit the spectrum of the injected dithering noise (known as 'colored' dithering) to be above the output filter's cutoff frequency* substantially reduced the residual noise observed at the output. Figure 3.15 shows a diagram of the period modulator including colored dithering.

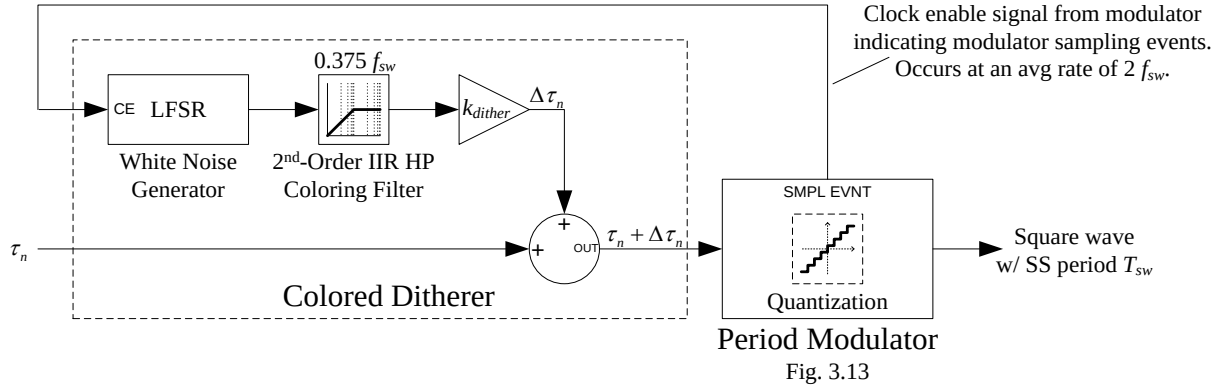


Fig. 3.13

Figure 3.15 – Block diagram of the dithered period modulator system.

The injection gain, k_{dither}, was chosen such that the peak-to-peak injected noise amplitude was approximately 4 times greater than the modulator's quantization interval. To achieve consistent dithering at all operating points without risking aliasing, the dithering noise is generated, filtered, and injected on a sample-by-sample basis at the modulator's switching frequency. Since the modulator's frequency varies with operating point, so does the spectrum of the injected noise. The bounds on the injected noise spectrum are proportional to the switching frequency and are shown in Figure 3.16, using a coloring filter consisting of a second-order, high-pass IIR filter section with a Chebyshev Type 1 prototype, a cut-off frequency of 0.375 f_{sw}, and a passband ripple spec of 2 dB.

* Based on the subject converter's output capacitor value (from Figure 2.6) and minimum open-loop output impedance (inferred from the constant frequency curves in Figure 2.7 to be ~3Ω), the maximum corner frequency of the output filter is ~113 Hz.

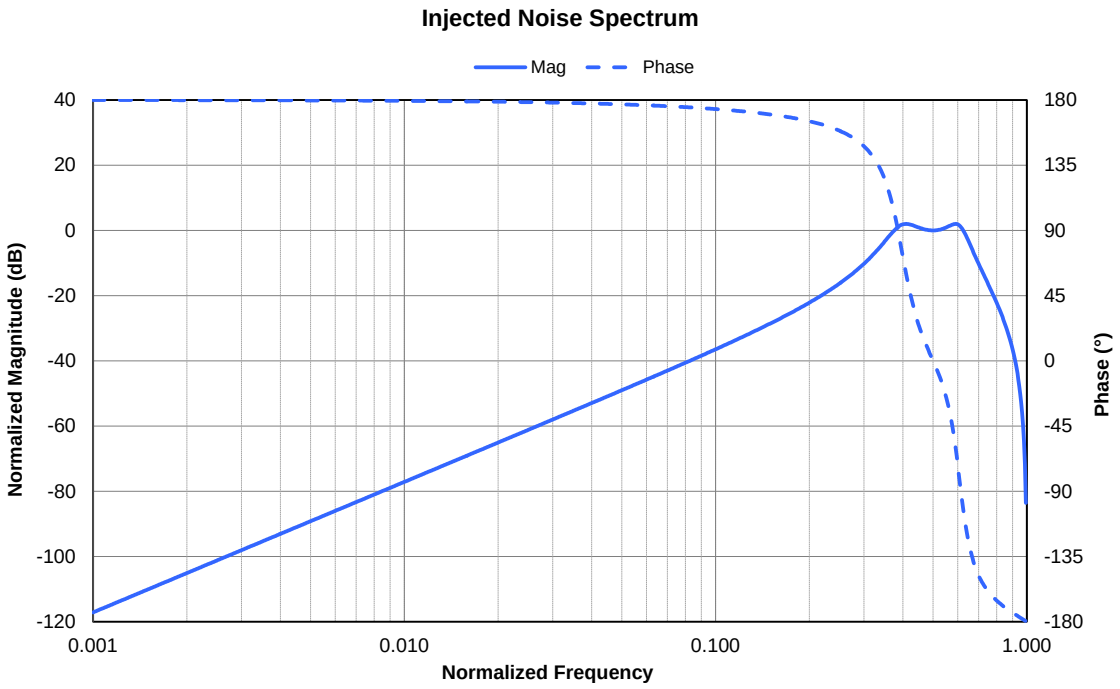


Figure 3.16 – Graph showing the normalized spectrum of the noise injected as part of colored dithering, normalized to the switching frequency.

3.2 Feedback Signal Selection and Sensor Design

I chose the rectifier current, i_R, as the controlled parameter instead of the output current, I_O, or voltage, V_O, since it is not subject to the low frequency pole created by the converter's substantial open-loop output impedance[*] and output filter capacitor, C_O. This allowed me to achieve much wider control bandwidth than practical by sensing I_O directly while still allowing me to control I_O indirectly by controlling the average of i_R.

In addition to rectifier current, output voltage needed to be fed-back for use by the gain-scheduling controller (see Chapter 5). Resonant capacitor voltage and resonant inductor current were not considered as additional feedback parameters because they could not be effectively measured at the chosen sample rate of 2.778 MS/s (see Section 3.3) given switching frequencies greater than 750 kHz at some operating points.

The sensors to measure output voltage and rectifier current consist of nothing more than a differential amplifier and a differential amplifier coupled to a current-sensing resistance, respectively. Figure 3.17 shows a simplified schematic of the converter including the sensor circuits. A complete circuit schematic is shown in on page 93 in Section C.1.

[*] The subject converter's minimum open-loop output impedance is ~3 Ω, as inferred from the constant frequency curves in Figure 2.7.

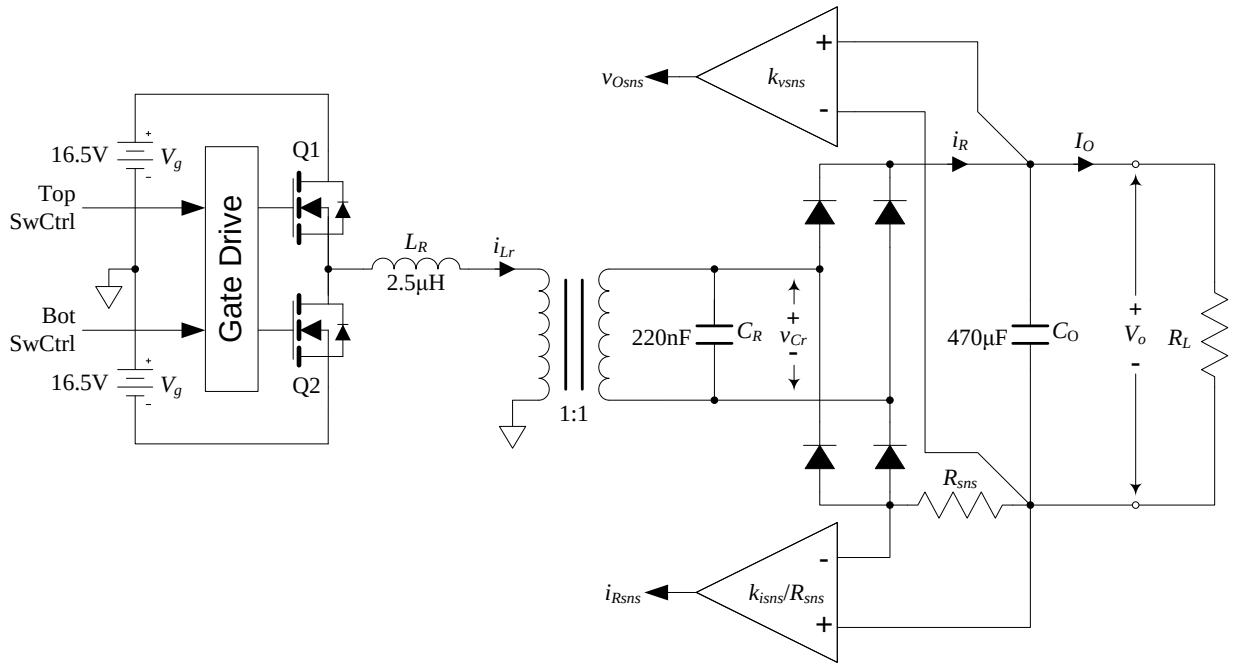


Figure 3.17 – Simplified schematic of the subject converter including feedback sensors.

3.3 Analog to Digital Conversion

Since the feedback signals provided by the sensor circuits described in Section 3.2 are analog voltages, they must be converted into the digital domain (meaning made discrete-time and quantized) before being fed into the digital controller. For this task, I considered three types of analog-to-digital converters (ADCs): delta-sigma (Δ-Σ), successive approximation (SAR), and a custom over-sampling architecture.

Delta-Sigma Converter

Off-the-shelf Δ-Σ converters grossly over-sample* a signal at low resolution and then decimate the result to yield a high-resolution stream of digital samples at the desired data rate. Figure 3.18 shows a simplified model of a Δ-Σ converter system which, for clarity, omits noise-shaping and multi-stage decimation.

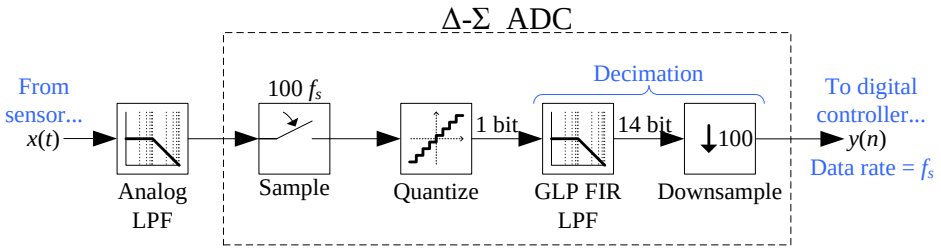


Figure 3.18 – Simple model of an ADC system using an off-the-shelf 100:1 oversampling Δ-Σ ADC.

* Roughly 40 to 100 times faster than necessary to meet the Nyquist criterion for the highest frequency of interest.

The advantage of this approach is that the high initial sample rate effectively eliminates the need for all but the most basic of anti-aliasing filters, thereby simplifying the analog circuitry required and practically eliminating the phase lag created by the aggressive analog anti-aliasing filters typically required with SAR converters. This approach has a significant disadvantage, however; to avoid introducing aliasing artifacts, the decimation process in off-the-shelf Δ-Σ ADCs necessarily involves filtering which is generally done by digital generalized linear phase (GLP) FIR filters. These types of filters introduce a large amount of latency, creating phase lag in the loop gain that severely limits control bandwidth.

Successive Approximation Converter

SAR converters have the advantage of being able to sample and quantize a signal in a single sampling period, while introducing only one sampling period of latency. A model of a SAR-based ADC system is shown in Figure 3.19. Assuming an appropriate sampling frequency is chosen, this adds only a relatively small amount of phase lag to the digital controller's loop gain. The disadvantage of SARs, however, is that they require aggressive analog anti-aliasing filters which add phase lag and circuit complexity.

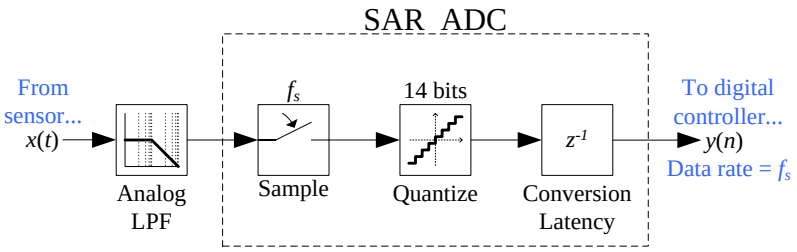


Figure 3.19 – Model of an ADC system using an off-the-shelf SAR ADC.

The effects of the disadvantages of both Δ-Σ and SAR converters can be mitigated by intentionally over-sampling the signals (yielding resultant data rates that are far in excess of the sampled signals' Nyquist rates). This assumes that: a) a cost-effective converter that has sufficiently high data rate and resolution is available and b) the digital controller is capable of processing data at the higher rate. These concerns are by no means trivial and they made over-sampling in this manner impractical in this design.

Hybrid Converter

Another ADC structure that I considered is a custom-built oversampling ADC (shown in Figure 3.20) that is somewhat of a hybrid of the Δ-Σ and SAR-style converters. It consists of a medium resolution SAR that moderately over-samples the signal of interest and then passes it to an IIR-based decimator with a filter chosen to optimize the trade-off between the attenuation of aliasing artifacts and phase lag within the target control bandwidth. At 10:1 oversampling, this approach still required a relatively aggressive analog anti-aliasing filter such that the sum of the phase lag contributed by it and the decimation filter was still more than that of the SAR arrangement mentioned above. However, I believe that with a more detailed investigation into optimizing the oversampling factor and anti-aliasing / decimation filter types and parameters, this approach has the potential to yield results superior to both of the standard Δ-Σ and SAR approaches mentioned above.

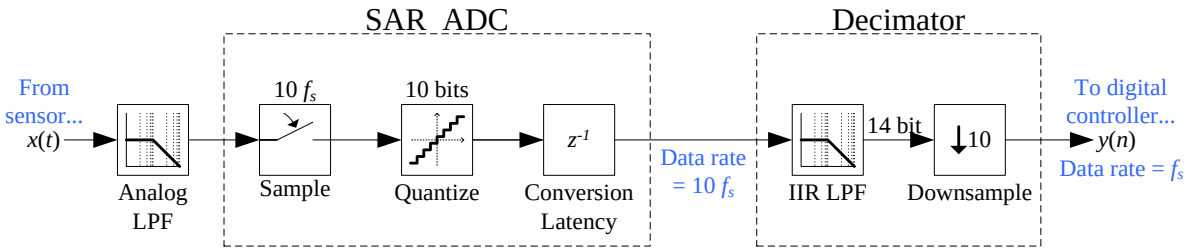


Figure 3.20 – Model of a custom-designed over-sampling ADC system.

Based on the above analysis, I chose to use a pair of readily available 14 bit SAR converters for this design, configured to sample the feedback signals at a rate of 2.778 MS/s.

3.4 Anti-Aliasing Filter Requirements and Design

The anti-aliasing filters in this design needed to satisfy three main requirements: they needed to

1. reduce aliasing artifacts from the ADC (analog to digital converter) sampling to the point of negligibility, and
2. sufficiently attenuate the rectifier current ripple such that it does not cause the ADC to either saturate or suffer a significant loss of resolution to avoid doing so.

The anti-aliasing filter design was to be dictated by whichever of these two requirements was most constraining.

ADC Anti-Aliasing Constraint

Anti-aliasing done in communications systems is typically comprehensive; it is designed to effectively eliminate aliasing altogether. This is done by choosing the beginning of the anti-aliasing filter's stopband to be at or below the Nyquist frequency ($f_s/2$, where f_s is the sampling frequency). Since this ADC is being used for feedback in a control system, I was able to specifically tailor the anti-aliasing requirements of the filter design for that application thereby reducing the filter's phase contribution. To do this, the anti-aliasing filter's stop band frequency was selected as shown in (3.12) to limit the magnitude of aliasing artifacts only within the approximate target control bandwidth, f_{bw} (since DC to f_{bw} is the frequency band of interest from the controller's perspective), ignoring any higher-frequency aliasing artifacts.

(3.12) $$f_{stopADC} = f_s - f_{bw}$$

Since f_{bw} is small relative to the sampling frequency, f_s, this allowed a near doubling of the filter's maximum cutoff frequency (as compared with comprehensive anti-aliasing) thereby substantially reducing the phase lag introduced within the frequency band of interest.

I somewhat arbitrarily decided to limit the relative amplitude of aliased artifacts within the target control bandwidth to be 80 dB below their original magnitude. This implies a constraint on the anti-aliasing filter gain magnitude of

(3.13) $$\left|H_{AA}\left[2\pi j f\right]\right| \leq -80 \text{ dB} \quad \text{for all} \quad f \geq f_s - f_{bw}$$

where the ADC sampling frequency is 2.778 MHz and the target control bandwidth 50 kHz.

ADC Ripple Constraint

Ripple was of particular concern in this controller design because one of the signals being measured is the converter's rectifier current, which is discontinuous and has a large ripple at twice the switching frequency. Figure 3.21 shows the rectifier current ripple of the subject converter at the four corner-case operating conditions, captured in simulation.

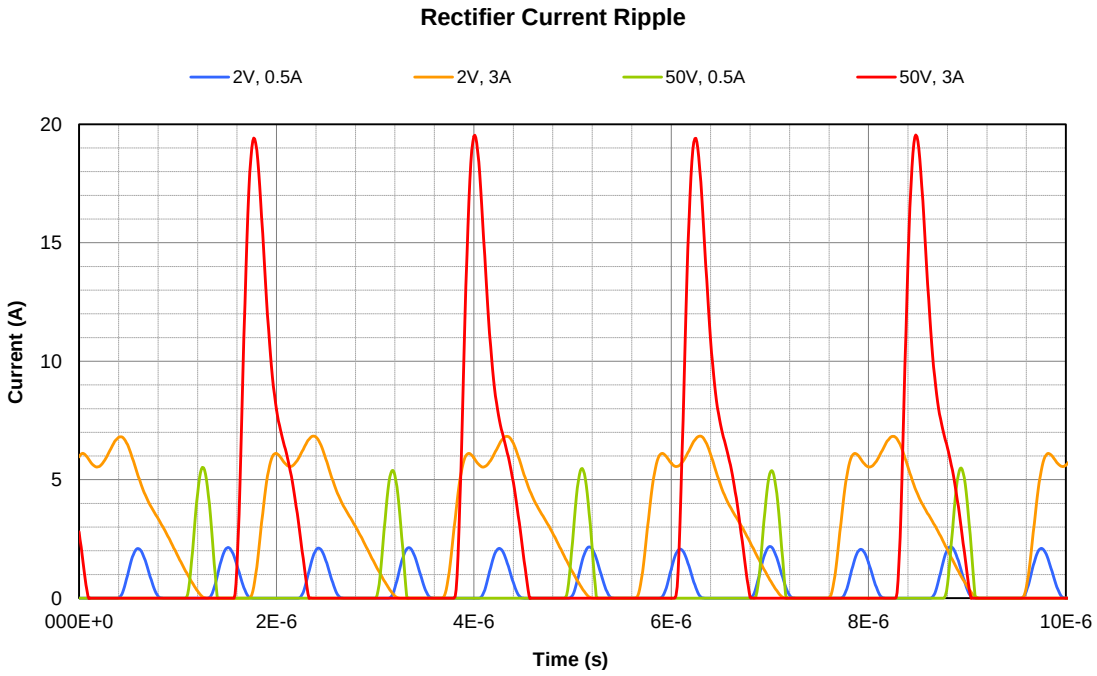


Figure 3.21 – Plot of the rectifier current, i_R, at the four corner-case operating points (from simulation).

Given the 3 A maximum DC output current rating of this converter, I somewhat arbitrarily decided that it was reasonable to tolerate a maximum peak ripple at the current sensor ADC equivalent to 1 A of rectifier current, thereby sacrificing roughly 40% of the ADC resolution to provide sufficient headroom to avoid clipping. To determine how much attenuation the filter would need to satisfy this constraint, I measured the harmonic content of the rectifier current waveforms (from Figure 3.21) in simulation. The results are shown plotted in Figure 3.22.

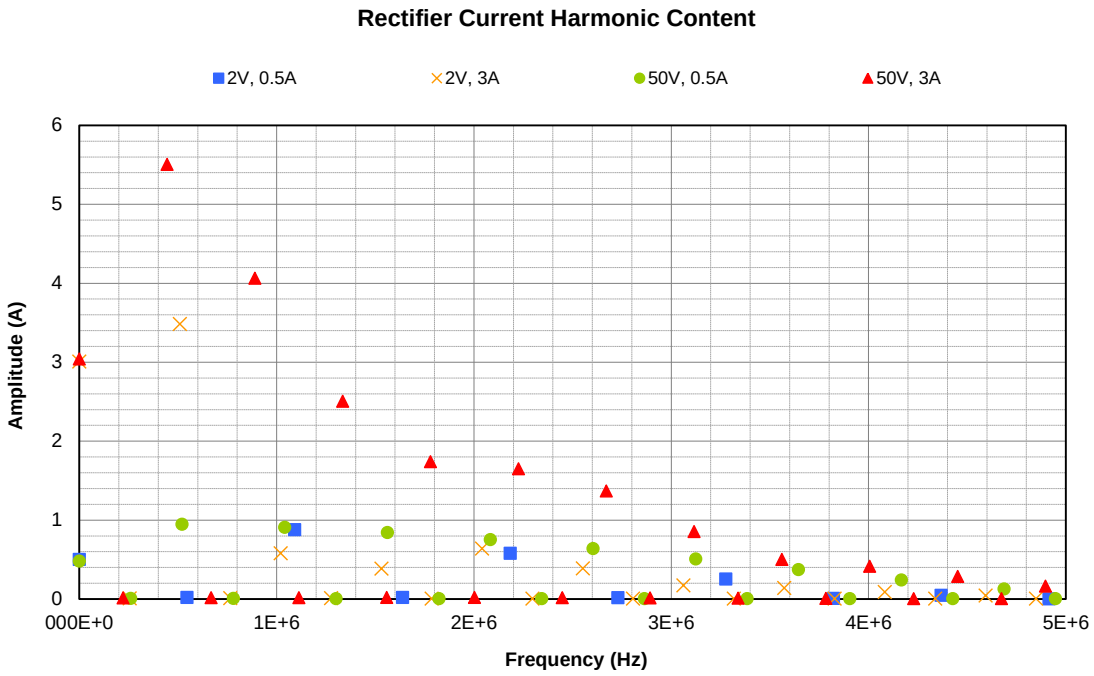


Figure 3.22 – Plot of the harmonic content of the rectifier current, i_R, at the four corner-case operating points (from simulation).

Since the anti-aliasing filter will have fairly steep roll-off, it is clear from Figure 3.22 that the only harmonic of concern is the second switching harmonic in the 50 V, 3A case, which has an amplitude of 5.5 A at 445 kHz. To satisfy the 1 A peak ripple constraint, this implies that the anti-aliasing filter must provide a minimum ripple attenuation of $5.5/1 = 5.5$ (or 14.8 dB) at 445 kHz. To further guard-band this I constrained the anti-aliasing filter to provide a minimum attenuation of 15 dB at $2 \cdot f_0$, since the minimum possible frequency where the second harmonic component could appear is twice the resonant frequency.

(3.14) $$\left| H_{AA}\left[2\pi j f\right] \right| \le -15 \text{ dB} \quad \text{for all} \quad f \ge 2 f_0$$

Filter Structure

To keep the design simple and parts count reasonable, the anti-aliasing filter was realized using two cascaded low-pass Sallen-Key filter sections, described in [13]. A typical low-pass Sallen-Key section is shown in Figure 3.23.

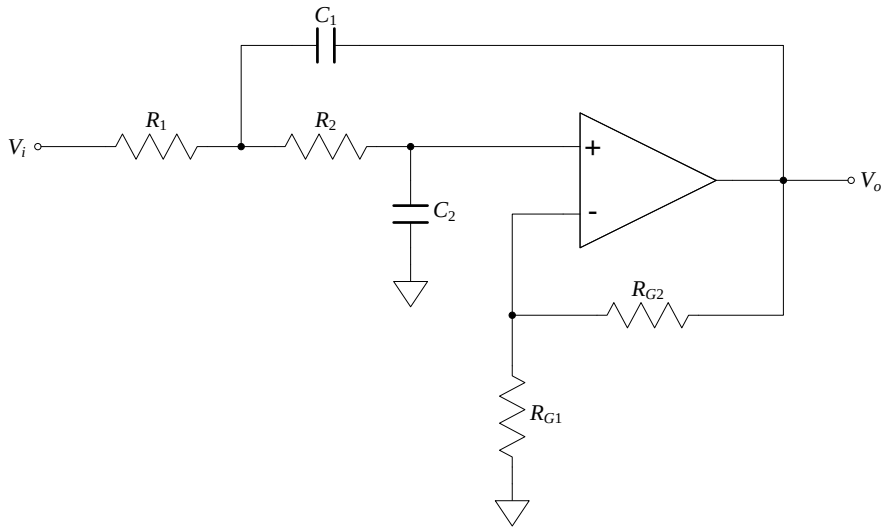


Figure 3.23 – Typical low-pass Sallen-Key filter section.

Using nodal analysis and assuming the opamp to be ideal (infinite gain at all frequencies), the transfer function $H_{SK}(s)$ from V_i to V_o of the circuit shown in Figure 3.23 can be computed to be

$$H_{SK}(s) = \frac{V_o(s)}{V_i(s)} = k \frac{1}{1 + \frac{1}{\omega_0 Q} s + \frac{1}{\omega_0^2} s^2} \tag{3.15}$$

where the DC gain, k, and complex pole pair corner frequency and quality factor, ω_0 and Q, respectively, are defined as

$$k = 1 + \frac{R_{G2}}{R_{G1}} \tag{3.16}$$

$$\omega_0 = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \tag{3.17}$$

$$Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{R_1 C_2 + R_2 C_2 - R_1 C_1 \frac{R_{G2}}{R_{G1}}} \tag{3.18}$$

Filter Design

The absence of zeros in equation (3.15) implies that any filter built of two cascaded low-pass Sallen-Key filter sections will be a 4th-order, all-pole, low-pass filter. The lack of zeros in the filter's transfer function somewhat restricted the selection of anti-aliasing filter types. Consequently, the only filter types considered were a Bessel, Butterworth, Chebyshev Type 1, and, for reference, an all-real filter.

Since this is a control application, flatness in the pass-band is only important in the context of its effect on compensation of the closed-loop system. On that basis, I somewhat arbitrarily chose to constrain the Chebyshev's pass-band ripple to ±1 dB, which seemed negligible in terms of its effect on the loop gain. Figure 3.24 shows a comparison of these filter types, with their gains normalized to unity at DC and their corner frequencies chosen to satisfy the constraints specified earlier in this section.

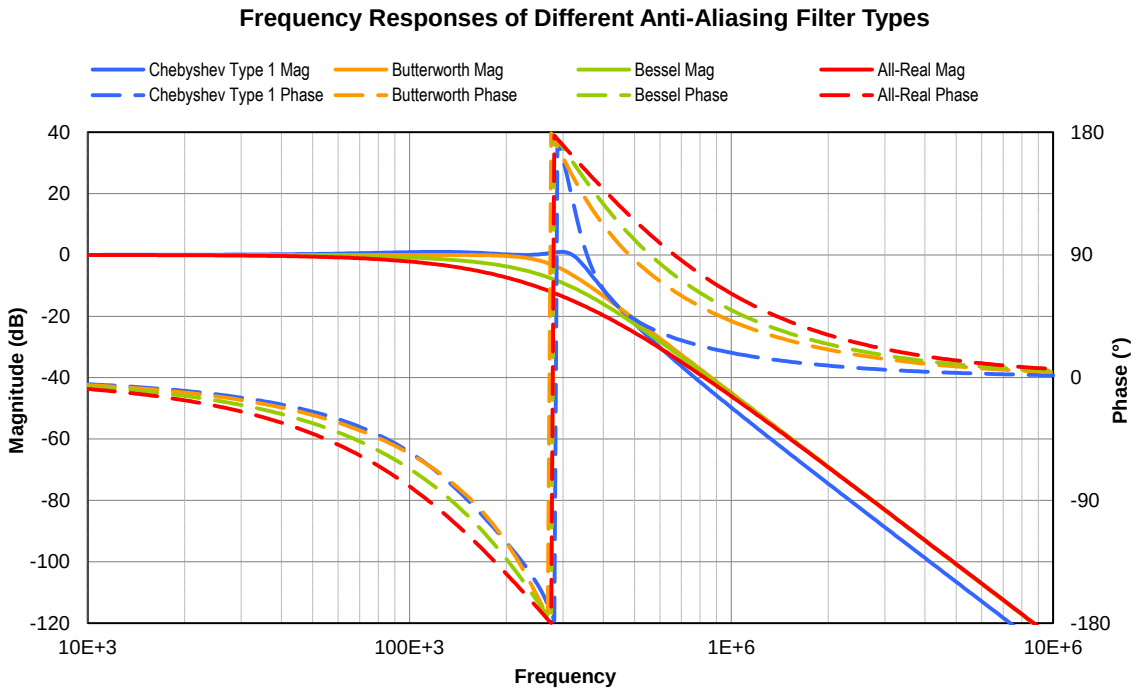


Figure 3.24 – Comparison of the four different 4th-order anti-aliasing filter prototypes, designed to meet the stated constraints and normalized to unity gain at DC.

Based on the phase contributions shown in Figure 3.24, I chose to use a Chebyshev type 1 with a -3 dB frequency of 320 kHz because it had the minimum phase lag below ~100 kHz.

Chapter 4: Digital Classical Control

4.1 Digitally-Controlled System

To create the digitally controlled system, I started with the simulation used to do the analog compensator design in Section 2.4 and added the digital controller infrastructure from Chapter 3. A diagram of the resultant system is shown in Figure 4.1. Current offset I_{ofs} was added to allow the ADC to measure the negative portion of the ripple when the output current is small.

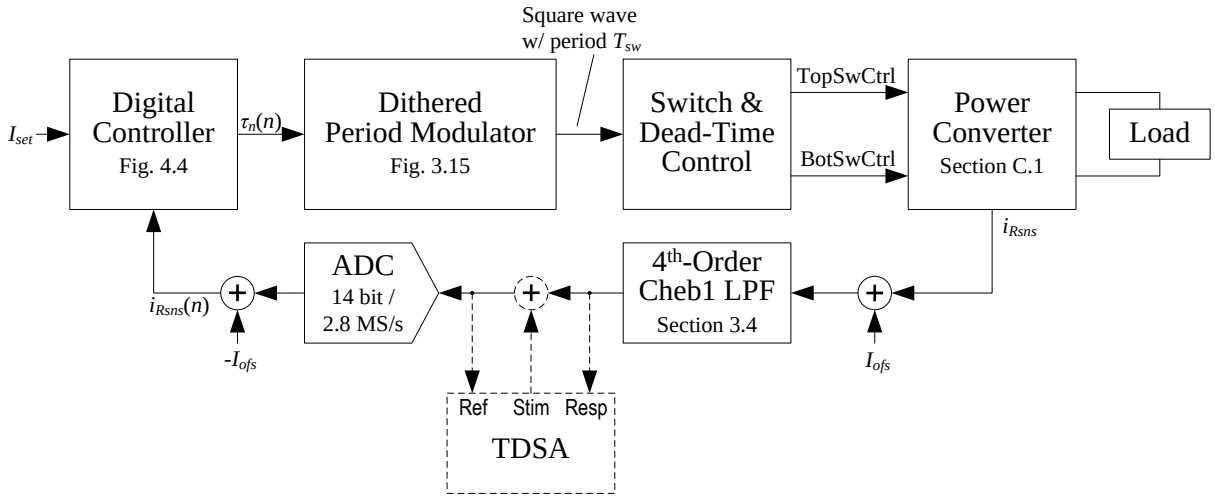


Figure 4.1 – Block diagram of the digitally controlled system. Current offset I_{ofs} was added to allow the ADC to measure the negative portion of the ripple when the output current is small.

Although the final implementation of this controller is to be digital (discrete time), it is generally easier to design the compensation in continuous time (*s*-domain) and then subsequently translate the design into discrete time (*z*-domain) for implementation. Figure 4.2 shows the process used to design the digital controller. Portions of the process that are identical to the analog controller design process from Figure 2.11 are described in Section 2.4.

Figure 4.2 – Digital controller design process.

4.2 s-Domain Compensation

Using the same integrator gain as the analog controller (k_i = 4 k), corner-case uncompensated ($H_c[s]$ = 1) loop gain measurements of the digital system were made. They are shown in Figure 4.3 and Figure 4.4. Note that the phase lag is substantially worse than the equivalent plots in Section 2.4; this is primarily due to latency introduced by the ADC and the discrete-time

modulator. Also note that the plots are 'noisier' at high frequencies, which is likely a result of the dithering added to overcome the modulator's quantization effects.

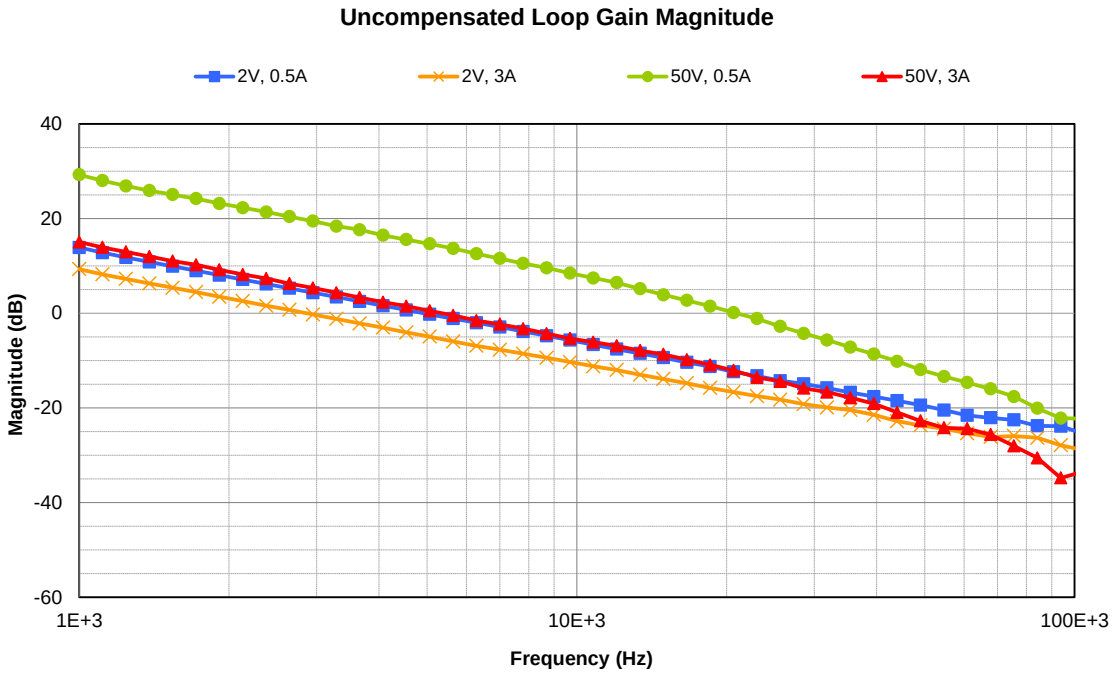


Figure 4.3 – Magnitude of the corner-case loop gain measurements of the uncompensated digital system, captured in simulation.

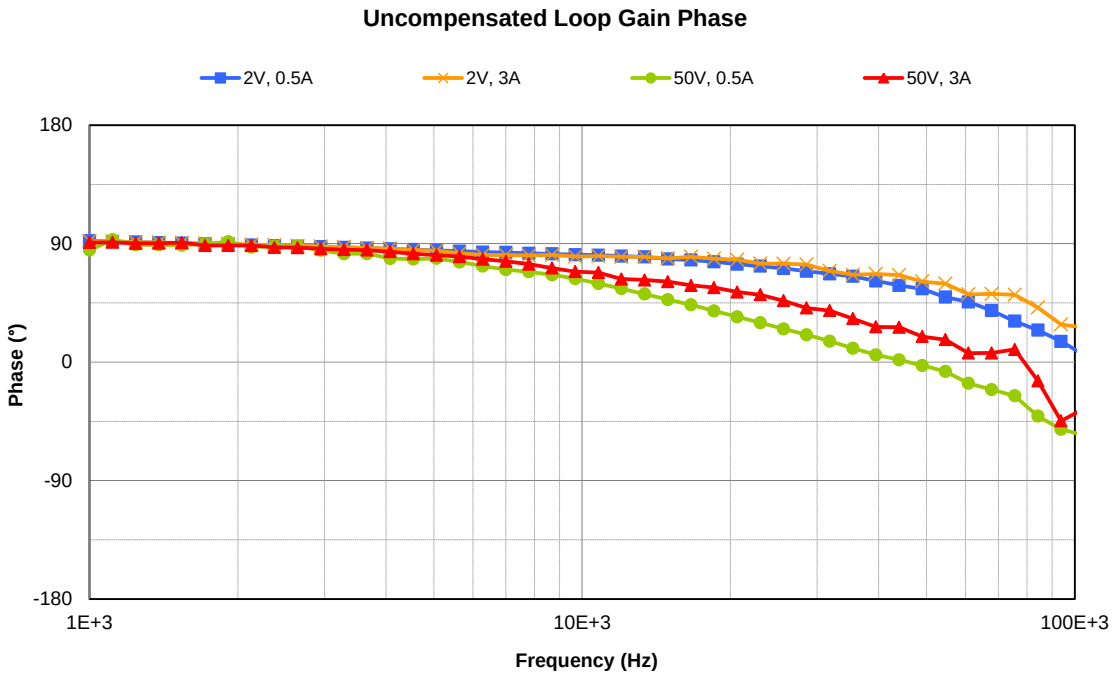


Figure 4.4 – Phase of the corner-case loop gain measurements of the uncompensated digital system, captured in simulation.

Based on these loop gain plots, I used the same continuous-time controller design approach used in Section 2.4 to compensate the system. This resulted in the *s*-domain controller parameters shown in Table 4.1.

Parameter	Value
k_i	4 k
k_{dc}	1.4
s_{z1}	-116 + j145 krad/s
s_{z2}	-116 – j145 krad/s
s_{p1}	-215 + j269 krad/s
s_{p2}	-215 – j269 krad/s

Table 4.1 – Table of the continuous-time controller parameters resulting from compensating the digitally controlled system.

4.3 Translation into *z*-Domain

z-Domain Controller Structure

For digital implementation, a discrete-time version of the controller shown in Figure 2.10 was required. It is shown in Figure 4.5.

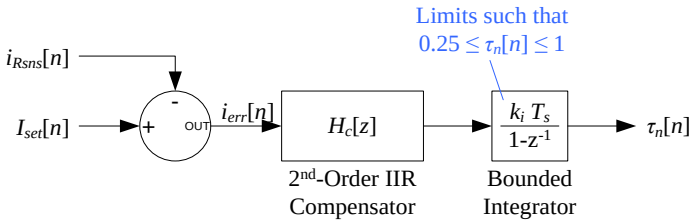


Figure 4.5 – Block diagram of a discrete-time version of the linear controller, where data in the system is processed at a rate of $1/T_s$.

The 2nd-order IIR compensator consists of a single second-order section (SOS), or

$$H_c[z] = H_{SOS}[z] \tag{4.1}$$

The discrete-time SOS was realized using what is commonly known as the Direct Form II structure with the addition of pre- and post-scaling to facilitate fixed-point implementation, as shown in Figure 4.6.

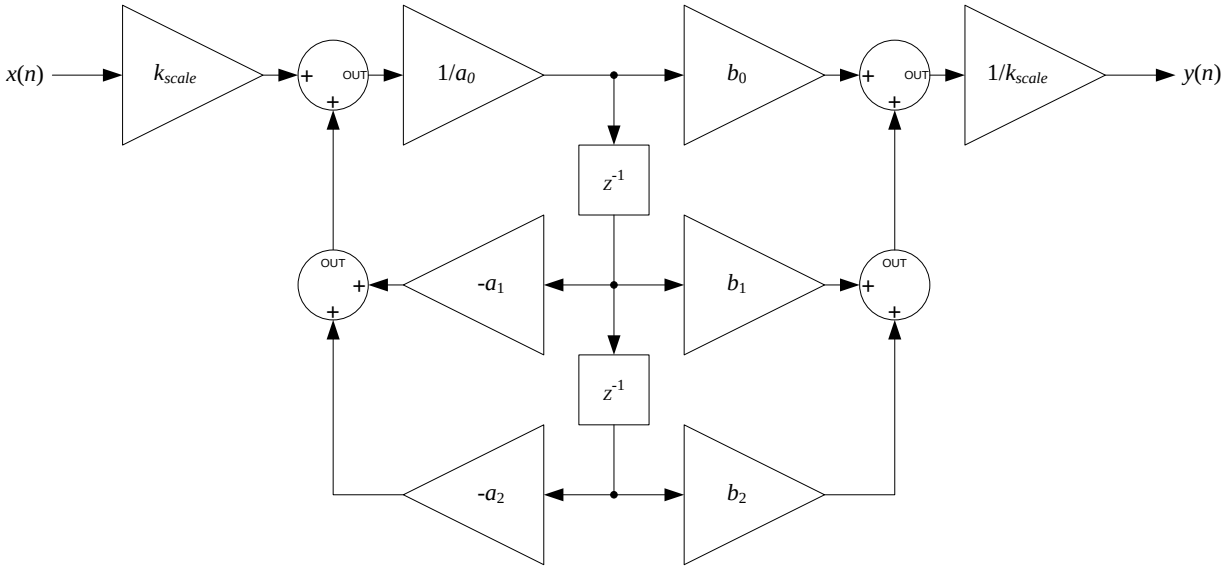


Figure 4.6 – Diagram of the digital compensator implementation (SOS).

The z-domain transfer function of the SOS shown in Figure 4.6 is

$$H_{SOS}[z] = \frac{y[z]}{x[z]} = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}} \tag{4.2}$$

The coefficients can be computed from the desired z-domain pole / zero locations and gain, k_z, to be

$$
\begin{aligned}
b_0 &= k_z \\
b_1 &= -2\,k_z\,\mathrm{Re}[z_z] \\
b_2 &= k_z\left(\mathrm{Re}[z_z]^2 + \mathrm{Im}[z_z]^2\right) \\
a_0 &= 1 \\
a_1 &= -2\,\mathrm{Re}[z_p] \\
a_2 &= \mathrm{Re}[z_p]^2 + \mathrm{Im}[z_p]^2
\end{aligned}
\tag{4.3}
$$

where the poles and zeros are in complex conjugate pairs, $\left(z_p, z_p^*\right)$ and $\left(z_z, z_z^*\right)$, respectively, or

$$
\begin{aligned}
b_0 &= k_z \\
b_1 &= -k_z\left(z_{z1} + z_{z2}\right) \\
b_2 &= k_z z_{z1} z_{z2} \\
a_0 &= 1 \\
a_1 &= -\left(z_{p1} + z_{p2}\right) \\
a_2 &= z_{p1} z_{p2}
\end{aligned}
\tag{4.4}
$$

where the pole and zero pairs are real.

Mapping Poles and Zeros into *z*-Domain

For implementation in a digital controller, the *s*-domain pole and zero locations decided upon in Section 4.2 need to be mapped into the *z*-domain. I did this using the matched *z*-transform method. Unlike other mapping methods (such as the bilinear transform), this transformation technique does not warp the frequency scale giving it the principal advantage of preserving *exact* pole and zero locations, which, consequently, preserves the Q and ω_0 of the *s*-domain compensator's pole and zero pairs. The matched *z*-transform is performed by mapping the *s*-domain poles and zeros into the *z*-domain using the standard relationship

$$z_i = e^{s_i T_s} \tag{4.5}$$

where z_i is the *z*-domain pole / zero location corresponding to *s*-domain pole / zero s_i. Performing this mapping on the *s*-domain pole / zero locations in equation (2.9) yields corresponding *z*-domain second-order section pole / zero locations of

$$
\begin{aligned}
z_{p1,p2} &= e^{-\frac{\omega_p T_s}{2Q_p} \pm \omega_p T_s \sqrt{\frac{1}{4Q_p^2} - 1}} \\
z_{z1,z2} &= e^{-\frac{\omega_z T_s}{2Q_z} \pm \omega_z T_s \sqrt{\frac{1}{4Q_z^2} - 1}}
\end{aligned}
\tag{4.6}
$$

which can be more conveniently expressed in polar form as

(4.7)
$$z_{p1,p2} = \rho_p e^{j\phi_p}$$
$$z_{z1,z2} = \rho_z e^{j\phi_z}$$

where

(4.8)
$$\left\{ \begin{array}{c} \rho_x = e^{-\frac{\omega_x T_s}{2Q_x} \pm \omega_x T_s \sqrt{\frac{1}{4Q_x^2} - 1}} \\ \phi_x = 0 \end{array} \right\} \quad \text{for real poles / zeros } \left(Q_x \le 0.5\right)$$

$$\left\{ \begin{array}{c} \rho_x = e^{-\frac{\omega_x T_s}{2Q_x}} \\ \phi_x = \pm \omega_x T_s \sqrt{1 - \frac{1}{4Q_x^2}} \end{array} \right\} \quad \text{for complex conjugate poles / zeros } \left(Q_x > 0.5\right)$$

Combining (4.3), (4.4), (4.7), and (4.8) and applying Euler's formula yields the *z*-domain SOS transfer function coefficient expressions shown in Table 4.2 and Table 4.3.

Num. Coeff.	**If Real Zero Pair…** $Q_z \le 0.5$	**If Complex Conj. Zero Pair…** $Q_z > 0.5$
b_0	k_z	k_z
b_1	$-k_z\left(e^{-\frac{\omega_z T_s}{2Q_z} + \omega_z T_s \sqrt{\frac{1}{4Q_z^2} - 1}} + e^{-\frac{\omega_z T_s}{2Q_z} - \omega_z T_s \sqrt{\frac{1}{4Q_z^2} - 1}}\right)$	$-2k_z e^{-\frac{\omega_z T_s}{2Q_z}} \cos\left[\omega_z T_s \sqrt{1 - \frac{1}{4Q_z^2}}\right]$
b_2	$k_z e^{-\frac{\omega_z T_s}{Q_z}}$	$k_z e^{-\frac{\omega_z T_s}{2Q_z}}$

Table 4.2 – The *z*-domain SOS's numerator coefficients in terms of the gain, k_z, and corner frequency and *Q* of the *s*-domain SOS's zeros.

Denom. Coeff.	**If Real Pole Pair… $Q_p \leq 0.5$**	**If Complex Conj. Pole Pair… $Q_p > 0.5$**
a_0	1	1
a_1	$-\left(e^{-\frac{\omega_p T_s}{2Q_p}+\omega_p T_s\sqrt{\frac{1}{4Q_p{}^2}-1}}+e^{-\frac{\omega_p T_s}{2Q_p}-\omega_p T_s\sqrt{\frac{1}{4Q_p{}^2}-1}}\right)$	$-2e^{-\frac{\omega_p T_s}{2Q_p}}\cos\left[\omega_p T_s\sqrt{1-\frac{1}{4Q_p{}^2}}\right]$
a_2	$e^{-\frac{\omega_p T_s}{Q_p}}$	$e^{-\frac{\omega_p T_s}{2Q_p}}$

Table 4.3 – The *z*-domain SOS's denominator coefficients in terms of the corner frequency and *Q* of the *s*-domain SOS's poles.

Since there are no poles or zeros at the origin in the target compensator transfer function (from Table 4.1), the gain of the *z*-domain SOS, k_z, can be computed by setting the DC gain in both domains to be equal and solving for k_z.

(4.9) $$H_{SOS}[z]\Big|_{z=1} = k_{DC}$$

Table 4.4 shows the *z*-domain compensator coefficients calculated by following this process. The implied transfer function's frequency response is shown plotted in Figure 4.7.

Coefficient	**Value**
b_0	3.4555
b_1	-6.6192
b_2	3.1785
a_0	1
a_1	-1.8426
a_2	0.8568

Table 4.4 – *z*-domain SOS coefficients of the digital compensator (prior to scaling for fixed-point implementation).

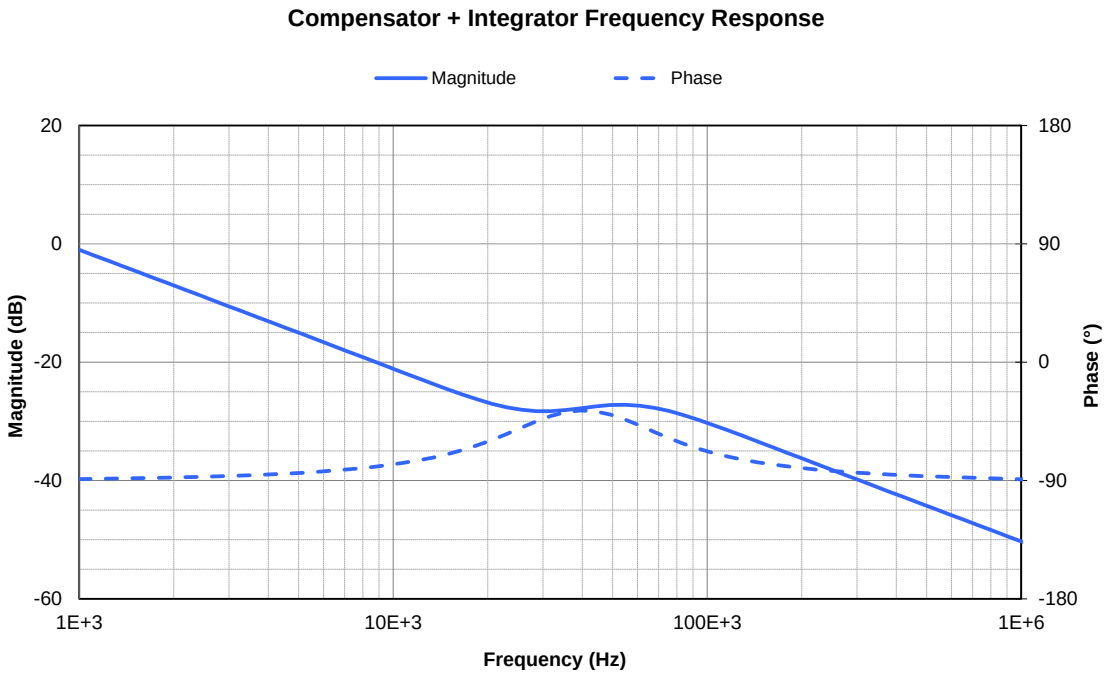


Figure 4.7 – Plot of the transfer function of the *z*-domain controller implied by the parameters in Table 4.4.

4.4 Results

The *z*-domain compensator implied by the parameters in Table 4.4 was implemented in Simulink and a co-simulation was run. Plots of the resultant compensated corner-case loop gains are shown in Figure 4.8 and Figure 4.9.

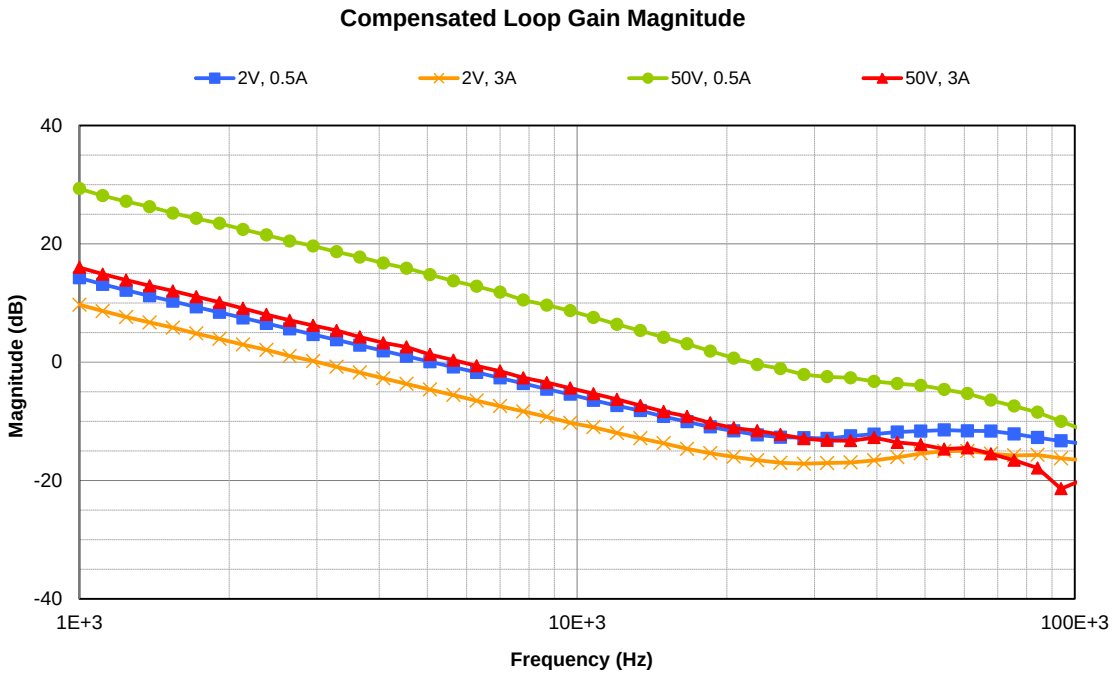


Figure 4.8 – Magnitude of the corner-case loop gain measurements of the compensated digital system, captured in simulation.

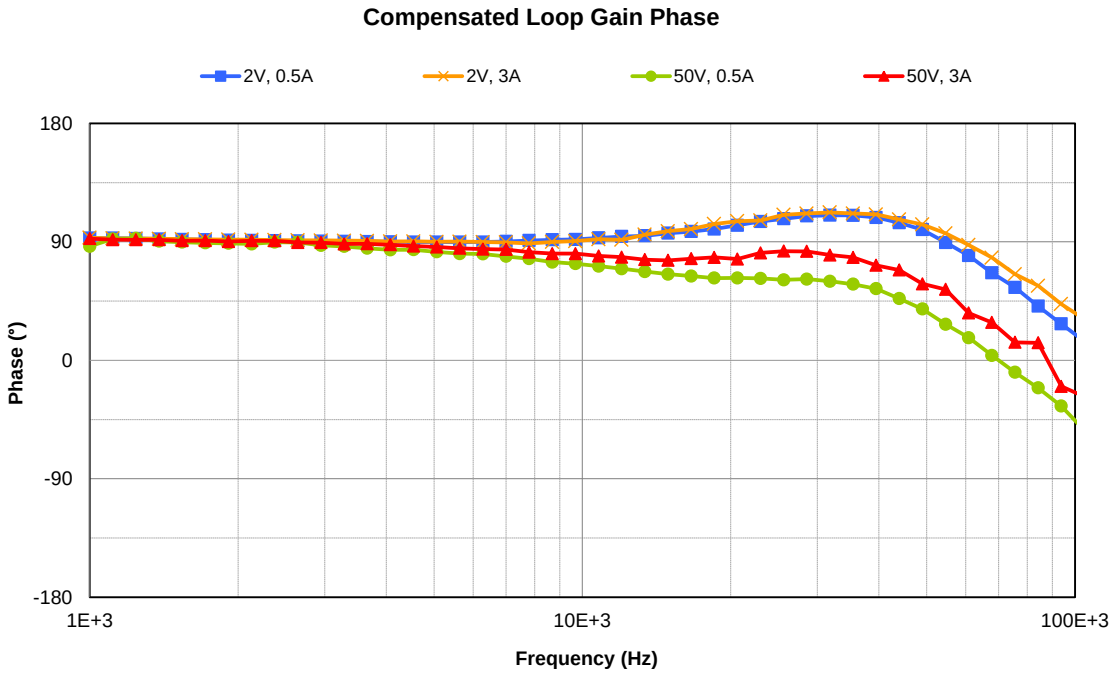


Figure 4.9 – Phase of the corner-case loop gain measurements of the compensated digital system, captured in simulation.

As with the analog system in Section 2.4, a large variation (~20 dB) was observed in overall loop gain magnitude with operating point. This translates into a similarly large variation in loop gain cross-over frequencies (~10:1), which results in inconsistent control-to-output frequency response characteristics (see Figure 4.10 and Figure 4.11) and transient behavior. The digitally compensated system's response to a 10% input step and 1 V load transient are shown in Figure 4.12 and Figure 4.13, respectively. Note the much larger noise in the transient plots, as compared with the corresponding plots of the analog-compensated system (Figure 2.19 and Figure 2.20, respectively); this is mostly the result of the dithering used in the modulator to prevent limit cycling (see Section 3.1), but may also be due, in part, to aliasing in the modulator (described on page 77). Results under all four corner-case conditions are summarized in Table 4.5.

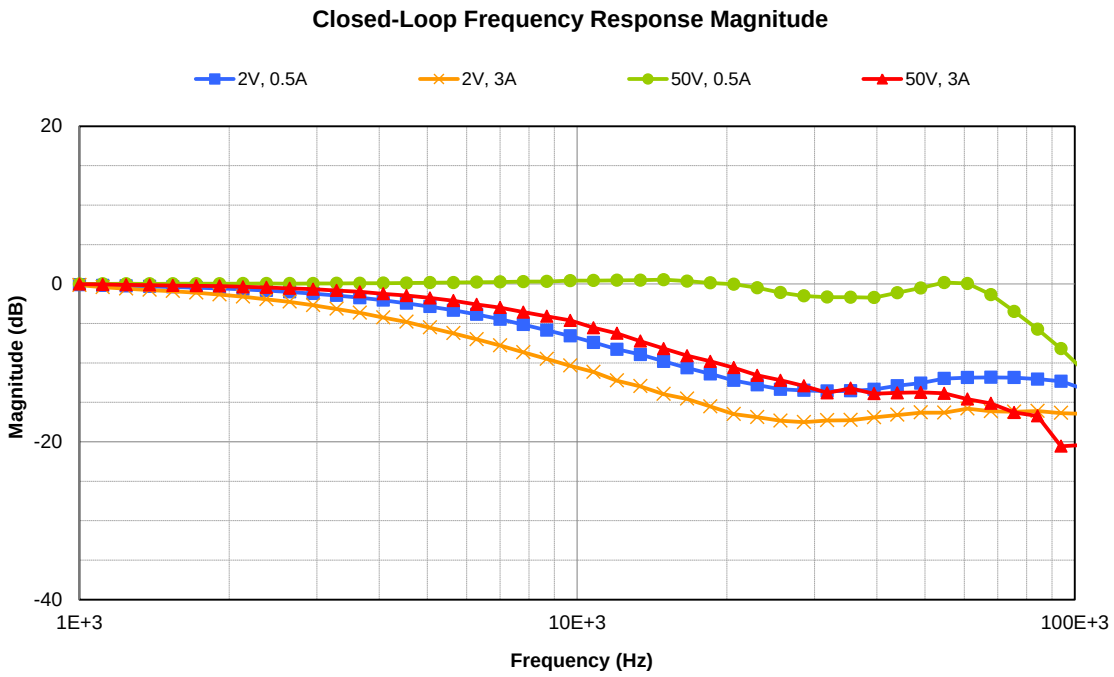


Figure 4.10 – Magnitude of the corner-case control-to-output frequency response measurements of the compensated digital system, captured in simulation.

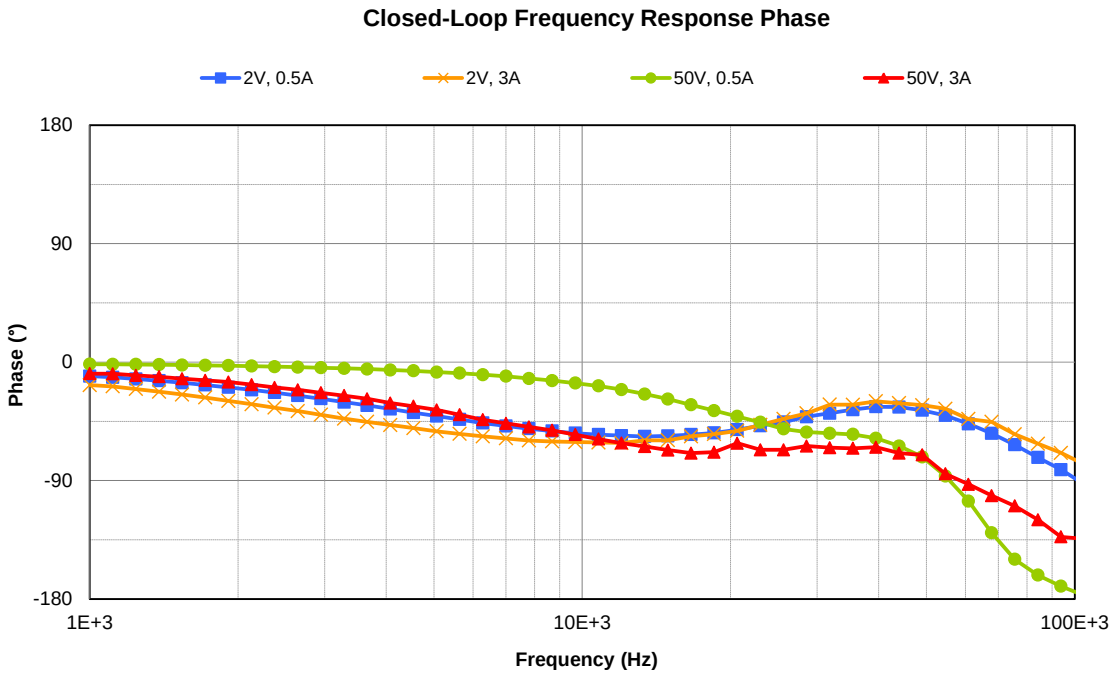


Figure 4.11 – Phase of the corner-case control-to-output frequency response measurements of the compensated digital system, captured in simulation.

Operating Point		Loop Gain Cross-over Frequency	Phase Margin	Gain Margin	Control-to-Output B.W. (-3 dB)
2 V	**0.5 A**	5.1 kHz	90°	15 dB	5.3 kHz
2 V	**3 A**	3.0 kHz	91°	17 dB	3.3 kHz
50 V	**0.5 A**	22 kHz	62°	6.5 dB	74 kHz
50 V	**3 A**	5.9 kHz	85°	19 dB	7.0 kHz

Table 4.5 – Summary of key simulated results of the compensated digital system at the four corner-case operating points.

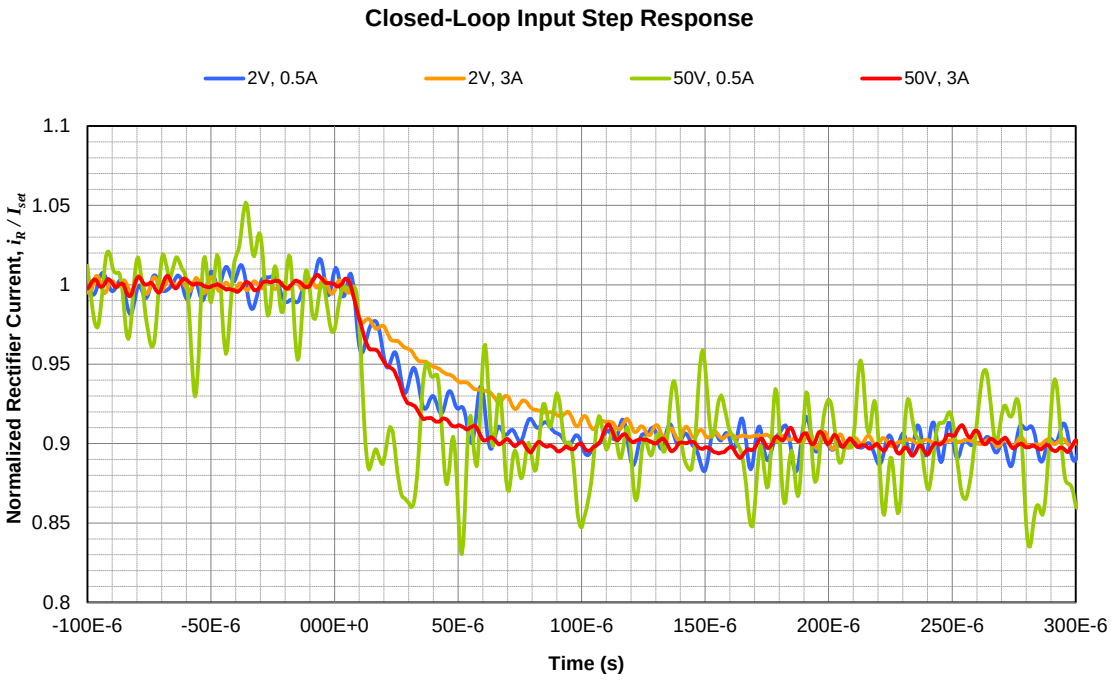


Figure 4.12 – Simulated corner-case closed-loop response of the digital system's average* rectifier current to a step in the current set point from 100% to 90%.

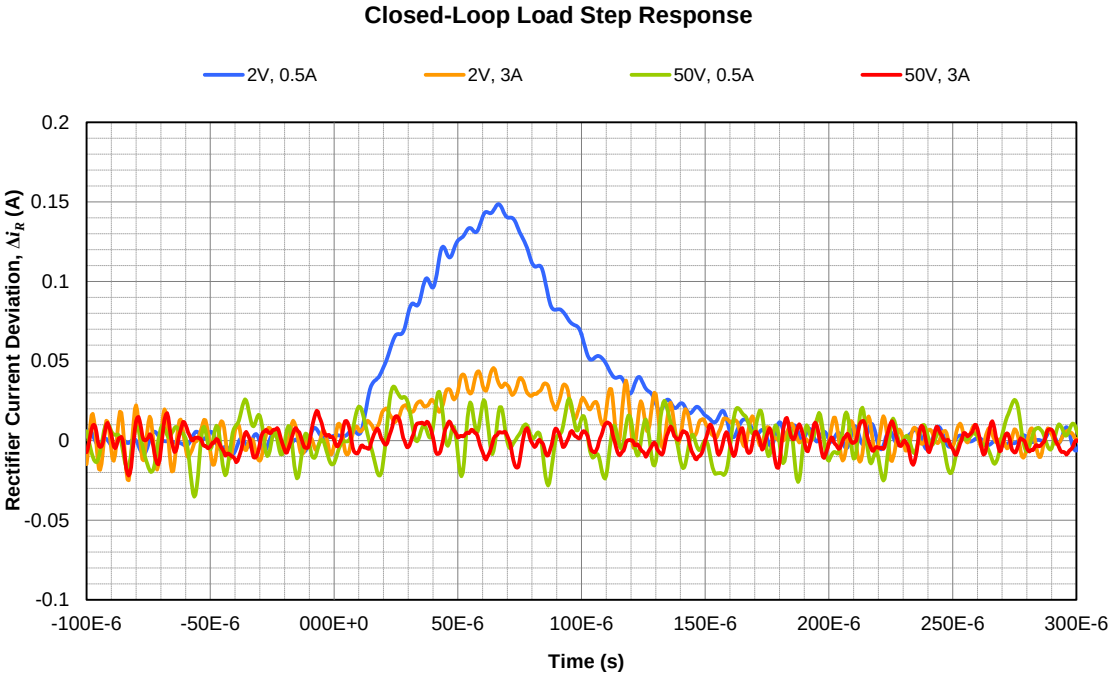


Figure 4.13 – Simulated corner-case closed-loop response of the digital system's average* rectifier current to a 1 V, 50 µs load step.

* Ripple was filtered using a 200 kHz 8th-order elliptic low-pass filter with 1 dB / 80 dB pass- / stop-band ripple.

Chapter 5: Digital Control with Gain-Scheduled Compensator

5.1 Rationale

When examining the closed-loop gain of the digitally-compensated converter in Figure 4.8 and Figure 4.9, two things are apparent:

1. As noted in Sections 2.4 and 4.4, there is a large (~20 dB) operating-point dependent loop gain variation.
2. The phase margin requirement in the 50 V, 0.5 A case is what limits the overall compensator gain (because of its relatively large loop gain magnitude), effectively penalizing the other three corner cases with dramatically poorer performance.

I hypothesized that if the operating point-dependent loop gain variability within the frequency range of interest (from DC to gain cross-over) could be reduced or eliminated, so would the corresponding operating point-dependent variability in closed-loop performance.

5.2 Gain-Scheduled Controller

The most direct way to reduce or eliminate the closed-loop gain variability with operating point seen in Figure 4.8 appeared to be to modulate the gain of the system with an inverse operating-point dependent correction, $k_c[I_R,V_O]$. More specifically,

$$k_c\left[I_R,V_O\right]=\frac{k}{\left|G_p\left[s,I_R,V_O\right]\right|} \tag{5.1}$$

where k is a gain normalization constant and G_p is the plant transfer function from τ_n to i_R. Inspection of the loop gain plots in Figure 4.8 reveals that the relationships between the gains at the different operating points are nearly independent of frequency within the frequency range of interest (DC to ~20 kHz). More explicitly,

$$G_p\left[2\pi f_1,I_{R1},V_{O1}\right]\approx k\cdot G_p\left[2\pi f_2,I_{R2},V_{O2}\right] \quad \text{where} \quad 0\le\left(f_1,f_2\right)\le 20\text{ kHz} \tag{5.2}$$

where k is a constant. This applies for any I_{R1}, I_{R2}, V_{O1}, and V_{O2} within the converter's operating range, and any f_1 and f_2, provided that both are less than ~20 kHz. Therefore, s in equation (5.1) can be substituted with the constant $2\pi f_{corr}$, where f_{corr} is the frequency at which the required plant gain correction is to be measured. This yields the gain correction function

$$k_c\left[I_R,V_O\right]=\frac{k}{\left|G_p\left[2\pi f_{corr},I_R,V_O\right]\right|} \quad \text{where} \quad 0\le f_{corr}\le 20\text{ kHz} \tag{5.3}$$

For implementation, the gain correction function must be defined in terms of the actual measured signals, v_{Osns} and i_{Rsns}, as shown in the block diagram of the gain-scheduled controller in Figure 5.1.

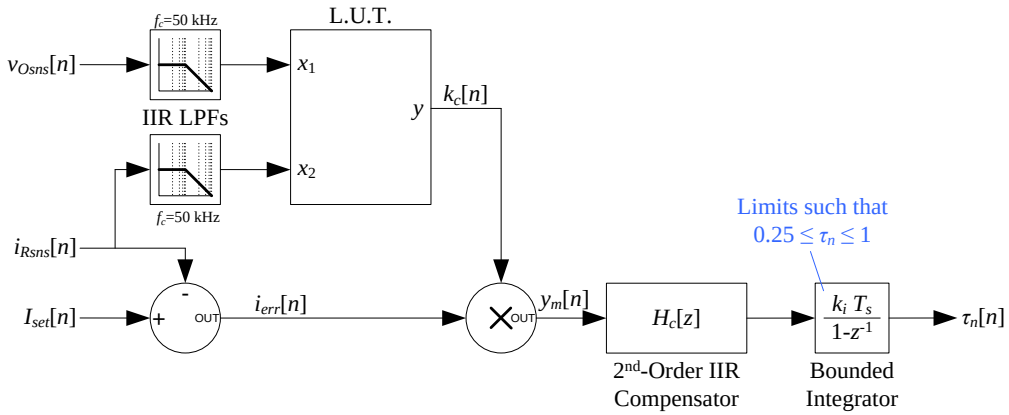


Figure 5.1 – Block diagram of the gain-scheduled discrete-time controller, where data in the system is processed at a rate of $1/T_s$

The look-up-table (LUT) in Figure 5.1 implements the function

$$y = f\left[x_1, x_2\right] = k_c\left[i_{Rsns}, v_{Osns}\right] = \frac{k_{fp}}{\left| G_p\left[2\pi f_{corr}, \frac{i_{Rsns}}{k_{isns}/R_{sns}}, \frac{v_{Osns}}{k_{vsns}} \right] \right|} \tag{5.4}$$

where k_{fp} is a constant chosen to facilitate fixed-point implementation, and k_{isns}, R_{sns}, and k_{vsns} are measurement constants as defined in Figure 3.17.

Effect on Small-Signal Stability

The output of the multiplier in Figure 5.1 is

$$y_m\left[i_{Rsns}, v_{Osns}\right] = \left(I_{set} - i_{Rsns}\right) \cdot k_c\left[i_{Rsns}, v_{Osns}\right] \tag{5.5}$$

For convenience, the time-varying quantities in (5.5) can be equivalently expressed as sums of their respective AC and DC components, or

$$\begin{aligned} i_{Rsns} &= I_{Rsns} + \hat{i}_{Rsns} \\ v_{Osns} &= V_{Osns} + \hat{v}_{Osns} \end{aligned} \tag{5.6}$$

Assuming that y_m is analytic, it can be equivalently expressed as a Taylor-series expansion about the DC operating point (I_{Rsns}, V_{Osns}).

$$y_m\left[i_{Rsns}, v_{Osns}\right] = \sum_{n_i=0}^{\infty} \sum_{n_v=0}^{\infty} \frac{\hat{i}_{Rsns}{}^{n_i} \cdot \hat{v}_{Osns}{}^{n_v}}{n_i! \cdot n_v!} \frac{\partial^{(n_i+n_v)} y_m\left[I_{Rsns}, V_{Osns}\right]}{\partial i_{Rsns}{}^{n_i} \cdot \partial v_{Osns}{}^{n_v}} \tag{5.7}$$

Assuming that the AC signal components $\hat{i}_{Rsns}$ and $\hat{v}_{Osns}$ are sufficiently small (the 'small-signal' assumption), all but the zeroth- and first-order terms of the expansion can be dropped allowing y_m to be approximated by the linear expression

$$y_m\left[i_{Rsns}, v_{Osns}\right] \approx y_m\left[I_{Rsns}, V_{Osns}\right] + \hat{v}_{Osns}\frac{\partial y_m\left[I_{Rsns}, V_{Osns}\right]}{\partial v_{Osns}} + \hat{i}_{Rsns}\frac{\partial y_m\left[I_{Rsns}, V_{Osns}\right]}{\partial i_{Rsns}} \tag{5.8}$$

Plugging (5.5) into (5.8) and evaluating the partial derivatives yields

$$\begin{aligned} & y_m\left[i_{Rsns}, v_{Osns}\right] \approx \\ & \left(I_{set} - I_{Rsns}\right)\cdot\left(k_c\left[I_{Rsns}, V_{Osns}\right] + \hat{v}_{Osns}\frac{\partial k_c\left[I_{Rsns}, V_{Osns}\right]}{\partial v_{Osns}} + \hat{i}_{Rsns}\frac{\partial k_c\left[I_{Rsns}, V_{Osns}\right]}{\partial i_{Rsns}}\right) \\ & -\hat{i}_{Rsns}\cdot k_c\left[I_{Rsns}, V_{Osns}\right] \end{aligned} \tag{5.9}$$

Because of the practically infinite integrator gain at DC, I_{set} and I_{Rsns} are equal, allowing this to be further simplified to

$$y_m\left[i_{Rsns}, v_{Osns}\right] \approx -\hat{i}_{Rsns}\cdot k_c\left[I_{Rsns}, V_{Osns}\right] \tag{5.10}$$

which implies that gain-scheduling has no effect on the small-signal stability of the system beyond the desired scaling of the loop gain. Note that this says nothing about the large-signal stability of the gain-scheduled system. To reduce the risk of large-signal instability, the LUT was designed to linearly interpolate between the measured data points (using a standard bilinear interpolation technique) and 50 kHz low-pass filters were added to its inputs (as shown in Figure 5.1).

These added filters force the gain correction to change relatively slowly with operating point (on the order of the control bandwidth), essentially providing crude time-scale separation (discussed in general in [7]). This helps to avoid unintentionally creating a complex high frequency non-linear system. Care must be taken, however, because putting the LUT filters too low in frequency risks leaving the system at an operating point with inappropriate gain correction on a transient basis, potentially leading to short-term linear stability problems while the filters catch-up.

5.3 Gain-Scheduled System

A block diagram of the gain-scheduled system is shown in Figure 5.2.

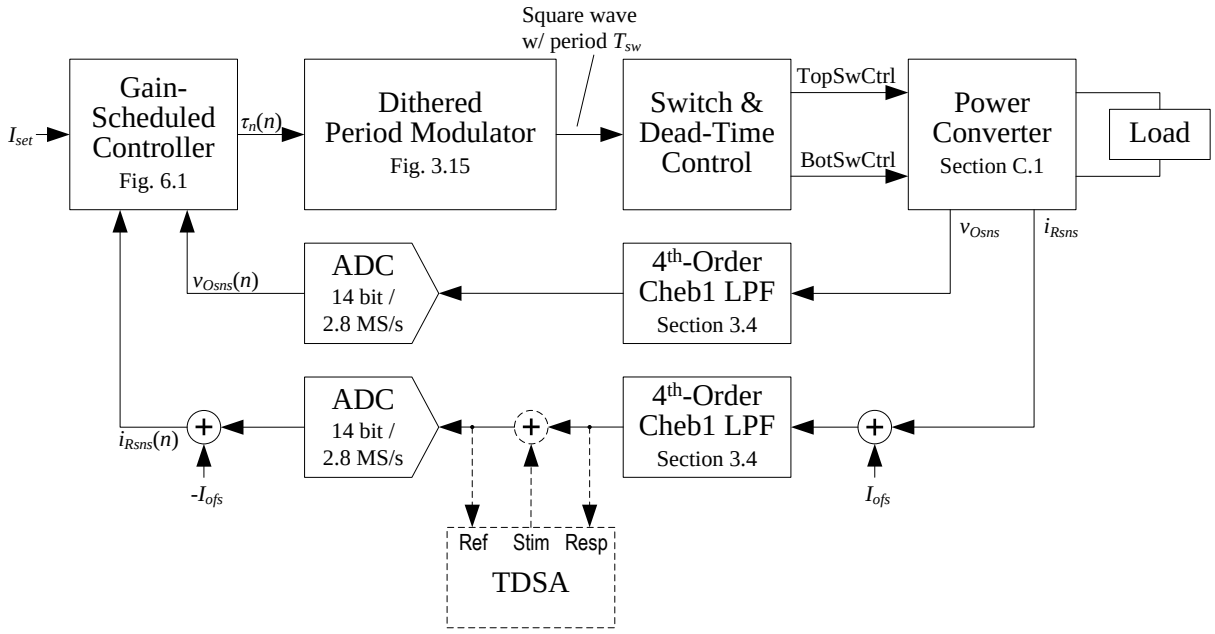


Figure 5.2 – Block diagram of the gain-scheduled system.

The process used to design the gain-scheduled controller is illustrated in Figure 5.3. Portions of the process that are identical to the analog or digital controller design processes from Figure 2.11 or Figure 4.2 are described in Sections 2.4 or 4.1, respectively.

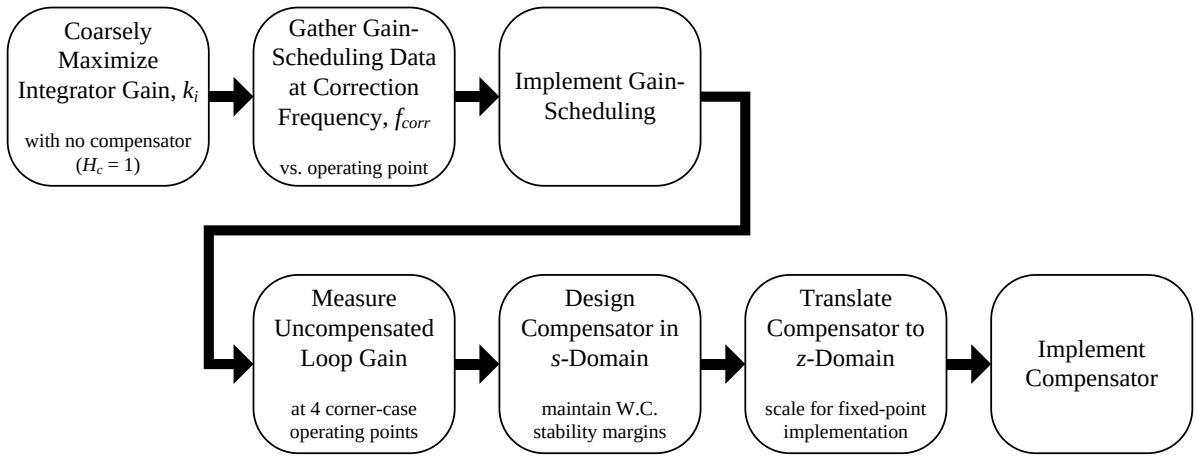


Figure 5.3 – Gain-scheduled controller design process.

5.4 Gathering Gain Scheduling Data (in simulation)

Using the Saber simulation used to model the classical digital system (Figure 4.1), the small-signal loop gain of the uncompensated system ($H_c[s] = 1$) was measured at f_{corr} = 10 kHz at a series of 32 × 32 points over the converter's entire operating range. The test frequency and number of points were chosen to keep the simulation time reasonable. Despite this, however, capturing the gain-scheduling data took more than 18 hours on a state-of-the-art workstation.

For reasons described in Section 2.2, there is no analytical means of deriving this this data for a super-resonant NC-PRC; it had to be done numerically.

Using k_{fp} = 0.25 (to keep $k_c[I_R,V_O]<1$ for convenient fixed-point implementation), I computed $k_c[I_R,V_O]$ as shown in (5.4). The results are plotted in Figure 5.4.

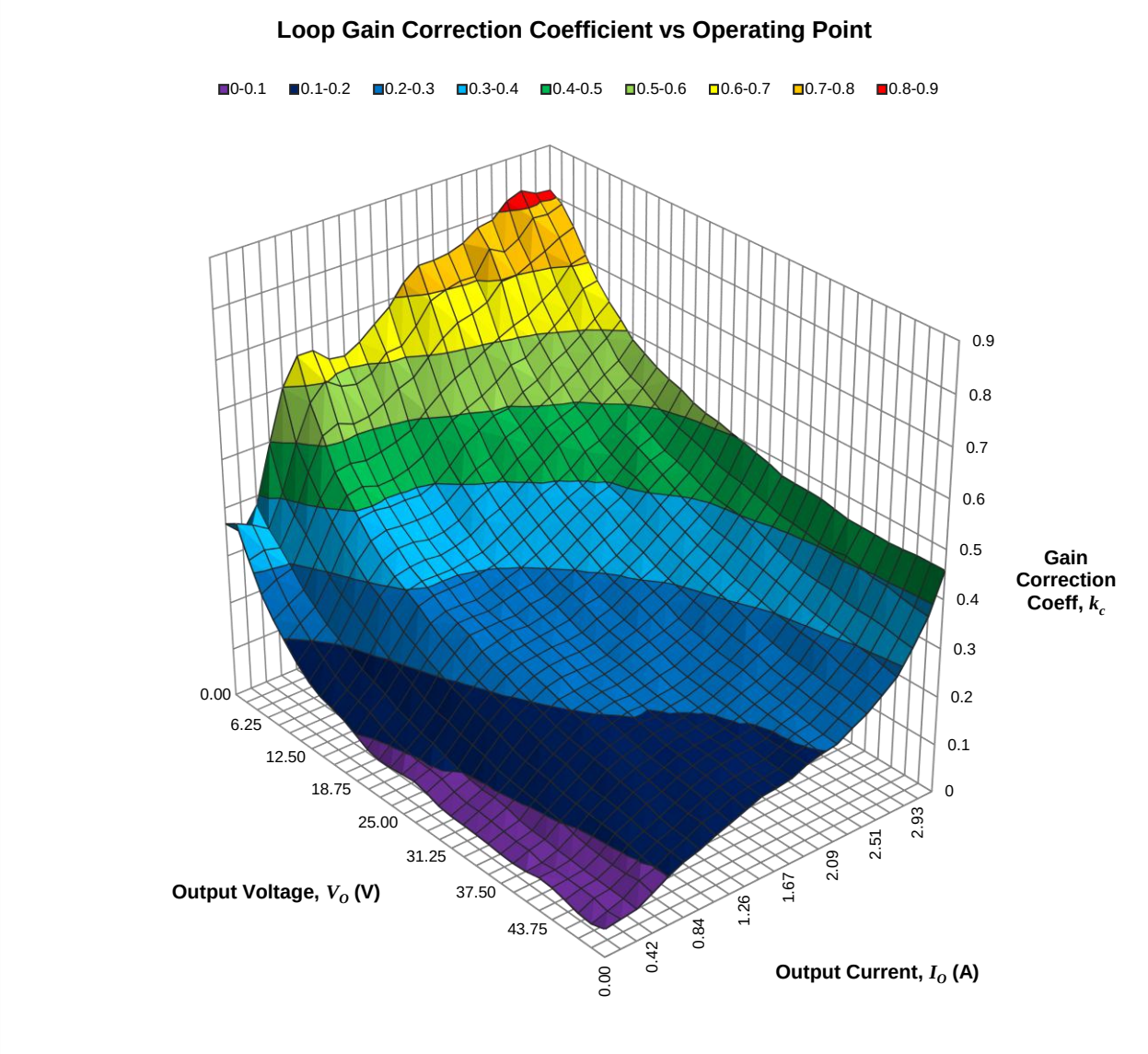


Figure 5.4 – Surface plot of the gain correction LUT function, $k_c[I_R,V_O]$, versus operating point, based on data captured in simulation at f_{corr} = 10 kHz.

5.5 Compensation Design

Following the process shown in Figure 5.3, gain-scheduling was implemented and a simulation was run to measure the loop gains of the uncompensated ($H_c[s]$ = 1) gain-scheduled system at the four corner-case operating points. They are shown plotted in Figure 5.5 and Figure 5.6.

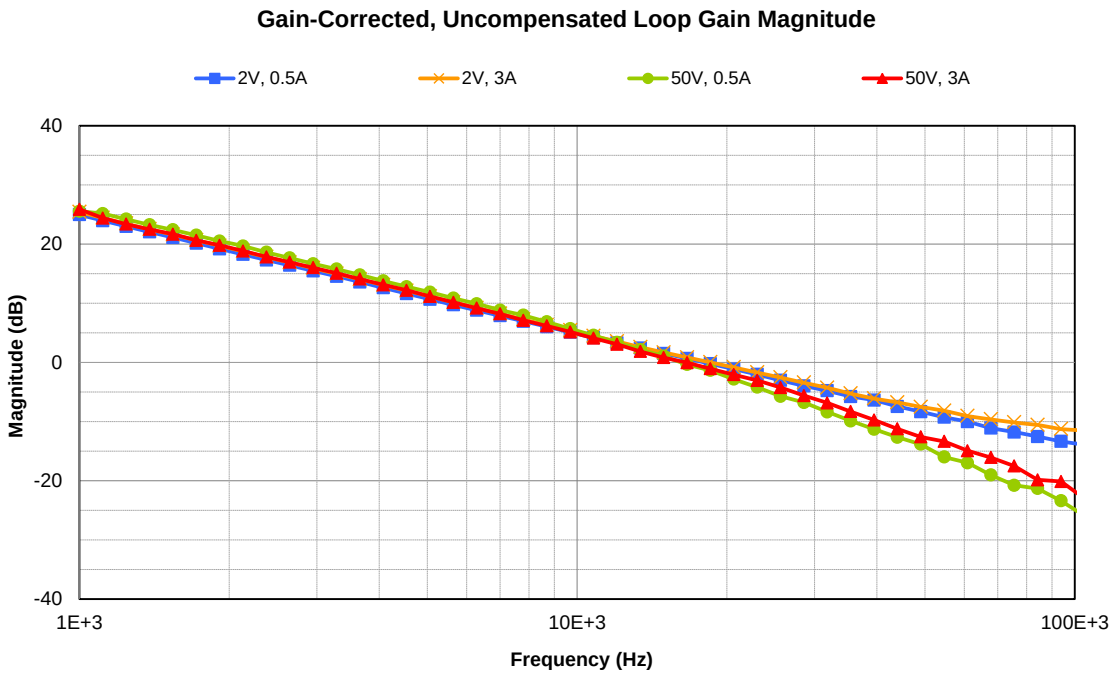


Figure 5.5 – Magnitude of the corner-case loop gain measurements of the uncompensated, gain-scheduled system, captured in simulation.

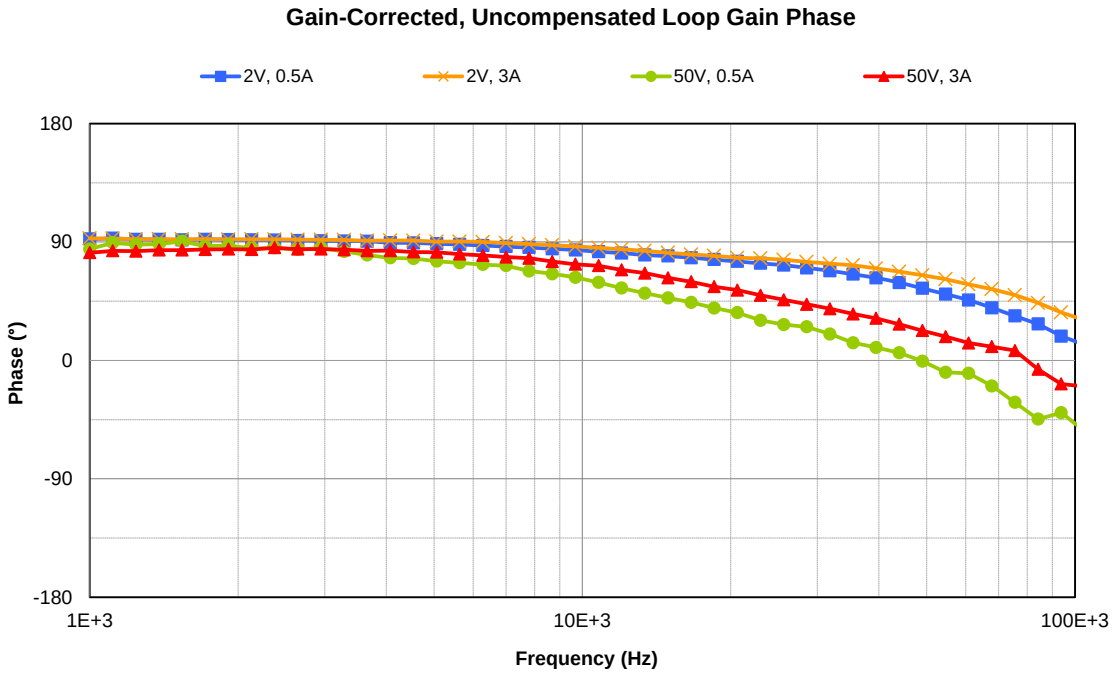


Figure 5.6 – Phase of the corner-case loop gain measurements of the uncompensated, gain-scheduled system, captured in simulation.

Notice that the loop gain magnitudes are nearly identical below ~10 kHz, unlike the similar plot in the non-gain-scheduled case (Figure 4.8). Based on these uncompensated loop gain measurements, I compensated the gain-scheduled system empirically using the same continuous-time classical compensator design technique used in Sections 2.4 and 4.2. This yielded the *s*-domain integrator and compensator parameters shown in Table 5.1.

Parameter	Value
k_i	32 k
k_{dc}	0.866
s_{z1}	-114 krad/s
s_{z2}	-1.71 Mrad/s
s_{p1}	-264 krad/s
s_{p2}	-3.96 Mrad/s

Table 5.1 – Table of the continuous-time controller parameters resulting from compensating the gain-scheduled system in simulation.

Following the process used in Section 4.3, this controller was translated into *z*-domain which yielded the *z*-domain compensator coefficients shown in Table 5.2. The implied transfer function's frequency response is shown plotted in Figure 5.7.

Coefficient	Value
b_0	3.5578
b_1	-5.2964
b_2	1.8060
a_0	1
a_1	-1.0772
a_2	0.1527

Table 5.2 – *z*-domain SOS coefficients for the gain-scheduled simulation's compensator (before scaling for fixed-point implementation).

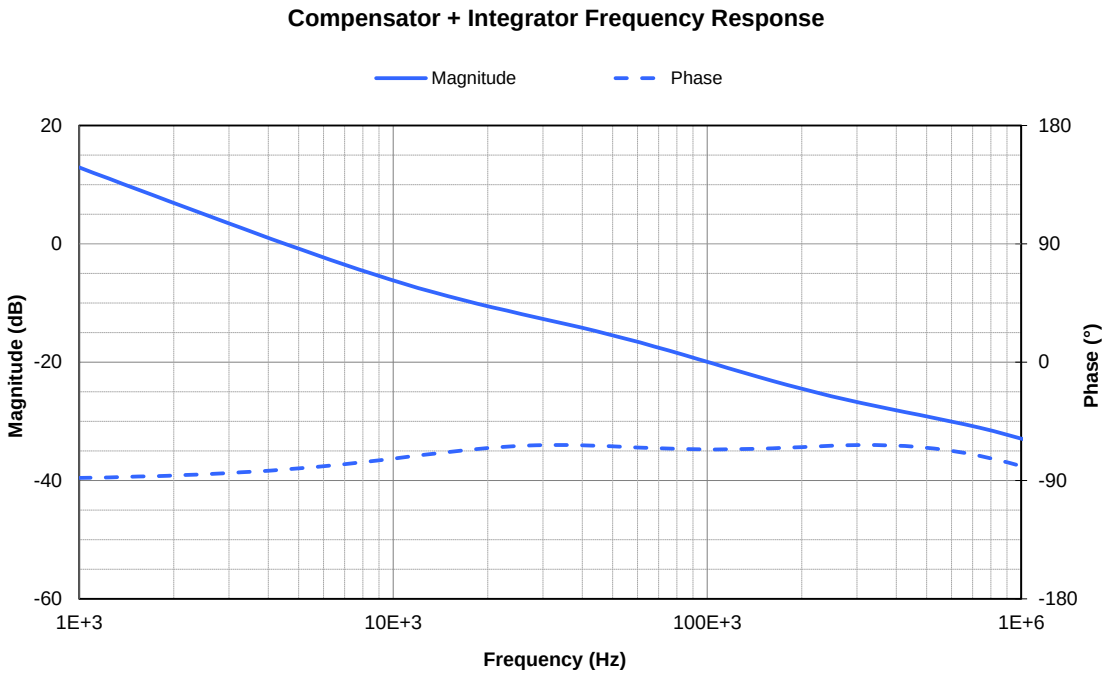


Figure 5.7 – Plot of the transfer function of the gain-scheduled system's *z*-domain compensator and integrator implied by the parameters from Table 5.2.

5.6 Results

The *z*-domain compensator implied by the parameters in Table 5.2 was implemented and a simulation was run. Plots of the resultant compensated corner-case loop gains are shown in Figure 5.8 and Figure 5.9.

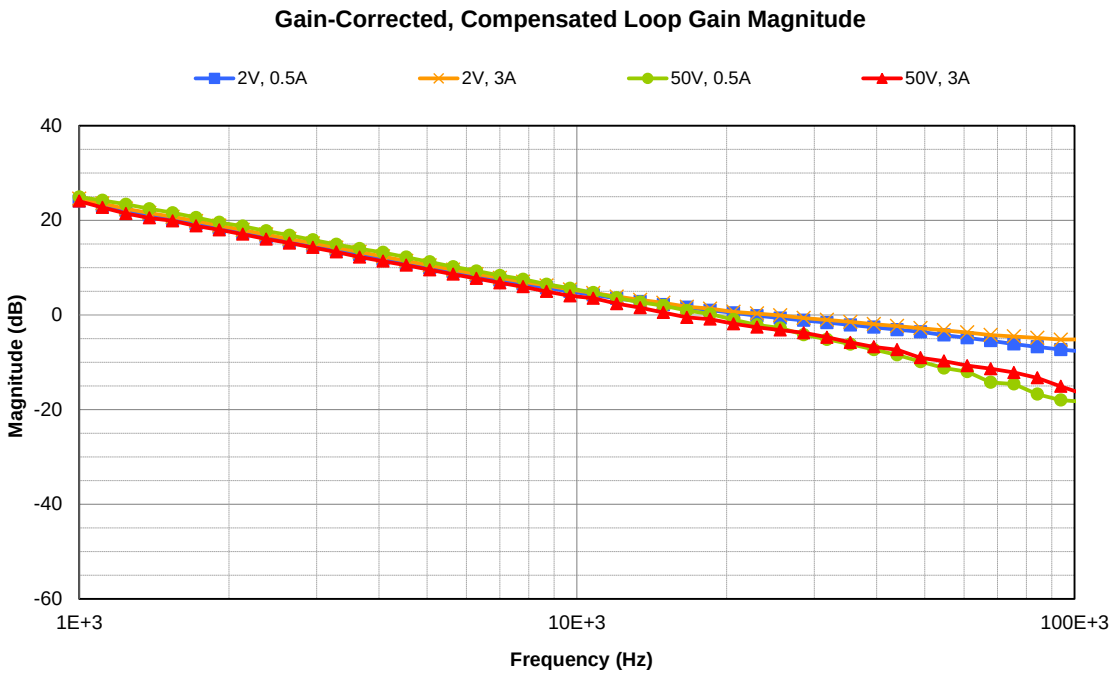


Figure 5.8 – Magnitude of the corner-case loop gain measurements of the compensated gain scheduled system, captured in simulation.

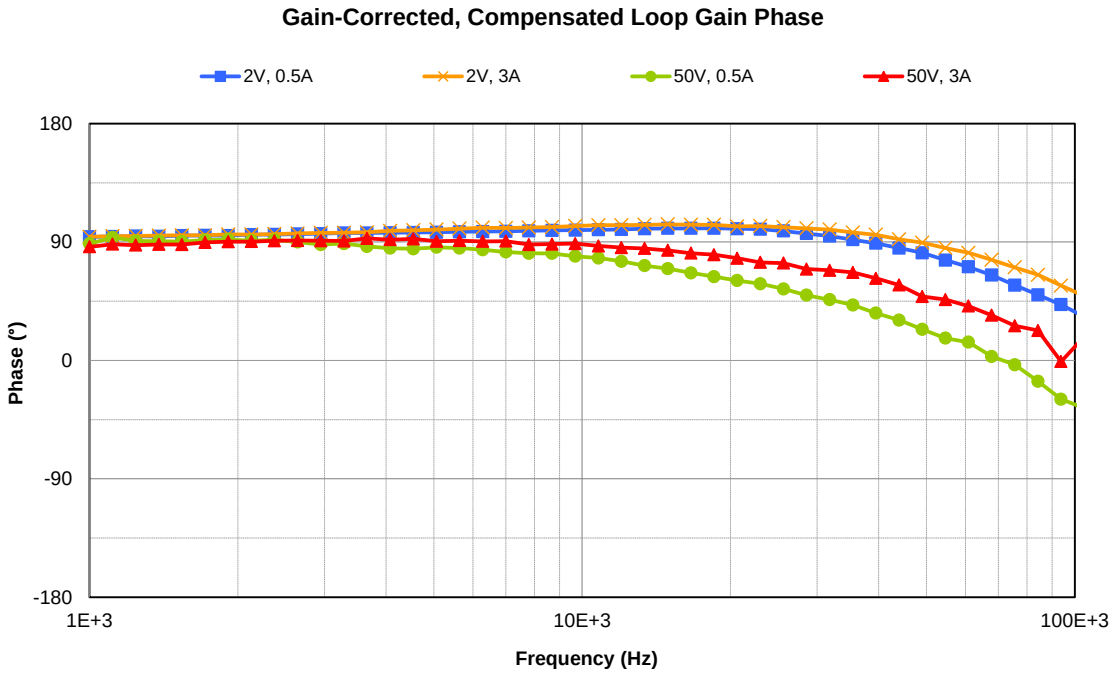


Figure 5.9 – Phase of the corner-case loop gain measurements of the compensated gain-scheduled system, captured in simulation.

As with the uncompensated loop gain, the compensated loop gain magnitudes of the gain corrected system at the four corner-case operating points are very similar* below ~10 kHz. This is in stark contrast to the similar plot non-gain-scheduled case (Figure 4.8) which shows low frequency gains that vary by ~20 dB. This more similar set of loop gain magnitudes correlates with the more similar control-to-output frequency response magnitudes shown in Figure 5.10 and Figure 5.11. Results under all four corner-case conditions are summarized in Table 5.3.

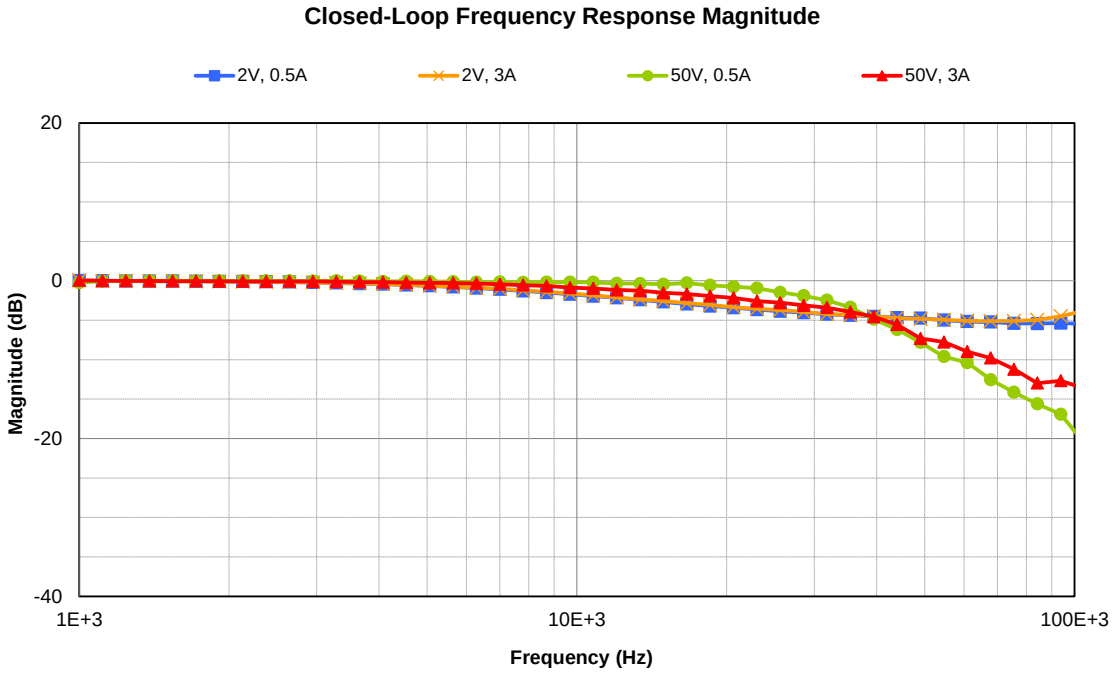


Figure 5.10 – Magnitude of the corner-case control-to-output frequency response measurements of the compensated gain-scheduled system, captured in simulation.

* Similar, but not identical. This is due to compromises made in simulation accuracy to keep simulation times reasonable.

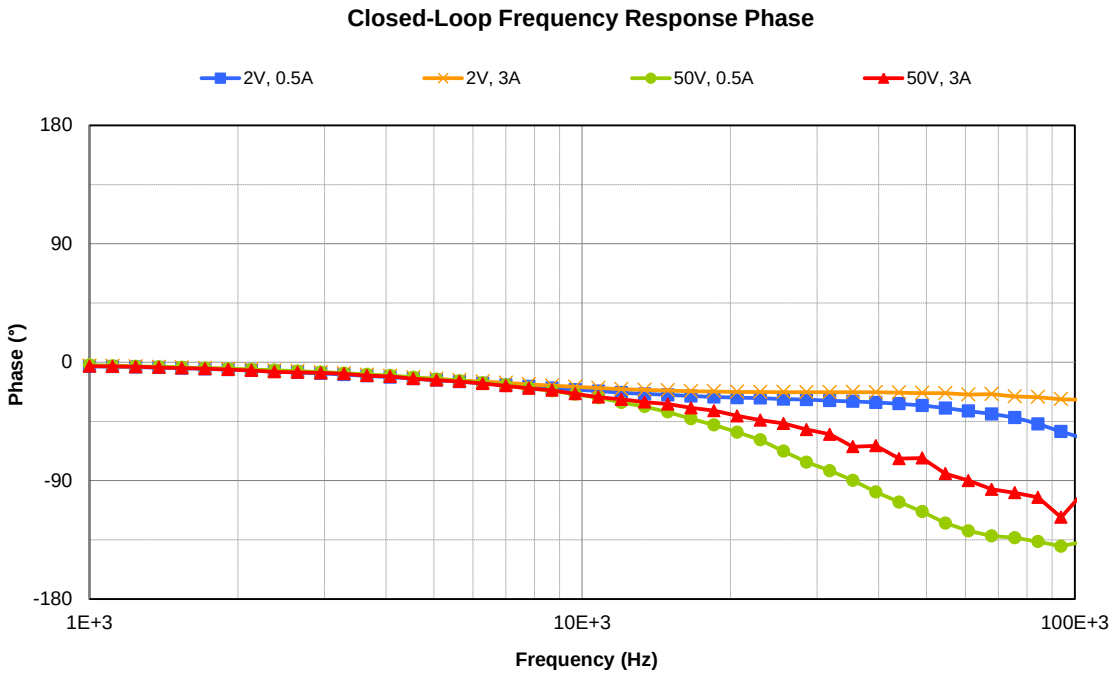


Figure 5.11 – Phase of the corner-case control-to-output frequency response measurements of the compensated gain-scheduled system, captured in simulation.

Operating Point		Loop Gain Cross-over Frequency	Phase Margin	Gain Margin	Control-to-Output B.W. (-3 dB)
2 V	**0.5 A**	23 kHz	100°	9.5 dB	17 kHz
2 V	**3 A**	25 kHz	101°	6 dB	18 kHz
50 V	**0.5 A**	19 kHz	63°	14 dB	34 kHz
50 V	**3 A**	16 kHz	83°	15 dB	28 kHz

Table 5.3 – Summary of key simulated results of the digitally compensated system at the four corner-case operating points.

The response of the compensated gain-scheduled system to a 10% input step and 1 V load transient are shown in Figure 5.12 and Figure 5.13, respectively. Note that the results in both cases are more similar across operating points than the corresponding plots from the non-gain-scheduled case (Figure 4.12 and Figure 4.13). There is still substantial variability in the load step response particularly at 2 V, 0.5 A. This is due to the NC-PRCs lower open-loop output impedance at light loads (as implied by the steep portions of the converter's constant-frequency curves in Figure 2.7) which is not accounted for by the gain-scheduling system. The noise is also noticeably larger and has more pronounced periodic components than in the non-gain-scheduled case at the 3 A operating points. As described on page 77, an analysis showed that this is likely caused by increased modulator aliasing artifacts resulting from the relatively higher controller gain at high currents resulting from gain scheduling as shown in Figure 5.4.

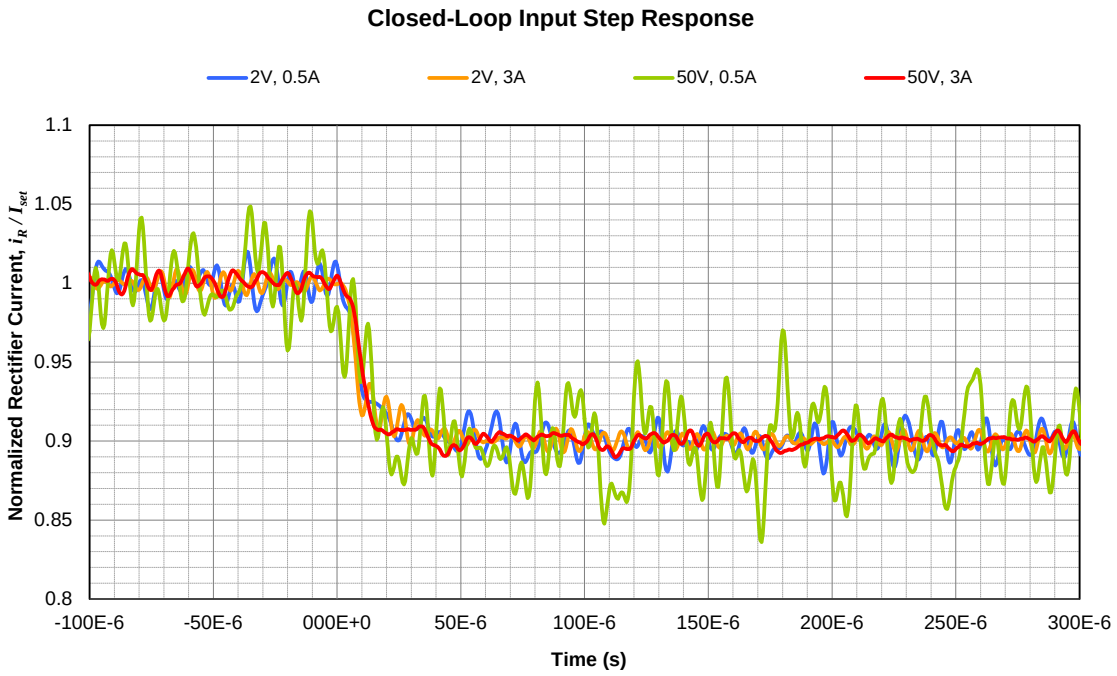


Figure 5.12 – Simulated corner-case closed-loop response of the gain-scheduled system's average* rectifier current to a step in the current set-point from 100% to 90%.

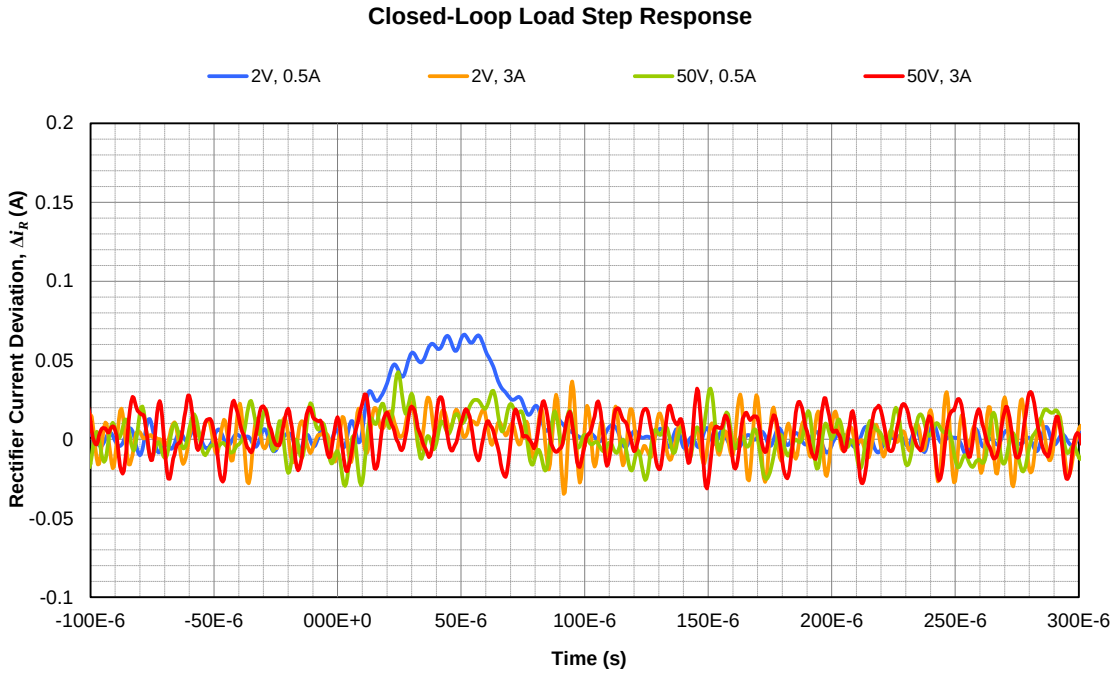


Figure 5.13 – Simulated corner-case closed-loop response of the gain-scheduled system's average* rectifier current to a 1 V, 50 µs load step.

* Ripple was filtered using a 200 kHz 8th-order elliptic low-pass filter with 1 dB / 80 dB pass- / stop-band ripple.

Chapter 6: Experimental Validation

6.1 Prototype design

To validate the simulation results obtained for the gain-scheduled controller design in Chapter 5 I designed and built a prototype of the subject converter and controller. Figure 6.1 shows a high-level block diagram of the prototype hardware. The complete schematic and PCB layout are shown in Appendix C.

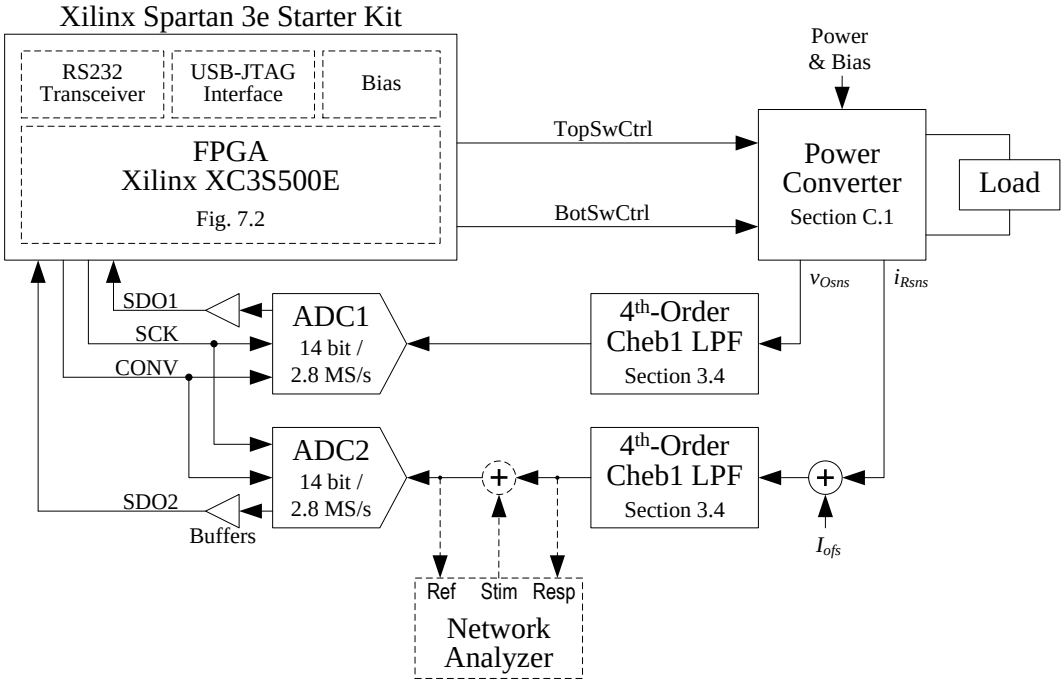


Figure 6.1 – High-level block diagram of the prototype hardware.

I chose to implement the controller using a Xilinx Spartan 3e Starter Kit, which is an off-the-shelf development board that includes a Xilinx XC3S500E FPGA, power supplies, a USB interface for configuration and debugging, and an RS232 serial port.

The controller design was created in Xilinx's ISE9.2 development environment using a combination of schematics, high-level system diagrams (using Xilinx System Generator 9.2 running in Simulink), and canned Xilinx IP (a PicoBlaze soft-core 8 bit microcontroller and UART). All filter scaling was done using algorithms written in Matlab M-code. The controller was made configurable from a PC through the use of the RS232 interface and the microcontroller, which was programmed to accept a basic command set. This allowed the converter current to be set and the dithering, compensation, and gain scheduling to be enabled or disabled using PC-based instrument automation tools. A high-level block diagram of the controller's FPGA design is shown in Figure 6.2, and selected portions of the controller schematics are shown in Appendix D.

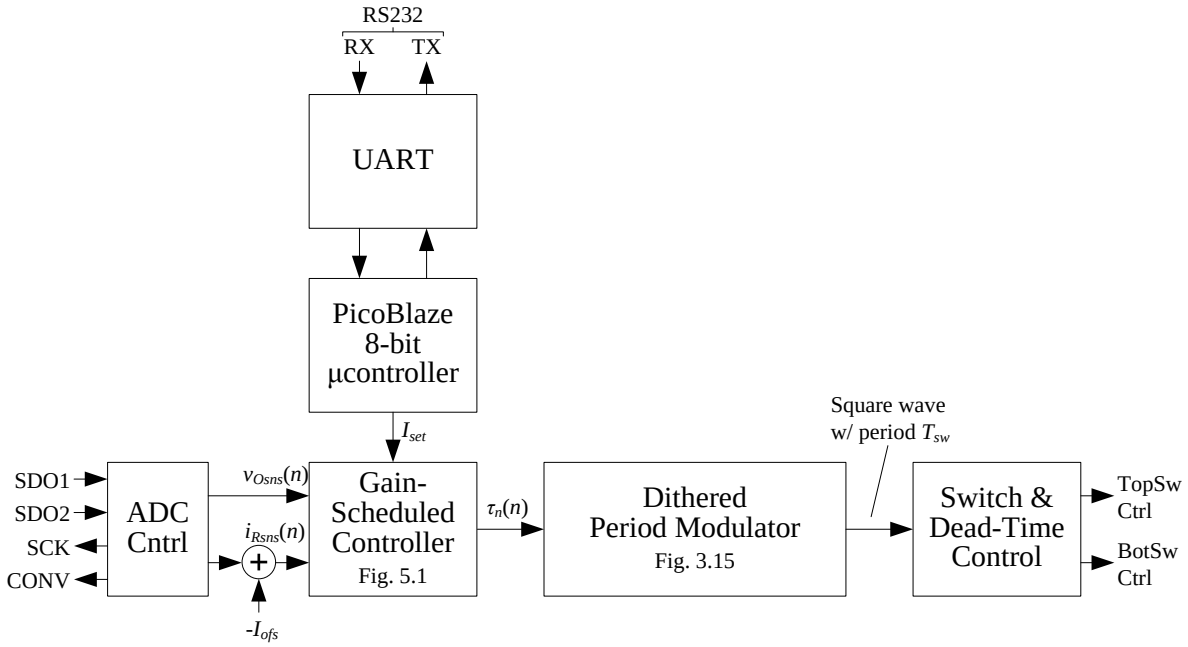


Figure 6.2 – High-level block diagram of the controller's FPGA design.

Converter Waveforms

After building and testing the converter, I measured four critical steady-state converter waveforms: rectifier current, resonant inductor current, the voltage across to resonant tank, and the resonant capacitor voltage. Plots of these waveforms at the four corner-case conditions are shown in Figure 6.3 through Figure 6.6.

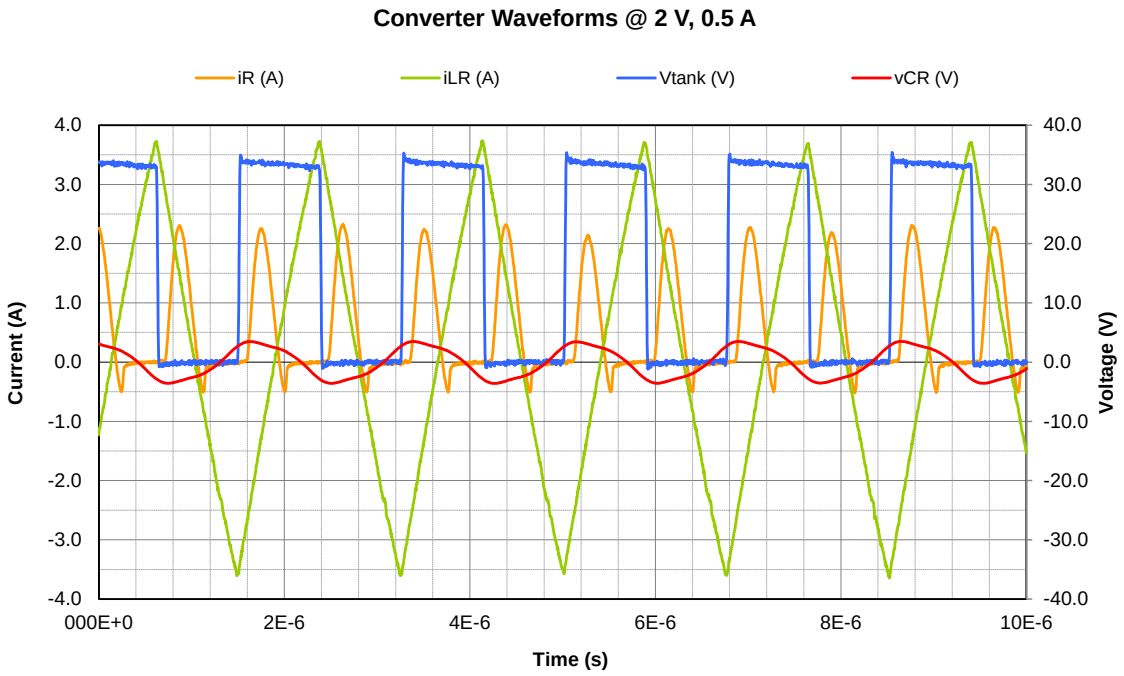


Figure 6.3 – Steady-state prototype converter waveforms at 2 V, 0.5 A operating point.

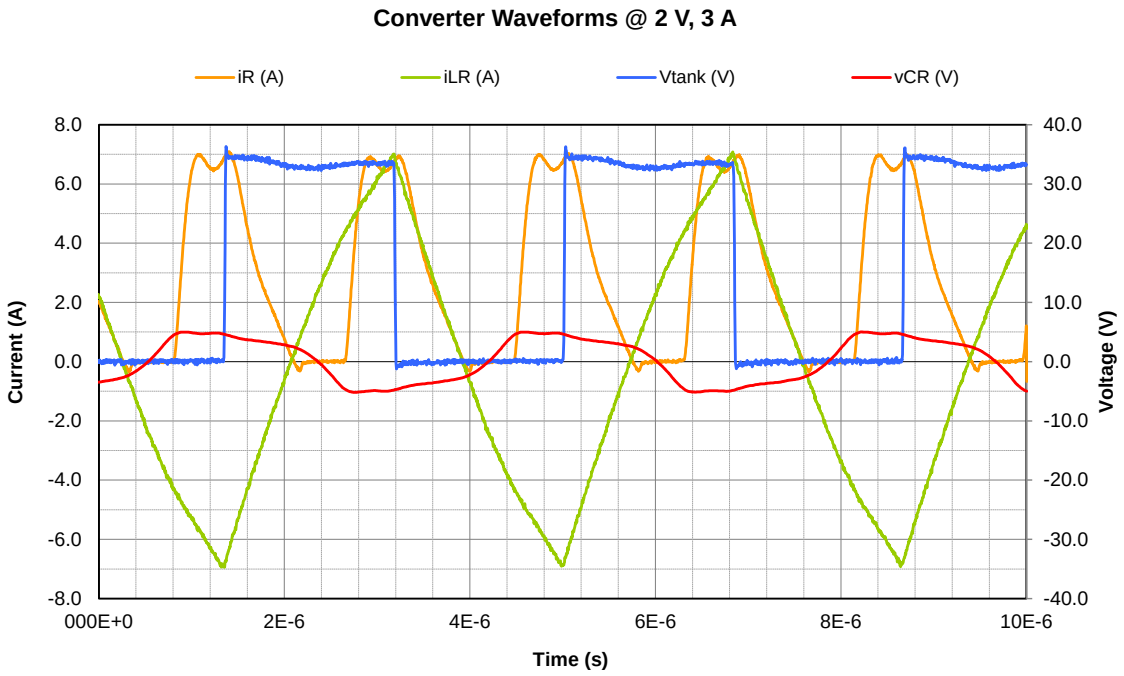


Figure 6.4 – Steady-state prototype converter waveforms at 2 V, 3 A operating point.

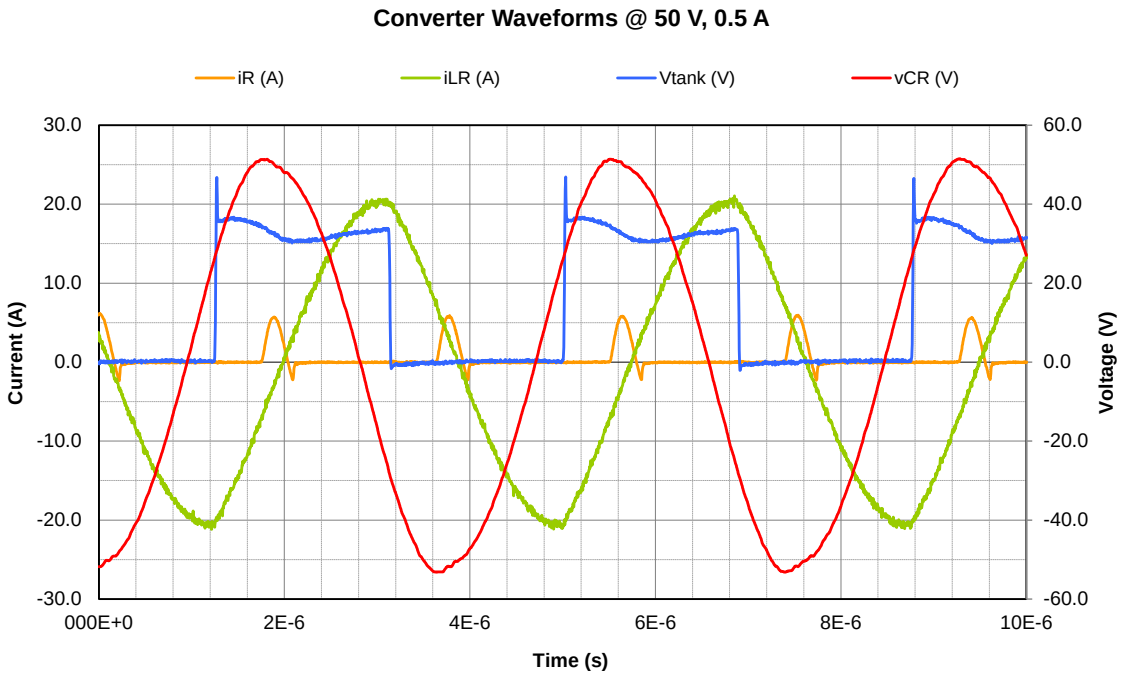


Figure 6.5 – Steady-state prototype converter waveforms at 50 V, 0.5 A operating point.

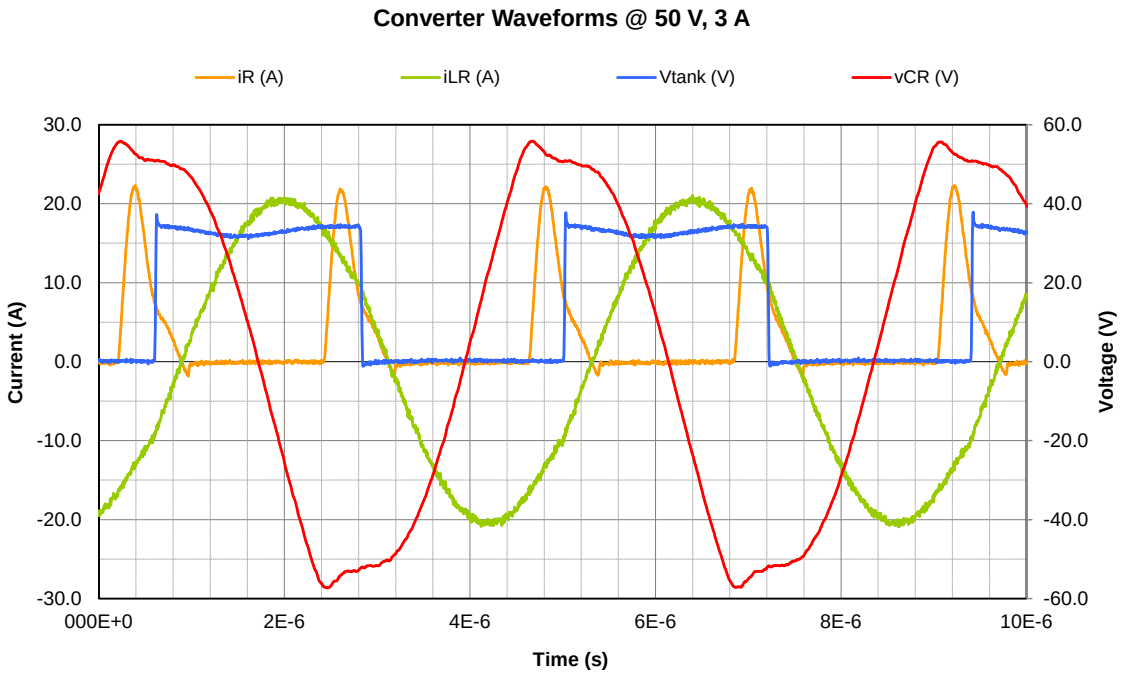


Figure 6.6 – Steady-state prototype converter waveforms at 50 V, 3 A operating point.

6.2 Gathering Gain Scheduling Data

I followed the same process used in Chapter 5 (shown in Figure 5.3) to design the prototype's controller. Using the prototype hardware shown in Figure 6.1, an electronic load, and a network analyzer, I measured the loop gain of the uncompensated system at 10 kHz at a series of 32 × 32 points over the converter's entire operating range. This process was automated using a program running in Excel VBA that swept the converter's operating point (by changing the converter's current setting and the load's voltage setting) and made loop gain measurements (using the network analyzer). In contrast to the simulation-based approach in Section 5.4, it took less than one hour to capture all of the gain-scheduling data from the prototype. With effort, that time could likely be substantially reduced.

As in Section 5.4, using a k_{fp} of 0.25 (to keep $k_c[I_R, V_O] < 1$ for convenient fixed-point implementation), I computed the prototype's gain correction function, $k_c[I_R, V_O]$, which is shown plotted in Figure 6.7.

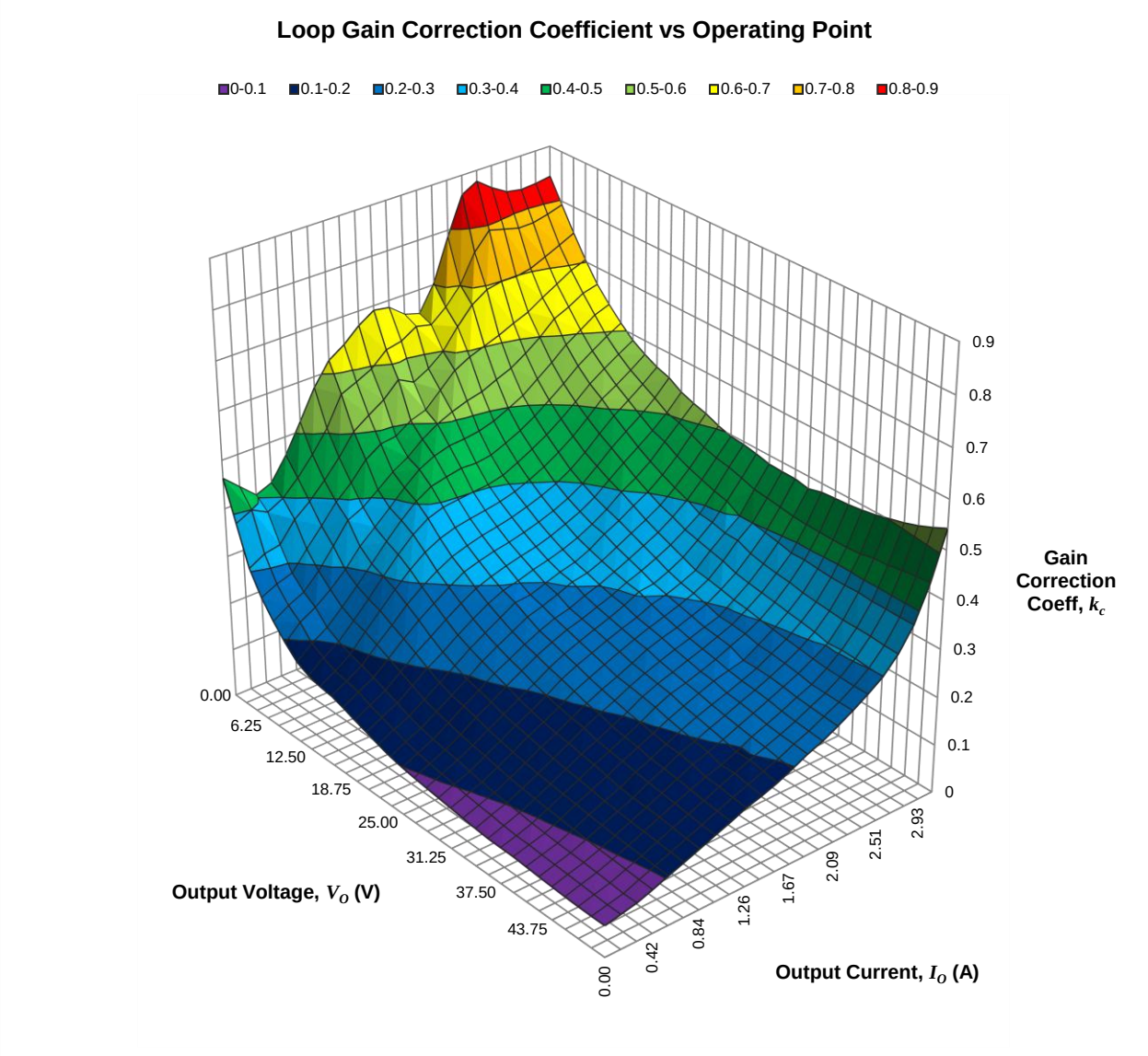


Figure 6.7 – Surface plot of the prototype's gain correction LUT function, $k_c[I_R,V_O]$, versus operating point, based on data captured experimentally at f_{corr} = 10 kHz.

6.3 Compensation

After incorporating the gain scheduling LUT data shown in Figure 6.7 into the controller, the loop gain of the uncompensated system was measured at the four corner-case operating points using a network analyzer. The results are shown plotted in Figure 6.8 and Figure 6.9.

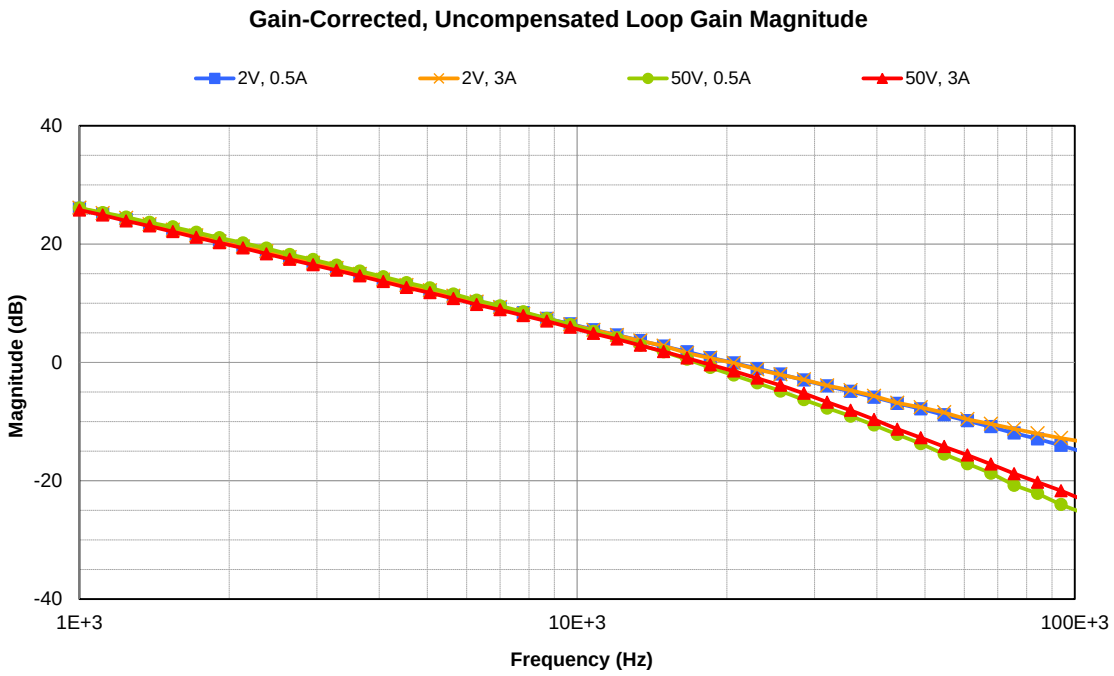


Figure 6.8 – Magnitude of the corner-case loop gain measurements of the uncompensated gain-scheduled system, captured experimentally (corresponds to simulation results in Figure 5.5).

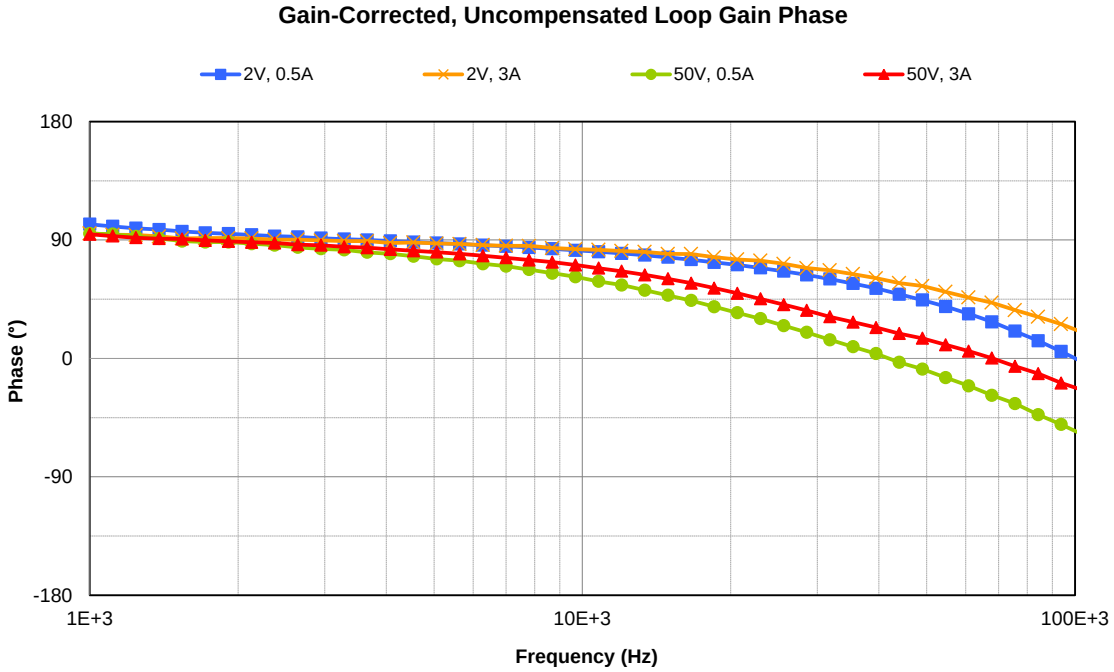


Figure 6.9 – Phase of the corner-case loop gain measurements of the uncompensated, gain-scheduled system, captured experimentally (corresponds to simulation results in Figure 5.6).

Notice that the loop gain magnitudes look nearly identical below ~10 kHz, just like the similar plots in Section 5.5. Based on these uncompensated loop gain measurements, I used the same continuous-time controller design approach used in Section 5.5 to compensate the system. This yielded the *s*-domain integrator and compensator parameters shown in Table 6.1.

Parameter	Value
k_i	32 k
k_{dc}	0.807
s_{z1}	-116 krad/s
s_{z2}	-1.74 Mrad/s
s_{p1}	-276 krad/s
s_{p2}	-4.14 Mrad/s

Table 6.1 – Table of the continuous-time controller parameters resulting from compensating the gain-scheduled prototype.

This controller was then translated into *z*-domain following the process used in Section 4.3 which yielded the *z*-domain compensator coefficients shown in Table 6.2. The implied transfer function's frequency response is shown plotted in Figure 6.10 alongside the compensator from Section 5.5 for comparison. Although optimized independently, note that the two compensators are practically identical.

Coefficient	Value
b_0	3.3319
b_1	-4.9347
b_2	1.6681
a_0	1
a_1	-1.0511
a_2	0.1320

Table 6.2 – *z*-domain SOS coefficients for the prototype's compensator (before scaling for fixed-point implementation).

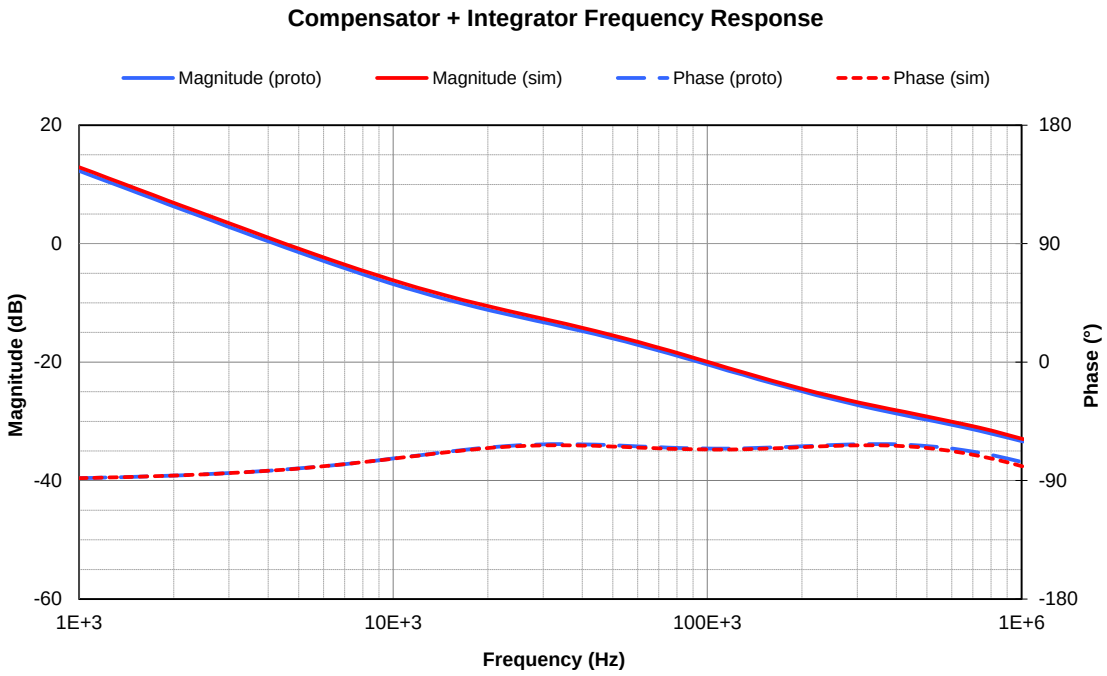


Figure 6.10 – Plot of the transfer function of the gain-scheduled system's *z*-domain compensator and integrator implied by the parameters from Table 6.2. The corresponding plot from the simulated system in Section 5.5 is included for comparison.

6.4 Experimental Results

The *z*-domain compensator implied by the parameters in Table 6.2 was added to the digital controller and the resultant compensated corner-case loop gains are shown in Figure 6.11, Figure 6.12, Figure 6.13, and Figure 6.14 alongside the corresponding plots from simulation.

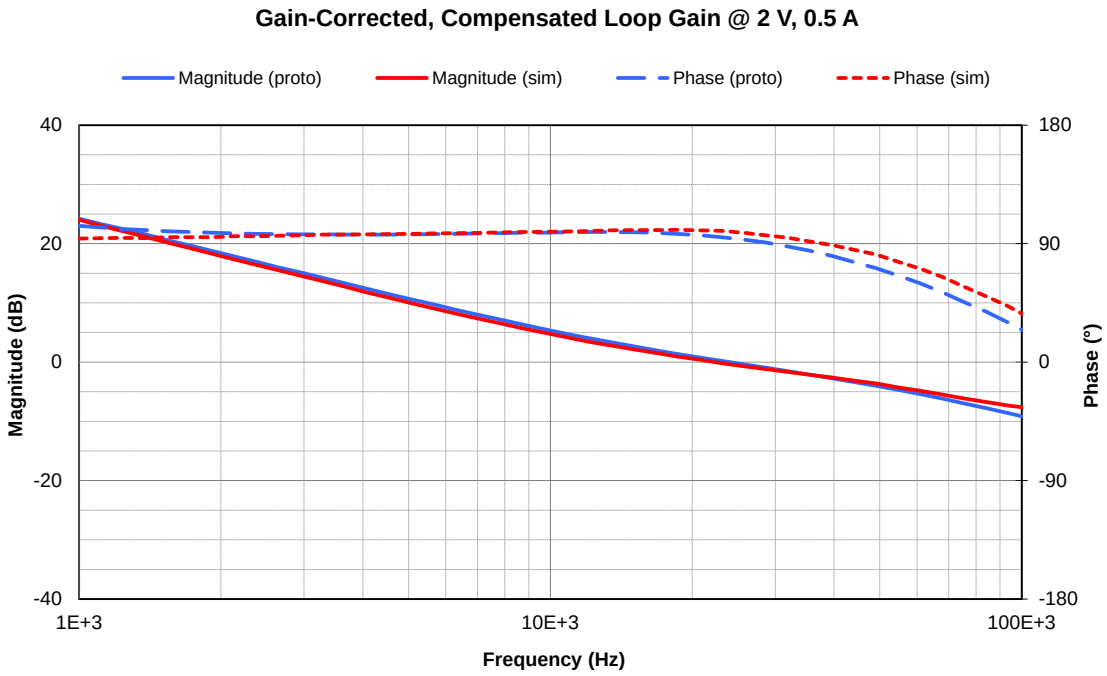


Figure 6.11 – Comparison of the simulated (from Figure 5.8 and Figure 5.9) and experimental loop gain measurements of the compensated gain-scheduled system at the 2 V, 0.5A operating point.

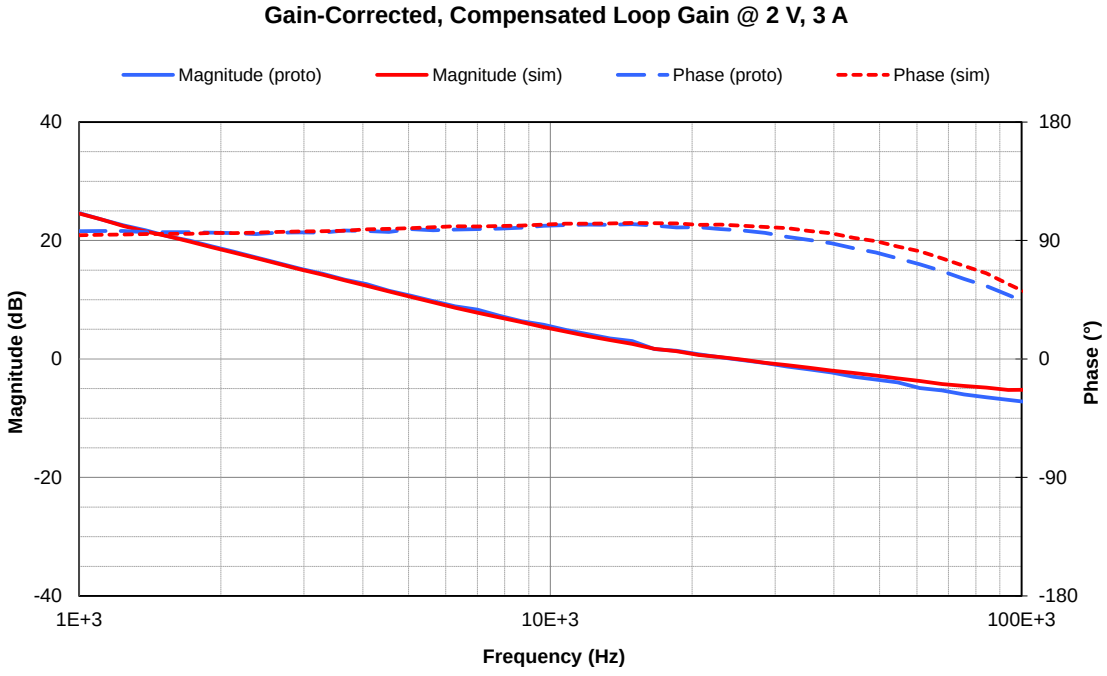


Figure 6.12 – Comparison of the simulated (from Figure 5.8 and Figure 5.9) and experimental loop gain measurements of the compensated gain-scheduled system at the 2 V, 3A operating point.

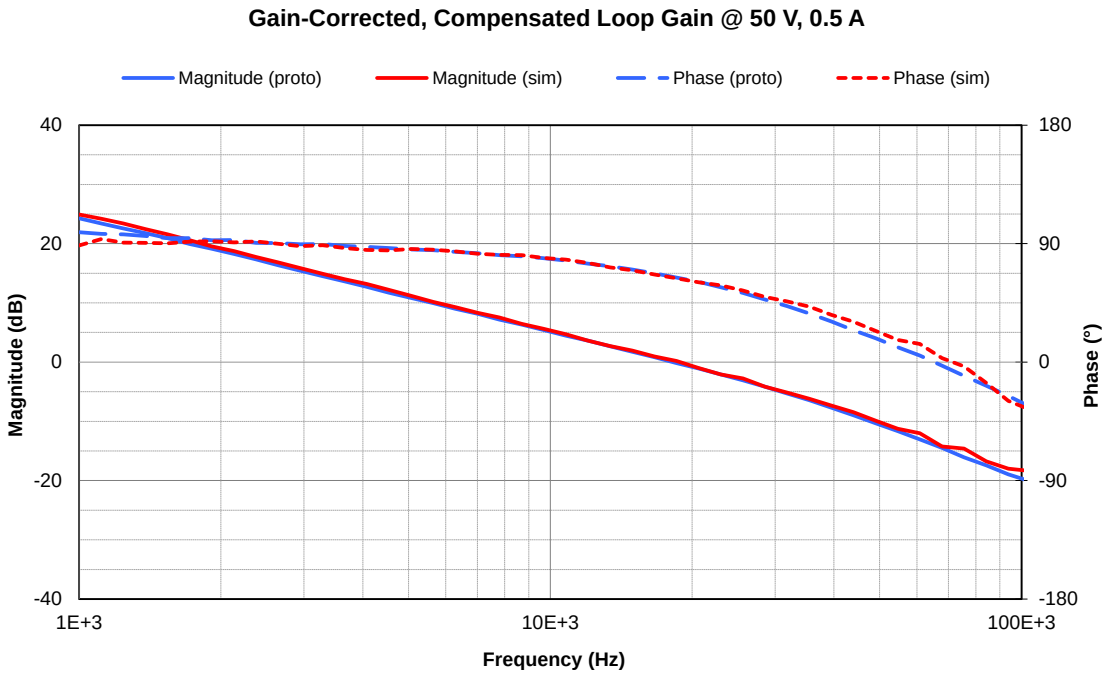


Figure 6.13 – Comparison of the simulated (from Figure 5.8 and Figure 5.9) and experimental loop gain measurements of the compensated gain-scheduled system at the 50 V, 0.5A operating point.

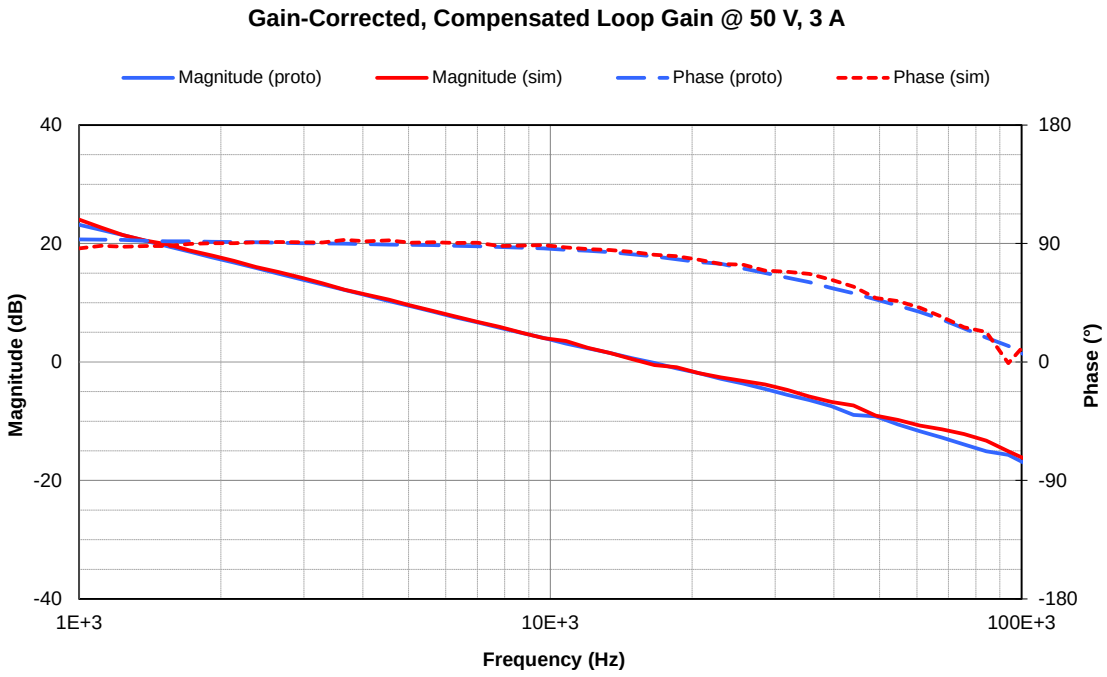


Figure 6.14 – Comparison of the simulated (from Figure 5.8 and Figure 5.9) and experimental loop gain measurements of the compensated gain-scheduled system at the 50 V, 3 A operating point.

Results under all four corner-case conditions are summarized in Table 6.3. Note that the closed-loop frequency response of the system could not be measured experimentally. This is a consequence of the reference for the control loop residing in the digital domain, preventing the use of a network analyzer. If this had been foreseen when the prototype was being designed, an extra ADC could have been added for this purpose and its effects modeled and corrected for in the results.

Operating Point		Loop Gain Cross-over Frequency	Phase Margin	Gain Margin	Control-to-Output B.W. (-3 dB)
2 V	**0.5 A**	24 kHz	94°	11 dB	*
2 V	**3 A**	24 kHz	98°	7 dB	*
50 V	**0.5 A**	18 kHz	64°	14 dB	*
50 V	**3 A**	16 kHz	80°	18 dB	*

** The closed-loop frequency response could not be measured experimentally.*

Table 6.3 – Summary of key results of the gain scheduled prototype at the four corner-case operating points.

The compensated gain-scheduled system's response to a 10% input step and 1 V load transient are shown in Figure 6.15 and Figure 6.16, respectively. Note that, as compared with the similar plots in Section 5.6 (Figure 5.12 and Figure 5.13), there is more pronounced periodic noise visible. As described on page 77, an analysis indicated that this is likely due to aliasing occurring in the modulator. Excluding this, the time-domain behavior of the prototype looks very similar to the simulated results.

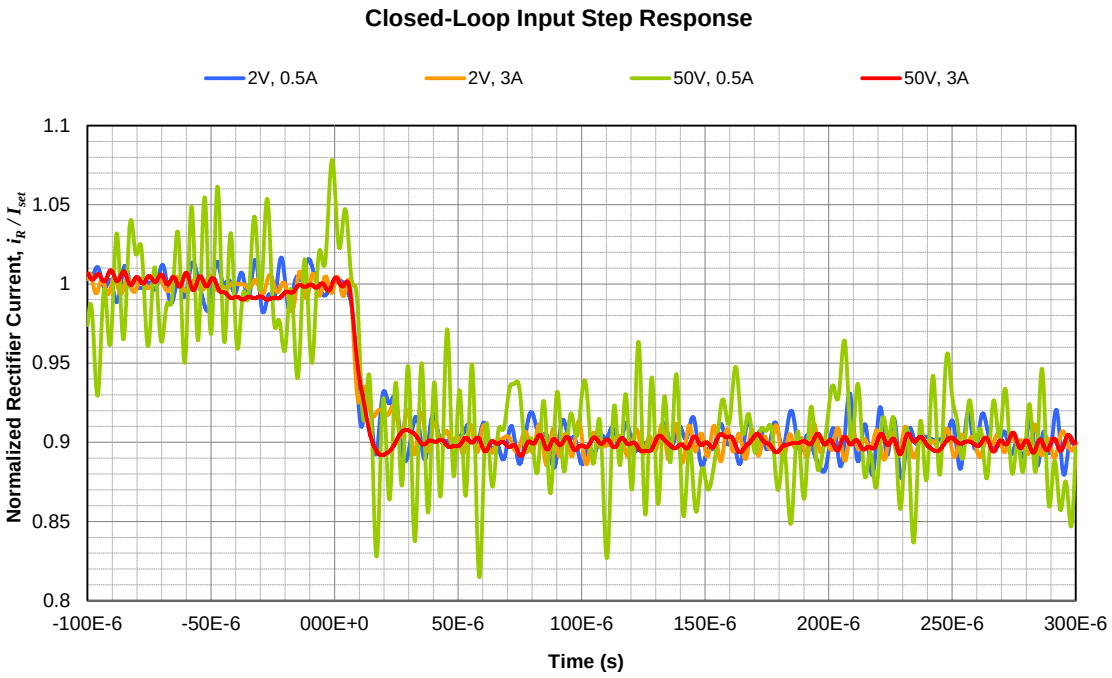


Figure 6.15 – Corner-case closed-loop response of the gain-scheduled prototype's average* rectifier current to a step in the current set-point from 100% to 90%.

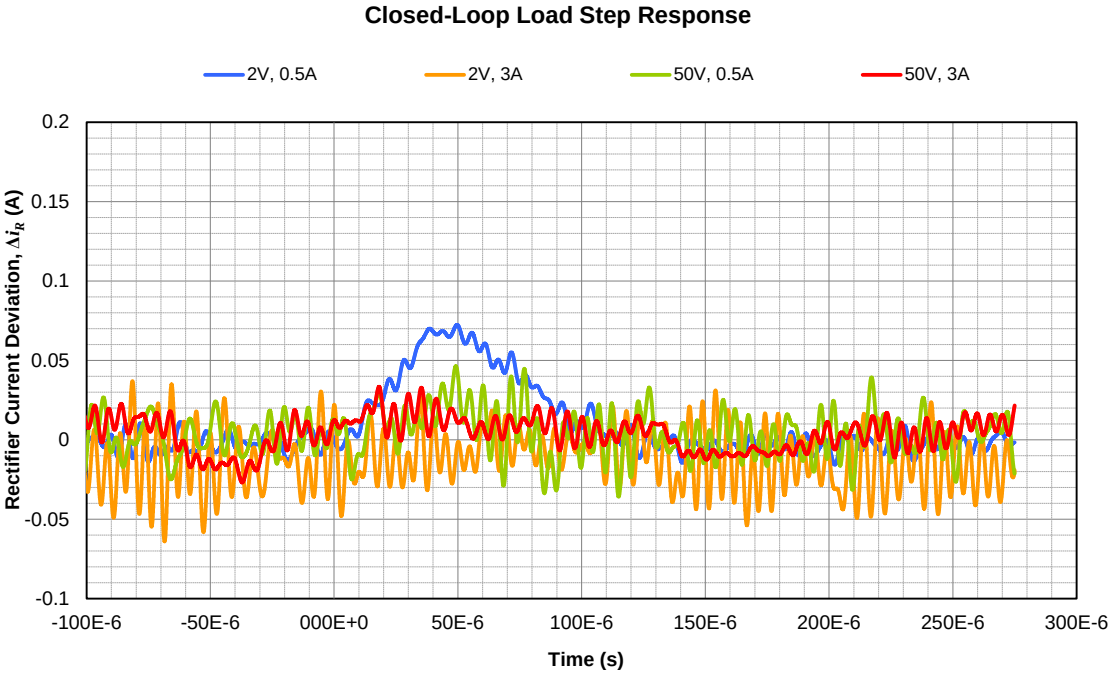


Figure 6.16 – Corner-case closed-loop response of the gain-scheduled prototype's average* rectifier current to a 1 V, 50 µs load step.

* Ripple was filtered using a 200kHz 8th-order elliptic low-pass filter with 1dB / 80dB pass- / stop-band ripple.

Closed-Loop Waveform Spectra

To gain insight into the effect of modulator dithering on the converter's behavior, I measured the spectra of a few converter signals (rectifier current, current feedback post anti-aliasing filter, and output voltage) using a spectrum analyzer*. In Figure 6.17 and Figure 6.19 notice the additional spectral components adjacent to the even harmonics when dithering is disabled, which likely indicate limit-cycling. With dithering enabled, these spectral components are absent and are instead replaced by a spread dithering noise spectrum that is similar to the transfer function of the dithering filter shown in Figure 3.16, as intended. In Figure 6.18 and Figure 6.20, however, there are pronounced narrowband spectral components despite dithering. An analysis indicated that this is a direct result of images of the residual 2nd harmonic ripple in the modulator input signal being aliased to low frequencies by the modulator. These are most pronounced at operating points where the controller's gain is high (due to gain-scheduling) and where the 2nd harmonic ripple frequency is low, resulting in the 2nd switching harmonic being attenuated less by the ripple filter and integrator.

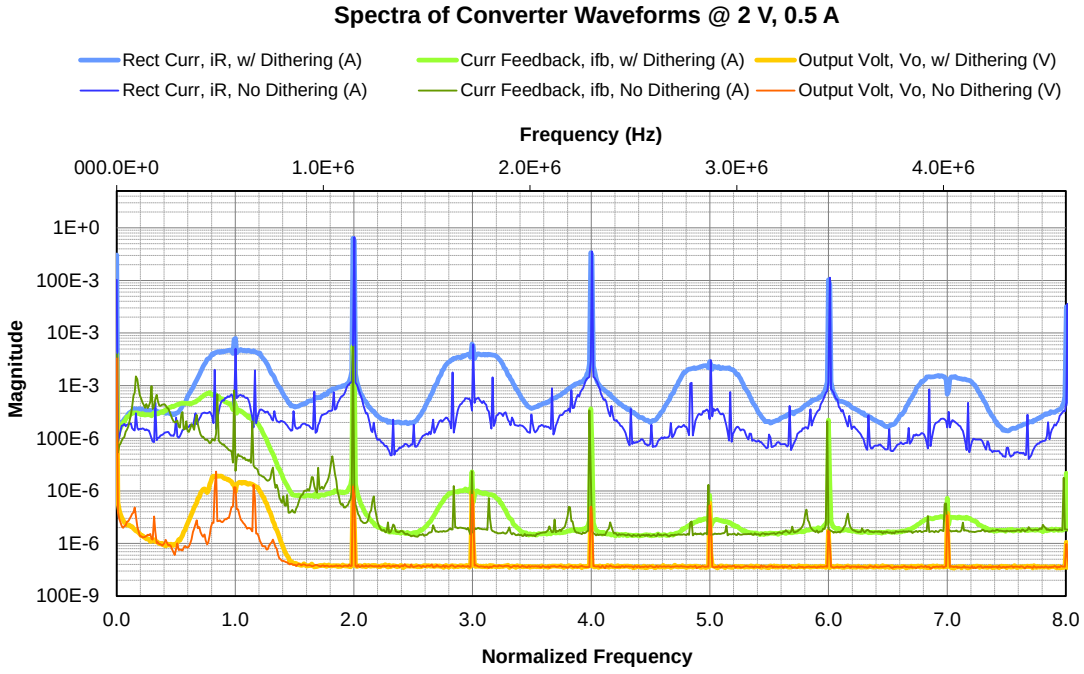


Figure 6.17 – Spectra of prototype converter waveforms while operating in steady-state at the 2 V, 0.5 A operating point, shown with modulator dithering enabled and disabled for comparison.

* The spectrum analyzer was configured to operate in 'positive peak-detect' mode. This allowed accurate measurement of narrowband spectral components but tends to over-emphasize the amplitude of wideband components (such as noise).

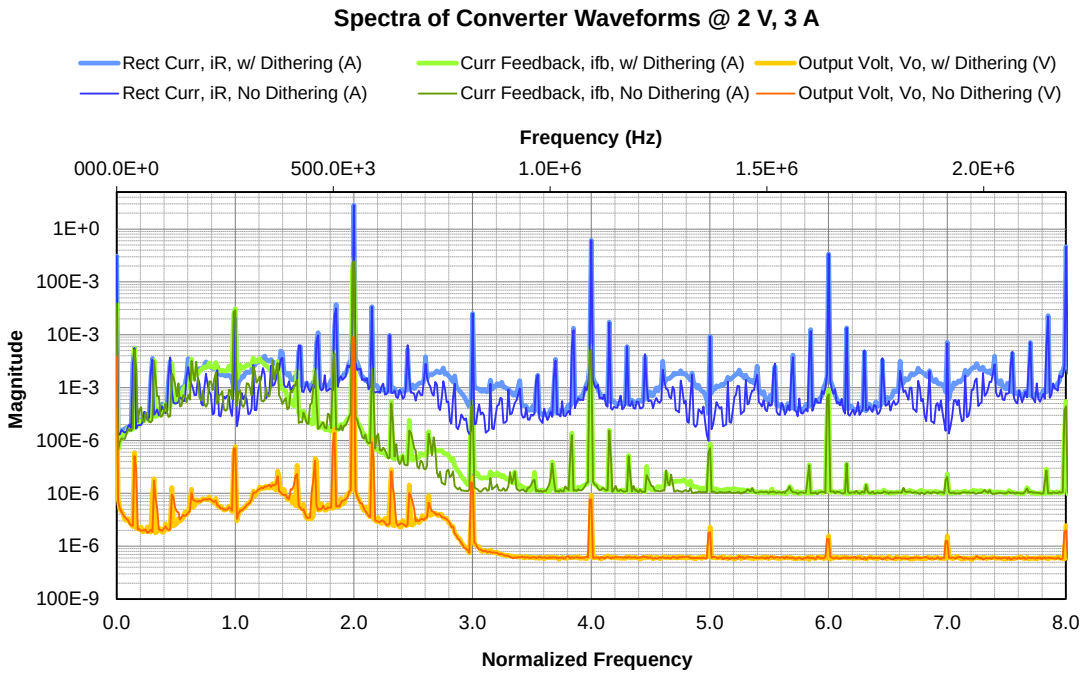


Figure 6.18 – Spectra of prototype converter waveforms while operating in steady-state at the 2 V, 3 A operating point, shown with modulator dithering enabled and disabled for comparison.

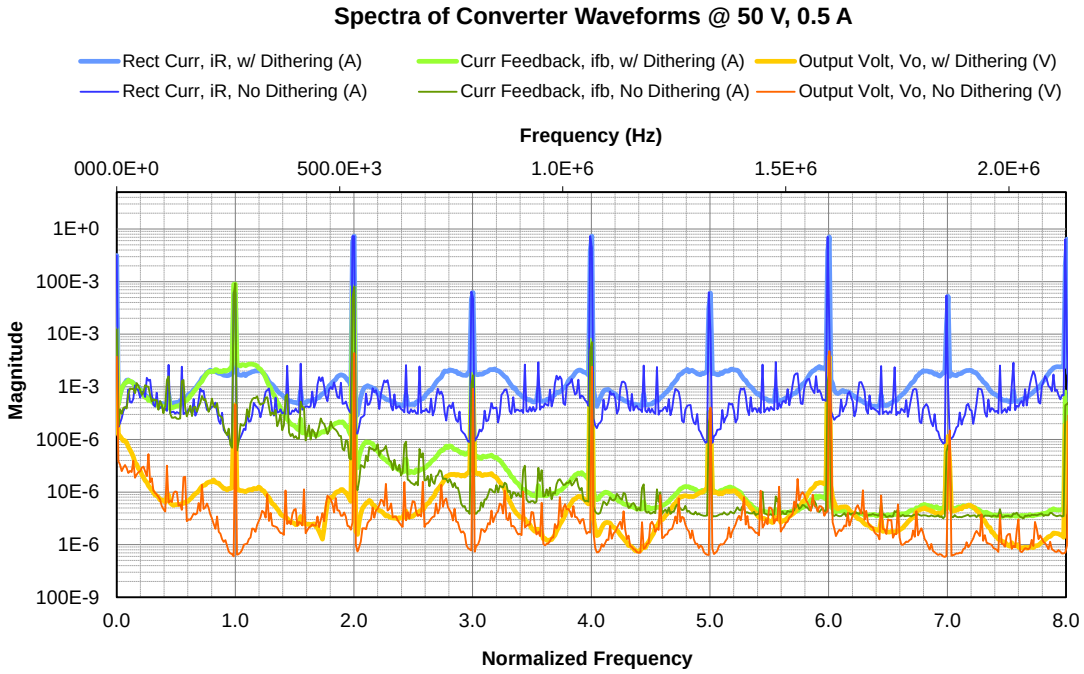


Figure 6.19 – Spectra of prototype converter waveforms while operating in steady-state at the 50 V, 0.5 A operating point, shown with modulator dithering enabled and disabled for comparison.

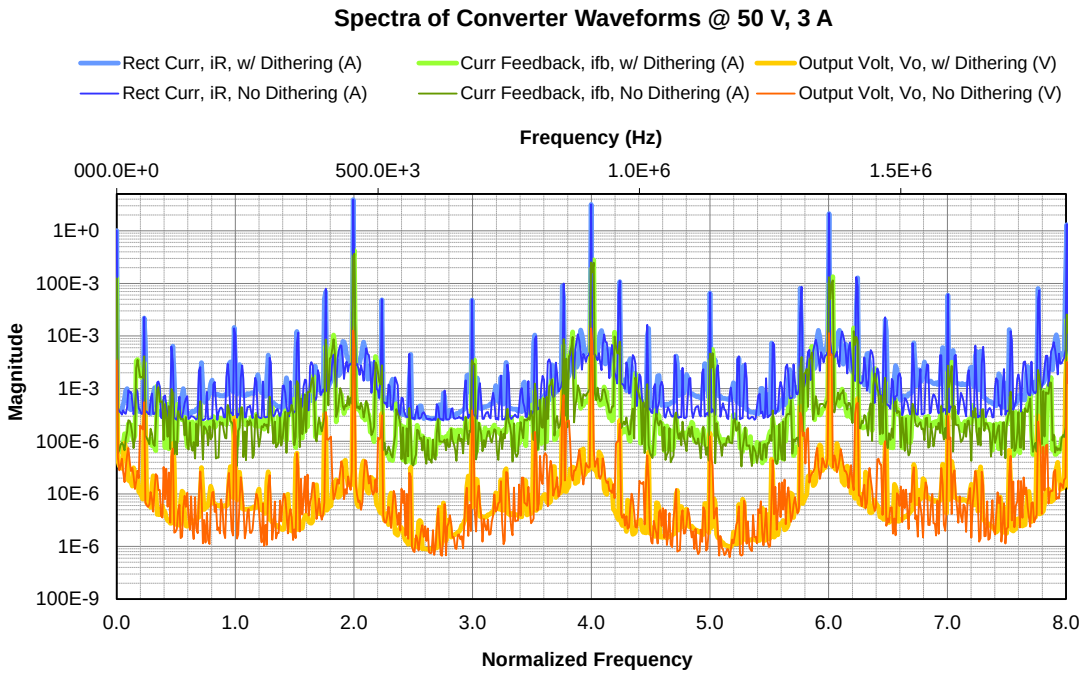


Figure 6.20 – Spectra of prototype converter waveforms while operating in steady-state at the 50 V, 3 A operating point, shown with modulator dithering enabled and disabled for comparison.

Chapter 7: Conclusions and Possible Further Research

7.1 Conclusions

Table 7.1, Figure 7.1 and Figure 7.2 show comparisons of key frequency domain performance metrics and the transient behaviors of the different control approaches investigated in this research. These were captured at the worst-case operating point based on the assumption that the system is only as good as its worst-case performance over the expected operating locus.

Metric	Analog Classical Control	Digital Classical Control	Gain-Sched. Digital Control	
			Simulation	Experiment
Worst-Case Control-to-Output B.W.	4.8 kHz	3.3 kHz	17 kHz	*
Worst-Case Phase Margin	63°	62°	63°	64°
Worst-Case Gain Margin	7.5 dB	6.5 dB	6 dB	7 dB

** The closed-loop frequency response could not be measured experimentally for reasons explained in Section 6.4.*

Table 7.1 – Comparison of frequency domain performance metrics of the different control approaches investigated.

The results in Table 7.1 show that the gain-scheduled system achieved a nearly 4:1 improvement in worst-case control bandwidth over the classical control systems while maintaining similar stability margins. The improvement in responsiveness is evident in the transient plots.

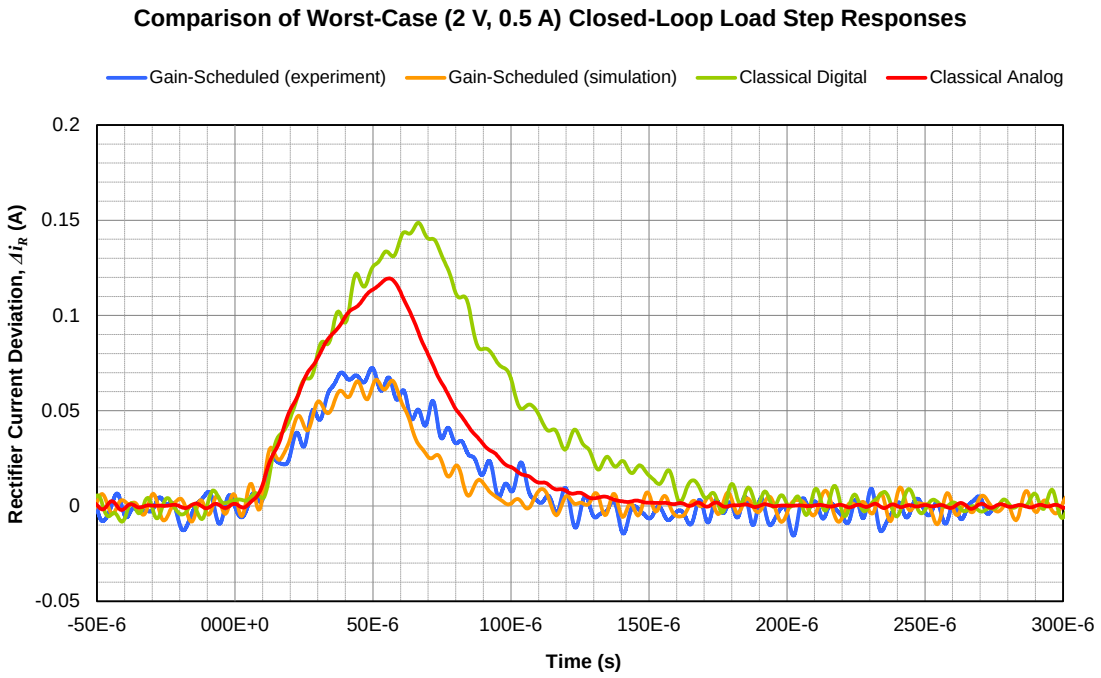


Figure 7.1 – Comparison of the converter's worst-case input step transient response* with each of the control approaches investigated (from Figure 6.15, Figure 5.12, Figure 4.12, and Figure 2.19).

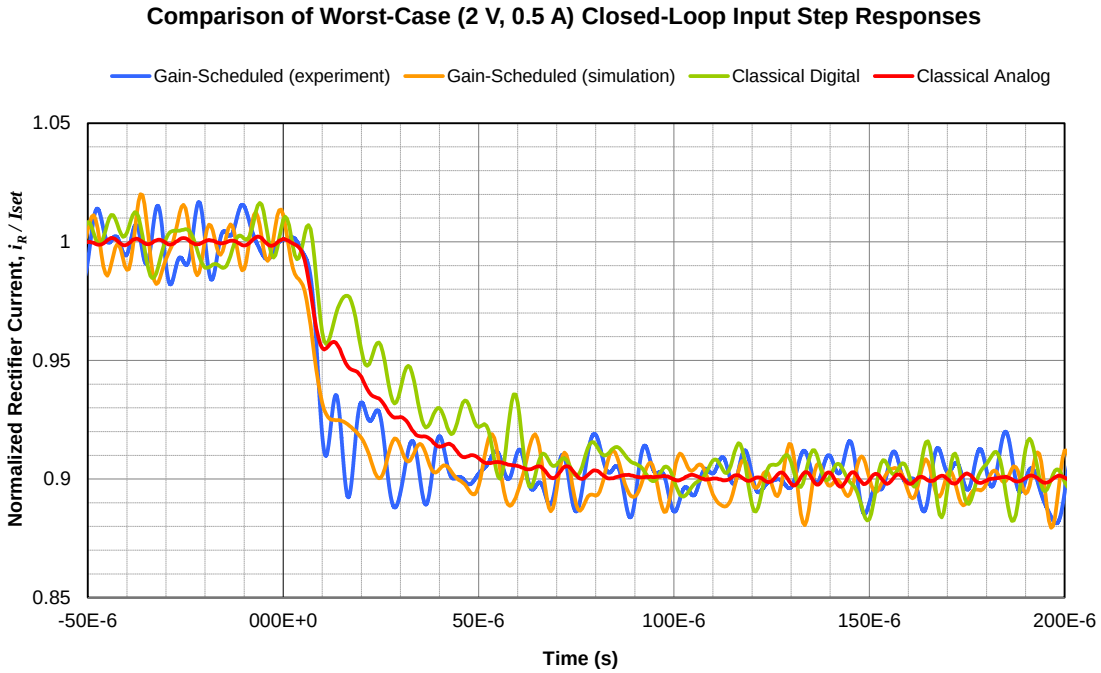


Figure 7.2 – Comparison of the converter's worst-case load step transient response* with each of the control approaches investigated (from Figure 6.16, Figure 5.13, Figure 4.13, and Figure 2.20).

* Ripple was filtered using a 200kHz 8th-order elliptic low-pass filter with 1dB / 80dB pass- / stop-band ripple.

Four conclusions can be reasonably drawn from these results:

1. Gain-scheduled digital control provides a large (~4:1) improvement in worst-case control bandwidth over the classical analog and digital control approaches without compromising stability margins. In addition, it yields more consistent closed-loop behavior over the operating locus.

2. As a result of the increased controller gain it creates at some operating points, the addition of gain scheduling makes the system more susceptible to aliasing in the modulator. This could be addressed by
    a. improving ripple attenuation by either altering the analog anti-aliasing filter or adding additional poles to the compensator (both likely at the expense of some reduction in performance to maintain stability margins) or
    b. increasing the complexity of the gain scheduling controller to include better ripple attenuation under high gain conditions.

3. Implementing an analog control design in the digital domain (as done with the classic digital control approach) results in substantially increased design complexity and cost (FPGA, ADCs, etc.) and slightly (30%) degraded performance. Unless one capitalizes on the more advanced control approaches or other enhancements that digital control makes possible (e.g. gain scheduling, soft re-configurability, or elimination of compensation parameter tolerances) it is not a logical choice for this type of converter design.

4. The digital implementations investigated here all resulted in higher sub-harmonic noise in the converter's output as compared with the analog implementation[*] as a result of dithering. This could be improved upon with a higher-resolution period.

Although these conclusions were drawn from simulations and experiments performed on a scaled-down, 150 W, 50 V converter, they can be reasonably expected to apply to the 30 kW, 10 kV converter on which it was based, or to similar converters of any power level.

7.2 Possible Further Research

1. Modify the controller and / or anti-aliasing filter design (to provide better ripple rejection thereby reducing modulator aliasing artifacts), while minimizing the adverse impact on dynamic performance.

2. Investigate limiting the proportional gain scheduling correction to a specific frequency range (using a controller such as the one shown in Figure 7.3) to reduce the operating point-dependent noise caused by switching ripple that is aliased by the modulator.

[*] This is of arguable significance since the injected noise would be overwhelmed by the rectifier current's large switching ripple were it not for the aggressive filters being used to enable observation of the average rectifier current.

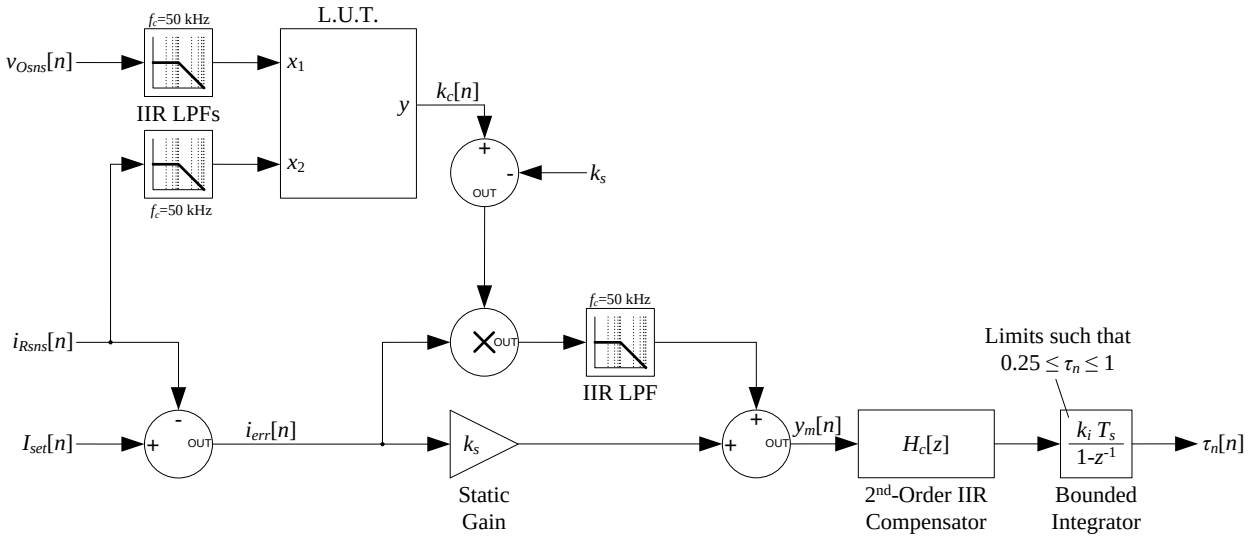


Figure 7.3 – Block diagram of proposed improved gain-scheduled controller.

3. Investigate the sensitivity of the gain-scheduling approach to tolerances and temperature drift of key component parameters.

4. Investigate the stability of the gain-scheduled system including all nonlinear effects.

5. Extend proportional gain scheduling into full compensator scheduling, allowing compensator coefficients to move with operating point.

6. Investigate ripple cancellation or a digital notch filter that tracks the 2nd switching harmonic to eliminate the steady-state ripple in T_n. What effect would this have on stability?

7. Investigate the optimal oversampled ADC configuration for a digital feedback system to minimize phase lag while still meeting minimum anti-aliasing requirements.

8. Optimize the Chebyshev anti-aliasing filter's pass band ripple to improve achievable control bandwidth.

9. Investigate the optimal filter design and corner frequency for the gain-scheduling LUT's filters and how they relate to the control bandwidth.

10. Use a technique such as the Extended Describing Function Method [20] to create an accurate small-signal model of the NC-PRC converter to allow optimization of the compensation using modern control design techniques (such as LQG or LQR).

11. Investigate how the performance of modern or other non-linear control techniques compare with the results obtained here.

Chapter 8: References

[1] P. P. Bonissone, P. S. Khedkar, and M. J. Schutten, "Fuzzy logic control of resonant converters for power supplies," *Proceeding of the 4th Annual IEEE Conference on Control Applications*, vol. 1, pp. 323–328, Sep. 1995.
[2] J. Chen, A. Prodic, R. W. Erickson, and D. Maksimovic, "Predictive digital current programmed control," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 411–419, Jan. 2003.
[3] C. Hattrup, H. W. van der Broeck, and M. Ossmann, "Fast estimation techniques for digital control of resonant converters," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 365–372, jan 2003.
[4] P. R. Holme and C. D. Manning, "Digital control of high frequency pwm converters," *Fifth European Conference on Power Electronics and Applications*, vol. 4, pp. 260–265, Sep. 1993.
[5] S. D. Johnson, "Steady-state analysis and design of the parallel resonant converter," Master's thesis, University of Colorado, 1986.
[6] S. D. Johnson and R. W. Erickson, "Steady-state analysis and design of the parallel resonant converter," *IEEE Transactions on Power Electronics*, vol. 3, no. 1, pp. 93–104, Jan. 1988.
[7] P. Kokotovic, "Separation of time-scales in modeling and control," *IEEE Conference on Decision and Control including the 14th Symposium on Adaptive Processes*, vol. 14, no. 1, pp. 463–466, 1975.
[8] C. Lee and S. Sooksatra, "Current programmed control nonresonant coupled parallel resonant converter," *IEE Proceedings-G*, vol. 138, no. 3, pp. 372–376, Jun. 1991.
[9] S. B. Leeb, "Putting profit into power electronic products with digital control," *Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition*, vol. 1, pp. 35–44, 2004.
[10] Y.-F. Liu and P. C. Sen, "Digital control of switching power converters," *Proceeding of the 2005 IEEE Conference on Control Applications*, vol. 1, pp. 635–640, Aug. 2005.
[11] D. Maksimovic, R. Zane, and R. W. Erickson, "Impact of digital control in power electronics," *Proceedings of 2004 International Symposium on Power Semiconductor Devices & ICs*, vol. 1, pp. 13–22, 2004.
[12] K. S. Mitra, *Digital Signal Processing: A computer-Based Approach*, 3rd, Ed. McGraw Hill, 2006.
[13] R. P. Sallen and E. L. Key, "A practical method of designing rc active filters," *IRE Transactions on Circuit Theory 2*, vol. 1, pp. 74–85, Mar. 1955.
[14] H. Sheng, W. Shen, H. Wang, D. Fu, Y. Pei, X. Yan, F. Wang, D. Boroyevich, F. C. Lee, and C. W. Tipton, "Design and implementation of high power density three-level parallel resonant converter for capacitor charger," *Twenty Second Annual IEEE Applied Power Electronics Conference*, vol. 1, pp. 745–749, Feb. 2007.
[15] H. Sheng, D. Fu, X. Yang, F. Wang, and F. C. Lee, "Comparison of zvs operation modes with and without phase shift for three-level resonant converters," *Proceedings of the Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition*, vol. 1, pp. 102–106, Mar 2006.

[16] S. Sooksatra and C. Lee, "Non-resonant coupled parallel resonant converter," *Proceedings of the 32nd Midwest Symposium on Circuits and Systems*, vol. 2, pp. 781–784, Aug. 1989.
[17] R. L. Steigerwald, "Analysis of a resonant transistor dc-dc converter with capacitive output filter," *IEEE Transactions on Industrial Electronics*, vol. IE-32, no. 4, pp. 439–444, Nov. 1985.
[18] P. Vallittu, T. Suntio, and S. J. Ovaska, "Digital control of power supplies - opportunities and constraints," *Proceeding of the 24th Annual Conference of the IEEE Industrial Electronics Society*, vol. 1, pp. 562–567, Aug. 1998.
[19] M. F. Wagdy, "Effect of various dither forms on quantization of ideal a/d converters," *IEEE Transactions on Instrumentation and Measurement*, vol. 38, no. 4, pp. 850–855, Aug. 1989.
[20] E. X.-Q. Yang, "Extended describing function method for small-signal modeling of resonant and multi-resonant converters," Ph.D. dissertation, Virginia Polytechnic Institute and State University, Blacksburg, Virginia, Feb. 1994.

Appendix A: NC-PRC Mode 1 Average Current Derivation

From [6], the normalized average output current of a NC-PRC can be derived to be

$$J = \frac{M_4\left[\frac{M_2(\gamma-\alpha)^2}{2} + M_1(\gamma-\alpha)\sin\alpha\right] - \frac{(M_1\sin\alpha)^2}{2}}{\gamma M_3} \tag{A.1}$$

where

$$\gamma \equiv \frac{\pi}{F} \tag{A.2}$$

and

$$\begin{aligned} \alpha &\equiv \arccos\left[M_2/M_1\right] \\ M_1 &\equiv (1-M_Q)+(M+2M_{D2}) \\ M_2 &\equiv (1-M_Q)-(M+2M_{D2}) \\ M_3 &\equiv 2-M_Q+M_{D1} \\ M_4 &\equiv (1+M_{D1})+(M+2M_{D2}) \end{aligned} \tag{A.3}$$

Assuming that all diode and switches are ideal ($\{M_Q, M_{D1}, M_{D2}\} = 0$) allows (A.3) to be simplified to

$$\begin{aligned} \alpha &\equiv \arccos\left[\frac{1-M}{1+M}\right] \\ M_1 &\equiv 1+M \\ M_2 &\equiv 1-M \\ M_3 &\equiv 2 \\ M_4 &\equiv 1+M \end{aligned} \tag{A.4}$$

Plugging (A.4) into (A.1) and applying the trigonometric identity

$$\sin\left[\arccos\left[\frac{1-M}{1+M}\right]\right] = \sqrt{1-\left(\frac{1-M}{1+M}\right)^2} \tag{A.5}$$

yields an ideal average output current of

$$J' =$$

$$\text{(A.6)} \qquad \frac{(1+M)\left[\frac{(1-M)(\gamma-\alpha)^2}{2}+(1+M)(\gamma-\alpha)\sqrt{1-\left(\frac{1-M}{1+M}\right)^2}\right]-\frac{\left((1+M)\sqrt{1-\left(\frac{1-M}{1+M}\right)^2}\right)^2}{2}}{2\gamma}$$

Assuming $M \geq 0$, recognizing that

$$\text{(A.7)} \qquad (1+M)\sqrt{1-\left(\frac{1-M}{1+M}\right)^2} = 2\sqrt{M} \quad \forall \quad \{M \geq 0\}$$

and simplifying yields

$$\text{(A.8)} \qquad J' = \frac{(1+M)\left[\frac{(1-M)(\gamma-\alpha)^2}{2}+2\sqrt{M}(\gamma-\alpha)\right]-2M}{2\gamma}$$

Further simplifying yields

$$\text{(A.9)} \qquad J' = \frac{(1+M)(\gamma-\alpha)\left((1-M)(\gamma-\alpha)+4\sqrt{M}\right)}{4\gamma}-\frac{M}{\gamma}$$

Plugging-in (A.2) and simplifying yields

$$\text{(A.10)} \qquad J' = \frac{(1+M)(\pi-F\alpha)\left((1-M)(\pi-F\alpha)+4F\sqrt{M}\right)}{4\pi F}-\frac{F\,M}{\pi}$$

Making the substitutions

$$\text{(A.11)} \qquad \begin{aligned} F &\rightarrow \omega_n \\ M &\rightarrow M_O \\ J &\rightarrow J_O \end{aligned}$$

And explicitly expressing α and J as functions to better align with the rest of this document yields

$$\text{(A.12)} \quad J_{O,\mathrm{M1}}[\omega_n, M_O] = \frac{(1+M_O)\left(\pi-\omega_n\alpha[M_O]\right)\left((1-M_O)\left(\pi-\omega_n\alpha[M_O]\right)+4\omega_n\sqrt{M_O}\right)}{4\pi\,\omega_n}-\frac{\omega_n M_O}{\pi}$$

where

(A.13) $$\alpha\left[M_O\right] = \arccos\left[\frac{1-M_O}{1+M_O}\right]$$

Appendix B: ARL Converter Simplification and Scaling

B.1 Simplification

The converter on which the subject converter is based is a three-level, high-density 30 kW NC-PRC (see Figure B.1) designed by a team of Virginia Tech graduate students and funded by the U.S. Army Research Lab (ARL), referenced in [14] and [15]. The converter is intended for use in a high pulse-power military application.

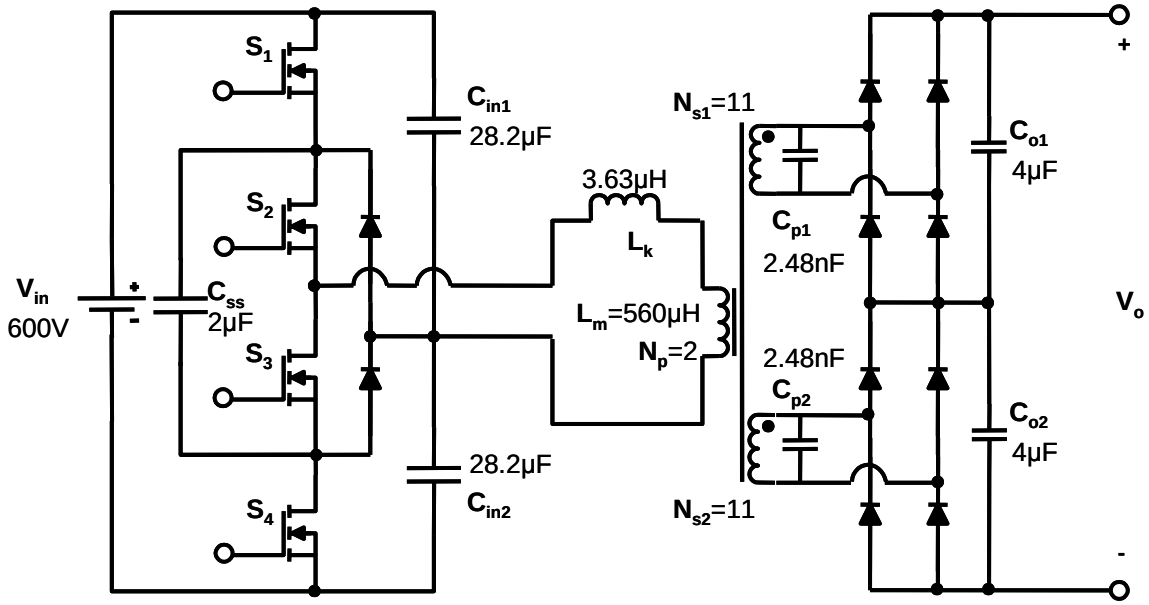


Figure B.1 – Three-level 30 kW pulsed power supply design used as the basis for the subject converter.

To facilitate prototyping, the converter was simplified using the following sequence of transformations, which assume ideal components and disregard component stresses.

Since this converter is operated with no phase shift (the top two switches are operated together, as are the bottom two) and component stresses are being disregarded, the three-level primary switch configuration can be equivalently replaced with a single pair of complementary switches and the primary diodes and C_{ss} can be eliminated, as shown in Figure B.2.

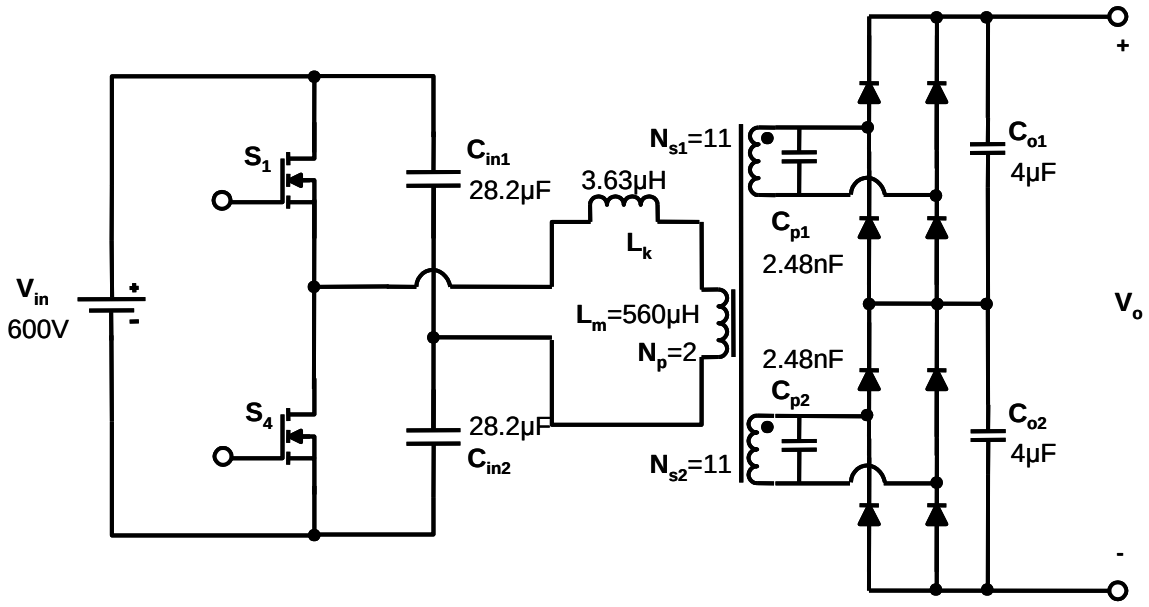


Figure B.2 – Behaviorally equivalent converter with a standard half-bridge switch configuration.

The resonant capacitors in Figure B.2 (C_{p1} and C_{p2}) are effectively in parallel and can be reflected to the primary and combined, creating a single resonant capacitor, C_p, of 150.04 nF as shown in Figure B.3.

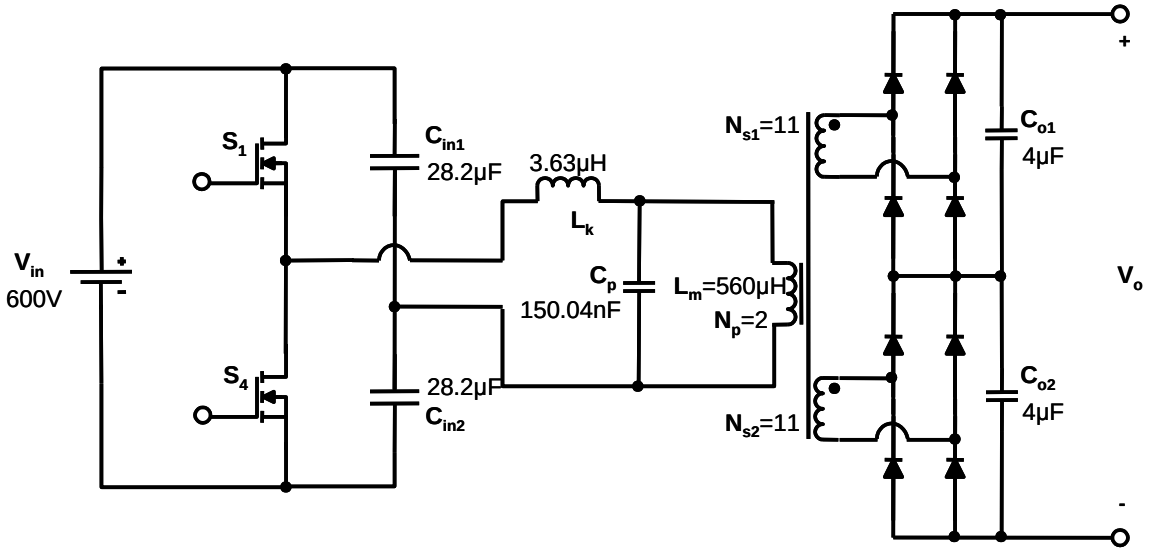


Figure B.3 – Behaviorally equivalent converter with the resonant capacitors reflected to the primary.

Since each secondary shown in Figure B.3 is ideally identical, each will assume precisely ½ of the output voltage. Therefore, the connection between the midpoint of capacitors C_{o1} and C_{o2} and the bridge carries no current and can be removed. This allows the series capacitors C_{o1} and

C_{o2} to be combined into a single output capacitor, C_o, of half the capacitance as shown in Figure B.4.

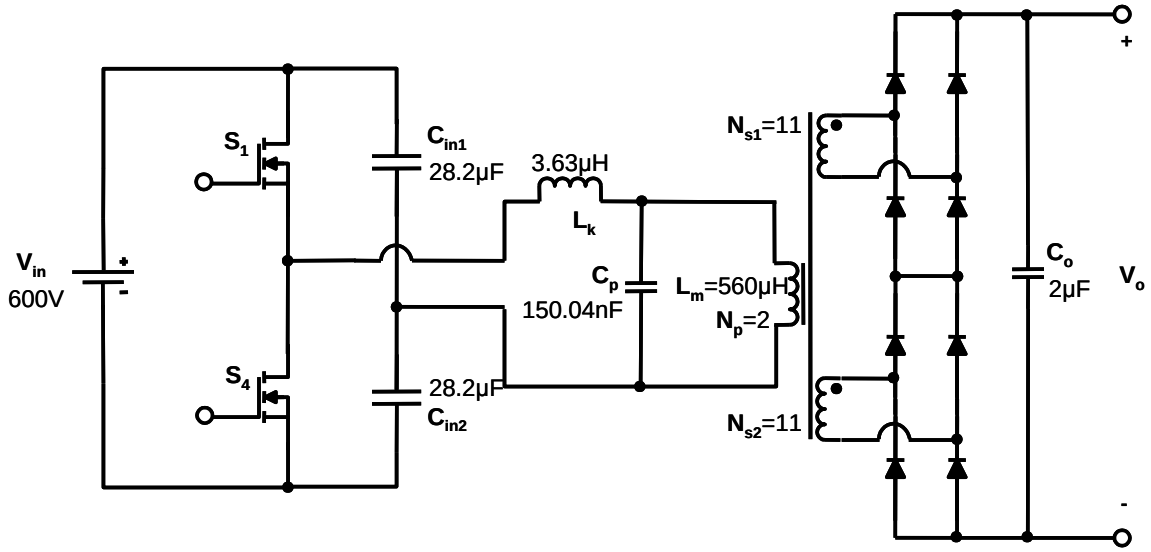


Figure B.4 – Behaviorally equivalent converter with a single output filter capacitor.

Assuming ideal diodes, the two duplicate 11-turn secondary windings and diode bridges in Figure A.4 can be equivalently combined into a single one with 22 turns as shown in Figure B.5.

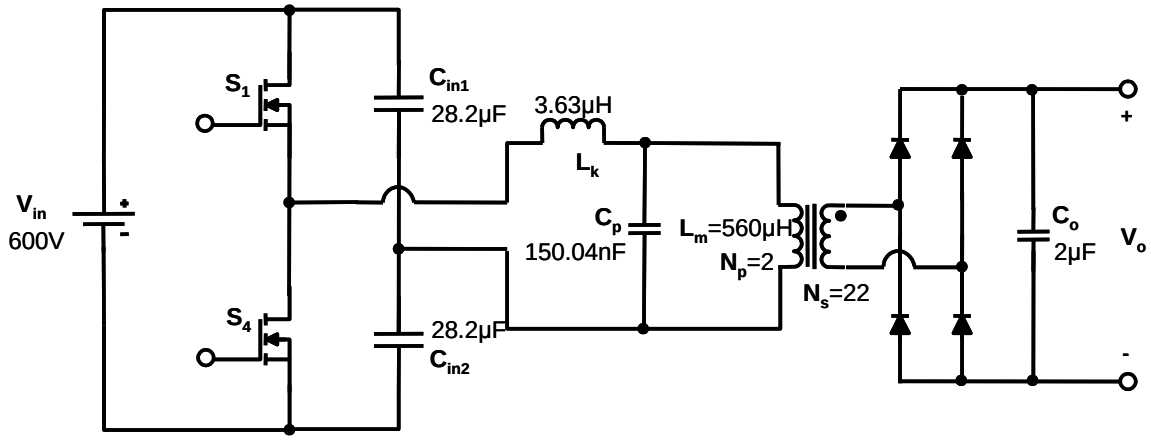


Figure B.5 – Behaviorally equivalent converter with a single secondary winding and rectifier bridge.

Assuming ideal components, the simplified circuit shown in Figure B.5 is functionally equivalent to the original from Figure B.1 in the context of controller design.

B.2 Scaling

The simplified converter in Figure B.5 is capable of delivering 30 kW and 10 kV. To further simplify prototyping, this converter was scaled down by a factor of 200 to 150 W and 50 V while preserving its resonant frequency, output current magnitudes, and relative filter capacitance using the following process.

1. The transformer turns ratio (N_s/N_p) was scaled by k_N,
2. all voltages and impedances on the primary were scaled by k_V / k_N and k_V / k_N^2, respectively, and
3. all voltages and impedances on the secondary were scaled by k_V,

where the scaling factors are defined as

$$k_V \equiv \frac{1}{200}$$
$$k_N \equiv \frac{1}{11} \tag{B.1}$$

This yielded the scaled converter shown in Figure B.6.

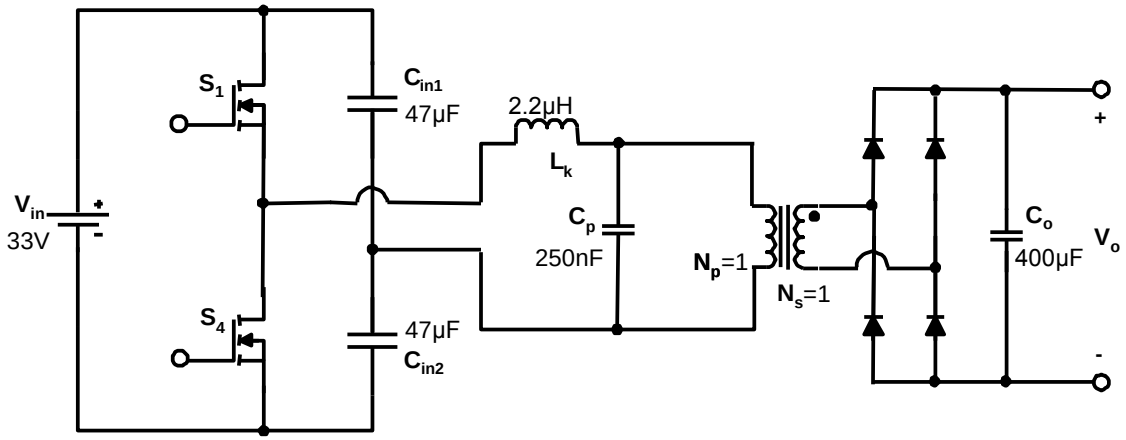
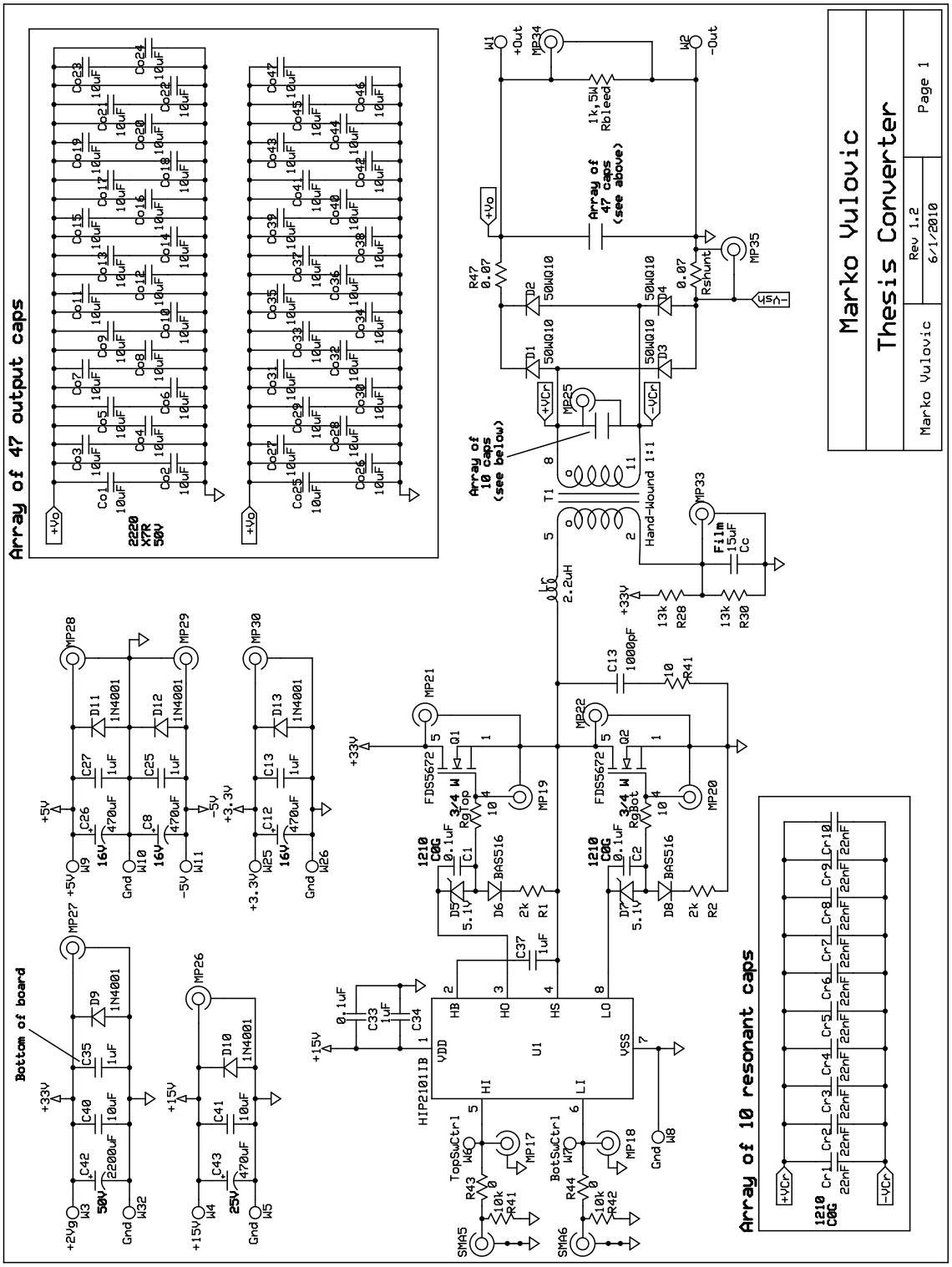
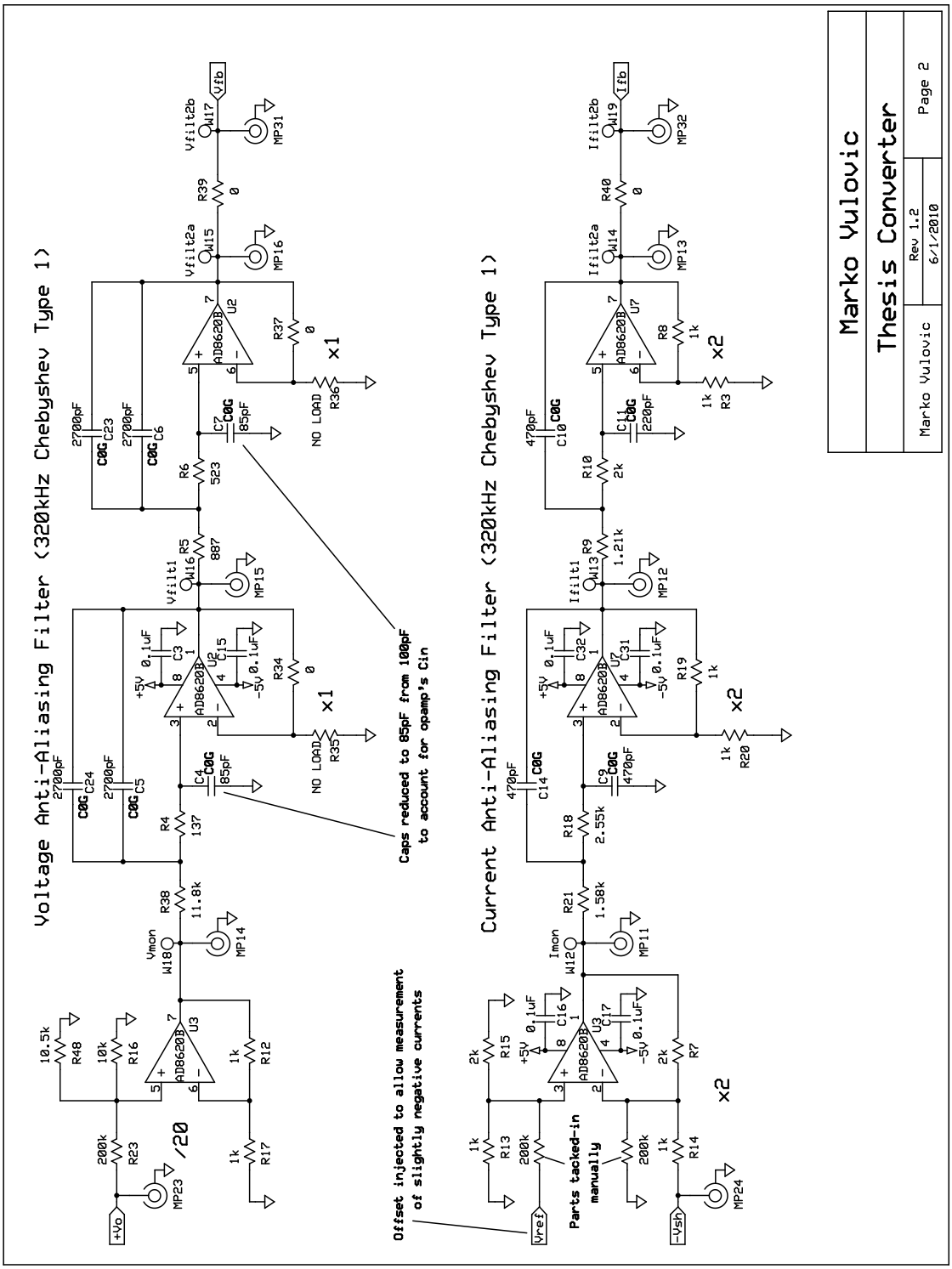


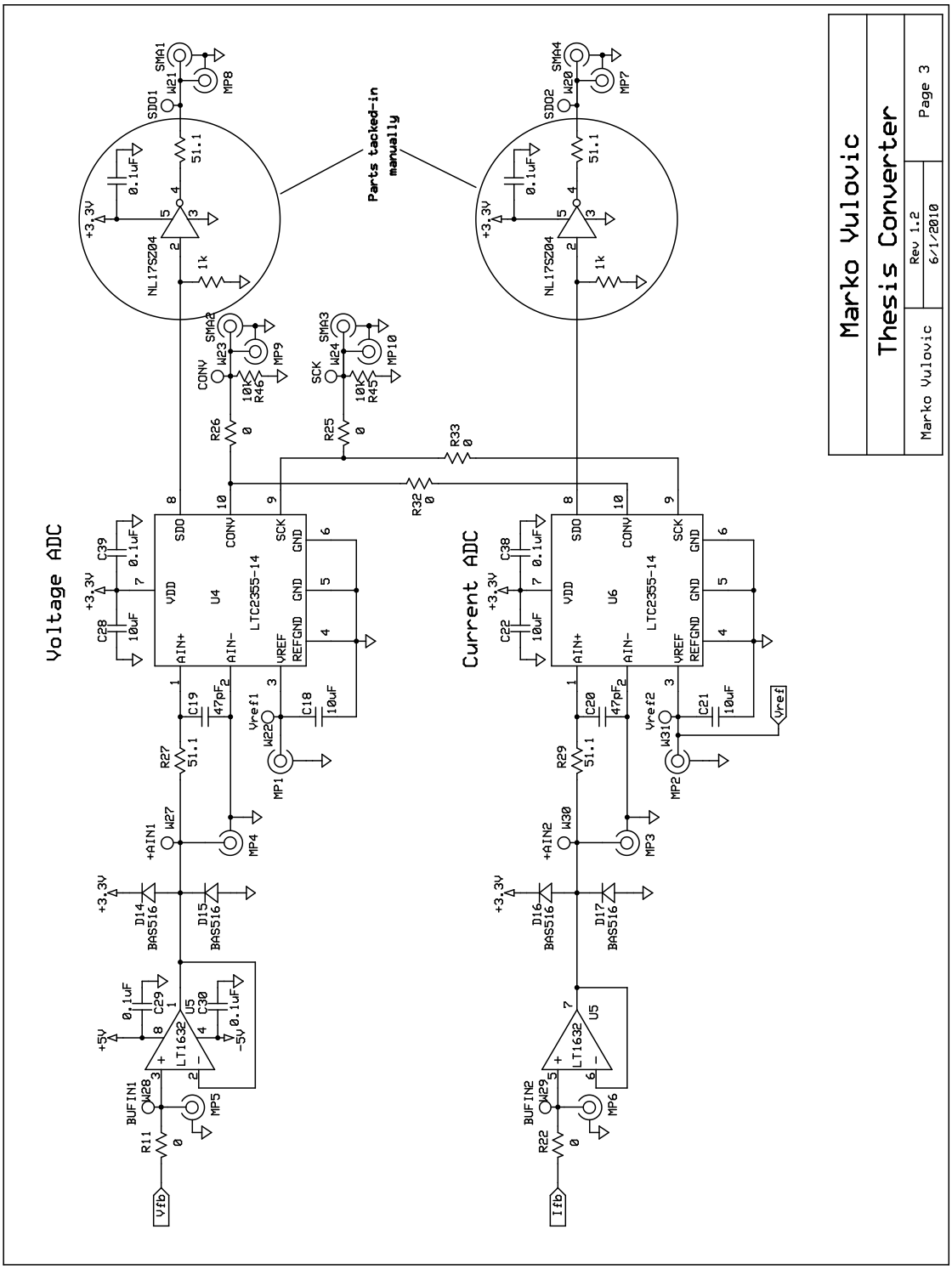
Figure B.6 – Simplified and scaled-down version of the converter shown in Figure B.1.

Appendix C: Prototype Schematic and PCB Layout

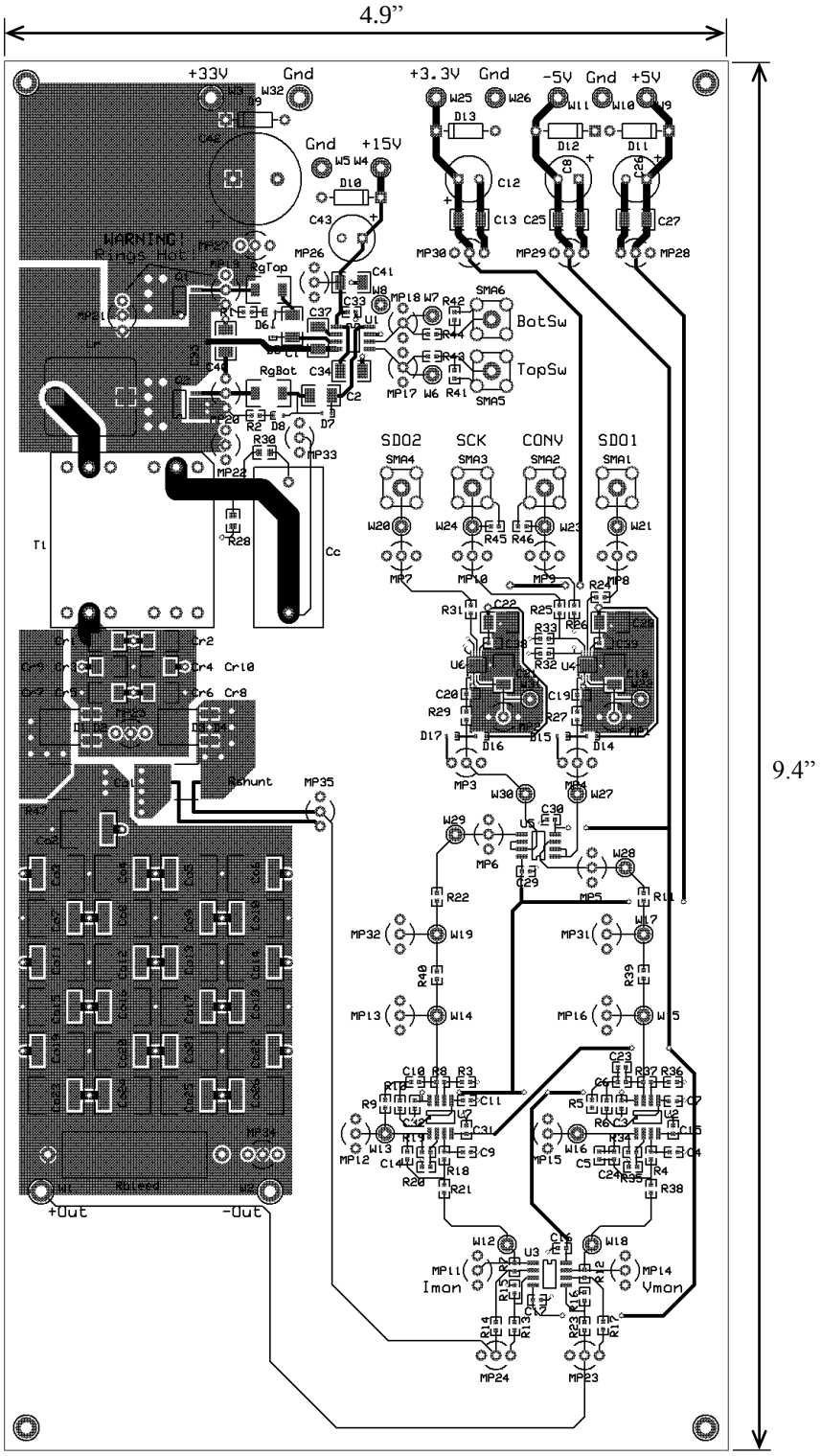
C.1 Prototype Schematic

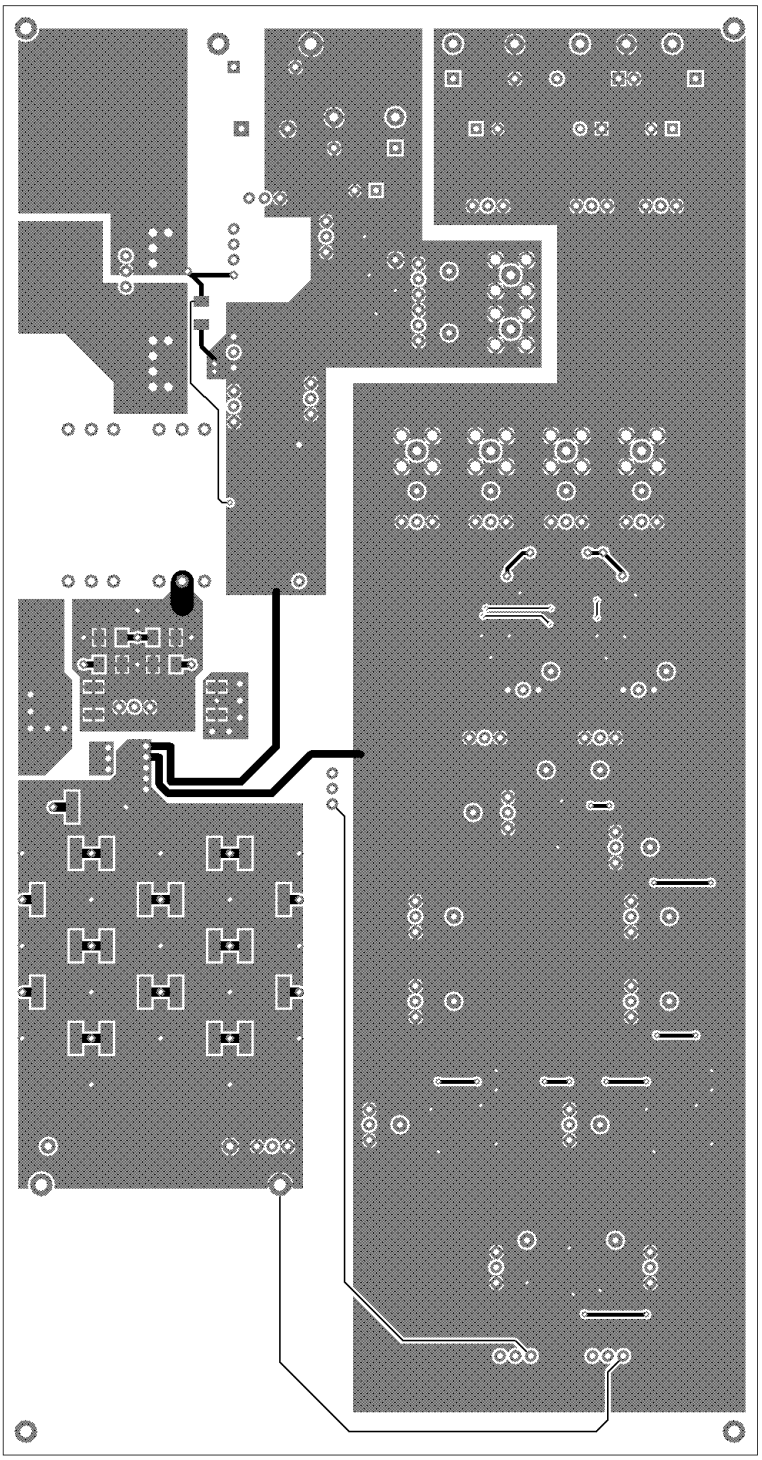



Voltage Anti-Aliasing Filter (320kHz Chebyshev Type 1)
Current Anti-Aliasing Filter (320kHz Chebyshev Type 1)
Caps reduced to 85pF from 100pF to account for opamp's Cin
Offset injected to allow measurement of slightly negative currents
Parts tacked-in manually
Marko Vulovic
Thesis Converter
Rev 1.2
6/1/2010
Page 2
Marko Vulovic

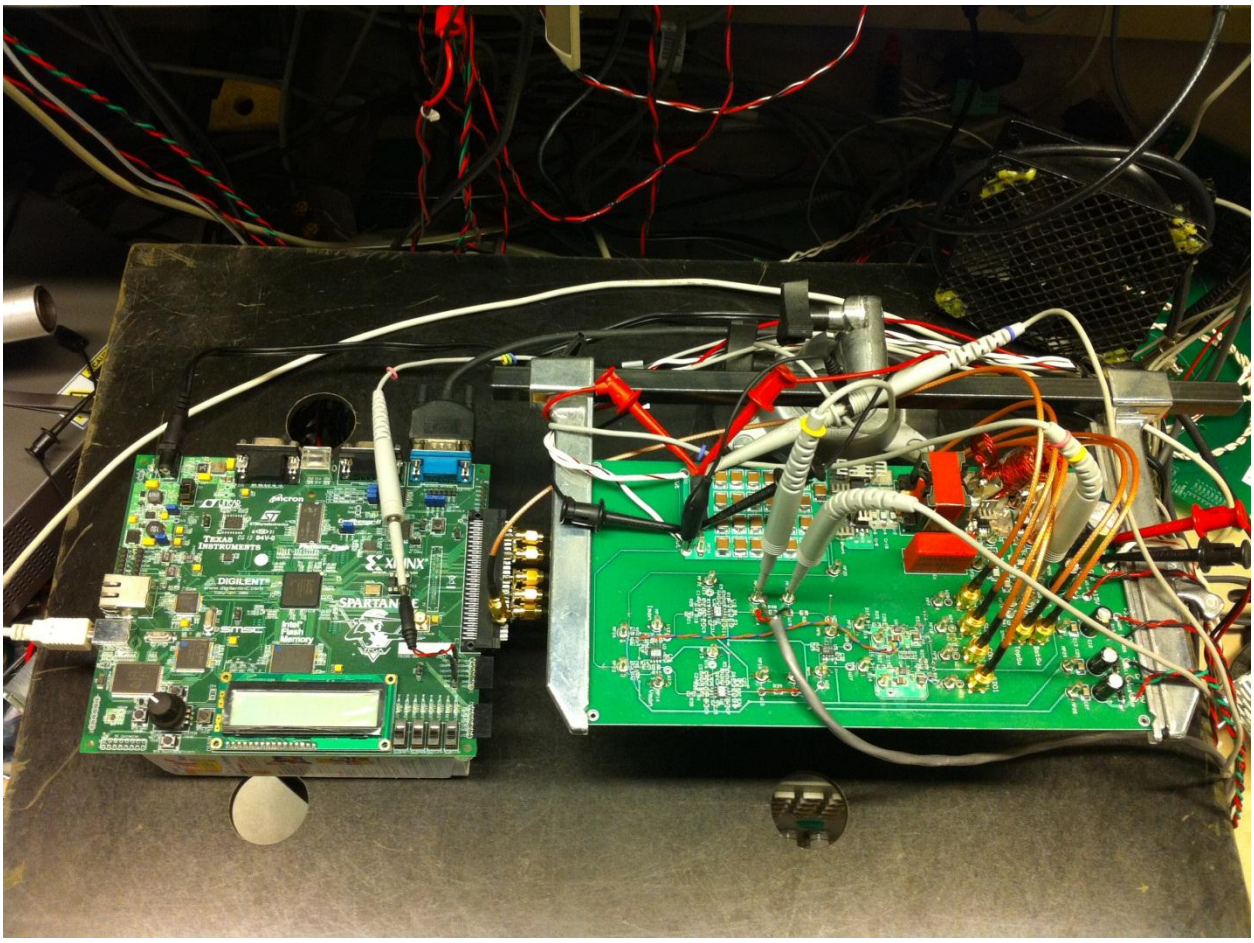

Marko Vulovic
Thesis Converter
Rev 1.2
6/1/2010
Page 3
Marko Vulovic
Parts tacked-in manually
Voltage ADC
Current ADC
LTC2355-14
LT1632
NL17SZ04
BAS516
SDO1
SDO2
CONV
SCK
Vref1
Vref2
Vref
+AIN1
+AIN2
BUFIN1
BUFIN2
Vfb
Ifb
+3.3V
+5V
-5V

C.2 Prototype Printed Circuit Board Layout



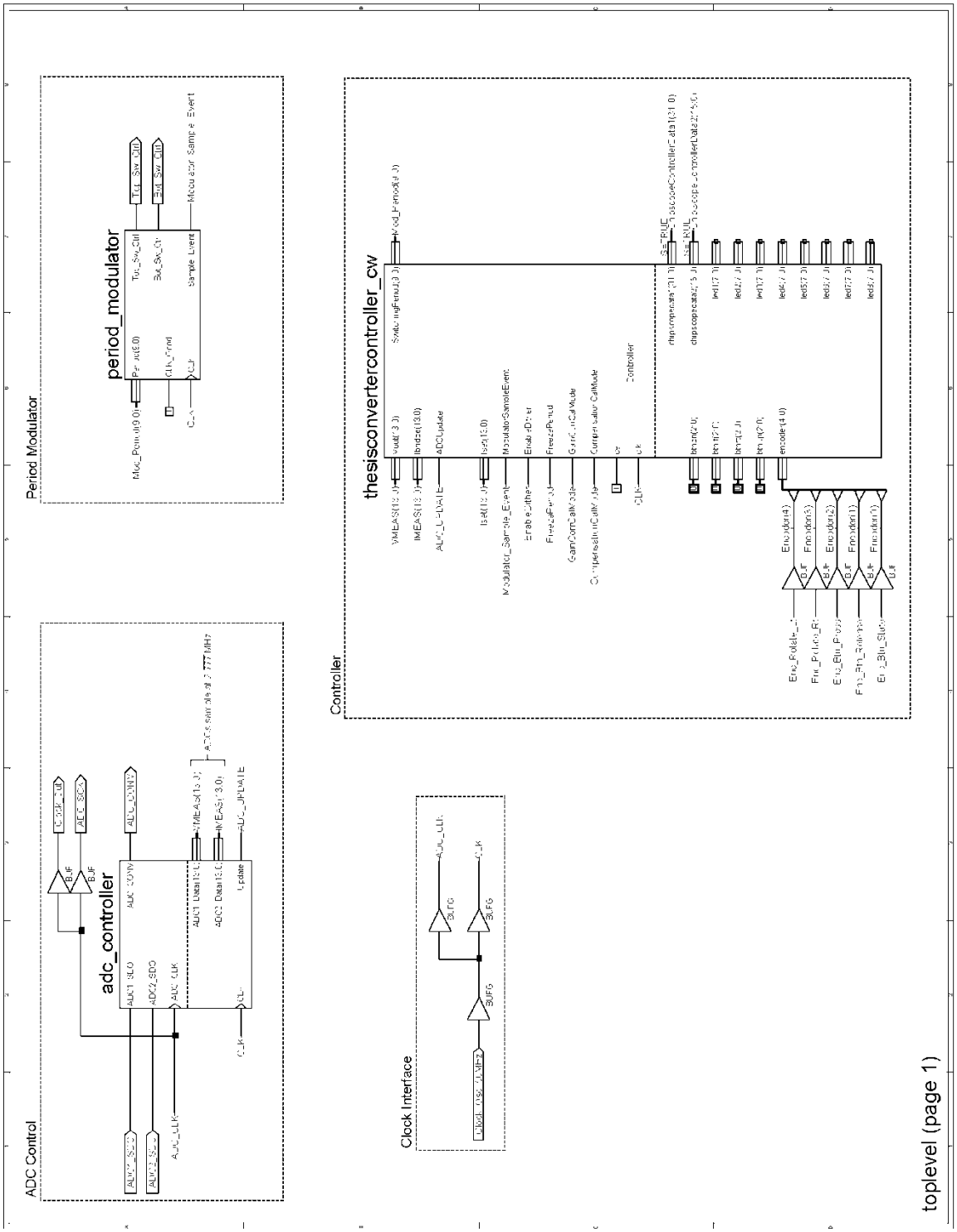


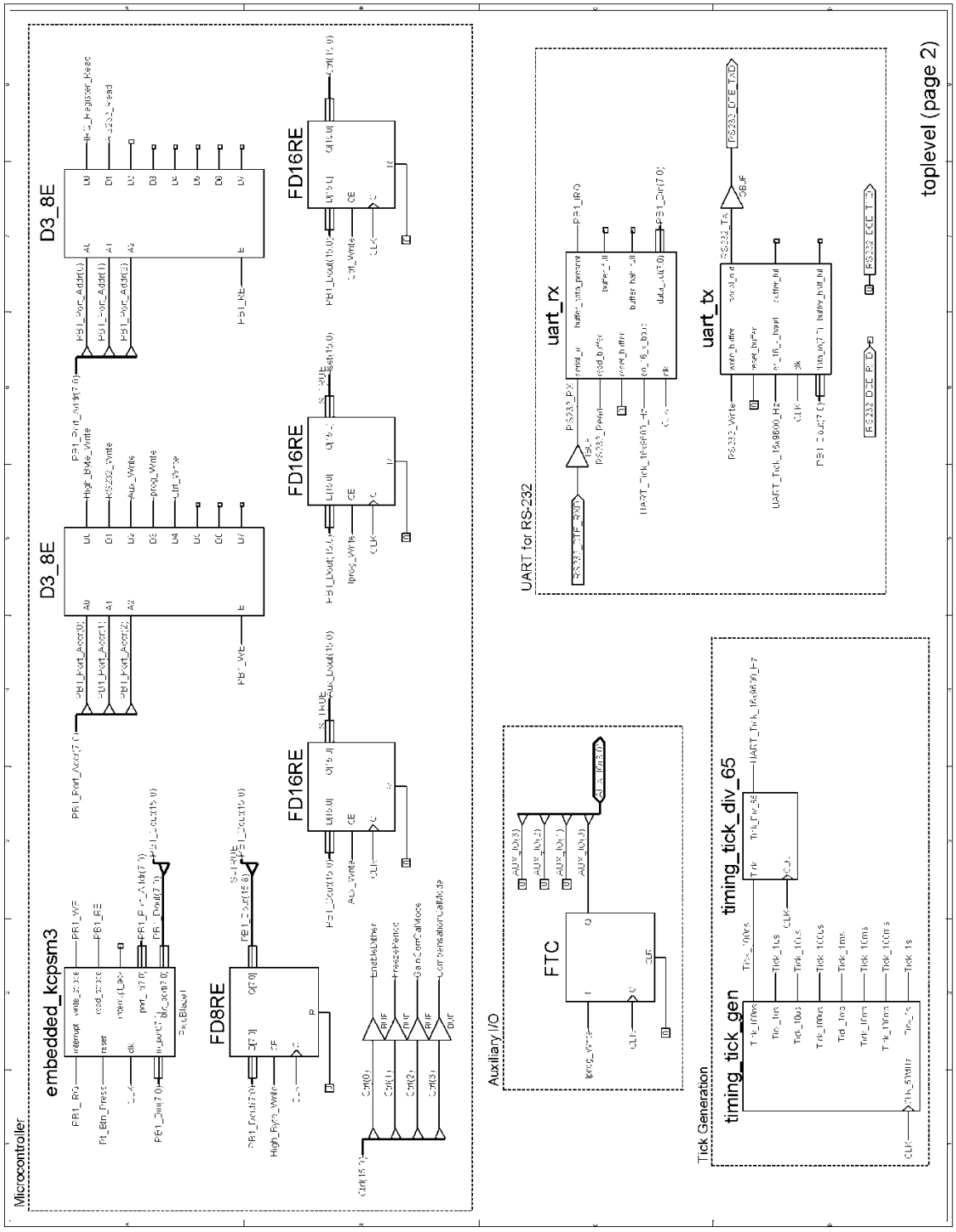
C.3 Picture of Prototype

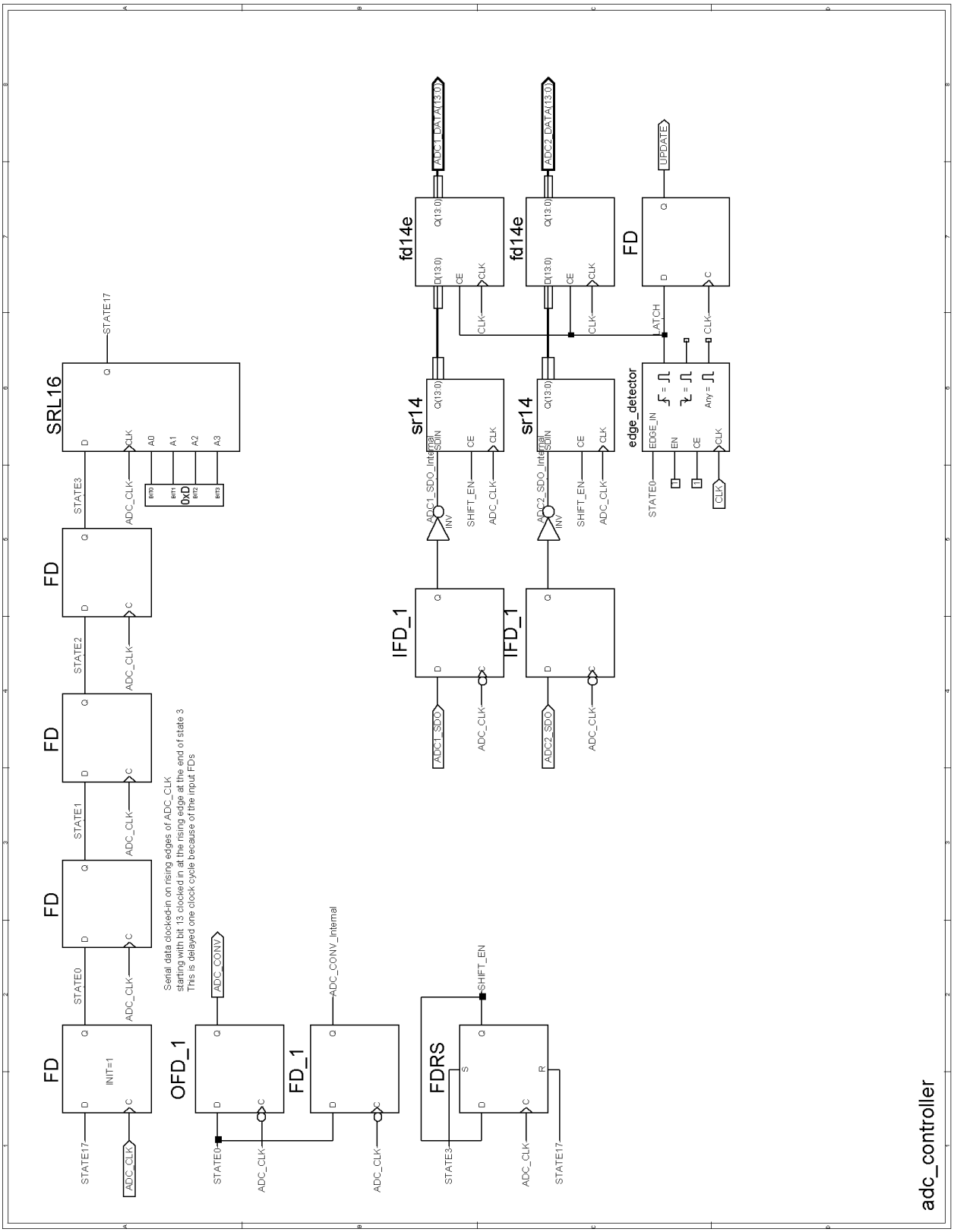


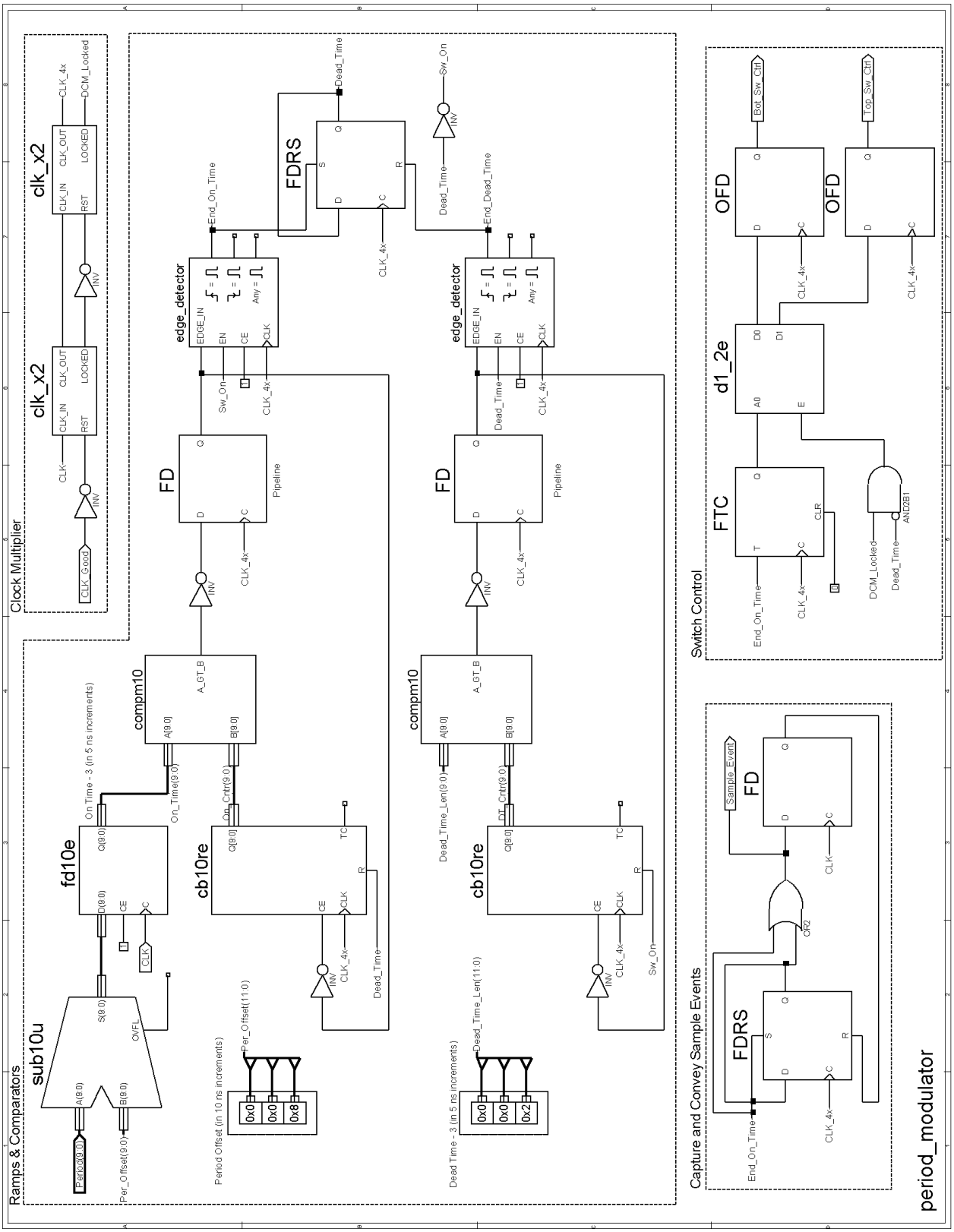
Appendix D: Prototype Controller FPGA Design

D.1 Top Level Controller Schematic

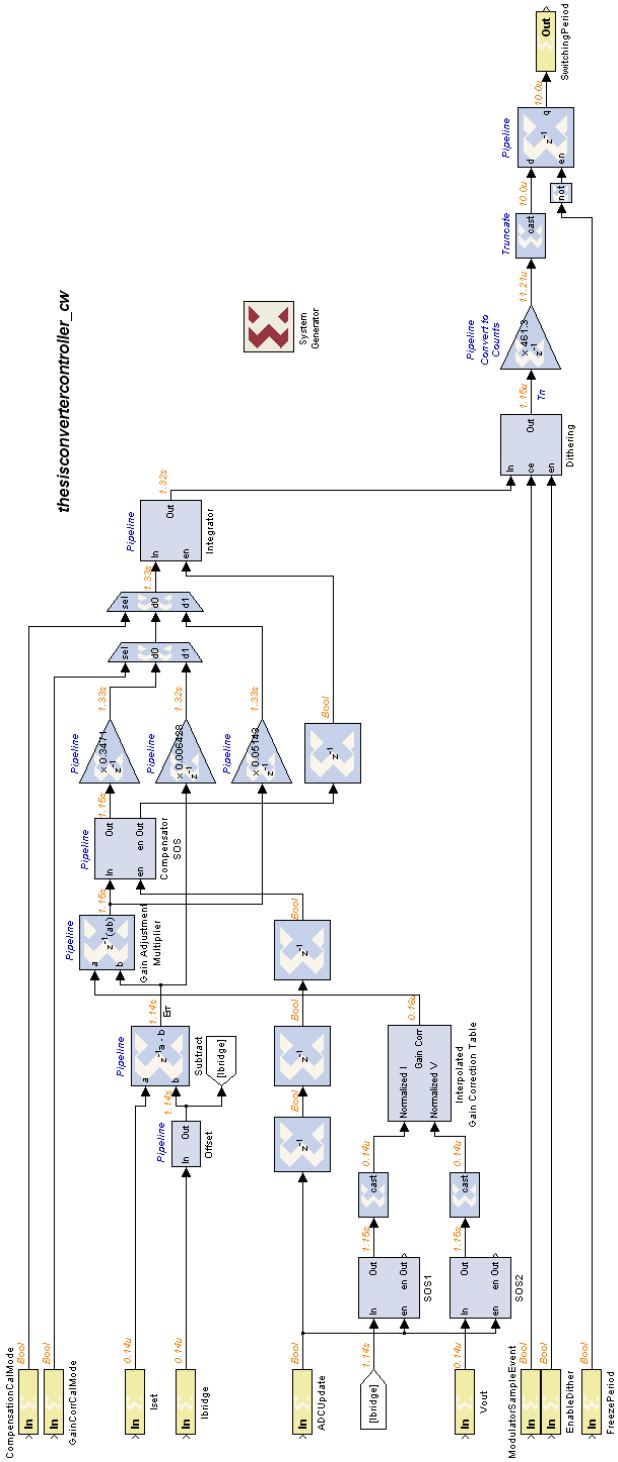


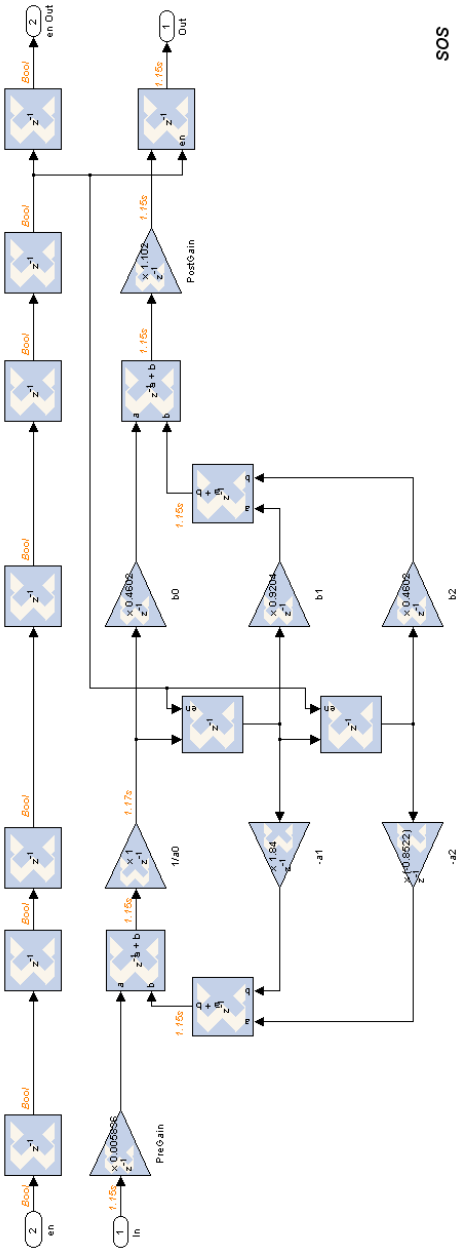

toplevel (page 2)
Microcontroller
embedded_kcpsm3
D3_8E
D3_8E
FD16RE
FD16RE
FD16RE
FD8RE
UART for RS-232
uart_rx
uart_tx
Auxiliary I/O
FTC
Tick Generation
timing_tick_gen
timing_tick_div_65

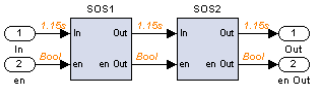

adc_controller
FD
INIT=1
STATE17
ADC_CLK
STATE0
STATE1
STATE2
STATE3
SRL16
A0
A1
A2
A3
0xD
OFD_1
ADC_CONV
FD_1
ADC_CONV_Internal
FDRS
SHIFT_EN
Serial data clocked-in on rising edges of ADC_CLK
starting with bit 13 clocked in at the rising edge at the end of state 3
This is delayed one clock cycle because of the input FDs
IFD_1
ADC1_SDO
ADC2_SDO
sr14
ADC1_SDO_Internal
ADC2_SDO_Internal
SHIFT_EN
fd14e
ADC1_DATA(13:0)
ADC2_DATA(13:0)
edge_detector
EDGE_IN
UPDATE
LATCH


Clock Multiplier
clk_x2
CLK_IN
CLK_OUT
RST
LOCKED
CLK_4x
DCM_Locked
CLK_Good
INV
Ramps & Comparators
sub10u
A(9:0)
B(9:0)
S(9:0)
OVFL
Period(9:0)
Per_Offset(9:0)
fd10e
D(9:0)
Q(9:0)
CE
C
CLK
On Time - 3 (in 5 ns increments)
On_Time(9:0)
compm10
A_GT_B
A[9:0]
B[9:0]
cb10re
On_Cntr(9:0)
Q[9:0]
TC
R
Dead_Time
Period Offset (in 10 ns increments)
Per_Offset(11:0)
0x0
0x8
edge_detector
EDGE_IN
EN
Any =
End_On_Time
Sw_On
FDRS
S
D
Q
R
Dead_Time
End_Dead_Time
FD
Pipeline
Dead_Time_Len(9:0)
DT_Cntr(9:0)
Dead_Time_Len(11:0)
0x2
Switch Control
FTC
T
CLR
d1_2e
A0
E
D0
D1
OFD
Bot_Sw_Ctrl
Top_Sw_Ctrl
DCM_Locked
ANDCB1
Capture and Convey Sample Events
Sample Event
OR2
period_modulator

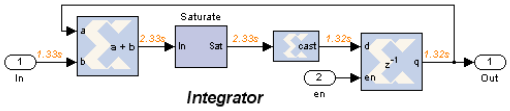
D.2 Main Controller Design (thesisconvertercontroller_cw)



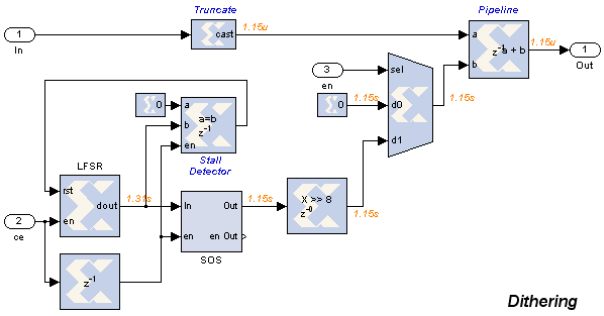

SOS
en Out
Out
PostGain
b0
b1
b2
1/a0
-a1
-a2
PreGain
en
In



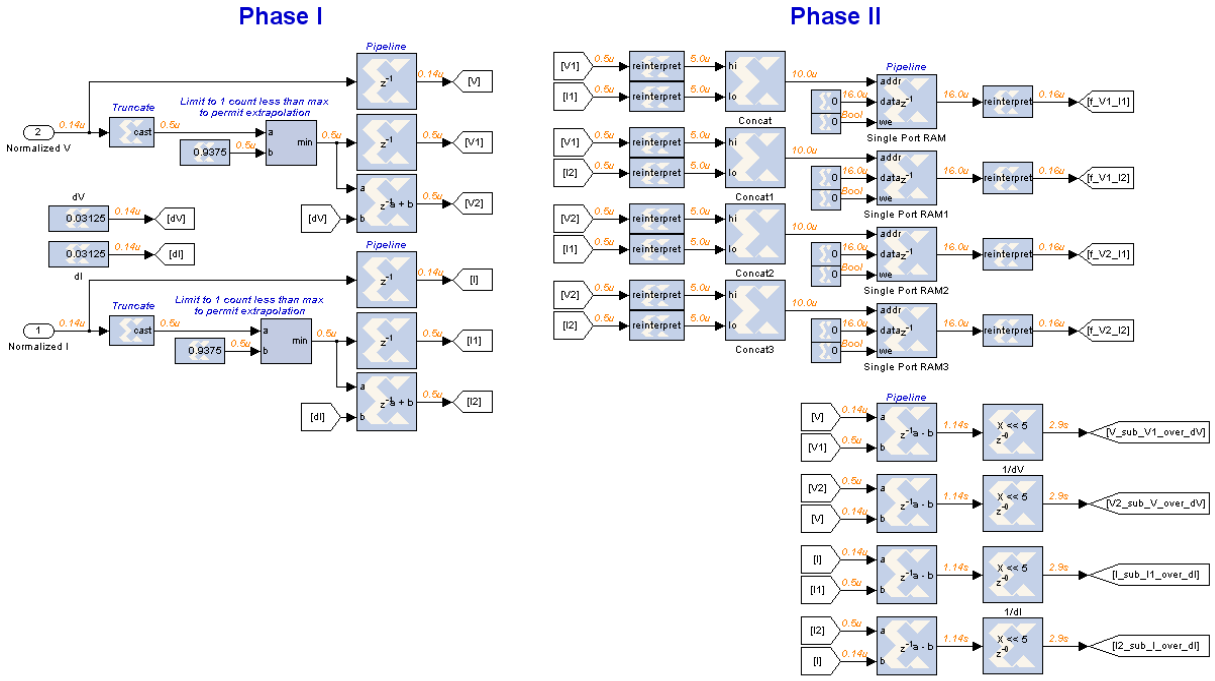
Compensator



Integrator



Dithering


Phase I
Phase II
Phase III
Phase IV
Pipeline
Truncate
Limit to 1 count less than max to permit extrapolation
Normalized V
Normalized I
dV
dI
0.03125
0.9375
[V]
[V1]
[V2]
[I]
[I1]
[I2]
Concat
Concat1
Concat2
Concat3
Single Port RAM
Single Port RAM1
Single Port RAM2
Single Port RAM3
[f_V1_I1]
[f_V1_I2]
[f_V2_I1]
[f_V2_I2]
[V_sub_V1_over_dV]
[V2_sub_V_over_dV]
[I_sub_I1_over_dI]
[I2_sub_I_over_dI]
1/dV
1/dI
Saturate
Should not be bigger than what can be represented by a 0.16 since V-V1 = 1-(V2-V)
Should not be bigger than what can be represented by a 0.16 since I-I1 = 1-(I2-I)
Gain Corr
Interpolated Gain Correction Table