Mixed-Signal IC design for Heterogeneously Integrated Multi-Analyte Chemical Sensor Arrays

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Thesis submitted to the Faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Master of Science
in
Electrical and Computer Engineering

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September 9, 2010
Blacksburg, Virginia

Keywords: Chemical Sensors, Sigma- Delta, Chemoresistive, Impedance Measurement,

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(ABSTRACT)

Wireless sensor nodes are emerging in a wide range of critical applications such as environmental monitoring, health applications, home automation and military surveillance and reconnaissance. The addition of low power wireless capability to such sensor nodes allows communication between a node and a base station or between nodes, resulting in the formation of wireless sensor networks. Sensor networks can use the information available from the distributed sensor nodes to determine the location and nature of a stimulus or environmental condition. The information collected by the base station can be used to determine the appropriate course of action for dealing with the stimulus. In chemical/biological defense or safety monitoring scenarios, wireless sensor networks can be used to identify and track harmful chemical or biological agents which might be present in a particular area. Due to the potentially remote areas that wireless sensor networks aim to cover, it is essential to minimize the power consumption of a sensor node so that it can operate over a long period of time without a connection to the power grid. Sensor nodes can contain multiple blocks, such as the readout circuit which interfaces with the sensor, an embedded processor, and the wireless transceiver circuits, all of which need to operate on a low power budget.

This thesis specifically focuses on design of low power mixed signal readout circuits which interface with chemoresistive chemical sensors, i.e. sensors that demonstrate a variation of resistance (or impedance) in the presence of chemical agents. For this thesis, the sensor can be either a chemoresistive bead or a nanowire. By integrating multiple non-specific chemoresistive sensors together in arrays, a cross-reactive array can be realized, where the combined response of the arrayed sensors can be used to determine analytes present in a mixture even if their concentrations are low.

In this thesis, a CMOS resistive readout circuit based on a sigma-delta ADC is presented. The design is used to measure the resistance of chemoresistive beads and nanowires with respect to time. The frequency of the ADC output varies as the resistance of a sensor changes and, based on the magnitude and duration of the variation, the type of chemical agent and its concentration can potentially be estimated. For future cross-reactive sensor applications, an array of 16x16 sites is also included in the readout circuit design. Individual sites in the sensor array can be accessed using addressing blocks which designed to select a particular row and column using an 8-bit addressing system. This thesis also covers the techniques used for integration of chemoresistive beads and nanowires into the array locations provided on the prefabricated CMOS IC. Measurement results that demonstrate the operation of the resistive readout circuitry are presented.

Finally, a second readout circuit is proposed to measure complex impedance variations of a sensor device. Measurement of magnitude and phase changes of a sensor device can provide another degree of freedom in the analysis of chemical mixture. Simulation results demonstrating the functionality of the proposed impedance measurement system are also presented.

This work was performed under SPAWAR SysCtr Pacific grant N66001-08-1-2046 sponsored by DARPA. Any opinions, findings, and conclusions or recommendations expressed in this publications are those of the author(s) and do not necessarily reflect the views of SPAWAR SysCtr Pacific or DARPA.

Acknowledgements

I would first like to thank my advisor, Dr. Sanjay Raman for providing me a wonderful opportunity to work in the Wireless Microsystems Lab (WML) and for his guidance, advice and motivation through this thesis. His passion for excellence in the field of electrical engineering is inspiring. I would also like to thank Dr. DaSilva and Dr. Ha for serving on my advisory committee and reviewing my thesis.

I am grateful to Dr. Amy Bell; Dr. Mayer and Dr. Mallouk of Penn State for collaborating in this work. I am also grateful to Jazz Semiconductors (now Tower Jazz) for providing me access to their IC technology and for fabricating the prototype designs.

I would like to thank my fellow Wireless Microsystem Lab members: Krishna Vummidi, Marcus Oliver and Parrish Ralston. I would also like to thank Shree, Phillip Zeller, Bassam Alfeeli and other members of the MEMS lab for their support and company. They helped long hours in the lab pass by quickly and made my graduate school experience one of the most memorable times in my life.

I would like to thank my parents, Nirmal and Reeta Kakkar for their love, support and belief in my abilities. Heartfelt thanks to my sister, Natasha for her encouragement and for always being there. I also want to thank my uncle, Vimal Kakkar, and his family for providing me a home away from home. Thanks to all my friends for their support and encouragement.

Finally, I thank the Lord for his blessings.

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Chapter 1

Introduction

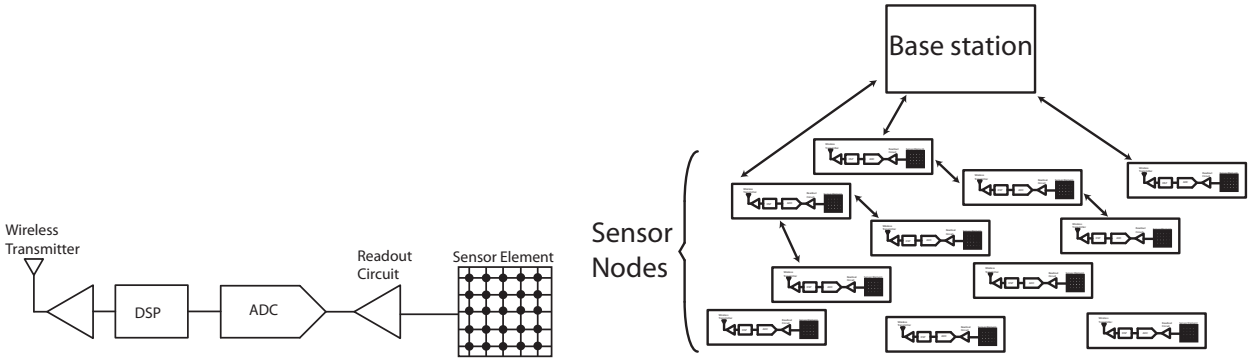
Sensors are devices which respond to changes in their environment (either physical or chemical, for example, heat, light, sound, pressure, presence of chemical compounds) and provide an output signal (typically electrical) which correlates to the stimulus to be observed. For example, a photodetector (consisting of a photodiode or a phototransistor) conducts current proportional to the illuminance of the incident light; a chemical/gas sensor demonstrates changes to its electrical properties (such as resistance or impedance) which are dependent on the type and concentration of gas/chemical it is exposed to [1]. A few basic attributes of a sensor can be listed are as follows [2, 3]:

- Sensors should be in direct contact with the stimulus to be observed.
- The output of a sensor should be sufficient to identify the cause of the stimulus and also quantify it. For example, the output of a chemical sensor should identify the analyte present as well as its concentration.
- Sensors should have low response times with high output accuracy and resolution.
- They should have as low as possible size, weight, power and cost while providing required performance

- Sensors should provide high reliability with minimal aging effects.

A typical sensor system may consist of one or more sensor element whose electrical properties vary due to the presence of a stimulus. A readout circuit can be used to monitor the changes in the electrical properties of the sensor element and generate an analog signal. The analog output of a readout circuit can be converted into a digital signal using an analog to digital converter (ADC). The digital output of a ADC can be processed using digital signal processing techniques to determine the nature of the stimulus (to identify the specific cause) and quantify it (to determine the magnitude of the stimulus). In case of silicon based sensors, it is possible to combine the sensor, readout circuitry, ADC and signal processing blocks on a single integrated circuit (IC). As the level of integration in a sensor system increases and its size decreases, the number of potential applications for sensors increases as well. Sensor systems based on integration of microelectromechanical systems (MEMS) devices with processing circuits are now practical. For example, MEMS accelerometers [4] and gyroscopes [5] have been demonstrated over the years. These integrated sensor systems benefit from the reduction of size, reduced power consumption and reduction of cost due to higher process yields.

By further integrating a communication transceiver and a microprocessor into a sensor system (Figure 1.1a), a sensor system can be used as a part of a wireless sensor network (Figure 1.1b). A wireless sensor network consists of multiple miniature low cost, low power, multifunctional sensor systems (or sensor nodes) that can communicate over short distances. The sensor nodes can use the processing ability of the microprocessor to perform simple computations and the wireless transceiver to transmit processed data to a central base station [6]. The base station can use the data received from multiple sensor nodes to determine the location of a stimulus and establish its significance. Sensor networks can be mesh based networks with multi-hop radio connectivity. Alternate networks can be either point-to-point or multipoint-to-point networks where the nodes are connected to the base station with single-hop radio connectivity. Mesh networks allow applications to have a high node count such



(a) (b)

Figure 1.1: (a) Block diagram for sensor node. (b) Infrastructure for Wireless Sensor Network.

as in environmental monitoring and national security applications, whereas point to point or multipoint to point networks support networks over a short range with a low data rate such as in RFID systems and home automation. Wireless standards such as IEEE 802.15 (for personal area networks) and ZigBee are used to provide the wireless capabilities in the sensor nodes used in applications focusing on low data rates and limited range [7, 8].

The versatile, robust and ubiquitous nature of wireless sensor networks makes them ideal candidates for use in wide range of applications such as [6]:

- *Environmental Monitoring*: Sensor networks can play a major role in flood detection [9], mapping the biodiversity of an ecosystem [10], tracking movements of animals [11] etc.

- *Health Applications*: Sensor networks can be used to collect physiological data for patients over a long period of time to observe health and to identify potentially harmful conditions [12, 13]

- *Automobile Monitoring*: Sensor networks can be used for tracking the position of traffic[14], preventing car theft [15] or even provide diagnostic information regarding

(a) (b)

Figure 1.2: (a) Mica2 wireless sensor node from Crossbow technologies (from [18]). (b) MicaZ wireless sensor node from Crossbow technologies (from [19]).

the various electrical and mechanical systems present in an automobile [16].

- *Home Automation*: Sensor networks can be used to develop smart homes which can adapt to the needs of end users. Smart homes offer the potential of self organizing, self regulated and adaptive systems which enhance energy efficiency and the quality of life for the inhabitants [17].

- *Military Applications*: Sensor networks can play an integral role in military command, control, communications, computing, intelligence, surveillance, reconnaissance and targeting systems (C4ISRT) . They can also play a major role in nuclear, biological and chemical attack detection and defense [6].

It is estimated that in 2010 more than half a billion sensor nodes will ship for wireless sensor applications, with the market worth more than $7 billion. Advanced radio frequency communication integrated circuits (RFICs) are now available for a low cost and smart sensor integrated circuits have become more commonplace [7]. Several examples of wireless sensor nodes are now available commercially. For example, Crossbow Technologies currently provides wireless sensor nodes developed as part of UC-Berkley's "Smart Dust" program (Figure 1.2).

Defense applications have fostered research and development in sensor networks during the past several decades. Programs such as DARPA Sensor Information Technology (SensIT) Program have focused on sensor networks for a battlefield environment. Similar programs have focused on development of chemical sensors which would eventually be deployed as sensor networks. Chemical sensors can play a critical part in the battlefields where the specter of chemical warfare is unfortunately becoming a renewed threat. For example, approximately a quarter of the veterans from the 1990-1991 gulf war suffer from the gulf war illness [20], which is a complex of multiple concurrent symptoms which typically include persistent memory and concentration problems, chronic headaches, gastrointestinal problems and other chronic abnormalities. One of the causes for this illness has been identified as exposure to nerve gas agents such as sarin and soman, as well as pesticides. Low power miniature chemical sensors could be very effective for operations in such environments, especially as a part of a network which will allow a quick response to such threats.

This thesis focuses on new circuit technologies for low power chemical sensor nodes. The next section provides an overview of some current research efforts in the field of chemical sensors. The final sections of this chapter provide a brief summary of the work presented in the thesis followed by an overview of the organization of the chapters.

1.1 Chemical Sensors

Chemical sensors respond to various chemicals or chemical reactions and are intended for identification and quantification of chemicals in either liquid or gaseous phases [3]. Some basic features present in chemical sensors are given below [2]:

- able to transform chemical information (composition analysis and/or concentration of specific targeted samples) into electrical signals (typically)
- miniature and cheap with low power consumption

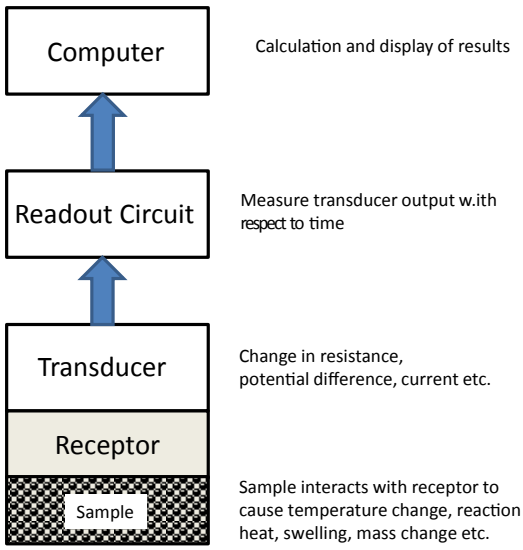


Figure 1.3: Block Diagram for typical chemical sensor system.

- rapid response and analysis time

As with other sensor systems, chemical sensors consist of a chemical or molecular recognition system (or the receptor) and the physiochemical transducer (Figure 1.3). The receptor can consist of a thin layer of a chemically or molecularly sensitive component which is deposited on top of a substrate. This layer interacts with the analyte molecules and, as a result, the properties of the receptor layer change. The receptor layer can be designed to be selective in its response so that its properties change for particular analytes or for a mixture of analytes. The main processes for interaction between the receptor and the analytes are adsorption, ion exchange or liquid-liquid extraction. These processes occur at the interface between the analyte and receptor layer where both are at a state of equilibrium. It is also possible for the receptor layer itself to act as the transducer — for example, metal oxide semiconductor gas sensors which change their conductivity in presence of gases [2].

Chemical sensors can be classified based on the nature of their output signal as follows:

- **Direct chemical sensors** demonstrate variation in a measurable electrical characteristic such as resistance, potential, current or capacitance upon exposure to stimulants.

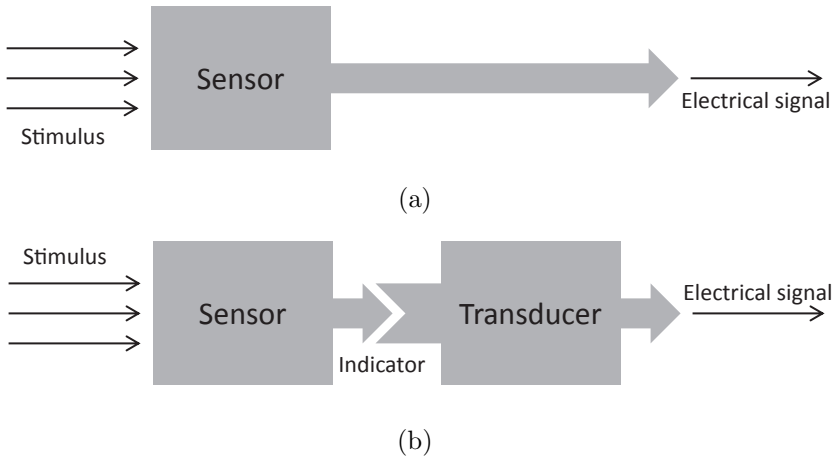


Figure 1.4: (a) Direct Chemical Sensors. (b) Indirect Chemical Sensors.

They require some electrical signal conditioning but no transducing. A block diagram for direct sensors can be seen in Figure 1.4a.

- **Indirect chemical sensors** demonstrate variation in non-electrical signals in presence of stimulants. Examples of non-electrical signal could be change in physical shape, frequency shift, modulation or emission of light, temperature change or mass change. A subsequent transducer is required to convert these non electrical signals and interface with processing circuitry. A block diagram for indirect sensors can be seen in Figure 1.4b.

Alternatively, chemical sensors can be classified based on the interaction between the sensing layer and the analyte.

- **Chemically active sensors** require a chemical reaction between the sensing element and the analyte which causes a measurable change in the output signal (electrical or non-electrical) of the sensor.

- **Physically active sensors** depend on a physical response of the sensing element and the analyte to indicate the presence of chemical species.

Recent research work presented in literature has demonstrated numerous chemical sensor technologies such as surface acoustic wave (SAW) sensors, MEMS cantilever based sensors, optical sensors, nanotube based sensors and chemoresistors to name a few. Table 1 demonstrates the overlap between the two classification methods and provides relevant examples. More information regarding the various sensor technologies will be provided in the following sections.

Table 1: Examples of various chemical sensor technologies

	Direct Sensors	**Indirect Sensors**
Chemically Active	***Metal oxide sensors*** - The conductivity/resistance of these sensors changes in the presence of gases such as volatile organic compounds and other reducible gases.	***Pellistor sensor*** - The analyte reacts with the sensor layer to undergo a catalytic reaction which produces heat. The temperature change is measured by a resistive temperature detector [3, 21]
Physically Active	***Polymer Conductive Composites*** - Polymer films coated with chemically sensitive layers which adsorb analytes causing them to swell and change their resistance.	***Fiberoptic sensors*** - These are based on the principle that in presence of gas analytes, the optical properties of the sensors (fluorescence, absorbance etc) change. Photodetectors are used to observe the reflected light from a sensor to determine the change.

The following sections provide a brief overview regarding these and other different technologies used to develop chemical sensors.

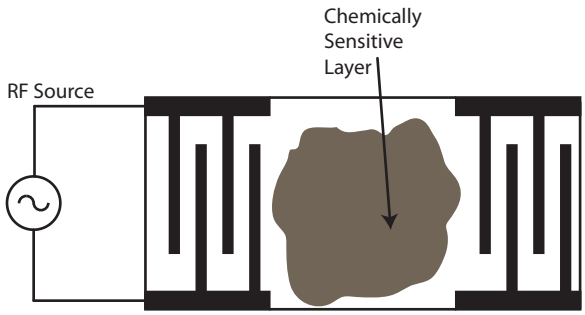


Figure 1.5: SAW sensors.

1.1.1 SAW chemical sensors

Sensors based on Surface acoustic wave phenomenon have been demonstrated in [22, 23]. The sensor consists of two thin film interdigitated structures separated by a distance on the surface of a piezoelectric crystal. The surface of the piezoelectric material between the two electrodes is covered with a chemically sensitive film. Applying an AC voltage at one of the electrodes (transmitter) results in mechanical wave oscillations which propagate along the surface of the piezoelectric crystal. The oscillations result in generation of an AC voltage at the second pair of electrodes (receiver) through the piezoelectric effect. The resonant frequency of the structure is dependent on the distance between the two sets of electrodes as well as the speed of the propagating acoustic wave. When a gas passes over the chemically sensitive layer, the molecules are absorbed on its surface which causes tiny mass changes on the film. The mass changes result in variation of the propagation velocity and consequently of the resonant frequency which can be measured by additional circuitry [2].

SAW sensors fall in the category of physically active and indirect chemical sensors [3]. Integration of SAW sensors into standard CMOS processes has proved to be a major hurdle in their commercial availability for chemical sensing applications.

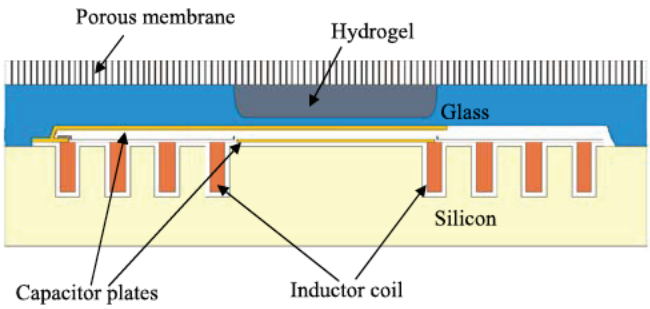


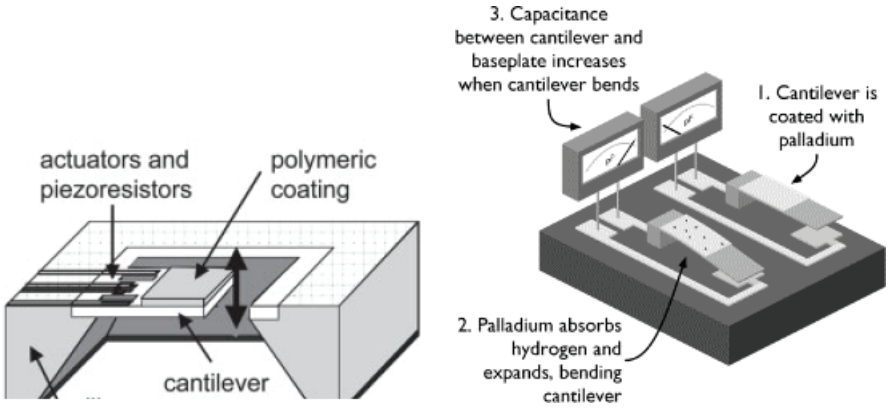
Figure 1.6: Hydrogel based chemical sensors (from [24]).

1.1.2 LC Tank resonance sensors

Similar to SAW sensors, the shift in resonant frequency of an inductor-capacitor (or LC) tank circuit can be used to identify analytes. A chemically sensitive structure (such as a hydrogel), which behaves as a variable capacitor, is coupled to an inductor to form the LC tank circuit such that the resonant frequency responds to the presence or absence of analytes [24]. Figure 1.6 demonstrates the cross section of such a sensor.

1.1.3 MEMS Chemical Sensors

MEMS structures such as cantilevers or membranes can be used for chemical sensing based on their mechanical properties, such as mass changes in a sensing layer. For example, the surface of a cantilever (Figure 1.7) can be coated with a particular sensing layer depending on analytes of interest. For sensing hydrogen, cantilevers can be coated with palladium. In presence of analytes, the response of the MEMS sensor can be detected based on any stress changes, mass loading or variations in resonant frequency observed in the MEMS structure [25].



(a) (b)

Figure 1.7: (a) MEMS cantilever based chemical sensors (from [26]). (b) MEMS chemical sensor based on capacitor measurement (from [27]).

1.1.4 Optical Chemical Sensors

Optical chemical sensors employ sensing layers which respond to analytes by demonstrating changes in optical fluorescence, absorbance, wavelength, reflectance, etc [3]. For example, bundles of optical fibers can be functionalized at one end of the fiber with chemically sensitive material whose optical properties change in presence of target compound. Ends of fibers have been functionalized with an adsorptive coating as seen in Figure 1.8a, or by placing porous functionalized silica microspheres at the fiber tips (Figure 1.8b). Excitation light is directed into the fiber towards the functionalized ends which are exposed to the chemical sample. The fluorescence of the sensors is isotropically emitted [1] and is transmitted back through the fiber where it is detected using conventional detectors such as charge coupled devices or CMOS cameras. Such systems have been demonstrated to detect several volatile organic compounds [28].

An alternate design used for detection of CO_2 is provided in Figure 1.8c. The design consists of two chambers which are illuminated by a common LED source. The chambers have

[1] Isotropic emissions have same optical properties in all directions

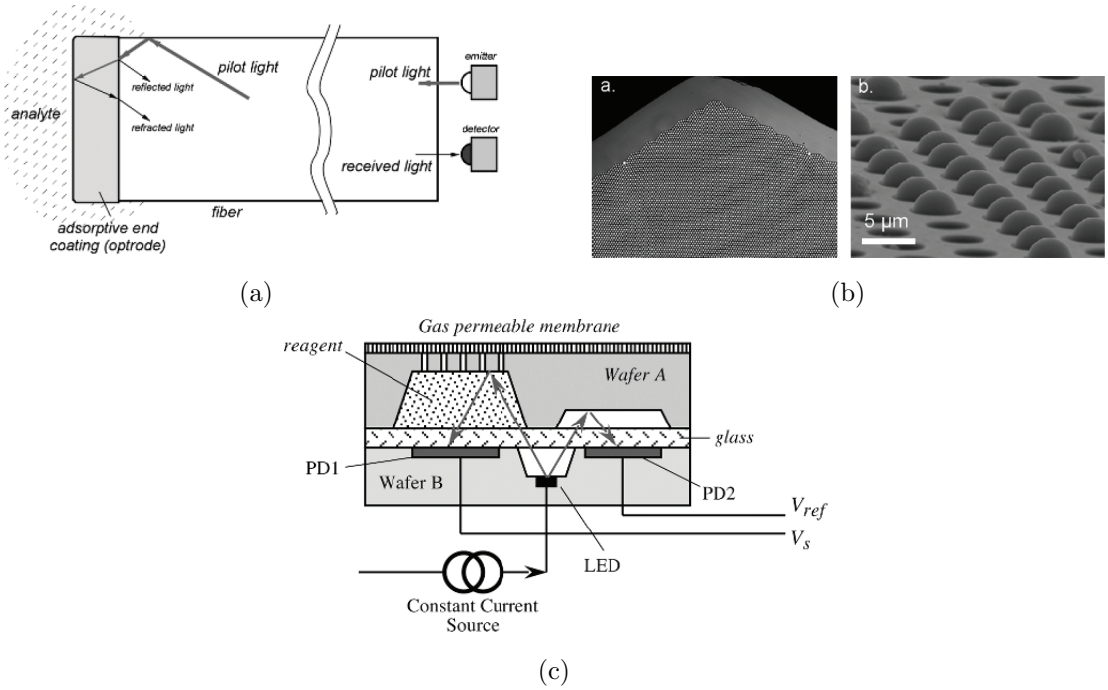


Figure 1.8: (a)Optical sensor design for optical fiber coated on one end by functionalized chemicals (from [3]). (b) Optical sensors using functionalized microspheres at tips of fibers [28]. (c) CO_2 sensor presented in [3].

metalized surfaces to ensure internal reflection. One of the chambers has a gas-permeable membrane which allows CO_2 to diffuse into the chamber. The second chamber is used as a reference measurement. Optical waveguides are placed in the chamber to measure the intensity of the internally reflected light. The chamber used for measuring CO_2 concentration is filled with a reagent whose pH changes due to presence of CO_2 in the chamber. Thus, by monitoring the intensity of the reflected light in both chambers, the concentration of the CO_2 can be determined.

The main drawback for such systems is that they are difficult to miniaturize and typically do not have low power consumption as required in wireless sensor nodes.

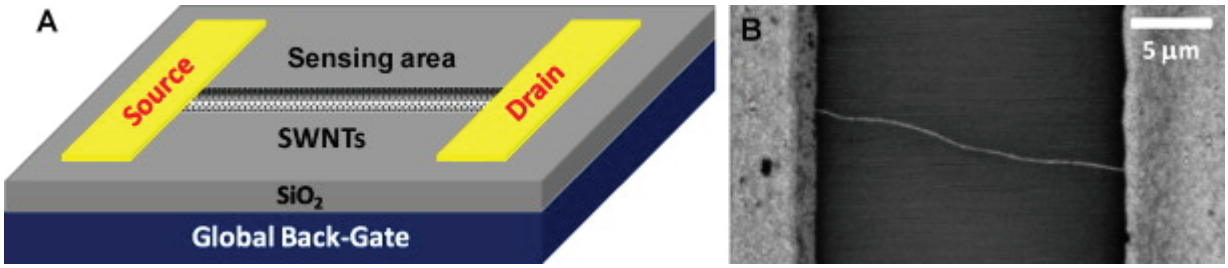


Figure 1.9: Nanotube Field Effect Transistor (from [29]).

1.1.5 Nanotube Chemical Sensors

Researchers have also demonstrated chemical sensors based on carbon nanotubes (CNT). As these nanotubes have a large surface-to-volume ratio, they can provide superior sensitivity to surface chemical processes [30]. CNT chemical sensors can be based on variations in electronic properties of pure nanotubes upon gas adsorption. Alternatively, it is also possible to functionalize CNT tips and/or sidewalls with metals or molecular groups to serve as sensing elements. Pure single wall CNTs (SWCNTs) or multi-wall CNTs(MWCNTs) can be used to detect oxygen, toxic gas molecules, ammonia, nitrogen dioxide, sulphur dioxide, nitrous oxide and other other gases. For example, the presence of these gases can be monitored by measuring the change in conductance of the nanotubes [31]. While CNTs demonstrate responses to several gases, they typically lack selectivity for a particular target gas [32]. Selectivity and sensitivity of CNTs can be improved by using different metallic particles to functionalize the CNT walls [31].

Semiconducting nanotubes can also be used to fabricate FET devices as see in Figure 1.9. The gate electrode is capacitively coupled to the nanotube through a thin dielectric and the source and drain electrodes are used to source and collect the current flowing through the nanotube. Due to interactions between the analyte molecules and surface of the carbon nanotubes, charge transfer might take place between the molecules and carbon nanotubes. As a result, the the threshold voltage of the FET device can become more negative (in case of electron-donating analytes) or become more positive (in case of electron-withdrawing an-

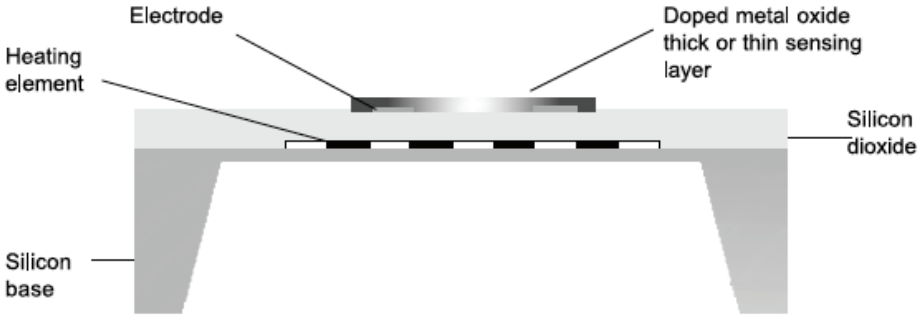


Figure 1.10: Metal oxide sensors with integrated heater (from [33]).

alytes) [29]. The variation in threshold voltage due the presence of analytes changes the current flowing through the FET and can be used to identify the analyte and its concentration.

A drawback for nanotube based sensors is that, in a number of cases, the sensing mechanism is not very well understood [29]. This, combined with the problem of integrating carbon nanotubes into standard CMOS process flows, has limited such sensors from being widely used.

1.1.6 Metal Oxide Chemical Sensors

The conductivity of metal-oxide sensors (such as tin-dioxide SnO_2) changes in presence of gaseous species which can donate electrons (for example, hydrogen) or accept electrons (for example, nitrogen oxide). When these gaseous species pass over a heated metal-oxide surface, they are adsorbed at the surface and form surface states leading to electron exchange with the semiconductor material (Figure 1.10). Gases whose molecules accept electrons extract them from the semiconductor metal-oxide and decrease the conductivity of the metal-oxide. In case of electron donating molecules, the conductivity increases [34]. The gases and their concentrations can be differentiated based on the characteristics of voltage vs. gas concentration response or the rate of change of conductivity [3]. The operating temperature

required by these devices requires a heating structure to be present in order for them to be integrated into an commercial circuit [35]. The elevated operating temperature, slow response times and drifts in the bulk conductivity present major drawbacks for these devices.

1.2 Cross reactive Arrays and "Electronic Nose" based chemical sensors

The sensor approaches discussed to this point are based on a "lock and key" approach in which the sensor layer responds selectively to certain analytes. This approach is very effective to detect the presence of specific analytes in the presence of interfering components. On the other hand, cross reactive sensor arrays provide an alternative to the conventional sensor systems and are also known as "electronic nose" sensors as they are inspired by the olfactory systems observed in nature. A cross reactive array uses an array of different sensors such that each element of the sensor array responds to a variety of chemicals. The sensors should provide a wide diversity in terms of chemical sensitivity to ensure that the array responds to the largest possible cross section of analytes. Cross reactive arrays use the non-specific response of sensors in the array to an analyte to obtain a fingerprint which is used to classify and identify the analyte (Figure 1.11). In case the background is unknown or if the background is constantly varying, multiple sensors prevent ambiguity in interpreting the output signal pattern. Multiple sensors allow the system to have redundancy by omitting any poorly performing sensors, which can also increase the signal-to-noise ratio [36].

Cross reactive arrays for odor detection were presented in literature as early as 1954 however, chemical sensor arrays were first demonstrated by Persaud and Dodd in 1982 using (SnO_2) sensors. Electronic nose systems usually consist of the following basic elements: an "odor" sensor array, a data processor and a pattern recognition system [30]. Signal processing algorithms and pattern recognition techniques play a major role in determining the sensitivity of cross reactive arrays or electronic nose systems [33]. Signal processing algorithms can be

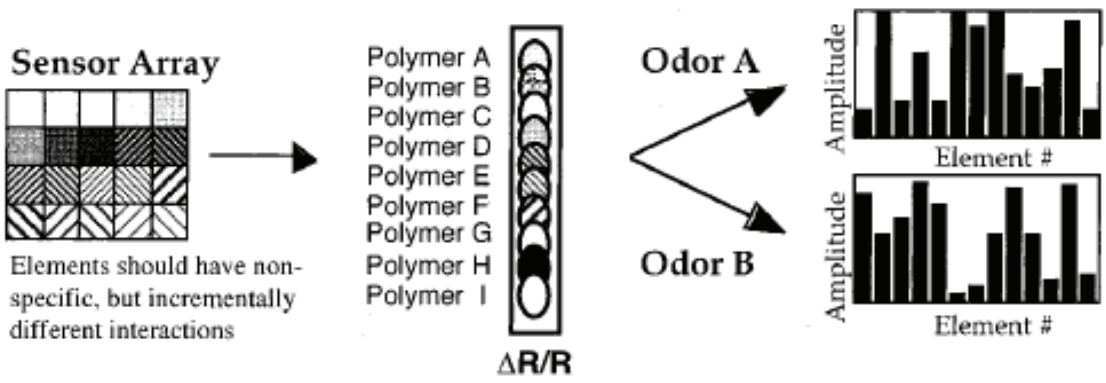
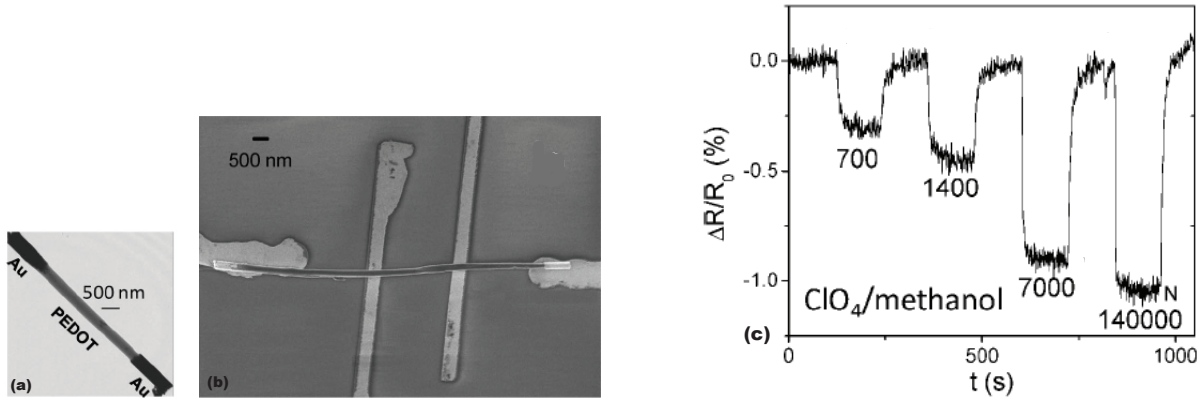


Figure 1.11: Cross reactive sensor arrays (from [36]).

based on statistically based chemometric methods, pattern recognition algorithms, neural networks or a combination of these systems. Such algorithms can allow cross reactive array based sensors to identify any previously unknown analytes based on their toxicity or virulence. However, this can increase the computational power required to identify an analyte in the presence of environmental and process variations as well as interfering signals. Increasing computational power can lead to an increase in overall system power consumption, which presents a hurdle in the widespread deployment of these sensors.

Sensor arrays for electronic nose systems using functionalized carbon nanotubes [37] and nanowires [38] as active elements have been demonstrated. Other examples for such systems include, SAW based arrays, optical arrays, metal-oxide arrays, etc. [30],[33]. Since cross reactive arrays require the presence of multiple chemical sensors, the size of the sensing elements becomes very critical in such applications. In this thesis, arrays of microscopic beads and nanowires coated with a chemoresistive layers are considered. Conducting polymer nanowires can play an important role in sensing applications because of large surface area available to the sensing layer as well as the high aspect ratio.

[39] provides a detailed discussion of sensing mechanisms and charge transport behavior of and PEDOT/ClO_4 nanowires, consisting of two metalized gold ends and a conducting



(a) (b) (c)

Figure 1.12: (a) PEDOT Nanowire, (b) Assembly setup (c) Measurement results (from [39]).

polymer central region (PEDOT [1]/PSS [2] or PEDOT/Perchlorate (ClO_4)) (Figure 1.12a). Upon integrating the nanowires with a four-point resistance measurement circuit (Figure 1.12b) and exposing them to chemical vapors, the response can be measured as a function of time as seen in Figure 1.12c. The base resistance of nanowire chemical sensors has been reported to vary from 10kΩ to 10MΩ. Since the change in resistance ΔR tends to be directly proportional to the base resistance, it is essential to ensure a wide measurement range for the readout circuit [40].

It is also possible to develop microbeads coated with conducting polymers similar to the nanowires discussed previously. As demonstrated in [41] it is possible to fabricate silica/polymer or metal oxide beads of precise dimensions and coat them with conducting polymers using methods presented in [42]. The potential for fluidic assembly of microbeads into pre-patterned arrays (discussed in Chapter 4) can lead to direct integration with the standard CMOS process flow, in contrast to the extra post-processing steps required for nanowire integration.

[1]PEDOT - poly-3,4-ethylenedioxythiophene

[2]PSS - polystyrenesulfonate

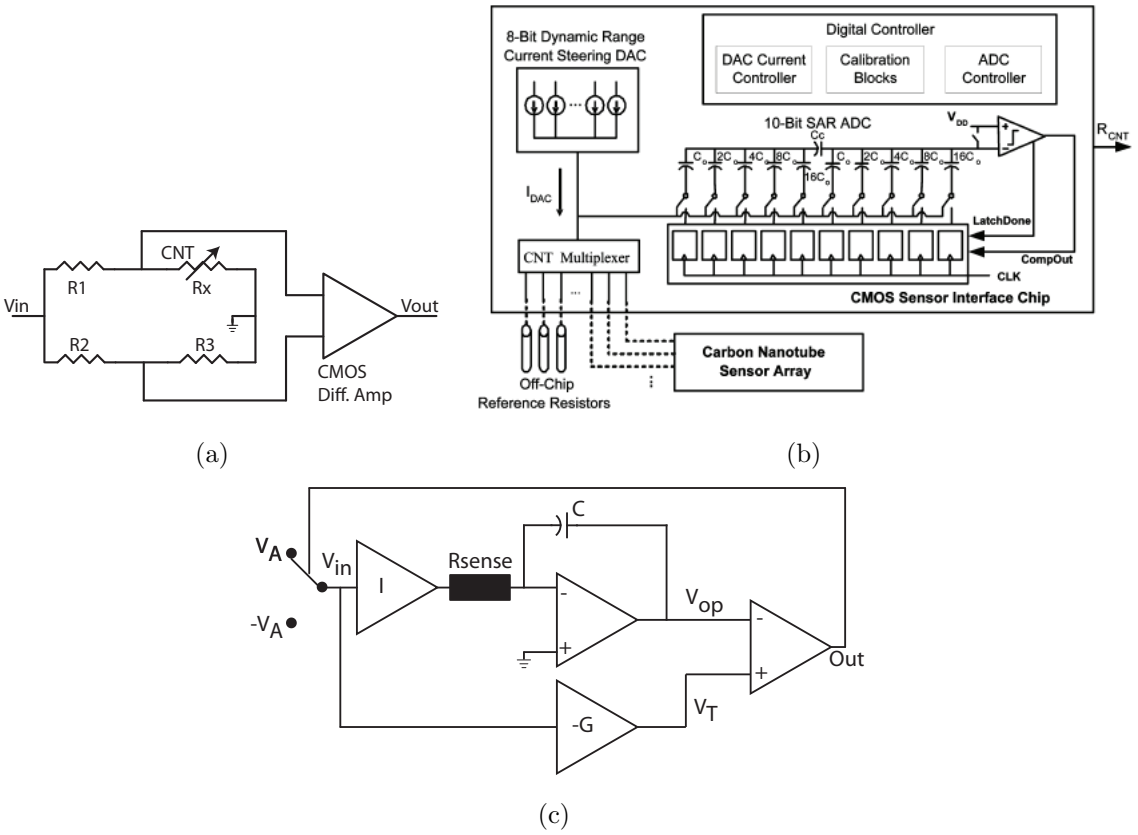


Figure 1.13: (a) Wheatstone bridge based readout circuit (from [43]), (b) Current source based readout circuit (from [44]), (c) Resistance-to-period converter based readout circuit (from [45]).

1.3 Readout circuits for resistive sensors

Readout circuits are required to detect the changes in properties of the sensors in presence of analytes. In case of sensors such as metal-oxide sensors, carbon-nanotube sensors or any other sensor which demonstrates a variation of resistance due to the presence of chemical agents, examples of resistance readout circuits are provided in [43, 44, 45].

In [43], a Wheatstone bridge consisting of three known resistance values and a two stage CMOS differential output amplifier is used to measure the resistance of a carbon nanotube (Figure 1.13a). The output of the resistance bridge is amplified to a measurable value using

the CMOS differential amplifier. The circuit presented can measure resistance values over a range of a few milliohms to 500 Ω.

Resistance of a sensor can also be determined by measuring the voltage drop across the sensor when a known amount of current flows through the sensor as demonstrated in [44] (Figure 1.13b). The voltage drop across the sensor can be converted into a digital value using a successive approximation register (SAR) or other types of ADC. In [44] a variable current source is implemented using a current steering DAC (digital to analog converter). The current source is controlled digitally to provide a range of discrete current values (100nA to 25.6μA) to the sensor resistance which in turn allows a wide range of resistance values to be measured. The main advantage of this design is that the resolution of the measurement can be controlled by changing the current flowing through the sensor since,

$$R_{LSB} = \frac{V_{LSB}}{I_{INPUT}} \tag{1.1}$$

For a particular sensor resistance, as the current is increased the voltage drop across the sensor resistance increases as well. For low sensor resistances, the accuracy of the ADC output can be increased by changing the voltage drop across the resistor so that any resistance change and corresponding voltage change for a fixed current covers the entire dynamic range of the ADC. Thus, for any resistance change the entire dynamic range of the ADC is utilized. The design in [44] can measure resistance values varying from 10kΩ - 9MΩ with a reported power consumption of 32μW at a sampling rate of 1.83kS/s. The low power consumption is achieved by duty cycling the system at low sampling rates to ensure circuit components which are not in use are turned off until they are required.

Readout circuits based on a resistance-to-period converter (RTP) [45] have also been demonstrated. In [45], a reference voltage (V_{IN}) is applied at the sensor and the constant current flowing through the sensor charges or discharges the capacitor C (Figure 1.13c). V_{OP}, which represents the integrated voltage at the output of op-amp A1, is compared against a reference voltage, V_T (V_T = -V_{IN}G) to determine the period of the voltage. V_{IN} can switch between two voltages V_A and -V_A based on the comparator output. Thus, when V_{IN} is connected to

V_A, V_{OP} decreases till its reaches V_T = -V_AG. At this moment, the comparator output is toggled and V_{IN} is connected to -V_A such that V_T=V_AG. At this point, V_{OP} rises linearly from -V_AG to V_AG. The time between the two consecutive transitions in the comparator output can be determined to be,

$$T = 2T_C = 4GR_{SENSE}C \tag{1.2}$$

where, T is the comparator output period, T_C is the time between comparator output transitions.

This design can measure resistances varying between 10kΩ and 10GΩ. However, the measurement time for the sensor can vary for microseconds (for small resistances) to seconds (for resistances on the order of 100GΩ). Moreover, the sensor is implemented using discrete components which results in a high power consumption ($\sim$ 500mW) which rules these devices out for low power applications as such wireless sensor nodes.

1.4 Thesis Overview

This work focuses on designing low power readout circuits for chemical sensor arrays which will potentially allow them to be integrated into a wireless sensor node. The first approach is based on measuring the resistance of chemoresistive beads and nanowires using sigma delta modulation. The design allows the resistance of the beads and nanowires to be observed with respect to time. Based on the magnitude and duration of the variation, information regarding the chemical analytes can be determined. The design also includes an array of locations where chemoresistive beads and nanowires can be integrated heterogeneously as described in this work. In case of chemoresistive beads, the array consists of openings in the passivation and top metal where beads can be placed so that they are connected to the sigma delta circuit. In case of chemoresistive nanowires, pads are provided on the top metal so that nanowires can be placed and connected to the sigma delta circuits via post CMOS electroplated posts. Measured results are provided for gold coated microbeads which were

successfully integrated into the array of a fabricated IC.

The second approach focuses on development of an on-chip impedance measurement system to determine the magnitude and phase information of a sensor which acts as a complex load. The integration of the impedance measurement system on die would be a novel approach which can provide another dimension to measurements of chemical sensors and their analysis. With some modifications to the design, the impedance measurement circuit can also be converted into an on-chip network analyzer which can be used to measure the S11 and S21 parameters of a varying load impedance.

1.5 Thesis Organization

The subsequent chapters presented in this thesis are organized as follows:

- *Chapter 2* The basics of sigma delta modulation are presented in this chapter. Measurement results from a previous IC design iteration are also presented in this chapter.
- *Chapter 3* discusses the procedure of assembling metal coated microbeads into an array coupled with the $\Sigma\Delta$ readout circuitry.
- *Chapter 4* covers the design, simulation, layout and measurement results for an improved design of the sigma delta readout circuit.
- *Chapter 5* covers the design and simulation results from a new impedance measurement approach.
- *Chapter 6* concludes the thesis with a brief summary of accomplishments of this work and a discussion of future research directions.

Chapter 2

Sigma Delta Modulator Design and Measurements

To monitor the resistance change of a chemoresistive sensor when a chemical agent is present, a readout circuit which can operate over a wide range of resistance values and a analog-to-digital converter (ADC) with a wide operating range are required. Since these circuits are required in wireless sensor nodes, they are required to operate with low power consumption. This thesis presents a readout circuit for chemoresistive sensors based on a charge to digital frequency circuit using a Sigma-Delta (Σ-Δ) modulator. The design can be used to measure a wide range of sensor resistance values while operating at minimal power consumption and is robust to CMOS parasitics, device mismatch and supply noise. The modulator design presented in this chapter, demonstrates a quick response time for resistance measurement which allows the modulator to monitor the sensor resistance for any brief resistance variations as the sensor is exposed to chemical agents.

Σ-Δ modulators are examples of oversampling modulators which use ADCs where the sampling frequency (f_s) which is much higher than the Nyquist frequency [1]. Oversampling ratio

[1] *Nyquist Frequency*: is defined as half the sampling frequency of a discrete signal processing system [46]

(OSR) of the modulator can be defined as follows:

$$OSR = \frac{f_s}{f_B} \tag{2.1}$$

where f_B is the maximum signal frequency.

Σ-Δ modulator uses feedback to improve its ADC by reducing the quantization error. The quantization error is reduced by adding a finite impulse response (FIR) loop filter to the feedback loop which allows the modulator to predict and correct the next quantization error value based on the current and preceding inputs for the modulator. The high sampling frequency of the modulator also spreads the quantization error over a wider range of frequencies while the signal power remains within the signal band. The high sampling frequency also relaxes the accuracy requirements on analog circuits, and also minimizes errors due to mismatch.

The block diagram for a sigma-delta(ΣΔ) (or delta-sigma (ΔΣ)) modulator is shown in Figure 2.1 where the input for the integrator ($x_\Delta(t)$) represesnts the difference (*delta*) between the input signal ($x(t)$) and quantized signal ($x_p(t)$). The integrator sums (*sigma*) this difference and feeds the quantizer with $x_\Sigma(t)$. The output of the quantizer ($y(n)$) is fed back to input via a DAC to calculate the difference. As a result, the output of the system tracks the average of the input signal. It is possible for $y(n)$ to be greater or smaller than the $x(t)$ for certain durations. However, over a large period of time, the average value of $y(n)$ should be identical to the input signal [47]. Thus, the output bit stream becomes related to the amplitude of the signal itself [48].

The loop filter of a ΣΔ modulator can be designed such that it shifts the ADC quantization noise out of the signal bandwidth to improve the signal to noise ratio of the modulator, thus improving its resolution [48]. Figure 2.2a presents the quantization noise shaping observed in a ΣΔ modulator. The resolution of ΣΔ modulators is also dependent on the oversampling ratio (OSR) of the modulators as presented in Figure 2.2b. As the OSR is doubled, the quantization noise decreases by 9dB which results in an increase of 1.5 dB in the ENOB [2]

[2]ENOB: Effective Number Of Bits

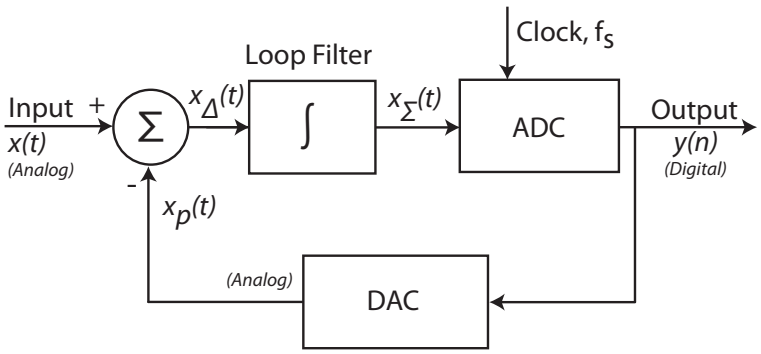
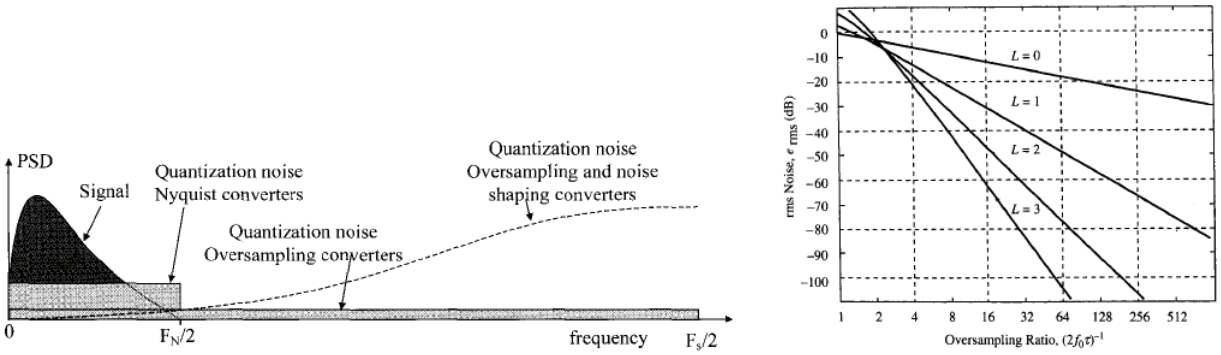


Figure 2.1: Block Diagram for 1st order ΣΔ modulator.



(a) (b)

Figure 2.2: (a) Noise shaping in ΣΔ modulators [from [48]]. (b) RMS noise vs. oversampling ratio for different orders of ΣΔ modulators [from [50]].

of the modulator [49, 50]. Recent work on ΣΔ modulators has focused on low power, high speed and high resolution designs for broadband ADCs [51], audio signal processing [52] and low power sensor interfaces [53].

The Σ-Δ modulator presented in this thesis is used to measure the variation of resistance with respect to time in chemoresistive beads and nanowires. The following sections provide discuss the operating principle for the modulator as well as detailed descriptions for each block of the modulator. This design was originally presented by J. M. Oliver *et. al.* in [54] and is extended and improved in this thesis.

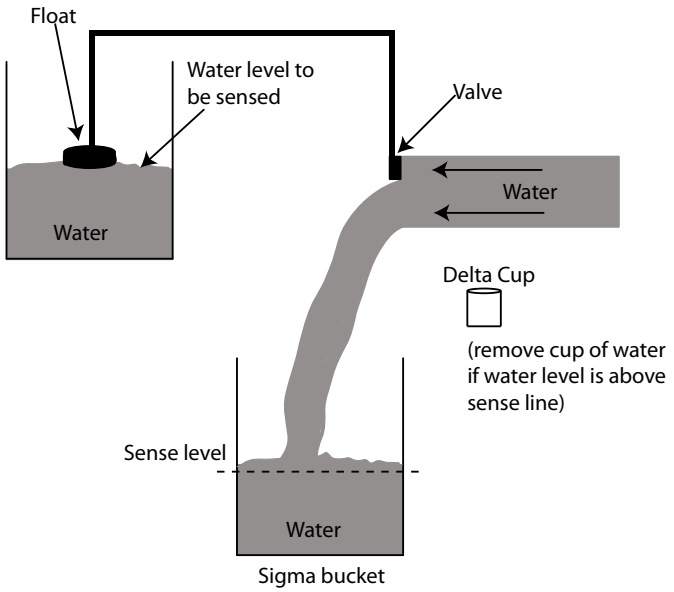


Figure 2.3: Water bucket analogy for sensing using $\Sigma\Delta$ modulators.

2.1 Sigma Delta modulator for resistive sensor readout

The design presented in [54] is based on the circuit discussed in [55] for measuring resistive memory cells and was modified for chemical sensing applications. Figure 2.3 presents the physical analogy for the Σ-Δ modulator design presented in [55]. Due to the floating valve in the sense bucket, the water level of the sense bucket controls the rate of water flowing from a supply pipe. As the water level increases the valve moves higher and the rate of water flow increases and vice versa. A "sigma" bucket is used to collect the water flowing out from the pipe and the water level of the sigma bucket is checked periodically to verify if it has crossed a certain threshold value (sense level). The sigma bucket is equivalent to an integrator or a first order loop filter and the periodic measurement of the water level is similar to the clocked quantizer used in a $\Sigma\Delta$ modulator as presented in Figure 2.1. When the water level in the bucket crosses the threshold, a "delta" cup with a known capacity is used to remove excess water and lower the water level to below its threshold value. The process of removing water from the sigma bucket when it crosses the threshold level is equivalent to subtraction of the feedback signal from the input signal (in Figure 2.1). Over an period of time, the rate

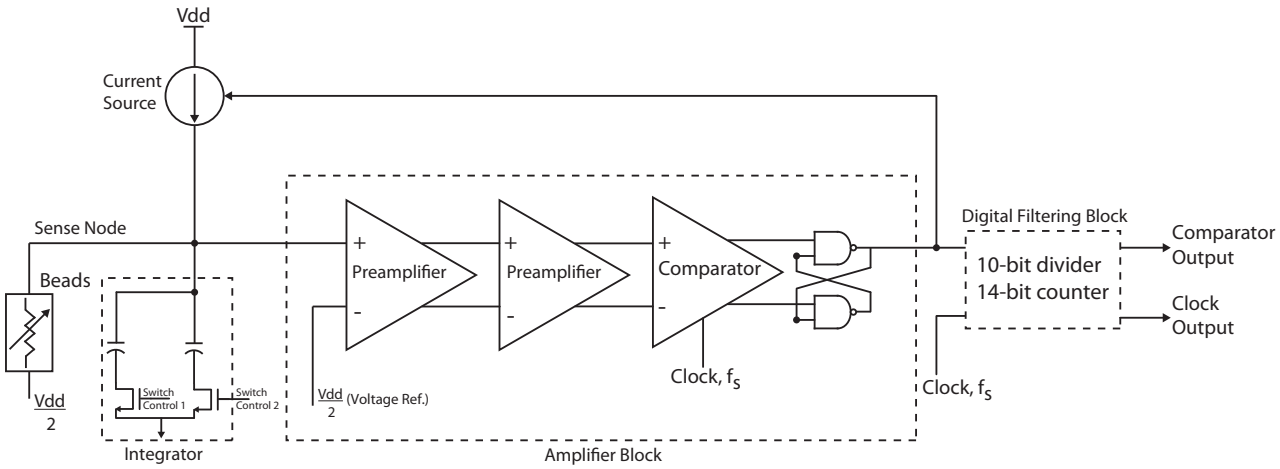


Figure 2.4: Block Diagram of $\Sigma\Delta$ modulator for chemoresistive beads and nanowires.

of water flow can be estimated by averaging the number of cups of water removed from the sigma bucket and the total number of times the water level of the sigma bucket is checked.

The block diagram for the modulator used in this thesis is shown in Figure 2.4. The capacitor and the current source in this figure are equivalent to the "sigma" bucket and the water flowing through the pipe respectively from the water bucket analogy presented earlier. The capacitors integrate (sigma) the difference (delta) between the current flowing out of the current source and current flowing through the resistive load. In the initial state, the capacitor is assumed to be charged to V_{DD} and the current source is off, thus, the capacitor discharges through the resistive load. When the voltage of the sense node falls below the reference voltage ($V_{DD}/2$) of the clocked comparator, the voltage drop across the resistor reaches zero since the lower end of the resistor is maintained at $V_{DD}/2$. This causes the output of the comparator to go low and turns the current source on to recharge the sense node to V_{DD}. When the capacitor is fully charged, the output of the comparator goes high to turn off the current source and the capacitor starts discharging through the resistor.

The toggling of the output due to the charging and discharging of RC circuit causes the period and duty cycle of the comparator output to vary as the resistance changes. As the resistance increases, the time constant increases which causes the current source to stay

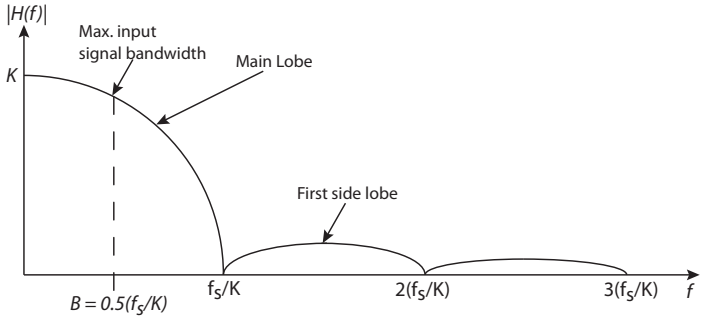


Figure 2.5: Frequency response of a counter.

turned on longer which, in turn, varies the duty cycle. The value of the resistance can therefore be associated with the duty cycle of the comparator output. In order to determine the average value of the duty cycle, the number of clock cycles for which the comparator output is high and total number of clock cycles need to be measured. This can be achieved by adding counters to the circuit to measure the number of cycles on the comparator output as well as the clock. The counter also serves as a low pass digital filter which filters the quantization noise and increases the resolution of the $\Sigma\Delta$ modulator. The low pass response of a counter (Figure 2.5) can be derived by relating the output to its inputs as shown in [47],

$$y[KiT_s] = \sum_{n=K(i-1)}^{Ki-1} x[nT_s] \tag{2.2}$$

where, K is the size of the counter and T_s is the period of the sampling clock with frequency f_s ($f_s = \frac{1}{T_s}$) between clock samples.

Equation 2.2 can be rewritten in z-domain as follows,

$$H(z) = \frac{Y(z)}{X(z)} = \sum_{n=0}^{K-1} z^{-n} = 1 + z^{-1} + z^{-2} + \ldots + z^{1-k} = \frac{1 - z^{-k}}{1 - z^{-1}} \tag{2.3}$$

From equation 2.3, the magnitude of the frequency response of the counter is determined to be,

$$|H(f)| = \left| \frac{1 - e^{-j.2\pi K \frac{f}{f_s}}}{1 - e^{-j.2\pi \frac{f}{f_s}}} \right| = \left| \frac{sin(\pi K \frac{f}{f_s})}{sin(\pi \frac{f}{f_s})} \right| \tag{2.4}$$

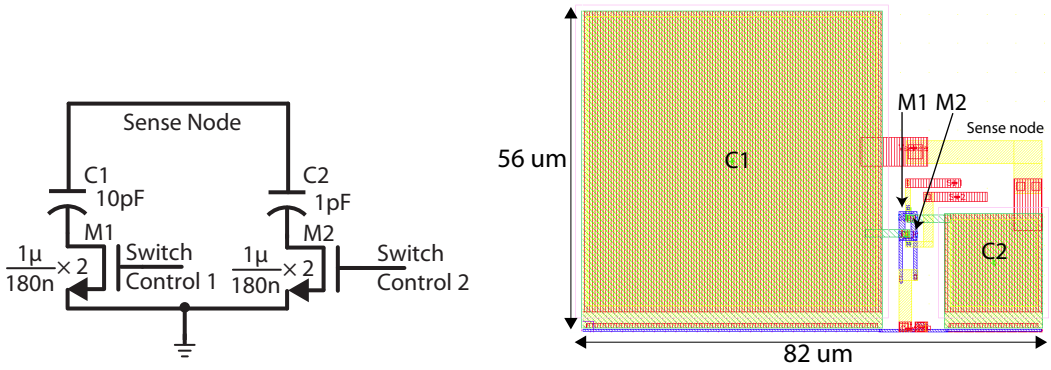
This can be re-written as,

$$|H(f)| = K \left| \frac{sinc(\pi K \frac{f}{f_s})}{sin(\pi \frac{f}{f_s})} \right| \tag{2.5}$$

The digital low-pass filtering provided by the counter helps eliminate the quantization noise and improve signal resolution since summing two N-bit words, requires a N+1 bit output to prevent any overflow. These filters also decimate the sampling rate which lowers the power dissipation (due to lower clock frequency). However, decimation results in aliasing of the quantization noise into the signal band. It is possible to improve the digital filter design by using products of sinc functions such as $sinc^2$ or $sinc^3$ functions to decrease aliasing and provide a sharper transition at the cutoff frequency.

A digital divider can also be used as a low pass filter since a divider acts as an up-counter and accumulates the output of the comparator block. The divider output corresponds to the MSB of the counter output which toggles when the counter overflows. Thus, the frequency response of the divider is also a sinc shaped response similar to that of the counter. In the design presented by Oliver *et. al.* [54], the counter was not integrated on chip to minimize the size of the IC. As the resistance of the load varies, the duty cycle and frequency of the comparator output change as well. The divider circuit lowers the output frequency and provides an output waveform with a 50% duty cycle. As the resistive load changes, the duty cycle and frequency of the comparator output change as well. Thus, changes in the resistance of the load can be represented as changes in the frequency of the divider output.

The Jazz semiconductor CA18HR 0.18μm CMOS technology was used for this design. The following sections discuss each block in the modulator in more detail and provide schematic and layouts. Relevant simulation results are also provided. Finally, measurement results for the prototype IC are presented.



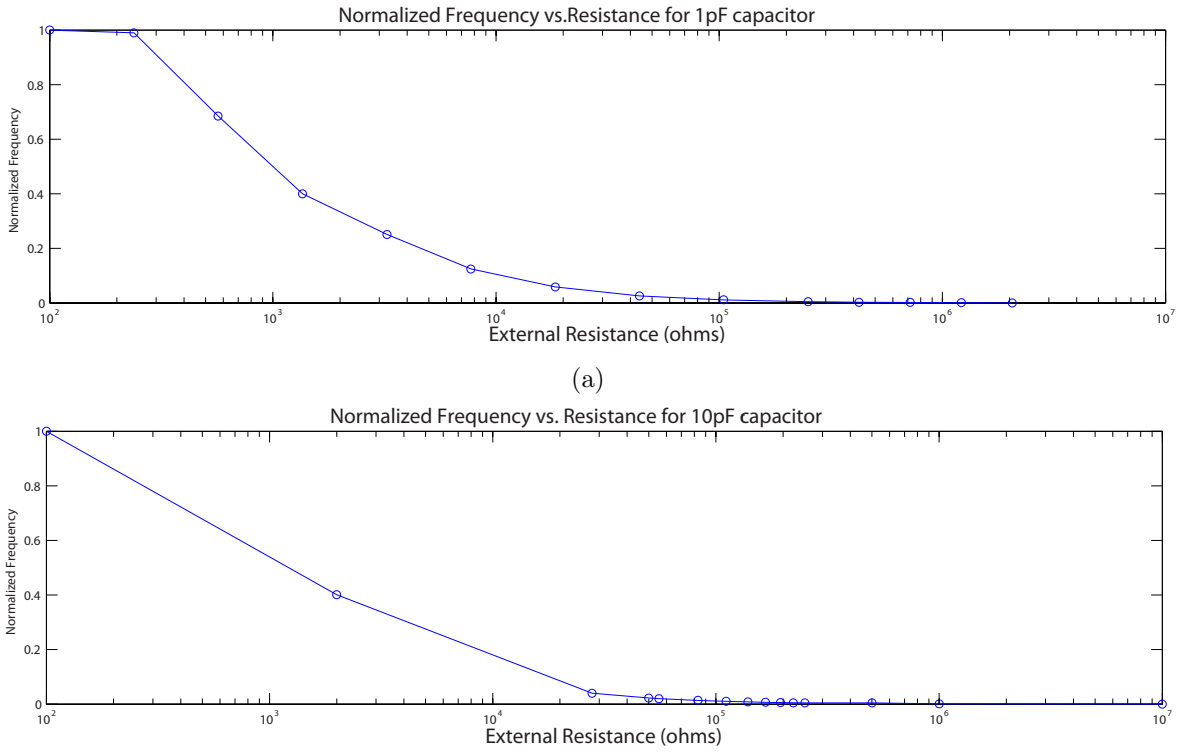
(a) (b)

Figure 2.6: (a) Schematic for integrator; (b) layout.

2.2 Integrator

The loop filter used in the design is a first-order integrator in the form of a capacitor. The top plate of the capacitor is connected to the resistance being measured (via the sense node in Figure 2.4). The bottom plate of the capacitor is connected to an NMOS transistor which is used as a switch. The switch provides the option of selecting different integrating capacitors in order to measure a particular frequency range. The NMOS switch is sized to provide a low source-drain resistance and when the switch is off, the lower plate of the capacitor is floating. When one of the switches is turned on, the lower plate of the capacitor is connected to ground and the capacitor forms an RC circuit due to the resistive sensor load. In [54], 1pF and 10pF capacitors were used so that for a fixed resistance value, the time constant for the RC circuit varied by an order of magnitude depending on the capacitor value selected. Using multiple capacitors provides control over the measurement range which can be varied by adding different integrating capacitors and selecting appropriate clock frequencies. The schematic and layout of the integrator block are provided in Figure 2.6.

The clock frequency used in the comparator was selected based on simulation results and is dependent on the capacitor value selected in the integrator. When a 400 MHz clock input is provided to the comparator and the 1pF capacitor is selected, the duty cycle and



(a)

(b)

Figure 2.7: Normalized output frequency for (a) 1pF capacitor with 400 MHz clock input; (b) 10pF capacitor with 40 MHz clock input.

output frequency of the comparator output are sensitive to the resistive load for resistances between 2kΩ and 100kΩ (Figure 2.7a). Similarly, when the clock input is 40 MHz and the 10pF capacitor is selected, the comparator output demonstrates sensitivity to resistances between 100kΩ and 30MΩ (Figure 2.7b). As mentioned earlier, although the duty cycle of the comparator output varies due to resistance variation, the divider output demonstrates variation in the output frequency as the resistive load varies.

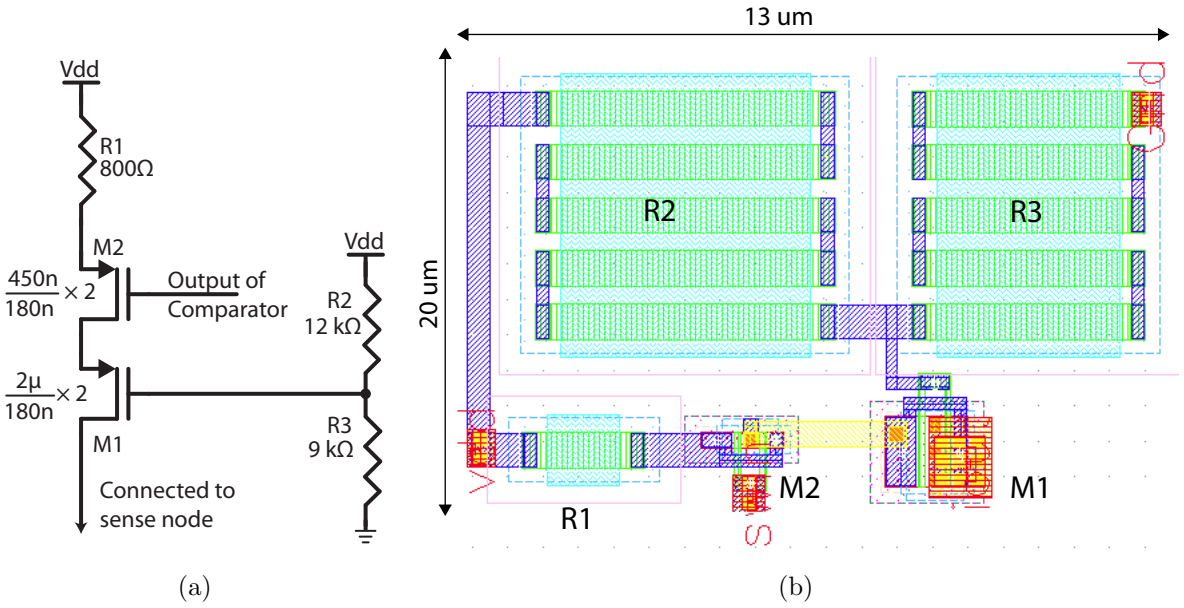


Figure 2.8: (a) Schematic for current source; (b) layout.

2.3 Current Source

The current source designed to recharge the integrating capacitors is shown in Figure 2.8. The current source consists of a resistive load, R1 (800Ω) to degenerate the switching transistor (M2). The load reduces the current rise time which prevents glitches since it reduces the stray capacitance and results in quicker charging/discharging of the parasitic capacitances. Transistor M1 is used a cascade buffer amplifier to minimize the clock feed-through to M2. Since M1 and M2 are PMOS transistors, the current source turns on when the comparator output is low i.e. the voltage of the sense node is below the reference voltage. When the current source is turned on, it provides 75μA of current to the RC circuit as observed in Figure 2.9.

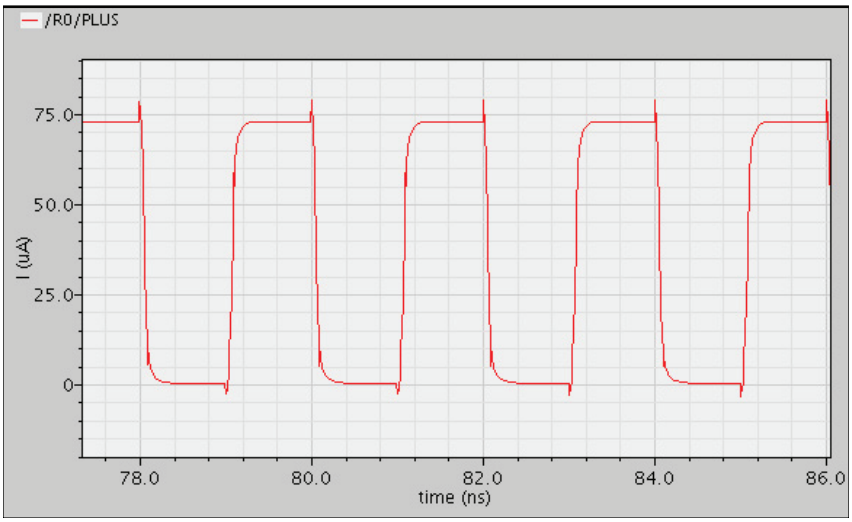


Figure 2.9: Simulated output for Current Source.

2.4 Comparator

In order to determine the sign of the difference between the input and reference voltages quickly, a high speed comparator is required [56]. High speed comparators should have a low propagation delay time, which is not possible when the input voltages are low. The RC circuit formed by the parasitic capacitance and resistance present in the comparator cause the propagation time to increase for low voltage inputs. As a result, preamplifiers are used to amplify low input signals so that the parasitic RC network present in a high speed comparator charges and discharges quicker. By placing preamplifiers before a comparator, the negative exponential response of a preamplifier and the positive exponential response of a comparator are combined as seen in Figure 2.10. The preamplifier amplifies the input voltage to a intermediate voltage level, V_X, in time t_1. This voltage is applied to the comparator input which amplifies V_X to the output voltage, V_{Out} in time t_2. As a result, the total propagation delay is t_1+t_2. If no preamplifier was used, the time required for the output voltage of the comparator to reach the upper voltage rail is greater than t_1+t_2. The preamplifier is designed so that it has a wide-bandwidth and uniform low-gain over the bandwidth. Cascading multiple preamplifiers decreases the delay time, t_1, further.

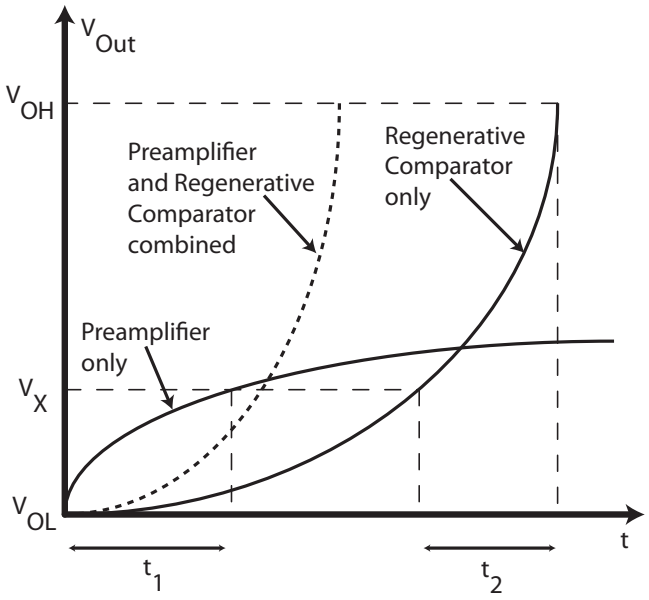
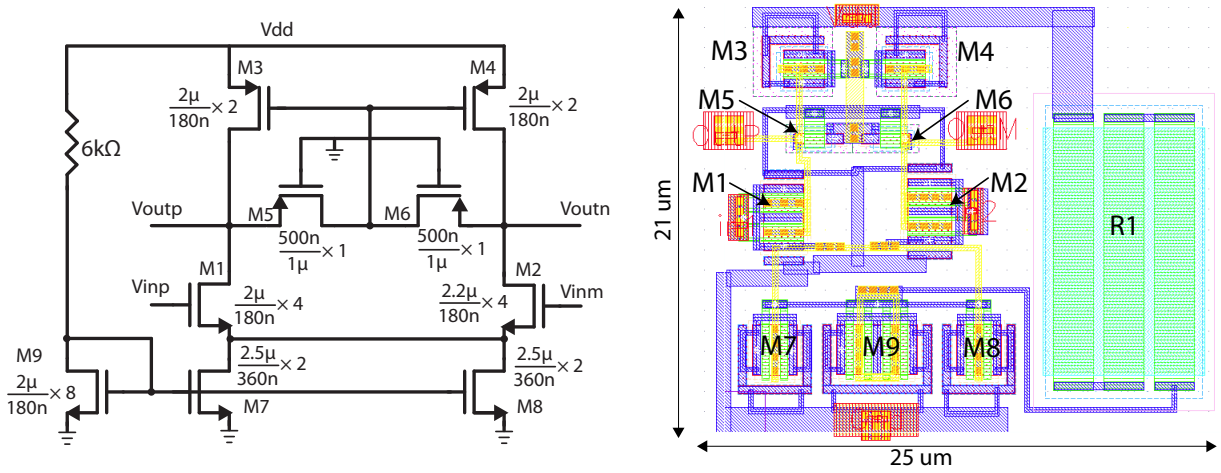


Figure 2.10: Step Response of a preamplifier and a regenerative comparator.

2.4.1 Preamplifier

In this design (Figure 2.11), two preamplifiers with a gain of 10V/V each are cascaded before the comparator. Each preamplifier consists of a differential pair of NMOS transistors (M1, M2) which drive the load transistors (M3-M6). In order to provide a common mode average of output signals to feedback into the current source loads M3 and M4, transistors M5 and M6 are biased to operate in the linear resistive region [54]. M7, M8 and M9 form the current mirror which is used to bias M1 and M2. The dimensions for the transistors were selected using simulation results to minimize power consumption and the propagation delay of the preamplifier. The exponential behavior of the preamplifier in case of a step voltage input can be observed in Figure 2.12a. Figure 2.12b shows the transient gain of the preamplifier, and the frequency/phase response can be observed in Figure 2.12c. The current consumption for the preamplifier block as simulated to be 370μA, where the current flowing through each leg of the preamplifier was 90μA.



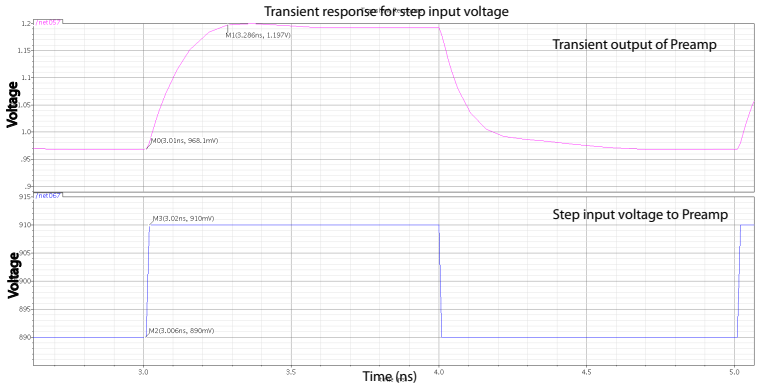
(a) (b)

Figure 2.11: (a) Schematic for preamplifier used in comparator; (b) layout for preamplifier used in comparator.

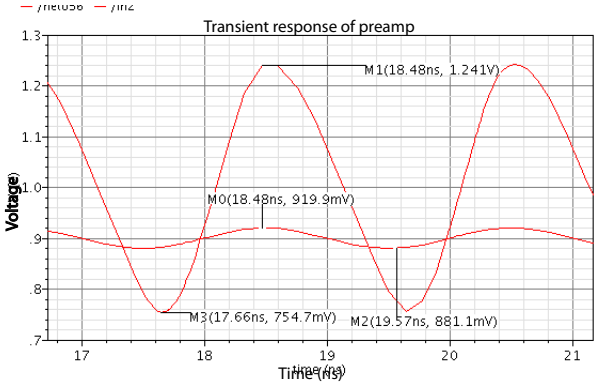
2.4.2 Comparator

The outputs of the preamplifier stage were used as inputs for a regenerative comparator which uses positive feedback to decrease the propagation delay of a signal through a comparator. A regenerative comparator is also known as a latch or a bistable comparator and require a clock signal to trigger a comparison of the input signals [56]. The schematic for the regenerative comparator used in this design is provided in Figure 2.13.

The comparator inputs are applied to the gates of transistors M1 and M2 which determines the current flowing through M3 and M4. When the clock is high (M5 acts a closed switch), the drains of M3 and M4 are connected to the outputs. Also, the signals at the gates of M7 (or M8) can go through either M7 (or M8) or through M3 (or M4). Thus, M3 and M4 form a parallel feedback path for the comparator. Regenerative comparators operate in two modes: the pre-trigger state while the clock is low and the regenerative state while the clock is high. At the positive clock edge, the difference between the input voltages is amplified to the voltage rails due to the positive feedback. The gain of the feedback path



(a)



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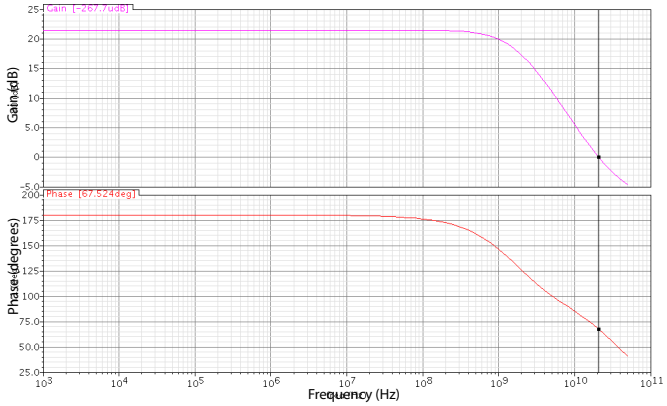
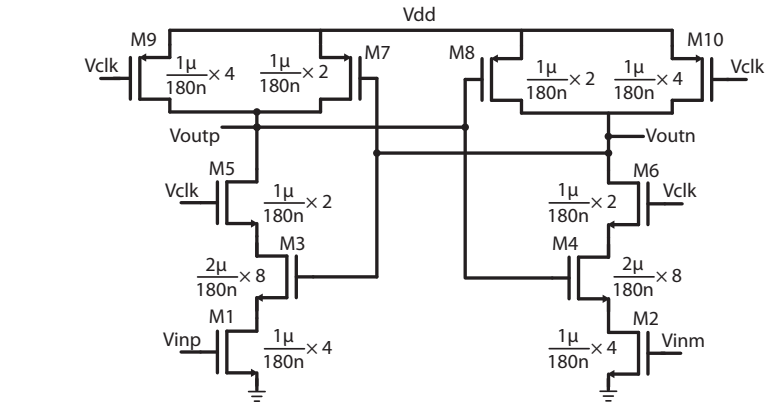


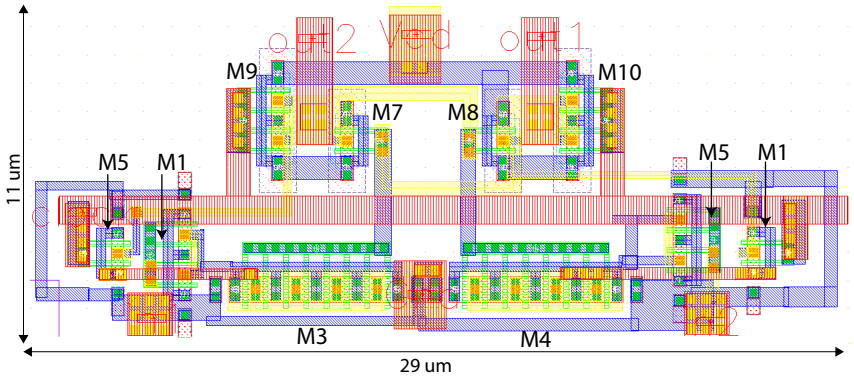
(c)

Figure 2.12: (a) Step response of preamplifier; (b) Small signal gain in preamplifier; (c) Frequency and phase response of preamplifier.

is determined by the current flowing through M3 and M4 and the side with the larger gain



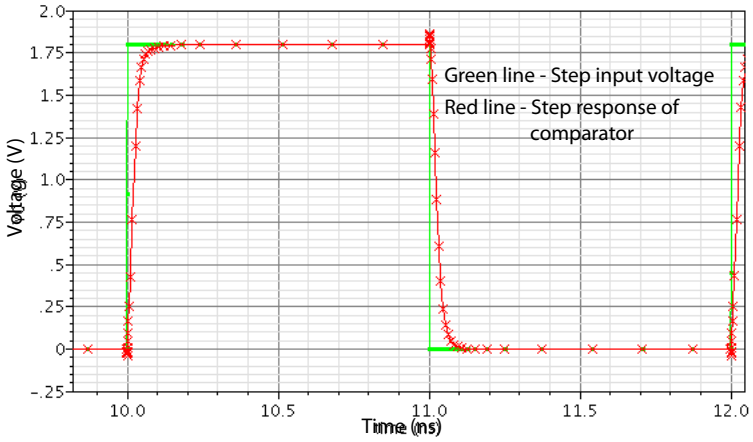
(a)



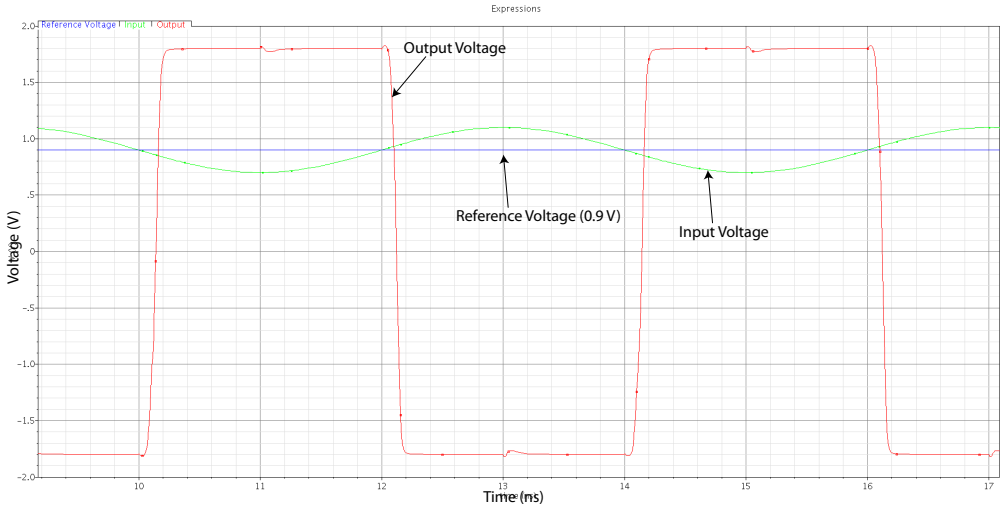
(b)

Figure 2.13: (a) Schematic for regenerative comparator; (b) layout.

moves towards the positive voltage rail [56]. The transistor sizes were selected based on simulations to provide a trade-off between power consumption and propagation delay of the comparator. The exponential step response of the comparator can be observed in Figure 2.14a and the comparator output with respect to the input can be observed in Figure 2.14b. The simulated value of dc current flowing through the comparator was determined to be approximately 0μA. This is due to the class B nature of the comparator which prevents a direct path from V_{DD} to ground when the clock is at a constant voltage.



(a)

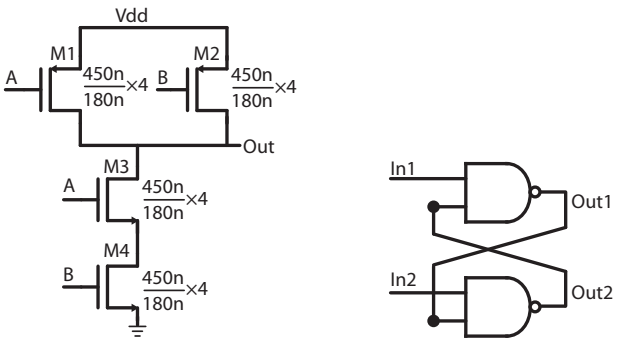


(b)

Figure 2.14: (a) Step response for the regenerative comparator; (b) Output of the regenerative comparator.

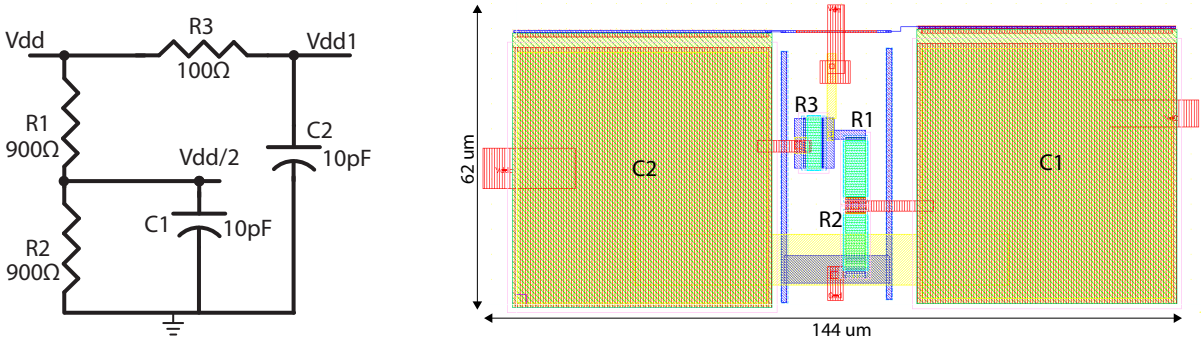
2.4.3 NAND Latch

The output of the comparator is held constant for one clock period using the latch formed using the NAND gates at the outputs of the comparator. At the start of each clock cycle, the latch value is updated based on the comparator output. The schematic and layout for the latch are shown in Figure 2.15. The transistor sizes for the NAND latch were optimized



(a) (b)

Figure 2.15: (a) Schematic for NAND gate; (b) Schematic for NAND latch.



(a) (b)

Figure 2.16: (a) Schematic for reference voltage generator; (b) layout.

using simulations.

2.4.4 Voltage Reference Generator

In order to generate a reference voltage for the comparator block on-chip, a simple resistive voltage divider was designed as shown in Figure 2.16. The 10pF capacitors, C1 and C2 shunt any high frequency signals (such as noise present in the power supply) to ground. While the voltage divider is a simple way to generate the $V_{DD}/2$ voltage, the current flowing through the resistor is approximately 800μA. Thus the power dissipation of the voltage reference generator is approximately 1.5 mW. This is targeted for improvement in future designs.

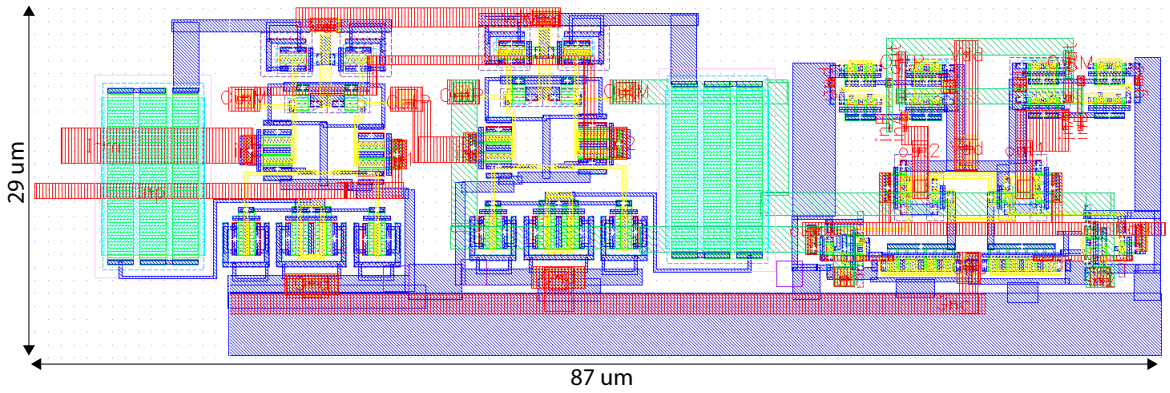


Figure 2.17: Layout of the comparator block.

The layout for the entire comparator block (without the reference voltage generator) is shown in Figure 2.17.

2.5 Output Block

As discussed earlier, the SNR of an Σ-Δ modulator can be improved by low pass filtering the comparator output. In this design, a 10-bit frequency divider circuit was used to provide low pass filtering. The dividers convert the duty cycle and period variations of the comparator output into a frequency variation and also lower the output frequency so that it can be measured using the available lab equipment. The divider is implemented by cascading D flip-flops. The D flip-flops are based on PowerPC flip-flop architecture and are also known as transmission gate flip flops. This architecture has a low clock-to-Q delay which makes it ideal for high-speed applications. The design is also ideal for low power designs due to the small number of transistors and the feedback path [57, 58]. The design of a single flip-flop block and its components is shown in Figure 2.18. The 10-bit divider is formed by cascaded flip-flops so that one of the outputs of the first flip-flop is used as clock for the second and so on, as seen in Figure 2.19.

The oversampling ratio for the modulator can be determined by dividing the sampling fre-

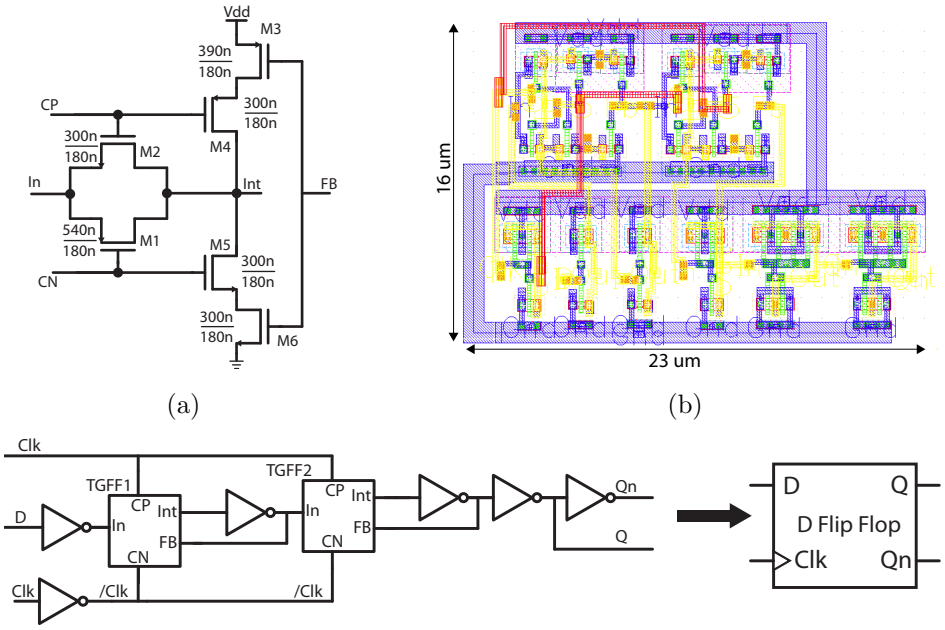


Figure 2.18: (a)Design of Transmission Gate used in flip-flop block. (b) Layout of D Flip-Flop. (c)Schematic of D flip-flop based on Power PC architecture.

quency of the comparator and output frequency. For a clock frequency of 40 MHz in the comparator, the output of the 10-bit divider is 39 kHz (40 MHz divided 2^{10}). Similarly, for a 400 MHz clock input, the output of the 10-bit divider is 390 kHz. Thus, the divider provides an oversampling ratio of 2^{10} for the modulator. The prototype IC which was used to perform measurements for this thesis, contained only the 10-bit divider on-chip. As a result, the oversampling ratio for the design was 2^{10}.

In the prototype IC design, the output of the divider is used as input for the output buffers in order to drive the output load with sufficient voltage and current. The buffer design is based on the exponential horn design, where the width of subsequent inverter stages increases exponentially (Figure 2.20). This design provides high gain in the buffer and allows it to drive large capacitive loads.

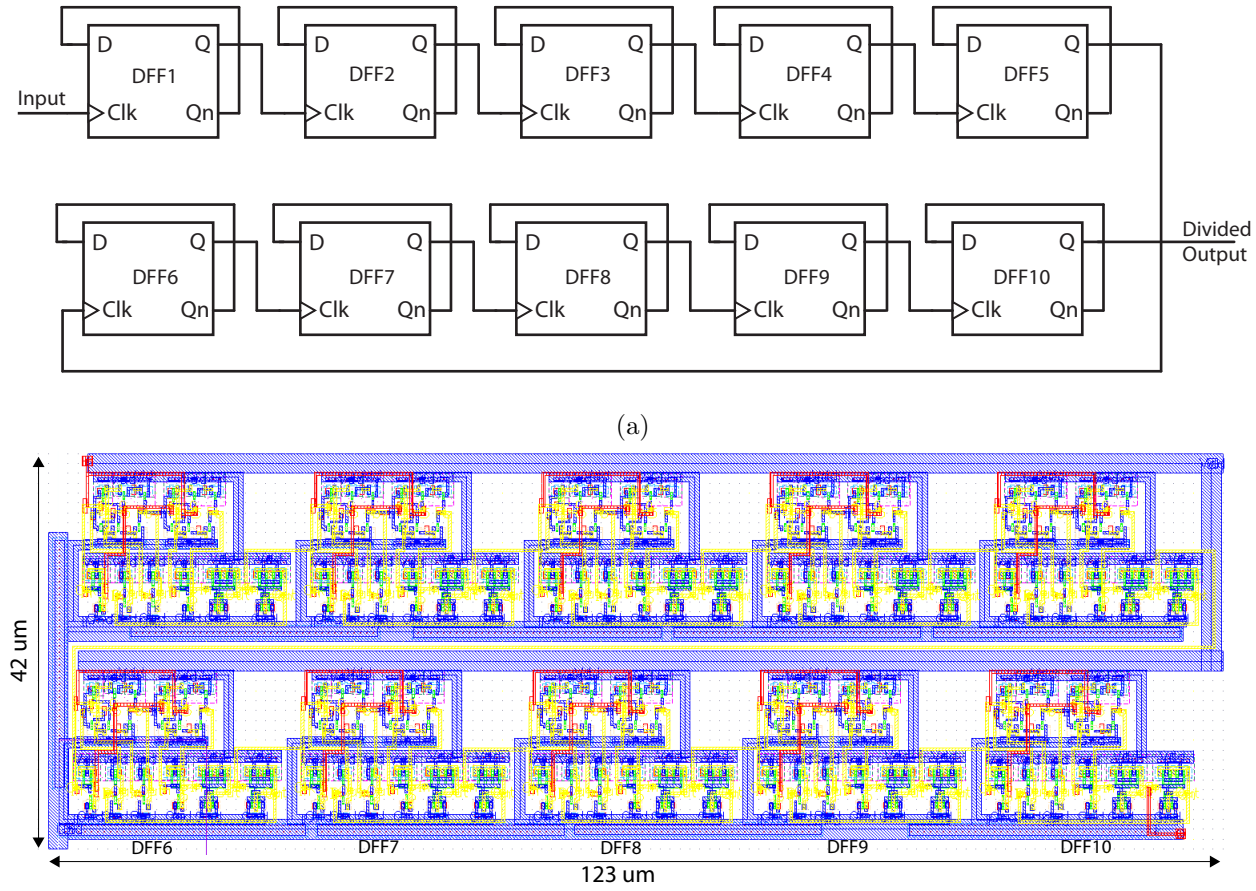


Figure 2.19: (a) 10-bit divider built using cascaded D flip flops. (b) Layout of 10-bit divider.

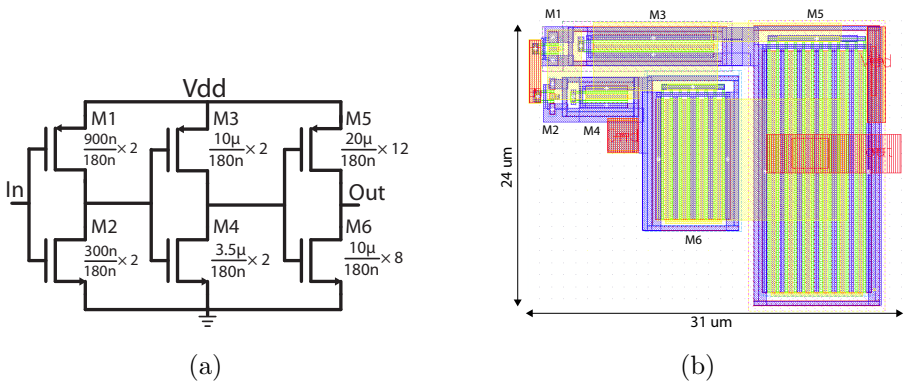


Figure 2.20: (a) Schematic for output buffer stage; (b) layout.

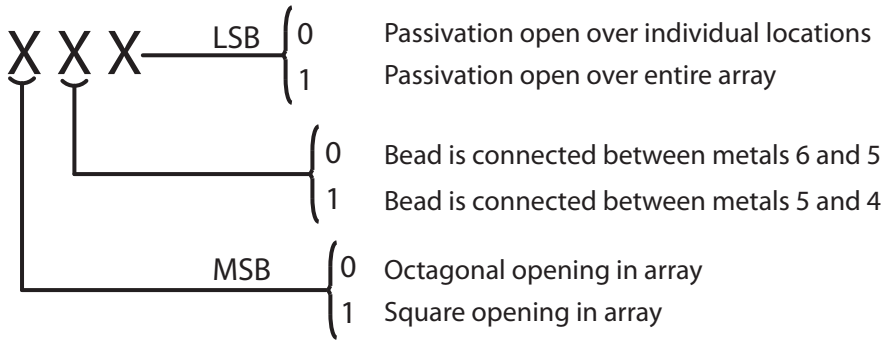


Figure 2.21: 3-bit encoding scheme for variants of array design.

2.6 Array Design and Addressing Logic

The design presented in [54] was targetted for arrays of chemoresistive beads. In order to integrate the beads on the surface of the IC, a 4x4 array of openings was designed using the metal and passivation layers present in the design kit.

Depending on the shape (octagonal or square), the process metal layers used for making contact with the bead (metals 4 and 5 or metals 5 and 6) or the passivation openings (passivation open over entire array or only around the openings), eight array variants were designed. The shape of the openings and size of passivation was varied to test bead integration. For ease of identification, the variants were given a 3-bit code as shown in Figure 2.21. SEM images of some variants can be observed in Figures 2.22.

The top metal layer in all array variants was connected to $V_{DD}/2$ and the bottom metal layer in all locations was connected to the sense voltage node (V_{sense}). When a chemoresistive bead is integrated into an opening, it should make contact with the top and bottom metal layers and its resistance is measured by the readout circuit. Cross-sectional images of the array opening configurations are shown in Figure 2.23 and the layouts for array variants 000 and 111 are shown in Figures 2.23c and 2.23d.

In order to access each individual location, a direct addressing scheme was implemented using four bits. Based on the addressing bits, a single array location is selected and the

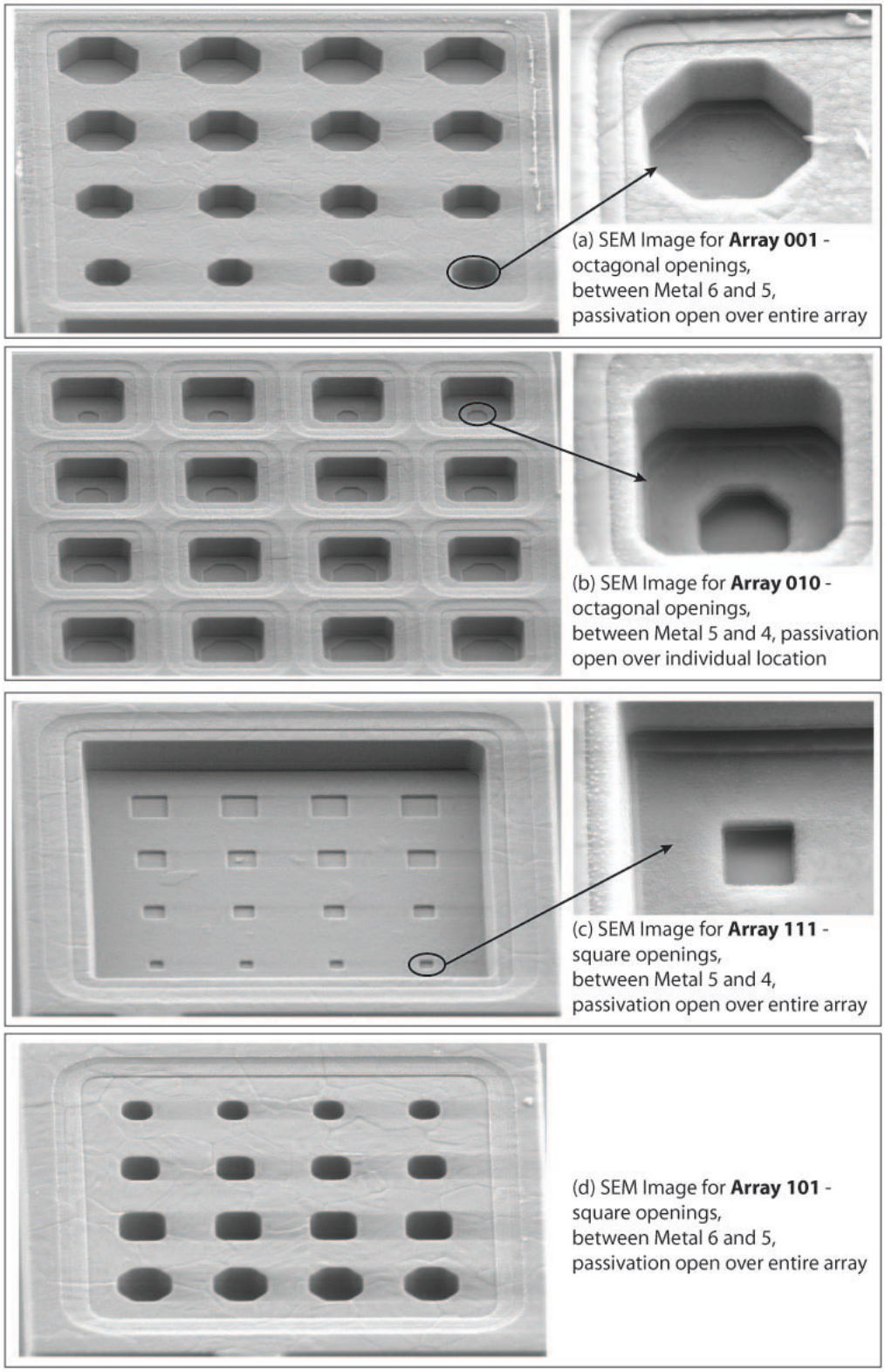


Figure 2.22: SEM Images of 4x4 arrays and close up of individual locations.

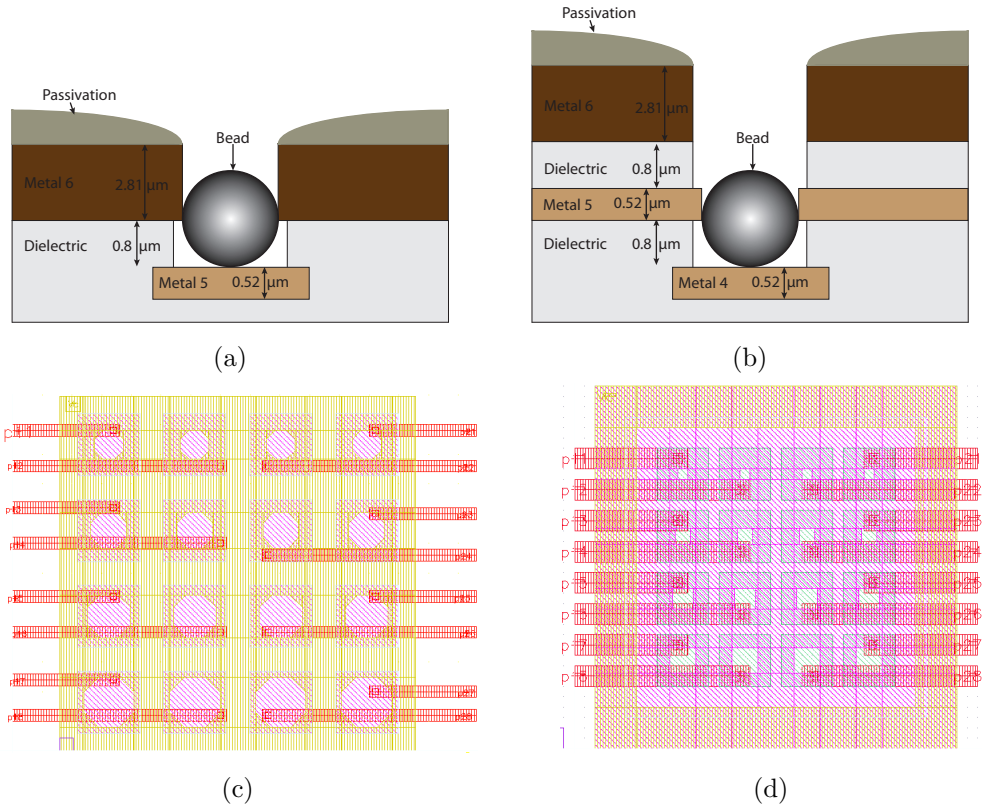


Figure 2.23: (a) Cross-section for beads between metal 6 and 5 (arrays numbered X0X). (b) Cross-section for beads between metal 5 and 4 (arrays numbered X1X). (c) Layout for Array 000. (d) Layout for Array 111.

corresponding access transistor turns on. When the access transistor turns on, it connects the lower metal layer to the V_{sense} node (one of the inputs to the comparator block). At this point, if the array location contains a chemoresistive bead in contact with the top and lower metal layers, the voltage drop across the bead will be V_{sense}-$V_{DD}/2$. Thus, the resistance of the bead can be periodically measured and monitored for any changes. The block diagram for the addressing block and the layout of the addressing design for array 000 is shown in Figure 2.24. Detailed schematics for the addressing blocks are provided in Figure 2.25.

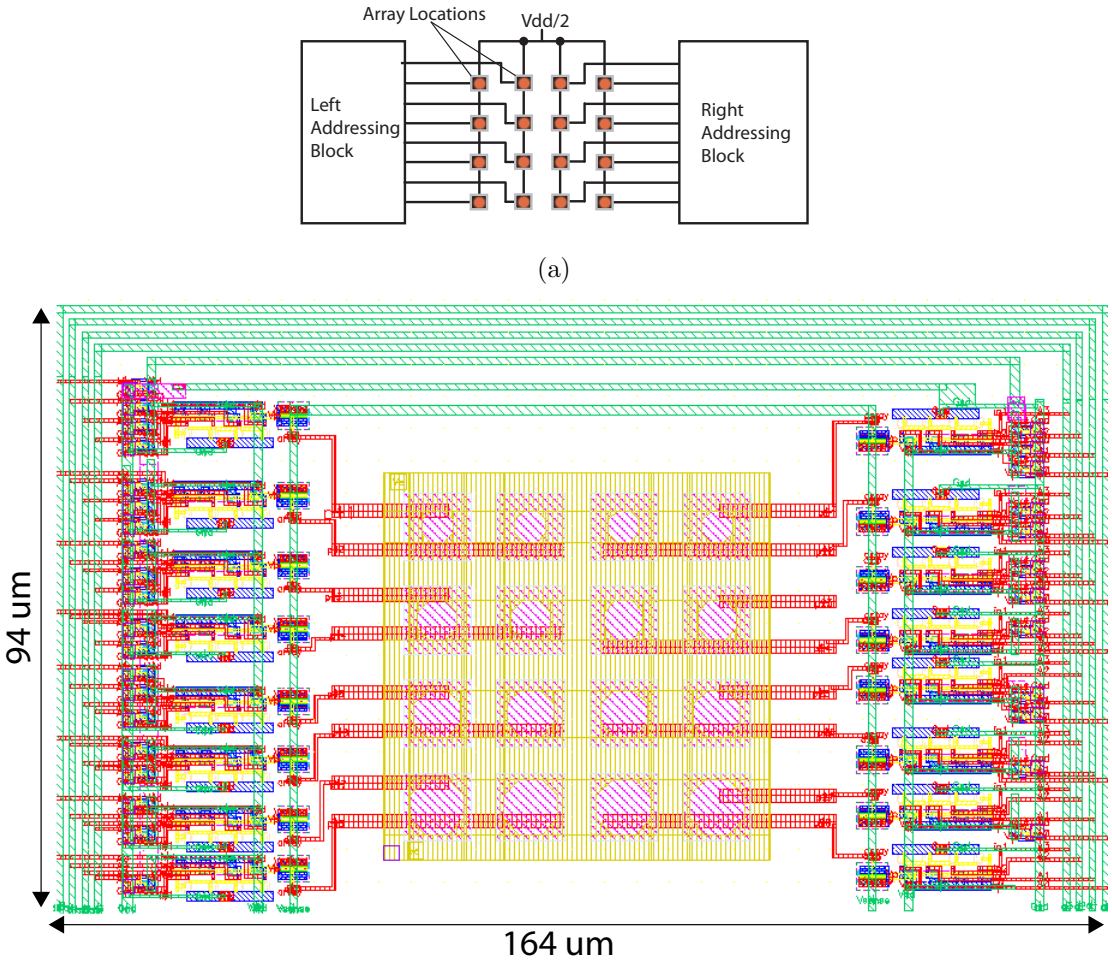


Figure 2.24: (a) Block diagram for addressing block. (b) Layout for array 000 - including addressing blocks.

2.7 Measurements and Results

The layout of the prototype IC and the corresponding fabricated IC is shown in Figure 2.26. In order to effectively utilize the die area, two variants of the array design were combined into one-quarter of the fabricated tile. Thus, a single tile contained eight variants of the array design. As seen in Figure 2.26a, a pad for connecting the IC to an external resistor was provided on the IC to enable direct testing of the $\Sigma\Delta$ modulator. One terminal of the

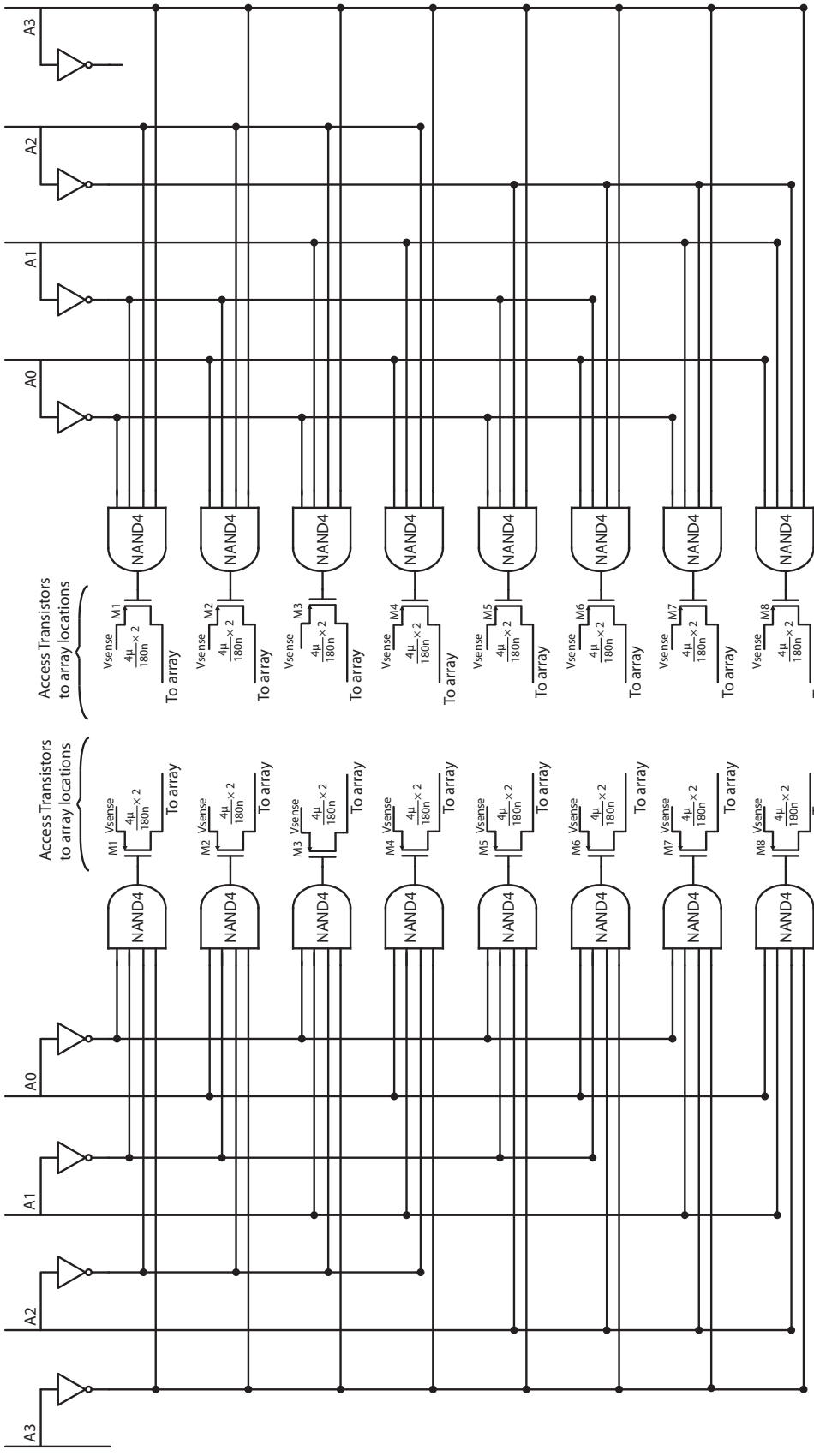
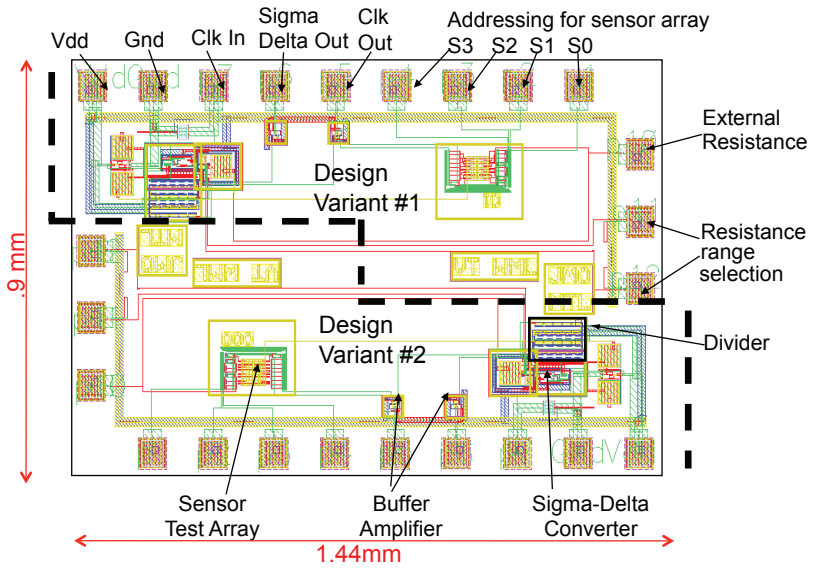
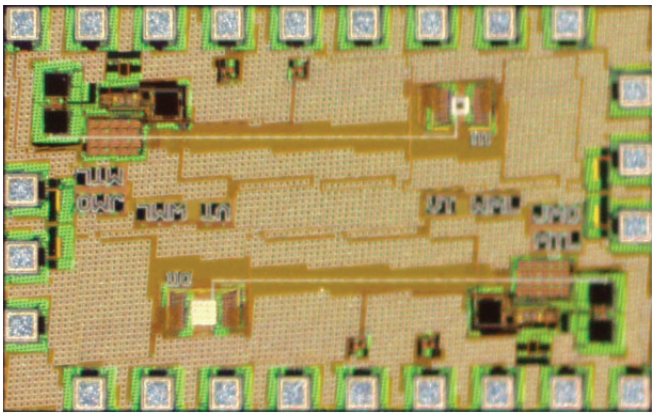


Figure 2.25: Schematic for array addressing.



(a)



(b)

Figure 2.26: (a) Layout for Prototype IC. (b) Fabricated Prototype IC.

external resistor was connected to the pad via a DC probe and the other end was held at 0.9 V through the power supply. The range selection pads provided on the IC are used to select an integrating capacitor by connecting the pad for the desired range to Vdd. The Vdd, Clk In, addressing voltages, $\Sigma\Delta$ Out and clock out pads were accessed using a 9 pin DC/low frequency probe (Figure 2.27). The frequency of the sigma delta out and clock out signals was observed on an oscilloscope to verify the operation of the IC.

The DC current provided by the power supply to the IC was 1.6 mA which results in a DC

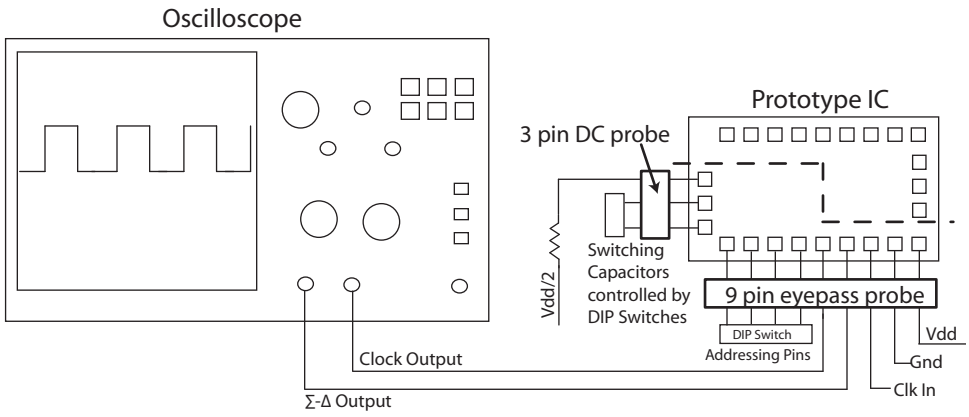
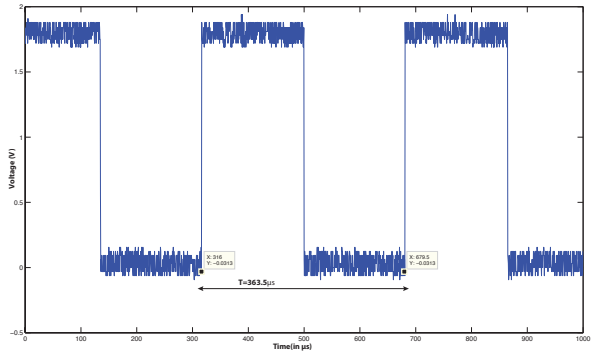


Figure 2.27: Test Setup for measurements of prototype IC.

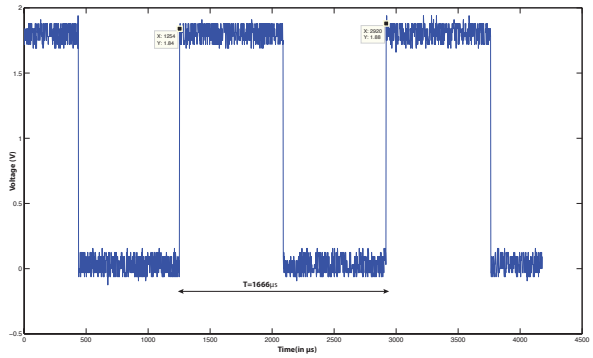
power consumption of 3mW. The resistive dividers used throughout the IC for biasing result in the relatively high power consumption. The main contributor is the resistive divider in the voltage generator with a power consumption of 1.98 mW. The ΣΔ modulator output for 56kΩ and 324kΩ external resistors is presented in Figure 2.28. Both output waveforms have a 50% duty cycle and the output frequencies were 2750 Hz for 56kΩ resistor and 600 Hz for 324kΩ. Thus as the resistance increases, the frequency decreases because the period of the comparator output increases.

A range of discrete external resistances were sequentially connected to the external resistance pad. The range of values measured varied from 2kΩ to 10MΩ (Figure 2.29). Since, higher resistance values were not readily available as discrete resistors, the measured plot was extrapolated to determine the highest measurable resistance. Based on the extrapolation, this value was determined to be 30 MΩ. The lowest resistance measurable resistance was determined to be 2kΩ which is higher than the minimum value obtained from simulations. This could be due to parasitic resistances in the sense node trace and the addressing block which were not taken into account. The external wiring and probe contact could also result in the deviation.

In order to verify the operation of the array sensor sites, a drop of deionized (DI) water was placed over the array with a specific site selected by setting the addressing voltage bits. The



(a)



(b)

Figure 2.28: Σ-Δ output for (a) 56kΩ and (b) 324kΩ external resistances.

output frequency was then measured as the water droplet evaporated. Since DI water has a very low concentration of ions, its resistivity is approximately 17MΩcm. The frequency of the output signal was also measured when a drop of ordinary tap water was placed over the array. Tap water contains ions and several dissolved metals which reduces the resistivity of water as compared to DI water. The variation of frequency in the output signal for DI and tap water droplets can be observed in Figure 2.30.

From figure 2.30, the initial frequency of the output signal for DI water is approximately 158 Hz and increases up to 200MHz when the water drop is placed over the array. Using the plot presented in Figure 2.29, the IC output frequency was measured to be 158 Hz when a $\sim$ 12.2MΩ resistance is connected to the IC. Similarly, the IC output frequency is 200 Hz when a 10.25MΩ resistance is connected to the IC. Thus, the resistance measured by the

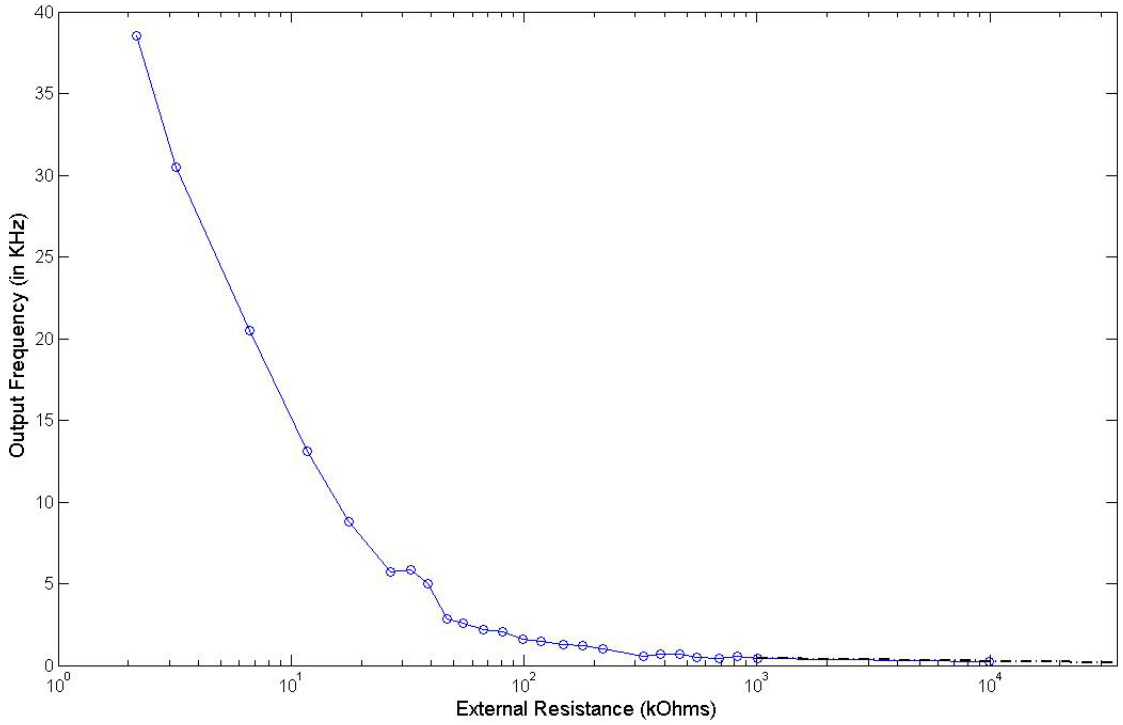


Figure 2.29: Measured output frequency for various external resistance values.

array before the DI water droplet is placed is $\sim$ 12.2MΩ and when the droplet is present on the surface, the measured resistance is 10.25MΩ.

Similarly, the initial output frequency in presence of tap water is $\sim$175 Hz which increases to 390 Hz when the water drop is placed on the array surface. Using figure 2.29, the initial resistance is estimated to be $\sim$11.5MΩ which decreases to $\sim$2.5MΩ (corresponding to 390 Hz) when the drop of tap water is placed over the array. In case of the tap water, the chemicals and minerals present in it could leave deposits behind which prevent formation of a good contact between the water drop and the metal surface. This could potentially result in measurement errors. However, no such effects were observed for the measurement results provided here.

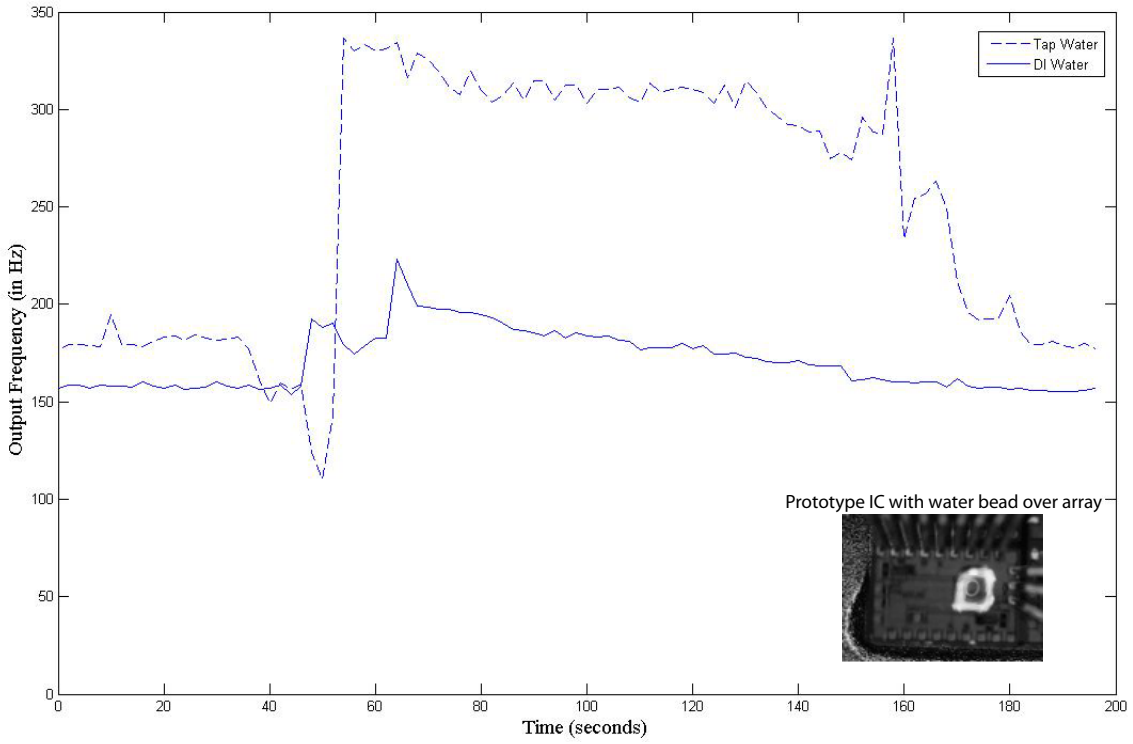


Figure 2.30: Variation of output frequency with time for DI water (solid) and tap water (dash) droplets. (Inset) Prototype IC with water drop present over array.

2.8 Summary

This chapter provides an overview of sensor resistance measurement using the $\Sigma\Delta$ modulator. Details regarding the design and simulation results for each individual component of a prototype IC are presented in this chapter. Measured results obtained from a prototype IC design are also presented. These results demonstrate the operation of the modulator with an external resistance connected to the modulator or in presence of a DI water drop over the array. The measured results also highlight some drawbacks of this design, such as the power consumption of the design and the array addressing design. The power consumption of this design was measured to be 3mW which is high from a low power application where these sensors would typically be used. Therefore, future design iterations require this power consumption to be lowered. The design of the addressing scheme in this design is not

scalable for large array sizes which are required for large scale integration of chemoresistive beads in cross-reactive arrays. Thus, a larger array size with an addressing scheme based on row/column selection is required. Based on the drawbacks, modifications to the existing design are discussed in the following chapters.

Chapter 3

Heterogeneous Integration of Chemoresistive Bead and Nanowires

The $\Sigma\Delta$ readout circuit presented in Chapter 2 demonstrated the operation of the array circuit in presence of water with different levels of conductivity. However, one of the drawbacks of the design highlighted in the previous chapter is the small array size (4x4) which limits the number of array locations available for integration of chemoresistive sensors. Since cross-reactive sensor arrays require a large number of sensors to successfully identify analytes present in a mixture, the size of the array needs to be increased to provide more array locations. As a result, a new array with 16x16 array locations was designed. The modified array design and the process flow used to integrate beads into the array locations are presented in this chapter.

This chapter also presents an alternate process flow for integrating chemoresistive nanowires with the IC. The modified array design for chemoresistive nanowires is also covered here. Chemoresistive nanowires provide a larger surface area for sensing analytes as compared to the beads and could increase the sensitivity of the readout circuit towards a larger range of analytes. The new array designs were used to create four IC variants such that two variants used chemoresistive beads and the other two variants used chemoresistive nanowires. The

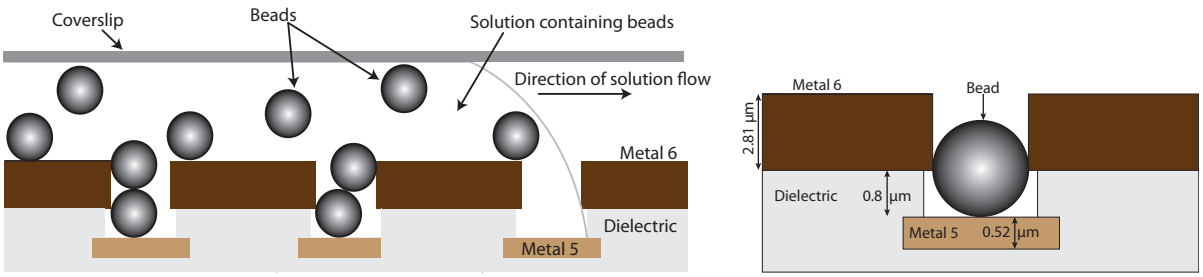
Table 2: List of design variants for second design iteration

Chip	**Sensor type**	**Details**
00	Chemoresistive beads	Octagonal array openings (4.5μm diameter) on top metal (metal 6) and metal 5
01	Chemoresistive beads	Square array openings (2μm side) on top metal (metal 6) and metal 5
10	Chemoresistive nanowires	Integration steps for nanowires require etching away excess metal present
11	Chemoresistive nanowires	No metal etching required for nanowire integration

readout circuit used in these variants was modified to improve on the design presented in the Chapter 2. The modifications to the readout circuit are discussed in detail in the next chapter (Chapter 4). The new IC was designed using the Jazz semiconductor CA18HR 0.18μm CMOS technology and the variants were numbered using a 2 bit coding scheme was shown in Table 2.

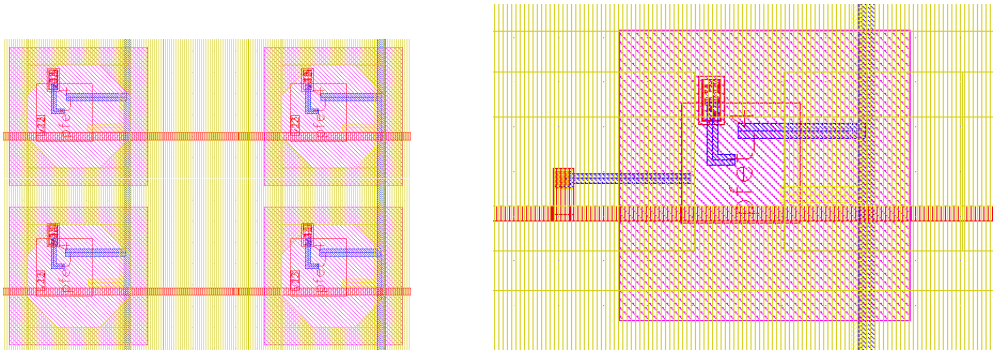
3.1 Integration of Chemoresistive Beads

The post-processing steps required to integrate chemoresistive beads into the array openings were developed in collaboration with researchers at Penn State. In the proposed method, a mixture of DI water and chemoresistive beads is allowed to flow between a glass cover slip and the top layer of the array. By controlling the flow of the liquid, a single chemoresistive bead can be assembled in each array opening (Figure 3.1). The array design used in the initial IC design in Chapter 2 was modified based on discussions with the Penn State team.



(a) (b)

Figure 3.1: (a) Proposed integration method for chemoresistive beads. (b) Cross section of opening used for bead integration.



(a) (b)

Figure 3.2: (a) Layout of octagonal shaped array openings for Chip 00 (b) Layout of square shaped array openings for Chip 01

The new array design consists of openings in the top metal (metal 6) and the bottom contact for the beads is designed in metal 5. The array opening shapes were designed to be either an octagon with 2μm sides or a square with 2μm sides which would allow integration of beads with a diameter of 1.5μm. The size of the openings was determined by the process design rule restrictions. The passivation layer (usually present over the top metal layer to provide isolation and protection) was removed over the entire array surface.

The top metal layer was extended on all sides of the array openings to minimize obstruction of the DI water and bead mixture as it passes over the array. To ensure a "channel"-like environment for the solution containing chemoresistive beads to flow through, several copies

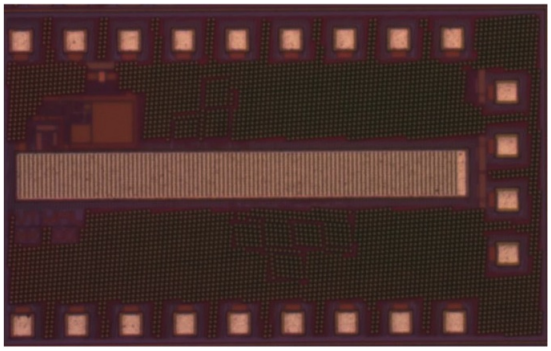
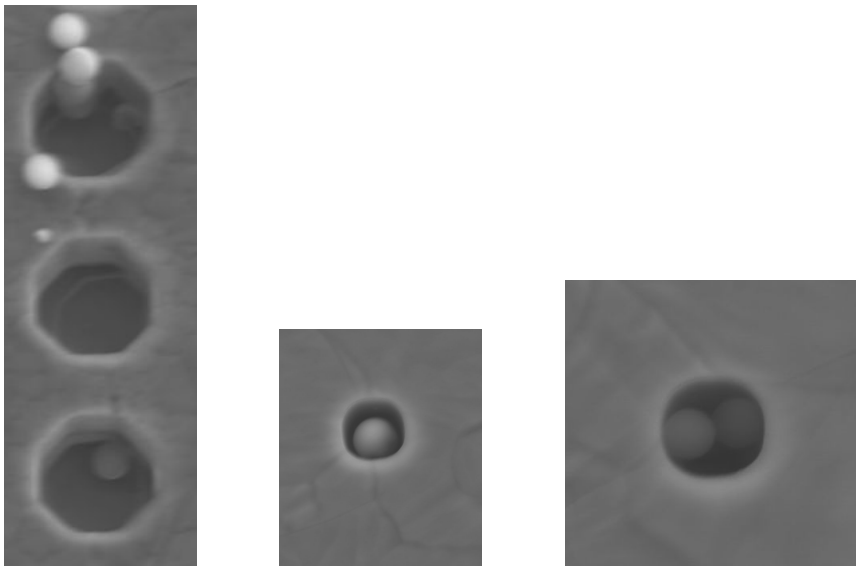


Figure 3.3: "Channel"-like array design for Chemoresistive bead integration

of the array were laid out along the length of the chip (Figure 3.3). Only one of these copies was connected to the addressing circuitry. The remaining copies of the array were unconnected and helped create a smooth flow for the solution containing chemoresistive beads.

Integrating beads by flowing them over the array surface requires accurate control of several parameters such as flow of the liquid, spacing between the array surface and glass cover slip etc. Therefore, a simpler technique was developed to test the operation of the array. Commercially available SiO_2 beads with a diameter of 1.5μm were coated with metal by sputtering 10-20 nm of titanium/gold and were integrated into the array openings as a test case. A few drops of a solution containing the metal coated beads were placed over the array surface and the IC was placed in an ultrasonic bath to provide agitation for 5 minutes. Excess solution was then removed by cleaning the surface of the array with a swab and the array openings were observed using an SEM.

From initial SEM images it was noticed that in some cases, the passivation layer present between metal 6 and metal 5 overlapped with the array opening, presumably due to processing issues. The excess passivation layer over the lower metal pad was removed by performing a pad etch for 7-8 minutes before placing drops of the solution containing metal coated beads on the array. In case of the array variant with octagonal shaped openings, placing a drop of the solution containing beads resulted in the presence of multiple beads in the same ar-



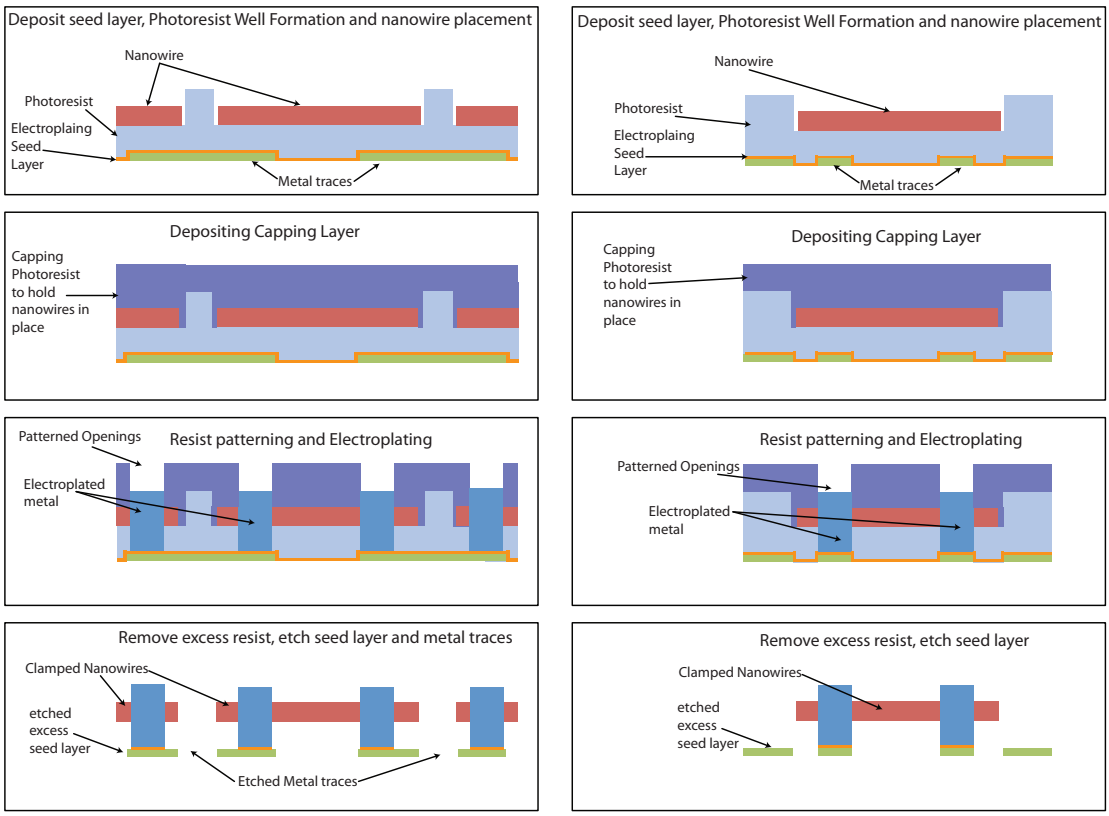
(a) (b) (c)

Figure 3.4: (a) Zoomed in view of Au-coated beads present in array locations for variant 00. (b) SEM of single bead present in variant 01. (c) Two beads present in single location in variant 01.

ray openings (Figure 3.4a) because of the larger array openings (octagonal openings have a diagonal dimension of 4.25μm). The smaller array openings available in the array variant with square openings (with 2μm sides) performed better since the size of the bead is roughly comparable to the size of the array opening Figure 3.4b and 3.4c). However, the small array openings also led to a lower integration rate for the beads.

3.2 Integration of Chemoresistive nanowires

Compared to chemoresistive beads, the integration of chemoresistive nanowires requires a different array design because they require intensive back-end processing (in comparison to chemoresistive beads) to successfully integrate them with two top metal layer pads provided on the array surface at each location. Assembly traces are also provided throughout the array to apply the post-processing voltages required to integrate the nanowires. The nanowires



(a) (b)

Figure 3.5: (a) Process flow for nanowire integration with variant 10. (b) Process flow for nanowire integration with variant 11.

are finally connected to the pads via electroplated posts which ensure good contact between the nanowire and the pads and also provide mechanical support to the nanowire.

The process flows for integrating the nanowires on chips 10 and 11 are shown in Figure 3.5. The first step in the integration process is the deposition of a seed layer for electroplating over the array. A layer of photo-resist is deposited over the IC and wells are patterned over the top metal layer pads by exposing the resist. At each array location, the patterned wells cover both top metal pads and are used to keep the the nanowire in place for further steps. Mask alignment marks are provided on the IC as shown in Figure 3.6. Nanowires are integrated into the patterned photoresist wells at each location using dielectrophoresis as demonstrated by

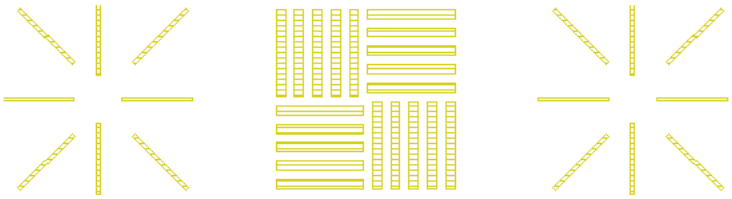


Figure 3.6: Alignment marks used for patterning photo-resist

Narayanan *et.al.* in [43]. Dielectrophoresis is defined as the motion of uncharged, polarizable particles in the presence of a nonuniform electric field. Upon application of an alternating electric field to the assembly traces, the nanostructures suspended in the liquid media are polarized and the dielectrophoretic force directs them towards high field density areas over the pads. If the length of a nanowire is comparable to the gap between the assembly traces, successful assembly of a nanowire at a particular location reduces the electric field between the assembly traces at the location. As a result, the probability of multiple nanowires being integrated into a particular location is minimal. After dielectrophoresis, a capping photo-resist layer is placed over the array to hold the nanowires in place in the photo-resist wells. The capping resist layer is also patterned to expose the regions where electroplated posts should be present (over the top metal layer pads). At each array location, electroplating is used to connect the nanowires to the top metal layer by creating metal posts. In case of variant 10, the electroplating voltage is applied on the assembly traces whereas in case of variant 11, the electroplating voltage is applied to each metal pad using the addressing blocks. The electroplated posts provide electrical connectivity between the nanowire and the Σ-Δ circuit as well as mechanical support to the nanowire. After electroplating is complete, any excess photo-resist and electroplating seed layer is stripped off.

In case of variant 10, the process flow requires an extra step which involves etching sections of the top metal traces to disconnect all the top metal layer pads from each other. The top view of the nanowire integrated array and the array layout for variant 10 is shown in Figure 3.8. Since the pads and assembly traces are designed using the top metal layer, after the post-processing steps, any excess top metal present in the array (which is not a part of the

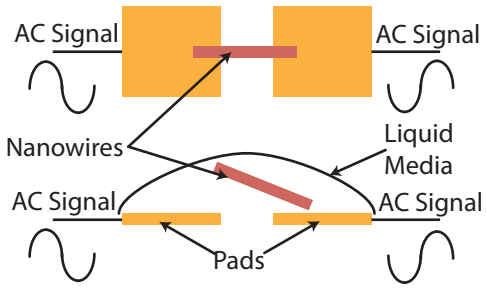


Figure 3.7: Dielectrophoretic assembly

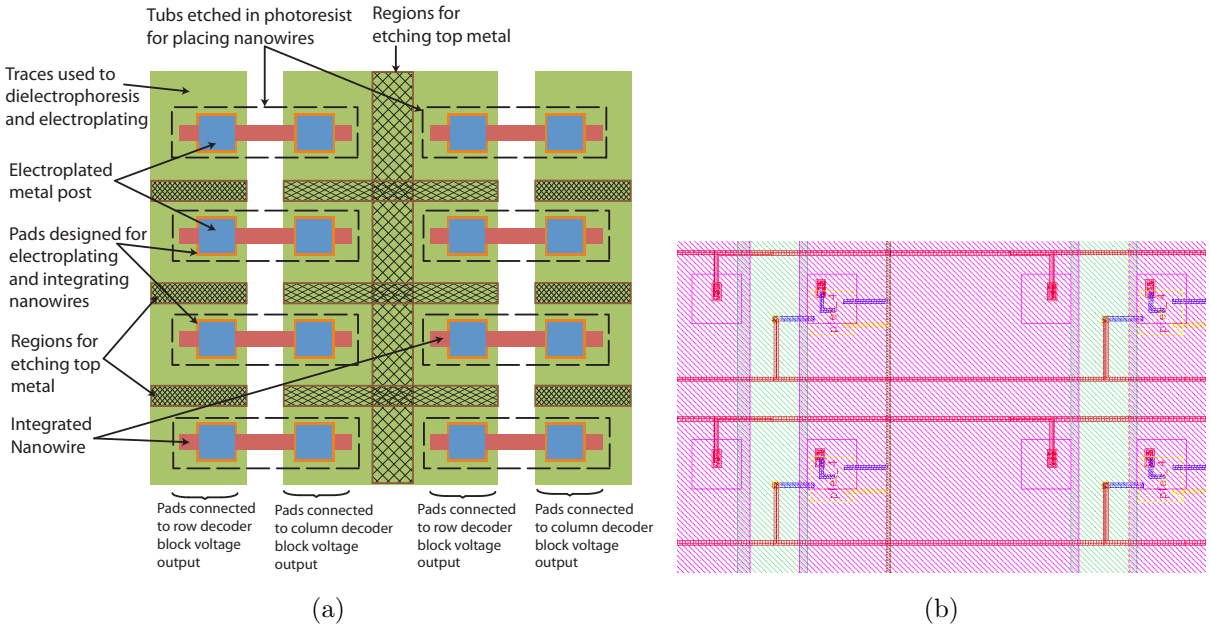


Figure 3.8: (a) Design of array for variant 10. (b) Layout.

pads at an array location) needs to be removed. The cross-hatched regions in Figure 3.8a represent the top metal layer regions which is to be etched. The main drawback of using this approach is the extensive etching of the top metal layer required after the post processing steps. During the etching process any traces below the top metal layer in the array or the top metal layer pads may be damaged which can degrade the circuit operation or yield.

In case of variant 11, the pads for integrating nanowires were separated from the assembly traces by design such that no top metal traces needed etching. Thus, the traces used for applying the dielectrophoresis voltage signal are separate from the top metal pads where the

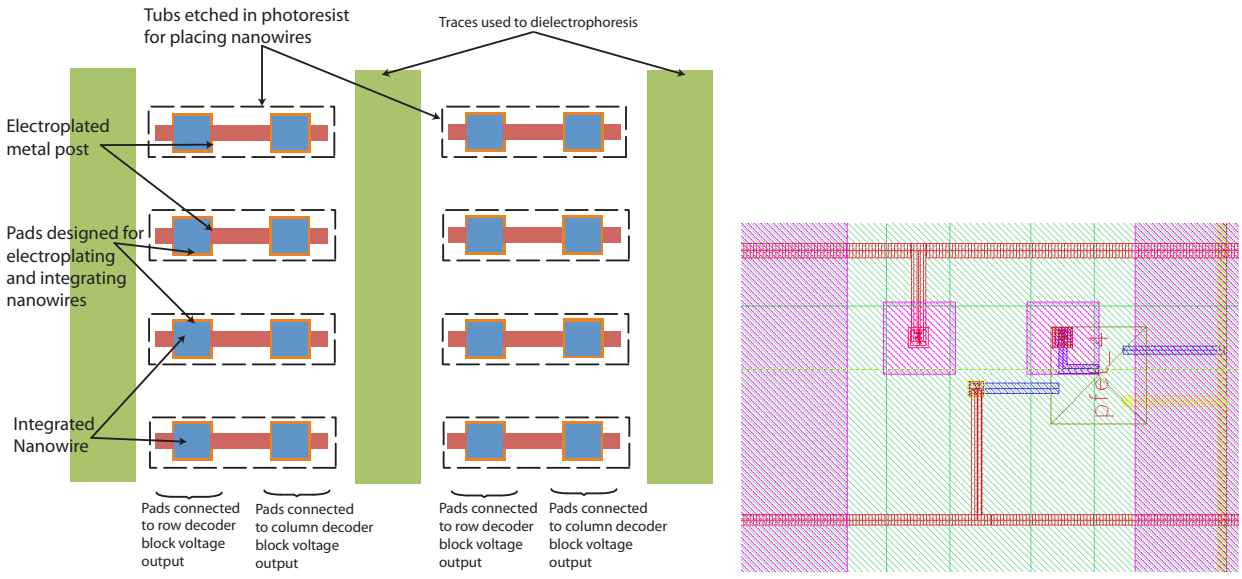


Figure 3.9: (a) Design of array for variant 11. (b) Layout.

electroplating voltage is applied (refer Figure 3.9). As a result, the array was designed such that the electroplating voltage could be applied to the pads via the addressing blocks to all the array locations at once. Thus, the addressing blocks were modified such that when the enable input on the addressing blocks was turned off all access transistors present in the array turn on and the electroplating voltage is applied directly to the pads.

The fabricated chips were transferred to Penn State for the post-process nano-wire assembly. No measurement results are available for the nanowires since no assembled chips were available from Penn State at the time of this writing.

3.3 Summary

This chapter has provided an in depth discussion of the integration techniques used to heterogeneously integrate chemoresistive beads and nanowires with the array designs developed in this thesis. The proposed method for integrating chemoresistive beads by flowing them

over the array surface was discussed. The array design required to integrate beads using the proposed method was also presented. A simplified bead assembly approach was also developed. This consisted of placing a drop of the solution containing metal coated beads over the surface of the array and agitating the IC by placing it in an ultrasonic bath. Finally, the array layouts for variants based on chemoresistive nanowires (variant 10 and 11) were described. The process flow used to integrate chemoresistive nanowires onto the array locations is also described for each of these design variants. The following chapter presents the design improvements as well as the measurement results for the modified readout circuitry used in the new prototype IC.

Chapter 4

Sigma Delta Modulator Design with low power voltage reference and modified addressing scheme

The $\Sigma\Delta$ readout circuit presented in Chapter 2 demonstrated a wide resistance measurement range and operation of the direct addressing scheme for a 4x4 array. However, the power consumption and the addressing scheme of the design need to be improved. The power consumption of the design (3mW) is high for applications such as wireless sensor nodes which require low power operation. The power consumed by the resistive divider circuit used to generate the $V_{DD}/2$ reference voltage for the comparator was determined to be $\sim$1.5mW. To lower this power consumption, an alternative low power bandgap voltage source can be designed to provide the reference voltage for the comparator.

As the array size is increased from 4x4 to 16x16, the direct addressing scheme used in the previous design needs to be modified. In this chapter, a row-column based addressing scheme for the 16x16 array design is presented. The modified addressing design uses an 8-bit input address to select a particular location on the array. Since the post-processing steps required to integrate chemoresistive beads and nanowires into the surface of the array are different, the

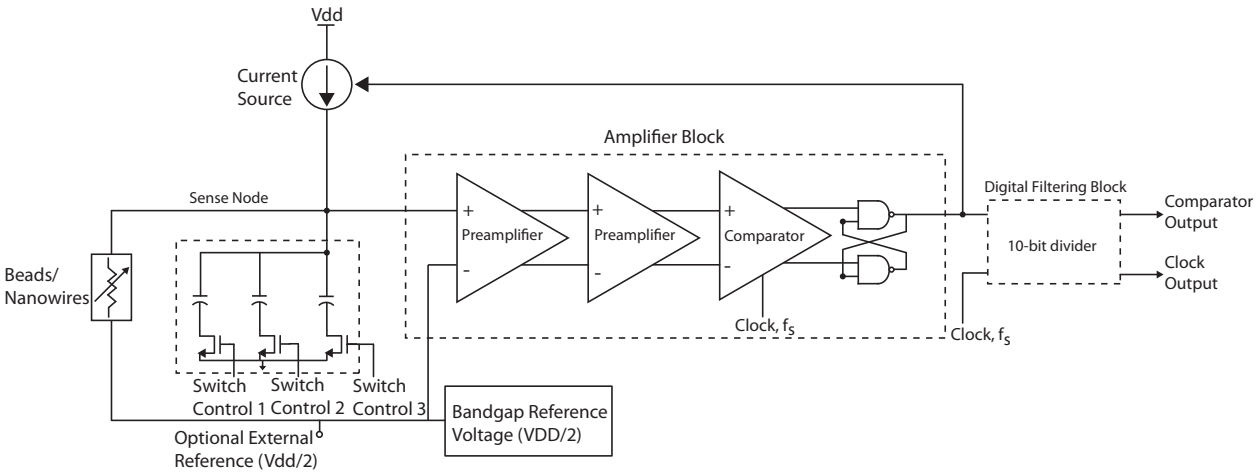
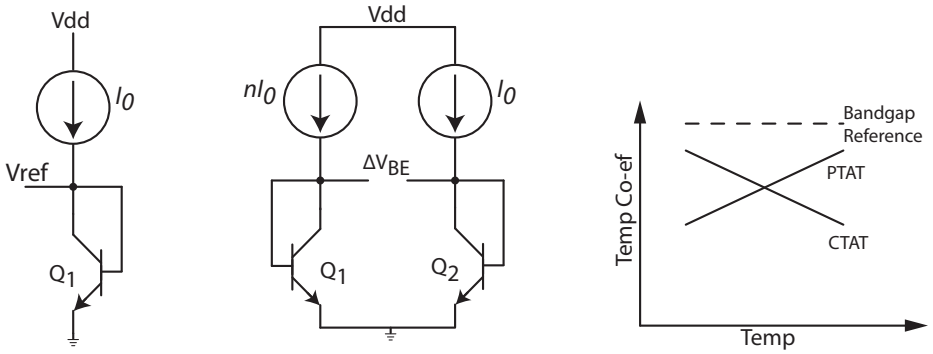


Figure 4.1: Modified block diagram for sigma delta modulator.

addressing circuitry for each array was designed based on the type of sensor to be integrated with the array. Finally, an extra capacitor was added on the integrator block of the $\Sigma\Delta$ modulator in order to increase the resistance measurement range. Figure 4.1 demonstrates the modified block diagram for the $\Sigma\Delta$ modulator presented in this chapter. The design of the bandgap voltage reference, new array addressing scheme and modifications to the integrator block are discussed in the following sections.

4.1 Bandgap Voltage Reference

Ideal voltage references generate a fixed voltage, V_{REF}, which is independent of power supply, temperature or process variations. However, realistic voltage references are non-ideal and are therefore dependent on temperature and other variations. These references can be classified as either *PTAT* (where voltage is directly proportional to absolute temperature) or *CTAT* (where voltage is inversely proportional to absolute temperature). For example, the difference between base-emitter voltages of two bipolar transistors which operate at unequal current densities is an example of a PTAT reference [59]. On the other hand, the base-emitter voltage of a bipolar transistor or the forward voltage of a pn-junction diode are examples of CTAT



(a) (b) (c)

Figure 4.2: (a) Schematic for CTAT voltage reference. (b) Schematic for PTAT voltage reference. (c) Temperature co-efficients of PTAT, CTAT and bandgap references vs temperature.

references [59].

The output voltage for the CTAT reference circuit in Figure 4.2a is simply the base-emitter voltage of the BJT as given by

$$V_{BE} = V_T \frac{I_C}{I_S} \tag{4.1}$$

where, V_T is the thermal voltage (kT/q), I_C is the collector current and I_S is the saturation current for the BJT.

The output voltage for a PTAT circuit (Figure 4.2b) can be written as,

$$\begin{aligned} \Delta V_{BE} &= V_{BE1} - V_{BE2} \\ &= V_T \ln \frac{N.I_0}{I_{S1}} - V_T \ln \frac{I_0}{I_{S2}} \end{aligned} \tag{4.2}$$

For identical Q_1 and Q_2, I_{S1}=I_{S2}, and equation 4.2 can be written as

$$\Delta V_{BE} = V_T \ln N \tag{4.3}$$

The opposing responses of PTAT and CTAT voltage references (Figure 4.2) can be used to design voltage references which are independent of temperature variation. These temperature

independent references are known as bandgap voltage references and their output voltage can be written as,

$$V_{REF} = \alpha_1 V_{BE} + \alpha_2 (V_T \ln N) \tag{4.4}$$

where, V_{BE} represents the CTAT component (as seen in equation 4.1) and $V_T \ln N$ is the PTAT component (as seen in equation 4.3). α_1 and α_2 are coefficients for CTAT and PTAT components whose values are selected such that V_{REF} is independent of temperature. By selecting the appropriate values for α_1 and α_2, equation 4.4 can also be rewritten as [59],

$$V_{REF} = \frac{E_g}{q} + (4 + m) V_T \tag{4.5}$$

where E_g/q is the bandgap voltage of silicon, m is the temperature exponent of mobility ($\mu \propto \mu_0 T^m$) and V_T is the thermal voltage. V_{REF} is referred to as the bandgap voltage because as $T \to 0$, $V_{REF} \to E_g/q$ or the bandgap voltage for silicon.

The design of the bandgap voltage reference used in this thesis is presented in the following sections. Schematics and simulation results for the various design blocks used in the bandgap voltage reference circuit.

4.1.1 Bandgap Voltage Reference Design

The bandgap reference design presented in the thesis is based on the bandgap reference design presented by K.N Leung *et. al.* in [60]. The design of the bandgap voltage circuit used in the modified IC design is presented in Figure 4.3. The design uses vertical PNP transistors provided in the design kit. The PNP transistor is formed using a p+ emitter, N well base and p-substrate collector.

Nodes 1 and 2 in Figure 4.3 are forced to be at the same voltage (since they are inputs to the op amp). The resistors $R_{2A1} = R_{2B1}$ and $R_{2A2} = R_{2B2}$ which forces the nodes 3 and 4 to the same voltage. The loop formed by Q_1, Q_2, R_1, R_{2A1}, R_{2B1}, R_{2A2} and R_{2B2} generates a current I given as,

$$I = \frac{V_{EB2}}{R_2} + \frac{V_T \ln N}{R_1} \tag{4.6}$$

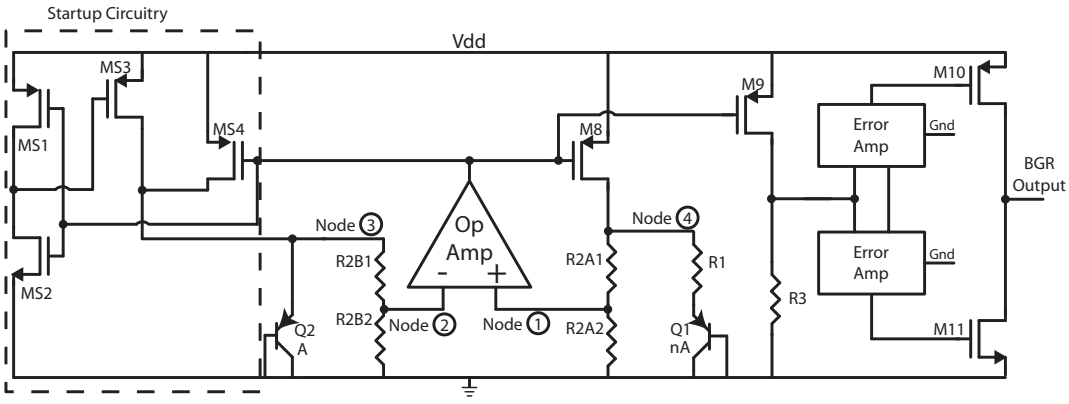


Figure 4.3: Bandgap voltage reference.

where N is the ratio of the emitter areas for Q_2 and Q_1, V_T is the thermal voltage and R_2=R_{2A1}+R_{2A2}=R_{2B1}+R_{2B2}.

M_{S4}, M_8 and M_9 form a current mirror and inject the current I into resistor R_3. The voltage drop across R_3 represents the output of the bandgap reference circuit and is written as,

$$V_{ref} = \frac{R_3}{R_2}\left[V_{EB2} + \left(\frac{R_2}{R_1}\ln N\right)V_T\right] \tag{4.7}$$

If the initial voltages at nodes 1 and 2 are zero, then the differential input for the op-amp turns off. Thus, a startup circuit is required to ensure that the op-amp turns on when V_{DD} is applied. In this design, the startup circuit consists of M_{S1}-M_{S4} as seen in Figure 4.3. The output of M_{S1} and M_{S2} (which form an inverter) is used as the input to the gate of PMOS transistor M_{S3} which drives the current into R_{2B1}, R_{2B2} and Q_1 allowing the op-amp to start operation. As the amplifier output increases, M_{S4} turns off and M_{S3} remains turned on allowing the op-amp input to remain above zero.

The op-amp circuit design is a simple single stage differential op-amp (Figure 4.4). The differential input pair consists of transistors M1 and M2, and M3 is used as the tail current source. M4 and M5 form a current source load for the differential pair. The frequency and phase response of the op-amp are provided in Figure 4.5. The transistor sizes were determined based on simulation of the bandgap reference circuit. Using simulations, the

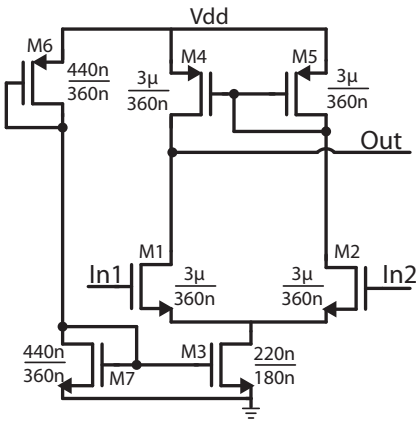


Figure 4.4: Schematic for op amp used in bandgap reference voltage.

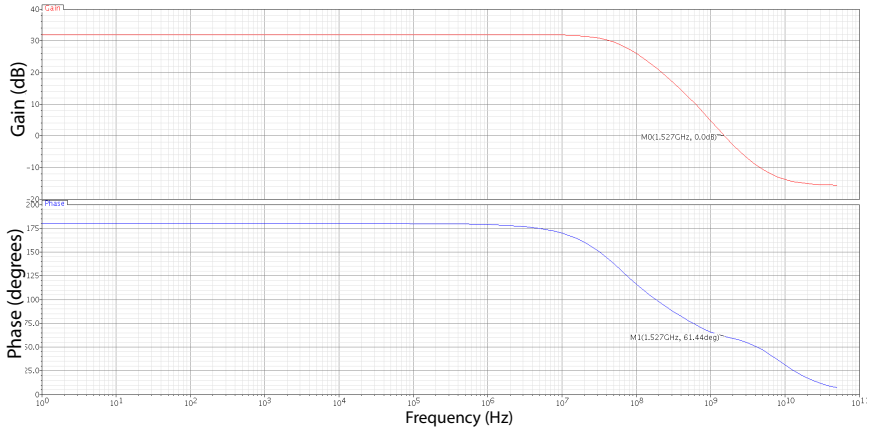


Figure 4.5: Gain and phase of op amp core in bandgap voltage reference.

passband gain of the op-amp was measured to be 32dB with a unity-gain bandwidth of $\sim$ 1.5 GHz. The simulated results show that the phase margin of the design is 61 degrees, which implies that the design is stable.

Ideally, the resistances which control the temperature coefficient in the design are trimmed to obtain the best temperature coefficient possible. In this design however, no extra resistors for trimming were added and the resistance values used were selected based on simulations to provide a reference voltage of 900mV at 25°C. The temperature co-efficient for the design is calculated by measuring the DC output voltage of the circuit over temperature and using

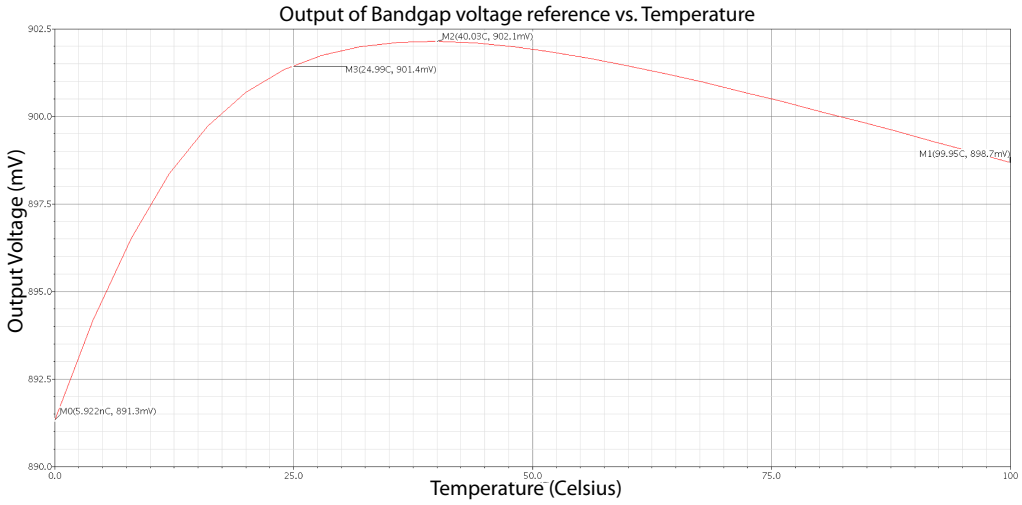


Figure 4.6: Variation of bandgap voltage reference output with respect to temperature.

the following equation,

$$TC = \left[\frac{V_{MAX} - V_{MIN}}{V_{nominal} \times (T_{MAX} - T_{MIN})}\right] \times 10^6 \tag{4.8}$$

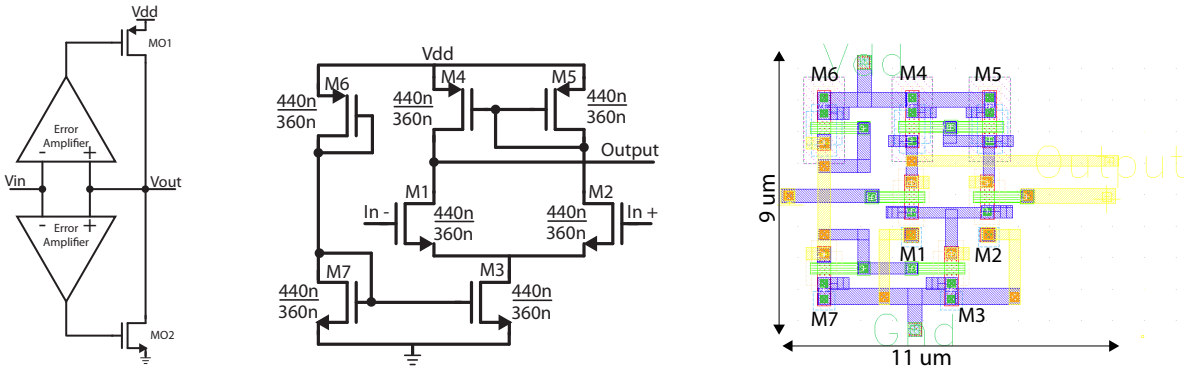
where V_{MAX} and V_{MIN} are the maximum and minimum output voltages respectively, $V_{nominal}$ is the output voltage at 25°C and T_{MAX} and T_{MIN} are the maximum and minimum temperatures, respectively.

After simulating the output voltage of the circuit with respect to temperature (Figure 4.6), the equation 4.8 can be written as

$$TC = \left[\frac{902.1mV - 891mV}{901.5mV \times (100 - 0)}\right] \times 10^6 \tag{4.9}$$

Thus, the temperature coefficient is determined to be *122 ppm*.

To allow the voltage reference to drive low resistance loads, error amplifiers were added at its output to reduce the output resistance of the design as suggested in [56]. Error amplifiers allow the size of the output stage of the reference to remain small while reducing the output resistance. The error amplifiers sample the output and input voltages and apply a negative shunt feedback to the gates of the common source transistors, MO1 and MO2 (Figure 4.7a). The error amplifiers are designed to turn on either MO1 or MO2 to avoid crossover distortion



(a) (b) (c)

Figure 4.7: (a) Use of error amplifiers to decrease R_{out}. (b) Schematic and (c) layout of an error amplifier.

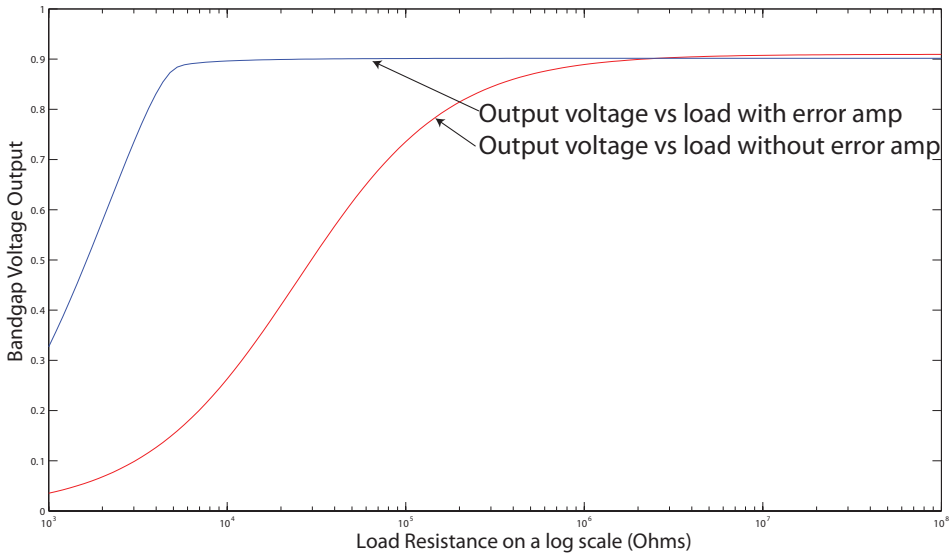


Figure 4.8: Output voltage of bandgap voltage reference with and without error amplifiers

and maximize efficiency.

The error amplifier used in this design was similar to the op-amp stage used in the bandgap reference circuitry (Figure 4.7b). M1 and M2 form the differential input to the amplifier and M4, M5 form the current source load. M3 acts as the tail current source. The bandgap voltage reference can source its output voltage for lower load resistances when the error

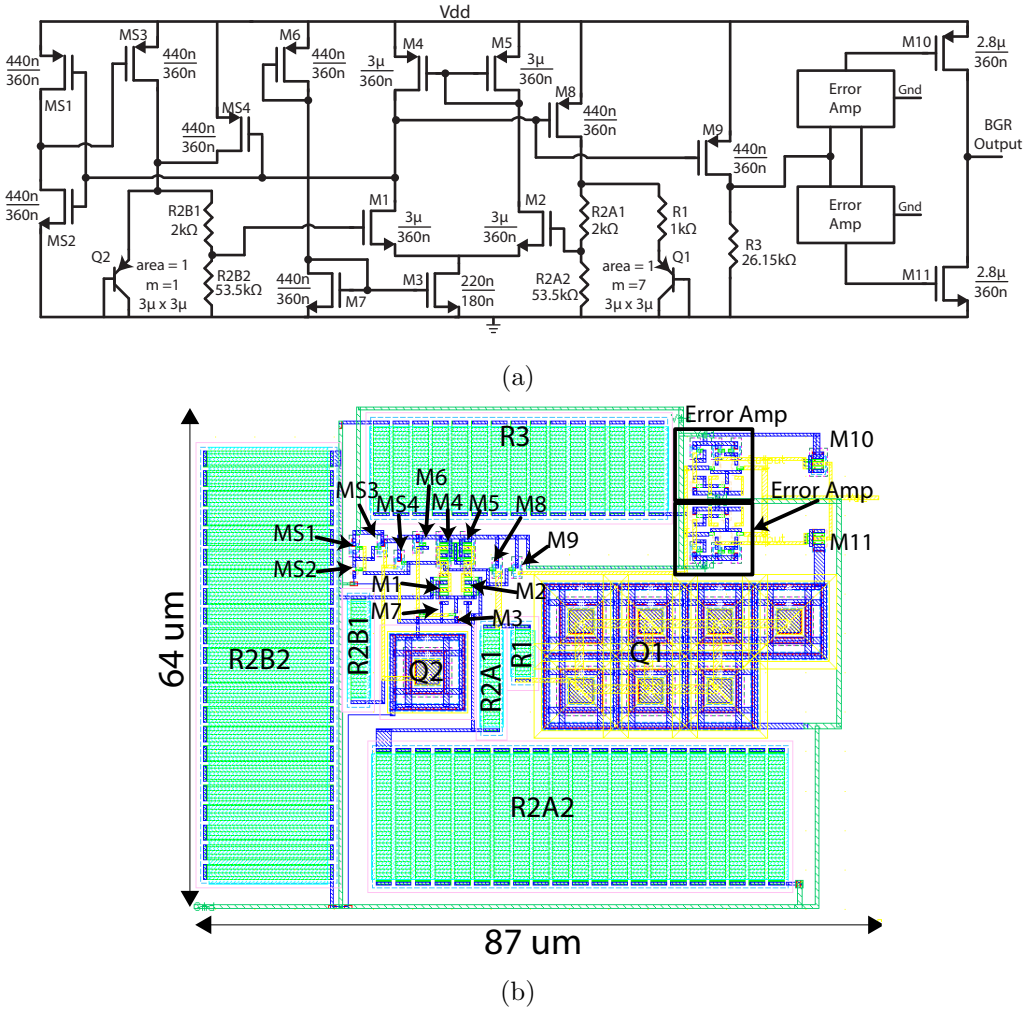
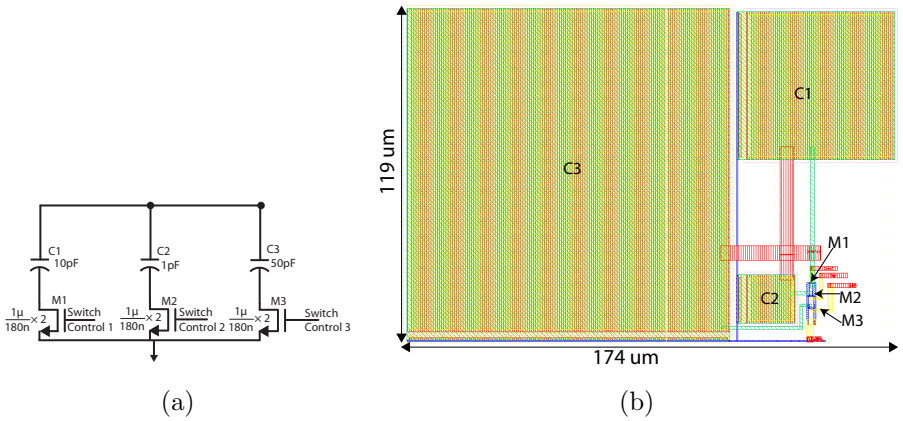


Figure 4.9: (a) Schematic and (b) layout for bandgap voltage reference.

amplifiers are connected at the output of the circuit (Figure 4.8). In the figure, the output voltage of the bandgap circuit is measured for a wide range of load resistances with and without any error amplifiers connected to the output of the bandgap circuit. When no error amplifiers are connected, the bandgap voltage reference output reaches its nominal value of 900mV for load resistances greater than 5MΩ; and if error amplifiers are used, the output voltage reaches its nominal value for resistances which are approximately 5kΩ.

The complete bandgap reference circuit schematic and layout are provided in Figure 4.9. The DC current flowing into the design was simulated to be 270μA, thus the power dissipation



(a) (b)

Figure 4.10: (a) Schematic and (b) layout for modified integrating capacitor block.

of the voltage reference was 486μW. The area of the design was 87μm x 64μm.

4.2 Modified Integrator Block

In order to lower the value of the lowest measurable resistance, another switched capacitor was included in the integrating capacitor block (Figure 4.10). In simulations, the lowest measurable resistance could be reduced from 2kΩ to 200Ω for a 50MHz clock input and a 50pF capacitor. Thus, an extra 50pF capacitance was added in the integrator block. The simulated resistance measurement range is provided in Figure 4.11. The simulated results also show that the use of a bandgap voltage reference has minimal impact on the measurement range of the design.

4.3 Addressing Block

In order to enable a larger chemoresistor array, the addressing scheme was modeled on the row-column scheme used in memory circuits. Memory circuit arrays use decoders to select a particular row (or column) from 2^N possible selections based on a N bit input. This design

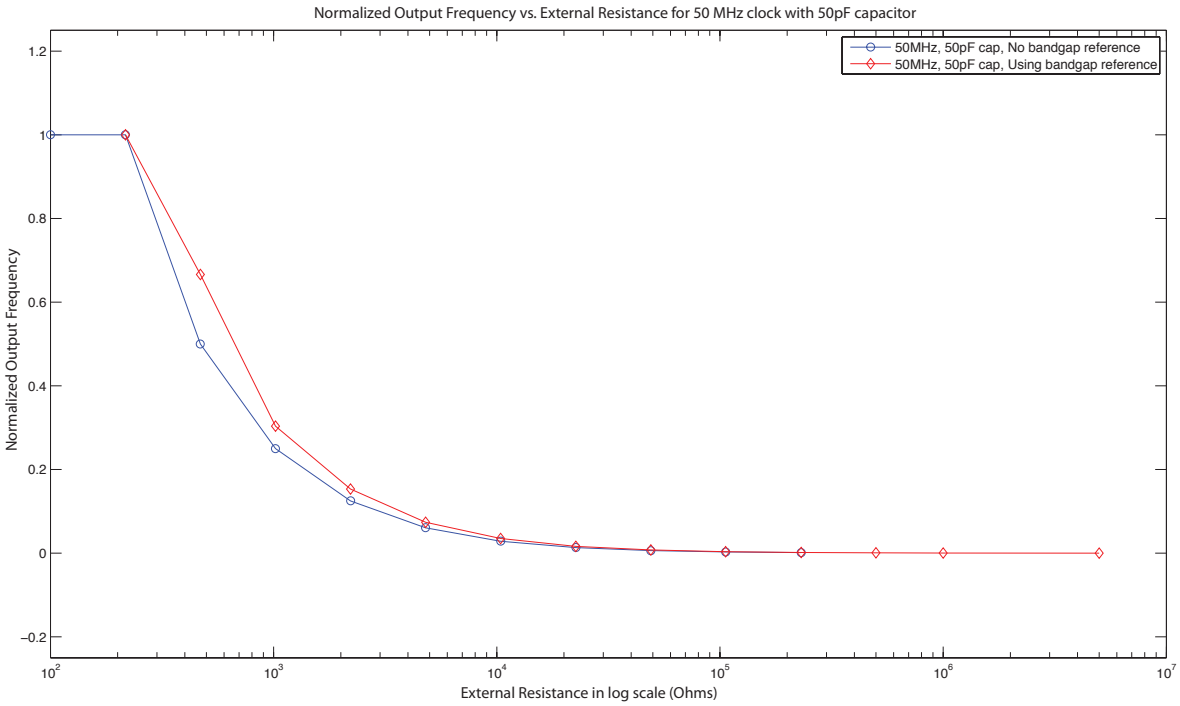
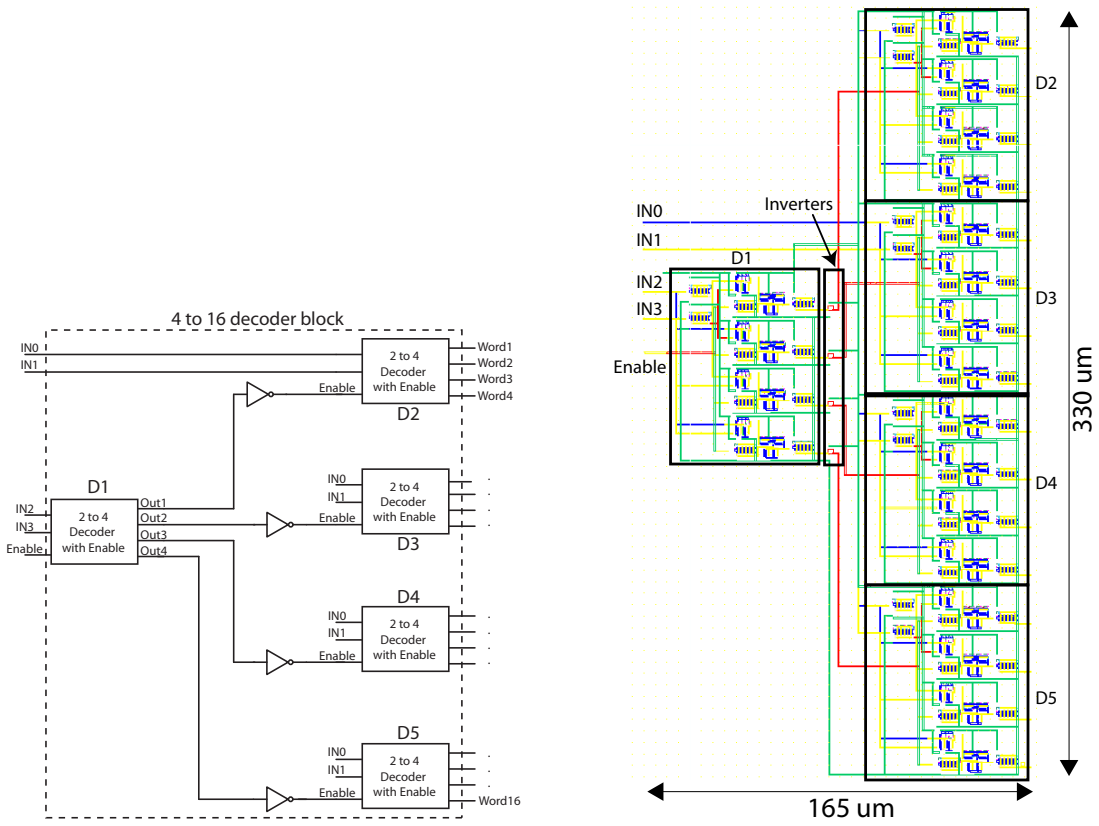


Figure 4.11: Normalized output frequency vs. resistance for 50pF cap with 50MHz clock.

is simple and scalable for large array dimensions as compared to a direct addressing scheme utilized in the previous design. The designed prototype tile contains four variants of the array design (as shown in Chapter 3) where two arrays are used with chemoresistive beads and the remaining variants are used with chemoresistive nanowires. The design variants which require chemoresistive beads for sensing use the same row and column addressing circuit design since the only difference between the variants is the shape of the openings at each array location. The design variants based on chemoresistive nanowires for sensing use different row and column addressing circuits since the process flow used to integrate the nanowires is different for each variant.

In all design variants, a 8 bit addressing input ($A_7A_6A_5A_4A_3A_2A_1A_0$) is used to select a particular location in the array. The bits A_7 to A_4 determine the selected row and A_3 to A_0 select a particular column. The selected array location corresponds to the array position located at the intersection of the selected row and column. In order to select a single row or

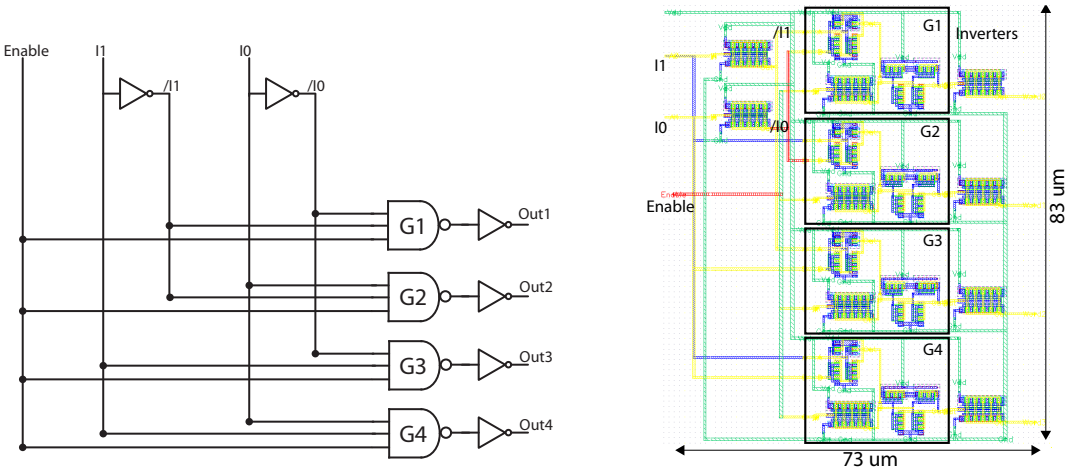


(a) (b)

Figure 4.12: (a) Schematic and (b) layout for 4 to 16 decoder.

column from 16 possible options, a 4 to 16 decoder was used. PMOS access transistors were placed at each array location and access transistor is controlled by the output of the decoder. A PMOS access transistor was used since the voltage at each array location will only vary between VDD/2 and VDD (minimum and maximum voltages for the Vsense node).

Since PMOS access transistors were used, the decoders were designed to generate an active low output such that the selected decoder output is a digital low (ground) whereas the unselected outputs are set to digital high (VDD). An enable input was also provided to control the operation of the decoder. When the enable input is low, all decoder outputs are high independent of the addressing input. When the enable input is high and an addressing input is provided, the selected decoder output is set to ground whereas remaining decoder



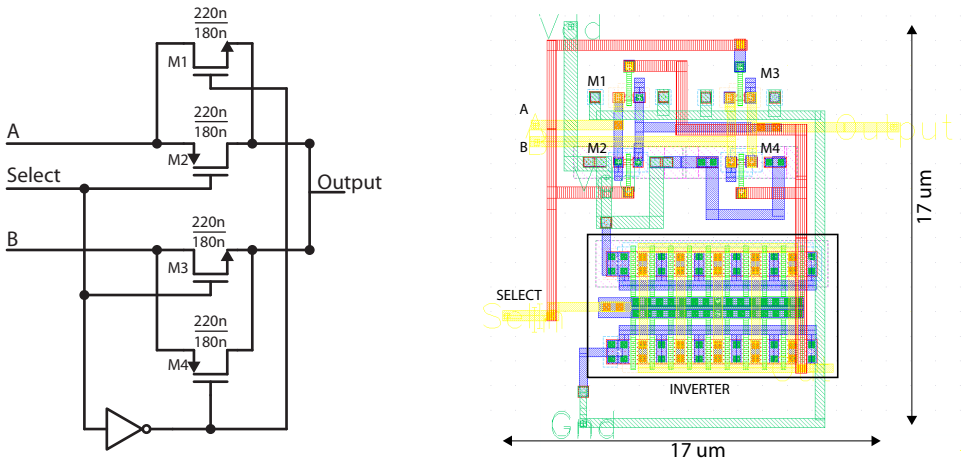
(a) (b)

Figure 4.13: (a) Schematic and (b) layout for 2 to 4 decoder block.

outputs are set to VDD.

The 4 to 16 decoder was built using multiple 2 to 4 decoders which are connected as shown in Figure 4.12. This design requires five 2 to 4 decoders which are connected such that for any given input only one 2 to 4 decoder is enabled. The addressing bits IN3 and IN2 determine which 2 to 4 decoder among D2, D3, D4 and D5 turns on, and addressing bits IN1 and IN0 determine which output is selected in the particular decoder. The inverters at the output of D1 convert the active low decoder output into active high values so that it can be used as enable inputs for the remaining 2 to 4 decoders. The 2 to 4 decoders (Figure 4.13) were built by connecting the two decoder inputs (I_1 and I_0) and the enable input to a 3 input AND gate (3 input NAND and a NOT gate in series). When the enable signal is low, the output of all AND gates is set high, whereas if the enable is high, the output value depends on the input bits.

In the addressing block design presented here the voltage applied at each column is determined based on the decoder output. In order to select between different input voltages based on the decoder output, a 2 x 1 multiplexer was used. The multiplexer design was based on transmission gate architecture (Figure 4.14) since the voltage at the comparator block input



(a) (b)

Figure 4.14: (a) Schematic and (b) layout for 2 to 1 multiplexer.

(V_{sense} node) is analog in nature and was one of the multiplexer inputs. Multiplexer designs based on inverters and NAND gates were unable to pass analog signal to the output without converting it to a digital high or low, thus were not feasible for this application. Depending on the value of the select input, one of the transmission gates turns on to connect the corresponding input to the output of the multiplexer.

4.3.1 Addressing block design for chemoresistive beads

A block diagram for the addressing scheme for chemoresistive sensor beads is presented in Figure 4.15. A row decoder output is selected based on the input addressing bits and all access transistors connected to selected output are turned on. The column addressing bits select a particular column and the column access transistor is turned on. Based on the output of the column decoder, the 2 x 1 multiplexers present at each output determine an input voltage for the columns. If the access transistor is turned on, the sense node voltage is applied throughout the entire column. For unselected decoder outputs, the input voltage to the column access transistor is set to $V_{DD}/2$ which is redundant since column access transistors connected to unselected decoder outputs are turned off. Therefore, at

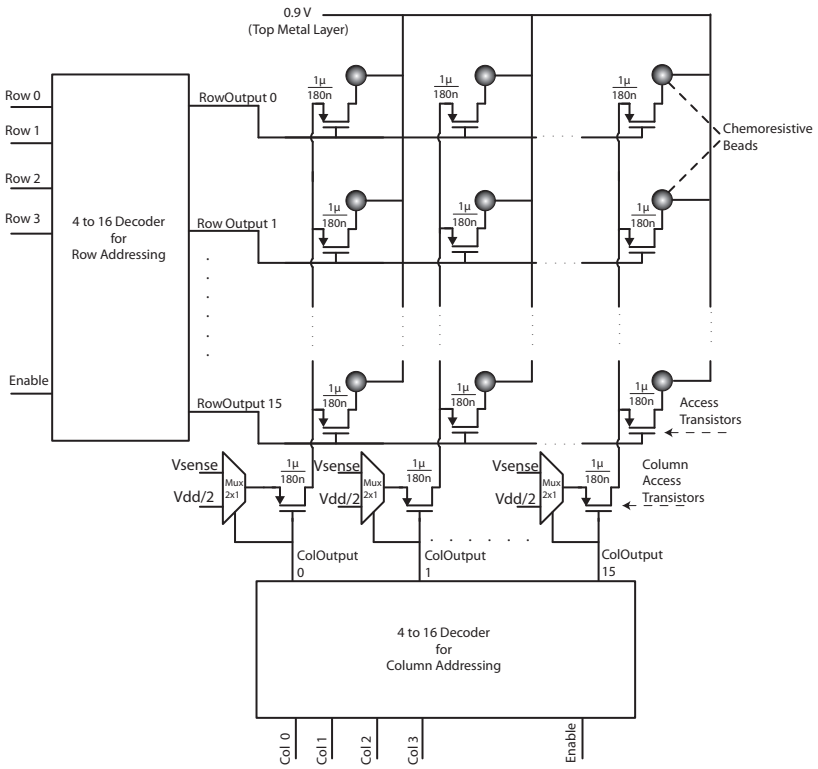


Figure 4.15: Block diagram of array addressing scheme for chemoresistive beads.

a selected location, the row decoder output turns on the access transistor at the location and the selected column decoder output determines the voltage applied at one end of the chemoresistive sensor. The other end of the sensor is connected to a voltage source which provides a voltage of $V_{DD}/2$ using either the bandgap reference voltage source or an external voltage source.

4.3.2 Addressing block design for chemoresistive nanowires

As presented in Chapter 3, the chemoresistive nanowire arrays for both design variants (variants 10 and 11) were implemented with two metal pads at each of the 16x16 array locations. The addressing blocks for the nanowire sensor based variants required modifications for each case due to the different post processing steps required for integrating nanowires in each of

the design variants. The main difference between the two designs is the different voltages required during the nanowire post-processing steps.

In both designs the resistance of the nanowire after assembly is measured by connecting one end of the nanowire to the V_{sense} node and the other end is connected to $V_{DD}/2$. This is done by connecting one of the pads at each array location in a row to the output of a 2 to 1 multiplexer whose select input is controlled by the output of the row decoder. Access transistors controlled by the outputs of the row decoder are present under the second pad (connected to $V_{DD}/2$) at each array location. When a particular output of the row decoder is selected, all access transistors connected to the selected row output turn on and the voltage present at each column trace is applied to the pad. The output of the column decoder is used to control the column access transistors. The column detector output is also connected to the select input of a column multiplexer which is used to select between different input voltages for a column based on the decoder output. When a column is selected, the column access transistors turn on and the selected multiplexer input is applied to the column trace.

As discussed in Chapter 3, for design variant 10 the array is designed such that the assembly and electroplating voltages are applied via assembly traces which connect all pads along a column. The assembly traces are connected to a pad on the IC and when the voltages are applied, the addressing circuit is turned off by setting the enable input to 0. For this design variant, the assembly traces are etched after the nanowires are integrated leaving only top metal layer pads at each location. As a result, the array and addressing circuit are connected as shown in Figure 4.16 and no assembly traces are shown in the figure. The row and column components each consist of a 4 to 16 decoder and 16 multiplexers to select the input voltages applied to the metal pads in each array location. When the enable inputs to the decoders are low, all decoder outputs are high which turns off access transistors at each location as well as column access transistors. When the enable input is high and an array location is selected, the row and column decoder outputs select an input voltage for the row and column multiplexers. For a selected row decoder output , the Vsense node is selected at the multiplexer. For unselected outputs of the row decoder, the $V_{DD}/2$ voltage is selected

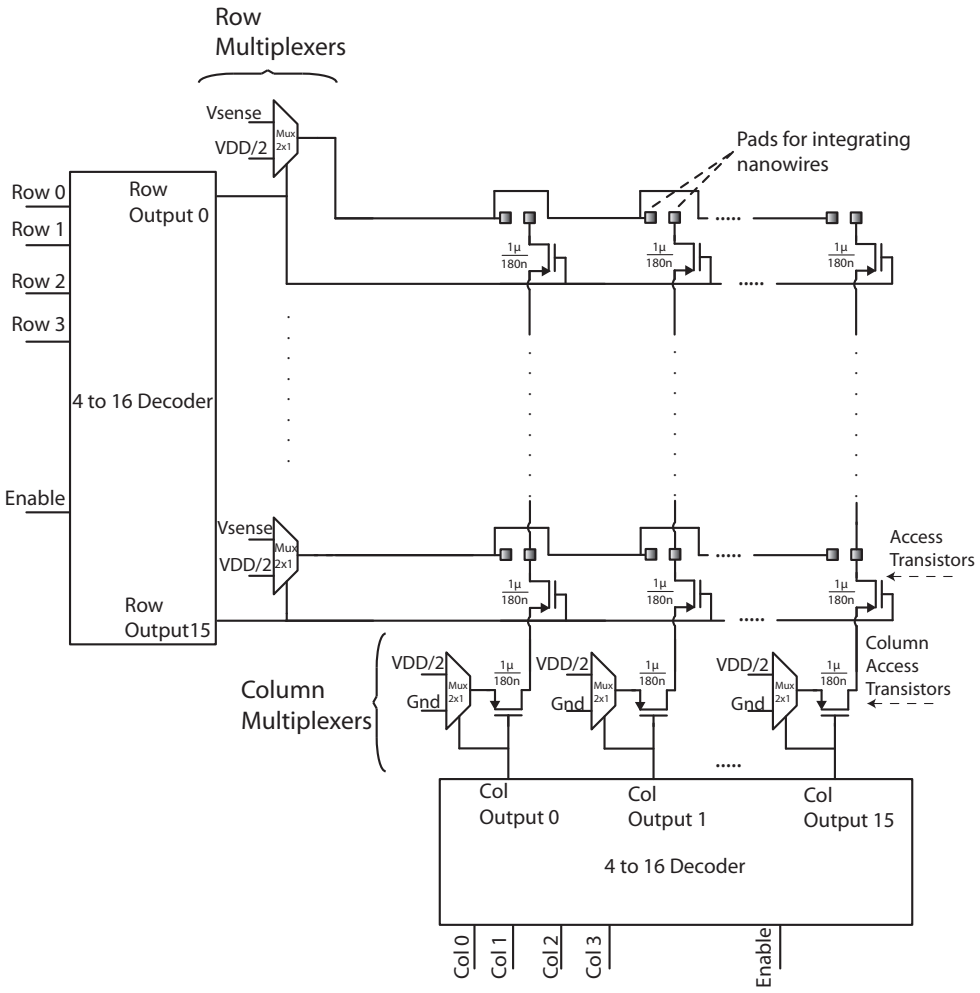


Figure 4.16: Block diagram of the addressing scheme for chemoresistive nanowires in design variant 10.

at the multiplexer inputs. Similarly, when a column decoder output is selected, the $V_{DD}/2$ voltage input of a column multiplexer is applied to the column trace. For unselected outputs of the column decoder, the ground voltage input of the multiplexer is selected. Thus, at the selected array location, the pad connected to the row multiplexer output is connected to the V_{sense} voltage and the second pad (connected to the array location access transistor) is connected to $V_{DD}/2$ voltage present along the column trace. At all other locations, either the access transistors at each array location or the column access transistor is turned off. As a result, no resistance changes can be measured at the unselected locations.

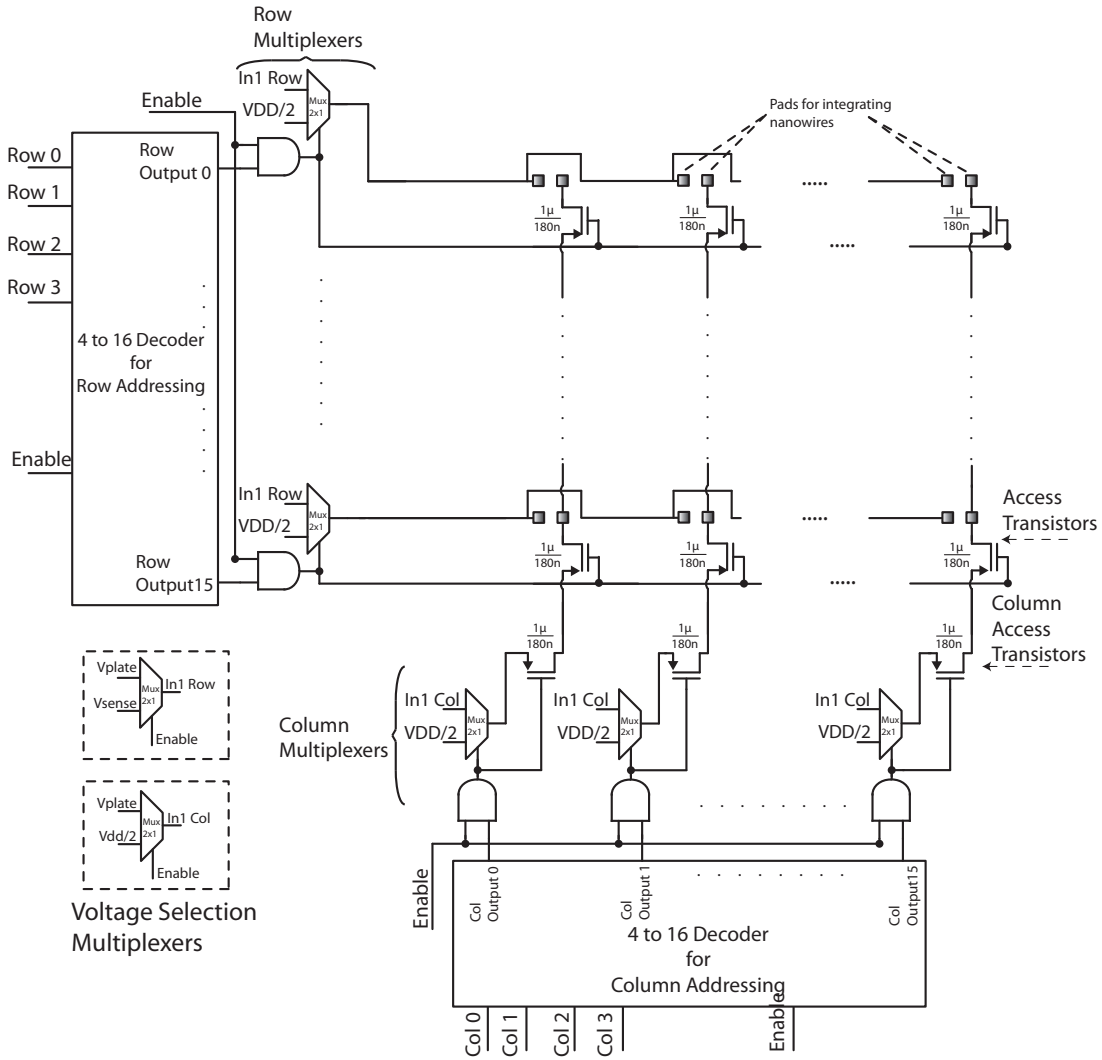
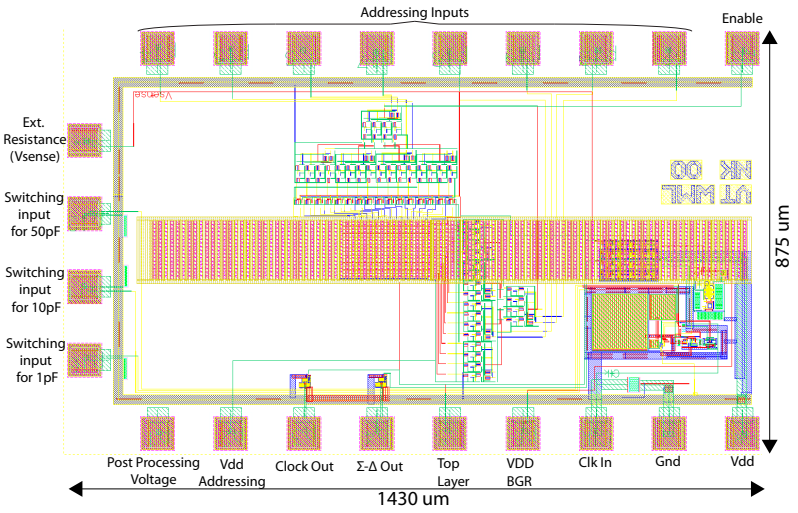


Figure 4.17: Block diagram of the addressing scheme for chemoresistive nanowires in design variant 11.

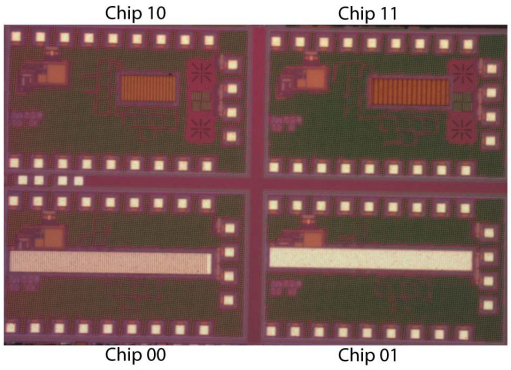
For design variant 11, during post processing steps for integrating nanowires the electroplating voltage is passed through the addressing blocks along with the V_{sense} and $V_{DD}/2$ voltages required for resistance measurement. As presented in Chapter 3, the assembly traces provided on the array are used to apply the voltage required for dielectrophoresis. The modified addressing block without the assembly traces is shown in Figure 4.17. In this design, the outputs of the 4 to 16 column and row decoders as well as the enable input signals are used

as inputs for logical AND gates. The output of the AND gate is used as the select input for the voltage selection multiplexers (present at the row and column decoder outputs). The output of the AND gate also controls the column access transistors as well as the access transistors present at each array location. The electroplating voltage required to build the electroplated posts at the top metal layer pads is applied to all array locations as once using the addressing blocks.

To turn on all access transistors (array location access transistors as well as column access transistors), a logical AND operation is performed using the output of the row and column decoders as well as the enable signal. During any post-processing steps, the enable is low which selects the electroplating voltage (V_plate) at the row and column voltage selection multiplexers. When the enable is low, the output of the AND gates present at the row and column decoder outputs is also low. Thus, the output of the voltage selection multiplexers (which corresponds to the electroplating voltage, V_{plate}) is applied to each pad in the array. When the enable is high and a particular row is selected, all array location access transistors connected to the selected row decoder output are turned on and V_{sense} is applied to all pads connected to the output of the row multiplexer. For unselected rows, the pads connected to the output of the row decoder multiplexer are connected to a voltage of $V_{DD}/2$ and all array location access transistors are turned off. When enable is high and a particular column is selected, the column access transistor turns on and $V_{DD}/2$ is applied to the entire column trace. Therefore, at the selected array location, the pad connected to the access transistor has a voltage of $V_{DD}/2$. The column access transistors for any unselected columns are turned off. At unselected array locations, the resistance change of chemoresistive nanowires is not measured since the voltage drop across the sensor is never V_{sense} - $V_{DD}/2$.



(a)



(b)

Figure 4.18: (a) Layout for design variant 00. (b) Fabricated prototype IC for modified design.

4.4 Results

The Jazz semiconductor CA18HR 0.18μm CMOS technology was used for this design iteration. The layout for design variant 00 is presented in Figure 4.18a and the fabricated prototype IC is shown in Figure 4.18b.

In Figure 4.18, the array openings are present along the length of the IC. This allows the formation of a "channel" through which a solution containing chemoresistive beads can be

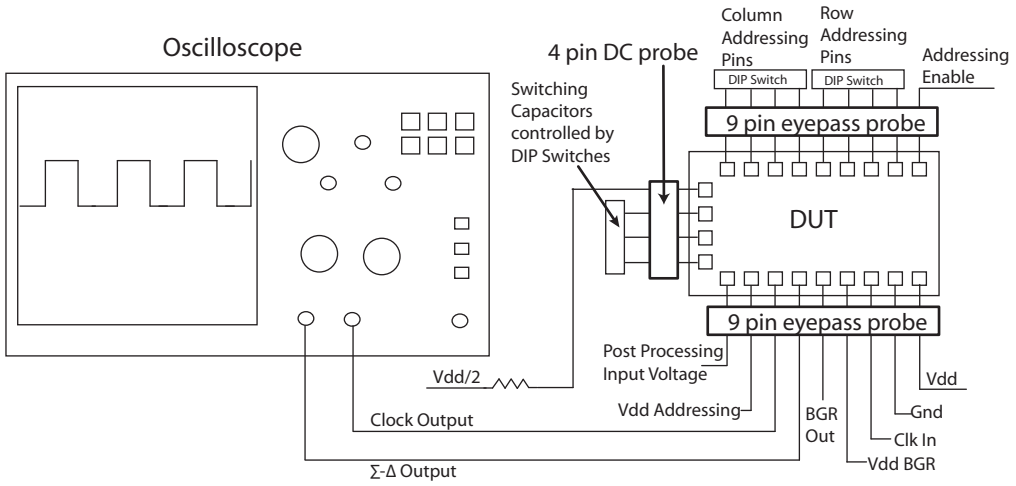


Figure 4.19: Measurement setup for prototype IC.

flowed. The "channel" consists of three copies of the 16x16 array in series, however only one of these copies is active and connected to the addressing blocks and used for measurements. The dummy array openings were added in the design to aid in the integration process. The design presented here has nine pads for controlling the addressing blocks - 1 bit enable and the 8 bit addressing inputs. There are also three inputs for the switching transistors in the integrator block and a pad for connecting the $\Sigma\Delta$ modulator to an external resistance load. As a result, the IC can sense either an external resistive load which is connected to the modulator via this pad or a chemoresistive bead/nanowire site on the IC. Separate V_{DD} pads for the $\Sigma\Delta$, bandgap reference voltage and addressing blocks are also provided along with pads for clock input. In order to provide a monitoring point for the bandgap reference output, a pad is connected to the output of the bandgap reference circuitry. This also provides an input for a external $V_{DD}/2$ source if the bandgap reference voltage is turned off. Finally, the two buffer outputs ($\Sigma\Delta$ output and clock out) are provided. The fabricated IC was measured using 2 nine pin eye-pass probes (from Cascade microtech) and a four pin DC probe (also from Cascade microtech). During measurements, the $\Sigma\Delta$ out and clock out can be measured on the oscilloscope and current consumed can be monitored on the power supplies. The measurement setup for this design is shown in Figure 4.19.

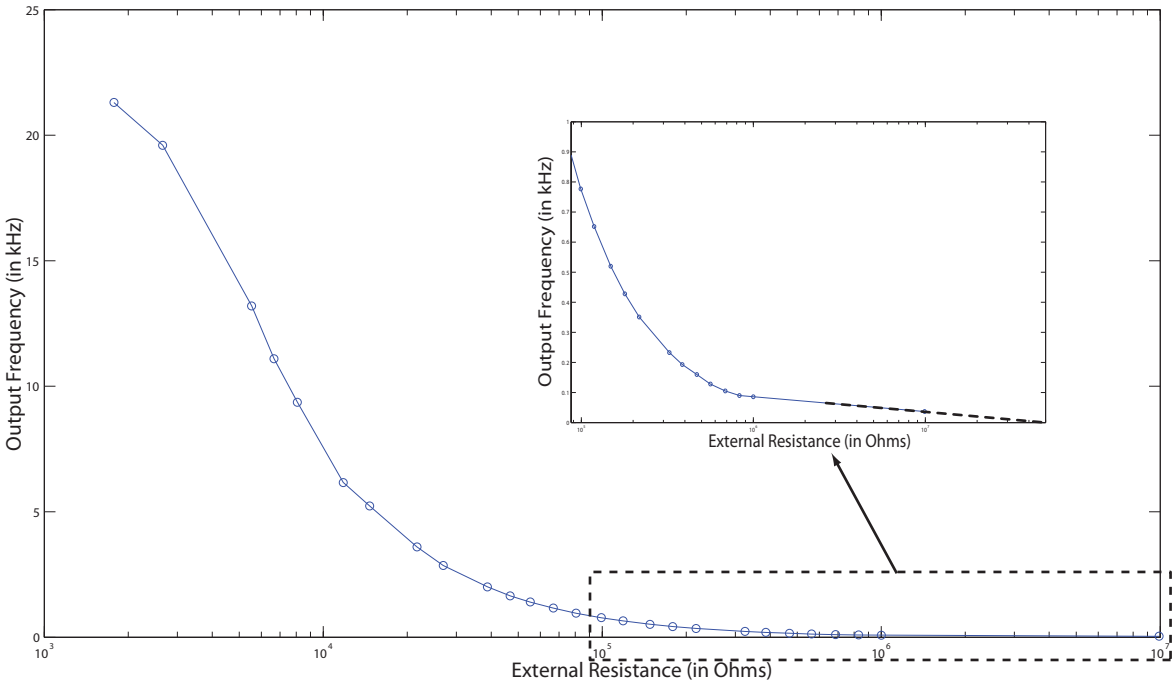


Figure 4.20: Measured output frequency vs external resistance for chip 00

The DC current consumed by the design was 1mA, which corresponds to 1.8mW of power consumption. In order to verify that the new design was similar to previous design, the frequency of the $\Sigma\Delta$ output was measured when different discrete external resistances were connected to the IC. The measured results are shown in Figure 4.20. One terminal of the external resistance was connected to an external $V_{DD}/2$ source as the bandgap reference was unable to sink the currents flowing through the external load. However, the comparator reference voltage was connected to the bandgap reference voltage. The highest measured frequency was 21.5kHz for a 1.77kΩ load and the lowest measured frequency was 36 Hz for 10MΩ resistance load. Since it was not possible to obtain discrete 30MΩ resistors for these experiments, the frequency was calculated based on extrapolation as seen in the inset plot. The output frequency was estimated to be 1 Hz for 30MΩ loads. Compared to the previous design, the value of the highest frequency achieved is lower and could be a result of parasitic loading caused by the large array. The frequency range of the output is smaller (between 21.5kHz to 38Hz) when compared with the previous design (38.9kHz to 200Hz). However,

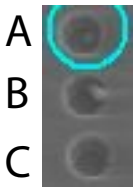


Figure 4.21: SEM of array locations used for frequency measurement in variant 00

the resistance measurement range is still the same. Adding the extra 50pF capacitor in the integrator block did not demonstrate the desired impact of lowering the lower measurement limit. In the simulation results shown earlier, no parasitics due to the wiring and DC probe used to connect the external resistance to the pad on the IC were taken into consideration which could explain the difference between measured and simulated results.

The operation of the array and the addressing blocks was tested by integrating gold coated SiO_2 beads (1.5μm in diameter) into the octagonal array openings of variant 00. Variant 00 was selected as it demonstrated a higher bead integration rate as discussed in Chapter 3. The beads were integrated by placing a drop of the solution containing the gold coated beads over the array openings of an IC which had been pad etched for ∼7 minutes. The IC was placed in an ultrasonic bath and agitated for 5 minutes. In order to verify if the beads were integrated successfully, the output frequency of the IC was measured at the array locations shown in Figure 4.21 before and after the beads were integrated. An external $V_{DD}/2$ source was used to provide the $V_{DD}/2$ voltage to the top metal layer as well as the comparator since the bandgap voltage reference could not sink the current flowing through the sensor. Before the beads were integrated, the output frequency for all three locations was measured to be 42 Hz, which corresponds to the output frequency of the IC when an 8MΩ resistor is connected to the external resistance pad on the IC (Figure 4.20). After the bead is integrated, the output frequency for location A and B increase due to presence of the gold coated beads in the openings. The output frequency for location C, however stays the same since no beads were present there. For locations A and B, the measured output frequency corresponds to the IC output frequency measured when ∼145kΩ and ∼140kΩ resistors were connected to

Table 3: Output Frequency before and after bead integration

Array Location	**Output frequency before beads (Hz)**	**Output frequency after beads (Hz)**
A	42	581
B	42	540
C	42.7	38

the external resistance pad of the IC (Figure 4.20).

4.5 Summary

The design presented in this chapter reduces the power consumption of the previous modulator design by 50% by using a bandgap voltage source instead of a resistive divider to generate a reference voltage. This design also modified the array addressing scheme to include a larger 16x16 array with a row/column based addressing scheme which can be scaled up for larger array sizes. The modified design of the array and addressing blocks allows heterogeneous integration of the chemoresistive bead and nanowires using simple post-processing steps. In order to compare the performance of the previous and current designs, the variation of output frequency for different external resistances was measured. The output frequency of the IC was measured before and after gold coated SiO_2 beads were integrated into the array openings of design variant 00. The measured results demonstrated the operation of the addressing blocks used in variant 00 as well as the successful integration of the gold coated beads.

Chapter 5

On-chip sensor RF impedance measurement

Particular chemical sensors, such as polypyrrole sensors, can be used for gas sensing applications based on variation of their complex impedance in the presence of various analytes [61, 62, 63, 64, 65, 66]. These sensors demonstrate a unique variation in the magnitude and phase components of their impedance with respect to time which can be used to identify particular analytes. Complex impedance variation provides an additional measurement variation beyond the simple resistance measurement described previously. Previous work in this area has focused on polypyrrole sensors which are created by depositing a layer of polypyrrole polymer over an electrode. An impedance measurement system such as a VNA can be used to measure the impedance variation in presence of an analyte. However, this approach is not well suited towards portable and integrated sensor systems. In this chapter, a new design for on-chip impedance measurement is presented which can be integrated directly with sensors and provide a more portable solution.

The impedance measurement circuitry described in this chapter can provide a new dimension for on-chip measurement and detection of chemical analytes. The design can measure the magnitude and phase of a complex impedance (such as a polypyrrole chemical sensor) at a

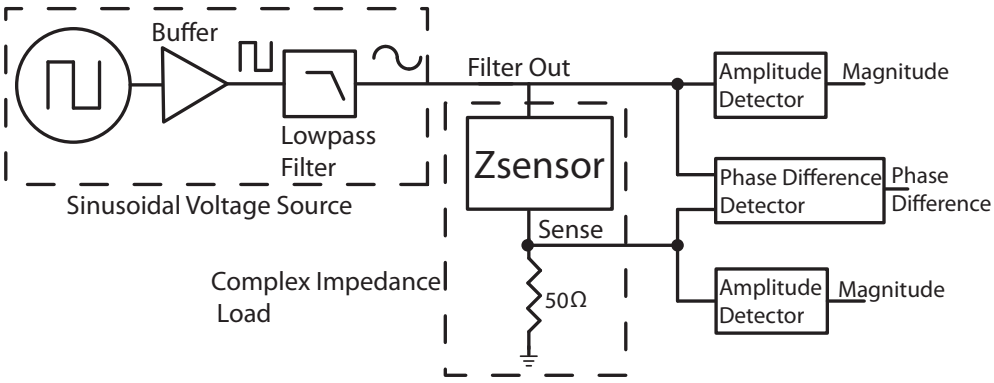


Figure 5.1: Block Diagram for Impedance measurement system.

particular frequency or over a wide range of frequencies. The following sections in this chapter discuss the design and operation of the proposed integrated circuit and its components. Simulation results are presented to demonstrate the operation of the proposed measurement IC.

5.1 Operation

The sensor impedance can be measured by applying a sinusoidal a.c. voltage across the load impedance and measuring the magnitude and phase variation due to the load. In this design, the load impedance consists of the complex impedance of the sensor and a 50Ω reference resistor connected in series. The magnitude and phase of the complex impedance (sensor) can be calculated by measuring the magnitude and phase of a signal at the input of the complex load and across the 50 Ω reference resistor (Figure 5.1). Using Ohm's law, the magnitude of the sensor impedance at the particular frequency can be calculated. Similarly, by measuring the phase difference between the input and output of the sensor, the phase of the sensor impedance can be calculated.

In this design, the sinusoidal a.c. signal is generated by a wide-band voltage controlled ring oscillator which can generate a square wave with frequencies varying between 200 MHz and

2 GHz. A buffer is provided at the output of the VCO so that a 50Ω resistive load can be driven. To convert the square wave into a sinusoidal signal, a low-pass filter is used to remove the odd harmonics of the fundamental frequency which are present in a square wave. The low-pass filter is designed such that its cutoff frequency suppresses the odd harmonics of the ring oscillator output for a wide range of output frequencies. The filtered output of the filter is used as input for the load impedance. The magnitude of the signal at the terminals of the sensor impedance is measured using amplitude detectors and the phase of the sensor impedance is measured using a phase detector. The magnitude of the voltage drop across the sensor impedance can be calculated using the difference of the amplitude detector outputs. The magnitude of the voltage at the output terminal of the sensor impedance is also used to calculate the current flowing through the load impedance based on Ohm's law. The magnitude of the load impedance can be calculated using the measured voltage drop across the sensor and the current flowing through it.

The proposed measurement IC was designed and simulated using the Jazz Semiconductor SBC18HA 0.18μm SiGe BiCMOS kit.

5.2 Ring Oscillator

In this design, the sinusoidal a.c. voltage is generated using a wide-band voltage controlled oscillator (VCO) which provides an output signal whose frequency varies from ∼200 MHz to ∼2 GHz. A VCO can be designed using either a L-C tank circuit or a ring oscillator. While L-C tank oscillators provide better phase noise performance, they have a limited tuning range and require a larger die area due to the presence of inductors. Ring oscillator based VCOs can be designed to operate over a wide frequency range while maintaining a smaller die size. However, the phase noise performance of a ring oscillator is worse compared to an LC tank circuit. The phase noise performance of the ring oscillator is not considered because the output frequency variation due phase noise does not result in a wide variation

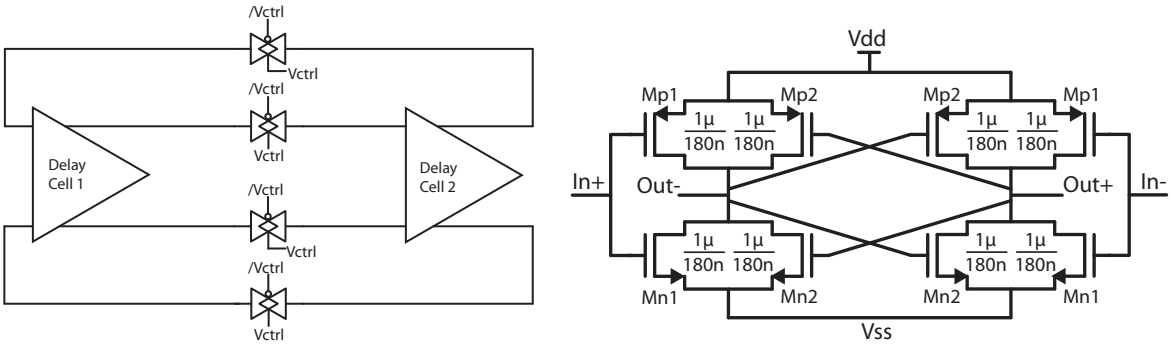


Figure 5.2: (a) Block diagram of ring oscillator. (b) Schematic of delay cell for ring oscillator.

of the measured impedance. The phase noise performance of the VCO can be improved in any future design iterations to increase the accuracy of design.

A ring oscillator consists of multiple delay cells connected together such that the output of the last stage acts as an input for the first stage. For oscillations to occur in a ring oscillator, the circuit should satisfy the following conditions (also known as Berkhausen criteria) [67]:

1. The loop gain of the ring oscillator should be greater than or equal to 1, and
2. The phase shift of the delay cells should be 180° (or odd multiples of 180°).

The ring oscillator used in the proposed measurement IC is based on the work presented by Chuang *et.al* in [68] (Figure 5.2a). The delay cell used in the ring oscillator has differential input and output. The delay cell consists of an input pair of transistors (MN1 and MP1) and a pair of positive feedback transistors (MN2 and MP2) which sustain oscillation. The ring oscillator uses two delay cells such that the differential inputs and outputs of each cell are connected via transmission gates (Figure 5.2b). The output frequency of the ring oscillator is controlled by the control voltage (V_{ctrl}) applied to the gates of the transmission gate transistors. Changing its control voltage varies the R_{ON} of the transmission gate which changes the delay time of a delay cell since the R_{ON} forms an RC network with the parasitic capacitance of a delay cell. As R_{ON} is varied, the time constant of the RC circuit changes,

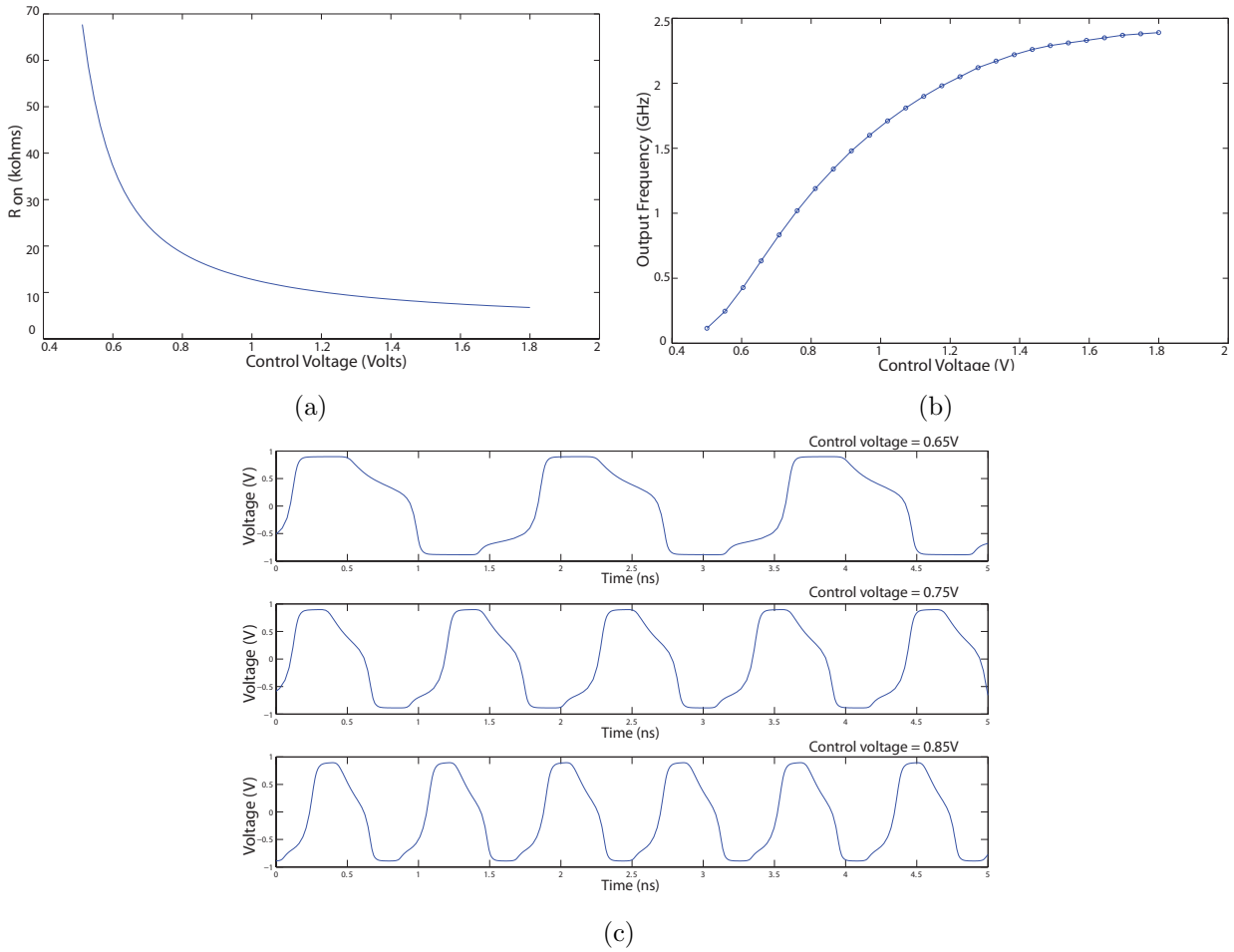


Figure 5.3: (a) Variation of transmission gate resistance vs. control voltage. (b) Variation of output frequency vs. control voltage. (c) Transient VCO output for different control voltages.

and the delay time of a delay cell varies. Since R_{ON} of a transmission gate varies linearly as the control voltages varies between 0.7 V and 1.2 V, the output frequency of the VCO also varies linearly over the same voltage range (Figure 5.3a and 5.3b).

The transistors of the delay cell are sized such that the VCO output frequency varies between 115 MHz (for control voltage = 0.5V) and 2.4GHz (for control voltage = 1.8V). In this region, the VCO operates linearly from ∼430MHz (for control voltage = 0.6V) and 1 GHz (for control

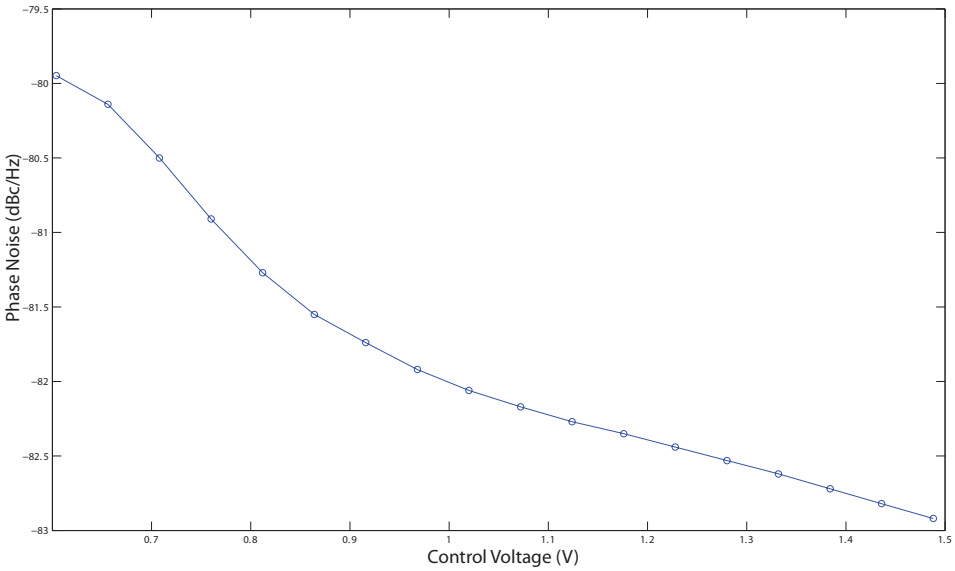
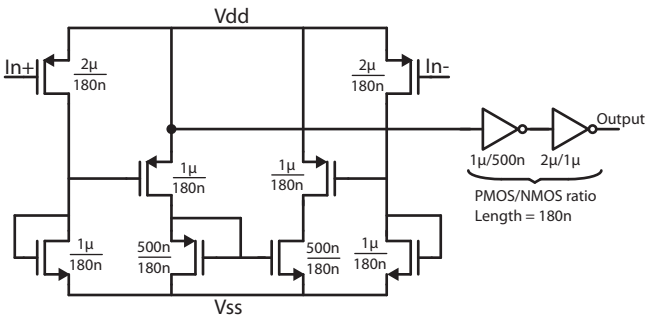


Figure 5.4: Phase noise of VCO vs. control voltage for VCO.

voltage = 1V). The transient output voltage of the VCO for three different control voltages is presented in Figure 5.3c. The simulated power consumption of this design for VDD = 1.8V was calculated to be 1.05mW. The phase noise for this VCO design is dependent on the control voltage (Figure 5.4) and was simulated to be -82 dBC/Hz at 1 MHz offset from the oscillation frequency for V_{ctrl} = 1V.

5.3 Duty Cycle Buffer

As discussed in the previous section, the output voltage of the VCO is not a perfect square wave with a 50% duty cycle because of the parasitic capacitance present in the delay cell. Therefore, a duty cycle buffer is used to generate a square wave signal with rail-to-rail voltage swing and 50% duty cycle. This buffer also converts the differential output of the VCO into a single ended signal [69]. The buffer consists of a two-stage differential input op-amp followed by an inverter buffer (Figure 5.5a). Simulation results were used to determine the transistor sizes for the op-amps. The duty cycle buffer output signals when inputs correspond to the



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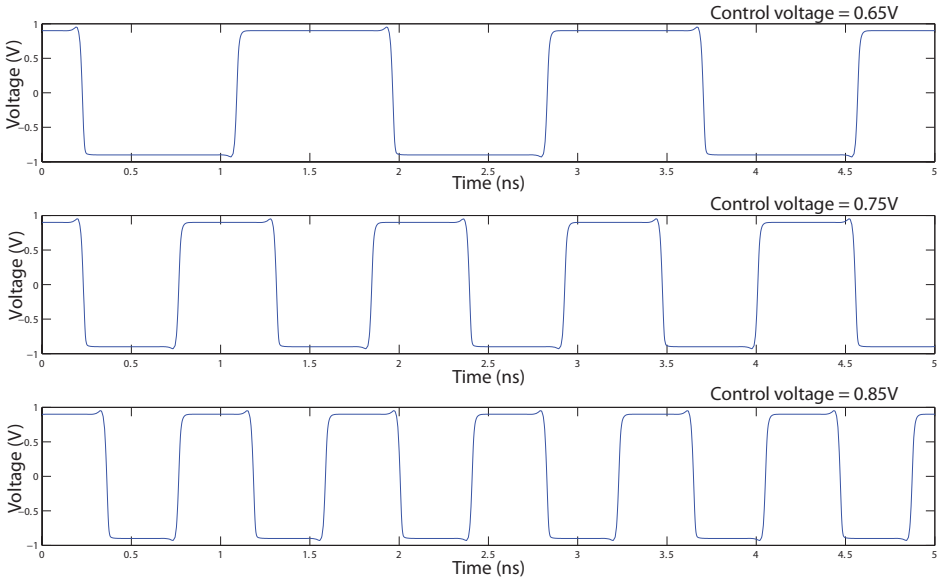


(b)

Figure 5.5: (a) Schematic of buffer/differential to single ended converter used at VCO output. (b) Transient output of duty cycle buffer where inputs corresponds to those in Figure 5.3c.

signals in Figure 5.3c are presented in Figure 5.5b. When compared with the input signals for the duty cycle buffer, its output are signals with a 50% duty cycle and small rise and fall times. Thus, the VCO output approaches the desired square wave signal.

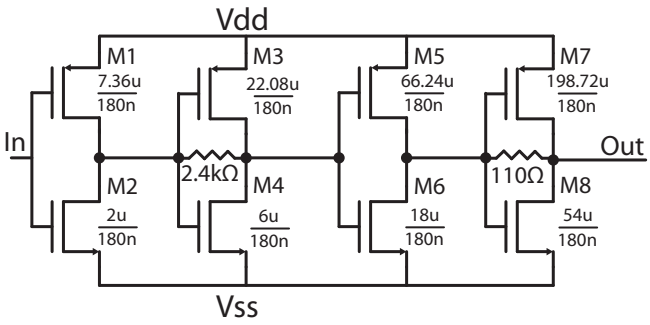


Figure 5.6: Design of VCO output buffer.

5.4 Output Buffer

A wide-band output buffer is connected at the VCO output so that the VCO can drive a 50Ω load resistance. The output buffer needs to operate over a wide frequency range to provide an output voltage swing which is constant over the entire VCO frequency range. The buffer design uses feedback resistors to increase the bandwidth similar to a Cherry-Hooper amplifier [70]. The buffer design consists of two stages where each stage consists of two inverters in series (Figure 5.6). A feedback resistor is included between the input and the output of the second inverter to decreases the input resistance of the second inverter. The small input resistance for the second inverter decreases the impact of the Miller effect in the first inverter and moves the pole to a higher frequency. The feedback resistor also lowers the output impedance of the second inverter which increases the output pole frequency. The transistor sizes were selected such that the final inverter can drive a 50 Ω load with a 1V swing.

The wide-band gain and phase response of the output buffer is presented in Figure 5.7. In simulations, the output resistance of the buffer was measured to be 17.8Ω and the power consumption of the buffer was calculated to be 43.03 mW. The power consumption of the buffer can be lowered by increasing the minimum load resistance from 50Ω or by decreasing the desired voltage swing across a 50Ω load resistance.

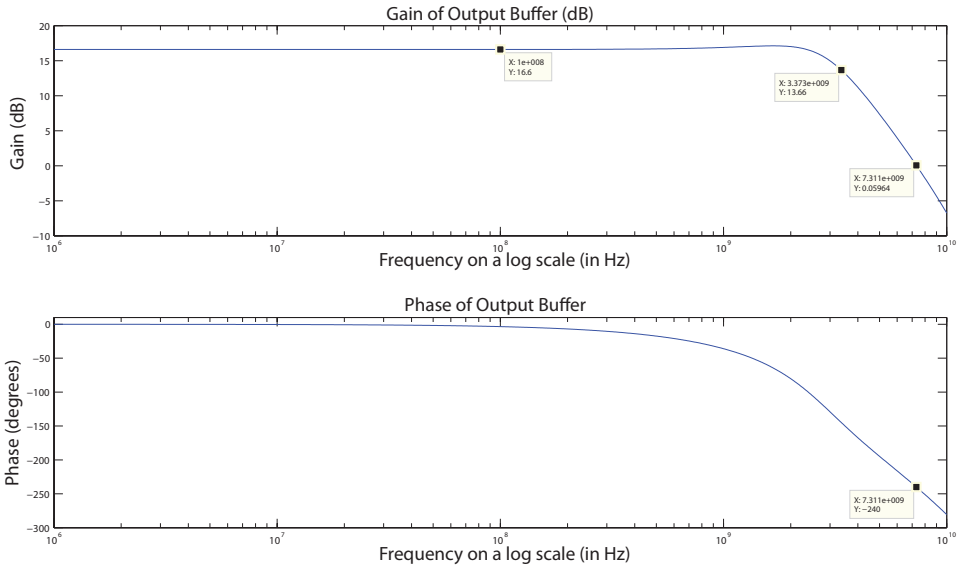


Figure 5.7: Gain and phase response of buffer amplifier.

5.5 Low-pass Filter

A square wave can be represented as the sum of its fundamental frequency and its odd harmonics. If a square wave is used to measure the impedance, any measured values will be inaccurate because of these harmonics. To obtain an accurate measurement with a square wave, the the odd harmonics of a square need to be filtered out using a low-pass filter. If the low-pass filter is designed with a cutoff frequency of f_C, odd harmonics of square waves with fundamental frequencies higher than $f_C/2$ can be removed. The low pass filter was designed as a pi-network chebyshev filter using passive inductors and capacitors (Figure 5.8a). The filter was designed with a 1 dB ripple and a cutoff frequency of 1.6 GHz. Thus, square waves with fundamental frequencies between ∼800 MHZ and 1.7 GHz can be filtered successfully to obtain a sinusoidal waveform (Figure 5.8c and 5.8e) The corresponding transient voltages at the filter input and output are also shown in Figure 5.8b and 5.8d. Any square waves with a fundamental frequency higher than 1.6 GHz will be attenuated the filter output since the fundamental frequency is higher than the cutoff frequency of the filter.

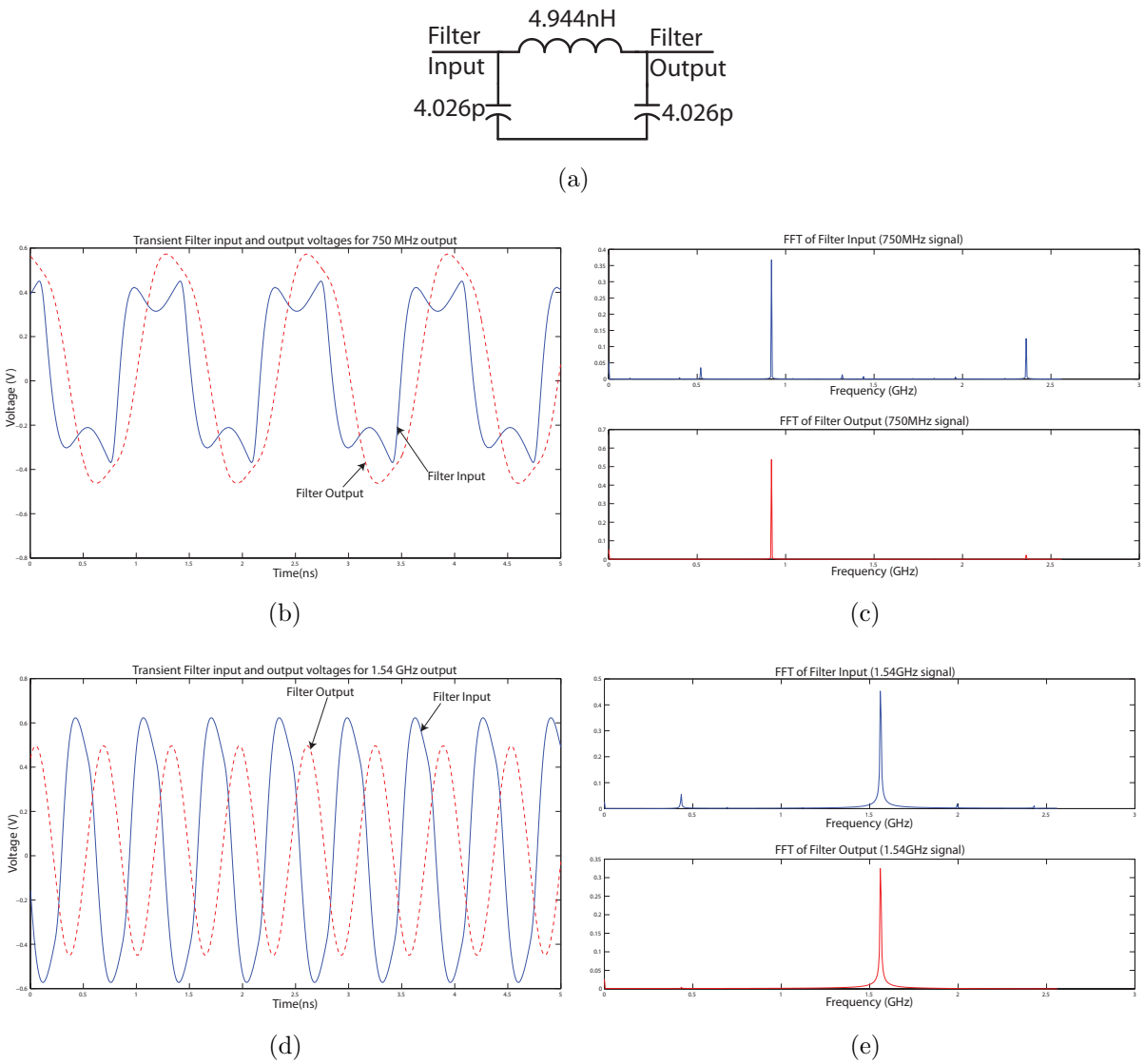
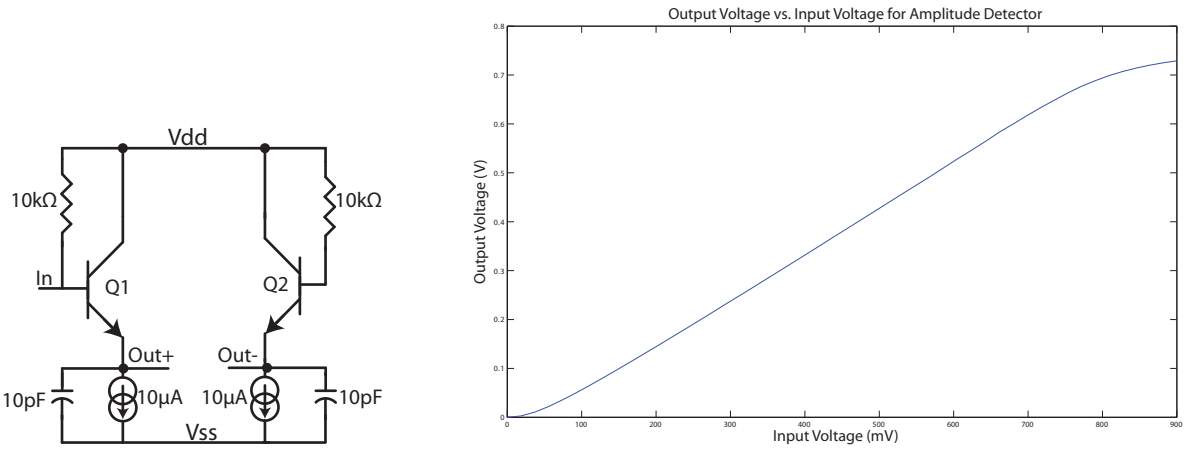


Figure 5.8: (a) Schematic of lowpass filter. (b) Transient input (blue) and output(red) for 750 MHz VCO signal. (c) FFT of filter input (blue) and output (red) for 750 MHz signal. (d) Transient input and output for 1.54 GHz VCO signal. (c) FFT of filter input (blue) and output (red) for 1.54 GHz signal.

5.6 Amplitude Detector

An amplitude detector based on [71] was designed to measure the magnitude of the signal on either side of the sensor impedance. The voltage magnitude below the sensor impedance



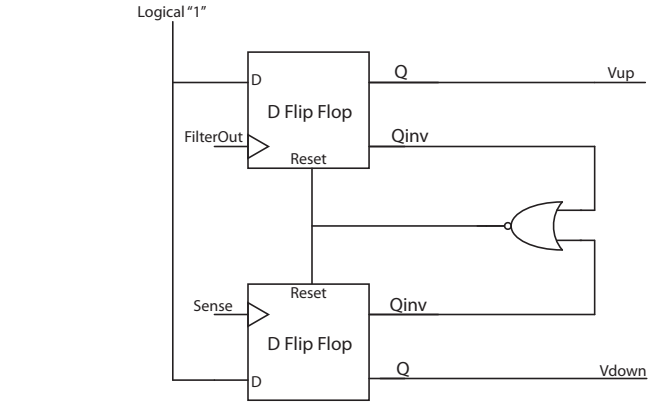
(a) (b)

Figure 5.9: (a) Schematic of amplitude detector (b) Relation between Vout vs. Vin for amplitude detector.

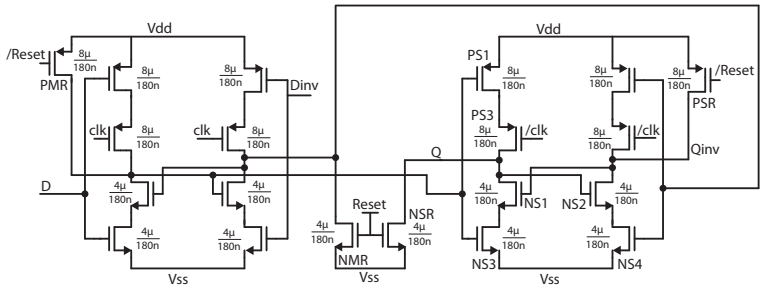
is equal the voltage drop across the 50Ω reference resistor and can also be used to calculate the current flowing through the load impedance.

The amplitude detector consists of a bipolar transistor (Q1) at the input to rectify the input voltage and transistor Q2 provides a DC offset voltage to cancel any DC components present in the input signal. The output of the amplitude detector is measured by subtracting the Out+ and Out- signals. Capacitor C1 and C2 are used to low pass filter the ac signal and power supply noise.

The relation between the input voltage amplitude and measured voltage output of the amplitude detector is presented in Figure 5.9b. The plot shows that the amplitude detector has a linear response for all input amplitudes between 50 mV and 850 mV. The plot correlates the output voltage to the input voltage and can be used to calculate the voltage drop across the sensor impedance as well as the reference resistor.



(a)



(b)

Figure 5.10: (a) Block diagram for phase detector (b) Schematic of D flip flop used in phase detector.

5.7 Phase Detector

The phase response of the sensor impedance is determined by measuring the phase difference between the input and output voltage signals of the load impedance. Since the phase response of an impedance can be leading (positive) or lagging (negative), the output of the phase detector should provide a value which can be used to determine if the measured voltage is leading or lagging the reference voltage. The phase detector used in this design is based on the work presented in [72]. The detector consists of two D flip-flops with asynchronous reset (refer Figure 5.10a). The input signals (FilterOut and Sense) for the detector are connected to the clock inputs of the D flip-flops and the asynchronous reset is controlled by the outputs

of the D flip flops (/UP and /DOWN). The data inputs of the flip-flops are connected to VDD. The phase difference between the input signals is represented by the average value of the difference between the UP and DOWN outputs of the D flip-flops.

The D flip flops used in the phase detector are designed to operate at high speeds so that the phase detector can operate for high frequency input signals. The D flip-flops use latches which are connected in a master-slave configuration (Figure 5.10b). The latches are designed to operate at low power and high speed by minimizing the number of transistors used. The master and slave latches are driven by complementary clocks such that for a given clock state, only one of the master or slave stages is enabled. While the CLK is low, the regenerative loop of the master latch (NM3 and NM4) causes the output of the master latch to go from 1 to 0 and enables the inverter (PS1 and NS3) of the slave latch. Since PS3 and PS4 are off, the output of the inverter does not effect the output of the slave latch. When CLK is high, the master latch is turned off and the slave latch is enabled. The regenerative loop of the slave latch (NS1 and NS2) determine output of the slave latch based on the input of the inverter (PS1 and NS3). The asynchronous RESET of the flip-flop is implemented using the PMR, NMR and PSR, NSR transistors. When RESET is high, PMR and PSR turn on and connect the output of the master and slave latches to the rails. When RESET is low, these transistors are off and the flip-flop behaves as normal. The use of NMOS transistors in the regenerative loops of the master and slave latches allows high speed and frequency operation for the design since the transistor sizes can be kept small and parasitics can be reduced.

Even though this design is targeted for high frequency signals, its measurement range decreases as frequency increases and the slope of the average output vs. phase curve increases (Figure 5.11). At 750 MHz, the detector can measure roughly 360 ° of phase difference. However, at 1.5 GHz the detector can only measure $\sim$290° which degrades the range of impedances that can be measured using this design. The plots presented the figure were obtained by varying the phase difference between two ideal sinusoidal voltage sources at the input of the phase detector and measuring the average DC output voltage.

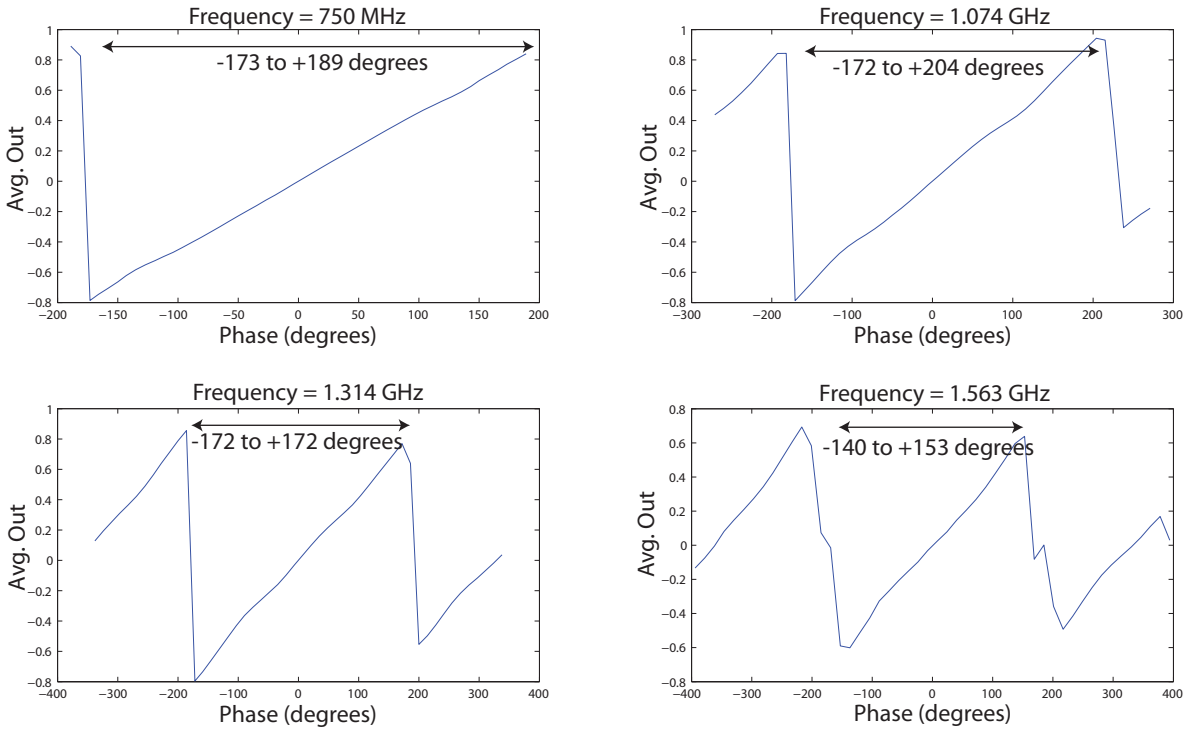


Figure 5.11: Average output of phase detector for various input frequencies.

5.8 Simulated Results

The impedance measurement circuitry was simulated to determine its measurement range and accuracy. As mentioned earlier, the magnitude of the impedance is determined using Ohm's law. The outputs of the amplitude detector are used to estimate the magnitude of the input signal (using the plot presented in Figure 5.9b). The voltage drop across the sensor impedance can be estimated by subtracting the voltage inputs for the amplitude detector. The current flowing through the sensor impedance is calculated using the voltage drop across the 50Ω reference resistor and Ohm's law. Thus, the magnitude of sensor impedance at a given time can be estimated using Ohm's law. With the voltage drop across the sensor impedance as well as the current known the magnitude of the sensor impedance can be calculated at a given point of time. The phase response of the sensor impedance is measured using the phase detector. The average value of the DC voltage at the phase detector output

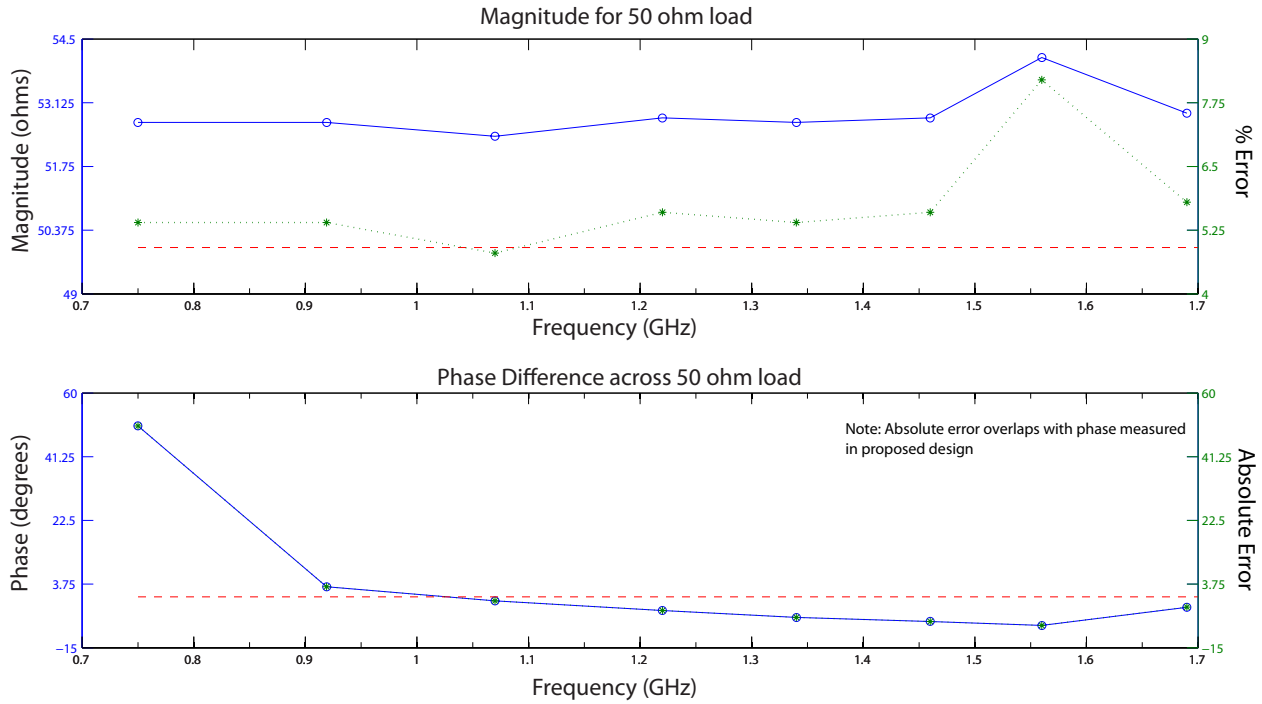


Figure 5.12: Magnitude and phase variation due to a purely resistive load.

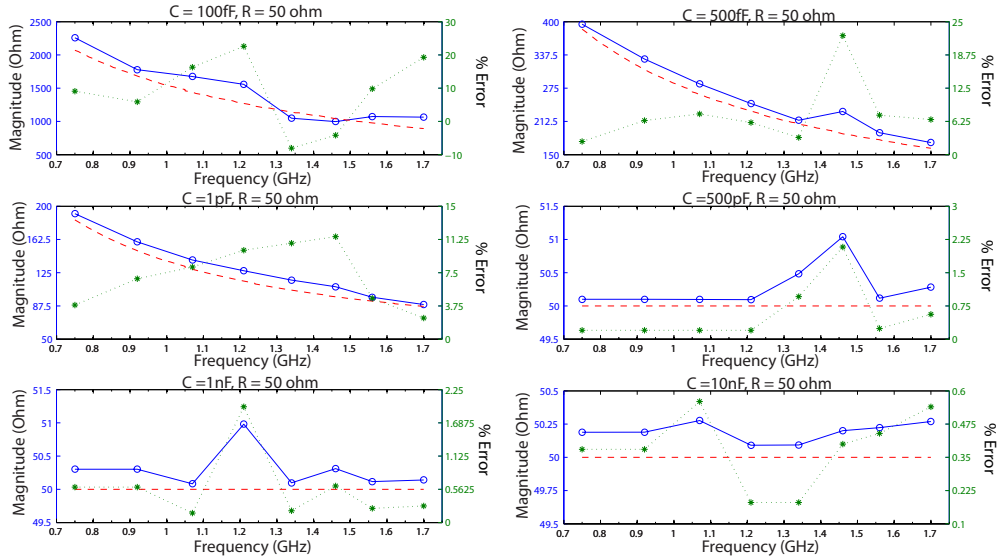
can be used to estimate the input phase difference using the plots similar to those presented in Figure 5.11. For a particular DC voltage at the phase detector output and signal frequency, the appropriate curve can be selected and the phase difference can be estimated. The design presented here can perform impedance measurements (magnitude and phase) at a fixed frequency such that the sensor impedance changes are measured with respect to time. It is also possible to sweep the frequency while measuring impedance (magnitude and phase).

The accuracy of the design was verified by comparing the simulated results to an ideal impedance measurement system which was simulated in Cadence using an ideal sinusoidal voltage source. The simplest test case for the impedance measurement system is a 50Ω resistive load as the sensor impedance. This resistive load was used to measure the errors in the phase detector since there should be no phase variation at all. The simulated magnitude and phase measurements of the circuit for the resistive load are presented in Figure 5.12 as the solid lines. The simulated results when using the ideal impedance measurement system

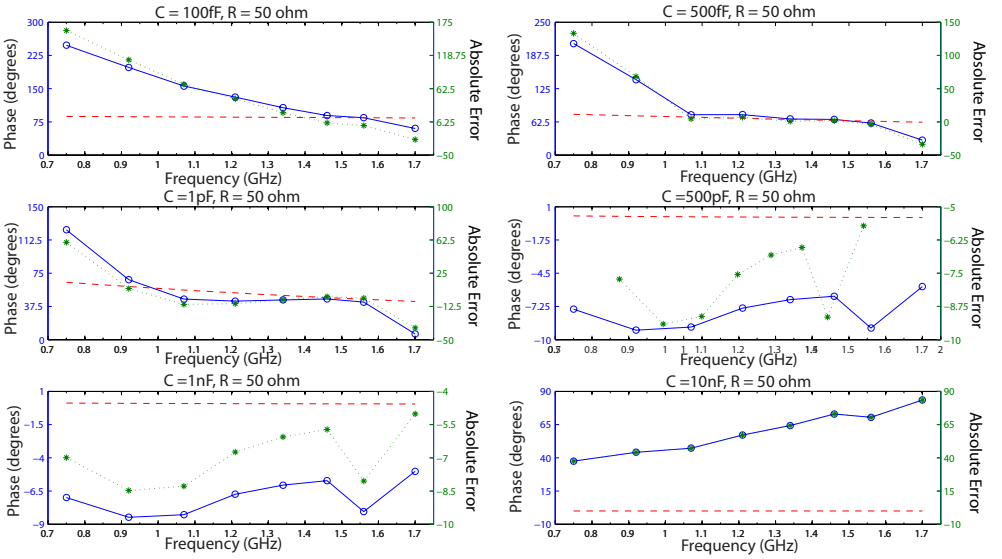
are shown as dashed lines. The Y-axis on the right of the magnitude and phase plots shows the percentage error and absolute error (between the proposed design and the ideal design) respectively. The error is plotted as a green line. The plot demonstrates the limitations of the impedance measurement system described in this chapter. The magnitude and phase measured in the ideal system are as expected (50 Ω magnitude and 0° phase) and remain constant with respect to frequency. However, the simulated values for the proposed design vary with frequency. The percentage error in magnitude is always less than 10% and can be considered to be the measurement error introduced by the design. These errors could be due to non-linearities present in the amplitude detector at high and low input voltages (Figure 5.9b). The error in magnitude could also be caused to presence of odd harmonic frequencies at the filter outputs. Towards the low end of the frequency range, the output of the low pass filter may contain harmonics which introduce the error in the magnitude calculations. The input to one of the amplitude detectors is close to VDD which is in the non-linear region of the amplitude detector. Inaccurate estimation of the input voltage for a particular output voltage could also lead to errors.

In case of phase, the error plot overlaps the phase measured in the proposed design. These errors could be introduced due to errors in estimation of the phase value based on the phase detector output since some interpolation is required to estimate the phase difference for a particular frequency. In the case of these simulations, plots similar to those presented in Figure 5.11 were used to estimate the phase difference for a given DC output voltage at a particular frequency. The number of points at which the average output voltage is measured was kept constant at all frequencies for simpler calculations. Increasing the number points for higher frequencies can increase the accuracy of the phase measurements. Thus, as the frequency increases the number of points between -180° and +180° for which the average DC output is calculated decreases. This implies that at higher frequencies, interpolation errors can become significant because of the lower number of measurements between -180° and +180° of phase difference.

Next the sensor impedance load was replaced with a series resistor-capacitor (RC) load.



(a)



(b)

Figure 5.13: (a) Magnitude of load vs. frequency for varying C (blue - proposed, red - ideal). (b) Phase of load vs. frequency for varying C (blue - proposed, red - ideal).

The measurement limits of the impedance measurement design were determined by varying the value of capacitance from 100fF to 10nF. The measured magnitude and phase of the RC impedance load for different capacitor values are presented in Figure 5.13a and 5.13b

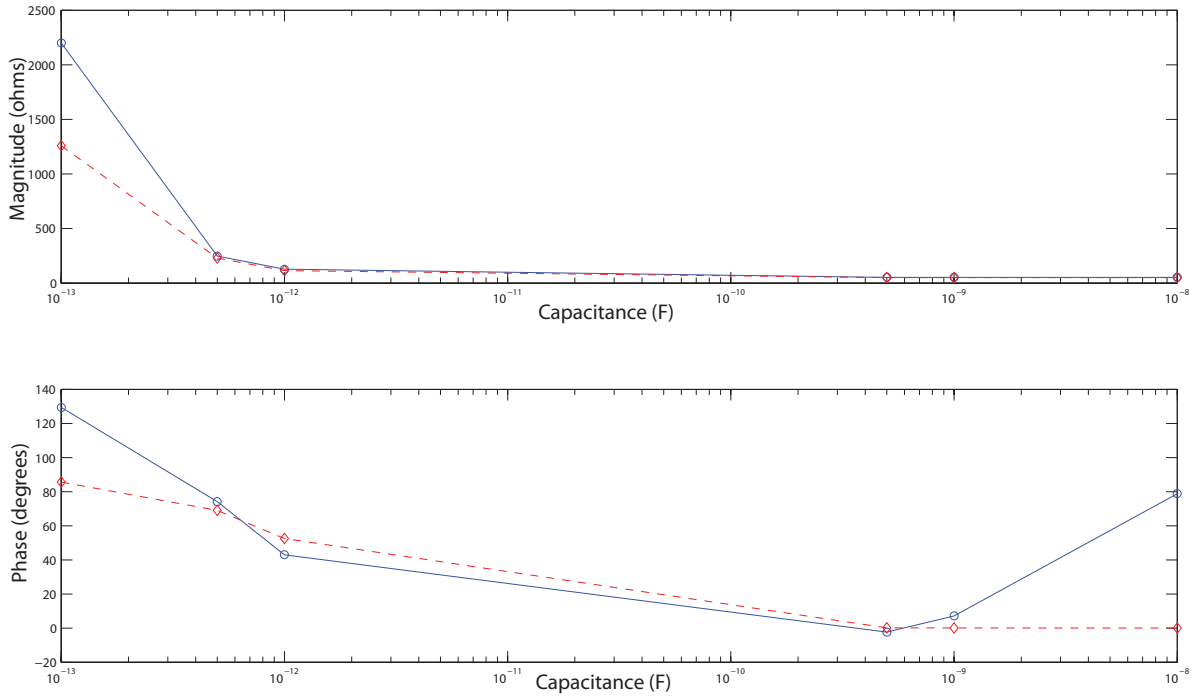


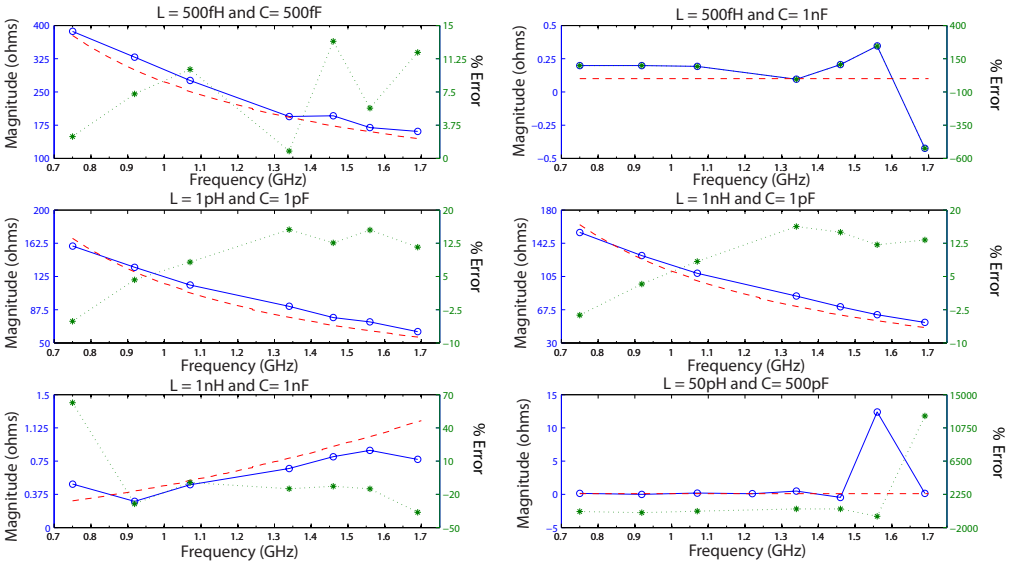
Figure 5.14: Magnitude and phase variation of a RC load for a fixed frequency as C varies.

respectively. The solid lines in the plots represent the measured values obtained using the design presented in this chapter and the dashed lines represent the results obtained using the ideal sinusoidal sources. The dashed green lines and the green axis on the right of each plot represents the error (percentage or absolute value) for each RC load. The error between ideal and proposed magnitude measurements is less than 10% over the entire frequency range for most loads except when C is 100fF and R is 50 Ω. The phase measurement has less than 10° error over majority of the frequency range for capacitance values between 500fF and 1nF. When the capacitance is either 100fF or 10nF, the error is much larger almost over the entire frequency range. The error in the magnitude estimation could be due to non-linearities in the amplitude detector. Interpolation is probably the biggest source of error in the phase measurements. The results presented here demonstrate the differences between ideal and proposed impedance measurement designs and can be used to estimate any correction factors used to offset any measurement errors. These results also demonstrate that the proposed design can measure the magnitude and phase of a RC load as the capacitance varies from

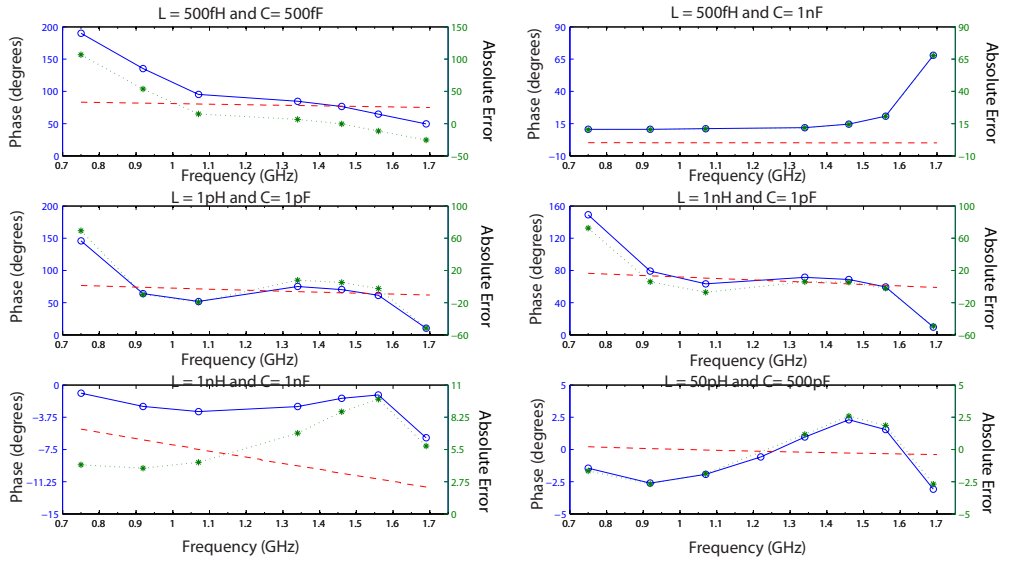
500fF to 1nF, which implies a measurement range of almost six orders of magnitude.

The measurement limits of the design can also be observed by varying the capacitance of the RC load from 100fF to 10nF for a fixed frequency of 1.22 GHz (Figure 5.14). Similar to the plots in Figure 5.13, the phase measurement for demonstrate a large error (error greater than 20°) for capacitance values less than 500fF or greater than 1nF. For the magnitude measurements, the error is large when the capacitance is 100fF. This correlates with the error measurements presented earlier.

Finally, a series inductor-capacitor (LC) load was used as the sensor impedance. The inductor and capacitor were swept over a wide range (500fH to 1nH for inductors and 500fF to 1nF for capacitors). The calculated magnitude and phase for the ideal (dashed line) and proposed (solid line) are presented in Figure 5.15. The error (percentage and absolute) is plotted as a green dashed line and the error axis is plotted on the right for each plot. As shown in the plots, for magnitude measurements, the percentage error is less than 12% over almost the entire frequency range for all combinations of the load except when L is 500fH and C is 1nF or L is 50pH and C is 500pF. For both loads, the magnitude of the load is almost zero since the resonant frequency of the load lies within the range of frequencies being measured. As a result the error percentage to be high. For these loads, absolute error would be a more accurate representation of the error. In case of phase measurements, the absolute error is approximately within 15 ° over most of the frequency range for all load conditions except when L is 500fH and C is 500fF. Thus, based on the results presented here, the proposed design can measure the magnitude and phase of a series LC load for almost all values of L and C except when L is 500fH and C is 500fF. Large percentage errors observed during magnitude measurements (when L is 500fH and C is 1nF or L is 50pH and C is 50pF) can be ignored since the reactances are canceled and any measurement errors are possibly due to limitations of the amplitude and phase detector designs. As mentioned in case of the RC load, towards the lower range, the filter may not be able to remove all odd harmonics of the fundamental frequency. This could result in the large error in phase measurements. Similarly, for frequencies above the range, the filter may be attenuating the signal as it starts



(a)



(b)

Figure 5.15: (a) Magnitude of load vs. frequency for varying L and C (blue - proposed, red - ideal). (b) Phase of load vs. frequency for varying C (blue - proposed, red - ideal).

approaching the cutoff frequency. This could result in the error observed towards the high frequencies.

5.9 Summary

This chapter demonstrates the operation of a proof of concept impedance measurement system using a ring oscillator with a wide tuning range and amplitude and phase detectors. The system can be used to measure the magnitude and phase response of a complex impedance load at a particular frequency or as the frequency is swept. The chapter presents detailed design information for each design block in the system as well as simulation results for each block. Simulated results are also presented for various loads such as purely resistive, RC and LC loads. In case of RC and LC loads, the inductive and capacitive components are varied for a wide range and the output of the design is compared with an ideal system. Simulation results demonstrate that for a 50 Ω load, the magnitude error is less than 10% and the phase error is less than 15 ° for frequencies between 0.9 GHz and 1.6 GHz. In case of a series RC load, the magnitude and phase measurements have less than 10% and 10 ° error respectively as the capacitance varies between 500fF and 1nF and resistance is held constant at 50Ω. For a series LC load, the inductor and capacitor values were varied from 500fH to 1nH and 500fF to 1nF respectively. The proposed design operates successfully over the entire range of L and C values except when L is 500fH and C is 500fF. For all other L and C values (whose resonant frequency lies outside the measurement range), the percentage and absolute error is less than 10% and 10 ° respectively. Overall, the proposed design closely follows the results obtained using an ideal sinusoidal source.

Chapter 6

Conclusion and Future Work

Miniaturized chemical sensing nodes, especially low power wireless based designs, can play a crucial role in environmental monitoring, health applications, home automation and military surveillance and reconnaissance by allowing rapid detection and analysis of chemical agents. Several approaches have been developed for integrated chemical sensors such as nanowires [39, 38], carbon nanotubes [37] etc where the resistance of the sensor varies depending on the type and concentration of the analyte present. In conjunction with such sensors, resistive readout circuits based on measuring the voltage drop across a resistor for a known current value [44], using Wheatstone bridges [43] or resistance-to-period converters [45] have been developed. In this thesis, a resistive readout circuit based on a sigma-delta ADC was designed using a 0.18μm CMOS process from Jazz Semiconductor. The thesis also presents the design of an impedance measurement circuit for complex loads which can measure the magnitude and phase information of a complex load impedance.

6.1 Conclusion

6.1.1 Resistive readout circuit using $\Sigma\Delta$ modulators

One of the goals of this thesis was to demonstrate improved resistance measurement using a sigma-delta modulator based circuit. Results demonstrating that a wide range of external resistances (from 2kΩ to 30MΩ) that can be measured using an existing version of the readout circuit design are presented in this thesis. An initial design with a 4x4 array of microbead sites was fabricated and measured. Although the measurement results demonstrate successful operation of the design, the relatively high power consumption ($\sim$ 3mW), small array size (4x4) and direct addressing scheme motivated the need for redesign of this work.

In the modified design, the power consumption was reduced by employing a bandgap voltage reference to generate the reference voltage for the comparator. The redesigned voltage reference lowered the power consumption of the IC design by 1.2mW. The array size in the new design was increased to a 16x16 array. A scalable memory based addressing scheme was also implemented using row and column decoders which select a particular row and column based on an 8-bit address code. The array and addressing scheme designs were also modified to allow heterogeneous integration of chemoresistive nanowires in addition to chemoresistive beads on the surface of a fabricated IC. In case of chemoresistive beads, this was achieved by integrating a series of arrays across the chip to provide a "channel" such that a solution containing beads could flow over the openings. In case of chemoresistive nanowires, the array layout and addressing blocks were designed such that post-processing voltages such as assembly voltage for dielectrophoresis and electroplating voltage could be applied to the array during the integration process.

Measured results for the new IC design were presented to demonstrate the performance of the design. Similar to the previous design, the output frequency of the design was measured for resistances varying from 2kΩ to 30MΩ. The output frequency of the IC was also measured before and after gold coated beads were integrated into the array openings. This result

was one of the major contributions of this work as it demonstrated the operation the Σ-Δ circuit as well as the array addressing designs. The successful integration of gold coated beads demonstrated that the design could be used in the future to measure the resistance of heterogeneously integrated chemoresistive beads in presence of chemical analytes.

6.1.2 Impedance Measurement

This thesis also presents the design of an impedance measurement circuit based on a wide-band ring oscillator VCO. Simulation results demonstrate that the proposed system could measure magnitude and phase of a complex impedance load with respect to frequency or with respect to time at a fixed frequency. The simulation results presented in this work demonstrate the measurement capabilities of the design for different load types such as purely resistive, series RC and series LC loads. In case of a series RC load, the proposed design can measure magnitude and phase when capacitance varies between 500fF and 1nF and the resistance is held constant at 50Ω. For a series LC load, the L and C values were varied from 500fH or 500 fF to 1nH or 1nF respectively. The proposed design demonstrated successful magnitude and phase measurements for all L and C values except when L was 500fH and C was 500fF. The work presented here demonstrates an integrated approach towards impedance measurement systems which can provide a new dimension in chemical sensing since the current approach focuses on measurement of resistance variation in a sensor when it is exposed to analytes. By measuring the impedance of a sensor, an alternate method for chemical sensing cab be implemented.

6.2 Future Work

The most immediate extension of research work presented in this thesis with respect to resistive readout circuits is the development of heterogeneous chemoresistive bead and nanowire integration techniques with high degree of control and success rate. The integration tech-

niques described in Chapter 3 do not guarantee a high success rate in case of chemoresistive beads and can be improved. Measurement results for integrated chemoresistive beads (and possibly nanowires) upon exposure to chemical analytes can further demonstrate the operating range of the readout circuitry as well as the addressing circuitry. Finally, a on-chip source for the clock signal required by the readout circuit could be designed to minimize the external components.

In case of the impedance measurement circuit, the next step would be layout and fabrication of the IC for characterization purposes. Multiple variants of the design could be fabricated based on variations in the VCO design and filter design. These factors will impact the range of frequencies over which impedance measurements can be made. Another avenue for future work in the impedance measurement system would be potentially integrating with sensor device arrays into the design to obtain a cross reactive array. Finally, the design presented in Chapter 5 can be modified to measure S11 and S21 parameters of a device under test for RF applications. This would involve designing a lumped element directional coupler which operates over the band of frequencies for which a sinusoidal waveform is obtained at the filter output. The architecture presented in [73] is presented in Figure 6.1. If the sinusoidal output from the VCO and low pass filter presented in this thesis is used as input for the directional coupler, an on-chip network analyzer can be designed to measure S21 and S11 parameters.

Further in the future, integrating wireless transceiver with chemical sensor arrays should be explored. For example, designs for ultra wide band (UWB) CMOS RFIC front ends have been demonstrated in [74, 75]. The wide bandwidth available in UWB front ends allows flexibility in wireless sensor network applications where multiple sensor nodes share the same band or hop over different bands depending on the data rate of the sensor node [76]. Moreover, since UWB systems use very short pulses for radio transmission, it is possible to design simple transceiver units which allow extremely low power consumption. For example, in [75] the power consumption of the transceiver is reported to be 0.7 mW. Thus, integrating a UWB wireless transceiver with the readout circuits presented in this thesis could allow

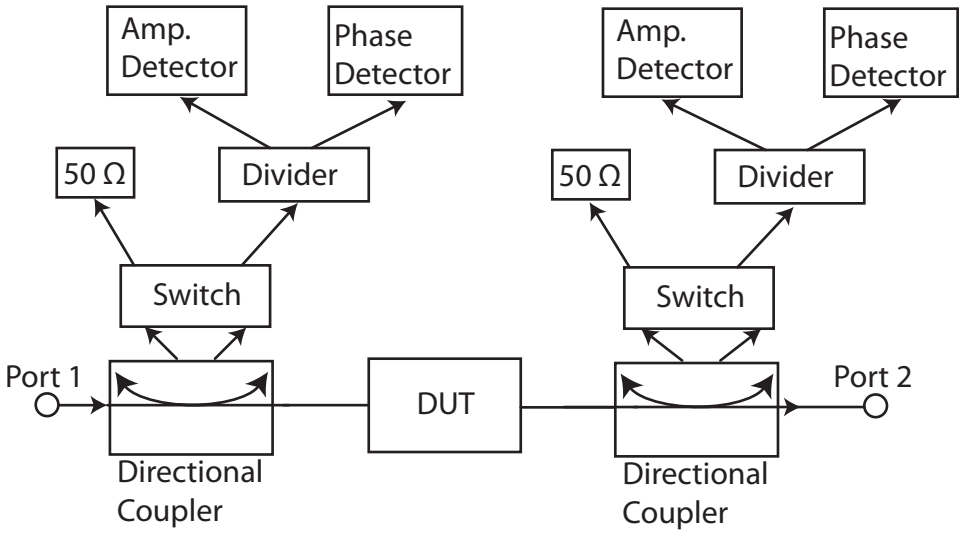


Figure 6.1: Integrated S parameter measurement system

them to operate as nodes in a wireless sensor network. These nodes could operate with low power consumption and use the heterogeneously integrated cross-reactive array for detecting a wide range of chemical agents.

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