Planar Packaging and Electrical Characterization of High Temperature SiC Power Electronic Devices

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Abstract

This thesis examines the packaging of high-temperature SiC power electronic devices. Current-voltage measurements were conducted on as-received and packaged SiC power devices. The planar structure was introduced and developed as a substitution for traditional wire-bonding vertical structure. The planar structure was applied to a high temperature (>250^{o}C) SiC power device. Based on the current-voltage (I-V) measurements, the packaging structures were improved, materials were selected, and processes were tightly controlled.

This study applies two types of planar structures, the direct bond and the bump bond, to the high-temperature packaging of high-temperature SiC diode. A drop in the reverse breakdown voltage was discovered in the packaging using a direct bond. The root cause for the drop in the breakdown voltage was identified and corrective solutions were evaluated. A few effective methods were suggested for solving the breakdown issue. The forward I-V curve of the planar packaging using direct bond showed excellent results due to the excellent electrical and thermal properties of sintered nanosilver. The packaging using a bump bond as an improved structure was processed and proved to possess desirable forward and reverse I-V behavior. The cross-sections of both planar structures were inspected.

High-temperature packaging materials, including nano-silver paste, high-lead solder ball and paste, adhesive epoxy, and encapsulant, were introduced and evaluated. The processes such as stencil printing, low-temperature sintering, solder reflowing, epoxy curing, sputtering deposition, electroplating, and patterning of direct-bond copper (DBC) were tightly controlled to ensure high-quality packaging with improved performance.

Finally, the planar packaging of the high temperature power device was evaluated and summarized, and the future work was recommended.

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I dedicate this achievement to my parents, my wife and my son

Without your encouragement and love, this work would not be possible. Thank you for being with me.

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Acronyms and Symbols

CMOS	Complementary Metal–Oxide–Semiconductor
DRAM	Dynamic Random Access Memory
I/O	Input/Output
TSSOP	Thin Shrink Small Outline Package
FQFP	Fine-pitch Quad Flat Package
RF	Radio Frequency
HBT	Heterogeneous Bipolar Transistor
MMIC	Monolithic Microwave Integrated Circuit
LED	Light Emitting Diode
VCSEL	Vertical Cavity Surface Emitting Laser
TAB	Tape Automated Bonding
WB	Wire Bonding
SBB	Solder Bump Bonding
FP	Flip Chip
BGA	Ball Grid Array
CSP	Chip Scale Packaging
WLP	Wafer Level Packaging
C4	Collapse Controlled Chip Carrier
DSP	Digital Signal Processor
UBM	Under Bump Metallurgy
DBC	Direct Bonded Copper
DBA	Direct Bonded Aluminum
CTE	Coefficient of Thermal Expansion
TO	Transistor Outline
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
POL	Power Over Lay
COF	Chip on Flex

MPIPS	Metal Post Interconnect Parallel Packaging System
D^2 BGA	Die Dimensional BGA
FCOF	Flip Chip on Flex
OFHC	Oxygen Free High Conductivity
CPES	Center for Power Electronics Systems
ROHS	Restriction of Hazardous Substance
WEEE	Waste for Electrical and Electronic equipment

Chapter 1

Introduction

Electronic packaging provides electrical connection or insulation, thermal dissipation, mechanical robustness, protection from the environment, long-term reliability, compatibility with next-level (board) assembly, and compliance with international standards for assembled power electronic devices. Therefore, electronic packaging plays an important role in ensuring good performance of electronic components. Thus, chip-level assembly is one of the determining factors of overall performance, cost, quality, and reliability of electronic components, multi-chip electronic modules, integrated electronic systems, and end-user electronic products. In order to ensure electronic chips or dice to have good electrical performance and long-term reliability, the following aspects need to be taken into consideration:

- Design of packaging architecture
- Selection of proper materials based on physical properties
- Thermo-mechanical stress analysis
- Electrical performance
- Thermal management
- Processability and manufacturability
- Environmental friendliness
- Acceptable cost
- Compatibility with higher-level assembly

In order to realize the aforementioned functions of electronic packaging, the tradeoffs among these aspects need to be taken into account. In addition to some common requirements such as good electrical, optical, or magnetic performance, low processing or manufacturing cost, and high reliability, different electronic devices each have their own special requirements for packaging or assembly techniques. For example, a digital device such as complementary metal–oxide–semiconductor (CMOS) or a dynamic random access memory (DRAM) device with a large number of input/output (I/O) pads requires that their packaging be high-density packaging that can be realized in thin-shrink small

outline packages (TSSOP) and fine pitch quad flat packages (FQFP). Radio frequency (RF)/microwave devices such as heterogeneous bipolar transistors (HBT) and monolithic microwave integrated circuits (MMIC) with high frequencies require their packaging to possess lower electrical parasitic effects such as resistance, inductance and capacitance since the comparable packaging dimension with signal wave length makes parasitic effects more obvious for microwave signals than low-frequency analog signals. Optical devices such as a light emitting diode (LED) and a vertical-cavity surface-emitting laser (VCSEL) need accurate alignment between them and the optical fiber and an efficient thermal dissipation; and for power electronic devices such as a rectifier diode and an insulated gate bipolar transistor, thermal management challenges are paramount for their packaging.

Therefore, the overall performance of the electronic components, modules, systems and end product depends not only on the electronic devices but also on the related packaging. Without good packaging, a device's potential function cannot be fully realized. For the packaging to realize desirable performance, the material selection, interconnecting method, and design structure need to be taken into consideration.

Admittedly, device fabrication techniques are developing at the rapid rate estimated by Moore's law. Moreover, some high-temperature semiconductor compounds, such as gallium nitride (GaN) and silicon carbide (SiC), enable some devices to withstand higher temperature than the previously possible. All these advancements in electronic device technology put pressure on the development of their packaging technology.

Without exception, power electronic packaging faces similar challenges to those presented by the fast development of power electronic devices. For instance, high-power electronics and high-junction-temperature devices necessitate high current-carrying and high heat-transfer packaging, respectively.

1.1 The Evolution of Interconnect in Electronic Packaging

a) Tape Automated Bonding (TAB)

Following the advent of the electronic device, TAB was initially used as an interconnect technology to interconnect the substrate with the integrated circuit (IC). A copper foil is patterned by photolithography so it is like a flexible circuit, and it is then

glued onto a prefabricated carrier consisting of a tape and a perforated polyamide film. A series of transport perforations and stamped openings are made for the IC and the connection leads (shown in Figure 1.1).

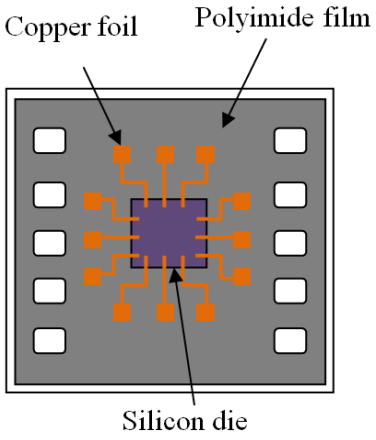


Figure 1.1 Die bonded to copper inner lead with TAB

The TAB technology provides several advantages over the wire bonding counterpart. These advantages include: (a) smaller bonding pad and smaller pad pitch; (b) higher I/O counts and lower interconnect profile; (c) reduction of process cycle time due to gang bonding; (d) stronger and more uniform inner lead bonding strength; and (e) lower parasitic effects and thus better electrical performance (especially for high-frequency applications).

At the beginning, TAB was processed manually at a slow speed. In the meantime, the wire bonder became automatic, programmable, and fast. Gradually, the initial advantages of TAB vanished and wire bonding emerged as a dominant interconnect technology, especially in high volume mass production.

b) Wire Bonding (WB)

Wire bonding is a major interconnect technology that is still widely used in the current electronic packaging industry. It electrically connects the chip and substrate or leadframe using fine aluminum or gold wire doped with trace amounts of strengthening elements such as magnesium, silicon, or beryllium, as shown in Figure 1.2. Currently, copper wire is also used as a bond wire because of its high electrical and thermal

conductivities, anti-sweep properties, and low cost. However, its susceptibility to oxidation requires a protective atmosphere for storage, handling, and processing. This requirement certainly incurs more cost and complicates the process. Although wire bonding interconnection can be highly automatic in high volume mass production, it is obvious that a thin, long loop of wire incurs parasitic electrical resistance and inductance, especially for high-frequency signals. Furthermore, the high profile and the long loop of a wire lead to thick packaging components and a small die-to-packaging ratio, wasting space when trying to realize three- dimensional (3D) high-density integration. Most importantly, higher thermal impedance plus less contact area between the wires and the die limit the major heat dissipation path to the bottom die attachment and thus prevent double-sided cooling from being applied.

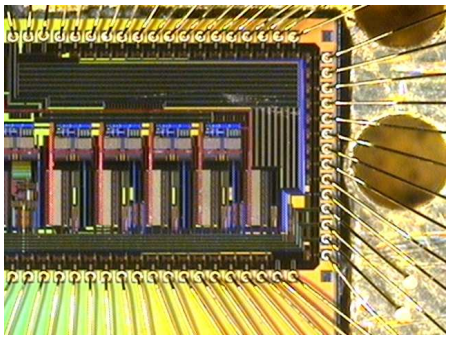


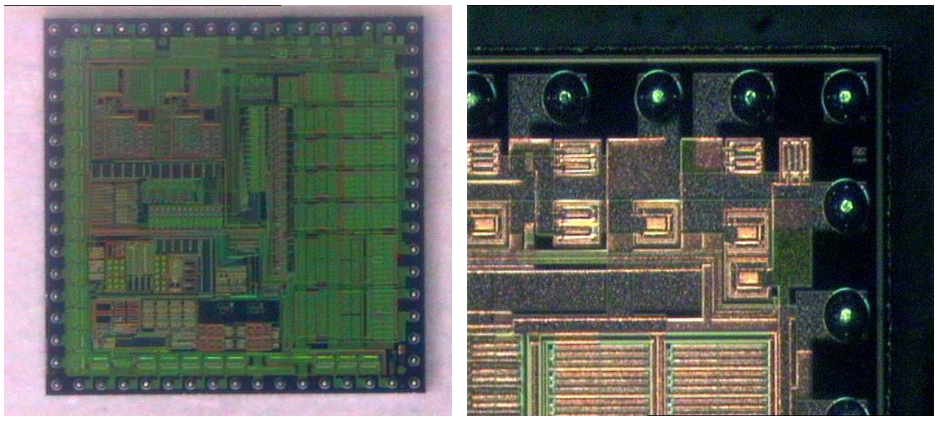
Figure 1.2 Wire bonding interconnect used in the packaging of application specific integrated circuit (ASIC) (ADVOTECH) [1]

c) Solder Bump Bonding (SBB)

SBB is an increasingly used interconnection technology which uses solder instead of copper foil or wire as an electrical link between the die pad and the leadframe or substrate. The forms and factors include the flip chip (FP), ball grid array (BGA), chip-scale packaging (CSP), and wafer-level packaging (WLP). The concept of SBB originates from IBM in the 1960's, and its packaging was first called collapse controlled chip carrier (C4).

Typically, in SBB a series of solder spheres are peripherally attached to pads on four edges of the die, as shown in Figure 1.3. Prior to ball attachment, the aluminum pads for wire bonding need to be pretreated with under-bump metallization technology, which

is a multi-layer thin film deposition that enables the wire-bondable pads to be solderable (as shown in Figure 1.4).



(a) Overview (b) Zoomed view

Figure 1.3 Digital signal processor chip in controlled collapse chip carrier (C4)

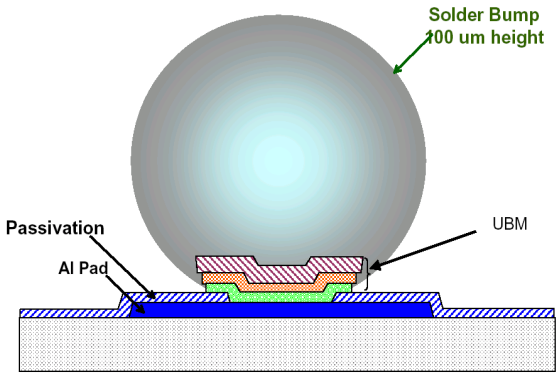


Figure 1.4 Schematic illustration of solder bump and UBM on flip chip

Compared to WD technology, SBB technology has better electrical performance for reducing both parasitic resistance and inductance. Moreover, it can also improve thermal performance by enabling double-sided cooling. However, the investment in infrastructure for UMB fabrication and the FC to board assembly prevents the rapid transition from WD to SBB.

Based on the three major interconnect techniques used in the electronic packaging described above, the packaging form and factor are developing toward improving signal integration, density integration, lower cost, miniaturization, and reliability. The general roadmap for packing evolution is shown in Figure 1.5.

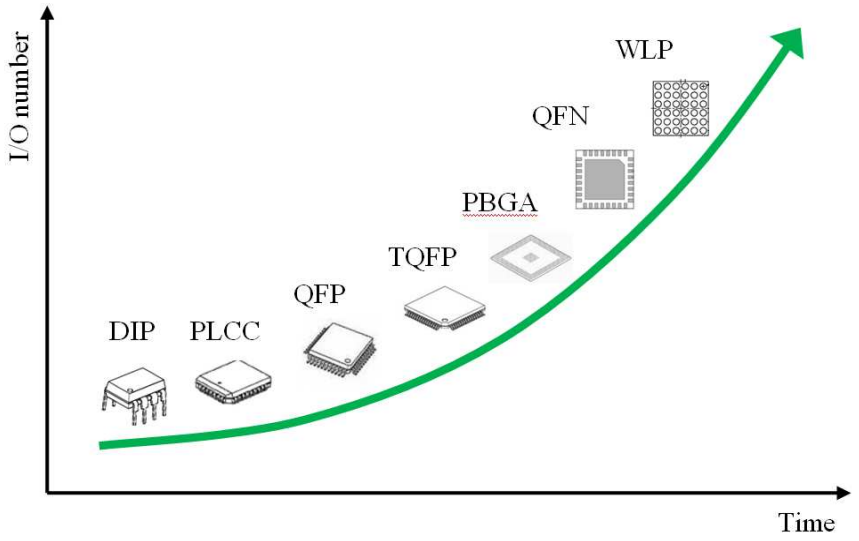


Figure 1.5 Packaging technology trend

1.2 The Evolution of Power Electronic Packaging

Similar to the packaging of other electronic devices, power electronic packaging is also the first level of assembly toward building the power electronic system or an end product. The first/chip-level power electronic packaging mainly involves die attachment, interconnection between die pads and the leadframe or substrate, and encapsulation. In most digital and analogue devices, the bottom of a power device is a terminal I/O pad bonded to the bottom substrate with thermally and electrically conductive die-attaching materials such as solder, conductive epoxy, or recently patented nanoscale silver paste. The particular operating mechanisms and their intended purposes present some challenging requirements.

First of all, the packaging needs to ensure desirable circuit performance and efficiency by minimizing parasitic effects (resistance, inductance, and capacitance), especially at high switching frequencies. Secondly, the large current and high voltage of power devices require the packaging materials and architecture to possess not only high current carrying capability but also excellent electrical insulating properties. Thirdly, the increasingly dense integration of power devices forces its packaging to have efficient heat dissipation. Finally, the reliability of power electronic packaging becomes relatively important due to high-power conversion and the accompanying loss. Typically, the following interconnection methods are employed in power electronics packaging.

a) Wire Bonding

With its mature technology, wire bonding was initially widely used and still dominates in electronic power packaging because it can effortlessly accommodate design changes in packaging and make use of existing infrastructure. Moreover, the reliability of wire bonding has been proved.

For single power chip packaging, the die is first attached to a conductive substrate using solder, and then the source and gate aluminum pads on the IGBT die or an anode aluminum pad on diode die are wire-bonded to a metallized copper alloy leadframe. Finally, the chip and bondwires are encapsulated with a molding compound for electrical insulation, mechanical robustness, protection from the environment, and improvement in reliability. An IGBT bonded with bondwires is schematically illustrated in Figure 1.6.

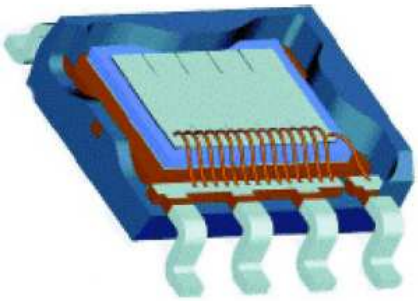


Figure 1.6 Schematic illustration of wire bonding in SO-8
single power device packaging [2]

As with the multi-chip wire bonding module, the multiple different switching dies are soldered to a direct-bond copper (DBC) or direct-bond aluminum (DBA) substrate. The substrate is pre-patterned with wet etching and laser cutting, which are discussed in Chapter 2. To increase the current-carrying capability, multiple aluminum wires ranging from 5mil (125μm) to 25mil (625μm) are ultrasonically bonded from one pad to a surrounding conductive trace, as shown in Figure 1.7 [3].

In practice, some disadvantages of wire bonding interconnection in power electronic packaging become obvious, especially for high-power and high-frequency applications. For instance, the thin, long wire leads to large electrical resistance of the

entire packaging. Correspondingly, parasitic inductance and thermal resistance also increase.

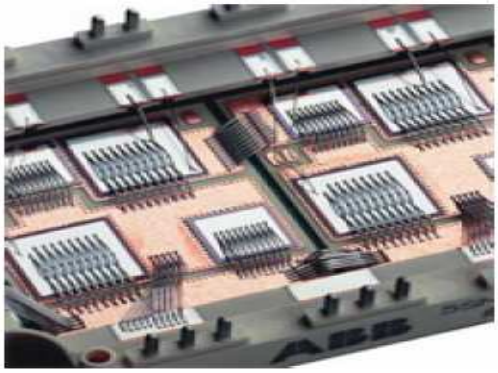


Figure 1.7 Top views of multiple chip power electronic module [3]

All these variations impair long term reliability and thus directly or indirectly result in early failure. Therefore, it is necessary to develop an alternative interconnect technology to overcome these drawbacks.

b) Ribbon Bonding

Ribbon is an alternative to bondwire for use in power electronic packaging to reduce electrical resistance and thus improve current handling capability. Compared with bondwire, the larger cross-section area of ribbon enables it to possess lower electrical resistance and thus carry larger current. Some wedge wire bonders can be accommodated to bond a ribbon. Figure 1.8 shows power devices bonded with aluminum ribbon.

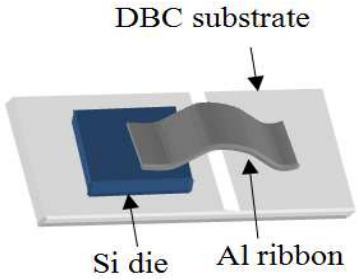


Figure 1.8 Power device ribbon-bonded to DBC substrate

Additional benefits provided by the use of ribbon instead of wire include improved reliability due to a larger cross-section at the heel of the bond; less heel

cracking due to the lower loop profile; less cratering because the bond force and ultrasonic energy are evenly distributed over a larger area; and there is no wire sway because of the structural rigidity of flat ribbon.

c) Solder Joint

Solder alloy, which is mainly used to attach the die to the substrate, can work as an interconnect between the top die pad and the leadframe or substrate. Normally, there are two types of solder joint connection: the collapse joint and the controlled collapse. A collapse solder joint is the same as a die attachment joined with solder. The concept of a controlled-collapse solder joint originated in IBM in the early 1960's and consists of solder bump being peripherally attached to edge-distributed pads designed for wire bonding. The UBM defined solder bumps are able to prevent the balls from collapse during soldering reflow.

To eliminate bondwire, Vishay Siliconix sandwiched power MOSFET devices between the top and bottom leadframes with solder, and brand-named it as PowerConnect technology [4], shown in Figure 1.9. Based on the report, the resistance between the source or gate and the top leadframe was significantly reduced compared to that of wirebonding. Additionally, the heat dissipation was dramatically improved due to an enlarged contact area between the leadframe and the gate and source terminal pads. However, reliability became a big concern due to the large coefficient thermal expansion (CTE) mismatch between the copper leadframe and the silicon die.

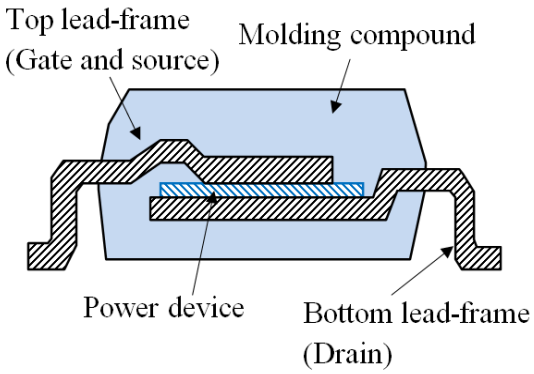


Figure 1.9 Cross-section illustration of PowerConnect chip-level packaging

To improve the reliability of solder joint connections in power electronic packaging, Fairchild Semiconductor applied solder balls interconnect to its TO-8 wireless packaging [5]. A solder ball joint not only can ameliorate the reliability concern of solder collapse-joint chip-level packaging caused by the large CTE mismatch between a large area leadframe and the die, but also can reduce the electrical and thermal impedance of the wire bonding interconnect of power electronic packaging. However, the major thermal dissipation channel is still through the bottom die attachment even though the solder ball can transfer heat to some extent. If both geometrical bonding structure and thermal transfer efficiency are taken into account, the collapse solder joint interconnect is more reliable than the solder ball interconnect [6]. Figure 1.10 shows the TO-8 wireless MOSFET packaging developed by Fairchild Semiconductor.

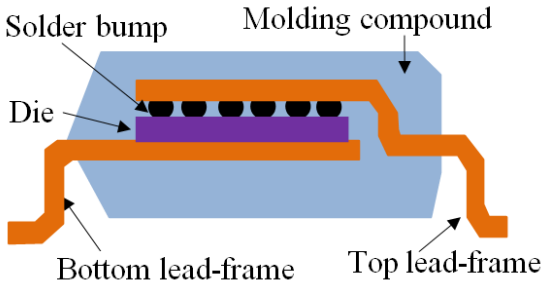


Figure 1.10 Schematic illustration of TO-8 wireless power MOSFET packaging

To further reduce packaging's resistance and to enhance heat transfer efficiency, solder balls are also applied to packaging to replace the external leadframe as the I/O terminals of the packaging. These balls may enlarge the total contact area between the packaging and the printed circuit board (PCB) and reduce the length between the die pads and the PCB's footprint. Consequently, heat dissipation and electrical performance are improved. For example, Fairchild Semiconductor's PowerTrench BGA MOSFET packaging [7] shown in Figure 1.11, replaces the leadframe with solder balls as the next-level interconnect between the packaging and the PCB board.

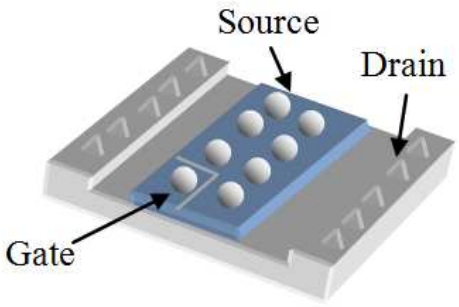


Figure 1.11 Schematic drawing of Fairchild Semiconductor's PowerTrench BGA MOSFET

d) Conductive Epoxy

To relieve the thermomechanical stress caused by the large CTE mismatch encountered in Vishay Siliconix's PowerConnect packaging, International Rectifier (IR) uses silver-filled conductivity epoxy to replace solder alloy as the top interconnect material [8]. IR's CopperStrap is shown in Figure 1.12. In contrast with the solder alloy, conductive epoxy, because of its lower elastic modulus, can relieve the stress caused by a large area CTE mismatch. However, the side effect is an increase in electrical and thermal impedance.

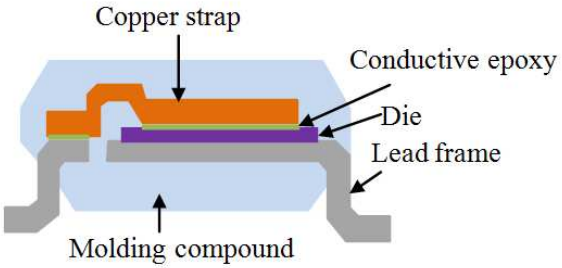
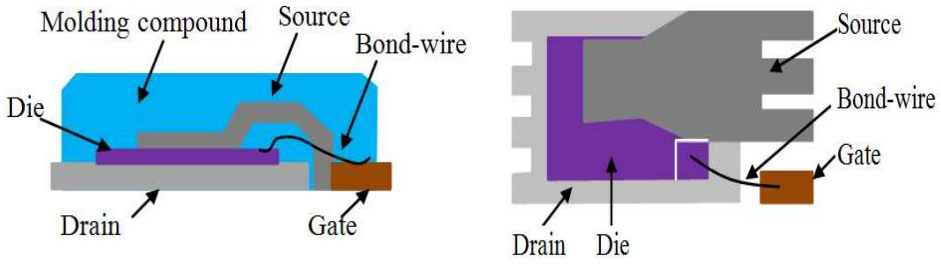


Figure 1.12 Schematic illustration of IR's CopperStrap power electronic packaging

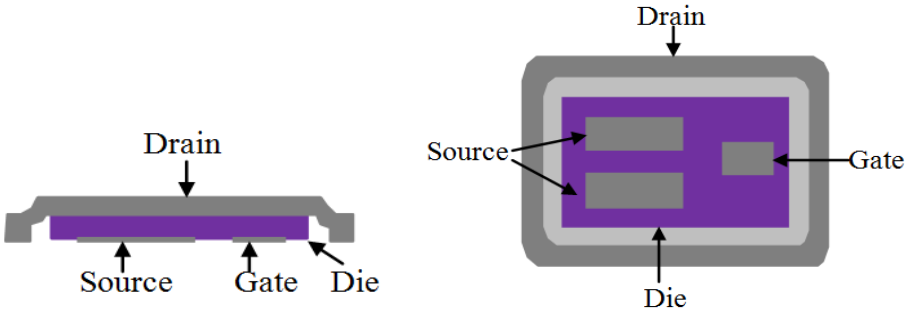
To improve heat dissipation of CopperStrap packaging, IR made an effort to develop a heat-enhanced bottomless packaging brand-named PowerPack shown in Figure 1.13. The major advantage of PowerPack is that a large area drain terminal can be directly soldered to the PCB, thus reducing electrical and thermal impedance. Furthermore, following the endeavor to perfect PowerPack packaging, IR developed and introduced a size-reduced PowerPack with the brand name of DirectFET^{TM} [8] shown in

Figure 1.14. In DirectFET™, not only was thermal dissipation enhanced, but the silicon-to-packaging ratio was also increased.



(a) Side view (b) Top view

Figure 1.13 Schematic illustration of PowerPack packaging developed by IR



(a) Side view (b) Bottom view

Figure 1.14 Schematic illustration of DirectFET packaging developed by IR

e) Metal Deposition

Imitating metal deposition as an interconnect in the fabrication of semiconductor integrated circuit (IC) devices, power electronic device packaging applies thin film technology to the interconnect between the terminal pad of die and the external circuit. The relevant deposition techniques include physical methods like sputtering and e-beam and electrochemical methods like electroplating and electroless-plating. The advantage of the thin-film interconnect is that multiple chips can be processed simultaneously. General Electric (GE) applied this technology to its power overlay (POL) packaging product [9] shown in Figure 1.15. Although the metal deposition process involves a long procedure, its capability for processing multiple dies and improving thermal and electrical performance earns it favor in power electronic packaging.

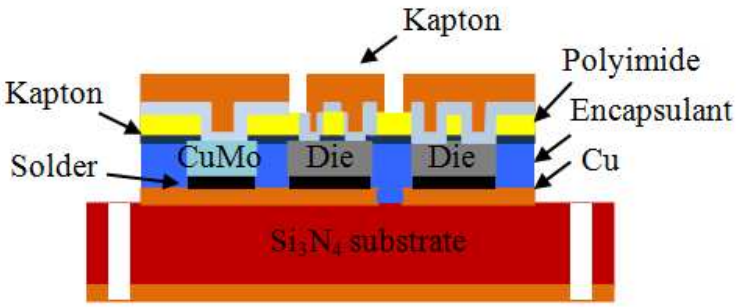


Figure 1.15 Illustration of a power overlay module developed by GE

Since the application of metal deposition to power electronic packaging is different from all other interconnect techniques, its process flow is elaborated here. In essence, the power overlay technology (POL) is a combination of chip-on-flex (COF) and thin-film deposition. The process starts with the lamination of a 50-μm -thick polyimide film using a thermoset adhesive to a metal frame, which eases handling and stabilizes the process. The frame is 200mm in diameter and provides a working area with a diameter of 150-170 mm [9]. The bottom side of the film is coated with a 12-μm-thick thermoset adhesive that is partially cured. A protective sheet is then applied over the adhesive to keep the adhesive from being contaminated during the subsequent processing steps. Through vias are formed by laser machining the flex structure, through the film and through the adhesive in locations that correspond to the electrical contact pads on the topside of the power semiconductor devices. The protective film is peeled off, removing laser ablation debris and the core portions of the vias shown in Figure 1.16. Multiple bare power chips are mounted face down onto the adhesive side of the flex, aligned to the via such that the chip metal contact pads cover the bottom of each via. The adhesive is cured using elevated temperature, a vacuum and finally pressure. A plasma etch is used to clean out any residue adhesive that may have flowed into the via or onto the exposed chip pads [9]. A seed metal layer (typically Ti: Cu) is applied to the top surface of the assembly, on the via side walls and on the chip pads. The seed layer provides a barrier to metal diffusion at the metal-to-polymer meeting point, provides metal-to-chip pad interfaces, and enables the subsequent copper electroplating. The metal layer is thickened to 50-150μm by electroplating using a bright, ductile copper bath.

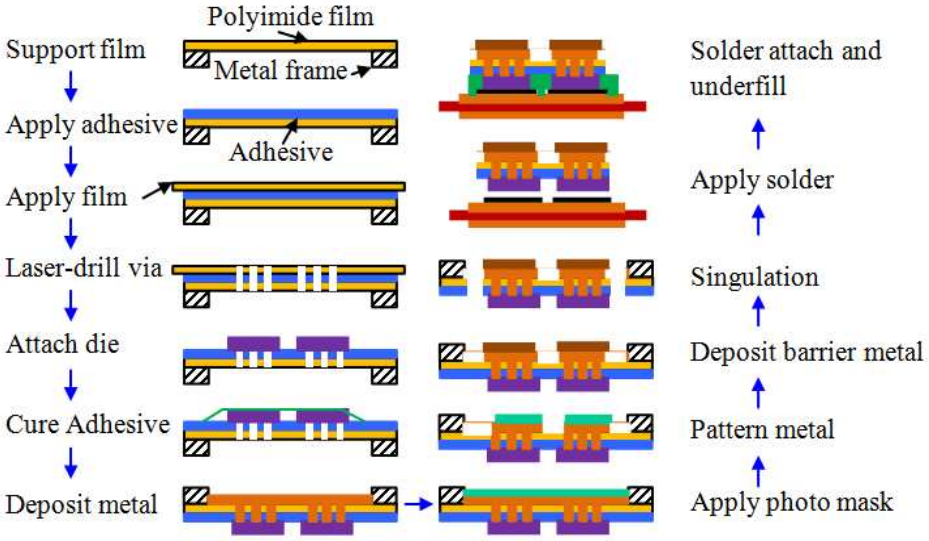


Figure 1.16 Power Overlay process flow

Subsequently, a photoresist is applied to the top surface and defined using either a mask-based exposure system or a direct-write laser. The metal is etched through the photoresist to form the desired interconnect structure. The exposed copper can then be electroless-plated with a solderable metal such as Ni:Au or Ni:Ag to facilitate mounting a component to the top or attaching I/O strap or cooling structures [9].

Finally, the individual power modules or chip-scale devices are then excised from the frame by mechanically cutting or laser scribing the flex. These power modules are solder-attached to a high-performance power substrate. The substrate must provide the metal solder mount down pads, an interconnect lead to bring the backside of the power device into contact with the substrate, electrical isolation for the mounting pads from the module's backside metal, mechanical stability, and a high-thermal-conductivity cooling path. DBC or DBA can serve as a substrate. Once the power overlay modules are mounted onto the module substrate, an underfill material is dispensed into the gaps between the chips and around the perimeter of the module. This material provides structure for the module, relieves stress between the COF interfaces and the chip solder attach, and eliminates any potential air dielectric breakdown within the module [9].

Although power overlay has excellent electrical and thermal performance, its reliability is still a big concern and needs to be evaluated.

f) Press Pack

To eliminate parasitic effects caused by bondwire and to relieve concerns about reliability of a solder interconnect or metal deposition, press-pack technology emerged as an effective interconnect method to not only handle high voltage and current but also to have improved reliability. Westcode, a subsidiary of IXYS Corporation, has built press-pack IGBT packaging [10], shown in Figure 1.17. In press-pack packaging, the contact to the die is made only through externally applied pressure, which eliminates the need for wire and substrate bonds, thus minimizing the stress and associated lifetime reduction factors for the die [10]. Individual die gate terminals are contacted via sprung pin, which is commonly connected to the external gate terminal via a planar distribution board, which is carefully configured to ensure series impedance to the die and therefore good homogeneous switching. However, the expensive manufacturing cost involved with precision machining and planarization limits the press-pack to high power packaging applications.

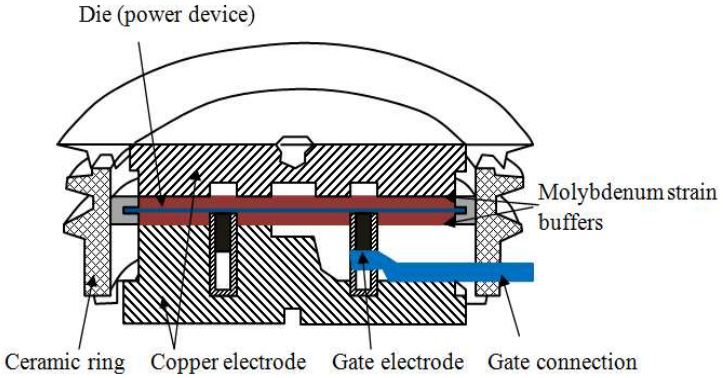


Figure 1.17 Schematic drawing of IGBT packaging by press-pack

g) Sintered Silver

The high junction temperature of SiC and GaN devices and the hard operating environment mean their packaging must withstand a high operating temperature. For example, some SiC power devices can work at up to 175^{o}C or even 250^{o}C, but at 250^{o}C, most solders would melt. Moreover, when the working temperature is close to the melting temperature, the long-term reliability of the device is compromised. To meet high power and high temperature requirements, Semikron [11] employed sintered silver as an

interconnect material because silver, with a melting point of 961°C, which is far beyond operating temperatures, is substantially cheaper than gold and palladium, is not susceptible to oxidation like other metals, and has significantly better electrical and thermal properties. Moreover, sintered silver is more reliable than bondwire and solder alloy since no intermetallic compound is involved in the bonding microstructure. However, a high sintering temperature of 600°C and a long processing time become an obstacle to the introduction of sintered silver into manufacturing. To facilitate sintering, assisted-pressure is applied during processing. Figure 1.18 shows sintered silver interconnection in a power module carried out by Semikron.

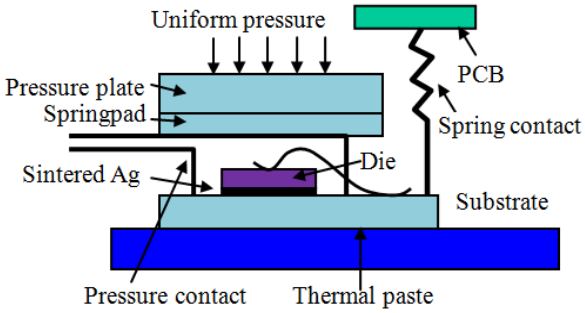


Figure 1.18 Schematic illustration of sinter silver in power electronic module by Semikron

1.3 The Development of Power Electronic Packaging in CPES

Over the past ten years, CPES has put a great deal of effort into developing new power electronic packaging technologies. The milestone packagings and modules include the metal post interconnect parallel packaging system (MPIPS), die dimensional BGA (D^2BGA), flip chip on flex (FCOF), the dimple array, embedded power, pseudo GE-POL, and flex power packaging technologies.

At the beginning, wire bonding was still used as an interconnect in power packaging or modules, as shown in Figure 1.19.

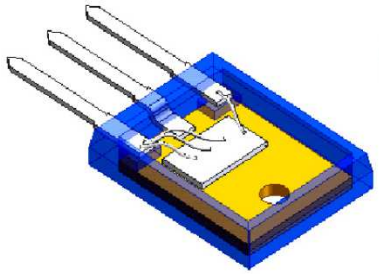


Figure 1.19 Wire bonding power electronic module by CPES [2]

To reduce parasitic effects and enhance thermal dissipation, the metal post was introduced and developed as an interconnection in power electronics packaging in 1999, as shown in Figure 1.20.

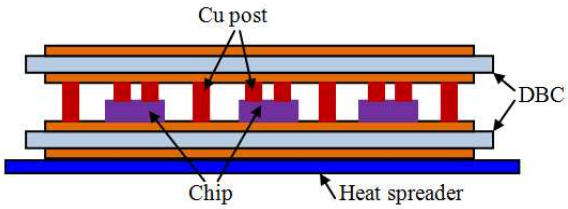


Figure 1.20 Illustration of MPIPPS module developed in 1999

In 2000, the solder bump was introduced into power electronics module to resolve the reliability issues encountered with MPIPPS. A series of bump interconnections, which have increased reliability, were evaluated and validated. The FCOF shown in Figure 1.21[12] and dimple array shown in Figure 1.22 were proven to be more reliable than MPIPPS.

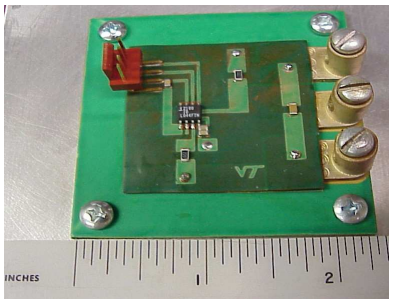


Figure 1.21 FCOF power electronic module developed by CPES [12]

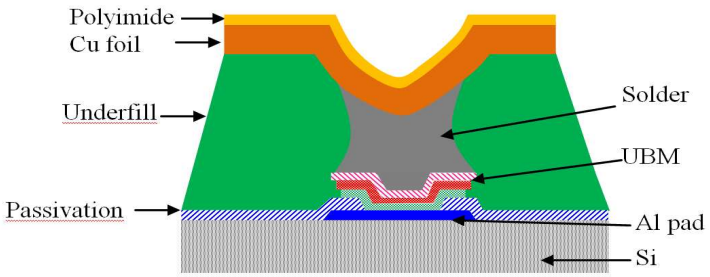


Figure 1.22 Illustration of Dimple array power module developed by CPES

Metal deposition interconnection was also employed to build two power electronics modules, the embedded power module shown in Figure 1.23 and the pseudo GE-POL shown in Figure 1.24, with the desired electrical performance.

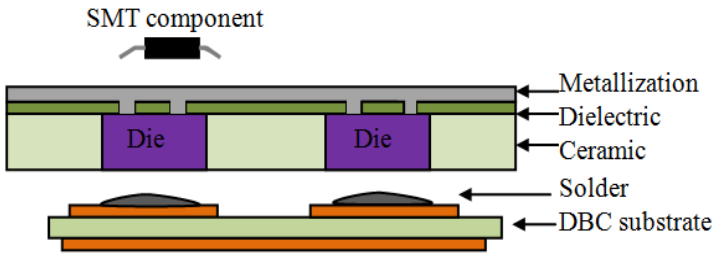


Figure 1.23 Illustration of Embedded Power module developed by CPES

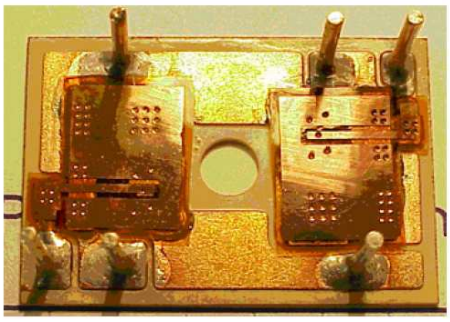


Figure 1.24 Pseudo GE-POL power module developed by CPES [13]

Finally, the high temperature interconnecting material, sintered nanoscale silver was synthesized. It can be applied to high temperature GaN or SiC power devices due to its high melting point.

1.4 The Focus of this Study

With the advent of high junction temperature power electronic device like GaN and SiC power devices and a high temperature working environment, packaging materials and technology are driven to withstand high temperatures. On the other hand, thermal management in the packaging design is becoming increasingly important for high temperature power electronic application. To evaluate the packaging for high temperature power electronic packaging, sintered silver and solder bump interconnections, are used in this study to improve electrical performance and heat dissipation. A planar structure is employed to realize double-sided cooling.

In one instance, one pair of high-temperature SiC devices are assembled in series into a planar power electronic module with only sintered nanoscale silver as the interconnection. The power module is then electrically characterized with a curve tracer. A reduction of the breakdown voltage of the module was observed and analyzed, and a solution is recommended and evaluated.

In the other instance, a solder bump interconnection is applied to planar packaging of a power IGBT device. The electrical performance of the packaging is characterized with a curve tracer, and found to have enhanced electrical performance.

1.5 The Organization of this Thesis

The thesis is divided into four chapters, arranged in the following sequence.

Chapter 1 reviews the evolution of general electronic packaging and power electronic packaging. The development of power electronic packaging at CPES is summarized. Finally, the focus of this study and the organization of the thesis are addressed.

Chapter 2 describes the packaging of a high temperature power module with a direct-bond planar structure in which two high temperature diodes in series are sandwiched between patterned and electroplated DBC. The materials selection, assembly process, and electrical characterization, along with the encountered issues, and their solutions, are addressed.

Chapter 3 concentrates on the application of solder bump interconnection to the packaging of IGBT power devices. The selection of materials, process control, and electrical characterization are described.

Chapter 4 summarizes this study and provides recommendation for future work.

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[13] J. G. Bai, "Low-temperature sintering of nanoscale silver paste for semiconductor device interconnection," *Ph.D Dissertation*, pp.5, Virginia Polytechnic Institute and State University, Blacksburg, VA 2005.

Chapter 2

High-Temperature Planar Packaging Using Sintered Nanoscale Silver as a Top Interconnect

This chapter describes the assembly of a bondwire-less planar structure with sintered nanoscale silver as the die attach and as the top interconnection materials, studies, evaluates and summarizes this structure. It is obvious that a planar packaging structure without bondwire should not only reduce or eliminate electrical parasitic effects like resistance and inductance, but should also enhance thermal transfer by reducing thermal impedance and realizing double-sided cooling. Lower-temperature sintered nanoscale silver, with a melting point of up to 961^{o}C, can be used as a substitute for solder to enable the packaging to tolerate a temperature close to silver's melting point as long as the device's junction temperature is below that temperature. It is known that some high lead solder alloys may possess a high melting point above 310^{o}C, but their peak processing temperatures must be 30-50^{o}C higher than the average processing temperature, which may compromise the device.

Moreover, in order to maintain good fatigue or creep strength and thus long term reliability, the melting point of the interconnect materials should much higher than the device's operating temperature. The higher the interconnecting material's melting point is, the better the reliability of the bonding will be. Lower temperature sintered nanosilver is an excellent candidate to enable the packaging to withstand higher temperatures, since its high melting point of 961^{o}C is much higher than that of other bonding materials.

2.1 Introduction

The direct bond interconnect, shown in Figure 2.1, has already commercially been applied to the packaging of normal power devices. For instance, IR and Denso have already improved their power modules using direct bonds [1]. However, although the planar structure has already been introduced to power electronic products, it has not been applied to the packaging of high-temperature power electronic devices. In this study, a power module composed of two diodes was series is built with a direct bond approach. Low-temperature sintered nanosilver was used as the die-to-top substrate/leadframe

interconnection, and the assembled module was electrically characterized with a curve tracer. The cross-section view of the module is shown in Figure 2.2.

Wide-bandgap semiconductor devices, such as those made with SiC, GaN, GaAs, InP, and diamond, are likely to have a higher power density, larger heat dissipation and wider operating temperature range[2-7] than conventional silicon devices. In particular, the high-voltage switching SiC diode used in public electric power distribution and electric vehicles [8-9] can operate at up to 600^{o}C [10]. High temperature power devices necessitate packaging materials to withstand correspondingly high temperatures. Similarly, high power electronic devices also require that the packaging design and materials have high heat-transfer efficiency. However, conventional die attach materials, such as solder alloy and electrically conductive epoxy, cannot tolerate such high temperatures. Moreover, the top interconnection with bondwire limits the heat transferring path to the die attach. Thus, in order to dissipate heat efficiently, the heat sink or heat plate can only be attached to the die attach side not wirebonding side. In other words, the wire-bonding approach constrains the thermal management to single-side cooling, thereby lowering the heat transferring efficiency.

To overcome these disadvantages of traditional packaging materials and design used in high temperature and high-power electronic devices, high-temperature bonding materials, sintered nanoscale silver, and the planar structure, which can enable double-sided cooling, were employed in this study. Solder alloy is commonly used to the bond die to the substrate, but most solder alloys' melting points are lower than 275^{o}C. Few solders have melting points of up to 400^{o}C, but their processing temperatures increase correspondingly, potentially impairing the device during the reflow process. However, sintered nanoscale silver not only possesses a very high melting point of 961^{o}C but can also be sintered below 300^{o}C. The relatively low processing temperature protects the die from damage during the assembly process and saves energy. In addition, sintered nanosilver has five times the electrical and thermal conductivity if most solder counterparts. Another bonus is that the low Young's module enables the bondline to have higher reliability than solder alloys.

From a processing perspective, nanoscale silver paste makes the realization of direct bond planar packaging structure easier than when using solder paste because

nanoscale silver paste does not flow during sintering. However, it is easy for solder to overflow during the reflow process if no solder mask or topper is applied to the die and the top substrate or leadframe. The extra process caused by soldering certainly increases the assembly cost.

The contribution of direct bond planar packaging structure to thermal management is the realization of double-sided cooling which is almost impossible when using wire-bonded packaging.

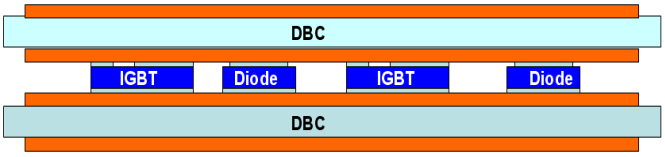


Figure 2.1 Schematic illustration of power electronic planar module

In this study, two power diodes in series were sandwiched between two silver over nickel electroplated DBC top and bottom substrates as shown in Figure 2.2 below.

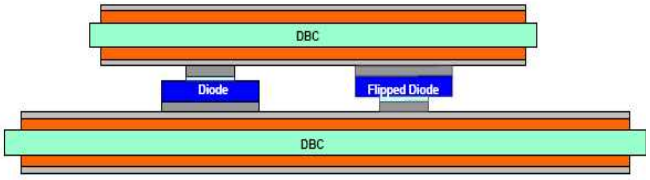


Figure 2.2 Cross-section view of power electronic module containing two diodes in series

2.2 Selection of Materials

a) Power Electronic Device

High-temperature SiC diodes with part number (P/N) CPWR-0600S010 from Cree, Inc. (NC, USA) were used in this study. The die's dimensions were $2.26\times2.26\times0.35mm^3$, as shown in Figure 2.3. The top was an anode with 4μm thick Al deposition, and the bottom was a cathode with 0.8μm thick Ni/Ag metallization. The anode pad size was $2.12\times2.12mm^2$ and the surrounding passivation/guardring was polyimide. The diode's electrical properties are summarized in Table 2.1 [11]. The device's junction temperature was 250^oC.

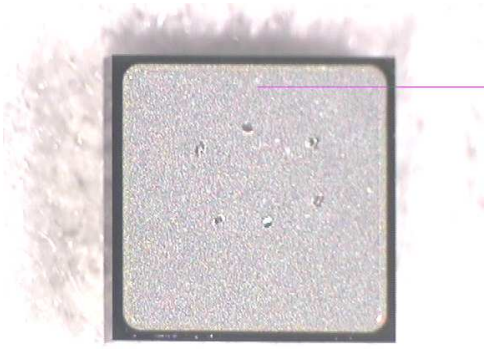


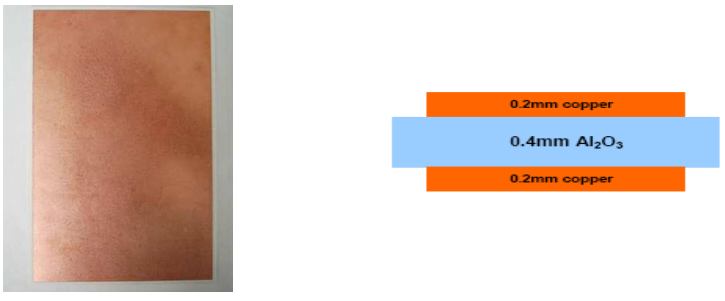
Figure 2.3 Power diode from Cree, Inc.

Table 2.1 Electrical properties of Cree power diode

Parameter		Symbol	Typ	Max	Units
Forward voltage	I_F=10A, T_J=25°C	V_F	1.6	1.8	V
	I_F=10A, T_J=150°C		2.0	2.4	
Reverse current	V_R=600V, T_J=25 °C	I_R	50	200	μA
	V_R=600V, T_J=150 °C		100	1000	

b) Top and Bottom Substrates

Direct bonded copper (DBC) from Curamik Electronics was used as the top and bottom substrates. DBC was a three-layer structure with one layer of electrically insulative ceramic sandwich-bonded with two layers of copper on each side, as shown in Figure 2.4.



(a) Top view (b) Side view

Figure 2.4 DBC substrate for power electronic packaging

DBC is made with a high temperature process to achieve an intimate bond

between the copper and the ceramic [12]. This was no solder or any other bonding materials used in the interface between copper and the ceramic surface. Rather, the combination of copper and ceramic was heated to about 1070^{o}C, slightly below copper's melting point, in an inert atmosphere. At this temperature, the copper oxides forms a eutectic melt that wets and then cools to form a strong bond between copper and ceramic [13].

Commercially, the ceramics used as insulating materials usually include Al_2O_3, AlN, Si_3N_4 and BeO. Aluminum oxide was used in this study because it was easily available in the commercial market and processable. As for AlN and Si_3N_4, they needed to be pretreated to be bonded with copper; they required an additional oxidation process at about 125^{o}C. The penalty of this extra process was the added oxygen diffused along the grain boundary which may downgrade the thermal conductivity of AlN and Si_3N_4 [13]. Although BeO has excellent thermal conductivity, it is seldom used commercially due to its toxicity.

DBC offered the following advantages for power packaging [14]:

- The copper and ceramic tend to act, through bonding, like an integral unit with a single coefficient of thermal expansion (CTE). This CTE was much lower than that of pure copper and more closely matches to that of the ceramic. Therefore, it was possible to solder even large-area chips directly onto the copper layer without risking stress damage.
- The copper used was of the high-purity, oxygen-free high-conductivity (OFHC) type. With proper line width and thickness, the metallization could be of very low electrical resistance and could handle a current well in excess of 100A.
- The thick layer of copper provides efficient heat spreading for the power chips.
- DBC was also corrosion resistant.

c) Interconnection Materials

Nanoscale silver paste (nanoTach®) from NBE Tech, LLC (VA, USA), was used as both bottom and top interconnections. The Nanoscale silver paste was a type of paste made up of nanoscale silver particles (30-50nm) and other organic substances, including dispersant/surfactant, binder and thinner [15]. It could be sintered at a temperature lower

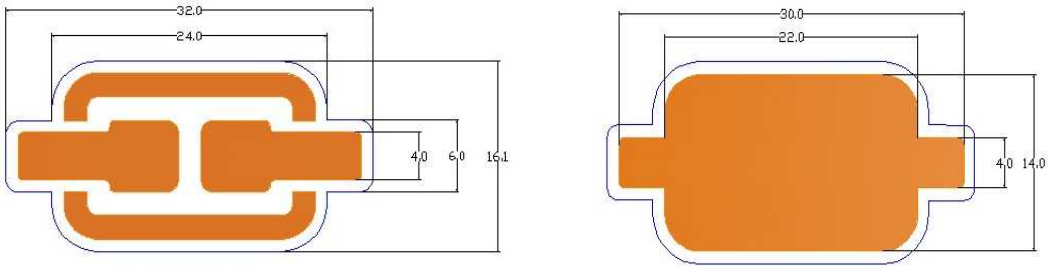
than 300°C, and the sintered nanoscale silver had some advantages over solder alloys and conductive epoxies, listed in Table 2.2 [16].

Table 2.2 Features of sintered nanoscale silver

Interconnecting materials	NBE's nanoTech®	High-lead solder (95Pb5Sn)	Eutectic AuSn solder	Hysol®QMI 3555R (epoxy)
Process temperature	<280°C	340°C	320-340 °C	300-450°C
Maximum use temperature	<961°C	<280°C	<280°C	<250°C
Bonding shear (MPa) (strength)	20-40	15	>100	20
Elastic modulus (GPa)	9	19	80	11.5
Electrical conductivity,10^5 $(\Omega \cdot cm)^{-1}$	3.8	0.45	0.625	$6.7x10^{-7}$
Thermal conductivity (W/K·m)	240	23	58	80
ROHS compliancy	Compliant	Not compliant	Compliant	Compliant

2.3 Design and Fabrication of Substrates

The layouts of the substrates were designed using AutoCAD 2007 and shown in Figures 2.5 and 2.6 where the yellow color stands for copper, the white color for ceramic, and the blue color for the outline of ceramic. Since copper etching was batch processed, as many single substrates as possible should be distributed in one DBC panel to efficiently use DBC materials. As shown in Figure 2.7 and 2.8, a total of sixteen boards/substrates could be arranged in one panel.



(a) Top side (b) Bottom side

Figure 2.5 AutoCAD drawing of bottom substrate layout (unit: mm)

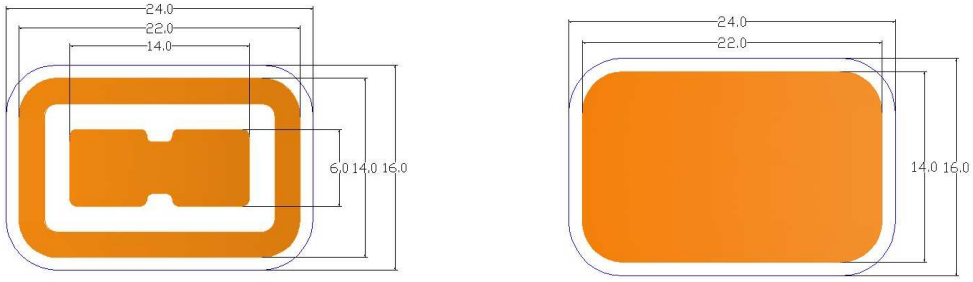
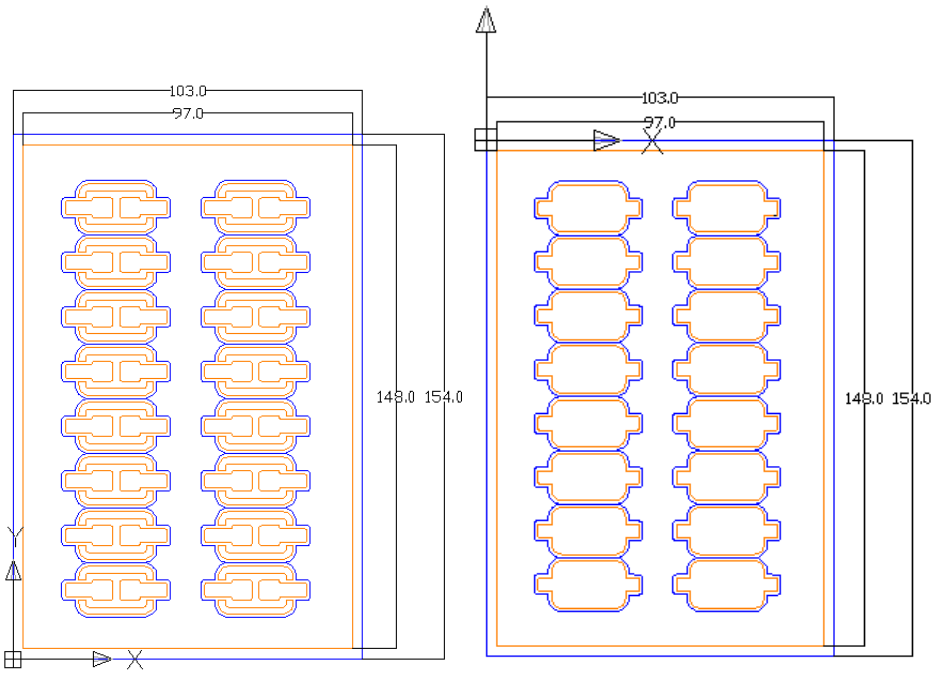


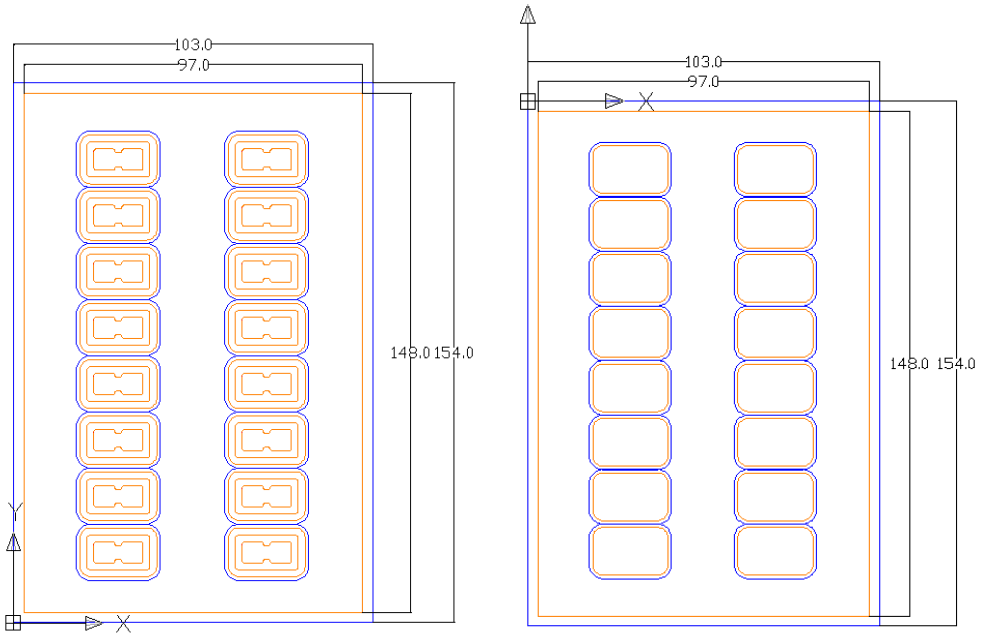
Figure 2.6 AutoCAD drawing of top substrate layout (unit: mm)

To transfer an AutoCAD layout drawing to a DBC panel, a RESONETICS laser cutting machine (Resonetics Micormaching Technology, Nahsua, NH, USA), shown in Figure 2.9, was used to cut the 2.5mil-thick polyimide Kapton® which was flatly applied onto the surface of DBC panel, as shown in Figure 2.10. Instead of using a hand, a soft rubber roller was used to apply Kapton® tape as it could press and push the tape evenly onto the DBC panel and avoided trapping any air bubbles between the tape and the DBC. As for the laser cutting of the tape, the two process parameters, laser power and pulse number, were be set to be 25-30W and 10-20cycles, respectively, to ensure high dimension resolution, as shown in Figures 2.11 and 2.12.



(a) Top (b) Bottom

Figure 2.7 Panel layout of bottom substrates (unit: mm)



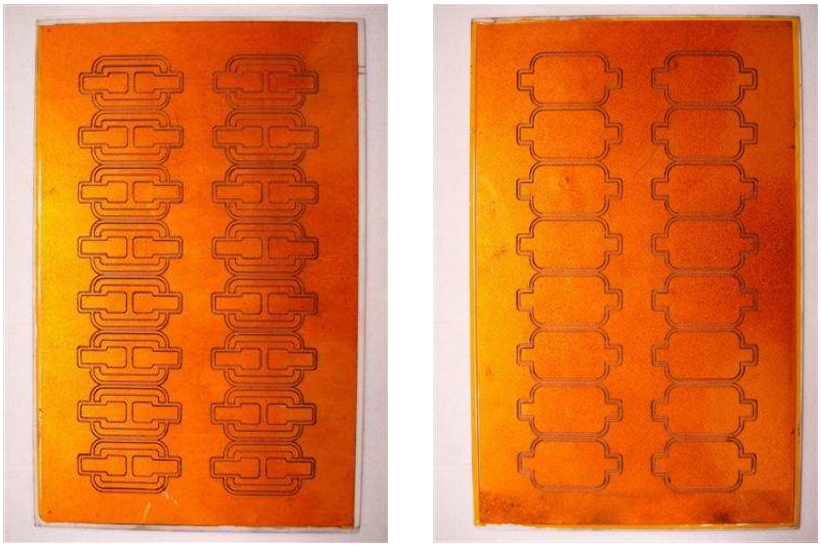
(a) Top (b) Bottom

Figure 2.8 Panel layout of top substrate (unit: mm)

Figure 2.9 Laser cutting machine to cut tape and ceramic

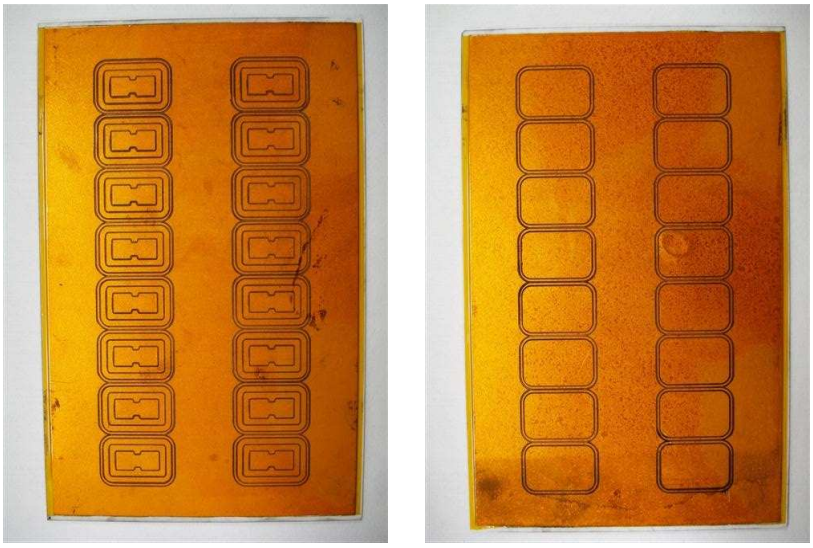
Figure 2.10 DBC panel covered with Kapton® tape

After the tape was laser cut, the unnecessary tape was removed from both sides of the DBC substrate, leaving the sample shown in Figure 2.13. Subsequently, the DBC panel with exposed copper was put into a Model BTD-201B, Bench-Top Developer (from Kepro Circuit System Inc. Fenton, MO, USA) shown in Figure 2.14, to remove unwanted copper. To etch away the copper, the etching solution ferric chloride ($FeCl_3$) was pressure-sprayed onto the DBC panel. The unmasked copper was removed through substituting chemical reaction.



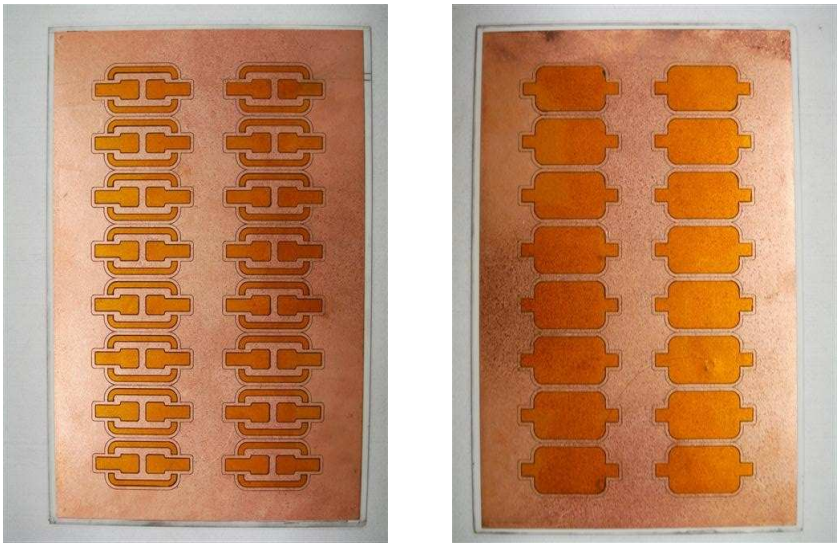
(a) Top side (b) Bottom side

Figure 2.11 Laser cutting of tape on bottom DBC substrate



(a) Bottom side (b) Top side

Figure 2.12 Laser cutting of tape on top DBC substrate



(a) Top side (b) Bottom side

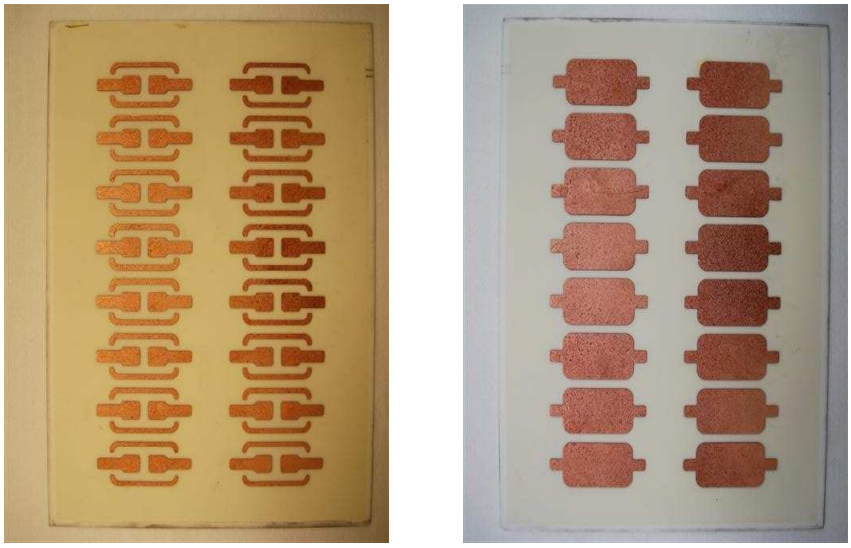
Figure 2.13 Bottom substrate after being stripped of tape

Figure 2.14 Copper-etching equipment

Upon the completion of copper etching, the etched DBC was taken out and immediately rinsed with tap water; otherwise, the etching solution residue would stick to the ceramic surface and contaminate the DBC substrate. Then, the remaining tape used to mask the copper during etching was stripped off from the etched DBC panel. The etched and stripped DBC panels are illustrated in Figures 2.15 and 2.16.

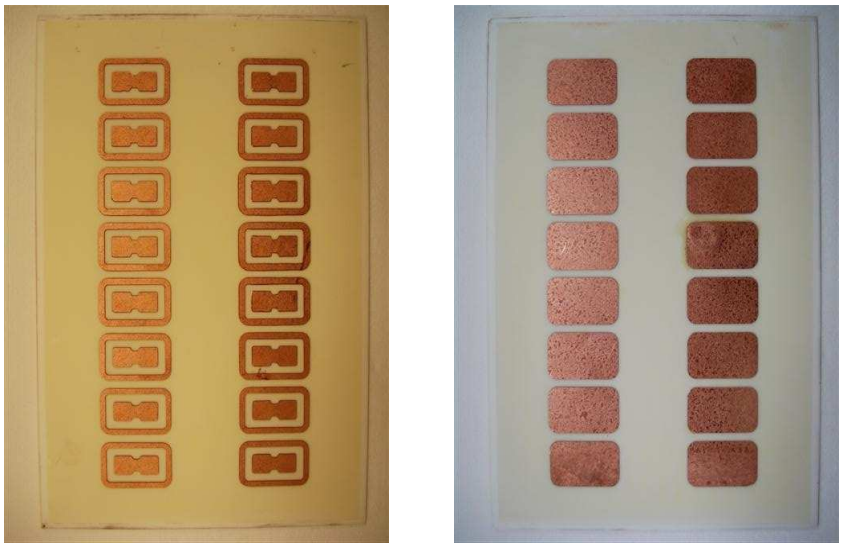
To de-panel the patterned DBC panel, a laser cutting process was employed again. A high laser power of more than 60W with a pulse of more than 600 cycles was used to

cut the ceramic Al_2O_3, as shown in Figures 2.17 and 2.18. During laser cutting, the individual board on the panel was attached to the work station temporarily to prevent the board from moving around.



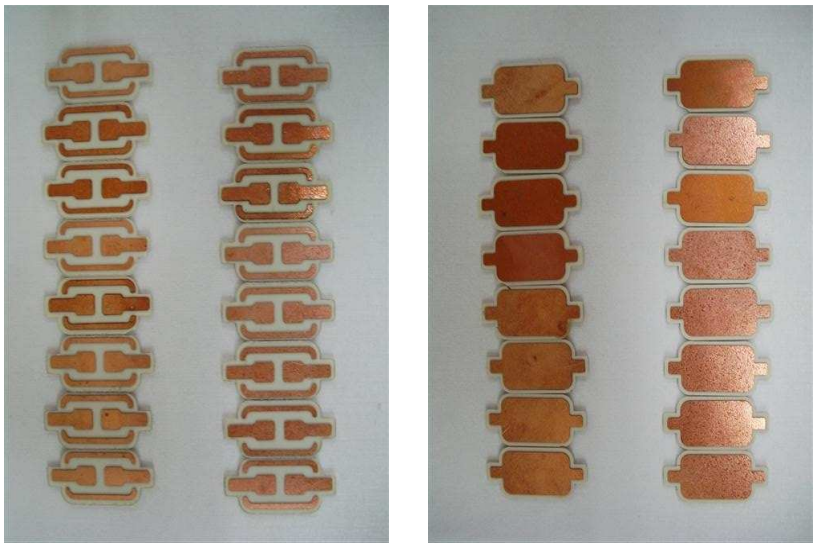
(a) Top side (b) Bottom side

Figure 2.15 Bottom DBC substrate panel after etching and stripping off the tape



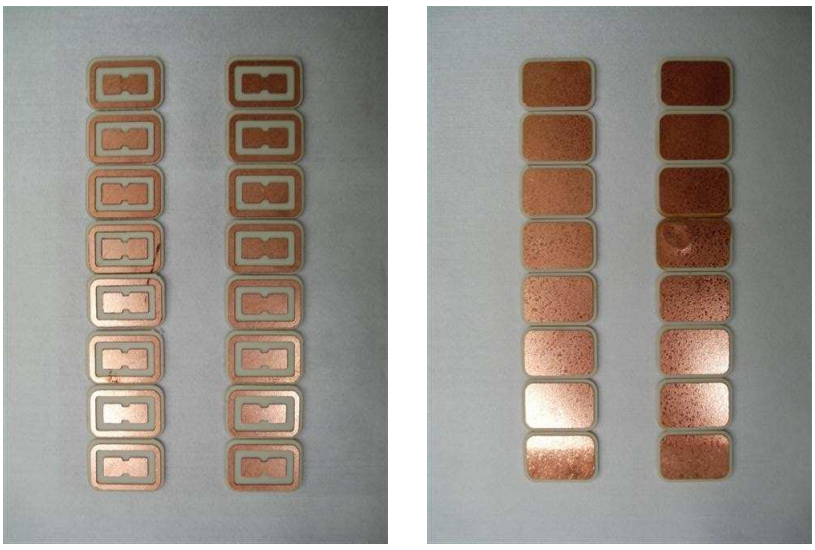
(a) Bottom side (b) Top side

Figure 2.16 Top DBC substrate panel after etching and stripping off the tape



(a) Top side (b) Bottom side

Figure 2.17 Bottom DBC substrate panel after laser cutting



(a) Bottom side (b) Top side

Figure 2.18 Top DBC substrate panel after laser cutting

Finally, the electroplating of silver over nickel on the patterned DBC substrate needed to be performed for the copper pad be soldered or sintered. Also, the

electroplating of noble metals such as silver or gold would protect the copper trace from further oxidation or corrosion during high-temperature processes or unfavorable service conditions. Since nanosilver paste is used as the interconnection material, the best surface finish candidate in terms of diffusion and reliability was silver metallization.

Prior to electroplating silver over nickel on the DBC substrate, the Model M20B, wedge wire bonder (Orthodyne Electronics, Irvine, CA, USA) shown in Figure 2.19 was used to bond 10 mil aluminum bondwire between the separated copper pads or traces to make them electrically connected, as shown in Figure 2.20, as the electroplating necessitated electrical current going through all copper to be plated.

Electroplating of silver over nickel started with the alkali solution (90%NaOH) cleaning of acidic substances on the DBC surface and nitride acid (10%HCl) solution removal of oxide from the DBC substrate. The cleaned DBC was put into a nickel-plating bath to plate nickel over the DBC. Before the strike plating of silver, the nickel-plated DBC was dipped into a cyanide solution to improve the silver's adhesion to nickel. Finally, the strike-plated silver was put into a silver-plating bath to the plate silver. The thickness of plated nickel and silver are each 10μm. A DC power supply was used to provide electrical current which was controlled at $20mA \cdot cm^{-2}$. The entire setup is shown in Figure 2.21. The entire electroplating process is illustrated in Figure 2.22. The total plating time for nickel and silver was about 8-10 minutes each. The strike plating of silver took 10-15 seconds. During plating, a mild stirring of the plating solution was activated. After the plating of silver, the DBC was flushed with tap water, and then with deionized water and alcohol to that ensure that no residue was left on DBC surface. The nickel/silver-plated top and bottom DBC substrates are shown in Figure 2.23.

Figure 2.19 Wedge wire bonder

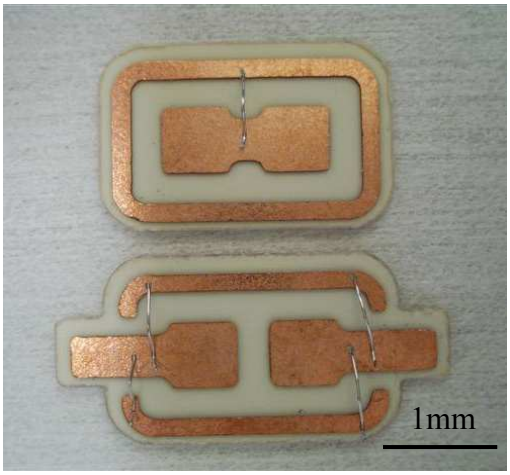


Figure 2.20 Wire-bonded substrates

Figure 2.21 The setup of nickel/silver electroplating

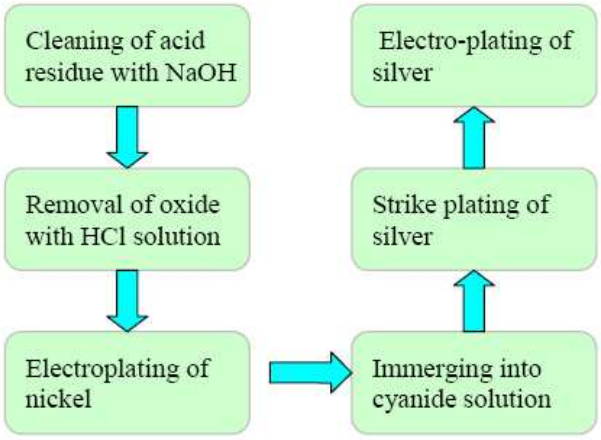


Figure 2.22 Process flow chart of nickel/silver electroplating on DBC

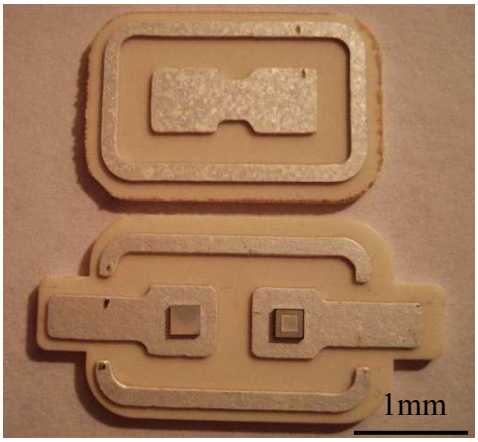


Figure 2.23 Silver over nickel plated top and bottom DBC substrates

2.4 Solderable Metallization of Wire-bondable Die Pad

Since an as-received device's aluminum pad is designed and fabricated for wire bonding and not soldering, it is necessary to make the die pad solderable or sinterable by metallization. In this study, an Auto306, Edwards radio frequency (RF) sputtering unit shown in Figure 2.24 was used to deposit three different thin-film metal layers: titanium, nickel, and silver. The first 0.2-0.4μm thick titanium layer was the adhesion layer which can adhere well to the device pad; the middle 3-4μm thick nickel layer was a barrier that prevents the inter-diffusion between titanium and silver; and the last 1-2μm silver layer

was the wetting layer. The structure of the three-metal deposition is illustrated in Figure 2.25.

Figure 2.24 RF sputter for deposition of thin metal film

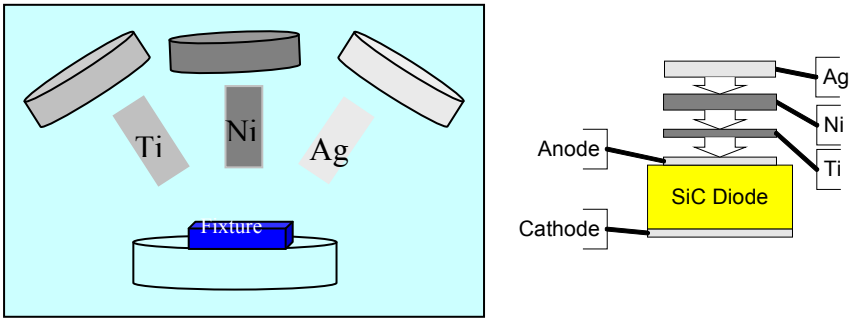


Figure 2.25 The schematic illustration of three-layer metal deposition

Before they were loaded into the chamber, the dies were cleaned by PLASMA-PREEN® II-973 (Plasmatic Systems Inc, North Brunswick, NJ, USA) microwave argon plasma cleaner (shown in Figure 2.26) to ensure good adhesion between the titanium layer and the die pad. To deposit metals in the designated pad area, an aluminum fixture (shown in Figure 2.27) with a stainless mask was used to fix and mask the dies during sputtering.

Figure 2.26 Plasma cleaner

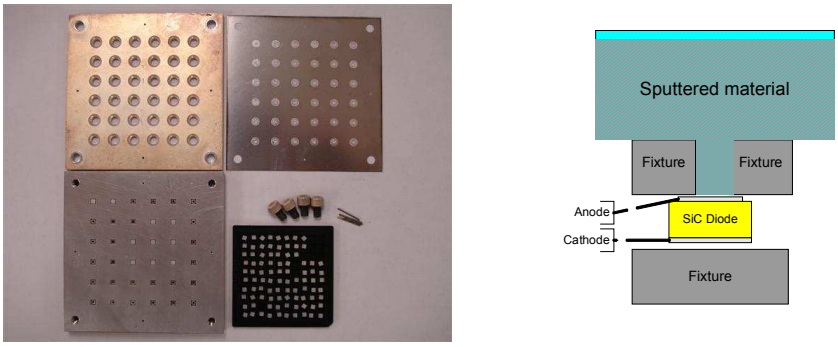
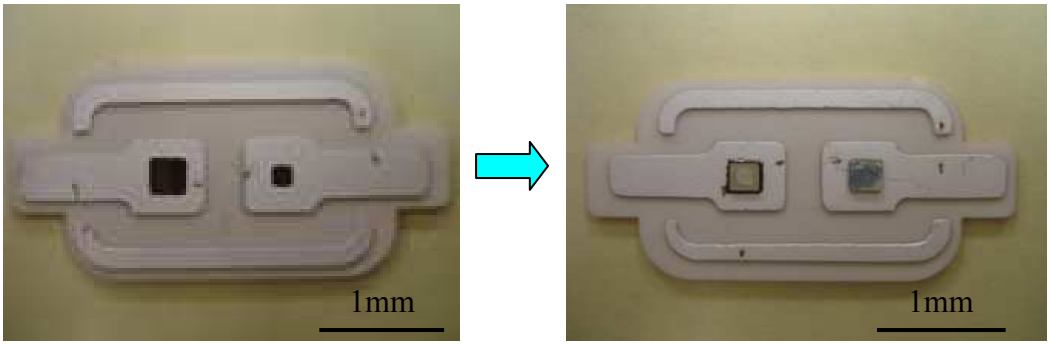


Figure 2.27 Fixture for masking dice during sputtering

2.5 Assembly Process

In general, the assembly process included the printing of the nanoscale silver paste, the die attachment, and the sintering of the nanoscale silver paste.

First, a 0.0635mm (2.5mil) thick polyimide tape was used as a stencil to print nanosilver paste onto the bottom DBC substrate. Two apertures were made on the tape: one was 2.5x2.5mm^2 for normal die attachment; the other was 1.1x1.1mm^2 for the flipped die attachment. Following the printing of the nanosilver paste, the two dies were placed on top of the paste: one is the normal die attachment, and the other is flipped and then attached, as shown in Figure 2.28.



(a) Printing of paste (b) Die attachment

Figure 2.28 The printing of nanosilver paste on the bottom substrate and die attachment

Secondly, the printed paste was sintered with a SIKAMA conduction belt oven (shown in Figure 2.29) according to the sintering temperature profile shown in Figure 2.30 [16].

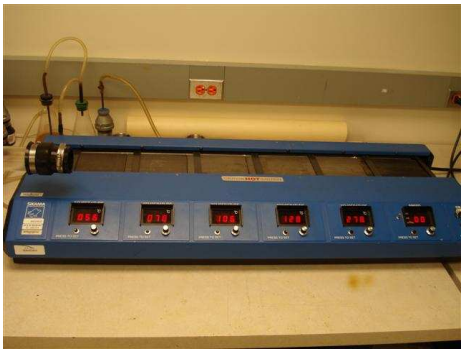


Figure 2.29 The belt oven for sintering nanosilver paste

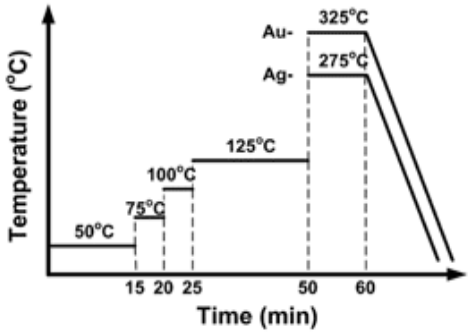
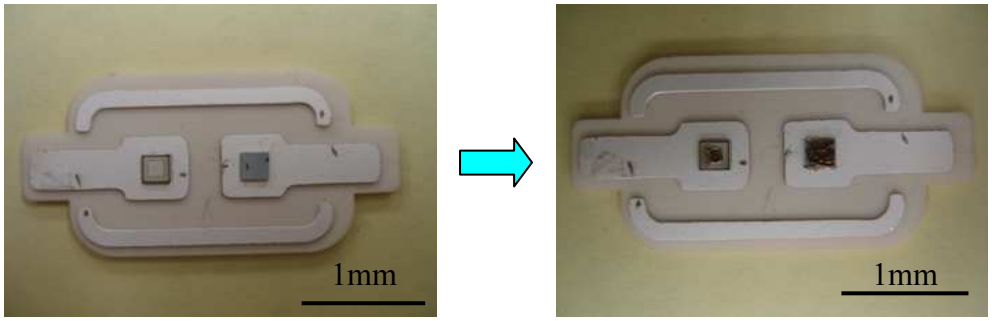


Figure 2.30 Temperature profile for sintering nanoscale silver paste

The entire sintering profile was divided into five stages corresponding to the oven's five thermal zones; the first four stages were mainly used to get rid of organic substances such as the dispersant, binder, and thinner, and the last stage is the sintering stage in which nanoscale silver is solidified and made as dense as possible. After the sintering of the once-printed nanoscale silver, nanosilver paste was printed on the two dies; the smaller area of paste is on the sputtered pad, and the larger area of paste is on non-sputtered pad, as shown in Figure 2.31.

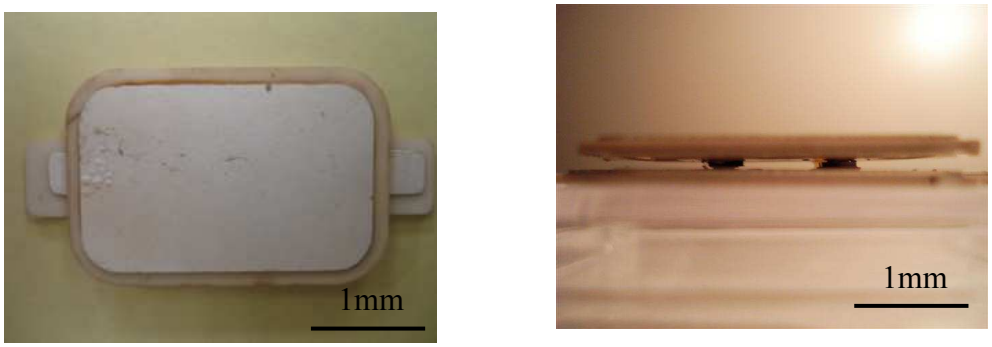


(a) Sintered (b) Printing of paste on dice

Figure 2.31 Die attachment with sintered nanoscale paste and the second printing

Finally, the top substrate was put on the top of the dies and aligned by outline. The whole packaging was put on the belt oven and sintered again. The assembled module is shown in Figure 2.32.

The entire assembly process flow is summarized in Figure 2.33.



(a) Top view (b) Side view

Figure 2.32 Power module with sintered nanosilver paste as an interconnection

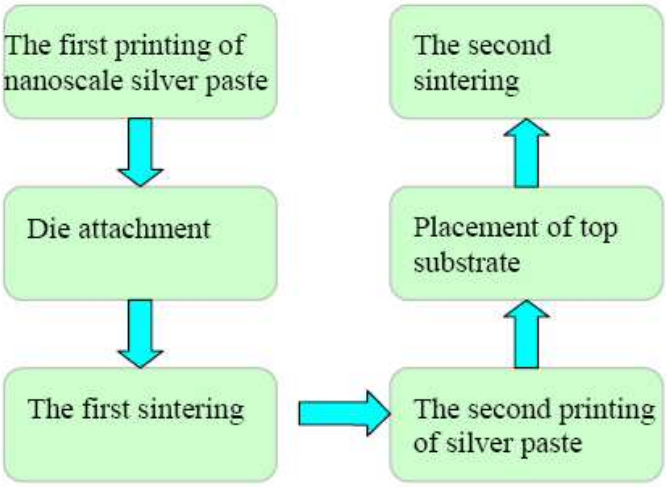


Figure 2.33 Assembly process flow for building power electronic power with sintered nanoscale silver

2.6 Electrical Characterization

The Tektronic, 371 high power curve-tracer shown in Figure 2.34 was used to measure the forward and reverse current and voltage of the bare dies and the assembled module. Before the measurement, the two probes' resistance was measured by shorting the two probes together, as shown in Figure 2.35. The sum of the resistance of two probes was measured to be 1.21Ω, as shown in Figure 2.36. Also, the forward I-V currents of the two bare dies were measured and compared as shown in Figures 2.37 and 2.38. From these two figures, the on resistances of the two bare dies were calculated to be 1.32Ω and 1.41Ω, respectively.

Figure 2.34 Curve tracer for measuring current and voltage

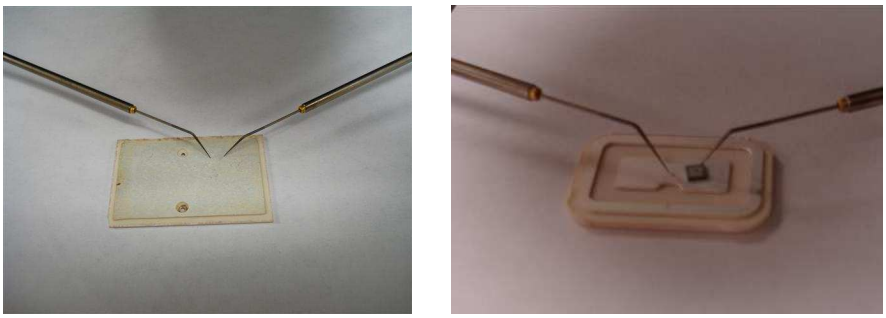


Figure 2.35 The setup for the I-V measuring of two probes' resistance and the die

Through deduction of the probes' resistance, we found that the actual on-resistances of two bare dies are 0.11Ω and 0.20Ω, respectively.

Before the two dies were assembled, the forward and reverse I-V curves the two sputtered dies were measured, as shown in Figures 2.39, 2.40, 2.41, and 2.42, respectively.

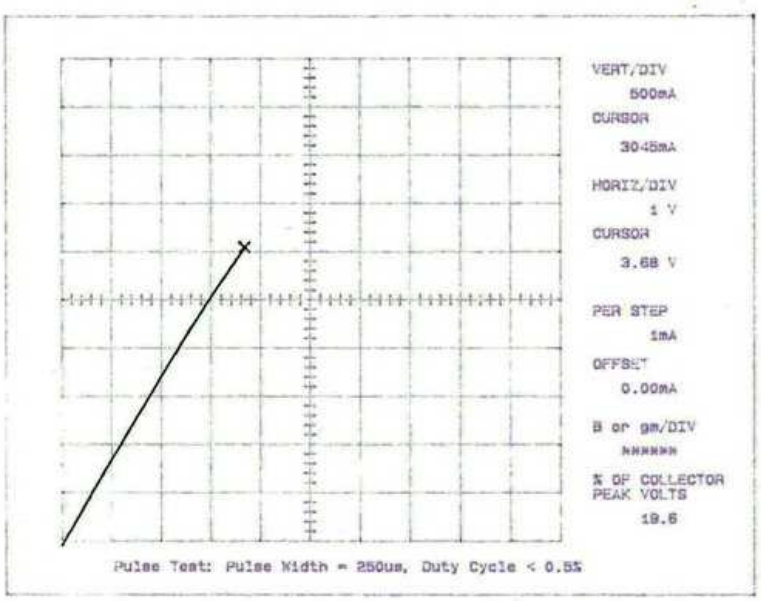


Figure 2.36 The current-voltage measurement of two probes

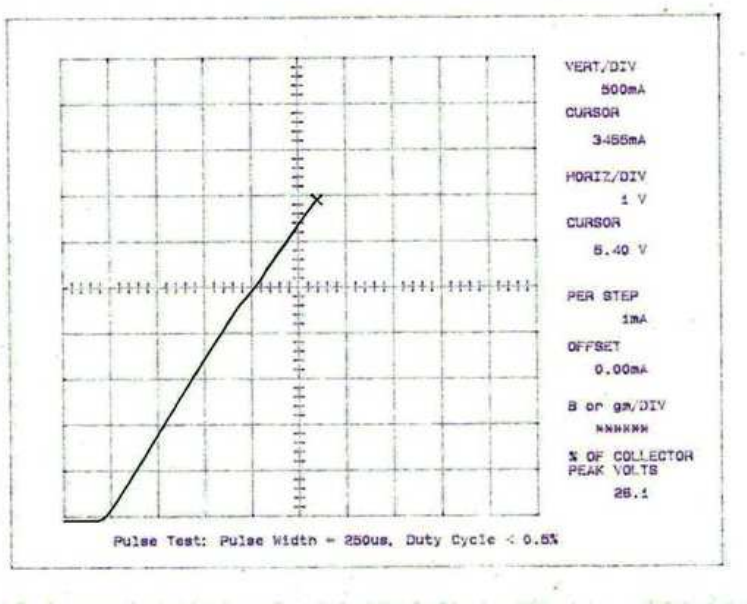


Figure 2.37 Forward I-V curve of bare die one

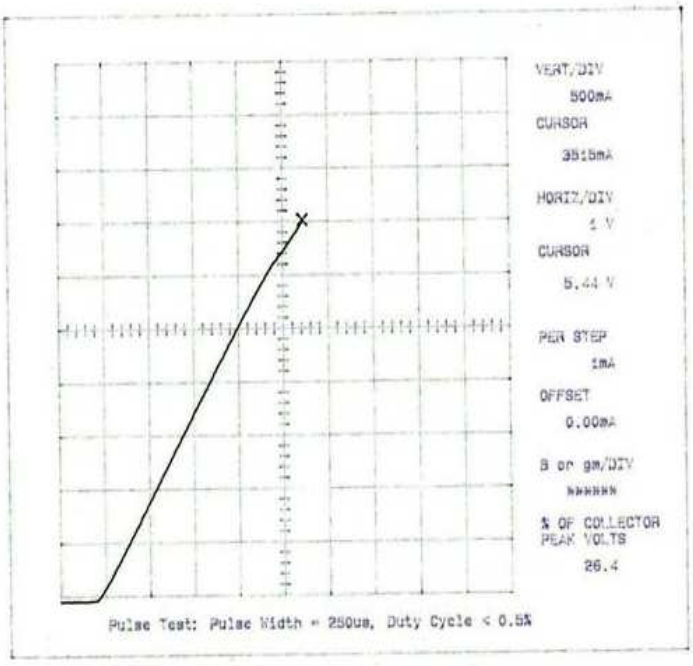


Figure 2.38 Forward I-V curve of bare die two

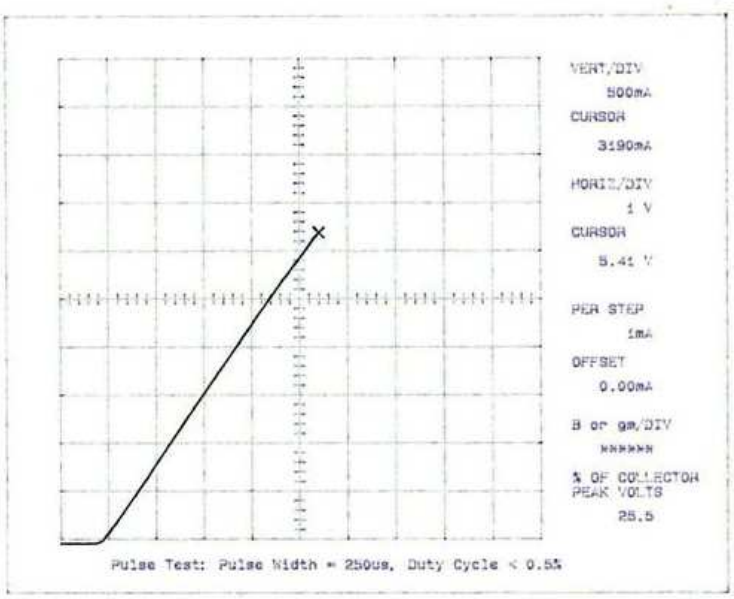


Figure 2.39 Forward I-V curve of sputtered die one

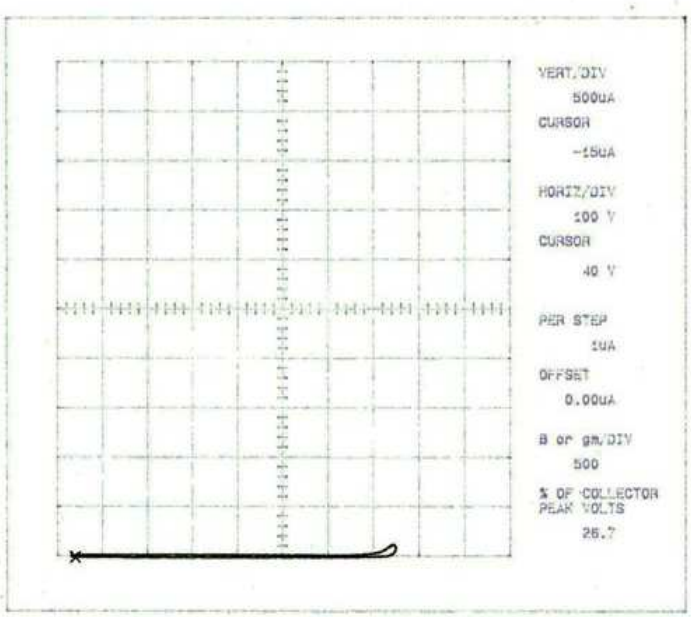


Figure 2.40 Reverse I-V curve of sputtered die one

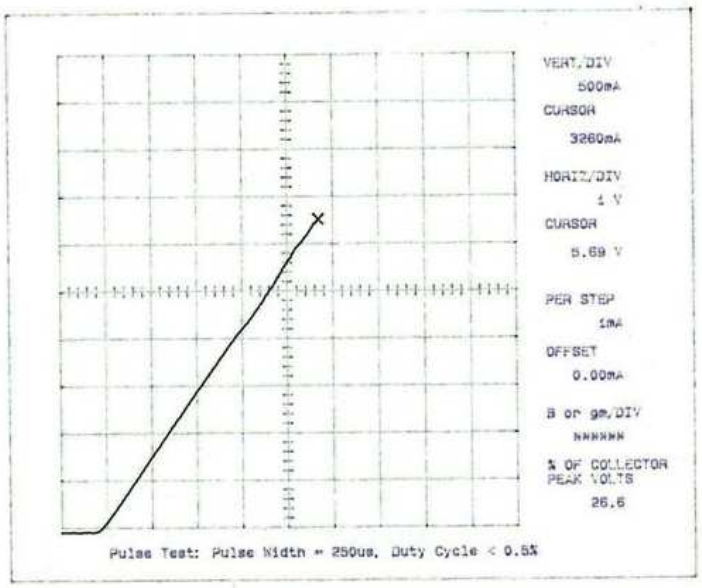


Figure 2.41 Forward I-V curve of sputtered die two

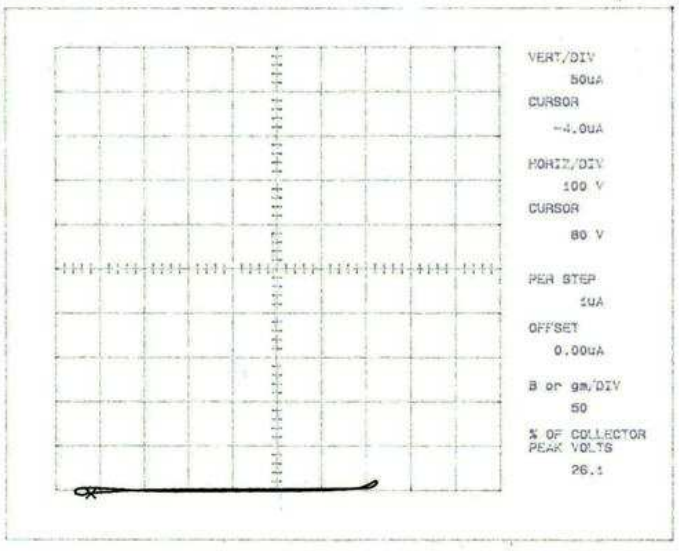


Figure 2.42 Reverse I-V curve of sputtered die two

From Figure 2.39, the on-resistance of sputtered die one was calculated to be 1.45Ω. Without the probes' resistance, it was 0.14Ω. The reverse breakdown in Figure 2.40 was about 720V at 15μA. The parameters of die two were calculated from Figures

2.41 and 2.42, and show that the on-resistance was 1.48Ω or 0.17Ω without probes' resistance. The breakdown was 710V at 4μA. Compared with the bare dies, the two dies' resistances increased by 118% and 35%, respectively.

Forward and reverse current-voltage (I-V) measurements were conducted on the planar power modules. The results were shown in Figures 2.43 and 2.44, respectively. The on-resistance of the module was 1.47Ω or 0.26 Ω without probes' resistance, and the reverse breakdown was only 1.16kV, which was much lower than the sum of the two dies' breakdown voltages. The breakdown voltage dropped from 1.43kV to 1.16kV by a reduction of 270V. However, it can observed that the total resistance of two diodes packaged in the module is much less that sum of individual resistance which was (0.24+0.27) Ω=0.51Ω. Two factors contribute this discrepancy: one was that an individual die was measured when the die was put on the top of subtrate without bonding, but the two dies in the module were bonded to the substrate with sintered nanosilver; the other has excellent electrical conductivity of the sintered nanosilver enable the measurement to be lower than that without bonding and sintered silver.

In order to improve the breakdown voltage of the module, the module was immerged into liquid Fluorinert, as shown in Figure 2.45, which was a type of very low-viscosity liquid that possessed a higher dielectric strength than air; the dielectric strength of Fluorinert was about 15MV/m, which was five times air's dielectric strength. The Fluorinert liquid did completely fill the gap between the top substrate and the guard-ring of the die.

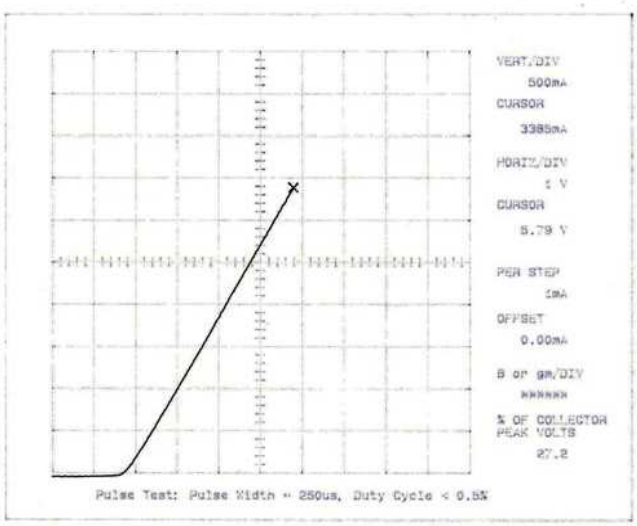


Figure 2.43 The forward I-V curve of the power module (probed) (250^{o}C)

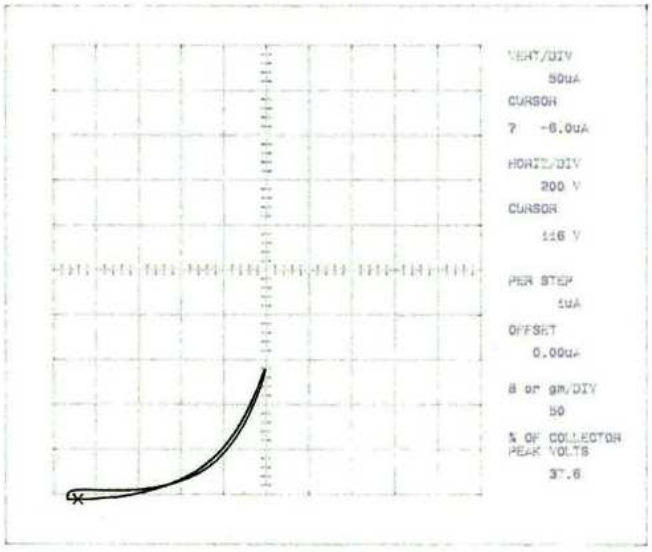


Figure 2.44 The reverse I-V curve of the power module (probed) (250^{o}C)

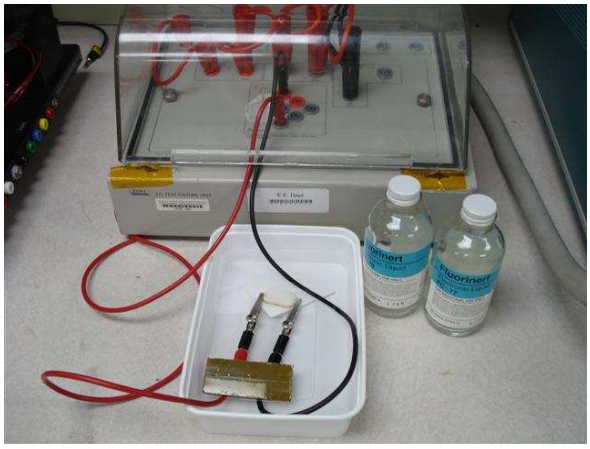


Figure 2.45 The power module immerged into Fluorinert

Clips with lower parasitic resistance were used to contact the two terminals of the module. The forward I-V curve was measured, and is shown in Figure 2.46; from this the on-resistance was calculated to be 0.39Ω, including the resistance of the clips.

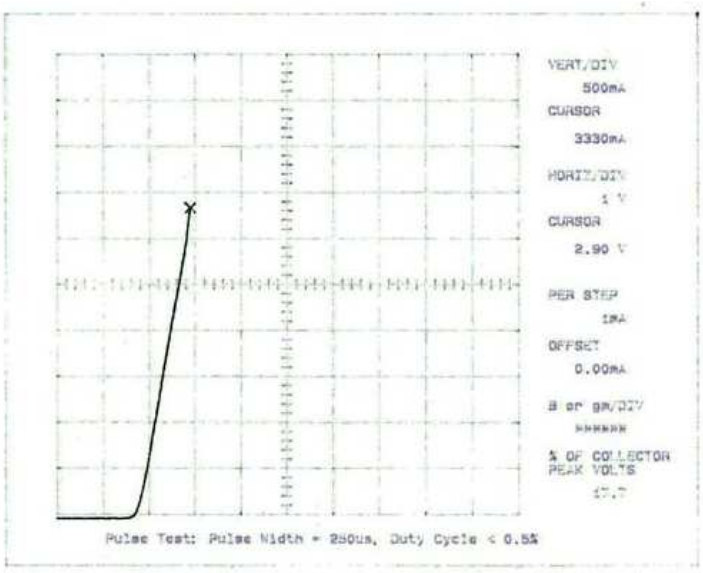


Figure 2.46 Forward I-V curve of power module (clipped) (250^{o}C)

The breakdown voltage of the module in Fluorinert shown in Figure 2.47 was about 1.4kV at 50μA. The breakdown voltage improved from 1.16kV to 1.4kV, which was an improvement of 240V. This was because the narrow 25-50μm (1-2mil) gap between the top substrate and the guard-ring of the die was free air and was easily

electrically broken through, causing whole module's breakdown strength to drop. The Fluorinert with its high breakdown strength can effectively improve the breakdown voltage of the direct-bond planar structure power module by filling the narrow gap between the top DBC substrate and the guard-rings of the diodes.

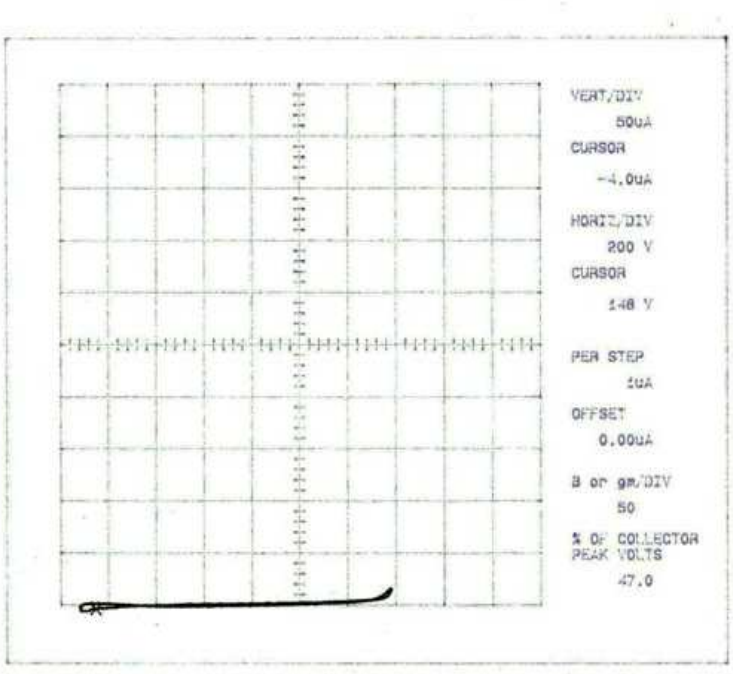


Figure 2.47 The reverse I-V measurement of power module in Fluorinert (250^{o}C)

2.7 The Inspection of Die Attachment Bondline

Following the electrical characterization of the direct bond planar power module, a cross-section of the bondline was taken to inspect integration and bonding of the structure. The optical micrograph of the bondline cross-section is shown in Figures 2.47 and 2.48.

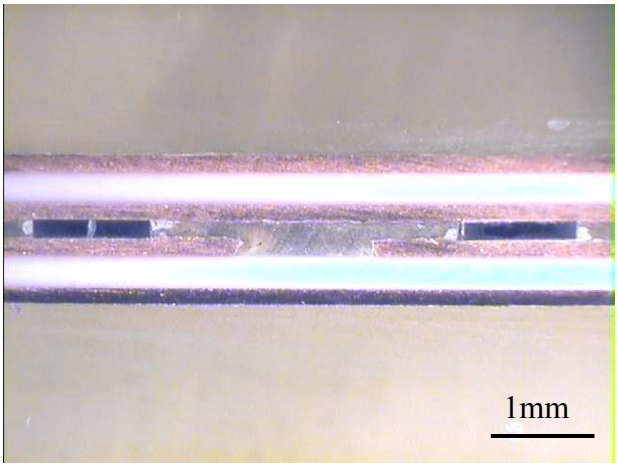
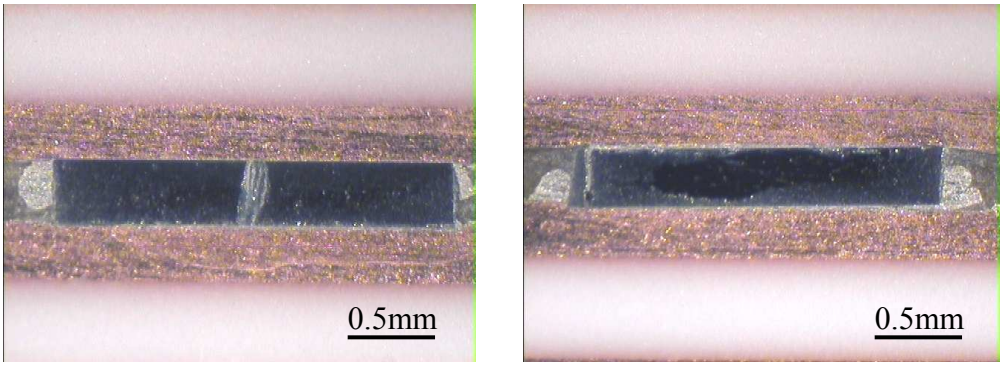


Figure 2.48 The micrograph of bondline cross-section of the planar power module (direct bond)



(a) Flipped die (b) Normal die

Figure 2.49 The micrograph of bondline cross-section of the individual die in the power module

From the above figures, it can be seen that the two dies were bonded between two layers of DBC with a thin layer of sintered nanoscale silver. The bondline made of sintered nanoscale silver was very thin at about 25-50μm (1-2mil). The nanoscale silver paste would shrink by half after sintering. The free air in the narrow gap between top substrate and the top the guard-ring can be easily broken through, resulting in a drop of the reverse break down voltage of the assembled diodes. To accommodate the negative effect of the narrow gap in the reverse breakdown voltage, a high-dielectric insulative

encapsulant may be employed to fill in the free air gap to improve the break down voltage.

2.8 Conclusions and Recommendations

Planar packaging of a high-temperature power device direct-bonded with sintered nanoscale silver was successfully built. The forward I-V measurement was desirable due to high electrical conductivity of sintered nanoscale silver, but the reverse breakdown drops due to the 25-50μm (1-2mil) gap between the top substrate and the guard-ring of the die. The root cause of the breakdown voltage drop was identified and validated using high dielectric strength liquid Fluorinert. However, for actual application, a type of curable polymer, top fill or encapsulant, needs to be applied. With cured polymer, both the breakdown voltage and reliability of the module will be improved. To reduce the mismatch of CTE between the top substrate and the top fill, some dielectric particles may be mixed into the topfill epoxy. Moreover, the surrounding area of bonding pad on top substrate may be etched down to increase the gap between top substrate and guard-ring of the diode die.

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Chapter 3
High Temperature Planar Packaging Using Bump Interconnect

In this part of the study, a high-lead solder ball was used as an interconnect instead of using sintered nanoscale silver to overcome the breakdown voltage drop encountered in Chapter 2. The 0.5mm-diameter solder ball can increase the gap between top substrate and guard-ring of the die, which is only 0.05mm (2mil) in the module built with sintered nanoscale silver in Chapter 2.

To simplify the assembly process, only one die was used in the packaging to improve the breakdown voltage drop issue. The planar packaging was processed, built, and electrically characterized as described in Chapter 2.

3.1 Introduction

An alternative approach to removing bondwire from power electronics packaging is to use solder bump instead. However, the melting point of most lead free solder alloys is below 300^{o}C although solder bump can widen the gap between the top substrate and the guard-ring. High-power, high-temperature SiC devices have some requirements beyond those of a low-temperature power device; they must have efficient thermal management, high voltage insulation, surface leakage passivation, moisture resistance, corrosion protection, and mechanical protection [1]. For high-temperature packaging, the packaging needs to tolerate a temperature above 250^{o}C.

It is very difficult for conventional packaging materials to meet the requirements of high operating temperatures. For example, most soft solders including lead and lead-free solders, have a melting point lower than 250^{o}C. Only high-lead solders which are not compliant with ROHS or WEEE regulations or expensive Au-containing solders possess a melting point of above 250^{o}C [2].

In this study, sintered nano-silver was adopted to attach the die to the bottom DBC substrate. A high-lead solder bump with a composition of PbSn5Ag1.5 was used as a top interconnection between the top substrate and the die.

Other high-temperature packaging materials such as a lead frame, encapsulant, and epoxy were carefully selected. The packaging was also electrically characterized with a curve tracer.

3.2 Packaging Design and Materials Selection

The same high-temperature diode used in Chapter 2 was die-attached to the bottom DBC substrate. The high-lead PbSn5Ag1.5 solder ball was attached to the die's sputtered pad with a high-lead PbSn12Ag2 solder paste, and a Kovar terminal pin was soldered to the top of the solder ball with PbSn12Ag2 solder paste. The Kovar terminal pin protruded through the hole in the top DBC substrate. A middle layer of ceramic with an opening in the center for the die was placed between the bottom and top DBC substrates to raise and strengthen the packaging. A pair of thermal coupling wires were inserted through a via on the top DBC substrate and soldered onto the inner side of the top DBC substrate. The whole structure is illustrated in Figure 3.1, and the high-temperature packaging materials used are listed in the Table 3.1.

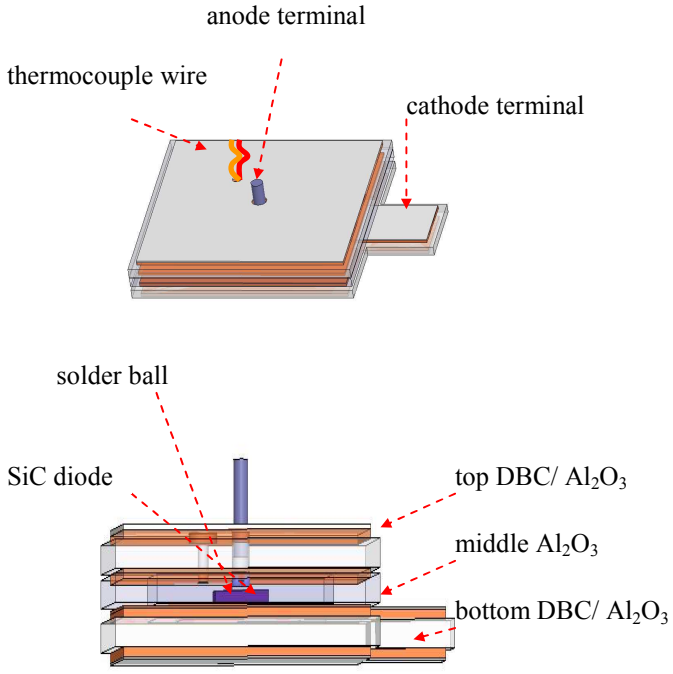


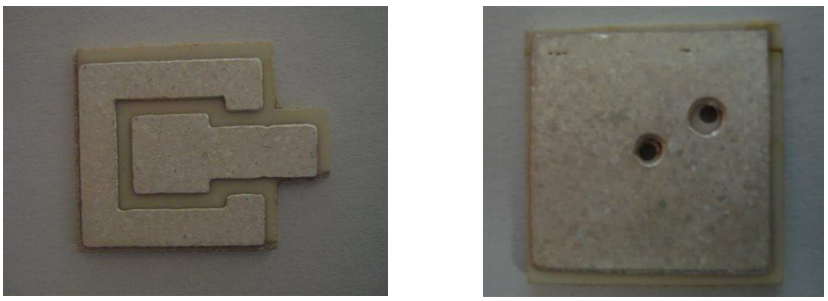
Figure 3.1 Packaging Structure

Table 3.1 The list of packaging materials

Materials	Function
DBC/Al_2O_3	Substrate
Nanoscale silver	Die attach
PbSn5Ag1.5	Solder ball
PbSn12Ag2	Solder paste to bond solder ball
Nusil R2188P	Encapsulate SiC die
Hysol QMI 3555R	Bond DBC to ceramic
Master Bond EP3HT	Fasten thermocouple and terminal

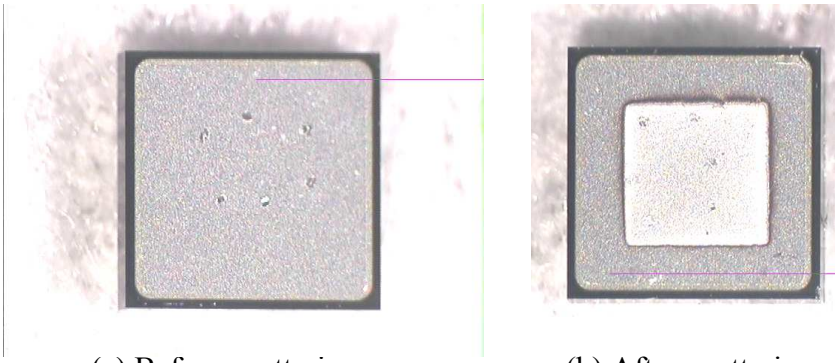
3.3 Assembly Process

Prior to assembly, the top and bottom DBC substrates were fabricated as described in Chapter 2, and the wire-bondable die was also made solderable by the sputtering process as described in Chapter 1. The processed substrates and diode die are shown in Figures 3.2 and 3.3, respectively.



(a) Bottom substrate (b) Top substrate

Figure 3.2 The top and bottom DBC substrates for bump interconnection packaging



(a) Before sputtering (b) After sputtering

Figure 3.3 High temperature SiC diode before and after sputtering metallization

Just as described in Chapter 1, the nanoscale silver paste was printed on the bottom substrate, the die was placed on the paste, and nanoscale silver paste was sintered on the belt oven. After sintering, the middle ceramic layer was bonded to the bottom substrate with conductive epoxy Hysol QMI 3555R, as shown in Figure 3.4. The ventilated baking oven VULCAN^{TM} 3-550 shown in Figure 3.5 was used to cure the epoxy Hysol QMI 3555R, Master Bond EP3HT, and Nusil R2188P.

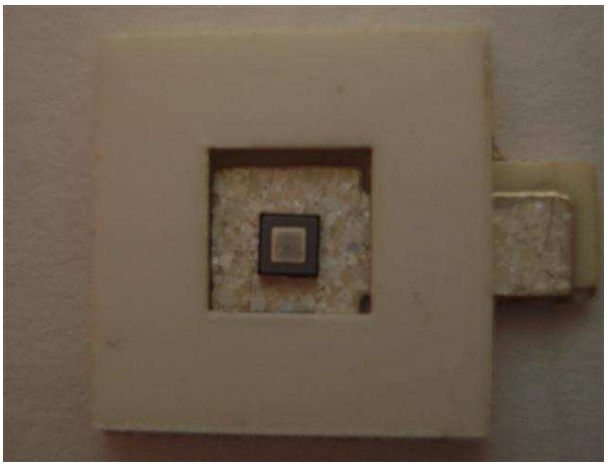


Figure 3.4 Die attachment and bonding of middle ceramic plate

Figure 3.5 Baking oven for curing epoxy

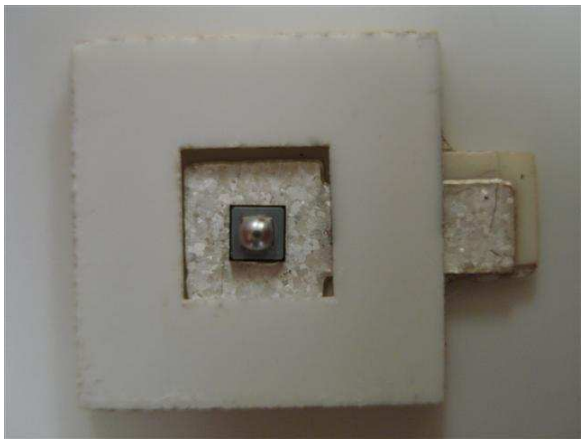


Figure 3.6 Solder ball attachment

Following the attachment of the solder ball (shown in Figure 3.6), the top substrate was placed on the middle ceramic and bonded with Hysol QMI 3555R. Then, the Kovar pin with PbSn12Ag2 solder paste applied on its tip was inserted into the hole in the top substrate and was connected with the top of the solder ball. Finally, the non-conductive Master Bond EP3HT was applied to bonding Kovar pin to the top substrate, to prevent the the solder join from cracking. The complete assembly process flow and packaging is illustrated in Figures 3.7 and 3.8.

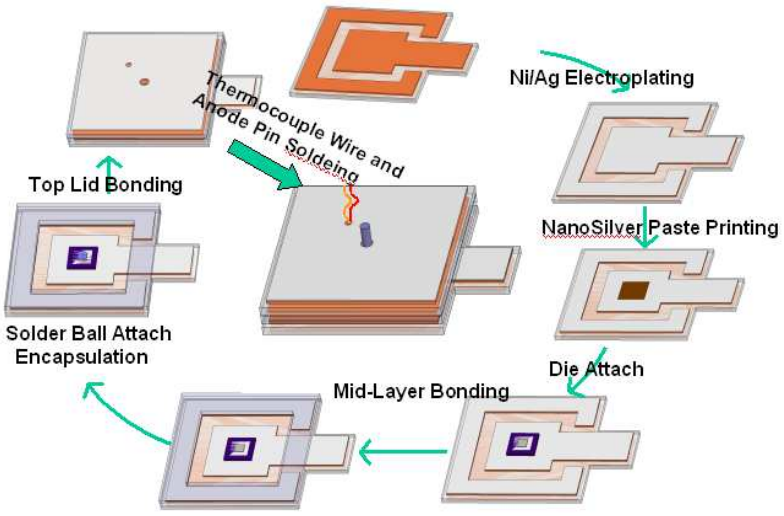


Figure 3.7 Assembly process flow

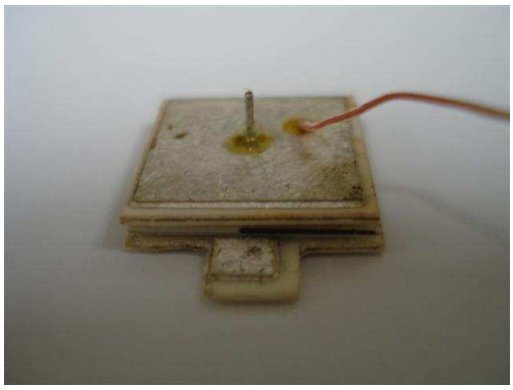


Figure 3.8 Packaging of high temperature power diode with solder bump

3.4 Electrical Characterization

To test the electrical performance of the module under 250°C, a curve tracer was used to characterize the V-I relationships. The entire test setup shown in Figure 3.10 included a temperature controller, heating plate, curve tracer, test fixture, and thermometer. The forward and reverse V-I curves were measured using a curve-tracer when the module is heated up to 250°C. The measurement results for the bare die and the packaged die are shown in Figures 3.10, 3.11, 3.12, and 3.13.

Figure 3.9 Electrical test setup

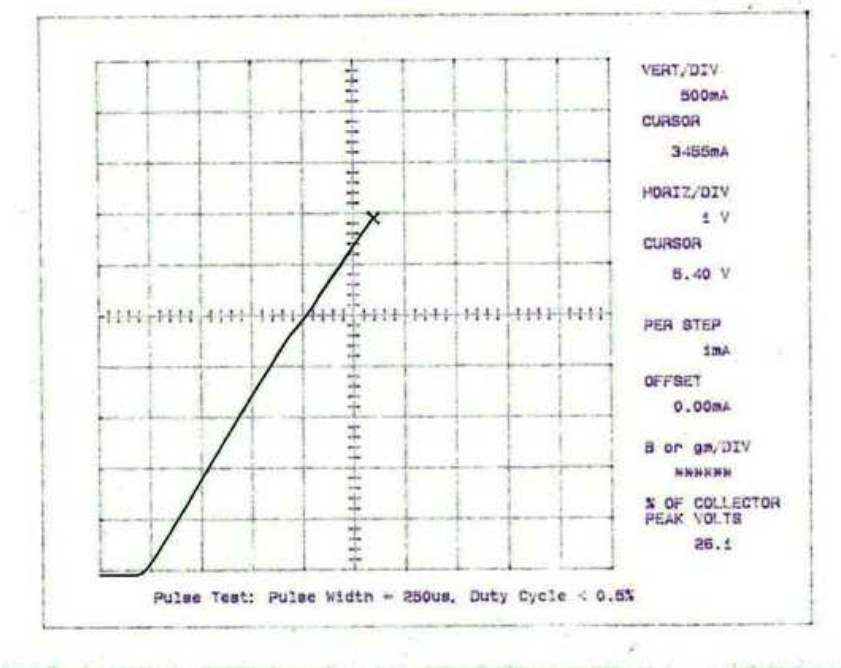


Figure 3.10 Forward I-V curve measurement of bare die (sputtered) (250°C)

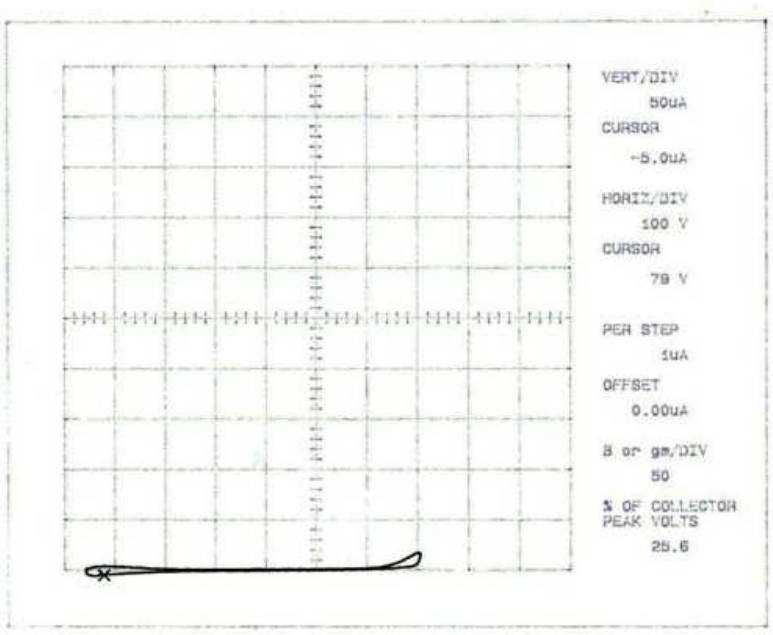


Figure 3.11 Reverse I-V measurement of bare die (sputtered) (250^{o}C)

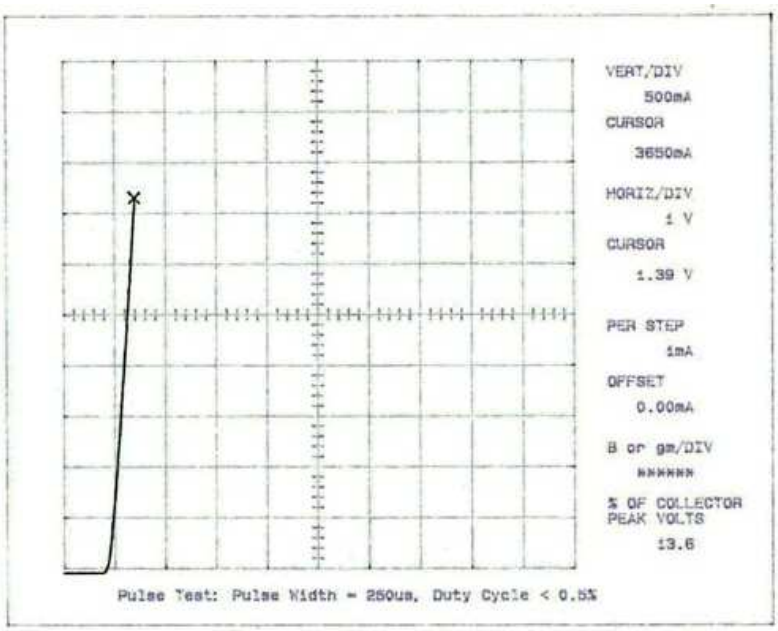


Figure 3.12 Forward I-V measurement of packaged die (250^{o}C)

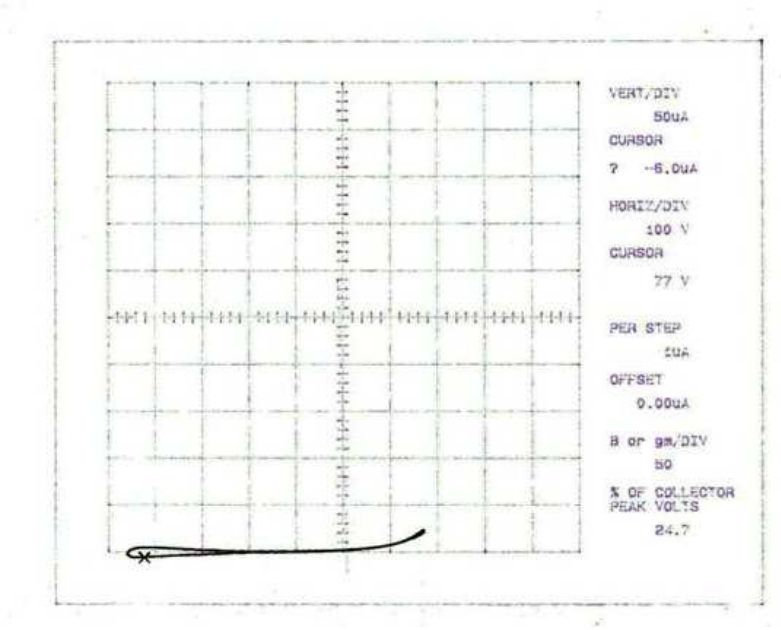


Figure 3.13 Reverse I-V measurement of packaged die (250^{o}C)

From Figure 3.10, the on resistance of the sputtered bare die was calculated to be 1.33Ω. With the deduction of the probes' resistance of 1.21Ω, the on resistance was 0.12Ω. The reverse breakdown of the sputtered bare die was 790V at 5μA. As for the packaged die, the forward resistance was 0.16Ω including clips' resistance; the reverse breakdown is about 770V at 6μA.

3.5 The Inspection of Die Attachment Bondline

Following the electrical characterization of the direct-bond planar power module, the cross-section of the bondline was carried out to inspect the integration and bonding of the structure. The optical micrograph of the bondline cross-section is shown in Figures 3.14 and 3.15.

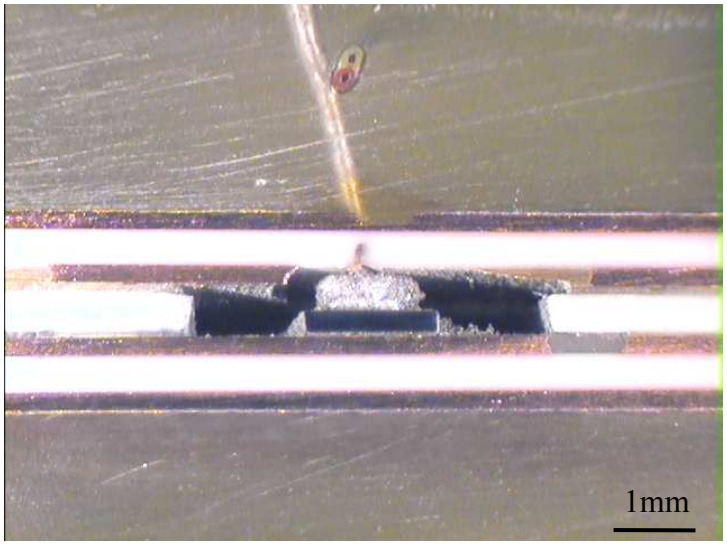


Figure 3.14 The micrograph of the cross-section of the planar power module (bump)

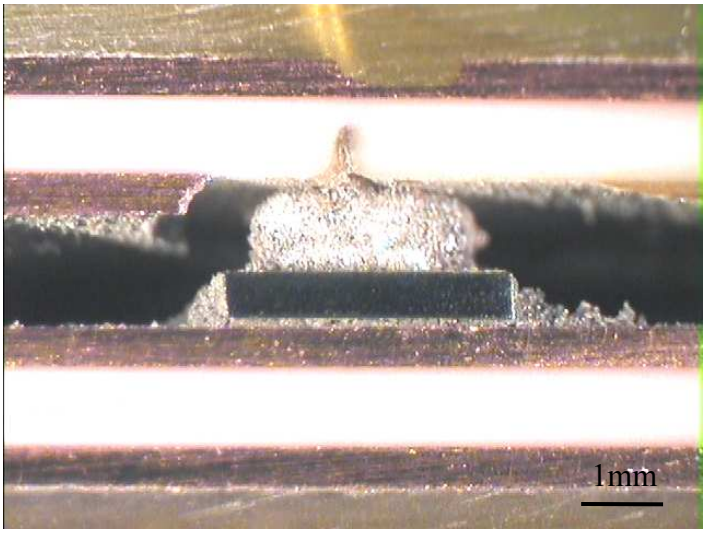


Figure 3.15 The micrograph of bondline cross-section of planar power module (bump)

From the above two pictures, it was that the die was bonded between two layers of DBC with sintered nanoscale silver on the bottom and high-lead solder on top. The the external Kolvar pin was bonded with a solder ball. A ball height of 0.3mm can improve the breakdown voltage by enhancing the gap between the top substrate and the die.

3.6 Conclusions and Recommendations

The planar packaging of a high-temperature power diode was successfully built using a high-lead bump as the top interconnection between substrate and die. The electrical measurement results show that the on-resistance and reverse breakdown voltage of the packaging is very close to those of bare die, respectively. The bump planar packaging is a feasible method to package high power electronic devices.

However, since high lead solder is not compliant with ROHS or WEEE regulation, a type of lead-free solder bump needs to be explored as a substitute.

References for Chapter 3

[1] B.Ozpineci, L.M. Tolbert, S.K.Islam, F.Z. Peng, "Testing, charactrization, modeling of SiC diodes for transportation applications," IEEE Power Electronics Specialists Condference, June 23-27, 2002, Cairns, Australia, pp.1673-1678.

[2] Sergent, J. E. and Krum,A., Thermal Management Handbook for Electronic Assemblies, McGraw-Hill, New York, 1998.

Chapter 4
Summary, Original Contribution, and Future Work

Two types of planar packaging for high temperature power electronic devices were explored: one used sintered nanoscale silver; the other used a high-lead solder bump and sintered nanoscale silver. The forward electrical performance of planar packaging was proven to be excellent due to the high electrical conductivity of sintered silver, but a reverse breakdown voltage drop was encountered in the planar packaging directly bonded with sintered nanoscale silver because of the narrow gap between the top substrate and die. No reverse breakdown voltage drop was observed in the bump interconnection as the bump height make the gap large enough avoiding a reduction in the breakdown voltage. Filling the narrow gap with a dielectric that has high breakdown strength dielectrics is proven to be an effective method.

For the future work, an underfill material with high dielectric strength and a good CTE match can be selected and evaluated. Alternatively, a the thicker layer of nanoscale silver paste may be printed to enhance the gap height, but there is a limit for the thickness of the printed paste due to pressure-assisted sintering. A copper shim may also be used to stake up the gap, but more bonding interfaces would be introduced to the packaging, increasing electrical and thermal impedance. Moreover, the surrounding area of bonding pad on top substrate may be etched down to increase the gap between top substrate and the guard-ring of diode die. With respect to the bump interconnect, the packaging bonded with solder bump possesses desirable forward and reverse current-voltage performances. However, the disadvantage is the difficulty in finding a lead-free solder ball for high-temperature applications. High-lead solder ball is not compliant with industrial ROHS or WEEE policies. Moreover, there is a limit to high lead solder alloy's melting temperature; it is lower than 350^{o}C.

Although the process and electrical characterization of planar packaging have been studied, a reliability test is a necessary aspect for future study. The planar structure with the elimination of bondwire and the introduction of more bonding interfaces is potentially vulnerable to the reliability due to the thermomechanical stress caused by CTE mismatch even though the planar structure may enhance thermal transfer. Therefore, a reliability test and corresponding electrical test should be evaluated in future study.

In order to optimize the packaging, the tradeoff considerations among materials selection, mechanical robustness, thermal dissipation, reliability, electrical performance, cost, cycle-time, processability, and manufacturability should be introduced into the further evaluation.