Appendix E: PLL Programming Information

The Harris PLL chip provides the following possible divider values.

Dual Modulus Prescaler P:	32/33 or 64/65 (RF)	8/9 or 16/17 (IF)
7-Bit Swallow Divider A:	0 ~ 127 (RF)	0 ~ 15 (IF)
11-Bit Program Divider B:	3 ~ 2047	

RF Synthesizer

To operate the RF synthesizer for the transmitting band (1922.5-1977.5MHz), the change of the divider values is on the swallow divider. All the other dividers are kept no change. Table E-1 lists all the divider values to the channels.

Table E-1. Divider values to the RF synthesizer. Note that the least significant bit is on left rather than on right as usual.

Dividers	**R**	**N** **A**	**B**	**P**
Decimal	4	*	24	32

	LSB Control		R Divider														Prog Mode				**MSB**
	C1	C2	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
RF R dvdr	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

	Control		N Divider																	Prog Mode				
			A Divider							B Divider														
	C1	C2	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	* **A**	(MHz)
RF N dvdr	1	1	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1922.5
	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	3	1927.5
	1	1	1	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	5	1932.5
	1	1	1	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	7	1937.5
	1	1	1	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	9	1942.5
	1	1	1	1	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	11	1947.5
	1	1	1	0	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	13	1952.5
	1	1	1	1	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	15	1957.5
	1	1	1	0	0	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	17	1962.5
	1	1	1	1	0	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	19	1967.5
	1	1	1	0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	21	1972.5
	1	1	1	1	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	23	1977.5

RF R-Divider

The first two bits identify which dividers to be programmed. Here they are ‘01’ for the RF R-divider. Then the bits 1 to 15 form the divider value that always is 4 to the radio. The final five bits are the program modes and they are:

		Description	‘0’	‘1’	Set
Bit	16	RF Phase Detector Polarity	-ve	+ve	1
	17	RF I_{CPO} – Charge Pump Current	low	high	0
	18	RF Detector O/P State	normal	high Z	0
	19	RF Lock Detect	no	yes	1
	20	RF F_O Out	no	yes	0

RF N-Divider

Again, the first two bits identify the selected divider and they are ‘11’. The bits 1 to 7 are the A-swallow divider value. Its value is changed based on the wanted frequency and the used values are listed in Table E-1. Then the bits 8 to 18 form the B-divider value and it always is 24. The last two bits select the prescaler P-counter value (32 or 64) and power mode (up or down). Set the bit 19 to ‘0’ for P-counter=32 and the bit 20 to ‘0’ for power up.

260MHz IF Synthesizer

This is a fix frequency synthesis. All of divider values are fixed for the wanted frequency of 260MHz. The IF synthesizer needs to program once as long as it is powered on. Table E-2 lists the divider values.

Table E-2. Divider values to the IF synthesizer. The least significant bit is on left.

Dividers	**R**	**N**		
		A	**B**	**P**
decimal	4	0	13	8

LSB	Control		R Divider														Prog Mode				**MSB**
	C1	C2	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
IF R dvdr	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

	Control		N Divider																	Prog Mode	
			A Divider							B Divider											
	C1	C2	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
IF N dvdr	1	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0

IF R-Counter

The first two bits identify which dividers to be programmed. Here they are ‘00’ for the IF R-counter. Then the bits 1 to 15 form the divider value that always is 4 to the radio. The final five bits are the program modes and they are:

		Description	‘0’	‘1’	Set
Bit	16	IF Phase Detector Polarity	-ve	+ve	1
	17	IF I_{CPO} – Charge Pump Current	low	high	0
	18	IF Detector O/P State	normal	high Z	0
	19	IF Lock Detect	no	yes	1
	20	IF F_O Out	no	yes	0

IF N-Counter

Similarly, the first two bits identify the divider to be selected. In this case, they are ‘10’. The bits 1 to 7 are the A-swallow divider value. It always is 0 for 260MHz. Then the bits 8 to 18 form the B-counter value and it always is 13. The last two bits select the prescaler P-divider value (8 or 16) and power mode (up or down). Set the bit 19 to ‘0’ for P-counter=8 and the bit 20 to ‘0’ for power up.

Remark:

- The divider values are stored individually. Changing the value of one divider does not affect the values of the other dividers.
- In practice, program the R-counter and then the N-counter in a program cycle.
- The divider values will stay as long as Vcc is supplied. However, refreshing them in every program cycle is valid.
- Send the data to the synthesizer with the MSB at first and a timing diagram is shown Figure E-1.

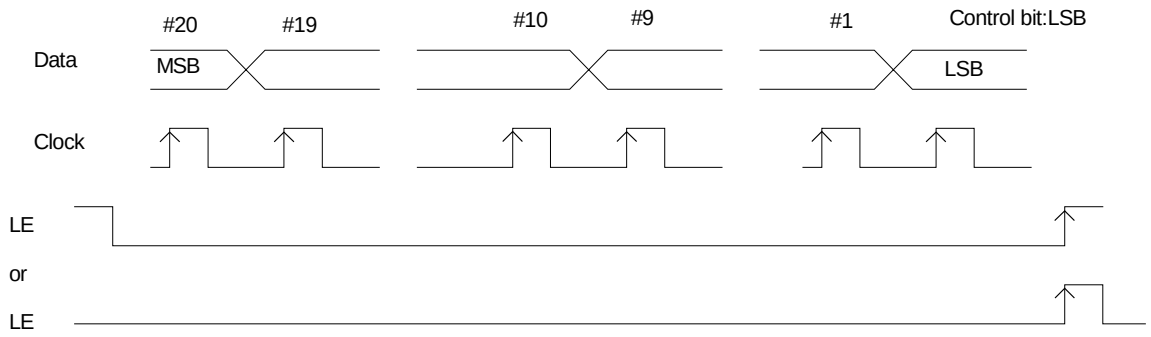

Figure E-1. Timing diagram of loading divider values