Thermo-Mechanical Reliability of Sintered-Silver Joint versus Lead-Free Solder for Attaching Large-Area Devices

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Abstract

This study mainly evaluated the thermo-mechanical reliability of lead-free packaging techniques for attaching large-area chip. With 3 MPa pressure, a low-temperature (<300^{o}C) sintering technique enabled by a nano-scale silver paste was developed for attaching 100 mm^{2} silicon die. This new lead-free packaging technique for die-attachment was compared with soldering by vacuum reflow. Lead-free solder SAC305 and SN100C were selected and used in this work since they were widely used in electronic packaging industry.

Inspection of as-prepared die-attachments by X-ray and optical microscopy (observation of cross-section) showed that the voids percentage in solder joint was less than 5% and no voids was observed at the scale of hundreds of micron in sintered silver joint. Then these die-attachment were thermal cycled with the temperature range from -40^{o}C to 125^{o}C. Deduction of curvature and residual stresses were found for both soldered and sintered die-attachment. After 800 cycles, the residual stresses in silicon-solder-copper sample already decreased to around 0.

The SEM images of solder and silver joint after 800 thermal cycles showed that

cracks longer than 2.5 mm already grew in both kinds of solder joint (die-attachment of Si-Solder-Copper). In contrast, no cracks or voids at the scale of hundreds of micron were defected in silver joint. Based on these observation, different mode of stress-relaxation were proposed for sintered silver and solder, respectively. While solder joint released stresses by crack growth, the silver joint relied on the deformation of porous structure, and plastic deformation may occur.

The pressure-sintering process with double printing and drying was proved to be a reliable process to produce sintered - silver bonding with high strength. The reliability of silver joint was better than that of SAC305 or SN100C. Besides, the technique of measuring the curvature by laser scanning, introduced in this work, showed its significance by directly reflecting the bonding integrity of die-attachment. As a nondestructive testing technique, It was a cheaper and faster way to examine the die-attachment. Additionally, it overcame the disadvantage of X-ray Inspection: it was of the ability to differentiate between layers of die-attachment.

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Chapter 1. INTRODUCTION

Electronic packaging provides electrical connection or insulation, thermal dissipation, mechanical robustness, protection from the environment, long-term reliability, compatibility with board assembly, and compliance with international standards for assembled power electronic devices [1].

Hierarchically, electronic packaging begins from the interface of a semiconductor chip itself--which is considered as the first-level or chip-level packaging--to higher levels of packaging such as board-level and system-level packaging. Chip-level packaging deals with the attachment of one or more bare chips to a substrate, the interconnection from these chips to package leads, and encapsulation [2]. In power electronic systems, the first-level chip interconnection plays a vital role because it directly interfaces with the power chips that contain millions of transistor circuits (In 2010, the transistor count for the latest GPUs (GF 100), one kind of microprocessor, is 3 billion from NVIDIA [3]) not only electrically but also thermally and mechanically. It has to fulfill different requirements compared with those for microelectronic integrated circuit (IC) chips [4]. Firstly, since power devices typically operate at high switching frequencies, parasitic noises must be reduced in order to maintain a high level of circuit performance and efficiency. Secondly, compared with IC interconnections, larger cross-sectional areas and current-handling capabilities are needed in power interconnections because the flowing current increases by several orders of magnitude. Furthermore, the increased power density drives the first-level packaging to improve its roles in heat dissipation and thermal management. At last, the reliability of the first-level power interconnections is essential to ensure the electronic systems to have an extended lifetime.

Electronic packaging is an interdisciplinary subject. Designing electronics packages involve consideration from different aspects of processing and reliability issues. Generally,

overall performance depends on electrical, thermal and mechanical characteristics of packaging.

Admittedly, device fabrication techniques are developing at the rapid rate estimated by Moore's law. Over last twenty years, industrial and academic research efforts on electronic power conversion are making the move toward high-frequency synthesis, which results in miniaturization in physical size and reduction of mass weight and loss. It is pushing the limits of existing power packaging and thermal management technology.

1.1. Significance of Power Electronic Packaging

Future electronic industry place extreme demands on power electronic. Necessarily, packaging of power electronic component provides high performance, high reliability power electronic devices. Major benefits from technology of power electronics assembly and packaging would be provided to industrial areas such as automobiles, naval ship, aircraft, electric power, deep-well drilling.

Understandably, all these require advanced packaging technique is to place electronics in extremely hazardous environments without elaborate enclosures or heavy thermal management systems. In today's power electronics industry, many manufacturers look to raise the chip junction temperature from 125 to 175°C and even beyond [5]. This movement is brought about by the progress in the technologies of power semiconductor device. It is also related to the drive to design and manufacture power systems with higher power density and, thus, reduced bulk and weight.

However, the conventional technology for interconnecting power devices typically involves die-attaching one terminal of the semiconductor die to a heat-sinking substrate with solder alloys or conductive epoxies, and wire-bonding fine aluminum or gold wires to the other terminal(s). Such an interconnect technology is limited to junction temperature of approximate 150°C and thus is not able to meet the high-temperature operating requirement of the wide band gap devices [6]. It is device interconnecting and packaging technology the dominant technical barrier that currently limits the rapid growth of power

electronics. New interconnecting materials and technologies are needed before high-temperature devices and circuits can be scaled-up and reliably incorporated into power electronic systems.

To guarantee the entire system operate reliably and efficiently at higher temperature, higher current density and smaller size than conventional approaches, the packaging technology for application at high operation temperature are developed.

1.2. Current Technologies for Device Attachment

As mentioned earlier, chip-level assembly is one of the determining factors of overall performance, cost, quality, and reliability of electronic components, multi-chip electronic modules, integrated electronic systems, and end-user electronic products. Die attachment is one common method for power device packaging at chip-level.

Die attachment is known as the process of mounting a semiconductor die/chip to a substrate or package. It is a practical and established process over the past 40 years. Initially, applications usually involved eutectic bonding or soldering on substrates. Due to the development of electronic industry, a higher requirement result in the improvement of soldering technique and utilization of other methods and materials. Current die attach techniques, particularly those based on adhesives, offer a rapid, low cost, technically sound method of attaching standard electronic devices. A reliable or processible die attach material depends on the application, but may include following aspects:

- Good mechanical strength;
- Process temperature that will not affect the die function;
- Absorption of stress from thermal expansion mismatch (CTE) between the die and substrate;
- Joint fatigue resistance - mechanical and thermal;
- Electrical/thermal conduction or isolation [7].

Around the world, interest in lead-free solder alternatives is increasing dramatically, primarily because of initiatives in both Asia and Europe to rapidly eliminate the presence of leaded solders in electronic assemblies. Japanese electronics manufacturers have voluntarily mandated that products manufactured or sold domestically be lead-free by 2001. Europe is also requiring lead-free electronics, as mandated by the 1998 Waste Electrical and Electronic Equipment directive (WEEE) [8]. There are a number of reasons behind the effort to eliminate lead from electronic solder materials. In addition to environmental pressures resulting from the element's toxicity, motivations include hazardous waste disposal concerns, workplace safety considerations, device reliability issues, market competitiveness and environmental corporate image maintenance.

The pressures experienced currently by electronics manufacturers in North America are economic, rather than regulatory, in nature. To eliminate the risk that products will no longer be acceptable for export to Asian and European electronics markets, manufacturers are seeking viable leaded solder substitutes, including lead-free solder materials and conductive adhesives. Three predominant lead-free methods in attaching devices to substrates are introduced in the following content. There are soldering, conductive epoxy and low-temperature joining technique.

1.2.1. Soldering

Solders are alloys of two or more metals. When these metals are alloyed together, the melting point of the alloy can be considerably lower than the melting point of either of the individual starting metals. This is the phenomenon which makes the soldering process possible. In the soldering process, the solder is placed between two metal surfaces to be soldered. Heat is applied to warm the solder alloy and eventually melt the solder layer. During melting, the molten solder dissolves a portion of these two surfaces and, when the solder cools, a junction or solder unit is formed, joining the two metal surfaces [9].

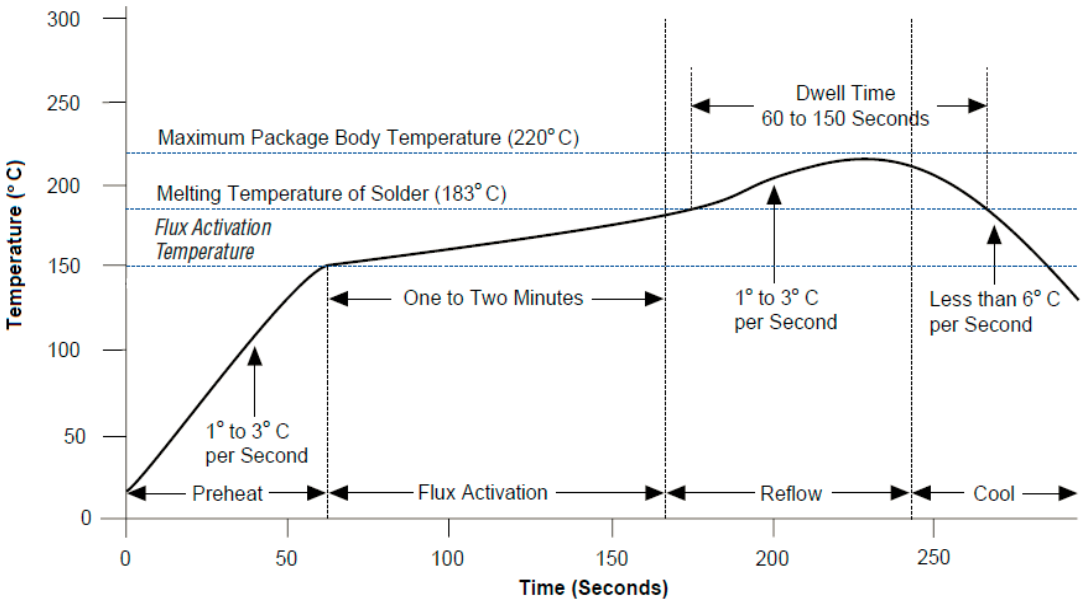


Figure 1.1. Heating profile for Sn37Pb eutectic solder [10].

For all soldering processes, temperature control is important, particularly for the reflow soldering process. Figure 1.1 shows the suggested temperature profile of using eutectic tin-lead (63Sn-37Pb) solder. In the preheat stage, the solder paste dries while its more volatile ingredients evaporate. After preheating, the leads should be kept at about 150°C for one to two minutes so the flux in the paste can clean the bonding surfaces properly. During the flux activation stage, the solder on all areas of the board should be roughly the same temperature. The devices enter the reflow stage when the temperature increases at a rate of 1° to 3°C per second. To prevent warping, bridging, and cold solder joints, keep the package body above the solder's melting point (183°C) for at least 60 seconds. The device body temperature which may vary from the temperature of the leads by as much as 15° C should not exceed 220° C. The package should be within 5°C of the actual peak temperature for 10 to 30 seconds. Small devices with a volume of less than 350 mm^3 will heat up more than larger packages. These devices have a maximum temperature rating of 240°C. The reflow stage is complete when the molten solder connections cool and solidify to form strong solder joint fillets. A fast cooling rate reduces the grain size of the intermetallic compounds and strengthens the solder joints. However,

controlled cooling is important to reduce stress on the component body and minimize warping; this can sometimes best be achieved by a slow cooling rate depending on oven capabilities (air velocity, placement of heating elements, belt width, etc.). After the soldering process, a simple wash with de-ionized water sufficiently removes most residues from the board. Most board-assembly manufacturers use either water-soluble fluxes with a tap water wash, or "no-clean" fluxes that do not require cleaning after reflow.

Lead-free solder as alternatives that satisfy wave soldering, SMT and hand assembly requirements are available on the market today. They can be purchased today in all forms - from bar to paste to preforms. Work continues in the development of new flux chemistries that will enable lead-free solders to deliver the same performance as leaded solder materials. Yet, more research is required in the areas of component lead-free alloys, board finish compatibility, flux system development and processing issues.

With the shift to lead free soldering, heat sensitive components will become more of an issue. Components will distort or become permanently damaged if the soldering process exceeds its maximum reflow temperature. Plastics, for example, are susceptible to either degrade or melt at high temperatures. Both these can degrade or destroy the function of the component. As lead-free solders require a higher reflow temperature than tin/lead, a wide variety of components may be unsuitable for use unless component manufacturers have modified these parts to increase their maximum reflow temperature [11]. Though many manufacturers have used lead-free alloys in niche applications to provide a higher melting point or to satisfy particular material requirements, not all substitute alloys can easily replace present soldering processes. The National Center for Manufacturing Sciences (NCMS) concluded in 1997 that there are no "drop-in" replacements for eutectic tin-lead solder. Research done in 1994 as part of Europe's IDEALS program found that, of more than 200 alloys studied, less than 10 lead-free solder options were viable. The goal of today's lead-free solder research is to determine which alloys should be used to replace the estimated 50,000 metric tons of tin-lead solder currently used each year. Eliminating

lead, which is abundant and inexpensive (approximately $0.40 per pound), and replacing it with another element(s) may well increase the cost of raw materials [12].

The materials chosen to replace lead must meet a variety of requirements:

- They must be available worldwide in quantities sufficient to supply global needs. Certain metals - such as indium and bismuth - are not available in large quantities and would be sufficient only as incremental additions to the lead-free solder alloy.
- The replacement alloy must also be considered non-toxic. Some replacement metals under consideration, such as cadmium or tellurium, are toxic; other metals, such as antimony, may fall into the toxic category as a result of changing regulations.
- The substitute alloys must be able to take all forms used by the electronics industry, including wire for repair and rework, powder for solder paste, bar for wave soldering, and as preforms. Not all proposed alloys can be manufactured in all forms; for example, a high bismuth content would make the alloy too brittle to be drawn into wire.
- Substitute alloys should also be recyclable - combining three or four metals into a lead-free substitute solder formulation may complicate and add expense to the recycling process.

Elements that are available in quantities sufficient to satisfy the high volume of demand for solder include tin (Sn), copper (Cu), silver (Ag) and antimony (Sb). Some commercially viable examples of lead-free alloys include 99.3 Sn/0.7Cu, 96.5Sn/3.5Ag, 95.5Sn/3.8Ag/0.7Cu, and 96.2Sn/2.5Ag/0.8Cu/0.5Sb. All of the elements incorporated into these substitute alloys have different melting points, mechanical properties, wetting characteristics and cosmetic appearances when compared to tin-lead solders. The current industry trend is to use the near-eutectic tin-silver-copper alloy [13].

Most of these lead-free alloys, including tin-silver-copper, have melting points in excess of 200°C - substantially higher than traditional tin-lead solders, which melt at approximately 180°C. These elevated melting points will require higher soldering

temperatures. For package and flip chip assemblies, the higher melting points of lead-free solders may prove to be a concern, because package substrates may not be able to withstand elevated reflow temperatures.

Board and component finishes also must be compatible with lead-free solders. For example, solder joints on boards with copper finishes may be affected both mechanically and cosmetically by the higher surface mount technology (SMT) reflow temperatures of lead-free solders, which can cause the formation of harmful intermetallics between tin and copper. The cosmetic appearance of lead-free solders is also different (for example, certain formulations appear bright but slightly less reflective than traditional tin-lead solders), and may require changes in standard quality control procedures. Finally, because no substitutes for high-lead-bearing solders exist at present, a completely lead-free assembly is not yet possible.

While current flux systems work well with tin-lead solders, lead-free substitute alloys will not behave similarly on all board component finishes and do not wet as easily to form the same types of intermetallic bonds. Therefore, modified fluxes may be required that promote better wetting and reduce voiding in BGA soldering.

The ideal lead-free solder alloy combination will offer manufacturers good electrical and mechanical properties, good wetting abilities, no electrolytic corrosion potential or dendritic growth concerns, acceptable cost, and current and future availability in different forms. The solder will use conventional flux systems and will not require the use of nitrogen to enable effective wetting [14].

Besides, the soldered chip joints are susceptible to fatigue failure under cyclic loading because of low yield strength and accumulation of high inelastic strains during deformation. This reliability issue becomes more troubling if the junction temperature is raised to 175°C or even higher as envisioned for some future systems [15]. Consequently, in the quest for 175°C power modules, one of the foremost challenges to overcome is the low melting temperature of solder attachments. The increased operating temperature is

very close to the melting point of the material, thus making the attachment susceptible to a host of thermo-mechanical and metallurgical problems.

1.2.2. Conductive Epoxy

Conductive epoxies are typically dielectric curable polymers that contain metallic conductive particles. Those particles can be tin, copper, graphite, gold, and silver. The most popular filler material is currently silver because of its moderate cost, wide availability and superior conductivity. Conductive epoxy are used as a connectivity compound for forming electrically conductive joints. They traditionally have been used as die-attach materials that bond integrated circuits to lead frames. They are also used to make laminates for printed circuits, to attach copper foil to boards or flexible substrates, and to bond circuits to heat sinks. As a result of lead-free initiatives, conductive adhesives have become an attractive alternative to solder for attaching surface mount components. Typically, they are in the form of a liquid, a viscous liquid. It would be applied by either dispensing or printing [16]. The polymer is an adhesive material that chemically reacts with metals to form a bond. The metallic particles in the adhesive form a network in the cured joint that provides a conduction path from the package to the board.

They are low processing temperature alternatives to solder alloys. They cure at room temperature or processing quickly with minimal exposure to temperatures between 100 and 150°C, these adhesives are excellent for bonding temperature-sensitive components and for providing electrical connections on non-solderable substrates like plastic and glass [17]. Available in highly flexible formulations, conductive adhesives are also a solution for applications such as assembly and repair of flexible circuits or bonding flexible substrates and connectors, as shown in Figure 1.2. Additionally, adhesive assembly and processing requires approximately half as much material as does solder for the same application. Also, the processing costs of adhesives can be substantially lower than those of solder because there are fewer steps involved in adhesive bonding. While processing times are very similar for both solder and adhesive bonding, adhesives do not

require the time and expense of flux application and cleaning, as occurs in a wave soldering application using water washable flux.

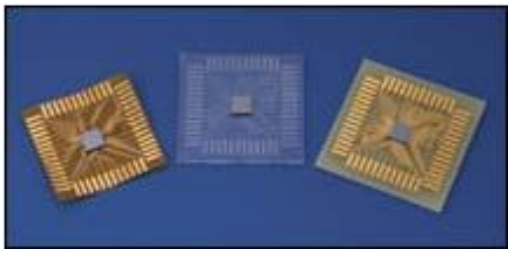


Figure 1.2. Electrically conductive epoxies develop strong, durable bonds on many different substrates (e.g., flex, glass and FR4) [18].

Conductive adhesives provide both a mechanical bond and an electrical interconnection between a device and a circuit board. Electrical and thermal conduction occurs when filler particles carry current through the cured adhesive resin. There are three types of electrically conductive adhesives formulated to provide specific benefits where an electrical interconnect is desired. Similar to solder, isotropic materials conduct electricity equally in all directions and can be used on devices that require a ground path. Conductive silicones help protect devices from environmental hazards, such as moisture, and shield electromagnetic and radio frequency interference (EMI/RFI) emissions. Anisotropic conductive polymers or z-axis adhesive films allow electrical current to flow in only a single direction, and provide electrical connectivity and strain relief for flip-chip devices.

However, conductive epoxies have disadvantages. One of the greatest concerns with the reliability of silver-filled conductive adhesive is silver migration. In this mechanism, the silver is ionized and migrates in a humid environment, forming electrically conductive dendrites that can result in electrical shorts between interconnects [19].

Additionally, pricing for conductive adhesives varies greatly, depending upon the type of filler used and its market price. Different formulations of conductive adhesives can vary by a factor of 10 or more. There is sometimes an inconsistency not only from vendor

to vendor in terms of the conductivity and resistivity of the materials, but even from batch to batch.

Besides, the material costs of conductive adhesives that use precious metals as fillers are relatively more than the material costs of lead-free solders or conventional adhesives. In terms of material costs alone, adhesives are typically several times more expensive than solder.

Finally, though a lot of these epoxies work very well for steady state temperature environments particularly at extreme temperatures, in terms of applications where you have thermal cycling, typically, conductive epoxy shows unreliable performance.

In summary, conductive epoxy is a promising die-attach material, with obvious advantages and disadvantages.

Table 1.1 Advantages and Disadvantages of Conductive Epoxies.

	Advantages	Disadvantages
Conductive Epoxies	➢ Lead free ➢ No flux involved ➢ Lower processing cost ➢ Lower Cure temperature (typically lower than reflow temperatures)	➢ Migration ➢ Higher material cost ➢ Bad performance under thermal cycling ➢ Inconsistency

1.2.3. Low Temperature Joining Technique

In the late 1980s, an alternative technique for the joining of large-area silicon devices with molybdenum plates was discovered. The so called low temperature joining technique (LTJT) was based on the sintering of silver powders and flakes. These silver powders and flakes were covered with an organic additive to protect them from low temperature (room temperature) agglomeration and aggregation. This additive was an ingredient for the production process of the silver powders, and would be oxidized and burned out when the temperature reaches 210^{o}C or above [20]. Therefore for LTJT process, an environment with adequate oxygen was needed to help remove the excessive

organic additive around the silver particles and flakes. Unlike the solder reflow process, the mechanical bonding of the LTJT technique was formed by a sintering process. This sintering process contains no reaction in liquid phase, because the melting point of silver is 960^{o}C, much higher than the processing temperature. Therefore, it was predicted that the interconnection formed by the LTJT technique possesses good stability even at temperatures higher than the processing temperature. Because the sintering bonding strength was based on the atomic diffusion of silver into joined materials, the bonded surface must have compatible metallization with silver. The diffusivity of silver atoms in these metallization layers must be reasonably high so that the as-formed bonding has a certain mechanical strength. In addition, the bonded materials must exhibit oxide-free surfaces. The sintering of powder compacts had been widely applied in microelectronics for making hybrid circuits, cofired multilayer metal/ceramic interconnecting substrates, multilayer ceramic capacitors, magnetic components, and etc. Since the conventional sintering normally requires a temperature that may be substantially higher than the maximum temperature a semiconductor device can tolerate, any means of lowing the sintering temperature is desirable and necessary for the successful implementation.

Often the surfaces are prepared with a diffusion barrier consisting of nickel and a thin noble metal finish or high purity electroless plating of silver, gold or platinum. The standard LTJT process consists of the following steps:

- Application of silver paste (powders and flakes with organic solvent);
- Drying (low temperature organic solvent evaporation);
- Placing the components/devices;
- Sintering of the silver paste, with pressure assistance.

Silver paste can be applied using by screen printing, stencil printing, spray coating, automated dispensing, or through a foil transfer method. The silver flakes are suspended in organic solvent with a viscosity adjustable to the respective application method. After applying the silver paste, the organic solvent has to be evaporated at a relatively low

temperature, about 150^{o}C [21]. By removing the organic solvent, the green density of the silver flakes is significantly increased; thus the densification rate can be increased during the sintering process. Components or devices will be placed on top of the paste after the drying stage. A hardened rubber is employed to cover the components, mainly to prevent direct mechanical contact between the metallic hydraulic press and the semiconductor devices, thereby protecting the devices during the process. For the sintering process, a hydraulic press is used to provide uniaxial and isostatic pressure. Up to 40 MPa pressure is usually applied at 230-250^{o}C to help promote the sintering of the silver flakes, as well as to secure the devices in place [22]. The sintered silver has a porosity of about 15%, and provides excellent thermal, electrical, and mechanical properties compared with solder alloys (Figure 1.3) [23].

Because of the high melting temperature of silver, LTJT is expected to have high reliability even at temperatures above 300^{o}C. The thermal conductivity is more than three times better than that of soft solder attachment. With a thinner bondline thickness, of about 20 to 30 μm, a very low thermal resistance can be achieved. In addition, the electrical conductivity is much better than that of solder too. LTJT is also employed to attach silver ribbons to the top of the diode, which also has the potential to replace wire-bond or ribbon bond to provide greatly improved reliability during power cycling and thermal cycling tests. An example of LTJT is shown in Figure 1.4 [23].

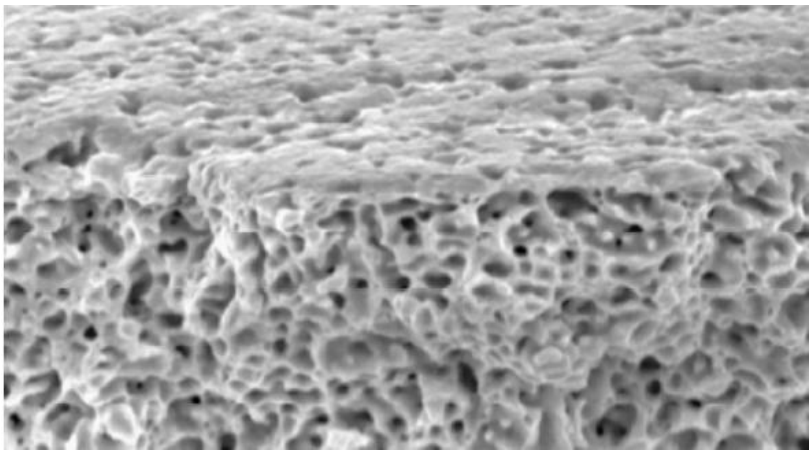


Figure 1.3. SEM image of sintered foil of LTJT.
(The width of the picture corresponds to about 25μm).

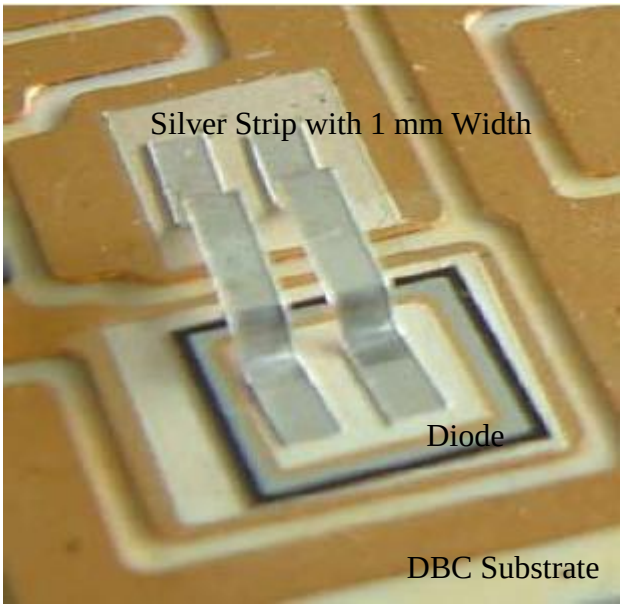


Figure 1.4. Double-sided joining by LTJT.

A significant improvement in the temperature cycling reliability test can be obtained by applying the LTJT technique in a large-area device attachment. The results show at least 10 times longer lifetime for sintered silver than standard solder layers [23]. Power cycling results of modules with an LTJT layer between a silicon chip and DBC substrate also prove the excellent stability of the LTJT layer. The main failure of the tested modules is the wire-bond lift-off. When the top-side wire-bond interconnection is replaced by another LTJT layer, the power cycling capability was found to be over two times higher than that of single-sided LTJT.

With the exceptionally high application temperature, excellent electrical and thermal properties, and proven long life-time in temperature cycling and power cycling tests, LTJT has become more and more popular in the power module industry, and is now finding its way in replacing many of the solder alloys and conductive epoxies in various applications.

However, a serious drawback of the technology is the use of high quasi-static pressure (> 40 MPa or 400 Kg-force per cm^2 chip area) necessary to lower the sintering temperature of existing thick-film silver pastes to less than 300^oC. The need of such large

pressure has hampered quick adaptation of the technology because it limits production throughput and places critical demands on substrate flatness and chip thickness. Similar to the press pack, the application of external pressure tends to complicate the manufacturing process and thus increases the cost.

1.3. Motivation of developing low-temperature sintering of Nano-Silver Paste

To overcome the barrier of utilizing LTJT, methods need to be find to lower or even eliminate the assisted pressure for sintering. Usually, there were two strategies to achieve low-temperature sintering: (1) using quasi-hydrostatic pressure to increase the sintering driving force; and (2) reducing the size of particles to nano-scale. Lu et al. investigated the fabrication process of nano-scale silver paste in which the commercial organic binder, thinner, and solvent were selected to produce high-performance silver paste with 30 nm silver particles.

To minimize or eliminate the use of pressure for the low temperature chip joining technique, nanoscale metal particles was used to lower the sintering temperature. This approach utilizes the large thermodynamic driving force for densification in place of the applied mechanical force. Based on the science of sintering, the driving force for densification of a particle compact increases with decreasing particle size due to increasing surface area to volume ratio and particle surface curvature. Thus the densification rate—a product of thermodynamic driving force and kinetics—of a nanoparticle compact can still be high at low-temperatures despite low atomic diffusion coefficients at low-temperatures [24].

After the nano-scale silver paste was heated to 280^{o}C under standard atmospheric pressure, the density of sintered silver actually reached 80 wt.% of bulk silver. The performance of sintered silver material was examined using different measurements. The thermal conductivity was 220 W/m/K measured by laser flash technology, and 417 W/m/K for bulk silver; the resistance was 4×10^{-6} cm or 1.6×10^{-6} cm for bulk silver; and the elastic modulus was 10 GPa and 75 GPa for bulk silver. This performance of sintered

silver paste significantly exceeded solder alloy materials [25]. Combustion chemical-vapor condensation (CCVC) is used for synthesizing Ag nanoparticles with 20 nm average particle size in which some nanoscale silver paste—and its subsequent low-temperature sintering process to provide high-quality power device joints at a relatively low cost level [26]. Because of the reduction of silver particle size and the proper selection of the organic vehicle for the paste system, external pressure is not necessary anymore to sinter the silver paste at low temperatures. The absence of external pressure during processing not only makes the 3-D high-density integration possible, but also greatly reduces the fabrication complexity and thus the cost. The nanoscale silver pastes can be either screen/stencil-printed or syringe-dispensed and they can be served as a direct drop-in substitution to the commercially available solders. They can be sintered to a density of over 80% after sintered at 280^{o}C, a temperature closes to the maximum processing temperature in today's lead-free soldering process. The electrical and thermal conductivities of the low-temperature sintered silver are around 3-5 times higher than those of the best solder or conductive epoxy. The silver joints formed by the low-temperature sintering technology have a bonding strength about 40 MPa on the silver-coated substrates, similar to the eutectic solder joint strength [27]. Due to the solidus inter-diffusion of bonding mechanism, initial voids are avoided from the silver joints and they are more uniform than solder joints and therefore they have better thermal management. Also, the porous microstructure gives the sintered material a low modulus of around 10 GPa, making it mechanically compliant for relieving thermo-mechanical stresses in the attachment [28]. Finally, once the attachment is formed at low temperatures, the maximum use temperature of the package is limited by the device and substrate, not by the die-attach material. Thus, the low-temperature sintering technology can be used to interconnect wide-bandgap semiconductor devices, such as SiC devices for switching power supplies or GaN light-emitting devices, to enable them to function at temperatures over 300^{o}C [29].

In the following, the detailed advantages of the low-temperature silver sintering technology are listed and discussed.

First, this technology is of reliable integration capability. Because of the elimination of external pressure during the low-temperature sintering of nanoscale silver paste, the interconnect technology can be easily adapted to build 3-D high-density power packages like processing conventional solder paste. Compared with solder reflow, the low-temperature sintering has extra advantages for simpler processing [30]. Unlike solder reflow, the nanoscale silver paste is sintered at temperatures far below the melting point of bulk silver. The sintered silver film or joint can retain their shapes at the sintering temperatures. Therefore, it is very convenient to process the low-temperature sintering as many times as desired to complete a 3-D high-density power package. Otherwise several solders with different melting points have to be carefully chosen in the construction of a solder-reflowed package.

Besides, sintered silver has very high electrical and conductivity. The electrical conductivity of the low-temperature sintered silver is about 3-5 times of those of the best solders and also much higher than that of the conductive epoxies. Therefore it has great current handling capability and excellent electrical performance. The thermal conductivity of the low-temperature sintered silver is also about 3-5 times of those of the best solders and also much higher than that of the conductive epoxies. Furthermore, the uniformity of silver joint eliminates the possible hot spots of the power device. Therefore low-temperature silver sintering has superior thermal management capability [31].

Finally, it has excellent reliability. The low-temperature sintered silver has around 20% porosity with microscale porous trapped in. The porous microstructure gives the sintered material a low effective modulus at about 10 GPa. The value is even lower than that of the soft solder such as eutectic lead-tin at the room temperature. For a power device-metalized substrate interconnection, a softer interconnecting material can be advantageous since it transfers less of thermal stress due to the semiconductor-metal CTE

mismatch. Using this argument, the low-temperature sintered silver has superior thermo-mechanical properties and it will help achieve a more reliable interconnection. Furthermore, since the interconnect material is pure silver, a single phase material with a much higher melting point than solders, its reliability is high because the phase separation and creep failure are avoided or greatly reduced [32].

1.4. Objective and Organization of the Thesis

The reliability of packaging are highly related with the die-attach layer. A significant thermo-mechanical stress may occur during the cycled operation of all attached layers due to the mismatch of the coefficients of thermal expansion (CTE) between devices and substrate. The die-attach layer not only needs to withstand cycled stress, but also to cushion thermo-mechanical stress to ensure proper operation of the devices. Thus, the mechanical properties of die-attach layer essentially affect the reliability of the power devices. Base on this consideration, one objective of this study is to investigate the thermal-mechanical reliability of die-attachment.

Additionally, recent trend of high density of power electronic assemblies has pushed to use smaller packages and larger silicon chips. Thus, the study of die-attachment with larger-area chip is another practical topic in this work. Besides, reliable process has been reported to use the nanoscale silver paste for bonding small chips without any applied pressure. Excellent reliability and mechanical properties were obtained with the sintered joints. To extended this work, large-area silicon will be used.

Another target of this work is to compare the reliability of sintered nano-scale silver paste with the lead-free solder, considering their leading role in electronic packaging industry.

The final goal is related to the testing methods. Curvature measurement of die-attachment sample would be introduced and utilized for testing the bending integrity as a nondestructive way of testing bond-line quality.

Based on the aforementioned objectives, this study is divided into the following tasks and arranged in the following sequence:

Chapter 1 has provided the application and challenge of power electronic packaging. The current die-attachment technology is summarized.

Chapter 2 details the design of experiment, fabrication procedures, and testing of as-prepared die-attachment. Materials selection and surface metallization technique are addressed and both techniques of solder vacuum reflow and pressure-sintering are introduced. Temperature cycling profile is selected in the end from JEDEC standard for accelerated testing.

Chapter 3 concentrates on results and discussion. Background of residual stresses is first presented. Then, measurement of curvature and calculation of residual stresses from curvature are described. Observation of the change in bending extent and corresponding residual stresses are shown with the increasing of the number of temperature cycles. SEM images of bond-lines are shown for investigating the mode of stress deduction in bond-line. Different way of stress deduction are proposed for solder joint and sintered silver joint, respectively. Comparison of reliability between two kinds of joint are stated in the end.

Chapter 4 summarizes this study and original work and provides recommendation for future work.

Chapter 2. FABRICATION OF DIE-ATTACHMENT BY SOLDERING AND PRESSURE-SINTERING

2.1. Sample Configuration

The die-attachment structure is shown in Figure 2.1. It simply consists of three layers: the silicon chip, the die-attach materials and the substrate.

Figure 2.1. Structure of die-attachment.

2.1.1. Silicon Die

Silicon dummy die, or mechanical die, was used in this work. Single side polished (SSP) silicon wafer was ordered at the beginning with the thickness of 500 μm. One reason of using polished silicon is to utilize its ability of reflecting the laser beam. This would be further discussed in the Chapter 3.2. To investigate large area die-attachment, chip size with 10 × 10 mm^2 was also used.

2.1.2. Selection of Substrate

Selection of substrate materials is another target in this step. DBC and copper were finally selected as substrates. DBC means Direct Bond Copper and denotes a process in which copper and a ceramic material are directly bonded. Normally, DBC has two layers of copper that are directly bonded onto an aluminum-oxide (Al_2O_3) or aluminum-nitride (AlN) ceramic base. The DBC process yields a super-thin base and eliminates the need for the thick, heavy copper bases that were used prior to this process. Because power modules with DBC bases have fewer layers, they have much lower thermal resistance values and

because the expansion coefficient matches silicon, they have much better power cycling capabilities (up to 50,000 cycles) [33].

DBC probably is the most widely used substrate material in power electronics due to its high current-carrying capacity (about 100 amperes), high thermal and electrical conductivity, and controlled coefficient of thermal expansion (CTE) (6 – 8 ppm/^{o}K for alumina-based DBC and 4 - 5 ppm/^{o}K for aluminum nitride-based DBC), which matches well with that of semiconductor devices (2.3 - 4.7 ppm/^{o}K for Si, and 4.5 – 4.9 ppm/^{o}K for SiC) [34]. In addition, DBC is replacing complicated assemblies based on lead-frames and refractory metalized substrates due to ease of assembly.

In summary, the properties of DBC ceramic substrates are shown below:

- Good mechanical strength; mechanically stable shape;
- Excellent electrical insulation; Very good thermal conductivity;
- The thermal expansion coefficient close to that of silicon;
- Good heat spreading.

In this study, a better thermo-mechanical reliability of using DBC as substrate than copper is demonstrated. As the title of the thesis reveals: thermo-mechanical is the core topic in this work. Generally speaking, the thermo-mechanical stresses mainly come from the CTE mismatch between the chip and substrate. Due to such a small CTE mismatch, the initial residual stresses after die-attachment process should be considerably small. The reliability of die-attachment, usually decided by the joint failure rate, should be much higher than silicon die attached to pure metal or alloy.

In order to observe the joint failure induced by thermo-mechanical stresses within 1000 thermal cycles (Industry experience [35]), other materials with much higher CTE were also selected. Copper and aluminum were two good choices since they greatly satisfy this requirement. Moreover, they were widely used and low cost.

Since the DBC was of the thickness around 0.8 mm, the copper with this thickness were also prepared as comparison.

2.1.3. Die-Attach Materials

Since nano-scale silver paste has been introduced in Chapter 1.3, lead-free solder were mainly introduced in this part. Two kinds of widely used lead-free solder had been selected: SAC305 (Sn-3.0Ag-0.5Cu) and SN100C.

While the situation varies from country to country, nearly one year after the RoHS Directive came into force implementation of lead-free solder is progressing steadily. For lead-free soldering to be considered successful it is not sufficient just to have dealt with the challenges of mass production. It is also necessary to establish that the soldered joints produced are at least as reliable as those made with Sn-37Pb alloy. In this context "reliability" means the length of time in service that the initial functionality of the joint can be maintained. In this work, solder joint reliability was investigated through a comparison of the properties of two alloys that were widely used for lead-free wave soldering, SAC305 and the Sn, Cu, Ni, Ge alloy SN100C.

SAC305 has been widely accepted in the industry. SN100C, on the other hand, has been widely tested and investigated in recent years and it is likely to replace the role of SAC305 in the global electronic industry of lead-free solder.

SN100C behaves is possible to achieve smooth bright fillets free of shrinkage defects (Figure 2.2) [36]. The high melting point and high creep resistance of lead-free solders means that large strain is imposed on solder joints as the result of the repeated expansion and contraction that occurs during thermal cycling. The result can be cracking of chip components. Although the strength of solders that contain silver, the most common of which is Sn-3.0Ag-0.5Cu, is high their low ductility means that they are not able to accommodate strain. By contrast, the high ductility of SN100C can accommodate substantial strain without embrittlement and cracking and that is apparent in the results of the cyclic strain test, thermal cycling test, impact test and vibration test. A further advantage of SN100C is that slower growth of interfacial intermetallic during aging. The consequence of all of these advantages is the high reliability of joints made with SN100C.

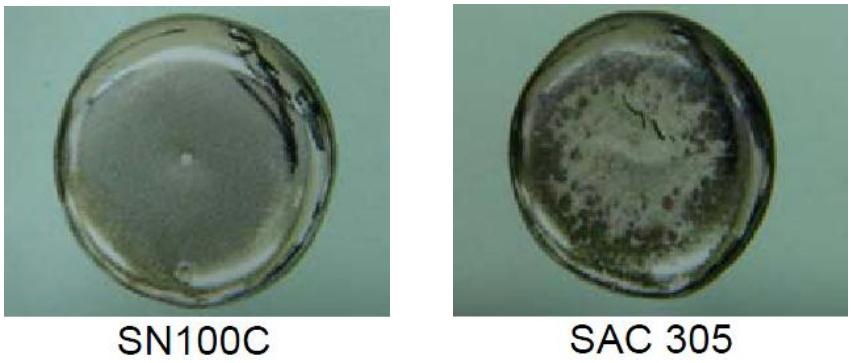


Figure 2.2. The addition of nickel promotes the precipitation of Cu_6Sn_5 which is evenly distributed in the solder, making appearance shiny and attractive.

Part of the advantages of SN100C (the patented addition of nickel to the tin-copper eutectic with 'Ge') are listed below:

- Surface mount pads are very uniform and flat.
- Lower cost than silver containing lead free alloys
- Minimal increase in operating temperature
- Eutectic solder.

According to the datasheet, the suggested peak temperature for soldering was 240^{o}C. However, 270^{o}C was used in the solder reflow of this work. From earlier experience, the voids percentage in solder joint with peak soldering temperature 270^{o}C was much lower than with 240^{o}C.

Table 2.1 shows the composition, peak temperature in the processing and their melting temperature. Peak processing temperature is worthy of attention since apart from CTE mismatch, the other decisive parameter that determines the residual stresses is the temperature difference between the peak processing temperature and room temperature. The melting temperature of nano-scale silver is marked red since this contributes to the excellent performance of sintered silver at higher working temperature.

Table 2.1. Composition and peak processing temperature of die-attach materials.

Materials	Composition	Peak Processing Temperature	Melting Temperature
SAC305	Sn-3.0Ag-0.5Cu	270°C	217°C - 218°C
SN100C	Sn-Cu0.7-Ni-Ge	270°C	227°C
Nano-Ag	30 nm Ag-Particles	275°C	961°C

2.2. Sample Preparation

2.2.1. Preparation of Discrete DBC

The purchased DBC was of the size around 12 cm × 18 cm. Thus, making discrete 10 × 10 mm^2 DBC substrate was the first step in the experiment.

The step of process was described in the Figure 2.3.

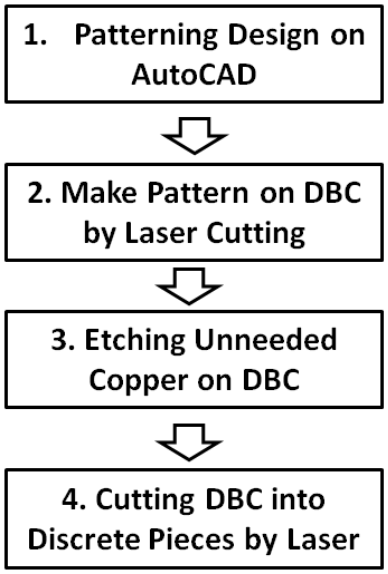


Figure 2.3. Process of making discrete DBC substrate.

Since the metal surface used in DBC was pure copper, it was easily etched by warm ferrite chloride acid solution (Table 2.2). For simplicity, Kapton tape was used to create the patterns on the copper surface instead of standard etching resist. Then laser machine (Figure 2.4) was used to cut the pattern, according the drawing pattern. Usually, the

pattern was first drawn by AutoCAD and saved in the format of .dxf. The etching process was done in a spray etch chamber (Figure 2.5), and when warm ferrite chloride acid solution was used, the copper etch speed was about 0.5-mil every minute, and the etch quality was excellent with sharp edges. After the copper was etched off, Al_2O_3 plate can be sliced by laser to form small pieces for further experiment. Similar step was used for preparing copper substrate.

However, if the ferric chloride acid was used, acid was necessary in the following step for remove the surface oxidation and residue of ferrite chloride. Evidence for surface contamination by ferrite chloride residue would be shown in the section of electroplating. One way to avoid using ferrite chloride was using Nitric acid with low concentration (15%) to etch the copper.

Table 2.2. Parameters for equipment settings.

Machine	Processing	Settings	Value
Laser cutting machine: Resonetics CO_2 Laser	Patterning Kapton	Stage lasing velocity (inch/s)	0.6
		Stage lasing velocity (inch/s)	1
		Focus	428
		Laser power (W)	5
		Pulse number	10
	Cutting Al_2O_3	Stage lasing velocity (inch/s)	0.1
		Stage lasing velocity (inch/s)	1
		Focus	433
		Laser power (W)	38
		Pulse number	300
Etching machine: Kepro BTD-201B	Etching copper	Etching time for 8 mil copper (minute)	15
Vacuum reflow machine: SST MV-2200	Reflowing SAC305, SN100C solder preform	Temperature profile	Shown in Figure 2.17

Figure 2.4. Laser-cutting machine.

Figure 2.5. Spray etching machine.

2.2.2. Surface Metallization

Surface metallization of noble metals such as silver or gold on the surface of chip and substrate would protect the copper trace from further oxidation or corrosion during high-temperature processes or unfavorable service conditions. Since nano-silver paste was used as the interconnection material, the best surface finish candidate in terms of diffusion and reliability was silver metallization. Two methods of surface metallization were used: Physical Vapor Deposition (PVD) and electroplating.

Surface metallization on silicon wafer was done by PVD at the 'Micron Lab' (Virginia Tech). 3 layers of metals (Chromium, Nickel, and Silver) were deposited on the wafer: the thicknesses were Cr 1500 Å; Ni 2000 Å; Ag 2500 Å, respectively (Figure 2.6).

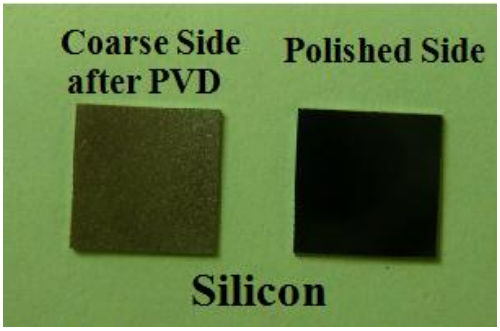


Figure 2.6. Silicon with surface metallization.

Silver electroplating was used for metallization on substrates. Before electroplating, electro-less silver plating should be effectively carried out, that is, coating a thin layer on the DBC or copper with strong adhesion (Figure 2.7). The function of this step was to stop copper diffusion during high temperature soaking or cycling.

The nitric acid with 15% was used as etching solution. After etching, copper grains could be observed on the well etched surface (Figure 2.8). Step 2 and 3 should be finished as soon as possible. When dipping the sample in plating solution, gently stirring the DBC in the solution would help to provide homogenous plated surface.

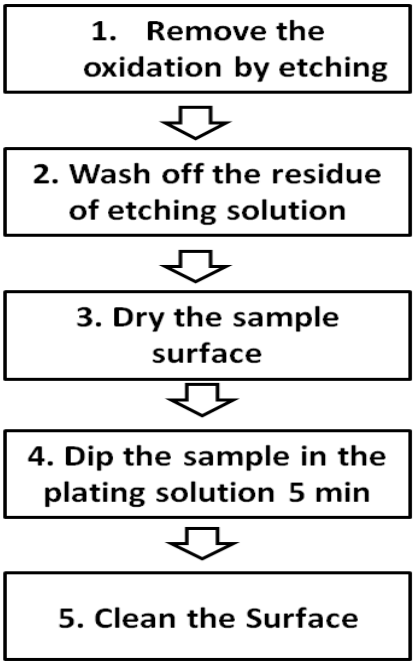


Figure 2.7. Process of electro-less silver plating.

During the plating process, the ambient temperature was kept between 75^{o}C to 85^{o}C. Because the reaction happened when Cu was exposed to Ag bath, it would stop when the Cu surface was fully covered with fresh Ag. The plating thickness was only several hundred nanometers, 300 ~ 400 nm. The plating duration is usually 5 - 10 minutes. DBC after Ag plating was shown in Figure 2.8.

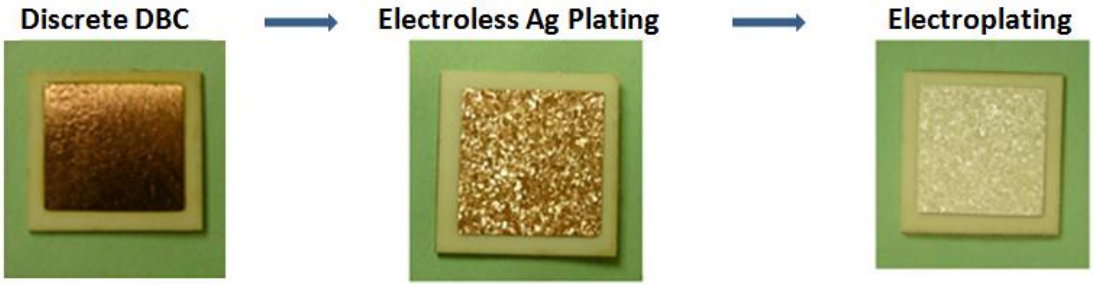


Figure 2.8. Process of silver plating.

As mentioned in Chapter 2.2, residue of ferric chloride ($FeCl_3$) would contaminate substrate surface. A clear evidence was shown in Figure 2.9.

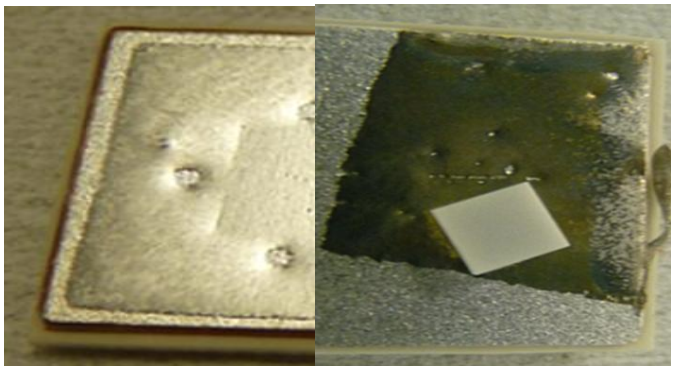


Figure 2.9. Comparison of surface color of solder with (right) and without (left) contamination of DBC surface by $FeCl_3$.

A clear difference of surface color between the two solder joint in Figure 2.9. For these two samples, the DBC was electro-less silver coated by the manufacturer. Therefore, no electro-less silver plating was involved in these two samples. The difference between them was that the one on the left using nitric acid for etching away the silver and copper to fabricate discrete piece and the other one (on the right) using $FeCl_3$. As revealed by the pictures, the residue of ferrite chloride diffused and reacted with the solder and generated the yellow green solder joint. Although 15 minutes of ultrasonic cleaning in both Acetone and ethanol respectively were done after using ferric chloride, the surface was still contaminated. This proved the difficulty to remove ferric chloride.

The DBC used for die-attachment in this work was the same as the one shown in Figure 2.8. Silver electroplating was following the electro-less silver plating. Thus, nitric acid was used to help to remove the residue of ferric chloride.

Electroplating of Ag is divided into two steps. First step is the activation of sample surface with “Silver Strike” plating bath. This plating bath contains high concentration of cyanide ions and low concentration of silver ions (Table 2.3). By applying “high” current density between the sample and the anode (silver plate), silver ions will attack the sample surface, and form a very thin yet porous silver layer. This step has to be very short, up to 30 seconds, so that the porous silver structure would not be too thick to cause weak adhesion problem. For the second electroplating step, the plating bath contains higher

concentration of silver ions (Table 2.4). The plating current density is only half of that used in the strike process. The plating time is about 10 to 15 minutes.

Table 2.3. Component of silver strike solution.

Silver cyanide	6.6 g/L
Potassium cyanide	75 g/L
Potassium carbonate	15 g/L
Temperature	Room temperature
Current density	20 ~ 25 mA/cm2
Duration	Up to 30 seconds
Anode	Silver plate

Table 2.4. Component of silver plating solution [37].

Silver cyanide	36 g/L
Potassium cyanide	60 g/L
Potassium carbonate	45 g/L
Temperature	Room temperature
Current density	10 mA/cm2
Duration	15 minutes for 8.5 µm
Anode	Silver plate

Though plating on pure copper substrate follows the same process as plating DBC, to coat silver on aluminum substrate was different. The process of silver metallization on aluminum surface was shown in Figure 2.10. Zincate treatment was necessary before any plating for metallization on aluminum.

Figure 2.10. Process of silver metallization on aluminum.

A zincate treatment was composed as the following steps:

- Degreasing: mildly alkaline aqueous immersing cleaning
- Etching: highly alkaline solution to remove oxides;
- Desmutting: acid solution to remove the pickling residues of etching;
- Zincate treatment: the zincate treatment can be applied two times, the first zincate layer is removed in nitric acid, and then the aluminium surface is immersed again into the zincate solution. The second zincate layer has a better adherence, finer crystals and is denser [38].

A schematic process of zincate treatment was also shown in Figure 2.11.

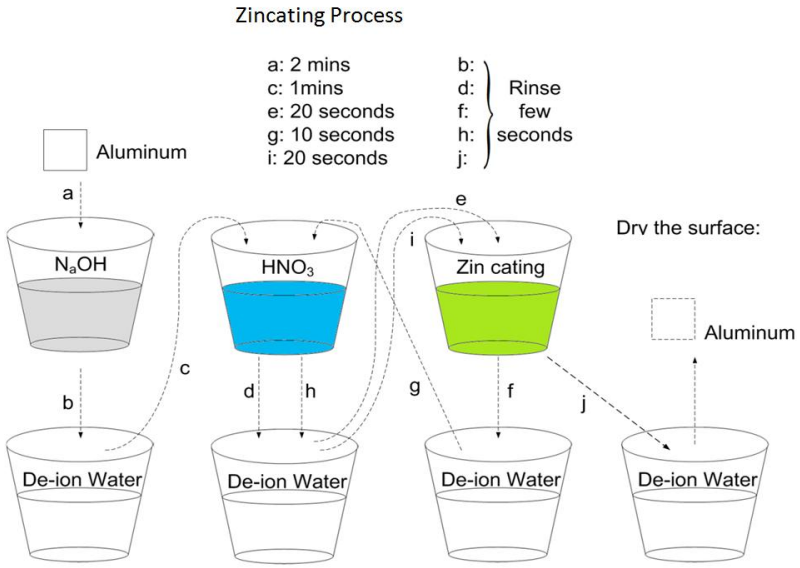


Figure 2.11. Process of zincate treatment.

2.2.3. Plating Examination of Metallization Quality

For both metallization methods, the quality and the adhesion of the metalized layer should be tested. Preliminary testing was done by the surface scratch test and the tape test. Then thermal treatment test was used to test whether the adherence strength of the PVD or the plating layer to the substrate surface was strong enough for used in electronic packaging. Soaking the metalized sample at 300 ^{o}C for half hour was used for this purpose.

Both the silicon die with deposited metal layers and the electroplated substrate passed this examination before being used for the following soldering and sintering.

2.3. Solder Vacuum Reflow

In this work, vacuum chamber (SST MV2200) was used for the process of solder reflow. The advantages of this solder vacuum reflow over the soldering in air were described here:

- Fabricated solder joint of lower voids percentages
- A clean process without using flux

Both of these advantages were of importance.

The occurrence of voids in the soldering process was common and had to be dealt with. Voids could impair the reliability of electronic board assemblies and influenced its electric integrity, mechanical and thermal performance. They limited heat dissipation of components or solder joint structures and influenced the stability of solder joint. They also limited the performance of components in high frequency applications, reduced stability against vibration of components.

Moreover, the vacuum and protective atmosphere provided the chance for soldering without flux. Flux was usually used to facilitate soldering by removing oxidation from the metals to be joined. It made the soldering operation tolerant to an ambient air environment and maintains the solderability of surfaces the heating cycle. However, the flux residue were left behind and they are never completely removed in normal cleaning procedures, and the contamination can impair the performance of solder joint [39].

Weight and fixture were used in reflow process. The weight would further help to reduce the percentage of solder joint (less than 10% or even 5% was preferred). Copper spacer was copper shim with the same thickness. It served as height control of the solder joint. Holes were punched on solder preform at four corners. As shown in Figure 2.12, spacer was insert into the holes.

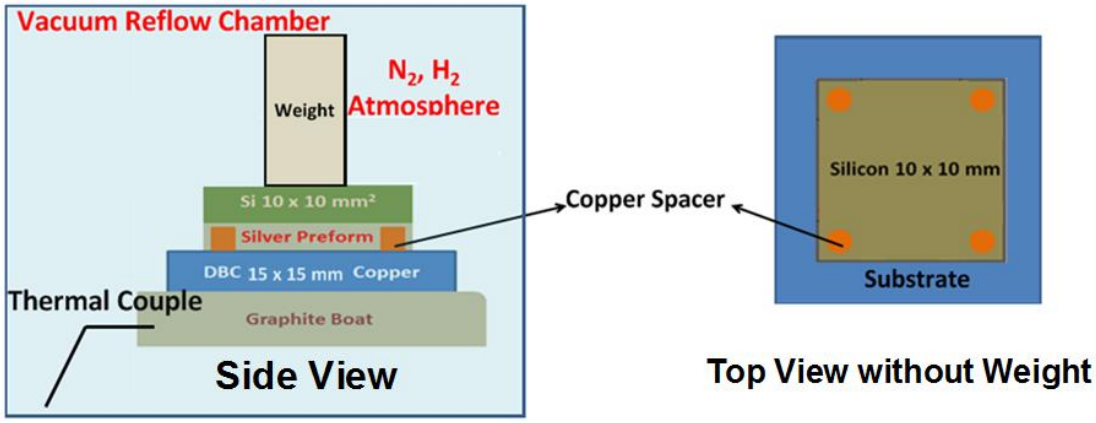


Figure 2.12. Sample configuration for solder vacuum reflow.

The process of fabricating copper spacer is shown in Figure 2.13. To make the surface flat, the copper sheet was pressed by press (Carver, Model 2112-1) (Figure 2.14) under around 3 MPa for 30 minutes at room temperature. Copper spacer fabricated by etching was shown in Figure 2.15. The thickness of solder preform available for both SAC305 and SN100C was 50 µm. Correspondingly, the copper spacer was designed to have the thickness around 35 µm.

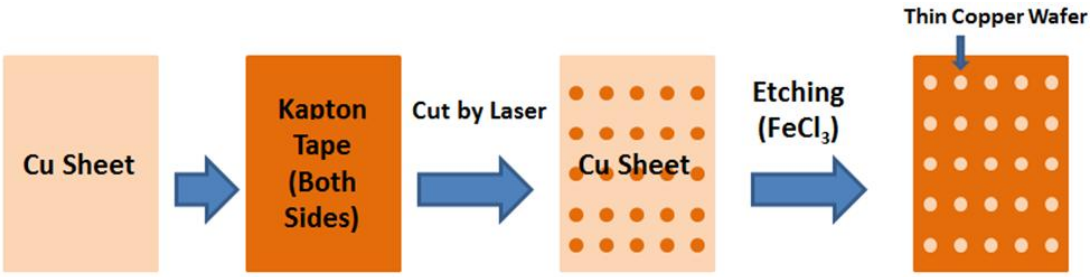


Figure 2.13. Process of fabricating copper spacer.

Figure 2.14. Press.

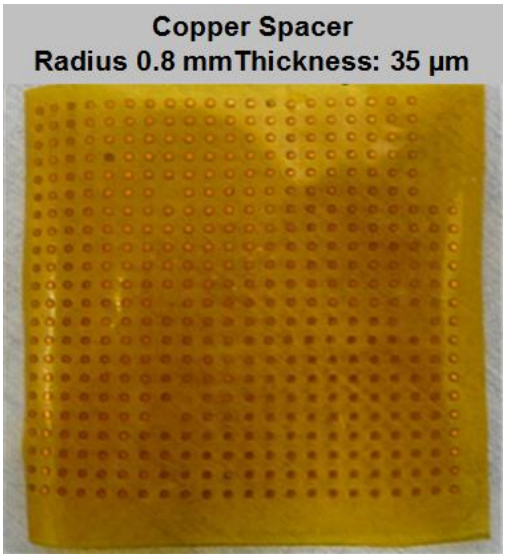


Figure 2.15. Copper spacer for height control.

Before soldering, the horizontal and vertical levels of graphite boat should be checked by gradienter (Figure 2.16).

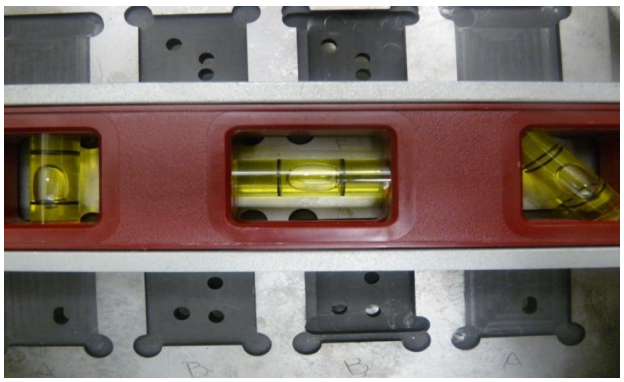


Figure 2.16. Level of graphite boat in vacuum chamber tested by gradienter.

The process of soldering would follow the temperature profile in Figure 2.17, The profile was programmed into the computer of vacuum chamber before soldering.

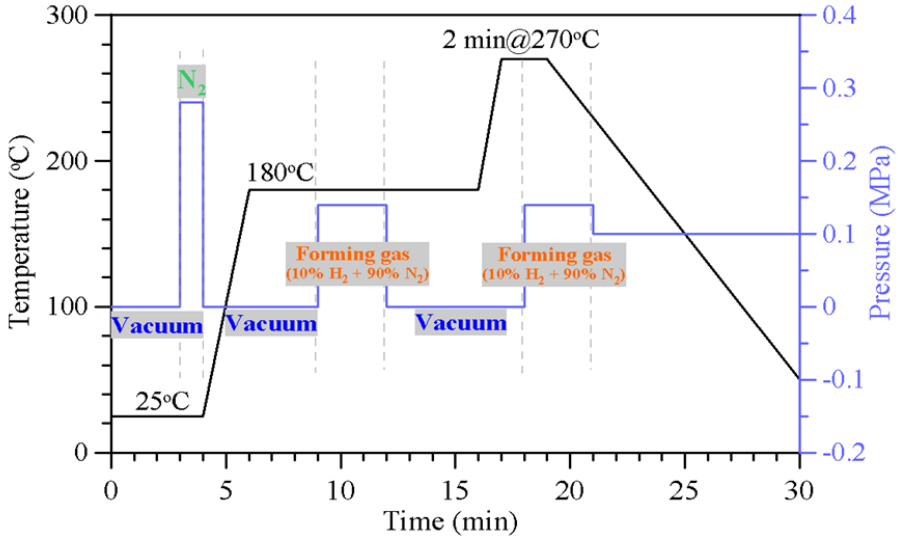


Figure 2.17. Temperature profile for vacuum solder reflow.

2.4. Pressure-Sintering with Double-Printing

In attaching small chips (3 × 3 mm^2) by silver sintering, single drying was enough for the evaporation of organic solvent insider the silver paste and no pressure was added to assist sintering. However, when the size of chip increased to 10 × 10 mm^2, a process with double-printing for drying was used. In addition, 3 MPa pressure was added during sintering. It was necessary to fabricate a strong sintered silver joint. The process flow was shown in Figure 2.18.

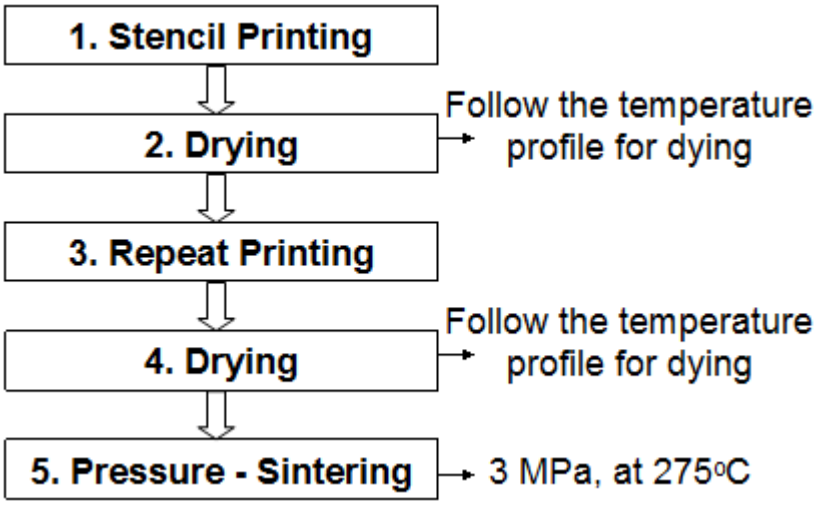


Figure 2.18. The process of pressure-sintering with double printing.

Nano-scale silver paste was printed by stencil, which was made of stainless steel (Figure 2.19).

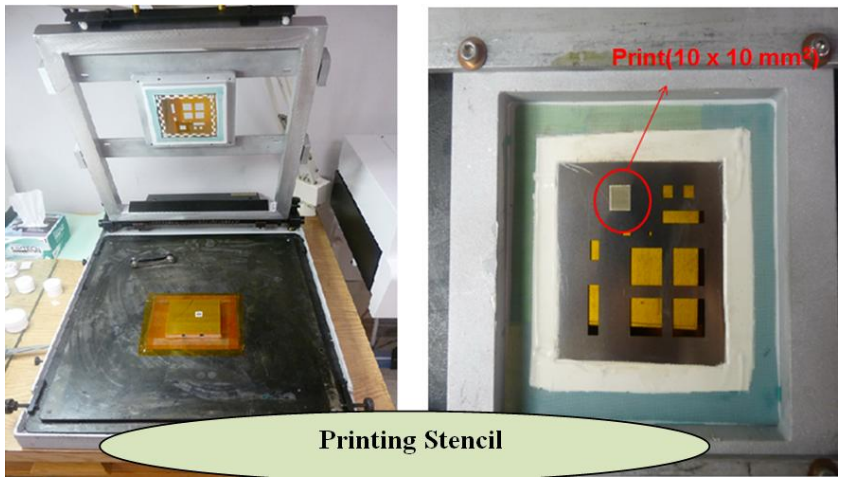


Figure 2.19. Stencil for printing nanosilver paste.

The heating profile in Figure 2.20 was used to dry silver paste. The three drying steps at 50°C, 100°C, and 180°C were designed to gradually remove the organic solvents in the paste to a high green density prior to sintering. A programmable hot-plate was used to control the heating rate as well as soaking time at each temperature step. Ideally the longer the time for drying, the less organics need to burnout at higher temperature, and the

better the bonding performance. However, it became impractical in manufacture if too much time was used in the drying stage. In this profile, a total 70 minutes was designed for drying stage.

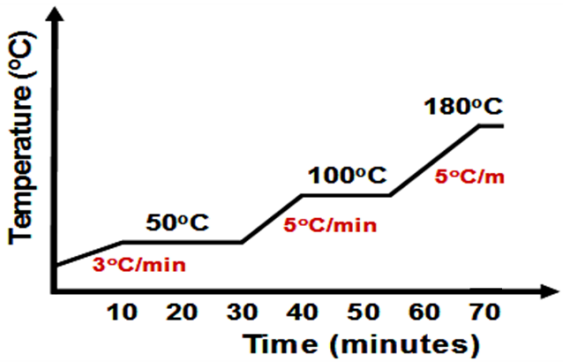


Figure 2.20. Dry profile for nanosilver paste.

Double printing and drying was used to increase the organic evaporation. Compared to small device attachment, say 3 × 3 mm^2, binder burnout became much more severe in large-area device attachment. There was much more organic need to evaporate: the area that directly contacted with air became around 3.3 times larger, but the area that needed evaporation increased around 11 times. Printing and drying twice not just prolonged the drying time, but also provided more access for organics to evaporate. Since the first printed layer had the porous structure and was able to provide more channel for the organics in the second printed layer to come out.

For sintering such a large-area silver paste, a pressure of 3 MPa was found useful and effective in getting high bonding strength. The purpose of the applied pressure was two-fold. Firstly, the pressure forced enhanced contact between the chip and the paste given any surface roughness and curvature of the chip and substrate, and satisfied the need to counter the out-gassing pressure due to the burn-out of organics during the sintering stage. Secondly, the pressure helped in gaining a more uniform and denser sintered microstructure while at the same time compensating for the lower sintering temperature to some extent.

During sintering, a fast heating rate about 100^{o}K/min was used to ramp up the temperature [40]. This was based on observations that rapid heating of a nanoparticle powder produced a denser material, which was influenced by the aggregation at lower temperatures of the nanoparticles prior to densification. The aggregation happened once the organic molecules separating the particles disappeared. Particle aggregation effectively reduced the densification rate because aggregated particles behaved as larger particles and possessed less driving force for sintering.

Based on these consideration, a custom-built hot press (Figure 2.21) was fabricate to provide both the heating and the external pressure. A temperature controller was setup to control the temperature, the heating rate, as well as the soaking time of the hot plate. Here, a period of 30 minutes was used for the soak time at the sintering temperature chips to sinter 10 × 10 mm^2 silver joint.

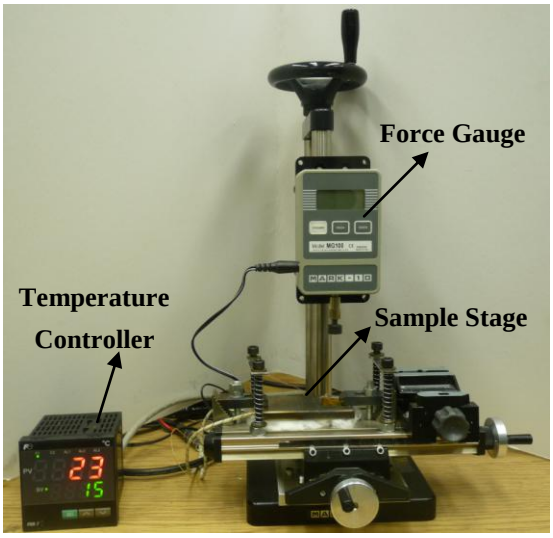


Figure 2.21. A custom-built hot press.

Silicon rubber was put over the chip to evenly distribute the external pressure during sintering. The effect of silicon rubber was demonstrated by testing the pressure-distribution with and without silicon rubber. In this test, sensor film for pressure-distribution was used (Sensor Products Inc.). The original color of the sensor film was light green. When pressure was added on it, the color would be changed into red. The

tested film were compared and shown in Figure 2.22. Clearly, without the rubber, the external press was loaded on just a small part of the silicon chip while it would be evenly distributed with the help from rubber.

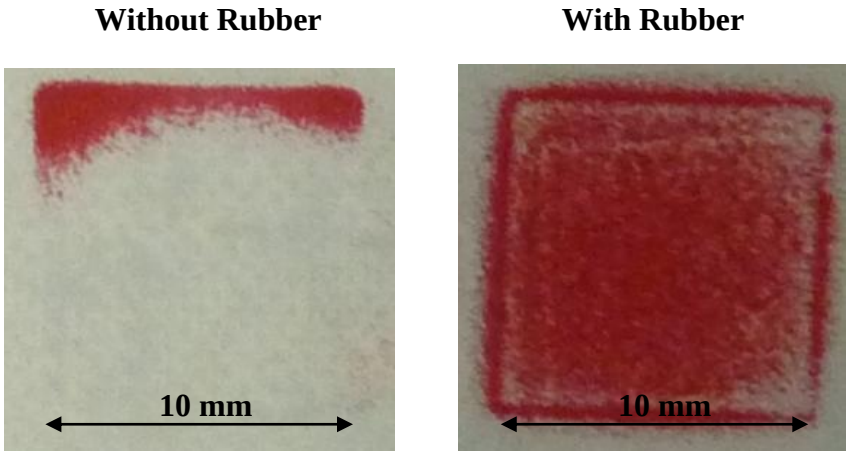


Figure 2.22. Testing of pressure distribution with and without rubber by pressure sensor film.

2.5. Quality of As-Fabricated Samples

An examination of the joint in as-prepared samples was necessary before accelerated temperature cycling or other testing. In this section, just the die-attachment with DBC and copper substrate were shown and tested. Samples of silicon attached to aluminum was shown in Chapter 3.1.

Both solder joint and sintered silver joints were expected to have the same thickness. Micrometer was used to measure the thickness of 6 points around the joint. Here, a rule was used to quantitatively evaluate whether the titling of the joint was within the tolerance. If the measured thicknesses of one tested sample would satisfy the inequation (3-1), then the die-attachment would be considered as of constant thickness of joint.

$\overline{T}$ = Average Thickness of 6 points $\quad T_i$ = thickness of any point

$$\left|\frac{T_i - \overline{T}}{\overline{T}}\right|_{Maximum} \leq 10\% \qquad (3\text{-}1)$$

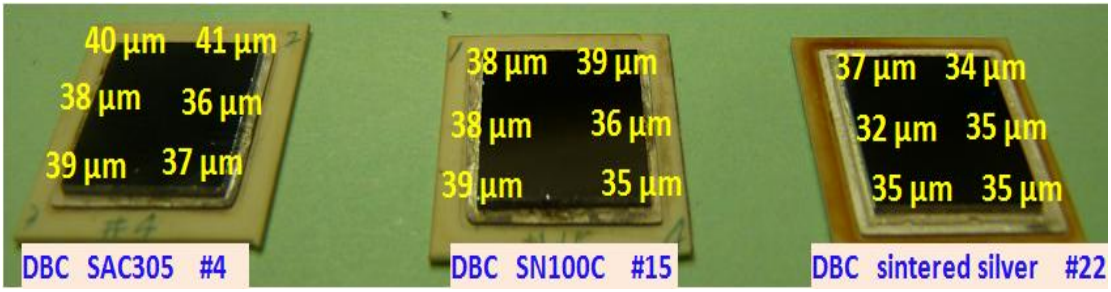


Figure 2.23. Measurement of bond-line thickness in as-prepared samples.

In Figure 2.23, die-attachment with all three kinds of joint were shown. The thicknesses of joint were measured and labeled. According to the inequation (3-1), the extent of tilting for all three samples were within tolerance. One reason to consider the tilting effect was related to the test of curvature measurement in the next chapter. Generally speaking, the extent of bending was expected to be constant for one die-attachment sample. If there was big difference among the bond-line thickness, the curvature of die-attachment would be different when measured from different directions.

Inspection by X-ray technique was also used in this work, which was done by Nordson Dage corporation. X-ray is one of the emerging technologies for non-destructive testing and inspection of electronic packages. It is especially useful when packages are encapsulated. Quality evaluation can be made by accurately detecting flaws and defects such as solder voiding, bridging, solder ball alignment. However, one of the shortcomings of X-ray inspection is that conventional X-ray cannot pass through dense materials such as copper and lead. Therefore in some cases of devices attached on thick copper substrate, X-ray is not very efficient to identify the flaws. Moreover, X-ray lacks the ability to differentiate between layers.

X-ray images in figure 2.24 show that the solder joint was of little voids (voids percent below 5%). This percentage of voids was acceptable [41]. The 4 circles in the X-ray image of SN100C joint were copper spacers. Besides, no cracks or voids were observed from the X-ray image of sintered silver joint.

Those tested samples were cut and the bond-line in the middle of die-attachment was observed by optical microscopy (brand). The cross-section image of sintered silver is also shown in Figure .

Based on these testing, the quality of as-prepared samples had been evaluated.

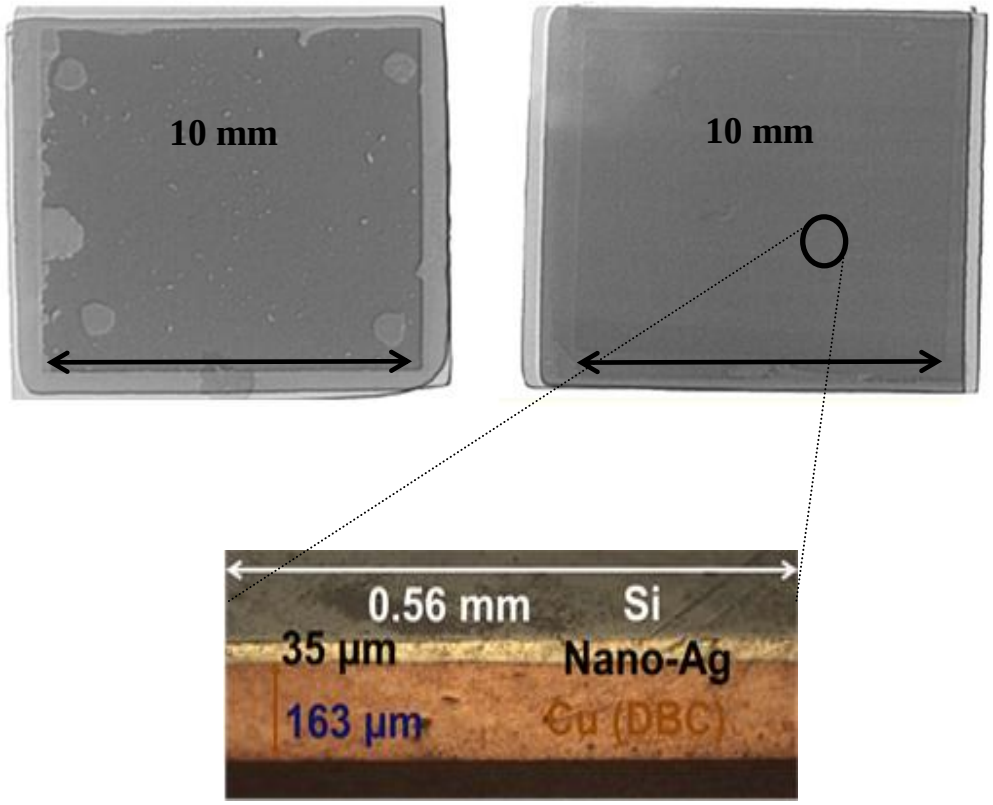


Figure 2.24. X-ray images of as-fabricated die-attach joint, followed by cross-section image under optical microscopy

2.6. Selection of Profile for Temperature Cycling

To speed up the failure rate, thermal cycling test was conducted to investigate the reliability of die-attachment with qualified quality of joint.

Temperature Cycle Testing (TCT) determines the ability of assembly to resist extremely low and extremely high temperatures, as well as their ability to withstand cyclical exposures to these temperature extremes. During this testing, the environment temperature of packaging was alternated between hot and cold extremes at a predetermined rate for a specified number of cycles using temperature cycle chamber.

It is an effective method for stressing wire bonds, solder joints, die bonds, and hermetic seals. Usually, failure mechanisms accelerated by temperature cycling include die cracking and joint failure. The alternating hot and cold temperatures act to flex the junctions, promoting the propagation of micro-cracks or voids which occur as a result of intermetallic compound formation, mismatched CTEs, improper wire-bonding parameters, and similar phenomena. Temperature cycling is becoming more prevalent, particularly in the automotive industry.

3 factors identify a temperature profile for cycling

- the difference between the high and low temperatures used;
- the transfer time between the two temperatures;
- the dwell times at the extreme temperatures.

A temperature profile shown in Figure was selected from JEDEC standard [42] at temperature range from -40˚C to 125˚C. The dwelling time at extreme temperatures is 10 minutes. It took around 100 minutes to finish one cycle.

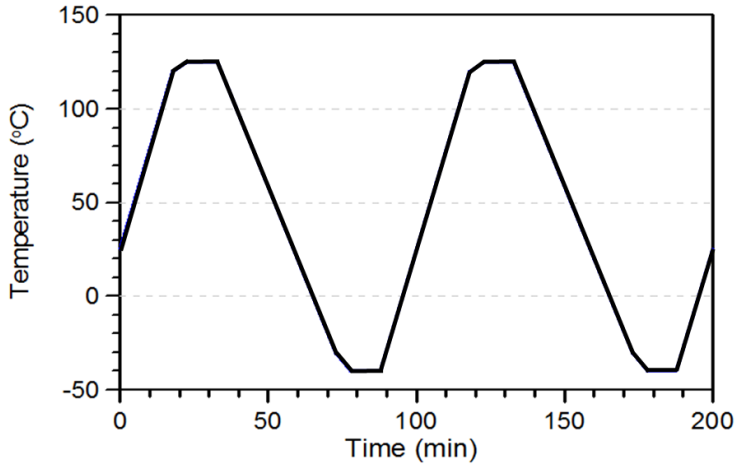


Figure 2.25.Temperature profile for thermal cycling testing.

Chapter 3. EVALUATION OF DIE-ATTACHMENT RELIABILITY BY THERMAL CYCLING TESTING

3.1. Introduction of Residual Stresses

Residual stress is a tension or compression stress that exists in a material without application of an external load. There are essentially two types of residual stresses.

One type of stress is intrinsic. It is related to film growth, and will generally be temperature independent. Factors responsible for this type of stress include deposition conditions, the growth morphology, and the possible lattice mismatch between layers. These additional stresses called “intrinsic stresses” being produced by non-equilibrium growth processes. These non-equilibrium microstructures lead to additional stresses caused by the tendency of the film to shrink or expand once it has been deposited onto its substrate. When the film initially shrinks relative to the substrate, the film is under residual tensile stress. When the film expands relative to the substrate, there is compressive stress on the film. These results are regardless of the specific mechanisms that cause films to stretch or shrink relative to substrates. Sometimes the tensile stresses are sufficiently large to cause a film fracture. Similarly, excessively high compressive stresses can cause film wrinkling and local loss of adhesion to the substrate [43].

The film under compression will expand if the substrate is thin, and the film will bow the substrate so that the film is on the convex side. If the film has a tensile stress, the film will contract, bowing the substrate so that the film is on the concave side. Tensile stress will relieve itself by micro-cracking the film. Compressive stress will relieve itself by bucking from contamination of the surface. If the adhesion between the film and the substrate is high, the stress can cause a fracture in the film or substrate material rather than at the interface. Compressive stress in a ductile material can relieve itself by generating hillocks.

Moreover, when film thickness and substrate thickness are compatible, especially when the substrate is a brittle material, the compressive stresses in the films can be so great that the corresponding tensile stresses in the uppermost layer of the substrate can cause the fracture of the substrate. The fracture, in turn, can cause electrical shorts to occur in the circuit if two metallization layers are in contact. Or it might lead to some form of delayed failure of the interconnecting metal. Such delayed failures might involve either corrosion of the interconnecting metal or electro-migration [44].

It is important to understand the mechanisms of the residual stresses and the mechanical properties of the films so that the circuit structures can be designed for mechanical reliability as well as for electronic device performance. Though the residual stress investigated in this study is not this type, the related knowledge could be use to explain and understand the observation stated later.

The residual stresses in die-attachment belongs to the other type, which is strongly temperature dependent. It is generated because of different thermal expansion coefficients (CTE) among layers. This thermal mismatch induced residual stresses are identified as one of the major causes of voiding and failure of some critical components in electronic packaging.

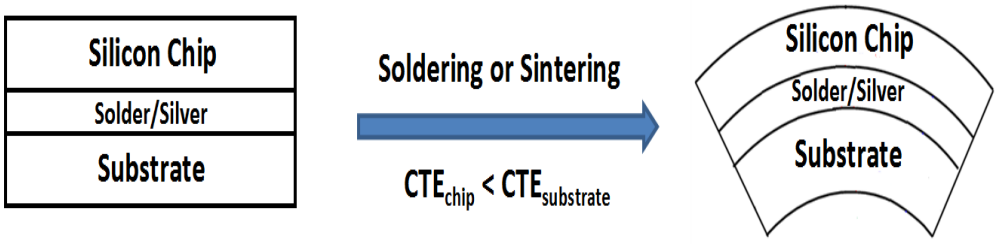


Figure 3.1. Formation of curvature in die-attachment.

Because of mismatch in coefficients of thermal expansion, the system is subjected to residual stresses when it is cooled to room temperature from its fabrication temperature or subjected to temperature change during its applications.

It is well known that silicon has a low CTE in the useful temperature range for electronic, which is as low as 2.6 - 3 ppm/^{o}C at room temperature. As introduced in selection of substrates (Chapter 2), the CTE of DBC (7.4 ppm/^{o}C) is close to that of the silicon, compared to copper (16.5 ppm/^{o}C) and aluminum (23.1 ppm/^{o}C). Therefore, the bending extent of die-attachment on DBC substrates would be much less than these with metals. Correspondingly, much higher residual stresses was expected in metal substrates samples. One thing is worthy of being pointed out here: the previous thought of quicker failure in copper samples than DBC was based on the propose that the residual stresses was harmful to the reliability of the bonding and higher stresses would induce larger rate of micro-cracks growth.

Because both soldering and pressure-sintering involved elevated temperatures (peak temperature around 270^{o}C), large thermal stresses were induced in these materials during the process of interconnecting and remain there during the subsequent use of the devices.

Consider the three layers of die-attachment as a beam. When a bending moment causes a beam to bend, the edge of the beam at the outside of the curve is stretched a little longer, and the inside edge is squeezed a little shorter. Correspondingly, the material at the outside edge is in tension and the inside edge is in compression. Almost each layer of the material gets some stress (internal force) from the bending. There can only be one plane through the bending that isn't either longer or shorter than it was before the bend. Usually, it is named "neutral plane". As shown in Figure 3.2 , above the neutral plane, material is longer than it was at rest, and is therefore in tension. Below the neutral plane, the material is in compression.

Quantitatively, the further from the neutral plane we get, the greater the tension and compression. The blue triangle represents the amount of tension at various distances from the neutral plane, and the red triangle the amount of compression. The shape is a triangle because the amount of elongation or shortening is directly proportional to the distance from the neutral plane; that's just geometry.

The sizes of the triangles keep the tension and compression in balance. They have to stay in balance if the shaft is not to come apart into a lot of little pieces. The forces and moments of tension, through the cross-section, have to equal those of compression.

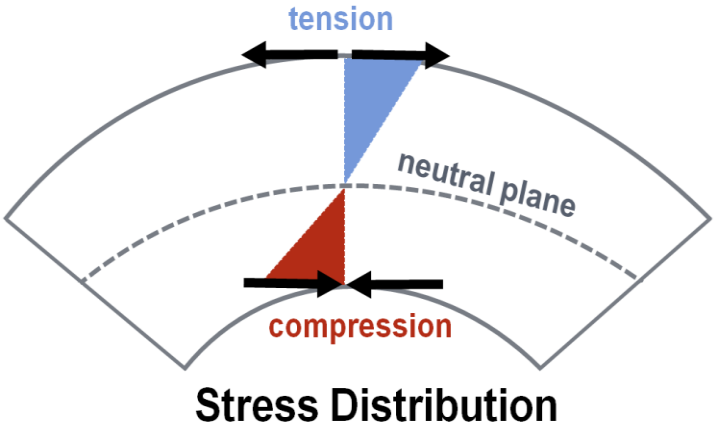


Figure 3.2. Stress distribution in a bending beam.

Residual Stresses in the Die-Attachment with Aluminum Substrate

Observation of as-prepared samples with aluminum substrate, as mentioned, was described here, after the introduction of residual stresses. Similar phenomenon was observed from both soldered and sintered samples with aluminum substrate: silicon chip in as-prepared samples cracked into triangle and parallelogram shape when the environment temperature cooled down to room temperature. Not matter cooling in the Nitrogen atmosphere for soldering or in the air for sintering, cooling stage of both process took less than 15 minutes. Besides, silicon after cracking was still strongly attached to the aluminum substrate by solder and silver joint.

The little difference was: silicon in soldered sample cracked after about 3 weeks after soldering. However, the silicon with sintering cracked (Figure 3.3 Left) within hours after cooling down to the room temperature. This was due to a larger initial stresses within the sintered die-attachment.

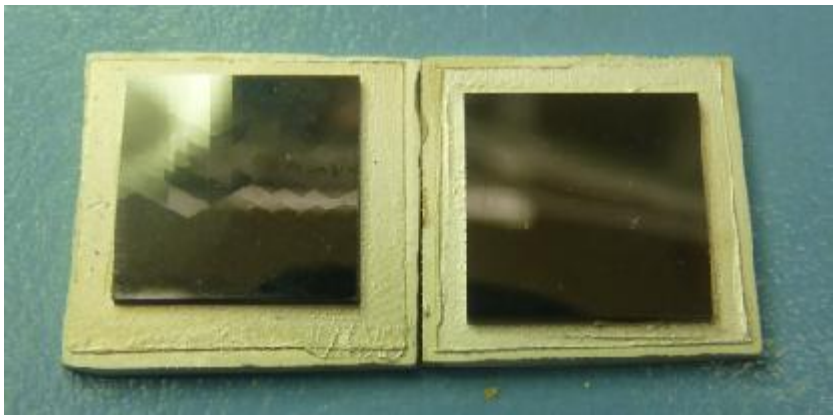


Figure 3.3. Silicon cracks in die-attachment without cracking and silicon without cracking in die-attachment by stress relief annealing.

The larger CTE mismatch between aluminum and silicon attributed to the cracking of silicon, while no cracking in the die - attachment with copper and DBC substrate.

Table 3.1. CTEs of Materials in this work.

Material	**Coefficient of Thermal Expansion ($\mu m \cdot m^{-1} \cdot {}^{o}K^{-1}$)**
Aluminum	23.1
Copper	16.5
DBC	7.4
Silicon	2.5 - 3

To fabricate the die-attachment of silicon on Aluminum without cracking, methods should be found to reduce the initial residual stresses. Stress relief annealing (SRA) was the one used in this study.

The purpose of stress relief annealing was exactly as its name describes – to reduce internal stresses, residual stresses, introduced by prior manufacturing processes such as rolling, machining, grinding, etc. It was performed at temperatures below the phase transformation temperature, and was therefore not designed to produce significant changes in microstructure or mechanical properties of the material. The stress relief anneal

temperature depended on the alloy and physical dimensions of the material. Annealing occurred by the diffusion of atoms within a solid material, so that the material progressed towards its equilibrium state. Heat was needed to increase the rate of diffusion by providing the energy needed to break bonds. The amount of process-initiating Gibbs free energy in a deformed metal was also reduced by the annealing process. In practice and industry, this reduction of Gibbs free energy was termed "stress relief". If a small amount of thermal energy was added (temperature below the eutectoid transformation temperature) the dislocations rearrange themselves into networks to relieve residual stresses. By this heat treatment, the ductility of materials was improved and strength did not change.

The relief of internal stresses was a thermodynamically spontaneous process; however, at room temperatures, it was a very slow process. The high temperatures at which the annealing process occurred served to accelerate this process. Usually, parts were heated to temperatures of up to 600 - 650ºC (1112 - 1202ºF), and held for an extended time (about 1 hour or more) and then slowly cooled in still air.

On the other hand, temperature for stress relief should not be too high. In annealing steel, heating temperature should be below the eutectoid transformation temperature to remove the effects of prior cold work and grain deformation. This allowed further forging or rolling operations. The requirement of heating temperature came from the consideration of recrystallization. When recrystallization occurred, new grains started to grow at the grain boundaries. The new grains had not been strain hardened and the recrystallized metal was ductile and has low strength. Most metals have a recrystallization temperature equal to about 40% of the melting point. The melting temperature of aluminum is 933^{o}K. So the temperature for annealing should be lower than 373^{o}K, that was 100^{o}C [45].

Silicon attached Aluminum substrate with sintered silver was repeated following the same process described in Chapter 2. Heating at 100^{o}C for 30 minutes as shown in Figure 3.4 was added after the sintering. Here, the cooling rate was designed to 13^{o}C/min, which was the cooling rate of pressure-sintering stage after soaking at the peak temperature.

Silicon did not crack (Figure 3.3 right) and therefore the target for reducing initial residual stresses was achieved.

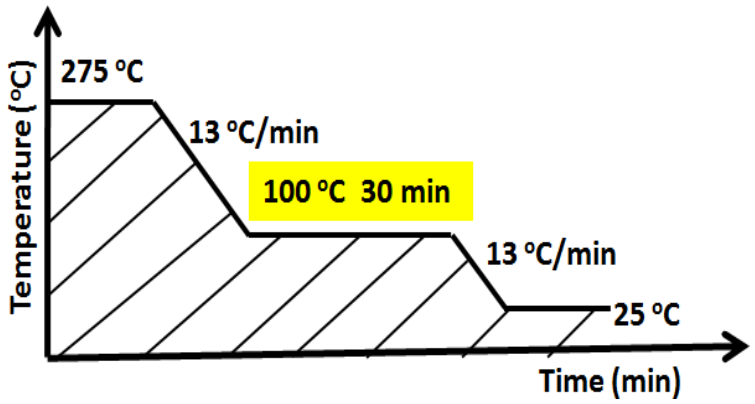


Figure 3.4. Temperature profile for stress relief annealing.

3.2. Curvature Measurement by Laser Scanning

The next step in this work was to find a reliable method to obtain the value of residual stresses by measurement and calculation. Mechanical methods such as hole drilling, curvature measurements, and crack compliance were the common methods to measure residual stress by changes in component distortion. Diffraction techniques such as Electron, X-Ray and neutron diffraction were also widely used. Other methods including magnetic, ultra-sonics, piezo-spectroscopy photo-elastic and thermo-elastic techniques were also being developed. Method of curvature measurements were introduced here.

Curvatures could be measured without direct contact methods (video, laser scanning, grids, double crystal diffraction topology). For a film–substrate bilayer bending composite (Figure 3.5), curvature is related to the residual stress using Stoney's equation.

$$\sigma = \frac{E_S}{6(1-\nu_S)} \frac{d_s^2}{d_f} \left[\frac{1}{R_2} - \frac{1}{R_1} \right] \qquad \text{Equation (3-1)}$$

In equation (3-1), $E_s/(1-\nu_s)$ was the substrate biaxial modulus, d_s and d_f were substrate and film thickness, R_1 and R_2 were radii of curvature of substrate before and after deposition respectively. It is assumed that $d_f << d_s$ [46].

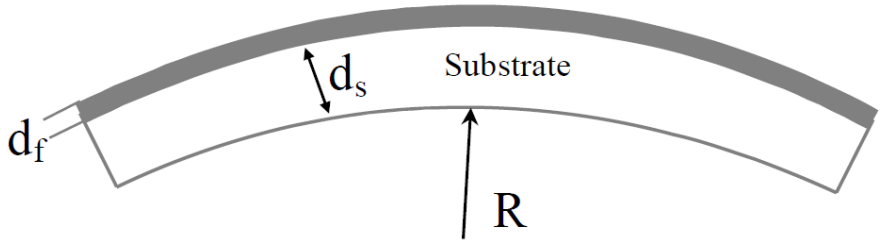


Figure 3.5. Schematic of bi-layer bending.

So, after the curvature 1/R of the bi-layer composite was obtained, the stress in the film could be estimated by using the Stoney formula. In this study, method of curvature measurement was used to estimate the residual stresses. However, a more complex model was used to calculate the stresses based on the curvature measurement since the fabricated die-attachment was a bending with three layers. The model for calculation was introduced in Chapter 3.4.

The optical setup for the curvature measurement was shown in Figure 3.6 and its schematic is shown as in Figure 3.7

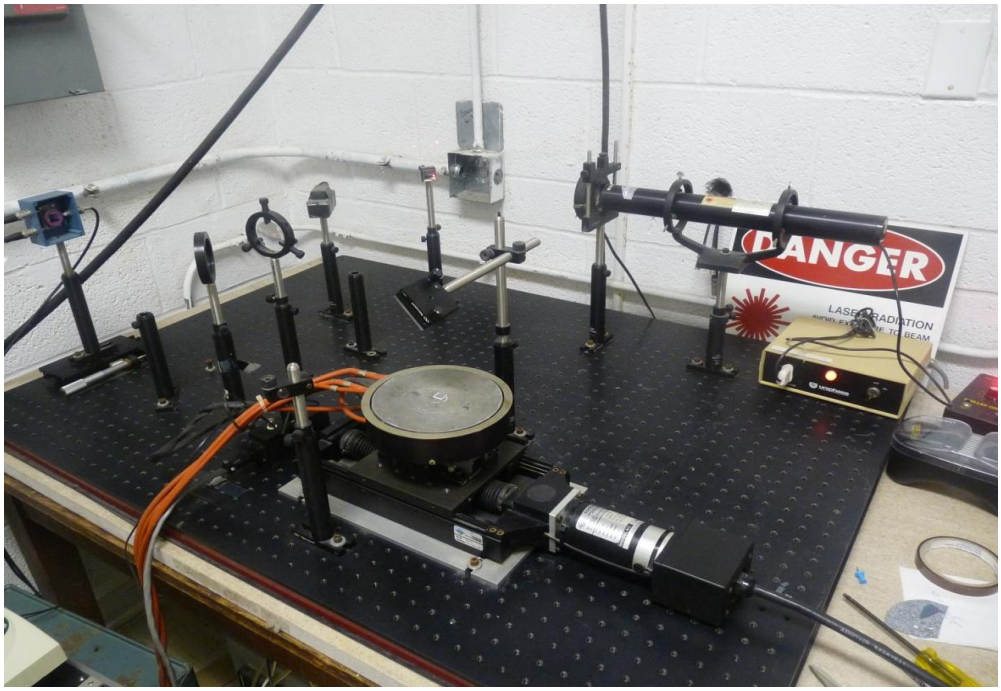


Figure 3.6. The optical setup for the curvature measurement.

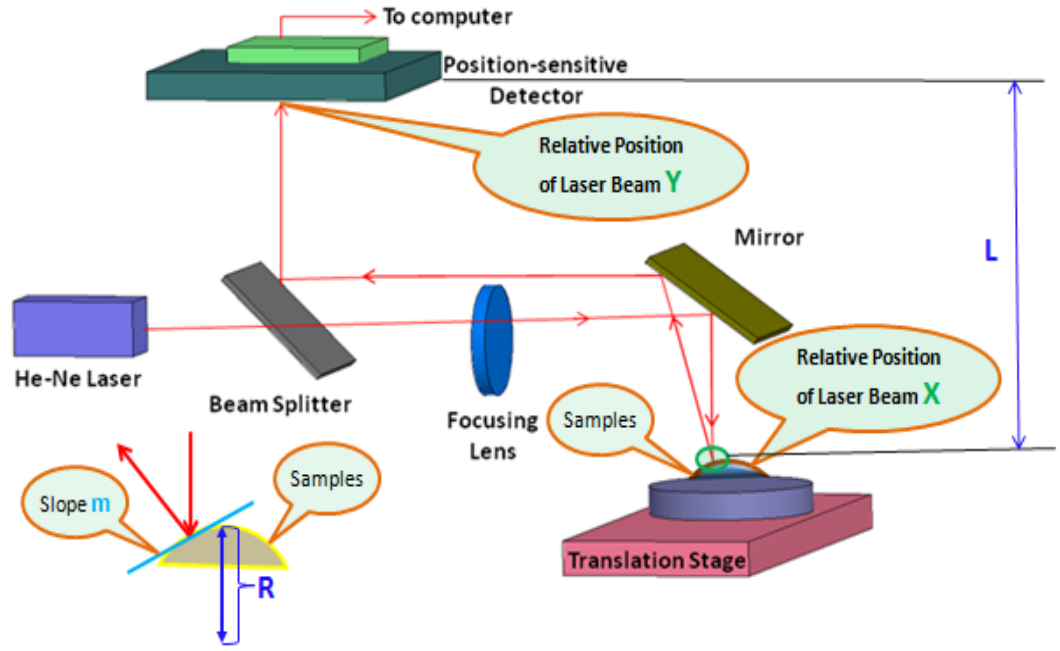


Figure 3.7. Schematic of the optical setup for the curvature measurement.

The optical setup mainly consisted of two parts: the optical scanning component and the hot stage mounted on the translation stage. Specifically, it consisted of a low-power HeNe laser (4 mW), beam splitter, mirror, focusing lenses, and a position-sensitive detector. During the curvature measurement, a bi-layer composite specimen was placed on the setter in the hot stage with the coated surface facing down. Then the smooth substrate surface (typically silicon) would reflect the incoming laser beam. The translation stage could carry the specimen to move so that the laser beam scanned a certain distance d on the curved composite specimens as shown in Figure 3.8. During the scanning, the reflected laser beam would be projected onto a position-sensitive photo-detector so that the distance changes d' due to the curvature could be recorded.

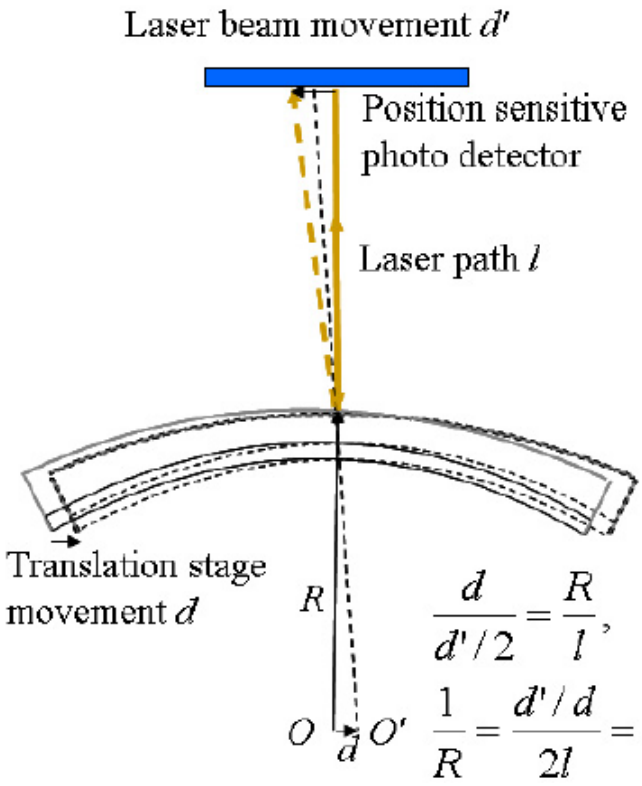


Figure 3.8. Mechanism of curvature measurement by optical set-up [46].

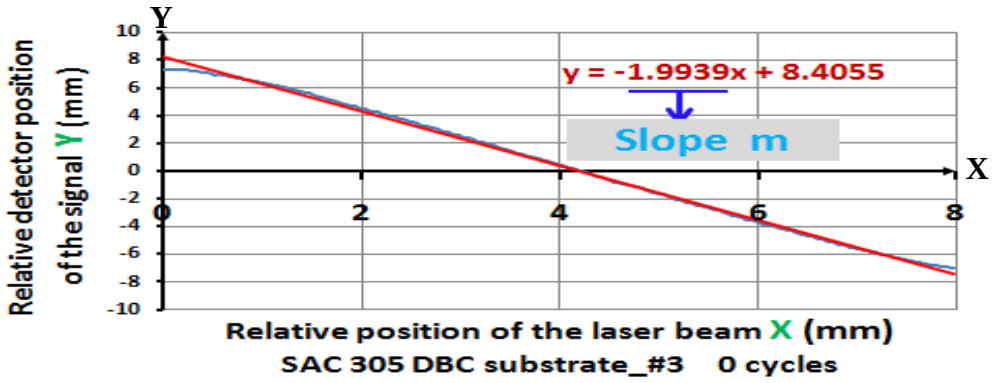
Figure 3.9. Schematic of the position-sensitive photo-detector [47].

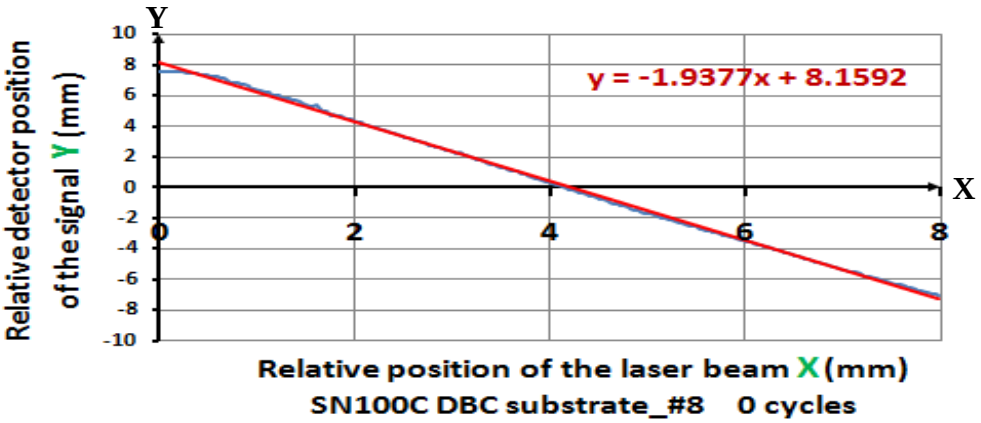
The position-sensitive photo-detector (Hamamatsu Corporation) could linearly change the perpendicular positions of an incoming laser beam into the output voltage values as shown in Figure 3.9. With the assistance of the photo-detector, the translate relationships in the optical setup during the measurement were shown in Figure 3.8. In the relationships, m=d'/d is the slope during the curvature scan and it could be determined by the experiment. So once the length of the optical path length L is measured, we can get the value of curvature, which equaled to 1/R.

Simply speaking, the curvature of the tested sample would calculated by using equation (3 -2), where m was obtained by scanned data and L was constant. In this study, L is 0.85, the distance between the substrate and detector.

$$\kappa = \frac{1}{R} \approx \left(\frac{m}{2L} \right) \qquad \text{Equation (3-2)}$$

The original result from the scanning were two column of data. They, respectively, represented the relatively detector position and relative position of the laser beam. The data of detector position from scanning was record by the electrical signal, that is, the voltage. Thus it need to time a factor 0.65 to be converted into data in length. Figure 3.10 showed examples of the slope, m, from curvature scan. DBC substrate was used in all these three scanned samples.





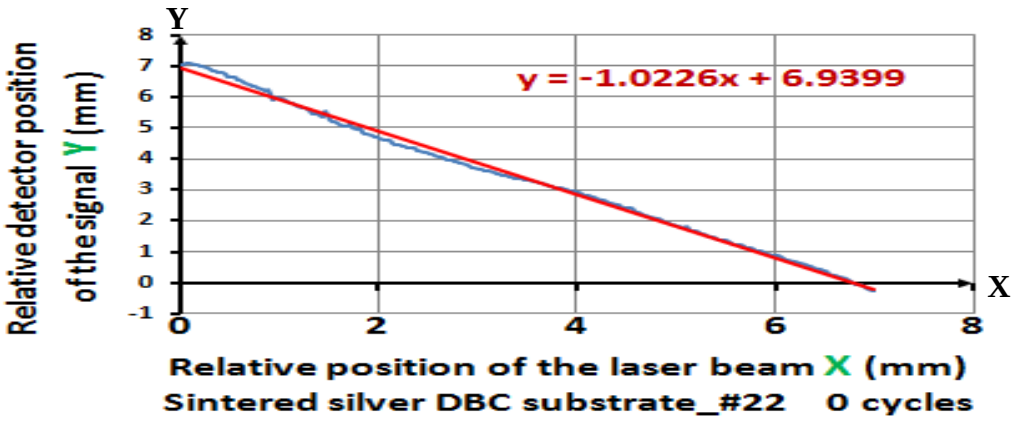


Figure 3.10. Plots of the position-sensitive detector versus sample position to determine the bending curvatures.

3.3. Calculation of Residual Stresses from Curvature

C.H. Hsueh proposed a model of elastic deformation of multilayers due to residual stresses [48]. Using this model, residual stresses was calculated from the curvature. The structure of die-attachment was considered as a 3-layer system. This system with different thicknesses was shown in Figure 3.11.

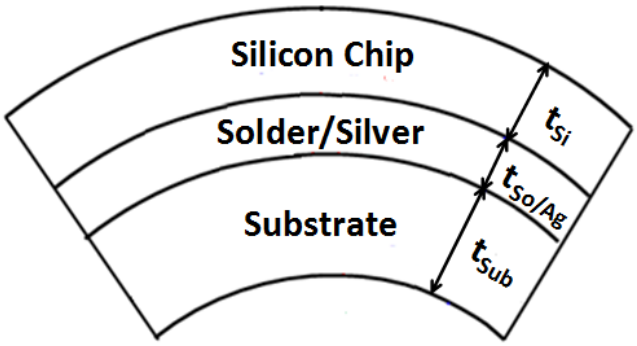


Figure 3.11. Schematic of 3 layers of bending in the die-attachment.

The strain distribution in the system, ε, could be decomposed into a uniform component *c* and a bending component $(z - t_b)k$. The strains may still be different in each layer.

$$\varepsilon = c + (z - t_b)\kappa \qquad (for -t_s \le z \le h_n) \qquad \text{Equation (3-3)}$$

where *z* represented the distance between layers and the surface of the substrate; t_b was the location of the bending axis. κ This location was defined as the line in the cross section of the system where the bending strain component was zero (while it was between $-t_s$ and h_n, t_b

may be not exactly at $z = 0$ due to the different properties and thickness in each layer); c and t_b was calculated by the equations below:

$$c = \frac{(E_s t_s \alpha_s + \sum_{i=1}^{n} E_i t_i \alpha_i)\Delta T}{E_s t_s + \sum_{i=1}^{n} E_i t_i} \qquad \text{Equation (3-4)}$$

$$t_b = \frac{-E_s^{\,2} t_s \sum_{i=1}^{n} (E_i 2 t_{i} \quad +}{2\ E_s \quad t_s + \sum_{i=1}^{n} \quad E_i \quad) t_i} \qquad \text{Equation (3-5)}$$

where the subscripts *s* and *i* represent the substrate and the i_{th} layer, respectively; α is the coefficient of thermal expansion; E is the biaxial modulus, which is equal to the Young modulus divided by (1-v), where v is the Poisson's ratio, and ΔT is the temperature difference during the process of assembly. In this experiment, the ΔT is 245^{o}C for samples fabricated with solder and 250^{o}C for samples with sintered silver.

The DBC used in the experiment was considered a three-layer composite, and the properties of each layer were used for calculation. All the properties of materials are shown in Table 3.2. Based on these properties and the calculated strain, residual stresses were calculated.

$$\sigma_i = E_i(\varepsilon - \alpha_i \Delta T) \qquad \text{Equation (3-6)}$$

Table 3.2. Properties of Materials.

	Alumina (94%)	Copper	Solder	Silver [49]	Silicon
E_i(GPa)	3.00E+11	1.20E+11	5.1E+10	9.00E+09	1.31E+11
α_i(μm·m^{-1}·K^{-1})	8.10E-06	1.65E-05	2.21E-05	1.96E-05	3.00E-06
t_i (m)	4.00E-04	1.75E-04	4.0/8.5E-05	3.5/6.5E-05	5.05E-04
v_i	0.21	3.40E-01	0.4	0.37	0.28

It was clear that the residual stress σ and strain ε in each layer maybe different. In this work, just the strain and residual stress in the silicon layer were calculated.

3.4. Reduction of Residual Stresses with Temperature Cycling

As-prepared samples by both soldering and sintering (Silicon on DBC and Silicon on Copper) underwent 800 of temperature cycles (40°C - 125°C). Every 100 cycles (around 1 week), all die-attachments were taken out of thermal chamber for curvature measurement. All the data was organized and correspond residual stresses was calculated from these data.

No direct debonding was observed among all the samples after 800 temperature cycles. Curvature data and corresponding residual stresses was organized and shown in the graph below (Figure 3.12).

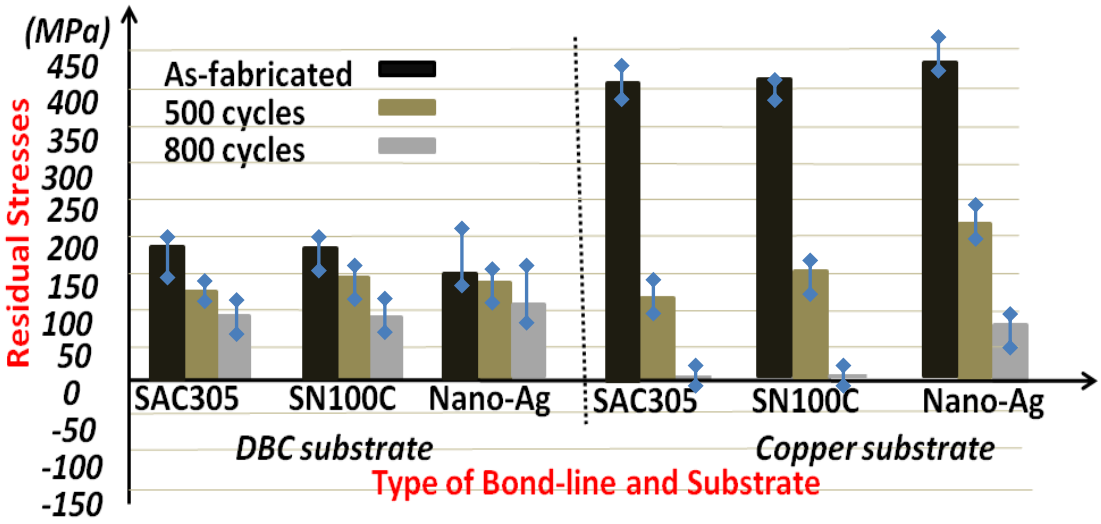


Figure 3.12. Deduction of residual stresses in all die-attachment after temperature cycling.

Obviously, not matter what kind of substrate or die-attach materials, residual stresses released in all samples after temperature cycling.

As expected, higher initial stresses was generated in as-prepared samples with copper substrate than these with DBC substrate. Moreover, the rate for stress deduction was different: stresses released around 5 times faster in copper samples than that in DBC samples. This indicated that the extent of bending is decreased faster in copper samples.

Besides, stresses released faster in soldered samples than corresponding sintered silver samples and so the change of bending extent.

These observations led us to think about what was the mechanism of stress deduction. Generally, there were two way: the growth of microcracks and plastic deformation. Now, a new target was clear: to find out which of these two ways that could be applied to the mechanism of stress deduction in solder and sintered silver. To achieve this target, images of joints with high magnification after 800 cycles were necessary. SEM was used to obtain this kind of images.

One thing need to be pointed out here: the reason why the temperature cycling was stopped at 800 was that: the curvature or the residual stresses in the die-attachment of silicon-solder-copper already became 0 after 800 cycles. The joint failure was likely to occur at this stage.

3.5. SEM Image of Joints After 800 Temperature Cycling

SEM is a powerful tool in inspecting the microstructure of electronic components and material interfaces. Major steps include sectioning and cutting, mounting, planar grinding, polishing and etching.

Most samples need to be sectioned to the area of interest using abrasive cutting or diamond wafer cutting. The latter is a better approach to cut electronic components because it causes less damage to the samples. Next, a mounting operation protects the specimen edge and maintains the integrity of a material's surface features. This step is done by encapsulating specimen using mounting resins (acrylic resins, epoxy resins, and polyester resins). Depending on the encapsulation depth of the site of interest, a second sectioning may be needed. A subsequent planar grinding planarizes the sample cross-sections and exposes the exact area of interest. A sequentially decreasing grit/particle size of the silicon carbide abrasive paper is normally used. For electronic components that have multiple materials with various hardness, it is recommended that fine abrasives such as 800 or 1200 grit SiC be used after sectioning to prevent brittle devices such as silicon from cracking. A coarser grit abrasive might produce more damage to the specimen that sectioning. Hard ceramic substrates, such as alumina, should be rough

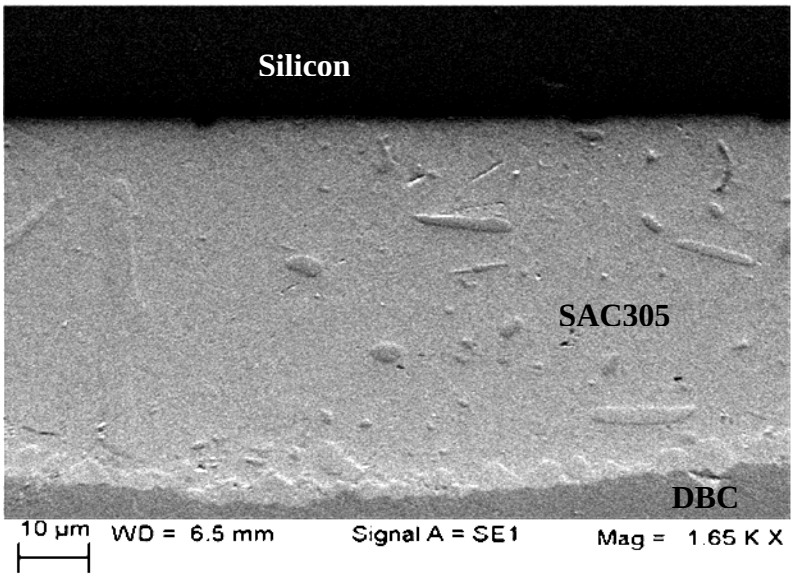
polished with diamond lapping films to minimize edge rounding. For SEM analysis, polishing of the specimen using diamond or alumina fine powder is usually required. The particle size starts from 5 μm, 1 μm, and can be as fine as 0.05 μm. Ultrasonic cleaning is recommended after every particle size polishing to thoroughly clean the surface because residual powder from last polishing step may contaminate the next level polishing mixtures and cause scratches on the sample surfaces. Figure 3.13 showed the Cross-section sample in epoxy after polishing.

Figure 3.13. Cross-section sample in epoxy after polishing.

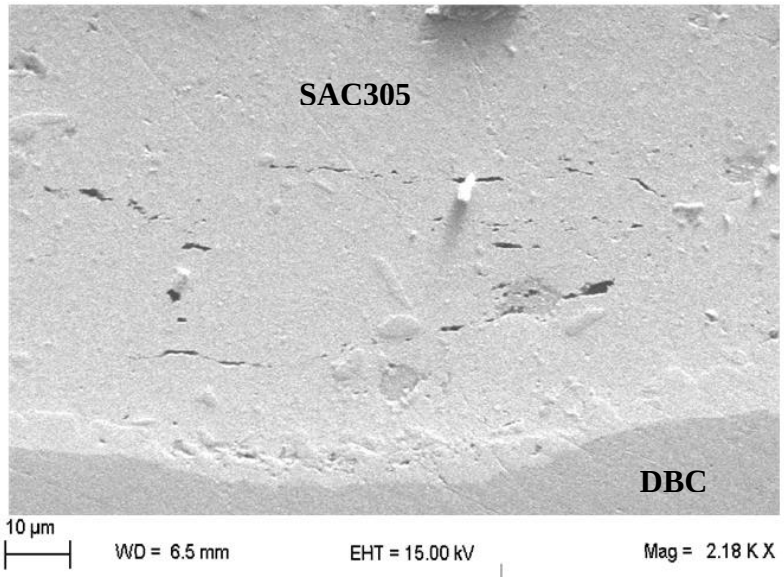
SEM Images of joints from die-attachment after 800 temperature cycles were shown below. The images would be divided into 2 parts: samples with DBC substrate and samples with copper substrate. In each part, images would be shown in the sequence of first SAC305 joint, then SN100C joint and finally sintered silver joint. For each of 2 part, a general discussion and conclusion would be given.

Figure 3.14 showed SAC305 joints with DBC substrate. Around 95% of the solder joint in this die-attachment was similar to the part of joint shown in Figure 3.14 (a). Few cracks or voids was observed. However, sphere, rod-like or axiolitic texture were distributed in the homogenous solder joints.

In Figure 3.14 (b) , cracks at the scale of 10 - 30 micron were observed. The location of these cracks were close to the solder-substrate interface.



(a)



(b)

Figure 3.14. Solder joint in Si-SAC305-DBC die-attachment after 800 temperature cycle.

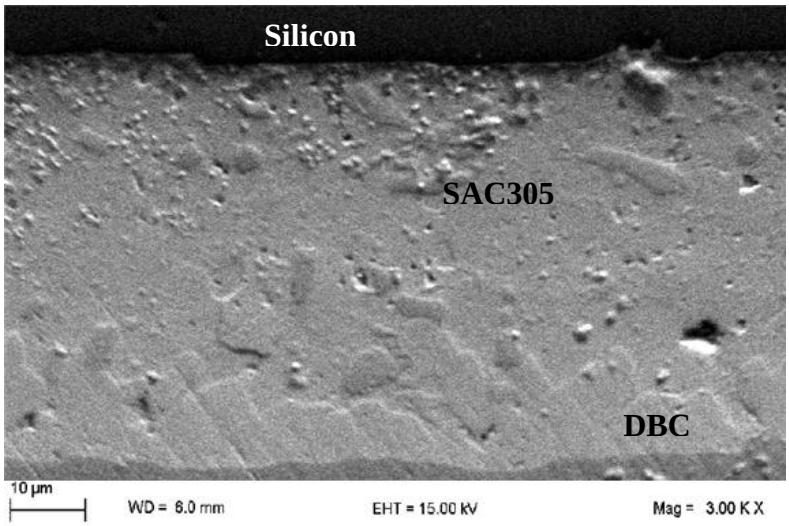
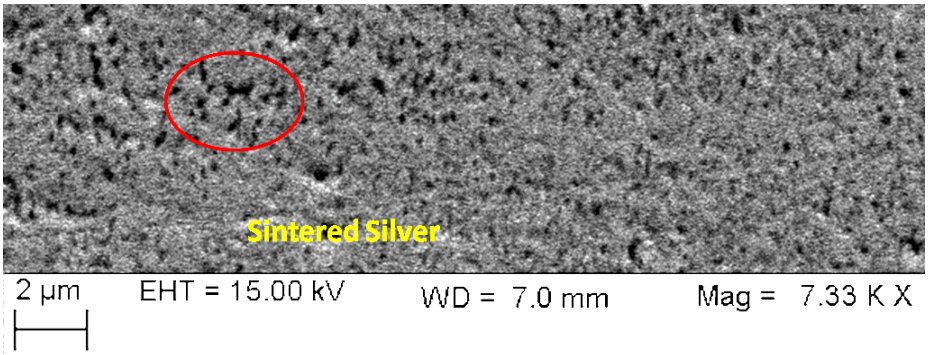


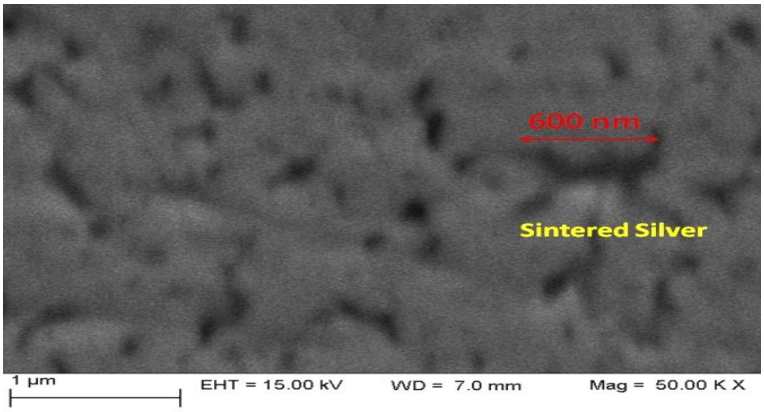
Figure 3.15. Solder joint in Si-SN100C-DBC die-attachment after 800 temperature cycle.

Figure 3.15 showed the SN100C joint with DBC substrate. No crack propagation across the whole joint. However, similar to SAC305 joints, sphere, rod-like or axiolitic texture were detected from the SEM image.

Figure 3.16 showed the sintered silver joint with DBC substrate after 800 cycles. Due to the porous structure of nano-scale silver paste, sintered silver was also with well-distributed pores. The largest pore was shown in Figure 3.16 and marked by a red ellipse. To further estimate the pore size, an image with higher magnification was shown in Figure 3.16 (b). The largest pore was of length around 600 nm. This indicated that the size of porous silver was within a comparatively low range, even after hundreds of temperature cycling.



(a)



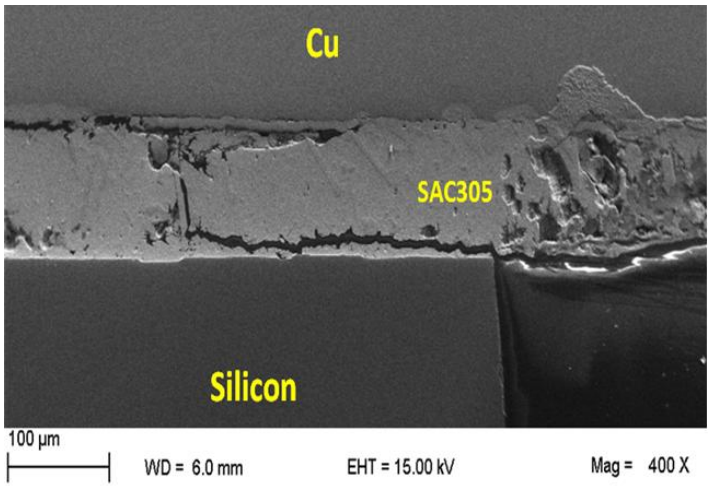
(b)

Figure 3.16. Sintered silver joint in Si-sintered silver -DBC die-attachment after 800 temperature cycle.

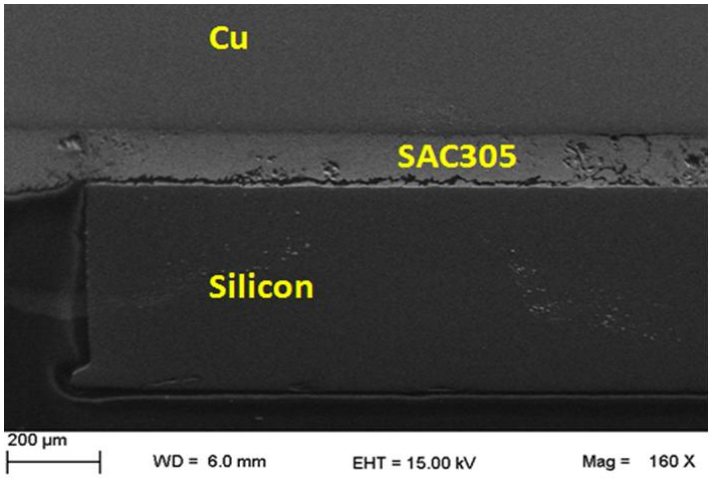
Based on the above SEM images from samples with DBC substrate, no joint failure were observed for all 3 kinds of die-attach materials. However, cracks with 10 -20 µm length were detected in the SAC305 solder joint. Besides, both solder joints show sphere, rod-like or axiolitic texture. According to the research of solder joint failure [50], these texture was likely to be the evidence of intermetallic growth, which initiated the growth of microcracks.

As mentioned in Chapter 2.1, larger CTE mismatch was between copper and silicon. Thus, compared with DBC die-attachment, a quicker failure may be observed.

Figure 3.17 showed the SEM images of SAC305 solder joint with copper substrate. Figure 3.17 (a) and (b) showed the two edge of solder joint. Cracks at the scale of hundreds of micron, or even millimeter, were observed at both edges. In Figure 3.17 (c), it was clearly shown that the cracks were initiated at the edge of solder-silicon interface. Additionally, the horizontal crack would become vertical and then continue grow in horizontal way (Figure 3.17 (a)). Moreover, in the Figure (c) , sphere, rod-like or axiolitic texture were also detected.



(a)



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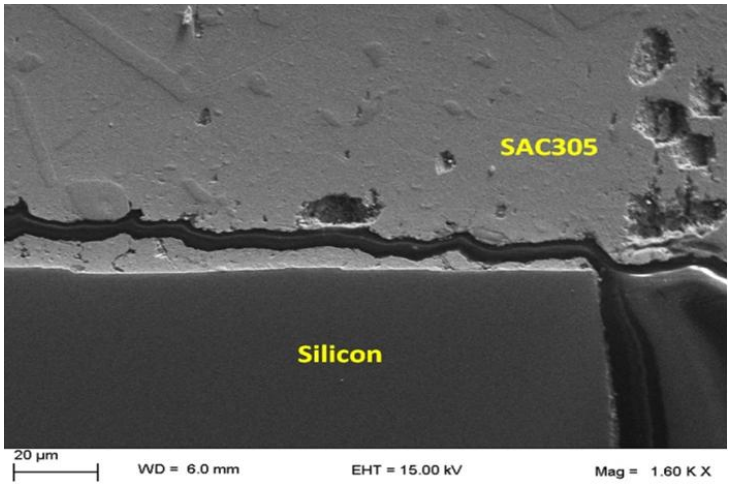
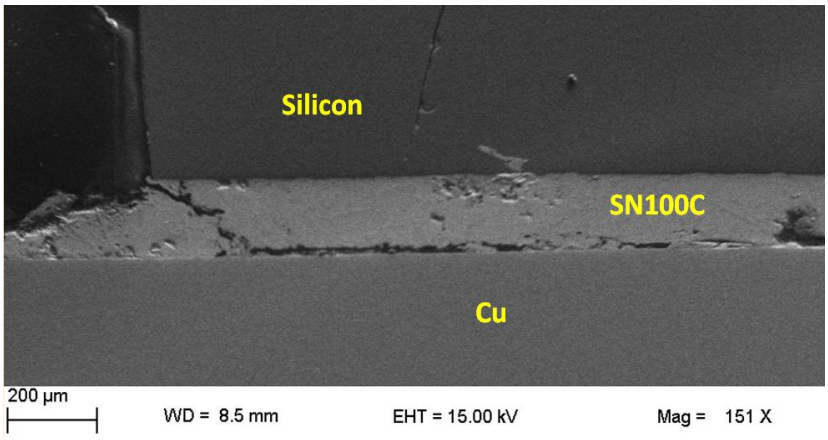


(c)

Figure 3.17. Solder joint in Si-SAC305-Cu die-attachment after 800 temperature cycle.

Figure 3.18 showed the SEM images of SN100C joint with copper substrate after 800 cycles. Figure 3.18 (a) and (b) showed the two edge of solder joint. Similar to SAC305, cracks at the scale of hundreds of micron were observed at both edges. However, at one edge, crack grow in a way with branch-shape as shown in Figure 3.17 (b). The crack was initiated at the silicon-solder interface, and it grew downward with an angle around 45^{o}C. Then it elongated along the solder-copper interface.



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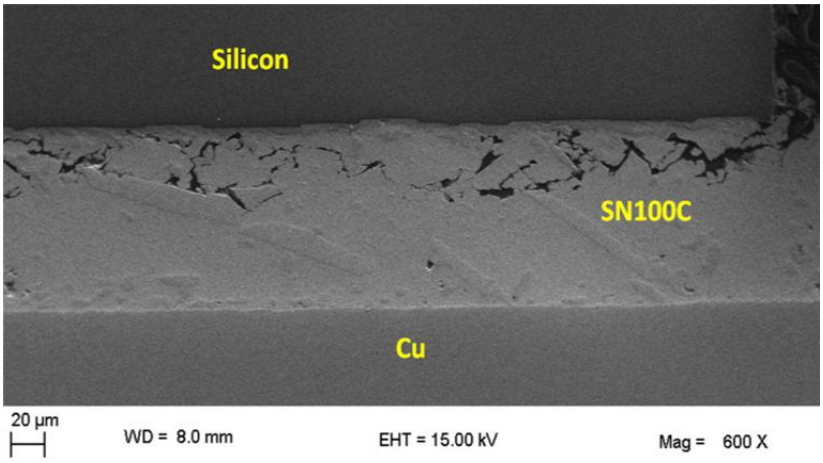

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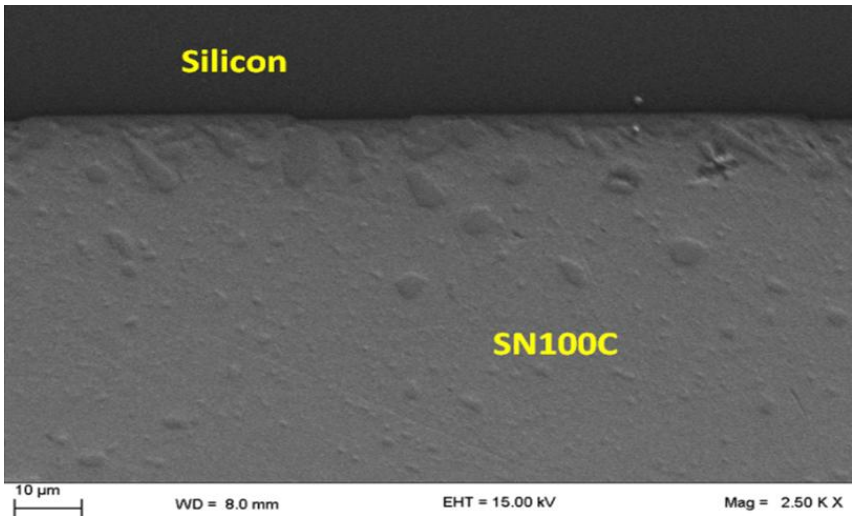
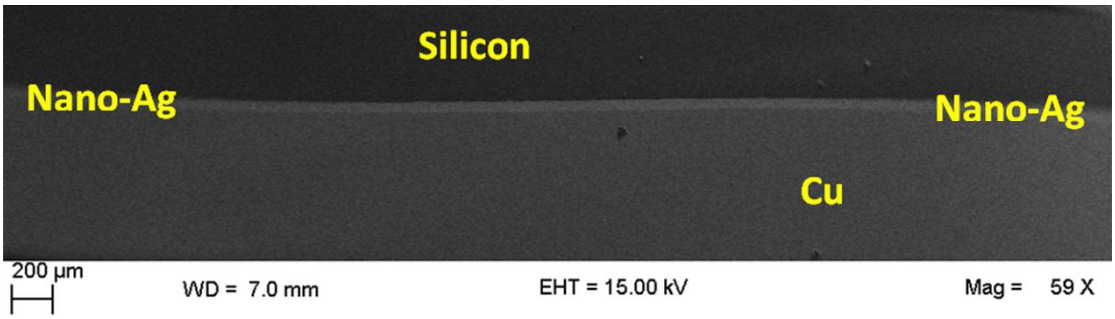


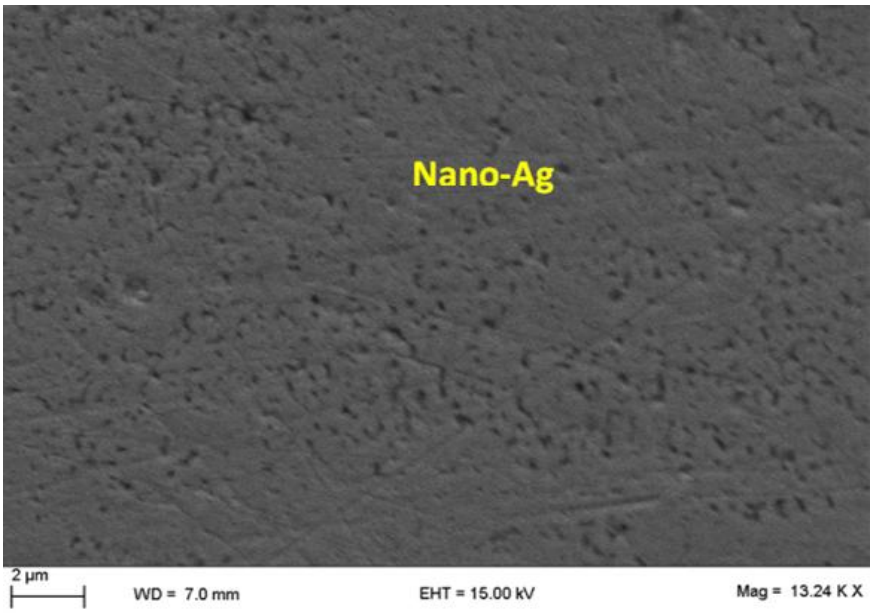
(c)

Figure 3.18. Solder joint in Si-SN100C-Cu die-attachment after 800 temperature cycle.

Figure 3.19 showed the SEM images of sintered silver joint with copper substrate. No cracks at the scale of tens of micron were observed. Even in image with higher magnification (13.24 X), no pore was observed of length at hundreds of micron scale.



(a)



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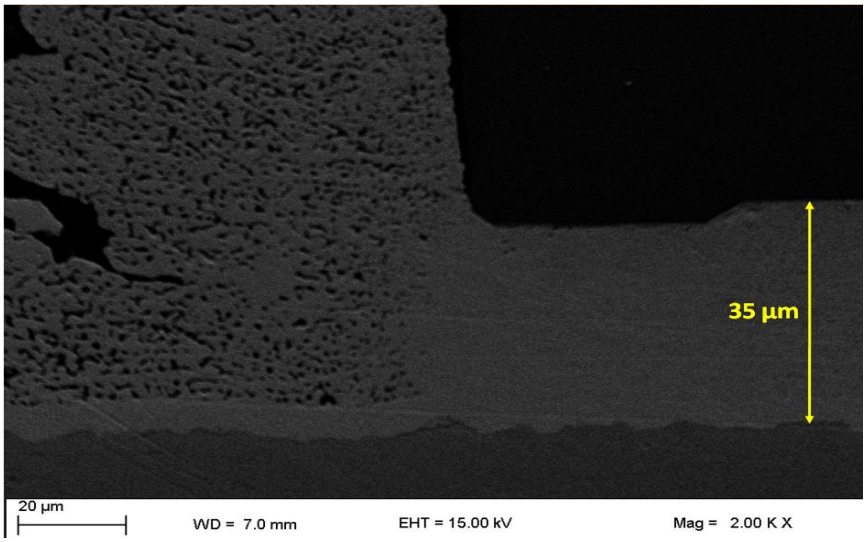
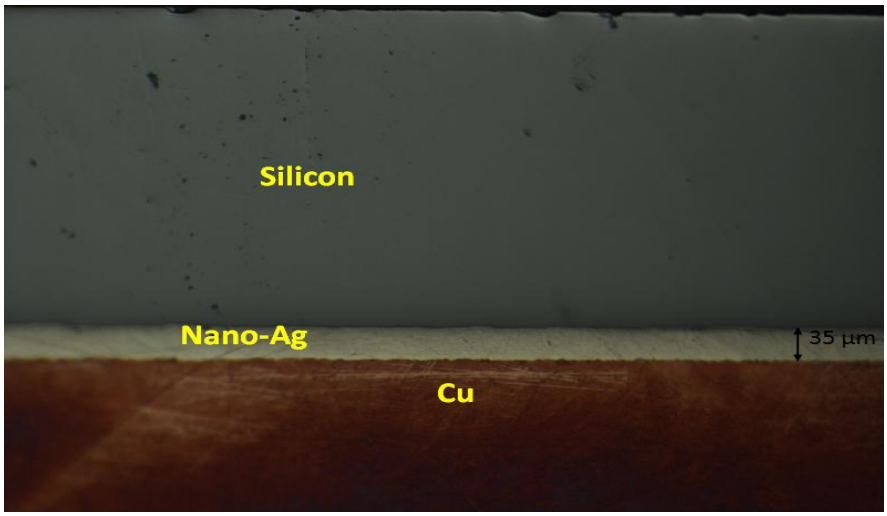


(c)

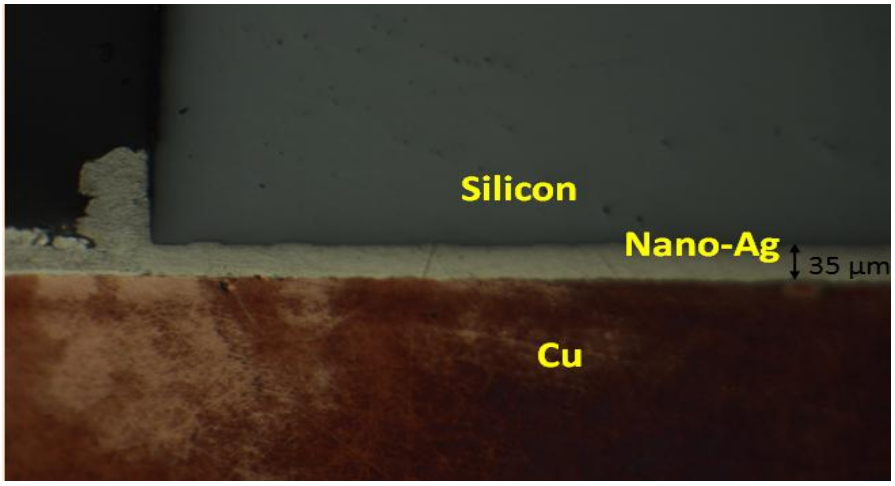
Figure 3.19. X-ray image of sintered silver joint in Si-sintered silver -Cu die-attachment after 800 temperature cycle.

Optical microscopy was used to show the bond-line at the length millimeter scale. As revealed in Figure 3.20, no cracks or voids were observed at both the edge and in the center of the joint after 800 of temperature cycles. An interest finding was shown in the SEM picture of Figure 3.19(c), the pore size of sintered silver around the silver joint was

at micrometers level, hundreds or even thousands times of the pore size inside the sintered silver below the silicon chip.



(a)



(b)

Figure 3.20. Optical microscopy image of sintered silver joint in Si-sintered silver -Cu die-attachment after 800 temperature cycle.

3.6. Discussion and Conclusion

As expected, the failure rate of the die-attachment of silicon attached to copper was much larger than that attached to DBC. No joint failure was observed in die-attachment with DBC substrate. This also proved that both soldering technique and the

pressure-sintering technique with double printing and drying were reliable to produce strong and reliable bonding.

For both solder materials attached to copper substrates, fatigue fracture observed started at the edge of the solder. Finite element simulations [51] confirmed this observation. Crack propagation longer than 25% length of chip was observed for both SAC305 and SN100C. This meant the solder joint after 800 temperature cycling reaching the failure threshold [52]. Also, the behavior of crack growth verified the previous failure mode that in joints of eutectic Sn-Ag alloy with copper alloy pads, failure occurred via interfacial separation at the solder-intermetallic interface because of the high strength of the solder. Two intermetallic compounds were known to form in Cu/Sn-Ag solder joint, Cu_6Sn_5 (η-phase) and Cu_3Sn (ε-phase) [53], which were of similar shape in SEM images. In the future, Energy dispersive spectroscopy (EDS) would be used for intermetllics identification to verify this. Also, rod-like dendrites were found in soldered DBC samples, which were consistent with the shape of Ag_3Sn (ε-phase) as Wenge Yang's work [54]. In contrast, no cracks or voids were observed in sintered silver joint for both DBC and copper die-attachment.

Generally speaking, sintered silver joint was more reliable than two kinds lead-free solder joint. Based on the observed phenomena, different modes of stress-relaxation were proposed here. For solder joints, phase transition or dislocation movement would help to release part of the residual stress; however, when stress was high enough, voids or cracks would form and stress would be further released by crack propagation. For sintered nano-silver, stress was also released during thermal cycling. However, since no cracks or big voids were found, crack growth theory could not be applied to this die-attach material. One propose was used here to explain the stress deduction: with low modulus, the porous structure of sintered silver would be easily deformed during thermal load, especially at edges. Very likely, this behavior was plastic deformation. It eventually decreased the extent of bending curvature and correspondingly decreased the residual stresses.

Chapter 4. SUMMARIES, ORIGINAL CONTRIBUTION AND FUTURE WORK

4.1. Summaries, Original Contribution

Die-attachment were prepared by soldering and silver sintering. The quality of both solder and silver joint was inspected by X-ray and optical microscopy. Both kinds of joint were demonstrated with little voids in the as-prepared samples.

In order to reduce the initial residual stresses in die-attachment of attaching aluminum to silicon, stress relief annealing was tried and the die-attachment without cracking the silicon was achieved.

Deduction of residual stresses was observed for both soldered and sintered die-attachment. Based on the observation from SEM images of solder and silver joint after 800 thermal cycles, different mode of stress-relaxation were proposed for sintered silver and solder, respectively. While solder joint released stress by crack growth, the silver joint relied on the deformation of porous structure, in which process the plastic deformation may occur.

The pressure-sintering process with double printing and drying was proved to be a reliable process to produce strong bonding for sintered silver. Its reliability was better than SAC305 and SN100C, two widely used solder preform. It was worthy of mentioning that the silicon rubber used in the pressure-sintering was necessary to evenly distribute the pressure.

The meaning of residual stresses would be emphasized here. Whether it was beneficial or harmful was always a controversy topic. Based on the observation in this study, the idea was proposed here: too much residual stresses was harmful because it may damage the chip or substrate. However, for a bi-layer or three layer attachment, the residual stresses indicated the bonding integrity. A high residual stresses may represent strong bonding strength.

More significantly, the bending, a more direct reflection of bonding integrity, should attract more attention. The technique of measuring the curvature by laser scanning, introduced in this work, was demonstrated as an effective tool for testing the quality of joint. Similar to X-ray technique, it was nondestructive way to observe the cross-section of bond-line. It was a cheaper and faster way to examine the die-attachment. Additionally, it overcame the lacks of X-ray: the ability to differentiate between layers. More discussion of it would be continued in the content of future work.

4.2. Recommendation for Future Work

4.2.1. High temperature cycling

As stated in the chapter 1, the main advantage of nanosilver paste over solder is its excellent performance at high operation temperature (junction temperature higher than 175^{o}C). Therefore, to continue the work in this thesis, die-attachment will be fabricated following the same or updated process. Then, the reliability will be tested by temperature cycle with higher peak temperature. One temperature profile is selected from the JEDEC standard: from -40^{o}C to 150^{o}C (or even higher).

4.2.2. Simulation

Although work has been reported about the simulation of die-attachment with solder joint, thermo-mechanical stress in the die-attachment with sintered-silver has not been studied. Simulation may be done on software like ANSYS. The simulation result can be compared with the observation in this work.

4.2.3. Multi-Chip Module

Due to the high performance and density of the integrated circuits packaged in multichip modules, the technique related to multi-chip module (MCM) become one of the major interest in electronic packaging technology.

Besides, the requirement of packaging to operate in harsh environments makes this technology immediately attractive for military motor drive applications (electric-hybrid vehicles, jet turbine units, electric actuators, etc.), industrial deep earth geological exploration (such as deep well seismic sources and on-site instrumentation), and commercial electric vehicles (in conjunction with advanced fuel cells and battery sources). These application drive the development of multichip power module. An idea has been proposed that the control and power circuitry components are integrated together into a single compact power module (Figure 4.1) [55].

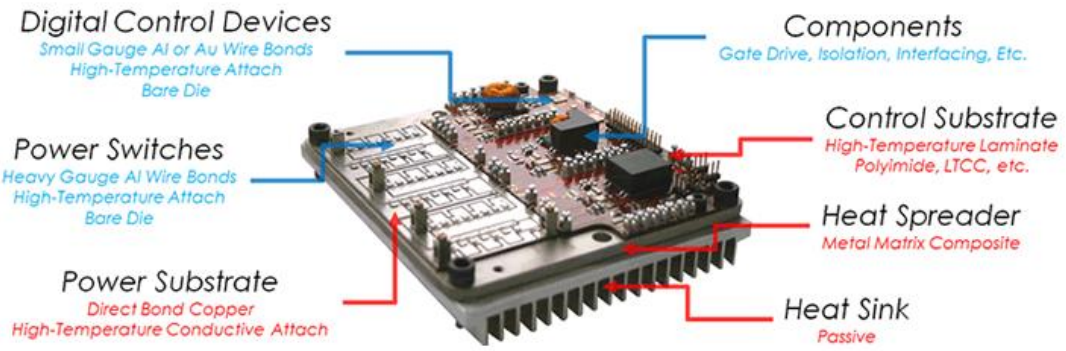
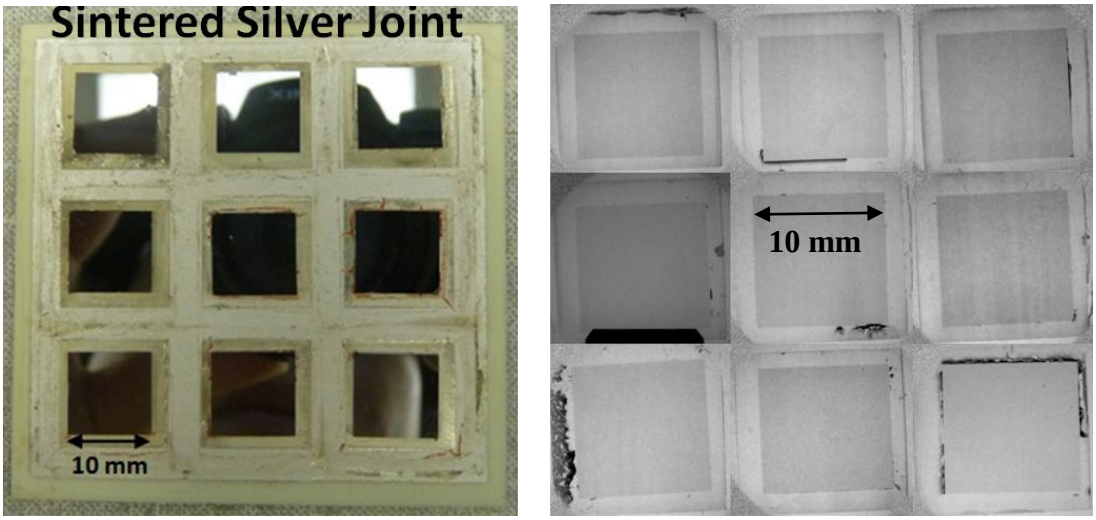


Figure 4.1. Multichip power module with the control and power circuitry components integrated into a single module

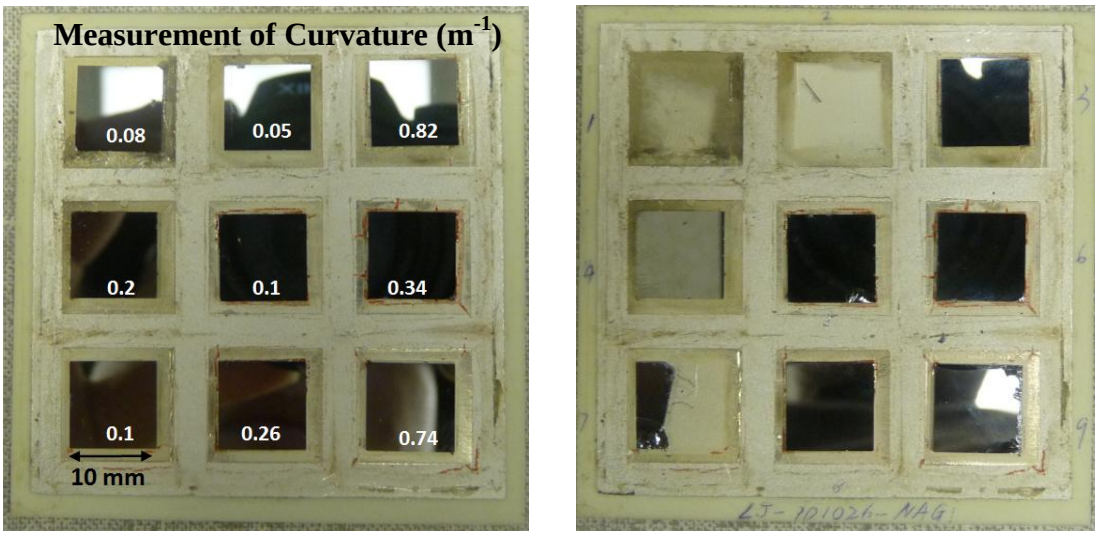
Consider the ability of sintered silver at high working temperature, it is worthy of investigating the technique of processing multichip module or power module by silver sintering.

A 9-chip module has been fabricated using the same silicon chip by pressure-sintering with double printing. DBC was used a substrate and rubber was used to evenly distribute the pressure. The fabricated module is shown in Figure 4.2 (a). Limited by the maximum size that can be examined by X-ray, the silver joint for attaching each silicon chip is inspected by X-ray technique one by one. The 9 X-ray images are collected and shown in Figure 4.2 (b).



(a) (b)

Figure 4.2. As-prepared 9 chip module and its X-ray images



(a) (b)

Figure 4.3. Curvature measurement of 9 chip module and the module after testing of bonding strength

However, the bonding quality of this modulus should not be strong for all 9 chips since the temperature are found not evenly distributed due to the size of heater. Figure 4.3 (a) shows the result of curvature measurement. It was found that just 2 of silicon has the curvature close to that in the work of this thesis. The silicon with low curvature would be

easily sheared off. In contrast, when shearing the silicon with a curvature about 0.74 m^{-1}, silicon itself cracks on the surface but still attached to the substrate as shown in Figure 4.3 (b). Either the process needs improvement or the sintering equipment.

4.2.4. Investigate the technique Curvature Measurement

An estimated evaluation of the bonding integrity in die-attachment can be easily and quickly obtained by curvature measurement technique. Moreover, unlike the X-ray, it is of the ability to differentiate between layers. However, currently, this technique is usually used for calculating the residual stresses. Looking back the work done in Chapter 3, The curvature itself was already able to reflect the bonding strength. Therefore, systematically study of applying this technique to the bonding test is also a valuable topic to study. An outline of experiment are described here: silicon die with polished surface with different sizes (3 × 3 mm^2, 5 × 5 mm^2 and 10 × 10 mm^2) are used as substrates. Samples will be fabricated by both soldering and silver sintering. It is promising to see that, combined curvature measurement with X-ray technique, an accurate evaluation of joint can be obtained.

REFERENCE

1 R. K. Ulrich, W. D. Brown, “Advanced Electronic Packaging”, Wiley Interscience, 2006

2 Rao R. Tummala, Eugene J. Rymaszewski and Alan G. Klopfenstein, Microelectronic Packaging Handbook, Part I., Technology Drivers, pp. I-65, Second Edition, International Thomson Publishing, 1996

3 IBM to Ship World's Fastest Microprocessor, http://www-03.ibm.com/press/us/en/pressrelease/32414.wss#release

4 A. Marshall, "Operating Power ICs at 200°C," in *23rd annual IEEE Power Electronics Specialists Conference*, Toledo, Spain, 1992, pp. 1033-1039.

5 S. C. Mathuna and M. Meinhardt, “PEI technologies, power electronic packaging”, PCIM, pp. 46-52, February 1999

6 J. W. Palmour, R. Singh, L. A. Lipkin and D. G. Waltz, "4H-SiC high temperature power devices," *Trans. HiTEC*, 1996, pp. XVI-9–XVI-14.

7 Asif Chowdhury, Bruce Guenin, Chan-Hee Woo1, Seung-Mo Kim, and Seri Lee, “The Effect of Die Attach Layer Delamination on the Thermal Performance of Plastic Packages”, *in Proc. of the IEEE Electronic Components & Technology Conference*, pp.1140-1147, May 1998.

8 Ning-Cheng Lee. “Reflow Soldering Processes and Troubleshooting: SMT, BGA, CSP and Flip Chip Technologies”, pp. 252, 2001

9 Derfiny, D. “Soldering Capability: PWB Design Viewpoint” *IPC Surface Mount Council White Paper: Soldering Capability* (1997)1-9.

10 Altera Corporation, “Reflow soldering guideline for surface mount devices,” http://www.altera.com/literature/an/an081.pdf.

11 Abtew, Mulugeta and Selvaduray, Guna. “Lead-free Solders in Microelectronics” *Materials Science and Engineering.* 27 (2000) 95-141.

12 Stam, F.A. and Davitt E. “Effects of thermomechanical cycling on lead and lead-free (SnPb and SnAgCu) surface mount solder joints” *Microelectronics Reliability*. 41 (2001) 1815-1822.

13 Arnold, J., McElroy, J., Gedney, R. “Roadmap of Lead-Free Assembly in North America” *JISSO/PROTEC Forum 2002, November 19-20, 2002; Japan*.

14 A. Kujala, T. Reinikainen, and W.Ren, “Transition to Pb-free Manufacturing Using Land Grid Array Packaging Technology,” *Proceedings of the Electronic Components and Technology Conference*, May 2000, pp. 359-364.

15 U. Scheuermann, "Low temperature joining technology - a high reliability alternative to solder contacts," in *Workshop on Metal Ceramic Composites for Functional Applicat*., Vienna, Austria, 1997.

16 H.L. Hvims, “Conductive adhesives for SMT and potential applications,” *IEEE-Compon. Hybrids Manufacturing Technol.*, vol. 18, pp. 284-291, 1995.

17 R.S. Rorgren and J. Liu, “Reliability assessment of isotropically conductive adhesive joints in surface mount applications,” *IEEE-Components Hybrids Manufacturing Technology*, vol. 18, pp. 305-312, 1995.

18 Lead-free solders vs. conductive adhesives http://www.electroiq.com/index/display/article-display/82206/articles/advanced-packaging/volume-9/issue-9/features/lead-free-solders-vs-conductive-adhesives.html

19 Soesatyo, B., Blicblau, A., Siores, E. “Effect of rapid curing doped epoxy adhesive between two polycarbonate substrates on the bond tensile strenth” *Journal of Materials Processing Technology*. 89-90 (1999) 451-456.

20 C. Göbl, P. Beckedahl, and H. Braml, "Low temperature sinter technology die attachment for automotive power electronic applications," in *Proc. Automotive Power Electron.*, Paris, France, 2006, pp. 1-5.

21 R. Amro, J. Lutz, J. Rudzki, R. Sittig, and M. Thoben, "Power cycling at high temperature swings of modules with low temperature joining technique," in *Proc. 18th Int. Symp. Power Semi. Devices & IC's*, Naples, Italy, 2006, pp. 217 – 220.

22 C. Göbl, P. Beckedahl, and H. Braml, "Low temperature sinter technology die attachment for automotive power electronic applications," in *Proc. Automotive Power Electron.*, Paris, France, 2006, pp. 1-5.

23 U. Scheuermann, and P. Beckedahl, "The road to the next generation power module – 100% solder free design," in *Proc. 5th Int. Conf. Integrated Power Electron. Syst(CIPS 2008)*, Nuremberg, Germany, 2008, p. 4.2.

24 Z. Z. Zhang, and G-Q. Lu, "Pressure-assisted low-temperature sintering of silver paste as an alternative die-attach solution to solder reflow," *IEEE Trans. Electron. Packag.* Manuf., vol. 25, no. 4, pp. 279-283, Oct. 2002.

25 J. G. Bai, Z. Z. Zhang, J. N. Calata, and G-Q. Lu, "Low-temperature sintered nanoscale silver as a novel semiconductor device-metallized substrate interconnect material," *IEEE Trans. Compon. Packag. Technol.*, vol. 29, no. 3, pp. 589-593, Sep. 2006.

26 J. G. Bai, Z. Z. Zhang, G-Q. Lu, J. Yin, J. D. van Wyk, L. Zhu, and T. P. Chow, "Low-temperature sintered silver attachment for high-temperature operation of SiC power devices," in Proc. 4th Int. Conf. Integrated Power Electron. Syst. (CIPS 2006), Naples, Italy, 2006, pp. 53-57.

27 Z. Z. Zhang, J. N. Calata, J. G. Bai, and G-Q. Lu, "Nanoscale silver sintering for high-temperature packaging of semiconductor devices," in 2004 TMS Annu. Meeting & Exhibition, Charlotte, NC., pp. 129-135.

28 J. G. Bai, J. N. Calata, G. Lei, Z. Zhang and G-Q. Lu, "Thermomechanical reliability of sintered silver die-attachment," in Proc. 10th Intersociety Conf. Thermal and Thermomechanical Phenomena in Electron. Syst. (ITHERM), San Diego, CA., 2006, pp. 1126-1130.

29 J. G. Bai, and G-Q Lu, “Thermomechanical reliability of low-temperature sintered silver die attached SiC power device assembly, ” IEEE Trans. Device and Mater. Rel., vol. 6, no. 3, pp. 436-443. Sep. 2006.

30 J. G. Bai, T. G. Lei, J. N. Calata, and G-Q. Lu, "Control of nanosilver sintering attained through organic binder burnout," *J. Mater. Res.*, vol. 22, no. 12, pp. 3494-3500, Dec. 2007.

31 J. G. Bai, "Low-temperature sintering of nanoscale silver paste for semiconductor device interconnection," Ph.D. dissertation, Dept. Mater. Sci. and Eng., Virginia Poly. Inst. and State Univ., Blacksburg, VA, 2005.

32 Tao Wang, Xu Chen, Guo-Quan Lu, Guangyin Lei, “Low-Temperature Sintering with Nano-Silver Paste in Die-Attached Interconnection”, J. Electronic Materials, Vol. 36, No. 10, pp. 1333-1340. 2007.

33 J. Schulz-Harder, “Advantages and new development of direct bonded copper substrates”, Microelectronics Reliability, vol. 43, pp. 359-365, 2003.

34 J. Schulz-Harder, K. Exel, “Recent developments of direct bonded copper (DBC) substrates for power modules”, ICEPT 2003.

35 Temperature Cycle Test (TCT) http://www.siliconfareast.com/TCT.htm

36 High Reliability Lead-free Solder SN100C （ Sn-0.7Cu-0.05Ni ＋ Ge ） http://www.smtnet.com/library/files/upload/paper_HighReliabilityLead-freeSolderSN100C_071023.pdf

37 Guangyin (Thomas) Lei, " Thermo-Mechanical Reliability of Low-Temperature Sintered Attachments on Direct Bonded Aluminum (DBA) Substrate for High-Temperature Electronics Packaging," Ph.D. dissertation, Dept. Mater. Sci. and Eng., Virginia Poly. Inst. and State Univ., Blacksburg, VA, 2010.

38 P. Volk, Zincate treatment of aluminium, 2004.

39 Frear D.R., Hosking F.M., Keicher D.M. and Peebles H.C., 1995, "Fluxless Soldering for Microelectronic Applications" Material for electronic packaging, Edit by Chung Deborah D.L, Butterworth Heinemann.

40 Thomas G. Lei, Jesus N. Calata, Shufang Luo, Xu Chen, and Guo-Quan Lu, "Low-Temperature Sintering of Nanoscale Silver Paste for Attaching Large-Area (> 100 mm2) Chips", IEEE Transactions on Components and Packaging Technologies, Vol. 33, No. 1, pp. 98-104, 2010.

41 Mohammad Yunus, K. Srihari, J. M. Pitarresi and Anthony Primavera, "Effect of voids on the reliability of BGA/CSP solder joints", Microelectronics Reliability Volume 43, Issue 12, December 2003, Pages 2077-2086.

42 Thermal cycling, JEDEC standard http://www.jedec.org/standards-documents/docs/jesd-22-a104d

43 Kang Ping Wang, Yonggang Young Huang, Abihijit Chandra, and Kai Xiong Hu; "Interfacial shear stress, peeling stress, and die cracking stress in trilayer electronic assemblies"; IEEE transactions on components and packaging technologies; vol. 23; June 2000.

44 S.H.Brongersma, E.Richard, I.Vervoort, and K.Maex, "Stress in Electrochemically Deposited Copper", Stress Induced Phenomena in Metallization Fifth international Workshop, Stuttgart, Germany, pp249-256, June1999.

45 R.Mitra, A.Madan, R.A.Hoffman, W.A.Chiou, J.R.Weertman; Effect of annealing on microstructure and properties of Al-Ti Multilayered films; Materials research society symposium proceedings volume 594; Thin films-stresses abd mechnical properties VIII; Symposium held November 29-December 3, 1999, Boston, Massachusetts, U.S.A; Editors Richard Vinci, Oliver Kraft, Neville Moody, Paul Besser, Edward Shaffer II; pp43-48.

46 Lu J 1996 *Handbook of Measurement of Residual Stresses* (Lilburn, GA: Fairmount Press).

47 J. G. Bai, “Low-temperature sintering of nanoscale silver paste for semiconductor device interconnection,” Ph.D Dissertation, pp.59, Virginia Polytechnic Institute and State University, Blacksburg, VA 2005.

48 C. H. Hsueh, "Modeling of elastic deformation of multilayers due to residual stresses and external bending," *Journal of Applied Physics*, vol. 91, pp. 9652-9656, Jun 2002.

49 X. Chen, R. Li, K. Qi, and G. Q. Lu, "Tensile behaviors and ratcheting effects of partially sintered chip-attachment films of a nanoscale silver paste," *Journal of Electronic Materials*, vol. 37, pp. 1574-1579, Oct 2008.

50 F. Q. Lang, Y. Hayashi, H. Nakagawa, M. Aoyagi, andH. Ohashi, "Joint Reliability of Double-Side Packaged SiC Power Devices to a DBC Substrate with High Temperature Solders," in Eptc: *2008 10th Electronics Packaging Technology Conference*, Vols 1-3 New York: IEEE, 2008, pp. 897-902.

51 R. K. Shiue, P. C. Chang, W. D. Zhuang, and S. Spie, "Stress and strain simulation of power MOSFET solder attachment on different substrates," in *2000 International Symposium on Microelectronics*. vol. 4339, 2000, pp. 105-111.

52 B. Vandevelde, "Thermo-mechanical modeling of solder joint reliability for electronic package systems," Ph.D. thesis, Catholic Univ. of Leuven, Belgium, Mar. 2002.

53 W. W. Lee, L. T. Nguyen and G. S. Selvaduray, "Solder joint fatigue models: review and applicability to chip scale packages" *Microelectronics Reliability*, pp.231-244, 2000.

54 Wenge Yang and Robert w. Messler, Jr, "Microstructure evolution of eutectic Sn-Ag solder joint"*Journal of Electronic Materials*, Vol.23, pp.765-771, No.8, 2004.

55 J. Hornberger, S. Mounce, R. Schupbach, H. A. Mantooth and A. B. Lostetter, "High-Temperature Silicon Carbide (SiC) Power Switches in Multichip Power Module (MCPM) Applications," IEEE Industry Applications Society Meeting, 6 pgs., Hong Kong, Oct. 2005.