

**HARMONIC REDUCTION IN A SINGLE-SWITCH THREE-PHASE
BOOST RECTIFIER WITH HARMONIC-INJECTED PWM**

by

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ABSTRACT

A constant switching frequency with the sixth-order harmonic injection PWM concept is established, and a sixth-order harmonic injection technique is developed for the harmonic reduction of a single-switch three-phase boost rectifier. The approach employs a constant duty cycle with sixth-order harmonic injection to suppress the dominant (fifth-order) harmonic in the input currents. Hence, to meet the THD<10% requirement, the rectifier voltage gain can be designed down to 1.45; to meet the IEC 1000-3-2 (A) standard, the output power can be pushed up to 10 kW for the application with a 3X220 V input and a 800 V output. The results are verified on a 6-kW prototype.

The injection principle is graphically explained in current waveforms and mathematically proved. Two injection methods are proposed to meet either the THD requirement or the IEC standard. The injection implementation and design guidelines are provided.

The boost inductor design and EMI filter design are discussed. An average small-signal model based on the equivalent multi-module model is developed and experimentally verified. The variations of the small-signal model against load are demonstrated, and the compensator design is discussed. The results show that at no load, the dominant pole of the control-to-output transfer function approaches the origin and causes more phase delay, making the control design difficult. To avoid the no load case and to simplify the control design, a 50-W dummy load (1% of the full load) is added. Finally, a simple nonlinear gain control circuit is presented to mitigate the load effect and reduce the dummy load to 10 W.

To My Country
The People's Republic of China

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1. Introduction

Traditionally, three-phase AC-to-DC conversions are performed by phase-controlled or diode rectifiers. Since these rectifiers draw non-sinusoidal currents or reactive power from the source, the power quality of the distribution network is greatly deteriorated, resulting in low efficiency of utilities.

Recently, more and more stringent limits on the level of harmonics promote the growth of power factor correction techniques in front-end power converters. Switching-mode rectifiers have gained great attention as a good solution, since they draw perfect sinusoidal currents from the power distribution network. Among three-phase AC-to-DC PWM rectifiers, boost-type topologies are frequently used because of continuous input currents and high output voltages. Basically, two topologies are most popular: a six-switch full-bridge boost rectifier and a single-switch boost rectifier. The first one uses six switches to achieve sinusoidal input current control and to share the output power. So its features include continuous input current, excellent power factor, and low switch current rating [1]. However, this circuit is very complicated in power stage and control, so it is too expensive for medium power level (5 kW-10 kW) applications. The second one uses six diodes and only one switch to control the input current and output power (Fig. 1.1) [2-8]. It is very simple in power stage and control circuit; hence, it is inexpensive. For medium power level applications, such as telecommunication and battery charge, this topology is a very attractive solution.

The power factor correction in a single-switch rectifier is performed by shaping input phase currents into discontinuous waveforms. The average values of these waveforms in one switching cycle are proportional to the instantaneous values of their corresponding phase voltages. As a result, the input phase currents are forced to track the input voltages, and an almost unity power factor is obtained.

However, the single-switch three-phase boost rectifier cannot be pushed to high power levels because its input current harmonics cannot meet the IEC 1000-3-2 (A) standard. Based on harmonic analysis, it is found that the current distortions are related to the rectifier voltage gain M , which is defined as:

$$M = \frac{V_o}{V_{lp}}, \quad (1.1)$$

where V_o is rectifier output voltage and V_{lp} is input line-line peak voltage. The higher the M is, the lower the harmonics become. A larger M means a high output voltage, yielding a high voltage stress on the devices.

To date, several efforts, concentrating on PWM control schemes, have been made to improve the input current distortions [3, 4]. The first example concerns a variable switching frequency PWM. With this PWM, the switch in the rectifier works in such a way that when the rectifier dc-side current falls to zero, the switch is turned on again immediately. Therefore, the input current harmonics are improved. The reason will be

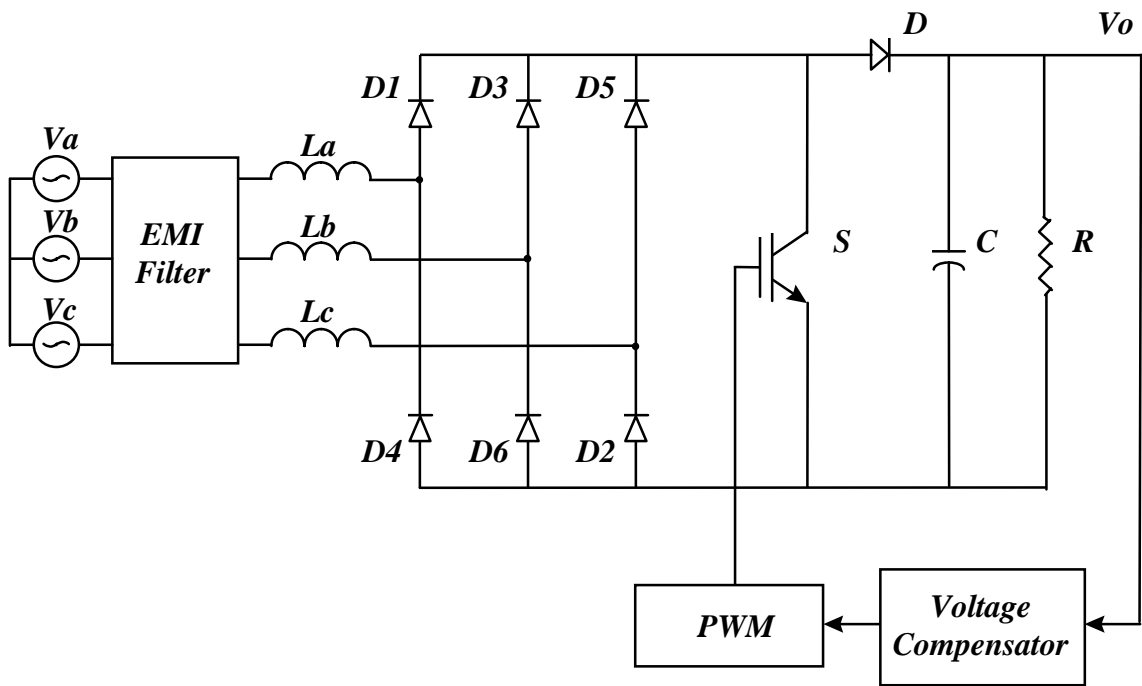


Fig. 1.1. A single-switch three-phase boost rectifier.

explained in Chapter 2. However, this control scheme suffers from a serious defect; namely, the switching frequency is load-dependent. At lighter load, the increase of switching frequency results in high switching losses, and the wide switching frequency range complicates boost inductor design, device selection, and EMI filter design.

The second example [4] concerns an output low-frequency ripple (sixth-order) feedback control PWM. For a rectifier with a resistive load and fed by a balanced three-phase AC power, the sixth-order output voltage ripple is created by a power ripple, which is represented as current harmonics in the inputs. The higher the ripple, the larger the input current harmonics. Hence, the improvement of current harmonics can be achieved by reducing the sixth-order ripple at the output. This concept is realized by a feedback control loop whose bandwidth is wide enough to pass the sixth-order ripple. Unfortunately, it is difficult to achieve a significant improvement of harmonics. This is because the real load of the rectifier is capacitive, which will cause a phase delay at the sixth-order frequency. Also, this delay is frequently load-dependent. In addition, a wide control bandwidth easily makes the control loop unstable at a light load.

In this thesis, a sixth-order harmonic-injected PWM concept is established first [8]. Based on harmonic analysis, it is found that the dominant harmonic in the single-switch three-phase boost rectifier with constant switching frequency PWM is the fifth-order harmonic. This harmonic can be reduced by modulating the duty cycle with a sixth-order harmonic. Even though a seventh-order harmonic is created at the same time, the total harmonic distortion is improved. By properly injecting the sixth-order harmonic, the input current harmonics can be optimized to meet either the IEC 1000-3-2 (A) standard or the THD requirement, while pushing the output power to a higher level.

Secondly, a harmonic injection technique is developed. Based on the voltage compensator designed for constant switching frequency PWM, a synchronized harmonic generator is used to provide a sixth-order sinusoidal signal. A multiplier is used to modify the signal with modulation index. An adder is used to inject the signal into the voltage feedback loop. Since the sixth-order harmonic is obtained from sensing three-phase input voltages, which are purely sinusoidal, the injection concept is ideally implemented.

Thirdly, the design of a single-switch three-phase boost rectifier is considered. Based on the steady-state analysis, the boost inductor design and the EMI filter design are addressed. An average small-signal model is developed and experimentally verified, and the variation of the model against load is investigated. Then, the small-signal model is used to design the voltage compensator for the single-switch three-phase boost rectifier. Generally, a front-end converter is required to operate from heavy load to light load, or even to no load. In such a wide load range, a linear controller is unsuitable due to the nonlinear nature of the power stage. To ensure the system performance, a nonlinear controller is necessary. However, most of nonlinear controllers are very complex and need to be implemented by a digital method [18-20], which increases the cost. In Chapter 4, a simple and inexpensive nonlinear gain controller is presented to mitigate the load effect in a single-switch three-phase boost rectifier.

2. Harmonics with Constant and Variable Switching Frequency PWMs

To qualify the performance of a switching mode rectifier with power factor correction, the quantity of input current harmonics is an important parameter. Clearly understanding the distorted mechanism will help us to find a proper way to suppress the harmonics. In this chapter, the harmonics in a single-switch three-phase boost rectifier with both constant and variable switching frequency PWMs are analyzed. It is found that the harmonics are greatly dependent on the rectifier voltage gain M . The higher the M , the lower the distortions. Among all orders of low-frequency harmonics, the fifth order is a dominant order for the rectifier with a constant switching frequency PWM. Therefore, in order to meet the IEC 1000-3-2 (A) standard, the power levels cannot be pushed above 5 kW (for 3×220 -Vrms input) because the fifth-order harmonic exceeds the limit. A simple way to reduce the fifth-order harmonic and to improve the total harmonic distortions is with a variable switching frequency PWM. However, in a such PWM, the switching frequency is relative to the load: the lighter the load, the higher the switching frequency. At light load, a significant increase of switching frequency will complicate the power stage design, resulting in a high cost.

2.1. Harmonics with Constant Switching Frequency PWM

The power stage and control block with a constant switching frequency PWM have been shown in Fig. 1.1. Under balanced and undistorted three-phase input voltages:

$$\begin{aligned} V_a &= V_m \sin(\omega t), \\ V_b &= V_m \sin(\omega t - \frac{2\pi}{3}), \\ V_c &= V_m \sin(\omega t - \frac{4\pi}{3}), \end{aligned} \quad (2.1)$$

three-phase input currents can be calculated. Over $(0, \pi/2)$ interval, the phase A input current (average) is given by [6]:

$$\begin{aligned} 0 \leq \omega t \leq \frac{\pi}{6} & \quad i_a = \frac{V_o T_{on}^2}{2 L T_{sw}} \frac{\sin(\omega t)}{\sqrt{3} M - 3 \sin(\omega t)}, \\ \frac{\pi}{6} \leq \omega t \leq \frac{\pi}{3} & \quad i_a = \frac{V_o T_{on}^2}{2 L T_{sw}} \frac{M \sin(\omega t) + \frac{1}{2} \sin(2\omega t - \frac{2\pi}{3})}{[\sqrt{3} M - 3 \sin(\omega t + \frac{2\pi}{3})][M - \sin(\omega t + \frac{\pi}{6})]}, \\ \frac{\pi}{3} \leq \omega t \leq \frac{\pi}{2} & \quad i_a = \frac{V_o T_{on}^2}{2 L T_{sw}} \frac{M \sin(\omega t) + \sin(2\omega t + \frac{\pi}{3})}{[\sqrt{3} M + 3 \sin(\omega t + \frac{2\pi}{3})][M - \sin(\omega t + \frac{\pi}{6})]}, \end{aligned} \quad (2.2)$$

where V_o is the output voltage, $T_{on} = dT_{sw}$, d is the duty cycle, T_{sw} is the switching period ($T_{sw} = 1/f$, f is the switching frequency), L is the input inductor, and M is the rectifier voltage gain. The phase A current i_a over $(\pi/2, 2\pi)$, and phase B and C currents i_b and i_c over $(0, 2\pi)$ can be obtained according to symmetrical properties of the waveforms. In Fig. 2.1, the phase A current with $M=1.5$ and 2 is plotted for a 6 kW rectifier with 3×220 -Vrms input ($L = 43 \mu H$, $f_s = 45 \text{ kHz}$). From both current equations and plot, it can be observed that the current shape is completely determined by the rectifier voltage gain M : the higher the M , the lower the distortions. On the other hand, the current shape is load-independent, because at a fixed load, the duty cycle D is constant over line cycles.

Generally, current distortions are quantified by the total harmonic distortions (THD) parameter, which is defined as

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} i_n^2}}{i_1}. \quad (2.3)$$

For the input currents in Eq. (2.2), the THDs are calculated and plotted with respect to M , as shown in Fig. 2.2. It is clear that the higher the M , the lower the THDs. The plot also shows that, in order to meet the THD<10% specification, M should be designed greater than 1.68, which limits the applications of the rectifier. For example, with a 3×220 -Vrms input, the output voltage should be boosted beyond 900 V in order to meet the THD<10% requirement.

Practically, the current distortions are governed by harmonic standards. Recently, IEC 1000-3-2 has become the most popular one, as shown in Fig. 2.3, where each order harmonic has a maximum limit. Hence, the worth of the single-switch three-phase boost rectifier can be evaluated by comparing its harmonic contents to the IEC limits.

According to Eq (2.2), the harmonic contents at different power levels for a rectifier with 3×220 -Vrms input and 800-V output are plotted as shown in Fig. 2.3. Two conclusions can be drawn from this plot. First, the input current is actually distorted by a dominant harmonic, the fifth-order harmonic. Secondly, in order to meet the IEC 1000-3-2 (A) standard, the power levels of the rectifier cannot be pushed above 5 kW.

The reasons of input current distortions in a single-switch three-phase boost rectifier can be further investigated from the details of current waveforms as shown in Fig. 2.4. During one switching cycle, when the switch is turned on, three phase voltages charge three input inductors, and input currents are built up. Both peak and average of these currents are proportional to input voltages. When the switch is turned off, the inductors discharge to output. Unfortunately, the discharge areas are not proportional to input voltages. So the average currents are not proportional to input voltages and there exist several low-order harmonics. It is obvious that the higher the output voltage, the smaller the discharge areas, and the less the current distortions. That is why the distortions are greatly dependent on the rectifier voltage gain M .

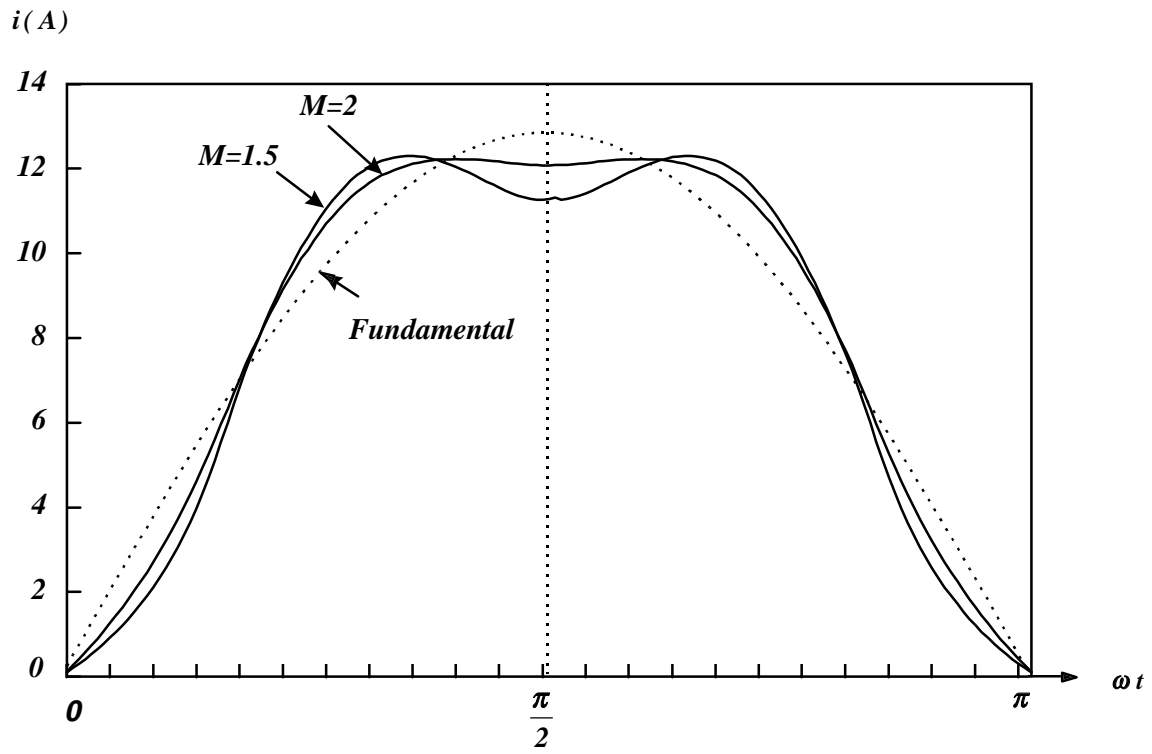


Fig. 2.1. Average input current at $M=1.5$ and $M=2$ for a 6-kW rectifier with $3X220$ -Vrms input

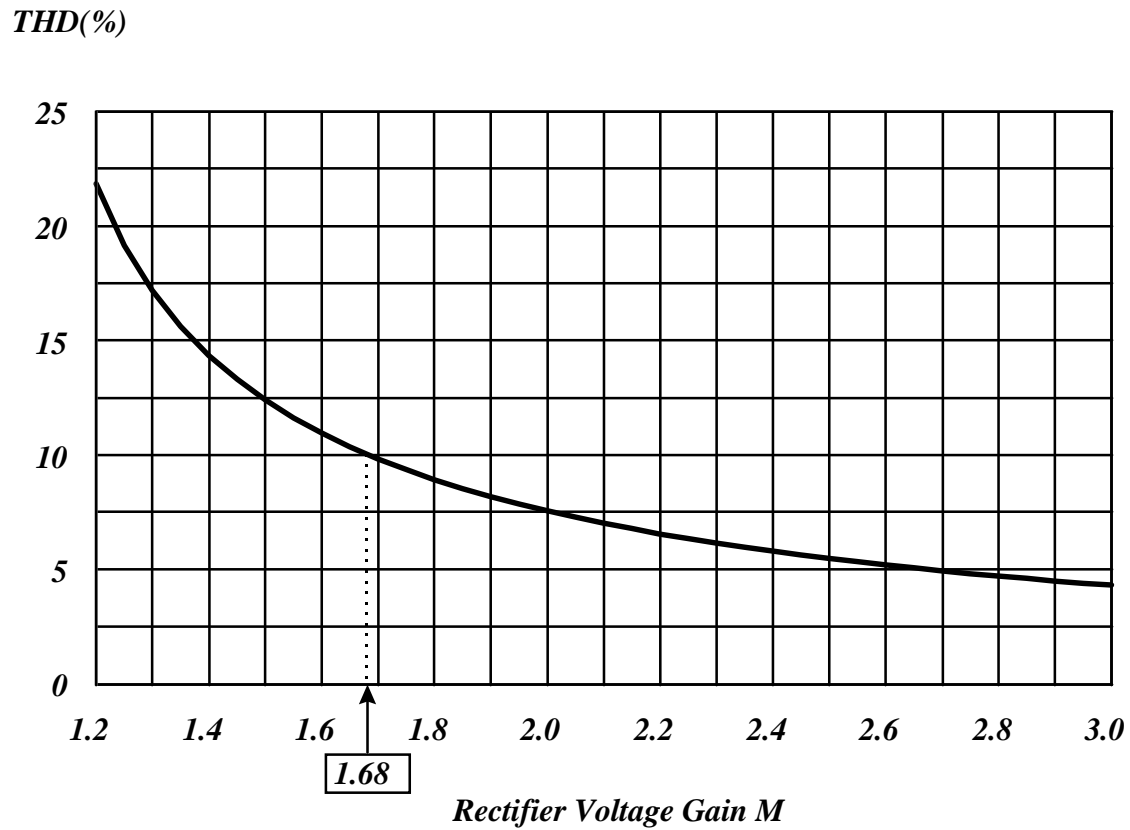
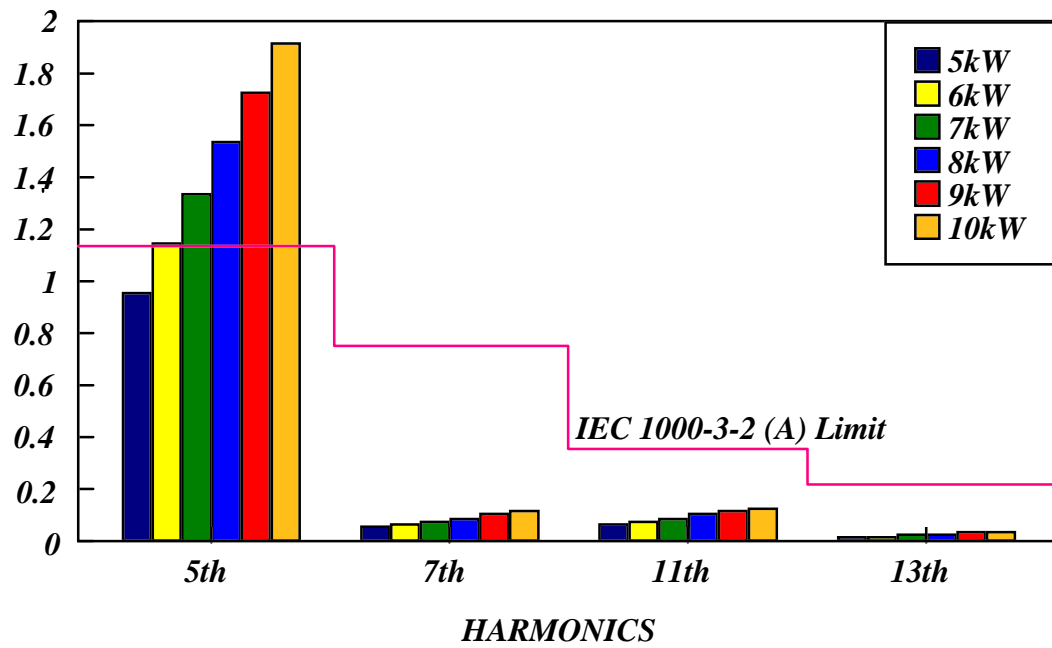


Fig. 2.2. THD as a function of M with constant switching frequency PWM

CURRENT [rms, A]



*Fig. 2.3. Harmonic contents with a constant switching frequency PWM
@3X220-Vrms input/800-V output*

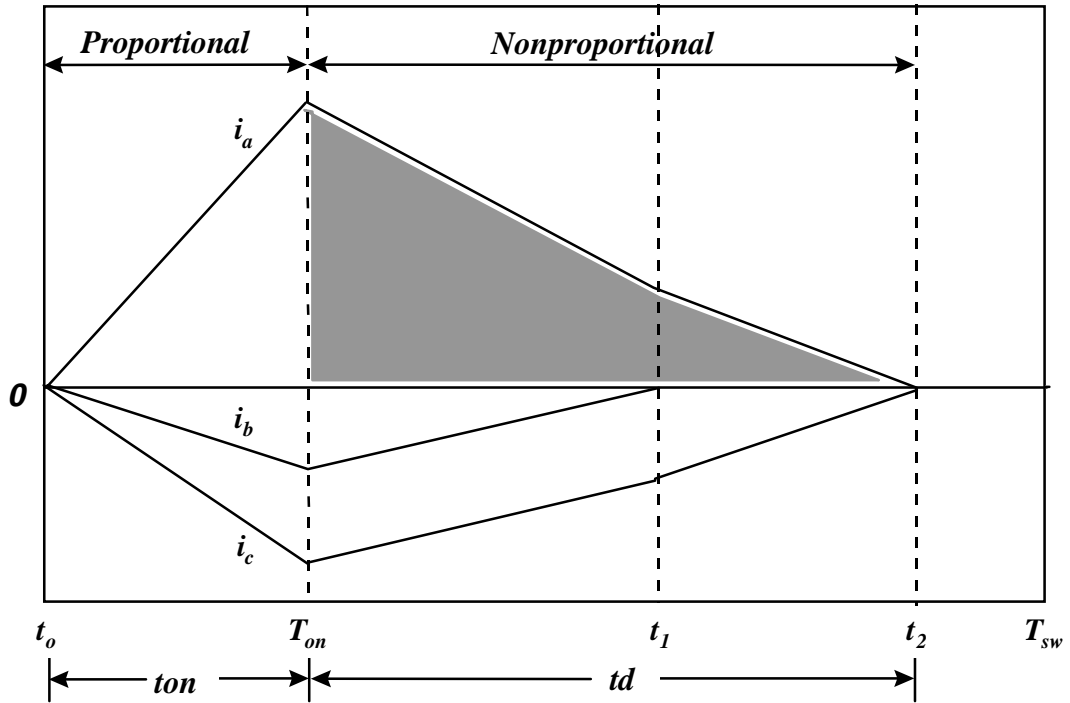


Fig. 2.4. The details of input inductor currents over one switching cycle

2.2 Harmonics with Variable Switching Frequency PWM

A simple way to improve the input current distortions in a single-switch three-phase boost rectifier is with a variable switching frequency PWM scheme [4]. The power stage and control block with this scheme are shown in Fig. 2.5. In the power stage, a current sensor is added on the rectifier dc-side to sense the output current of the diode rectifier. When the sensed current falls to zero, the switch is controlled to turn on again immediately. With this control scheme, the switching frequency is variable over one line cycle. On the other hand, the switch turn-off is controlled by the output or the duty cycle is regulated by load, which is similar to the rectifier with a constant switching frequency PWM.

Under balanced and undistorted three-phase input voltages in Eq. (2.1), three-phase input currents can be calculated. Over $(0, \pi/2)$ interval, the phase A input current (average) is given by [3]:

$$\begin{aligned}
 0 \leq \omega t \leq \frac{\pi}{6} \quad i_a &= \frac{V_o T_{on}}{2L} \frac{\sin(\omega t) - \frac{1}{2M} \sin(2\omega t)}{\sqrt{3}M - 3 \sin(\omega t)}, \\
 \frac{\pi}{6} \leq \omega t \leq \frac{\pi}{3} \quad i_a &= \frac{V_o T_{on}}{2L} \frac{\sin(\omega t) + \frac{1}{2M} \sin(2\omega t - \frac{2\pi}{3})}{\sqrt{3}M - 3 \sin(\omega t - \frac{4\pi}{3})}, \\
 \frac{\pi}{3} \leq \omega t \leq \frac{\pi}{2} \quad i_a &= \frac{V_o T_{on}}{2L} \frac{\sin(\omega t) + \frac{1}{M} \sin(2\omega t + \frac{\pi}{3})}{\sqrt{3}M + 3 \sin(\omega t - \frac{4\pi}{3})}.
 \end{aligned} \tag{2.4}$$

From the above equations, the THD is plotted in Fig. 2.6. Compared to the rectifier with a constant switching frequency PWM, it is obvious that the current distortions are improved. To meet the THD < 10% specification, the M can be designed down to 1.48. For a rectifier with a 3×220 -Vrms input, the output can be designed as low as 780 V.

With a variable switching frequency PWM, the switching frequency repeats each 60° over one line cycle. Between $-30^\circ \leq \omega t \leq 30^\circ$, it is given by:

$$f_s = \frac{1 - \frac{1}{M} \cos(\omega t)}{D} f_o, \tag{2.5}$$

where f_o is an equivalent switching frequency and is a constant, D is duty cycle, which is load-dependent.

As sketched in Fig. 2.7, the switching frequency in Eq. (2.5) is relative to both time instant and load. At a fixed load, D is a constant, and the switching frequency is slightly varied with ωt . At $\omega t = -30^\circ$, it reaches the maximum, and at $\omega t = 30^\circ$, it reaches the minimum. On the other hand, the switching frequency greatly depends on load. When the load changes from 100% to 50%, the switching frequency at $\omega t = 30^\circ$ changes from 50 kHz to 240 kHz. This will complicate inductor design, device selection, and EMI filter design.

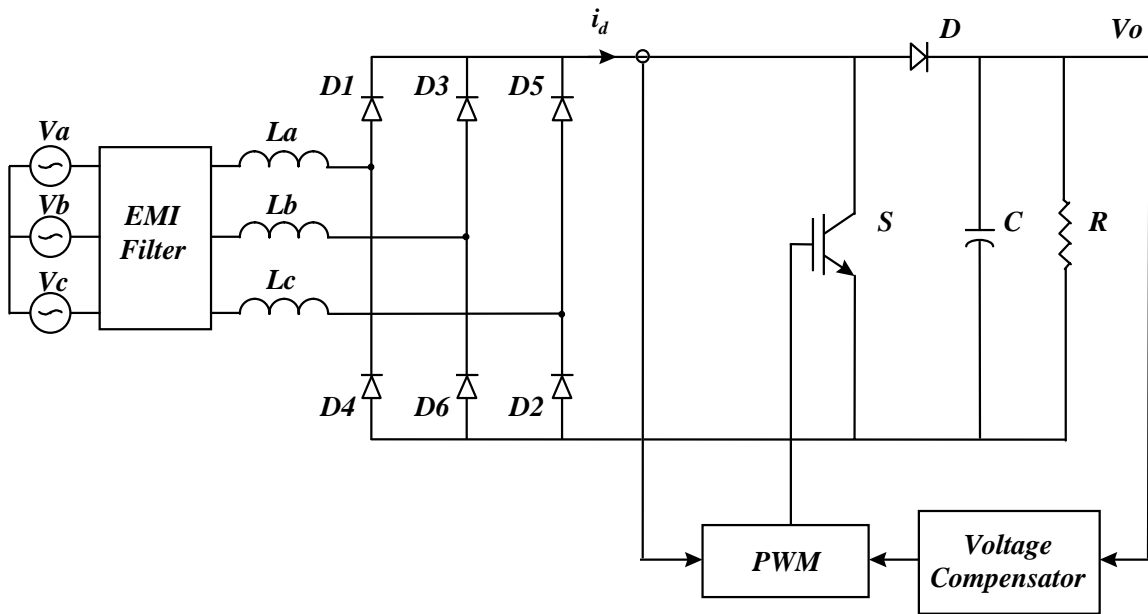


Fig. 2.5. A single-switch rectifier with variable switching frequency PWM

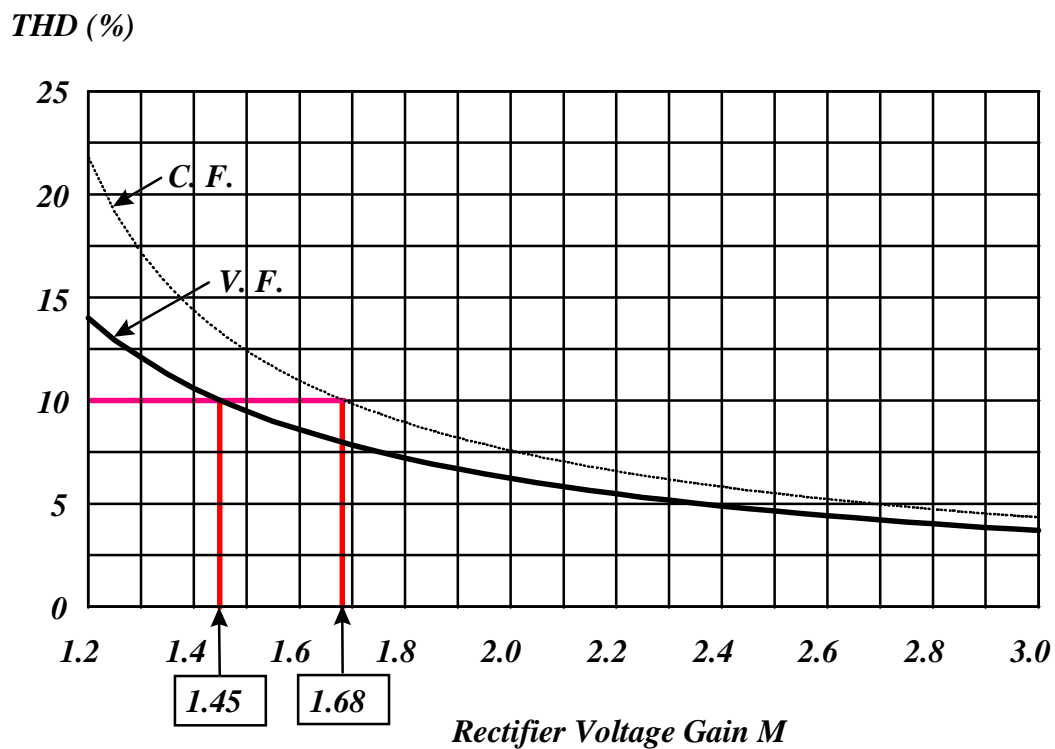


Fig. 2.6. THD as a function of M with variable switching frequency PWM

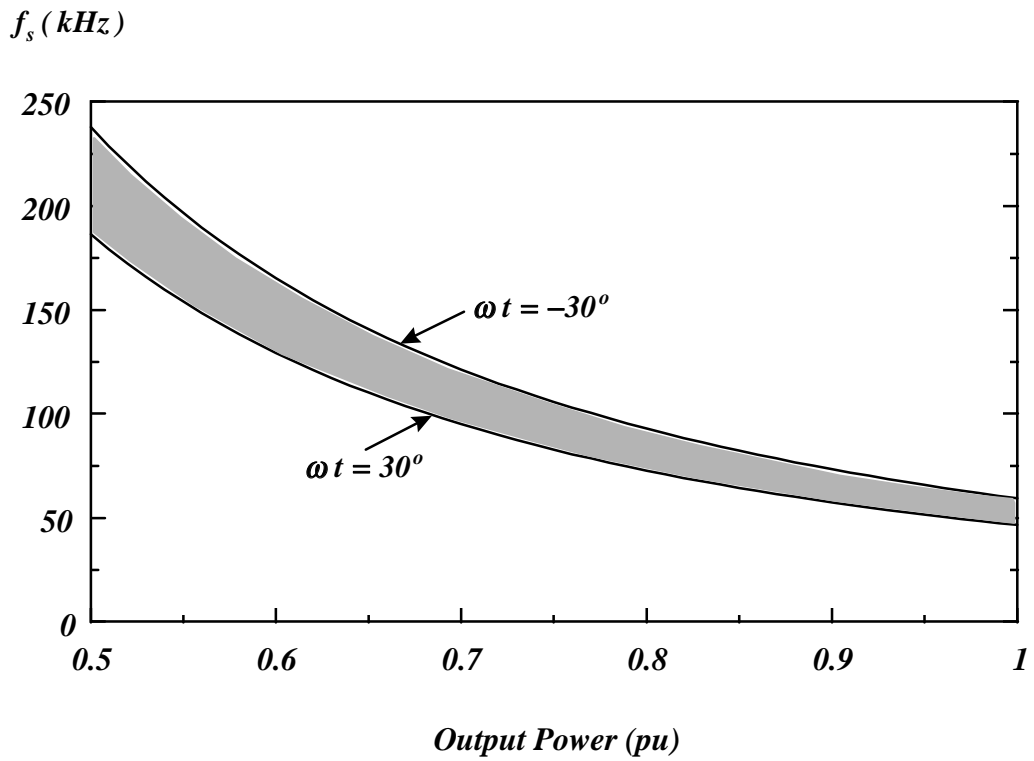


Fig. 2.7. Switching frequency variations against load over one line cycle

3. Harmonic Reduction with Harmonic-Injected PWM

In order to simplify the power stage design and reduce the cost, a constant switching frequency PWM is preferred. As discussed in Chapter 2, with this technique, a high fifth-order harmonic is resulted in. Intuitively, it sounds possible to reduce the fifth-order harmonic and improve the THD by modulating the duty cycle with some harmonics.

In this chapter, a sixth-order harmonic injected PWM concept is established based on the intuition of the duty cycle modulation. Then a harmonic injection technique is developed to implement the concept. Finally, both simulation and experimental results are provided to demonstrate the validity of the method.

3.1 Harmonic-Injected PWM Concept

The harmonic-injected PWM concept is established based on the current waveform analysis. Through examining the current equations for a rectifier with a constant switching frequency PWM in Eq. (2.2), it can be found that the current magnitudes are linearly proportional to the square of duty cycle. Properly modulating the duty cycle can directly change the current shapes or distortions. For simplicity, this principle is graphically explained for one-phase current first. In Fig. 3.1, phase A current i_a over $(0, \pi)$ is plotted along with its fundamental i_{af} . In order to reduce the current distortion, the duty cycle modulation is processed in such a way that during $(0, a)$ the duty cycle is increased to make i_a close to i_{af} , and during (a, b) the duty cycle is decreased to make i_a close to i_{af} , and so on. Therefore, the phase A current will coincide with its fundamental, and the distortion can be eliminated. Over one line cycle, one modulated duty cycle is obtained, which is a constant duty cycle with the 5th-order harmonic injection.

However, in three-phase currents, there is no such a straightforward solution, because three phase currents are distorted in different directions. As shown in Fig. 3.2, in which three phase currents i_a, i_b, i_c over $(0, \pi)$ are plotted, along with their corresponding fundamentals i_{af}, i_{bf}, i_{cf} , if the duty cycle is decreased during $(0, a)$, the current distortions in phase B and C can be improved, but phase A will get worse. So it is difficult to say how to modulate the duty cycle. The only thing that can be done is to make tradeoff among the three phases in a reasonable manner.

Namely, the duty cycle should be modulated to reduce the distortions of two phases and not to worsen the third phase too much. For example, in Fig. 3.2, during $(0, a)$, the duty cycle D is decreased to reduce phase B and C distortions and not to worsen phase A too much; during (a, b) , D is increased to improve phase A and C distortions and not to

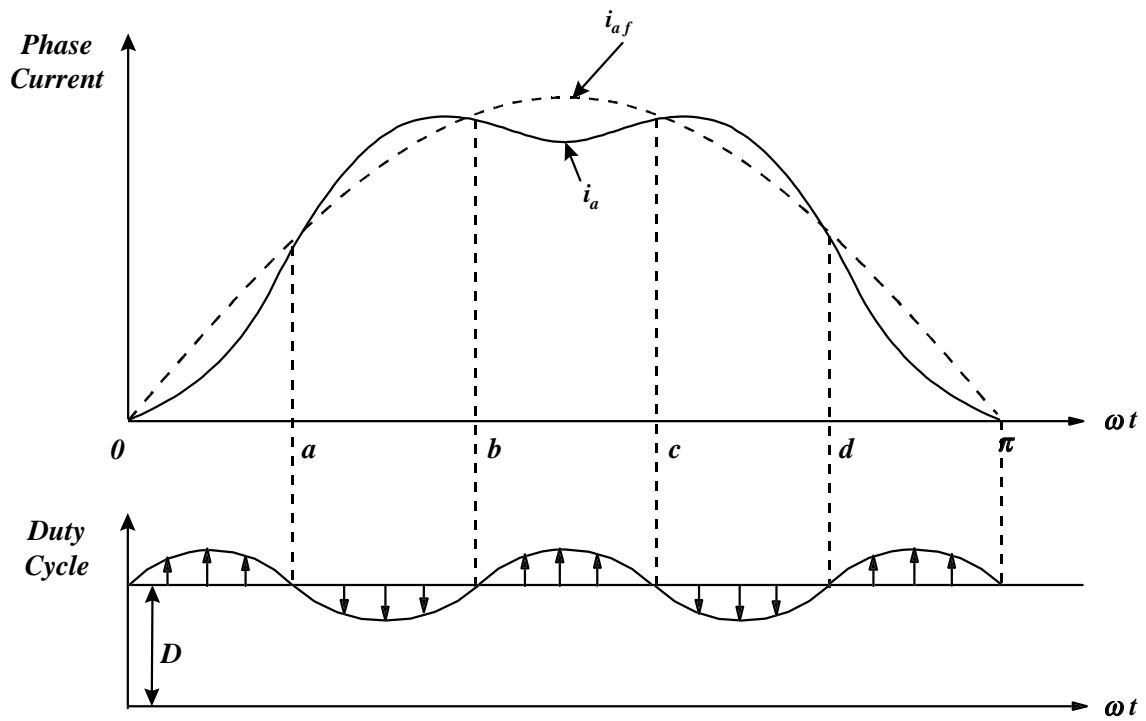


Fig. 3.1. Duty cycle modulation concept in one phase current

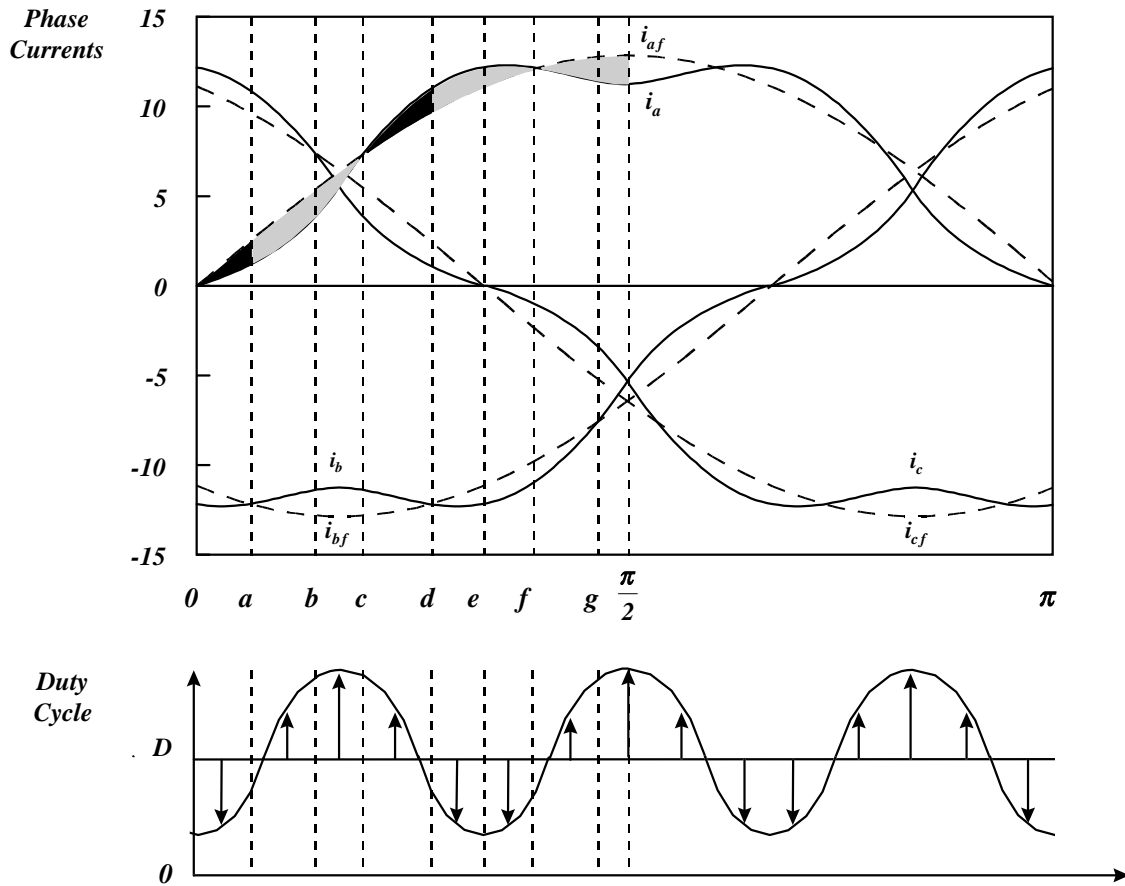


Fig. 3.2. Duty cycle modulation concept in three phase currents

worsen phase B too much, and so on. By doing this, during $(0, \pi/2)$ interval, all periods of phase A current benefit from this modulation except in $(0, a)$ and (c, d) (black areas) where distortions get worse. Therefore, the three-phase current distortions are improved. Observing one line cycle, a duty cycle in such variation is a constant duty cycle with a sixth-order harmonic injection.

Hence, the proposed duty cycle modulation method, a constant switching frequency with harmonic injection, selects the duty cycle as

$$d(t) = D[1 + m \sin(6\omega t + \frac{3\pi}{2})], \quad (3.1)$$

where m ($0 < m < 1$) is a modulation index.

With a sixth-order harmonic-injected PWM, the three-phase current distortions in a single-switch three-phase boost rectifier are improved. In the following, the validity of this approach is further proved mathematically.

Since the fifth-order harmonic is dominant, and the seventh-order and higher order harmonics are insignificant, the three-phase currents in Eq. (2.2) can be approximately expressed as:

$$\begin{aligned} i_a &= I_1 \sin \omega t + I_5 \sin(5\omega t + \pi), \\ i_b &= I_1 \sin(\omega t - \frac{2\pi}{3}) + I_5 \sin(5\omega t - \frac{\pi}{3}), \\ i_c &= I_1 \sin(\omega t - \frac{4\pi}{3}) + I_5 \sin(5\omega t + \frac{\pi}{3}), \end{aligned} \quad (3.2)$$

where the initial phases of the fifth-order harmonics are obtained by using Fourier analysis. The THD of these currents is

$$Thd_1 = \frac{I_5}{I_1}. \quad (3.3)$$

Similarly to Eq. (2.2), the magnitudes I_1 and I_5 in Eq. (3.2) are linearly proportional to the square of the duty cycle. Substituting this duty cycle with the modulated duty cycle defined in Eq. (3.1), and ignoring the presence of m^2 ($m^2 \ll 1$) terms and high-order harmonics ($n > 7$), Eq. (3.2) becomes (refer Appendix 6.1 in details):

$$\begin{aligned} i'_a &= I_1 \sin \omega t + (I_5 - mI_1) \sin(5\omega t + \pi) - mI_1 \sin 7\omega t, \\ i'_b &= I_1 \sin(\omega t - \frac{2\pi}{3}) + (I_5 - mI_1) \sin(5\omega t - \frac{\pi}{3}) - mI_1 \sin(7\omega t - \frac{2\pi}{3}), \\ i'_c &= I_1 \sin(\omega t - \frac{4\pi}{3}) + (I_5 - mI_1) \sin(5\omega t + \frac{\pi}{3}) - mI_1 \sin(7\omega t - \frac{4\pi}{3}), \end{aligned} \quad (3.4)$$

which are the three-phase currents with the sixth-order harmonic injection. The THD of this current is

$$Thd_2 = \frac{\sqrt{(I_5 - mI_1)^2 + (mI_1)^2}}{I_1}. \quad (3.5)$$

Compared Eq. (3.5) to Eq. (3.3), if $0 < m < I_5 / I_1$, the following inequality is always satisfied:

$$Thd_2 < Thd_1. \quad (3.6)$$

That means that if one does not attempt to eliminate the fifth-order harmonic, the THD is always improved by using harmonic injection. In other words, with sixth-order harmonic injection, the fifth-order harmonic can be suppressed. Even though the seventh-order harmonic is increased by the same amplitude at the same time, the THD is improved.

In practice, how to select the magnitude of the sixth-order harmonic or the modulation index m in Eq. (3.1) greatly depends on the design objectives. In the follow, two injection methods are proposed in order to reduce the harmonics to meet either the THD requirement or the IEC standard.

3.2 Injection Method I: To Meet THD Requirement

In the applications, if the current distortions of a rectifier are qualified by the THD, a minimum THD is usually desired. With the sixth-order harmonic injection, the THD is represented in Eq. (3.5) and can be minimized, as long as the modulation index m is properly selected. This m can be obtained from

$$\frac{\partial Thd_2}{\partial m} = 0. \quad (3.7)$$

After solving Eq. (3.7), the m is calculated as

$$m = 0.5 \frac{I_5}{I_1}, \quad (3.8)$$

which can be further described as

$$m = 0.5 Thd_1. \quad (3.9)$$

So, if m is selected as in Eq. (3.9), Thd_2 in Eq. (3.5) can be minimized. In Fig. 3.3, the minimized Thd_2 is plotted, in the same way, with respect to the rectifier voltage gain M . In comparison to the result (Thd_1) without harmonic injection, the THD is reduced and the current distortions are improved, especially for a lower M . Particularly, in order to meet the THD<10% requirement, M can now be designed down to 1.45. For a rectifier with 3×220 -Vrms input, the output voltage can be designed as low as 780 V. Without harmonic injection, to meet the THD<10% requirement, the required M should be as high as 1.68 and the output voltage should be greater than 900 V. With harmonic injection, the improvement is obvious.

3.3 Injection Method II: To Meet IEC Standard

On the other hand, if the objective is to meet the IEC1000-3-2 (A) standard, the modulation index m can be selected so that the ratio of the fifth- to seventh-order harmonics is directly proportional to those of the IEC1000-3-2 (A) limits (Fig. 2.3). Therefore the rectifier can be pushed to as high power levels as possible under the conditions that the harmonic contents still meet the standard. So, m is selected to meet:

$$\frac{I_5 - mI_1}{mI_1} = \frac{1.14}{0.77}, \quad (3.10)$$

or to meet

$$m = 0.4 \frac{I_5}{I_1} = 0.4 Thd_1, \quad (3.11)$$

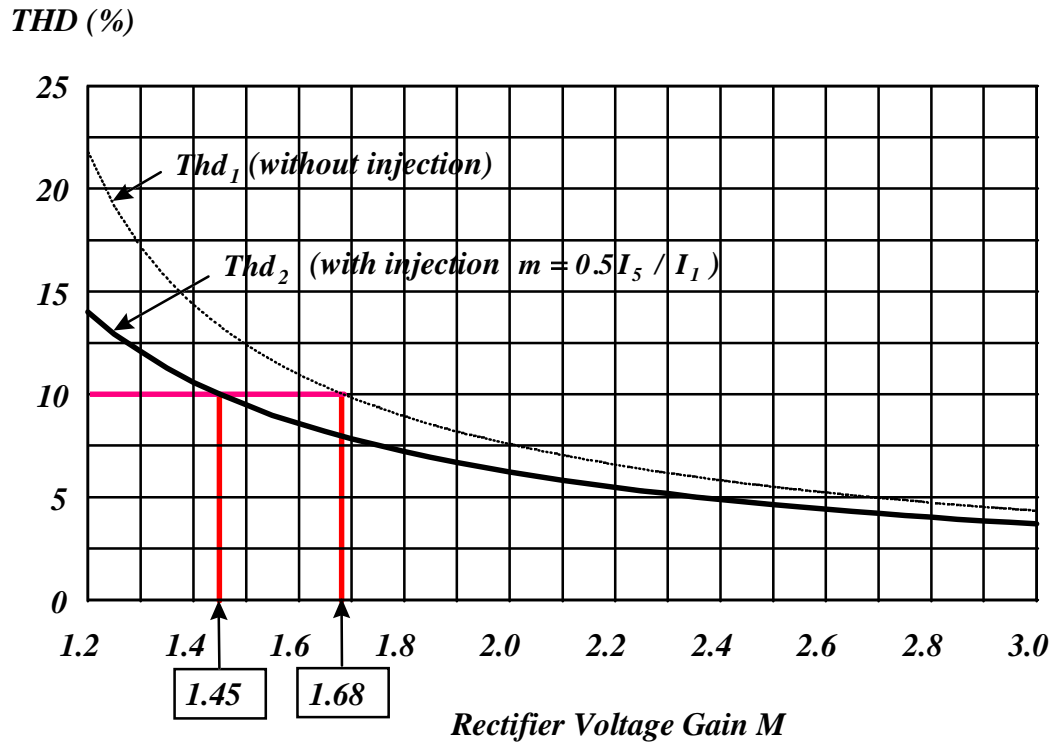


Fig. 3.3. THD as a function of M in constant switching frequency with harmonic-injected PWM

where 1.14 and 0.77 are the fifth- and seventh- order harmonics limited by the IEC 1000-3-2 (A) standard.

The harmonic contents with this selected m value for a rectifier with 3×220 -Vrms input/800-V output are plotted in Fig. 3.4. Compared to the IEC 1000-3-2 (A) standard, the results show that the rectifier can now be pushed up to around 10-kW power level. Without harmonic injection, to meet the IEC 1000-3-2 (A) standard, the output power only can be pushed to 5 kW for the rectifier with 3×220 -Vrms input/800-V output. With harmonic injection, the improvement is obvious.

All above results show that for one phase current, the distortions can be dramatically suppressed or even eliminated using the duty cycle modulation. However, the harmonic reduction in the three-phase rectifier is restrictive. Since only one switch is connected on the rectifier dc-side, it is impossible to balance three phase currents whose distortions are in different directions. As shown in Fig. 3.2, at almost all time intervals, any attempt to improve the distortions in two phases is at the penalty of increasing distortion in the third phase. So the THD improvement is an optimization problem. The proposed sixth-order harmonic injected PWM is a reasonable attempt at a search for this optimum PWM scheme.

CURRENT [rms, A]

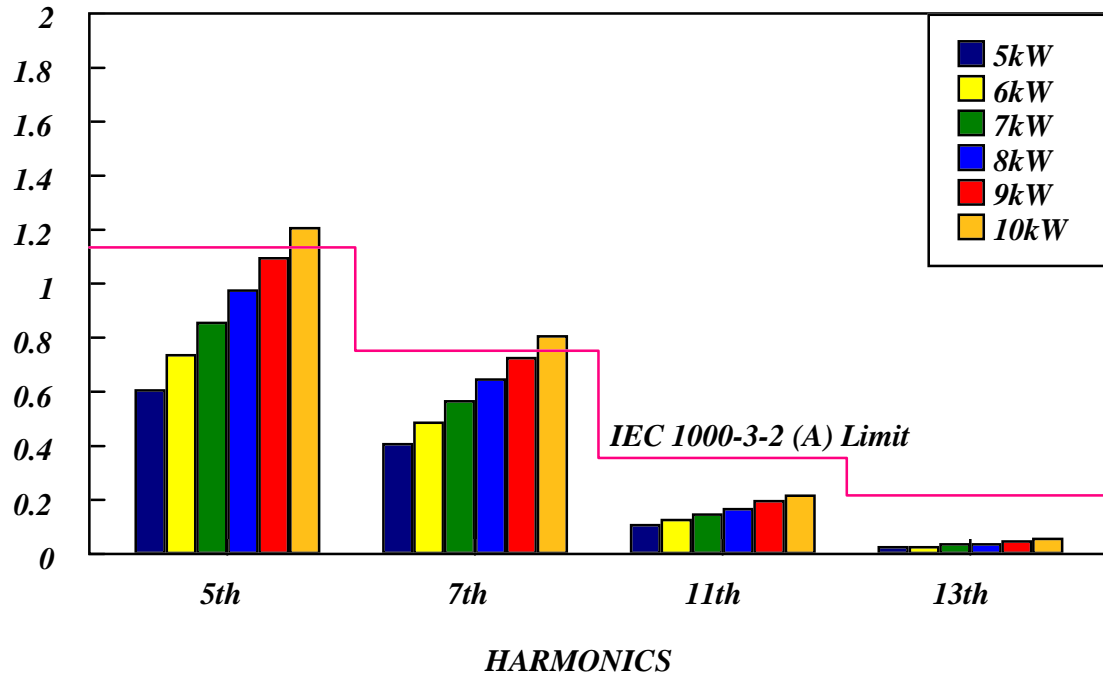


Fig. 3.4. Harmonic contents in constant switching frequency with harmonic-injected PWM @3X220-Vrms input/800-V output

3.4 Implementation of Injection

In the above sections, the harmonic-injected PWM concept has been established. In this section, a technique used to implement the harmonic injection will be developed.

As shown in Fig. 3.5, the implementation of harmonic injection is very simple. Based on the control loop designed for a constant switching frequency PWM, a synchronized harmonic generator is used to provide a sixth-order sinusoidal signal with a unity amplitude. A multiplier is used to modify the amplitude of the sixth-order harmonic by the modulation index. An adder is used to combine the injected signal with the feedback. Therefore, the equivalent duty cycle is going to be

$$d(t) = D[1 + m \sin(6\omega t + \frac{3\pi}{2})],$$

which is the required signal in Eq. (3.1).

3.4.1 Harmonic Generator

The harmonic generator is used to sense the three-phase voltages and to generate a synchronized sixth-order harmonic with a unity amplitude when the input voltages are nominal:

$$V_{hg_out} = \sin(6\omega t + 270^\circ). \quad (3.12)$$

As shown in Fig. 3.6, the harmonic generator consists of three transformers connected in $Y-\Delta$ style, a full-bridge diode rectifier, a divider, and an active bandpass filter. The harmonic generator is detailed in Fig. 3.7.

From the input to output of the harmonic generator, the phase shift for the sixth-order harmonic should be $+270^\circ$. As shown in Fig. 3.8, the three transformers connected in $Y-\Delta$ style are used to produce a synchronized signal with -30° phase shift for the fundamental. This phase shift becomes -180° for the sixth-order harmonic. A full-bridge diode rectifier is used to generate high-order harmonics whose fundamental is a sixth-order harmonic with $+90^\circ$ phase shift. A bandpass filter with 0° phase shift is used to get a pure sixth-order harmonic. Then the total phase shift from the input to output of the harmonic generator is

$$\varphi = -180^\circ + 90^\circ + 0^\circ = -90^\circ, \quad (3.13)$$

or $+270^\circ$, which meets the required phase shift in Eq. (3.1).

In order to obtain a pure sixth-order harmonic, the bandpass filter should be carefully designed. The bandpass filter is a combination of a lowpass filter and a highpass filter, as shown in Fig. 3.7. The input of the bandpass filter is the output of the diode rectifier, as shown in Fig. 3.8 (c). This signal consists of a dc value, a sixth-order harmonic, and twelfth-order and higher-order harmonics. To get the sixth-order harmonic, the responses of the lowpass filter and highpass filter are selected as:

Lowpass filter: 3 dB at 600 Hz, 60 dB at 6 kHz, ($f_{c1} = 600$ Hz)

Highpass filter: 3 dB at 100 Hz, 60 dB at 10 Hz, ($f_{c2} = 100$ Hz)

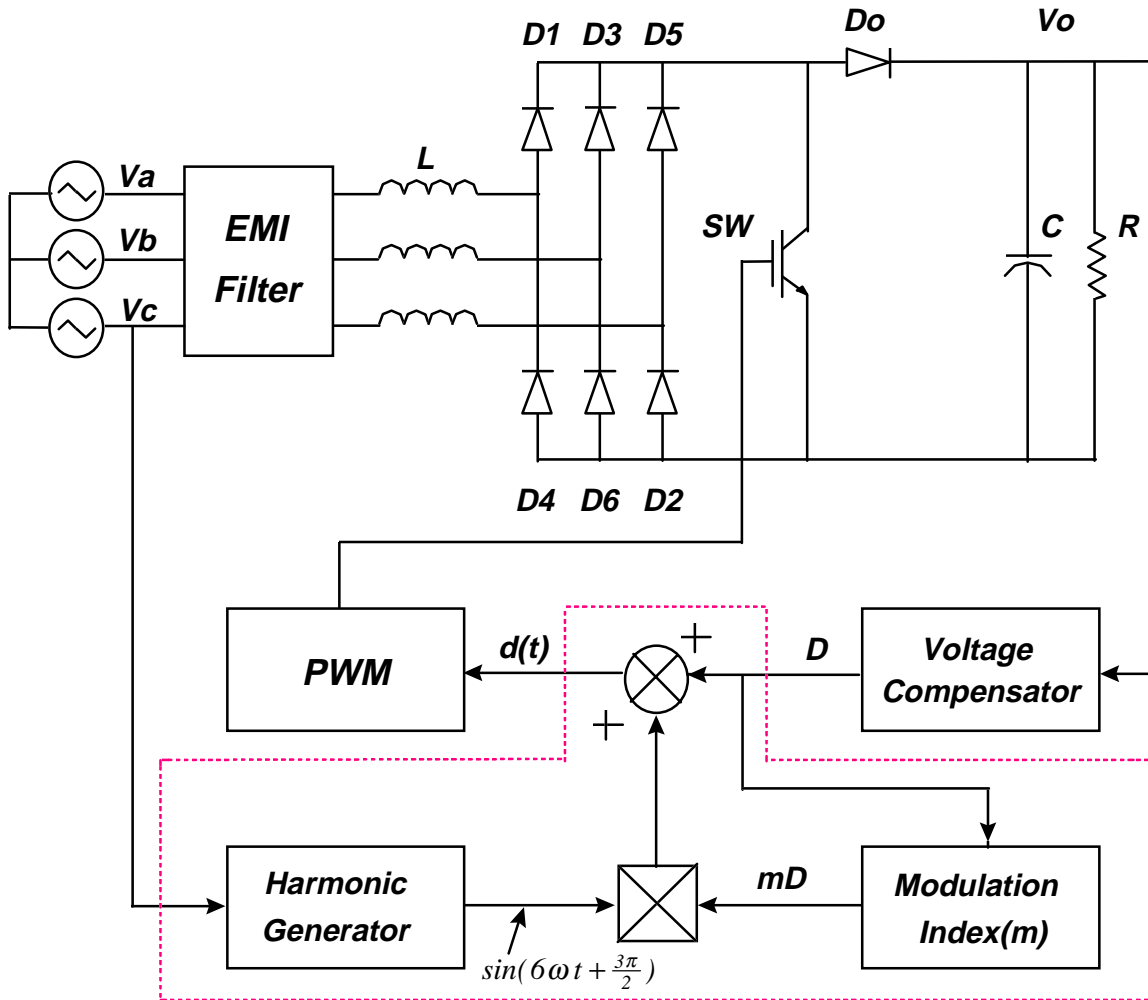


Fig. 3.5. Implementation of the injection

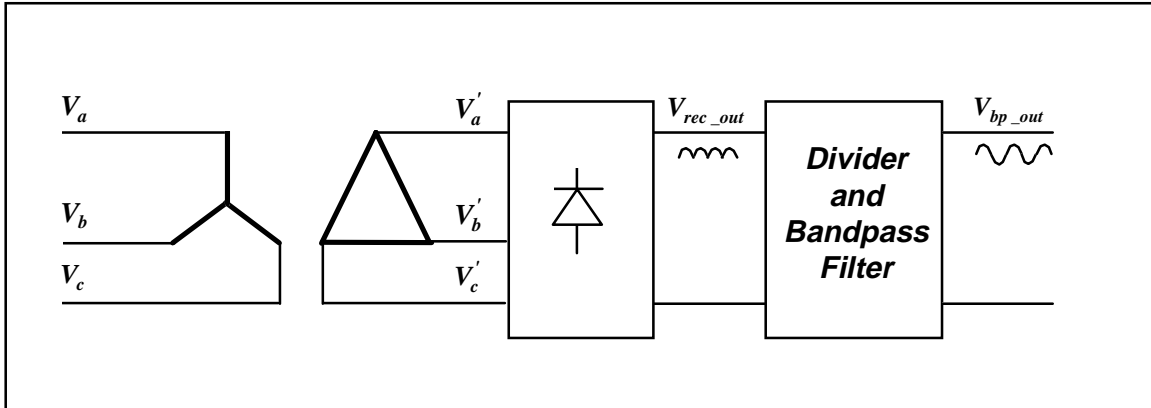


Fig. 3.6. Harmonic generator

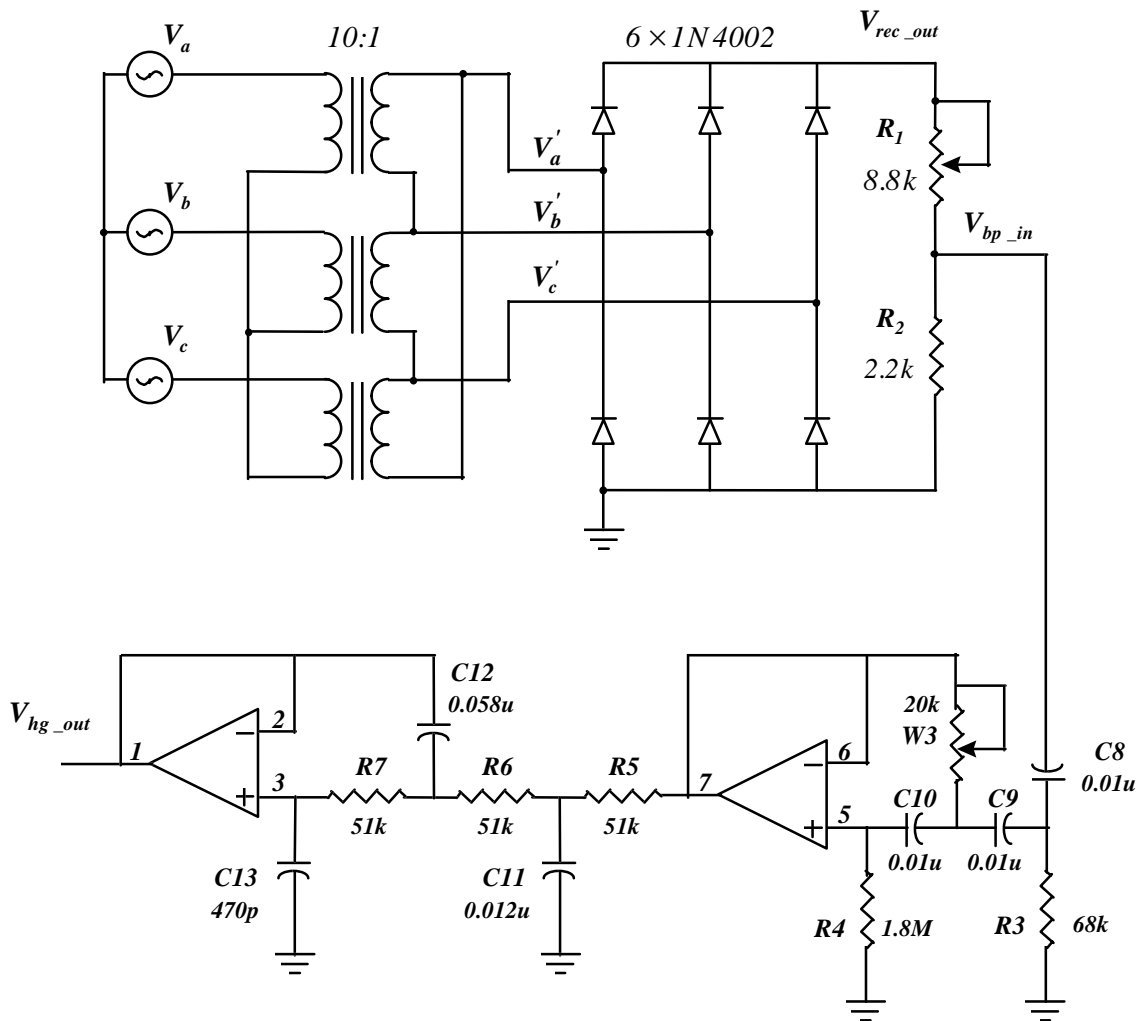


Fig. 3.7. Circuit implementation of harmonic generator

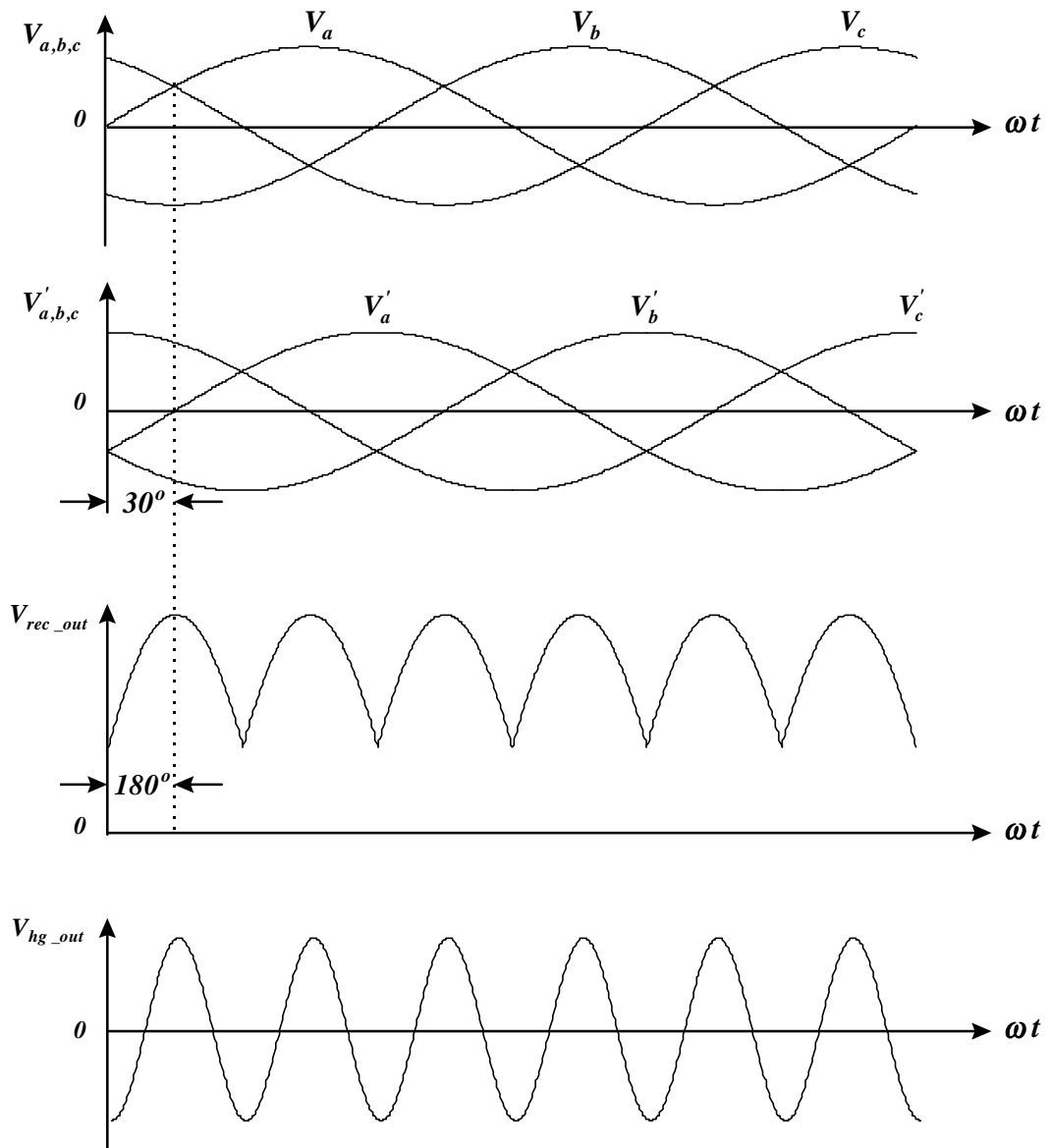


Fig. 3.8. The waveforms in harmonic generator

The procedure of filter design can be referred to [10]. Here, the lowpass filter is designed:

(a) Compute lowpass steepness factor As

$$A_s = \frac{f_s}{f_{c1}} = \frac{6000}{600} = 10.$$

(b) The response curve in [10, pp2-46] indicates that a third-order Chebyshev lowpass filter meets the 60 dB requirement.

(c) The normalized values can be found in [10, pp11-43]

$$R'_5 = R'_6 = R'_7 = 1,$$

$$C'_{11} = 2.25, C'_{12} = 11.23, C'_{13} = 0.0895.$$

(d) The frequency scaling factor is calculated:

$$FSF = 2\pi f_{c1} = 2\pi \times 600 = 3.77 \times 10^3.$$

With an impedance-scaling factor $Z = 5.1 \times 10^4$, the filter components are calculated as:

$$R_5 = R'_5 \times Z = 5.1k, R_6 = R_7 = 5.1k,$$

$$C_{11} = \frac{C'_{11}}{FSF \times Z} = \frac{2.25}{3.77 \times 10^3 \times 5.1 \times 10^4} = 0.012 \mu F,$$

$$C_{12} = 0.058 \mu F, C_{13} = 470 pF.$$

The highpass filter can be designed in the same way. The designed components are

$$C_8 = C_9 = C_{10} = 0.1 \mu F,$$

$$W_3 = 14k, R_3 = 68k, R_4 = 1.8M.$$

The phase delay of the lowpass filter at the sixth-order harmonic ($f = 360$ Hz) is given by

$$\phi_L = -\frac{135 \times f}{f_{c1}} = -\frac{135 \times 360}{600} = -81^\circ.$$

The phase lead of the highpass filter at the sixth-order harmonic can be calculated in the same formula, which is $|\phi_L|$. Therefore, the total phase shift in the bandpass filter is zero.

The designed bandpass filter is tested by using HP4194A. The input to output transfer function is plotted in Fig. 3.9. At 360 Hz, the gain is 7.5 dB and phase shift is close to zero. The total phase shift is tuned by W3 in Fig. 3.7.

The output of the harmonic generator should be designed with a unity amplitude when the three-phase input voltages are nominal. In order to attenuate the three-phase input voltages into the range of control circuit power supply (± 15 V), the transformer turns ratio N is selected as 10. The type of transformer is PSD2-36. Therefore, with nominal three-phase input voltages

$$V_a = V_m \sin(\omega t),$$

$$V_b = V_m \sin(\omega t - \frac{2\pi}{3}),$$

$$V_c = V_m \sin(\omega t - \frac{4\pi}{3}),$$

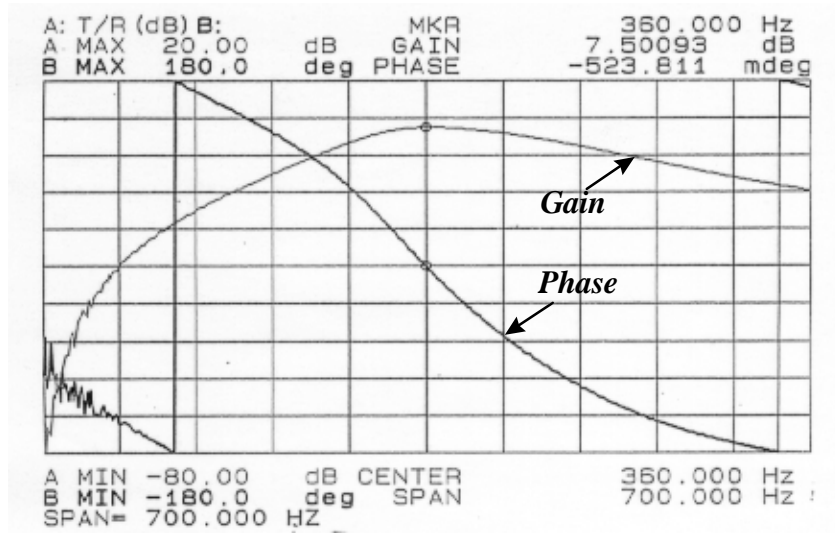


Fig. 3.9. Input to output transfer function of the designed bandpass filter

the transformer outputs are

$$V'_a = V'_m \sin(\omega t - \frac{\pi}{6}), \quad V'_b = V'_m \sin(\omega t - \frac{2\pi}{3} - \frac{\pi}{6}), \quad V'_c = V'_m \sin(\omega t - \frac{4\pi}{3} - \frac{\pi}{6}),$$

where $|V'_m|$ is given by

$$|V'_m| = \frac{1}{N} \frac{1}{\sqrt{3}} |V_m| = \frac{311}{10\sqrt{3}} = 17.96V.$$

Hence, from the waveforms in Fig. 3.8, the magnitude of the sixth order harmonic at the rectifier output can be estimated:

$$|V_{rec_out}| = \frac{1}{2} [(V'_c - V'_b)_{\omega t=0} - (V'_c - V'_b)_{\omega t=30^\circ}] = \frac{2\sqrt{3}-3}{4} |V'_m| = 2.10V.$$

Since the bandpass filter gain is 7.5 dB, i.e.:

$$20 \log\left(\frac{V_{hg_out}}{V_{bp_in}}\right) = 7.5dB,$$

the input of the bandpass filter should be:

$$V_{bp_in} = \frac{V_{hg_out}}{2.37} = \frac{1.0}{2.37} = 0.422V,$$

from which the divider gain can be calculated as:

$$\frac{R_2}{R_1 + R_2} = \frac{V_{bp_in}}{V_{rec_out}} = \frac{0.422}{2.10} = 0.20.$$

So, if $R_2 = 2.2k$ is selected, $R_1 = 8.8k$ is obtained.

3.4.2. Modulation Index, Multiplier, and Adder

The circuit implementation of the multiplier and modulation index blocks are given in Fig. 3.10. The multiplier is implemented by an AD 633 chip, whose output-input relation is given by:

$$W = \frac{X_1 Y_1}{10}.$$

The modulation index is simply implemented by a resistor divider, R_8 and W_4 . Therefore, the input-output relation of the circuit in Fig.3.10 is

$$d(t) = D \left[1 + \frac{W_4}{10(R_8 + W_4)} V_{hg_out} \right].$$

The modulation index is represented by

$$m = \frac{W_4}{10(R_8 + W_4)}.$$

If the output of the harmonic generator is plugged in, the above equation becomes:

$$d(t) = D \left[1 + m \sin(6\omega t + \frac{3\pi}{2}) \right],$$

which meets the required signal in Eq. (3.1).

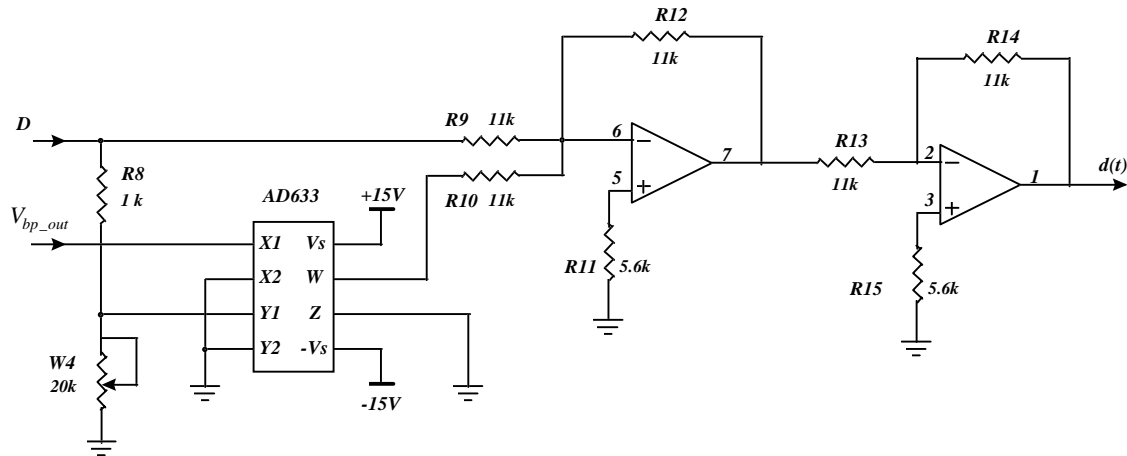


Fig. 3.10. Circuit implementation of multiplier, modulation index, and adder

3.5 Verification of Injection

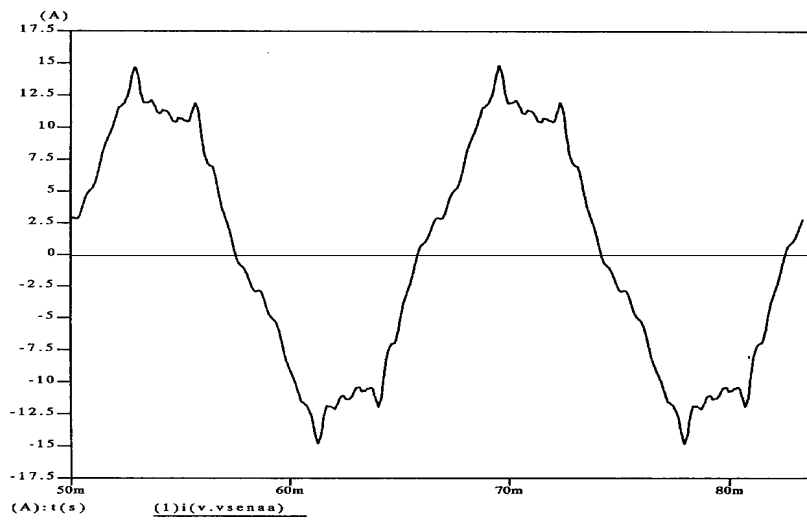
The single-switch three-phase boost rectifier with harmonic-injected PWM has been studied on both a simulation model and an experimental prototype to demonstrate the validity of the harmonic-injected approach and the system performance.

The prototype is designed with the following parameters:

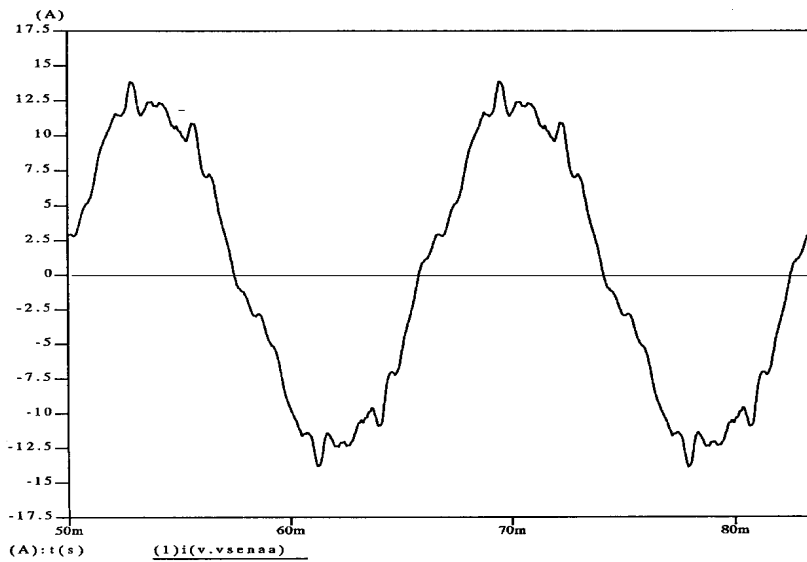
- Input/output: 3X220 V_{rms}/60 Hz, 800 V/6 kW;
- Switching frequency: 45 kHz;
- Modulation index m : 4.6%;
- Control bandwidth: 300 Hz;
- EMI filter: 70 dB/30 kHz
- Input inductor: 60 μH
- Output capacitor: 440 μF

In comparison to the results without harmonic injection, the simulation current waveforms and their frequency spectra are presented in Fig. 3.11 and Fig. 3.12. The experimental current waveforms are presented in Fig. 3.13. The THD and harmonic contents coming from both simulation and experiment are listed in Table 3.1.

The results show that both simulation and experimental data match the theoretical derivation very well.

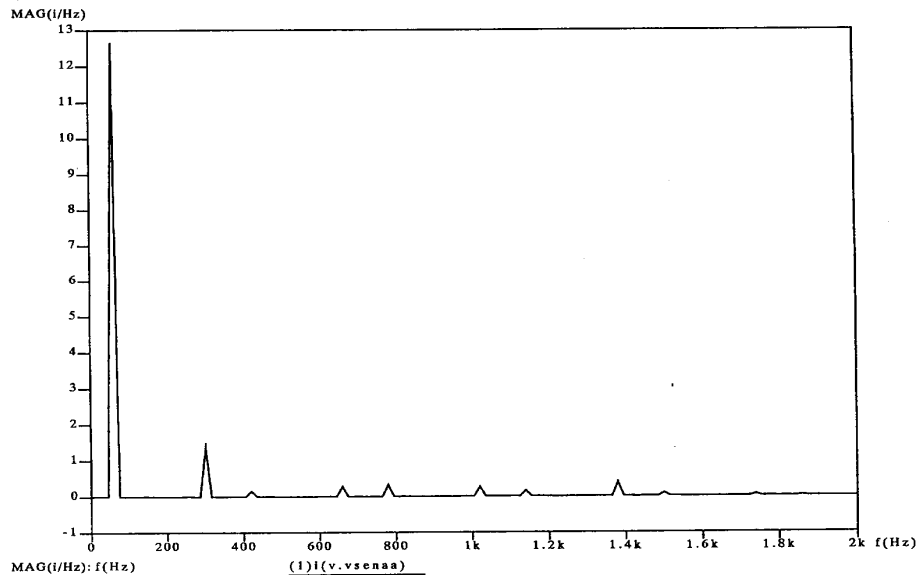


(a) Without harmonic injection ($m=0$)

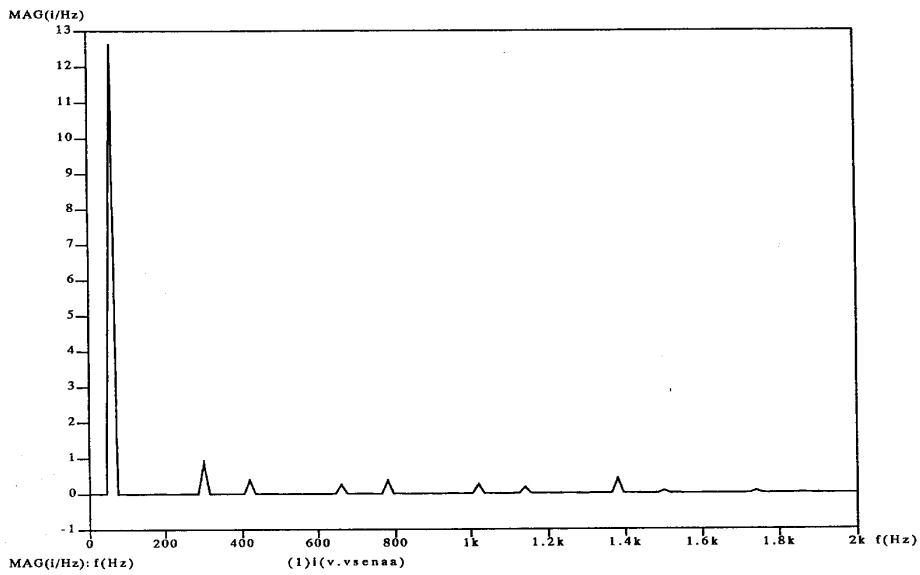


(b) With harmonic injection ($m=4.6\%$)

Fig. 3.11. Simulation current waveforms

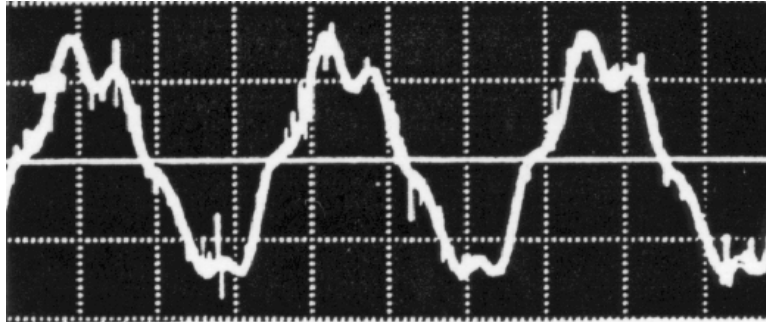


(a) Without harmonic injection ($m=0$)

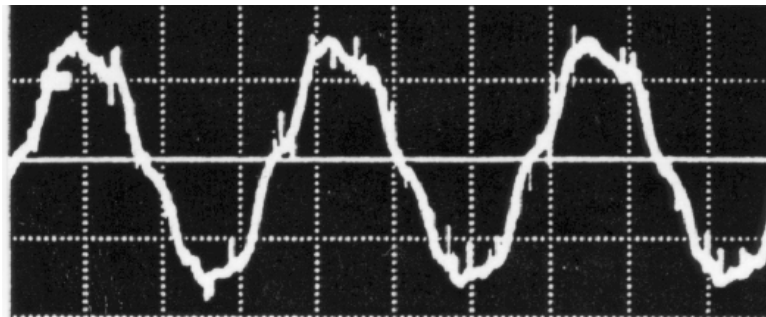


(b) With harmonic injection ($m=4.6\%$)

Fig. 3.12. Frequency spectra of the currents



(a). $m=0$



(b). $m=4.6\%$

Fig. 3.13. Experimental current waveforms (X:5 ms/div, Y:10 A/div)

Table 3.1. Harmonic contents [rms, A] in simulation and experiment

Modulation index	Simulation		Experiment	
	<i>m=0</i>	<i>m=4.6%</i>	<i>m=0</i>	<i>m=4.6%</i>
<i>THD</i>	<i>12.0%</i>	<i>9.2%</i>	<i>12.7%</i>	<i>9.5%</i>
<i>5th</i>	<i>0.96</i>	<i>0.61</i>	<i>1.15</i>	<i>0.71</i>
<i>7th</i>	<i>0.11</i>	<i>0.27</i>	<i>0.07</i>	<i>0.41</i>
<i>11th</i>	<i>0.20</i>	<i>0.18</i>	<i>0.06</i>	<i>0.20</i>
<i>13th</i>	<i>0.23</i>	<i>0.25</i>	<i>0.03</i>	<i>0.15</i>

4. Power Stage and Control Design

In this chapter, the inductor design and EMI filter design are presented first. Then the small signal model using the PWM switch model is developed and experimentally verified. Finally, the control design is discussed and a nonlinear gain controller is presented to improve the loop gain at the heavy load.

All numerical and experimental results demonstrated in this chapter are obtained from a rectifier (Fig. 1.1) designed with the following parameters:

- Input and output: 3X220 V_{rms}/60 Hz, 750 V;
- Switching frequency: 45 kHz;
- Load power: 6 kW to 50 W;
- Output Capacitor: 440 uF (capacitor ESR: 0.05 Ω).

4.1. Boost Inductor Design

Due to the DCM operation, the boost inductor design in a single-switch three-phase boost rectifier is critical. Conventionally, the design was carried out graphically, which is cumbersome, and the results are inaccurate [11]. In this section, a simple and straightforward approach is introduced to simplify the design procedure.

For a DC/DC boost converter, the results shown in Appendix 6.2 can be directly used to calculate the boost inductor. In fact, if the boost inductor of the DC/DC converter is selected so that the critical power in Eq. (A-8) is greater than the maximum delivered power, the DC/DC converter operates in DCM.

For a single-switch three-phase boost rectifier, the solution is not so straightforward. That is because the duty cycle D , critical power, and delivered power are functions of the instant of the sinusoidal input voltages. In other words, over one line cycle, the critical power is time-variant. At some instants, the critical power is going to be minimum. Hence, if these instants can be found and the inductor is designed at these worse cases, then the converter will operate at DCM over the whole line cycle.

Under balanced three-phase input voltages in Eq. (2.1), the equivalent input voltage of the circuit in Fig. 4.1 has to be:

$$V_{in_e} = \max[|V_{ab}(\omega t)|, |V_{bc}(\omega t)|, |V_{ca}(\omega t)|], \quad (4.1)$$

which repeats every 60° and reaches maximum at $\omega t = n \times 60^\circ$, $n = 0, 1, 2 \dots$, when the equivalent inductor is $L_e = 2L$. This is because at these moments one phase voltage is zero, and other two phase voltages applied to the input see two inductors in series. According to Eq. (A-8), once the input voltage reaches the maximum, the duty cycle D is minimum, and the critical power reaches the minimum. In other words, at these moments, the converter is going to operate in CCM the earliest as load is increased. For example,

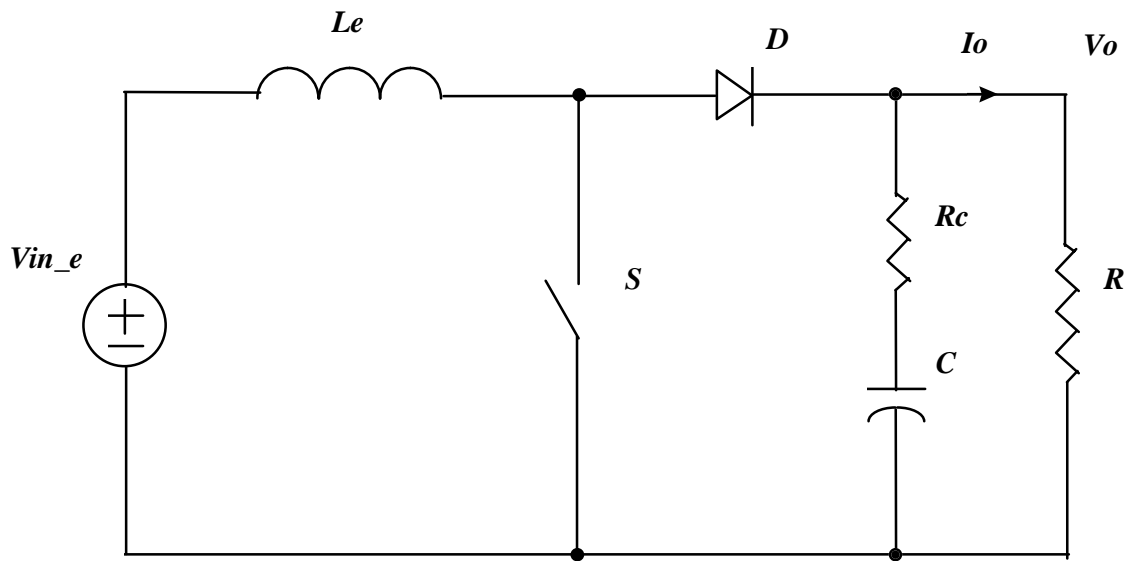


Fig. 4.1. An equivalent circuit of the single-switch three-phase boost rectifier

during $0^\circ \leq \omega t \leq 60^\circ$, $\omega t = 0^\circ$ and $\omega t = 60^\circ$ are the two moments at which the critical power reaches the minimum, and the converter is going to operate in CCM earlier than the other moments. So, as long as the inductors are selected to ensure the DCM operation at these two particular moments as load is maximum, the converter is going to operate in DCM in the whole load ranges and whole time periods. This is the inductor design guideline for the single-switch three-phase boost rectifier.

Typically, with the parameters in the designed rectifier, the maximum equivalent input voltage is

$$V_{in_e} = |V_{bc}(\omega t = 0^\circ)| = \sqrt{3}V_m \cos 0^\circ = 539 V. \quad (4.2)$$

Then the duty cycle in CCM is $D = 1 - V_{in_e} / V_o = 0.281$. To ensure the DCM operation, the critical power at this moment should be equal to the maximum load, then the equivalent boost inductor is obtained:

$$L_e = \frac{V_o^2}{2P_{o_max} f} D (1 - D)^2 = 151 \mu H, \quad (4.3)$$

and the boost inductor is $L = L_e / 2 = 75.5 \mu H$. With the 20% margin, the inductor should be selected as $60 \mu H$.

4.2. EMI Filter Design

The EMI filter design procedure was introduced in [12]. In this section, this procedure is adopted to design the differential-mode-conducted EMI filter. First, the required attenuation is obtained by comparing the real EMI emission with the CISPR 22 (A) standard. Recently, more and more manufacturers adopt CISPR 22 (Class A) as the EMI regulation, whose limits are 79 dBuV in 150 kHz-500 kHz, and 73 dBuV in 500 kHz-30 MHz. On the other hand, the real EMI emission is measured from the input current spectra in simulation. Due to the DCM operation, the EMI emission spectra are directly proportional to the output power. The higher the output power, the greater the conducted EMI emission. Hence, the maximum emission happens at full load. Secondly, in order to reduce the phase shift at the fundamental frequency, the upper value for the sum of all capacitors existing in the filter is limited:

$$C_{max} = \frac{I_m}{\omega V_m} \tan(\cos^{-1} IDF), \quad (4.4)$$

where V_m and I_m are the input voltage and current amplitudes, respectively, IDF is the input displacement factor which is defined as $IDF = \cos(\theta)$, and θ is the phase shift between input voltage and current. Thirdly, a damping branch is added in the input to control the impedance interaction between the input filter and rectifier, and to achieve the overall system stability.

The EMI filter design procedure is demonstrated in greater detail for the designed rectifier. First, the rectifier is simulated at full load (6 kW) by using SABER. The

Table 4.1. DM EMI emission and EMI filter attenuation

Frequency (kHz)	45	90	135	180	225	270	315	360	405	450	495
DM EMI Emission (dBuV)	177	167	155	146	146	146	145	134	130	138	136
CISPR 22 (A) Limits (dBuV)	N/A	N/A	N/A	79	79	79	79	79	79	73	73
EMI Filter Attenuation (dB)				67	67	67	66	55	51	65	63

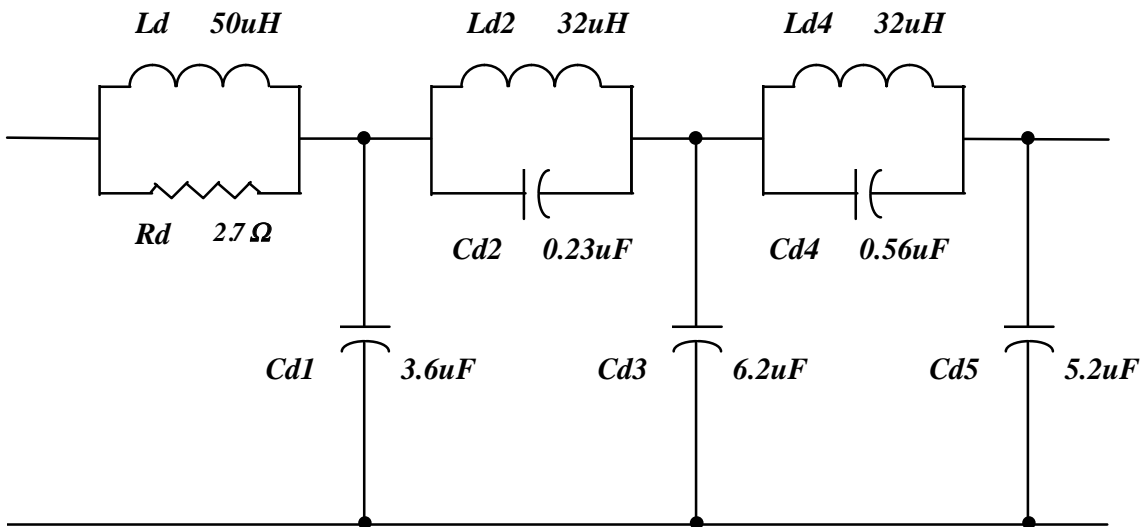


Fig. 4.2. The differential-mode EMI filter for the designed rectifier

differential-mode EMI emission is summarized in Table 4.1. Compared with CISPR 22 (A), it is shown that, at full load, the maximum conducted emission is 146 dB at 180 kHz. Hence, the minimum attenuation of the EMI filter (Differential Mode) is 67 dB. (EMI emission is less than 136 dBuV for high-frequency [$f > 495$ kHz] components). So, the attenuation of the EMI filter is selected as 70 dB.

Secondly, the input displacement factor is selected as

$$IDF = \cos(7.7^\circ) = 0.99. \quad (4.5)$$

Therefore, the upper value for the sum of all capacitors is calculated as

$$C_{max} = \frac{I_m}{\omega V_m} \tan(\cos^{-1} IDF) = \frac{12.86}{2\pi \times 60 \times 311} \tan(7.7^\circ) = 15\mu F. \quad (4.6)$$

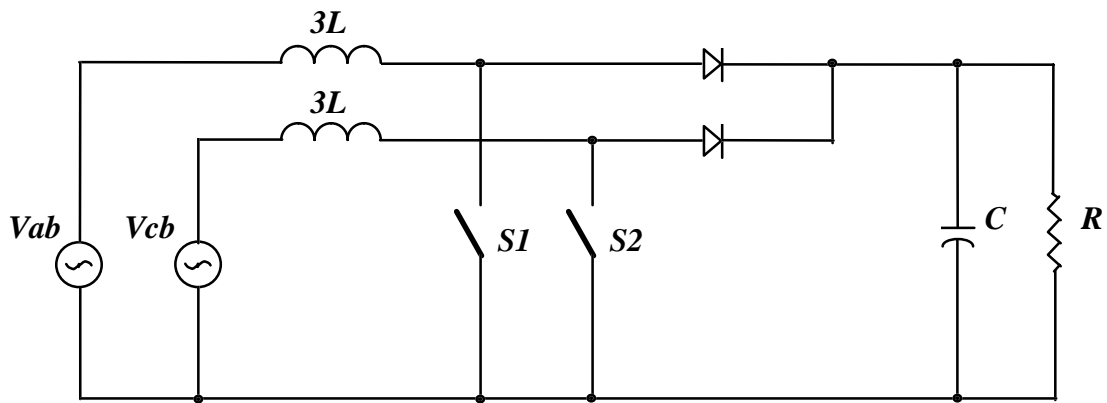
If the filter order is chosen as $n=5$, the normalized filter parameters are obtained [13, pp.222-223]: $\Omega_s = 2$, $C_1 = 1.097$, $C_2 = 0.07$, $L_2 = 1.35$, $C_3 = 1.9$, $C_4 = 0.17$, $L_4 = 1.34$, and $C_5 = 1.58$. The reference frequency is $\omega_r = 1.131E5 \text{ rad/s}$. The damping resistor is $R_d = 2.7 \Omega$. Therefore, the denormalized filter parameters are $C_{d1} = 3.6\mu F$, $C_{d2} = 0.23\mu F$, $L_{d2} = 32\mu H$, $C_{d3} = 6.2\mu F$, $C_{d4} = 0.56\mu F$, $L_{d4} = 32\mu H$, and $C_{d5} = 5.2\mu F$. A MATHCAD program to calculate these parameters is listed in Appendix 6.3. Thirdly, the damping branch is designed with $R_d = 2.7\Omega$ and $L_d = 50 \mu H$. The designed EMI filter is shown in Fig. 4.2.

4.3. Small Signal Model

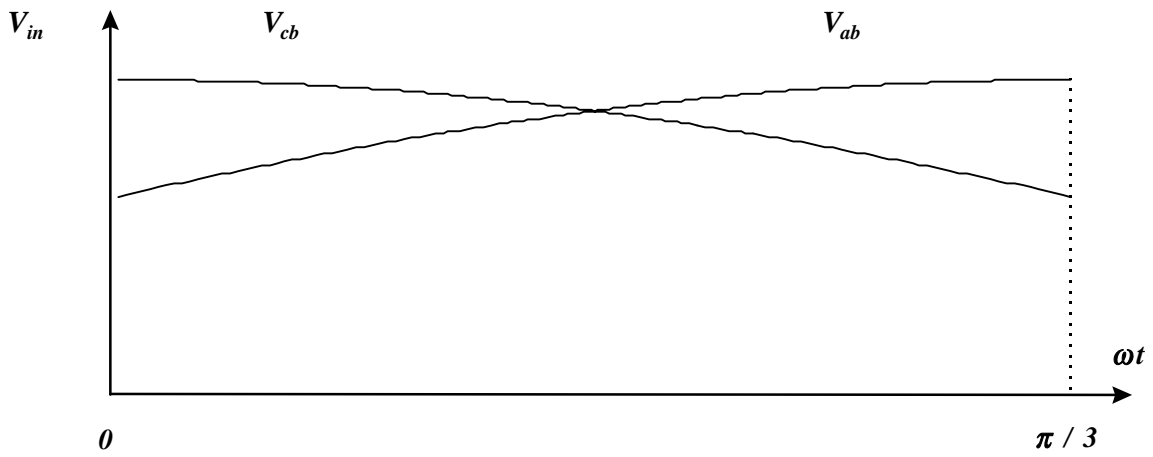
In order to properly control the single-switch three-phase boost rectifier, an accurate small-signal model is necessary. Two small-signal models, the state-space averaging model, and the PWM switch model, have been used [5] to describe the dynamic performance of the single-switch three-phase boost rectifier. The results showed that the PWM switch model was more accurate than the state-space averaging model. At high frequency, the state-space averaging model cannot predict the phase delay, since the model ignores the existence of a high-frequency pole and a right half-plane zero.

In this section, the PWM switch model is physically explained by using the equivalent multi-module model [15], which has been successfully employed in developing a small-signal model for the six-switch full-bridge rectifier [16]. Then, based on the steady-state analysis, the variations of the small-signal model against load are demonstrated. Finally, the PWM small-signal model is experimentally verified.

Under balanced three-phase voltages in Eq. (2.1), the single-switch three-phase boost rectifier can be viewed as two subconverters in parallel, as shown in Fig. 4.3 (a). Both subconverters include one switch, one inductor ($3L$), and one input voltage (V_{ab} or V_{cb}). Since the input voltage of each subconverter (Fig. 4.3 (b)) repeats every 60° and changes slowly, and since the required control bandwidth is lower than the frequency of the 6th order harmonic so that the harmonic injection technique can be applied, the average small-signal model developed in [17] can be used to describe the subconverter's small-



(a). The equivalent converter using two subconverters in parallel



(b). The equivalent input voltages

Fig. 4.3. The equivalent converter and its input voltages

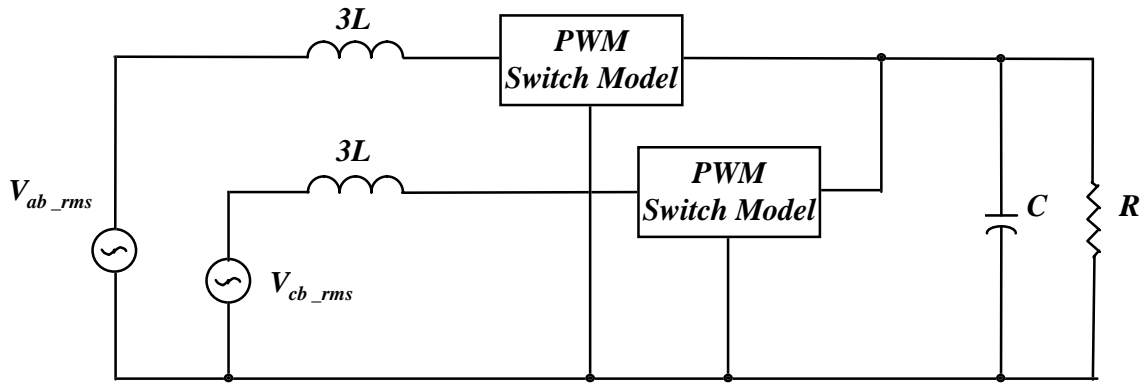


Fig. 4.4. Average model of subconverters

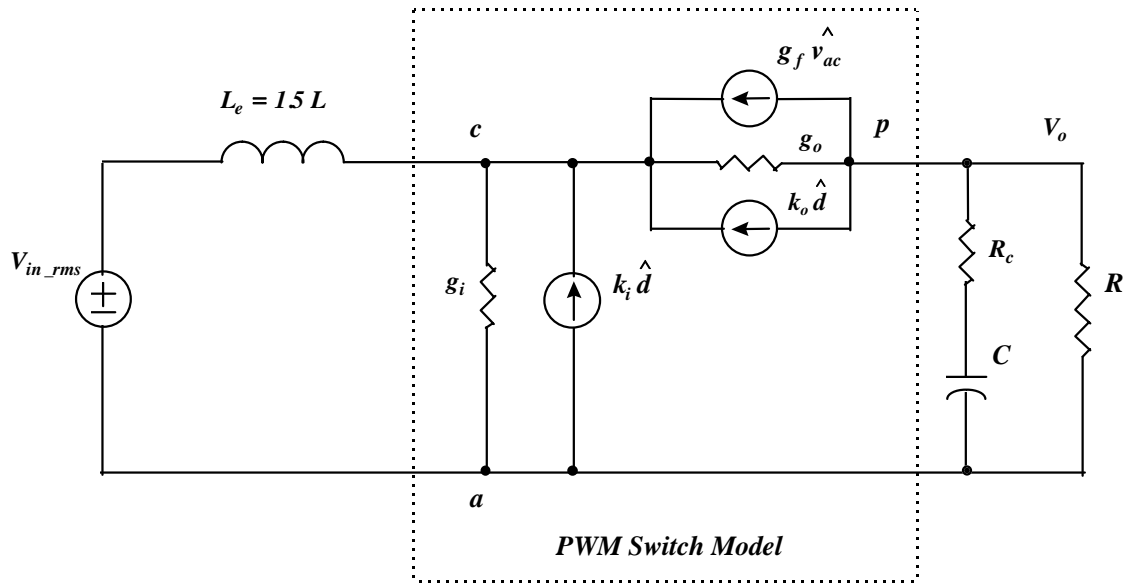


Fig. 4.5. PWM switch model of a single-switch three-phase rectifier
 $(g_i = M(M-1)/R, \quad g_o = M/(M-1)R, \quad g_f = 2M/R, \quad k_o = -2V_o/dR)$

signal model, as shown in Fig. 4.4. The equivalent input of each model is the RMS of the applied voltage. Then, according to [15], these two parallel subconverters, which have the same electric parameters, can be modeled by one converter with a series of equivalent parameters, as shown in Fig. 4.5. In the model, the equivalent input is given by:

$$\begin{aligned} V_{in_rms} &= \sqrt{\frac{3}{\pi} \int_0^{\pi/3} V_{bc}^2 d(\omega t)} = \sqrt{\frac{3}{\pi} \int_0^{\pi/3} 3V_m^2 \cos^2(\omega t) d(\omega t)} \\ &= \sqrt{\frac{3}{2} + \frac{9\sqrt{3}}{8\pi}} V_m = 1.46V_m, \end{aligned} \quad (4.7)$$

and the equivalent boost inductor is given by:

$$L_e = 1.5L. \quad (4.8)$$

Hence, a small signal model of the single-switch three-phase boost rectifier is obtained. From this model, the control-to-output transfer function can be derived:

$$\frac{\hat{v}_o}{\hat{d}} = \frac{2(M-1)V_o}{(2M-1)d} \frac{(1+s/s_{z1})(1-s/s_{z2})}{(1+s/s_{p1})(1+s/s_{p2})}, \quad (4.9)$$

where $s_{p1} = (2M-1)/((M-1)RC)$, $s_{p2} = (M-1)R/(M^3L_e)$, $s_{z1} = 1/R_cC$, $s_{z2} = R/(M^2L_e)$, $M = V_o/V_{in_rms}$, and d is duty cycle.

In this model, the dc-gain is load-dependent. To predict the dc-gain variations when the load is changed, the steady-state should be analyzed. For the designed example, $V_o = 750V$, $V_{in_rms} = 1.46 \times 311 = 454V$, $D = 1 - V_{in_rms}/V_o = 0.395$, $L_e = 90\mu H$, and $M = V_o/V_{in_rms} = 1.65$. According to Eq. (A-8), the critical power is given by

$$P_c = \frac{V_o^2}{2L_e f} D(1-D)^2 = 10.0kW. \quad (4.10)$$

At a given load P_o , the duty cycle can be computed using Eq. (A-6):

$$d = \sqrt{\frac{P_o}{P_c}} D. \quad (4.11)$$

With respect to P_o , Eq. (4.11) is plotted in Fig. 4.6. It is indicated that from heavy load to light load, the duty cycle gradually decreases. At no load, the duty cycle approaches zero. In Fig. 4.7, the dc-gain of the control-to-output transfer function is sketched with respect to load. It is shown that at no load, the dc-gain is infinite.

As shown in Eq. (4.9), the control-to-output transfer function represents a double-pole and double-zero plant. This plant exhibits a dominant pole S_{p1} , which is very close to the imaginary axis. The other pole S_{p2} and zeros S_{z1} and S_{z2} are far away from the imaginary axis, no matter what the load is. Hence, the plant performance will be mainly determined by the dominant pole. At low frequency, the plant behaves as a first-order system.

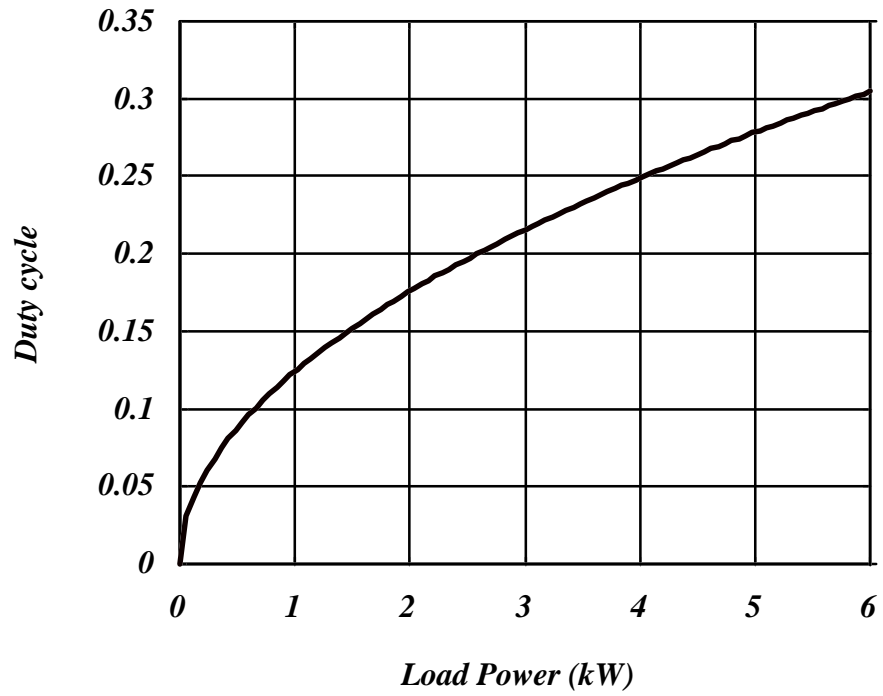


Fig. 4.6. Load effect on the duty cycle of a single-switch boost rectifier

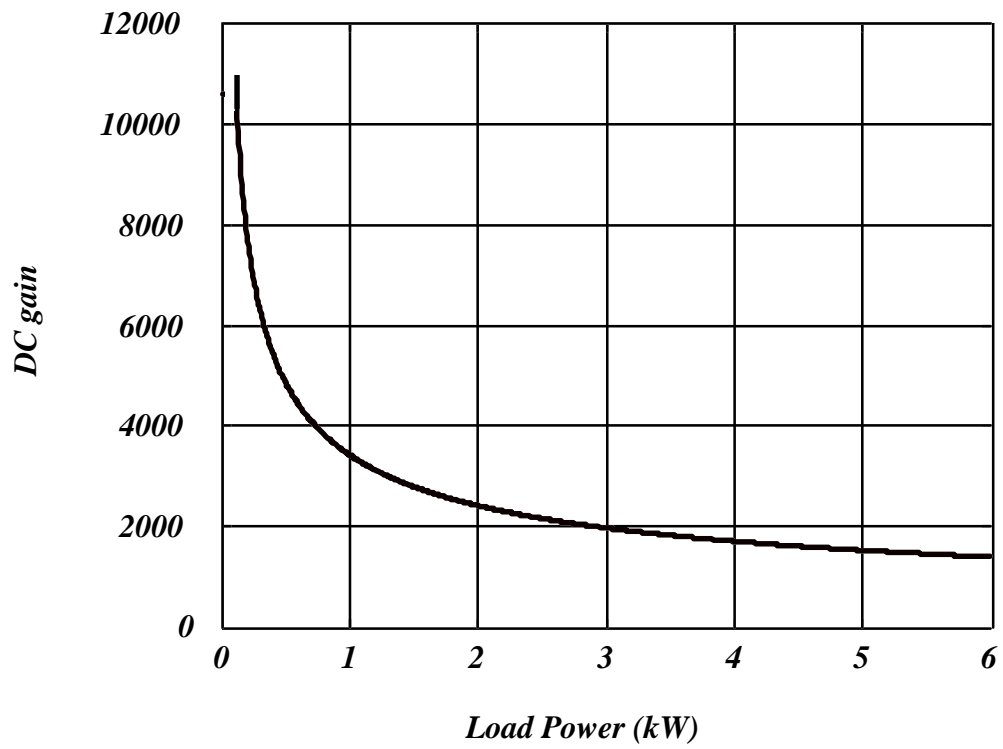


Fig. 4.7. Load effect on the dc-gain of control-to-output transfer function

However, even though it is the first-order system, the dominant pole in the plant is a moving pole when the load is changed. At light load, this pole moves close to the imaginary axis and creates more phase delay at low frequency. In Fig. 4.8, the control-to-output transfer functions at 6 kW, 50 W, 0.5 W and 0.005 W are plotted. At 6 kW, the control-to-output transfer function is given by:

$$\left. \frac{\hat{v}_o}{\hat{d}} \right|_{6kW_load} = 1.39 \times 10^3 \frac{(1 + \frac{s}{4.6 \times 10^4})(1 - \frac{s}{3.8 \times 10^5})}{(1 + \frac{s}{85.7})(1 + \frac{s}{1.5 \times 10^5})}, \quad (4.12)$$

At 50 W, 0.5 W, and 0.005 W, the control-to-output transfer functions are given by:

$$\left. \frac{\hat{v}_o}{\hat{d}} \right|_{50W_load} = 1.52 \times 10^4 \frac{(1 + \frac{s}{4.6 \times 10^4})(1 - \frac{s}{4.6 \times 10^7})}{(1 + \frac{s}{7.1 \times 10^{-1}})(1 + \frac{s}{1.81 \times 10^7})}; \quad (4.13)$$

$$\left. \frac{\hat{v}_o}{\hat{d}} \right|_{0.5W_load} = 1.52 \times 10^5 \frac{(1 + \frac{s}{4.6 \times 10^4})(1 - \frac{s}{4.6 \times 10^9})}{(1 + \frac{s}{7.1 \times 10^{-3}})(1 + \frac{s}{1.81 \times 10^9})}; \quad (4.14)$$

$$\left. \frac{\hat{v}_o}{\hat{d}} \right|_{0.005W_load} = 1.52 \times 10^6 \frac{(1 + \frac{s}{4.6 \times 10^4})(1 - \frac{s}{4.6 \times 10^{11}})}{(1 + \frac{s}{7.1 \times 10^{-5}})(1 + \frac{s}{1.81 \times 10^{11}})}. \quad (4.15)$$

The results in Fig. 4.8 show that from full load (6 kW) to a light load (0.005 W), the dominant pole moves from 13.6 Hz to 1.13×10^{-5} Hz, which is very close to the origin and causes more phase delay at low frequency region. For example, over the region where the frequency is greater than 0.01 Hz, this phase delay is 90° . Hence, with a linear control, in order to maintain the same control performance over the whole load ranges, the controller should be carefully designed.

The derived small-signal model is experimentally verified in the designed example with the parameters: $V_o = 730$ V, $V_{in_rms} = 1.46 \times 300 = 438$ V, $L_e = 90 \mu\text{H}$, $C = 440 \mu\text{F}$, and $R_c = 50$ m Ω . The first case is at a heavy load $R = 110 \Omega$ ($P_o = 4.8$ kW), whose control-to-output transfer function is given by

$$\left. \frac{\hat{v}_o}{\hat{d}} \right|_{4.8kW_load} = 3.22 \frac{(1 + \frac{s}{4.6 \times 10^4})(1 - \frac{s}{3.6 \times 10^5})}{(1 + \frac{s}{65.6})(1 + \frac{s}{1.6 \times 10^5})}. \quad (4.16)$$

The second case is at a light load $R = 9.8$ k Ω ($P_o = 54$ W), whose control-to-output transfer function is given by

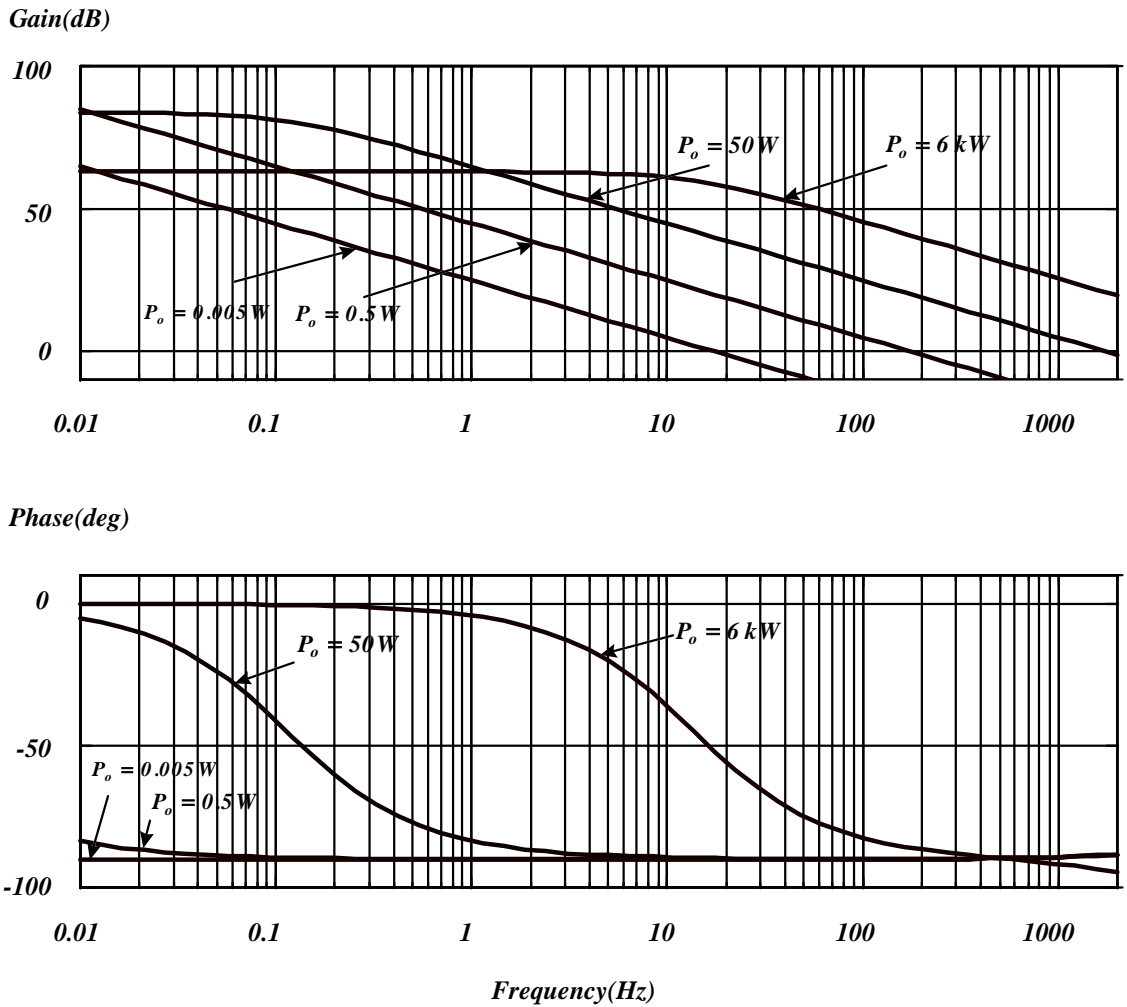


Fig. 4.8. Bode plots of control-to-output transfer function at 6 kW, 50 W, 0.5 W, and 0.005 W.

$$\left. \frac{\hat{v}_o}{\hat{d}} \right|_{54W_load} = 30.4 \frac{(1 + \frac{s}{4.6 \times 10^4})(1 - \frac{s}{3.2 \times 10^7})}{(1 + \frac{s}{0.74})(1 + \frac{s}{1.5 \times 10^7})}. \quad (4.17)$$

For a convenient comparison with the measured results, the dc-gains in both transfer functions include the attenuation caused by the output voltage sensor (46.4 dB) and the PWM chip (6.0 dB). The measurement set-up is shown in Fig. 4.9.

The derived and experimental control-to-output transfer functions are shown in Figs. 4.10 and 4.11, respectively. The measurement was completed using the impedance/gain-phase analyzer HP 4194A, whose lowest measurable frequency is 10 Hz. The integration time is set to “LONG”, the number of averaged measurement is set to “256”, and the signal level is selected as -20 dBV. To avoid measurement noise, the cable ground and shielding should be carefully made. The results indicate that both the magnitudes and phases obtained experimentally agree with those derived from the formulas very well. In the measurement, the glitches caused by 60 Hz line interference are visible at 60 Hz and 120 Hz. The visible glitch which occurred at 360 Hz is caused by the rectifier output voltage ripple.

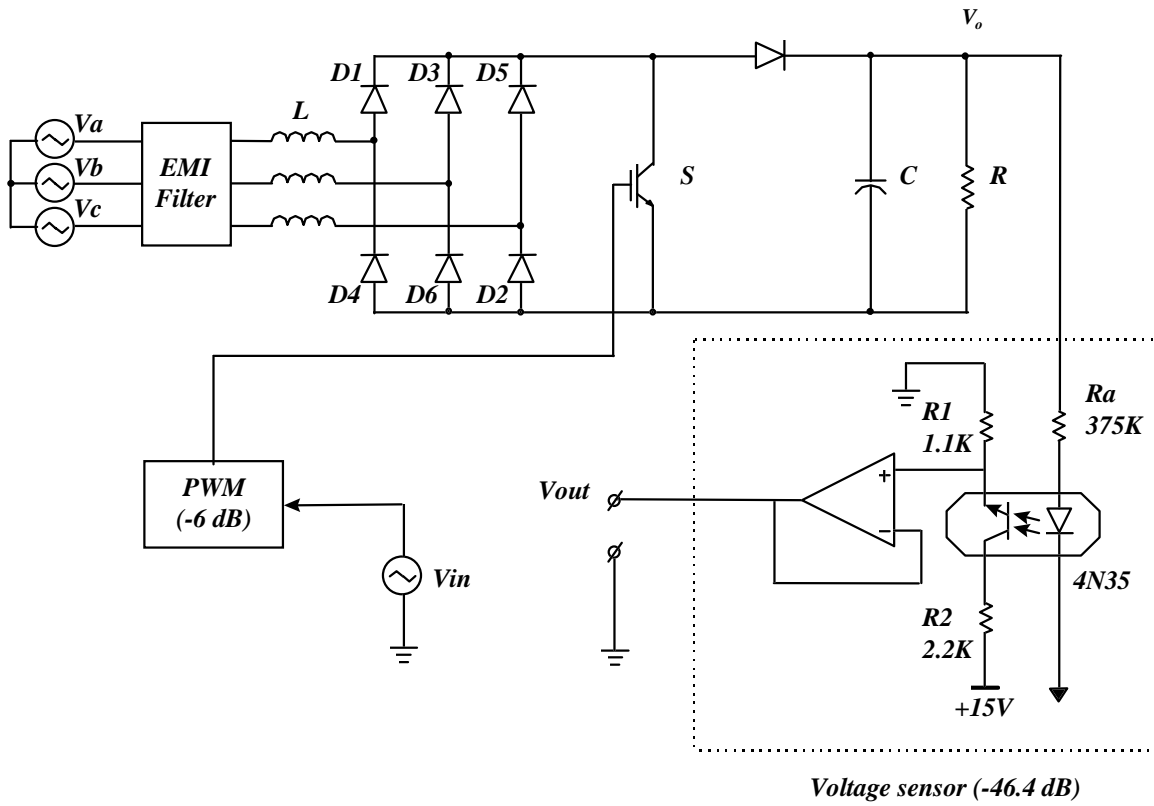
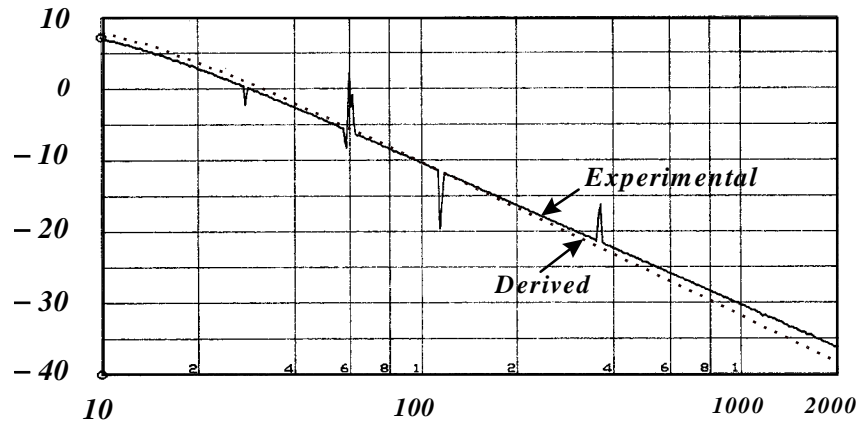


Fig. 4.9. Set-up of control-to-output transfer function measurement

Magnitude (dB)



Phase(deg)

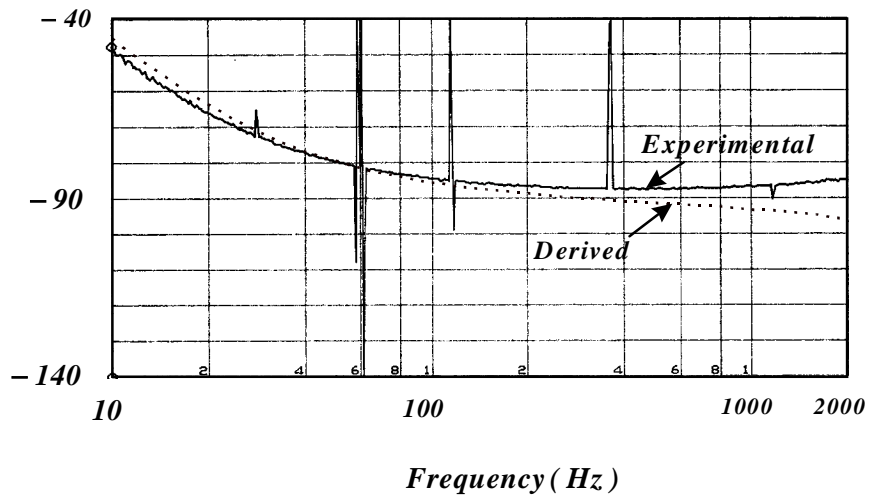


Fig. 4.10. Derived and experimental control-to-output transfer functions at a heavy load (4.8 kW) using the PWM switch model

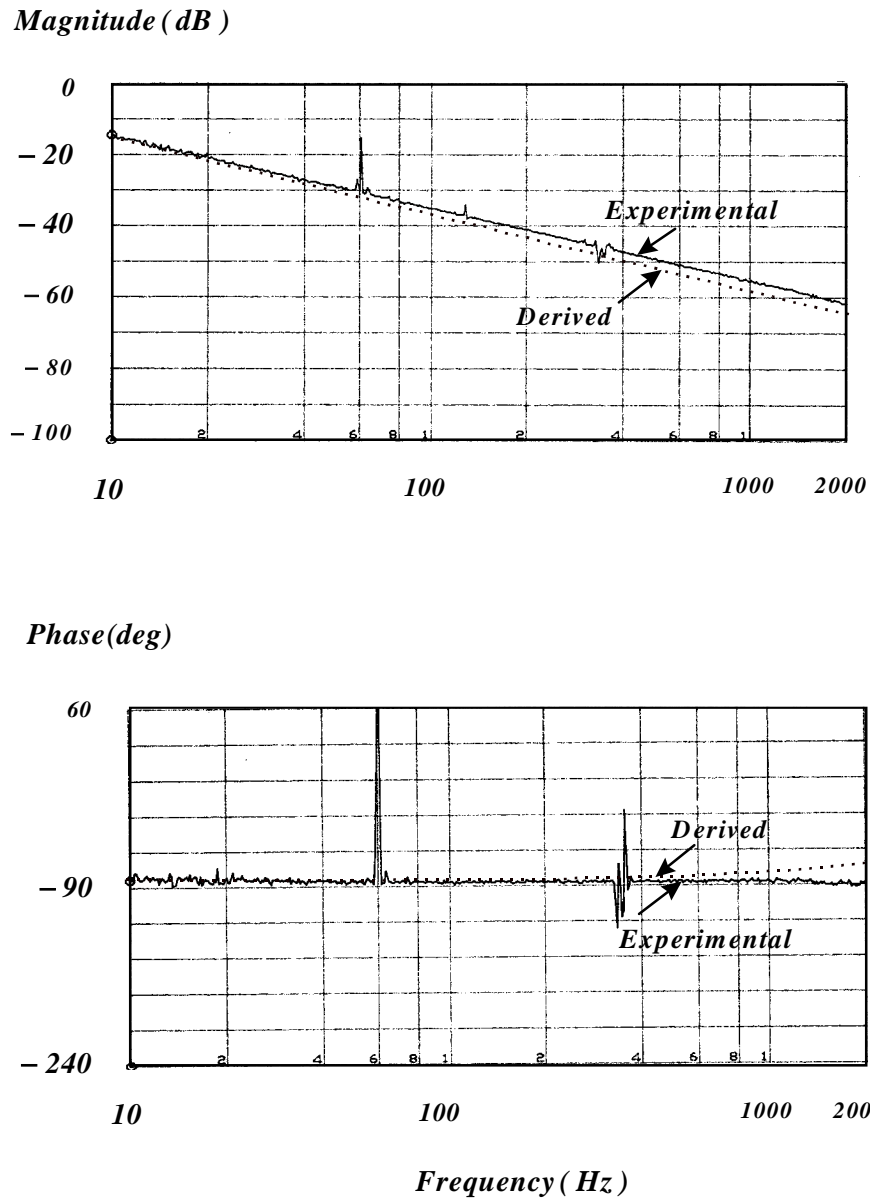


Fig. 4.11. *Derived and experimental control-to-output transfer functions at a light load (54 W) using the PWM switch model*

4.4. Voltage Compensator Design

Due to the DCM operation, the three-phase input currents of the single-switch three-phase boost rectifier are decoupling. Hence, only a single loop, specifically an output voltage loop, is necessary to achieve both the high quality input current control and the output voltage regulation. In addition, in order to apply the technique of the harmonic injection, the control bandwidth should be designed lower than the sixth-order harmonic (360 Hz).

Since at low frequency, the control-to-output transfer function of the single-switch three-phase boost rectifier behaves as a first order system, a compensator with one integrator, one zero, and one pole is selected as the voltage controller:

$$G_c = K_c \frac{1 + s / Z}{s(1 + s / P)}. \quad (4.18)$$

In Eq. (4.18), the integrator is used to increase the control loop dc-gain and reduce the steady-state error. The zero Z is used to compensate for the phase delay caused by the integrator and the dominant pole. The high-frequency pole P is used to suppress high-frequency noise.

Because the control bandwidth of the single-switch three-phase boost rectifier is less than 2262 rad/sec (360 Hz), the high-frequency pole of the compensator is selected as 3500 rad/sec. However, the selection of the zero is not so straightforward. The single-switch three-phase boost rectifier is required to operate from heavy load to light load, or even to no load, and, as shown in the last section, at no load, the system dominant pole approaches the origin, resulting in a 90° phase delay. Hence, over the whole load ranges, finding a proper way to choose the zero to compensate for this delay is a big challenge. In the following, the trial and error method is used to determine the location of the zero.

First, design the zero according to the full load case. The dominant pole at the full load is 85.7 rad/sec. Hence, the zero is selected as 350 rad/sec to compensate for the phase delay caused by this pole. To ensure the control bandwidth, the compensator gain is selected as $K_c=2800$ by using MATLAB. In addition, the attenuation caused by the PWM chip (6.0 dB) and the output voltage sensor (46.4 dB) is also considered. Therefore, the compensator is:

$$G_{c1} = 2800 \frac{1 + s / 350}{s(1 + s / 3500)}. \quad (4.19)$$

In Fig. 4.12, four loop gains, obtained with this compensator at 6 kW, 50 W, 10 W, and 1 W, are plotted. At the full load, a 50° phase margin and a 100-dB (at 0.01 Hz) gain are obtained. For the 50-W load, a 38° phase margin is obtained. However, if the phase margin is examined for the whole frequency ranges where the gain is greater than 0 dB, the phase margin for the 50-W load reduces to 5° (at 2 Hz), and the phase margins for 10-W and 1-W loads are around zero.

In order to compensate for the light load, the zero is moved to $Z_c=10$ rad/sec and the dc-gain is adjusted as $K_c=80$. Therefore, the compensator is:

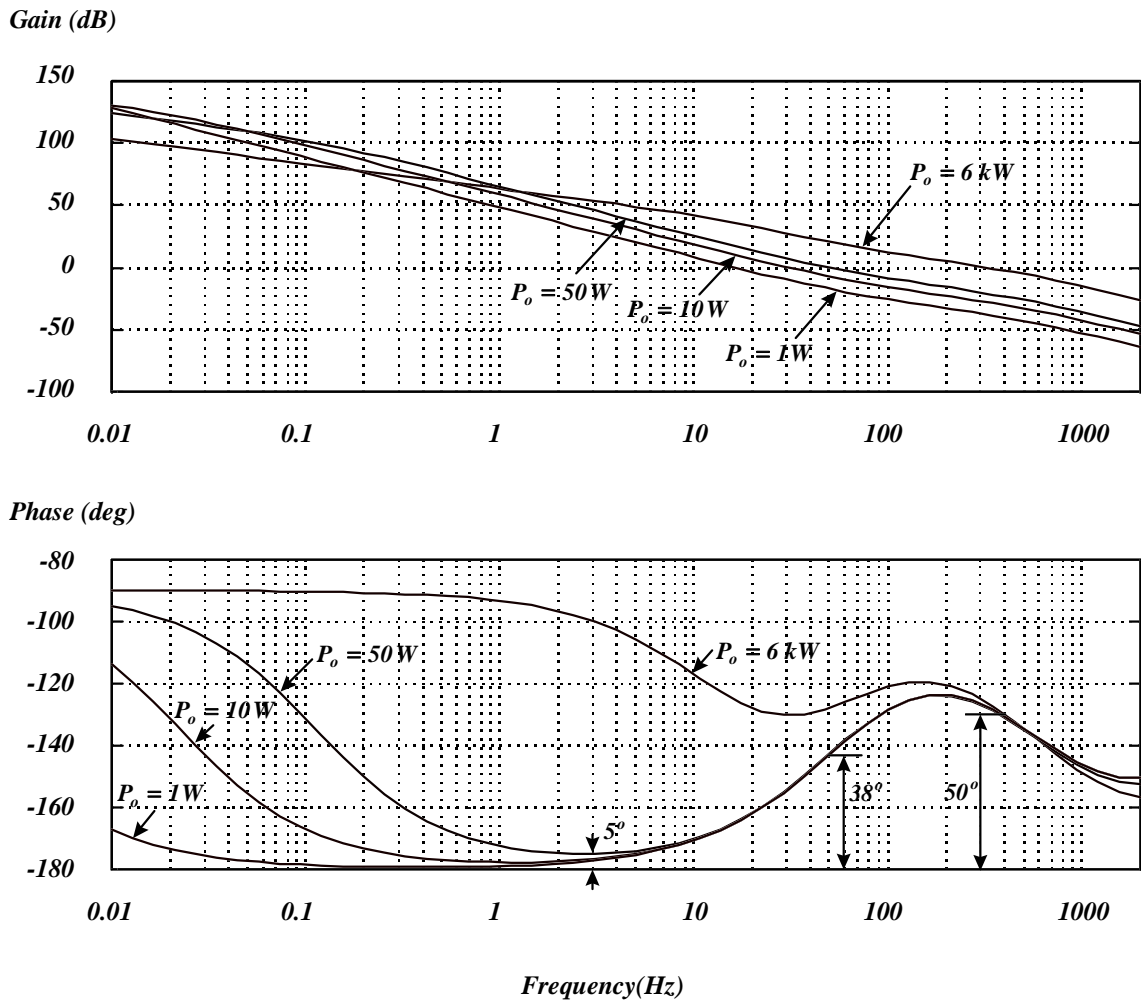


Fig. 4.12. Loop gains at 6 kW, 50 W, 10 W, and 1 W with compensator in Eq. (4.19)

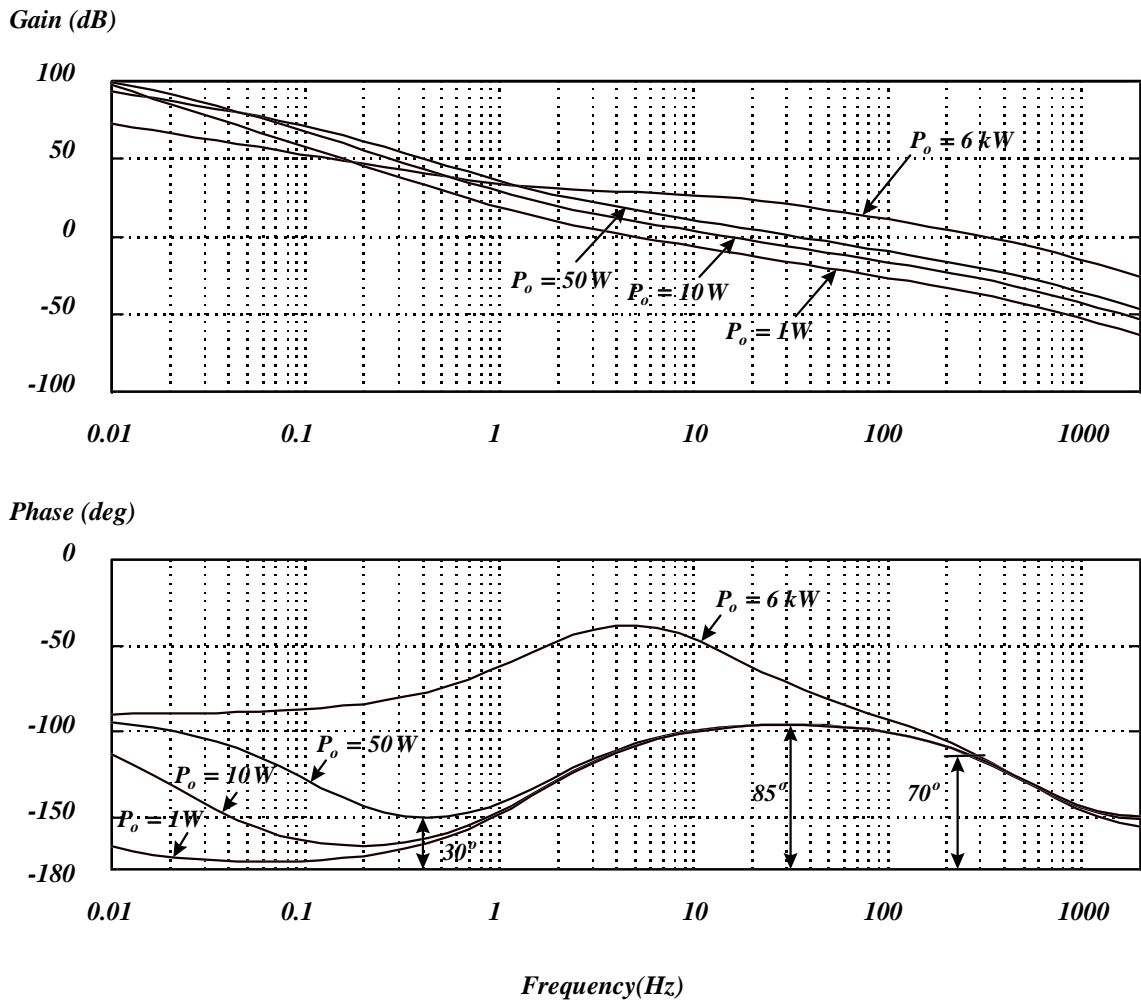


Fig. 4.13. Loop gains at 6 kW, 50 W, 10 W, and 1 W with compensator in Eq. (4.20)

$$G_{c2} = 80 \frac{1 + s/10}{s(1 + s/3500)}. \quad (4.20)$$

In Fig. 4.13, four loop gains, obtained with this compensator at 6 kW, 50 W, 10 W, and 1 W, are plotted. Now, at full load, the phase margin is 70° , but the gain at 0.01 Hz reduces to 75 dB . At the 50-W load, the minimum phase margin is boosted up to 30° . However, for 10-W and 1-W loads, the minimum phase margins are still very low.

To increase the minimum phase margin at light load, the zero is further moved close to the origin. If $Z_c=1 \text{ rad/sec}$ and $K_c=8$ are selected, the compensator is:

$$G_{c3} = 8 \frac{1 + s}{s(1 + s/3500)} \quad (4.21)$$

In Fig. 4.14, four loop gains, obtained with this compensator at 6 kW, 50 W, 10 W, and 1 W, are plotted. Now, at full load, the phase margin is 65° , but the gain at 0.01 Hz reduces to 50 dB . For the 10-W load, the minimum phase margin is boosted up to 30° , but for the 1-W load, the minimum phase margin is very low (around 10°).

The above discussions show that unless the zero is designed to lie at the origin (or the integrator is removed), there always exist low-phase-margin cases if the compensator in Eq. (4.18) is used. On the other hand, to place the zero too close to the origin will reduce the loop gain at full load, yielding a high steady-state error and degrading a low system dynamic response. Hence, to avoid the very light load operation, a dummy load is necessary. In the design, a 50-W (around 1% of full load) dummy load is selected. With this dummy load, the compensator design objective becomes:

- Control bandwidth: $< 360 \text{ Hz}$;
- Phase margin from full load (6 kW) to light load (50 W): $\geq 45^\circ$;
- Minimum phase margin from full load (6 kW) to light load (50 W): $\geq 30^\circ$.

According to the above discussions, the compensator in Eq. (4.20) can be used to meet this objective.

With the compensator in Eq. (4.20), the control circuit parameters are calculated as: $C_1 = 5780 \text{ pF}$, $C_2 = 2.02 \text{ }\mu\text{F}$, $R_4 = 49.5 \text{ k}\Omega$. The selected values are: $C_1 = 5600 \text{ pF}$, $C_2 = 2.0 \text{ }\mu\text{F}$, $R_3 = 10 \text{ k}\Omega$, $R_4 = 51 \text{ k}\Omega$, $R_5 = 1 \text{ k}\Omega$, $R_6 = 620 \text{ }\Omega$. The voltage compensator is implemented in Fig. 4.15.

The loop gains with the designed compensator were also measured at a heavy load (4.8 kW) and a light load (54 W). The measurement set-up is shown in Fig. 4.16. A $50 \text{ }\Omega$ resistor is used to match the signal generator output impedance. In Figs. 4.17 and 4.18, the measured loop gains are provided along with the derived one. It is shown that both magnitude and phase agree very well. In the results, the glitches are also visible at 60 Hz and 120 Hz, which are caused by 60-Hz line interference. The visible glitch at 360 Hz is caused by the rectifier output voltage ripple.

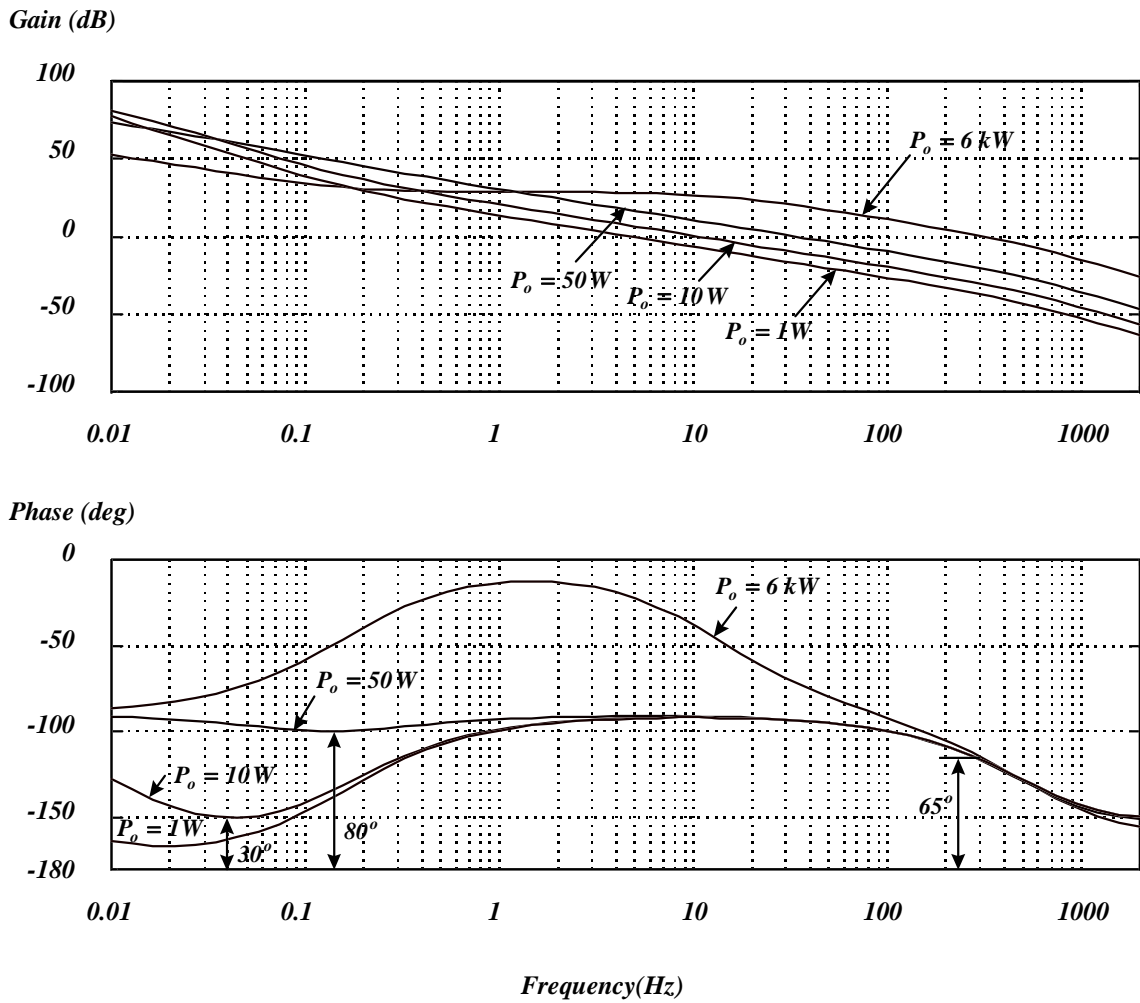


Fig. 4.14. Loop gains at 6 kW, 50 W, 10 W, and 1 W with compensator in Eq. (4.21)

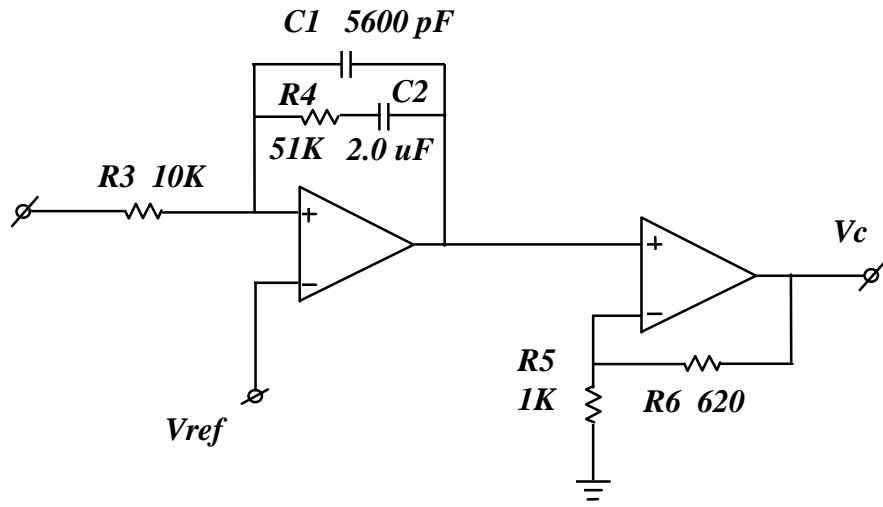


Fig. 4.15. The circuit of voltage compensator

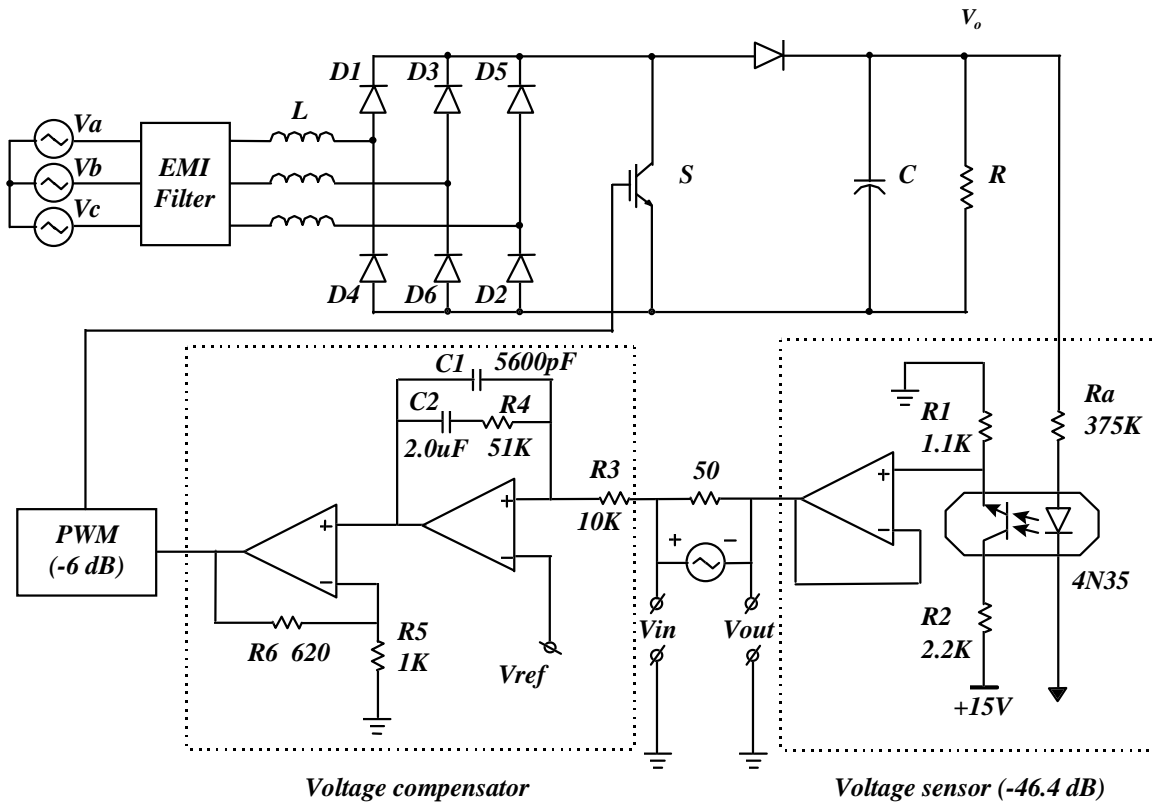
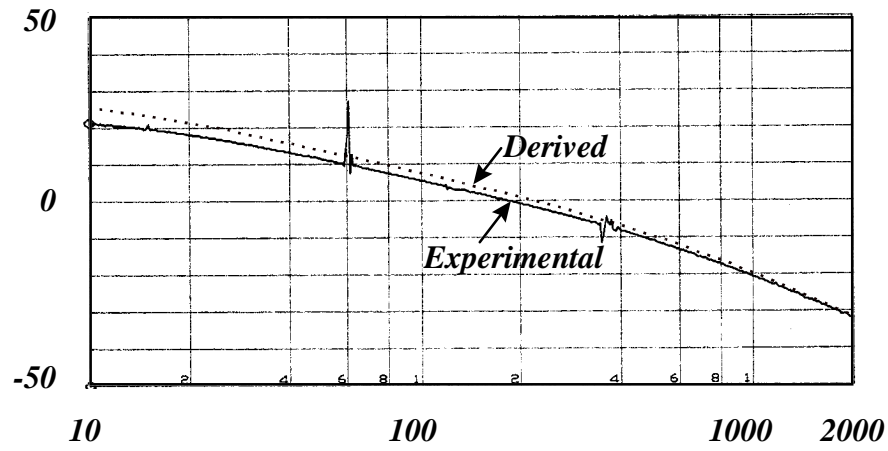


Fig. 4.16. Set-up of loop gain measurement

Magnitude (dB)



Phase (deg)

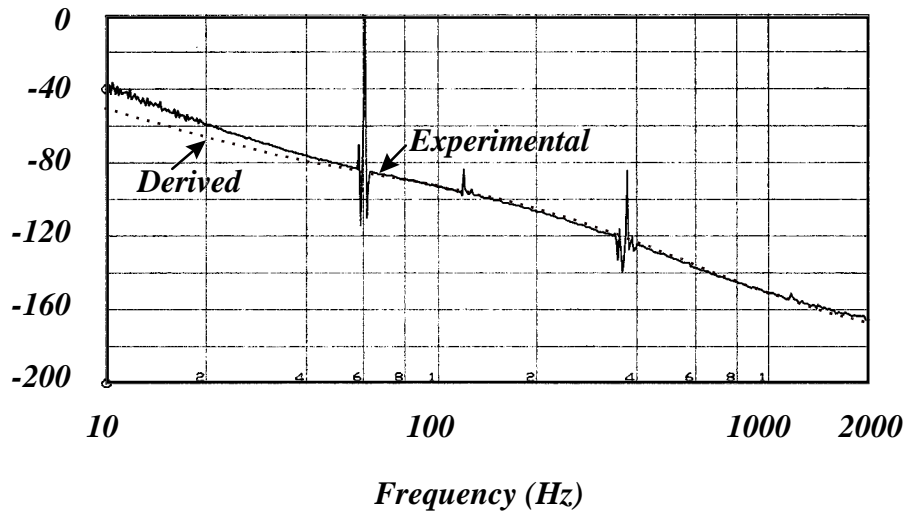
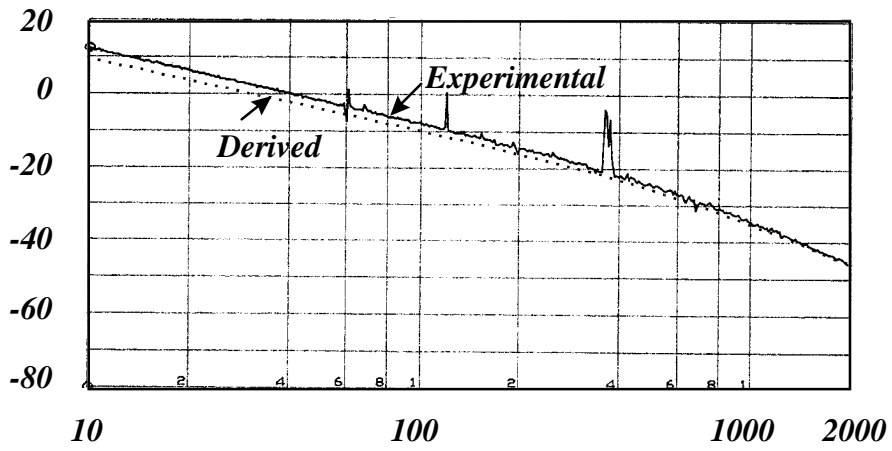


Fig. 4.17. Derived and experimental loop gains at a heavy load (4.8 kW)

Magnitude (dB)



Phase (deg)

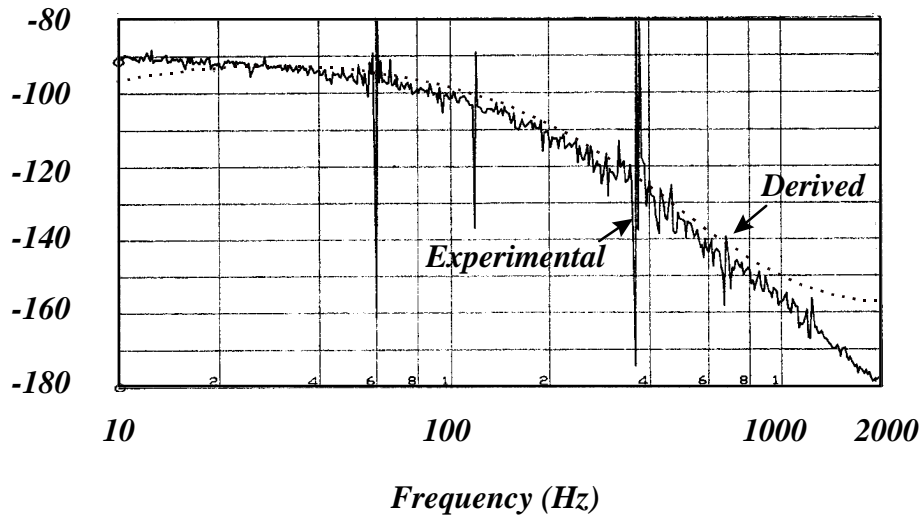


Fig. 4.18. Derived and experimental loop gains at light load (54 W)

4.5. Nonlinear Control

As shown in the last section, to stabilize the system at light load with a linear voltage controller, a dummy load is necessary. To reduce the dummy load by moving the zero closer to the origin will degrade the performance at full load. Hence, the dummy load cannot be too small. This results in a low efficiency. A simple way to improve the efficiency is to remove the dummy load at full load. However, this method needs an extra high voltage switch and its control circuit, yielding extra cost. If the dummy load can be decreased by modifying the controller, the cost and size can be reduced. A straightforward solution to modify the controller is to adopt a nonlinear controller.

There are a lot of nonlinear control schemes. Most of them use load current feedback and very complex [18-20]. In order to reduce the cost and simplify the design, simple nonlinear controllers are preferred. In this section, a nonlinear gain controller, which is very simple and inexpensive, is introduced to reduce the dummy load.

With the compensator in Eq. (4.20), the phase margin of the system becomes the minimum 30° when the load is 50 W. If the load is lighter, this phase margin is less than 30° and cannot meet the design requirement. A simple way to boost the minimum phase margin up at light load is to limit the loop gain. In Fig. 4.19, the loop gain for the 10-W load is plotted. It is shown that if this loop gain is reduced by 80 dB , the phase margin will be 30° and can meet the design requirement. Therefore, with the same pole and zero, the dummy load can be reduced from 50 W to 10 W. This is the principle of the nonlinear gain control.

4.5.1. Continuous Gain Control

In the implementation, the 80-dB gain attenuation is obtained using a nonlinear gain block, which consists of two voltage references and four diodes (1N4148) and is connected between the compensator output and PWM chip input, as shown in Fig. 4.20.

Without the nonlinear gain block, the control voltage V_c' is equal to the compensator output V_c . The relationship between V_c' and V_c is linear, as shown in Fig. 4.21. From full load to no load, the voltages V_c' and V_c vary from A (3.05 V) to B (2.25 V). Since $V_c' = V_c$, the corresponding ac-gain $\Delta V_c' / \Delta V_c$ is unity. So, the attenuation is 0 dB.

Because of the nonlinear characteristics of the diodes, the input V_c in the nonlinear gain block is changed from 6.3 V to -15 V in order to provide the same control voltage V_c' (3.05 V to 2.25 V) for the PWM chip from full load to no load. Hence, the relationship between V_c' and V_c becomes nonlinear, as shown in the curve CDEFG in Fig. 4.21. From $\Delta V_c' / \Delta V_c$, the ac-gains of the nonlinear gain block are calculated and presented in Fig. 4.22. When the converter operates from 6 kW to 1.5 kW, the ac-gain is

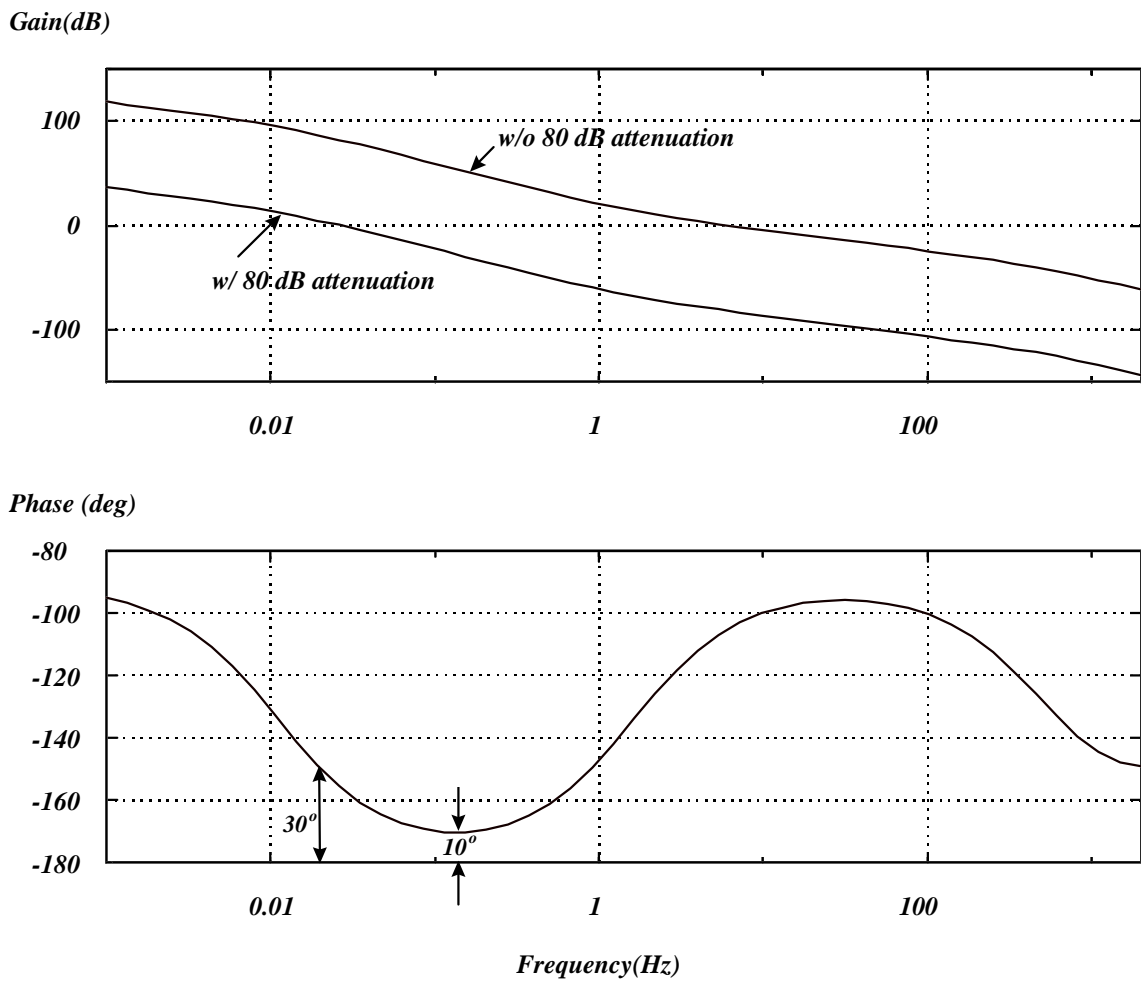


Fig. 4.19. Loop gains at 10 W with and without 80-dB attenuation

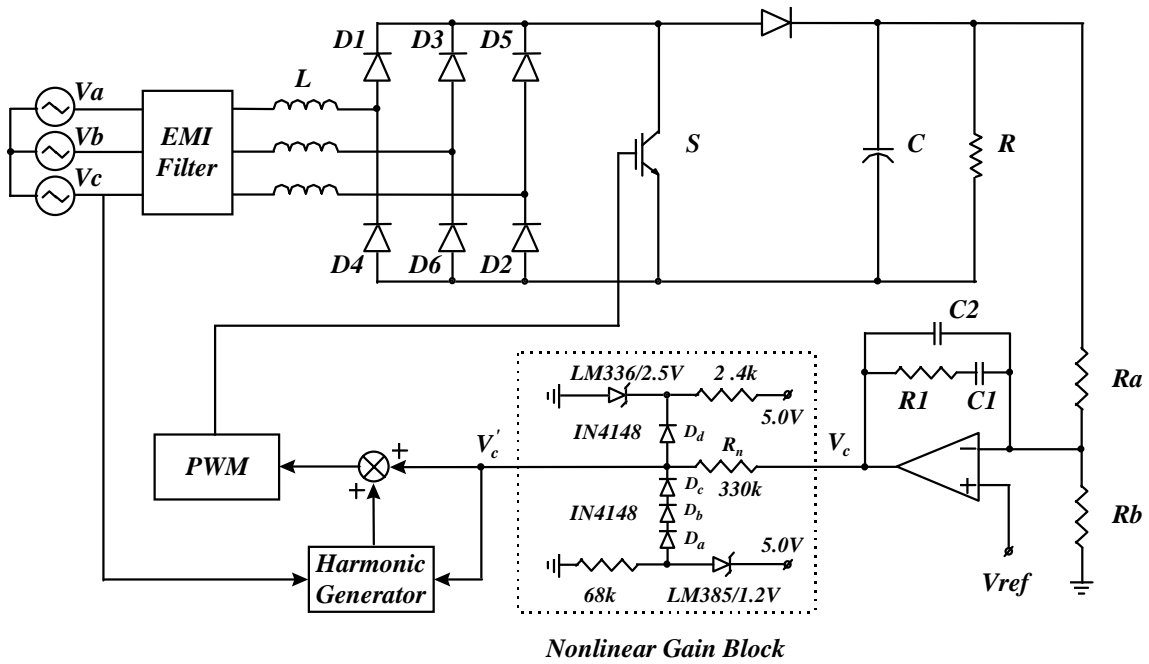


Fig. 4.20. The system diagram with a nonlinear gain block

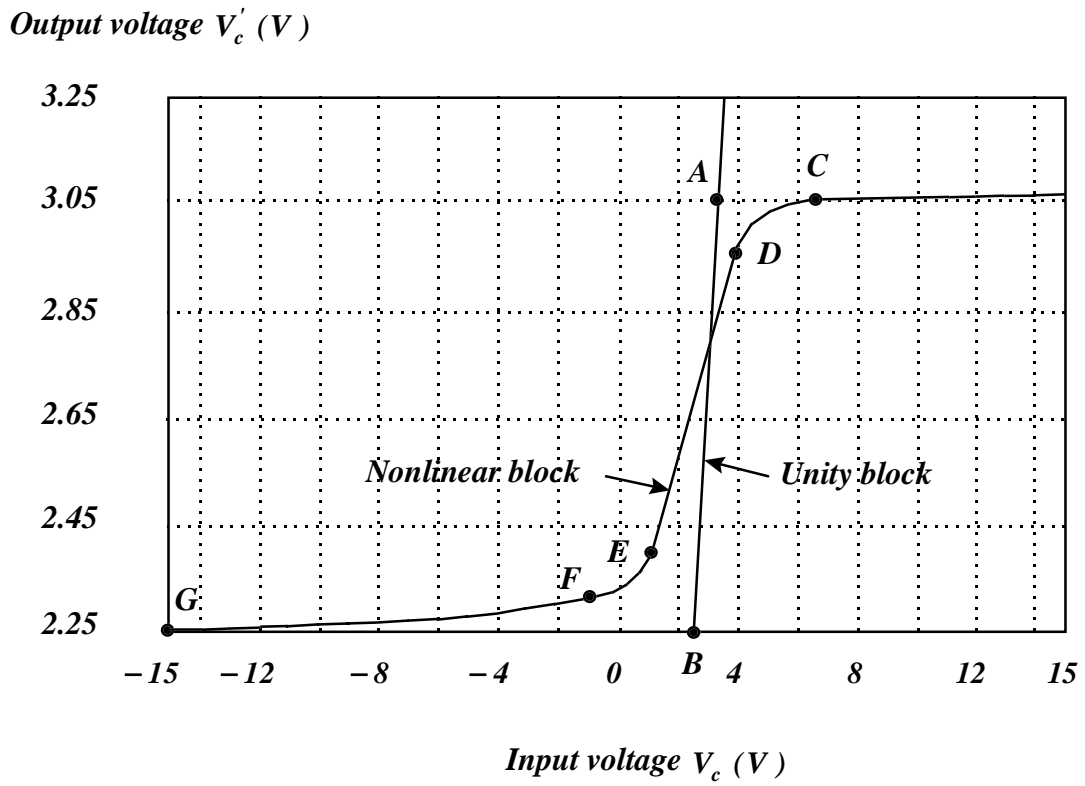


Fig. 4.21. Input-output characteristics of nonlinear gain block

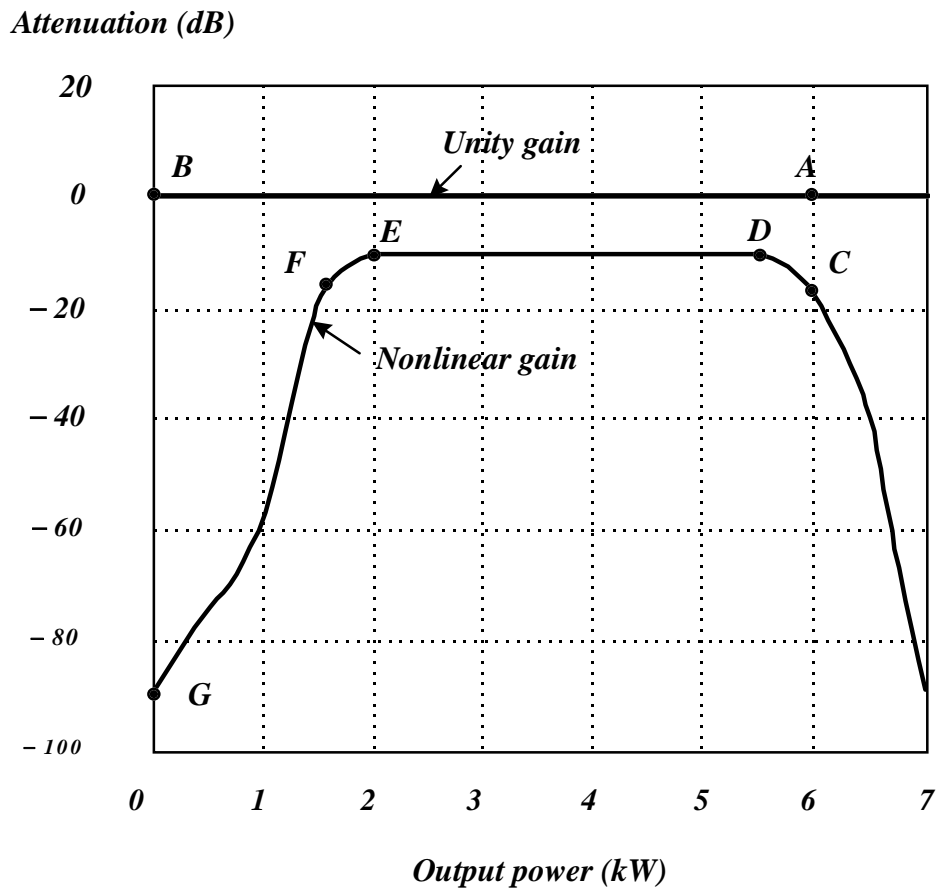


Fig. 4.22. The attenuation (ac-gain) of nonlinear gain block with respect to output power

around -12 dB. When the output power is less than 300 W, the ac-gain is less than -90 dB, which meets the required attenuation.

The operation principle of the nonlinear gain block is further detailed in Table 4.2. When $V_c \geq 6.3V$, the output voltage is clamped at 3.05 V by diode D_d , and all other diodes D_a , D_b , and D_c , are off. When $4V \leq V_c \leq 6.3V$, D_d operates in the nonlinear region and the output voltage is determined by diode D_d and resistor R_n . When $1V \leq V_c \leq 4V$, all diodes are off and the output voltage is almost determined by the input voltage. When $-1V \leq V_c \leq 1V$, D_a , D_b , and D_c operate in the nonlinear region and the output voltage is determined by the diodes D_a , D_b , D_c and resistor R_n . When $-15V \leq V_c \leq 1V$, the output voltage is clamped between 2.30 V to 2.25 V by diodes D_a , D_b , and D_c , and diode D_d is off. The characteristics of each diode are shown in Fig. 4.23. When $V_c = -15V$, $V_c' = 2.25V$, and the voltage drop across D_a , D_b , and D_c is 1.55 V. Then the current through D_a , D_b , and D_c is 0.04 mA. So, the resistor R_n is:

$$R_n = \frac{V_c' - V_c}{I_F} = \frac{17.25}{0.04 \times 10^{-3}} = 345 k\Omega.$$

R_n is selected as $330 k\Omega$.

Since the 12-dB gain attenuation caused by the nonlinear gain block should be compensated at the full load, the voltage compensator in Eq. (4.20) is modified as:

$$G_c = 320 \frac{1 + s/10}{s(1 + s/3500)}. \quad (4.22)$$

Therefore, the control circuit parameters are calculated as: $C_1 = 1446 pF$, $C_2 = 0.5 \mu F$, $R_4 = 198 k\Omega$. The selected values are: $C_1 = 1500 pF$, $C_2 = 0.47 \mu F$, $R_3 = 10 k\Omega$, $R_4 = 200 k\Omega$, $R_5 = 1 k\Omega$, $R_6 = 620 \Omega$. The modified voltage compensator is shown in Fig. 4.24.

The loop gains with this compensator were also measured at a heavy load (4.8 kW) and the light load (10 W). The measurement set-up is the same, as shown in Fig. 4.16. In Figs. 4.25 and 4.26, the measured loop gains are provided, along with the derived one. It is shown that both magnitude and phase agree very well.

4.5.2. Step Gain Control

The nonlinear gain control in Fig. 4.20 is a very simple and inexpensive method to meet the required gain attenuation. However, in the design, the gain attenuation is very sensitive to the parameters of the diodes. This is a disadvantage of this implementation. Another implementation, which is more precise, is to adopt a step-gain attenuation block.

In Fig. 4.27, on the basic voltage compensator, one resistor R32 ($200 M\Omega$), one switch, and its control circuit are added. The switch's on or off is controlled by the load current. When the load is heavy ($\geq 300W$), the load current is higher than the reference, and the switch is on. Then the compensator gain is determined by the resistor R31

Table 4.2. The input-output characteristics of nonlinear gain block related to diode operating points

<i>Input V_c</i>	D_a	D_b	D_c	D_d	<i>Output V'_c</i>
$\geq 6.3V$	<i>off</i>	<i>off</i>	<i>off</i>	<i>clamp (0.5 V)</i>	$3.05V$
$4V \leq V_c \leq 6.3$	<i>off</i>	<i>off</i>	<i>off</i>	<i>nonlinear</i>	$2.9V \leq V'_c \leq 3.05V$
$1V \leq V_c \leq 4V$	<i>off</i>	<i>off</i>	<i>off</i>	<i>off</i>	$2.4V \leq V'_c \leq 2.9V$
$-1V \leq V_c \leq 1V$	<i>nonlinear</i>	<i>nonlinear</i>	<i>nonlinear</i>	<i>off</i>	$2.3V \leq V'_c \leq 2.4V$
$-15V \leq V_c \leq -1V$	<i>clamp (0.5 V)</i>	<i>clamp (0.5 V)</i>	<i>clamp (0.5 V)</i>	<i>off</i>	$2.25V \leq V'_c \leq 2.3V$

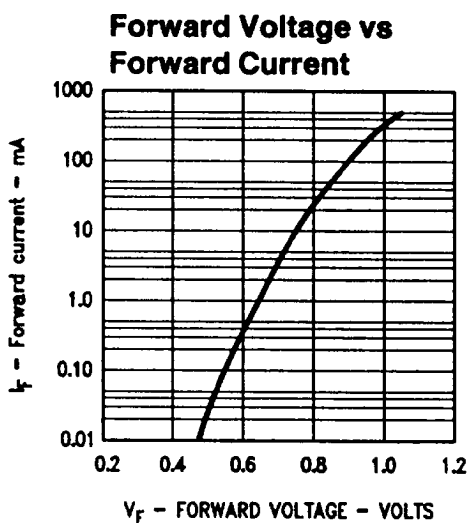


Fig. 4.23. Diode 1N4148 characteristics

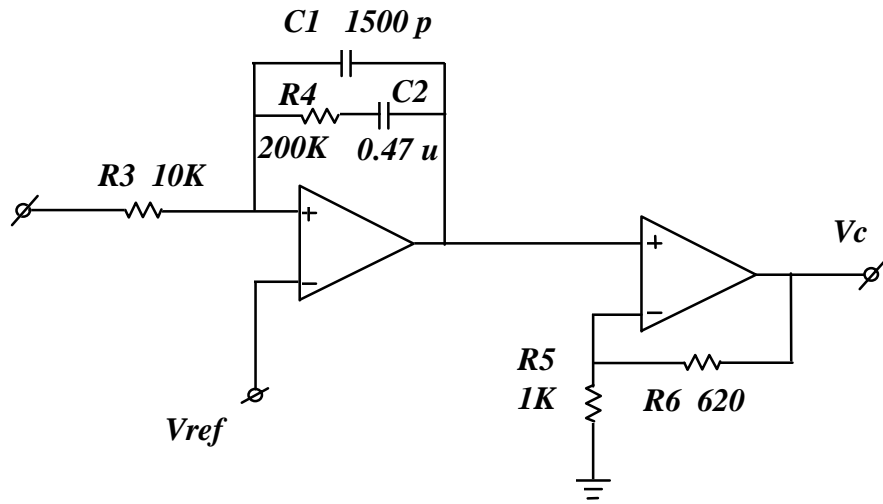
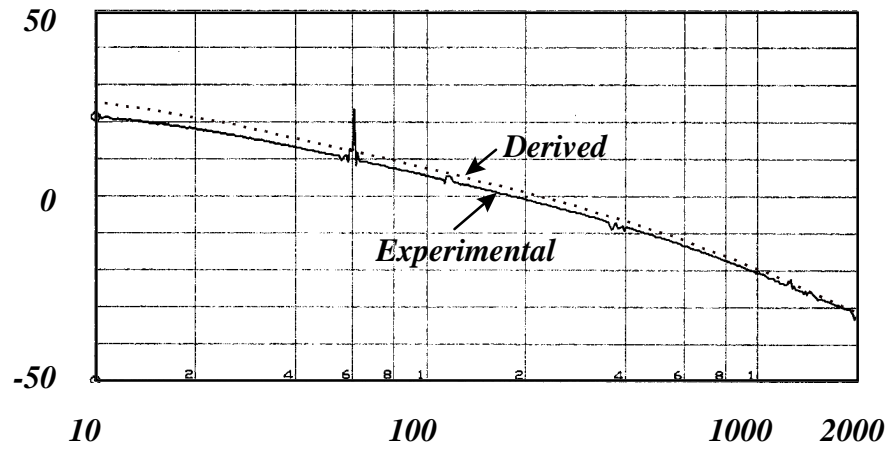


Fig. 4.24. The modified voltage compensator for nonlinear gain control

Magnitude (dB)



Phase (deg)

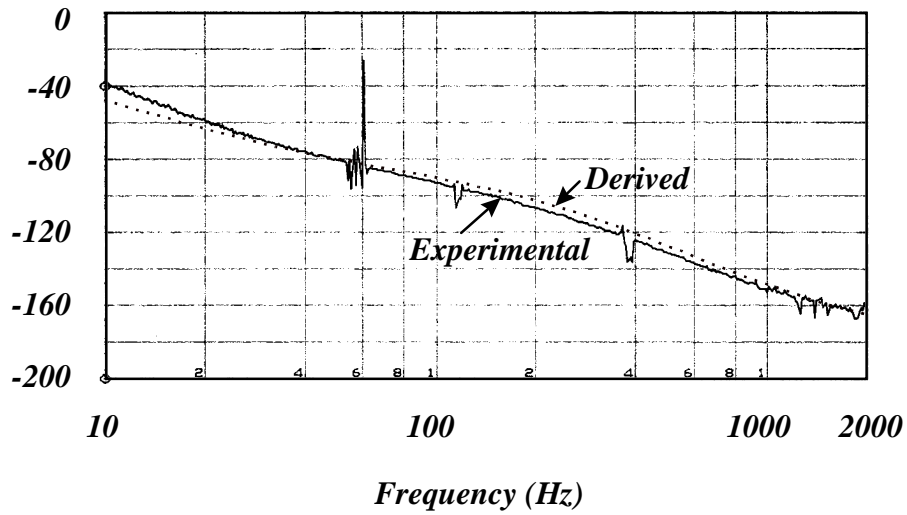
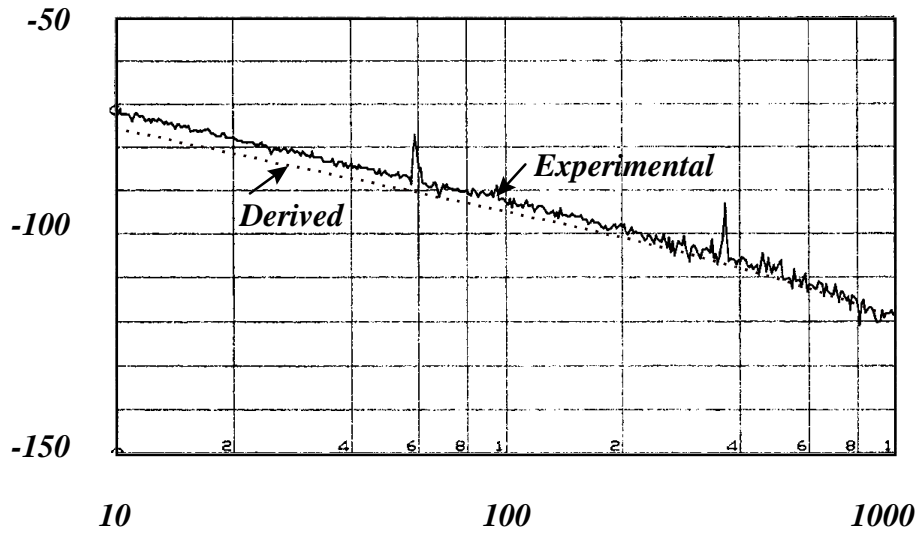


Fig. 4.25. Derived and experimental loop gains at a heavy load (4.8 kW) with nonlinear gain control

Magnitude (dB)



Phase (deg)

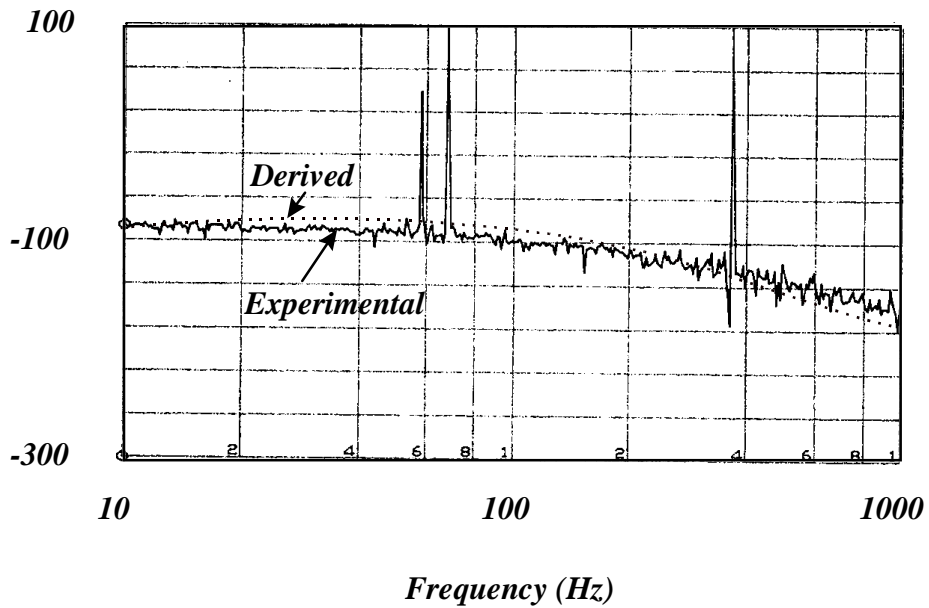


Fig. 4.26. Derived and experimental loop gains at light load (10 W) with nonlinear gain control

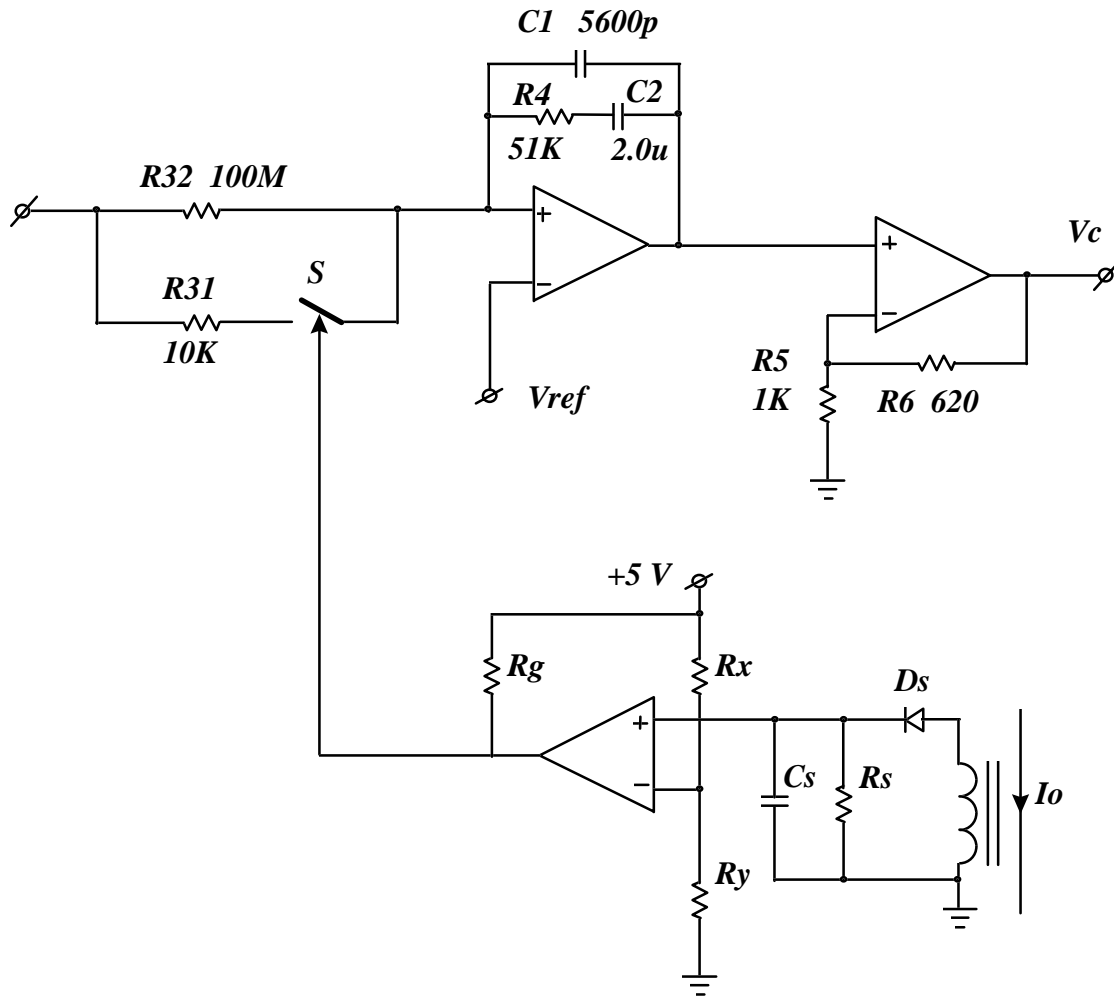


Fig. 4.27. The circuit of step-gain control

($20\text{ K}\Omega$) and the function in Eq. (4.22) is obtained. When the load is light (300 W to 10 W), the load current is lower than the reference, and the switch is off. Then the compensator gain is determined by resistor R32 ($200\text{ M}\Omega$) and a 80-dB gain attenuation is obtained. Compared with the nonlinear gain block shown in Fig. 4.20, the step-gain control is a little more complex.

4.5.3. Moving Zero (Pole) Control

The most serious concerns in the compensator design for the single-switch three-phase boost rectifier are the dynamic response at heavy load and the stability at light load. With a linear controller, the improvement of the dynamic response and the minimization of the dummy load are contradictory because the dominant pole in the plant is a moving pole. However, if the compensator can provide a moving zero to compensate for this moving pole, the system performance can be improved at both full load and light load. Hence, another kind of nonlinear control is the moving zero control. The strategy of this control method is: at heavy loads, in order to boost the loop gain up, the control is designed with a high-frequency zero; at light loads, to stabilize the system, the control is designed with a low-frequency zero. For example, from 6 kW to 1.5 kW , the compensator is designed as:

$$G_{c_heavy\ load} = 2800 \frac{1 + s / 350}{s(1 + s / 3500)}, \quad (4.23)$$

and from 1.5 kW to 10 W , the compensator is designed as:

$$G_{c_light\ load} = \frac{1 + s}{s(1 + s / 10)}. \quad (4.24)$$

In Figs. 4.28 and 4.29, the loop gains of the designed rectifier with the above two compensators are plotted. The results show that at full load, the loop gain at 0.01 Hz is 100 dB . At the 10-W load, the minimum phase margin is 30 and the crossover frequency is 3 Hz , which is much higher than in the case with the nonlinear gain control.

The moving zero control is implemented in Fig. 4.30. Based on the voltage compensator, two resistors R32 ($30\text{ M}\Omega$) and R42 ($20\text{ M}\Omega$), two switches S1 and S2, and their control circuit are added. The switch's on or off is controlled by the load current. At a heavy load ($\geq 1.5\text{ kW}$), the load current is higher than the reference and the switch is on. Then the compensator is determined by the resistors R31 ($20\text{ K}\Omega$) and R41 ($56\text{ K}\Omega$), and the function in Eq. (4.22) is obtained. At a light load (1.5 kW to 10 W), the load current is lower than the reference and the switch is off. Then the compensator is determined by the resistors R32 and R42, and the function in Eq. (4.23) is obtained. Due to the time limit, the step-gain control and moving-zero (pole) control have not been completed. These will be the subject of future work.

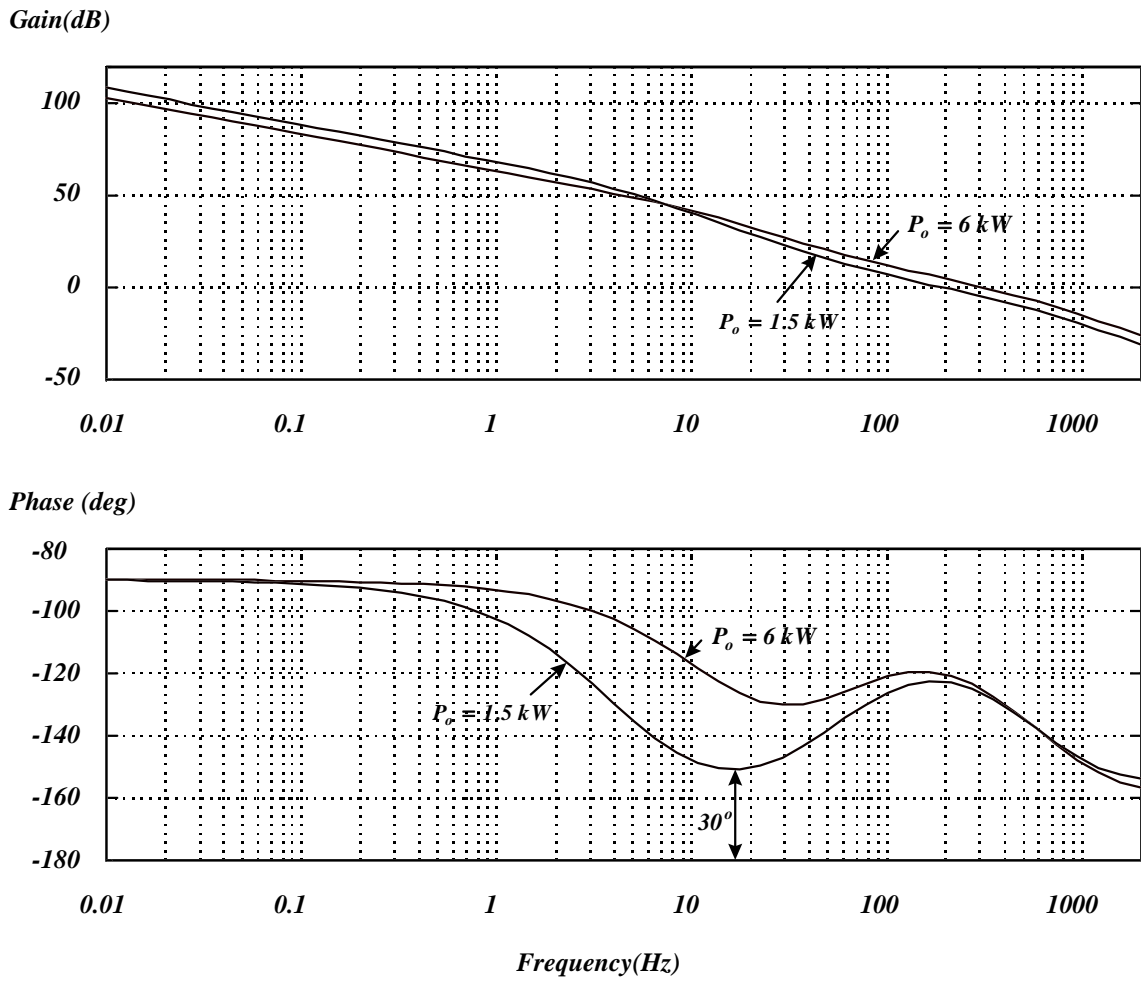


Fig. 4.28. Loop gains at 6 kW and 1.5 kW with compensator in Eq. (4.23)

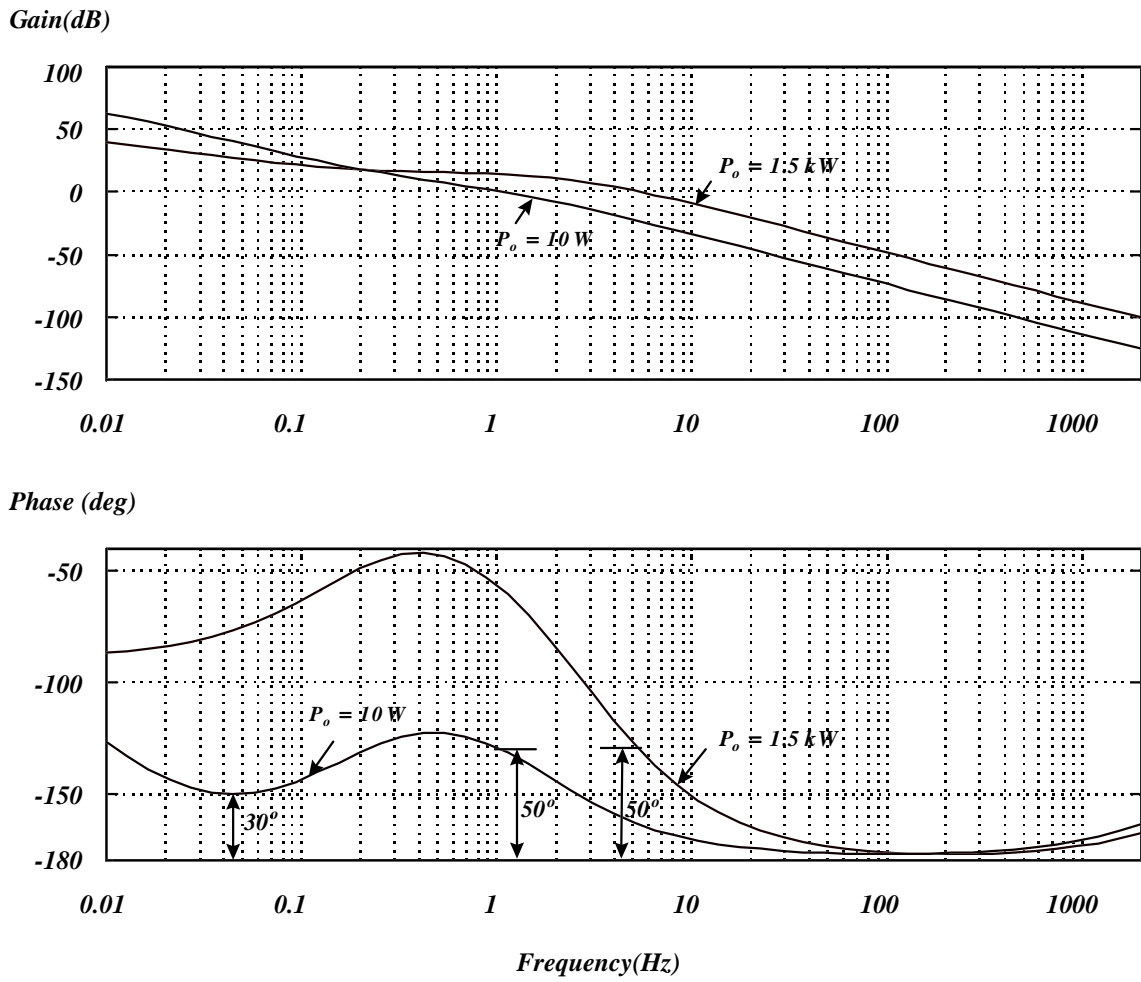


Fig. 4.29. Loop gains at 1.5 kW and 10 W with compensator in Eq. (4.24)

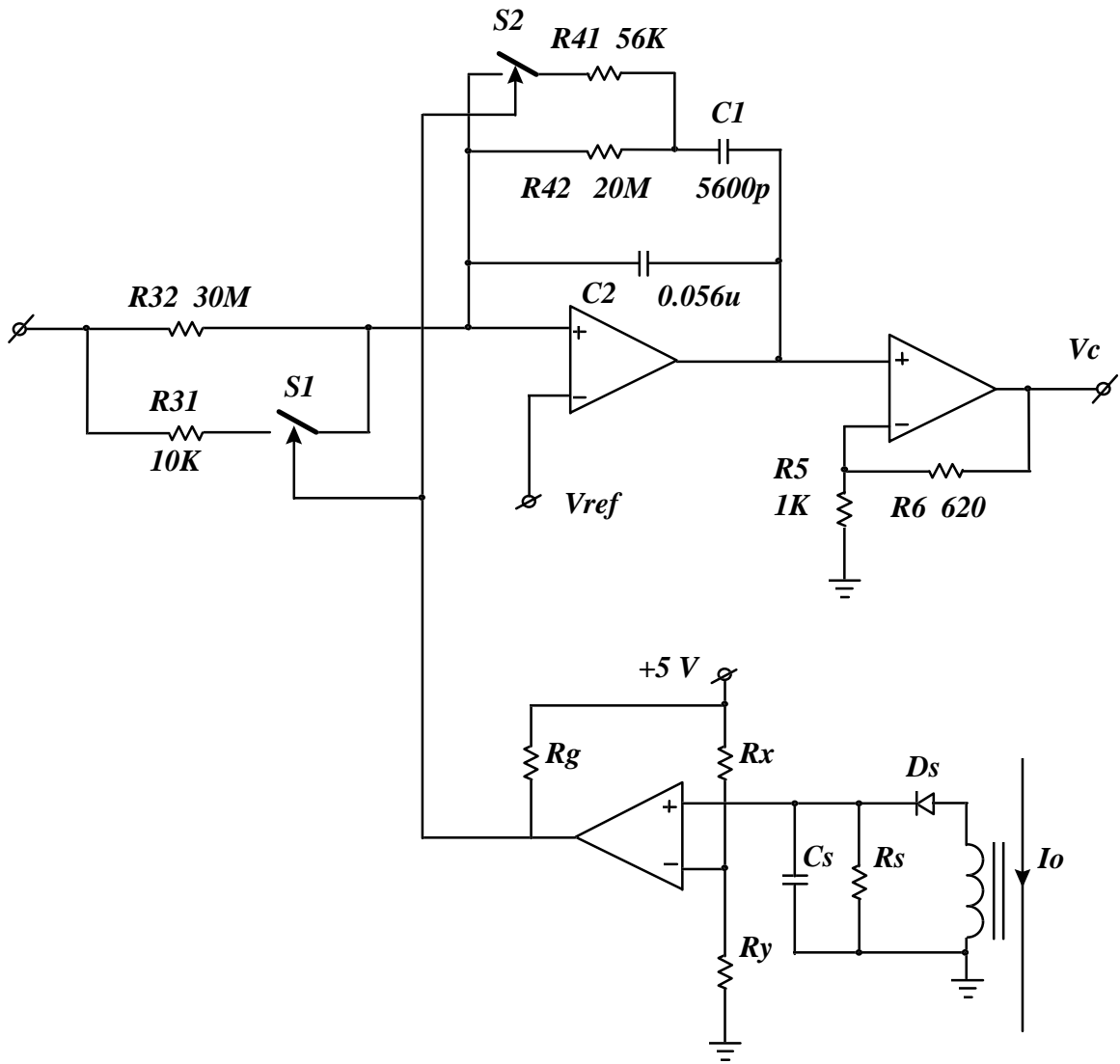


Fig. 4.30. Implementation of moving zero (pole) control

5. Conclusions

The harmonic injection concept was proposed [9] to reduce the line-current harmonics by modulating the converter dc-side currents at a harmonic frequency and then injecting the modulated currents back into the ac-side. So several magnetic components operating at low frequency and high voltage/current stress were required. The proposed approach, sixth-order harmonic injected PWM, simply realizes the injection concept at the control circuit so that the cost of the power stage is reduced. By using harmonic injected PWM, the THD in a single-switch rectifier is improved, especially for lower M values. From the results of analysis, simulation, and experiment, it can be concluded that:

- 1) To meet the THD<10% requirement, the rectifier voltage gain can be designed down to 1.45. So, an application with a 3x220-V_{rms}-input/800-V output becomes practical;
- 2) To meet the IEC 1000-3-2 (class A) standard, the output power can be pushed up to around 10-kW level for the rectifier with a 3x220-V_{rms}-input/800-V output;
- 3) Owing to constant switching frequency and load-independent harmonic injection, it is easy to design the power stage, the control circuit, and the EMI filter.

Unlike in a single phase rectifier, in which the current harmonics can be dramatically suppressed or even eliminated by using the duty cycle modulation, the harmonic reduction in the three-phase rectifier is restrictive. Because of only one switch connected on the rectifier dc-side, it is impossible to balance three phase currents whose distortions are in different directions. As shown in Fig. 3.2, at almost all time intervals, any attempt to improve the distortions in two phases entails the penalty of increasing distortion in the third phase. So the THD improvement is an optimization problem. The proposed sixth-order harmonic injected PWM is a reasonable attempt at a search for this optimum PWM scheme.

Due to the DCM operation, the small-signal model of the single-switch three-phase boost rectifier behaves as a first-order system, which depends on a dominant pole. However, this dominant pole is greatly load-dependent. At no load, this pole approaches the origin and results in more phase delay, making the compensator design difficult. Hence, to avoid the converter operating at no load, a dummy load is added on the converter output. Then, a nonlinear gain control circuit is presented to mitigate the load effect and to minimize the dummy load.

Future work includes searching for an optimum PWM scheme which can be easily implemented, compensating for the phase shift at the fifth-order frequency caused by EMI filter, and using a moving-zero controller to compensate for the load effect on the dominant pole and to improve the control bandwidth. This work has not been completed because of time constraints.

6. Appendix

6.1. Three-Phase Currents with Harmonic-Injected PWM

The derivation is carried out on the phase A current first. Since the magnitudes I_1 and I_5 are linearly proportional to the square of the duty cycle, the phase A current in Eq. (3.2) can be rewritten as

$$i_a = C_1 D^2 \sin \omega t + C_5 D^2 \sin(5\omega t + \pi), \quad (\text{A-1})$$

where C_1 and C_5 , which are constant, are the functions of V_o , L , and f as shown in Eq. (2.2). Substituting the duty cycle D in Eq. (A-1) with the modulated duty cycle defined in Eq. (3.1), the phase A current becomes

$$\begin{aligned} i_a' &= C_1 [D(1 + m \sin(6\omega t + \frac{3\pi}{2}))]^2 \sin \omega t + \\ &+ C_5 [D(1 + m \sin(6\omega t + \frac{3\pi}{2}))]^2 \sin(5\omega t + \pi). \end{aligned} \quad (\text{A-2})$$

If the presence of m^2 ($m^2 \ll 1$) terms are ignored, the above equation can be simplified as

$$\begin{aligned} i_a' &= I_1 [1 + 2m \sin(6\omega t + \frac{3\pi}{2})] \sin \omega t + \\ &+ I_5 [1 + 2m \sin(6\omega t + \frac{3\pi}{2})] \sin(5\omega t + \pi) \\ &= I_1 \sin(\omega t) + 2m \sin(6\omega t + \frac{3\pi}{2}) \sin \omega t + \\ &+ I_5 \sin(5\omega t + \pi) + 2m I_5 \sin(6\omega t + \frac{3\pi}{2}) \sin(5\omega t + \pi) \\ &= I_1 \sin(\omega t) - m I_1 \sin(5\omega t + \pi) - m I_1 \sin(7\omega t) \\ &+ I_5 \sin(5\omega t + \pi) - m I_5 \sin(\omega t) + m I_5 \sin(11\omega t). \end{aligned} \quad (\text{A-3})$$

Since $m I_5 \ll I_1$, and if the high-order harmonics ($n > 7$) is ignored, Eq. (A-3) becomes

$$i_a' = I_1 \sin \omega t + (I_5 - m I_1) \sin(5\omega t + \pi) - m I_1 \sin 7\omega t. \quad (\text{A-4})$$

For phase B and C currents, the same results can be obtained. Hence, the three-phase currents with harmonic-injected PWM are

$$\begin{aligned} i_a' &= I_1 \sin \omega t + (I_5 - m I_1) \sin(5\omega t + \pi) - m I_1 \sin 7\omega t, \\ i_b' &= I_1 \sin(\omega t - \frac{2\pi}{3}) + (I_5 - m I_1) \sin(5\omega t - \frac{\pi}{3}) - m I_1 \sin(7\omega t - \frac{2\pi}{3}), \\ i_c' &= I_1 \sin(\omega t - \frac{4\pi}{3}) + (I_5 - m I_1) \sin(5\omega t + \frac{\pi}{3}) - m I_1 \sin(7\omega t - \frac{4\pi}{3}). \end{aligned} \quad (\text{A-5})$$

6.2. A Simple Method of Steady-State Analysis of PWM Converters

The steady-state analysis of PWM converters is the basis of the analysis and design. Here, a simple method [21] for steady-state analysis is introduced based on a DC/DC boost converter as shown in Fig. A-1. Generally, this method can be extended to other type converters, including DC/AC and AC/DC converters.

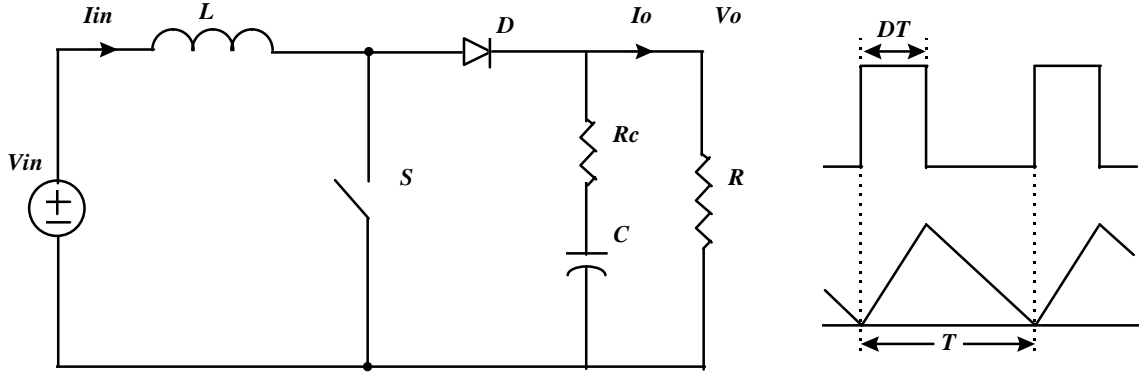


Fig. A-1. A DC/DC boost converter and its current waveform

At first, some nomenclatures are defined: the *critical power* P_c is load power when the converter operates in conduction boundary between CCM and DCM; the *delivered power* P is power delivered by the converter from source to load; and d is the duty cycle in both CCM and DCM. Therefore, the critical power can be derived according to its inductor current waveform. At the boundary operation, the average inductor current is given by

$$I_{in} = \frac{1}{2} i_p = \frac{1}{2} \frac{V_{in}}{L} DT, \quad (\text{A-6})$$

where i_p is peak inductor current, D duty cycle in CCM, f switching frequency and $T = 1/f$. Since it is still in CCM, the voltages and currents in input and output are related by

$$V_{in} = (1-D)V_o \quad \text{and} \quad I_{in} = \frac{1}{1-D} I_o. \quad (\text{A-7})$$

Substituting Eq. (A-7) into (A-6), the load current can be found. Thus, the critical power is obtained

$$P_c = V_o I_o = \frac{V_o^2}{2Lf} D(1-D)^2. \quad (\text{A-8})$$

Comparing the delivered power $P = V_o^2 / R$ to the critical power in Eq. (A-8), the steady-state can be obtained. On the one hand, if P is larger than P_c , the converter operates in CCM. The duty cycle is load independent and given by

$$d = D. \quad (\text{A-9})$$

On the other hand, if P is less than P_c , the converter operates in DCM, and the duty cycle is load-dependent. For constant output voltage, the voltage gain in DCM (referred to Table A-1) should be regulated to be equal to that in CCM, i.e.:

$$\frac{V_o}{V_{in}} = \frac{1 + \sqrt{1 + 2d^2 R / Lf}}{2} = \frac{1}{1 - D}. \quad (\text{A-10})$$

Figuring out d and simplifying the expression by using P and P_c , the duty cycle can be represented as

$$d = \sqrt{\frac{P}{P_c}} D. \quad (\text{A-11})$$

So, from heavy load to no load, the steady-state is given by Eq. (A-9) or (A-11). Summarizing the above discuss yields a method for steady-state analysis of a DC/DC boost converter:

For a designed PWM converter, if the delivered power P is larger than P_c , then the converter operates in CCM and the duty cycle is given by Eq. (A-9). Otherwise, the converter operates in DCM and the duty cycle is given by Eq. (A-11).

It can be proved that the above method still holds for buck-type and flyback-type converters. The difference is that the critical power in Eq. (A-8) should be replaced by those listed in Table A-1.

In AC/DC PFC converters or DC/AC inverters, the above method still can be used, even though the duty cycle D , critical power, and delivered power are functions of the instant of the sinusoidal input voltages. This is because, at a fixed ωt , these variables can be considered as constant and the method can be applied just as on a DC/DC converter. The most important thing is to find out proper representations of these variables.

Table A-1. Critical power and voltage gains for general type PWM converters

	<i>Boost-Type</i>	<i>Buck-Type</i>	<i>Flyback-Type</i>
<i>Critical Power</i>	$\frac{V_o^2}{2Lf} D(1-D)^2$	$\frac{V_o^2}{2Lf} (1-D)$	$\frac{V_o^2}{2Lf} (1-D)^2$
<i>Voltage Gain (CCM)</i>	$\frac{1}{1-D}$	D	$\frac{D}{1-D}$
<i>Voltage Gain (DCM)</i>	$\frac{1 + \sqrt{1 + 2d^2 R / Lf}}{2}$	$\frac{2}{1 + \sqrt{1 + 8Lf / d^2 R}}$	$\sqrt{\frac{R}{2Lf}} d$

6.3. A MATHCAD Code for EMI Filter Design (A=70dB)

$$n = 5 \quad A_{min} = 70 \quad p = \frac{50}{100} \quad A_{max} = 1.25 \quad C_{max} = 15\mu F$$

$$\Omega_s = 2$$

$$C_1 = 1.0968$$

$$C_2 = 0.0703 \quad L_2 = 1.3461$$

$$C_3 = 1.883$$

$$C_4 = 0.171 \quad L_4 = 1.34$$

$$C_5 = 1.5804$$

$$f_{sw} = 45\text{kHz}$$

$$\omega_r = 0.82 \times 2 \times \pi \times \frac{f_{sw}}{\Omega_s} = 1.131e5$$

$$R_d = \frac{C_1 + C_3 + C_5}{\omega_r C_{max}} = 2.668$$

$$C_{d1} = \frac{C_1}{\omega_r R_d} = 3.608e-6$$

$$C_{d2} = \frac{C_2}{\omega_r R_d} = 2.312e-7 \quad L_{d2} = L_2 \frac{R_d}{\omega_r} = 3.199e-5$$

$$C_{d3} = \frac{C_3}{\omega_r R_d} = 6.194e-6$$

$$C_{d4} = \frac{C_4}{\omega_r R_d} = 5.625e-7 \quad L_{d4} = L_4 \frac{R_d}{\omega_r} = 3.185e-5$$

$$C_{d5} = \frac{C_5}{\omega_r R_d} = 5.198e-6$$

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