voltages in a one cycle Fourier transform to find the fundamental phasors. The zero sequence voltage, (or, more precisely, $3E_0$) is the sum of the three line voltages

Two torque equations are used to determine if the fault is in the operating direction. For current polarization, the equation is $T_{cur} = \cos\{-70^0 - (\angle I_0 - \angle I_{polar})\}$. For voltage polarization, the equation is $T_{volt} = \cos\{-100^0 - (\angle 3E_0 - \angle I_0)\}$. If the value of both torques is greater than a threshold, the fault is in the operating direction. The threshold in both cases is zero.

Table 18: DirOC Relay Settings

Setting	Units
High side voltage	kV
Low side voltage	kV
High side CT ratio	turns ratio
Low side CT ratio	turns ratio

5.3.2.4 Diff

Diff is a percentage differential harmonic restraint transformer algorithm. This algorithm trips if the differential current exceeds a threshold. It restrains trip if the differential current contains high levels of 2nd harmonic current (present during magnetizing inrush current) or 5th harmonic current (present during overexcitation). As such, the algorithm needs to calculate the 2nd and 5th harmonic phasors, as well as the fundamental frequency phasors for all high side, low side, and tertiary currents. Of course, CTs need to be delta connected on wye windings, and wye connected on delta windings, to account for the transformer phase shift. If they are not, the equivalent efect can be obtained by calculation in the algorithm.

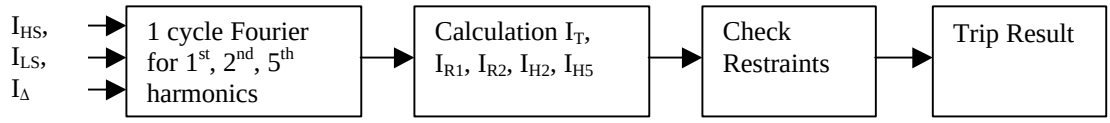

Figure 16: Transformer Differential Relay Algorithm

There are 5 equations to be calculated for each phase. The trip current equation is $I_T = I_{HS} - I_{LS} - I_{\Delta}$.

There are two restraint current equations: $I_{R1} = I_{HS} + I_{LS} + I_{\Delta}$ and $I_{R2} = -I_{HS} + I_{LS} - I_{\Delta}$. These three equations determine if the relay should trip for the fundamental frequency operating current.

The two harmonic restraint equations are :

$I_{H2} = |I_{HS2}| + |I_{LS2}| + |I_{\Delta 2}|$ for the 2nd harmonic

$I_{H5} = |I_{HS5}| + |I_{LS5}| + |I_{\Delta 5}|$ for the 5th harmonic across each phase.

For each phase, these five equations are compared to a restraining quantity. If any one of the restraint equations are true, the relay is restrained from operating.[10]

$$|I_T| < a$$

$$|I_T| < b|I_{R1}|$$
$$|I_T| < b|I_{R2}|$$
$$|I_{H2}| > g|I_T|$$
$$|I_{H5}| > d|I_T|$$

If any phase of the relay trips, the whole relay returns a trip signal.

Table 19: Transformer Differential Relay Settings

Setting	Units
High side voltage	kV
Low side voltage	kV
Tertiary voltage	kV
High side CT ratio	turns ratio
Low side CT ratio	turns ratio
Tertiary CT ratio	turns ratio
α	constant
β	constant
γ	constant
δ	constant

5.3.2.5 BkrFail

The BkrFail algorithm supervises breaker failure timers. When the breaker receives a trip

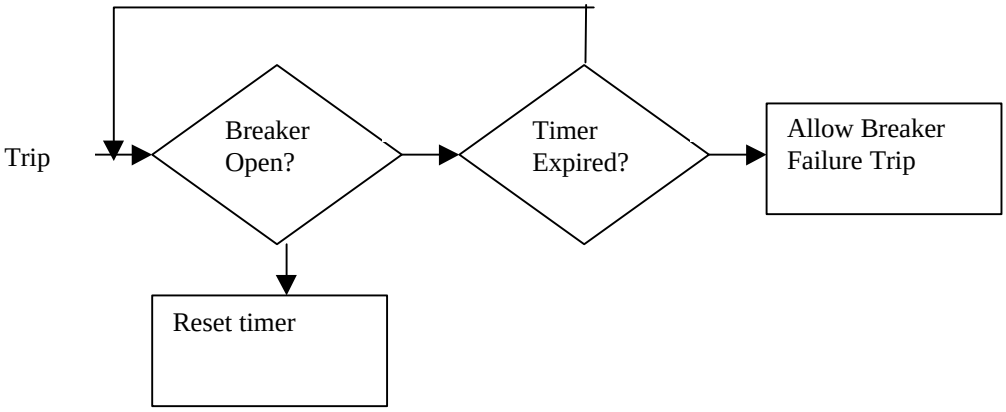

Figure 17: BkrFail Relay Algorithm

signal, the algorithm starts a timer stored in TimerBlock for the breaker. Until the timer expires, no trip of a breaker failure scheme is permitted. Once this specific breaker trips, the timer is reset to zero. As long as a trip signal for the breaker exists, the value of the timer is incremented every sample, until the timer equals the operating time of the breaker failure scheme. If this occurs, the algorithm sets thr TripBlock output contact for every breaker included in the breaker failure scheme.

Table 20: BkrFail Relay Settings

Setting	Units
Breaker Failure Operating Time	Cycles

5.3.3 Vote Logic Supervision

The vote logic scheme works on a combination of a logical OR function and a logical

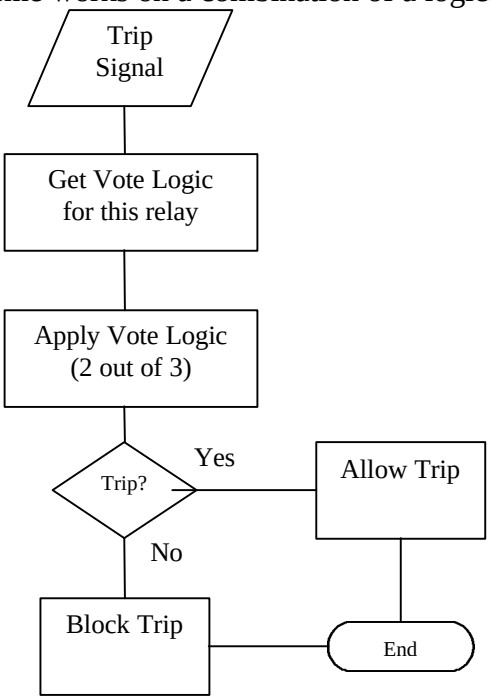

Figure 18: Vote Logic Algorithm

AND function to adjust the security and dependability balance of the existing protection system. The vote logic array for a specific device is a two dimensional array storing pointers to TerminalBlock, which holds the trip signals from the existing relays. Upon retrieving the logic scheme from VoteLogic, each row is tested through the OR function, and the results of each OR function are combined through the AND function. The output of the AND function is the trip signal. If the array in VoteLogic is empty, this specific device and protection scheme is supervised by the hidden failure supervision scheme for the device. This scheme is very flexible, as it allows any combination of protections for a vote logic.

Table 21: Vote Logic - Line Phase Protection

Line Protection Scheme				Function
Zone 1	Zone 2	Zone 3	DCB	OR
DCB	PCB			OR
PCB	Zone 1	Zone 2	Zone 3	OR
				AND

Table 22: Vote Logic - Line Ground Protection

Line Protection Scheme				Function
Zone 1	Zone 2	Zone 3	PCB	OR
PCB	Dir OC			OR
Dir OC	Zone 1	Zone 2	Zone 3	OR
				AND

5.3.4 RSS Internal Components

The RSS has several important sections that store information or interact with the existing relays.

5.3.4.4 TerminalBlock

TerminalBlock is the input point for trip signals from existing relays. Each block is associated with a specific line and specific protection scheme. The value of an individual block is 1 if the existing relay has operated.

5.3.4.5 TripBlock

TripBlock stores the status of trip output for individual breakers. This is the part of the RSS that actually supervises circuit breaker operation. The output of TripBlock controls contacts in series with the breaker trip coils.

5.3.4.6 VoteLogic

VoteLogic stores the logic schemes for the vote mode for each line. Separate phase and ground schemes are stored. Each scheme is stored in a two dimensional array of pointers to TerminalBlock for specific protection scheme status.

5.3.4.7 DataBuffer

DataBuffer stores 2 seconds of waveform sample data, or

$2\,\text{sec} \times 60\,{}^{\text{cycles}}\!/_{\text{sec}} \times 12\,{}^{\text{samples}}\!/_{\text{cycle}} = 1440$ samples, for every supervised device. A waveform is stored from every CT and PT modeled. DataBuffer stuffs the current sample for all waveforms in the top of the array, forcing the oldest sample out. Two seconds of data allows the use of long coordination timer settings for step-distance relays. DataBuffer is initialized by storing a normal conditions case for the system.

5.3.4.8 LineBkr

LineBkr stores the circuit breakers associated with an individual device. This information determines what points in TripBlock to set for a successful trip operation.

5.3.4.9 BkrBkr

BkrBkr stores the circuit breakers associated with an individual breaker failure scheme. This information determines what points in TripBlock to set for a successful breaker failure operation.

5.4 Inputs to Run a Data Case

The system model requires several input files to run a data case. The existing relays require two files. One is a text file naming faulted line, distance to the fault (in % of line length), and type of fault (Phase, Ground, or both). The other is a file containing the steady state current value for each CT, used by the existing relay models that rely on fault current magnitude. The faulted line name establishes fault direction. The type of fault determines with relay algorithms to perform. The distance to the fault and the fault current magnitude determines if the fault is in the zone of protection for the relay. The RSS model requires two input files of waveform samples taken from EMTP. One file contains EMTP data of normal operating conditions for the system to initialize the DataBuffer. The other file contains EMTP data for the specific fault case. The EMTP model represents a CT as a 50 ohm burden, and provides a secondary voltage as an output. The input section of the RSS model divides the secondary voltage by the 50 ohm burden to produce the desired secondary amps.

The EMTP data cases contain a fault inception switch. This is a dummy switch activated in EMTP at the same instant in time when the actual fault switch closes. This switch tells the existing relay models when to start timing for a fault, which is equivalent to an actual relay recognizing a fault condition.