1 INTRODUCTION

Improvements in fast switching power devices have led to an increased interest in voltage source inverters (VSI) with pulse width modulation control (PWM). Control methods which generate the necessary PWM patterns have been discussed extensively in literature. These could be classified as voltage controlled and current controlled PWM. This thesis deals with voltage control PWM methods.

Several voltage controlled PWM methods have been proposed in literature [1,2,4,5,6] e.g., sinusoidal PWM, sinusoidal PWM with third harmonic injection and space vector modulation. All these methods aim at generating a sinusoidal inverter output voltage without low-order harmonics. This is possible if the sampling frequency is high compared to the fundamental output frequency of the inverter.

The performance of each of these control methods is usually judged based on the following parameters: a) Total harmonic distortion (THD) of the voltage and current at the output of the inverter, b) Switching losses within the inverter, c) Peak-to-peak ripple in the load current, and d) Maximum inverter output voltage for a given DC rail voltage.

The performance of sinusoidal PWM and sinusoidal PWM with third harmonic injection has been studied extensively in literature. This thesis deals with space vector modulation.

Space vector modulation is based on representation of the three phase voltages as space vectors. Most space vector modulation schemes generate the same required output voltage but differ in their performance with respect to THD, peak-to-peak ripple and switching losses. Many of these issues have been addressed in literature [1,3,6].

The main objective of this thesis is to recommend a scheme that is best suitable for a given application. Applications can be distinguished mainly based on their power level and hence the switching frequency or by the type of load.

To achieve this goal several space vector modulation schemes have been considered. The choice of these schemes was governed mainly by the performance criteria described above. Analysis was first performed for each of these schemes to develop expressions and generate a series of curves under various operating conditions. Then the circuit was simulated in SABER to verify the expressions developed and finally the modulation schemes were tested real-time on a prototype inverter to verify the validity of both the analysis and simulation.

The first part of the thesis deals with three-leg voltage source inverters (Fig.1.1), which are standard inverters providing three-phase three-wire output. Four space vector modulation schemes are considered here. Their performance with respect to for each of the above mentioned factors is analyzed over the entire range of modulation index and for varying load power factor angles. A novel procedure for the calculation of THD has also been proposed. The analysis is verified using simulation and experiments.

The second part of the thesis deals with four-leg voltage source inverters (Fig.1.2), which are very attractive for applications where three-phase four-wire output is required. This topology is known to produce balanced output voltages even under unbalanced load conditions [9,10]. Due to the additional leg, the number of topologies which this inverter could assume is sixteen which is twice that of a conventional three-leg inverter. The process of space vector modulation and duty cycle calculation for this four-leg topology is reviewed first. Then the techniques developed for the analysis of three-leg voltage

source inverter in the first part of the thesis are used to analyze a four-leg voltage source inverter. Three space vector modulation schemes have been addressed here. Their performance with respect to THD and switching losses is analyzed. The analysis is performed for both balanced and unbalanced load conditions. For the balanced case, the analysis is performed over the entire range of modulation index and over varying load power factors. For the unbalanced case two kinds of unbalance have been considered 1) load power factor unbalance 2) load magnitude unbalance. The analysis is verified using simulation.

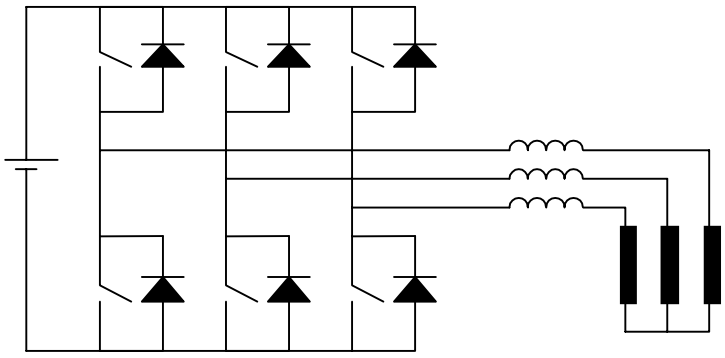

Fig. 1.1. Topology of a three-leg voltage source inverter.

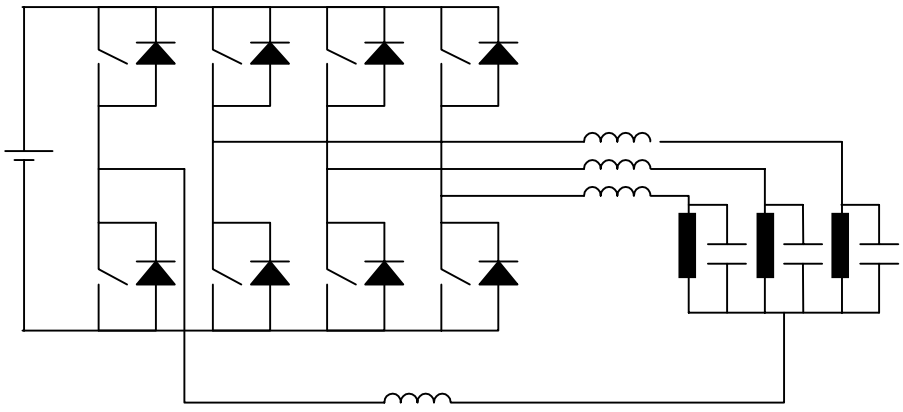

Fig. 1.2. Topology of a four-leg voltage source inverter.