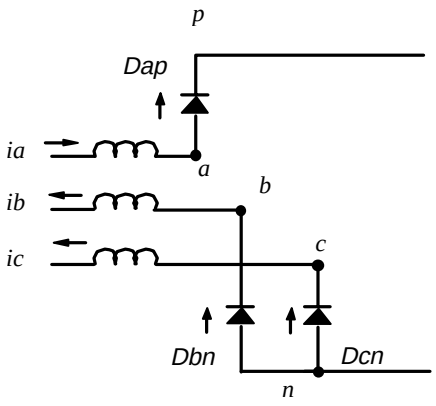
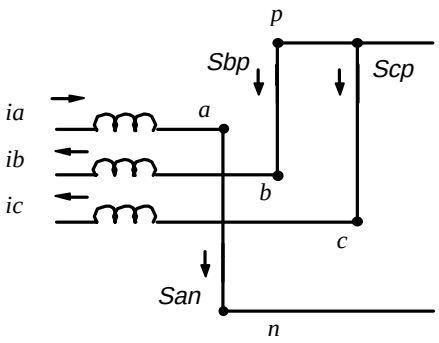
3. INFLUENCE OF ZVT OPERATION ON SVM

3.1. Effects of ZVT

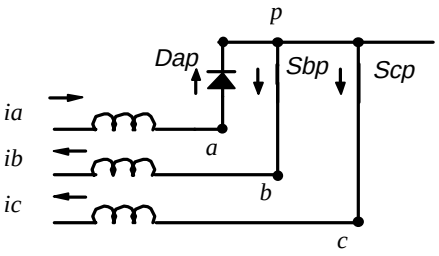
Influence of the AUXI on SVM can be studied on the SVM example in Fig. 2.2(b). Assume that the circuit produces the non-zero SSV $\boldsymbol{V}_{pnn}$, Fig. 3.1(a), and that the ac currents are $i_a>0$, $i_b<0$ and $i_c<0$, *i.e.* that the circuit is in the same state as at the beginning of the AUXI example considered above, Fig. 2.3(a). After the AUXI takes place the circuit is brought to the SSV $\boldsymbol{V}_{npp}$, which is complementary to $\boldsymbol{V}_{pnn}$, and has three switches conducting, Fig 3.1(b). From this point the circuit can be transferred to a state producing any SSV solely by opening switches. The vectors required in the SVM example are $\boldsymbol{V}_{ppn}$, $\boldsymbol{V}_{pnn}$, and $\boldsymbol{V}_{ppp}$ or $\boldsymbol{V}_{nnn}$. If the sequence $\boldsymbol{V}_{npp}\rightarrow\boldsymbol{V}_{ppp}\rightarrow\boldsymbol{V}_{ppn}\rightarrow\boldsymbol{V}_{pnn}$ is followed, only one switch opening is used for each transition. For instance, the circuit is brought from the SSV $\boldsymbol{V}_{npp}$, Fig. 9(b), to the SSV $\boldsymbol{V}_{ppp}$, Fig. 3.1(c), by opening of the switch S_{an} which transfers the current i_a to the diode D_{ap}. The transitions $\boldsymbol{V}_{ppp}\rightarrow\boldsymbol{V}_{ppn}\rightarrow\boldsymbol{V}_{pnn}$ occur in a similar way when the sequential opening of switches S_{cp} and S_{bp} takes place as shown in Fig. 3.1(c, d, a).



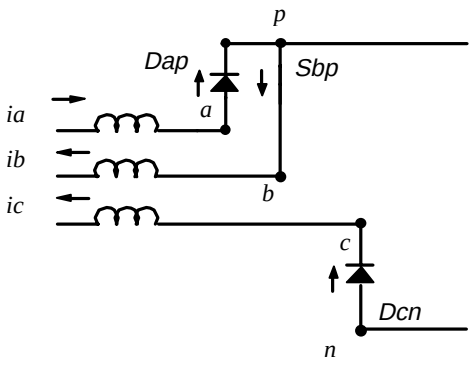
a) SSV Vpnn



b) SSV Vnpp



c) SSV Vppp



d) SSV Vppn

Fig. 3.1 Influence of ZVT on SVM sequence.

If a different sequence were used and the circuit were brought to the SSV $\boldsymbol{V}_{ppp}$ from SSV $\boldsymbol{V}_{pnn}$ by closing switches S_{bp} and S_{cp}, significant losses would be produced due to the reverse recovery of the diodes D_{bn} and D_{cn}. A single AUXI can eliminate the reverse recovery only if the proper switching sequence is used for SVM. This is always possible because any two adjacent SSVs and a zero vector can be reached from a state with three switches conducting, without ever commutating a diode.

Since two complementary vectors are never adjacent, an undesired SSV is always produced in SVM due to ZVT operation. In the above example this is the SSV $\boldsymbol{V}_{npp}$. Its effect in the synthesis of $\boldsymbol{V}_r$ can be canceled out by extending the duty-cycle of the required complementary SSV $\boldsymbol{V}_{pnn}$, and shortening the duty-cycle of the zero-vector, $\boldsymbol{V}_{ppp}$. Therefore, instead of according to (2.1), the reference vector $\boldsymbol{V}_r$ is synthesized as:

$$\boldsymbol{V}_r = d_2 \cdot \boldsymbol{V}_{ppn} + (d_1 + d_c) \cdot \boldsymbol{V}_{pnn} + d_c \cdot \boldsymbol{V}_{npp} + (d_0 - 2 \cdot d_c) \cdot \boldsymbol{V}_{ppp} \qquad (3.1)$$

where d_c is the minimum duty-cycle of the undesired SSV $\boldsymbol{V}_{npp}$ necessary to complete the ZVT process.

3.2 Incorporating ZVT operation

In order to accommodate the ZVT operation, the modified SVM has to determine a correct switching sequence for any combination of desired SSVs and three-phase currents, as well as to cancel the influence of the undesired SSVs generated in the process.

With six sectors and six possible combinations of three-phase current directions, there are 36 different switching sequences. They can be grouped in three characteristic cases, each containing twelve sequences. The cases are distinguished based on the directions of the currents i_a, i_b, and i_c, and on the polarities of the nodes *a*, *b*, and *c* in Fig. 1.2.

3.2.1 Case 1. Current directions are the same as node polarities in one of the adjacent SSVs in SVM

This represents normal rectifying operation and corresponds to the previous example. The desired SSV with node polarities same as the current directions has three diodes conducting. The auxiliary circuit is activated at the end of this state which transfers the circuit into the complementary undesired SSV with

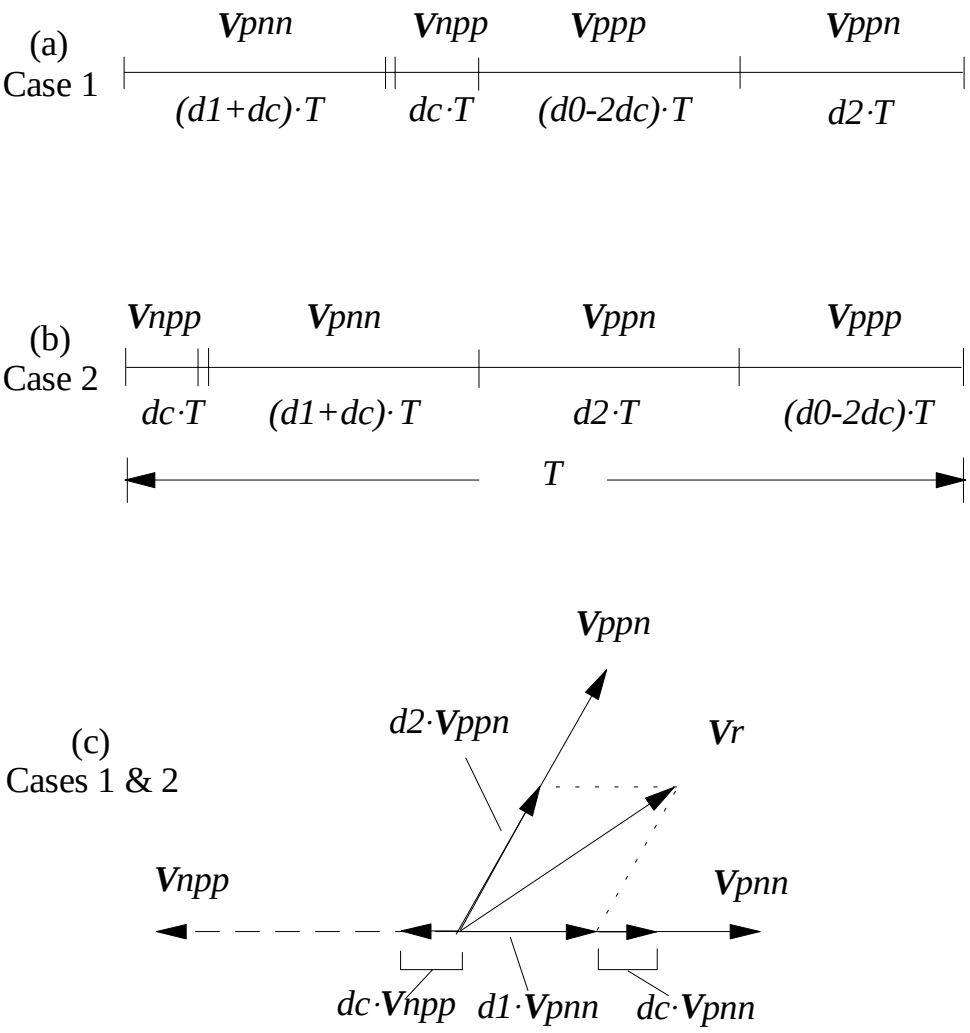


Fig. 3.2 Modified SVM (Cases 1 and 2).

three switches conducting. The remaining desired SSVs are then obtained by opening the switches, one at a time.

The switching sequence within the switching period T is shown in Fig. 3.2(a) for the previous example. The corresponding vector synthesis of the reference vector $\boldsymbol{V}_r$ is illustrated in Fig. 3.2(c). The undesired SSV $\boldsymbol{V}_{npp}$ is generated for a minimum time necessary to complete the AUXI, $d_c \cdot T$. This is compensated by extending the duration of its complementary desired SSV $\boldsymbol{V}_{pnn}$ by the same amount, thus generating the effective zero-voltage with duration $2 \cdot d_c \cdot T$. Therefore, the duration of the zero SSV $\boldsymbol{V}_{ppp}$ has to be reduced by $2 \cdot d_c \cdot T$. Duty-cycle of the SSV $\boldsymbol{V}_{ppn}$ is left unchanged. As a result the reference vector is synthesized according to (3.1).

3.2.2. Case 2: Current directions are opposite to the node polarities in one of the adjacent SSVs in SVM

This represents normal inverting operation. This case is opposite to the previous one. The desired SSV with node polarities opposite to the current directions has three switches conducting. The remaining desired SSVs are obtained by opening of the two switches, one at a time. After the final switch is opened the

circuit is in the state with all diodes conducting which generates the undesired complementary SSV. The AUXI then transfers the circuit back into the state with three switches conducting.

The switching sequence is illustrated in Fig. 3.2(b) for the case when $i_a<0$, $i_b>0$, and $i_c>0$, and the reference vector V_r is in sector II. The sequence starts from the undesired SSV $\boldsymbol{V}_{npp}$ with three diodes conducting, which is changed to its complementary desired SSV $\boldsymbol{V}_{pnn}$ after AUXI. The remaining transitions are achieved by opening the switches. The influence of the undesired vector is canceled in the same way as in Case 1, *i.e.* by using (3).

3.2.3. Case 3. Current directions are not the same nor opposite to the node polarities of the adjacent SSVs in SVM

This situation happens during transients or when the inverter is operating with very reactive loads. The phase shift between the ac currents and voltages is more than 30° lagging or leading. In this case the circuit state in which three diodes conduct produces none of the desired SSVs nor their complements. However the intended vector $\boldsymbol{V}_r$ can still be synthesized with only one AUXI by eliminating the zero-vector from the SVM sequence.

This is illustrated in Fig. 3.3 for the case when $i_a<0$, $i_b>0$, and $i_c<0$, and the reference vector $\boldsymbol{V}_r$ in the sector II. The circuit state in which only diodes conduct produces the undesired SSV $\boldsymbol{V}_{npn}$. After AUXI, the main bridge is transferred to the state producing another undesired SSV, $\boldsymbol{V}_{pnp}$. Fortunately, the transitions $\boldsymbol{V}_{pnp} \rightarrow \boldsymbol{V}_{pnn} \rightarrow \boldsymbol{V}_{ppn} \rightarrow \boldsymbol{V}_{npn}$ can all be obtained by simply opening the main bridge switches without ever commutating current from a diode. If the vectors $\boldsymbol{V}_{npn}$ and $\boldsymbol{V}_{pnp}$ are applied for the same duration they will cancel out and actually produce the zero-vector effect. The intended vector $\boldsymbol{V}_r$ can be synthesized as shown in Fig. 3.3, *i.e.* according to

$$\boldsymbol{V}_r = d_1 \cdot \boldsymbol{V}_{pnn} + d_2 \cdot \boldsymbol{V}_{ppn} + \frac{d_0}{2} \cdot \boldsymbol{V}_{npn} + \frac{d_0}{2} \cdot \boldsymbol{V}_{pnp} \ , \qquad (3.2)$$

where d_0 is given by (2.2).

3.3. Sequence Determination.

The SSV sequences in modified SVM when the reference vector is in the sector II are summarized in Fig. 3.4 for the three cases. The time sequence is from left to right, and the number of conducting switches is also indicated. The latter shows that AUXI is placed between the first and the second state in all the sequences, i.e. three diodes were conducting and then three switches appear

conducting, so two complementary SSVs are applied. For the remaining part of the sequences only one switch opening is used to change the applied SSV. The figure also shows when the zero-vector is applied and when it is replaced by two complementary SSVs.

Selection of the first state, in all the sequences, as the one with three diodes conducting is critical to preserve soft-switching in the main bridge during the transition between sequences. Nevertheless the soft-switching condition can be lost due to two reasons: error in current direction detection and very small or zero instantaneous phase current. Since the phase current values change little within a switching cycle, then when going from a sequence to another, the only possible error in current detection under normal operating conditions will occur in the phase current which is near crossover. If the error in current direction detection occurs there will be hard switching actions in the corresponding leg of the main bridge. However the diode which is turned-off hard will be conducting a small instantaneous current and the reverse recovery problem will not be severe, but the node capacitance formed by the parallel combination of the parasitic and the snubbing capacitances will be discharged through the switch. The latter can also happen when the instantaneous phase current is zero or very small and it can not swing the node voltage to the opposite rail. As a result there exists an optimum value of snubbing capacitance as far as efficiency is concerned.

Among the sources of error in current direction detection, noise induced by digital to analog conversion and the current ripple are the relevant ones. This subject is further discussed in Chapter 4.

Table 3.1 presents in detail the sequences summarized in Fig. 3.4. Consider the column corresponding to case 1. The letters *a*, *b*, and *c*, represent the respective phases. The polarities of the phase currents are indicated as $i_a>0$, (+), $i_b<0$, (-), and $i_c<0$, (-). When the SSV $\boldsymbol{V}_{pnn}$ is applied, the node voltages coincide with the phase current polarities and three diodes are conducting, D_{ap}., D_{bn}., and D_{cn}. Even though the diodes are known to be conducting the gate signals of the antiparallel switches are activated, therefore, S_{ap}, S_{bn}, and S_{cn}, have their gate signals active, and the remaining switches, S_{an}, S_{bp}, and S_{cp}, are off. So the positions filled in the table indicate which gate signals are active (on) and the blank positions indicate the inactive ones (off).

From the SSV $\boldsymbol{V}_{pnn}$ the circuit is brought to the SSV $\boldsymbol{V}_{npp}$ after AUXI. This changes the polarity in the three nodes as the arrows indicate. When the SSV $\boldsymbol{V}_{npp}$ is applied, three switches S_{an}, S_{bp}, and S_{cp}, conduct as shown in their respective positions. From this state the circuit is taken to the SSV $\boldsymbol{V}_{ppp}$ by the opening of switch S_{an} which is indicated by the arrow in the column *a* and the appearance of diode D_{ap} conducting when node *a* changes polarity.

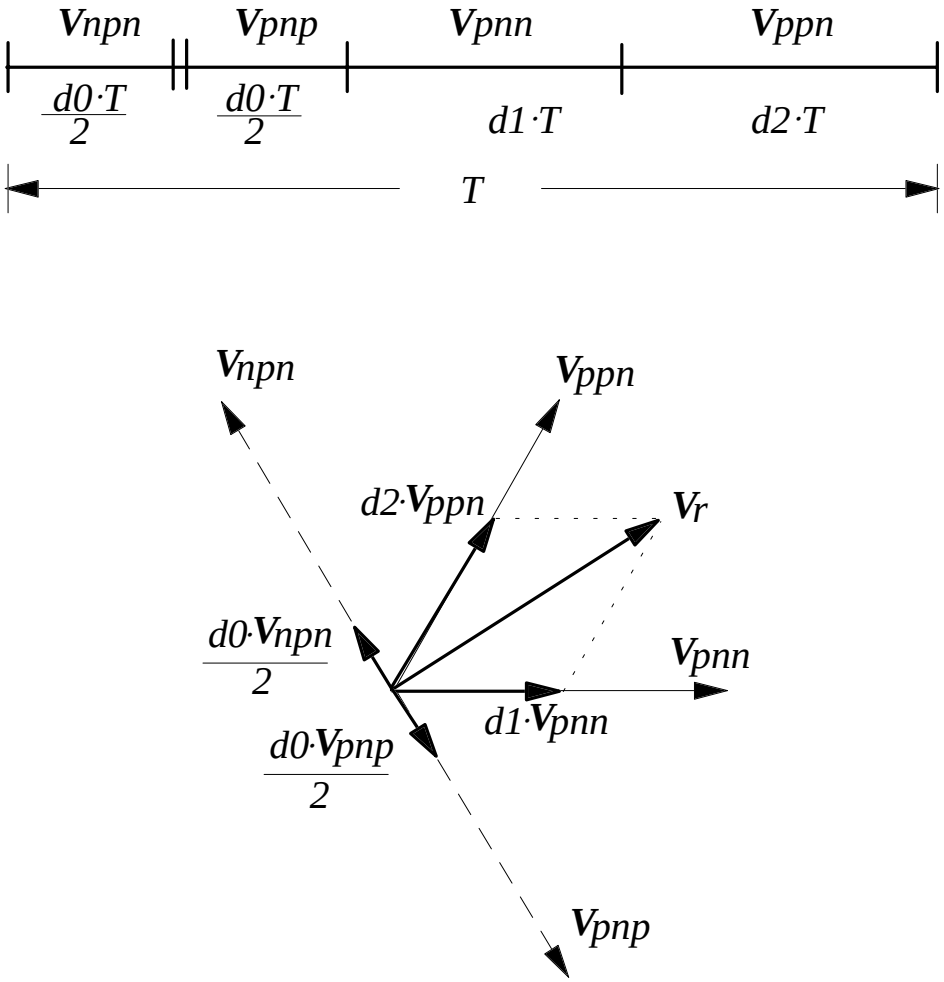


Fig. 3.3 Modified SVM (Case 3).

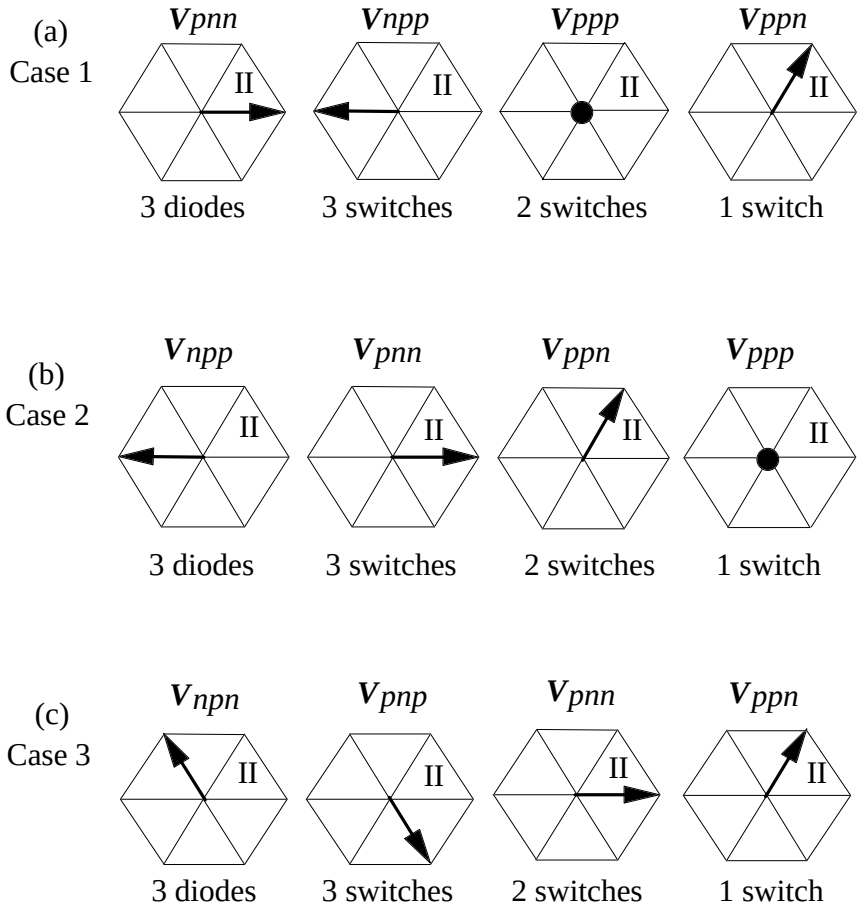


Fig. 3.4 SSV sequences in modified SVM with reference vector in sector II.

Table 3.1 Sequences in Sector II

	CASE 1				CASE 2				CASE 3			
i	SSV	a	b	c	SSV	a	b	c	SSV	a	b	c
		+	-	-		-	+	+		-	+	-
p	*pnn*	*Dap*			*npp*		*Dbp*	*Dcp*	*npn*		*Dbp*	
n			*Dbn*	*Dcn*		*Dan*				*Dan*		*Dcn*
Auxi		↓	↑	↑		↑	↓	↓		↑	↓	↑
p	*npp*		*Sbp*	*Scp*	*pnn*	*Sap*			*pnp*	*Sap*		*Scp*
n		*San*					*Sbn*	*Scn*			*Sbn*	
		↑					↑					↓
p	*ppp*	*Dap*	*Sbp*	*Scp*	*ppn*	*Sap*	*Dbp*		*pnn*	*Sap*		
n								*Scn*			*Sbn*	*Dcn*
				↓				↑			↑	
p	*ppn*	*Dap*	*Sbp*		*ppp*	*Sap*	*Dbp*	*Dcp*	*ppn*	*Sap*	*Dbp*	
n				*Dcn*								*Dcn*
			↓			↓				↓		

t ↓

Then, the circuit is taken to SSV $\boldsymbol{V}_{ppn}$ by the opening of switch S_{cp}, and the change in node c voltage is shown by the arrow and the indication of D_{cn} conducting. From this state the circuit is brought back to SSV $\boldsymbol{V}_{pnn}$ to start a new cycle by the opening of switch S_{bp}. This action is also indicated by the arrow showing the change in polarity for node *b*. In a similar way cases 2 and 3 are described in Table 3.1. It can be inferred from the procedure shown in Table 3.1 and Fig. 3.4, that the rest of the sequences can be obtained by identifying the SSV in which three diodes are conducting and the adjacent vectors required by SVM. With this information the case to which the sequence belongs is easily determined, *i.e*. the SSV with node polarities coincident with current directions (three diodes conducting) is a desired adjacent SSV, a complementary to a desired adjacent one, or none of the above. Once this is known the sequence is established by noting that the next SSV in the sequence is the complementary one, and that the rest of the SSVs are reached by solely opening switches, one at a time. The latter implies that the sequence continues from a SSV to one of its adjacent ones, *i.e*. a SSV whose node polarities differ at most in one. This classification includes the zero SSVs $\boldsymbol{V}_{ppp}$ and $\boldsymbol{V}_{nnn}$, as can be seen in Fig. 3.4 for cases 1 and 2 where SSV $\boldsymbol{V}_{ppp}$ is reached. Obviously there are sequences where $\boldsymbol{V}_{nnn}$ is the desired adjacent vector to complete ZVT operation. By symmetry the number of sequences is equal to one

third of the total, that is 12. All the sequences are displayed in similar tables contained in Appendix A.

From Table 3.1 and Figures 2.3 and 3.1 it is clear that in the modified SVM all the switches are operated at constant frequency. This means that in the main bridge there are six soft turn-on actions and six hard turn-off actions every cycle. In addition to this, the auxiliary circuit presents one turn-on action and one turn-off action per cycle.

In the regular PWM where one switch is kept on while the switches in the other two legs of the bridge are commutating, there are four switching events which include two hard turn-on actions and two hard turn-off actions. In the standard SVM with alternating zero vector, there are three switching events but the effective switching frequency for the devices in the main bridge is halved with respect to that in the modified SVM and therefore the ripple frequency is also halved. The switching events include one and half hard turn-on actions and one and half hard turn-off actions.