4. IMPLEMENTATION AND EXPERIMENTAL RESULTS

4.1 Power Stage

The experimental converter, Fig. 4.1, was built for V_{pn} = 800 V, maximum rms line voltage of 480 V, and rated power of 10 kW. The main bridge is a 6MBI50L-120 IGBT six pack with an 8.2 nF snubbing capacitor across each switch. Other circuit components are L_f = 1.0 mH, C_f = 12.5 μF, L_x = 6 μH. Diodes in the auxiliary circuit are DSE120-10A, the auxiliary switch is implemented with four IXTH12N90 MOSFETs connected in parallel, and UZ708 zener diodes are used.

4.2 Controller

The converter controller was implemented using ADSP2101 digital signal processor and one Altera EPM5192 programmable logic device (Appendix B).

The modified SVM was tested with the converter operating as an inverter and as a rectifier, and for each case a different control program (Appendix C) and state machine were used, although this is not necessary in practice.

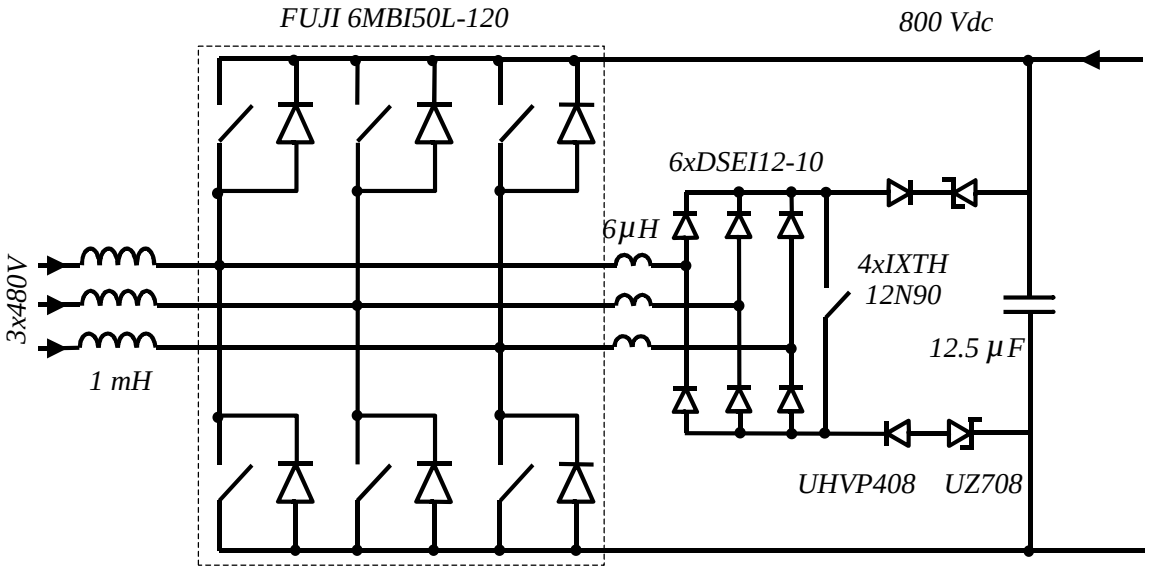


Fig. 4.1. Experimental Prototype.

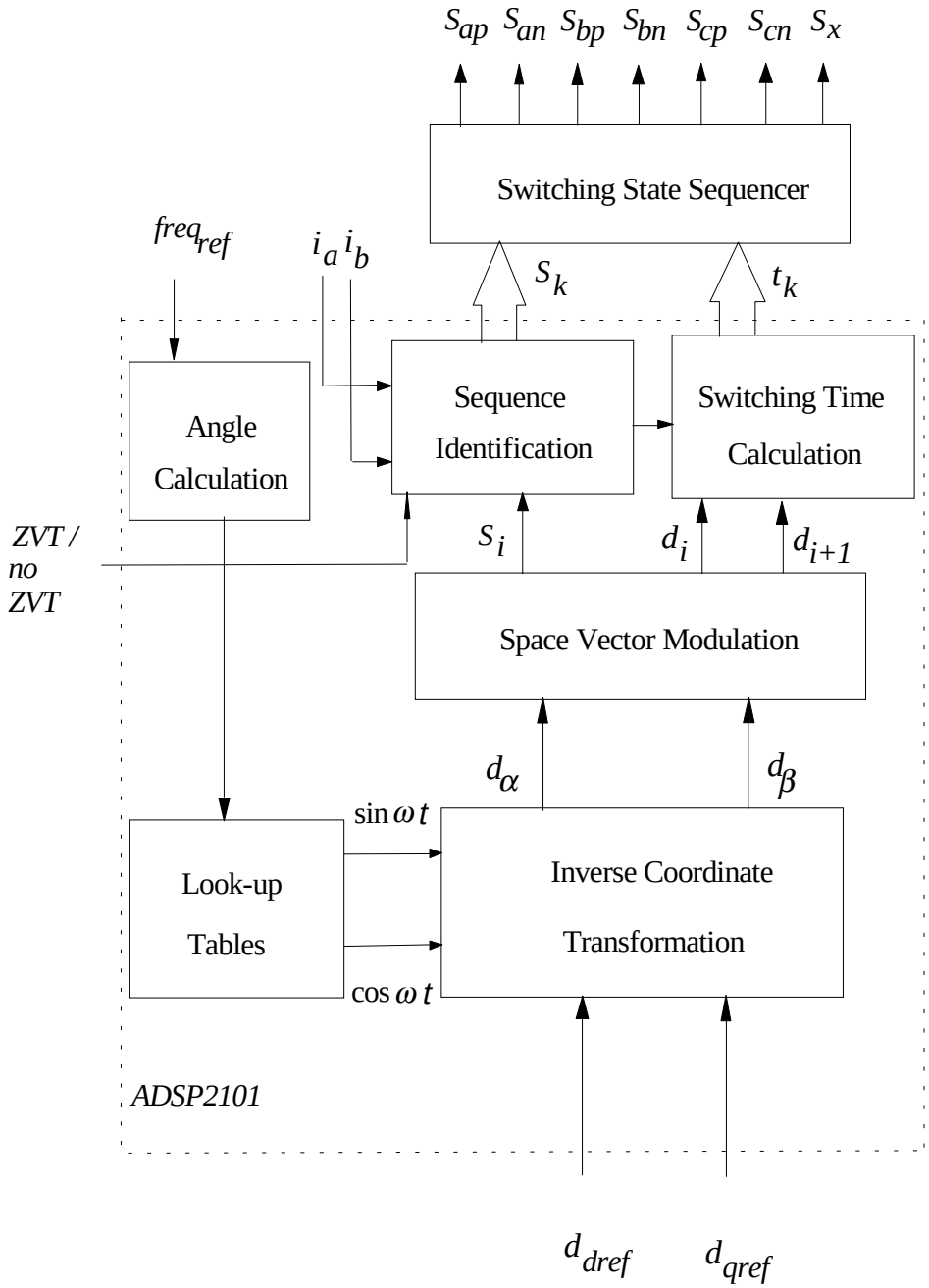


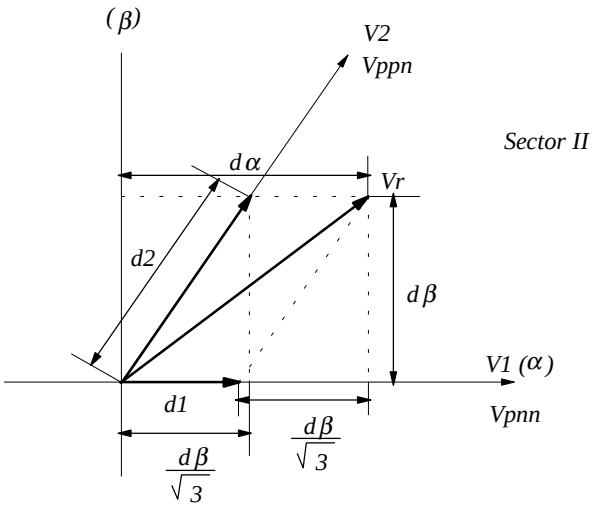
Fig. 4.2. Inverter control functional block diagram.

4.2.1. Inverter Control

The functional block diagram of this control is shown in Fig. 4.2. It incorporates the features needed to control a three-phase motor, *i.e*. frequency and direct and quadrature duty-cycle inputs and the choice between standard and modified (ZVT) SVM. The angle, ωt needed for $sin(\omega t)$and $cos(\omega t)$ calculation, is generated by using the internal DSP clock together with the frequency command , $freq_{\text{ref}}$. The *sine* and *cosine* function values are computed through a look-up table. Reference values for direct (d_{dref}) and quadrature (d_{qref}) duty-cycles are entered through two channels of an analog to digital converter (ADC). They are converted into the stationary duty-cycles d_α and d_β according to:

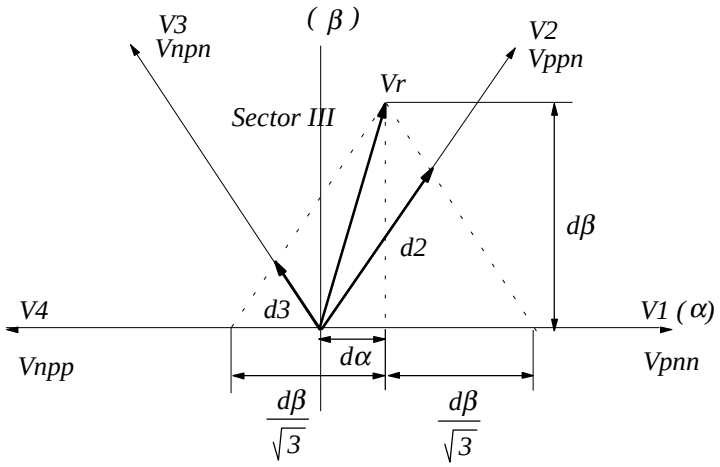
$$\begin{bmatrix} d_\alpha \\ d_\beta \end{bmatrix} = \begin{bmatrix} cos(\omega t) & -sin(\omega t) \\ sin(\omega t) & cos(\omega t) \end{bmatrix} \begin{bmatrix} d_{dref} \\ d_{qref} \end{bmatrix} \tag{4.1}$$

Figures 4.3 and 4.4 describe sector identification and adjacent vector duty-cycle computation in SVM. The flow chart in Fig. 4.4 exploits the symmetry in order to produce an efficient computation. To this end the SSVs $\boldsymbol{V}_{pnn}$, $\boldsymbol{V}_{ppn}$, $\boldsymbol{V}_{npn}$, $\boldsymbol{V}_{npp}$, $\boldsymbol{V}_{nnp}$, and $\boldsymbol{V}_{pnp}$ were renamed $\boldsymbol{V}_1$, through $\boldsymbol{V}_6$, respectively.



$$d_1\left(d_{pnn}\right) = \left|d_\alpha\right| - \left|d_\beta\right| / \sqrt{3} \qquad d_2\left(d_{ppn}\right) = 2\left|d_\beta\right| / \sqrt{3}$$

a) Sector II, condition: $\sqrt{3}\left|d_\alpha\right| > \left|d_\beta\right|$



$$d_2\left(d_{ppn}\right) = \left|d_\beta\right| / \sqrt{3} + \left|d_\alpha\right| \qquad d_3\left(d_{npn}\right) = \left|d_\beta\right| / \sqrt{3} - \left|d_\alpha\right|$$

b) Sector III, condition: $\sqrt{3}\left|d_\alpha\right| \le \left|d_\beta\right|$

Fig. 4.3. Duty-cycle calculation examples

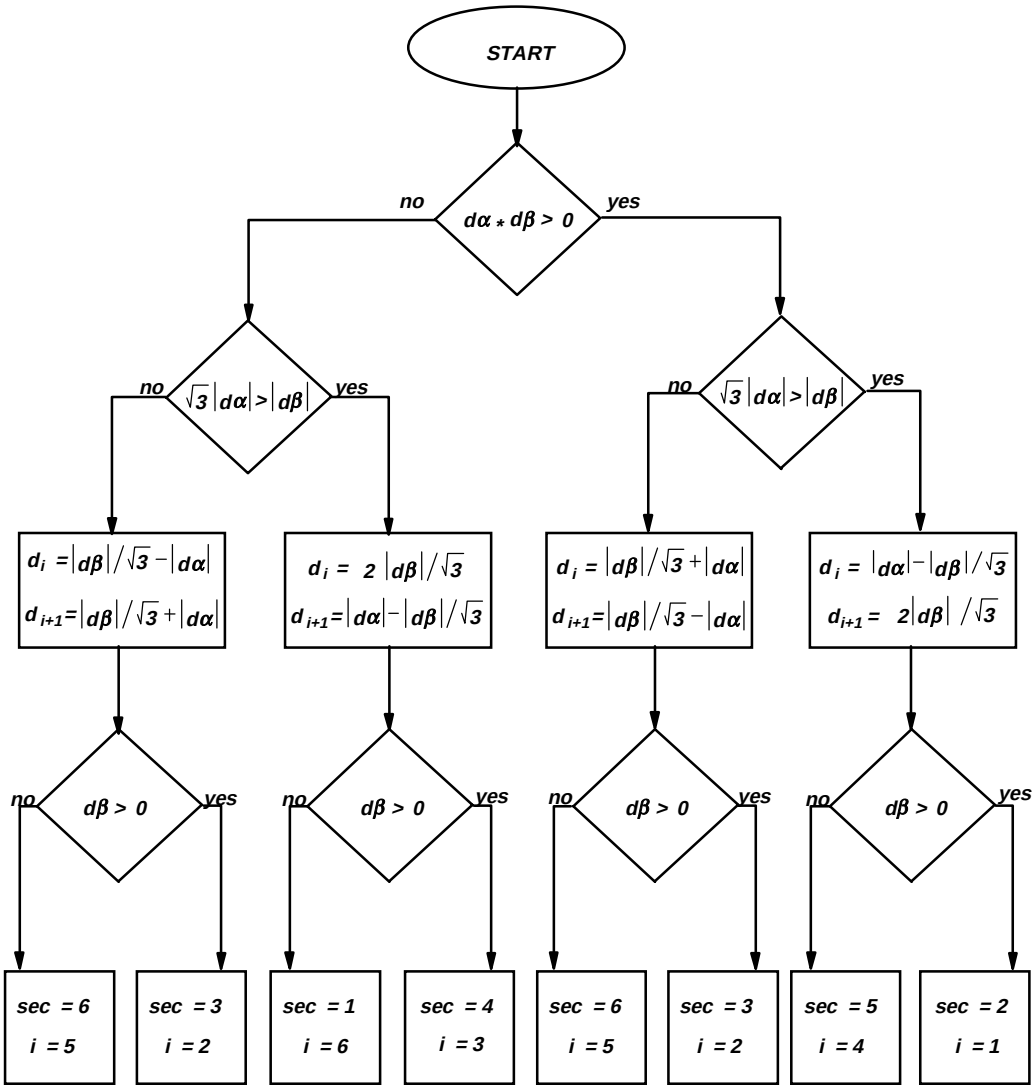


Fig. 4.4. Sector identification and duty-cycle calculation.

When standard SVM is used the current polarities are not needed. It is not the case when modified SVM is applied. The standard SVM only has one sequence and therefore only requires the calculation of adjacent vector duty-cycles. The zero-vector duty-cycle is left active during the remaining portion of the cycle according to (2.2).

In the modified SVM, sequence identification requires current polarities and sector information. Hall sensors are used to measure phase currents i_a and i_b, which are then read through the ADC. From this, all the current polarities are obtained and the required sequences can be determined.

From required sequence and adjacent vector duty-cycle information switching time values, t_k, are obtained. The latter, together with the switch combinations, S_k, are passed to the switching state sequencer, which produces the switching gate signals. This sequencer is implemented in a programmable logic device, Altera EPM5192 (Appendix B).

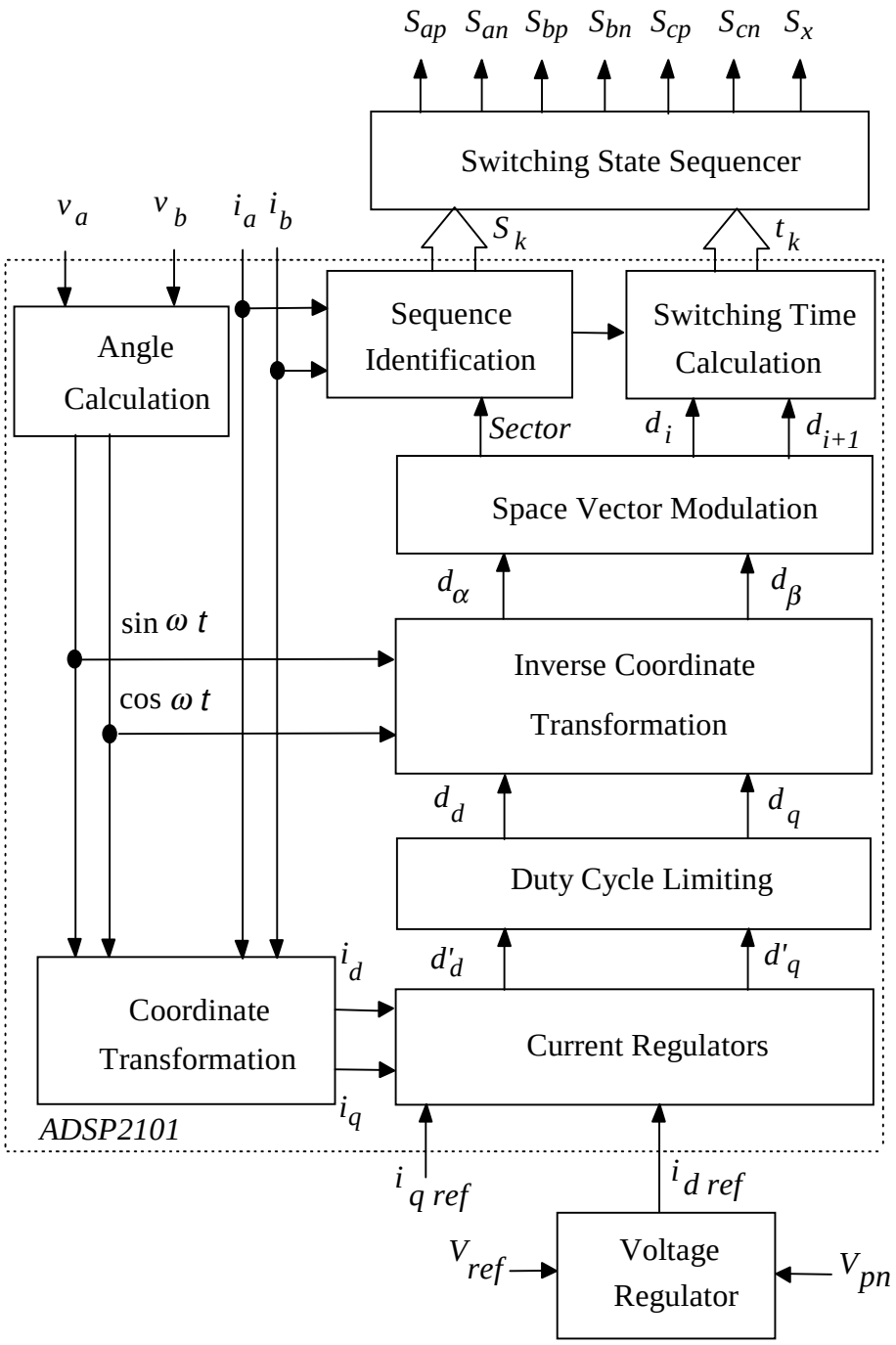


Fig. 4.5. Rectifier control functional block diagram.

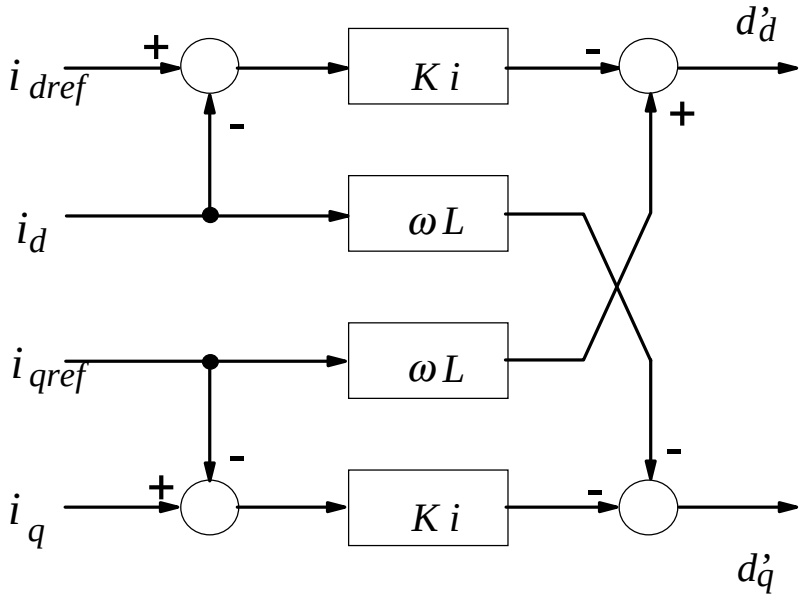


Fig. 4.6. Current regulators in rotating d-q coordinates.

4.2.2. Rectifier Control

The functional block diagram of this control is shown in Fig. 4.5. In this case *sin(ωt)* and *cos(ωt)* references are synchronized to phase voltages according to

$$cos(\omega t) = \frac{V_a}{V_{a(pk)}}, \tag{4.2}$$

$$sin(\omega t) = \frac{V_a + 2V_b}{\sqrt{3}V_{a(pk)}}, \tag{4.3}$$

where a balanced system has been assumed.

The coordinate transformation used to calculate direct and quadrature current components, i_d and i_q, in rotating coordinates is:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} cos(\omega t) & sin(\omega t) \\ -sin(\omega t) & cos(\omega t) \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}, \tag{4.4}$$

where

$$i_\alpha = i_a , \tag{4.5}$$

and

$$i_\beta = \frac{i_a + 2i_b}{\sqrt{3}} . \tag{4.6}$$

The current regulators are shown in Fig. 4.6. The blocks ωL are used to cancel the coupling effect between the *d* and *q* axes introduced by the inductors. The references i_{dref} and i_{qref} are read through the ADC. The direct current component determines the active power transfer through the converter and its reference comes from the analog output voltage regulator circuit. The quadrature current component determines the reactive input power, *i.e*. the input displacement factor. For unity power factor, $i_q = 0$ and therefore $i_{qref} = 0$.

In order to control distortion of the currents during transients, duty-cycle limiting is implemented in polar coordinates. The maximum duty-cycle vector magnitude, $\sqrt{d_d^2 + d_q^2}$, is restricted below unity but the direction of the duty-cycle vector is kept unchanged. The inverse coordinate transformation and the rest of the functions are the same as those used in the inverter case.

It is important to note that this rectifier control scheme automatically provides for regeneration. If $V_{pn}<V_{ref}$ for longer time, the output of the voltage regulator, i_{dref} will become negative and the input currents will reverse sign resulting in reversal of the power flow.

4.2.3. Variable Sensing and A/D Converter

The A/D converter used, MAX158 features 8-channels and 2.5μs conversion time. This leads to sequential sensing of the variables and appearance of their ripples as strong noise in the measurements when no compensation or filtering is added. Clearly controller's speed and performance are limited .

4.2.4. State Machine Considerations

As it is well known, a delay between turn-off and turn-on of switches in the same leg is required for this topology. If these delays were directly controlled by the DSP the size of the state machine would be excessively increased. This can be easily seen in its diagram on Appendix B. The number of registers in cascade at the top of the diagram is directly related to the number of switch combinations which gets doubled by delay times should the latter be handled by state machine. In addition, a similar increase would occur to the registers at the bottom of the

diagram where the number of pairs depends on the number of independent time intervals assigned to switch combinations. In order to minimize state-machine size the delays are adjusted in the gate drives and set up equal to the minimum time required by the auxiliary circuit during its resonance stage.

4.2.5 Modified SVM Implementation

According to section 3.2, desired vector V_r and current directions determine sequence and SSVs used. This information, stored in a table, is sent to the state machine, Appendix B, and used by the top set of registers mentioned in 4.2.4 to produce the signals delivered to the gate drivers. In addition, duty-cycles for SSVs are calculated and sent to the bottom set of registers, also mentioned in 4.2.4, together with values for duration of *charging* and *discharging* stages in the auxiliary sequence. This information determines time intervals during which SSVs and auxiliary-switch gate signal are applied.

4.3 Current Ripple and Main Inductors

As it was pointed out in section 3.2, error in the detection of instantaneous current direction leads to loss of ZVT due to the selection of the wrong sequence. This detection error is greatly influenced by the current ripple since the sampling is performed sequentially and the conversion time is not negligible for the switching

frequency used here. Even though filtering (analog and/or digital) of the sensed currents helps control performance by allowing better estimation of variable averages in both coordinate frames, rotating and stationary, it does degrade the accuracy in the detection of instantaneous current direction and therefore increases the interval around current cross-over without ZVT . Furthermore, the latter can happen if the ripple is too large, irrespective of correct detection of the instantaneous current direction since this can change during a switching cycle.

From the above discussion it is clear that a higher inductor value will allow better ZVT operation and smoother control by providing lower current ripple. Unfortunately, as it is pointed out by [29] the close-loop bandwidth is inversely related to the main inductor value. So, if a fast response is needed, as it is usually the case, a compromise among current ripple, current loop speed and interval length with loss of ZVT has to be arrived at in order to determine the inductor value. Since it is obvious that main inductors and current ripple are directly related an approximated relation, assuming unity power factor operation, is developed to help with the design procedure. From the current waveforms in Fig. 4.8 it is apparent that maximum ripple occurs near phase peak currents. Since at unity power factor the voltage produced by the main bridge must be lagging the mains, when the SSV of the currents coincides with SSV V_1 for the main bridge the

desired vector V_r is inside Sector II as in Fig. 2.2. Therefore, according to Fig. 4.7, d_α and d_β, are defined by

$$d_\alpha = \frac{3 \cdot V_{pk}}{2 \cdot V_{dc}} \qquad \text{and} \qquad d_\beta = \frac{3 \cdot V_{pk} \cdot \omega \cdot L}{2 \cdot V_{dc} \cdot R_{eq}}, \tag{4.7}$$

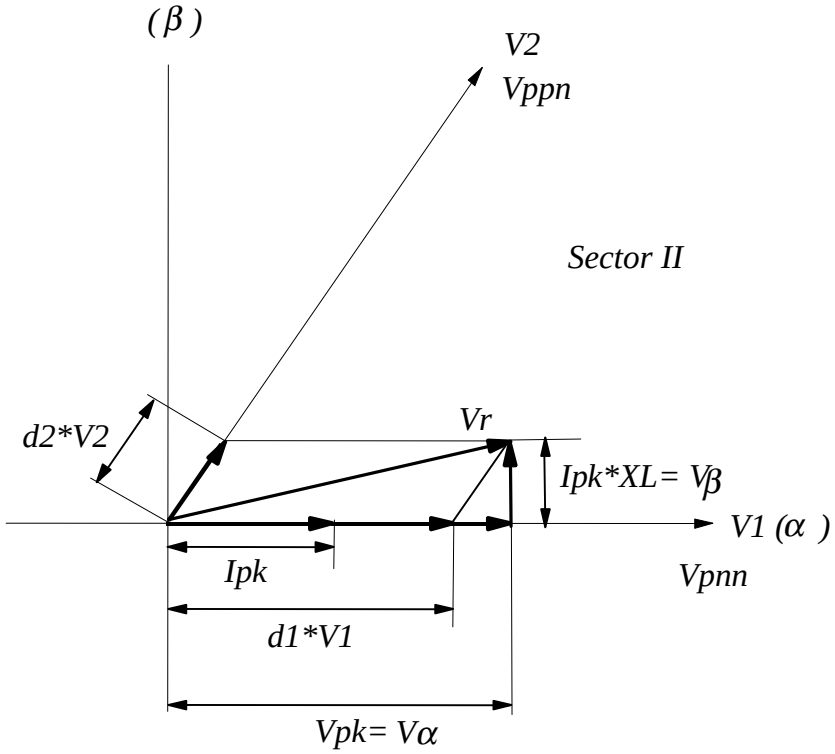
where $R_{eq} = \frac{3 \cdot V_{pk}^2}{2 \cdot P_o}$ and $\omega = 2 \cdot \pi \cdot freq$. Also from Fig. 4.4a

$$d_1 = |d_\alpha| - \frac{|d_\beta|}{\sqrt{3}} \quad \text{and} \qquad d_2 = \frac{2 \cdot |d_\beta|}{\sqrt{3}}. \tag{4.8}$$

According to Fig. 3.2 an extension by d_c of d_1 or d_2 must considered when computing the changes in inductor current during these duty-cycles which are

$$\Delta i_1 = \frac{\left(\frac{2}{3} \cdot V_{dc} - V_{pk}\right) \cdot d_1 \cdot T_s}{L} \quad \text{and} \quad \Delta i_2 = \frac{\left(\frac{V_{dc}}{3} - V_{pk}\right) \cdot d_2 \cdot T_s}{L} \tag{4.9}$$

respectively. Note that Δi_2 shows two cases. For $V_{dc} \geq 3 \cdot V_{pk}$ the total current ripple is given $\Delta i_1 + \Delta i_2$ or otherwise by Δi_1.



$$d_\alpha = \frac{3 \cdot V_{pk}}{2 \cdot V_{dc}} \qquad d_\beta = \frac{3 \cdot V_{pk} \cdot \omega \cdot L}{2 \cdot V_{dc} \cdot R_{eq}} \qquad R_{eq} = \frac{3 \cdot V_{pk}^2}{2 \cdot P_o}$$

$$d_1 = |d_\alpha| - \frac{|d_\beta|}{\sqrt{3}} \qquad d_2 = \frac{2 \cdot |d_\beta|}{\sqrt{3}}$$

$$\Delta i_1 = \frac{\left(\frac{2}{3} \cdot V_{dc} - V_{pk}\right) \cdot d_1 \cdot T_s}{L} \qquad \Delta i_2 = \frac{\left(\frac{V_{dc}}{3} - V_{pk}\right) \cdot d_2 \cdot T_s}{L}$$

Fig. 4.7. Filter inductor and current ripple relation.

4.4 Auxiliary Circuit Design

Design of the auxiliary circuit consists of choosing the commutation inductor values, determining the timing for the auxiliary switch control and selecting the commutation circuit components.

Duration of the charging and discharging states within AUXI (t_2 - t_1 and t_4 - t_3 in Figs. 2.4 and 2.6) are approximately equal because the auxiliary inductors are always charged and discharged with the same, constant dc voltage, V_{pn}. The charging phase should be longer than the reverse recovery time of the main bridge diodes, but in the inverter mode of operation it also must be longer than the minimum time necessary to produce the SSV with all diodes conducting ($\boldsymbol{V}_{pnn}$ in Fig. 2.5). In the rectifier mode, the discharging phase must be longer than the minimum time necessary to produce the SSV with all switches conducting ($\boldsymbol{V}_{pnn}$ in Fig. 2.3). Although these SSV are undesired in SVM they must be used, as explained in Chapter 3. Since the SSVs involve one main switch turn-off, the duration of the charging and discharging states may be determined by the switch turn-off time instead of the diode reverse recovery time. This is especially the case with IGBTs which may be slower then their anti-parallel diodes. Addition of the loss-less capacitive snubbers to reduce the turn-off loss of the main switches, further prolongs the turn-off time, and hence, has the adverse effect on the

duration of AUXI and the achievement of ZVT near phase current crossover as pointed out in section 3.2.

Once the duration of the charging state is known, the auxiliary inductors, L_x, should be selected so that enough energy is stored in them to commutate the nodes a, b, and c during the resonance state. Selecting the value of the largest auxiliary current at the end of the charging state to be atleast $\sqrt{3}$ times the amplitude of the phase current under full load guarantees ZVS for all load and line conditions [4]. This is due fact that two of the auxiliary inductors are connected in parallel during the charging state and hence carry half the current that flows in the third. After taking into account the auxiliary current rise during the resonant phase, and adding some margin, it follows that the peak current I_x, through the auxiliary switch S_x, must be almost two times larger than the maximum amplitude of the phase currents. If a lower value of I_x is chosen, ZVS is partially lost during part of the ac line cycle, resulting in somewhat increased switching losses and electromagnetic interference (EMI).

In the following design procedure [4], the charging time is then given by:

$$T_c = \frac{3L_x}{2V_{dc}} I_c \tag{4.7}$$

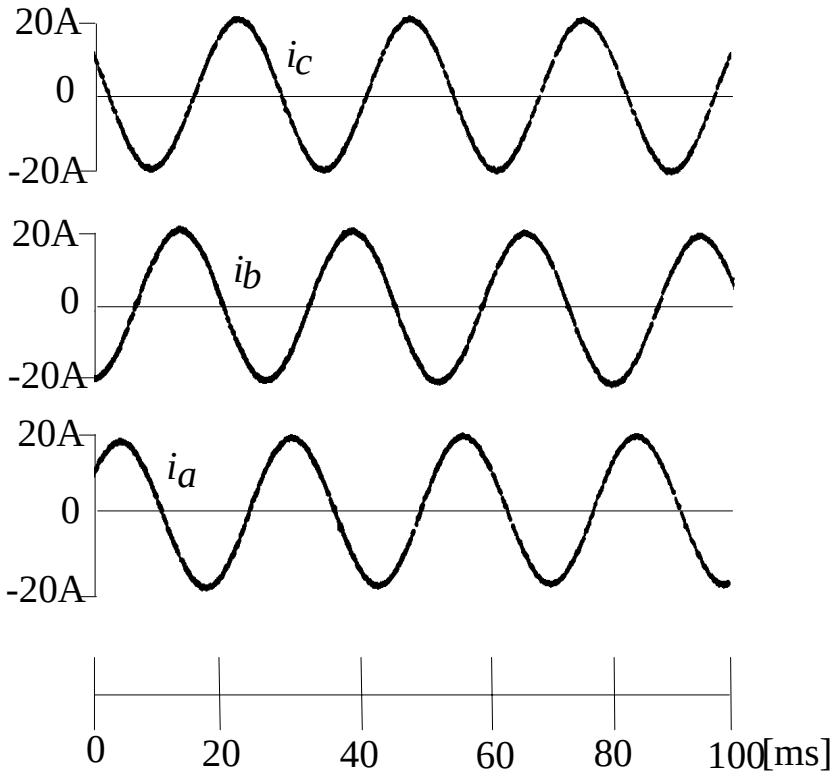


Fig. 4.8. Experimental low frequency ac currents in inverter mode.

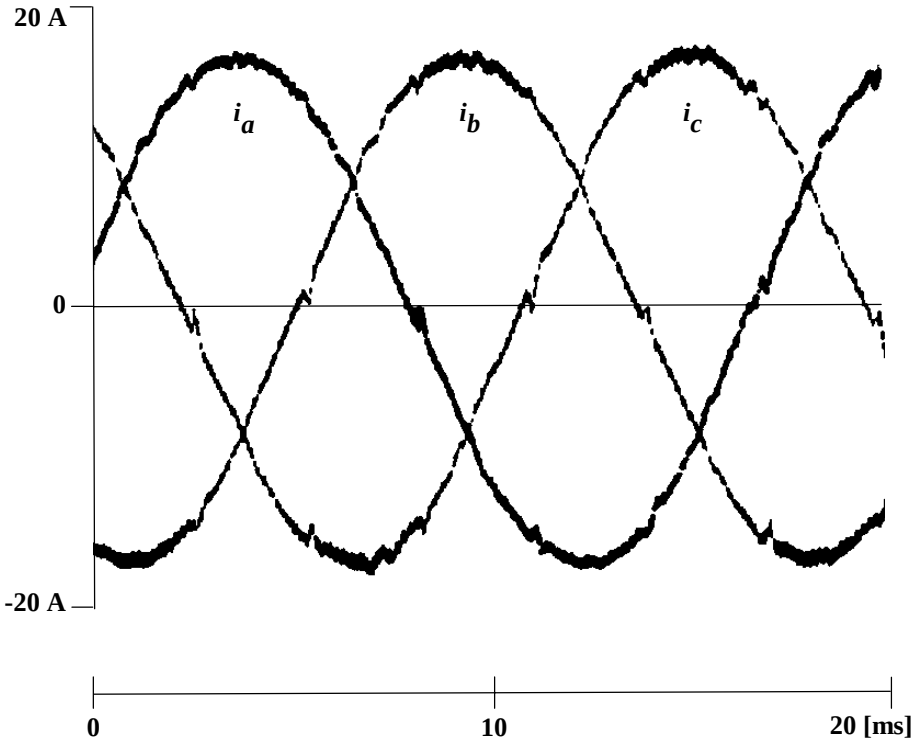


Fig. 4.9. Experimental low frequency waveforms in rectifier mode.

where I_C is the selected auxiliary current value for commutation of the diodes, and for the full ZVS range it should be $Ic > \sqrt{3}\, I_m$, where I_m is the amplitude of the input phase currents under full load.

At the end of the charging state, the three switches carrying the charging currents (S_{ap}, S_{bn}, and S_{cn} in Fig. 2.3(b)) are turned-off, and their complementary switches are turned-on after the resonant state. This requires a time delay between a switch turn-off and the turn-on of the other switch in the same bridge leg. The same time delay can be used for switch commutations after the AUXI, as the dead-time for short-through prevention. For reliability reasons, it is also preferable to implement this turn-on delay in the hardware of gate drives.

The resonant time can be estimated as:

$$T_r = \pi \sqrt{L_x C_x} \tag{4.3}$$

where C_x is the capacitance of the nodes *a*, *b*, or *c*. The resonant current amplitude can be estimated from Fig. 2.3(c) under different operating conditions to be given by:

$$I_r = \frac{2V_{dc}}{3\sqrt{L_x / C_x}} \tag{4.4}$$

The peak auxiliary current, I_x, is thus:

$$I_x = I_c + I_r \tag{4.5}$$

The discharging phase duration, T_d, is approximately equal to the charging phase duration, T_c. The total on-time of S_x, T_x, is given by:

$$T_x = T_c + T_r + T_d = 3\frac{L_x}{V_{dc}} I_c + \sqrt{L_x C_x} \tag{4.6}$$

Thus the auxiliary switch is controlled by a constant frequency, constant duty-cycle clock signal. The timing of the bridge switches (turn-on and turn-off delay) is fixed and does not depend on line or load variations or on the mode of operation.

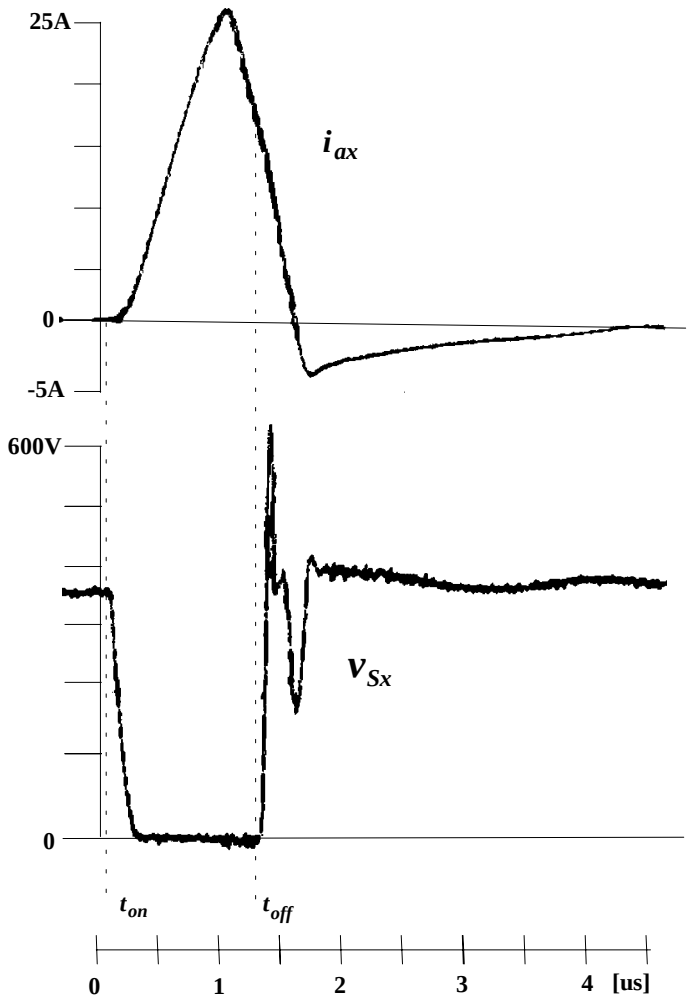


Fig. 4.10(a). Effect of turn-off timing on auxiliary switch voltage stress (early turn-off).

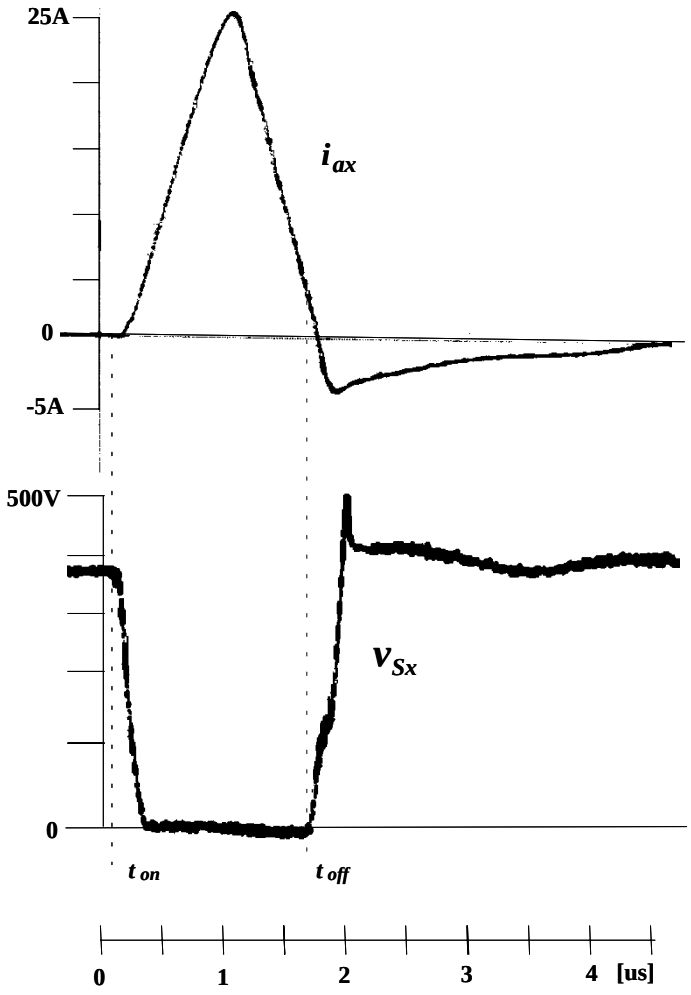


Fig. 4.10(b). Effect of turn-off timing on auxiliary switch voltage stress (on time turn-off).

The average value of the auxiliary switch current, $\overline{I_X}$, is:

$$\overline{I_X} = \frac{I_X T_X}{2T} \tag{4.7}$$

where T is the switching period.

During the discharging state the energy stored in the auxiliary inductors is returned back to the dc side. Therefore, the major losses in the auxiliary circuit are conduction losses in the diode bridge and auxiliary switch S_X. This may lead to the conclusion that S_X should be an IGBT. However, if the switch S_X is still conducting at the end of the discharging state, a large reverse current can build up in the auxiliary inductors. This current would be later dissipated in the zener diodes during the slow discharge state. This situation can be prevented by early turn-off of the auxiliary switch but this will result in large turn-off losses and very high voltage stress due to parasitics, as can be seen in Fig. 4.9(a). Therefore S_X should be implemented as a fast MOSFET, (unless AUXI is relatively long), and turned-off with very little current, Fig. 4.9(b).

Currents through the auxiliary circuit diodes have the same slope as the currents in the main bridge. Hence, the auxiliary diodes have to be at least as fast

as the main bridge diodes. Voltage of the zener diodes is not a major design concern. It only influences duration of the slow discharge state but not the dissipation because the residual energy in the auxiliary inductors will be dissipated anyway.

Although the auxiliary circuit is inactive before the AUXI, the S_X is not turned-on under zero-voltage conditions because its parasitic capacitance is charged by the leakage currents of the diodes D_{xp} and D_{xn} while S_x is off.

4.5. Experimental Waveforms

The experimental results shown in Figs. 2.6 and 4.6 were obtained with the converter operating as an inverter at 6 kW and V_{pn}=400 V. The situation depicted in Fig. 2.6 corresponds to Case 2 and reference vector $\boldsymbol{V}_r$ in sector IV when the correct SSV sequence is $\boldsymbol{V}_{pnn}\rightarrow\boldsymbol{V}_{npp}\rightarrow\boldsymbol{V}_{npn}\rightarrow\boldsymbol{V}_{nnn}$.

Figs. 2.3 and 4.7 illustrate operation of the converter as rectifier at 40% load, Vin = 230 Vrms, Vout = 500 V and close to unity power factor.

Very smooth low frequency waveforms in both modes of operation confirm that the modified SVM completely compensates undesirable effects of the ZVT operation. Very clean high frequency waveforms demonstrate that the ZVT

operation successfully absorbed all the circuit parasitics, and as a result EMI and ringing are significantly reduced.

4.6 Low Frequency Distortion and Gain Limitations

The proposed modified SVM eliminates most of the low frequency distortion that would result from the ZVT operation by compensating the SSV duty-cycles according to (3.1) and (3.2). The only low frequency characteristics affected by ZVT are the ratio of ac and dc voltages and the local average of the line voltages in the transition between switching sequences.

The ratio of ac and dc voltages is limited to

$$\frac{V_m}{V_{pn}} \leq 1 - 2 \cdot d_c \ , \tag{4.8}$$

where V_m is the ac line voltage amplitude, and directly follows from (3.1) and (3.2) because the minimum duration of the effective zero-vector is $2 \cdot d_c \cdot T$.

The perturbation in local average voltage is due to either the sector crossing of the desired space vector or the change in current combination. This small change in the local average voltage has an effect on the instantaneous *d* and *q* current components, which can be appreciated in Fig. 4.10 through 4.21 for

rectifier and inverter modes of operation. This effect on phase currents can be easily understood by resorting to Figs. 3.2 and 3.4, and Appendix A. Particularly for the waveforms in rectifier mode shown in Fig. 4.10, the sequences have an adjacent vector followed by the undesired vector, then the zero vector and finally the other adjacent vector. When moving from one sequence to another, in steady state, the adjacent vector that was placed last is now placed first. This is confirmed by the continuation of the same current slope at the end of the switching cycle and this is what affects the local average. Changes in the other cases can be explained in a similar way.

In the rectifier mode of operation this perturbation in phase currents is promptly corrected by the current loop as seen in Fig. 4.8 and the distortion is kept to a minimum. In addition, this distortion can be further reduced if the control algorithm becomes more elaborate and alters the duration of the first switching state in the next couple of cycles of the new sequence for the case discussed. For other sequence transitions the variations can include changes in the switching states used to synthesize the required space vector.

In order to avoid chattering in the transition between sequences during phase current crossover a hysteresis loop was introduced in the program. As it can be inferred, this reduces distortion in local average voltage and as a result in phase currents. Because of the loss of ZVT near phase current crossover, mentioned in

section 3.2, there will be a compromise between losses and distortion in the selection of hysteresis-loop width.

4.7. Efficiency Analysis

Measured efficiency of the experimental converter operating in the inverter mode is shown in Figs. 4.13 and 4.14. If the converter is operated with standard SVM without ZVT the turn-on losses are approximately 300 W, which is 3% of the full power. Even though these losses are eliminated by using ZVT, the efficiency increase is only 2% due to the increased turn-off losses with ZVT operation. In standard SVM only two of the six bridge switches are operating at any given time. For example, if the reference vector $\boldsymbol{V}_r$ is in sector II and the three-phase currents are $i_a > 0 > i_b > i_c$, only switches S_{bp} and S_{cp} will be operating while all the other switches will be off. In the ZVT circuit all six switches operate all the time, thus increasing the turn-off losses approximately three times. Therefore, the ZVT converter in Fig. 1.2 is best suited for applications with the dc

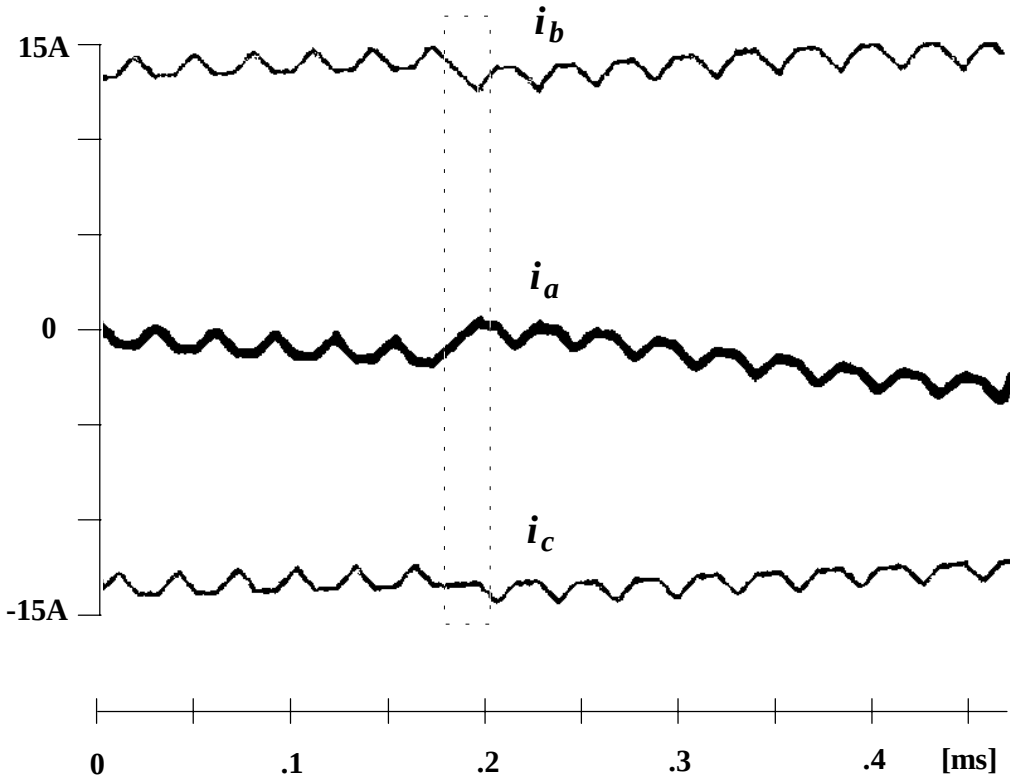


Fig. 4.11. Effect of sequence transition on phase currents. in rectifier mode

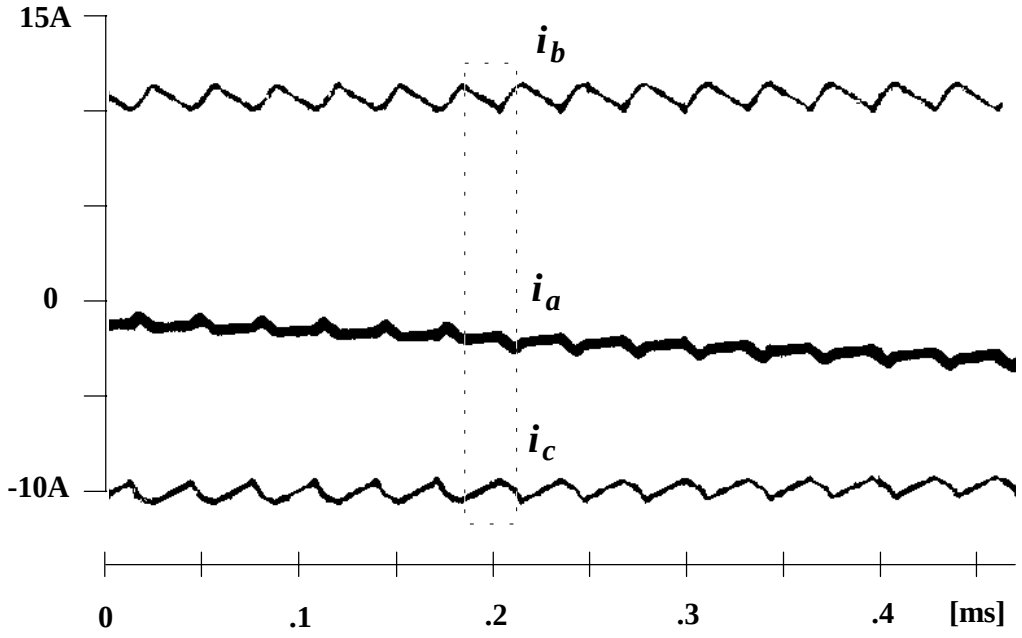


Fig. 4.12. Effect of sequence transition on phase current. in inverter mode for delta-connected resistive load

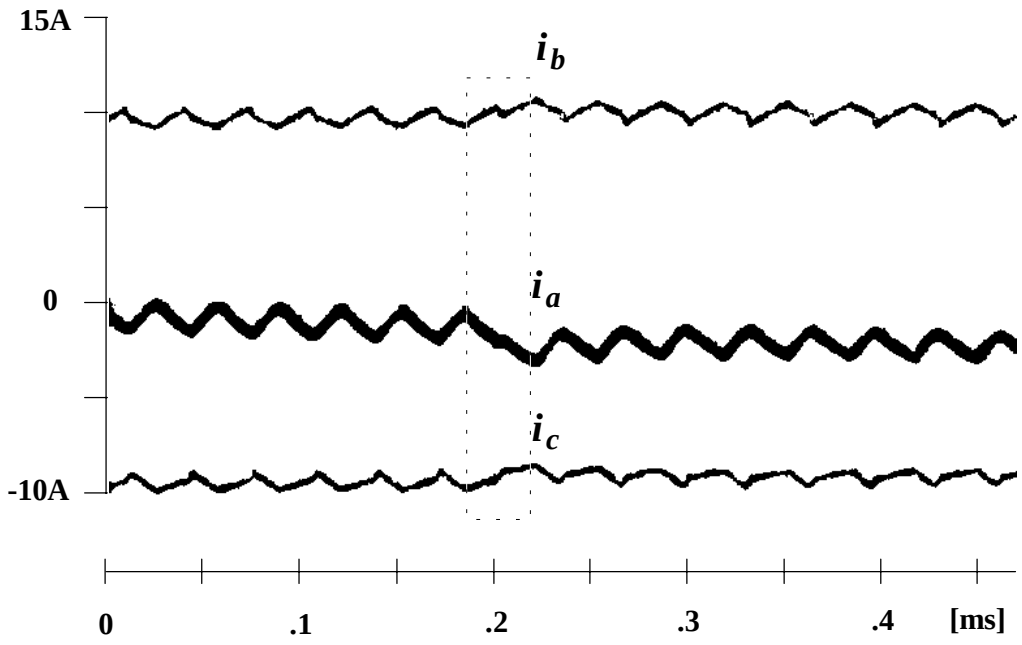


Fig. 4.13. Effect of sequence transition on phase current. in inverter mode for wye-connected resistive load

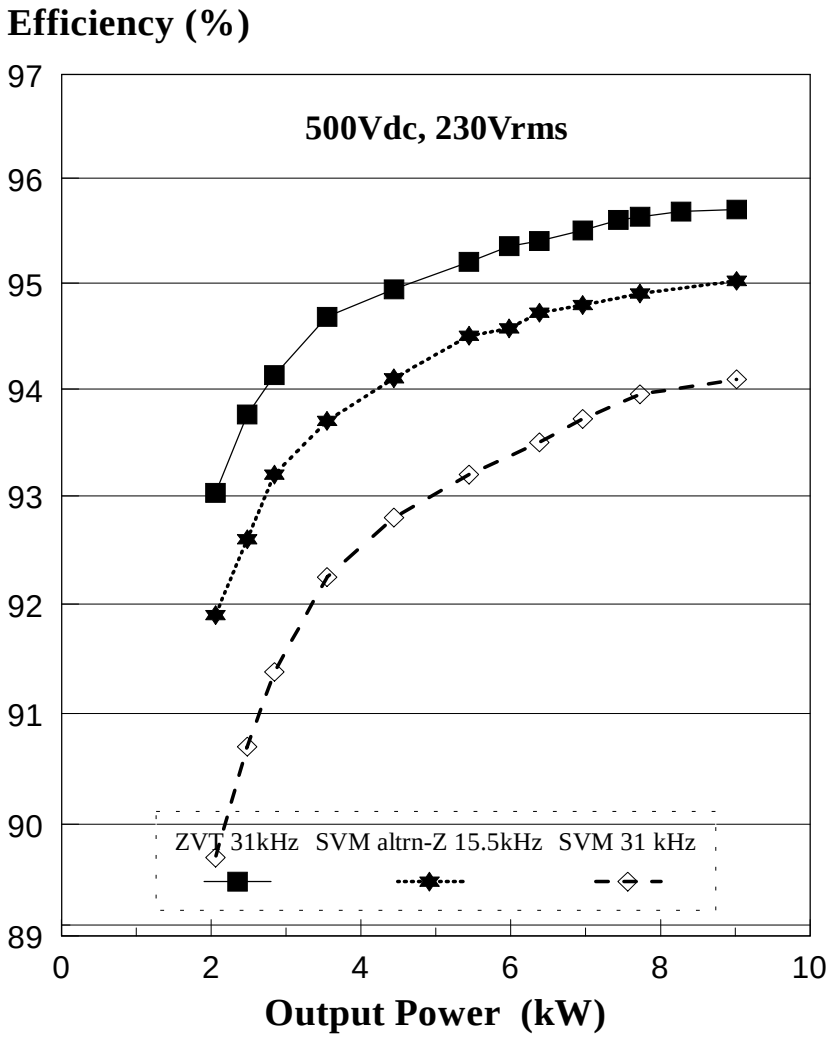


Fig. 4.14. Efficiency vs. output power in inverter mode (ZVT and PWM @ 31kHz, and SVM with alternating zero vector @ 15.5 kHz).

voltage below 600 V when fast MOSFETs can be used. Due to the very low MOSFET turn-off losses it is estimated that a 10 kW, 500 V, 100 kHz, ZVT converter could achieve 97% efficiency, even though the conduction losses would be higher.

Fig. 4.14 shows the ZVT converter efficiency for two different values of the peak auxiliary switch current, I_x. When I_x is approximately two times larger than the phase current amplitude at full load, ZVS is always achieved, but the efficiency reduces faster at low loads. This is due to the fact that the turn-off losses in the ZVT converter remain approximately constant at all power levels. Currents in the three switches that turn-off during AUXI are equal to the differences between the main phase currents and the auxiliary circuit currents. Because the auxiliary currents are the same at any load, the turn-off losses of these switches actually increase at light load. Since the other three switches turn-off with reduced currents at light loads, the total turn-off losses remain constant.

The turn-off loss at light load can be reduced if lower value of I_{aux} is chosen. In that case the efficiency is significantly increased at light loads but it decreases at heavy loads because ZVS is lost during large parts of the input line cycle. The optimum solution is to adjust the value of I_x according to the actual values of the main phase currents. This can be easily done in the DSP controller

implementation by making the duration of the charging and discharging times proportional to the peak values of the currents i_a and i_b which are already measured for the current regulator. The ZVT efficiency curve in Fig. 4.13 corresponds to the best possible $I_{aux\text{-}pk}$, i.e. it is obtained when the auxiliary timing is changed on-line.

Fig. 4.13 also shows the efficiency obtained with standard PWM and alternating zero vector, which effectively commutates the switches at half the original frequency. As can be seen the ZVT converter is still more efficient than the converter without soft-switching operating at half the original switching frequency.

Efficiency measurements for the converter operating in the rectifier mode with standard PWM and hard-switching as compared to those with ZVT and the new algorithm are shown in Fig. 4.14. As expected these efficiency characteristics are slightly higher than those in inverter mode because the main currents are now carried during longer time by main bridge diodes, and the latter have lower voltage drop than the main switches. The longer diode conduction period can be seen in the sequences shown in Fig. 3.4. In case 1, *i.e*. rectifier mode, the switching state with 3 conducting diodes is an adjacent vector and the other adjacent vector has two conducting diodes. Conversely, in case 3, *i.e*. inverter mode, the switching

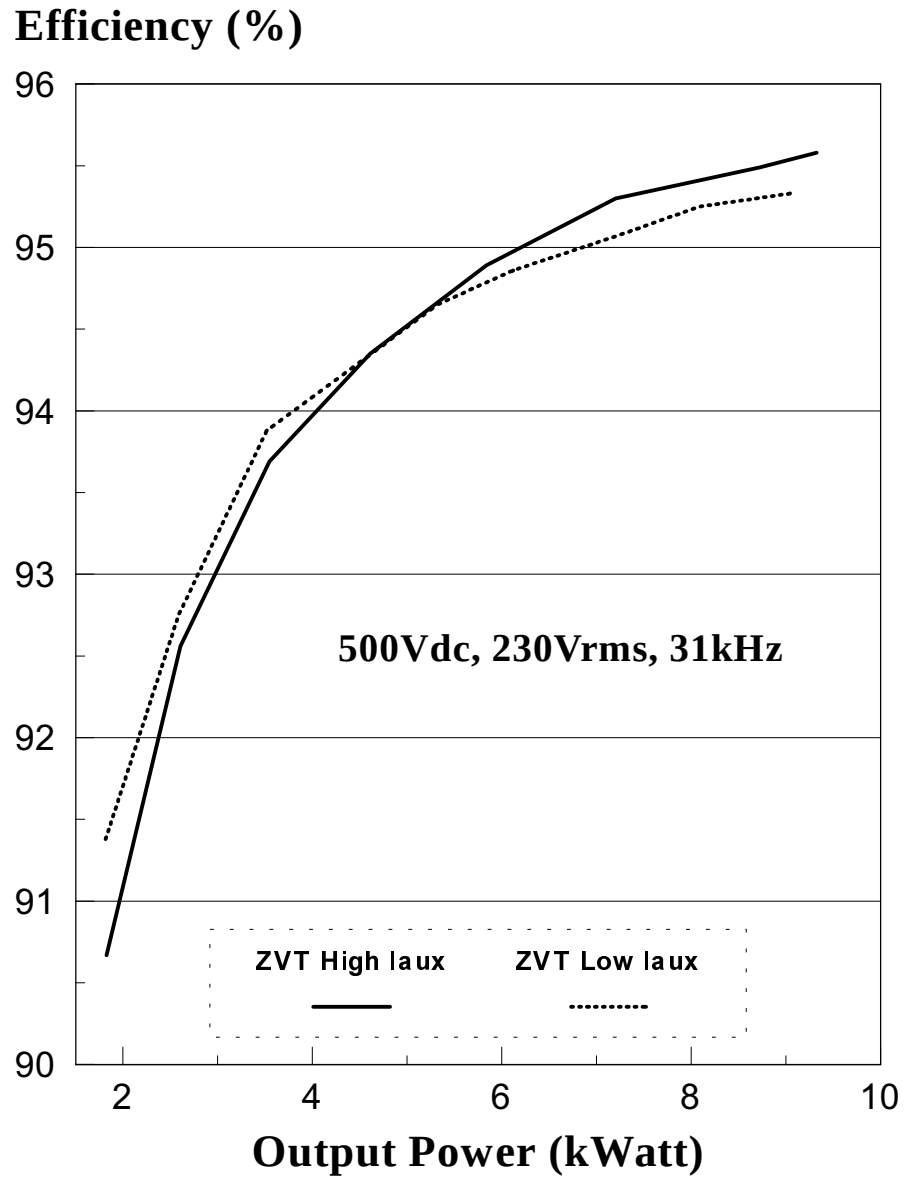


Fig. 4.15. Efficiency vs. output power in inverter mode (ZVT @ 31 kHz and two different $I_{aux\text{-}pk}$ values).

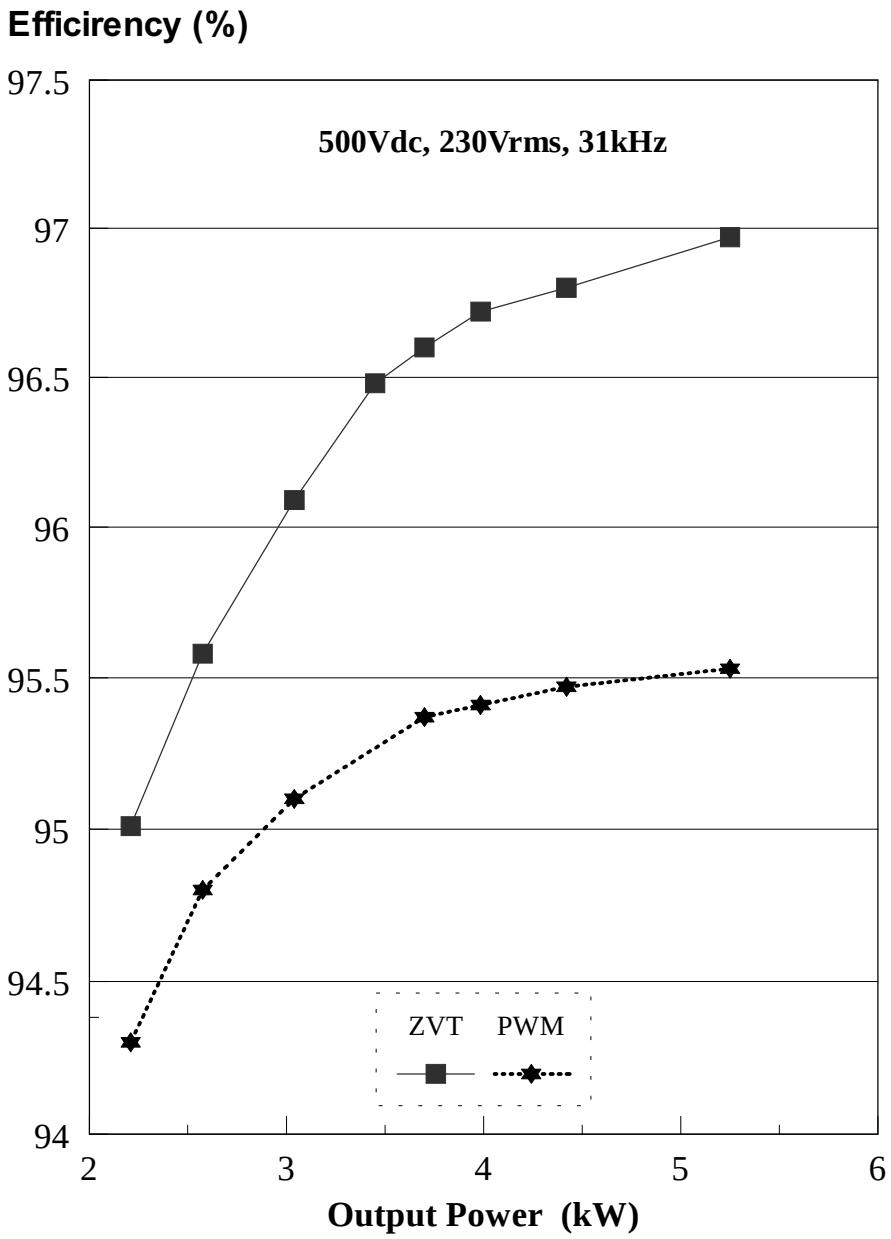


Fig. 4.16. Efficiency vs. output power in rectifier mode (ZVT and PWM @ 31kHz).

state with 3 conducting diodes corresponds to the undesired vector and lasts a minimum, and the adjacent vectors, which last longer in average, have none or just one conducting diode.

4.8. Small Signal Transfer Functions.

Bode plots for one of the small signal transfer functions needed to characterize the converters depicted in Fig. 1.1 and 1.2, in open loop, are presented in Fig.4.16, as described in [29]. For the converter in Fig. 1.1 these measurements were taken with standard SVM and alternating zero vector, which as explained above gives an effective switching frequency of half the original frequency in the ZVT converter. The converter used here has an effective switching frequency of 15.6 kHz, and operating point defined by $V_q=0$, $I_q=0$, P_o=1.6 kW, and V_{pn}=200V.

According to [29] the model depends mainly on the low frequency components of the duty-cycles. Therefore, as expected, the ZVT converter of Fig. 1.2 when operated with the modified SVM, which preserves the low frequency components of the duty-cycles, presents very similar characteristics to those shown by the hard-switched converter. So the modified space vector modulation allows the ZVT converter to be controlled in a very similar way, *i.e.* to

provide similar response, to PWM counterpart and therefore to be used in the same type of applications such as motor drives, etc. Nevertheless, the right-half plane zero, present in some of the transfer functions, and dependent on the operating point duty-cycle and main inductor values [29], remains the strongest constraint on the final bandwidth.

Based upon some small signal transfer functions a closed-loop design was carried out. However, it is important to keep in mind that the small-signal transfer functions are strongly influenced by the operating point.

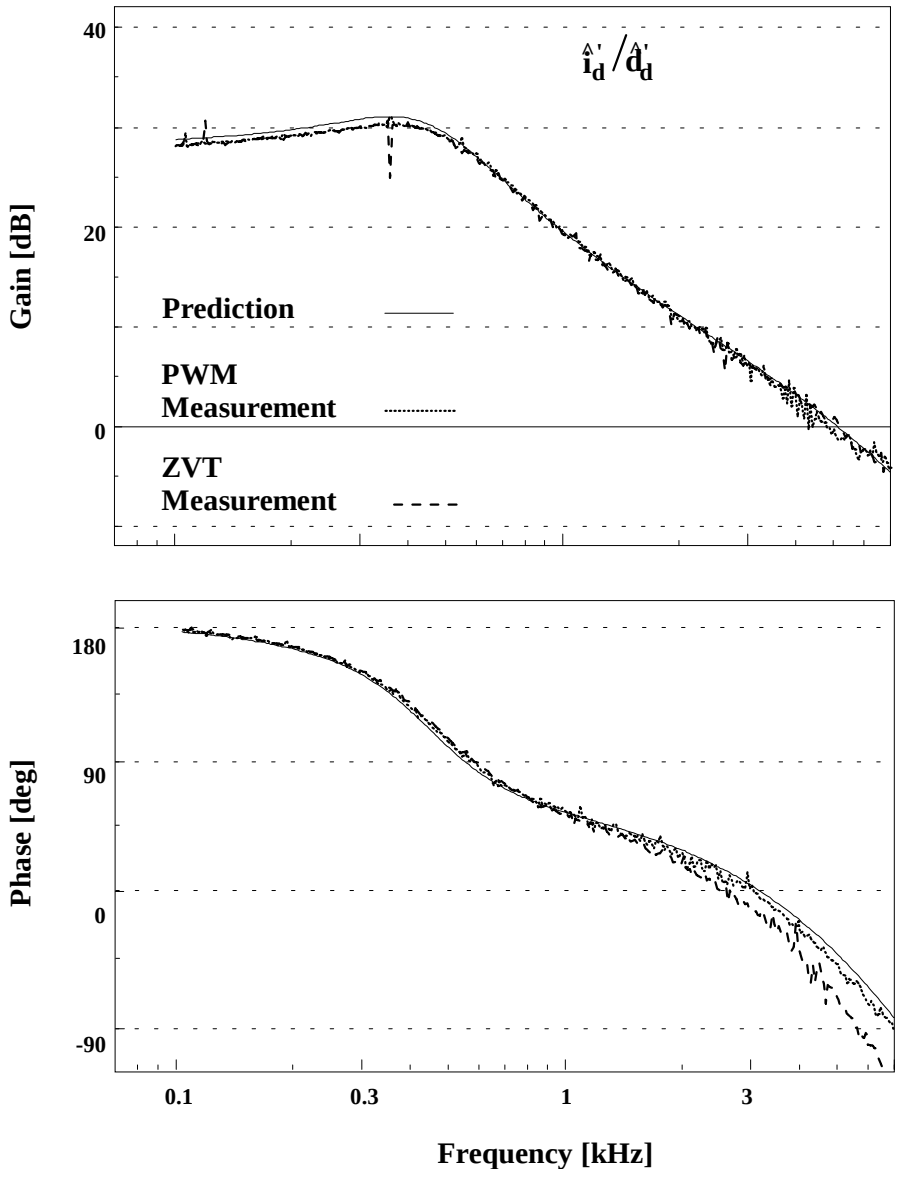


Fig. 4.17. Predicted and measured control transfer functions for boost rectifier (31.1 kHz).